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A 1.2 V, 8-bit, 100 MHz pipelined analog-to-digital converter

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A 1.2 V, 8-bit, 100 MHz Pipelined Analog-to-Digital Converter

by

Shahab Ardalan

A thesis
presented to Ryerson University
in partial fulfillment of the
requirement for the degree of
Master of Applied Science
in the Program of
Electrical & Computer Engineering

Toronto, Ontario, Canada, 2002

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A 1.2 V, 8-bit, 100 MHz Pipelined Analog-to-Digital Converter

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Abstract

A 1.2 V, 8 bit, 100 MSample/Sec Pipeline Analog-to-Digital Converter is designed in 0.18- μm standard CMOS technology. An emphasis was placed on observing the low voltage and low power design. The architecture of this ADC is 1 bit/stage pipelined configuration.

With above specifications the designed ADC can be applicable for DVI flat-panel display; Giga bit Ethernet on copper, RGB to LCD converter and cable modem.

This designed ADC can achieve SNDR 56dB in 100 MHz sampling frequency with 8 bit resolution. Total power dissipation is 40.6mW and INL is around 1 LSB and the maximum swing of the input is 1Volt peak to peak which is almost rail-to-rail situation. The core area of the ADC excluding pads is around 0.25mm².

Acknowledgement

I would like to thank my thesis supervisor, Professor Kaamran Raahemifar, for his support, guidance, advice and educative attitude throughout my study. His suggestions and observations were invaluable.

Special thanks to Professor Fei Yuan, my thesis co-supervisor, for his support, advice on design issues and his willingness of always discussing and answering questions.

Thanks to Professors Alireza Sadeghian, Gul Khan and Sridhar Krishnan for their prompt feedback and insightful comments.

I would like to express my appreciation to my brother, Kasra, for his kind help, constant guidance and encouragement. His technical assistance in Cadence CAD tools and great suggestions on analog circuit design were beneficial.

Thanks to my friends, Sotoudeh Hamed-Hagh and Amir Haji-abdolhamid for their technical advice about circuit design and layout. Their clever and bright explanations were very useful.

Thanks to my peers in SoC Research Laboratory. Thanks to Korosh Shahbazi and Amir Khatibzadeh for their remarks on thesis writing, discussion on system design and great ideas for break times.

Finally, I wish to express my extreme gratitude to my parents for their support and patience.

This thesis is dedicated to:

My mother who taught me how to calculate $2+2$,

My father who taught me how to live,

And my brother who taught me how to bias a simple amplifier.

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Chapter

Introduction

1.1 Project Overview

This integrated circuit design consists of an 8-bit, 100 MHz sampling frequency, 1.2V supply voltage analog to digital converter with a pipelined architecture. The design is based on switch capacitor circuitry. There are eight stages in this design, each consists of an Operational Trans-conductor Amplifier (OTA), comparator and one bit digital-to-analog converter.

Technology scaling will drive the supply voltage of digital circuits down to 1.2V by 2004 and 0.9 V by 2008, according to Semiconductor Industry Association's Road Map [1.1]. At the same time, the migration toward System-On-a-Chip (SoC) adds a pressure on analog circuits to follow this trend [1.2] and also for battery-powered portable applications we need suitable power dissipation. Low voltage operation is one of the important key constraints in this design. With the trend ADC interfaces are incorporated as a cell in complex mixed-signal IC's consisting mostly of digital blocks for digital

signal processing and control units, the use of the same supply-voltage for both analog and digital circuits can gain advantages in reducing the overall system cost by eliminating the need for generating multiple supply voltages [1.3].

CMOS analog-to-digital converters (ADCs), implemented in current-mode techniques, have been demonstrated to be capable of operating with supply voltages of 1.5 V and below [1.4], [1.5]. The current-mode circuits, however, seem to have limited linearity especially at higher signal frequencies. The switched capacitor (SC) technique, which inherently has a good linearity, has been widely employed in pipelined ADCs with supply voltages above 2.5 V, but the insufficient switch overdrive prevents the use of it for low-voltage applications in its standard form. Fortunately, there are at least three different approaches to overcome the switch driving problem. The first is to use small size transistors as switches. This, however, requires a special technology and may suffer from leakage of the stored charge. Locally boosting the switch-transistor gate voltage above the supply voltage with a charge-pump circuit has been used [1.6]. Long-term reliability problems, due to exceeding the technology specifications for the maximum voltage, have formerly been associated with these circuits, but recently a bootstrapped switch which does not violate the process constraints has been used to implement a 1.5-V pipelined ADC [1.7].

The third low-voltage SC technique is the switched-opamp (SO) technique. It is based on the observation that in conventional SC circuits, switches suffering from an insufficient voltage overdrive are connected to the output of an opamp; all the other switches operate around a constant voltage level that can be adjusted to be suitable for the switches. In SO circuits, the problematic switches are removed and their function is realized by

“switching off” the Opamp, i.e., allowing turning its output stage into a high-impedance state. The resultant circuits can operate at voltages less than 1 V. The SO technique was first introduced in [1.8] and further developed in [1.9] by making the circuit fully differential and separating the input and output common-mode levels. It is not obvious whether the SO technique and the switch boosting are better methods to achieve the low-voltage operation with SC circuits, since both increase circuit complexity and internal capacitive loads [1.2].

1.2 Fundamental of Data Converting

1.2.1 Nyquist-Rate Converters

A Nyquist-Rate converter generates a series of output data that have a one-to-one correspondence to the input single. Nyquist-Rate converters operate at the rate that is 1.5 to 10 times the Nyquist rate [1.10].

1.2.2 Over-sampling Converters

Over-sampling converters are defined as those converters that operate much faster than the input signal's Nyquist rate, typically 20 to 512 times faster.

1.2.3 Ideal Analog-to-Digital Converter (ADC)

The block diagram of the ideal analog-to digital converter is known in Fig1-1, where V_{in} is analog input, B_{out} is the digital output and V_{ref} is reference voltage.

Fig1-2 is the input-output characteristics of an ideal 2-bit analog-to-digital converter.

Fig1-1: Block diagram of ideal ADC

Fig1-2: Input-Output characteristics of 2-Bit ADC

The quantization step, V_{LSB} , is defined as the difference between two adjacent transition voltages.

For an n-bit analog-to-digital converter when V_{in} is greater than 0 and less than the V_{ref} , the transition voltages are ideally as follows.

$$V_{Tn} = \frac{V_{ref}}{2^N} n, \quad n = \sum_{i=1}^N 2^{i-1} \cdot b_i, \quad b_i \in \{0,1\}, \quad n > 0,$$

where 'n' and V_{ref} represent the digital output code and the applied reference voltage.

1.3 Static Parameters of ADC

1.3.1 Offset Error

Offset error, E_{offset} , is defined in (1) where V_T is the transition voltage, V'_T is the ideal transition voltage, and V_{LSB} is quantization step.

$$E_{offset} = \frac{V'_T - V_T}{V_{LSB}} \quad (1)$$

1.3.2 Integral Non-Linearity (INL)

The Integral Non-Linearity (INL) is defined as the deviation of each transition voltage of each code from the ideal transition voltage estimated from the straight line connecting the two endpoint of the conversion characteristic.

$$V'_{LSB} = \frac{V'_{T(2^n-1)} - V'_{T1}}{2^n - 1},$$

$$INL(n) = \frac{V'_{T(n)} - (n-1)V'_{LSB} - V'_{T1}}{V'_{LSB}}, \quad n \in [1, 2^N - 1],$$

where $V'_{T(n)}$ is the n -th transition voltage and N is the resolution of the ADC [2.11].

Fig1-3: $INL(3)$ and V'_{LSB} in 2-Bit ADC

1.4 Dynamic Parameters of ADC

1.4.1 Signal-to-Noise Ratio (SNR)

The ratio of the signal power to the noise power at the output in the hold mode is the signal-to-noise ratio (SNR). Theoretically the maximum of the signal-to-noise ratio for an n -bit resolution analog-to-digital converter is given by (2).

$$SNR_{Max} = 6.02n + 1.76 \quad (dB) \quad (2)$$

1.4.2 Signal-to-Noise plus Distortion Ratio (SNDR)

The ratio of the signal power to the total noise and harmonic power at the output in the hold mode is Signal-to-Noise plus Distortion Ratio (SNDR).

1.4.3 Effective Number of Bits (ENOB)

The Effective Number of Bits (ENOB) is defined in (3) where $SNDR_{dB}(f_{in})$ is the signal-to-noise plus distortion ratio at the input frequency of the f_{in} in decibels.

The ENOB is one of the dynamic parameters of analog-to-digital converters that measures the performance of the ADCs, since it also comprises information about the Effective Resolution Bandwidth (ERB) [1.11].

$$ENOB(f_{in}) = \frac{SNDR_{dB}(f_{in}) - 1.76}{6.02} \quad (bits) \quad (3)$$

1.5 References

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Chapter

Analog-to-Digital Converter Applications and Architectures

2.1 Applications

2.1.1 RGB-to-LCD Converter

Cathode Ray Tube (CRT) displays typically incorporate three 8-bit RAM-DACs to display the analog RGB images on a CRT monitors. But in the flat-panel LCD displays, it is necessary to convert the analog RGB signals to the digital format which is required for LCD displays [2.1].

Fig. 2-1 shows RGB to LCD converter system using three analog-to-digital converters in parallel configuration. Power dissipation is a critical issue for this application. Low voltage design is another important aspect for battery used devices.

Fig2-1: The Block diagram of RGB-to-LCD converter system

2.1.2 Gigabit Ethernet

Fig. 2-2 shows the block diagram of the analog interface of a gigabit copper system. Similar to previous application, this system requires more than one analog-to-digital converter. The ADCs must reach perfect dynamic range so as to contain a large echo and signal level alteration by reason of the shrinking through the cable. Power dissipation and supply voltage are important issues in this application.

Fig2-2: Block diagram of Gigabit Ethernet on copper

2.1.3 Cable Modem

The ADCs also can be a part of the receiver of cable modem which is shown in Fig. 2-3.

The receiver consists of an RF tuner, an analog-to-digital converter and a demodulator.

The RF tuner takes analog RF signal as an analog input from coaxial cable and data is sampled and converted to digital form by ADC block then demodulator extracts data from the modulated signal and passes it through the Media Access Control Block (MAC).

And also transmitter consists of an modulator and digital-to-analog converter and power amplifier.

Fig2-3: Block diagram of cable modem receiver

2.2 Analog-to-Digital Converter Architectures

2.2.1 Flash Architecture

The block diagram of an N-bit flash analog-to-digital is shown in Fig2-4. The analog input signal is simultaneously compared with the threshold voltages of the ADC by an array of 2^N comparators, thereby producing a thermometer code. The result is subsequently converted into a binary output by an encoder. The threshold voltages are usually generated by a ladder consisting of a series of matched resistors [2.1].

Fig 2-4: Flash-ADC Block Diagram

The principal advantage of the flash architecture is its high throughput rate. The conversion of each sample takes only one clock period. However, many issues limit the efficacy of this approach for resolutions above 6 bits. The exponential growth of the input capacitance, power dissipation, and area are important drawbacks. Furthermore, the fixed reference voltage [2.1], the offset of the comparators, the feed through of the analog input to the resistor hierarchy [2.2], the slew-dependent comparator delay [2.3] [2.4] and the problem of bubbles in the thermometer code [2.2] [2.3] degrade the static and dynamic performance of the flash ADCs.

2.2.2 Two-Step Architecture

The required large number of low offset comparators is the major problem in flash converters. In order to avoid the exponential expansion encountered in flash ADCs the two-step architecture is used.

Fig2-5 shows a block diagram of a two-step flash Analog-to-Digital converter which reduces the comparator count down to $2^{\frac{n}{2}+1}$. Similar to flash converters, the analog input is first sampled by a S/H circuit; During the hold period, the first flash ADC performs a coarse quantization on the held signal. The held signal is then subtracted from the output of DAC; The residue of the subtraction is then passed down for fine quantization to the full resolution of the converter. Although this architecture requires a low offset comparator with the full resolution of the converter, the number of low offset comparator required is reduced significantly. With $2^{\frac{n}{2}}$ coarse comparators required in the first half of the converter, the total number of comparators is also reduced. By using concurrent

processing, the throughput of this architecture can sustain the same rate as a flash ADC. However, the converted outputs have a latency of two clock cycles due to the extra stage to reduce the number of precision comparators [2.5].

Fig. 2-5: Two-Stage ADC Block Diagram

For example the mapping scheme of a 4-bit two-stage analog-to-digital converter is shown in Fig 2-6. In the two-step topology, the input range is first divided into four equal segments, and a coarse quantizer is used to determine in which segment the analog input lies, thus producing the most significant bit (MSB). Next, each segment is divided into four segments, and a fine quantizer detects the least significant bit (LSB). The advantage of this architecture is the low number of precision comparators, lowering power consumption. The throughput is the same as flash ASCs because of the concurrent

processing of signals. An extra clock cycle, however, is required to complete the conversion.

Fig 2-6: An example of 4-bit Two-Stage ADC

If the system can tolerate the latency of converted signal, two-step flash is a solution with advantages on power and area. The disadvantage is that the both subtraction and precision comparators still need to meet the full resolution of the ADC. As mentioned earlier, it is very difficult to achieve resolution above 8-bit in CMOS without using special techniques to compensate for the offset. Subtraction accuracy can be relaxed by using a wider range of precision comparators in the second stage, i.e. the digital correction stage. Inter-stage gain can be used here to tolerate a large comparator offset for the second stage precision comparators [2.1].

2.2.3 Pipelined Architecture

In the 2-step flash converter, an inter-stage gain amplifier can be used to relax the comparator offset in the second stage. In the same way, if we amplify the subtracted residue signal from the first stage to the full scale, the offset requirement for the 2nd-stage comparators can be relaxed. Fig 2.3 shows a 2-step flash converter with an inter-stage gain. However, the inter-stage gain needs to be carefully designed according to the first stage resolution and the overall ADC resolution.

For example, a 10-bit 2-step flash A/D converter utilizes a switched capacitor inter-stage amplifier. The amplifier is required to settle to 10 bit resolution in roughly half the clock period with the gain of $2^5 = 32$. At high frequency circuit achieving this requirement in switched capacitor (SC) circuit is very difficult and may take a lot of power consumption, mainly due to the small feedback factor [2.5].

Fig 2-7: Pipelined ADC block diagram

Fig. 2-8: Block Diagram of the M^{th} - stage

In order to further reduce the power consumption, one can reduce the per-stage resolution and cascade more stages to get the full resolution. This particular architecture is called the pipelined architecture, mainly because the analog input signal is passed through a pipeline of flash ADC (sub-ADC) and inter-stage gain blocks. Fig. 2-8 shows a conventional pipelined block diagram [2.5].

Same as previous architecture cases, the analog input signal is sampled by a sample and hold circuit. The sampled input signal is then converted to the resolution of the stage, 2 bits; and is subtracted from the DAC output of the present stage digital output. The residue is then amplified by a factor of 2 and passed down to the next stage. The advantage of this architecture is its reduced complexity. With a given per-stage resolution, an analog-to-digital converter of a given resolution can be achieved by cascading an appropriate number of identical pipelined stages. Therefore, the hardware

cost is a linear function of the resolution, given that all the requirements are met. Some capacitor trimming techniques may be required to correct for SC circuit gain and non-ideal subtraction (capacitor mismatch). With concurrent processing (interleaving between stages), the throughput achieved is the same as the flash case, a set of output bits per clock cycle. The primary drawback of the conventional pipelined topology is the need for high precision in the inter-stage SHAs, DACs, and subtractors, especially at the front end. The precision typically mandates the use of op amps, imposing severe trade-offs on speed, voltage swing, gain, and power dissipation. As device dimensions, supply voltages, and the intrinsic gain ($gmro$) of MOSFETs continue to scale down, the design of op amps becomes increasingly difficult. Another disadvantage of this architecture is the latency of the converter. Generally, if concurrent/interleaving processing is used, the delay through the converter is roughly $\frac{N}{2}$ clock cycles, where N is the number of output bits. The conventional pipelined architecture has the most flexibility and the least number of precision components required to have an accurate converter to the full resolution of the converter [2.5].

Fig. 2-9: Ideal transfer function of a 2-bit pipelined stage

(a)

(b)

Time offset: 0

Time offset: 0

Fig. 2-10: (a) - Input of the first stage, (b) - Output of first stage

(a)

(b)

Time offset: 0

Time offset: 0

Fig. 2-11: (a) - Output of the third stage, (b) - Output of fourth stage

2.2.4 Interleaved Pipelined Architecture

In the pipelined topology, the conversion rate is limited by the settling time and accuracy requirements of the inter-stage operations. Interleaving can be used to further improve the throughput rate. The basic principle behind interleaving is illustrated in Fig 2-12. The architecture employs M identical sub-ADCs, each incorporating a sample-and-hold-amplifier (SHA) that tracks for T_1 seconds and holds for $(M-1)T_1$ seconds, as shown in Fig 2-13. Each sub-ADC is allotted $(M-1)T_1$ seconds for one conversion.

The use of multiple parallel channels, however, introduces serious difficulties due to device mismatches. Tones at f_{Clock}/M and fixed-pattern noise are generally caused by offset mismatches. Sideband modulation around f_{Clock}/M is caused by gain mismatches [2.1].

Fig. 2- 12: Block diagram of an interleaved ADC

Fig. 2-13: Wave form of the clocks in interleaved ADC

2.2.5 Interpolating Architecture

As mentioned in Section 2.2.1, one of the critical disadvantages of the flash topology is the large input capacitance. This problem can be alleviated by applying interpolation as shown in Fig. 2-14. The idea is that if V_{in} crosses $(V_{R1} + V_{R2})/2$, then V_{O2} crosses zero, increasing the resolution by a factor of two. In essence, interpolation adds zero crossings to the set of input/output characteristics of a flash stage [2.1].

Interpolation lends itself to implementation in submicron technologies because the amplifiers used in Fig14 dose not need to have an accurate gain, high linearity, or large output swings. Also, it can reduce the differential nonlinearity (DNL) resulting from the offset of the preamplifiers [2.6]. However, the simple scheme shown in Fig. 2-14 still

suffers from high power consumption and substantial hardware requirement because of the 2^x growth in each interpolation step. Furthermore, the offset voltages of the amplifiers lead to uncorrected integral nonlinearity (INL) [2.1].

Fig 2-14: A 2^X active interpolating ADC

2.3 An Overview of Published Pipelined ADC

Table 2-1 shows an overview of published pipelined analog-to-digital converters [2.39].

<i>First Author, Ref.</i>	<i>Year</i>	<i>Sampling Frequenc (MS/s)</i>	<i>Res.</i>	<i>Technology</i>	<i>Power Supply (V)</i>	<i>Power Dissip. (mW)</i>	<i>Die Area (mm²)</i>
Lewis, [2.7]	1987	5	9/8	3 μm CMOS	10	180	22.6
Sutarja, [2.8]	1988	0.25	13	3 μm CMOS	5	15	2.3
Song, [2.9]	1988	1	12	1.75 μm CMOS	5	400	14
Lin, [2.10]	1991	2.5	13	3 μm CMOS	5	100	26
Lewis, [2.11]	1992	20	10	0.9 μm CMOS	5	240	8.7
Coleran, [2.12]	1993	100	10	12GHz Bipolar	5	800	19.3
Yotsuyanagi, [2.13]	1993	50	10	0.8 μm CMOS	5	900	18
Conroy, [2.14]	1993	85	8	1 μm CMOS	5	1100	2.5
Kusumoto, [2.15]	1993	20	10	0.8 μm CMOS	5	30	6.5
Cho, [2.16]	1995	20	10	1.2 μm CMOS	5	35	10.5
Song, [2.17]	1995	20	10	1.2 μm CMOS	5	50	13
Nakamura, [2.18]	1995	40	10	0.8 μm CMOS	5	85	4
Shu, [2.19]	1995	10	13	1.4 μm BiCMOS	5	360	33.4
Cline, [2.20]	1996	5	13	1.2 μm CMOS	5	166	49
Opris, [2.21]	1998	20	12	0.7 μm CMOS	5	250	9.92
Fu, [2.22]	1998	40	10	1 μm CMOS	5	565	42
Dyer, [2.23]	1998	40	10	1 μm CMOS	5	650	47

<i>First Author, Ref.</i>	<i>Year</i>	<i>Sampling Frequenc (MS/s)</i>	<i>Res.</i>	<i>Technology</i>	<i>Power Supply (V)</i>	<i>Power Dissip. (mW)</i>	<i>Die Area (mm²)</i>
Nagaraj, [2.25]	1999	75	6	0.5 μm CMOS	3.3	110	1
Erdogan, [2.26]	1999	0.125	12	1.5 μm CMOS	5	16	5.9
Ploeg, [2.27]	1999	25	10	0.35 μm CMOS	3.3	195	0.66
Paul, [2.28]	1999	18	13	1.2 μm CMOS	3.3	324	48
Opris [2.29]	2000	5	14	0.5 μm CMOS	5	320	10.9
Wang [2.30]	2000	150	8	0.6 μm CMOS	3.3	395	1.8
Mehr[2.31]	2000	40	10	0.35 μm CMOS	3	55	2.6
Choe[2.32]	2000	40	13	0.5 μm CMOS	5	800	8.7
Moreland[2.33]	2000	100	10	0.8m DI/SOI Bi.	5	1250	28
Waltari, [2.34]	2001	14	9	0.5 μm CMOS	1	1.6	1.3
Thompson, [2.35]	2001	15	20	0.5 μm CMOS	4.5	380	13.7
Chen, [2.36]	2001	14	20	0.5 μm CMOS	5	720	10.8
Sumanen, [2.37]	2001	10	200	0.5 μm CMOS	3	280	7.4
Ming, [2.38]	2001	8	80	0.5 μm CMOS	3	268	10.3

Table 2-1: Overview of the published pipeline ADCs

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Chapter

Circuit Design Techniques

In this chapter, the design of building blocks of the analog-to-digital converter is presented.

3.1 Boot-Strap Circuit

Switching delay is suffered by using low-supply voltage and this effect degrades circuit performance. One approach for solving the switching delay due to lower supply voltage is to use boot-strapped clock to gain better performance in high-speed low-voltage design. Fig.3-1 shows responses of the CMOS inverter in $0.18\mu\text{m}$ technology to the high-to-low clock transition to different inputs. The dashed line is the output to the boot-strapped clock (0 and 2.4V) and the solid line is the output to the normal clock (0 and 1.2V). Fig.3-2 shows that the delay in case 1 is less than the delay in case 2 (which belongs to normal clock).

Fig.3-3 shows the schematic of the bootstrap circuit and its response is shown in Fig 3-4.

Fig.3-1: Block diagram of inverter

Fig.3-2: Response of inverter to boot-strapped input and normal input

Fig.3-3: Schematic of bootstrap circuit

Fig.: 3-4: Input and Output wave forms of the bootstrap circuit

The circuit in Fig.3-3 consists of two capacitors for doubling the DC level and a dynamic charge pump circuit. When the input clock is high, the capacitors are charged to V_{DD} through the charge pump. When the input clock is low, the voltage of C_2 increases, in this case M_4 is “off”, M_3 is “on” and a boosted clock voltage is generated [3.1].

The size of the transistor and the value of the capacitors used in this circuit are shown in Table 3-1.

Transistor	M1	M2	M3	M4
Width	$5\mu m$	$5\mu m$	$0.5\mu m$	$0.5\mu m$
Length	$0.18\mu m$	$0.18\mu m$	$0.18\mu m$	$0.18\mu m$
Capacitor	C1		C2	
Capacitance	250fF		250fF	

Table: 3-1: Transistors' size and capacitors' value used in bootstrap circuit

Fig.: 3-5: Transistors' size and capacitors' value used in bootstrap circuit

3.2 Track and Hold Circuit

Fig.3-6 shows a simple track-and-hold circuit. In the sampling mode, switch S is “ON” and the output voltage, V_{OUT} , tracks the input voltage, V_{IN} .

Fig.: 3-6: Schematic of the simple track-and-hold

The boot-strapped clock, as shown in Fig.3-1, is used to reduce the delay during switching. The track-and-hold circuit is used as the first stage in the analog-to-digital converter to provide distortion-less input signal whose variation is less than $\frac{1}{2}$ LSB [3.2].

Fig.3-7 shows the schematic of the track-and-hold circuit.

M_1, M_2, C_1 and C_2 form a charge pump which helps the voltage doublers. When CK_{IN} is low, the M_9 and M_{11} are “on”, discharging the gate of M_1 to ground.

At this time the C_3 charges to V_{DD} through M_5 and M_6 . When CK_{IN} is high, M_5 , M_6 and M_{11} are “off”, M_7 and M_{10} are “on”, and the gate voltage of the switch is almost one V_{DD} more than source voltage.

M_9 and M_{10} limit the voltage drop across the terminals of M_{11} and M_7 [3.1].

The size of the transistors and the value of the capacitor are provided in Table 3-2.

Fig.3-7 shows the layout of this block.

Fig.: 3-7: Schematic of the track-and-hold circuit

The sizes of the transistors and the value of the capacitances are shown in Table 3-2.

<i>Transistor</i>	<i>M1</i>	<i>M2</i>	<i>M3</i>	<i>M4</i>
<i>Width</i>	$0.6\mu\text{m}$	$0.6\mu\text{m}$	$1.5\mu\text{m}$	$0.6\mu\text{m}$
<i>Length</i>	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$
<i>Transistor</i>	<i>M5</i>	<i>M6</i>	<i>M7</i>	<i>M8</i>
<i>Width</i>	$2\mu\text{m}$	$0.6\mu\text{m}$	$1\mu\text{m}$	$0.6\mu\text{m}$
<i>Length</i>	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$
<i>Transistor</i>	<i>M9</i>	<i>M10</i>	<i>M11</i>	<i>M12</i>
<i>Width</i>	$0.6\mu\text{m}$	$12\mu\text{m}$	$2\mu\text{m}$	$1.5\mu\text{m}$
<i>Length</i>	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$
<i>Capacitor</i>	<i>C1</i>	<i>C2</i>	<i>C3</i>	<i>C4</i>
<i>Capacitance</i>	250 fF	250 fF	500 fF	1 pF

Table: 3-2: Transistors' size and capacitors' value used in T&H circuit

Fig.3-9: Layout of the track-and-hold circuit

Fig.3-10 shows simulation the results of this block with a 100MHz sampling clock and a 1.2V power supply.

Fig.3-10: Input and Output waveforms of track and hold circuit

3.3 Operational Amplifier

A two-stage configuration (Fig.3-11) for operational amplifier is used in this design. This configuration offers an important feature that can be exploited if maximum dynamic range is the primary concern; the G_m stage provides a high gain, while the amplifier A1 is designed for nearly rail-to-rail output swings.

Fig.3-11: Two-Stage Operational Amplifier configuration

Another advantage of the two-stage configuration is its high stability in switching capacitor circuits because of employing the Miller compensation capacitor (C_C).

Fig.3-12 shows the schematic of the two-stage operational amplifier used in this analog-to-digital converter.

Transistors, M_1 , M_2 , M_3 , M_4 and M_5 form current mirrors to fix biasing current generated by the biasing circuitry.

M_7 and M_8 are main transistors of the first stage (Gm Stage) of this amplifier in differential pair; M_9 and M_{10} are loads for this amplifier. The larger length of M_9 and M_{10} , the higher gain will be. The second stage consists of two transistors (M_{12} and M_{13}) in a common source configuration to increase the output levels and keep the swings as close as possible to the rail voltages.

Fig.3-12: Schematic of the two-stage Operational Amplifier

One of the challenges of designing a two-stage operational amplifier is to design the compensator circuit used to keep the output in a stable region by manipulating the phase-

margin. M_{11} and C_c are playing this role [3.3]. M_{11} must be in the triode region to act as a resistor. M_{11} together with the compensating capacitor (C_c) tend to ease the stability of this configuration.

The value of the used Miller Capacitor (compensating capacitor) is 1 pF. Table 3-3 tabulates the sizes of the transistors used in this circuit.

<i>Transistor</i>	<i>M1</i>	<i>M2</i>	<i>M3</i>	<i>M4</i>
<i>Width</i>	$1\mu m$	$1\mu m$	$1\mu m$	$10\mu m$
<i>Length</i>	$0.6\mu m$	$1.2\mu m$	$0.5\mu m$	$0.5\mu m$
<i>Transistor</i>	<i>M5</i>	<i>M6</i>	<i>M7</i>	<i>M8</i>
<i>Width</i>	$10\mu m$	$30\mu m$	$20\mu m$	$20\mu m$
<i>Length</i>	$0.9\mu m$	$0.5\mu m$	$0.18\mu m$	$0.18\mu m$
<i>Transistor</i>	<i>M9</i>	<i>M10</i>	<i>M12</i>	<i>M13</i>
<i>Width</i>	$50\mu m$	$50\mu m$	$20\mu m$	$38.5\mu m$
<i>Length</i>	$1\mu m$	$1\mu m$	$1\mu m$	$0.18\mu m$

Table: 3-2: Transistors' size and capacitors' value used in T&H circuit

Fig.3-13 shows the frequency response of the operational amplifier in $0.18\mu m$ CMOS technology. Fig.3-14 shows the phase response of the amplifier.

The layout of this block is shown in Fig.3-15. The characteristics' simulated of this operational amplifier are shown in Table 3-3.

Fig.3-13: Magnitude of the frequency response of operational amplifier

Fig.3-12: Phase of the frequency response of the operational amplifier

Fig.3-13: Layout of the operational amplifier

Table 3-4 shows the characteristics of the operational amplifier block found from simulation result in 0.18 μ m CMOS technology.

Unity gain frequency	410 MHz
DC gain	81 dB
Phase Margin	75°
Power Dissipation	2mW
Power Supply	1.2V
Maximum Input Signal Swing	1 V
Total Load Capacitor	700 fF
Input Referred Noise	16 pV

Table: 3-4: Operational Amplifier Characteristics

3.4 Residue Amplifier

The inter-stage sampling, subtracting and amplifying-by-two circuit is shown in Fig.3-14.

This switching-capacitor circuit uses operational amplifier and its switching-capacitor feed back to generate residue output for next the stage.

Fig.3-14: Schematic of the reduces amplifier

The internal circuitry of the switch is shown in Fig.3-15. As shown, an N-MOS and a P-MOS transistor are used in parallel configuration to reduce the internal resistance of the switch [3.4].

Fig.3-15: Schematic of the switch

The switch used for this research is shown in Fig.3-15. Building the switch using complementary clocks is not a drawback for this circuit since complementary clocks are used in other sections and blocks of our design.

Fig.3-16 shows the internal resistance of different kind of switches in 1.2 μ CMOS

technology when $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = \frac{1.8\mu m}{1.2\mu m}$.

Fig.3-16: Comparing of the internal resistor of the different switches

When CK_2 is high and CK_1 is low; SW1, SW3, SW4, SW5, and SW7 are closed and SW2 and SW6 are open (sampling phase), C_1 , C_2 are connected to the V_{in} , sampling it. In the next phase (Amplifying Phase), SW2 and SW6 are closed and other switches are open. The feedback switch is closed and V_D is connected to C_2 .

We have

$$V_{out} = \left(\frac{C_1 + C_2}{C_1} \right) \times V_{in} - \left(\frac{C_2}{C_1} \right) \times V_D$$

If $C_1 = C_2$ then we have $V_{out} = 2V_{in} - V_D$

Fig.3-17: The Layout of the Residue Amplifier Block

3.5 One-bit Digital-to-Analog Converter

A one-bit digital-to-analog, shown in Fig.3-18, converts one bit digital input to analog output. One of the two DC values is selected by the digital single-bit input of the switch.

Fig.3-18: Block diagrams of one bit digital-to-analog converter

The schematic of this block is shown in Fig.3-19. The minimum size transistors are selected to reduce the switching non-idealities.

Fig.3-19: Schematic of the 1-bit digital-to-analog converter

The layout of this block is shown in Fig.3-20.

Fig.3-20: The layout of the 1-bit DAC block converter

3.6 Comparator

The performance of analog-to-digital converters that employ parallelism to achieve a high speed strongly depends on that of their comparators.

A logic output of “Low” or “High” is produced using the comparator depending on the polarity of a given input [3.2].

Fig.3-21 shows characteristic of the ideal and non-ideal comparators.

Fig.3-21: Block diagram and Characteristic of the ideal and real comparators

The comparator used in this design consists of a preamplifier followed by a latch and output buffer as shown in Fig.3-22.

Fig.3-22: Typical comparator block diagram

This architecture is very fast and has low power dissipation. The aspect ratio of the buffer inverter determines the output response delay of the comparator, which is as low as several hundred pico seconds [3.5].

The schematic of the comparator block is shown in Fig.3-23.

Fig.3-23: Schematic of the pre-amplifier

Fig.3-24: Wave form of the simulation

Fig.3-24 shows simulation result of the comparator block when V_{in-} is a DC voltage equal to half of the supply voltage (600mV) and V_{in+} is square wave with levels of 600.1mV and 599.9mV and frequency of the clock is 100MHz. This simulation is done in 0.18 μ m CMOS standard technology with 1.2 V supply voltage. The transistor sizes are listed in Table 3-5. The characteristic of this comparator is shown in Table 3-6. Layout of this block which is drawn for fabrication and post layout simulation is also shown in Fig.3-25.

Transistor	M1	M2	M3	M4
<i>Width</i>	$7\mu\text{m}$	$18.8\mu\text{m}$	$18.8\mu\text{m}$	$10\mu\text{m}$
<i>Length</i>	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.4\mu\text{m}$
Transistor	M5	M6	M7	M8
<i>Width</i>	$10\mu\text{m}$	$1\mu\text{m}$	$2\mu\text{m}$	$0.5\mu\text{m}$
<i>Length</i>	$0.4\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$
Transistor	M9	M10	M11	M12
<i>Width</i>	$0.5\mu\text{m}$	$2\mu\text{m}$	$2\mu\text{m}$	$2\mu\text{m}$
<i>Length</i>	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$
Transistor	M13	M14	M15	M16
<i>Width</i>	$0.5\mu\text{m}$	$2\mu\text{m}$	$0.5\mu\text{m}$	$2\mu\text{m}$
<i>Length</i>	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$
Transistor	M17	M18	M19	M20
<i>Width</i>	$1.25\mu\text{m}$	$0.5\mu\text{m}$	$1.25\mu\text{m}$	$0.5\mu\text{m}$
<i>Length</i>	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$

Table: 3-5: Transistors' size of the comparator circuit

Fig.3-25: The layout of the fully differentiate comparator

Resolution	100 μ V
DC Gain of Pre-Amplifier	31 dB
Clock Frequency	100MHz
Power Dissipation	81 μ W
Power Supply	1.2V
Output levels (Low and High)	0 and 1.2V
Output and Input	Fully Differentiate

Table 3-6: Comparator's characteristic

3.7 Bias Circuit

The comparator block and operational amplifier block need proper bias voltages to operate as expected. The trans-conductance of MOSFETs plays a critical role in analog circuits in determining such performance parameter as noise, small-signal gain and speed. Consequently, it is often required to bias the transistors such that their trans-conductance does not depend on the temperature, process or supply voltage.

In variety of different types of the biasing circuit a “Wide-Swing Current Mirror with Enhanced Output Impedance” is selected for this mixed-mode integrated circuit.

Because of small number of stacking transistors, this design is good choice for low-voltage low-power design [3.3].

Fig.3-26: The schematic of the biasing circuit

<i>Transistor</i>	<i>M1</i>	<i>M2</i>	<i>M3</i>	<i>M4</i>
<i>Width</i>	$7\mu m$	$18.8\mu m$	$18.8\mu m$	$10\mu m$
<i>Length</i>	$0.18\mu m$	$0.18\mu m$	$0.18\mu m$	$0.4\mu m$
<i>Transistor</i>	<i>M5</i>	<i>M6</i>	<i>M7</i>	<i>M8</i>
<i>Width</i>	$10\mu m$	$1\mu m$	$2\mu m$	$0.5\mu m$
<i>Length</i>	$0.4\mu m$	$0.18\mu m$	$0.18\mu m$	$0.18\mu m$
<i>Transistor</i>	<i>M9</i>	<i>M10</i>	<i>M11</i>	<i>M12</i>
<i>Width</i>	$0.5\mu m$	$2\mu m$	$2\mu m$	$2\mu m$
<i>Length</i>	$0.18\mu m$	$0.18\mu m$	$0.18\mu m$	$0.18\mu m$

Table: 3-7: Transistors' size of the bias circuit

Fig.: 3-27: Sensitivity of output current to the temperature

Fig.3-27: The layout of the biasing circuit

Transistor sizes are listed in Table 3-6. Fig.3-26 shows that variation of the output current is 0.42% with different temperature from 10°C to 100°C, when the load is 10K Ω , pure resistive. Furthermore DC analysis shows 100 μ A/V as the sensitivity of the circuit to variation of supply voltage. Power dissipation of this circuit is approximately 1mW at 10K Ω load and 118 μ A output current.

3.8 MDAC (Multiplying Digital-to-Analog Converter)

Combination of the three blocks (comparator, residue amplifier and 1-bit digital-to-analog converter) is called multiplying digital-to-analog converter or MDAC.

This block, shown in Fig.3-28, is the inter-stage in the pipelined analog-to-digital converter.

Fig.3-28: Block diagram of the MDAC

V_{Low} in this design is set to 100mV and V_{High} is 1.1V and V_{ref} is equal to half of the supply voltage (600mV). The analog outputs of the MDAC in the first stage are shown in Fig.3-29 and 3-30.

Fig.3-31 shows layout of this block in 0.18 μ m CMOS technology.

Fig.3-29: Analog input and analog output of the MDAC Block

Fig.3-30: Analog input and digital output of the MDAC Block

Fig.3-31: The layout of the MDAC block

3.9 Synchronizer

Due to the delay of each stage in pipelined architecture we need a synchronizer circuit is used to align and order the digital outputs by using a matrix of D flip flop as shown in Fig.3-32.

Fig.3-32: The block diagram of the synchronizer

Complementary clock signals in odd and even stages are used to trigger these flip-flops. The schematic of the D-flip-flop circuit used in this block, shown in Fig.3-33, has a dynamic positive edge trigger architecture which is very fast and low power, see [3.6]. Transistor with minimum size are used in this design.

Fig.3-33a: The schematic of the D-flip-flop

Fig.3-33b: The layout of the D-flip-flop

Fig.3-34: The layout of the synchronizer

3.10 Pipelined Analog-to-Digital Converter

This 8-bit analog-to-digital converter is designed at 100MHz sampling frequency with 1.2V supply voltage. The design consists of one sample and track block, seven MDAC blocks, one comparator to generate MSB, and one synchronizer to align digital outputs, as shown in Fig.3.35.

Fig.3-35: Block diagram of the Pipelined ADC

Fig.3-36: Digital and Analog output of the first MDAC

Fig.3-37: Digital and Analog output of the second MDAC

Fig.3-38: Digital and Analog output of the third MDAC

Fig.3-39: Digital and Analog output of the fourth MDAC

Fig.3-40: Output of the Synchronizer (D0 to D3)

Fig.3-41: Output of the Synchronizer (D4 to D7)

The layout of the chip is shown in Fig.3.42.

Fig.3.42: Layout of the Pipelined ADC

Table 3.8 tabulates characteristics of the designed analog-to-digital converter.

Architecture	Pipelined
Bit per stage	1 bit
Resolution	8-bit
Sampling Frequency	100 MHz
Supply Voltage	1.2 V
Input Swing Range	1 V
Power Dissipation	41mW
INL	around 1
Technology	0.18 μ m CMOS
Capacitance	MIM Cap.
Area (excluding pads)	0.25 mm ²

Table 3-8: Characteristic of the ADC

3.11 References

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Chapter

4

Layout Considerations

The layout of the analog-to-digital converter must deal with issues related to routing of critical path, switching noise reduction, and matching between capacitors and input transistors which affect the accuracy of the stages in this design. Simultaneous switching noise is another critical unwanted effect in system-on-chip design which should be solved at the layout level.

4.1 Transistor Layout

Transistors are laid out in multiple-gate fingers, Fig. 4-1, since they are typically much wider in analog circuit than their counterpart in digital circuit.

Fig. 4-1: Layout of the Pipelined ADC

4.2 Differential Pair Transistor Layout

When accurate matching among transistors is required, not only individual transistors are built by combinational transistor, but the fingers of the one transistor also contribute to the fingers of the other transistors.

This technique, common-centroid layout, helps match errors caused by gradient effects across a micro circuit, such as the temperature or gate-oxide thickness change across the microcircuit [4.1]. Fig. 4.2 shows a differential pair transistor which is laid out with common-centroid layout. This technique is very useful for differential input pair and also current mirror.

Fig 4.2: Layout of the Differential pair

4.3 Simultaneous Switching Noise

Simultaneous switching noise (SSN), also referred to as ΔI noise or ground/power bounce, is caused by the large instantaneous current, due to the switching of multiple drivers and switches, through the parasitic inductance at the ground (or power) node. SSN causes serious system degradation. It generates glitches on the ground and power-supply wires, decreases the effective driving strength of the circuits, causes output signal distortion, and reduces the overall noise margin of a system.

The effect of SSN is getting more attention as a result of the continuous increase in integration level on a single chip and the operating speed in mixed mode circuits [4.2].

Fig. 4.3: Unique pad for digital and analog blocks

To steer clear of simultaneous switching noise one can separate digital supply pads from analog supply by using multiple pads and pins for power supply and the ground [4.3].

Fig. 4.4 shows a chip with just one pad as a power connection and one pad for ground which carry lots of simultaneous switching noise.

Fig. 4.4: Unique pad for digital and analog blocks

4.4 Metal-Insulator-Metal Capacitors (MIM)

The Metal-insulator-metal capacitor, shown in Fig. 4.5, uses two metal layers for metal plates. This compensates the effects of simultaneous switching noise.

Metal-insulator-metal (MIM) capacitors are very valuable in many applications. They can be used in radio frequency (RF) circuits, in various configurations in analog ICs, and for decoupling capacitance in microprocessor units (MPUs).

In general, good capacitor matching, precision control of capacitor values, and small parasitic capacitance are required for analog switching circuits.

Fig. 4.5: Structure of the MIM capacitors used in this design

In a switched-capacitor circuit, the transfer function of the circuit depends on the ratio of the values of two capacitors, not the absolute value of one capacitor. If the MIM process has a 10% tolerance in the dielectric thickness from one lot to the next lot, but 0.1% thickness uniformity within one chip, the ratio of the value of two capacitors on the same chip can be expected to have 0.1% accuracy. This is an important advantage of the switched-capacitor circuits. The voltage dependent device capacitance, which is connected to the voltage-independent MIM capacitance, is to be treated as parasitic capacitance in the switched-capacitor circuits. It is desirable to use the parasitic-insensitive integrators to realize the desired circuit

In comparison with the *pn*-junction and MIS capacitance, the MIM capacitor has a high linearity over a wide voltage range, which is very desirable for these applications. For example, the switched-capacitor filter circuits have become extremely popular due to their accurate frequency response (depending on capacitance ratio), as well as good linearity and dynamic range [4.4].

4.5 Reference

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Chapter

Conclusion and Future Work

5.1 Conclusion

It is clear that the operating voltage for CMOS technology is decreasing much faster than predicted. The main drive behind this trend is the long-term production reliability and low-power, digital operation.

A low voltage, low power analog-to-digital converter with scaled technology has been investigated in this thesis for applications such as DVI flat-panel displays, RGB-to-LCD drivers, Gigabit Ethernet systems and cable modems.

To achieve the specifications required by those applications, the A/D converter was realized using 1 bit per stage pipelined architecture in 0.18 μm CMOS standard process.

The performance of the analog-to-digital converter indicates 8 bit resolution at 100MSampling/Sec with a 1.2V supply voltage and 40.6 mW power dissipation. The INL is around 1 LSB and voltage swing is 1 volt peak-to-peak (0.1V to 1.1V).

The area of the design excluding the pads is $0.25 \mu\text{m}^2$ and including the pad circuits is $1.2 \mu\text{m}^2$.

5.2 Future Works

5.2.1 Resolution

8-bit resolution is enough for the Giga bit Ethernet systems or RGB-to-LCD drivers. For other application such as cable modems, more resolution helps system to get better performance. One can achieve 10-bit resolution or better using 2 or 3 stages flash comparators to generate more output bits. But the disadvantage of using this method is the increase in the power dissipations.

5.2.2 Accuracy

Another open research area is the accuracy. One method to increase the accuracy is by adding redundancy to the stages of the pipelined analog-to-digital converter to compensate the offset errors of the comparators.

The most common method to realize this is to use 1.5 bit per stage architecture as well as digital calibration circuitry.

Any method, which eliminates the effects of the capacitor mismatch of the inter-stage switching capacitor circuit such as the feed-forward and the feed-back capacitors, could be a solution for better accuracy.

5.2.3 Power Dissipation

The size of the feedback capacitors in the inter-stage switched capacitor circuit is determined by the resolution, the power dissipation, and the speed factors.

Scaling is a method to reduce the power consumption of the pipelined analog-to-digital converter. This method can help designers to reduce the power dissipation with an acceptable drawback in speed and accuracy.

Another method which can reduce power dissipation is using dynamic comparators instead of the static comparators. The main drawback of this method is speed. Also, there would be little room for supply voltage reduction.