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A CMOS voltage-mode image sensing system

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A CMOS Voltage-Mode Image Sensing System

by

Jun Zhang

A project report
presented to Ryerson University
in partial fulfillment of the
requirement for the degree of
Master of Engineering
in the Program of
Electrical and Computer Engineering.

Toronto, Ontario, Canada, 2007

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A CMOS Voltage-Mode Image Sensing System

Master of Engineering, 2007

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Abstract

A CMOS image sensor consists of a light sensing region that converts photonic energy to an electrical signal and a peripheral circuitry that performs signal conditioning and post-processing. This project investigates the principle and design of CMOS active image sensors. The basic concepts and principle of CMOS image sensors are investigated. The advantages of CMOS image sensors over charge-coupled device (CCD) image sensors are presented. Both passive pixel sensors (PFS) and active pixel sensors (APS) are examined in detail. The noise of CMOS image sensors is investigated and correlated double sampling (CDS) techniques are examined. The design of APS arrays, CDS circuits and 8-bit analog-to-digital converters in TSMC-0.18 μm 1.8V CMOS technology is presented. The simulation results and layout of the designed CMOS image sensor are presented.

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Abbreviations

1. CCD ..... Charge-coupled device
2. PPS ..... Passive pixel sensor
3. SNR ..... Signal-to-noise ratio
4. RS ..... Row selection
5. SF ..... Source follower
6. S/H ..... Sample-and-hold
7. CDS ..... Correlated double sampling
8. ADC ..... Analog-to-digital converter
9. FPN ..... Fixed pattern noise
10. TTL ..... Transistor-transistor logic
11. PSD ..... Power spectral density
12. LSB ..... Least significant bit
13. DNL ..... Differential non-linearity
14. INL ..... Integral non-linearity
15. FFT ..... Fast Fourier transform
16. THD ..... Total harmonic distortion
17. SiNAD ..... Signal-to-noise distortion
18. SFDR ..... Spurious-free dynamic range

19. SD	Sigma-delta
20. T/H	Track-and-hold
21. SW	Switch
22. OP AMP	Operational amplifier
23. MDAC	Multiplying digital-to-analog converter
24. DFF	D-flip flop

Chapter 1

Introduction

This chapter introduces light sensor-photodiodes and types of image sensors. The first section illustrates the important characteristics of photodiodes. The second section discusses the types and differences of image sensors.

1.1 Photodiodes

1.1.1 Electrical Characteristics

Photodiodes are semiconductor light sensors that generate a current or voltage when the P-N junction in the semiconductor is illuminated by light. The term photodiode can be broadly defined to include even solar batteries, but it usually refers to sensors used to detect light. There are several types of photodiodes possessing different functions. This chapter focuses on PN photodiodes [1]. Fig. 1.1 gives equivalent circuit of the silicon photodiodes.

Figure 1.1: Equivalent circuit of the silicon photodiodes.

A silicon photodiode can be modeled by a current source in parallel with an ideal diode. The current source represents the current generated by the incident radiation, while the diode

represents the p-n junction. In addition, a junction capacitance (C_j) and a shunt resistance (R_{SH}) are in parallel with the other components. A series resistance (R_s) is connected in series with all components.

A. Shunt Resistance (R_{SH})

The shunt resistance is the slope of the current-voltage curve of the photodiode at the origin ($V = 0$). Although an ideal photodiode has an infinite shunt resistance, practical photodiodes have a finite shunt resistance in the range of $10M\Omega$ – $1G\Omega$. The shunt resistance is used to determine the noise current in the photodiode with no bias. For the best photodiode performance the highest shunt resistance is desired. The higher the shunt resistance, the less the shunt current so that the output current of the photodiode more precisely reflect the actual illumination intensity.

B. Series Resistance (R_s)

The series resistance of a photodiode arises from the resistance of the contacts and the resistance of the undepleted silicon of the diode. It is given by

$$R_s = \frac{(W_s - W_d)\rho}{A} + R_c, \quad (1.1)$$

where W_s is the thickness of the substrate, W_d is the width of the depleted region, A is the diffusion area of the junction, ρ is the resistivity of the substrate, and R_c is the contact resistance. The series resistance is used to determine the linearity of the photodiode in the photovoltaic mode. Although an ideal photodiode should have a zero series resistance, the typical value of the series resistance ranges from 10Ω to $1k\Omega$.

C. Junction Capacitance (C_j)

The boundaries of the depletion region act as the plates of a parallel plate capacitor. The junction capacitance is directly proportional to the diffusion area and inversely proportional

to the width of the depletion region. In addition, substrates with a high resistivity have a small junction capacitance. Moreover, the capacitance is dependent on the reverse biasing voltage as per

$$C_J = \frac{\epsilon_{Si}\epsilon_0 A}{\sqrt{2\mu_n(V_A + V_{bi})}}, \quad (1.2)$$

where $\epsilon_0 = 8.854 \times 10^{-14} F/cm$ is the permittivity of free space, $\epsilon_{Si} = 11.9$ is the dielectric constant of silicon, $\mu_n = 1400 \text{ cm}^2/V_s$ is the bulk mobility of the electrons at 300K, ρ is the resistivity of the silicon, V_{bi} is the built-in voltage of the pn-junction, and V_A is the reverse biasing voltage. Fig. 1.2 shows capacitance of photoconductive devices versus reverse bias voltage.

Figure 1.2: Capacitance of photoconductive devices versus reverse bias voltage.

1.1.2 I-V Characteristics

The current-voltage characteristics of a photodiode with no incident light are similar to those of a rectifying diode. When the photodiode is forward biased, there is an exponential increase in the current. When a reverse bias is applied, a small reverse saturation current appears. It is related to dark current as

$$I_D = I_{sat}(e^{\frac{qV_A}{K_B T}} - 1), \quad (1.3)$$

where I_D is the photodiode dark current, I_{sat} is the reverse saturation current, q is the electron charge, V_A is the applied bias voltage, $K_B=1.38 \times 10^{-23} \text{ J/K}$ is Boltzmann constant and T is the absolute temperature in degrees Kelvin.

Figure 1.3: I-V curves of photodiodes.

This relation is shown in Fig. 1.3. From Eq. (1.3), three states can be defined:

- (a) $V_A=0$: The current becomes the reverse saturation current.
- (b) $V_A > 0$: The current increases exponentially. This state is also known as the forward bias mode.
- (c) $V_A < 0$: When a reverse biasing voltage is applied across the photodiode, the current behaves as shown in Fig. 1.3.

Illuminating the photodiode with an optical radiation shifts the I-V curve by the amount of the photocurrent (I_P). Thus,

$$I_{total} = I_{sat}(e^{\frac{qV_A}{K_B T}} - 1) - I_P. \quad (1.4)$$

As the reverse biasing voltage increases, there is a sharp increase in the photodiode current. The applied reverse biasing voltage at this point is referred to as the breakdown voltage. This is the maximum reverse biasing voltage and photodiodes should operate below

the breakdown voltage. Breakdown voltage varies from one photodiode to another and is usually measured, for small active areas, at a photodiode current of $10\mu A$.

1.1.3 Noise

Shot noise is related to the random fluctuation in both the photocurrent and the dark current of a photodiode. The power of the shot noise is given by

$$\overline{i_{sn}^2} = 2q(I_P + I_D)\Delta f, \quad (1.5)$$

where $q=1.6\times 10^{-19}C$, is the electron charge, I_P is the photo-generated current, I_D is the photo-detector dark current and Δf is the noise measurement bandwidth. Shot noise is the dominating source when photodiodes are operated in the photoconductive mode.

A. Thermal Noise

The shunt resistance of a photo-detector generates thermal noise. This is due to the thermal generation of carriers. The magnitude of this thermal noise is given by

$$\overline{i_{jn}^2} = \frac{4k_B T \Delta f}{R_{SH}}, \quad (1.6)$$

where R_{SH} is the shunt resistance of the photodiode. Thermal noise is the dominant current noise in the photovoltaic operation mode.

B. Total Noise

The total noise current generated in a photo-detector is determined by

$$\overline{i_{tn}^2} = \overline{i_{sn}^2} + \overline{i_{jn}^2}. \quad (1.7)$$

1.1.4 Temperature Effect

The performance of a photodiode including shunt resistance, dark current, breakdown voltage, responsivity, and junction capacitance, is affected by temperature. There are two major currents in a photodiode contributing to dark current and shunt resistance. Diffusion current is the dominating factor in photovoltaic mode of operation, which determines the shunt resistance. It is a square function of temperature. In photoconductive mode, however, the drift current becomes the dominant current (dark current) and varies directly with temperature. Thus, photo-detectors are more sensitive to temperature in the photovoltaic mode than in the photoconductive mode of operation. In the photoconductive mode the dark current approximately doubles for every 10°C increase in temperature. In the photovoltaic mode, the shunt resistance approximately doubles for every 6°C decrease in temperature. The exact amount depends on other parameters such as the reverse bias, the resistivity of the substrate and the thickness of the substrate.

1.2 Types of Image Sensors

An image sensor is a device that converts a visual image to an electric signal. It is widely used in digital cameras and other imaging devices. It is usually an array of either charge-coupled devices (CCD) or CMOS pixels.

1.2.1 CCD Image Sensors

CCD image sensors are electronic devices that are capable of transforming a light pattern (image) into an electric charge pattern (an electronic image). A CCD consists of several individual elements that have the capability of collecting, storing and transporting electrical charges from one element to another. This together with the photosensitive characteristics of silicon is used to design image sensors. Each photosensitive element represents a picture element (pixel). With semiconductor technologies and design rules, structures are made that form lines, or matrices of pixels. One or more output amplifiers at the edge of the chip collect the signals from the CCD. An electronic image can be obtained by exposing the sensor to

a light pattern, and applying a series of pulses that transfer the charge of pixels to output amplifiers.

1.2.2 CMOS Image Senosrs

Unlike CCD sensors, CMOS image sensors do not use charge coupling, that transfers charges to a second bank of photo-sites before sending them out for analog-to-digital conversion. CMOS image sensors have amplifiers and output circuitry fabricated near each photo-site.

1.2.3 Comparison of CCD and CMOS Sensors

CCDs use a special manufacturing process to create the ability to transport charges across the chip without distortion. This process leads to very high-quality sensors in terms of fidelity and light sensitivity. CMOS chips, on the other hand, use traditional manufacturing processes to create the chip – the same processes used to make most microprocessors. Because of the differences in fabrication, there are some notable differences between CCD and CMOS sensors [2].

- CCD sensors create high-quality, low-noise images. CMOS sensors are more susceptible to noise.
- Because each pixel of a CMOS sensor consists of a photodiode and several transistors, the light sensitivity of a CMOS sensor tends to be lower. Many of the photons hitting the chip hit the transistors instead of the photodiode.
- CMOS consumes little power. Implementing a sensor in CMOS yields a low-power sensor. CCD, on the other hand, suffers from a high level of power consumption.
- CMOS sensors are fabricated in standard CMOS technologies with a low cost.

Chapter 2

CMOS Image Sensors

CMOS pixels can be classified into two main categories: passive pixel sensors (PPSs) and active pixel sensors (APSs). Each individual pixel of a PPS array has only a photo-sensing element and a switching MOSFET. The signal is detected either by an output amplifier implemented in each column or by a single output for the entire imaging device. Each pixel of a APS array, on the other hand, has an amplifier built in the pixel to improve signal-to-noise ratio.

2.1 Passive Pixel Sensors

A PPS consists of a photodiode and a transistor. TX is applied to the gate of the transistor, switching the contents of the pixel to the charge integration amplifier (CIA). Fig. 2.1 shows the PPS structure.

Figure 2.1: Structure of passive pixel sensors.

These passive pixel CMOS sensors operate like analog DRAMs, as shown in Fig. 2.2.

The passive pixel structure suffers from a large capacitive load. Since the large bus is

Figure 2.2: Basic architecture of PPS.

directly connected to each pixel during a readout operation, the RC time constant is very high and the readout signal is slow. In addition, passive pixel readout noise is typically high-on the order of 250 electrons rms compared to the less than 10 electrons rms for commercial CCDs. Because of these factors, PPS does not scale with a larger array size or a higher pixel readout rate. PPS, on the other hand, has the highest fill factor since each pixel has only one transistor. In addition, quantum efficiency can be quite high due to its large fill factor.

2.2 Active Pixel Sensors

An active pixel sensor has an active amplifier (a source follower transistor) built within the pixel [3]. Fig. 2.3 shows the architecture of APS arrays.

Active pixels typically have a fill factor of only 50-70% . However, the reduced capacitance in each pixel leads to lower readout noise, which increases both the dynamic range and the signal-to-noise ratio (SNR). The pixel used in these sensors can be classified into three types: photodiodes, photogates and pinned photodiodes.

Figure 2.3: General architecture of APS arrays.

2.2.1 Photodiode APS

A photodiode APS employs a photodiode and a readout circuit of three transistors: a photodiode reset transistor (Reset), a row select transistor (RS) and a source-follower transistor (SF). The schematics of this pixel is shown in Fig. 2.4.

Figure 2.4: Basic photodiode APS pixel.

The charge-to-voltage conversion is performed by the sense mode capacitor whose capacitance includes the photodiode capacitance and all other parasitic capacitances connected to the node including the source capacitance of the Reset transistor and the gate capacitance of the SF transistor. The SF transistor acts as a buffer amplifier to isolate the sensing node. The load of the buffer (the active-current-source load) is located at each column rather than in each pixel to keep the fill factor high and to reduce pixel-to-pixel variations. The Reset transistor controls the integration time and is usually implemented with an NMOS transistor. Since no additional well is required for NMOS implementation, this allows a higher fill factor. However, an NMOS transistor with V_{DD} on the both gate and drain can only reach a source voltage (at the photodiode node) of $V_{DD}-V_T$, thereby decreasing the dynamic range of the pixel. Generally, pixel operation can be divided into two stages: reset and photo-transduction.

(a) Reset stage—During this stage, the photodiode capacitance is charged to a reset voltage by turning on the Reset transistor. This reset voltage is read out to one of sample-and-holds (S/H) in a correlated double sampling (CDS) circuit. The CDS circuit, usually located at the bottom of each column, subtracts the signal pixel value from the reset value. Its main purpose is to eliminate the fixed pattern noise caused by the random variation in the

threshold voltage of the reset and pixel amplifier transistors, variations in the photodetector geometry and variations in the dark current. In addition, it eliminates the $1/f$ noise of the circuit.

(b) Photo-transduction stage-During this stage, the photodiode capacitor is discharged with a constant integration time at a rate approximately proportional to the incident illumination. A bright pixel produces a low analog signal voltage and a dark pixel gives a high signal voltage. This voltage is read out to the second S/H of the CDS by enabling the row select transistor of the pixel. The CDS outputs the difference between the reset voltage level and the photo-voltage level.

Because the readout of the all pixels cannot be performed in parallel, a rolling readout technique is applied. All the pixels in each row are reset and read out in parallel, but the different rows are processed sequentially.

2.2.2 Photogate APS

Fig. 2.5 shows the common architecture of photogate pixels [4], [5]. The basic concept for the photogate pixel arose from CCD technology. While photon-generated charge is integrated under a photogate with a high potential well, the output floating node is reset and the corresponding voltage is read out to the S/H of the CDS. When the integration is completed, the charge is transferred to the output floating node by the signal pulse on the photogate. Then the corresponding voltage from the integrated charge is read by the source follower to the second S/H of the CDS. The CDS outputs the difference between the reset voltage level and the photo-voltage level.

2.2.3 Pinned Photodiode APS

The pinned photodiode pixel consists of a pinned diode, where the photon collection area is dragged away from the surface in order to reduce surface defect noise [6]. Photo-generated charge is integrated under a pinned diode and transferred to the output floating diffusion for the readout. As in the photogate APS, the sense node and integration node are separated

Figure 2.5: Basic architecture of photogate pixels.

to minimize noise. However, the primary difference is that the potential well for charge collection in a pinned diode is generated by a buried intrinsic layer instead of a pulsed gate voltage as in the photogate. Each pinned diode pixel has four transistors and five control lines, resulting in a fill factor higher than photogate pixels, but lower than photodiode pixels. However, the small photon collection area of the pinned diode results in a very small full well for photon-generated charge collection and lower quantum efficiency compared to photodiode pixels. Fig. 2.6 shows the basic architecture of pinned photodiode pixels.

Figure 2.6: Basic architecture of pinned photodiode pixels.

2.3 Architecture of CMOS Image Sensors

Fig. 2.7 shows the architecture of CMOS image sensors. There are five major components: (1) a two-dimensional array, (2) a controller, (3) a correlated double sampling (CDS) circuit, (4) a column multiplexer, and (5) an analog-to-digital converter (ADC) [7].

Figure 2.7: Architecture of CMOS image sensors.

The two-dimensional pixel array is used to sense the image and convert the light intensity of pixel into an analog signal. The controller with row decoding circuitry selects the row of pixels to be read out at any given time. Also it regulates the operation of the entire chip. The CDS circuit is used to eliminate the FPN. The column multiplexer selects one column output at a time to the analog-to-digital converter that converts an analog voltage to an 8-bit digital code as the final output.

Chapter 3

Correlated Double Sampling

CMOS imagers suffer from a high level of noise. Reducing the noise level is critical to increase the dynamic range of CMOS imagers. This chapter focuses on correlated double sampling circuit that is widely used to reduce the noise of CMOS image sensors [8].

3.1 Why is CDS Needed?

3.1.1 Analysis of Temporal Noise in CMOS APS

The readout path in a CMOS image sensor, by comparison, comprises several active devices that introduce both temporal noise and FPN [9], [10].

Temporal noise is the most fundamental non-ideality in an image sensor as it sets the ultimate limit on signal fidelity. Temporal noise is independent across pixels and varies from frame to frame. In the CMOS active pixel sensor described in this project, each pixel unit cell contains an imaging element and three transistors for readout, selection, and reset. The imager is read out a row at a time using column parallel readout architecture. The image sensor is operated with transistor-transistor logic (TTL) clocks and at most two other DC voltages. The main temporal noise sources associated with this system are reset noise on the reset transistor, $1/f$ noise from the input transistor of the in-pixel source-follower, dark current shot noise, reset noise on the sample-and-hold capacitors, white noise and $1/f$ noise from the second source-follower [11].

Fig. 3.1 shows APS circuit. During integration, the dominant noise source is shot noise

Figure 3.1: APS circuit.

$I_s(t)$ due to the dark current i_{dc} and the photocurrent i_{ph} , which is given by modeled as white Gaussian noise with two sided power spectral density

$$S_{I_s(t)} = q(i_{ph} + i_{dc}) \quad A^2/Hz. \quad (3.1)$$

To analyze the noise, we let $V_{pd}(t) = v_{pd}(t) + V_n(t)$ be the voltage of the photodiode during the integration, where $v_{pd}(t)$ is the signal voltage and $V_n(t)$ is the noise voltage. It then follows that

$$\frac{dV_{pd}(t)}{dt} = -\frac{i_{ph} + i_{dc} + I_s(t)}{C_{pd}(V_{pd}(t))}. \quad (3.2)$$

If the photodiode capacitance is constant over the integration time, one can show that the mean square value of the noise voltage sampled at the end of the integration, at t_{int} , is given by

$$\overline{V_n^2(t_{int})} = \frac{q(i_{ph} + i_{dc})}{C_{pd}} t_{int}. \quad (3.3)$$

The photodiode capacitance, however, is a function of its reverse bias voltage. As the result, the photodiode output voltage is nonlinear. Assuming that the noise is much smaller than the signal, we can write the noise part as

$$\frac{dV_n(t)}{dt} - \frac{1}{C_{pd}^2(v_{pd}(t))} \frac{dC_{pd}(v_{pd}(t))}{dv_{pd}(t)} V_n(t)(i_{ph} + i_{dc}) = -\frac{I_s(t)}{C_{pd}(v_{pd}(t))}. \quad (3.4)$$

The mean square value of V_n at the end of the integration is thus given by

$$\overline{V_n^2(t_{int})} = q(i_{ph} + i_{dc}) \int_0^{t_{int}} \frac{1}{C_{pd}^2(v_{pd}(\tau))} e^{-2(i_{ph} + i_{dc}) \int_\tau^{t_{int}} \frac{d(1/C_{pd}(v_{pd}(\tau_0)))}{dv_{pd}(\tau_0)} d\tau_0} d\tau. \quad (3.5)$$

During the reset, M3 is turned off and a V_{dd} pulse is applied to the gate of M1. At the beginning, and for a very short amount of time, M1 is in the saturation region. It then goes below the threshold for the reset of the reset time. In the subthreshold region the transistor noise is mainly due to shot noise with two-sided PSD given by

$$S_{I_d}(t) = qi_d \quad (A^2/Hz), \quad (3.6)$$

where i_d is the drain current of M1. If the reset time t_r is larger than the settling time t_{settle} , defined as the time at which the transistor subthreshold current equals the photodiode current $i_{ph} + i_{dc}$, the average reset noise power is given by

$$\overline{V_n^2} = \int_{\min}^{\max} \frac{2q(i_{ph} + i_{dc})}{(g_{m1} + g_{mb1})^2} \frac{1}{1 + (2\pi f \frac{C_{pd}}{g_{m1} + g_{mb1}})^2} df, \quad (3.7)$$

where g_{mb1} is the transconductances of M1 in subthreshold, and the factor of 2 is due to the fact that in the steady state, $i_d = i_{ph} + i_{dc}$. Performing integral we get

$$\overline{V_n^2} = \frac{q(i_{ph} + i_{dc})}{C_{pd}(g_{m1} + g_{mb1})}. \quad (3.8)$$

During the readout, the noise circuit is due to transistors M2, M3, M4, and the column and chip level circuits thermal and $1/f$ noise. Ignoring the noise contribution of the column and chip level circuits, and the $1/f$ noise, readout noise can be computed via the small signal circuit in Fig. 3.2.

Figure 3.2: Small signal circuit for noise analysis during the readout.

In this figure, $I_{M2}(t)$, $V_{M3}(t)$, and $I_{M4}(t)$ are the thermal noise sources associated with M2, M3, and M4, respectively, g_{m2} and g_{m4} are the transconductances of M2 and M4 respectively, g_{d3} is the channel conductance of M3, and C_0 is the column storage capacitance including the bit-line capacitance. In the steady state, it can be shown that the bit-line referred mean square noise voltage due to M2, M3, and M4 are given by

$$\overline{V_{n,M2}^2} = \frac{2}{3} \frac{kT}{C_0} \frac{1}{1 + \frac{g_{m2}}{g_{d3}}}, \quad (3.9)$$

$$\overline{V_{n,M3}^2} = \frac{kT}{C_0} \frac{1}{g_{d3} \left(\frac{1}{g_{d3}} + \frac{1}{g_{m2}} \right)}, \quad (3.10)$$

and

$$\overline{V_{n,M4}^2} = \frac{2}{3} \frac{kT}{C_0} g_{m4} \left(\frac{1}{g_{d3}} + \frac{1}{g_{m2}} \right). \quad (3.11)$$

3.1.2 Fixed Pattern Noise

Fixed pattern noise (FPN) is due to device and interconnects mismatches across an image sensor [12]. FPN gives rise to different pixel outputs under uniform illumination. FPN is mainly due to variations in photodetector area and dark current, which are spatially

uncorrelated. The white noise model is not adequate for characterizing FPN in CMOS sensors because the readout signal paths of both CMOS passive and active pixel sensors include several amplifiers some of which are shared by pixels and some are not. These amplifiers introduce additional FPN [13]. FPN due to the variations in column amplifier offsets and gains causes “striped” noise.

Figure 3.3: APS signal path.

Fig. 3.3 is used to explain FPN. Pixel FPN is caused by photodiode leakage, variations in photodiode size, variations in photodiode capacitance, channel charge injection from M1, capacitive coupling from the overlap capacitance of M1, threshold variations in M1, and threshold variations in the column amplifier.

The setup used to measure FPN is described by Fowler et al. [14]. It consists of a DC light source, a monochromator, an integrating sphere, and a calibrated photodiode. The measurements were performed under no illumination (dark) and at typically illumination using a monochromatic source, of wavelength $\lambda = 600nm$. The results clearly showed that CDS reduced FPN for both PPS and APS. After CDS the FPN of PPS is higher than that of APS. The FPN correlation between pixels is high for PPS and low for APS. This suggests that variations in column amplifier offset, charge injection, and capacitive coupling, which

dominate pixel FPN in PPS are highly correlated, while pixel area and dark current, which dominate pixel FPN in APS, vary rapidly from pixel to pixel [15].

3.2 Correlated Double Sampling

The reset and signal levels are read differentially, allowing CDS to suppress KTC noise, $1/f$ noise, and fixed pattern noise.

A schematic of the baseline pixel design and readout circuit used in CMOS APS arrays is shown in Fig. 3.4 [4]. The pixel unit cell is shown within the dotted outline. The imaging structure consists of a photodiode, a reset transistor (MR), the input transistor of the in-pixel source-follower (MIN), and a row selection transistor (MX).

The readout circuit, which is common to an entire column of pixels, includes the load transistor of the first source follower (MLN) and two sample-and-hold circuits for storing the signal level and the reset level. Sampling both the reset and signal levels permits correlated double sampling (CDS), which suppresses reset noise of the pixel, $1/f$ noise and threshold variations from the source-follower transistor within the pixel [16], [17], [18]. Each sample-and-hold circuit consists of a sample-and-hold switch (MSHS or MSHR), capacitor (CS or CR), a column source-follower (MP1 or MP2), and column selection transistor (MY1 or MY2) to buffer the capacitor voltages and to drive the high capacitance horizontal bus at higher readout speeds. The load transistors of the column source-followers (MLP1 and MLP2) are common to the entire array of pixels. P-channel source-followers are used in the column circuit to compensate for the level shifting of the signal due to the n-channel source-followers within the pixels. The transistor and capacitor sizes are summarized in Table 3.1.

Table 3.1: Value of the parameters of CDS.

Transistor	MR	MIN	MX	MLN	MSHS	MSHR
Width	$0.7\mu m$	$0.7\mu m$	$0.7\mu m$	$1\mu m$	$1\mu m$	$1\mu m$
Transistor	MP1	MP2	MY1	MY2	MLP1	MLP2
Width	$5\mu m$	$5\mu m$	$1\mu m$	$1\mu m$	$0.7\mu m$	$0.7\mu m$
Capacitor	$CS = 1pF$	$CR = 1pF$				

The operation of this image sensor is illustrated as the following: The input transistor of the in-pixel source follower and the column source-followers MLN, MLP1, and MLP2 in Fig. 3.4 are DC biased at the diode connection, $1.8V$ and $1.8V$ respectively. During the reset, the reset transistor MR is biased at $1.8V$, allowing the photodiode to be in reversing biasing. Following the integration, an entire row of pixels is read out simultaneously. First, the pixels in the row to be read out are addressed by enabling the row selection switch MX. This resets the photodiode to reverse bias status without illumination. The output of the first source-follower is sampled onto capacitor CR at the bottom of column by enabling the sample-and-hold switch MSHR. During the photo-transduction status, the reset transistor is pulsed low to $0v$, the charge stored in the photodiode capacitance and the other parasitic capacitance at the output of photodiode starts to discharge by the reverse saturation current. In this project the reverse saturation current generated by illumination is in the range from several hundred nanoamperes to several microamperes. After the integration, the new output voltage is sampled onto capacitor CS by enabling the sample and hold switch MSHS. The stored reset and signal levels are sequentially scanned through the second set of source-followers by enabling the column address switches MY1 and MY2. The timing sequence is shown in Fig. 3.5. The simulation results are shown in Fig. 3.6. Here X axis represents the current value arising from different optical radiations on the photodiode, and Y axis represents the output of the CDS circuit in the signal sampling and reset period. Fig. 3.7 shows the layout of CDS circuit.

3.3 Subtraction and Level Shift

After the readout of reset and signal, the outputs of the reset and signal branches are again read out differentially, thereby generating a voltage which is proportional to the difference between the reset and signal levels [19]. In this project the subtraction of reset and signal is implemented by a differential-input and single-ended output amplifier [20]. Pixel circuits successively output a signal level and a reset level voltage within a horizontal period, and column CDS circuits receive these two voltage values. The output circuit of the amplifier

Figure 3.6: Signal and reset outputs of CDS circuit.

subtracts these signals to generate an output signal without FPN. In order to make the signal generated fit the input swing range of the ADC, the source follower is used to perform a level shift. The circuit of subtraction and level shift is shown in Fig. 3.8. Table 3.2 shows transistor sizes of subtraction and level shift circuit.

Table 3.2: Parameters of subtraction and level shift circuit.

Transistor	M1	M2	M3	M4	M5	M6	M7
Width	$1\mu m$	$1\mu m$	$10\mu m$	$10\mu m$	$5\mu m$	$1\mu m$	$1\mu m$

Figure 3.7: Layout of CDS circuit.

Figure 3.8: Subtraction and level shift circuit.

Chapter 4

8-Bit Pipelined Analog-to-Digital Converter

In this chapter the design of an 8-bit pipelined analog to digital converter is presented.

4.1 Basic Concepts

A. The Ideal Transfer Function

The transfer function of an A/D is a plot of the input voltage of the ADC versus the code's output of the ADC [21]. This plot is not continuous but rather a plot of 2^N codes, where N is the ADC's resolution in bits. If you were to connect the codes by lines (usually at code-transition boundaries), the ideal transfer function would plot a straight line. A line drawn through the points at each code boundary would begin at the origin of the plot, and the slope of plot for each supplied ADC would be the same as shown in Fig. 4.1.

Fig. 4.1 shows the ideal transfer function of a 3-bit ADC with reference points at code transition boundaries. The output code is at its lowest (000) when input voltage is less than 1/8 of the full-scale (the size of this ADC's code width). Also, the ADC reaches its full-scale output code (111) at 7/8 of full scale [22].

4.1.1 Static Performance

A. Full-Scale Error

To understand full-scale error, offset error must be introduced. Offset error, often called

Figure 4.1: Ideal transfer function of 3-bit ADCs.

“zero-scale” error, indicates how well the actual transfer function matches the ideal transfer function at a single point. For an ADC, the zero-scale voltage is applied to the analog input and is increased until the first transition occurs. Full-scale error is the difference between the ideal code transition to the highest output code and the actual transition to the output code when the offset error is zero. This is observed as a change in the slope of the transfer function line, as shown in Fig. 4.2. A similar specification, gain error, also describes the non-ideal slope of the transfer function and what the highest code transition would be without the offset error. Full-scale error accounts for both gain and offset deviations from the ideal transfer function.

Figure 4.2: Full-scale error.

B. Nonlinearity

Ideally, each code width (LSB) of an ADC's transfer function should be uniform in size. For example, all codes in Fig. 4.1 should represent exactly $1/8$ of the ADC's full-scale voltage reference. The difference in code width from one code to the next is differential nonlinearity (DNL). The code width or LSB of a N-bit ADC is given by

$$LSB = \frac{V_{ref}}{2^N}. \quad (4.1)$$

The voltage difference between each code transition should be equal to LSB. The deviation of each code from LSB is measured as DNL. This can be observed as uneven spacing of the code “steps” or transition boundaries in the ADC’s transfer function plot. In Fig. 4.3, a selected digital output code width is larger than the step size of the previous code. This difference is the DNL error. DNL is calculated from

Figure 4.3: Differential nonlinearity.

$$DNL = \frac{V_{n+1} - V_n}{V_{LSB}}, \quad (4.2)$$

where V_n is the physical value corresponding to the digital output code n , and V_{LSB} is the ideal spacing for two adjacent digital codes.

The integral nonlinearity (INL) is the deviation of an ADC’s transfer function from a straight line. This line is often a best-fit line among the points in the plot but can also be a line that connects the highest and lowest data points. INL is determined by measuring the voltage at which all code transitions occur and comparing them to the ideal. The difference

between the ideal voltage levels at which code transitions occur and the actual voltage is the INL error, expressed in LSBs. An INL error at any given point in an ADC's transfer function is the accumulation of all DNL errors of all previous (or lower) ADC codes, hence it is called the integral nonlinearity. This is observed as the deviation from a straight-line transfer function, as shown in Fig. 4.4.

Figure 4.4: Integral nonlinearity error.

Because nonlinearity in measurement will cause distortion, INL will also affect the dynamic performance of an ADC.

4.1.2 Dynamic Performance

The dynamic performance of an ADC is specified using parameters obtained via frequency-domain analysis and is typically measured by performing a fast Fourier transform (FFT) on the output codes of the ADC. The fundamental frequency is the input signal frequency. This is the signal measured with the ADC. Everything else is noise to be characterized with respect to the desired signal. This includes harmonic distortion, thermal noise, $1/f$ noise, and quantization noise.

A. Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is the ratio of the power of the input signal to the noise power (excluding harmonic distortion), expressed in decibels (dB)

$$SNR = 10 \log \left(\frac{V_{signal}^2}{V_{noise}^2} \right). \quad (4.3)$$

The noise measured in an SNR calculation does not include harmonic distortion but does include quantization noise (an artifact of quantization error) and all other sources of noise. For a given ADC resolution, the quantization noise is what limits an ADC to its theoretical best SNR because the quantization error is the only error in an ideal ADC. The theoretical best SNR is calculated from

$$SNR = 6.02N + 1.76, \quad (4.4)$$

where N is the ADC resolution.

B. Harmonic Distortion

Nonlinearity in a data converter results in harmonic distortion when analyzed in the frequency domain. Such distortion is observed as “spurs” at the harmonics of the signal. The total harmonic distortion (THD) is calculated from

$$THD = 20 \log \left(\frac{\sqrt{V_2^2 + V_3^2 + \dots + V_n^2}}{V_1} \right), \quad (4.5)$$

where V_1 means the fundamental frequency voltage, and V_n means the RMS voltage of harmonic n .

C. Signal-to-Noise and Distortion

Signal-to-noise and distortion (SiNAD) offers a more complete picture by including the

noise and harmonic distortion in one specification. SiNAD gives a description of how the measured signal will compare to the noise and distortion and is defined as

$$SiNAD = 20 \log \left(\frac{V_1}{\sqrt{V_2^2 + V_3^2 + \dots + V_n^2 + V_{noise}^2}} \right). \quad (4.6)$$

D. Spurious-Free Dynamic Range

Finally, the spurious-free dynamic range (SFDR) is the difference between the magnitude of the measured signal and its highest spur peak. The spur is typically a harmonic of the measured signal.

4.2 Architecture of Pipelined Analog-to-Digital Converters

The most popular ADC architectures available today include successive approximations (sometimes called SAR), flash (all decisions made simultaneously), pipelined (with multiple flash stages), and sigma-delta (SD), charge-balancing. All A/D converters require one or more steps involving a comparison of an input signal with a reference. This project uses an 8-bit pipelined analog-to-digital converter as the column ADC of the CMOS image sensor [23].

The pipelined architecture effectively overcomes the limitation of the flash architecture. A pipelined converter divides the conversion task into several consecutive stages. Each of these stages, as shown in Fig. 4.5, consists of a sample-and-hold circuit, a N-bit ADC, and a M-bit DAC. The sample-and-hold circuit samples the signal. The N-bit ADC converts the sampled signal to a digital datum. The conversion result forms the most significant bits of the digital output. This same digital output is fed into the M-bit digital-to-analog converter, and its output is subtracted from the original sampled signal. The residual analog signal is then amplified and sent to the next stage in the pipeline. This process is repeated until the desired resolution is obtained. In principle, a pipelined converter with p pipelined stages,

each with M -bit DAC, can produce a high-speed ADC with a resolution of $N = p * M$ bits using $p * (2M - 1)$ comparators.

Figure 4.5: A single pipelined converter stage.

4.3 Circuit Design of ADC

4.3.1 Track-and-Hold (T/H) Circuit

Fig. 4.6 shows a simple track-and-hold circuit. In the sampling mode, switch S is *ON* and the output voltage, V_{OUT} , tracks the input voltage, V_{IN} [24].

Figure 4.6: Sampling circuit with a NMOS switch.

Two problems encountered in using an NMOS sampling switch in a Track-and-Hold circuit are: input-dependent ON-resistance and input-dependent charge injection.

- Input-dependent ON-resistance of MOS sampling switch: for a square-law NMOS device that operates in the triode region, its ON-resistance R_{on} is given by

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})}. \quad (4.7)$$

Since V_{gs} is equal to $V_{dd} - V_{in}$ in Fig. 4.6, R_{on} depends on V_{in} , which causes harmonic distortion [25]. Also since V_{dd} is relatively small (1.8V), V_{gs} is small, and hence in order to make R_{on} sufficiently small for a wideband track mode, W has to be large. This, however, will causes a large charge injection.

- Input-dependent charge injection: when a MOS switch turns off, the amount of charge Q_{ch} stored its channel is given by [26]:

$$Q_{ch} \approx WLC_{ox}(V_{gs} - V_{th}). \quad (4.8)$$

We see that since V_{gs} is equal to $V_{dd} - V_{in}$ in the T/H circuit, Q_{ch} depends on V_{in} , which causes pedestal errors.

These two problems can be solved by using a bootstrap switch driver for the NMOS sampling switch, as shown in Fig. 4.7.

Figure 4.7: Schematic of Bootstrap.

The circuit in Fig. 4.7 consists of two capacitors for doubling the DC level and a dynamic charge pump circuit. When the input clock is high, the capacitors are charged to V_{dd} through the charge pump. When the input clock is low, the voltage of C2 increases. M4 is OFF, M3 is ON. A boosted clock voltage is generated [27]. Fig. 4.8 shows the T/H circuit implementation, and Fig. 4.9 shows layout of T/H circuit.

Figure 4.8: Schematic of track-and-hold circuit.

Table 4.1: Parameters of T/H circuit.

Transistor	M1	M2	M3	M4	M5	M6
Width	$0.6\mu m$	$0.6\mu m$	$2\mu m$	$1\mu m$	$2\mu m$	$0.6\mu m$
Transistor	M7	M8	M9	M10	M11	M12
Width	$1\mu m$	$0.6\mu m$	$0.6\mu m$	$2\mu m$	$12\mu m$	$1.5\mu m$
Capcitor	$C1 = 0.3pF$	$C2 = 0.3pF$	$C3 = 0.6pF$	$C4 = 1pF$		

The T/H circuit parameters are tabulated in Table 4.1

M1, M2, C1 and C2 form a charge pump. When $THCLK$ is low, M6 and M9 are ON, connecting the gate of M12 to the ground. At this time C3 charges to V_{dd} through M5 and M6. When $THCLK$ is high, M5, M6 and M9 are OFF, M7 and M10 are ON, and the gate voltage of the switch is almost one V_{dd} above the source voltage. M9 and M10 limit the voltage drop across the terminals of M7 and M11.

4.3.2 One-Bit Digital-to-Analog Converter

One-bit digital-to-analog converter converts an one-bit digital input to an analog output [28]. One of the two analog values is selected by the digital single-bit input of the switch shown in Fig. 4.10.

The schematica of this block is shown in Fig. 4.11. Fig. 4.12 shows layout of switch. Transistors of the minimum size used to reduce switching non-idealities.

Figure 4.9: Layout of the track-and-hold circuit.

Figure 4.10: Block diagram of one-bit digital-to-analog converter.

Figure 4.11: Schematic of one-bit digital-to-analog converter.

Figure 4.12: Layout of the switch.

4.3.3 Comparator

A comparator is a device that compares two analog signals, and produces a binary output as per

$$V_{out} = \begin{cases} V_{max} & \text{if } v_+ > v_- \\ V_{min} & \text{if } v_+ < v_- \end{cases} . \quad (4.9)$$

Its characteristic is shown in Fig. 4.13.

Figure 4.13: Characteristic of comparators.

The comparator used in this design consists of a preamplifier followed by a latch and output buffer, as shown in Fig. 4.14.

The aspect ratio of the buffer inverter determines the output response delay of the comparator [29]. The schematic of the preamplifier is shown in Fig. 4.15. The differential configuration is adopted. V_{IN+} and V_{IN-} represent the two signals that need to be compared. M5 is used as the biasing current source. M1 and M2 are current source loads.

Figure 4.14: Typical structure of comparators.

Figure 4.15: Schematic of the preamplifier.

Figure 4.16: Schematic of the latch.

Fig. 4.16 is about the latch circuit.

The two outputs of the preamplifier act as two signal inputs in the latch. M7 and M8 form the latch. V-Latch actually plays the role of reset function. When V-Latch is low, the output of comparator is low without considering the value of inputs. When V-Latch is high, M10 and M11 are ON and the output of comparator will present high or low voltage level depending on the value of input signals. The output buffer circuit is shown in Fig. 4.17.

Figure 4.17: Schematic of the output buffer.

The above has given the integral schematic of comparator made up of three separate parts. Fig. 4.18 shows the simulation result of comparator block. Fig. 4.19 shows layout of comparator. The simulation is finished in $0.18\mu m$ CMOS standard technology with $1.8V$ supply voltage. The transistor sizes are listed in Table 4.2.

Table 4.2: Transistors' size of comparator.

Transistor	M1	M2	M3	M4	M5
Width	$10\mu m$	$10\mu m$	$40\mu m$	$40\mu m$	$10\mu m$
Transistor	M6	M7	M8	M9	M10
Width	$15\mu m$	$0.5\mu m$	$0.5\mu m$	$15\mu m$	$1\mu m$
Transistor	M11	M12	M13	M14	M15
Width	$1\mu m$	$15\mu m$	$0.5\mu m$	$0.5\mu m$	$15\mu m$
Transistor	M16	M17	M18	M19	
Width	$1\mu m$	$2\mu m$	$1\mu m$	$2\mu m$	

4.3.4 Operational Amplifier

Since an op amp is employed to implement the feedback system in this project, its open-loop gain should satisfy the precision required by the closed-loop circuit. The high-frequency behavior of the op amp plays a critical role. As the frequency of operation increases, the

Figure 4.18: Waveform of the comparator.

open-loop gain of the op amp begins to drop, creating a larger error in the feedback system. Cascode topology possesses an important property, a high output impedance, which can provide a high gain. In some applications the gain and/or output swings provided by cascode op amps are not enough. To solve this problem, a two-stage op amp is employed with the first stage to provide a high gain and the second stage to provide a large swing.

A two-stage configuration with a single-ended output shown in Fig. 4.20 is used in this project. Also layout of the operational amplifier circuit is given in Fig. 4.21. The first stage utilizes telescopic and folded-cascode structure to achieve a high gain and to alleviate the drawbacks of limiting output swing and difficulty in shorting the input and output [30]. Specially, M8 and M9 are biased at the edge of the triode region, and the maximum value of V_{out} can be increased by one PMOS threshold voltage. The common source configuration with a current source load constitutes the second stage.

Fig. 4.22 shows the magnitude and phase of the frequency response of the operational amplifier implemented in TSMC's $0.18\mu m$ $1.8V$ CMOS technology. The parameters of op

Figure 4.19: layout of the comparator.

Table 4.3: Parameters of the OP AMP.

4.3.5 Residue Amplifier

The switched-capacitor circuit uses an operational amplifier and its switched-capacitor feedback to generate a residue output for the next stage. The internal circuits of the op amp and the switch are shown in Fig. 4.20 and Fig. 4.24 [31].

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Figure 4.21: Layout of the operational amplifier.

Figure 4.22: Frequency response of the operational amplifier.

Figure 4.23: Schematic of the residue amplifier.

Figure 4.24: Schematic of the switch.

are non-conducting. On the other hand, if the gate voltage of the N-MOS transistor is V_{DD} and the gate voltage of the P-MOS transistor is GND, both transistors are conducting. If the source voltage is near V_{dd} , there is a voltage drop across the N-MOS transistor but no voltage drop across the P-MOS transistor. If the source voltage is near GND, the N-MOS transistor has no voltage drop. Finally the internal resistance of the switch is reduced.

When CK1 is high and CK2 is low, SW1, SW2, SW4, SW6 and SW7 are closed and SW3 and SW5 are open, C1, C2 are connected to the V_{IN-} . In the next phase, SW3 and SW5 are closed and other switches are open. The feedback switch is closed and V_D is connected to C2. The output voltage is given by

$$V_{OUT} = \left(\frac{C_1 + C_2}{C_1} \right) \times V_{IN-} - \left(\frac{C_2}{C_1} \right) \times V_D. \quad (4.10)$$

If $C_1 = C_2$, $V_{OUT} = 2V_{IN-} - V_D$.

The layout of the residue amplifier in Fig. 4.25.

4.3.6 MDAC(Multiplying Digital-to-Analog Converter)

A multiplying digital-to-analog converter or MDAC is the combination of three blocks: a comparator, a residue amplifier and a one-bit digital-to-analog converter. The block shown in Fig. 4.26 is a stage in the pipelined analog-to-digital converter. At the same time the layout of the MDAC is given in Fig. 4.27.

V_{Low} in this project is set to 0 V and V_{High} is 1 V and V_{ref} is equal to half of voltage

Figure 4.25: Layout of the residue amplifier.

Figure 4.26: Block diagram of the MDAC.

range 500mV.

Figure 4.27: Layout of the MDAC.

4.3.7 Synchronizer

Due to the delay of each stage in the pipelined architecture a synchronizer circuit is used to align and order the digital outputs by using a matrix of D-flip flop as shown in Fig.4.28.

Complementary clock signals in odd and even stages are used to trigger these flip-flops. The schematic of the D-flip-flop circuit shown in Fig. 4.29, has a dynamic positive edge trigger architecture. Transistors with the minimum size are used.

Figure 4.28: Block diagram of the synchronizer.

Figure 4.29: Schematic of the D-flip-flop.

The size of the transistors of the DFF is tabulated in Table 4.4.

Table 4.4: Transistors' size of D-flip-flop.

Transistor	M1	M2	M3	M4
Width	$1\mu m$	$1\mu m$	$1\mu m$	$5\mu m$
Transistor	M5	M6	M7	M8
Width	$5\mu m$	$1\mu m$	$1\mu m$	$1\mu m$
Transistor	M9	M10	M11	
Wdith	$5\mu m$	$1\mu m$	$2\mu m$	

The simulation results are shown in the following Fig. 4.30 and Fig. 4.31.

Figure 4.30: Single-bit input signal of the synchronizer.

Finally the layout of the synchronizer is shown in Fig. 4.32.

4.3.8 Pipelined Analog-to-Digital Converter

The 8-bit analog-to-digital converter is designed with 80 MHz sampling frequency. The ADC consists of one sample-and-track block, seven MDAC blocks, one comparator to generate

Figure 4.31: Single-bit output signal of the synchronizer.

LSB, and one synchronizer to align digital outputs, as shown in Fig. 4.33.

Figure 4.32: Layout of the synchronizer.
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Figure 4.33: Block diagram of the pipelined ADCs.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this project a complete voltage mode CMOS image sensing system has been designed based on 30 frames/s. Firstly the characteristics of photodiodes have been introduced in detail. At the same time the work principle and differences of CCD and CMOS image sensors have been presented. Secondly CMOS image sensors have two categories, and this project focused on the photodiode active pixel sensors. In Chapter 2 the analysis of using APS structure has been given. Thirdly this project used the correlated double sampling circuit to reduce Fixed Pattern Noise which acts as the most critical noise source in CMOS image sensors. The correlated double sampling circuit obtains signal and reset voltage through two consecutive sampling periods. In order to correspond with the analog-to-digital converter in the next stage, the subtraction and level shift circuit has been designed. Finally a 8-bit 80MHz pipelined analog-to-digital converter has been finished. In this project the CMOS image sensing system adopted the column A/D to relax the speed requirement of A/D operation. The A/D included the track-and-hold circuit, the digital-to-analog converter, the comparator, the two-stage operational amplifier, the residue amplifier, and the synchronizer. To solve the problems of ON-resistance and charge injection in the track-and-hold circuit, this project employed the bootstrap switch driver. The 68dB gain and phase margin of 62° ensure the accuracy and stability of operational amplifier. The synchronizer circuit aligned the 8-bit digital output signals.

All the simulation results and layouts were completed in TSMC-0.18 μm CMOS technology with supply voltage 1.8V.

5.2 Future Work

CMOS image sensors benefit from technology scaling by reducing pixel size, increasing resolution, and integrating more analog and digital circuits on the same chip with sensors. In deep micron CMOS technologies, the use of shallow junction and high doping result in a low photoresponsivity. Thin gate oxide causes a high dark current. Furthermore in-pixel transistor leakage becomes a significant source of dark current. Indeed in a standard process, dark current due to reset transistor off-current and the follower transistor gate leakage current can be higher than the diode leakage itself. As a result of these major problems, process modifications are mandatory [32].

Another idea that takes advantage of scaling is increasing pixel-level processing by adding more transistors to each pixel. Image sensors explore architecture with per-pixel ADCs. This architecture offers several advantages over current analog pixel architectures such as APS including, better technology scaling due to reduced analog circuit performance demands, the elimination of column temporal noise and FPN, and high speed readout.

Several researchers have recently shown that high frame rate can also benefit still and video rate imaging. Using the high frame rate to over-sampling the scene obtains more accurate information about illumination and motion.

Of course the resolution of ADC directly affects the image quality of image sensors. Increasing the performance of ADC is the one of critical challenges in image sensing systems.

Bibliography

- [1] B. Koren, *Photodiodes*, Advanced Photonix, Aug. 2000.
- [2] *What's the Difference between CMOS Sensors and CCD Ones*, Webcam Corp., April 1997.
- [3] P. Noble, "Self-scanned image detector arrays," *IEEE Trans. Electron Devices*, vol. 5 No. 8, pp. 583-586, Dec. 1968.
- [4] S. Mendis, B. Pain, S. Kemeny, R. Gee, Q. Kim and E. Possum, "CMOS active pixel image sensor for highly integrated imaging systems," *IEEE Journal of Solid-State Circuits*, vol. 32, No. 2, pp. 187-197, Feb. 1997.
- [5] H. Tian, X. Liu, S. Lim, S. Kleinfelder, and A. Gamal, "Active pixel sensors fabricated in a standard 0.18 μ m CMOS technology, "in *Proc. of SPIE*, vol. 4306, pp. 441-449, May 2001.
- [6] O. Yadid-Pecht, R. Ginosar, and Y. Diamand, "A random access photodiode array for intelligent image capture," *IEEE J. Solid-State Circuits*, vol. 38, No. 8, pp. 1772-1780, Aug. 1991.
- [7] B. Lin, S. Huang, C. Lai, and Y. King, "A high dynamic range CMOS image sensor design based on two-frame composition," in *Proc. IEEE SOC Conference* pp. 389-392, 2003.

- [8] Y. Degerli, F. Lavernhe, P. Magnan, and J. Farre, "Temporal noise in CMOS image sensors for low-light levels," *IEEE Trans. Electron Devices*, vol. 47, No. 5, pp. 949-962, May 2000.
- [9] A. Gamal and H. Eltoukhy, "CMOS image sensors," *IEEE Circuits & Devices Magazine*, vol. 21, No. 3, pp. 6-20, May-June 2005.
- [10] I. Fujimori, C. Wang, and C. Sodini, "A 256x256 CMOS differential passive pixel imager with FPN reduction techniques," *IEEE Journal of Solid-State Circuits*, vol. 35, No. 12, pp. 2031-2037, Dec. 2000.
- [11] H. Tian., B. Fowler, and A. Gamal, "Analysis of temporal noise in CMOS APS," *Information Systems Laboratory, Stanford University, CA 94305 USA*, 1998.
- [12] A. Gamal, B. Fowler, H. Min, and X. Liu, "Modeling and estimation of FPN components in CMOS image sensors," *Information System Laboratory, Stanford University, CA 94305 USA*, 1998.
- [13] B. Dierickx, G. Meynants, and D. Imec, "Offset-free offset correction for active pixel sensors," *IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, pp. 34-38, June 1997.
- [14] B. Fowler, A. Gamal, and D. Yang, "A method for estimating quantum efficiency for CMOS image sensor," in *Proc. of SPIE*, vol. 3301, pp. 178-185, Apr. 1998.
- [15] K. Yonemoto and H. Sumi, "A CMOS image sensor with a simple fixed-pattern-noise-reduction technology and a hole accumulation diode," *IEEE J. Solid-State Circuits*, vol. 35, No. 12, pp. 2038-2043, Dec. 2000.
- [16] M. White, D. Lampe, F. Blaha, and I. Mack, "Characterization of surface channel CCD image arrays at low light levels," *IEEE J. Solid-State Circuits*, vol. 9, No. 1, pp. 1-12, Feb. 1974.

- [17] J. Hynecek, "A new device architecture suitable for high-resolution and high performance image sensors," *IEEE Trans. Electron Devices*, vol. 35, No. 5, pp. 646-652, May 1998.
- [18] N. Tanaka, "A 310k pixel bipolar image (BASIS)," *IEEE International*, Vol. 2, No. 15-17, pp. 96-97, Feb. 1989.
- [19] Z. Zhang, X. Yuan, and Y. Huang, "CMOS correlated-double-sampling and hold structure based on novel dynamic source-follower for large format infrared focal-plane-array," *Semicond. Sci. Technol*, vol. 18, pp. 680-684, June 2003.
- [20] M. Sakakibara, S. Kawahito, D. Handoko, N. Nakamura, H. Satoh, M. Higashi, K. Mabuchi, and H. Sumi, "A high-sensitivity CMOS image sensor with gain-adaptive column amplifiers," *IEEE J. of Solid-State Circuits*, vol. 40, No. 5, pp. 1147-1156, May 2005.
- [21] *A/D Converter Definition of Terms*, National Semiconductor, Jan. 2000.
- [22] D. Goes, J. Vitasl, and J. Franca, *Systematic Design for Optimization of Pipelined ADCs*, Kluwer Academic Publishers, July 2001.
- [23] B. Black, *Analog-to-Digital Converter Architectures and Choices for System Design*, Analog Devices, 1999.
- [24] H. Kobayashi, M. Zin, K. Kobayashi, H. San, H. Sato, J. Ichimura, Y. Onays, Y. Takahashi, N. Kurosawa, Y. Kimura, Y. Yuminaka, K. Tanaka, T. Myono, and F. Abe, "High-speed CMOS track/hold circuit design," *Analog Integrated Circuits and Signal Processing*, vol. 27, No. 1-2, April-May 2001.
- [25] V. Passche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*, Springer, May 2003.
- [26] B. Razavi, *Principle of Data Conversion System Design*, IEEE Press, 1994.

- [27] S. Hamed-Hagh and C. Salama, "A 10-bit 50M sample/s, low power pipelined A/D converter for cable modem application," in *IEEE Proc. of International Symposium on Circuits and System*, vol. 1, pp. 424-427, May 2001.
- [28] S. Ardalan, *A 1.2V 8-bit 100MHz Pipelined Analog-to-digital Converter*, M.Sc thesis, Ryerson University, 2002.
- [29] J. Ho and H. Luong, "A 3-V 1.47mW, 120MHz comparator for used in a pipelined ADC," in *Proc. of IEEE Asia Pacific Conf. On CAS*, pp. 413-416, Nov. 1996.
- [30] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, Aug. 2001.
- [31] J. Rabaey, *Digital Integrated Circuits*, Prentice Hall, Dec. 1995.
- [32] E. Fossum, "Active pixel sensors: are CCDs dinosaurs?," in *Proc. of SPIE*, vol. 1900, pp. 2-14, July 1998.