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Adaptive digital predistortion to linearize nonlinear distortion in radio-over-fiber links

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ADAPTIVE DIGITAL PREDISTORTION TO LINEARIZE NONLINEAR DISTORTION IN RADIO-OVER-FIBER LINKS

By

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Bachelor of Computer Engineering

Kwangwoon University

Seoul, Republic of Korea, 1997

A Thesis

Presented to Ryerson University

in Partial Fulfillment of the

Requirements for the Degree of

Master of Applied Science

in the Program of

Electrical and Computer Engineering

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ABSTRACT

Adaptive Digital Predistortion to Linearize Nonlinear Distortion in Radio-over-Fiber Link

Hyunsuk Moon, Master of Applied Science, ELCE, Ryerson University 2005

The applications of Radio-Over-Fiber (ROF) links are widely used in wireless communications. However, due to the nonlinear characteristics of the link distortion will be introduced at the output of the link. As a result, unwanted frequencies and signals end up being delivered by an antenna. In the thesis, a technique of adaptive digital predistortion is presented. This complex gain predistortion technique requires that no detailed knowledge of the link characteristics and supports tracking of the modifications and drifts in the link characteristic. A prototype of this predistortion system is designed and implemented on a Field Programmable Gate Array (FPGA). Experiment results show that amplitude and phase nonlinearity of the ROF link are compensated with the system. The experiments demonstrated that this system shows promising results and that good compensation of distortion is achieved.

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CHAPTER 1

INTRODUCTION

1.1 Overview

Over the past decade there have been great advances in the areas of wireless and optical fiber communications. As wireless communications shift from voice to multimedia, existing users desire trustworthy and cost effective communication systems that offer anytime, anywhere, any media they want. Moreover, the increasing numbers of subscribers demand more capacity in an already restricted bandwidth. One solution to the problem is to combine the high capacity of optical networks with the flexibility of radio networks.

The use of ROF technology enables optical networks to be more easily combined with the flexibility and mobility of wireless access networks at lower costs. The ROF link concept involves transporting information over optical fiber by modulating light with radio signals either at the carrier frequency or at an intermediate frequency. The ROF link system offers low signal attenuation in the fiber, improved coverage and system performance, enhanced capacity, and reduced complexity due to the centralized processing of Radio Frequency (RF) signals [1].

The performance of an ROF link system can be severely reduced, however, when the wireless link component of the system is connected in series with the ROF link, particularly under multi-user conditions. The major concern becomes the nonlinear distortion of the ROF link, mainly due to the electrical to optical conversion. Additional sources of distortion could

include fiber dispersion and attenuation, internal noise and the nonlinearity of the RF amplifier. Furthermore, fading and shadowing in the wireless link and path loss, also affects the nonlinearity of ROF links [2]. In order to have a large linear region, these nonlinear distortions must be compensated.

1.2 Contributions

The objective of the thesis is to explore the linearization of ROF links using the adaptive digital predistortion technique and to implement this technique on an FPGA. The overall research contributions that led to this thesis include:

- Design of an adaptive digital predistorter that compensates amplitude and phase nonlinearity of the ROF links
- Implementation of this design on an FPGA and analysis of its performance in terms of various input signals and adaptation coefficients
- Design and implementation of a hardware model for an adequate ROF link
- Examination of the manner in which the performance of the system can be affected by the abrupt changes of the input signal powers and link characteristics

1.3 Organization of Thesis

This thesis is organized as follows: Chapter 2 gives an overview of the ROF link and its nonlinearity and also looks at the COordinate Rotation DIGital Computer (CORDIC) algorithm theory. Chapter 3 describes the research being conducted to solve the nonlinearity problem for ROF links and explains the predistortion technique. Chapter 4 presents the adaptive digital predistortion system that was created as part of this thesis and proposes a new adaptive digital predistortion technique. Chapter 5 provides details on the predistorter, presents the actual hardware implementation of the adaptive digital predistorter and also

provides information concerning performance and resource utilization of the FPGA-based design. Chapter 6 presents the results of various performance tests run in real environments. Finally, Chapter 7 summarizes this thesis and discusses the possibilities for future research.

CHAPTER 2

BACKGROUND

2.1 Radio-over-Fiber Link

An ROF link is an analog optical link that transmits modulated RF signals from a Central Site (CS) to a Remote Site (RS) or vice versa. For example, if the application area was a wireless Local Area Network (WLAN), the CS would be the Base Station while the Radio Access Point would work as the RS as in shown in Figure 2.1 [2].

Figure 2.1: ROF link System

ROF link systems can be used to transport modulated intermediate frequency (IF), or modulated RF signals. The electrical signals must be available at the input of the ROF link

and are then transferred over the optical fiber link to a radio access point. At the radio access point the data is transformed back into electrical form by the photo diode and then radiated by antennas. In many current systems these ROF link systems are also designed to perform added radio-system functionalities, such as data modulation and signal processing [3][4].

The main advantage of ROF link systems is the use of simpler radio access points by concentrating most of the costly and complex equipment at a base station. Other benefits include:

- Transmission distances are improved several times and the required transmission powers are reduced significantly by transmitting signals in the optical form.
- The large optical bandwidth enables the ROF link system to perform high speed signal processing that may be more complex in electronic systems.
- Easy installation and maintenance is possible [5] when complex and expensive equipment is kept at the base stations.

2.1.1 Laser Diode Transmitter

A main element of an ROF link system is the laser diode, which converts an electrical current into light. Characteristics of the laser diode strongly affect the output performance of the ROF link. In general, a laser diode has several inherent attractive properties for fiber optics. First, laser diodes are small and have high radiance. They also have long life and can be modulated at high speeds. Usually, laser diodes are constructed of GaAlAs (gallium aluminium arsenide) for short-wavelength devices. Long-wavelength devices generally incorporate InGaAsP (indium gallium arsenide phosphide) [6].

Nonlinear distortion of the laser diode is the biggest concern in the ROF link. Nonlinearity of a laser diode occurs when impulsive and stimulated emission mechanisms are joined with gain compression characteristics [7]. Nonlinearity in lasers causes harmonic distortion in the analog signal that is transmitted over the analog fiber optic link.

A laser diode is classified by dynamic and static nonlinearity. The dynamic nonlinearity is defined through well-known laser rate equations. Although it is mainly frequency dependant, it can be frequency independent when the frequency of operation is at least five

times less than the laser resonance frequency. Rate of change of photons can be represented by:

$$\frac{d\Phi}{dt} = Cn\Phi + R_{sp} - \frac{\Phi}{\tau_{ph}} \quad (2.1)$$

And, rate of change of electrons can be represented by:

$$\frac{dn}{dt} = \frac{J}{qd} - \frac{n}{\tau_{sp}} - Cn\Phi \quad (2.2)$$

where n is number of electrons, Φ is number of photons, C is Einstein's Coefficient, τ_{ph} is photon lifetime, R_{sp} is rate of spontaneous emission, τ_{sp} is spontaneous recombination lifetime, J is injection current density, q is the electron charge, and d is laser cavity [7].

Static nonlinearity is defined through the use of a third order polynomial equation, which is given below

$$P_{optical}(t) = P_o [1 + A_1 m s(t) + A_2 m^2 s^2(t) + A_3 m^3 s^3(t)] \quad (2.3)$$

where $s(t)$ is input electrical signal, P_o is average optical power, m is optical modulation index, A_1 , A_2 , and A_3 are device dependent nonlinear coefficients [7].

Although the analysis of dynamic nonlinearity would be a significant task under transient conditions, it is not a main concern in data communications because only steady state conditions are considered. Therefore, static nonlinearity is of greater interest.

Leakage current and axial hole burning can also influence laser diode nonlinearity. As the injected current grows the leakage current increases. Axial hole burning results when the optical power density along the length of the laser is non-uniform. All of the causes can affect the linearity of the laser diode. Thus, lasers require a method of stabilizing the threshold to achieve maximum performance.

2.1.2 Single-Mode Optical Fiber

Optical fiber refers to the medium associated with the transmission of information in the form of light along a glass or fiber. Thanks to the technical progress of fiber manufacturing, optical fiber carries much more information than conventional coaxial cable and is subject to far less electromagnetic interference [6]. However, optical fiber cable is costly and has a potential hazard to break more easily than traditional coaxial cables.

The main advantages of optical fiber include:

- Resistance to external electromagnetic and light interference
- Less attenuation of the signal
- High bandwidth

There are two main concerns with a single-mode fiber; attenuation and chromatic dispersion. Attenuation is typically 0.5dB/kM [2]. Chromatic dispersion can be described as a transfer function of the fiber given by Equation (2.4), where α is the dispersion coefficient, l is fiber length, $(f - f_o)$ is the RF frequency and f_o is the optical carrier frequency.

$$H(f) = e^{-jal(f-f_o)^2} \quad (2.4)$$

If the frequency is less than a few GHz, chromatic dispersion is irrelevant based on the quantitative analysis of Equation (2.4). The fiber can thus be modeled as an all pass filter with minor attenuation, which is length dependent.

2.1.3 Photo Diode and Amplifiers

The photo diode is an electronic component which converts optical power into electrical current. It is composed of a p-n junction consisting of heavily doped p-type and n-type materials. A small intrinsic region also exists between the two material types [8].

Photo diodes can be used in either zero bias or reverse bias. In zero bias, light falling in the diode causes a voltage to develop across the device, leading to current in the forward bias direction, referred to as the photovoltaic effect. In reverse bias, the diodes usually have

extremely high resistance. This resistance is reduced when light of an appropriate wavelength shines on the junction. Therefore, a reverse biased diode can be used as a detector by monitoring the current running through it. Circuits based on this effect are more sensitive to light than ones based on the photovoltaic effect.

Due to the photon to electron conversion the photo diode generates several internal noise sources, which are imposed on the signal. These noise sources include thermal noise, shot noise, and dark current noise [6]. Due to the operation of resistive elements thermal noise results in temperature elevation. Thermal noise power is described by:

$$\langle i_t^2 \rangle = \frac{4k_B T B}{R_L} \quad (2.5)$$

where k_B is Boltzman's constant, T is the temperature, R_L is the load resistance, and B is the signal bandwidth. It shows noise power rises as the temperature is increased.

Also, shot noise is present because of random generation of electrons in the diode. The shot noise power is defined by the following equation:

$$\langle i_d^2 \rangle = 2qI_p B \quad (2.6)$$

where q is the charge of an electron and I_p is the dc current at the output of the diode. This equation shows that noise power is proportional to the dc current which includes optical power.

To obtain better results, the signal power from the photo diode can be boosted before it transfers to the system. For this purpose, a power amplifier usually follows the photo diode. However, an amplifier can introduce additional nonlinear distortion. Amplifier linearization is a critical issue and the focus of extensive research. [9] [10].

2.1.4 ROF Link Nonlinearity

There are generally two sources of nonlinearity, namely amplitude to amplitude distortion (AM/AM) and amplitude to phase distortion (AM/PM) [11]. Memory effects also take place in the link. Figure 2.2 shows measured responses of a typical ROF link, where the output RF power from the link is plotted versus the input RF power into the link [2].

Figure 2.2: Transfer characteristics of an ROF link [2]

2.1.4.1 AM/AM distortion

The ideal ROF link is linear for all input powers. Nonetheless, a practical ROF link has a maximum output power, which will restrict the output power. In reality, as the limit is gradually approached the apparent gain of the link decreases with increasing input power. The AM/AM distortion is created by this variation in the gain of the ROF link across different input powers.

The simulated 16-QAM (quadrature amplitude modulation) constellation graph based on AM/AM distortion is shown in Figure 2.3. The distortion in the constellation is not due to

noise, as this signal contained no noise. The 'X' shows the desired constellation point location. The inner four points are dispersed around the ideal point while the outer points are compressed with the corner points showing the most compression.

Figure 2.3: Simulated 16-QAM constellations with AM/AM distortion

2.1.4.2 AM/PM distortion

AM/PM distortion introduced into the ROF link results from amplitude dependent carrier delay and is dependent on input phase. AM/PM distortion refers to a change in the phase between the input and output signal of the ROF link. Figure 2.4 shows the signal constellation of phase distortion. This distortion tends to skew or twist the constellation through angles that depend on the magnitude of the signal.

Figure 2.4: Simulated 16-QAM constellations with AM/PM distortion

2.1.4.3 Memory Effect

If an ROF link introduces a phase distortion then memory is present. These memory effects are generally described as the envelope frequency dependence of the link. The main difference between a system without memory and a system with memory is that nonlinearities generate new spectral components because the output signal is not only a function of the instantaneous input signal, but also a function of previous input values. However, if the time constants of the memory are smaller than the maximum envelope frequency, the system can be considered a quasi-memory-less system [12].

Memory effects are usually caused by time constants in the biasing circuit or are due to an impedance mismatch with the link. The AM/AM and AM/PM characteristics vary for different symbol rates if the time constants of the memory are larger than the inverse of the maximum envelope frequency.

2.2 CORDIC Algorithm

The CORDIC algorithm was developed by Jack E. Volder in 1959 for the calculation of trigonometric functions, multiplication, division, and conversion between binary and mixed radix number systems. The CORDIC algorithm provides an iterative method of performing vector rotations by arbitrary angles using only shift and add operations [13] [14].

The basic idea of the CORDIC algorithm is to perform the rotation of a point (X, Y) by an angle ϕ . The coordinates for the new point (X_{new}, Y_{new}) are

$$\begin{aligned} X_{new} &= X \cos(\phi) - Y \sin(\phi) \\ Y_{new} &= Y \cos(\phi) + X \sin(\phi) \end{aligned} \quad (2.7)$$

Figure 2.5 shows the rotation of a vector (X_{new}, Y_{new}) by the angle ϕ .

Figure 2.5: the rotation of a vector (X_{new}, Y_{new}) by the angle ϕ

The individual equations for X_{new} and Y_{new} can be rewritten as (2.8)

$$\begin{aligned} X_{new} &= \cos(\phi) * (X - Y \tan(\phi)) \\ Y_{new} &= \cos(\phi) * (Y + X \tan(\phi)) \end{aligned} \quad (2.8)$$

Multiplication by the tangent term can be simplified to a shift operation if the rotation angles are limited so that $\tan(\phi) = \pm 1/2^n$. Furthermore, if these rotations are performed iteratively and in both directions, every value of $\tan(\phi)$ can be represented. With $\phi = \arctan(1/2^n)$ the cosine term can also be simplified and since $\cos(\phi)$ is equal to $\cos(-\phi)$, it is a constant for a fixed number of iterations. This iterative rotation can now be expressed as

$$\begin{aligned} X(n+1) &= P(n) * (X(n) - d(n) \cdot \frac{Y(n)}{2^n}) \\ Y(n+1) &= P(n) * (Y(n) + d(n) \cdot \frac{X(n)}{2^n}) \end{aligned} \quad (2.9)$$

where $P(n) = \cos(\arctan(1/2^n))$ and $d(n) = \pm 1$. The product of $P(n)$ represents P factor.

$$P = \prod_{n=0}^{\infty} \cos(\arctan(\frac{1}{2^n})) \quad (2.10)$$

This P factor can be calculated in advance and applied elsewhere in the system. A good way to implement the P factor is to initialize the iteration rotation with a vector of length $|P|$ which compensates the gain inherent in the CORDIC algorithm.

Equation (2.9) can be simplified to the basic CORDIC equations;

$$\begin{aligned}
X(n+1) &= X(n) - d(n) \cdot \frac{Y(n)}{2^n} \\
Y(n+1) &= Y(n) + d(n) \cdot \frac{X(n)}{2^n}
\end{aligned} \tag{2.11}$$

The direction of each rotation is defined by $d(n)$ and the sequence of all $d(n)$'s determines the final vector. This yields to a third equation which acts as an angle accumulator and keeps track of the angle already rotated. Each vector can be described by either the vector length and angle or by its coordinates X and Y . Following this incident, the CORDIC algorithm is capable of determining the direction of rotation using both the rotation mode and the vectoring mode. Both methods initialize the angle accumulator with the desired angle $Z(0)$. The rotation mode determines the right sequence as the angle accumulator approaches to zero while the vectoring mode minimizes the Y component of the input vector.

The angle accumulator is defined by

$$Z(n+1) = Z(n) - d(n) \cdot \arctan\left(\frac{1}{2^n}\right) \tag{2.12}$$

where the sum of an infinite number of iterative rotation angles equals the input angle ϕ

$$\phi = \sum d(n) \cdot \arctan\left(\frac{1}{2^n}\right) \tag{2.13}$$

The values of $\arctan(1/2^n)$ can be stored in a small lookup table or hardware depending on the method of implementation. Since the question is in which direction to rotate rather than whether or not to rotate, $d(n)$ is sensitive to the sign of $z(n)$. Therefore $d(n)$ can be described as

$$d(n) = \begin{cases} -1, & \text{if } z(n) < 0 \\ +1, & \text{if } z(n) \geq 0 \end{cases} \tag{2.14}$$

Equation (2.14) completely describes the CORDIC algorithm in rotation mode. Note that as described, the CORDIC method performs rotations only within $-\pi/2$ and $\pi/2$. This limitation comes from the use of 2^0 for tangent in the first iteration. However, since a sine wave is symmetric from quadrant to quadrant, every sine value from zero to 2π can be represented by reflecting and/or inverting the first quadrant appropriately.

This algorithm can have two general forms: driving Z to zero and driving Y to zero, expressed as

$$\begin{aligned} [X_{new}, Y_{new}, Z_{new}] = \\ [P(X \cos(Z) - Y \sin(Z)), P(Y \cos(Z) + X \sin(Z)), 0] \end{aligned} \quad (2.15)$$

and

$$[X_{new}, Y_{new}, Z_{new}] = [P\sqrt{X^2 + Y^2}, 0, Z + \arctan(\frac{Y}{X})] \quad (2.16)$$

In equation (2.15) if the variables are substituted as follows, sine and cosine values can be calculated.

$$\begin{aligned} X = \frac{1}{P} = K \cong 0.60725 \quad Y = 0 \quad Z = \phi \\ [X_{new}, Y_{new}, Z_{new}] = [\cos \phi, \sin \phi, 0] \end{aligned} \quad (2.17)$$

It follows then that after calculating $\cos \phi$ and $\sin \phi$ and multiplying with the amplitude, polar to rectangular conversion can be performed.

Also, Equation (2.16) can be used to obtain amplitude and phase by substituting the variables as below.

$$\begin{aligned} X = X \quad Y = Y \quad Z = 0 \\ [X_{new}, Y_{new}, Z_{new}] = [P\sqrt{X^2 + Y^2}, 0, \arctan(\frac{Y}{X})] \end{aligned} \quad (2.18)$$

Using this case, rectangular to polar conversion (R-to-P) is possible. The CORDIC algorithm performs the multiplication as part of the rotation operation, and therefore eliminates the need for a pair of explicit multipliers. The output of the rotator is scaled by rotator gain.

CHAPTER 3

LINEARIZATION TECHNIQUES AND PREDISTORTION THEORY

3.1 LINEARIZATION TECHNIQUES

Various researchers propose alternative approaches for characterizing and solving the problem of nonlinear distortion. These approaches can be categorized into several methods.

3.1.1. Modeling Laser Diode

For this method, several authors have attempted to directly model the laser by solving the laser equations and using equivalent circuit models [15] [16]. Using these equations, several linearization methods such as “post nonlinearity recovery block” [17], “feed forward compensation” [18], and “electrical pre-distortion” [19] [20] were presented. These solutions would be perfect if accurate physical parameters of the device were known.

In reality however, these device parameters are device dependent. For instance, large differences have been presented in the modulation response of similar distributed feedback lasers [21]. In addition, other unknown nonlinear components in the link may also have to be adequately modeled if these approaches are used.

Figure 3.1 shows a diagram of the feed forward technique.

Figure 3.1: Feed forward technique

3.1.2 Dynamic Range Enhancement Technique (DRET)

This DRET uses variable attenuators to control the laser diode input signal level [22]. If the input power exceeds a defined threshold, the variable attenuator reduces the input signal level to the threshold level. At same time a control signal is transmitted to the receiving end of the link where an attenuator is used to restore the signal back to the correct level. Thus, an overall constant link gain independent of input level is maintained. Figure 3.2 illustrates this technique.

Figure 3.2: Block diagram of DRET

Due to the variations in the timing of stimulated photon generation, the phase response of the laser is nonlinear even in the so-called linear region. Additional linear amplification elements are also required at the receiver.

3.1.3 Cartesian Loop Feedback

The Cartesian Loop Feedback method uses the error signal which is combined with the input to the ROF link [23]. A sample of the output is quadrature down-converted to analog baseband signals. The sample output is subtracted from the desired signal and the result is delivered to the link. Figure 3.3 shows a diagram of Cartesian loop feedback. However, the delay of the signal traveling through the ROF link and frequency conversions limits the bandwidth of the scheme.

Figure 3.3: Cartesian loop feedback

3.1.4 Adaptive Asymmetric Linearization

Adaptive Asymmetric Linearization implements a high order adaptive filter for nonlinearity compensation [2]. This approach requires separate pre-compensation and post-compensation for amplitude and phase compensations. Even though this scheme shows adequate linearization results, the order of the filters must be adequate for a given dynamic range. The adaptive asymmetric linearization technique is presented in Figure 3.4.

Figure 3.4: Adaptive asymmetric linearization technique

3.1.5 Several Other Methods

Another approach involves allocating frequency channels to the ROF link in such a way as to prevent the cross-modulation products from overlapping [24]. However, this will result in reduced trunking capacity. Also suggested is the use of more than one remote access point per base station [25], which, unfortunately, would significantly increase infrastructure cost. Another work suggests canceling the nonlinearity similarly to the way multi-user interference is cancelled in code division multiple access (CDMA) schemes [26]. This, however, would further increase the complexity of already complex CDMA receivers. Furthermore, none of these techniques solves the emission problem.

3.2 Predistortion Theory

The basic idea of predistortion is straightforward. Before feeding the input signal to a nonlinear component such as an ROF link, intentional distortion of the signal is processed to affect a linear output from the link. A basic system description is shown in Figure 3.5.

Figure 3.5: Basic system description of predistortion technique

This is realized by designing the predistorter to be as close as possible to the inverse of the ROF link characteristics. If the transfer functions of the two systems are $P(X)$ and $R(Y)$, the cascaded system response will be

$$Z = R(Y) = R(P(X)) \quad (3.1)$$

If $R(P(X))$ is close to X , a linear response has been achieved by letting two nonlinear systems, the predistorter and ROF link, work together.

This technique can be established by two methods; analog predistortion and digital predistortion. Although several analog techniques have been presented [20], including rapid digital electronics development and digital signal processing (DSP), the interest in digital predistortion has been growing in recent years.

Digital predistortion predicts the required correction using past knowledge of the link characteristics in contrast to using feedback from the current signal as with analog predistortion. The predistortion prediction adjusts much like an equalizer to minimize the error between the input signal and the output signal of the link.

There are many variations of digital predistortion systems but all have the same basic principle. The RF signal is measured and a memory is addressed depending on the signal. The memory contains information of correction to the signal in order to achieve a suitable, predistorted signal as input to the link.

Predistortion can be introduced by static or adaptive algorithms. Although static algorithms are simple, they are sensitive to link characteristic variations. Adaptive algorithms are more complex since feedback line is required to find the error and feed the algorithm to adapt to variations [27].

Since the characteristics of the ROF link should be linear to all the input signals, if the gain of the link is one, it becomes

$$Z = R(Y) = R(P(X)) = X \quad (3.2)$$

which provides the following result:

$$P(X) = R^{-1}(X) \quad (3.3)$$

Thus, the desired function for the predistorter is the inverse of the ROF link function.

To compensate amplitude error to zero,

$$|Z| = |X| \quad (3.4)$$

For the phase

$$\angle Z = \angle Y + \phi(|Y|) = \angle X + \angle P(|X|) + \phi(|P(X)|) \quad (3.5)$$

where ϕ is the AM/PM characteristics of the link. Therefore, if phase error

$$\angle Z - \angle X = \angle P(X) + \phi(|P(X)|) \quad (3.6)$$

is equal to zero, it becomes

$$\angle P(X) \Rightarrow -\phi(|P(X)|) \quad (3.7)$$

Thus the phase shift introduced by the link is solved.

CHAPTER 4

SYSTEM OVERVIEW AND ADAPTIVE DIGITAL PREDISTORTER

4.1. System Overview

Figure 4.1 shows the system block diagram of the system that corrects ROF link nonlinearity.

Figure 4.1: Adaptive digital predistortion system overview

In the adaptive digital predistortion system, the ROF link is preceded by the predistorter in order to acquire mapping between the input baseband signal and the received output baseband signal.

After random QAM signal generation, the Cartesian signals X are sent to the adaptive digital predistorter in digital form through a pulse shaping filter and an analog-to-digital converter (ADC) in the downlink. The adaptive digital predistorter generates predistorted digital Cartesian signals Y based on the input signals, and the signals are then reconverted to analog form by the digital-to-analog converter (DAC). These analog signals are quadrature-modulated to RF and sent to the ROF link. At the other end of the link, digitized baseband Cartesian output signals Z are obtained and demodulated through a quadrature demodulator and an ADC. Finally, these signals are sent back to the predistorter for comparison with the input signals.

4.2. Adaptive Digital Predistorter

Figure 4.2 shows a diagram of the proposed adaptive digital predistorter. In this work, a level dependent complex gain predistortion technique is applied to achieve predistortion by manipulating polar forms of signals and LUT coefficients [10].

Figure 4.2: Proposed adaptive digital predistorter

Here, the polar forms of X and Z are obtained by R-to-P converters from the input signals and the received output signals using the CORDIC algorithm [13].

Next, the address generator produces an index address of the LUT based on the input signal amplitude. Some authors have suggested that by biasing the indexing on the square of input signal amplitude instead of input signal amplitude itself, a higher proportional number of LUT levels are accomplished where nonlinear components like power amplifiers have their most nonlinear amplitude behavior [28]. However, because the ROF link has large phase distortion from low input power level, the input signal amplitude for indexing was applied.

After generating the index address, the input signal is stored in the first-in-first-out (FIFO) memory with the address. The FIFO holds the input signals and addresses until the received output signals Z come into the predistorter. The stored data is then transferred to the algorithm block.

The generated address from the address generator is sent to the LUT and the stored predistortion LUT coefficients are obtained. These LUT coefficients are added to the input signal, which is in polar form, and the added signal is sent to the output in the predistorter output block. Finally, this polar form of the output signal is converted back to rectangular form by a P-to-R converter. In addition, the predistorter generates a signature signal for delay estimation after sending the output signal during the training period.

In order to simultaneously compare the input signal and the received output signal in the predistorter, a delayed version of the input signal is required. Compensation for this delay must be solved if the adaptation algorithm block is to compare the input signal and the received output signal correctly. In this work, the signature method is applied for delay compensation.

In the adaptation algorithm block, LUT coefficients are calculated using an adaptive algorithm [10]. Even though many adaptive algorithms are proposed, the linear convergence method offers reasonable speed and computational load. This adaptive algorithm compares the input and the output signals separately in amplitude and phase and produces the LUT coefficients.

In as much as the ROF link has phase and amplitude distortions that depend on the total input power of the wireless system, and because the number of users continuously varies, the

individual amplitude of each carrier could fluctuate in wireless systems [29]. Thus, the output amplitude and phase of each sub-carrier are distorted independent of their respective amplitude. In this paper, however, only single-user conditions were considered because of the difficulty in estimating the total input power under multi-user conditions.

CHAPTER 5

IMPLEMENTATION

5.1 General Design Overview

The hardware available for the implementation was the Memec Embedded Develop Board. This board provides a complete solution for developing prototype designs and applications based on the Xilinx Virtex-II FPGA family [30]. The Vertex-II FPGA, XC2V1000-4FG456C on the board, the 456 fine-pitch ball grid package, provides fast, customizable, and flexible resources. The high gate density and large number of user I/Os allow complete system solutions to be implemented in the advanced platform FPGA. The advanced features of the Virtex-II FPGA family fit demanding, high-performance applications such as DSP systems. The P160 prototype board was used to connect the ADC to the main system development board, which was then connected to the logic analyzer. The P160 prototype module provides a useful expansion, probe, and prototype feature in a small, low cost daughter card form-factor.

The available ADC supports the 8-bit 2's complement 2 channel. It supports up to 180,000 samples per second per channel. The ADC was implemented on a Microchip DSPIC30F4012 digital signal controller [31]. Although system speed limit comes from the speed of the ADC, it does not necessarily impose a further limit on the performance of the system.

Before FPGA implementation, the data format must be decided. In the system, input and output signals are 16-bit 2's complement formats for both inphase (I) and quadrature (Q). These types of signals are changed to 20-bit 2's complement fixed point formats after polar conversion. Therefore, all signal types in the predistorter are 20-bit signals. The first 16 bits are integer part and the last 4 bits are fractional part.

First, the adaptive digital predistortion system was simulated in Matlab in order to ensure the correct working of the concepts developed. The working system was then coded in VHDL under a Xilinx ISE 6.3 environment [32]. All the functional modules of the system have been designed as synchronous circuits, separately verified with test-bench and integrated.

5.2 VHDL Implementation

5.2.1 Top Module

Figure 5.1 shows a top module for the system implementation. The module consists of an input signal controller, the predistorter, and the ROF link hardware model.

Figure 5.1: Top Module

The input signal generator produces input signals I_{in} and Q_{in} from the ADC output by multiplying $Signal_Power$, and allows the adaptive digital predistorter to generate predistorted I and Q signals. The ROF link model produces distorted signals I_{out} and Q_{out}

based on the input signals and transmits the signals to the predistorter for adaptive predistortion.

Signal *ENA* comes from the ADC whenever input signals *SIGIN_I* and *SIGIN_Q* are valid. Also, signal *START* is connected with an external switch and activated when the adaptation process starts. Signal *RSTn* initializes all the registers and internal signals.

Detailed block descriptions are presented in the following sections.

5.2.2 Input Signal Controller

The input signal controller handles communication with the outer system through the external ports. It is also used to manipulate the input signals and transfer the signals to the adaptive digital predistorter.

Figure 5.2: Input Signal Controller

Since the function generator generates analog baseband signals between 1 V and -1 V and the ADC generates two 8-bit 2's complement I and Q signals from the baseband signals, this

controller needs to modify the signals with various input powers and expand the signals to 16 bits. Figure 5.2 shows the schematic diagram of the input signal controller.

Four-bit *SIGNAL_POWER* input signals are assigned to external switches so that the user can control the input signal power manually. *START* and *RSTn* signals are also manually controlled with external switches. The output signals *SIG_I* and *SIG_Q* are produced by multiplying input signals with *SIGNAL_POWER* and expanded to 16-bit signals. Finally, a data-ready signal *DRDY_SG* is transmitted when signal outputs are sent.

5.2.3 Adaptive Digital Predistorter

5.2.3.1 R-to-P and P-to-R Converters

As mentioned earlier, the CORDIC algorithm is used for R-to-P and P-to-R converters. Because it is dominated by additions and subtractions [13] the CORDIC algorithm is highly suitable for FPGA mechanization.

The converters are designed based on an iterative method using a pipeline. The CORDIC algorithm block consists of three serial adder/subtractors, three shifters, three registers, and a serial read only memory (ROM) which contains pre-calculated arctangent values. Additionally, 3 multiplexers are included in the block for selecting initial inputs or the right shifted cross terms. Figure 5.3 shows the CORDIC algorithm module architecture.

During operation the initial values are loaded through multiplexers on the left of the main algorithm block. Once loaded, the data is shifted right through the adder/subtractor, on into the register and returned to the multiplexer. Since the output word length is 20 bits, each iteration requires 20 clock cycles to generate the result to the register. At the beginning of each iteration, adder/subtractor controllers are set based on the sign of the Y signal for the R-to-P converter. When this structure is used as a P-to-R converter, the sign of the Z signal is used. Also, to present the proper elementary angle value to the adder/subtractor for Z_n , the ROM address is increased at each iteration. At the final iteration, the results are obtained directly from the adder/subtractors.

Figure 5.3: CORDIC algorithm module architecture

The CORDIC algorithm does not cover input angles $|\theta| > \pi$. In order to support the full range of input angles, an additional processing stage is required for the R-to-P converter. The pre-processor rotates the original quadrant to a manageable quadrant and the post-processor returns to the original quadrant after CORDIC processing. The P-to-R converter needs two multipliers in order to generate the I and Q signals by multiplying amplitude and the sine and cosine values.

Figures 5.4 and 5.5 show the schematic diagrams of the R-to-P and the P-to-R converters. For the R-to-P converter, input Z is grounded to zero based on Equation (2.27) and input Y is grounded to zero for the P-to-R converter as shown in Equation (2.28). Also, control signals with the original quadrant information are delayed until pipeline outputs are available.

Figure 5.4: Schematic diagram of R-to-P converter

Figure 5.5: Schematic diagram of P-to-R converter

5.2.3.2 Address Generator and Predistorter Output

Ideally, the predistorter should support all possible input amplitudes to attain the best indexing results. However, since it takes a huge amount of memory to cover all the possible

input amplitudes and is time-consuming to adapt, a linear interpolation method is used to approximate the output amplitude and phase in this work.

Figure 5.6 shows the mapping diagram.

Figure 5.6: Mapping diagram of address generator

If the input signal amplitude $|X_i|$ is between r_k and r_{k+1} , then the predistorter output amplitude and phase will be

$$|Y_i| = ro_k + |X_i| \quad (5.1)$$

$$\angle Y_i = \theta_{rok} + \angle X_i \quad (5.2)$$

In the address generator, address spaces are classified to 16 regions from the active region of the link. Corresponding addresses are assigned based on the input signal amplitude level. Thus, when the input amplitude is in a specific region, the generator produces appropriate LUT address. LUT coefficients are delivered to the predistorter output module based on the address.

Figure 5.7 illustrates the schematic diagram of the address generator. After comparing the input amplitude $R1_IND$ with stored values, a 4-bit address signal $ADDR_IND$ is generated with the original signals.

Figure 5.7: Address Generator

The predistorter output module generates a predistorted signal for ROF link linearization. With input signal X_i , corresponding LUT coefficients are transferred to the output module. Therefore, the original input signals are added to the LUT coefficients and transmitted to the output. In this module, the phase adding operation could exceed 360 degrees or be below 0. Thus, the adjusting circuit must keep the predistorted phase output between 0 and 360 degrees.

The process diagram of the module is presented in Figure 5.8. At the end of each predistorted output signal, the signature signal is attached and delivered.

Figure 5.8: Predistorter Output Module

5.2.3.3 Delay Estimator and First-In First-Out (FIFO)

Because of the time difference between the input signal and the received output signal it is very difficult to simultaneously compare the two signals. Moreover, the time difference fluctuates based on link and system conditions. Even though a delay compensation algorithm has been proposed, experimental experience has shown that distortion can substantially impair precision of the delay estimate [9].

In this thesis, the delay compensation is solved using a delay estimator and a FIFO. During the adaptation stage the input signals are stored in the FIFO with the address after address generation. Also, the predistorter output generates a signature after each signal. Therefore, the delay estimator searches for signatures from the link output signals. Whenever the signature is found, the estimator sends a read signal to the FIFO, which sends the delayed version of the input signal to the algorithm block.

Figure 5.9 illustrates the schematic diagram of the FIFO. Input signals *Data_in_A*, *Data_in_R*, and *Data_in_Addr* are stored whenever the *WE* signal is triggered. When the *RE* signal is triggered output signals *Data_out_A*, *Data_out_R*, and *Data_out_Addr* are transmitted to the output with *DRDY* signal.

Figure 5.9: Schematic diagram of the FIFO

5.2.3.4 Adaptation Algorithm Block

The adaptation algorithm block generates LUT coefficients comparing the input and received output signals. Figure 5.10 describes a simplified diagram of the whole system to illustrate how the algorithm works.

Figure 5.10: Simple diagram of the predistortion system

If $r \cdot e^{j\theta_{in}}$ is the input of predistorter X , Y and Z will be

$$Y = A_p(r) \cdot e^{j(\theta_p(r) + \theta_{in})} \quad (5.3)$$

$$Z = A_r(|Y|) \cdot e^{j(\theta_r(|Y|) + \angle Y)} = A_r(|Y|) \cdot (\cos(\theta_r(|Y|) + \angle Y) + j \sin(\theta_r(|Y|) + \angle Y)) \quad (5.4)$$

where $A_p(r)$ and $\theta_p(r)$ are the AM/AM and AM/PM conversions of predistorter and $A_r(r)$ and $\theta_r(r)$ denote AM/AM and AM/PM distortion characteristics of the ROF link.

Thus, the amplitude and phase errors can be calculated as

$$Error_{amp} = |X| - |Z| = r - A_r(A_p(r)) \quad (5.5)$$

$$Error_{pha} = \angle X - \angle Z = \theta_{in} - \theta_r(A_p(r)) - \theta_p(r) \quad (5.6)$$

As shown, the adaptive method is applied in the block in order to minimize the errors. The adaptive algorithm should be able to identify the link characteristics and update the LUT to adapt with the variation of the predistorter characteristics. LUT updating is based on minimizing the error, which is defined as the difference between the input and the output.

Thus, the $K + 1^{th}$ iteration of entry i is updated as followings

$$ro_{i,k+1} = ro_{i,k} + \Delta_{am} \cdot Error_{amp}(i) \quad (5.7)$$

$$\theta ro_{i,k+1} = \theta ro_{i,k} + \Delta_{ph} \cdot Error_{pha}(i) \quad (5.8)$$

where $ro_i, \theta ro_i$ are amplitude and phase LUT values coefficients and Δ_{am}, Δ_{ph} are the step sizes for the algorithm.

Figure 5.11 shows the steps of the adaptation algorithm. In step 1, LUT coefficients, i.e. $ro_{i,k}$ and $\theta ro_{i,k}$, must be given to the module with the input signal X and the received output signal Z before processing the adaptation. The differences between the two input signals are calculated separately in step 2 and compared with the threshold values in step 3. If the differences are greater than the values each LUT coefficient is updated by subtracting some portion of the difference from the old LUT coefficient during step 4, and is then saved back to the LUT.

Figure 5.11: Adaptation algorithm

5.2.4 ROF link Model

An adequate hardware model of the ROF links must be made to test this predistortion system. An ROF link model is designed based on third order polynomial representations (5.9) and (5.10) in [29].

$$R_{out} = 1.3762p - 0.83406p^2 + 0.16306p^3 + N_0 \quad (5.9)$$

$$A_{shift} = 2.548 - 1.696p + 0.796p^2 - 0.124p^3 + N_0 \quad (5.10)$$

where R_{out} and A_{shift} are the output amplitude and phase. Both are functions of input amplitude ' p '. N_0 is the noise term.

For hardware model design, the whole input power region is partitioned to a group of small regions and then mathematical linear equations for each region are calculated. Combining these equations for whole region, an equivalent ROF link model is designed and implemented by VHDL. Figure 5.12 shows the method of designing the hardware model.

Figure 5.12: Method of designing the ROF link model

Also, R-to-P and P-to-R converters are used to design this link model because the above equations require the polar forms of signals and the input and output of the link are in rectangular form.

Figure 5.13 and 5.14 show the ROF link model AM/AM and AM/PM characteristics.

Figure 5.13: AM/AM characteristic of ROF link model

Figure 5.14: AM/PM characteristic of ROF link model

5.3 FPGA Implementation

Before FPGA implementation a VHDL test bench was written and the design was verified through functional simulation using Modelsim. Functional simulation verifies the operation of the system without timing considerations. The simulation has shown suitable results. The final schematic diagram of the predistorer is shown in Figure 5.15. Figure 5.16 presents the functional simulation results.

Figure 5.15: Schematic diagram of the predistorer

Figure 5.16: Functional simulation results

The LUT coefficients signals *mema* and *memr* in Figure 5.16 are updated whenever a new index address, *addr*, comes in. After a training period the LUT coefficients are frozen to fixed values. Therefore, whenever index addresses are come in, the corresponding LUT coefficients which are already frozen are sent to output. Also, signals *update_r* and *update_a* indicate whether the LUT coefficients are updating or not.

A design is ready for synthesis once it simulates correctly. Synthesis is the process of taking an input like VHDL to a device-specific form such as a programming file. All synthesis steps were done using Xilinx ISE 6.3. The target FPGA chip is Xilinx Virtex-II FPGA, XC2V1000-4FG456. Table 5.1 lists the synthesis results.

XC2V1000-4FG45	Resource Used	Performance
Number of Slices	4995 out of 5120	97%
Number of Slice Flip Flops	6814 out of 10240	66%
Number of 4 input LUTs	7436 out of 10240	72%
Number of bonded IOBs	94 out of 328	28%
Number of MULT18X18s	8 out of 40	20%
Maximum Frequency	-	52.421MHz

Table 5.1: Xilinx ISE 6.3 synthesis results

The Memec Virtex-II V2MB1000 development board is used for implementation. This board provides a complete solution for developing designs and applications based on the Xilinx Virtex-II FPGA family [33].

During the initial synthesis step, the VHDL codes were interpreted and logic was assembled and mapped to the target FPGA. In this stage, floor planning and pin assignments were performed. Because this system used over 95 percent of the slice resource in the target FPGA, the ISE tool performed floor planning by applying the best algorithms to optimize the design for area and speed. Figure 5.17 shows the floor planning results with LUT selected.

Figure 5.17: Floor planning result with LUT selected

Once the required components have been defined, they can be assigned to actual chip locations and connections can be made between them. Pin assignment was performed using the Xilinx PACE tool. Since the development board already allocates 323 out of a total 432 pins to other internal components, pin assignment was performed manually. Figure 5.18 shows the pin assignment results. Table 2.2 displays the pin assignment descriptions.

Figure 5.18: Pin assignment in the FPGA

I/O Name	I/O Direction	Vertex-II Location	Description
ADAPTn	Input	D6	Adaptation On/Off
CLOCK	Input	D11	System Clock
DRDY_AD	Output	Y14	Predistorter Data Ready
DRDY_PR	Output	W13	P-to-R Converter Data Ready

DRDY_RP	Output	Y13	R-to-P Converter Data Ready
DRDY_SG	Output	AB17	Signal Controller Data Ready
ENA_core	Input	AA5	ADC Enable
Input_power<0>	Input	C5	Input Signal Power Switch
Input_power<1>	Input	C4	
Input_power<2>	Input	A4	
Input_power<3>	Input	B4	
I_in<0>	Output	AB5	Input Signal I to Predistorter
I_in<1>	Output	AA6	
I_in<2>	Output	AB6	
I_in<3>	Output	AA7	
I_in<4>	Output	AB7	
I_in<5>	Output	AA8	
I_in<6>	Output	AB8	
I_in<7>	Output	AA9	
I_in<8>	Output	AB9	
I_in<9>	Output	AB13	
I_in<10>	Output	AA13	
I_in<11>	Output	AB14	
I_in<12>	Output	AA14	
I_in<13>	Output	AB15	
I_in<14>	Output	AA15	
I_in<15>	Output	AB16	
I_out<0>	Output	A10	Output Signal I from the ROF link
I_out<1>	Output	E18	
I_out<2>	Output	G18	
I_out<3>	Output	J18	
I_out<4>	Output	K17	
I_out<5>	Output	E20	
I_out<6>	Output	G20	

I_out<7>	Output	J19	
I_out<8>	Output	K20	
I_out<9>	Output	L19	
I_out<10>	Output	C22	
I_out<11>	Output	E21	
I_out<12>	Output	F22	
I_out<13>	Output	H21	
I_out<14>	Output	J22	
I_out<15>	Output	L21	
Q_in<0>	Output	V7	Input Signal Q to Predistorter
Q_in<1>	Output	V8	
Q_in<2>	Output	V9	
Q_in<3>	Output	U9	
Q_in<4>	Output	U10	
Q_in<5>	Output	U11	
Q_in<6>	Output	U12	
Q_in<7>	Output	U13	
Q_in<8>	Output	U14	
Q_in<9>	Output	V14	
Q_in<10>	Output	W15	
Q_in<11>	Output	V16	
Q_in<12>	Output	Y16	
Q_in<13>	Output	W16	
Q_in<14>	Output	Y17	
Q_in<15>	Output	W17	
Q_out<0>	Output	B10	Output Signal I from the ROF link
Q_out<1>	Output	E11	
Q_out<2>	Output	F18	
Q_out<3>	Output	H18	
Q_out<4>	Output	J17	

Q_out<5>	Output	L17	
Q_out<6>	Output	E19	
Q_out<7>	Output	H19	
Q_out<8>	Output	J20	
Q_out<9>	Output	K18	
Q_out<10>	Output	L18	
Q_out<11>	Output	D21	
Q_out<12>	Output	E22	
Q_out<13>	Output	G21	
Q_out<14>	Output	H22	
Q_out<15>	Output	K21	
RSTn	Input	A6	Reset Signal Input
SIGIN_I<0>	Input	L20	Signal Input I from ADC
SIGIN_I<1>	Input	C21	
SIGIN_I<2>	Input	D22	
SIGIN_I<3>	Input	F21	
SIGIN_I<4>	Input	G22	
SIGIN_I<5>	Input	J21	
SIGIN_I<6>	Input	K22	
SIGIN_I<7>	Input	Y15	Signal Input I from ADC
SIGIN_Q<0>	Input	V6	
SIGIN_Q<1>	Input	D8	
SIGIN_Q<2>	Input	C8	
SIGIN_Q<3>	Input	F19	
SIGIN_Q<4>	Input	F20	
SIGIN_Q<5>	Input	G19	
SIGIN_Q<6>	Input	H20	
SIGIN_Q<7>	Input	K19	
START	Input	C6	System Start On/Off

Table 5.2: Pin assignment descriptions

Once the design is placed and routed, a binary file is generated containing all the information needed for programming the FPGA with the design.

There are generally two methods of programming an FPGA with a binary file. One involves programming directly through flash memory and the other is indirect programming through flash memory. In this research, iMPACT software was used to program the FPGA with a JTAG port. Figure 5.19 shows the implementation of the actual system on the FPGA.

Figure 5.19: Predistortion system on FPGA

5.4 Analog-Digital Converter

To produce digitized input signals an ADC is required before the predistorter. The ADC is implemented on a Microchip DSPIC30F4012 micro controller.

The DSPIC30F4012 controller operates at 5V and features 48 Kbytes of self-programming Flash memory, controller area network capability with extended temperature range, and performance of 20 or 30 MIPS. Other features include 2 Kbytes SRAM, 1 Kbytes EEPROM data memory, a 10-bit A/D converter with nine channels at 500K samples per second, and five 16-bit timers. Interface support includes SPI, I2C and two UARTs.

The input of the ADC is 2 channels of analog data in range 1 V to -1 V with respect to common ground. The output is 8-bit digital 2's complement signals of each channel and 1 data-ready signal.

First, each input signal is shifted from the range of $\{-1, 1\}$ V to the range of $\{0, 3.3\}$ V due to the input requirements of the DSPIC30F4012 fast ADC module. This is accomplished by feeding each channel to a two-stage amplifier and a multiplier. The signal manipulation stage is shown in Figure 5.20.

The first stage of the circuit adds one volt constant offsets to the input signal and then negates the signal to the range of $\{-2, 0\}$ V. The second stage then scales the shifted and negated signal by -1.638 to the range of $\{0, 3.3\}$ V. Therefore, the output routes to the appropriate ADC input channel.

Next, the ADC module is programmed using the C language. The C code of the module is available in Optimization Problem Research and Application Laboratory (OPRAL).

This implemented ADC supports up to 180,000 samples per second per channel. The ADC is pictured in Figure 5.21.

Figure 5.20: Signal manipulation stage

Figure 5.21: Analog-to-Digital Converter

CHAPTER 6

EXPERIMENTS and RESULTS

6.1. TEST SETUP

In order to test the prototype of the system, the following setup was configured (Figure 6.1). The setup consists of an arbitrary function generator (SMIQ03B), a logic analyzer (TLA715), a dual-channel ADC, an ROF link hardware model, the predistortion system, and a PC for data comparison.

SMIQ03B is ideal for use in development and type-approval testing and supports signal generation such as Quadrature Phase-Shift Keying (QPSK) and QAM and signal quality [34]. TLA715 includes logic analyzer modules which provide solutions for large numbers of buses and high channel count requirements as well as TLA7PG2 pattern generator modules [35].

Figure 6.1: Test setup diagram

For real system implementation a frequency conversion must be carried out in order to support the real ROF link. In this work, however, RF frequency conversion is not considered for testing of the predistortion system.

The analog QAM baseband input signals I, Q with a range between -1V to 1V were generated via the SMIQ03B based on the pseudo random digital sequence with rectangular pulse coding.

After baseband signal generation with SMIQ03B, a dual-channel 8-bit ADC digitized the baseband signals to 8-bit I and Q signals. The digitized signals were sent to the predistortion system which is implemented in Xilinx Vertex-II FPGA, XC2V1000-4FG456. Extra switches were added in the system to produce variable signal power. The system outputs were fed internally to the ROF link model in the same FPGA. Finally, the hardware model generated output signals and sent them back to the predistorter. A TLA715 was used to obtain the digitalized ROF link output signals and passed the data to the PC for further analysis. The PC evaluated the input and the output signals with MATLAB and produced several comparison results. Also, adaptation step size was applied to 0.0625. For testing purposes, the phase threshold value is 10 degrees and amplitude threshold value is 0.035 mW.

The testing system is pictured in Figure 6.2.

Figure 6.2: Testing system setup

6.2 Experimental Results

Initially, baseband I and Q sequences were generated from SMIQ03B at 50 kilo symbol rate per second. These I and Q signals were converted to digital forms and transmitted through the system at 150 kHz sampling rate. The pattern generator module in the TLA715 generated system clock to the predistortion system at 1.5 MHz.

This predistortion system was run for 40 training iterations at each power level to observe the adaptation process. After a reasonable training period, the input and output signals were compared. Although the output signals and input signals began differently, both signals were very close after the period.

Figure 6.3 shows the AM/AM adaptation graph. Since the AM/AM characteristic is almost linear up to 5 mW, no amplitude error is shown. Nevertheless, the system began to adapt AM/AM characteristic errors. However, after the input power went beyond 0.8mW, the system could not adapt the AM/AM nonlinear distortion as the amplitude gain became almost flat.

Figure 6.3: AM/AM Adaptation Graph

The AM/PM adaptation graph shown in Figure 6.4 is quite different from the AM/AM adaptation graph. Because AM/PM distortion is great at a small input amplitude the system must adapt the distortion errors. The graph shows similar adaptation periods for all input amplitudes in spite of the error's range. However, these results can be different based on the step sizes and threshold values.

Figure 6.4: AM/PM Adaptation Graph

Figures 6.5 and 6.6 show the amplitude and phase responses before predistortion and after predistortion. The amplitude response of the predistorter became linear in the whole input power region and the phase response went almost to zero after predistortion.

Figure 6.5: Predistorter Amplitude Characteristics

Figure 6.6: Predistorter Phase Characteristics

Figure 6.7 shows the constellations of the input and output signals without predistortion and with predistortion. This result clearly demonstrates that the linearity of an ROF link can be achieved using the adaptive digital predistortion system compared to that without predistortion.

a. Input signal (mW) b. Output without predistortion(mW) c. Output with predistortion(mW)

Figure 6.7: Constellations of input signal and output signals without and with predistortion

CHAPTER 7

CONCLUSIONS and FUTURE WORKS

7.1 Conclusions

This thesis presents the adaptive digital predistortion system with an ROF link model for FPGA implementation. An FPGA, an A/D converter, an arbitrary waveform generator, and a logic analyzer were used for this prototype implementation. Also, the CORDIC algorithm is employed for R-to-P and P-to-R conversion. The adaptive algorithm was applied through the initial stream of input signals with various input power to update the LUT coefficients used to linearize the ROF link.

A complete system was implemented on the Memec Embedded Development Board with Xilinx Vertex-II FPGA, XC2V1000-4FG456. The actual implementation development was satisfying in terms of performance and function. The selected Vertex-II FPGA met the high speed and resource demands to host a quite complex DSP system. The ability to assign the Vertex-II resources to where they were most needed was critical. Also, the ADC was implemented with a Microchip DSPIC30F4012 Controller.

Although the experiments were performed at 1.5 MHz due to the ADC's speed limitation, this system supports up to 52 MHz. Moreover, without the ROF link model, this system could support up to 102 MHz.

The experiments carried out in this work imply that the adaptive digital predistortion technique for ROF link is promising. It has been shown that this adaptive digital predistorter

can be successfully applied to compensate nonlinearity of the ROF link. The adaptive predistortion method presented here is a function of input-output characteristics and independent of specific knowledge regarding individual optical link parameters such as fiber length and the laser characteristics. In spite of large phase distortion of the ROF link this system can handle the distortion well. However, real ROF links implementation must be done to confirm and measure the quality of results that can be achieved. The model used in the experiment is not true in the sense that it confines all nonlinear characteristics. For instance, memory effects are not covered at all by the model. Inasmuch as this adaptive predistortion method is independent of link characteristics, the same approach can be used for different types of links.

7.2 Future Works

The tested ROF link model was assumed to be memoryless. It would be rewarding to test the algorithm if a model with more accurate and extensive characteristics were synthesized.

The addition of or modification to the algorithm coefficients, i.e. threshold values and step sizes, is a potential area of future research. Such coefficients could greatly influence system performance. Thus, a more efficient adaptation algorithm would be desirable when it is possible to monitor the actual behavior of the system. Also, the error measure sensitivity is an important feature to cover when testing real ROF links.

Further areas to be addressed include implementation issues. In a multi-user situation, the total input power into the ROF link should be known before adaptation. Furthermore, several imperfections in the system such as quantization, amplitude and phase errors in the quantization conversions and errors in delay estimation were not considered. The feedback path for adaptation training should also be considered and could potentially be through another ROF link to produce additional nonlinear distortion.

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