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Modeling and simulation of power system protection relays in a transmission-level application

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**MODELING AND SIMULATION OF POWER SYSTEM
PROTECTION RELAYS IN A TRANSMISSION-LEVEL
APPLICATION**

By

James P. Kelly, B.Eng.Mgt.

**A Final Project Report
presented to Ryerson University**

**in partial fulfillment
of the requirements for the degree of
Master of Engineering
in the program of
Electrical and Computer Engineering**

Toronto, Ontario, Canada, 2008

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Abstract

MODELING AND SIMULATION OF POWER SYSTEM PROTECTION RELAYS IN A TRANSMISSION-LEVEL APPLICATION

Master of Engineering 2008

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Electrical and Computer Engineering

Ryerson University

This report presents the findings of an in-depth literature review on protective relaying. The project focuses on protection system practices which are relevant to transmission-level applications. Various implementations of differential, phase distance and ground distance relays were investigated and ultimately modeled in the Matlab Simulink environment. A further model for a saturable iron-core current transformer was also investigated and developed. These models were tested to ensure compliance with expected results.

The developed relay and current transformer models are used to complete a detailed protection design for a sample power system. A small 230kV bulk-power transmission system is presented and modeled in the Simulink environment. A fault study is completed and current transformers are specified in accordance with IEEE standards. Bus and line protections are selected from the various implementations discussed in the report. The settings for all protection relays are developed in detail based on system analysis and the expert guidelines obtained from a wide literature review. The resulting protection design was tested in a systematic fashion and demonstrated to be effective.

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The author is greatly indebted to his partner Tasneem Essaji for her continued love, support and patience. The author also recognizes his parents, Thomas and Sharon Kelly, for their unwavering encouragement, guidance and love.

***This effort is lovingly dedicated to my beautiful teammate Tasneem
and my wonderful parents.***

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Chapter 1 – Introduction

1.1 The Need for Power System Protection

In modern society, power delivery has become a core necessity of our day-to-day lives. Reliable power delivery is fundamental for a large portion of our daily lives, from the industries that produce our goods, to the hospitals that care for our sick and even to our home refrigerators which preserve our food. This fact was made obvious by the Northeast blackout of 2003 which left 50 million people in Canada and the United States without power for days [1]. This event reaffirmed the criticality and strategic importance of reliable power delivery.

Electric power systems are made up of infrastructure to generate, transmit and distribute electrical energy. These power systems are some of the most complex and costly man-made systems. Faults within these power systems are an unavoidable reality. Electrical faults impose strain on all levels of this infrastructure. If left uncorrected, these faults would quickly destroy this infrastructure and lead to the collapse of the power system. This fact identifies the need for an auxiliary system responsible for the protection of the infrastructure from faults and abnormal operation.

Protection systems include equipment, schemes and policies to detect abnormal conditions and to implement corrective action. The protection systems for electricity generation and transmission almost invariably consist of circuit breakers, measurement devices and protective relays. The circuit breakers have the ability to interrupt and reconnect the electrical power circuits while the measurement devices provide safe and accurate measurements of the power system conditions. The protective relays employ these measurements along with embedded logic to control the circuit breaker operation. These systems are not required during normal power system operation but are critical to operation in abnormal conditions. The protection system ensures that the infrastructure remains protected from damage during abnormal conditions. The protection system also attempts to maximize availability and reliability of the power supply for end users.

1.2 Report Objectives

This report will outline the findings of an in-depth literature review on protective relaying. From the literature background, the report will develop a sample application and complete a protection design. Also from the literature review, the report will develop MATLAB Simulink models of the protection relays and elements being studied. The relays and elements being studied will then be simulated in the sample application. The results of the simulation will be used to evaluate the effectiveness of the protection design and the validity of the relay models.

As the entire field of protective relaying is far too broad to cover in a single project, the scope of the project will be limited. The application to be developed will be based on a small 230kV bulk-power transmission system. The application protection design will be completed from the perspective of the transmission system owner/operator, Hydro One in Ontario. The protection relays to be studied will be limited to two commonly used protection relays at the transmission-level. In this report, the differential and distance (phase and ground) protection relays will be studied in detail. Additionally, this report will study the design and simulation of saturable current transformers which are critical to the functionality of protection systems.

1.3 Report Organization

This report has been organized into the following broad sections: theory, modeling, application, simulation, conclusions and recommendations. The theory chapter develops the theory of power system relaying. The chapter investigates power system faults, the design of instrument transformers and the algorithms of the protective relays being studied. The modeling chapter introduces the Simulink models that have been developed to allow simulation of the transmission protection systems. The chapter introduces models for the various protective relays and realistic current transformers. The application chapter provides a sample protection design for a 230kV transmission system. The chapter designs the protection zones, completes a small short circuit study and specifies the appropriate relay settings to protect the system. The simulation chapter

introduces an overall model of the transmission system including the modeled protection elements. The chapter provides the simulation results of the transmission protection system using the previously designed protections. The chapter introduces the comprehensive testing philosophy, provides highlighted simulation results and tabulates the comprehensive testing results. Finally, the conclusions and recommendations section identifies the significant findings and provides recommendations based on the results of the report.

Chapter 2 – Theoretical Basis of Power System Relaying

2.1 The Nature of Power System Faults

An initial requirement for studying protective relaying is an understanding of power system faults. To develop this understanding one must become familiar with the typical short-circuit current waveform. Additionally, one must understand all of the possible short circuits that can be present in a three-phase power system and their relative severity. This basic understanding is fundamental in the rating and design of all power system equipment. The following sections will develop this basic understanding.

2.1.1 The Typical Short-Circuit Current Waveform

Consider the simple power system shown in Figure 2.1. The system can be represented by a 1st order differential equation:

$L \frac{di}{dt} + Ri = E_m \sin(\omega t + \theta)$, where θ is the voltage angle at the moment the fault occurs.

Figure 2.1 – Simple Power System

The solution to the differential equation can be given by:

$$i = I_m \sin(\omega t + \theta - \phi) - I_m \sin(\theta - \phi) e^{-Rt/L}$$

I_m is the peak steady state current and ϕ is the angle between the voltage and current waveforms ($\phi = \tan^{-1} \frac{\omega L}{R} = \tan^{-1} \frac{X}{R}$). It can be seen that the resulting current will consist of a symmetrical

continuous current and an exponentially decaying D.C. transient current. It can also be seen that the initial magnitude of D.C. current will be heavily influenced by the phase difference between the pre-fault voltage waveform and the fault current waveform. In un-faulted power systems the current angle is typically in the range of $(0^\circ, \pm 32^\circ)$ corresponding to power factors greater than 0.85. In a faulted power system the current angle will approach 90° corresponding to a power factor of 0. If a fault current power factor of 0 is assumed (ie. $\phi=90^\circ$), then the maximum D.C. transient current will be observed when the fault occurs at $\theta=0^\circ$. This corresponds to a fault occurring at the moment the voltage waveform crosses the x-axis. This has been illustrated in Figure 2.2(a). This results in a peak short-circuit current of roughly $i=2I_m$. The phenomenon is often referred to as the 'doubling effect'. If the fault occurs at $\theta=90^\circ$, the peak of the voltage waveform, then there will be no D.C. transient current. This has been illustrated in Figure 2.2(b).

Figure 2.2 – Typical Short Circuit Current Waveforms

a: Maximum Asymmetrical Fault Current

b: Non-Asymmetrical Fault Current

[2, {1.1}]

To understand the origin of the D.C. transient, one must recall that the current through an inductor cannot change infinitely fast unless infinite voltage is applied. In realistic scenarios, it is sufficient to say that the inductor current cannot change instantaneously. Notice in Figure 2.2(a), at the moment of the fault, the symmetrical fault current instantaneously changes from zero to its negative peak value ($-I_m$). This is the case because the fault current is assumed to be lagging the voltage waveform by 90° during a fault. Hence, when the voltage waveform is passing through zero in the positive direction, the 90° lagging current waveform is expected to be at its negative peak. To satisfy the physical law, a D.C. current is created which is equal and opposite to the instantaneous change in the symmetrical current. Thus, the symmetrical current

will change instantaneously but the total (actual) current will not. Notice in Figure 2.2(b), at the moment of the fault, the symmetrical current has no instantaneous change. This is the case because at the peak of the voltage waveform, the 90° lagging current waveform is expected to equal zero. As there is no instantaneous change in the symmetrical current, no D.C. current is required to satisfy the physical law.

2.1.2 The Types and Severity of System Faults

To study protection systems, one must first develop an understanding of the types of faults that can be present in three-phase electrical systems. Each type of fault will create a distinct distortion of the normal voltage and current waveforms. To protect equipment from each type of fault, it is necessary to understand the distortions that will be present.

A three-phase system is subjected to the following types of faults: [3, {2.4.1}]

- Three-phase ungrounded fault;
- Three-phase grounded fault;
- Phase-to-phase ungrounded fault;
- Phase-to-phase grounded fault; and
- Phase-to-ground fault.

Faults in which the three-phases are equally affected (i.e. the three-phase faults) are termed as symmetrical faults. Faults which un-equally affect the three-phases are termed as unsymmetrical. Unsymmetrical faults are far more common [2, {2.1}]. Typically, the three-phase ungrounded fault imposes the most severe duty on a circuit breaker as the first phase to interrupt faces the highest recovery voltage [2, {7.4}]. The three-phase fault typically causes the highest fault currents. There can however, be cases where a phase-to-ground fault may produce a higher fault current than a three-phase fault. This is the condition where the zero-sequence reactance at the point of the fault is less than the positive-sequence reactance [2, {7.4}]. This condition will result in higher fault currents if the positive and zero-sequence currents flow in the same direction. For this reason, short circuit calculations are typically carried out for both the three-phase faults and the phase-to-ground faults.

Knowledge of the various faults and their characteristics allows for the development of a protective relaying philosophy which will allow for comprehensive protection against all of the possible faults. The normal and faulted system phasor representations are shown in Figure 2.3.

Figure 2.3 – Normal and Various Faulted Conditions

2.2 Analysis of Unbalanced Three-Phase Systems

In three-phase balanced systems, it is sufficient to calculate the currents and voltages in one phase and accept that the currents and voltages in the other two phases are simply equal in magnitude and phase displaced by $\pm 120^\circ$. In unbalanced systems, this simplification is not valid. Unbalance can occur in three-phase transmission systems due to faults, single-phase loads, untransposed transmission lines and non-equilateral conductor spacing [2, {1.2}]. Figure 2.3 demonstrates severe unbalance that can be present during many of the faulted conditions. Whenever an unbalanced system is to be analyzed, more sophisticated analysis techniques must be employed. One convenient and commonly used method is the method of symmetrical components first developed by C.L. Fortescue in 1918 [4, {4.1}].

2.2.1 Method of Symmetrical Components

Under the method of symmetrical components, the three-phase voltages and currents, which may be unbalanced, are transformed into three sets of balanced voltages and currents which become the symmetrical components.

$$V_a = V_{a0} + V_{a1} + V_{a2}$$

$$V_b = V_{b0} + V_{b1} + V_{b2}$$

$$V_c = V_{c0} + V_{c1} + V_{c2}$$

If 'a' is defined as a unit-magnitude vector at 120° rotating in a counterclockwise direction:

$$a = -0.5 + j0.866 = 1 \angle 120^\circ$$

$$a^2 = -0.5 - j0.866 = 1 \angle -120^\circ$$

$$a^3 = 1$$

The positive-sequence is made up of V_{a1} , V_{b1} and V_{c1} where:

$$V_{b1} = a^2 V_{a1} \quad \text{and} \quad V_{c1} = a V_{a1}$$

The negative-sequence is made up of V_{a2} , V_{b2} and V_{c2} where:

$$V_{b2} = a V_{a2} \quad \text{and} \quad V_{c2} = a^2 V_{a2}$$

The 'zero-sequence' is made up of V_{a0} , V_{b0} and V_{c0} where:

$$V_{a0} = V_{b0} = V_{c0}$$

From this, the follow matrix relationship can be established:

$$\begin{matrix} V_a & 1 & 1 & 1 & V_{a0} \\ V_b & 1 & a^2 & a & V_{a1} \\ V_c & 1 & a & a^2 & V_{a2} \end{matrix} \quad \text{or } V_{abc} = T_s V_{012}$$

Figure 2.4 – Graphical Representation of Sequence Components

2.2.2 Representation of Faults via Symmetrical Components

The previous section outlined the methods used to represent unbalanced voltage vectors by their symmetrical components. It follows logically that each symmetrical voltage component will have a corresponding current and impedance component.

$$\begin{matrix} V_a & 1 & 1 & 1 & V_{a0} \\ V_b & 1 & a^2 & a & V_{a1} \\ V_c & 1 & a & a^2 & V_{a2} \end{matrix} \quad \text{or } V_{abc} = T_s V_{012}$$

Hence,

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} Z_0 & 0 & 0 \\ 0 & Z_1 & 0 \\ 0 & 0 & Z_2 \end{bmatrix} \begin{bmatrix} I_{a0} \\ I_{a1} \\ I_{a2} \end{bmatrix} \quad \text{or } V_{abc} = T_s Z_s I_{012}$$

The sequence impedances Z_0 , Z_1 and Z_2 can all be different values depending on the system being studied. The reason for the varying impedance is the mutual coupling between phases of the transmission system. This coupling is determined by many factors such as conductor spacing, conductor arrangement and voltage level. An analysis of transmission line design factors which influence this coupling is beyond the scope of this report. This report will simplify this phenomenon by using typical observed values. For most overhead transmission lines the positive and negative-sequence impedances are equal (ie. $Z_1 = Z_2$). The zero-sequence impedance for most overhead transmission lines is 2.5-3.5 times the positive-sequence impedance [5, 110]. This report will assume the impedance relationships conform to typically observed values as follows: $Z_0 = 3Z_1 = 3Z_2$.

Under three-phase balanced operation, generators produce only positive-sequence voltages and only positive-sequence currents flow. Therefore, in balanced operation, the negative and zero-sequence components are not present. In symmetrical systems, the currents and voltages of the various sequences do not affect each other. For example, negative-sequence currents produce only negative-sequence voltage drops. Consider the simplified transmission line system shown in Figure 2.5.

Figure 2.5 – Simplified Transmission System (Only Phase ‘a’ Shown)

The simplified un-faulted transmission line can be represented by the sequence networks shown in Figure 2.6. Notice that under normal balanced operation, the negative and zero-sequence networks are disconnected and no current flows.

Figure 2.6 – Simplified Transmission System: Normal Condition Sequence Networks

Under fault conditions, the three-phase system can be modeled with various interconnections of the sequence networks. Figure 2.7 demonstrates some of the typical interconnections for various faults. The system voltages are represented on top and the corresponding sequence networks are shown on the bottom.

Figure 2.7 – Fault Representation via Sequence Networks

[5, 267]

As an example, consider a phase-to-ground fault occurring between line 1 and line 2 of the system in Figure 2.5. This fault can be represented by the interconnection of the sequence networks as shown in Figure 2.8.

Figure 2.8 – Simplified Transmission System: Phase-to-Ground Sequence Networks

These sequence networks will provide the foundation for the fault analysis that will be presented in later sections.

It is important to note the simplifications which have been assumed. The examples presented included only ideal voltage sources and impedances. In more realistic systems with transformers, motors and generators, the sequence networks become significantly more complicated. The basic concepts demonstrated, however, will be sufficient to develop the focus of this report.

2.3 Short Circuit Calculations

In the design of power systems, one of the most critical pieces of information is the available fault current. The fault current rating for most power system equipment such as circuit breakers, switchgear, and transformers will have a significant impact on the design and cost of these items. If a circuit breaker were to not have the necessary fault rating, the breaker could fail to interrupt during a fault with disastrous consequences. For this reason, short circuit calculations are an integral part of power system design and protection. For most overhead transmission lines, the three-phase fault provides the worst-case fault current. There are, however, some cases where the phase-to-ground fault can provide the worst-case fault current. It is common practice in industry to include both the three-phase fault and the phase-to-ground fault in short circuit studies. This section will derive the necessary equations to evaluate the fault current in each of these scenarios.

2.3.1 Three-Phase Fault

Consider the simple three-phase faulted system demonstrated in Figure 2.9(a). It is assumed that $Z_x = Z_y$ and $Z_n = 0$ (see Figure 2.7). The corresponding sequence network representation is shown in Figure 2.9(b).

From Figure 2.9(b) it can be seen that the zero and negative-sequence currents will be zero. This is expected as the three-phase fault is a symmetrical fault. Therefore, only positive-sequence currents will flow. It follows logically that the per-phase short circuit current can be calculated as follows:

$$I_{a_SC} = \frac{V_a}{Z_1 + Z_x} \quad (\text{three-phase Fault})$$

Figure 2.9 – Simple Three-Phase Fault

a: Physical System Representation

b: Sequence Network Representation

2.3.2 Phase-to-Ground Fault

Consider the simple system demonstrated in Figure 2.10(a) with a phase-to-ground fault on phase 'a'. For this calculation, it is assumed that the load current is zero, hence phases 'b' and 'c' are open circuited. The corresponding sequence network representation is shown in Figure 2.10(b).

$$I_{012} = T_S^{-1} I_{abc}$$

$$\begin{aligned} I_{a0} &= \frac{1}{3} \cdot \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \cdot \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \end{aligned} \quad \text{recall: } I_b \text{ and } I_c = 0$$

$$\begin{aligned} I_{a0} &= \frac{1}{3} \cdot \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \cdot \begin{bmatrix} I_a \\ 0 \\ 0 \end{bmatrix} \end{aligned} \quad \therefore I_{a0} = I_{a1} = I_{a2} = \frac{1}{3} I_a$$

From Figure 2.10(b):

$$3Z_X I_{a0} = V_0 + V_1 + V_2 = V_a - I_{a0}Z_0 - I_{a1}Z_1 - I_{a2}Z_2$$

$$3Z_X I_{a0} + I_{a0}Z_0 + I_{a1}Z_1 + I_{a2}Z_2 = V_a \quad \text{recall: } I_{a0} = I_{a1} = I_{a2}$$

$$I_{a0} (3Z_X + Z_0 + Z_1 + Z_2) = V_a$$

$$I_{a0} = \frac{V_a}{Z_0 + Z_1 + Z_2 + 3Z_X} \quad \text{recall: } I_{a0} = \frac{1}{3} I_a$$

Therefore, the short-circuit current is given by:

$$I_{a_SC} = \frac{3V_a}{Z_0 + Z_1 + Z_2 + 3Z_X} \quad (\text{Phase-to-Ground Fault})$$

Figure 2.10 – Simple Phase-to-Ground Fault

a: Physical System Representation

b: Sequence Network Representation

2.3.3 Asymmetrical Factors

It is important to stress, that the formulas derived in this section to calculate the short circuit current levels apply only to the symmetrical component of the short circuit waveform. As was identified in Section 2.1.1, there will almost always be a D.C. component to the short circuit waveform. These formulas do not account for this phenomenon. It is frequently sufficient to know the symmetrical short circuit current alone. For example, in low voltage systems the X/R ratio is usually low and the D.C. component is therefore lessened and rapidly decaying. As such, it is frequently sufficient to study the symmetrical short circuit current alone in low voltage systems.

However, for high-voltage systems, the X/R ratios can be very high. This can lead to significant and sustained D.C. components to the fault current. For example, when specifying high-voltage circuit breakers, it is necessary to specify both the symmetrical and asymmetrical short circuit ratings. IEEE standard C37.010 provides methods to estimate the asymmetrical short circuit requirements for high-voltage circuit breakers. The standard provides methods to estimate the X/R ratio for complex transmission networks. With the estimated X/R ratio and the expected breaker operating time, tables of multiplication factors are used to compensate the symmetrical current for the D.C. component. All of these multiplication factors are keyed for the expected breaker interrupting moment, such that the exponential decay can be accounted for in the breaker specification. This report will not investigate the calculation of the asymmetrical currents in detail as this is not critical for protective relaying. This report will, however, identify the significance of the asymmetrical current and identify the issues it creates regarding protective relaying.

2.4 Fundamentals of Protective Relaying

A protective relay is defined as “a relay whose function is to detect defective lines or apparatus or other power system conditions of an abnormal or dangerous nature and to initiate appropriate control circuit action” [6]. A protective relay is a non-revenue producing device which is not required in the power system under normal operating conditions. A protective relay is intended

to automate the detection and remediation of power system faults. They are a necessity in power systems as human intervention would be far too slow to prevent massive equipment damage during faults. Furthermore, the complexity of a protection decision could not feasibly be handled by humans in emergency (time-critical) situations. Protection relays allow for quick and predictable responses to power system faults.

2.4.1 Dependability and Security

Dependability is defined as the measure of the certainty that the relays will operate correctly for all the faults for which they are designed to operate [5, 6]. Security is the measure of the certainty that the relay will **not** operate incorrectly for any fault [5, 6]. In other words, security is the measure of certainty that the relay will not operate for faults that it is not intended to protect. Protection systems are generally designed with dependability as the first priority. This is evidenced by the fact that power systems are composed of several overlapping zones of protection and backup protection. In other words, if the nearest relay to a fault fails, the next closest relay has generally been designed to also detect the same fault and should back-up the primary relay. It logically follows that this bias towards dependability will ultimately reduce the security of the power system. This statement is confirmed by the fact that the majority of relay mis-operations are found to be unwanted trips caused by insecure relay operations [5, 6]. As a power system generally provides many alternative paths for power to flow, a bias towards dependability seems justified. There are many cases, such as radial power systems and emergency power systems where this bias for dependability may not be as appropriate. Regardless of the appropriate bias, it should be the goal of a protection system designer to maximize both the dependability and security of the protection system. This is generally accomplished by establishing zones of protection within the power system.

2.4.2 Zones of Protection

Zones of protection are generally arranged with the current transformers (C.T.s) providing the boundaries. C.T.s define the boundaries as they provide the window through which the relay 'sees' the power system. A zone is defined as a 'closed zone' when it is bounded at all ends by

current transformers (i.e. differential protection). A zone is defined as an open zone when the length of a zone is not bounded by a current transformer (i.e. over-current and distance protection). Therefore, the precise length of an open zone is unknown as the length of the zone can vary with fault current levels and measurement errors.

To ensure that adequate protection of power system equipment, the following requirements should be met:

- 1) All power system elements must be encompassed by at least one zone. Critical equipment should be included in at least two zones. This is demonstrated in Figure 2.11.
- 2) Zones of protection must overlap to prevent any element in the power system from being unprotected. This overlap should be made as small as possible, but cannot be eliminated. Faults occurring in the region of overlap will cause the protections of both zones to operate which will remove a larger segment of the power system from service. This is demonstrated in Figure 2.12.

Figure 2.11 – Typical ‘Closed’ Zones of Protection

[4, {1.10}]

Figure 2.12 – Typical Overlap of Protection Zones

a: Dead-tank Circuit Breakers

b: Live-tank Circuit Breakers

[4, {1.10}]

Figure 2.12 demonstrates the typical zone overlaps for different current transformer and breaker topologies. Notice that no portion of the power system goes unprotected at the boundary. Faults which occur in the overlap zone will cause the protections of both Zones X and Y to operate. This will result in the tripping of a larger section of the power system than may be required. Figure 2.12(a) demonstrates the ideal case with ‘dead-tank’ circuit breakers. Dead-tank breakers are those whose casings are at ground potential. This is the typical case for oil circuit breakers. As the casing is at ground potential, current transformers can easily be installed in the breaker bushings. This is the ideal case as faults in the overlap zone (i.e. in the breaker itself) should be tripped by both zones X and Y. Figure 2.12(b) demonstrates the less ideal case of ‘live-tank’ circuit breakers. Live-tank breakers are those whose casings are at line potential. This is typical for SF6 breakers. As the casings are at line potential, the current transformers must be installed

with their own insulation system in a separate free-standing structure. This separate structure is expensive and it is generally not cost effective to install one on each side of the breaker. Hence, for live tank breakers, both C.T.s are likely to be found in the same structure and arranged as shown. In the case of Figure 2.12(b), a fault in the overlap zone will unnecessarily trip Zone X. Realistically, this overlap length is extremely small and does not present a significant problem.

2.5 Instrument Transformers

Protective relays require accurate representation of the power system operating state. This is primarily achieved through the use of voltage transformers (frequently referred to as potential transformers) and current transformers. These devices are most commonly referred to by their acronyms: V.T.'s (or P.T.'s) and C.T.'s. The purpose of these devices is to transform the power system voltage and current waveforms into lower voltages and current suitable for safe and economical measurement. This section will overview some of the main features of these devices and some of the problems faced in their application.

2.5.1 Voltage Transformers

There are two main types of voltage transformers used in protection systems. The first type is simply known as a voltage transformer (V.T.) and has its primary directly connected to the power system. The second type is known as a coupling capacitor voltage transformer (C.C.V.T) and has its primary connected between a string of capacitors and ground. Both of these transformer types are shown in Figure 2.13. The use of the basic V.T. is generally preferred due to its simplicity and accuracy. In fact, basic V.T.s are considered to be essentially error-free from 0-110% of their normal operating range for relaying applications [5, 63]. Basic voltage transformers would be used almost universally if not for their cost of production at high-voltages. For voltages in excess of 115kV, the C.C.V.T. type generally becomes more economical. The C.C.V.T. uses capacitors as potential dividers to reduce the system voltage to 1-4kV. From there, a standard transformer reduces the voltage to the standard levels. There are two further problems which must be dealt with in C.C.V.T.'s. As the capacitors introduce an unacceptable phase shift of the voltage waveform, the transformer must be connected through an inductance which is

tuned to cancel this phase shift. Furthermore, this capacitance/inductance combination creates a resonant circuit. This resonant circuit requires a special damping circuit to be installed in the transformer secondary to suppress any ferroresonance. It is beyond the scope of this report to investigate the design of C.C.V.T.'s in detail. These issues were raised to highlight the fact that these transformers require fairly complex designs and are subject to many sources of error not found in standard voltage transformers.

Figure 2.13 – Typical Voltage Sources for Protective Relaying

- a: Basic Voltage Transformer with Double Secondary
- b: Coupling Capacitor Voltage Transformer [Only one phase shown, 'b' and 'c' phases duplicate with secondaries connected as in (a)]

[4, {5.14}]

Voltage transformer secondary voltages have been standardized at 120V phase-phase and 69.3V phase-neutral [5, 62]. It is common to find V.T.s with double secondaries as shown in Figure 2.13. This is required as phase-protection relays require the phase-neutral or phase-phase voltages while ground relays typically require the zero-sequence voltage ($3V_0$) which requires the open-corner voltage of a broken delta secondary.

2.5.2 Current Transformers

The current transformer is the single most important input device for protective relaying. They are single primary, single secondary, magnetically coupled transformers. C.T.s can come in several types, the through-type, the bar-type and the wound primary type. The through-type has no primary winding as the primary conductor is simply fed through opening. Similarly, the bar-type is a through-type with a conducting bar permanently fed through the opening. The primary conductor is then attached via terminals to each end of the conducting bars. Lastly, the wound primary-type will include one or more turns of the primary conductor around the core. The structure of a typical through-type C.T. is shown in Figure 2.14.

Figure 2.14 – Structure of a Through-Type Toroidal Core Current Transformer

A: Core Cross-sectional Area

N: Number of Turns

i: Secondary Current

[7, 3]

The through-type and bar-type C.T.s are the most common as the secondary winding can be symmetrically distributed around the core. This allows for low leakage flux and more accurate measurements.

Regardless of whether the primary is physically wound around the core or the core is 'wound' around the primary (in the case of the through and bar types), the primary of the C.T. is connected in series with the power system conductor. This allows the standard transformer relationship shown below:

$$\frac{N_S}{N_P} = \frac{I_P}{I_S}$$

Where: N_P – number of primary turns I_P – primary current (A)
 N_S – number of secondary turns I_S – secondary current (A)

C.T. secondaries have a standard rating of 5 amps in North America. 1 amp secondaries are also available and are frequently used in other countries. The basic ratio of a current transformer is generally specified by the ratio of rated primary to secondary current. For example, a 600:5 C.T. is rated for 5A secondary current at 600A primary current and the ratio is 120 (N_S/N_P). These ratings specify the continuous operating capabilities of the current transformer and these would roughly correspond to the normal system conditions. Of much more importance however, is the performance of the C.T. under fault condition when the current will vastly exceed these values.

2.5.2.1 Saturation in Current Transformers

Under fault conditions, the flux in the C.T. core will increase and can ultimately saturate the core. As the flux approaches saturation, the ideal relationship developed above will no longer hold true. The equivalent circuit of the current transformer is used to understand this effect. Figure 2.15 demonstrates this circuit. The primary resistance and reactance have been omitted as they have no appreciable effect on the C.T. accuracy. From the equivalent circuit, it is possible to construct a generalized phasor diagram to represent the transformer operation (see Figure 2.16).

Figure 2.15 – Simplified Equivalent Circuit of a C.T. and its Burden

[8, 4]

Table 2.1 – Symbols Used in Figure 2.15 and 2.16

V_S	Secondary exciting voltage	V_B	CT terminal voltage across external burden
I_P	Primary current	Z_E	Exciting impedance
I_{ST}	Total secondary current	R_S	Secondary resistance
I_S	Secondary load current	X_L	Leakage reactance (negligible in Class C CTs)
I_E	Exciting current	Z_B	Burden impedance (includes secondary devices and leads)
N_2/N_1	CT turns ratio		

[8, 5]

Figure 2.16 – Phasor Diagram of a C.T. With a Standard Burden

[8, 6]

From the phasor diagram of Figure 2.16, it can be seen that the excitation current (I_E) will cause an error in the C.T. output (I_S). This excitation current (I_E) is synonymous with the magnetic field required to generate the flux in the C.T. core (in the simplified case where $I_{LOSS} = 0$). When the core flux is low, the magnetizing current is very small compared to the C.T. output. This results in no significant errors. When the core flux approaches the saturation point, the magnetizing current must increase disproportionately to the flux created. In this case the magnetizing current becomes quite significant when compared to the C.T. output. Thus, as the C.T. approaches the saturation point, the error in the output current will increase dramatically. C.T. operation over all ranges is illustrated using excitation curves. These curves show the relationship between the secondary exciting voltage (V_S) and the secondary exciting current (I_E).

The secondary exciting voltage is equal to the derivative of the core flux. Furthermore, the derivative of the core flux is proportional to the derivative of the core flux density. This means is that the V_s versus I_e excitation curve is closely related to the standard B versus H curve (magnetic flux density versus magnetic field strength).

Figure 2.17 – Typical Current Transformer Excitation Curves

As an illustration, the magnetizing impedance can be calculated by dividing each voltage value on the graph by the corresponding excitation current value. Table 2.2 demonstrates the excitation impedance for the 1200:5 C.T. demonstrated in Figure 2.17. The table demonstrates that the excitation impedance increases to a maximum at the curve 'knee-point' voltage (roughly 310V). This point corresponds to the maximum permeability of the core. Past this point, the excitation impedance falls to 25Ω at 10 amps of excitation current. When referring back to

Figure 2.15, it is easy to see that as the excitation impedance falls, there will be a greater error present in the burden current I_s .

Table 2.2 –Typical 1200:5 Current Transformer Excitation Impedance

$V_s, \text{rms (V)}$	$I_{e, \text{sec, rms (A)}}$	$Z_{e, \text{rms (ohms)}}$
2.8	0.002	1400
12	0.005	2400
32.5	0.01	3250
95	0.02	4750
335	0.05	6700
410	0.1	4100
420	0.2	2100
435	0.5	870
450	1	450
460	2	230
475	5	95
490	10	49
500	20	25
525	50	10.5
550	100	5.5
Extrapolated		

The above analysis leads to the conclusion that core saturation is the main issue when sizing C.T.s for protection applications. Furthermore, it is obvious that the core flux is primarily determined by two aspects: the primary current and the secondary burden. Thus, the IEEE has developed standard C.T. classifications for relaying which are primarily based on these two parameters.

2.5.2.2 IEEE Classifications of Current Transformers

The standard format of the IEEE classification is shown below:

Table 2.3 – Standard IEEE Current Transformer Classification

	Current Ratio	,	Letter Class Code	Rated Secondary Voltage
	I_p/I_s (A)	,	C, K, T, H or L	V_s (V)
Example	1200/5	,	C	800
Example	600/5	,	T	200

The letter class codes are defined as follows [8, 8]:

- C: The C.T. ratio error has been estimated by calculation. This indicates that the leakage flux is negligible (i.e. $X_L=0$) and the excitation characteristic can be used directly to determine performance. This also assumes that the burden and excitation currents are in-phase and that the secondary winding is symmetrically distributed. Class 'C' C.T.s are the most common type in use for protective relaying.
- K: Similar to class 'C' with the additional requirement that the knee-point voltage must be at least 70% of the secondary terminal voltage rating. This results in larger core cross sections and/or core material with higher magnetic saturation ratings.
- T: The C.T. ratio error has been estimated by test. This indicates that the core has appreciable leakage flux. Thus, testing must be employed to determine the ratio error.
- H, L: Old ANSI classifications used for C.T.s manufactured before 1954. These classifications are no-longer in use but could still be identified on existing equipment.

The rated secondary voltage corresponds to the secondary exciting voltage that the C.T. is capable of producing at 20-times the rated secondary current with no-more than 10% error. For example: a 1200/5, C800 C.T. should be able to produce a secondary voltage of at-least 800V at 100A ($20 \times 5A$) with no-more the 10% error. The 800V rating indirectly specifies the allowable secondary burden. In this case the maximum allowable secondary burden would be 8Ω ($800V/100A$) to ensure that there would be less than 10% error. Notice that at 100A of secondary current, the maximum allowable error would be 10A ($100A \times 10\%$). This error current will be the excitation current I_E . Hence, the excitation curve can be used to estimate the

rated secondary voltage (in the case of class 'C' C.T.s only). From Table 2.2, it can be seen that the C.T. is capable of a secondary voltage of 490V at an excitation current of 10A. Consider the C.T. of Table 2.2. If it is assumed to be a class 'C', it would be rated as a C400 provided the winding resistance meets the following criteria:

$$R_s \leq [(490V - 90A \cdot 4\Omega) / 90A] = 1.44\Omega$$

The rated secondary voltages for protective relaying are standardized at 100V, 200V, 400V and 800V corresponding to maximum burdens of 1 Ω , 2 Ω , 4 Ω and 8 Ω respectively.

Table 2.4 – Standard Relay Burden Designations

(Characteristics for 60Hz System and 5A Secondary Circuit)

Standard Impedance Designation	Impedance (Ω)	Apparent Power (VA)
B-1	1	25
B-2	2	50
B-4	4	100
B-8	8	200

Consider the following simple sizing example:

Specify the C.T. required for the following application such that the error does not exceed 10% at the rated fault current. (Assume there will be no D.C. component in the fault current.)

Full-load current: 1000A

Symmetrical short circuit current: 22kA

Relay burden: 1 Ω

Secondary Leads: 150m of #12cu AWG (one-way), #12cu AWG resistivity= 5.4m Ω /m

Answer: The current ratings must be sized as $\max\{1000A, 22kA/20\} = 1100A$. As 1100A is a non-standard size, the next largest size would be used. Hence, the C.T. current ratio would be 1200/5. Next, the total burden must be calculated. $R_{\text{Burden}} = 1 + 2(150m \times 5.4m\Omega/m) = 2.6\Omega$

Hence, to meet the requirements, a 1200/5 C400 C.T. should be specified.

2.5.2.3 Asymmetrical Current Considerations

All of the analysis of current transformers above has assumed that the primary current is symmetrical. Section 2.1.1 demonstrated that there will almost always be a D.C. component of the fault current and the magnitude and duration of the fault current is related to the system X/R ratio. In high-voltage systems, the X/R ratios are typically high and the D.C. component can rarely be neglected. The D.C. component of a C.T.'s primary current will greatly increase the flux in the core. When the D.C. component is at its maximum, the flux can potentially increase to $1+X/R$ times the flux resulting from the symmetrical component [8, 12].

To avoid saturation completely, it is necessary to define the saturation voltage (V_X) which is the voltage across the transformer secondary for which the peak induction just exceeds the saturation flux density. Graphically, this can be found as the voltage at the intersection point of the two straight line segments on the saturation curve. It can be shown that saturation can be avoided if the following relationship is met:

$$V_X > I_{ST}(1 + \frac{X}{R})(R_S + R_{Burden})$$

[9]

By continuing on the previous example, it can be seen that the 1200:5 C.T. of Figure 2.17 has a saturation voltage of approximately 350V. Assume that the C.T. winding resistance is 1.44Ω (the maximum allowable for the C400 rating) and that the system in the previous example is a 230kV system with an X/R ratio of 10. The minimum required saturation voltage can be determined as follows:

$$V_{X,minimum} = \frac{22000A}{1200/5}(1 + 10)(1.44\Omega + 2.6\Omega) = 4074 V$$

Obviously, the 1200:5 C.T. of Figure 2.17 will demonstrate significant error due to saturation in this application due to the asymmetrical current. Application of this method of C.T. sizing frequently results in transformers which are impractically large. This method creates C.T.s with primary current ratings approaching $(1+X/R)$ times the ratings achieved on a symmetrical current

basis alone. In this example, the resulting C.T. designed primary current would likely exceed 10000A. The actual rating of such a C.T. would depend on the saturation characteristics which, given the size of these C.T.s, are difficult to obtain from manufacturers without purchasing.

In many applications, saturation of current transformers during the maximum asymmetrical fault must be accepted. A general rule of thumb to minimize the C.T. saturation effects is to select a C.T. with a 'C' voltage rating at least twice that which is required for the maximum steady-state symmetrical fault current [8, 30]. Knowing that a C.T. may saturate necessitates reviewing each application to determine how the protections may function under saturation. Over-current and distance protection should be checked to ensure that the instantaneous trip will be initiated before the saturation levels (along with the appropriate directional checks). For differential protection, the C.T.s should be exactly matched and the relaying should provide some immunity from saturation. Traditionally, this would be provided by percentage differential or high-impedance differential relays. Modern microprocessor-based differential relays allow for various schemes to detect and compensate for C.T. saturation in differential relays.

2.6 Directionality

Directionality refers to the ability of a relay to detect currents flowing in one direction versus another. In lower voltage applications it is common for there to be only one source of power and only one path for the power to flow. In these simple applications, directional protection is not generally required. At higher voltage levels, there are typically many sources and many redundant paths for power to flow. The desired protection for a fault in one direction is likely very different from the desired protection for a fault in the other direction. At the transmission-level, proper detection of fault direction is of critical importance.

The direction of current waveform can be determined through the use of a directional element. A directional element determines the direction to a fault by examining the phase angle of the current waveform with the phase angle of another **constant** system phasor. This other constant system phasor is known as the polarizing quantity and is almost always one of the system voltage phasors at the relay.

Figure 2.18 – Polarization Example

Consider the system shown in Figure 2.18 with only the 'a' phase current shown. The phase 'a' current is gradually decreased from I_a to zero and then increased in the negative direction to $I_{a'}$ to complete a directional change. At the point at which the current passes through zero, the phase of the current vector will change by 180° . To properly detect this phase change, the phase of the current waveform must be compared with the phase of a polarizing source. The polarizing source is simply another system phasor that will provide a point of reference to measure the phase angle of the current phasor. This polarizing source could be any of the voltage vectors. It is important to remember, as identified in Figure 2.3, that at the moment a fault occurs, the voltage phasors can become severely distorted.

To avoid the effects of fault distortion, traditional electromechanical relays would typically use 'cross-polarization'. As an example, V_{bc} would typically be chosen as the polarizing source for I_a as it will be least affected by faults involving the 'a' phase. In the generic case, it could be stated that power flow was forward if the angle from V_{bc} to I_a was within the range of $(0^\circ, 180^\circ)$ (assume that current leading is defined in the positive direction while lagging is defined in the negative direction). The generic approach is typically used in metering applications while attempting to measure power flow in normal operations. One problem with the generic approach for protective relaying is that during a fault, the current will lag the phase voltage by almost 90° .

This will cause the phase difference during a fault to be very close to the 0° forward/reverse decision boundary. Due to the volatility in the waveform measurements during a fault, it is likely that the phase difference will overshoot the decision boundary in the transient period. This can cause unacceptable errors in the directional decisions. For protective relaying, it is more desirable to set the decision boundary to be perpendicular to the expected fault current phasor. For example, assume the I_a fault current phasor was expected to lag the phase voltage by 85° during a fault and that V_{bc} will be the polarizing source. In this case, it would be appropriate to set the forward decision boundaries to $(-85^\circ, 95^\circ)$. This will cause the directional element to improperly detect the direction during normal load conditions with leading power factors. As a protection relay is unconcerned with normal power flow, this does not create a problem.

Modern microprocessor relays typically avoid the effects of fault distortion through the use of 'memory-polarization'. Under this scheme, the polarizing source is sampled and delayed by a few cycles. When a fault occurs which causes the voltage waveforms to become distorted, the polarizing source is remembered from its last reliable value and used for directional decisions. Some supervisory logic is required to monitor the power system and trigger the memory-polarization. Typically, memory-polarization is triggered by an under-voltage condition. Under this scheme, cross-polarization is unnecessary, thus a current's own phase voltage or positive sequence phase voltage are frequently used to provide this polarizing reference. As an example, V_a could be chosen as the polarizing source for I_a if memory-polarization is utilized. In the generic case, it could be stated that power flow was forward if the angle from V_a to I_a was within the range of $(-90^\circ, 90^\circ)$ (assume that current leading is defined in the positive direction while lagging is defined in the negative direction). Again, during faults the current will lag the phase voltage by almost 90° . This will cause the phase difference during a fault to be very close to the -90° forward/reverse decision boundary. Assume that the I_a fault current phasor was expected to lag the phase voltage by 85° during a fault and that V_a will be the polarizing source. In this case, it would be appropriate to set the forward decision boundaries to $(-175^\circ, 5^\circ)$ for protection purposes.

2.7 Differential Protection – ANSI 87

The single best protection technique is known as differential protection [4, {6.1}]. Differential relays measure the current differential by summing the current waveforms of all lines into and out-of a protected zone. Differential protection can be applied to any and all parts of the power system including generators, motors, buses, transformers, lines, capacitors and reactors. It can also be applied effectively at all voltage levels. Traditionally, the only limitation on the application of differential protection was the length of the protected zone as the current waveforms could not be transmitted over long distances. Modern microprocessor-based relays with high speed communication pathways have further reduced this limitation such that differential protection can be applied almost universally. This section will explore the necessary concepts to develop differential protection schemes.

2.7.1 Theory of Differential Protection

The fundamental principle of differential relaying is as follows:

“The sum of currents flowing into a protected zone will essentially equal the sum of currents flowing out of a protected zone under normal conditions.”

[4, {6.2}]

With this principle, the operation of the relay can be based on the current differential alone. Figure 2.19 illustrates a simple 2-terminal current differential scheme. It can be seen that under normal conditions, the relay operating (I_{OP}) current is the difference between the error currents (I_e) in the two current transformers. The error between the two C.T.s can be made quite small by matching the ratios and classification of the C.T.s, but the error will never be zero. Under the fault condition, the relay operating (I_{OP}) current increases dramatically by the summation the fault currents (I_F). The function of the relay is to attempt to distinguish between the normal error current and the fault current. This can be accomplished with a simple over-current relay.

Figure 2.19 – Basic 2-Terminal Current Differential Scheme

Top: Normal conditions, $I_{OP} = I_e'' - I_e'$

Bottom: Fault condition, $I_{OP} = I_{F1} + I_{F2} - (I_e' + I_e'')$

[4, {6.2}]

This scheme however, does not function well when the number of terminals increases beyond two. In a normal bus configuration, there are generally three or more terminals. In this case, a close-in external fault with high fault current could cause one C.T. to go into saturation while the others operate linearly. This can cause high operating current (I_{OP}) and cause the relay to improperly trip for an external fault. To avoid this, the over-current relay must either have a very high 'pick-up' current or be a time-delay relay. As the fault current levels at busses are typically quite high, these approaches are generally discouraged. The following section will detail a useful approach to help overcome this problem.

2.7.2 The Percentage Differential Relay

The main issue with differential protection is the problems caused by current transformer measurement errors. When applying differential protection, great care should be taken to properly specify the C.T.s, to keep them as close to identical as possible and to minimize the relay burdens. All of these things will help to minimize the errors between C.T.s which can cause relay mis-operation. Unfortunately, it is rarely possible to ensure that protection C.T.s will never saturate. That being said, there are a few methods to help deal with this.

The most commonly used method to help account for C.T. error is to 'restrain' the relay operation based on the magnitude of the current flowing through the zone terminals. This is known as percentage differential relaying. In this scheme, the relay's operating criteria (I_{OP}) must be greater than a percentage of the relay's restraining current (I_R). In traditional electromechanical relays, the restraining current was typically the average of the zone terminal currents. In microprocessor based relays, the restraining current is typically the maximum zone terminal current. The percentage can be set by the designer and is typically set at the maximum expected measurement error plus a safety margin. Typically the restraint percentage is set within the range of 10-40%.

Figure 2.20 – Percentage Differential Scheme

Left: external fault, Right: internal fault

[4, {6.2}]

Figures 2.20 and 2.21 demonstrate the electromechanical basis of the percentage differential relay scheme. The operating coil (OP) and the restraining coils (R) are all non-directional. Current flowing through the operating coil will work to cause the relay to operate while the current flowing through the restraint coils will work to prevent the relay from operating. The percentage of restraint is set by coil taps on the relay itself.

Figure 2.21 – Electromechanical Percentage Differential Relay

[5, 222]

2.7.3 The Directional Differential Relay

Percentage differential relaying is widely used and quite effective at reducing nuisance trips due to C.T. saturation. Despite this, a badly saturated C.T. can still cause a nuisance trip. Another method to deal with this problem is to determine the directionality of the current at each terminal. If all current is heading into the protected zone, then there is an internal fault. If at least one current waveform is heading out of the protected zone then there is no fault within the zone. This supervisory scheme can eliminate the problems associated with C.T. errors (saturation). This is due to the fact that even under severe saturation, the phase of the fault current produced by the C.T. secondary is still relatively accurate.

Figure 2.22 – C.T. Secondary Waveforms During a Fault

Top: Unsaturated, Bottom: Saturated

[10, 10]

It can be seen in Figure 2.22 that the phase of the saturated secondary waveform will be shifted in the leading direction. Logically, it can be stated that the magnitude of this shift will always be less than 90° . Thus, if the polarizing source is taken as one of the other current waveforms from the same bus, the directional principles discussed in Section 2.6 will be able to accurately detect the relative direction regardless of this phase shift.

Historically however, this approach was rarely used due to the complexity necessary to implement it. It required an electromechanical directional relay for each phase of each terminal and the settings, wiring and coordination of the relays became extremely complex. This limited its use to only a few problem applications. Modern microprocessor-based relays, like the GE Multilin B30, are able to implement this functionality with little added complexity. In newer applications, this approach can be easily used to increase security and ease the tolerances on the C.T.s.

Other differential schemes have been developed including high impedance relays and relays with saturation detection to provide immunity from the effects of saturation [11, 5]. These types of relays will not be discussed in this report.

2.8 Distance Protection – ANSI 21

Distance relays are normally used to protect high-voltage transmission and sub-transmission-level power lines [5, 100]. Distance relays are, however, increasingly being used in lower voltage applications [3, {12.12}]. Distance relays measure the impedance between the relay location and the fault location. As the impedance/km of a transmission lines remains relatively constant, these relays essentially respond to the ‘distance’ to a fault. This protection philosophy has found favor as the set-points are based on the line impedance which is relatively constant and easy to determine. As these set-points do not vary considerably with load currents or short-circuit levels, distance relay settings can remain constant regardless of many changes in the transmission network. This section will explore the necessary concepts to develop distance protection relays.

2.8.1 Theory of Distance Protection

The fundamental principle of distance relaying is as follows:

“Regardless of the type of fault involved, the voltage and current used to energize the appropriate relay are such that the relay will measure the positive-sequence impedance to the fault.” [5, 107]

With this principle, the zone settings of all relays can be based upon the positive-sequence impedance of the line and will perform consistently regardless of the fault type involved. To implement this principle, one must determine the appropriate current and voltage inputs and algorithm required to measure the positive-sequence impedance of the line. In normal balanced operation, the phase voltage and current can be directly used to calculate the positive-sequence impedances via Ohm’s Law. The previous sections have demonstrated that under fault conditions, severe distortions of the voltage and current waveforms are possible. These distortions result in the creation of negative and zero-sequence voltages and currents. The presence of the negative and zero-sequence components prohibits the direct use of Ohm’s Law to calculate the positive-sequence impedance. As it is not possible to directly measure only the

positive-sequence phase currents and voltages, several algorithms will need to be developed to facilitate these measurements under the various fault conditions. The following section will examine the possible fault types and develop the appropriate algorithm to measure the positive-sequence impedance to the fault in each case.

Phase-to-Phase Ungrounded Fault: For the purposes of this calculation, consider a fault between phases 'b' and 'c' as shown in Figure 2.7. By setting the fault impedance $Z_x = 0$ the phase-to-phase fault can be represented by the sequence network shown in Figure 2.23. The positive and negative-sequence voltages at the faulted bus are equal and given by:

$$E_{1F} = E_{2F} = E_1 - Z_{1F}I_1 = E_2 - Z_{1F}I_2$$

$$\frac{E_1 - E_2}{I_1 - I_2} = Z_{1F}$$

$$\text{Recall that: } E_b = E_0 + a^2E_1 + aE_2 \quad \text{and} \quad E_c = E_0 + aE_1 + a^2E_2$$

$$\text{Therefore: } E_b - E_c = (a^2 - a)(E_1 - E_2) \quad \text{and} \quad I_b - I_c = (a^2 - a)(I_1 - I_2)$$

After making the necessary substitutions, the following result develops:

$$\frac{E_b - E_c}{I_b - I_c} = \frac{E_1 - E_2}{I_1 - I_2} = Z_{1F_{bc}} \quad \text{Eq.\#1b}$$

Figure 2.23 – Symmetrical Component Circuit for Phase b and c Fault

[5, 107]

Thus a distance relay reading the line-line voltage between phases 'b' and 'c' and the difference between the currents in the two phases will measure the positive-sequence impedance between the phases when a b-c fault occurs. Similar analysis will show this to be true for the other two types of phase-to-phase faults.

$$\frac{E_a - E_b}{I_a - I_b} = \frac{E_1 - E_2}{I_1 - I_2} = Z_{1F_ab} \quad \text{Eq.\#1a}$$

$$\frac{E_b - E_c}{I_b - I_c} = \frac{E_1 - E_2}{I_1 - I_2} = Z_{1F_bc} \quad \text{Eq.\#1b}$$

$$\frac{E_c - E_a}{I_c - I_a} = \frac{E_1 - E_2}{I_1 - I_2} = Z_{1F_ca} \quad \text{Eq.\#1c}$$

Phase-to-Ground Fault: For the purposes of this calculation, consider a fault between phase 'a' and ground as shown in Figure 2.7. By setting the fault resistance $Z_x = 0$ the phase-to-ground fault can be represented by the sequence network shown in Figure 2.24. The voltages and currents in the three sequence networks at the relay location can be given as:

$$E_{1F} = E_1 - Z_{1F}I_1$$

$$E_{2F} = E_2 - Z_{1F}I_2 \quad \text{*assumes } Z_{1F} = Z_{2F}, \text{ which is normally the case.}$$

$$E_{0F} = E_0 - Z_{0F}I_0$$

Recalling that at the fault point (F), the voltage of phase 'a' equals zero (ie. $E_{1F} = E_{2F} = E_{0F} = 0$):

$$E_1 = Z_{1F}I_1$$

$$E_2 = Z_{1F}I_2$$

$$E_0 = Z_{0F}I_0$$

Figure 2.24 – Symmetrical Component Circuit for Phase 'a' to Ground Fault

[5, 107]

Thus, the voltage of phase 'a' at the relay location A is given by:

$$E_a = E_1 + E_2 + E_0 = Z_{1F}(I_1 + I_2) + Z_{0F}I_0$$

$$E_a = Z_{1F}(I_1 + I_2 + I_0) + (Z_{0F} - Z_{1F})I_0$$

$$E_a = Z_{1F}(I_a) + (Z_{0F} - Z_{1F})I_0$$

$$E_a = Z_{1F}[I_a + \frac{Z_{0F}-Z_{1F}}{Z_{1F}}I_0]$$

$$\text{Define: } m = \frac{Z_{0F}-Z_{1F}}{Z_{1F}}$$

$$E_a = Z_{1F}[I_a + mI_0]$$

Therefore:

$$\frac{E_a}{I_a + mI_0} = Z_{1F_a}$$

Eq.#2a

The factor of 'm' introduced is commonly referred to as the compensation factor. The compensation factor compensates the current measurement for the effects of the mutual coupling between the faulted phase and the two un-faulted phases. This coupling is determined by many factors such as conductor spacing, conductor arrangement and voltage level. An analysis of transmission line design factors which influence this coupling is beyond the scope of this report. This report will simplify this phenomenon by using typical values. The 'm' factor for most overhead transmission lines ranges from 1.5 to 2.5. A frequently used value is m=2 which corresponds to $Z_0 = 3Z_1$ [5, 110].

Thus a distance relay reading the phase 'a' voltage, phase 'a' current and the compensated zero-sequence current (either from a ground C.T. or the residual of the three-phase C.T.s) will measure the positive-sequence impedance to ground when a phase 'a'-to-ground fault occurs. Similar analysis can be employed to show this to be true for the other two types of phase-to-ground faults as well.

$$\frac{E_a}{I_a + mI_0} = Z_{1F_a}$$

Eq.#2a

$$\frac{E_b}{I_b + mI_0} = Z_{1F_b}$$

Eq.#2b

$$\frac{E_c}{I_c + mI_0} = Z_{1F_c}$$

Eq.#2c

Three-Phase Fault (Ungrounded and Grounded): For the purposes of this calculation, the three-phase fault will be assumed to be a balanced fault. Furthermore, a fault impedance of zero will be assumed (i.e. $Z_y = Z_x = 0$ referring to Figure 2.7). In the ungrounded case Z_n will be open circuited and in the grounded case Z_n will be short circuited. The full sequence network for the grounded three-phase fault is shown in Figure 2.9. Regardless of grounding, the positive-sequence network becomes shorted to itself resulting in no current flowing the negative and zero-sequence networks. Thus, the sequence network for the grounded and ungrounded three-phase fault can be simplified as shown in Figure 2.25. The positive-sequence voltage at the relay location 'A' is given by:

$$E_1 = E_a = Z_{1F} I_1 = Z_{1F} I_a$$

$$\frac{E_1}{I_1} = \frac{E_a}{I_a} = Z_{1F} \quad \text{Eq.\#3}$$

The above result is valid, however, a result in the form of Eq.#1 and/or Eq.#2 (above) would be preferred. By taking into account that:

$$E_2 = E_0 = 0 \text{ and } I_2 = I_0 = 0 \quad (\text{in this case})$$

$$E_a = E_1, E_b = a^2 E_1 \text{ and } E_c = a E_1 \quad (\text{in this case})$$

Figure 2.25 – Symmetrical Component Circuit for Three-Phase Fault

[5, 108]

It can be observed that Eq.#1 and Eq.#3 are equivalent during a three-phase fault as E_2 and I_2 equal zero. Hence:

$$\frac{E_a - E_b}{I_a - I_b} = \frac{E_b - E_c}{I_b - I_c} = \frac{E_c - E_a}{I_c - I_a} = Z_{1F} \quad \text{Eq.\#1 a-c}$$

It can be also be observed that Eq.#2 and Eq.#3 are equivalent during a three-phase fault as I_0 equals zero. Hence:

$$\frac{E_a}{I_a + m I_0} = \frac{E_b}{I_b + m I_0} = \frac{E_c}{I_c + m I_0} = Z_{1F} \quad \text{Eq.\#2 a-c}$$

Double Phase-to-Ground Fault: For the purposes of this calculation, consider a fault between 'b' 'c' and ground as shown in Figure 2.7. As such, by setting the fault impedances to zero $Z_y = Z_n = 0$, the double phase-to-ground fault can be represented by the sequence network shown in Figure 2.26. The positive and negative-sequence voltages at the faulted bus are equal and given by:

$$E_{1F} = E_{2F} = E_1 - Z_{1F}I_1 = E_2 - Z_{1F}I_2$$

$$\frac{E_1 - E_2}{I_1 - I_2} = Z_{1F}$$

$$\text{Recall that: } E_b = E_0 + a^2E_1 + aE_2 \quad \text{and} \quad E_c = E_0 + aE_1 + a^2E_2$$

$$\text{Therefore: } E_b - E_c = (a^2 - a)(E_1 - E_2) \quad \text{and} \quad I_b - I_c = (a^2 - a)(I_1 - I_2)$$

After making the necessary substitutions, the following result develops:

$$\frac{E_b - E_c}{I_b - I_c} = \frac{E_1 - E_2}{I_1 - I_2} = Z_{1F} \quad \text{Eq.\#1}$$

Figure 2.26 – Symmetrical Component Circuit for Phase b and c to Ground Fault

2.8.2 Apparent Impedance Measurements

The above analysis has shown, for all faults involving two or more phases, Eq.#1 a-c can accurately measure the positive-sequence impedance to the fault. These three equations form the basis of what is known as the apparent impedance measurements for multi-phase faults. These equations are summarized in Table 2.5.

Table 2.5 – Apparent Impedance Equations for Multi-phase Faults

Equation		Suitable for Faults:
1a	$\frac{E_a - E_b}{I_a - I_b} = \frac{E_1 - E_2}{I_1 - I_2} = Z_{1F_{ab}}$	'a'-'b' Ungrounded 'a'-'b' Grounded 3-Phase Ungrounded 3-Phase Grounded
1b	$\frac{E_b - E_c}{I_b - I_c} = \frac{E_2 - E_3}{I_2 - I_3} = Z_{1F_{bc}}$	'b'-'c' Ungrounded 'b'-'c' Grounded 3-Phase Ungrounded 3-Phase Grounded
1c	$\frac{E_c - E_a}{I_c - I_a} = \frac{E_3 - E_1}{I_3 - I_1} = Z_{1F_{ca}}$	'c'-'a' Ungrounded 'c'-'a' Grounded 3-Phase Ungrounded 3-Phase Grounded

Similarly, for faults involving a single phase and ground, Eq.#2 a-c can accurately measure the positive-sequence impedance to the fault. These three equations form the basis of what is known as the apparent impedance measurements for phase-to-ground faults. These equations are summarized in Table 2.6.

Table 2.6 – Apparent Impedance Equations for Phase-to-Ground Faults

Equation		Suitable for Faults:
2a	$\frac{E_a}{I_a + mI_0} = Z_{1F_a}$	'a' to Ground
2b	$\frac{E_b}{I_b + mI_0} = Z_{1F_b}$	'b' to Ground
2c	$\frac{E_c}{I_c + mI_0} = Z_{1F_c}$	'c' to Ground

2.8.3 The ANSI 21 Protection Relays

The previous sections have demonstrated the methods which can be employed to calculate the apparent positive sequence impedance to a fault. It is possible to use the apparent impedance directly to implement distance protection by comparing the measured impedance with some type of impedance characteristic represented by a geometric shape, like a circle or box. Indeed this method been used in several commercially available protection relays. The performance of the apparent impedance approach, however, has been shown to suffer from many practical conditions of load flow and fault impedance [12]. Improved performance can be obtained by utilizing methods which resemble the operating and restraining torque characteristics of the proven electromechanical distance relays. Most modern microprocessor distance relays use methods similar to those detailed below.

The operating characteristics of distance relays can be obtained by either amplitude comparison or phase comparison of the sets of vectors derived from the current and voltage signals of the protected line. Equivalent performance is obtained in either case, however, phase comparison is more easily understood and more widely implemented in modern relays [13]. Hence, this project will focus on the phase comparison implementation alone.

A general distance relay characteristic is derived by a two-input phase comparator of vectors S_1 and S_2 below:

$$S_1 = I_r \angle (-\varphi) \cdot Z_R \angle \theta - K_1 V_r \angle 0$$

$$S_2 = K_2 V_r \angle 0 + K_3 I_r \angle (-\varphi) \cdot Z_R \angle \theta + K_4 V_{pol}$$

[14]

Where:

S_1	is the phasor of the operating voltage;
S_2	is the phasor of the polarization voltage;
I_r	is the current of the particular fault loop;
φ	is the angle by which the voltage phasor leads the current phasor;
$V_r \angle 0$	is the voltage of the particular impedance loop;

$Z_R \angle \theta$ is the reach of the distance detector;
 V_{pol} is the memory or cross-polarization voltage; and
 K_1, K_2, K_3 and K_4 are complex constants chosen to define the operating characteristic.

The parameters V_r and I_r are the appropriate loop voltages and currents as calculated in the previous sections. Examples are listed below:

$V_r = V_a - V_b$, for the A-B element;
 $I_r = I_a - I_b$, for the A-B element;
 $V_r = V_a$, for the A-Ground element; and
 $I_r = I_a + mI_0$, for the A-Ground element;

The angular displacement of vectors S_1 and S_2 is considered positive if S_1 leads S_2 . The phase comparator operates if the following condition is satisfied [15].

$$-90^\circ \leq \arg(S_1) - \arg(S_2) \leq 90^\circ$$

Or,

$$|\arg(S_1) - \arg(S_2)| \leq 90^\circ$$

The 'K' parameters of the vectors S_1 and S_2 define the shape, size and position of the distance characteristic in the impedance plane. These characteristics typically take the form of circles (e.g. impedance, mho and lens) and straight lines (e.g. reactance and quadrilateral). The development of the impedance and mho characteristics will be developed in the following subsections.

2.8.3.1 ANSI 21 Impedance Relay

The impedance relay characteristic is defined as a circle in the impedance plane with zero as its center. This characteristic is obtained by setting: $K_1, K_2, K_3 = 1$ and $K_4 = 0$. Hence:

$$S_1 = I_r \angle (-\varphi) \cdot Z_R \angle \theta - V_r \angle 0$$

$$S_2 = V_r \angle 0 + I_r \angle (-\varphi) \cdot Z_R \angle \theta$$

To represent the impedance relay characteristic, it is necessary to represent the voltage phasors S_1 and S_2 in the impedance plane. This is accomplished by dividing the above equations by the current I_r :

$$S'_1 = Z_R \angle \theta - Z_r \angle \phi$$

$$S'_2 = Z_r \angle \phi + Z_R \angle \theta$$

Where Z_r is the apparent impedance observed by the relay.

Figure 2.27 – Impedance Characteristic R-X Diagram

It is typical to display the operating characteristics of distance relays with an R-X diagram. The R-X diagram allows the characteristic to be represented with only two quantities, R and X (or Z and θ). This avoids the confusion of using three parameters E, I and θ . Figure 2.27(a) demonstrates an example of the impedance relay with the operating conditions met. It can be seen that with Z_r measured inside of the characteristic circle, the angular difference between S'_1 and S'_2 will be less than 90 degrees, which fulfills the operating condition. Figure 2.27(b) demonstrates an example of the impedance relay with the operating conditions not met. It can be seen that with Z_r measured outside of the characteristic circle, the angular difference between S'_1 and S'_2 will be greater than 90 degrees, which does not fulfill the operating condition. This simple geometric demonstration can be repeated for all points in the R-X plane to demonstrate

that only points falling within the characteristic circle, centered at the origin with radius of $|Z_R|$, will cause the relay to operate.

2.8.3.2 ANSI 21 Mho Relay

The mho relay characteristic is defined as a circle in the impedance plane which passes through the origin. This characteristic is obtained by setting: $K_1, K_2 = 1$ and $K_3, K_4 = 0$. Hence:

$$S_1 = I_r \angle (-\varphi) \cdot Z_R \angle \theta - V_r \angle 0$$

$$S_2 = V_r \angle 0$$

These phasors represent the simplest of mho characteristics, the self-polarized. It is called the self-polarized as the only phasor in the polarization vector (S_2) is the voltage of the impedance loop being measured. To represent the mho relay characteristic, it is necessary to represent the voltage phasors S_1 and S_2 in the impedance plane. Again, this is accomplished by dividing the above equations by the current I_r :

$$S'_1 = Z_R \angle \theta - Z_r \angle \varphi$$

$$S'_2 = Z_r \angle \varphi$$

Figure 2.28 – Mho Characteristic R-X Diagram

a) Operating Condition

b) Non-operating Condition

Figure 2.28(a) demonstrates an example of the mho relay with the operating conditions met. It can be seen that with Z_r measured inside of the characteristic circle, the angular difference between $S1'$ and $S2'$ will be less than 90 degrees, which fulfils the operating condition. Figure 2.28(b) demonstrates an example of the mho relay with the operating conditions not met. It can be seen that with Z_r measured outside of the characteristic circle, the angular difference between $S1'$ and $S2'$ will be greater than 90 degrees, which does not fulfill the operating condition. This simple geometric demonstration can be repeated for all points in the R-X plane to demonstrate that only points falling within the characteristic circle, centered at $\frac{Z_R \angle \theta}{2}$ with a radius of $\frac{|Z_R|}{2}$, will cause the relay to operate.

2.8.3.3 Dynamic Performance of Memory-Polarized Mho Characteristics

One of the key benefits of using the mho characteristic and the methods identified in Section 2.8.3.2 is the dynamic shift that can be obtained during faults. If the polarizing source is memorized from a pre-fault value, the mho characteristic will include a dynamic shift during various faults.

Figure 2.29 – Dynamic Shift In Memory-Polarized Mho Characteristic

If it is assumed that the characteristic depicted in Figure 2.29 is a forward zone, it can be seen that this shift provides a desirable shift away from the origin during reverse faults. This will help to ensure directional integrity. Also, during forward faults the characteristic will shift in the negative direction to increase coverage for resistive faults. For this reason, memory-polarized mho characteristics are generally recommended [17]. This report will utilize memory-polarization in all developed models.

2.9 Phasor Estimation

All of the relay algorithms introduced will require a phasor estimation of the appropriate power system waveforms (voltage and current) to function properly. Each algorithm makes use of the magnitude and/or phase of the voltage and current waveforms to provide protection. Estimation of these phasors is integral to the functionality of almost all modern microprocessor protection relays. There are many algorithms available to obtain this estimation but few are as pervasive as the Fourier Transform. The Fourier Transform functions on the premise that any periodic function can be represented by a linear combination of two orthogonal functions. The Fourier Transform uses sine and cosine functions which are well-known orthogonal functions. This transformation allows any periodic function to be represented by a fundamental frequency and a series of harmonic frequencies. A useful simplification to the evaluation of the entire Fourier series allows the magnitude of any particular component frequency to be evaluated as follows [3, {5.2}]:

$$a_n = \frac{2}{T_0} \int_{-T_0/2}^{T_0/2} f(t) \cos(n\omega t) dt$$

$$b_n = \frac{2}{T_0} \int_{-T_0/2}^{T_0/2} f(t) \sin(n\omega t) dt$$

$$f_n(t) = a_n \cos(\omega_n t) + b_n \sin(\omega_n t)$$

Where $f(t)$ is the original waveform, T_0 is the period of the waveform and 'n' is the order of the harmonic. The sum of the product of the orthogonal set and the function, taken over the fundamental period, produces a total that contains only the desired frequency. This will allow the evaluation of the magnitude and phase of a desired frequency (i.e. 50Hz or 60Hz) to be extracted from a distorted waveform with all other frequencies excluded.

In microprocessor relays this process is implemented discretely using sampled waveforms. If a voltage waveform (V) is sampled N times over the fundamental period with a step size of Δt , then the Real and Imaginary components of the phasor are defined as follows:

$$\text{Re}(V) = \frac{2}{N} \sum_{i=1}^N v_i \sin(\omega i \Delta t)$$

$$\text{Im}(V) = \frac{2}{N} \sum_{i=1}^N v_i \cos(\omega i \Delta t)$$

These equations form the basis for what is known as the Discrete Fourier-Notch Filter [3, {5.3}]. The rectangular components are easily converted into the required polar form. The magnitude represents the peak waveform amplitude while the phase will be referenced to the phase of the orthogonal set used in the multiplication. In absolute terms, the resulting phase angle is of little use as it is not properly referenced to any power system phasor. To be of practical use, the phase angles must always be compared to the phase angles of other power system phasors to obtain a relative angle. This Discrete Fourier-Notch Filter will be a fundamental building block in the modeling of all protection relays in this report.

Chapter 3 – Modeling of the Protection System

This chapter will present the MATLAB/Simulink models developed to allow simulation of the protection systems. The chapter will present models for various differential relays, phase distance relays and ground distance relays. Additionally, a model will be presented for a saturable current transformer.

3.1 Instrument Transformers

With the analysis completed in Section 2.5, it is necessary to develop models for the realistic instrument transformers. For this project, it will be assumed that a standard (non-C.C.V.T.) voltage transformer will be used. As such, it will be assumed that the potential transformer is error free. With this assumption, the built-in Simulink models for voltage measurement will be sufficient. The current transformer however, will be assumed to have a realistic, saturable iron-core. Saturation is the predominant non-linear effect in iron-core transformers [18, 1]. The lesser non-linear effects of eddy current and hysteresis will not be modeled. The following section will present a Simulink model of a saturable current transformer.

3.1.1 Saturable Current Transformer

Simulink does not include a specific model for a saturable C.T. Simulink does however include a saturable two-winding transformer model which can be used to construct a saturable C.T. The saturable transformer model accounts for saturation through the use of a time-variant, primary-side inductance ' L_{SAT} '. The model accepts pairs of peak flux and peak magnetizing current values and performs a linear interpolation to acquire the saturation performance. The equivalent circuit of the saturable transformer model is shown in Figure 3.1.

Figure 3.1 – Simulink Saturable Transformer Model

[19]

The developed model for a saturable two-winding transformer used as a saturable C.T. is shown in Figure 3.2. Notice that the power system is connected in series with the primary winding (which does not physically exist in most actual C.T.s). Nonetheless, the fictitious primary winding allows for the necessary coupling between the power system and the C.T. secondary. It will be assumed that the C.T.s will be wye-connected at the station. This means that regardless of the type of fault, the connected burden will include two-times the one-way lead burden.

Figure 3.2 – Saturable Current Transformer Model

The obvious extension to model above is the three-phase C.T. shown in Figure 3.3. Notice that the secondary currents are all scaled to their equivalent primary currents. This is a common feature of microprocessor relays that allow all set-points and measurements to be provided in equivalent primary quantities. Also included is the 'M1' measurement block which will provide the phase voltage measurements as well as the ideal current measurements that will be used to assess the performance of the saturable C.T.

Figure 3.3 – Three-Phase Saturable Current Transformer Block

3.1.1.1 Instantaneous Current Transformer Saturation Parameters

To properly model the dynamic performance of a C.T. using Simulink (or other simulation packages) it is necessary to provide the relationship between the flux and the magnetization current. A problem arises due to the fact that manufacturers will not provide this relationship due to the difficulties involved with measuring these values. Instead, manufacturers will provide an R.M.S. excitation curve similar the curves in Figure 2.17. The methods used to measure these excitation voltages and currents are standardized across the industry by IEEE standard C57.13-1993(R2003) [20]. Manufacturers are very reluctant to provide any additional performance information. As such, to model the current transformer in the Simulink environment, the following parameter translations must be made:

- It will be assumed that the excitation losses (dielectric and core losses) are negligible (ie. $I_{LOSS}=0$ referring to Figure 2.16). This allows the excitation current to equal the magnetization current (ie. $I_E = I_M$).
- Translation of the R.M.S. excitation (V_s , I_s) curve into the peak flux linkage versus peak magnetizing current (λ , i) curve. This translation will be undertaken in the following section.

In Table 2.2, the effects of saturation were summarized by showing the disproportionate increase in excitation current with increasing excitation voltage on an RMS basis. That demonstration is overly simplified for modeling purposes. In actuality, the excitation current will vary

dramatically with the instantaneous value of the core flux as saturation increases. Figure 3.4 demonstrates this effect. Thus, it becomes necessary to obtain the relationship between the instantaneous flux linkage and instantaneous magnetizing current to properly model the transformer during saturation.

Figure 3.4 – Instantaneous C.T. Flux and Magnetization Current

(left: Unsaturated, right: Saturated)

Several studies were undertaken to understand and model saturation in transformers. Various approaches and algorithms have been produced and verified by lab experiments [21], [22] and [23]. The approach by Prusty and Rao allows for a direct piecewise linearized method to convert R.M.S. saturation characteristics to an instantaneous saturation curve [24]. The method converts the continuous R.M.S. (V, I) curve to a piecewise (λ, i) curve. Selected points on the R.M.S. curve $(V_1, I_1), (V_2, I_2), \dots, (V_N, I_N)$ will be translated to points $(\lambda_1, i_1), (\lambda_2, i_2), \dots, (\lambda_N, i_N)$ on the instantaneous curve (See Figure 3.5). The steps of this method will be detailed below.

Figure 3.5 – Piecewise Linear Construction of the Instantaneous Saturation Curve

[24]

All peak flux linkage points can be directly translated by a simple rescaling procedure:

$$\lambda_n = \frac{\sqrt{2}V_n}{\omega}$$

The first peak current must be chosen in the linear region and can be calculated by:

$$i_1 = \sqrt{2}I_1$$

If K_n denotes the slope of the segment, the current can be represented as follows:

$$i_1 = K_1 \lambda_1 \sin \theta$$

Notice that R.M.S. value can be related to the peak value using ¼ wave symmetry:

$$I_1 = \left[\frac{2}{\pi} \int_0^{\pi/2} K_1^2 \lambda_1^2 \sin^2 \theta d\theta \right]^{1/2}$$

The method proposes the following general form for calculating the slope of the N'th segment (K_N) by equating the N'th segment's R.M.S. value to the piecewise R.M.S. contributions of the previous N-1 segments:

$$\begin{aligned} \frac{\pi}{2} I_N^2 = & \int_0^{\theta_1} (K_1 \lambda_N \sin \theta)^2 d\theta + \int_{\theta_1}^{\theta_2} \{i_1 + K_2 (\lambda_N \sin \theta - \lambda_1)\}^2 d\theta \\ & + \dots + \int_{\theta_{n-1}}^{\theta_n} \{i_{n-1} + K_n (\lambda_N \sin \theta - \lambda_{n-1})\}^2 d\theta \\ & + \dots + \int_{\theta_{N-1}}^{\pi/2} \{i_{N-1} + K_N (\lambda_N \sin \theta - \lambda_{N-1})\}^2 d\theta \end{aligned} \quad (\text{Eq. 3.1})$$

Where:

$$i_n = K_n (\lambda_n - \lambda_{n-1}) + K_{n-1} (\lambda_{n-1} - \lambda_{n-2}) + \dots + K_1 \lambda_1$$

$$\theta_n = \sin^{-1} \left(\frac{\lambda_n}{\lambda_N} \right)$$

Equation 3.1 can be simplified as:

$$A_N K_N^2 + B_N K_N + C_N = 0$$

Where:

$$K_N = \frac{-B_N + \sqrt{B_N^2 - 4A_N C_N}}{2A_N}$$

$$A_n = \frac{\lambda_N^2}{2} (t_n - s_n) + 2\lambda_N \lambda_{n-1} g_n + \lambda_{n-1}^2 t_n$$

$$B_n = -2i_{n-1} (\lambda_N g_n + \lambda_{n-1} t_n)$$

$$C_N = d_N + \left\{ \sum_{n=1}^{N-1} (A_n K_n^2 + B_n K_n + d_n) \right\} - \frac{\pi}{2} I_N^2$$

$$d_n = t_{n-1}^2 t_n$$

$$t_n = \theta_n - \theta_{n-1}$$

$$s_n = \frac{1}{2} (\sin 2\theta_n - \sin 2\theta_{n-1})$$

$$g_n = \cos \theta_n - \cos \theta_{n-1}$$

Thus, by successive evaluations of the interval slope K_N , it is possible to construct the set of peak flux linkage and magnetizing current (λ_1, i_1) , (λ_2, i_2) , ... (λ_N, i_N) . This computation of the instantaneous saturation curve is usually completed using 5 to 15 segments and is cumbersome to

manually calculate. The ElectroMagnetic Transient Program (EMTP) and the Alternative Transients Program (ATP) contain functions SATURATION (in EMTP) and SATURA (in ATP) to obtain the instantaneous saturation parameters from the R.M.S. saturation parameters [25, 3], [26, 3]. As an alternative to the use of these programs, a spreadsheet has been developed to implement the approach of Prusty and Rao. Table 3.1 shows an abbreviated version of the spreadsheet for the 1200:5 C.T. which was detailed in Figure 2.17 and Table 2.2. The complete spreadsheets have been included in Appendix A.

Table 3.1 – Calculation of the Instantaneous Saturation Parameters for a Typical 1200:5 Current Transformer

N	1	2	3	4	...	14	15
Is,rms (A)	0.002	0.005	0.01	0.02	...	50	100
Vs,rms (V)	2.8	12	32.5	95	...	525	550
Kn	0.26927937	0.108947753	0.064717303	0.050843694	...	685.858204	1149.553015
An	8.72542E-06	0.000810582	0.003629605	0.034494223	...	0.001450088	0.001416637
Bn	0	0.000168279	0.000785558	0.004300742	...	2.265456713	4.643751176
Cn	-2.85876E-05	-2.79549E-05	-6.60411E-05	-0.000307836	...	-2235.90544	-7210.284769
theta, n (°)	13.49339882	90	90	90	...	90	90
theta, n-1 (°)	0	13.49339882	21.66818466	20.00519009	...	72.24720984	72.6585572
dn	0	1.06823E-05	5.17686E-05	0.000163403	...	1062.766846	4570.687682
tn (rad)	0.235504237	1.33529209	1.192615162	1.221639892	...	0.30984464	0.302665274
sn	0.226892589	-0.226892589	-0.343140089	-0.321463191	...	-0.290391122	-0.284516961
gn	-0.02760319	-0.97239681	-0.929337742	-0.939661635	...	-0.304910678	-0.298065387
Cn Summation Term	6.32692E-07	3.86372E-05	0.00011781	0.000471239	...	3298.672286	11780.97245
Flux-linkage,rms (Wb*turns)	0.007427231	0.031830989	0.086208928	0.251995327	...	1.392605752	1.458920312
Flux-linkage,pk (Wb*turns)	0.0105	0.0450	0.1219	0.3564	...	1.969	2.063
Is,pk (A)	0.0028	0.0066	0.0116	0.0235	...	122.9	230.7
Parameters for Simulink:							
Turns Ratio (Ns/Np)=	240	1200:5					
Ip,pk (A)	0.6788	1.581	2.776	5.637	...	29493	55367
Flux,pk (Wb)	4.38E-05	1.88E-04	5.08E-04	1.48E-03	...	8.21E-03	8.60E-03

The bottom four rows complete the transformation of the parameters into those required for simulation in Simulink. Simulink requires pairs of peak flux and peak primary magnetizing current. The flux is obtained by dividing the secondary flux linkage by the number of secondary turns. The primary magnetizing current is obtained by multiplying the secondary magnetizing current by the turns ratio (Ns/Np). Table 3.2 summarizes the transformation to instantaneous parameters for the 1200:5 C.T. which was detailed in Figure 2.17 and Table 2.2.

Table 3.2 – Typical 1200:5 Current Transformer Instantaneous Flux and Magnetizing Current Relationship

Vs,rms (V)	Flux,peak (Vs)	Ie,sec,rms (A)	Im,sec,peak (A)	Im,pri,peak (A)
2.8	4.38E-05	0.002	0.0028	0.679
12	1.88E-04	0.005	0.0066	1.581
32.5	5.08E-04	0.01	0.0116	2.776
95	1.48E-03	0.02	0.0235	5.637
335	5.24E-03	0.05	0.0633	15.18
410	6.41E-03	0.1	0.1710	41.05
420	6.56E-03	0.2	0.5860	140.6
435	6.80E-03	0.5	1.3513	324.3
450	7.03E-03	1	2.4848	596.3
460	7.19E-03	2	5.7344	1376
475	7.42E-03	5	13.909	3338
490	7.66E-03	10	25.342	6082
500	7.82E-03	20	58.566	14056
525	8.21E-03	50	122.89	29493
550	8.60E-03	100	230.70	55367

Extrapolated

Table 3.2 and Figure 3.6 demonstrate the non-linear relationship between the RMS magnetizing current and the peak magnetizing current. It can be clearly seen that the peak current as a ratio of the RMS current will increase dramatically as the transformer core saturation increases. The relationship developed in this section will provide the necessary basis to allow for simulation of the saturable current transformer.

Figure 3.6 – Typical 1200:5 Current Transformer

Instantaneous Flux versus Secondary Magnetizing Current (RMS and Peak)

3.2 Differential Protection

With the principles introduced in Section 2.7, it is now possible to construct a MATLAB Simulink model for an ANSI 87B bus differential relay. The following subsections will introduce the relay models for several different implementations of bus differential protection.

3.2.1 Unrestrained Differential

The unrestrained differential relay is the simplest implementation of differential protection. It is frequently referred to as a differential over-current relay. The relay simply defines a maximum acceptable differential current (I_D) which is known as the pick-up current. When the pick-up current has been exceeded, an on-delay timer is initiated. When the timer completes, the trip signal (52-TC) is initiated.

Figure 3.7 – Sample Unrestrained Differential Relay Characteristic

Figure 3.8 – Unrestrained Differential Relay Model

Figure 3.8 shows the relay model developed to implement the unrestrained differential relay for a 3-terminal bus. The model can be expanded to allow for an increased number of terminals by adding the appropriate phase currents to each summation block. Different polarity C.T.s can be compensated with an inversion block as shown. The summation blocks will sum all current waveforms to produce the waveform of the differential (i.e. error) current. Each discrete Fourier block will sample the differential waveform 64-times per power cycle and calculate the waveform magnitude at 60Hz using the method described in Section 2.9. This is the same method used in one of the industry leading protection relays, the GE Multilin B30 [27, {8.3.2}]. The three differential amplitudes are scaled to RMS and fed into comparison blocks to check if they exceed the pick-up current. A value exceeding the pick-up current will start an on-delay timer which will initiate the trip (52-TC) if the timer completes.

Notice high-pass filters that have been added to the current inputs. As there can be a significant DC component to fault currents, it is desirable to filter this out to ensure that the calculations are not adversely affected. In this case, the filters are all 1st order with a cut-off of 1Hz for the high-pass filters. These values represent very conservative filtering choices. Most commercially available microprocessor-based relays employ sophisticated and often proprietary filtering techniques. As an example, the GE Multilin D30 uses a modified MIMIC-type digital filter [28, {8.1.2}]. Input filtering can greatly improve the transient performance of micro-processor based relays. As this project is not primarily concerned with signal analysis techniques, only simple and conservative filtering has been employed.

The unrestrained differential relay is effective to demonstrate the basic concept of differential relaying. However, it would rarely be used for transmission-level applications. This relay provides little immunity from measurement errors (C.T. errors, ratio mismatch, saturation, and etc.). As such, the pick-up current and time delay must frequently be set quite high to ensure system security. These high set-points limit the application of this relay to lower-voltage distribution applications where fault currents and D.C. offsets are small. As this project is focused on transmission-level applications, the focus will shift to relays suitable for transmission-level applications rather than the unrestrained differential relay.

3.2.2 Restrained Differential

The restrained differential relay improves upon the previous relay by accounting for many of the expected errors which vary with increasing current. This approach can account for all types of errors which can be simplified and assumed to vary linearly up to 20 x the Rated Current. These errors can include the standard protection C.T. error (10% @ 20 x Rated Current), any errors due to ratio mismatches among the bus terminals and any errors caused by the use of auxiliary C.T.s. Section 2.7.2 described the theory behind restrained (percentage) differential relays. The general characteristic of this type of relay is shown in Figure 3.9.

Figure 3.9 – Sample Restrained Differential Relay Characteristic

It should be evident when comparing Figure 3.7 and 3.9 that the restrained differential relay allows for a significantly lower setting of the pick-up current (I_{PU}). This allows the relay of respond to smaller differential fault currents while still maintaining security. Figures 3.10 and 3.11 demonstrate the models developed to implement the restrained differential relay characteristic.

Figure 3.10 – Restrained Differential Relay Model

Figure 3.11 – Contents of Phase Blocks Shown in Figure 3.10

Figure 3.10 exhibits the restrained differential relay model. This model is very similar to the unrestrained model with two main additions. First, each phase element calculates its restraining current as the maximum RMS current measured by all of the bus terminals. Second, the comparisons to initiate the trip-delay timers are driven by the maximum of the pick-up current and the percentage restraining current. This effectively implements the characteristic of Figure 3.9.

3.2.3 Restrained Directional Differential

It is important to note that the restrained differential relay is still not immune to the affects of C.T. saturation due to the D.C. component of fault waveforms. A close-proximity, out-of-zone fault with significant D.C. offset, can still drive and C.T. into saturation and cause the differential protection to improperly trip. For this reason, the time delay would still need to be large enough to allow the out-of-zone protection to clear any out-of-zone faults before initiating the trip. This time delay can be intolerable in many applications. As such, several approaches including the directional differential relay have been developed to provide immunity to this problem. The restrained directional differential relay has the same characteristic of the restrained differential relay. What differentiates the restrained directional differential relay is the addition of a directional permissive to initiate a trip. With the directional permissive, the relay time delay can be minimized or eliminated to greatly reduce the possibility of equipment damage. The model for this relay is shown in Figures 3.12 and 3.13.

Figure 3.12 – Restrained Directional Differential Relay Model

This model is very similar to the restrained model with addition of the directional permissives (i.e. 'AND' gates) which enable and disable the trip output.

Figure 3.13 – Contents of Phase Blocks Shown in Figure 3.12

Figure 3.13 exhibits the contents of each phase block. Notice that each phase's RMS current is fed into a 'LESS-THAN' comparison block. These blocks determine which currents will be used in the directional test. If a terminal is out of service, the phase of that current will be unpredictable and should not be used in the directional check. The magnitude check will flag any currents below a minimum value such that they are assumed to meet the directional criteria regardless of phase. The lower section of logic implements the actual directional check. With the terminal out of service problem, this logic becomes relatively complex as it must cover all possible terminal status combinations. This complexity is the main reason this scheme is rarely implemented with electromechanical relays. The phases of each current waveform are

differenced and tested to see if each waveform is in-phase or not. In-phase waveforms will difference to approximately zero while out-of-phase waveforms will difference to approximately $\pm 180^\circ$. The interval test will check that the differences fall in the range of -90° to $+90^\circ$. If all tests are 'true' then all currents are flowing into the bus (i.e. there is a fault present). If at least one current is flowing out of the bus, then the situation is normal.

3.3 Phase Distance Protection

With the analysis completed in Section 2.8, it is now possible to construct a MATLAB Simulink model for an ANSI 21P phase-distance relay. The following subsections will introduce the relay models for several different implementations of phase-distance protection.

3.3.1 Directional Phase Impedance Characteristic

The impedance characteristic is the simplest implementation of distance protection. The typical characteristic is displayed in Figure 2.27. It simply defines a minimum impedance; if any measurement produces a result smaller than the minimum impedance, the relay will initiate corrective action (i.e. trip/time-delayed trip). The impedance relay is effective to demonstrate the basic concept of distance relaying. However, it is rarely used in practical applications. The impedance relay is non-directional and therefore it cannot distinguish between upstream or downstream faults. As directionality is essentially mandatory in dual transmission line applications, a relay based on this characteristic would be of little use in this project.

The impedance relay can be made into a practically useful relay with the addition of directional elements. A directional element for a phase relay determines the direction to a fault using the method described in Section 2.6. Figure 3.14 demonstrates a sample directional impedance characteristic. It can be seen that with the directional characteristic several overlapping forward and reverse zones of protection are possible. The reasons and rationale for this will be explained in Section 4.5 when the set-points for the relays are being developed.

Figure 3.14 – Sample Directional Characteristic R-X Diagram

Notice in Figure 3.14 that with the line of directionality positioned perpendicular to the line impedance, the relay will improperly detect the directionality of normal power flow for some leading power factors. As the relay is un-concerned with normal power flow, this is not an issue. Having the line of directionality situated perpendicular to the transmission line impedance will allow for the most accurate directional decisions for forward and reverse faults.

Figure 3.15 shows the relay model developed to implement the directional phase impedance relay algorithms. All of the 'delta' values are calculated by differencing the appropriate waveforms and fed into corresponding relay elements. Notice that three high-pass filters have been added to the current inputs. As there is a significant DC component to fault currents, it is desirable to filter this out to ensure that the calculations are not adversely affected. In this case, the filters are all 1st order with a cut-off of 1Hz for the high-pass. These values represent very conservative filtering choices. Most commercially available microprocessor-based relays

employ sophisticated and proprietary filtering techniques. As an example, the GE Multilin D30 uses a modified MIMIC-type digital filter [28, {8.1.2}]. Input filtering can greatly improve the transient performance of micro-processor based relays. As this project is not primarily concerned with signal analysis techniques, only simple and conservative filtering has been employed.

Figure 3.15 – Directional Phase Impedance Relay Model

Notice that the polarizing source for each element will be the positive sequence voltage. The phase angle of the positive sequence voltage has been compensated for each element to produce a polarizing source which is in-phase with the element's operating voltage. Use of the positive

sequence voltage as a common polarizing reference is a common practice in distance relaying [17]. The settings for each element are fed into the blocks in vector form. The contents of each element are demonstrated in Figure 3.16.

Figure 3.16 – Directional Phase Impedance Relay Element Model

The ‘delta’ value magnitudes are calculated with a discrete Fourier algorithm. This is the same method used in the GE Multilin D30 [28, {8.1.2}]. Each discrete Fourier block will sample the delta values 64-times per power cycle and calculate the magnitude of the waveform at 60Hz. The magnitude of the apparent positive-sequence impedances then are calculated using the equations of Table 2.5 for reference only. The actual operating characteristics are defined by the corresponding zone calculations in the lower half of the model. It can be seen that the relay will implement the characteristic equations presented in Section 2.8.3.1. If the angular criteria of any characteristic calculation is met, an ‘on-delay’ timer will activate and trip the breaker after the appropriate delay. Notice that each zone can be enabled or disabled based on the ‘FWD’ signal

which determines the direction of the current waveform by differencing its phase and the phase of the positive sequence voltage. This phase difference is compared with the line of directionality and a forward/reverse decision is made. The phase of the positive sequence voltage is fed into a memory circuit prior to being used in the directional determination. The contents of the memory circuit are demonstrated in Figure 3.17.

Figure 3.17 – Memory Circuit Contents

The phase of the polarizing source is continually sampled from a delayed (1-3 cycles) source as long as the operating voltage has not collapsed. This ensures that the phase of the polarizing source is not affected by distortions caused by faults. During a voltage collapse (fault), the phase of the polarizing source will be remembered from its last reliable value and remain static throughout the fault period. This is a typical feature of modern directional relays [20, 8-6]. The set-points for the supervisory under-voltage and the line of directionality will be detailed later in Section 4.5.

3.3.2 Phase Mho Characteristic

The directional impedance relay is a practically useful relay, however, it does have one drawback. The zone boundaries extend equally in the direction of the fault phasor and the direction of the load phasor. Ideally, the relay zones would extend more in the direction of the fault phasor and less in the direction of the load phasor. This would allow the ultimate loadability of the relay to be increased without sacrificing protection during faults. The mho characteristic essentially allows the activation of the relay to be controlled by admittance parameters. To implement the basic mho characteristic, a circle is drawn passing through the origin and the desired zone reach limit along the line impedance phasor. The center of the circle will fall at $\frac{1}{2}$ of the zone reach along the line impedance phasor.

Figure 3.18 – Sample Mho Characteristic R-X Diagram

Figure 3.18 demonstrates a sample mho characteristic in 'FWD ZONE 1', 'FWD ZONE2' and 'REV ZONE1'. The figure also demonstrates that the loadability of this relay will be significantly increased compared to the direction impedance characteristic. Additionally, the mho characteristic is innately directional without the need of directional elements (i.e. no line of

directionality). For these reasons, the mho characteristic is the most commonly used distance characteristic.

Figure 3.19 – Mho Phase Impedance Relay Element Model

The overall structure of the mho characteristic is identical to the directional structure shown in Figure 3.15. The differences emerge in the individual elements. Figure 3.19 demonstrates the relay element model developed to implement the mho characteristic. The mho characteristic element is very similar to the directional impedance element with two significant differences. First, there is no directional decision signal as the mho characteristic is innately directional. Second, the operating characteristic implements the equations presented in Section 2.8.3.2. All other functionality is identical to the directional phase impedance relay.

3.4 Ground Distance Protection

With the analysis completed in Section 2.8, it is now possible to construct a MATLAB Simulink model for an ANSI 21G ground-distance relay. The following subsections will introduce the relay models for several different implementations of ground-distance protection.

3.4.1 Directional Ground Impedance Characteristic

The directional ground impedance characteristic for the ground distance relay is identical to the directional impedance characteristic of the phase distance relay (See Figure 3.14).

Figure 3.20 – Directional Ground Impedance Relay Model

Figure 3.20 shows the relay model developed to implement the ground impedance relay algorithms. This model is very similar to the directional phase impedance relay with three modifications. First, the compensated zero-sequence current (mI_0) has been calculated and added to each phase current. Second, the phase voltages and compensated phase currents are the new operating quantities instead of the 'delta' values used in the phase relays. Lastly, the polarizing positive sequence voltage phase angle has been adjusted to be in-phase with the new operating voltages. Outside of the three modifications, the functionality and settings of the relay are identical to the directional phase impedance relay. The contents of each relay element are identical to those used in the directional phase impedance relay. The memory circuit in the relay elements are identical to the circuit shown in Figure 3.17 with the exception that the per-unit conversion has modified for phase voltage inputs (i.e. a factor of $\sqrt{3}$ has been included).

3.4.2 Ground Mho Characteristic

The directional ground impedance relay is practical and easy to implement. It is, however, increasingly being replaced with ground mho characteristic relays. The reasons for this are similar to the reasons driving the use of the phase mho characteristic. The R-X diagram of the mho ground characteristic is identical to the phase mho characteristic shown in Figure 3.18.

The overall structure of the ground mho relay is identical to the directional ground relay model shown in Figure 3.20. The elements for the ground mho relay are identical to the elements for the phase mho relay shown in Figure 3.19. Again, the memory circuit in the relay elements are identical to the circuit shown in Figure 3.17 with the exception that the per-unit conversion has modified for phase voltage inputs (i.e. a factor of $\sqrt{3}$ has been included).

Chapter 4 – Protection Design for a Transmission-Level Application

The purpose of this section will be to create a protection design for a sample transmission-level application. The sample transmission scheme and operating scenario will be presented. From the presented application, a fault study will be completed and current transformers will be specified. The protection relays will then be selected from the models developed in Chapter 3 and all the necessary relay settings will be developed.

4.1 A Sample Transmission Scheme

The transmission-level application to be examined is shown in Figure 4.1.

Figure 4.1 – The Sample Application: A 230kV Transmission System

The goal of this relaying application will be to design the protections for lines 1-6 and buses A and B. It will be assumed that the remote ends of lines 1, 2, 4 and 6 are to be protected by 'others'. This is consistent with the theme of this transmission-level study. Large generation

and load centers are protected via internal protection systems which are out-of-scope for the transmission system owner/operator. The duty of the transmission system owner/operator is to disconnect faulted generation/load centers from the grid to ensure grid stability.

As is frequently the case in transmission-level applications, the power flow could be in any direction from one set of sources to another. This leads to many scenarios in which the protection systems must perform consistently. One of the most important scenarios is the scenario of maximum power transfer. For this application, this will be assumed to fall under the scenario of power transfer from Sources 1 and 2 to Sources 3 and 4. From this point forth, power flow from Sources 1 and 2 to Sources 3 and 4 will be assumed.

The power flows from Sources 1 and 2 to Station #1 through 35Km lines. Station #1 has a dual element spot network (DESN) topology. The DESN topology includes a normally-closed tie breaker which allows disconnection of the two busses. On loss of one supply, all loads can remain in service by opening the appropriate line breaker. In the event of a bus fault, one half of the network will be disabled. From Station #1, the power flows to Station #2 through 75Km lines. Station #2 is a ring bus topology. The ring bus topology requires one less breaker than the DESN and has no 'bus' zones. All parts of the ring are treated as 'line' zones. On loss of one supply, all loads can remain in service by opening the two appropriate line breakers. From Station #2, power then flows to Sources 3 and 4 through 75Km lines.

All transmission lines will be modeled as a resistance and inductance with mutual coupling between phases. The following typical transmission line parameters will be assumed:

$$R_1 = 0.050 \Omega/\text{km}$$

$$X_1 = 0.488 \Omega/\text{km} @ 60\text{Hz} (L = 1.29\text{mH}/\text{km})$$

$$Z_{1,\text{line}/\text{km}} = (0.05 + j0.488) \Omega/\text{km}$$

$$Z_{2,\text{line}/\text{km}} = Z_{1,\text{line}/\text{km}} = (0.05 + j0.488) \Omega/\text{km}$$

$$Z_{0,\text{line}/\text{km}} = 3 * Z_{1,\text{line}/\text{km}} = (0.15 + j1.464) \Omega/\text{km}$$

All other bus, breaker and source impedances will be assumed to be negligible.

For the purposes of this project, it will be assumed that the system is operating at maximum power transfer between Sources 1/2 and Sources 3/4. This will be assumed to occur at the following conditions given in phase voltage and angle.

$$\begin{aligned} E_1 &= \frac{230\text{kV}}{\sqrt{3}} = 132.8\text{kV} & \angle_1 &= 0^\circ & E_3 &= 0.85 * 132.8\text{kV} & \angle_3 &= -30^\circ \\ E_2 &= \frac{230\text{kV}}{\sqrt{3}} = 132.8\text{kV} & \angle_2 &= 0^\circ & E_4 &= 0.85 * 132.8\text{kV} & \angle_4 &= -30^\circ \end{aligned}$$

Thus, the system can be simplified as two sources and a reactance:

$$X_{eq} = \frac{35\text{km} * (0.488\Omega/\text{km})}{2} + \frac{75\text{km} * (0.488\Omega/\text{km})}{2} + \frac{75\text{km} * (0.488\Omega/\text{km})}{2} = 45.14\Omega$$

The maximum combined active and reactive power transfer from Sources 1/2 is given by:

$$P_{1\&2} = \frac{3 * (132.8\text{kV}) * 0.85(132.8\text{kV})}{45.14} \sin 30^\circ = 498.1\text{MW}$$

$$Q_{1\&2} = \frac{3 * [(132.8\text{kV})^2 - (132.8\text{kV})0.85(132.8\text{kV}) \cos 30^\circ]}{45.14} = 309.3\text{MVA}$$

The combined complex power and power factor can be calculated as follows:

$$S_{1\&2} = \sqrt{(498.1\text{MW})^2 + (309.3\text{MVA})^2} = 586.3\text{MVA}$$

$$\text{PF}_{1\&2} = \frac{498.1\text{ MW}}{586.3\text{ MVA}} = 0.85$$

For distance relaying, it is necessary to identify the minimum load impedance. This is calculated as follows:

$$|I_{1\&2}| = \frac{586.3\text{ MVA}}{3 * 132.8\text{ kV}} = 1472\text{ A}$$

$$|Z_{\text{Load},3\&4}| = \frac{132.8\text{ kV}}{1472\text{ A}} = 90.2\ \Omega$$

Note: This impedance represents the observed impedance of both loads in parallel without the line impedance. It will be assumed that the load impedance could fall anywhere in the range of 1.0-0.80 power factor

Calculating the impedance of the lines to be protected:

Lines 1 and 2:

$$Z_{\text{Lines},1\&2} = 35\text{km} \cdot (0.05 + j0.488) \Omega/\text{km}$$

$$Z_{\text{Lines},1\&2} = (1.75 + j17.08) \Omega = 17.17 \angle 84.15^\circ \Omega$$

Lines 3, 4, 5, 6:

$$Z_{\text{Lines},3,4,5\&6} = 75\text{km} \cdot (0.05 + j0.488) \Omega/\text{km}$$

$$Z_{\text{Lines},3,4,5\&6} = (3.75 + j36.6) \Omega = 36.79 \angle 84.15^\circ \Omega$$

4.1.1 Modeling of the Application

This section will detail the important aspects of how the transmission components will be modeled in the Simulink environment.

Transmission Lines:

The transmission lines will be modeled using the built-in Mutual Inductance (Z1/Z0) block. This block allows for simple modeling of the transmission lines via the positive and zero-sequence impedances. The mutual coupling between phases is established via the three-winding transformer model of Figure 4.2.

Figure 4.2 – Simulink Mutual Inductance Model

If all phase self impedances are assumed to be balanced the self and mutual impedances become:

$$Z_S = R_1 + j\omega L_1 + Z_M = R_2 + j\omega L_2 + Z_M = R_3 + j\omega L_3 + Z_M$$

$$Z_M = R_m + j\omega L_m$$

The resulting phase impedances can be represented in the following matrix:

$$Z_{abc} = \begin{bmatrix} Z_S & Z_M & Z_M \\ Z_M & Z_S & Z_M \\ Z_M & Z_M & Z_S \end{bmatrix}$$

The phase impedances can be translated to the sequence impedances via the $Z_{012} = T_S^{-1} Z_{abc} T_S$ transformation [30, 2]:

$$Z_{012} = \begin{bmatrix} Z_S + 2Z_M & 0 & 0 \\ 0 & Z_S - Z_M & 0 \\ 0 & 0 & Z_S - Z_M \end{bmatrix}$$

Thus, the sequence impedances can be related to the self and mutual impedances as follows:

$$Z_0 = Z_S + 2Z_M$$

$$Z_1 = Z_2 = Z_S - Z_M$$

Sources:

The sources (1-4) will be modeled as wye-connected, ideal voltage sources. The neutrals of all sources will be solidly grounded. A small source impedance is required for simulation and will be set as $X=0.25\Omega$, $X/R = 40$.

Buses:

The buses (A and B) will be modeled as ideal (i.e. zero impedance).

Circuit Breakers:

The breakers will be modeled using the built-in Simulink circuit breaker model with a small modification. Upon receiving the trip signal, the breakers will delay operating for 1 cycle and then interrupt the current at the next current zero-crossing. This has been done to more closely match the performance of realistic circuit breakers at the 230kV level. The forward resistance of the breaker will be set at $1m\Omega$. For the purposes of simulation, a snubber circuit must be included to allow interruption of inductive circuits. The snubber circuit will be set as purely resistive with a value of $1M\Omega$.

Faults:

The faults will be modeled using the built-in Simulink fault block. The fault will be modeled as a near 'bolted-bus' short. That is, the fault impedance has been set to the approximate impedance of a 10m segment of transmission line.

$$Z_{\text{fault}} = 0.01 * (0.05 + 0.488j \Omega/\text{km}) = 4.9 \angle 84.15^\circ \text{ m}\Omega$$

4.2 Short Circuit Study

To begin the design of the protection system, it is necessary to know the available fault current at the location of the circuit breakers and current transformers. This is accomplished by the E/X and E/Z methods described by IEEE Standard C37.010-1999 [31, 39]. To complete a thorough short circuit study, it is necessary to identify all of the possible operating scenarios and to calculate the possible short circuit currents for each. For this report, the maximum power flow scenario presented earlier will be used. To complete the study, both the three-phase and single phase to ground fault will be considered.

At Station #1

Three-Phase Fault:

$$I_{a_SC} = \frac{V_a}{Z_1 + Z_x}, \text{ from Section 2.3.1}$$

By setting the fault resistance to zero ($Z_x=0$) and neglecting the small breaker and source impedances, the symmetrical short circuit current can be calculated by superposition:

$$I_{a_SC} = \frac{V_{1\&2}}{\frac{Z_{1,\text{line}1} * Z_{1,\text{line}2}}{Z_{1,\text{line}1} + Z_{1,\text{line}2}}} + \frac{V_{3\&4}}{\frac{Z_{1,\text{line}3} * Z_{1,\text{line}4}}{Z_{1,\text{line}3} + Z_{1,\text{line}4}} + \frac{Z_{1,\text{line}5} * Z_{1,\text{line}6}}{Z_{1,\text{line}5} + Z_{1,\text{line}6}}}$$
$$I_{a_SC} = \frac{132800V}{\frac{(17.17)(17.17)}{(17.17)+(17.17)}} + \frac{0.85*132800V}{\frac{(36.79)(36.79)}{(36.79)+(36.79)} + \frac{(36.79)(36.79)}{(36.79)+(36.79)}} = 15469 + 3068 = 18537 \text{ A}$$

Phase-to-Ground Fault:

$$I_{a_SC} = \frac{3V_a}{Z_0 + Z_1 + Z_2 + 3Z_x}, \text{ from Section 2.3.2}$$

By setting the fault resistance to zero ($Z_x=0$) and neglecting the small breaker and source impedances, the symmetrical short circuit current can be calculated by superposition:

$$I_{a_SC} = \frac{3V_{1\&2}}{(3+1+1) \frac{Z_{1, \text{line}1} \cdot Z_{1, \text{line}2}}{Z_{1, \text{line}1} + Z_{1, \text{line}2}}} + \frac{3V_{3\&4}}{(3+1+1) \left[\frac{Z_{1, \text{line}3} \cdot Z_{1, \text{line}4}}{Z_{1, \text{line}3} + Z_{1, \text{line}4}} + \frac{Z_{1, \text{line}5} \cdot Z_{1, \text{line}6}}{Z_{1, \text{line}5} + Z_{1, \text{line}6}} \right]}$$

-recalling that $Z_0 = 3Z_1$, and $Z_2 = Z_1$

$$I_{a_SC} = \frac{3 \cdot 132800V}{5 \cdot \frac{(17.17)(17.17)}{(17.17)+(17.17)}} + \frac{3 \cdot 0.85 \cdot 132800V}{5 \cdot \left[\frac{(36.79)(36.79)}{(36.79)+(36.79)} + \frac{(36.79)(36.79)}{(36.79)+(36.79)} \right]} = 9281 + 1841 = 11122 \text{ A}$$

At Station #2

Three-Phase Fault:

$$I_{a_SC} = \frac{V_a}{Z_1 + Z_x}, \text{ from Section 2.3.1}$$

By setting the fault resistance to zero ($Z_x=0$) and neglecting the small breaker and source impedances, the symmetrical short circuit current can be calculated by superposition:

$$I_{a_SC} = \frac{V_{1\&2}}{\frac{Z_{1, \text{line}1} \cdot Z_{1, \text{line}2}}{Z_{1, \text{line}1} + Z_{1, \text{line}2}} + \frac{Z_{1, \text{line}3} \cdot Z_{1, \text{line}4}}{Z_{1, \text{line}3} + Z_{1, \text{line}4}}} + \frac{V_{3\&4}}{\frac{Z_{1, \text{line}5} \cdot Z_{1, \text{line}6}}{Z_{1, \text{line}5} + Z_{1, \text{line}6}}}$$

$$I_{a_SC} = \frac{132800V}{\frac{(17.17)(17.17)}{(17.17)+(17.17)} + \frac{(36.79)(36.79)}{(36.79)+(36.79)}} + \frac{0.85 \cdot 132800V}{\frac{(36.79)(36.79)}{(36.79)+(36.79)}} = 4922 + 6136 = 11058 \text{ A}$$

Phase-to-Ground Fault:

$$I_{a_SC} = \frac{3V_a}{Z_0 + Z_1 + Z_2 + 3Z_x}, \text{ from Section 2.3.2}$$

By setting the fault resistance to zero ($Z_x=0$) and neglecting the small breaker and source impedances, the symmetrical short circuit current can be calculated by superposition:

$$I_{a_SC} = \frac{3V_{1\&2}}{(3+1+1) \left[\frac{Z_{1, \text{line}1} \cdot Z_{1, \text{line}2}}{Z_{1, \text{line}1} + Z_{1, \text{line}2}} + \frac{Z_{1, \text{line}3} \cdot Z_{1, \text{line}4}}{Z_{1, \text{line}3} + Z_{1, \text{line}4}} \right]} + \frac{3V_{3\&4}}{(3+1+1) \frac{Z_{1, \text{line}5} \cdot Z_{1, \text{line}6}}{Z_{1, \text{line}5} + Z_{1, \text{line}6}}}$$

-recalling that $Z_0 = 3Z_1$, and $Z_2 = Z_1$

$$I_{a_SC} = \frac{3 \cdot 132800V}{5 \cdot \left[\frac{(17.17)(17.17)}{(17.17)+(17.17)} + \frac{(36.79)(36.79)}{(36.79)+(36.79)} \right]} + \frac{3 \cdot 0.85 \cdot 132800V}{5 \cdot \frac{(36.79)(36.79)}{(36.79)+(36.79)}} = 2953 + 3685 = 6638 \text{ A}$$

The values previously calculated represent the total available fault current at Stations #1 and #2. It becomes obvious that the three-phase fault provides the worst-case fault current in this application. The values calculated include currents which are coming from different directions into a fault. These values are important factors for many design issues such as equipment ratings and arc-flash calculations. For the design of protection systems, it more appropriate to calculate the total available fault current that can pass through a current transformer or circuit breaker. To

calculate these values it is most common to determine the worst-case system configuration and repeat the calculations for the 'through' fault current.

As an example, consider the breaker and current transformer M4. It can be seen that the worst-case through fault current will occur when breakers T2 and M6 are open and a three-phase fault occurs at the near terminals of Line 4. In this case the through fault current can be calculated as:

$$I_{a_SC} = \frac{V_a}{Z_1 + Z_x}, \text{ from Section 2.3.1}$$

By setting the fault resistance to zero ($Z_x=0$) and by neglecting the small breaker and source impedances, the symmetrical short circuit current can be calculated by superposition:

$$I_{a_SC} = \frac{V_{1\&2}}{\frac{Z_{1, \text{line}1} \cdot Z_{1, \text{line}2}}{Z_{1, \text{line}1} + Z_{1, \text{line}2}}} + \frac{V_{3\&4}}{\frac{Z_{1, \text{line}3} \cdot Z_{1, \text{line}5} \cdot Z_{1, \text{line}6}}{Z_{1, \text{line}3} + Z_{1, \text{line}5} + Z_{1, \text{line}6}}}$$

$$I_{a_SC} = \frac{132800V}{\frac{(17.17)(17.17)}{(17.17)+(17.17)}} + \frac{0.85 \cdot 132800V}{36.79 + \frac{(36.79)(36.79)}{(36.79)+(36.79)}} = 15469 + 2045 = 17514 \text{ A}$$

Obviously the through fault current will always be less than or equal to the total available fault current. This type of analysis has been repeated for all breaker/C.T. locations. The results are summarized in Table 4.1.

Table 4.1 – Through Fault Current at All Breaker/C.T. Locations

Breaker/C.T.	Maximum Through Fault Current (A) (Symmetrical)	Conditions
M1	10802	N/A
M2	10802	N/A
M3	17514	T2 & M5 Open
M4	17514	T2 & M6 Open
T1	9780	T2 & M5 (or M6) Open
M5	9063	M3 & T2 Open
M6	9063	M4 & T2 Open
T2	9063	M4 & M6 (or M3 & M5) Open
T3	7990	M5 (or M6) Open

4.3 Current Transformer Selection

Current transformers must be designed to accommodate the expected fault current for short durations and the expected load currents for continuous duration. With the through fault current for each C.T. location specified, it is now required to identify the maximum load current that each C.T. could experience. To accomplish this, the maximum load transfer scenario will be used and the system configuration will be examined for each current transformer to determine the maximum load current. Note that it will be assumed that the sources will be modified to achieve equivalent maximum load transfer regardless of line outages.

From Section 4.1, the total phase current during maximum load transfer will be 1465A. Due to the symmetrical nature of the network, this current will be split between the two sources on the sending end and the two sources on the receiving end. By examining the system configuration to determine the maximum load current through each C.T., the following table can be developed.

Table 4.2 – Maximum Load Current at All Breaker/C.T. Locations

Breaker/C.T.	Maximum Load Current (A)	Conditions
M1	732.5	N/A
M2	732.5	N/A
M3	1465	M4 Open
M4	1465	M3 Open
T1	732.5	M3 (or M4) Open
M5	1465	M6 Open
M6	1465	M5 Open
T2	1465	M4 & M6 (or M3 & M5) Open
T3	732.5	M5 (or M6) Open

With the maximum load current and through fault current known, the C.T. ratios can now be specified. To avoid (delay) C.T. saturation due to the asymmetrical fault current, this report will follow the sizing recommendations of IEEE standard C37.110 [8, 30]. This standard specifies the recommended practice of sizing the C.T.s for twice the expected symmetrical fault current. This will not eliminate the possibility of C.T. saturation, but this will ensure a reasonable, ‘time-to-saturate’ such that many types of protection relays can account for the problem. This sizing is

viewed as a minimum standard for C.T. sizing. This report will implement this minimum standard such that the effects of C.T. saturation on the modeled relays can be observed.

Table 4.3 – Current Transformer Selections

A	B	C	D	E	F
Breaker/C.T.	I, Load (A)	I, Fault (A)	$2 \cdot (I, \text{Fault}) / 20$	$\max(B, D)$	Selected C.T. Ratio
M1	732.5	10802	1080.2	1080.2	1200:5
M2	732.5	10802	1080.2	1080.2	1200:5
M3	1465	17514	1751.4	1751.4	2000:5
M4	1465	17514	1751.4	1751.4	2000:5
T1	732.5	9780	978	978	1200:5
M5	1465	9063	906.3	1465	2000:5
M6	1465	9063	906.3	1465	2000:5
T2	1465	9063	906.3	1465	2000:5
T3	732.5	7990	799	799	800:5

The selected C.T. ratios of Table 4.3 were selected from the standard offerings available from ABB [32, 2]. The excitation curves for the standard offerings are shown in Figure 4.3.

Figure 4.3 – Current Transformer Excitation Curves for Design Example

[32, 5]

With the C.T. ratios defined, it is now necessary to determine the rated secondary voltage and burdens. All of the C.T.s in Figure 4.3 are class C. By examining the secondary exciting voltage at 10A of exciting current, it can be seen that the selected C.T.s are likely to have the following ratings:

2000:5 C800

1200:5 C400

800:5 C200

This application may not require the ratings provided, however, it will be assumed that there is little cost/benefit to having lower-rated C.T.s custom made. Instead, the burden will be adjusted (where required) to ensure that the ratings are sufficient. For each C.T., the relay burden will be assumed to be 1Ω and the lead length will be 150m (one-way). The following wire resistances will be assumed:

#14cu AWG resistivity= $8.5\text{m}\Omega/\text{m}$

Total lead resistance = 2.55Ω

#12cu AWG resistivity= $5.4\text{m}\Omega/\text{m}$

Total lead resistance = 1.62Ω

#10cu AWG resistivity= $3.4\text{m}\Omega/\text{m}$

Total lead resistance = 1.02Ω

#8cu AWG resistivity= $2.2\text{m}\Omega/\text{m}$

Total lead resistance = 0.66Ω

It has been assumed that the minimum acceptable wire gauge is #14AWG. Obviously, the C800 and C400 burdens will be within specification with the #14AWG leads. The C200 burden will require the #8AWG leads to remain within specification.

Table 4.4 – Final C.T Selections and Connected Burdens

Breaker/C.T.	C.T. Designation	Total Connected Burden (Ω)
M1	1200:5 C400	3.55
M2	1200:5 C400	3.55
M3	2000:5 C800	3.55
M4	2000:5 C800	3.55
T1	1200:5 C400	3.55
M5	2000:5 C800	3.55
M6	2000:5 C800	3.55
T2	2000:5 C800	3.55
T3	800:5 C200	1.66

In realistic applications, it would be unusual to specify the absolute minimum wire gauge to be used. As identified in Section 2.5.2.3, the saturation performance of the current transformer can be greatly improved through minimizing the connected load. Reducing the wire resistance (via increased gauge) is generally the most cost-effective way to improve the saturation performance. Nonetheless, for this project, the minimum gauge will be used to observe the relay performance with C.T.s operating at minimum specification levels.

To properly model each of these current transformers, it is necessary to construct the instantaneous saturation parameters. These parameters have been derived from the excitation curves of Figure 4.3 using the method introduced in Section 3.1.1.1. The results have been included in Appendix A. All of the remaining C.T. parameters required for simulation have been identified in Table 4.5. The secondary winding resistances have been calculated to be the maximum allowable while still retaining the required secondary voltage rating.

Table 4.5 – C.T. Parameters for Simulation (Excluding Saturation Parameters)

	P (VA)	f (Hz)	V2rms (V)	R2 (Ω)	L2 (Ω)	V1rms (V)	R1 (pu)	L1 (pu)	Rm (pu)
800:5 C200	50	60	10	2.333	0	10/160	0.35	0	50
1200:5 C400	100	60	20	1.389	0	20/240	0.35	0	50
2000:5 C800	200	60	40	1.444	0	40/400	0.35	0	50

4.4 Differential Relay Settings

This section will detail the settings for the differential relays protecting busses ‘A’ and ‘B’ at Station #1 (See Figure 4.1). There is no definitive method available which allows a protection designer to identify the optimal relay settings for any given application. Instead, protection designers rely on experience, knowledge of the application, knowledge of the limitations of the protection strategy and proven ‘rules of thumb’. The settings developed in this section will identify the important design criteria, the generally accepted (standard) practice, and the rationale behind the selected settings.

4.4.1 Station #1 Bus 'A' Protection (87B)

Bus 'A' will be protected by a restrained differential relay. The restrained differential relay is not generally recommended for transmission-level applications due to the high X/R ratio (asymmetrical fault currents). The restrained differential relay cannot correct for C.T. saturation during faults which is likely to occur in these applications. Nonetheless, this relay will be used to help examine its performance and shortcomings. The three main settings which must be determined in the setting of this type of relay are the pick-up current, percentage restraint and time delay.

Pick-up Current Setting:

The pick-up current setting is intended to define the minimum differential current required to operate (trip) the relay. The purpose of this setting is to eliminate nuisance trips due to errors in the current measurement devices at very low current levels. The bound of the setting range on the 'low-end' is the sum of all measurement errors at low current levels. The bound of the setting range on the 'high-end' is the maximum allowable continuous fault current which will not cause damage to the equipment or cause out-of-zone relays to operate. Blackburn indicates that typical pick-up current settings range from 3-60% of largest C.T.'s primary rated current [4, {6.2}] while Horowitz recommends a pick-up setting of approximately 5% [5, 195]. Modern microprocessor based relays like the GE Multilin B30 and SEL 487B allow for pick-up current settings in the range of 5-200% and 5-100% of C.T. rated current respectively [27, {2.2.1}] [33, U.1.13]. The errors which must be accounted for are errors caused by the C.T., the relay transducer and the relay processing errors. Although more difficult to quantify, errors caused by electromagnetic interference and noise must also be considered. The highest ratio C.T. in the differential scheme is generally the C.T. which will contribute the highest error at very low current levels (all other factors being equal). From the excitation curves of Figure 4.3, it is possible to estimate the expected C.T. error at the minimum excitation levels shown on the curves.

$$I_{S,min,2000:5} = \frac{4}{1.444 + 3.55} = 0.801A$$

$$I_{P,min,2000:5} = \frac{2000}{5} * (0.001A + 0.801A) = 320.8A \text{ (16\% of primary rated)}$$

$$e_{\min,2000:5} = \frac{\frac{2000}{5} * 0.801 - 320.8}{320.8} * 100\% = -0.125\%$$

$$I_{S,\min,1200:5} = \frac{1.35}{1.389 + 3.55} = 0.273A$$

$$I_{P,\min,1200:5} = \frac{1200}{5} * (0.001A + 0.273A) = 65.76A \text{ (5.5\% of primary rated)}$$

$$e_{\min,1200:5} = \frac{\frac{1200}{5} * 0.273 - 65.76}{65.76} * 100\% = -0.365\%$$

Obviously, the expected errors in the C.T.s at the minimum excitation levels indicated on the curves are very small. In realistic applications, errors of the relay must also be considered. In microprocessor-based relays, these errors are typically on the order of 1-3%. As an example, the GE Multilin B30 offers a minimum conversion range of 2% of the C.T. rating with an accuracy of $\pm 0.25\%$ of reading [27, 2-10]. In this simulation, the relay current transducer will be modeled as ideal. In addition to all other errors, there must be sufficient margin to account for noise and interference in the measurement signals. For this application, it is recommended to implement a pick-up current of 5% of the largest C.T. primary current rating. This roughly corresponds to the minimum of the recommended range and the minimum available set-point for modern differential relays. Hence:

$$I_{PU} = 0.05 * (2000A) = 100A$$

For the high-end considerations, a set-point of 100A will not be hazardous to equipment designed for load currents of $\sim 1500A$ and fault currents of $\sim 19kA$. A high-impedance fault of less than 100A (e.g. a branch, animal, ext.) is not likely to remain indefinitely. In some cases they can extinguish naturally but more commonly they will increase in severity (beyond 100A) and be cleared by the protection systems as required. To ensure that no out-of-zone protection systems will operate for a 100A fault, it is necessary to examine the surrounding protection relays. This bus zone is bounded by another differential zone (Bus 'B') and two distance zones (Lines 1 and 3). The differential zone will be unaffected by low magnitude out-of-zone faults. To ensure the distance relays will not operate, it is necessary to examine the minimum observed impedance of the 100A fault. The observed impedance to this fault will be minimized when the fault current comes from the single source with the largest impedance (i.e. maximum voltage

collapse). This will occur when breakers M1, T1, T3 and T4 are open and the fault is fed solely from Source 3. As the bus impedance has been assumed to be essentially zero, the distance relays will measure only the fault impedance in this case. The fault impedance can be calculated using the short circuit equations of Sections 2.3.1 and 2.3.2.

$$I_{a_SC} = \frac{V_a}{Z_1 + Z_x}, \text{ Three-Phase Fault}$$

$$Z_x = \frac{V_a}{I_{a_SC}} - Z_1 = \frac{132800V}{100} - 2 * 36.79 = 1254\Omega$$

$$I_{a_SC} = \frac{3V_a}{Z_0 + Z_1 + Z_2 + 3Z_x}, \text{ Single-Phase Fault}$$

$$Z_x = \frac{V_a}{I_{a_SC}} - \frac{Z_0 + Z_1 + Z_2}{3} = \frac{132800V}{100} - \frac{2*(3+1+1)*36.79}{3} = 1205\Omega$$

Obviously, the distance relays observing these impedances will not operate as these impedances are far greater than the minimum load impedance ($\sim 90\Omega$).

Percentage Restraint Setting:

The percentage restraint setting is intended to define the minimum differential current required to operate the relay as a linear function of restraining current. The rational and typical setting ranges regarding this parameter have been discussed in Sections 2.7.2 and 3.2.2. In this application, the only source of error will be the 10% error expected based on the standard C.T. accuracy classifications. Ratio-mismatch errors have been eliminated by scaling (only possible in microprocessor based relays) and the transducer errors will be zero in this application. Hence, the percentage restraint will be set to the expected error plus a 10% safety margin:

$$\%_{\text{RESTRAINT}} = 20\%$$

Figure 4.4 – ANSI 87 Restraint Characteristic for Bus A and B Relays

Time Delay Setting:

The time delay setting will be the most critical setting to ensure proper co-ordination with the surrounding protection devices. The C.T.s have not been sized to ensure that saturation cannot occur and the restrained differential relay cannot account for hard saturation due to asymmetrical fault currents. Thus, the time delay must be set with the knowledge that nearby out-of-zone faults will cause hard saturation of the C.T. and may cause the relay to mis-operate. The basic idea is to set the time delay of the relay long enough to allow the primary protection of the adjacent equipment to clear nearby faults in their zones. This will allow a reasonable assurance that, by the time the delay has elapsed, the fault is within the zone regardless of saturation of one or more of the C.T.s. Blackburn indicates that the operating times of these relays are usually in the range of 50-100msec [4, {10.11.1}]. If the adjacent primary protections cannot clear a fault in their zones in this time-frame, then a more sophisticated relay should be used as the stress on the bus is likely to be too high. For this application, it will be assumed that the surrounding distance and differential relays will all operate in 1 cycle or less. Fast circuit breakers at the 230kV level can clear a fault in 1-3 cycles (i.e. 2nd-6th zero crossing). For this application, fast circuit breakers will be assumed. Hence, the time delay will be set to the sum of these times plus an additional safety margin.

$$T_{\text{Delay}} = T_{\text{Relay}} + T_{\text{Breaker}} + T_{\text{Margin}}$$

The margin will be set to one cycle:

$$T_{\text{Delay}} = 1\text{cycle} + 3\text{cycles} + 1\text{cycle} = 5\text{ cycles} = 83.3\text{msec}$$

4.4.2 Station #1 Bus 'B' Protection (87B)

Bus 'B' will be protected by a restrained directional differential relay. The restrained directional differential relay is much more suitable for a transmission-level application. This relay is unaffected by C.T. saturation and therefore does not require the long time delay introduced at Bus 'A'. Again, the three main settings which must be determined in the setting of this type of relay are the pick-up current, percentage restraint and time delay. Additionally, the supervisory magnitude checks of the phase current must be set to ensure reliable directionality.

Pick-up Current Setting:

The rationale for the setting of the pick-up current is identical to the setting of Bus 'A' in Section 4.4.1. Hence:

$$I_{PU} = 0.05 * (2000A) = 100A$$

Percentage Restraint Setting:

The rationale for the percentage restraint is identical to the setting of Bus 'A' in Section 4.4.1. Hence:

$$\%_{RESTR} = 20\% \text{ (See Figure 4.4)}$$

Time Delay Setting:

The rationale for the time delay setting for the restrained directional differential relay is different than for the restrained differential relay. As the directional differential relay is not affected by C.T. saturation, the time delay is not required to coordinate with external protections. For electromechanical implementations of this relay, Horowitz recommends a delay of approximately 4 cycles [5, 226]. This delay allows for numerous independent directional relays and their mechanical contacts to coordinate and de-bounce. The relay model being used is modeled after a microprocessor implementation which has no independent directional relays or mechanical contacts. The model being implemented uses a discrete Fourier algorithm to compute the magnitude and phase of the current waveform at the fundamental frequency. As was mentioned in Section 3.2.1, the presence of the decaying D.C. component of the fault current can cause transient over-shoot and ringing in the measured magnitude and phase of the current waveforms. Most commercially available relays include sophisticated filtering methods to suppress these transients which have not been included in this relay model. Thus, during this transient period immediately following a fault, the magnitude and phase could move into/out-of the trip range unexpectedly. This can cause the relay to mis-operate. The lack of sophisticated filtering leads to a recommendation to implement a very small time delay of $\frac{1}{4}$ cycle.

$$T_{Delay} = 0.25 \text{ cycle} = 4.167\text{msec}$$

Supervisory Under-Current Check:

The supervisory under-current check ensures that only bus terminals which are carrying current (i.e. in-service) are included in the directional permissive logic. This ensures that unpredictable operation due to terminals being out-of-service is avoided. The setting for this check follows the same logic as the pick-up current setting detailed in Section 4.4.1. Correspondingly, the magnitude check will be set to 100A.

$$I_{\text{Sup,U/C,RMS}}=100\text{A}$$

4.5 Distance Relay Settings

This section will detail the settings for the distance relays protecting lines 1-6 (See Figure 4.1). Again, there is no definitive method available which allows a protection designer to identify the optimal relay settings for any given application. As was done in setting the differential relays, the settings developed in this section will identify the important design criteria, the generally accepted (standard) practice, and the rationale behind the selected settings.

4.5.1 Station #1 Lines 1 and 2 Protection (21PG – Directional Characteristic)

Lines 1 and 2 will be protected by directional characteristic phase and ground distance relays. Due to the symmetry in the application, the settings for the Line 1 and Line 2 relays will be identical. For this application, two forward zones and one reverse zone of protection will be assumed. The settings which must be determined are the reach and time delay of each of the three zones as well as the lines of directionality for relays. Additionally, the supervisory under-voltage for the memory circuits must be determined.

Forward Zone 1 Settings:

Recall that the forward direction is defined as ‘into’ the line being protected. Hence, the forward zones will extend from Station #1 towards Sources 1 and 2. Distance protection zones are open at the far end. This means that there is some uncertainty in the exact length of the zone. To ensure proper coordination with the remote-end protections, stepped distance protection is used. The first zone is set to operate very fast while under-reaching the total zone length. Subsequent

zones are progressively time delayed and set to over-reach the total zone by varying lengths. The uncertainty in the zone length is typically about 5% [5, 100]. The uncertainty in the zone length comes about due to the errors in measuring/estimating the total transmission line impedances, the variation in the transmission line impedance due to temperature variation and the mutual coupling with adjacent transmission lines. Additionally, realistic relays will have measurement errors which will contribute to the uncertainty in zone length. The GE Multilin D30 claims a reach accuracy of $\pm 5\%$ [28, {2.2.1}]. Horowitz recommends a zone 1 reach of 85-90% while Blackburn recommends a zone 1 reach of 90% of the line length [5, 100] [4, {12.12}]. This sample application is relatively ideal in that the transmission line impedance is definitively known, there are no temperature variations and there has been no modeling of coupling between the separate transmission lines. For these reasons, the forward zone 1 reach will be set to the most aggressive setting in the recommended range:

$$\text{Reach}_{\text{Fwd,Zone1}} = 0.90 * |Z_{\text{Lines,1\&2}}|$$

$$\text{Recalling that } |Z_{\text{Lines,1\&2}}| = 17.17\Omega$$

$$\text{Reach}_{\text{Fwd,Zone1}} = 15.45\Omega$$

An additional error which can affect the reach of zone 1 in the case of the ground distance relay is the compensation factor which accounts for the mutual coupling between phases of the transmission line. In realistic systems, this compensation factor is usually an estimate or a calculated value from a simplified representation of the system. The resulting value can typically include a significant error. Additionally, the mutual coupling will have small variations with ambient conditions. For these reasons, Blackburn recommends that the zone 1 reach for ground faults be reduced by 5% from the zone 1 reach for phase faults [4, {12.17}]. In this application, the mutual coupling is known and non-variable. For this reason, the reach for the phase and ground relays will be set equal.

The zone 1 time delay is generally set to very small values if not zero (i.e. instantaneous) as this zone is not required to co-ordinate with the protections of any other zones. However, the model being implemented uses a discrete Fourier algorithm to compute the magnitude and phase of the current waveform at the fundamental frequency. As was mentioned in Section 3.3.1, the presence of the decaying D.C. component of the fault current can cause transient overshoot and

ringing in the measured magnitude and phase of the current waveforms. Most commercially available relays include sophisticated filtering methods to suppress these transients which have not been included in this relay model. Thus, during this transient period immediately following a fault, the magnitude and phase could move into/out-of the trip range unexpectedly. This can cause the relay to mis-operate. The lack of sophisticated filtering leads to a recommendation to implement a very small time delay of $\frac{1}{4}$ cycle.

$$T_{\text{Delay,Fwd,Zone1}} = 0.25 \text{ cycle} = 4.167 \text{ msec}$$

Forward Zone 2 Settings:

The forward zone 2 setting is intended to over-reach the line with a longer time delay to ensure the entire line is protected. Elmore recommends that the zone length be set to 100% of the line plus 50% of the shortest adjacent line from the remote bus [3, {4.4.1}]. Horowitz recommends that the zone length be set at 120-150% of the line length [5, 101]. The limitation on the zone 2 length is that it must not exceed the zone 1 length of all lines extending from the remote bus. In this application, the remote ends of Lines 1 and 2 are protected by others. As such, the zone 2 length will be set to the minimum of the recommended range.

$$\text{Reach}_{\text{Fwd,Zone2}} = 1.20 * |Z_{\text{Lines,1\&2}}|$$

$$\text{Recalling that } |Z_{\text{Lines,1\&2}}| = 17.17\Omega$$

$$\text{Reach}_{\text{Fwd,Zone2}} = 20.60\Omega$$

The time delay of the zone 2 must be set to ensure that it does not operate before the primary protections of the remote lines. Horowitz recommends a time delay of approximately 18 cycles to allow coordination. This time delay must exceed the sum of the remote relay operating time, the remote breaker clearing time and an additional safety margin. As remote-end faults result in relatively small fault currents at the local station, this time delay need not be set aggressively. In a realistic application, the protections at the remote ends should be examined to ensure proper coordination. In this application, the recommendations of Horowitz will be assumed sufficient:

$$T_{\text{Delay,Fwd,Zone2}} = \frac{18}{60} = 0.3 \text{ sec}$$

Reverse Zone 1 Settings:

The reverse zone 1 setting is intended to provide backup protection for the bus and adjacent lines. In this case, the reverse zone protection will provide backup protection for faults on Buses 'A' and 'B', Lines 3 and 4 as well as the opposite adjacent line (Line 1 or 2). There are no static recommended ranges for setting of backup protection. However, the reach of the backup protection should be less than the reach of the primary protection and more than any over-reaching zone 2 protection from remote relays. The limiting case is invariably the shortest line of the bus. In this application, the limiting case will be the opposite adjacent line (Line 1 or 2). The settings for the reverse zone will be set on the basis that approximately 50% of Line 1 or 2 will be protected by in the zone 2 of a protection device at Station #2. It is recommended to set the reverse zone 1 reach approximately half way between the lines zone 1 (90%) coverage and the remote zone 2 (50%) coverage. The reverse zone reach will be set to 75% of the line length as this provides a large backup coverage while providing a 15% margin from the forward zone 1.

$$\text{Reach}_{\text{Rev,Zone1}} = 0.75 * |Z_{\text{Lines,1\&2}}|$$

$$\text{Recalling that } |Z_{\text{Lines,1\&2}}| = 17.17\Omega$$

$$\text{Reach}_{\text{Rev,Zone1}} = 12.88\Omega$$

The time delay of the reverse zone must be set to ensure that it does not operate before the primary protections it is backing-up and that it does operate before the remote zone 2 protection. If it is assumed that the remote zone 2 has a time delay of 0.3sec and that the primary protection is essentially instantaneous, the reverse zone time delay should be set in the middle of these two delays. Hence:

$$T_{\text{Delay}} = \frac{9}{60} = 0.15\text{sec}$$

Note that this time delay must not operate before the bus differential protection as well. The slow restrained differential protection at Bus 'A' will provide this limiting case. Thus the reverse zone time delay must operate only after the maximum clearing time plus a safety margin. It will again be assumed that the differential relay operating time is at most 1 cycle, the time delay is 5 cycles and the maximum breaker clearing time is 3 cycles. Hence:

$$T_{\text{Delay,Rev,Zone1}} = T_{\text{Relay}} + T_{\text{Delay}} + T_{\text{Breaker}} + T_{\text{Margin}}$$

The margin will be set to one cycle:

$$T_{\text{Delay,Rev,Zone1}} = 1\text{cycle} + 5\text{cycles} + 3\text{cycles} + 1\text{cycle} = 10\text{ cycles} = 0.166\text{sec}$$

This delay will still coordinate well with the 0.3sec delay of the remote zone 2.

Lines of Directionality:

For the phase and ground relays, the polarizing source will be selected as the appropriate positive sequence voltage phasor. The common positive sequence reference angle will be adjusted by the appropriate angle for each distance element. For example, the 'c'-'a' element will be polarized by $\angle V_{a_1} + 30^\circ + 120^\circ$. Where the 30° term compensates for the line-line phase difference and the 120° term compensates for the different system phases. In each case, the angle of the polarizing source will be in-phase with the each elements voltage input. Thus, the angle of the polarizing source is equivalent to the phase angle produced by the phase current passing through a purely resistive impedance. Hence, the polarizing source can be represented by a vector along the positive resistance (R) axis of the R-X diagram. The line of directionality will be situated perpendicular to the line impedance. If lagging is defined in the positive direction and leading is defined in the negative direction, the angles of forward directionality become $(-6^\circ, +174^\circ)$. See Figure 4.5.

Forward-Criteria = $(-6^\circ, +174^\circ)$

Figure 4.5 – ANSI 21 Directional Characteristic for Lines 1 and 2 Relays

Supervisory Phase Under-Voltage:

The supervisory under-voltage parameter triggers memory-polarization. This will ensure that the polarizing source of the relay is remembered from its last reliable value when a fault occurs (voltage collapse). As the relays have been designed using self-polarization, they are particularly susceptible to a loss of polarization due to voltage collapse. This setting will be determined by examining the acceptable normal and emergency voltage variations on the 230kV grid and applying an additional safety margin. In Ontario, the Independent Electrical System Operator identifies the continuous operating voltage levels of the 230kV grid to fall within the range of (220-250kV) [34, A4.1-1]. Additionally, the Ontario Energy Board's Transmission System Code specifies that all systems must function normally during emergencies with an additional voltage variation of $\pm 6\%$ of the nominal voltage [35, {7.1.1}]. Hence, the protection system should not trigger memory-polarization for line voltages equal to or exceeding 206.2kV. An

additional safety margin of 10% will be applied. Converting to per-unit form, the supervisory phase under-voltage is:

$$V_{\text{Sup,U/V}} = 0.80 \text{ pu}$$

4.5.2 Station #1 Lines 3 and 4 Protection (21PG – Mho Characteristic)

Lines 3 and 4 extending from Station #1 will be protected by mho characteristic phase and ground distance relays. Due to the symmetry in the application, the settings for the Line 3 and Line 4 relays will be identical. The settings which must be determined are the reach and time delay of each of the three zones. Additionally, the supervisory under-voltage for the memory circuits must be determined.

Forward Zone 1 Settings:

Using the same rationale in Section 4.5.1, the reach will be set to 90% of the line impedance.

$$\text{Hence: } \text{Reach}_{\text{Fwd,Zone1}} = 0.90 * Z_{\text{Lines,3\&4}}$$

$$\text{Recalling that } Z_{\text{Lines,3\&4}} = 36.79 \angle 84.15^\circ \Omega$$

$$\text{Reach}_{\text{Fwd,Zone1}} = 33.11 \angle 84.15^\circ \Omega$$

The time delay will be set using the same rationale in Section 4.5.1. Hence:

$$T_{\text{Delay,Fwd,Zone1}} = 0.25 \text{ cycle} = 4.167 \text{ msec}$$

Forward Zone 2 Settings:

Using the rationale in Section 4.5.1, the reach will be set to 100% of the line impedance plus 50% of the Line 5/6 Impedance. Hence: $\text{Reach}_{\text{Fwd,Zone2}} = Z_{\text{Lines,3\&4}} + 0.5 * Z_{\text{Lines,5\&6}}$

$$\text{Recalling that } Z_{\text{Lines,3\&4}} = Z_{\text{Lines,5\&6}} = 36.79 \angle 84.15^\circ \Omega$$

$$\text{Reach}_{\text{Fwd,Zone2}} = 55.19 \angle 84.15^\circ \Omega$$

The time delay will be set using the same rationale in Section 4.5.1. Hence:

$$T_{\text{Delay,Fwd,Zone2}} = 0.3 \text{ sec}$$

Reverse Zone 1 Settings:

Using the rationale in Section 4.5.1, the reach will be set to 75% of the Lines 1/2 impedance in the negative direction. Hence: $\text{Reach}_{\text{Rev,Zone1}} = -(0.75 * Z_{\text{Lines,1\&2}})$

Recalling that $Z_{\text{Lines,1\&2}} = 17.17 \angle 84.15^\circ \Omega$

$$\text{Reach}_{\text{Rev,Zone1}} = -12.88 \angle 84.15^\circ \Omega$$

The time delay will be set using the same rationale in Section 4.5.1. Hence:

$$T_{\text{Delay,Rev,Zone1}} = 0.166\text{sec}$$

Figure 4.6 – ANSI 21 Mho Characteristic for Line 3 and 4 Protection from Station #1

Supervisory Phase Under-Voltage:

Using the rationale in Section 4.5.1, the supervisory under-voltage will be set to 0.8pu.

$$V_{\text{Sup,U/V}} = 0.80 \text{ pu}$$

4.5.3 Station #2 Lines 3 and 4 Protection (21PG – Directional Characteristic)

Lines 3 and 4 extending from Station #2 will be protected by directional characteristic phase and ground distance relays. Due to the symmetry in the application, the settings for the Line 3 and Line 4 relays will be identical. The settings which must be determined are the reach and time delay of each of the three zones as well as the lines of directionality for relays. Additionally, the supervisory under-voltage for the memory circuits must be determined.

Forward Zone 1 Settings:

Using the same rationale in Section 4.5.1, the reach will be set to 90% of the line impedance.

$$\text{Reach}_{\text{Fwd,Zone1}} = 0.90 * |Z_{\text{Lines,3\&4}}|$$

$$\text{Recalling that } |Z_{\text{Lines,3\&4}}| = 36.79\Omega$$

$$\text{Reach}_{\text{Fwd,Zone1}} = 33.11\Omega$$

The time delay will be set using the same rationale in Section 4.5.1. Hence:

$$T_{\text{Delay,Fwd,Zone1}} = 0.25 \text{ cycle} = 4.167\text{msec}$$

Forward Zone 2 Settings:

Using the rationale identified in Section 4.5.1, the reach will be set to the line impedance (100%) plus 50% of the impedance of the shortest line extending from the remote bus.

$$\text{Reach}_{\text{Fwd,Zone2}} = 1 * |Z_{\text{Lines,3\&4}}| + 0.5 * |Z_{\text{Lines,1\&2}}|$$

$$\text{Recalling that } |Z_{\text{Lines,1\&2}}| = 17.17\Omega \text{ and } |Z_{\text{Lines,3\&4}}| = 36.79\Omega$$

$$\text{Reach}_{\text{Fwd,Zone2}} = 45.38\Omega$$

The time delay will be set using the same rationale in Section 4.5.1. Hence:

$$T_{\text{Delay,Fwd,Zone2}} = \frac{18}{60} = 0.3\text{sec}$$

Reverse Zone 1 Settings:

Using the rationale in Section 4.5.1, the reach will be set to 75% of the Lines 5/6 impedance.

$$\text{Hence: } \text{Reach}_{\text{Rev,Zone1}} = 0.75 * Z_{\text{Lines,5\&6}}$$

$$\text{Reach}_{\text{Rev,Zone1}} = 0.75 * |Z_{\text{Lines,5\&6}}|$$

$$\text{Recalling that } |Z_{\text{Lines,5\&6}}| = 36.79\Omega$$

$$\text{Reach}_{\text{Rev,Zone1}} = 27.59\Omega$$

The time delay will be set using the same rationale in Section 4.5.1 with the exception that there is no bus protection to coordinate with at Station #2. Hence:

$$T_{\text{Delay}} = \frac{9}{60} = 0.15\text{sec}$$

Lines of Directionality:

The lines of directionality will be identical to those developed in Section 4.5.1.

Forward-Criteria = $(-6^\circ, +174^\circ)$

Figure 4.7 – ANSI 21 Directional Characteristic for Lines 3 and 4 21P Relays

Supervisory Phase Under-Voltage:

Using the rationale in Section 4.5.1, the supervisory under-voltage will be set to 0.8pu.

$$V_{\text{Sup,U/V}} = 0.80 \text{ pu}$$

4.5.4 Station #2 Lines 5 and 6 Protection (21PG – Mho Characteristic)

Lines 5 and 6 will be protected by mho characteristic phase and ground distance relays. Due to the symmetry in the application, the settings for the Line 5 and Line 6 relays will be identical. The settings which must be determined are the reach and time delay of each of the three zones. Additionally, the supervisory under-voltage for the memory circuits must be determined.

Forward Zone 1 Settings:

Using the same rationale in Section 4.5.1, the reach will be set to 90% of the line impedance.

$$\text{Hence: } \text{Reach}_{\text{Fwd,Zone1}} = 0.90 * Z_{\text{Lines,5\&6}}$$

$$\text{Recalling that } Z_{\text{Lines,3\&4}} = 36.79 \angle 84.15^\circ \Omega$$

$$\text{Reach}_{\text{Fwd,Zone1}} = 33.11 \angle 84.15^\circ \Omega$$

The time delay will be set using the same rationale in Section 4.5.1. Hence:

$$T_{\text{Delay,Fwd,Zone1}} = 0.25 \text{ cycle} = 4.167 \text{ msec}$$

Forward Zone 2 Settings:

Using the rationale in Section 4.5.1, the reach will be set to 120% of the line impedance. Hence:

$$\text{Reach}_{\text{Fwd,Zone2}} = 1.20 * Z_{\text{Lines,5\&6}}$$

$$\text{Recalling that } Z_{\text{Lines,5\&6}} = 36.79 \angle 84.15^\circ \Omega$$

$$\text{Reach}_{\text{Fwd,Zone2}} = 44.15 \angle 84.15^\circ \Omega$$

The time delay will be set using the same rationale in Section 4.5.1. Hence:

$$T_{\text{Delay,Fwd,Zone2}} = 0.3 \text{ sec}$$

Reverse Zone 1 Settings:

Using the rationale in Section 4.5.1, the reach will be set to 75% of the Lines 3/4 impedance in the negative direction. Hence: $\text{Reach}_{\text{Rev,Zone1}} = -(0.75 * Z_{\text{Lines,3\&4}})$

$$\text{Recalling that } Z_{\text{Lines,1\&2}} = 36.79 \angle 84.15^\circ \Omega$$

$$\text{Reach}_{\text{Rev,Zone1}} = -27.59 \angle 84.15^\circ \Omega$$

The time delay will be set using the same rationale in Section 4.5.1 with the exception that there is no bus protection to coordinate with at Station #2. Hence:

$$T_{\text{Delay,Rev,Zone1}} = 0.15\text{sec}$$

Figure 4.8 – ANSI 21 Mho Characteristic for Line 5 and 6 Protection from Station #2

Supervisory Phase Under-Voltage:

Using the rationale in Section 4.5.1, the supervisory under-voltage will be set to 0.8pu.

$$V_{\text{Sup,U/V}} = 0.80 \text{ pu}$$

4.5.5 Distance Protection Summary

Coordination in distance protection is most commonly demonstrated via a distance versus time graph. Figures 4.9 and 4.10 have been drawn to scale to demonstrate the coordination for each

zone. Each protection zone has been labeled by an abbreviation following the format: ('Station Number'-'Primary Protected Equipment'-'Zone Identifier'). For example S1-L3-FZ2 represents the forward zone #2 of the relay at Station #1 whose primary function is protecting Line #3. S2-L3/4/5-RZ1 represents the reverse #1 zone of the three relays at Station #2 whose primary functions are protecting Lines 3, 4 and 5.

Figure 4.9 – Stepped-Distance Protection for Lines 1, 3 and 5 and Bus A

Figure 4.10 – Stepped-Distance Protection for Lines 2, 4 and 6 and Bus B

Top: From Stations #1 and 2 towards Source 4

Bottom: Top: From Stations #1 and 2 towards Source 2

Chapter 5 – Simulated Application Performance

The purpose of this section is to simulate and analyze the various aspects of the designed protection system. The transmission system of Figure 4.1 has been modeled in the Simulink environment along with the protection elements designed in Chapter 4. This model is used to test the expected performance of all protection elements against their simulated performance. The performance of the current transformers will be examined under the extreme symmetrical and asymmetrical current conditions. The calculated fault currents will be verified at all breaker/C.T. locations. Finally, a testing strategy will be developed to verify the accuracy of the modeled protection relays and to determine the soundness of the protection design.

5.1 The Simulink Model

Figure 5.1 demonstrates the overall Simulink model of the transmission system of Figure 4.1. The developed current transformer blocks are shown adjacent to each circuit breaker. The remainder of the protection system has been included in the blocks identified as ‘Station #1/2 Protection Logic’. The contents of these blocks have been included in Figures 5.2 and 5.3.

Figure 5.1 – Simulink Model of the Designed Transmission System

Figure 5.2 – Station #1 Protection Logic

Notice that outputs to the breakers are controlled by S-R flip-flops. They are initialized as 'set' (i.e. breaker closed) and upon receiving a trip signal, they will 'reset' (i.e. latch to breaker open). The protection logic for each breaker has been programmed using the appropriate gate logic. Notice that each protection relay at Station #2 will trip two breakers as is necessary due to the ring-bus configuration.

Figure 5.3 – Station #2 Protection Logic

5.2 Current Transformer Accuracy Verification

The purpose of this section is to examine the performance of the modeled current transformers in reproducing symmetrical current waveforms. Loads will be adjusted for each of the three modeled C.T.s to produce symmetrical primary currents at 20x the rated primary current. The protection systems will be disabled during this testing. The results will be compared with the results of ideal current measurements to verify their performance against expectations.

Figure 5.4 demonstrates the modeled 2000:5 C.T. performance at 40kA symmetrical primary current. An RMS error of $(40\text{kA} - 37.7\text{kA}) / 40\text{kA} = 5.8\%$ can be observed. This error is less than the allowable 10%. This is expected as the secondary leakage inductance and core loss have been modeled as relatively ideal. Additionally, small errors in the saturation characteristic will be present due to the piece-wise linear estimation and from reading of data-points from the manufacturer's saturation curve. Due to the non-linear saturation characteristics, the error is expected to quickly exceed 10% at current higher current levels. The figure effectively demonstrates the dramatic increase in magnetizing current as the core saturates. The difference between the ideal and saturable C.T. waveforms can be directly attributed to the magnetizing current (neglecting core loss).

Figure 5.4 – 2000:5 C.T. Performance at 40kA Symmetrical Primary Current

Time offset: 0

Figure 5.5 – 1200:5 C.T. Performance at 24kA Symmetrical Primary Current

Figure 5.5 demonstrates an RMS error of $(24\text{kA}-22.5\text{kA})/24\text{kA} = 6.3\%$. Again, this error is less than the allowable 10%.

Figure 5.6 – 800:5 C.T. Performance at 16kA Symmetrical Primary Current

Figure 5.6 demonstrates an RMS error of $(16\text{kA}-14.9\text{kA})/16\text{kA} = 6.9\%$. Again, this error is less than the allowable 10%.

5.3 Short Circuit Current Verification and C.T. Performance Evaluation

The purpose of this section is to verify the through fault currents calculated in Table 4.1. This is done by disabling the protection systems and simulating the faults for each of the operating scenarios identified in the Table. The resulting symmetrical fault currents are compared with the expected results and the unsymmetrical aspects are examined. Additionally, the current transformer performance on the unsymmetrical fault currents will be examined.

The figure below demonstrates the instantaneous and RMS current waveforms for each phase at M1 during a three-phase fault at the Line 1 terminals. The RMS waveforms include the total, symmetrical and DC components of the fault current. It can be seen that the symmetrical current approaches a value of 10400A. This yields an error of $(10802A - 10400A)/10400A = 3.9\%$. Thus, the calculations were slightly conservative. This is expected as the calculations neglected the small source, breaker and fault impedances. The effects of the DC component of the fault current can also be observed. The peak of the total asymmetrical currents is maximized in the 'a' phase and hits 21.4kA or 206% of the observed symmetrical current. This observation is in-line with the 'doubling effect' discussed in Section 2.1.1. The peak exceeds the expected 200% due to the decaying oscillations in the symmetrical component. The decaying oscillations (at fundamental frequency) in the symmetrical component are an expected phenomenon which is not present in the actual current waveforms. The overshoot was the largest in the 'a' phase and was equal to $11760A - 10400A = 1360A$ or 13.1%. This demonstrates the limitation of the Fourier algorithm used to calculate the magnitude of the symmetrical current. The decaying DC component of the fault current will cause decaying oscillations at the fundamental frequency in the output of the Fourier algorithm. It is worth noting that the high-pass filtering of the current waveform had to be removed for this test. This filtering is expected to improve this transient performance. The time constant of the decaying DC component can be calculated by comparing two points on the decaying DC curve: [8435V, 0.09s] and [831V, 0.15s]. Thus:

$$\tau = \frac{L}{R} = \frac{t_2 - t_1}{\ln\left(\frac{V_1}{V_2}\right)} = \frac{0.15 - 0.09}{\ln\left(\frac{8435}{831}\right)} = 25.9ms$$

This closely matches the design parameters of Section 4.1: $\frac{L}{R} = \frac{1.29mH/km}{0.05\Omega/km} = 25.8ms$

Figure 5.7 – Currents at M1 During a Three-Phase Fault at the Line 1 Terminals

Figure 5.8 – M1 Phase ‘a’ C.T. Performance During a Three-Phase Fault at the Line 1 Terminals

Time offset: 0

The figure above demonstrates the M1 phase 'a' C.T. performance during a three-phase fault at the Line 1 terminals. The peak error in the symmetrical RMS waveforms (actual steady state versus saturable) can be seen to be approximately $(4175\text{A} - 10400\text{A})/10400\text{A} = -59.9\%$. Obviously, the DC component of the fault waveform has a dramatic detrimental effect on the C.T. performance. It can be seen that the DC component causes an asymmetrical shift in the core flux which quickly drives the C.T. into saturation. When the DC component of the fault waveform has significantly decayed, the normal performance is essentially restored. Notice that the flux waveform retains its asymmetry once the DC fault current has decayed. This asymmetry will gradually decay due to the slightly higher saturation losses at the higher flux levels versus the lower flux levels.

The figure below demonstrates the instantaneous and RMS current waveforms at M1 during a single-phase-to-ground fault at the Line 1 terminals with Source 1 out of service. It can be seen that the symmetrical RMS fault current is approximately 6275A. As this fault current is much less than the 10400A three-phase fault current, the three-phase fault provides the worst-case fault current. This supports the same assertion developed in Section 4.2.

Figure 5.9 – Currents at M1 During a Phase-to-Ground Fault at the Line 1 Terminals

The through fault current at all breaker/C.T. locations was examined through simulation as was done in Figure 5.7 according to the conditions of Table 4.1. These results have been summarized in Table 5.1.

Table 5.1 – Through Fault Current at All Breaker/C.T. Locations

Breaker/C.T.	Maximum Through Fault Current (A) (Symmetrical)		Error (%)	Simulation Conditions
	Calculation	Simulation		
M1	10802	10400	3.87	N/A
M2	10802	10400	3.87	N/A
M3	17514	17140	2.18	T2 & M5 Open
M4	17514	17140	2.18	T2 & M6 Open
T1	9780	9490	3.06	T2 & M5 Open
M5	9063	8710	4.05	M3 & T2 Open
M6	9063	8710	4.05	M4 & T2 Open
T2	9063	8710	4.05	M4 & M6 Open

Table 5.1 demonstrates results consistent with the findings of Figure 5.7. All calculation results have proven to be slightly conservative as they disregarded several of the smaller system impedances (source, breaker and fault impedances). These results can be seen to validate the analysis undertaken in the fault study.

5.4 Relay Testing Strategy

There is an almost limitless number of fault scenarios which could be developed for the small sample application developed for this report. The number of possible fault locations, fault types, system conditions and system configurations leads to an unending number of testing scenarios. Realistically, this report must limit the testing results displayed to keep the report from becoming prohibitively long. Individual differential relays are tested in detail for both internal and all adjacent external faults. Each distance relay type is tested in detail at various points within their zones of protection to verify accuracy and functionality. Finally, the overall protection design is verified by testing faults at 0%, 50% and 100% of each line and at all busses. The overall expected and simulated results for the protection design are presented in tabular form.

To simplify the discussion in the following sections, Figure 5.10 provides numerical identification of all fault locations to be tested.

Figure 5.10 – Identification of Fault Placement Locations for Testing

5.4.1 Individual Differential Relay Testing Results

For this testing, all breakers are disabled to ensure that no other relays interfere with the relay being tested. The fault is initiated at a time of 4 cycles into the simulation, such that the 'a' phase voltage is zero at the initiation of the fault. This will ensure that the 'a' phase fault current has the maximum possible DC offset.

5.4.1.1 Restrained Differential Relay at Bus A

The restrained differential relay is tested under the worst-case scenarios. As C.T. saturation is the main cause of false trips in differential relays, the worst-case scenarios will be high-current faults just outside of the protected zone. The restrained differential relay at Bus A will be tested under three-phase fault conditions at 3, 8 and 9 and under various internal fault conditions (at 7).

Figure 5.11 demonstrates the differential relay parameters during an out-of-zone three-phase fault at location 8. It can be seen that the fault causes C.T. saturation which leads to a differential current in excess of 2000A. It can also be seen that the differential current exceeds the 20% restraining current as the trip delay timer activates. The delay timer reaches approximately 1.83 cycles before the C.T. saturation decreases enough to reduce the differential current below the 20% restraining current. The trip delay timer is set for 5 cycles to allow the adjacent protections to clear faults before allowing the relay to trip. This figure suggests the basis of the time delay may be conservative as the C.T.s may come out of saturation before adjacent protections will operate.

Figure 5.11 – Bus A Differential Relay Operation During a Three-Phase Fault at 8

Figure 5.12 – Bus A Differential Relay Operation During a Three-Phase Fault at 7

Time offset: 0

Figure 5.12 demonstrates the differential relay parameters during an in-zone three-phase fault at location 7. The differential current can be seen to rise quickly to over 12kA which enables the trip delay timer. C.T. saturation can be seen to cause temporary decreases in both the differential and restraining currents. At all times during the fault, the differential current exceeds the 20% restraining current. The delay timer reaches 5 cycles and the trip output is asserted after a total of 5.05 cycles from the time the fault was initiated.

Figure 5.13 demonstrates a plot of the differential currents versus the restraining currents for the previous two faults. It can be seen that in-zone faults result in an immediate upward trajectory. Out-of-zone faults result in 'loop-like' patterns. Notice that the restraining current rapidly increases while the C.T.s are still unsaturated. As the C.T. saturation takes effect, the differential current increase and restraining current decreases. As the asymmetrical current decays and saturation decreases, the differential current again approaches zero.

Figure 5.13 – Bus A Differential Restraint Characteristic During Three-Phase Faults at 7 and 8

The differing trajectories demonstrated in Figure 5.13 create an opportunity for the implementation of saturation detection algorithms. These algorithms could be used to alert the relay of C.T. problems. These alerts could be used to enable variable time-delays and diagnostic alarms to improve the system reliability. The investigation of such algorithms and applications has been left as an area of future research.

Table 5.2 summarizes the testing results for the restrained differential relay at Bus A. It can be seen that the relay properly operated for all internal faults and did not operate for all external faults. The table demonstrates that the 5 cycle time delay has been set fairly conservatively. The results support a possible reduction in the time delay, should the application require it. For this study, the time delay of 5 cycles will be maintained. The table also demonstrates that the relay operation occurs very quickly (beyond the intentional time delay). It is expected that higher impedance faults will result in slightly longer time delays due to the running mean value used in the discrete Fourier magnitude evaluation.

Table 5.2 – Summary of Test Results for the Restrained Differential Relay at Bus A

Location	Fault Type	Timer Enable Duration (cycles)	Trip	Total Trip Delay (cycles)
8	3-phase	1.86	No	N/A
3	3-phase	1.86	No	N/A
9	3-phase	1.05	No	N/A
7	3-phase	5	Yes	5.05
7	a-b	5	Yes	5.06
7	a-ground	5	Yes	5.13
7	a-c-ground	5	Yes	5.06

5.4.1.2 Restrained Directional Differential Relay at Bus B

The restrained directional differential relay will be tested using the same approach in Section 5.4.1.1. The relay will be tested under three-phase fault conditions at 7, 6 and 12 and under various internal fault conditions (at 8).

Figure 5.14 demonstrates the differential relay parameters during an out-of-zone three-phase fault at location 7. It can be seen that the fault causes C.T. saturation which leads to a differential current in excess of 2000A. It can also be seen that the differential current exceeds the 20% restraining current. Notice that the directional trip permissive is not met at any point throughout the fault. Thus the trip delay timer is never activated and the relay does not issue a trip command. This operation is in accordance with expectations.

Figure 5.14 – Bus B Differential Relay Operation During a Three-Phase Fault at 7

Time offset: 0

Figure 5.15 – Bus B Differential Relay Operation During a Three-Phase Fault at 8

Figure 5.15 demonstrates the differential relay parameters during an in-zone three-phase fault at location 8. The differential current can be seen to rise quickly to over 12kA which almost instantly exceeds the restraining current. The directional trip permissive is met after a delay of approximately 0.39 cycles. This enables the trip delay timer which times-out after 0.25 cycles and generates the trip output. The total delay from occurrence of the fault to the issuance of the trip command is 0.64 cycles. This operation is in accordance with expectations. It can be seen that the directional differential relay offers significantly improved response time over the non-directional implementation while maintaining security.

Table 5.3 summarizes the testing results for the restrained directional differential relay at Bus B. It can be seen the relay properly operated for all internal faults and did not operate for all external faults. Again, the superior response time is demonstrated for all fault types. In all cases, the relay operates in less than 1 cycle even with the inclusion of the $\frac{1}{4}$ cycle delay. Again, it is expected that, higher impedance faults will result in slightly longer time delays due to the running mean value used in the discrete Fourier magnitude evaluation.

Table 5.3 – Summary of Test Results for the Restrained Directional Differential Relay at Bus B

Location	Fault Type	Timer Enable Duration (cycles)	Trip	Total Trip Delay (cycles)
7	3-phase	0	No	N/A
6	3-phase	0	No	N/A
12	3-phase	0	No	N/A
8	3-phase	0.25	Yes	0.64
8	a-b	0.25	Yes	0.58
8	a-ground	0.25	Yes	0.75
8	a-c-ground	0.25	Yes	0.72

5.4.2 Individual Distance Relay Testing Results

There are four different distance relays used in the sample application, the phase and ground relays in both the mho and directional characteristics. One particular instance of each relay will be selected from the sample application for testing. This testing will verify the relay's performance and functionality for several of the fault types and fault locations for which the relay is intended to protect. For this testing, all breakers will be disabled to ensure that no other relays interfere with the relay being tested. The fault will be initiated at a time of 4 cycles into the simulation, such that the 'a' phase voltage will be zero at the initiation of the fault. This will ensure that the 'a' phase fault current has the maximum possible DC offset.

5.4.2.1 Phase Distance Relay (Mho Characteristic) at M4

Testing of this particular relay will be representative of the phase distance relay at M3 and the phase distance relays protecting Line 5 and 6 at Station #2. This relay will be tested with three-phase and phase-to-phase faults at locations 6, 12, 13 and 14. This corresponds to testing at 0%, 50% and 100% of the line length in the forward direction as well as testing in the immediate reverse direction.

Figure 5.16 demonstrates the phase distance relay parameters during a three-phase fault at 13. Prior to the fault the relay measures an impedance of approximately 180Ω despite the fact that the load impedance was calculated to be 90.6Ω in Section 4.1. The observation can be explained by what is known as the 'in-feed' effect. As there are multiple (two) paths for the total current to flow to the load(s), any particular distance relay may only see a fraction of that current. In this case, the relay only observes half of the current and therefore the relay calculates an impedance which is double that of the true load impedance. The 'in-feed' effect will not cause errors for faults on the local line, but can frequently cause impedance measurement errors for faults on remote lines. It can be seen that, in steady-state, the relay measures the apparent impedance to the fault as $18.47\angle 81.25^\circ\Omega$ which closely matches the expected value of $18.395\angle 84.15^\circ\Omega$. The forward zone 1 time delay is enabled 0.5 cycles after the initiation of the fault and the trip signal is generated 0.25 cycles later. This operation is in accordance with expectations.

Figure 5.16 – M4 Phase Distance Relay Operation During a Three-Phase Fault at 13

Figure 5.17 – M4 Phase Distance Relay Operation During a Phase ‘a’-‘b’ Fault at 6

Time offset: 0

Figure 5.17 demonstrates the phase distance relay parameters during a phase 'a'-'b' fault at 6. Notice the discontinuities in the magnitude and phase waveforms. As this fault involves a current reversal, the current magnitude will pass through zero which causes the phase reversal and the spike in the magnitude waveform. It can be seen that the relay measures an apparent impedance which approaches zero with a phase of approximately -80° . The reverse zone 1 time delay is enabled 0.78 cycles after the initiation of the fault and the trip signal is generated 10 cycles later. This operation is in accordance with expectations.

Figure 5.18 demonstrates a plot of the measured apparent impedances for various faults against the relay R-X diagram. The figure demonstrates consistent operation of the phase distance relay for the various multiphase faults. Notice that the transient oscillations in the output of the discrete Fourier algorithm results in vortex-like shapes as the measured impedances approach steady-state. It can be seen that these oscillations could cause the relay to over-reach (i.e. a zone 2 fault could be treated as a zone 1). The graph, however, demonstrates that the 90% zone 1 settings do not over-reach the line during this transient operation. Nonetheless, the 10% safety margin only included a 5% margin for relay error. It can be seen in Figure 5.18 that the entire 10% margin has been used for the relay error. This leaves no margin remaining for the line length estimation and impedance variation errors. It is recommended to include a minimum additional 5% margin in the relay reach settings in future applications employing this relay model. The current application testing will however, be completed on the basis of the originally designed settings.

Figure 5.18 – M4 Apparent Impedances During Faults at 6, 13 and 14

It can be seen that low impedance faults result in very little oscillation while higher impedance faults experience larger oscillations. This observation reveals a limitation of the discrete Fourier algorithm used to calculate the voltage and current phasors. Additional research into this phenomenon has revealed the exponentially decaying DC component of the fault current to be the underlying cause [36], [37]. The simple high-pass filters used in the relay models are ineffective at removing the decaying DC component as the non-periodic signal's frequency spectrum encompasses all frequencies [38]. Several papers have identified more sophisticated filtering methods capable of reducing the transient errors observed here. These filters include MIMIC, least-squares-fitting, cosine and Kalman filters to name only a few. The investigation of these alternative filters and algorithms has been left as an area of future research.

Table 5.4 summarizes the testing results for the phase distance relay at M4. It can be seen that the relay operated as expected for all multi-phase faults. The relay demonstrated very quick operating times as low as 0.47 cycles (including the 0.25 cycle definite time delay). As expected, higher impedance faults result in slightly longer operating times (beyond the 0.25, 10 and 18 cycle definite time delays for the various zones).

Table 5.4 – Summary of Test Results for the Phase Distance Relay at M4

Location	Fault Type	Expected Trip	Verified	Total Trip Delay (cycles)
6	3-phase	Reverse Zone 1	Yes	10.766
6	a-b	Reverse Zone 1	Yes	10.784
12	3-phase	Forward Zone 1	Yes	0.47
12	a-b	Forward Zone 1	Yes	0.56
13	3-phase	Forward Zone 1	Yes	0.752
13	a-b	Forward Zone 1	Yes	0.752
14	3-phase	Forward Zone 2	Yes	18.626
14	a-b	Forward Zone 2	Yes	18.626

5.4.2.2 Ground Distance Relay (Mho Characteristic) at M4

Testing of this particular relay will be representative of the ground distance relay at M3 and the ground distance relays protecting Line 5 and 6 at Station #2. This relay will be tested with phase-to-ground faults at locations 6, 12, 13 and 14. This corresponds to testing at 0%, 50% and 100% of the line length in the forward direction as well as testing in the immediate reverse direction.

Figure 5.19 demonstrates the ground distance relay parameters during a phase-to-ground fault at 14. It can be seen that, in steady-state, the relay measures the impedance to the fault as $36.9 \angle 78.4^\circ \Omega$ which closely matches the expected value of $36.79 \angle 84.15^\circ \Omega$. The forward zone 2 time delay is enabled 0.61 cycles after the initiation of the fault and the trip signal is generated 18 cycles later. This operation is in accordance with expectations.

Figure 5.19 – M4 Ground Distance Relay Operation During a Phase-to-Ground Fault at 14

Time offset: 0

Figure 5.20 – M4 Ground Distance Relay Operation During a Phase-to-Ground Fault at 12

Figure 5.20 demonstrates the ground distance relay parameters during a phase-to-ground fault at 12. It can be seen that the relay measures an impedance which approaches zero with a phase of approximately 80° . The forward zone 1 time delay is enabled 0.39 cycles after the initiation of the fault and the trip signal is generated 0.25 cycles later. This operation is in accordance with expectations.

Figure 5.21 demonstrates a plot of the measured apparent impedances for phase-to-ground faults at various locations against the relay R-X diagram. Notice the same vortex-like shapes observed in phase distance relay can be seen in the ground distance relay as well. The graph, however, demonstrates that the 90% zone 1 settings do not over-reach the line during this transient operation. Similarly, the recommendations made in Section 5.4.2.1 apply equally to the ground distance relay.

Figure 5.21 – M4 Apparent Impedances During Ground Faults at 6, 12, 13 and 14

Table 5.4 summarizes the testing results for the ground distance relay at M4. It can be seen that the relay operated as expected for all phase-to-ground faults. The relay demonstrated very quick operating times as low as 0.64 cycles (including the 0.25 cycle definite time delay). As expected, higher impedance faults result in slightly longer operating times (beyond the 0.25, 10 and 18 cycle definite time delays for the various zones).

Table 5.5 – Summary of Test Results for the Ground Distance Relay at M4

Location	Fault Type	Expected Trip	Verified	Total Trip Delay (cycles)
6	'a'-ground	Reverse Zone 1	Yes	10.874
12	'a'-ground	Forward Zone 1	Yes	0.638
13	'a'-ground	Forward Zone 1	Yes	0.83
14	'a'-ground	Forward Zone 2	Yes	18.608

5.4.2.3 Phase Distance Relay (Directional Characteristic) at M2

Testing of this particular relay will be representative of the directional phase distance relay at M1 and the directional phase distance relays protecting Line 5 and 6 at Station #2. This relay will be tested with three-phase and phase-to-phase faults at locations 4, 5, 6 and 12. This corresponds to testing at 0%, 50% and 100% of the line length in the forward direction as well as testing in the immediate reverse direction.

Figure 5.22 demonstrates the phase distance relay parameters during a phase 'a'-to-'b' fault at 5. It can be seen that, in steady-state, the relay measures the impedance to the fault as 8.67Ω which closely matches the expected value of 8.59Ω leading to an error of less than 1%. The forward direction is detected 0.39 cycles after the initiation of the fault. The forward zone 1 time delay is enabled 0.64 cycles after the initiation of the fault and the trip signal is generated 0.25 cycles later. This operation is in accordance with expectations.

A further observation can be made regarding the momentary reset of the forward zone 1 timer after the initiation of the trip signal. It can be seen that the measured impedance temporarily rises before returning to steady-state. An examination of the current waveforms reveals that C.T. saturation caused a temporary decrease in the measured current and a corresponding increase in the measured impedance. In this case, C.T. saturation has not degraded the relay performance.

Figure 5.22 – M2 Phase Distance Relay Operation During a Phase ‘a’-to-‘b’ Fault at 5

Time offset: 0

Figure 5.23 – M2 Phase Distance Relay Operation During a Three-Phase Fault at 12

Time offset: 0

Figure 5.23 demonstrates the phase distance relay parameters during a three-phase fault at 12. It can be seen that the relay measures an impedance which approaches zero in the reverse direction. The reverse zone 1 time delay is enabled 0.39 cycles after the initiation of the fault and the trip signal is generated 10 cycles later. This operation is in accordance with expectations.

Table 5.6 summarizes the testing results for the phase distance relay at M2. It can be seen that the relay operated as expected for all multi-phase faults. The relay demonstrated very quick operating times as low as 0.596 cycles (including the 0.25 cycle definite time delay). As expected, higher impedance faults resulted in slightly longer operating times (beyond the 0.25, 10 and 18 cycle definite time delays for the various zones).

Table 5.6 – Summary of Test Results for the Phase Distance Relay at M2

Location	Fault Type	Expected Trip	Verified	Total Trip Delay (cycles)
4	3-phase	Forward Zone 2	Yes	18.842
4	'a'-'b'	Forward Zone 2	Yes	18.92
5	3-phase	Forward Zone 1	Yes	0.89
5	'a'-'b'	Forward Zone 1	Yes	0.89
6	3-phase	Forward Zone 1	Yes	0.596
6	'a'-'b'	Forward Zone 1	Yes	0.638
12	3-phase	Reverse Zone 1	Yes	10.388
12	'a'-'b'	Reverse Zone 1	Yes	10.388

Note: Source #2 was taken out of service for testing at location #4.

5.4.2.3 Ground Distance Relay (Directional Characteristic) at M2

Testing of this particular relay will be representative of the directional ground distance relay at M1 and the ground distance relays protecting Line 5 and 6 at Station #2. This relay will be tested with phase-to-ground faults at locations 4, 5, 6 and 12. This corresponds to testing at 0%, 50% and 100% of the line length in the forward direction as well as testing in the immediate reverse direction.

Figure 5.24 demonstrates the ground distance relay parameters during a phase-to-ground fault at 5. It can be seen that, in steady-state, the relay measures the impedance to the fault as 8.65Ω which closely matches the expected value of 8.59Ω leading to an error of less than 1%. The forward direction is detected 0.11 cycles after the initiation of the fault. The forward zone 1 time delay is enabled 0.69 cycles after the initiation of the fault and the trip signal is generated 0.25 cycles later. This operation is in accordance with expectations.

Figure 5.24 – M2 Ground Distance Relay Operation During a Phase-to-Ground Fault at 5

Figure 5.25 – M2 Ground Distance Relay Operation During a Phase-to-Ground Fault at 6

Figure 5.25 demonstrates the ground distance relay parameters during a phase-to-ground fault at 12. It can be seen that the relay properly measures an impedance which approaches zero. The forward direction is detected 0.09 cycles after the initiation of the fault. The forward zone 1 time delay is enabled 0.40 cycles after the initiation of the fault and the trip signal is generated 0.25 cycles later. This operation is in accordance with expectations.

Table 5.7 summarizes the testing results for the ground distance relay at M4. It can be seen that the relay operated as expected for all phase-to-ground faults. The relay demonstrated very quick operating times as low as 0.656 cycles (including the 0.25 cycle definite time delay). As expected, higher impedance faults result in slightly longer operating times (beyond the 0.25, 10 and 18 cycle definite time delays for the various zones).

Table 5.7 – Summary of Test Results for the Ground Distance Relay at M2

Location	Fault Type	Expected Trip	Verified	Total Trip Delay (cycles)
4	'a'-ground	Forward Zone 2	Yes	18.86
5	'a'-ground	Forward Zone 1	Yes	0.938
6	'a'-ground	Forward Zone 1	Yes	0.656
12	'a'-ground	Reverse Zone 1	Yes	10.454

Note: Source #2 was taken out of service for testing at location #4.

5.4.3 Comprehensive Primary Protection Testing Results

The intent of this section is to comprehensively verify the functionality and coordination of the designed protection system. This will be the final verification to demonstrate the functionality of the individual protection elements, the validity of the relay settings and the interaction/coordination of all the simulated devices. To perform the verification, faults are simulated at all locations indicated on Figure 5.10. This test is repeated to include each of the three-phase, phase-to-phase and phase-to-ground faults.

Including all of the waveforms of this testing would make this report prohibitively long. As such, these results will be presented in tabular form (see Table 5.8). As an example of the results observed throughout the testing, Figures, 5.26 and 5.27 display the various breaker statuses and current waveforms at each of the two stations during a phase 'b'-'c' fault at location 12.

Figure 5.26 demonstrates the Station #2 waveforms. Notice the expected forward zone 2 time delay of 0.3 seconds (18 cycles) before clearing the fault. It can also be seen that the proper two breakers, M6 and T2 clear this fault. Thus, Figure 5.26 represents a successful validation of the Station #2 operation for this fault.

Figure 5.27 demonstrates the Station #1 waveforms. Notice the expected forward zone 1 time delay of 0.25 cycles (almost instantaneous) before clearing the fault. It can also be seen that the proper breaker, M4 clears this fault. Thus, Figure 5.27 represents a successful validation of the Station #1 operation for this fault.

Figure 5.26 – Breaker Statuses and Current Waveforms at Station #2 During a Phase ‘b’-‘c’

Fault at Location 12

Figure 5.27 – Breaker Statuses and Current Waveforms at Station #1 During a Phase ‘b’-‘c’
Fault at Location 12

Time offset: 0

Table 5.8 – Comprehensive Protection Verification Summary

Protection	Fault Location																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
S1-L1	FZ2	FZ1	FZ1																	
S1-L2				FZ2	FZ1	FZ1														
Bus A							Trip													
Bus B								Trip												
S1-L3									FZ1	FZ1	FZ2									
S1-L4												FZ1	FZ1	FZ2						
S2-L3									FZ2	FZ1	FZ1									
S2-L4												FZ2	FZ1	FZ1						
S2-L5															FZ1	FZ1	FZ2			
S2-L6																		FZ1	FZ1	FZ2
Verification																				
3-Phase	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Phase 'b'-'c'	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Phase 'c'-Ground	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Note: Testing at locations 1, 4, 17 and 20 was completed with the adjacent source disabled.

Table 5.8 displays the comprehensive testing results. The distance protection devices and trip types are identified using the nomenclature presented in Section 4.5.5. Due to the near-ideal modeling of the Sources 1-4, it was necessary to disable each source while testing faults at the source terminals (locations 1, 4, 17, 20). All successful verifications have been identified with a checkmark at the bottom of the table. The verification has proven that the protection elements and settings operate as expected.

Chapter 6 – Conclusions and Recommendations

Simulation packages like the Matlab Simulink software used throughout this report have gained widespread use in various engineering fields. Early designers of protection systems were limited to laboratory testing and actual field testing to verify the performance of their designs. This type of testing is expensive, time consuming and often impractical. This report has demonstrated that these simulation packages are invaluable for learning and understanding protection systems as well as verifying and troubleshooting protection system designs.

A model for a saturable iron-core current transformer was developed and the necessary instantaneous saturation parameters were successfully derived from manufacturer supplied data. The model was found to suitably match expected performance. This model enhanced the testing of the protective relays by providing a more realistic current measurement. The lesser non-linear effects of eddy current and hysteresis were not modeled and have been left as an area of future work.

Several differential relay models were produced and tested. This modeling provided valuable learning regarding their relative performance and weaknesses. The differential relay models were tested under various fault conditions and performance closely matched expectations. It was observed that current transformer errors, predominantly due to saturation, can cause differential protection to trip unnecessarily. As it is generally impractical to eliminate the possibility of current transformer saturation during faults, several methods of mitigating this problem were examined and modeled. One particular method, known as a restrained directional differential relay, was proven to provide sub-cycle protection and immunity to the effects of current transformer saturation.

Several models for both phase and ground distance protection relays were developed. The directional and mho characteristic types of these relays were tested and both performed as expected in steady state. Under transient conditions, these relays were observed to exhibit ringing in the measured apparent impedances. This was seen to cause overshoot of the actual impedance and increases the possibility of a transient zone over-reaching trip. The source of this

transient performance was determined to be caused by the decaying DC component of the fault current and the discrete Fourier transform methods employed to estimate the voltage and current phasors. Commercially available protection relays frequently use similar Fourier methods with more sophisticated filtering to obtain superior transient performance over the models developed in this report. Further work could include investigation of improved filtering and alternative algorithms that could improve this transient performance.

A small sample bulk-power transmission system was presented. Using the modeled protection elements, a protection design for the system was created. Current transformers were all sized in accordance with generally accepted practice recommended in IEEE C37-110. All of the relay settings were developed from system analysis and the expert guidelines obtained from a wide literature review. The resulting design was tested in a systematic fashion and was demonstrated to be effective. Notably, the safety margins recommended by expert guidelines were found to be necessary due to the transient overshoot observed in the phasor estimation. It is recommended to include the transient performance of the phasor estimation techniques in the rationale for future protection design settings. The simulation of all the various faults at all of the key locations in the power system was invaluable to proving and troubleshooting the protection design. For this project, this was undertaken as a manual operation and found to be quite cumbersome. It is recommended to investigate a methodology to automate this type of validation.

Appendix A – Instantaneous Saturation Parameter Calculations

Table A.1 – Instantaneous Saturation Parameters for the 1200:5 Current Transformer of Figure 2.17

N	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Is,rms (A)	0.002	0.005	0.01	0.02	0.05	0.1	0.2	0.5	1	2	5	10	20	50	100
Vs,rms (V)	2.8	12	32.5	95	335	410	420	435	450	460	475	490	500	525	550
Kn	0.2693	0.1089	0.0647	0.0508	0.0442	0.3830	11.06	13.60	20.14	86.63	145.3	203.2	885.7	685.9	1150
An	8.7E-06	0.0008	0.0036	0.0345	0.5321	0.0257	0.0002	0.0004	0.0004	0.0002	0.0004	0.0004	0.0002	0.0015	0.0014
Bn	0	0.0002	0.0008	0.0043	0.0351	0.0145	0.0019	0.0116	0.0262	0.0259	0.1083	0.2586	0.2538	2.2655	4.6438
Cn	-2.9E-05	-2.8E-05	-6.6E-05	-3.1E-04	-2.6E-03	-9.3E-03	-4.1E-02	-2.4E-01	-7.1E-01	-3.4E+00	-2.5E+01	-7.0E+01	-3.4E+02	-2.2E+03	-7.2E+03
theta, n (°)	13.49	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00
theta, n-1 (°)	0	13.49	21.67	20.01	16.47	54.79	77.47	74.91	75.16	78.03	75.56	75.79	78.52	72.25	72.66
dn	0.0E+00	1.1E-05	5.2E-05	1.6E-04	7.1E-04	2.5E-03	6.4E-03	9.0E-02	4.7E-01	1.3E+00	8.3E+00	4.8E+01	1.3E+02	1.1E+03	4.6E+03
tn (rad)	0.2355	1.3353	1.1926	1.2216	1.2833	0.6145	0.2187	0.2634	0.2589	0.2089	0.2520	0.2481	0.2003	0.3098	0.3027
sn	0.2269	-0.2269	-0.3431	-0.3215	-0.2719	-0.4711	-0.2118	-0.2514	-0.2475	-0.2029	-0.2414	-0.2380	-0.1950	-0.2904	-0.2845
gn	-0.0276	-0.9724	-0.9293	-0.9397	-0.9589	-0.5765	-0.2169	-0.2603	-0.2560	-0.2074	-0.2493	-0.2455	-0.1990	-0.3049	-0.2981
Cn Summation Term	6.3E-07	3.9E-05	1.2E-04	4.7E-04	3.3E-03	1.2E-02	4.7E-02	3.3E-01	1.2E+00	4.7E+00	3.3E+01	1.2E+02	4.7E+02	3.3E+03	1.2E+04
Flux-linkage,rms (Wb*turns)	0.0074	0.0318	0.0862	0.2520	0.8886	1.0876	1.1141	1.1539	1.1937	1.2202	1.2600	1.2998	1.3263	1.3926	1.4589
Flux-linkage,pk (Wb*turns)	0.0105	0.0450	0.1219	0.3564	1.2567	1.5380	1.5756	1.6318	1.6881	1.7256	1.7819	1.8381	1.8757	1.9694	2.0632
Is,pk (A)	0.0028	0.0066	0.0116	0.0235	0.0633	0.1710	0.5860	1.351	2.485	5.734	13.91	25.34	58.57	122.9	230.7
Parameters for Simulink:															
Turns Ratio=	240	1200:5													
Ip,pk (A)	0.6788	1.581	2.776	5.637	15.18	41.05	140.6	324.3	596.3	1376	3338	6082	14056	29493	55367
Flux,pk (Wb)	4.4E-05	1.9E-04	5.1E-04	1.5E-03	5.2E-03	6.4E-03	6.6E-03	6.8E-03	7.0E-03	7.2E-03	7.4E-03	7.7E-03	7.8E-03	8.2E-03	8.6E-03

Table A.2 – Instantaneous Saturation Parameters for the 800:5 Current Transformer of Figure 4.3

N	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
I _{s,rms} (A)	0.002	0.005	0.01	0.02	0.05	0.1	0.2	0.5	1	2	5	10	20	50	100
V _{s,rms} (V)	1.6	4.6	11.5	40	200	295	305	330	345	355	375	390	395	405	430
K _n	0.4712	0.3622	0.1824	0.1049	0.0641	0.2359	10.65	5.75	23.29	78.76	89.6	218.2	2282.0	2092.3	624
A _n	4.3E-06	0.0001	0.0004	0.0075	0.2508	0.0550	0.0002	0.0018	0.0005	0.0002	0.0010	0.0005	0.0000	0.0002	0.0016
B _n	0	0.0001	0.0003	0.0021	0.0242	0.0238	0.0019	0.0266	0.0240	0.0285	0.1752	0.2517	0.0970	0.7473	6.2284
C _n	-3.0E-05	-2.9E-05	-6.3E-05	-3.0E-04	-2.6E-03	-8.7E-03	-4.2E-02	-2.1E-01	-8.3E-01	-3.3E+00	-2.4E+01	-7.7E+01	-3.8E+02	-2.3E+03	-4.5E+03
theta, n (°)	20.35	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00
theta, n-1 (°)	0	20.35	23.58	16.71	11.54	42.68	75.29	67.55	73.04	76.37	71.20	74.06	80.87	77.24	70.37
d _n	0.0E+00	9.7E-06	5.5E-05	1.7E-04	7.1E-04	3.1E-03	5.4E-03	1.2E-01	3.5E-01	1.4E+00	9.4E+00	4.1E+01	9.4E+01	1.0E+03	7.3E+03
t _n (rad)	0.3553	1.2155	1.1593	1.2792	1.3694	0.8258	0.2568	0.3917	0.2960	0.2379	0.3281	0.2782	0.1593	0.2227	0.3427
s _n	0.3261	-0.3261	-0.3666	-0.2754	-0.1960	-0.4984	-0.2456	-0.3529	-0.2790	-0.2290	-0.3050	-0.2641	-0.1566	-0.2154	-0.3165
g _n	-0.0624	-0.9376	-0.9165	-0.9578	-0.9798	-0.7351	-0.2540	-0.3818	-0.2917	-0.2357	-0.3222	-0.2747	-0.1586	-0.2208	-0.3360
C _n Summation Term	9.6E-07	3.8E-05	1.2E-04	4.7E-04	3.3E-03	1.2E-02	4.7E-02	3.3E-01	1.2E+00	4.7E+00	3.3E+01	1.2E+02	4.7E+02	3.3E+03	1.2E+04
Flux-linkage,rms (Wb*turns)	0.0042	0.0122	0.0305	0.1061	0.5305	0.7825	0.8090	0.8754	0.9151	0.9417	0.9947	1.0345	1.0478	1.0743	1.1406
Flux-linkage,pk (Wb*turns)	0.0060	0.0173	0.0431	0.1501	0.7503	1.1066	1.1442	1.2379	1.2942	1.3317	1.4067	1.4630	1.4818	1.5193	1.6131
I _{s,pk} (A)	0.0028	0.0069	0.0116	0.0228	0.0613	0.1454	0.5449	1.084	2.395	5.349	12.07	24.35	67.15	145.6	204.2
Parameters for Simulink:															
Turns Ratio=	160	800:5													
I _{p,pk} (A)	0.4525	1.105	1.860	3.655	9.82	23.27	87.2	173.4	383.1	856	1932	3896	10744	23303	32669
Flux,pk (Wb)	3.8E-05	1.1E-04	2.7E-04	9.4E-04	4.7E-03	6.9E-03	7.2E-03	7.7E-03	8.1E-03	8.3E-03	8.8E-03	9.1E-03	9.3E-03	9.5E-03	1.0E-02

Table A.3 – Instantaneous Saturation Parameters for the 1200:5 Current Transformer of Figure 4.3

N	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$I_{s,rms}$ (A)	0.002	0.005	0.01	0.02	0.05	0.1	0.2	0.5	1	2	5	10	20	50	100
$V_{s,rms}$ (V)	3.2	17	43	85	345	405	410	435	445	455	475	485	495	505	520
K_n	0.2356	0.0705	0.0544	0.0881	0.0366	0.5374	27.57	4.43	47.21	71.33	97.2	429.2	748.0	2719.8	1614
A_n	9.1E-06	0.0019	0.0057	0.0134	0.6415	0.0148	0.0000	0.0016	0.0002	0.0002	0.0009	0.0002	0.0002	0.0001	0.0004
B_n	0	0.0003	0.0010	0.0025	0.0428	0.0101	0.0007	0.0297	0.0118	0.0303	0.1618	0.1307	0.2914	0.5681	2.8702
C_n	-2.8E-05	-2.8E-05	-6.9E-05	-3.3E-04	-2.4E-03	-9.7E-03	-4.2E-02	-1.6E-01	-9.1E-01	-3.0E+00	-2.4E+01	-8.4E+01	-3.0E+02	-2.7E+03	-5.7E+03
θ_{n1} , n (°)	10.85	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00
θ_{n2} , n-1 (°)	0	10.85	23.29	30.39	14.26	58.41	81.04	70.48	77.83	77.97	73.31	78.34	78.46	78.58	76.20
d_n	0.0E+00	1.1E-05	4.9E-05	1.4E-04	8.7E-04	2.1E-03	5.2E-03	1.7E-01	2.6E-01	1.7E+00	9.0E+00	3.4E+01	1.7E+02	6.5E+02	6.1E+03
t_n (rad)	0.1894	1.3814	1.1643	1.0404	1.3219	0.5513	0.1563	0.3407	0.2124	0.2100	0.2912	0.2034	0.2013	0.1993	0.2408
s_n	0.1849	-0.1849	-0.3631	-0.4364	-0.2388	-0.4462	-0.1538	-0.3149	-0.2061	-0.2039	-0.2750	-0.1979	-0.1959	-0.1941	-0.2316
g_n	-0.0179	-0.9821	-0.9185	-0.8626	-0.9692	-0.5238	-0.1557	-0.3341	-0.2108	-0.2085	-0.2871	-0.2020	-0.2000	-0.1980	-0.2385
Cn Summation Term	5.1E-07	3.9E-05	1.2E-04	4.7E-04	3.3E-03	1.2E-02	4.7E-02	3.3E-01	1.2E+00	4.7E+00	3.3E+01	1.2E+02	4.7E+02	3.3E+03	1.2E+04
Flux-linkage,rms (Wb*turns)	0.0085	0.0451	0.1141	0.2255	0.9151	1.0743	1.0876	1.1539	1.1804	1.2069	1.2600	1.2865	1.3130	1.3396	1.3793
Flux-linkage,pk (Wb*turns)	0.0120	0.0638	0.1613	0.3189	1.2942	1.5193	1.5380	1.6318	1.6693	1.7068	1.7819	1.8194	1.8569	1.8944	1.9507
$I_{s,pk}$ (A)	0.0028	0.0065	0.0118	0.0257	0.0614	0.1824	0.6994	1.115	2.886	5.562	12.86	28.96	57.01	159.0	249.9
Parameters for Simulink:															
Turns Ratio=	240	1200:5													
$I_{p,pk}$ (A)	0.6788	1.555	2.827	6.160	14.74	43.77	167.9	267.7	692.7	1335	3085	6949	13683	38170	59968
Flux,pk (Wb)	5.0E-05	2.7E-04	6.7E-04	1.3E-03	5.4E-03	6.3E-03	6.4E-03	6.8E-03	7.0E-03	7.1E-03	7.4E-03	7.6E-03	7.7E-03	7.9E-03	8.1E-03

Table A.4 – Instantaneous Saturation Parameters for the 2000:5 Current Transformer of Figure 4.3

N	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$I_s, \text{rms (A)}$	0.002	0.005	0.01	0.02	0.05	0.1	0.2	0.5	1	2	5	10	20	50	100
$V_s, \text{rms (V)}$	8.6	37	88	205	555	625	650	700	725	755	800	850	875	885	900
K_n	0.0877	0.0353	0.0278	0.0286	0.0312	0.4969	3.29	3.28	15.25	19.73	43.4	49.5	350.1	3538.3	1739
A_n	8.2E-05	0.0077	0.0215	0.1122	1.0579	0.0175	0.0013	0.0071	0.0012	0.0019	0.0051	0.0064	0.0011	0.0001	0.0003
B_n	0	0.0005	0.0019	0.0077	0.0498	0.0109	0.0068	0.0478	0.0368	0.1081	0.3611	1.0412	0.6401	0.4079	2.5630
C_n	-2.9E-05	-2.8E-05	-6.8E-05	-3.1E-04	-2.6E-03	-9.7E-03	-3.6E-02	-2.3E-01	-8.5E-01	-2.9E+00	-2.5E+01	-6.7E+01	-3.6E+02	-2.9E+03	-5.4E+03
$\theta_n, n(^{\circ})$	13.44	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00	90.00
$\theta_n, n-1(^{\circ})$	0	13.44	24.86	25.42	21.68	62.62	74.06	68.21	74.91	73.79	70.69	70.25	76.27	81.38	79.52
d_n	0.0E+00	1.1E-05	4.9E-05	1.6E-04	7.1E-04	2.0E-03	1.1E-02	9.7E-02	3.3E-01	1.8E+00	7.7E+00	5.0E+01	1.1E+02	4.4E+02	6.4E+03
$t_n \text{ (rad)}$	0.2346	1.3362	1.1369	1.1271	1.1925	0.4778	0.2782	0.3803	0.2634	0.2828	0.3370	0.3447	0.2396	0.1505	0.1828
s_n	0.2261	-0.2261	-0.3815	-0.3877	-0.3432	-0.4083	-0.2641	-0.3446	-0.2514	-0.2680	-0.3121	-0.3180	-0.2306	-0.1482	-0.1788
g_n	-0.0274	-0.9726	-0.9073	-0.9032	-0.9293	-0.4598	-0.2747	-0.3712	-0.2603	-0.2791	-0.3307	-0.3379	-0.2373	-0.1499	-0.1818
Cn Summation Term	6.3E-07	3.9E-05	1.2E-04	4.7E-04	3.3E-03	1.2E-02	4.7E-02	3.3E-01	1.2E+00	4.7E+00	3.3E+01	1.2E+02	4.7E+02	3.3E+03	1.2E+04
Flux-linkage,rms (Wb*turns)	0.0228	0.0981	0.2334	0.5438	1.4722	1.6579	1.7242	1.8568	1.9231	2.0027	2.1221	2.2547	2.3210	2.3475	2.3873
Flux-linkage,pk (Wb*turns)	0.0323	0.1388	0.3301	0.7690	2.0820	2.3446	2.4384	2.6259	2.7197	2.8322	3.0011	3.1886	3.2824	3.3199	3.3762
$I_s, \text{pk (A)}$	0.0028	0.0066	0.0119	0.0245	0.0654	0.1959	0.5041	1.119	2.549	4.770	12.10	21.38	54.22	187.0	284.8
Parameters for Simulink:															
Turns Ratio=	400	2000:5													
$I_p, \text{pk (A)}$	1.1314	2.634	4.762	9.785	26.18	78.37	201.6	447.6	1019.7	1908	4841	8554	21686	74780	113928
Flux,pk (Wb)	8.1E-05	3.5E-04	8.3E-04	1.9E-03	5.2E-03	5.9E-03	6.1E-03	6.6E-03	6.8E-03	7.1E-03	7.5E-03	8.0E-03	8.2E-03	8.3E-03	8.4E-03

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