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Multilevel neutral point clamped/H-bridge inverters with sinusoidal pulse width modulation

Arifur Rahman Shohel
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Multilevel Neutral Point Clamped/H-Bridge Inverters with Sinusoidal Pulse Width Modulation

by

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**Bachelor of Engineering, Dhaka University of Engineering and Technology
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A project

presented to Ryerson University

**In partial fulfillment of the
requirements for the degree of
Master of Engineering
in the program of
Electrical and Computer Engineering**

Toronto, Ontario, Canada, 2007

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Multilevel Neutral Point Clamped/H-bridge Inverters with Sinusoidal Pulse Width Modulation

Master of Engineering

2007

Arifur Rahman Shohel

Electrical and computer Engineering

Ryerson University, Canada

ABSTRACT

This project focuses on the topology of multilevel neutral point clamped (NPC)/H-bridge inverters and their modified modulation technique for high-power (megawatts) medium voltage (typically 6000V) applications. A sinusoidal pulse width in-phase disposition modulation is proposed for five-level NPC/H-bridge inverters. The inverter achieves good harmonic performance and low dv/dt in its output voltage waveforms in comparison to the conventional three-level NPC inverter. A seven-level NPC/H-bridge topology and its sinusoidal pulse width in-phase disposition modulation are also proposed and investigated, which has better performance than the five-level inverters.

Theoretical analysis and computer simulation are carried out for the proposed inverter topologies and algorithms. The output voltage waveforms and harmonic performance are verified by experiments on a five-level NPC/H-bridge inverter.

ACKNOWLEDGEMENTS

The work presented in the thesis was carried out at the Laboratory of Electric Drive Research and Application (LEDAR) at Ryerson University.

At first I would like to thank GOD to allow me to study in engineering and to get me a best supervisor Professor Dr. Bin Wu. Also I would like to thank Professor Dr. Wu for his continues support and help during the period when I studied at Ryerson University. The precious advices and numerous discussions triggered insightful research and enhanced my academic knowledge and scientific inspiration.

I am grateful to Professor Dr. Richard Cheung and Professor Dr. David Xu and all the fellow students at LEDAR new and old lab for their support and friendly atmosphere. My appreciation also goes to Mr. Behran Azizi for his help and support.

I would like to share the joy of achievements with my families, my parents my brothers and my lovely wife Tinni. I am very grateful to my wife and my parents for their understanding and support.

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NOMENCLATURE

Generic Variable Usage Conventions

Variable Format	Meaning
F	CAPITALS: peak AC, rms AC or average DC value
f	LOWER CASE: instantaneous values
$[., ., .]$	SQUARE BRACKETS: switching states
$(., ., .)$	PARENTHESES: coordinate triple, 3-phase instantaneous values
$\mathbf{AB}$	BOLD CAPITALS: vector with tail A and tip B
$\mathbf{f}$	BOLD LOWER CASE: vector

Specific Variable Definitions

Variable	Meaning
a, b, c, o	inverter output terminals; transformer secondary terminals
(a, b, c)	three phase variables
A, B, C	transformer primary terminals
C	DC link capacitance
D	clamping diodes
E	capacitor voltage, voltage levels
f_1	fundamental frequency
f_{sw-dev}	device switching frequency
h	harmonic order
m_a	amplitude modulation index
m_f	frequency modulation index
N	AC neutral point
R_s	total mail-side resistance
s	time second
S	state value; switching function; power capacity
$[S_a, S_b, S_c]$	three-phase switching states
T_s	sampling period
THD	total harmonic distortion
V_{1rms}	rms value of the fundamental
$V_{1rms-max}$	maximum rms value of the fundamental
(v_a, v_b, v_c)	three-phase voltage
V_{ab}	line-to-line voltage
V_{an}	phase voltage
V_d	DC link voltage; rectifier output voltage
V_{ref}	magnitude of reference vector
ΔS	total state value change
δ	phase shift angle
δS	phase state value change
γ	arbitrary angle
ω	angular frequency

CHAPTER 1 INTRODUCTION

1.1 Background

Recent advances in the power-handling capabilities of static switch devices such as IGBTs with higher voltage rating has made the use of voltage inverter (VSI) feasible for high-power applications. High-power and high-voltage conversion systems have become very important issue for the power electronic industry handling the large ac drive and electrical power applications. Multilevel pulse width modulation (PWM) inverter topologies have drawn tremendous interest in the power industry since it can provide the high-power required for high power application.

The unique structure of multilevel voltage source inverters allows them to operate at high voltages without switching devices connected in series, which eliminates the device dynamic and static voltage sharing problems. The inverter is also capable to operate at megawatt power level, with low harmonic distortion and low dv/dt . All these features make this inverter technology applicable to high power utility interface and drives^{[1][2]}.

A limited number of multilevel topologies are suitable for medium voltage applications. The most known topologies are Neutral Point Clamped (NPC), Flying Capacitor (FC) Cascaded H-bridge (CHB) multilevel inverters. Other topologies such as hybrid converters have been proposed, but they are not fully accepted for the industrial applications^{[1][3]}.

There are a number of modulation schemes for multilevel inverters. The most popular schemes include Sinusoidal Pulse Width Modulation (SPWM), Space Vector Modulation (SVM), Selective Harmonic Elimination (SHE), Delta Modulation^[4]. In this thesis a modified sinusoidal pulse width modulation scheme, i.e., sinusoidal pulse width in-phase disposition modulation, is fully investigated for multilevel NPC/H-bridge inverters.

1.2 Neutral Point Clamped (NPC) Inverters

a. Three-level Neutral Point Clamped (NPC) Inverter

Among the other multilevel topologies, the three-level neutral point clamped (NPC) topology has been widely used^{[3][4]}. Fig. 1.1 shows a simplified circuit diagram of a three-level NPC inverter, where only one DC source V_d is needed. Two capacitors are used to split the DC voltage and provide a neutral point Z . The inverter leg A is composed of four active switches S_1 to S_4 with four anti-parallel diodes D_1 to D_4 . In high power industrial drives using this inverter topology, either IGBT or IGCT can be employed as a switching device.

Fig. 1.1 Three-level neutral point clamped (NPC) inverter.

The four switches are controlled as two complementary pairs. For example, switches S_1 and S_3 , S_2 and S_4 are complementary pairs. Each phase can be connected to three potentials: $V_{d/2}$, 0 , or $-V_{d/2}$.

The maximum rms value of the fundamental line-to-line voltage V_{1rms_max} is for sinusoidal pulse width modulation (SPWM) modulation it is

$$V_{1rms_max} = 0.5 \frac{\sqrt{3}}{\sqrt{2}} V_d = 0.61 V_d.$$

Table 1.1 Definition of switching states

Switching State	Device Switching Status (Phase A)				Inverter Terminal v_{AZ}
	S_1	S_2	S_3	S_4	
P	ON	ON	OFF	OFF	E
O	OFF	ON	ON	OFF	0
P	OFF	Off	ON	ON	E

The operating status of the switches can be represented by switching states shown in Table 1.1. The switching state 'P' denotes that the upper two switches in leg A are "ON" and the inverter terminal voltage v_{AZ} , which is the voltage at terminal A with respect to neutral point Z, is $+E$, whereas 'N' indicates that the lower two switches conduct, leading to $v_{AZ} = -E$. Switching state 'O' signifies that the two inner switches S_2 and S_3 are on and v_{AZ} is clamped to zero through the clamping diodes. Depending on the direction of load current i_A , one of the two clamping diodes is turned on. For instance, a positive load current ($i_A > 0$) forces D_{Z1} to turn on, and the terminal A is connected to the neutral point Z through the conduction of D_{Z1} and S_2 . It can be observed from Table. 1.1 that switches S_1 and S_3 operate in a complementary manner. With one switched on, the other must be off. Similarly, S_2 and S_4 also a complementary pair.

Fig. 1.2 Switching state, gate signals and inverter terminal voltage v_{AZ} (Phase A).

Fig.1.2 shows an example of switching state and gate signal arrangements, where v_{g1} to v_{g4} are the gate signals for S_1 to S_4 , respectively. The gate signals can be generated by carrier-based modulation, space vector modulation or selective harmonic elimination schemes. The waveform of the inverter terminal voltage v_{AZ} has three voltage levels, $+E$, 0 and $-E$. Compared with the two-level inverter, the three-level NPC inverter is able to eliminate more harmonics for a given switching frequency.^[5]

b. Five-level Neutral Point Clamped (NPC) Inverter

The simplified per-phase diagram of the five-level neutral point clamped (NPC) inverter is shown in Fig. 1.3. The inverter is composed of eight active switches and a number of clamping diodes per phase. The dc capacitors C_d are shared by all three phases. The voltage across each capacitor is E and total V_d is equally divided by capacitors ($V_d = 4E$). When the top three switches in leg A are on v_{AN} is $4E$ whereas the conduction of the bottom three switches creates v_{AN} to be zero.

Fig. 1.3 Per-phase diagram of the five-level NPC inverter

This is important to mention that the clamping diodes may withstand different reverse blocking voltages. For instance, when the inverter operates with $S_1 = S_2 = S_3 = S_4 = "I"$, the anode of the clamping diodes D_1 , D_2 and D_3 in Fig. 1.3 are connected to positive dc bus. The voltage applied to D_1 , D_2 and D_3 is the E , $2E$ and $3E$, respectively. In practice, the voltage rating for all the clamping diodes is normally selected to be the same as the active switches. As a result three diodes in series in D_3 and D'_1 , two diodes in series in D_2 and D'_2 .

Table 1.2 lists the component count for the multilevel diode clamped inverters. It has assumed that all the active switches and clamping diodes have the same voltage rating, the rated inverter output voltage is proportional to the number of active switches^[1]. The three-level inverter requires only six clamping diodes while the five-level inverter needs thirty-six clamping diodes. This is in fact one of the main reasons why the five-level NPC inverters are limited in industrial application.

Table 1.2 Component count of the multi-level NPC inverters

Voltage Level	Active switches	Clamping diodes	DC Capacitors
m	$6(m-1)$	$3(m-1)(m-2)$	$(m-1)$
3	12	6	2
4	18	18	3
5	24	36	4
6	30	60	5

1.3 Neutral Point Clamped (NPC)/H-bridge Inverters

a. Five-level Neutral Point Clamped (NPC)/H-bridge Inverter

The five-level NPC/H-bridge inverter shown Fig. 1.4 has some advantages over the three-level NPC inverter. The inverter phase voltages, v_{AN} , v_{BN} and v_{CN} , contain five voltage levels instead of three levels for the NPC inverter, leading to a lower dv/dt and total harmonic distortion (THD). The inverter does not have any switching devices in series, which eliminates the device dynamic and static voltage sharing problems^{[1][6][7]}.

Fig. 1.4 Five level Neutral Point Clamped/H-bridge inverter.

A modified in-phase disposition (IPD) modulation scheme for the five-level NPC/H-bridge inverter is shown in Fig. 1.5, where only the waveforms for the inverter phase A are given. The two modulating waves, v_{m1} and v_{m2} , have the same frequency and amplitude, but are 180° out of phase. The triangular carriers v_{cr1} and v_{cr2} are in phase but vertically disposed. The frequency modulation index is defined by $m_f = f_{cr} / f_m$, where f_m and f_{cr} are the frequencies of the modulating and carrier waves, respectively. The amplitude modulation index is given by $m_a = \hat{V}_m / \hat{V}_{cr}$, where $\hat{V}_m$ and $\hat{V}_{cr}$ are the peak amplitudes of the modulating and carrier waves, respectively.

The eight switches in inverter phase A constitute four complementary switch pairs: (S_{11}, S_{13}) , (S_{12}, S_{14}) , (S_{21}, S_{23}) and (S_{22}, S_{24}) . Therefore, the modulation scheme needs to generate only four independent gate signals for the top and bottom four switches. The modulating wave v_{m1} is used to generate the gating v_{g11} and v_{g14} for S_{11} and S_{14} , where v_{g11} is generated during the positive half cycle of v_{m1} while v_{g14} is produced during the negative half cycle of v_{m1} . The gate signals for S_{21} and S_{24} are arranged in a similar manner. The waveform for the inverter phase voltage v_{AN} is formed with five voltage levels.

Fig. 1.5 Modified IPD modulation for the five-level NPC/H-bridge inverter ($m_f = 6$).

b. Seven-level Neutral Point Clamped (NPC)/H-bridge Inverter

The output voltage and power of a three-level NPC inverter can be tripled by using 36 active switches, every three of which are connected in series. The seven-level NPC/H-

bridge inverter uses 36 active switches to achieve the same voltage and power ratings as the 36-switch NPC inverter. Each of the inverter phases is composed of two NPC legs in an H-bridge form. The seven-level NPC/H-bridge inverter has some advantages over the three-level NPC and the five-level NPC/H-bridge inverter. The inverter phase voltages contain seven voltage levels instead of three and five levels for the NPC inverter, leading to a lower dv/dt and total harmonic distortion (THD).

The inverter does not have any switching devices in series, which eliminates the device dynamic and static voltage sharing problems. However, the inverter requires three isolated dc supplies, which increases the complexity and cost of the dc supply system.

Multilevel inverters are used to meet the requirements coming from the motor side. One of the major advantages of multi-level inverters is the high inverter voltage they can achieve. The inverter voltage is decided by the voltage ratings of the switching devices. The majority of the MV drives from 1MW to 4MW work at 3.3kV to 6.6kV voltage levels. However, the voltage ratings of the switching devices are often limited. For MV drives they are often rated at 6kV for GTO/GCT, 1.7kV, 2.5kV, 3.3kV, 4.5kV or 6.5kV for IGBTs.

Among the other multilevel topologies, the three-level neutral point clamped (NPC) topology has been widely used. The maximum *rms* value of the fundamental of the line-to-line voltage $V_{l_{rms_max}}$ for SPWM modulation is

$$V_{l_{rms_max}} = 0.5 \frac{\sqrt{3}}{\sqrt{2}} V_d = 0.61 V_d$$

if the motor voltage is 2.3kV, the DC link voltage can be calculated to be around 3.3kV. For 3.3kV IGBTs, the highest inverter voltage of the three-level NPC topology can achieve is 2.3kV. If the inverter voltage is more than 2.3kV, for example 3.3kV, 4.16kV the device voltage rating should be more than 5.4kV in the NPC topology. However the voltage of the MV drives is often higher than 2.3kV, with most of them being at 4.16kV level. For the inverters with 4.16kV output voltage, the device rating is 5.5kV GCTs without any device in series.

The five-level NPC/H-bridge inverter is designed for inverter voltage higher than 4.16kV. It can achieve over 4.16kV inverter voltage without any device in series. However the output voltage is doubled in comparison with three-level NPC topology. For the five-level NPC/H-bridge inverters with SPWM modulation, the maximum *rms* value of the fundamental V_{1rms_max} is

$$V_{1rms_max} = \frac{\sqrt{3}}{\sqrt{2}} V_d = 1.224 V_d.$$

Let's consider the 6kV inverter with the NPC/H-bridge topology. The required DC link voltage is now 4.9kV and the device voltage will be of the same level.

To summarize, Table 1.3 compares the NPC and NPC/H-bridge topologies. It can be concluded that if 3.3kV IGBT's are used, the NPC topology is for drives up to 2.3kV and the NPC/H-bridge topology is for drives up to 4.16kV.

Table 1.3 Comparison of NPC and NPC/H-bridge inverters

Item/ Topology	Voltage levels	Max device voltage	Max gain (V_{1rms_max}/V_d)	# of IGBTs	# of clamping diodes	# of isolated DC supply	Max inverter voltage with 3.3kV IGBT
NPC	3	$V_d/2$	0.61	12	6	1	2.3kV
NPC/ H- bridge	5	$V_d/2$	1.22	24	12	3	4.16kV

1.4 Flying Capacitor Inverter

A typical configuration of the five-level flying-capacitor inverter is shown in Fig. 1.6. It is evolved from the two-level inverter by adding dc capacitors to the cascaded switches.

Assuming all the capacitors have the same voltage ratings. The five-level inverter requires twenty-two dc capacitors. There are four complementary switch pairs in each of the inverter legs. Therefore, only four independent gate signals are required for each inverter phase^{[8][9]}.

Fig. 1.6 Five-level Flying-Capacitor Inverter.

The flying-capacitor inverter can produce an inverter phase voltage with five voltage levels. When switches S_1 , S_2 , S_3 and S_4 conduct, the inverter phase voltage v_{AN} is $4E$, which is the voltage at the inverter terminal A with respect to the negative dc bus N. Similarly, with S_1 , S_2 and S_3 switched on, $v_{AN} = 3E$. It is noted that some voltage levels can be obtained by more than one switching state. The voltage level $2E$, for instance, can be produced by six sets of different switching states. The switching state redundancy is a common phenomenon in multilevel converters, which provides a great flexibility for the switching pattern design^[9].

Since the flying-capacitor inverter topology is derived from the two-level inverter, it carries the same features as the two-level inverter such as modular structure for the switching devices. It is also a multilevel inverter, producing the voltage waveforms with

reduced dv/dt and THD^[10]. However, the flying-capacitor inverter has some limitations, including:

- A large number of dc capacitors with separate pre-charge circuit. The inverter requires several banks of bulky dc capacitors, each of which needs a separate pre-charge circuit.
- Complex capacitor voltage balancing control. The dc capacitor voltages in the inverter normally vary with the inverter operating conditions. To avoid the problems caused by the dc voltage deviation, the voltages on the dc flying capacitors should be tightly controlled, which increases the complexity of the control scheme.

Due to the above mentioned drawbacks, the practical use of the flying-capacitor inverter in the drive system seems limited.

1.5 Cascaded H-bridge (CHB) Multilevel Inverter

The cascaded H-bridge multilevel inverter uses multilevel units of H-bridge power cells connected in series chain to generate high ac voltages^[11]. A typical configuration of a five-level CHB inverter is shown in Fig. 1.7, where each phase leg consists of two H-bridge cells powered by two isolated dc supplies of equal voltage E . The dc supplies are normally obtained by multi pulse diode rectifiers. The CHB inverter can produce a phase voltage with five voltage levels. When switches S_{11}, S_{21}, S_{12} and S_{22} conduct, The output voltage of the H-bridge cells H1 and H2 is $V_{H1} = V_{H2} = E$, The resultant inverter phase voltage is $V_{AN} = V_{H1} + V_{H2} = 2E$, which is the voltage at the inverter terminal A with respect to the inverter neutral N . Similarly, with S_{31}, S_{41}, S_{32} and S_{42} switched on $V_{AN} = -2E$. The other three voltage levels are E , 0 and $-E$. It is worth noting that the inverter phase voltage V_{AN} may not necessarily equal the load phase voltage V_{AO} , which is the voltage at node A with respect to the load neutral O .

Fig. 1.7 Five-level Cascaded H-bridge inverter.

The voltage level E , for instance, can be produced by three sets of different switching states. The switching state redundancy is a common phenomenon in multilevel converters. It provides a great flexibility for switching pattern design. The number of voltage levels in CHB inverter can be found from $m = (2H+1)$ where H is number of H-bridge cells per phase leg. The voltage level m is always an odd number for the CHB inverter while the other multilevel topologies such as neutral point clamped (NPC) inverters, it can be either an even or odd number^[12].

1.6 Modulation Techniques

The main function of a voltage source inverter (VSI) is to convert a fixed dc voltage to a three-phase ac voltage with variable magnitude and frequency. Selecting modulation technique depends on application, performance and cost. Among all modulation techniques four kinds of techniques are used. They are sinusoidal pulse width modulation, space vector modulation, selective harmonic elimination, and delta modulation.

a. Sinusoidal pulse width modulation (SPWM)

The technique of pulse width modulation changes the pulse width according to the modulation waveform (sinusoidal, trapezoidal) the carrier waveform is triangle waveform. The main purpose of pulse width modulation is to make inverter output voltage adjustable, make inverter output frequency adjustable and eliminate lower order harmonics^{[13][17]}.

Fig. 1.8 Three phase inverter with Sinusoidal pulse width modulation.

Fig. 1.9 Sinusoidal pulse width modulation.

The principle of the sinusoidal pulse width modulation schemes for two level inverter Fig. 1.8 is illustrated in Fig. 1.9, where V_{mA} , V_{mB} and V_{mC} are the three-phase sinusoidal modulating waves and V_{cr} is the triangle carrier wave. The fundamental-frequency component is the inverter output voltage controlled by the amplitude modulation index m_a

$$m_a = \frac{V_m}{V_{cr}}$$

where V_m and V_{cr} are the peak values of the modulating and carrier waves respectively. The amplitude modulation index m_a is usually adjusted by varying V_m while keeping V_{cr} fixed. The frequency modulation index is defined by m_f .

$$m_f = \frac{f_{cr}}{f_m}$$

where f_m and f_{cr} are the frequencies of the modulating and carrier waves, respectively. The fundamental component is proportional to modulation index and the fundamental frequency is determined by the frequency on modulating waveform.

There are two types of sinusoidal pulse width modulation schemes for multi-level inverter. They are phase-shifted modulation scheme and level-shifted modulation scheme. The level-shifted modulation also in three kinds they are in-phase disposition (IPD), alternative phase opposition disposition (APOD) and phase opposite disposition (POD).

Fig. 1.10(a) shows the principle of the phase-shifted modulation scheme where four triangular carriers waves are 90° (degree) phase displacement between any two adjacent carriers. There are three-phase sinusoidal modulating waves, only the phase A modulating wave V_m is shown in Fig. for simplicity^{[14][15]}.

Fig 1.10(b), (c), (d) show three schemes for the level-shifted multi-carrier modulation: (b) in-phase disposition (IPD), where all carriers are in phase; (c) alternative phase opposition disposition (APOD), where all carriers are alternatively in opposite disposition and (d) phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference. In what follows, only IPD modulation scheme is discussed since provides the best harmonic profile of all three modulation schemes^[15].

(a) Phase-shifted pulse width modulation scheme.

(b) In-phase disposition (IPD) pulse width modulation scheme.

(c) Alternative phase opposition disposition (APOD) pulse width modulation scheme.

(d) Phase opposite disposition (POD) pulse width modulation scheme.

Fig. 1.10 Sinusoidal pulse width modulation for multi-level inverter.

b. Space vector modulation (SVM)

Space vector modulation (SVM) is one of the preferred real-time modulation techniques and is widely used for digital control of voltage source inverters. There are eight possible combinations of switching states in the two-level inverter, among eight switching states, [PPP] and [OOO] are zero states and others are active states.

To derive the relationship between the space vectors and switching states assume that the operation of the inverter is three-phase balanced, we have

$$V_{AO}(t) + V_{BO}(t) + V_{CO}(t) = 0$$

Where V_{AO} , V_{BO} and V_{CO} are the instantaneous load phase voltages.

From mathematical point of view, one of the phase voltages is redundant since given any two phase voltage; the third can be readily calculated. Therefore, it is possible to transform the three-phase variables to equivalent two-phase variables. A typical space vector diagram for two level inverter is shown Fig. 1.11, where the six active vectors V_1 to V_6 form a regular hexagon with six equal sectors (I to VI). The zero vector V_0 lies on the centre of the hexagon.

The dwell time for the stationary vectors essentially represents the duty-cycle time (on-state or off-state time) of the chosen switches during a sampling period T_s of the modulation scheme.

$$T_0 = T_s - T_a - T_b$$

$$T_a = T_s m_a \sin\left(\frac{\pi}{3} - \theta\right)$$

$$T_b = T_s m_a \sin \theta$$

$$T_0 = T_s - T_b - T_c$$

$$m_a = \frac{\sqrt{3}}{V_d} V_{ref}$$

Fig. 1.11 Space vector diagram.

To adjust fundamental frequency of fundamental voltage the frequency of reference voltage V_{ref} need to be adjusted and to adjust magnitude of fundamental voltage the magnitude of V_{ref} need to be adjusted^[16].

c. Selected harmonic elimination (SHE)

This technique combines the square-wave switching and PWM to control the fundamental output voltage as to eliminate the designated harmonics from the output.

The voltage V_{Ao} , of an inverter leg, normalized by $\frac{1}{2}V_d$ is plotted in Fig. 1.12, where, six notches are introduced in the otherwise square-wave output, to control the magnitude of the fundamental voltage and to eliminate fifth and seventh harmonics. On a half-cycle basis, each notch provides one degree of freedom, that is, having three notches per half-cycle provides control of fundamental and elimination of two harmonics (in this case fifth and seventh).

Fig. 1.11 shows that the output waveform has odd half-wave symmetry (some-times it is referred to odd quarter-wave symmetry). Therefore, only odd harmonics (coefficient of sine series) will be present. Since in a three-phase inverter (consisting of three such inverter legs), the third harmonics and its multiples are canceled out in the output, these harmonics need not be eliminated from the output of the inverter leg by means of waveform notching. The switching frequency of a switch is seven times the switching frequency associated with a square-wave operation.

Fig. 1.12 Output waveform of programmed harmonic elimination of fifth and seventh harmonics.

The main purpose of selected harmonic elimination is to eliminate a number of unwanted low order harmonics and to control fundamental output voltage^[17].

The primary function of a voltage source inverter (VSI) is to convert a fixed dc voltage to a three-phase ac voltage with variable magnitude and frequency. Sinusoidal pulse width modulation has some advantages which makes this scheme popular than other modulation schemes. Space vector modulation (SVM) is one of the preferred real-time modulation techniques and is widely used for digital control of voltage source inverters. By comparing with sinusoidal pulse width modulation space vector modulation is complex. Selected harmonic elimination (SHE) is technique combines the square-wave switching and PWM to control the fundamental output voltage as to eliminate the designated harmonics from the output. Delta modulation is current regulated modulation

the inverter switching frequency may vary with parameters. This is considered as a major drawback of the current regulated inverter with the tolerance band control. When the inverter uses other modulation techniques such as SPWM and SVM, its switching frequency is set by the modulation scheme, independent of motor parameters. The advantages of Sinusoidal pulse width modulation are as follows:

- The output voltage magnitude is easy to adjust by adjusting amplitude modulation index (m_a);
- The fundamental frequency is easy to adjust by adjusting frequency of modulating wave (V_m);
- The lower order harmonics are eliminated;
- The switching frequency is set by the modulation scheme, independent from motor parameters.

1.7 Motivation and Objectives

There are generally three methods for higher inverter output voltage: connecting devices in series, using switching devices with higher voltage rating, or adopting multilevel topology. The first method can be used only when the problem of dynamic voltage sharing has been efficiently solved. Otherwise it should be avoided. The choice of the second method is really a complicated compromise of the cost, reliability and availability. Given limited device voltage ratings, the most effective solution to higher inverter voltage is multilevel topologies.

As mentioned earlier, there are a limited number of inverter topologies that provide multilevel voltages suitable for medium voltage applications. The most known topologies

are the Neutral Point Clamped (NPC), the Flying capacitor (FC) and Cascaded H-bridge (CHB) multilevel inverters. Other topologies such as hybrid converters have been proposed, but they are not fully accepted for the industrial applications. The NPC/H-bridge inverter has some unique features. It needs only three isolated DC sources. The phase voltage has a higher voltage level which leads to lower dv/dt , lower EMI and lower total harmonic distortion (THD). The inverter does not have any switching devices in series, which eliminates the device dynamic and static voltage sharing problems.

Modulation schemes for multilevel inverters are 1) Sinusoidal Pulse Width Modulation (SPWM) 2) Space Vector Modulation (SVM) 3) Selective Harmonic Elimination (SHE), and 4) Delta Modulation. This project focuses on sinusoidal pulse width (SPWM) in-phase disposition (IPD) modulation for multilevel NPC/H-bridge inverter because this modulation schemes has some advantages over other modulation schemes, including 1) the output voltage and fundamental frequency are easy to adjust by adjusting amplitude modulation index (m_a) and modulating wave frequency (V_m), 2) lower order harmonics are eliminated and 3) the switching frequency is set by the modulation scheme, independent of motor parameters.

In summary, the objectives of the thesis are;

- To design a sinusoidal pulse width modulation scheme for the multilevel Neutral Point Clamped (NPC)/H-bridge inverter to achieve better performance.
- To evaluate the performance of the multilevel NPC/H-bridge inverter.
- To analyze and investigate the harmonic contents and total harmonic distortion of the multilevel NPC/H-bridge inverter.
- To verify the performance of the multilevel NPC/H-bridge inverter experimentally.

1.8 Thesis Organization

The work of the thesis is organized in to five chapters.

Chapter 1 provides detailed theoretical background of multilevel inverters, including NPC inverters, NPC/H-bridge inverters, cascaded H-bridge inverters, and flying capacitor inverter.

Chapter 2 investigates a new modified sinusoidal pulse width in-phase disposition modulation schemes for the five-level NPC/H-bridge inverter. This chapter provides a detailed analysis on harmonic contents and total harmonic distortion (THD). The performance of the modulation scheme at different amplitude and frequency modulation indices is also evaluated.

Chapter 3 introduces the seven-level NPC/H-bridge inverter and its modified sinusoidal pulse width in-phase disposition modulation schemes. This chapter provides a detailed analysis on harmonic contents and total harmonic distortion. The performance of the modulation scheme at different amplitude and frequency modulation indices is also evaluated.

Chapter 4 provides the experimental verification of the five-level NPC/H-bridge inverter with sinusoidal pulse width modulation introduced in Chapter 2. It also verifies the voltage waveforms and harmonic contents.

Chapter 5 is the conclusions drawn from the research in this project.

Other supporting materials are attached in the appendix.

CHAPTER 2 FIVE LEVEL NEUTRAL POINT CLAMPED/H-BRIDGE INVERTER

2.1 Introduction

The diode clamped multilevel inverter (NPC) has been used in megawatt AC drives over the last decade. It uses clamping diodes and a group of cascaded DC capacitors to achieve multiple levels in the inverter output voltage for the reduction of dv/dt and total harmonic distortion (THD). The diode clamped inverter also features high operation voltage without switching devices in series. The inverter can be configured as a three-level, four-level and five-level topology. The five-level NPC/H-bridge inverter is developed from the three-level NPC inverter topology. The five-level inverter has some unique features that have promoted its application in the MV drive industry^{[1][2][4]}.

This chapter presents the five-level NPC/H-bridge topology with sinusoidal pulse width (SPWM) in-phase disposition (IPD) modulation technique. The operation principle of this inverter is discussed, and its harmonic performance under different operating conditions is analyzed.

2.2 Inverter Topology

The output voltage and power of the three-level NPC inverter can be doubled by using 24 active switches, every two of which are connected in series. The five-level NPC/H-bridge inverter shown in Fig. 2.1 also uses 24 active switches to achieve the same voltage and power ratings as the 24-switch NPC inverter. Each of the inverter phases is composed of two NPC legs in an H-bridge form. The five-level NPC/H-bridge inverter has some advantages over the three-level NPC inverter. The inverter phase voltages, v_{AN} , v_{BN} and

v_{CN} , contain five voltage levels instead of three levels for the NPC inverter, leading to a lower dv/dt and total harmonic distortion.

Fig. 2.1 Five-level neutral point clamped (NPC)/H bridge inverter.

The inverter does not have any switching devices in series, which eliminates the device dynamic and static voltage sharing problems.

2.3 Modulation Scheme

a. Principle

A modified sinusoidal pulse width in-phase disposition (IPD) modulation scheme shown in Fig. 2.2 for the five-level NPC/H-bridge inverter, where only the waveforms for the inverter phase A are given. The two modulating waves, v_{m1} and v_{m2} , have the same frequency and amplitude, but are 180° out of phase. The triangular carriers v_{cr1} and v_{cr2} are in phase but vertically disposed. The frequency modulation index m_f is defined by $m_f = f_{cr} / f_m$, where f_m and f_{cr} are the frequencies of the modulating and carrier waves, respectively. The amplitude modulation index m_a is given by $m_a = \hat{V}_m / \hat{V}_{cr}$, where $\hat{V}_m$ and $\hat{V}_{cr}$ are the peak amplitudes of the modulating and carrier waves, respectively.

The eight switches in inverter phase A constitute four complementary switch pairs: (S_{11}, S_{13}) , (S_{12}, S_{14}) , (S_{21}, S_{23}) and (S_{22}, S_{24}) . Therefore, the modulation scheme needs to generate only four independent gate signals for the top and bottom four switches. The modulating wave v_{m1} is used to generate the gating v_{g11} and v_{g14} for S_{11} and S_{14} , where v_{g11} is generated during the positive half cycle of v_{m1} while v_{g14} is produced during the negative half cycle of v_{m1} . The gate signals for S_{21} and S_{24} are arranged in a similar manner. The waveform for the inverter phase voltage v_{AN} is formed with five voltage levels.

Fig. 2.2 Modified IPD modulation for the five-level NPC/H-bridge inverter ($m_f=9$).

b. Example

The simulated waveform for the phase voltage v_{AN} of the five-level NPC/H-bridge inverter and its harmonic content are illustrated in Fig. 2.3. The inverter operates under the condition of $f_m = 60\text{Hz}$, $m_f = 15$ and $m_a = 0.8$. The device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 2 = 450\text{Hz}$. The waveform of v_{AN} is composed of five voltage levels, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 23th, but has triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$.

Fig. 2.3 Waveform and spectrum of the inverter phase voltage

($f_m = 60\text{Hz}$, $f_{sw,dev} = 450\text{Hz}$, $m_f = 15$ and $m_a = 0.8$).

The simulated waveform for the inverter line-to-line voltage v_{AB} is illustrated in Fig. 2.4. It contains nine voltage levels. The triplen harmonics in v_{AN} do not appear in v_{AB} due to the three-phase balanced system, resulting in a reduction of THD from 36.36% to 27.74%.

Fig. 2.4 Waveform and spectrum of inverter line to line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 450\text{Hz}, m_f = 15 \text{ and } m_a = 0.8).$$

2.4 Waveforms and Harmonic Content with variable amplitude modulation index (m_a)

The simulated waveforms for the five-level NPC/H-bridge inverter and its harmonic contents at variable amplitude modulation index (m_a) are discussed in this section. The

inverter operates under the condition of $f_m = 60\text{Hz}$, $m_f = 15$ and $m_a = 0.2$ to 1.0. The device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 2 = 540\text{Hz}$.

The waveform of v_{AN} is shown in Fig. 2.5 composed of three voltage levels at $m_a = 0.2$ and maintained three levels up to $m_a = 0.5$ shown in Fig. 2.6 whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 27th for $m_a = 0.2$ and 25th for $m_a = 0.5$ but has triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$.

Fig. 2.5 Waveform and spectrum of inverter phase and line voltage

($f_m = 60\text{Hz}$, $f_{sw,dev} = 450\text{Hz}$, $m_f = 15$ and $m_a = 0.2$).

The line-to-line voltage v_{AB} contains five voltage levels. The triplen harmonics in v_{AN} do not appear in v_{AB} due to the three-phase balanced system, resulting in a reduction of total harmonic distortion (THD).

Fig. 2.6 Waveform and spectrum of inverter phase and line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 450\text{Hz}, m_f = 15 \text{ and } m_a = 0.5).$$

From amplitude modulation index $m_a = 0.1$ to $m_a = 0.5$ inverter act as a three level inverter. It starts five level at $m_a = 0.51$.

Fig. 2.7 Waveform and spectrum of inverter phase and line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 450\text{Hz}, m_f = 15 \text{ and } m_a = 0.6).$$

In Fig. 2.7 shows waveform and spectrum of inverter at the condition of $m_a = 0.6$. Five voltage level starts from $m_a = 0.51$. As amplitude modulation index m_a increases then the voltage level increases with lower order harmonics also increases. In $m_a = 0.6$ a very small 23rd order harmonics also visible. In Fig. 2.8 shows waveform and spectrum of inverter at the condition of $m_a = 1.0$. The waveform of v_{AN} is composed of five voltage levels, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than 23rd. In this case The maximum fundamental-frequency voltage at $m_a = 1$ is given by $V_{AB1,max} = 1.224V_d$, which is two times that of the three-level NPC inverter.

Fig. 2.8 Waveform and spectrum of inverter phase and line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 450\text{Hz}, m_f = 15 \text{ and } m_a = 1.0).$$

The harmonic content of v_{AB} versus modulation index m_a is shown in Fig. 2.9. Since the high-order harmonic components can be easily attenuated by filters or load inductances, only the dominant harmonics centered around $2m_f$ are plotted. The n^{th} order harmonic voltage V_{ABn} (rms) is normalized with respect to the dc voltage V_d . The maximum fundamental-frequency voltage at $m_a = 1$ is given by $V_{AB1,\max} = 1.224V_d$, which is two times that of the three-level NPC inverter.

Fig. 2.9 Harmonic content of the five-level NPC/H-bridge inverter ($m_f = 15$).

Fig. 2.10 THD and m_a of the five-level NPC/H-bridge inverter ($m_f = 15$).

2.5 Waveforms and Harmonic Content with variable frequency modulation index (m_f)

The simulated waveform for the phase voltage v_{AN} of the five-level NPC/H-bridge inverter and its harmonic content is shown in Fig. 2.11(a). The inverter operates under the condition of $f_m = 60\text{Hz}$, $m_f = 18$ and $m_a = 0.9$. The device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 2 = 540\text{Hz}$. The waveform of v_{AN} is composed of five voltage levels, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 27th, but has triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$.

Fig. 2.11 Waveform and spectrum of inverter phase and line voltage

($f_m = 60\text{Hz}$, $f_{sw,dev} = 540\text{Hz}$, $m_f = 18$ and $m_a = 0.9$).

Line-to-line voltage v_{AB} is illustrated in Fig. 2.11(b). It contains nine voltage levels. The triplen harmonics in v_{AN} do not appear in v_{AB} due to the three-phase balanced system, resulting in a reduction of total harmonic distortion (THD).

Fig. 2.12 Waveform and spectrum of inverter phase and line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 630\text{Hz}, m_f = 21 \text{ and } m_a = 0.9).$$

The waveforms for the phase voltage v_{AN} and line-to-line voltage v_{AB} of the NPC/H-bridge inverter and its harmonic content are shown in Fig. 2.12 at $m_f = 21$ and in Fig. 2.13 at $m_f = 24$. The inverter operates under the condition of $f_m = 60\text{Hz}$ and $m_a = 0.9$. The device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 2 = 630\text{Hz}$ and $f_{sw,dev} = f_m \times m_f / 2 = 720\text{Hz}$ respectively.

The waveform of v_{AN} is composed of five voltage levels, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 33rd and 43rd respectively but has triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$. The line-to-line voltage v_{AB} contains nine voltage levels. The triplen harmonics in v_{AN} do not appear in v_{AB} due to the three-phase balanced system, resulting in a reduction of THD.

Fig. 2.13 Waveform and spectrum of inverter phase and line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 720\text{Hz}, m_f = 24 \text{ and } m_a = 0.9).$$

To summarize the operation of the five-level NPC/H-bridge inverter at fixed amplitude modulation index (m_a) with variable frequency modulation index (m_f) harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. When $m_f = 18$, harmonics are centered around 36th and 72nd and phase voltage v_{AN} does not contain any harmonics with the order lower than the 27th is shown in Fig. 2.12. When $m_f = 15$,

harmonics with lower order than the 23rd. At higher frequency modulation index (m_f) like $m_f = 21$ or $m_f = 24$ the waveform has same characteristics with sideband harmonics and harmonic with lower order also higher. The phase voltage contains triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$ but line-to-line voltage do not appear triplen harmonics due to the three-phase balanced system.

2.6 Other Modulation Scheme

The phase-shifted multi carrier modulation, phase opposition disposition (POD) and alternative phase opposition disposition (APOD) produce three level voltage waveform for the NPC/H-bridge inverter which has illustrated in Fig. 2.14. Applying APOD modulation scheme the waveform became three level with lots of lower order harmonics ($1mf+1$), ($1mf-1$) and poor THD=65.45%

Fig. 2.14 Waveform and spectrum of inverter line to line voltage at APOD modulation scheme with ($f_m = 60\text{Hz}$, $f_{sw,dev} = 450\text{Hz}$, $m_f = 15$ and $m_a = 0.8$).

2.7 Summary

This chapter introduces modified in-phase disposition sinusoidal pulse width modulation (SPWM-IPD) technique for the five-level Neutral Point Clamped (NPC)/H-bridge inverter. The operating principle of this inverter is explained and modulation schemes are discussed. Simulations are carried out in variable amplitude modulation index (m_a) and variable frequency modulation index (m_f). The SPWM-IPD modulation technique features low total harmonic distortion, simple modulation scheme and easy to implement. The above mentioned features of the five-level NPC/H-bridge inverter have promoted its application in the MV drives.

CHAPTER 3 SEVEN LEVEL NEUTRAL POINT CLAMPED/H-BRIDGE INVERTER

3.1 Introduction

Multilevel NPC/H-bridge inverters use clamping diodes and a group of cascaded DC capacitors to achieve multiple levels in the inverter output voltage for the reduction of dv/dt and total harmonic distortion (THD). The inverter also features high operation voltage without switching devices in series.

The seven-level neutral point clamped (NPC)/H-bridge inverter is developed from the five-level NPC/H-bridge inverter topology. This inverter has some unique features that have promoted its application in the MV drive industry. The operation principle of this inverter is discussed, and its harmonic performance under different operating conditions is analyzed.

3.2 Inverter Topology

The output voltage and power of a three-level NPC inverter can be tripled by using 36 active switches, every three of which are connected in series. The seven-level NPC/H-bridge inverter illustrated in Fig. 3.1 also uses 36 active switches to achieve the same voltage and power ratings as the 36-switch NPC inverter. Each of the inverter phases is composed of two NPC legs in an H-bridge form. The seven-level NPC/H-bridge inverter has some advantages over the three-level NPC and the five-level NPC/H-bridge inverter. The inverter phase voltages, v_{AN} , v_{BN} and v_{CN} , contain seven voltage levels instead of three and five levels for the NPC inverter, leading to a lower dv/dt and total harmonic distortion (THD).

Fig. 3.1 The seven-level NPC/H bridge inverter.

The inverter does not have any switching devices in series, which eliminates the device dynamic and static voltage sharing problems. However, the inverter requires three isolated dc supplies, which increases the complexity and cost of the dc supply system.

Each leg of seven-level NPC/H-bridge inverter is composed of six active switches, three dc capacitor and a number of clamping diodes per phase. In this inverter voltage across each capacitor is E and the total dc voltage V_d is equally shared by the capacitor that's means $V_d = E + E + E = 3E$.

3.3 Modulation Scheme

a. Principle

A modified sinusoidal pulse width in-phase disposition (IPD) modulation scheme for the seven-level NPC/H-bridge inverter illustrates in Fig. 3.2, where only the waveforms for the inverter phase A are given.

Fig. 3.2 Modified IPD modulation for the seven-level NPC/H-bridge inverter ($m_f = 9$).

The two modulating waves, V_{m1} and V_{m2} have the same frequency and amplitude, but are 180° out of phase. The triangular carriers V_{cr1} , V_{cr2} and V_{cr3} are in phase but vertically disposed. The frequency modulation index m_f is defined by $m_f = f_{cr} / f_m$, where f_m and f_{cr} are the frequencies of the modulating and carrier waves, respectively. The amplitude modulation index m_a is given by $m_a = \hat{V}_m / \hat{V}_{cr}$, where $\hat{V}_m$ and $\hat{V}_{cr}$ are the peak amplitudes of the modulating and carrier waves, respectively.

The twelve switches in inverter phase A constitute six complementary switch pairs: (S_{11}, S_{14}) , (S_{12}, S_{15}) , (S_{13}, S_{16}) , (S_{21}, S_{24}) , (S_{22}, S_{25}) and (S_{23}, S_{26}) . Therefore, the modulation scheme needs to generate only six independent gate signals for the top and bottom six switches. The modulating wave v_{m1} is used to generate the gating v_{g11} , v_{g15} and v_{g16} for S_{11} , S_{15} and S_{16} , where v_{g11} is generated during the positive half cycle of v_{m1} while v_{g15} and v_{g16} is produced during the negative half cycle of v_{m1} . The gate signals for S_{21} , S_{25} and S_{26} are arranged in a similar manner. The waveform for the inverter phase voltage v_{AN} is formed with seven voltage levels.

There are three neutral points in the inverter, whose potential may need a tight control to avoid any voltage deviation. However, for the drive system using a multi-pulse diode rectifier as a front end, the rectifier can be designed such that its mid-points can be directly connected to the neutral points of the inverter. In doing so, the inverter neutral point voltage are fixed by the rectifier and thus do not vary with the inverter operating conditions.

b. Example

The simulated waveform for the phase voltage v_{AN} of the seven-level NPC/H-bridge inverter and its harmonic content illustrates in Fig. 3.3. The inverter operates under the condition of $f_m = 60\text{Hz}$, $m_f = 15$ and $m_a = 0.8$.

Fig. 3.3 Waveform and spectrum of the inverter phase voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 300\text{Hz}, m_f = 15 \text{ and } m_a = 0.8).$$

The device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 3 = 300\text{Hz}$. The waveform of v_{AN} is composed of seven voltage levels, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 23rd, but has triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$.

Fig. 3.4 Waveform and spectrum of the inverter line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 300\text{Hz}, m_f = 15 \text{ and } m_a = 0.8).$$

The simulated waveform for the inverter line-to-line voltage v_{AB} is illustrates in Fig. 3.4. It contains thirteen voltage levels. The triplen harmonics in v_{AN} do not appear in v_{AB} due to the three-phase balanced system, resulting in a reduction of THD from 23.09% to 18.35%.

3.4 Waveforms and Harmonic Content with variable amplitude modulation index (m_a)

The simulated waveforms for the seven-level NPC/H-bridge inverter and its harmonic content shows in this section. The inverter operates under the condition of $f_m = 60\text{Hz}$, $m_f = 15$ and $m_a = 0.2$ to 1.0. The device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 3 = 300\text{Hz}$.

The waveform of v_{AN} is shown in Fig. 3.5 composed of three voltage levels at $m_a = 0.2$, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 27th, but has triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$.

Fig. 3.5 Waveform and spectrum of inverter Phase and line voltage

($f_m = 60\text{Hz}$, $f_{sw,dev} = 300\text{Hz}$, $m_f = 15$ and $m_a = 0.2$).

In line-to-line voltage v_{AB} is contains five voltage levels. The triplen harmonics in v_{AN} do not appear in v_{AB} due to the three-phase balanced system, resulting in a reduction of THD. The waveform of v_{AN} is shown in Fig. 3.6 composed of three voltage levels up to $m_a = 0.33$, wave form change from three level to five level at $m_a = 0.34$ whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 23rd.

Fig. 3.6 Waveform and spectrum of inverter phase and line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 300\text{Hz}, m_f = 15 \text{ and } m_a = 0.6).$$

In line-to-line voltage v_{AB} is contains nine voltage levels. The triplen harmonics in v_{AN} do not appear in v_{AB} due to the three-phase balanced system, resulting in a reduction of THD. The waveform of v_{AN} is shown in Fig. 3.7 composed of five voltage levels up to $m_a = 0.66$, waveform change from three level to seven level at $m_a = 0.67$ whose

harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 23rd.

The harmonic content of v_{AB} versus modulation index m_a is shown in Fig. 3.8. Since the high-order harmonic components can be easily attenuated by filters or load inductances, only the dominant harmonics centered around $2m_f$ are plotted. The n^{th} order harmonic voltage V_{ABn} (rms) is normalized with respect to the dc voltage V_d . The maximum fundamental-frequency voltage at $m_a = 1$ is given by $V_{AB1,\text{max}} = 1.224V_d$, which is two times that of the three-level NPC inverter.

Fig. 3.7 Waveform and spectrum of inverter Phase and line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 300\text{Hz}, m_f = 15 \text{ and } m_a = 0.9).$$

The curve total harmonic distortion (THD) versus modulation index (m_a) is shown in Fig. 3.9. It is worth mentioning that v_{AN} is composed of three, five and seven levels for $0 < m_a < 0.33$, $0.33 < m_a < 0.66$ and $0.66 < m_a < 1.0$ respectively.

Fig. 3.8 Harmonic contents of seven-level NPC/H-bridge inverter ($m_f=15$).

Fig. 3.9 THD and m_a of Seven Level NPC/H-bridge inverter ($m_f=15$).

3.5 Waveforms and Harmonic Content with variable frequency modulation index (m_f)

Fig. 3.10 shows waveform and spectrum of inverter phase and line-to-line voltage of the seven-level NPC/H-bridge inverter when $f_m = 60\text{Hz}$, $m_f = 18$ and $m_a = 0.9$ the device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 3 = 360\text{Hz}$. Fig. 3.11 shows waveform and spectrum of inverter Phase and line voltage of the seven-level NPC/H-bridge inverter when $f_m = 60\text{Hz}$, $m_f = 21$ and $m_a = 0.9$ the device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 3 = 420\text{Hz}$.

Fig. 3.10 Waveform and spectrum of inverter phase and line voltage

($f_m = 60\text{Hz}$, $f_{sw,dev} = 360\text{Hz}$, $m_f = 18$ and $m_a = 0.9$).

The waveform of v_{AN} is composed of seven voltage levels, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN}

does not contain any harmonics with the order lower than the 23rd, but has triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$. The triplen harmonics in v_{AN} do not appear in v_{AB} due to the three-phase balanced system,

Fig. 3.11 Waveform and spectrum of inverter phase and line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 360\text{Hz}, m_f = 21 \text{ and } m_a = 0.9).$$

To summarize the operation of the seven-level NPC/H-bridge inverter at fixed amplitude modulation index (m_a) with variable frequency modulation index (m_f) harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. When $m_f = 18$, harmonics are centered around 36th and 72nd and phase voltage v_{AN} does not contain any harmonics with the order lower than the 27th is shown in Fig. 3.10. When $m_f = 21$, harmonics with lower order than the 33rd is illustrated at Fig. 3.11. At higher frequency modulation index (m_f) like $m_f = 24$ the waveform has same characteristics with sideband harmonics and harmonic with lower order also higher. The phase voltage

contains triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$ but line-to-line voltage do not appear triplen harmonics due to the three-phase balanced system.

3.6 Other Modulation Scheme

The seven-level NPC/H-bridge Inverter produce same output characteristics both modulation scheme in-phase disposition (IPD) and alternative phase opposition disposition (APOD). Simulated waveform of the seven-level NPC/H-bridge inverter using APOD modulation scheme illustrates in Fig. 3.12. The inverter operates under the condition of $f_m = 60\text{Hz}$, $m_a = 0.9$ and $m_f = 24$. The device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 3 = 480\text{Hz}$. The line-to-line voltage waveform V_{AB} and its harmonic spectrum are identical with IPD modulation scheme explained in chapter 2.

Fig. 3.12 Waveform and spectrum of inverter line to line voltage at APOD modulation scheme ($f_m = 60\text{Hz}$, $f_{sw,dev} = 450\text{Hz}$, $m_f = 15$ and $m_a = 0.8$).

3.7 Nine level Neutral Point Clamped/H-bridge Inverter

Each leg of the nine-level NPC H-bridge inverter is composed of eight active switches, three dc capacitor and a number of clamping diodes per phase. In this inverter voltage across each capacitor is E and the total dc voltage V_d is equally shared by the capacitor that's means $V_d = E + E + E + E = 4E$.

Fig. 3.13 The nine-level inverter one leg of phase A.

One leg of phase circuit diagram of the nine-level inverter is illustrated in Fig. 3.13 and relationship between the switch status and V_{AN} for nine level inverter is given Table 3.1. With various combination of switch operating status, the waveform of V_{AN} contains five voltage levels: $4E, 3E, 2E, E$ and 0 .

Table 3.1 Switch status and inverter terminal voltage V_{AN} .

Five-level Inverter								V_{AN}
S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4	
1	1	1	1	0	0	0	0	$4E$
0	1	1	1	1	0	0	0	$3E$
0	0	1	1	1	1	0	0	$2E$
0	0	0	1	1	1	1	0	E
0	0	0	0	1	1	1	1	0

3.7 Summary

This chapter introduces a modified in-phase disposition sinusoidal pulse width modulation (SPWM-IPD) technique for the seven-level Neutral Point Clamped (NPC)/H-bridge inverter. The operating principle of this inverter is explained and modulation schemes are discussed. Simulations are carried out in variable amplitude modulation index (m_a) and variable frequency modulation index (m_f). The inverter phase voltage V_{AN} has lower THD than the five-level NPC/H-bridge inverter. The output voltage waveforms and harmonic spectrum of the seven-level NPC/H-bridge inverter are identical in alternative phase opposition disposition (APOD) modulation scheme. The SPWM-IPD modulation technique features low total harmonic distortion, simple modulation scheme and easy to implement. The above mentioned features of the seven-level NPC/H-bridge inverter have promoted its application in the MV drives.

CHAPTER 4 EXPERIMENTS

A prototype converter system is used to verify the performance of the proposed sinusoidal pulse width modified in-phase disposition (IPD) modulation scheme for the five-level NPC/H-bridge inverter. This chapter introduces the experimental setup, including the system block diagrams, simulink/RTI model for controller of the five-level NPC/H-bridge inverter and its modulation scheme. The experimental results of the harmonic contents of the output voltages are discussed in association with the theoretical expectation of Chapter 2.

The SPWM modified IPD modulation scheme switching sequences are implemented via dSpace rapid control prototyping system. The experimental output voltage waveforms and the spectra are compared to the simulation results. The principle of the proposed modulation scheme and performance of the five-level NPC/H-bridge is confirmed by the experimental results.

4.1 Experiment Setup

a. System Configuration

The three-phase utility power is connected to the two 18-pulse phase shifted transformers (PST) through the pre-charging circuit and regulated voltage supply, which are used to limit the inrush current and low voltage supply at the startup. Six 3-phase diode rectifiers are powered by two 18-pulse PSTs and their DC outputs are connected according to the in Fig. 4.1.

Fig. 4.1 System block diagram of the experimental setup.

The control of the inverter is based on dSpace hardware-in-the-loop simulation environment, which allows easy prototyping of controllers with the Simulink/RTI and downloading of these controllers to dedicated Digital Signal Processor (DSP) based systems for implementation. The dSpace main board DS1103 is embedded within the host PC, on which the Simulink/RTI environment is running. Digital I/O bits IO_0 to IO_{11} are used for the gating signals for the top and bottom switches of the NPC arms. These signals are shifted from TTL level to CMOS level by the interface board. Complementary gating signals for the middle switches are generated by the interface board. All these signals are buffered and sent to the gating boards.

The gating signals are reshaped, amplified, isolated and passed to the 12-IGBT modules by 12 gating boards. Semikron SKHI 22B hybrid dual IGBT driver modules are used. The blank-off time is set to $4.3\mu s$ and the short-pulse suppress is $500ns$. The gating

boards also generate error signals in the case of short-circuit, low supply voltage or all-high gating signals. The error signal is passed to the controller running in DS1103 via INT₀, provoking service subroutine for fault processing. If an error occurs, all the gating signals at IO₀ to IO₁₁ will be cleared and a FORBIDDEN signal is sent to the interface board via IO₁₂, which is then used to block all the complementary gating signals. As a result all the IGBTs will be switched off.

Fig. 4.2 Photo of the experiment setup.

The picture of the experiment setup is illustrated in Fig. 4.2. The converter cabinet stands at the middle. It holds the fuses, rectifiers, DC link capacitors, inverters, interface board, gating board, heat sink and so on. The computer equipped with dSpace main board DS1103 is located in right of the cabinet. It is connected to the interface board through

I/O box CP1103. To the right of the cabinet are the two 18-pulse PSTs, which power the dual 18-pulse rectifier.

b. Simulink/RTI Model for the Controller

The Simulink/RTI model for the implementation of the sinusoidal pulse width modulation (SPWM) scheme is illustrated in Fig. 4.3. There are main three subsystems they are pulse generator (SPWM-IPD modulation), gettings to the inverter, error detect. The pulse generator subsystem implements the sinusoidal pulse-width in-phase disposition modulation. The second subsystem assigns the gating signals to the dSpace I/O ports. The third subsystem is safety while the error happened the interrupt service subroutine for INT. Execution of the 'Error detect' will set the error flag 'FORBID', which is read by the 'Output' subsystem to clear IO0 to IO11 and set IO12 to high. IO12 is then used by the interface board to block all the complementary gating signals. As a result, all gating signals are cancelled.

Fig. 4.3 Block diagram of Simulink/RTI model of the inverter controller.

4.2 Experiment Results

a. Fundamental output voltage verses m_a

The Performance of the five-level NPC/H-bridge inverter with sinusoidal pulse width in-phase disposition modulation schemes is compared at different amplitude modulation index (m_a) and frequency modulation index (m_f). The output line-to-line voltage and phase voltage and their spectra are recorded. The experimented waveform for the phase voltage v_{AN} of the five-level NPC/H-bridge inverter and its harmonic content are illustrated in Fig. 4.4. The inverter operates under the condition of $f_m = 60\text{Hz}$, $m_f = 15$ and $m_a = 0.8$. The device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 2 = 450\text{Hz}$. The waveform of v_{AN} is composed of five voltage levels,

Fig. 4.4 Waveform and spectrum of the inverter phase voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 450\text{Hz}, m_f = 15 \text{ and } m_a = 0.8).$$

whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 27th, but has triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$.

The experimented waveform for the inverter line-to-line voltage v_{AB} is illustrated in Fig. 4.5. It contains nine voltage levels. The triplen harmonics in v_{AN} do not appear in v_{AB} due to the three-phase balanced system.

Fig. 4.5 Waveform and spectrum of inverter line to line voltage

$$(f_m = 60\text{Hz}, f_{sw,dev} = 450\text{Hz}, m_f = 15 \text{ and } m_a = 0.8).$$

Table 4.1 illustrated input voltage and output fundamental voltage with amplitude modulation index m_a . The three-phase power is supplied to the two 18-pulse phase shifted transformers (PST) through regulated voltage supply, which are used for low voltage supply $V_{ab}=20\text{VAC}$, $V_d=24\text{VDC}$. The fundamental output voltage changes with m_a .

Table 4.1 Input and output voltage of The five-level NPC/H-bridge Inverter

m_a	V_{ab}	V_{AB1}	V_d	V_{AB1}/V_d
0.1	20V	2.88V	24V	0.120
0.2	20V	5.80V	24V	0.241
0.3	20V	8.76V	24V	0.365
0.4	20V	11.72V	24V	0.488
0.5	20V	14.64V	24V	0.610
0.6	20V	17.59V	24V	0.734
0.7	20V	20.52V	24V	0.855
0.8	20V	23.28V	24V	0.970
0.9	20V	26.37V	24V	1.090
1.0	20V	29.37V	24V	1.224

The fundamental frequency component of v_{AB} versus modulation index m_a is illustrated in Fig. 4.6. The maximum fundamental-frequency voltage at $m_a=1$ is given by $V_{AB1,max} = 1.224V_d$, which is two times that of the three-level NPC inverter. Output phase and line-to-line voltage and voltage and harmonic spectrum are identical which discussed in chapter 2.

Fig. 4.6 Fundamental frequency component of the five-level NPC/H-bridge inverter ($f_m = 60\text{Hz}$, $m_f = 15$).

b. Output Voltage of the Inverter

The waveforms of the five-level NPC/H-bridge inverter are compared at different amplitude modulation index (m_a) and frequency modulation index (m_f). The output line-to-line voltage, phase voltage and their spectra has recorded.

i. Waveforms and Harmonic Content with variable amplitude modulation index (m_a)

The waveforms of the five-level NPC/H-bridge inverter is compared at different amplitude modulation index (m_a) . The output line-to-line voltage, phase voltage and their spectra has recorded.

Fig. 4.7 Phase voltage and Line Voltage waveform and spectra of five level NPC/H-bridge inverter at ($f_m=60\text{Hz}$, $m_a=0.5$ and $m_f=15$).

Fig. 4.7 and Fig. 4.8 illustrates simulated and experimented waveforms of the five-level NPC/H-bridge inverter. The inverter operates under the condition of $f_m = 60\text{Hz}$, $m_f = 15$, $m_a = 0.5$ and $m_a = 0.6$, respectively. The device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 2 = 450\text{Hz}$. The waveform of v_{AN} is composed of five voltage levels, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$.

The output voltage level changes from three level to five level when amplitude modulation index (m_a) changes from $m_a = 0.5$ to 0.51. The maximum fundamental-frequency voltage at $m_a = 1$ is given by $V_{AB1,max} = 1.224V_d$, which is two times that of the three-level NPC inverter.

Fig. 4.8 Phase voltage and Line-to-line Voltage waveforms and spectra of five level NPC/H-bridge inverter at ($f_m=60\text{Hz}$, $m_a=0.8$ and $m_f=15$).

ii. Waveforms and Harmonic Content with variable frequency modulation index (m_f)

The waveforms of the five-level NPC/H-bridge inverter was compared at different frequency modulation index (m_f). The output line-to-line voltage, phase voltage and their spectra has recorded.

Fig. 4.9 Phase voltage waveform and spectra of the five-level NPC/H-bridge inverter at ($f_m=60\text{Hz}$, $m_a=0.9$ and $m_f=18$).

Fig. 4.9 illustrates simulated and experimented waveforms for the phase voltage v_{AN} of the five-level NPC/H-bridge inverter and its harmonic content. The inverter operates under the condition of $f_m=60\text{Hz}$, $m_f=18$ and $m_a=0.9$. The device switching

frequency can be found from $f_{sw,dev} = f_m \times m_f / 2 = 540\text{Hz}$. The waveform of v_{AN} is composed of five voltage levels, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 27th, but has triplen harmonics such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$.

Fig. 4.10 Line voltage waveform and spectra of the five-level NPC/H-bridge inverter at ($f_m=60\text{Hz}$, $m_a = 0.9$ and $m_f = 18$).

Simulated and experimented line-to-line voltage V_{AB} waveform and its spectra are illustrated in Fig. 4.10. It contains nine voltage levels. The triplen harmonics in does not appear in V_{AB} due to the three-phase balanced system.

Fig. 4.11 Line voltage waveform and spectra of the five-level NPC/H-bridge inverter at ($f_m = 60\text{Hz}$, $m_a = 0.9$ and $m_f = 24$).

Simulated and experimented phase voltage and line-to-line voltage of five level NPC/H-bridge inverter are illustrated in Fig. 4.11. The inverter operates under the condition of $f_m = 60\text{Hz}$, $m_f = 24$ and $m_a = 0.9$. The device switching frequency can be found from $f_{sw,dev} = f_m \times m_f / 2 = 720\text{Hz}$. The waveform of v_{AN} is composed of five voltage levels, whose harmonics appear as sidebands centered around $2m_f$ and its multiples such as $4m_f$. The phase voltage v_{AN} does not contain any harmonics with the order lower than the 43th. Line-to-line voltage V_{AB} waveform contains nine voltage levels. The triplen harmonics does not appear in V_{AB} due to the three-phase balanced system.

Output phase and line-to-line voltage and harmonic spectrum at fixed amplitude modulation index (m_a) and variable frequency modulation index (m_f). is identical which discussed in chapter 2.

4.3 Summary

This chapter presents the experimental setup and results. The overall block diagram of the system, the matlab model and its simulink/RTI controller are introduced. Experiments are carried out to investigate the sinusoidal pulse width in-phase disposition (IPD) modulation scheme for the five-level NPC/H-bridge inverter in variable amplitude modulation indexes and frequency modulation indexes. The performance of output voltage waveforms with their harmonic contents is investigated. It can be concluding that:

- 1) The voltage waveforms, voltage levels are consistence with the theoretical expectation;
- 2) The proposed sinusoidal pulse width in-phase disposition modulation scheme is one of the best modulation schemes; and
- 3) The performance of the proposed modulation scheme is verified by the experiment.

CHAPTER 5 CONCLUSIONS

The multilevel power converter topologies provide an excellent way to connecting semiconductor switches, thus enabling the processing of voltages that are higher than the device rating. The multilevel inverters improve the topology of the circuit, obtain high quality output waveforms, and in the meantime conquer many defects that the two-level inverters have.

This project is devoted to the development of a sinusoidal pulse width in-phase disposition (IPD) modulation scheme for the five- and the seven-level Neutral Point Clamped (NPC)/H-bridge inverters. The research can be divided in to two parts: the sinusoidal pulse width modulation scheme for the multilevel inverter and experimental verification, both of which involve extensive theoretical analysis and computer simulation. The main contributions of the thesis project are as follows:

- Design a sinusoidal pulse width in-phase disposition (IPD) modulation scheme for the five-level NPC/H-bridge inverter. This involves theoretical analysis of output voltage waveforms and harmonic contents. Computer simulation has been carried out using various modulation schemes with variable amplitude modulation index (m_a) and frequency modulation index (m_f).
- Verify the proposed sinusoidal pulse width (IPD) modulation scheme for the five-level NPC/H bridge inverter by experiment. The experiment has carried out on a prototype converter with dSpace rapid control systems. Comparison of output voltage waveforms and harmonic contents has performed under various converter operating conditions.

- Design a sinusoidal pulse width modulation scheme for the seven-level NPC/H-bridge inverter. This involves theoretical analysis of output voltage waveforms and harmonic contents. Computer simulation has been carried out based on various modulation schemes with variable m_a and m_f .
- Investigate SPWM modulation scheme for the seven-level NPC/H-bridge inverter to achieve better performance. This includes analysis the performance of sinusoidal pulse width modulation scheme (SPWM) in both in-phase disposition (IPD) and alternative phase opposition disposition (APOD) modulation schemes.

The performance of the proposed sinusoidal pulse width modulated IPD scheme for the five-level NPC/H-bridge inverter has been verified by experiment.

For future work, it is suggested to

- 1) further verify the seven-level NPC/H-bridge inverter by experiment; and
- 2) compare the output waveforms, harmonic contents and performance with theoretical analysis in Chapter Three.

APPENDIX

A1. Simulink Model

The simulink model of sinusoidal pulse width in-phase disposition modulation generator for phase *A* is illustrated in Fig. A1. This is main part of project. SPWM generator of phase *B* and *C* is identical but sine wave generator changes its position 120 degree leading and lagging.

Fig. A1 Simulink/RTI model of the inverter SPWM generator.

The simulink model of the five-level NPC/H-bridge inverter is illustrated in Fig. A2. In model each phase is shown as a block and simulink model of phase *A* is illustrated in Fig. A3. The block diagram of Simulink/RTI model of the inverter controller is illustrated in Fig. A4 and switching sequence of the five-level NPC/H-bridge inverter is illustrated in Table A1.

Fig. A2 Simulink/RTI model of the five-level NPC/H-bridge inverter .

Fig. A3 Simulink/RTI model of the five-level NPC/H-bridge inverter phase A.

Fig. A4 Block diagram of Simulink/RTI model of the inverter controller.

Table A1 switching sequence of the five-level NPC/H-bridge inverter.

Sequence	Switch	IO
3	SA21	IO0
4	SA24	IO1
1	SA11	IO2
2	SA14	IO3
7	SB21	IO4
8	SB24	IO5
5	SB11	IO6
6	SB14	IO7
11	SC21	IO8
12	SC24	IO9
9	SC21	IO10
10	SC14	IO11

A2. dSPACE Blocks

<p>BIT #0..7</p> <p>DS1103BIT_OUT8_G0</p>	<p>DS1103: BIT_OUT8_G0 [arif_testa/output ...]</p> <p>DS1103 Bit-Wise Digital Output</p> <p>Unit specification</p> <p>Group number: 0</p> <p>Assigned bits: 0-7</p>
<p>BIT #8..15</p> <p>DS1103BIT_OUT8_G1</p>	<p>DS1103: BIT_OUT8_G0 [arif_testa/output ...]</p> <p>DS1103 Bit-Wise Digital Output</p> <p>Unit specification</p> <p>Bits of group 0: 0-7</p> <p>Initial output</p> <p>Value (0-255): 0 decimal, 0x00 hexadecimal, 0000 0000 binary</p> <p>Termination output</p> <p>set for: 0 decimal, 0x00 hexadecimal, 0000 0000 binary</p>
<p>Bit to Integer Converter</p>	<p>Block Parameters: Bit to Integer Converter</p> <p>Bit to Integer Converter (mask) (bit)</p> <p>Map a vector of bits to a corresponding vector of integers. The first bit of the input vector is assumed to be the most significant bit (MSB). The number of bits per integer value defines how many bits are mapped to each integer.</p> <p>Parameters</p> <p>Number of bits per integer: 8</p>
<p>Selector</p>	<p>Block Parameters: Selector</p> <p>Selector</p> <p>Select or re-order the specified elements of an input vector or matrix.</p> <p>Parameters</p> <p>Input Type: Vector</p> <p>Source of element indices: Internal</p> <p>Elements: [1 4 3]</p> <p>Input port width: 4</p>

A3. Algorithms to MatLab Realtime

Configuring dSPACE Software for MATLAB 6.1.0.450 (R12.1) ...

RTI	Real-Time Interface to Simulink (RTI1103)	4.3.1p1	17-Jul-2003	okay
DSSIMULINK	dSPACE ControlDesk to Simulink Interface	1.0	30-Jan-2001	okay
MLIB/MTRACE	MATLAB-dSPACE Interface Libraries	4.4.1	10-Jun-2003	okay

dSPACE configuration okay.

TIP: You have RTI relevant MATLAB Toolboxes or Simulink Blocksets installed.

You can get information on RTI compatibility from one of the links below:

- <http://www.dspace.de/en/Support/TMWBSTbx.htm>
- <http://www.dspaceinc.com/en/Support/TMWBSTbx.htm>

Warning: Output port 1 of block 'arif_testa/output signals/voltage measure/Sum9' is not connected.
Warning: Output port 1 of block 'arif_testa/output signals/voltage measure/Sum9' is not connected.

```
*** Starting RTI build procedure with RTI 4.3.1p1 (RTI1103, 17-Jul-2003)
*** Optional User System Description File arif_testa_usr.sdf not available
*** Initializing code generation
### Starting Real-Time Workshop build procedure for model: arif_testa
### Generating code into build directory: \arif_testa_rti1103
Warning: Output port 1 of block 'arif_testa/output signals/voltage measure/Sum9' is not connected.
### Invoking Target Language Compiler on arif_testa.rtw
tlc -r \arif_testa_rti1103\arif_testa.rtw -c:\dSPACE~1.1\matlab\rti1103\tlc\rti1103.tlc -O.\arif_testa_rti1103 -l:
c:\dSPACE~1.1\matlab\rti1103\tlc -lc:\dSPACE~1.1\matlab\rti1103\tlc -ID:\MATLAB6P1\rtw\tlc -aEnforceIntegerDowncast=0 -
aExtMode=1 -aFoldNonRolledExpr=0 -aForceParamTrailComments=0 -aGenerateComments=1 -aIncHierarchyInIds=0 -
aInlineInvariantSignals=0 -aInlineParameters=0 -aLocalBlockOutputs=0 -aRTWVerbose=1 -aRollThreshold=5 -
aShowEliminatedStatements=1 -aReleaseVersion=12.1 -p10000
### Loading TMW TLC function libraries
..
### Initial pass through model to cache user defined code
.....
*** Postprocessing RTI blocks
*** Starting I/O block checking
.
*** Passed I/O block checking
### Caching model source code
.....
### Creating (RealTime) source file arif_testa.c
.
### Creating model header file arif_testa.h
### Creating model header file arif_testa_export.h
### Creating parameter file arif_testa_prm.h
### Creating registration file arif_testa_reg.h
.
### Creating data type transition file arif_testa_dt.c
### TLC code generation complete.
### Generating TLC interface API.
.....
*** Generating file arif_testa_rti.c
...
*** Generating file arif_testa_rti.mk
*** Generating Variable Description File arif_testa.trc
.....
*** Optional User Variable Description File arif_testa_usr.trc not available
*** Found User-Code File arif_testa_usr.c from 20-Apr-2007 12:20:30
*** Found User Makefile arif_testa_usr.mk from 20-Apr-2007 12:20:30
### Include Communications Blockset directories
### arif_testa.mk which is generated from c:\dSPACE~1.1\matlab\rti1103\m\rti1103.tmf is up to date
### Building arif_testa: dsmake -f arif_testa.mk WORKINGBOARD=ds1103
```

BUILDING APPLICATION (Single Timer Task Mode)

WORK DIRECTORY "D:\MATLAB6P1\WORK"
BUILD DIRECTORY "D:\MATLAB6P1\WORK\ARIF_TESTA_RTI1103"
TARGET COMPILER "C:\PPCTOO~2"

COMPILING arif_testa.c
COMPILING C:\DSPACE~1.1\MATLAB\RTI1103\C\rti_sim_engine.c

LINKING APPLICATION ...
LINKING FINISHED

LOADING APPLICATION "arif_testa.sdf" ...
[#1] ds1103 - RTI: Initializing ... (720)
[#2] ds1103 - RTI: Initialization completed (721)
[#3] ds1103 - RTI: Simulation state: RUN (700)
LOADING FINISHED

MAKE PROCESS SUCCEEDED

Successful completion of Real-Time Workshop build procedure for model: arif_testa
*** Finished RTI build procedure for model arif_testa

>> =====
Configuring dSPACE Software for MATLAB 6.1.0.450 (R12.1) ...

RTI Real-Time Interface to Simulink (RTI1103) 4.3.1p1 17-Jul-2003 okay
DSSIMULINK dSPACE ControlDesk to Simulink Interface 1.0 30-Jan-2001 okay
MLIB/MTRACE MATLAB-dSPACE Interface Libraries 4.4.1 10-Jun-2003 okay

dSPACE configuration okay.

TIP: You have RTI relevant MATLAB Toolboxes or Simulink Blocksets installed.

You can get information on RTI compatibility from one of the links below:

- <http://www.dspace.de/en/Support/TMWBSTbx.htm>
- <http://www.dspaceinc.com/en/Support/TMWBSTbx.htm>

Warning: Output port 1 of block 'arif_testa/output signals/voltage measure/Sum9' is not connected.
Warning: Output port 1 of block 'arif_testa/output signals/voltage measure/Sum9' is not connected.

*** Starting RTI build procedure with RTI 4.3.1p1 (RTI1103, 17-Jul-2003)
*** Optional User System Description File arif_testa_usr.sdf not available
*** Initializing code generation
Starting Real-Time Workshop build procedure for model: arif_testa
Generating code into build directory: \arif_testa_rti1103
Warning: Output port 1 of block 'arif_testa/output signals/voltage measure/Sum9' is not connected.
Invoking Target Language Compiler on arif_testa.rtw
tlc -r \arif_testa_rti1103\arif_testa.rtw 'c:\dspac~1.1\matlab\rti1103\tlc\rti1103.tlc' -O.\arif_testa_rti1103 '-
lc:\dspac~1.1\matlab\rti1103\tlc' -lc:\dspac~1.1\matlab\rti1103\tlc -ID:\MATLAB6P1\rtw\c\tlc' -aEnforceIntegerDowncast=0 -
aExtMode=1 -aFoldNonRolledExpr=0 -aForceParamTrailComments=0 -aGenerateComments=1 -aIncHierarchyInIds=0 -
aInlineInvariantSignals=0 -aInlineParameters=0 -aLocalBlockOutputs=0 -aRTWVerbose=1 -aRollThreshold=5 -
aShowEliminatedStatements=1 -aReleaseVersion=12.1 -p10000
Loading TMW TLC function libraries
..
Initial pass through model to cache user defined code
.....
*** Postprocessing RTI blocks
*** Starting I/O block checking
.
*** Passed I/O block checking
Caching model source code
.....
Creating (RealTime) source file arif_testa.c
.
Creating model header file arif_testa.h
Creating model header file arif_testa_export.h
Creating parameter file arif_testa_prm.h
Creating registration file arif_testa_reg.h


```

### Creating data type transition file arif_testa_dt.c
### TLC code generation complete.
### Generating TLC interface API.
.....
*** Generating file arif_testa_rti.c
...
*** Generating file arif_testa_rti.mk
*** Generating Variable Description File arif_testa.trc
.....
*** Optional User Variable Description File arif_testa_usr.trc not available
*** Found User-Code File arif_testa_usr.c from 20-Apr-2007 12:20:30
*** Found User Makefile arif_testa_usr.mk from 20-Apr-2007 12:20:30
### Include Communications Blockset directories
### arif_testa.mk which is generated from c:\dSPACE~1.1\matlab\rti1103\m\rti1103.tmf is up to date
### Building arif_testa: dsmake -f arif_testa.mk WORKINGBOARD=ds1103

```

BUILDING APPLICATION (Single Timer Task Mode)

```

WORK DIRECTORY "D:\MATLAB6P1\WORK"
BUILD DIRECTORY "D:\MATLAB6P1\WORK\ARIF_TESTA_RTII103"
TARGET COMPILER "C:\PPCTOO~2"

```

```

COMPILING arif_testa.c
COMPILING C:\DSPSPACE~1.1\MATLAB\RTII103\C\rti_sim_engine.c

```

```

LINKING APPLICATION ...
LINKING FINISHED

```

```

LOADING APPLICATION "arif_testa.sdf" ...
[#1] ds1103 - RTI: Initializing ... (720)
[#2] ds1103 - RTI: Initialization completed (721)
[#3] ds1103 - RTI: Simulation state: RUN (700)
LOADING FINISHED

```

MAKE PROCESS SUCCEEDED

```

### Successful completion of Real-Time Workshop build procedure for model: arif_testa
*** Finished RTI build procedure for model arif_testa

```

aa

Configuring dSPACE Software for MATLAB 6.1.0.450 (R12.1) ...

```

RTI      Real-Time Interface to Simulink (RTI1103)  4.3.1p1  17-Jul-2003  okay
DSSIMULINK dSPACE ControlDesk to Simulink Interface  1.0    30-Jan-2001  okay
MLIB/MTRACE MATLAB-dSPACE Interface Libraries      4.4.1   10-Jun-2003  okay

```

dSPACE configuration okay.

TIP: You have RTI relevant MATLAB Toolboxes or Simulink Blocksets installed.

You can get information on RTI compatibility from one of the links below:

- <http://www.dspace.de/en/Support/TMWBSTbx.htm>
- <http://www.dspaceinc.com/en/Support/TMWBSTbx.htm>

Warning: Output port 1 of block 'arif_testa/output signals/voltage measure/Sum9' is not connected.

```

*** Starting RTI build procedure with RTI 4.3.1p1 (RTI1103, 17-Jul-2003)
*** Optional User System Description File arif_testa_usr.sdf not available
*** Initializing code generation
### Starting Real-Time Workshop build procedure for model: arif_testa
### Generating code into build directory: .arif_testa_rti1103
Warning: Output port 1 of block 'arif_testa/output signals/voltage measure/Sum9' is not connected.

```

```

### Invoking Target Language Compiler on arif_testa.rtw
tlc -r .\arif_testa_rti1103\arif_testa.rtw 'c:\dsp\space~1.1\matlab\rti1103\tlc\rti1103.tlc' -O.\arif_testa_rti1103 '-
lc:\dsp\space~1.1\matlab\rti1103\tlc' -lc:\dsp\space~1.1\matlab\rti1103\tlc -ID:\MATLAB6P1\rtw\c\tlc' -aEnforceIntegerDowncast=0 -
aExtMode=1 -aFoldNonRolledExpr=0 -aForceParamTrailComments=0 -aGenerateComments=1 -aIncHierarchyInIds=0 -
aInlineInvariantSignals=0 -aInlineParameters=0 -aLocalBlockOutputs=0 -aRTWVerbose=1 -aRollThreshold=5 -
aShowEliminatedStatements=1 -aReleaseVersion=12.1 -p10000
### Loading TMW TLC function libraries
..
### Initial pass through model to cache user defined code
.....
*** Postprocessing RTI blocks
*** Starting I/O block checking
.
*** Passed I/O block checking
### Caching model source code
.....
### Creating (RealTime) source file arif_testa.c
.
### Creating model header file arif_testa.h
### Creating model header file arif_testa_export.h
### Creating parameter file arif_testa_prm.h
### Creating registration file arif_testa_reg.h
.
### Creating data type transition file arif_testa_dt.c
### TLC code generation complete.
### Generating TLC interface API.
.....
*** Generating file arif_testa_rti.c
...
*** Generating file arif_testa_rti.mk
*** Generating Variable Description File arif_testa.trc
.....
*** Optional User Variable Description File arif_testa_usr.trc not available
*** Found User-Code File arif_testa_usr.c from 20-Apr-2007 12:20:30
*** Found User Makefile arif_testa_usr.mk from 20-Apr-2007 12:20:30
### Include Communications Blockset directories
### arif_testa.mk which is generated from c:\dsp\space~1.1\matlab\rti1103\m\rti1103.tmf is up to date
### Building arif_testa: dsmake -f arif_testa.mk WORKINGBOARD=ds1103

BUILDING APPLICATION (Single Timer Task Mode)

WORK DIRECTORY "D:\MATLAB6P1\WORK"
BUILD DIRECTORY "D:\MATLAB6P1\WORK\ARIF_TESTA_RTI1103"
TARGET COMPILER "C:\PPCTOO~2"

COMPILING arif_testa.c
COMPILING C:\DSP\SPACE~1.1\MATLAB\RTI1103\C\rti_sim_engine.c

LINKING APPLICATION ...
LINKING FINISHED

LOADING APPLICATION "arif_testa.sdf" ...
[#1] ds1103 - RTI:   Initializing ... (720)
[#2] ds1103 - RTI:   Initialization completed (721)
[#3] ds1103 - RTI:   Simulation state: RUN (700)
LOADING FINISHED

MAKE PROCESS SUCCEEDED

### Successful completion of Real-Time Workshop build procedure for model: arif_testa
*** Finished RTI build procedure for model arif_testa
>>

```

A4. Output Voltage of the Inverter

The waveforms of the five-level NPC/H-bridge inverter is compared at different amplitude modulation index (m_a) and frequency modulation index (m_f). The output line-to-line voltage V_{AB} and phase voltage V_{AN} and their spectra have recorded.

Fig. A5 Phase voltage waveform and spectra of the five-level NPC/H-bridge inverter at $m_a=0.2$ and $m_f=15$.

Fig. A6 Line-to-line voltage waveform and spectra of the five- level NPC/H-bridge inverter at $m_a=0.2$ and $m_f=15$.

Fig. A7 Phase voltage and line-to-line voltage waveform and spectra of the five-level NPC/H-bridge inverter at $m_a=0.6$ and $m_f=15$

Fig. A8 Phase voltage and line-to-line voltage waveform and spectra of the five-level NPC/H-bridge inverter at $m_a = 1.0$ and $m_f = 15$

Fig. A9 Phase voltage and line-to-line voltage waveform and spectra of the five-level NPC/H-bridge inverter at $m_a = 0.9$ and $m_f = 21$

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