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Reliability of soldered joints for aerospace applications

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RELIABILITY OF SOLDERED JOINTS FOR AEROSPACE APPLICATIONS

by

Brigitte Desrochers, B. Eng, Carleton University, 2002

A project
presented to Ryerson University
in partial fulfillment of the
requirements for the degree of
Masters of Engineering
in the Program of
Mechanical Engineering

Toronto, Ontario, Canada

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ABSTRACT

Known to be highly reliable, Tin-Lead (SnPb) solders have long been used in commercial and aerospace electronic assemblies due to their ability to withstand thermo-mechanical fatigue. A number of constitutive and thermo-mechanical life models for SnPb soldered joints can be used to determine whether a given board design meets the reliability requirements of a system.

Due to environmental and toxicological concerns, government legislations worldwide now limit the use of Pb in manufacturing processes. Therefore, the aerospace industry must understand the reliability of proposed Pb-free alternatives prior to using them in the aerospace applications. In order to improve the space-readiness of Pb-free solders, a well-rounded collection of space-specific test results must be compiled and test-verified predictive life models must be developed. Finally, quality control processes associated with manufacturing, handling, and repairing Pb-free solders will have to be created before the space industry can make the transition from SnPb to Pb-free solders.

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1 Introduction

In order to ensure a reliable electronic device, it is important to understand the reliability of its soldered joints, which provide electrical and mechanical connections between electronic components and the underlying board. As a result, high reliability applications, such as in the aerospace industry, require that all aspects of the design and manufacture of soldered joints be well understood and tightly controlled. An abundance of literature pertaining to the general reliability of soldered joints exists, but the unique requirements of the aerospace industry have not been thoroughly addressed.

The purpose of this report is to provide electrical engineers and electronics board designers in the aerospace industry with some general design guidelines for optimizing the mechanical aspects of the board design in order to improve device reliability, while also providing mechanical/structural engineers with analytical solutions for evaluating the thermo-mechanical fatigue life of electronic packages. As a result, the body of this report is structured into three main sections. The first section provides an in-depth review of the most critical factor affecting the reliability of soldered joints: thermo-mechanical fatigue. The second section provides a general overview of the design and manufacturing parameters to be considered when optimizing a board for a long fatigue life. Finally, the third section discusses the emergence of lead-free (Pb-free) solder and evaluates the feasibility of transitioning from the traditional lead-tin (Pb-Sn) to Pb-free solders in the aerospace industry.

1.1 Soldering basics

1.1.1 Types of soldered joints

Soldered joints can be divided into two categories: Type I and Type II packaging. In Type I packaging, solder is used to bond a die, otherwise known as a silicon chip, to an appropriate substrate, the bonding pad. In Type II packaging, the solder is used to mount individual components onto a printed circuit board (PCB).

1.1.1.1 Flip chip connection

The flip chip connection, shown in Figure 1, is the typical soldering application in Type I packaging. Solder bumps are used instead of wire connections to bond a flipped silicon chip onto the substrate. The use of solder bumps allows for a greater number of input/output ports to the substrate than the traditional wire connections. A typical solder ball in a flip chip connection will have dimensions in the order of 100 μm in diameter.

Figure 1: Flip chip connection, cross-section [2]

1.1.1.2 Ball grid array connection

The Ball Grid Array (BGA connection) is similar to the flip chip connection in that it consists of an array interconnection scheme. However, the BGA method is an example of Type II packaging whereby a plastic or ceramic chip is mounted to a printed circuit board. A typical solder ball in a BGA will have dimensions in the order of 600 to 900 μm in diameter.

1.1.1.3 Pin through hole connection

The pin through hole connection (PTH), shown in Figure 2, is another method of Type II packaging. The leads of individual components are inserted into holes through the PCB substrate. The solder creates a joint within the holes in the PCB substrate.

Figure 2: Pin through hole (PTH) connection, cross-section [2]

1.1.1.4 Surface mount connection

Surface mount technology (SMT) is a third method of Type II packaging. The individual components are bonded to leads on the surface of the PCB substrate through a solder joint.

Figure 3: Surface mount connection, cross section [2]

1.1.2 Soldering processes

Three commonly used soldering processes exist for creating soldered joints: hand soldering, wave soldering and reflow soldering.

1.1.2.1 Hand soldering

Hand soldering is the method of choice for the amateur electronics assemblers by which a soldering iron is used to melt the tip of a solder alloy onto the desired joining location. In commercial and aerospace applications, the hand soldering technique is used mainly as a circuit board repair method as it is not a sufficiently efficient process to be considered for high-volume production of commercial PCBs. Another disadvantage of hand soldering is the lack of process control parameters. The temperature of the soldering iron is not normally monitored and high precision placement of the solidified joint is difficult to achieve.

1.1.2.2 Wave soldering

Wave soldering, shown in Figure 4, is the process by which the assembled PCBs are transported by conveyor belt over a bath of molten solder. The liquid solder is then pumped out of the bath and forced into the holes of the PCBs, through the bottom of the substrate, to create PTH connections. Consequently, component mounting locations must be limited to one side of the PCB substrate. Wave soldering is a cost-effective process

that allows for high volume production of PCB assemblies and generally results in high-yield production runs.

Figure 4: Wave soldering process [2]

1.1.2.3 Reflow soldering

Reflow soldering is the principal soldering technique used to manufacture SMT circuit boards. A solder paste is deposited onto the PCB leads where a solder joint is desired. The PCBs, with the solder paste spheres deposited on the leads and the surface mounted components in place, are then placed in a reflow oven to melt the solder paste. The liquid solder completely wets the PCB lead and coats the surface mounted component lead wire. Upon cooling and solidification of the liquid solder, a reliable joint is created. Reflow soldering allows for individual electronic components to be mounted on both sides of the PCB substrate. Although less cost effective than the wave soldering process, the reflow soldering process monopolizes less floor space within the manufacturer's facilities and also produces consistently robust joints.

1.1.3 Solder Compositions

In order to discuss the reliability of soldered joints, it is important to first understand the basic compositions of solder alloys. The selection of a solder material is dependent upon a few unique characteristics. First of all, a low melting temperature is desired in order to avoid damaging delicate electronics by exposing them to excessively high temperatures during the manufacturing process. Secondly, a strong conductive path (low resistance) is

desired through the soldered joint. Finally, good mechanical reliability is desired in each soldered joint.

Tin (Sn) is used as the primary alloying in almost all solders. Sn is an ideal candidate for soldering applications due to its low elemental melting temperature of 231°C, and ability to wet many types of substrates with the help of fluxes. In order to design an optimum soldering material, Sn is alloyed with a number of different elements to optimize its electrical and mechanical properties.

Until recently, lead (Pb) alloyed with Sn has been used extensively as solder in the microelectronics industry. By far, the most common of all Pb-containing solders are the eutectic composition, 63Sn-37Pb and the near-eutectic composition, 60Sn-40Pb. Solders with high lead content such as 90Pb-10Sn are sometimes used for ceramic BGAs (CBGAs).

However, due to the environmental and toxicological concerns created by the use of Pb as the alloying metal with Sn, government legislation and regulations have been recently put in place to limit or eliminate the use of lead in manufacturing processes, as further discussed in section 1.2. As such, electronics manufacturers have been developing new Pb-free solder compositions. Several promising candidates have been identified to date, with the focus lying primarily on near-ternary eutectic Sn-Silver (Ag)-Copper (Cu) compositions, also known as SAC systems.

The compositions and associated melting points of a few lead-containing and lead-free solders is shown in Table 1 [9].

Table 1: Compositions of common lead-containing and lead-free solders

Composition (wt %)	Melting Point (°C)	Application
63Sn-37Pb	183	PTH, SMT, BGA
97Pb-3Sn	317	Flip-chip, BGA
Sn-3.5Ag	221	SMT, flip-chip
Sn-3.8Ag-0.7Cu	217	SMT, PTH, BGA
Sn-3.5Ag-3Bi	208-215	SMT
Sn-0.7Cu	227	PTH, flip-chip

1.2 RoHS Directive

1.2.1 Europe

A restriction of the use of certain hazardous substances in electrical and electronic equipment, the RoHS Directive (2002/95/EC), was implemented by the European Union (EU) Environment Commission in July 2006. By implementing the RoHS Directive, the EU restricts excessive use of heavy metals (lead, cadmium, mercury, and hexavalent chromium) as well as two types of flame retardants (polybrominated biphenyl (PBB) and polybrominated diphenyl ether (PBDE)) in electrical and electronic equipment. The RoHS Directive was drafted by the EU as a measure to meet the goals in reduction of e-waste set out in another EU directive, the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC).

Although the RoHS directive itself is not a law, the individual European states comprising the EU create laws and regulations enforcing the guidelines set forth in the directive. As a result, each European state must ensure that the intentions of the RoHS Directive are met.

1.2.2 Japan

Although Japan does not directly enforce the RoHS directive (or similar legislation), the Japanese government has taken the more generic approach of enforcing strict standards on Recycling, Re-using and Reducing waste (otherwise known as the three R's), as mandated by the Law for Promotion of Effective Utilization of Resources. A recent

amendment to the judgement criteria for Law for Promotion of Effective Utilization of Resources (JIS C 0950, effective July 2006) requires that all Japanese manufacturers and importers of computers, televisions, refrigerators, washers and dryers, microwaves, and air conditioners label their products to indicate presence of the six RoHS substances. This amendment, known as J-MOSS, results in reluctance on the behalf of Japanese consumers to purchase products containing the six RoHS substances, which do not meet the regulations outlined in the Law for Promotion of Effective Utilization of Resources.

1.2.3 China

Following an approach similar the one taken by Japan, China has created a law entitled Administration on the Control of Pollution Caused by Electronic Information Products. This law, in effect as of March 2007, requires that products containing excessive levels of the six RoHS substances be appropriately labelled in order to disclose the quantities of hazardous substances to the public. Although the current law is quite vague and does not restrict the use of the six RoHS substances, a future amendment to the law is planned to include a catalogue of substance restrictions and certification requirements.

1.2.4 Korea

Korea is the latest country to draft government regulations similar to the EU's RoHS. The law, entitled Act for Resource Recycling of Electrical and Electronic Equipment and Vehicles, has a compliance date set for January 2008. Although it does not enforce specific labelling requirements, the law will provide a list of restricted substances (including the six RoHS substances) and requires that all applicable products be registered with the government to verify compliance with the legislation.

1.2.5 North America

There are currently no federal regulations imposed by the United States, Canada or Mexico to limit or restrict the use of the six RoHS substances for the purpose of environmental protection. However, the state of California has drafted two senate bills, Electronic Waste Recycling Act (SB 20) and the corresponding Emergency Amendment to SB 20 (SB 50), which contain provisions for both RoHS and WEEE. The RoHS provisions came into effect in January 2007, and restrict the use of the four heavy metals

identified in the RoHS directive but allow the use of the two flame retardants (PBB and PBDE). The California senate bills require that manufacturers of applicable electronic devices file annual reports detailing:

- the number of covered electronic devices sold in California,
- the total amount of hazardous substances contained in the devices,
- the manufacturer's reduction in use of hazardous materials and increase in use of recyclable materials from the year before, and
- all efforts to design more environmentally friendly products

1.2.6 RoHS Consequences

The obvious end benefit of all variations of the RoHS directive is a reduction the amount of hazardous waste due to the disposal of electrical and electronic equipment. In response to the various RoHS-like legislations, manufacturers of electrical electronic equipment strive to create products that meet the smallest common denominator of acceptability with respect the applicable laws of their international customers. This has resulted in a recent focus on the development of Pb-free electrical and electronic assemblies, including the material used to solder components to the underlying board. While the long-term reliability of Pb-containing solders is well understood, the emergence of Pb-free solders is relatively new and the effects of long-term reliability have not yet been fully experienced.

1.3 Reliability requirements in the aerospace industry

1.3.1 Definition

In general terms, reliability can be defined as the ability of an item to perform a required function under stated conditions for a specified period of time [10]. In the context of reliability engineering, the reliability of an item or system is quantitatively captured as the probability that it will perform its function without failure, over a specified period of time, under stated conditions. Both definitions address the three aspects of reliability:

1. Performing a function without failure

2. Specified period of time

3. Stated conditions

1.3.2 Requirement Development

In the aerospace industry, specific reliability requirements are developed at the system requirements definition stage of a program. The required reliability level developed will be dependant upon the three aspects of reliability listed above. Specifically, the required level of reliability will increase with increasing function criticality, duration of the mission, and severity of environmental conditions. Aerospace applications impose unique constraints on system developers due to:

- The inability to replace or perform maintenance on failed components once on-orbit (with the exception of replaceable modules called On-orbit Replaceable Units (ORUs))
- Extreme environmental conditions (wide range in operational temperatures, severe vibration environment during launch, etc.)
- Sometimes lengthy mission durations

Such design constraints inevitably result in high reliability requirements for aerospace applications. Since high reliability requirements can also drive the overall cost of a program (through the introduction of redundancy, testing, etc.), it is important to balance the required reliability level with the cost constraints of the program.

1.3.3 IPC Reliability Guidelines

When specific program requirements for reliability have not been developed, designers may refer to the reliability levels recommended by the Institute for Interconnecting and Packaging Electronic Circuits (IPC). The design guideline IPC-D-279 recommends an acceptable failure probability of $\sim 0.001\%$ for space applications given average use environments and a typical service life of 10 years [19]. A failure probability of 0.001% translates into a reliability level of 99.999% for space applications.

2 Thermo-Mechanical Fatigue of Soldered Joints

2.1 Thermal Fatigue Damage Mechanism

2.1.1 Solder Microstructure

A typical solder joint is an inhomogeneous structure, consisting of a number of different materials. A solder joint consists of:

1. The base metal at the printed wiring board (PWB)
2. One or more intermetallic compounds (IMCs) – solid solutions of a solder constituent (typically tin (Sn)) with the PWB base metal
3. A layer from which the solder constituent forming the PWB side IMCs has been depleted
4. The solder grain structure, consisting of at least two phases containing different proportions of the solder constituents as well as any deliberate or inadvertent contaminations
5. A layer from which the solder constituent forming the component side IMCs has been depleted
6. One or more IMC layers of a solder constituent with the component base metal
7. The base metal at the component

A sample Scanning Electron Microscopy (SEM) photograph of the IMC layers formed at the interface of a lead-free solder and copper substrate is shown in the following figure.

Figure 5: IMC layers at the solder to substrate interface [3]

2.1.2 Damage Accumulation

The grain structure of solder materials is inherently unstable. In order to reduce the internal energy of a fine-grained structure, the grains will grow in size over time. Elevated temperatures as well as strain energy input during cyclic mechanical loading accelerate such grain growth. Hence, the amount of grain growth in the solder metallurgical structure can be used as an indication of accumulated fatigue damage. Furthermore, contaminants will tend to coalesce at the grain boundaries. Defects and irregularities in the microstructure typically serve as crack initiation sites. As the grains grow, the concentration of contaminants will increase, thus weakening the boundaries. As the grain boundaries weaken, micro voids begin to form (after ~25% of fatigue life is consumed), leading to micro-cracks (after ~40% of fatigue life) and, eventually, macro-cracks causing failure (100% of fatigue life). The accumulation of fatigue damage in the bulk material of a soldered joint is depicted in Figure 6.

Figure 6: Depiction of the effects of accumulating fatigue damage in solder joint structure [4]

More specifically, fatigue damage in a soldered joint tends to initiate close to the upper and lower boundaries and at the center of the bump. Often, the material properties of IMC layers between the solder bump and the component as well as between the solder bump and the substrate differ from those of the bulk material. As such, stress concentrations occur at the grain boundaries between the IMC layers and the bulk material, further encouraging the initiation of micro voids. Later on, damage propagates throughout the entire bump leading to complete failure, as depicted in Figure 7.

Figure 7: Damage distribution in a solder joint at increasing number cycles [5]

The following figure shows a eutectic Pb-Sn solder bump that fractured along the joint between the solder and the substrate following fatigue testing. Soldered joints will consistently fracture along the brittle interface between the bulk material and the IMC layer, where damage accumulation is the most severe, after exposure to thermal and/or mechanical fatigue.

Figure 8: Fatigue fracture of a eutectic Pb-Sn solder bump [9]

In a filleted soldered joint (for leadless components), there are typically two areas of crack growth to consider: cracking through the thin layer of solder between the leadless component and board (parallel to the component), and cracking through the solder fillet (at approximately 45° through the fillet).

Figure 9: Fatigue fracture of a SnAgCu fillet solder joint [12]

As damage progresses in the solder bump, the overall stiffness decreases and the load required to achieve an equivalent strain level decreases. Therefore, smaller load levels will cause greater damage as damage accumulates in the soldered joint. Initially, slow softening of the joint occurs while rapid softening of the joint is observed as failure is approached.

2.1.3 Thermal Cycling Induced Damage

2.1.3.1 Creep

Creep can be defined as a measure of time required for a material to fail when it is under a constant load at an elevated temperature [7]. Generally, creep becomes a critical material parameter when the in-service temperature exceeds half of the absolute melting temperature (in degree Kelvin). Since the melting temperatures of soldering alloys are generally low, their average in-service temperature is consequently at or above half of the melting temperature (note: $183^{\circ}\text{C} = 456^{\circ}\text{K}$; $228^{\circ}\text{K} = -45^{\circ}\text{C}$). As such, when an electronic component is exposed to low-cycle thermal fatigue, creep is likely to occur in the soldered joint. Creep is therefore the dominant mechanism through which plastic deformation occurs in a soldered joint.

The microstructure of the bulk material in Pb-Sn soldered joints consists of equiaxed grains of Pb-rich and Sn-rich phases, both of which will coarsen upon exposure to low cycle thermal fatigue. The creep profile of Pb-Sn soldered joints is therefore dominated by the diffusional creep mechanism, where atoms diffuse through and around grain boundaries when a material is under stress.

The microstructure of the bulk material in a Pb-free soldered joint includes small IMC particles typically dispersed within the tin matrix. As the Pb-free joint is exposed to low cycle thermal fatigue, the IMC particles coalesce, offering increased resistance to the occurrence of dislocation creep. The creep profile of Pb-free soldered joints is therefore dominated by the dislocation creep mechanism, where dislocations climb through the material matrix and their movement is opposed by obstacles such as grain boundaries, solutes, and other dislocations.

A typical creep curve is comprised of three areas, after the initial time-independent stress-strain response (both elastic and plastic):

1. Primary creep, where the strain rate decreases as the material strain-hardens,
2. Secondary creep, where deformations continue to increase at a steady strain rate, and

3. Tertiary creep, where the strain rate rapidly increases until rupture.

Figure 10: Typical creep curve of a soldered joint [8]

2.1.3.1.1 General Secondary Creep Rate

The creep behaviour of near-eutectic Sn-Pb solders has been studied by many researchers, focussing mainly on the steady-state portion of the creep curve (secondary creep), as it is the most influential portion of the creep curve on the solder's fatigue life.

The secondary creep rate can be expressed by Dorn's equation [13]:

$$\dot{\epsilon}_{ss} = A \left(\frac{b}{g} \right)^p \frac{E(T)}{kT} \left(\frac{\sigma}{E(T)} \right)^n \exp \left(-\frac{Q}{kT} \right) \quad (1)$$

Where: $\dot{\epsilon}_{ss}$ is the secondary creep rate

A is a material constant

b is the magnitude of the material Burgers vector

g is the material's grain size

T is the temperature

E(T) is the temperature-dependant Young's modulus

k is Boltzmann's constant

σ is the stress magnitude

Q is the activation energy of the rate controlling diffusion mechanism

p and n are constant exponents

As can be deduced from equation (1) above, the steady-state creep rate generally has a strong dependence on stress, temperature, and grain size.

2.1.3.1.2 Effects on Solder Creep Curves

Two factors that influence the creep rates of soldered joints are material composition and the geometry of the joint.

As mentioned above, the creep mechanisms for Sn-Pb and Pb-free solders are different. Consequently, their creep rates differ as well. Villain *et al* have plotted master creep curves at high homologous temperatures for both near eutectic Sn-60Pb-40 solder and Sn-96Ag-3.5 solder, as shown in Figure 11 and Figure 12, respectively. Ignoring the effects of instantaneous time-independent strains, the results show that the lead-free solder exhibits a much lower creep rate than the near eutectic Sn-Pb solder.

Villain *et al* further demonstrated the effect of joint geometry on the creep rate of soldered joints. As shown in Figure 13, specimens with smaller joint volumes will tend to exhibit larger creep rates at high temperatures.

Figure 11: Master creep curve for Sn60Pb40 [11]

Figure 12: Master creep curve for Sn96.5Ag3.5 [11]

Figure 13: Comparison of creep behaviour of small and large specimens (stress 5 N/mm²; T=22°C) [11]

2.1.3.2 Thermo-Mechanically Induced Loads

The following figure shows an idealized representation of a solder joint, joining a leadless component to a substrate, with the forces and moments acting on it due to mismatched coefficients of thermal expansion. Assuming that the Coefficient of Thermal Expansion (CTE) of the component (above) is smaller than that of the substrate (below), the component expands less than the substrate when exposed to high temperatures. The substrate pad will thus move further to the right than the component, causing both shear and bending loads on the solder joint.

Figure 14: Resultant loads on a solder joint due to mismatched coefficients of thermal expansion

Both global and local CTE mismatches can induce thermo-mechanically applied loads into a soldered joint. A global CTE mismatch occurs when the CTE of the component differs from that of the substrate. As a result, the relative displacement between the component and the substrate, under a change in temperature, is accommodated by the assembly leads (if applicable) and the soldered joint. A local CTE mismatch occurs when the CTEs of the board /component / leads differ from that of the solder material. As a result, the soft solder material plastically deforms to accommodate the effective relative displacement between the board / component / lead system and the solder material.

2.2 Accelerated Thermo-mechanical Fatigue Testing

The ideal method for characterizing the thermo-mechanical fatigue life of an electronic package is to perform fatigue testing on the board under conditions mimicking expected operational conditions. However, due to the impractical time investment required to perform fatigue tests on multiple samples, exactly simulating expected operational conditions, it is preferable to perform accelerated fatigue testing instead. This section presents a summary of the surface mount technology specification IPC-SM-785 [14],

section 7.0, outlining general guidelines for performing accelerate fatigue testing on electronic packages.

2.2.1 Purpose

Accelerated testing is undertaken to simulate failure or accumulate damage in the soldered joint by the same mechanism, but in a shorter time frame than would normally be required during product use. This testing and the corresponding failure data helps to establish the statistical model required to implement statistical process controls in the manufacturing process. Given the accelerated nature of the testing, it is essential to understand the relationship between the test and natural operating conditions. Of particular interest is the controlling variable and how it is affected by a change in rate or range of operation with respect to expected life. Thermal fatigue, when tested in an accelerated fashion, based on real operating conditions, can establish solder joint life.

2.2.2 Functional Cycling

Functional cycling refers to the process of simulating operating conditions as closely as possible. In order to best approximate normal operating conditions, only one or two parameters should be subjected to well-controlled deviations. This strategy will facilitate test accelerations while minimizing uncontrollable influences.

2.2.2.1 Dwell Time

Decreasing dwell time is one common method used to accelerate failure. This method results in reduced fatigue per cycle, and therefore more cycles required to failure than would be expected under regular operating conditions. However, the time to failure under test conditions is significantly less than would be expected under normal operating conditions because the cycles are shorter allowing a greater number of cycles in an equivalent time frame.

2.2.2.2 CTE Mismatch

Another accelerated testing method involves increasing cyclic fatigue by introducing a greater mismatch between the component and the substrate. However, increasing the difference in thermal expansion coefficients will also introduce other, uncontrollable

damage mechanisms and different material behaviour making the results difficult if not impossible to analyze.

2.2.2.3 Temperature Range

Temperature cycling, as the name implies, is the process of subjecting the test assembly to alternating high and low temperatures for pre-determined dwell times. Typically, the rate of change in temperature should be maintained at less than 20 °C/min such that thermal shocking is avoided. Temperature ranges of +25 to +100 °C or 0 to +100 °C with 15 minute dwell times at each extreme can be used to impose creep and fatigue to the solder joints. Cold cycling (possibly -40 to 0 °C) can be used to impose fatigue damage but minimize stress relaxation and creep mechanisms.

For applications where larger temperature swings occur under normal duty conditions (under the hood of a motor vehicle), the potential damage mechanisms are many, interactive with each other and generally not well understood or documented.

2.2.3 Temperature Monitoring

It is important to measure the temperature at each testing specimen rather than simply inside the testing apparatus. The response of the specimen as well as the apparatus can vary as a function of the total test thermal load (which is a function of the number of test specimens, the thermal mass of each specimen as well as that of the testing apparatus), specimen distribution within the apparatus as well as the airflow rate through the apparatus.

2.2.4 Failure Criteria

IPC-SM-785 recommends the following failure criteria for the purpose of accelerated reliability testing. Failure of a solder joint is defined as the first interruption of electrical continuity, and subsequently confirmed by 9 additional interruptions within 10% of the predicted cyclic life.

2.2.5 Acceleration Factors

Based on the life results obtained from accelerated testing, a predicted service life can be estimated by applying the appropriate Acceleration Factor (AF). There are two types of acceleration factors to consider:

1. AF(cycles), which relates the cyclic fatigue life of the component in test to the expected cyclic fatigue life of the component in a given operational environment.
2. AF(MTTF), which relates the mean time to failure of a component in test to the expected mean time to failure of the component in a given operational environment.

Acceleration factors must be obtained by considering both empirical and computational solder joint reliability studies.

2.3 Overview of Constitutive and Reliability Models

It is generally unrealistic to perform accelerated thermo-mechanical fatigue testing of each electronic package designed for a given application. Therefore, designers can make use of existing constitutive and reliability models reported in the literature in order to predict the fatigue life of a package. However, care must be taken to ensure that the predictive models were developed for similar specimens and expected operational conditions in order to maintain their validity for a given application.

Since eutectic and near-eutectic Sn-Pb solders have been used in the design of electronic components for over 50 years, the mechanics of such joints have been widely studied. As a result, a number of constitutive models for predicting the stress-strain behaviour of Sn-Pb soldered joints have been proposed, as well as a variety of reliability models for predicting their fatigue life.

2.3.1 Constitutive Models

Although soldered joints are tiny structures, their stress-strain behaviour is quite complex and can be affected by many parameters including:

- Joint microstructure

- Joint size
- Assembly cooling rate
- In-service ageing

Although variations in test parameters have contributed to a scatter in mechanical properties reported in the literature, simplified constitutive models for predicting the mechanical behaviour of Sn-Pb soldered joints have nonetheless been developed and validated. In all cases, the mechanical property leading to complex modelling is the steady-state creep behaviour of Sn-Pb alloys, since the creep response of a soldered joint varies with the size of the specimen under test. Consequently, constitutive models developed from experimental measurements of actual soldered joint specimens can be of practical use to engineers. Three examples of solder constitutive models are reported below.

2.3.1.1 Darveaux's Model

Darveaux's constitutive model is based on extensive testing of flip-chip and BGA solder joints and predicts the time-independent plastic flow as well as the time-dependent creep strain of several solder alloys [15]. Further validations of Darveaux's model confirmed that it applies consistently to several solder alloys, over a wide range of temperatures, and for several orders of magnitude in strain rates.

The initial step in a creep test consists of an instantaneous strain (including elastic and plastic strain), representing time-independent plastic flow. The plastic strains can be captured by the following strain hardening law:

$$\gamma_p = C \left(\frac{\tau}{G(T)} \right)^m \quad (2)$$

Where:

γ_p	is plastic flow strain
C	is a material constant
m	is the material exponent

τ is the applied shear stress

$G(T)$ is the temperature-dependent shear modulus

Darveaux presents the temperature-dependant shear modulus as well as the strain hardening parameters C and m for several Sn-Pb solder alloys.

The second step in a creep test is the primary (transient) creep, whose strain is described by the following equation:

$$\gamma_C^1 = \frac{d\gamma_s}{dt}t + \gamma_T \left[1 - \exp\left(-B \frac{d\gamma_s}{dt}t\right) \right] \quad (3)$$

Where:

γ_C^1 is the primary creep strain

γ_T is the transient creep strain constant

B is the transient creep strain coefficient

$\frac{d\gamma_s}{dt}$ is the steady state creep rate

Darveaux presents primary creep constants for several Sn-Pb alloys.

Finally, the third step in a creep test is the steady state creep. A more general relationship was found for the secondary (steady-state) creep rate of soldered joints, as shown below:

$$\frac{d\gamma_s}{dt} = C_1 [\sinh(\alpha\tau)]^n \exp\left(\frac{-Q_a}{kT}\right) \quad (4)$$

Where:

$\frac{d\gamma_s}{dt}$ is the steady state strain rate

C_1 and α are constants

- n is the creep exponent, dependant upon the controlling creep mechanism
- k is Boltzmann's constant
- Q_a is the apparent activation energy
- T is the absolute temperature

Once again, Darveaux supplies the necessary constants for a number of Sn-Pb soldered joints.

Equations (2), (3) and (4) can be used to describe the stress-strain (including creep) behaviour of flip chip and BGA assemblies. Darveaux also implemented his model into two finite element tools, namely: ANSYS and ABAQUS. With proper material constant inputs, such finite element tools can be used model the creep behaviour of Sn-Pb alloys over a wide range of temperatures.

2.3.1.2 Knecht and Fox's Model

Knecht and Fox conducted isothermal mechanical fatigue testing, under torsion loads, of eutectic soldered joints for a Leadless Ceramic Chip Carrier (LCCC) test vehicle [16]. The tests were performed at temperatures of 25°C, 60°C and 100°C. They found that creep rate versus stress curves are bi-linear, with each linear portion associated with a different creep mechanism: grain boundary creep at low stresses and matrix creep at high stresses. Furthermore, they concluded that creep-fatigue failures are dominated by the steady-state portion of the creep curve.

The total shear strain can thus be summarized by the following equation:

$$\gamma = \gamma_E + \gamma_P + \gamma_C \quad (5)$$

Where:

γ is the total shear strain

γ_E is the elastic strain

γ_P is the time-independent plastic strain

γ_C is the secondary creep strain

The elastic component can be described by:

$$\gamma_E = \frac{\tau}{G(T)} \quad (6)$$

Where:

τ is the applied shear stress

$G(T)$ is the temperature dependent shear modulus

The time-dependent plastic strain can be described by the following plastic flow rule:

$$\gamma_P = \left(\frac{\tau}{\tau_P(T)} \right)^2 \quad (7)$$

Where:

τ_P is the temperature-dependent plasticity parameter

The temperature-dependant plasticity parameter can be obtained by curve-fitting the experimental data published by Knecht and Fox.

Finally, the creep strain can be obtained by integrating the steady state creep strain rate expression given below:

$$\frac{d\gamma_C}{dt} = 8.31 \cdot \exp\left(-\frac{0.5eV}{kT}\right) \tau^2 + 1.12 \cdot \exp\left(-\frac{0.84eV}{kT}\right) \tau^{7.1} \quad (8a)$$

or

$$\frac{d\gamma_C}{dt} = 3.952 \times 10^{-4} \cdot \exp\left(-\frac{0.5eV}{kT}\right) \tau^2 + 5.327 \times 10^{-5} \cdot \exp\left(-\frac{0.84eV}{kT}\right) \tau^{7.1} \quad (8b)$$

Where:

k is Boltzmann's constant

T is the absolute temperature

Equation (8a) is used when τ is expressed in MPa, while equation (8b) is used when τ is expressed in psi.

The first term in equation (8), with a stress exponent of 2 and activation energy of 0.5eV, describes grain boundary creep. The second term, with a stress exponent of 7.1 and activation energy of 0.84eV describes matrix creep.

2.3.1.3 Wong's Model

Wong et al. compiled Sn-Pb eutectic solder steady state creep data from seven independent sources, covering several orders of magnitude in stress level and creep rates [17]. The data was found to fit within the correlation band shown in the following figure.

Figure 15: Creep rate plot for Pb-Sn eutectic solder

As is generally expected from creep-life experiments, the raw data produced by Wong et al. fell within a band of approximately one order of magnitude in the vertical direction. The data in Figure 15 is scaled by the temperature-dependent Young's modulus along the horizontal axis, and is normalized by an Arrhenius-type temperature-dependent diffusion parameter $D(T)$ along the vertical axis:

$$D(T) = \exp\left(-\frac{Q_c}{RT}\right) = \exp\left(-\frac{5473}{T}\right) \quad (9)$$

Where:

Q_c is the average activation energy for creep of eutectic S-Pb solder

$$(Q_c = 45 \text{ kJ/mole} = 0.47 \text{ eV})$$

R is the universal gas constant ($R=8.314 \text{ J/}^\circ\text{K}\cdot\text{mole}$)

The curves in Figure 15 show two segments, each with distinct slopes, that describe different creep mechanisms: dislocation glide (with a stress exponent of 3, in the low stress region) and dislocation climb (with a stress exponent of 7 in the high stress region).

Based on data points falling within the curve shown in Figure 15, Wong expressed the average creep rate of eutectic Sn-Pb solder with the following equation:

$$\frac{d\varepsilon_{ss}/dt}{D(T)} = 1.7 \times 10^{12} \left(\frac{\sigma_{ss}}{E(T)} \right)^3 + 8.9 \times 10^{24} \left(\frac{\sigma_{ss}}{E(T)} \right)^7 \quad (10)$$

Where:

$d\varepsilon_{ss}/dt$ is the steady state creep strain rate

$D(T)$ is the temperature dependent diffusion parameter

σ_{ss} is the steady state stress

$E(T)$ is the temperature-dependent Young's modulus

2.3.2 Life Models for Thermo-Mechanical Fatigue

The primary failure mechanism of soldered joint is ductile low cycle fatigue (LCF) failure, where the cyclic thermo-mechanical loads (as well as creep) cause severe plastic deformation of the joint. Therefore, fatigue laws used to predict the life of soldered joints

are typically based on the classical Coffin-Manson law or the Morrow law, both strain-based models. Three examples of solder life prediction models are described below.

2.3.2.1 Coffin-Manson Law

Clech has reported using the following modified Coffin-Manson law, with an adjustment for crack area, to predict the characteristic life per unit crack area of a soldered joint [18].

$$\frac{N_f}{A} = c_1 (\Delta\gamma)^{-c_2} \quad (11)$$

Where:

N_f is the number of cycles to failure

A is the minimum area of the soldered joint along the crack propagation axis

c_1, c_2 are empirical material constants

$\Delta\gamma$ is the cyclic strain range

Clech proposes calculating the strain range under the assumption that compliance in the solder joint accounts for the entire load due to thermal mismatch between the component and the substrate, as follows:

$$\Delta\gamma = \frac{L\Delta\alpha\Delta T}{h} \quad (12)$$

Where:

L is the distance to the neutral point

$\Delta\alpha$ is the difference in CTE between the component and the substrate

ΔT is the difference in temperature between the hot and cold extremes during thermal cycling

h solder joint height

From the expressions shown above, it is clear that the life model does not take into account the effect of the creep behaviour of soldered joints. Nonetheless, predictions made using this method have been correlated (with an accuracy in the range of $\pm 2\times$) with the datasets of 27 experiments.

2.3.2.2 Morrow Law

In order to take into consideration the plastic deformation due to creep, variations of the more general Morrow law have been proposed in order to predict the thermo-mechanical fatigue life of soldered joints. The Morrow law is based on the plastic strain energy experience by the solder joint per cycle (due to mechanically applied plastic deformation as well as plastic deformation due to creep), rather than solely based on mechanically applied plastic strains.

2.3.2.2.1 Engelmaier-Wild Model

The standard IPC-D-279 proposes the Engelmaier-Wild solder creep fatigue expression shown below [19]:

$$N_f = \frac{1}{2} \left[\frac{2\varepsilon'_f}{\Delta D} \right]^{-\frac{1}{c}} \quad (13)$$

Where:

ε'_f is the fatigue ductility coefficient (0.325 for eutectic Sn-Pb solder)

ΔD is the fatigue damage term (comparable to the strain energy term in the typical Morrow expression for fatigue life) representing complete creep/stress relaxation of the solder

Hence, the variable c is a temperature and time-dependent factor used to compensate for incomplete stress relaxation and creep in the solder due to limited dwell times at thermal plateaux (seen during accelerated thermal tests or in-service).

$$c = -0.442 - 6 \times 10^{-4} T_{sj} + 1.74 \times 10^{-2} \ln \left(1 + \frac{360}{t_D} \right) \quad (14)$$

Where:

T_{SJ} is the mean cyclic solder joint temperature

t_D is the half-cycle dwell time in minutes

Cyclically applied time-independent plastic strains as well as time / temperature / stress dependent creep strains will form a hysteresis loop characterizing the solder joint's response to thermo-mechanical cycling. The damage term shown in equation (13) represents the area of the hysteresis loop and quantifies the cyclically accumulated fatigue damage.

Depending on the type of assembly (leadless or leadless), IPC-D-279 offers different expressions for computing the damage term, as follows:

For leadless assemblies:
$$\Delta D = \frac{FL_D \Delta(\alpha \Delta T)}{h} \quad (15)$$

For leaded assemblies:
$$\Delta D = \frac{FK_D (L_D \Delta(\alpha \Delta T))^2}{(919kPa)Ah} \quad (16)$$

Where:

F is the empirical factor describing “non-ideal” deviations of the actual soldered joints compared to idealizing assumptions

K_D is the component lead stiffness

L_D is the distance to the neutral point

H is the solder joint height

$\Delta(\alpha \Delta T)$ is the cyclic expansion mismatch between the component and substrate

A is the effective minimum load bearing solder joint area

Due to the conditions and assumptions under which the Engelmaier-Wild model was developed, the model is subjected to some restrictive caveats. Use outside of the intended regimes will not give accurate results. The caveats associated with the Engelmaier-Wild model are as follows:

Caveat 1: Solder Joint Quality. This caveat is to ensure that the failure mechanism is a ductile failure in the solder and not brittle fracture at the interface due to a poor material choice for lead or base metal.

Caveat 2: Large Temperature Excursions. The damage mechanism changes in the solder in joints experiencing large temperature swings.

Caveat 3: High frequency/low temperature. Stress relaxation / creep may not be the dominant mechanism and direct application of the Coffin-Manson equation may be more appropriate.

Caveat 4: Local expansion mismatch. When the local CTE mismatch between the solder and the interfaces is the dominant response, the above equations do not apply.

Caveat 5: Very stiff leads/very large expansion mismatches. The damage models do not consider the Young's Modulus of any of the materials so they cannot accurately predict the amount of strain that would occur in the joint, leads, component, and substrate.

2.3.2.2.2 Clech Model

The following energy-based model proposed by Clech [20] is similar, in form, to his Coffin-Manson type model described in equation (11):

$$\frac{N_f}{A} = \frac{6.149 \times 10^7 \times C}{\Delta W^{0.998}} \quad (17)$$

Where:

N_f is the number of cycles to failure

- A is the minimum area of the soldered joint along the crack propagation axis
- C is a model correlation factor
- ΔW is the cyclic plastic strain energy per unit volume (sum of the contributions due to both local and global CTE mismatches)

The cyclic plastic strain energy is obtained as the area of the hysteresis loop, taking into account thermo-mechanically applied strain (at both the local and global levels) as well as strain due to creep. This model was based on test results of 19 experiments, and further correlated with test results of 14 subsequent experiments. As such, the model is supported by 33 experiments.

2.3.3 Solder Reliability Solutions™

Solder Reliability Solutions™ (SRS) is a PC-based model used to determine the reliability of Pb-Sn soldered joints for practical engineering applications [20]. The software was first developed and introduced by J.P. Clech and has been subsequently implemented within a number of industries in order to rapidly predict the reliability of an electronic package early in the design stage.

2.3.3.1 Model Description

The SRS software is based on the plastic strain energy model described in section 2.3.2.2.2 and uses Wong's constitutive model, described in section 2.3.1.3, in the construction of the soldered joint hysteresis loop required for determining the cyclic plastic strain energy term. Hysteresis loops are developed for both the global CTE mismatch between board and component and the local CTE mismatch between the lead to solder and solder to board differences. The total strain energy for the cycle is thus the sum of both energies for the local and global mismatch.

2.3.3.2 Global Mismatch

The SRS model uses simplified one-dimensional structural assumptions to estimate the solder joint stress / strain due to the global CTE mismatch. This mismatch deforms the solder in shear due to the different relative expansions between the board and component.

However, not all deformation occurs solely in the solder, some elastic deformation occurs in the compliant members of the assembly as well, consequently reducing the magnitude of plastic strain assumed in the soldered joint.

To account for this reduction, a stress reduction line equation is used to reduce the maximum stress during the loading of the solder joint, as described by the following equation:

$$\gamma + \frac{\tau}{k} = \gamma_{MAX} \quad (18)$$

Where:

γ is the shear strain in the soldered joint

τ is the shear stress in the soldered joint

k is the slope of the stress reduction line

γ_{MAX} is the maximum shear strain in the solder joint should the solder itself absorb all the thermal strain (as defined in equation (12))

The parameter k is defined as follows:

$$k = \frac{K * h_s}{A} \quad (19)$$

Where:

K is the assembly stiffness

A is the solder shear area

h_s is the height of the joint

The assembly stiffness parameter accounts for the local stiffness details of the assembly. Methodologies from literature are given to account for the stiffness of leaded assemblies, ball grid arrays, leadless chip carriers, etc.

2.3.3.3 Local Mismatch

The SRS model uses a tri-layer model where a relatively soft layer of solder is constrained between two stiff layers: the substrate material on the bottom and the lead material (or the component, in the case of a leadless chip carrier) on the top. A methodology is given to determine the equations of the stress reduction line for the local CTE mismatch problem. The procedure equates the shear forces developed in each layer and uses strain compatibility equations for the boundaries to determine the stress reduction line equation as:

$$\varepsilon_{in} + \sigma \left(\frac{1}{E(T)} + \frac{1}{k_L} \right) = (\alpha_{EFF} - \alpha_s) \Delta T \quad (20)$$

Where:

ε_{in} is the inelastic strain in the soldered joint

σ is the normal stress in the soldered joint

$E(T)$ is the temperature-dependent Young's modulus for the solder material

k_L is local stiffness parameter

α_{EFF} is the effective local CTE for the board and component working against the solder

α_s is the CTE of the solder

ΔT is the change in Temperature

The effective local CTE is defined as:

$$\alpha_{EFF} = \frac{E_L h_L \alpha_L + E_b h_b \alpha_b}{E_L h_L + E_b h_b} \quad (21)$$

Where:

E , h , and α are the Young's modulus, height and CTE respectively

L, b correspond the local and board properties, respectively

The local stiffness parameter used in the stress reduction equation is defined as:

$$k_L = E_L \frac{h_L}{h_s} + E_b \frac{h_b}{h_s}, \quad (22)$$

where each variable has been previously defined.

2.3.3.4 Hysteresis Loop Construction

The hysteresis loop is formed in a series of 6 steps. Each of the steps is the same for both the local and global CTE mismatches. In effect, for one thermal cycle, two hysteresis loops are formed and are assumed to be acting independently. The description of the hysteresis loop construction is based on the following figure.

Figure 16: Hysteresis loop construction

Step 1: The loop starts at an arbitrary strain level γ_A at a zero stress state. The solder joint deforms during the temperature ramp. This deformation is assumed to be time-independent plastic deformation described by the plastic flow rule proposed by Knecht and Fox (refer to equation (7)). Point B is determined as the intersection between the plastic flow line (AB) and the stress reduction line (BC).

Step 2: During the dwell time at the hot side of the temperature cycle, the solder joint stress relaxes from point B to C. The stress reduction (B to C) and creep strains (B to C)

are calculated using the dislocation glide portion of the creep rate law proposed by Wong (refer to equation (10)). Differentiating the creep rate equation, it can be solved to determine the value of the shear stress at point C. Substituting this into the stress reduction equation yields the corresponding shear strain at C.

Step 3: When the thermal cycle reverses, unloading of the solder joint occurs, as shown from point C to D. It is assumed that the unloading line is a straight vertical line. Elastic strain recovery is not accounted for because, in general, the elastic portion of the total strain is almost negligible when compared to plastic and creep strains. As a result, point D has the same ordinate as point C, but a different abscissa value ($\tau_D = 0$).

Step 4: Upon further cooling of the joint, stress builds up in the opposite direction due to the CTE mismatch between component and substrate. Analogous to Step 1, point E is determined as the intersection point of the plastic flow line and the stress reduction line.

Step 5: Depending on the temperature at the cold end of the cyclic temperature, creep may occur as well even though the temperature is lower. Therefore, procedure identical to the procedure outlined in step 2 is performed to locate point F.

Step 6: When the thermal cycle reverses once more (the temperature increases), the unloading line is again a straight vertical line, neglecting elastic strains as in step 3.

The loop is assumed closed, as shown in Figure 17, if γ_F is equal to γ_A or within a specified tolerance. Otherwise, the procedure is repeated again with a new initial strain condition, γ_A . The strain range, γ_D to γ_A (width of the loop) gives the cyclic inelastic strain for each cycle.

Figure 17: Closed hysteresis loop

With the inelastic strain energy determined, the joint characteristic life is then determined from the SRS model. The number of cycles to a fraction failed is determined using a two-parameter Weibull failure function.

$$N(F) = \alpha_{joint} \left[-\ln(1 - F) \right]^{\frac{1}{\beta}} \quad (23)$$

Where:

$N(F)$ is the number of cycles to a fraction failed (F) of the population

α_{joint} is the joint characteristic life

β is a parameter greater than unity describing the variability of the population and must be determined through experimentation

F is a measure of the reliability of the population and is determined by the analyst for the application being studied.

For each thermal condition (or cycle range), the above procedure can be repeated to determine another number of cycles to failure. Using the cumulative damage rule known as Miner's rule, the electronic package can be assessed for fatigue life.

2.3.3.5 Sample Analysis

A sample analysis of an electronic board using the Solder Reliability Solutions™ software package, as well as the interpretation of the results, is included in Appendix A: of this report. The analysis was performed on a board encased in the Pheonix Mars Lander's meteorological system, the Canadian Space Agency's contribution to the Pheonix program.

3 Optimization of Fatigue Life in Soldered Joints

When designing an electronic package, a number of design and manufacturing parameters must be considered in order to optimize the fatigue life of the assembly, which is typically limited by the fatigue life of the soldered joints. Often, trade-offs must be performed in order to balance parameters influencing the fatigue life of the package and parameters influencing the efficiency of the design with respect to size and capacity of the circuit board. This section presents a summary of the surface mount technology specification IPC-SM-785 [14], sections 5.0 and 6.0.

3.1 Design Parameters

3.1.1 Primary Design Parameters

The following parameters have been identified as having primary (order of magnitude) influence on the fatigue reliability of soldered connections:

- a) **Component Size** governs the relative displacement between the substrate and component when subjected to thermal expansion and contraction. Larger components are more likely to negatively affect reliability.
- b) **Attachment Type**, either leadless or leaded, influences the maximum strain level that can occur in a given assembly during thermal cycling. A leaded assembly will typically result in a longer fatigue life since the leads offer sufficient elastic compliance to accommodate the global CTE mismatch between the component and the board.
- c) **Solder Joint Height** governs the level of strain measured in the solder joint when subjected to a given displacement between a component and substrate. A larger solder joint height will typically result in improved reliability.
- d) **Solder Joint Area** governs the stresses experienced in the solder joint due to a given thermal displacement between the component and substrate. As can be expected, a larger solder joint area will result in improved reliability by reducing the applied stress magnitude.

- e) **Lead Stiffness** governs the forces present within the solder joint as a result of a given displacement between a component and substrate. Lower lead stiffness (or increased lead compliance) results in improved reliability.
- f) **CTE-Mismatch and Cyclic Expansion Mismatch** govern the change in linear dimension (material expansion) a given material (substrate and component) will undergo when exposed to a change in temperature. The difference in CTE between the materials being joined must be managed in order to minimize the forces exerted within the solder joint when subjected to thermal cycling. A lower CTE mismatch between the substrate and component typically results in greater joint reliability.
- g) **Cyclic Temperature Swing** is the difference between maximum and minimum steady-state temperatures indicative of normal operating conditions. They can be the result of daily temperature or load variations. Typically, the temperature swing of the substrate is not equal to that of the component. Therefore, it is advantageous to minimize the difference in temperature realized under normal operating conditions in order to improve joint reliability.

3.1.2 Secondary Design Parameters

Although the effects of secondary design parameters are of lesser importance on their own, their influence in addition to the primary design parameters can be significant. The following parameters have been identified, by themselves, as having secondary influence on the fatigue reliability of soldered connections:

- a) **Solder/Base-Material CTE-Mismatch** – A local difference in coefficients of thermal expansion introduces internal forces increasing damage caused by cyclic fatigue. A reduced local CTE mismatch will typically improve the joint reliability.
- b) **Solder Joint Shape/Fillet/Volume** – The shape, fillet and volume of the solder joint have been found affect joint reliability. The fillet in particular affects the time necessary for crack propagation, as it influences the required distance of crack propagation before rupture.

- c) **Initial Solder Joint Grain Structure** – An initially fine grain structure in solder joints has been found to improve the cyclic life in highly accelerated testing. However, given the instability of the solder grain structure, a fine grain structure will only slightly improve the joint's fatigue life.
- d) **Conformal Coating** – The benefits of applying conformal coatings to solder joints is dependant on several factors including the type of material, thickness and location. One advantage of conformal coating is that it protects surface cracks by inhibiting corrosion. However, depending on the thermal expansion coefficient of the conformal coating material, additional forces may be introduced as a result of the conformal coating application.
- e) **Compliant Substrate Surface Layers** – The inclusion of compliant layers on the substrate surface can result in improved reliability margins.
- f) **Solder Composition** – The most common solder composition being eutectic and near-eutectic Sn-Pb is well documented. However, other compositions, which may have higher or lower fatigue reliability, are not as thoroughly documented nor understood.

3.2 *Manufacturing Parameters*

Due to the high density and small scale of soldered joints, visual inspection of electronic assemblies after the manufacturing process has been proven to be largely ineffective in identifying defects and is unlikely to uncover more than 70% of defects. Even double visual inspection is unlikely to uncover more than 91% of defects. Therefore, by applying statistical process controls, defects can be limited to as low as 50 ppm or 0.005%. In order to effectively execute statistical process controls, process capability studies must be conducted on all parameters affecting the manufacturing process. Final product verification is accomplished through careful monitoring of trends and distributions as established via the process capability studies.

There are various defects occurring during the manufacturing process that can affect the quality of the final product. It is important that they are accurately modeled during the process capability studies so that the process controls can adequately control the quality

of the manufacturing process. The following list captures common manufacturing defects requiring system controls:

- a) **Wetting Defects** – Poor wetting can cause insufficient joint formation resulting in poor reliability in mechanical and fatigue testing, indicate poor metallurgical bonding, or in some cases allow for corrosion.
- b) **Surface Contamination** – Surface contamination can result in the formation of a poor solder joint. In addition, contaminants in the solder joint after soldering can promote corrosion.
- c) **Solder Contamination** – Solder contamination can drastically affect the visual and mechanical properties of the soldered joint, and reduce the fatigue life of the joint.
- d) **Solder Volume** – An increase or decrease in solder volume may result in altered fatigue life, mechanical strength, and soldered component life.
- e) **Solder Joint Touch-up, Rework and Repair** – Touch-up, rework and repair often require that the solder joint be reheated above the liquidus temperature of the solder. In doing so, the printed board assembly is subjected to temperatures above their critical temperature. In addition, board cleanliness, flexure, tool impact, and electrostatic discharge must be closely managed to minimize further defects incurred by additional repair and rework.

Materials used in the fabrication process typically have material properties that change with temperature. This variation must be considered when process capability testing is designed to ensure accurate results. Of particular note is the relationship between temperature and the properties of the solder, conformal coating materials, individual components, and the printed board materials.

4 Evaluation of Pb-free Solders for Aerospace Applications

4.1 Pb-free Solder Compositions

Some of the proposed Pb-free solders are listed in Table 2, along with the breakdown of their compositions. It can be easily seen that the majority of the Pb-free solders maintain the use of Sn as the principal alloying element. Sn continues to be an ideal candidate for soldering applications due to its low elemental melting temperature of 231°C, and ability to wet many types of substrates with the help of fluxes. In order to design an optimum soldering material, Sn is alloyed with a number of different elements in order to overcome some of its weaknesses such as: being prone to pest, demonstrating poor response to thermal cycling, and being prone to whisker growth.

Table 2: Pb-free solder alloy compositions

Alloys	Sn	In	Zn	Ag	Bi	Sb	Cu	Mg	Fe
Bi-26In-17Sn	17	26			57				
Bi-32In		32			68				
Bi-41.7Sn-1.3Zn	41.7		1.3		57				
Bi-41Sn-1Ag	41			1	58				
Bi-42Sn	42				58				
Bi-43Sn (eutectic)	43				57				
Bi-43Sn-2.5Fe	43				54.5				2.5
Bi-45Sn-0.33Ag	45			0.33	54.7				
In-3Ag		97		3					
In-34Bi		66			34				
In-48Sn (eutectic)		52			48				
Sn-1Ag-1Sb	98			1		1			
Sn-1Ag-1Sb-1Zn	97		1	1		1			
Sn-2.5Ag-0.8Cu-0.5Sb	96.2			2.5		0.5	0.8		
Sn-2.8Ag-20In	77.2	20		2.8					
Sn-25Ag-10Sb	65			25		10			
Sn-2Ag	98			2					
Sn-2Ag-0.8Cu-0.6Sb	96.6			2		0.6	0.8		
Sn-2Ag-0.8Cu-6Zn	91.2		6	2			0.8		
Sn-2Ag-0.8Cu-8Zn	89.2		8	2			0.8		
Sn-3.5Ag	96.5			3.5					
Sn-3.5Ag-6Bi	90.5			3.5	6				
Sn-3.5Ag-1Zn	95.5		1	3.5					
Sn-3.5Ag-1Zn-0.5Cu	95		1	3.5			0.5		
Sn-3.6Ag-1.5Cu	94.9			3.6			1.5		
Sn-4.7Ag-1.7Cu	93.6			4.7			1.7		
Sn-4Ag	96			4					
Sn-4Ag-7Sb	89			4		7			
Sn-4Ag-7Sb-1Zn	88		1	4		7			

Alloys	Sn	In	Zn	Ag	Bi	Sb	Cu	Mg	Fe
Sn-10Bi-0.8Cu	89.2				10		0.8		
Sn-10Bi-0.8Cu-1Zn	88.2		1		10		0.8		
Sn-10Bi-5Sb	85				10	5			
Sn-10Bi-5Sb-1Zn	84		1		10	5			
Sn-4.8Bi-3.4Ag	91.8			3.4	4.8				
Sn-42Bi	58				42				
Sn-45Bi-3Sb	52				45	3			
Sn-45Bi-3Sb-1Zn	51		1		45	3			
Sn-56Bi-1Ag	43			1	56				
Sn-5Bi-3.5Ag	91.5			3.5	5				
Sn-7.5Bi-2Ag-0.5Cu	90			2	7.5		0.5		
Sn-0.75Cu	99.25						0.75		
Sn-0.7Cu (eutectic)	99.3						0.7		
Sn-2Cu-0.8Sb-0.2Ag	97			0.2		0.8	2		
Sn-3Cu	97						3		
Sn-4Cu-0.5Ag	95.5			0.5			4		
Sn-10In-1Ag-10.5Bi	78.5	10		1	10.5				
Sn-20In-2.8Ag	77.2	20		2.8					
Sn-42In	58	42							
Sn-5In-3.5Ag	91.5	5		3.5					
Sn-10In-1Ag-0.5Sb	88.5	10		1		0.5			
Sn-36In	64	36							
Sn-50In	50	50							
Sn-8.8In-7.6Zn	83.6	8.8	7.6						
Sn-2Mg (eutectic)	98							2	
Sn-5Sb	95					5			
Sn-4Sb-8Zn	88		8			4			
Sn-7Zn-10In-2Sb	81	10	7			2			
Sn-8Zn-10In-2Bi	80	10	8		2				
Sn-8Zn-4In	88	4	8						
Sn-8Zn-5In-	86.5	5	8	0.5					
(0.1-0.5)Ag									
Sn-9Zn-10In	81	10	9						
Sn-5.5Zn-4.5In-3.5Bi	86.5	4.5	5.5		3.5				
Sn-6Zn-6Bi	88		6		6				
Sn-9Zn (eutectic)	91		9						
Sn-9Zn-5In	86	5	9						

When considering Pb-free alternatives for soldering, such as those listed above, it is important that they demonstrate equivalent or superior properties to the traditional Sn-Pb alloys. The properties typically considered when evaluating Pb-free alloys are listed in Table 3.

Table 3: Important properties of soldering alloys

Properties related to manufacturing	Properties related to reliability
Cost	Solder to substrate bonding
Availability	Solidification behaviour
Toxicity	Strength
Melting Point	Creep resistance
Wetting ability	Thermal performance
	Fatigue life

4.2 Properties Related to Manufacturing Process Reliability

4.2.1 Cost

Since the electronics industry is a highly competitive industry whereby the manufacturers are continually striving to produce higher performing PCBs at lower cost, the cost of the soldering alloy is critical. Since Sn and Pb are both inexpensive metals, it is difficult to develop a Pb-free alloy with an equivalently low cost since the typical alloying elements that are added to the Sn are generally more costly, as shown in Table 4 [2].

Table 4: Elemental costs of alloying metals

Alloying Element	Cost, US\$/kg (1997)
Lead, Pb	1.10
Zinc, Zn	1.08
Copper, Cu	2.24
Antimony, Sb	2.64
Bismuth, Bi	7.15
Tin, Sn	8.67
Silver, Ag	153.19
Indium, In	194.59

Due to the significant cost difference between the elements listed above, the advantages in mechanical properties and long-term reliability of using a costly element such as Ag must outweigh the initial procurement cost of the alloy.

Although the space industry is also trying to reduce manufacturing costs, the justification of using expensive raw materials may be more easily made for space applications where

the production runs of a specific PCB are much smaller. Consequently, the total raw material cost represents a much smaller portion of the overall program cost, even when minimum purchase requirements are in effect. Hence, it is unlikely that the relatively small savings in selecting a less costly alloying material will outweigh the potentially greater risk cost associated with decreased long-term reliability.

4.2.2 Availability

When selecting an alloying candidate for a Sn-based Pb-free solder, the availability of the alloying metal must be considered in order to ensure a practical manufacturing process. In fact, some of the elements listed in Table 4 are known to be precious metals with limited world production. For example, indium is scarcely produced worldwide and must not be used as a major alloying element. The NCMS report estimated that the maximum amount of indium in the Pb-free solder alloy must be less than 0.5 wt% [26]. According to the NCMS report, bismuth is also a rare metal and its use must be less than 15 wt% in solder alloys.

4.2.3 Toxicity

Since Pb is being eliminated from solder alloys due to its toxicity, one must be prudent in selecting alloying elements for Pb-free solders to ensure that the candidate substitution material does not present a similar hazard. For example, the following candidate metals are known to be hazardous to human health. Introduced to the human body through inhalation, Indium is reported to be harmful to the heart, kidney, and liver [29]. Human exposure to antimony through inhalation is also known to be a hazardous, causing effects on the skin, eyes and respiratory system [30]. Finally, bismuth inhalation can result in decreased appetite, weakness, pneumatic pain, fever, and gingivitis [31].

As the harmful effects of In, Sb, and Bi can occur due to occupational exposure to the aforementioned elements, any manufacturing process containing those metals must be tightly controlled. The daily concentration of exposure to the toxic metals must be kept to a minimum, as outlined by the American Conference of Governmental Industrial Hygienists (ACGIH).

Table 5: Threshold exposures to toxic metals

Metal	Concentration of exposure per 8 hour day
Lead, Pb	0.15 mg Pb/m ³
Indium, In	0.1 mg In/m ³
Antimony, Sb	0.5 mg/m ³
Bismuth, Bi	N/A (though known to be toxic)

4.2.4 Melting temperature

The melting point of Pb-free soldering alloys is a critical property in the soldered joint manufacturing process. Since the high-yield wave and reflow soldering processes described in sections 1.1.2.1 and 1.1.2.2 have been developed specifically for the Sn-Pb solders, the Pb-free candidate replacement alloys would ideally have a similar melting temperature to that of eutectic Sn-Pb solder, namely 183°C. For Sn-Pb alloys, the typical wave soldering and reflow soldering temperatures are 250°C and 230°C, respectively. Maintaining a Pb-free solder melting temperature comparable to 183°C will facilitate a more seamless adaptation of the traditional wave and reflow soldering processes for Pb-free solders.

The melting temperature of Pb-free solders must also be considered from the perspective of potential damage to the PCBs. It is important to avoid a melting temperature that is significantly higher than the melting temperature of eutectic Sn-Pb in order to protect the individual electronic components on the PCBs as well as the PCB substrate. Electronic components such as capacitors and switches cannot tolerate an increase in reflow temperature. Furthermore, the PCB substrate is typically manufactured from thermoset polymers that must not degrade during the soldering operation due to exposure to high temperatures.

Typical processing temperatures of Pb-free solder candidates are given in Table 6 [21]. It can be seen that Pb-free solders based on Sn-Ag and Sn-Cu binary systems require processing temperatures that are only slightly higher than those for eutectic Sn-Pb. However, since the melting temperature of Sn-Ag and Sn-Cu alloys (around 230°C) is significantly higher than the T_m for eutectic Sn-Pb, the processing temperature window is much narrower. On the other hand, Pb-free solders based on the Sn-Bi binary system

have slightly lower processing temperatures than eutectic Sn-Pb. Although advantageous with respect to the damage control of electronic components and substrate materials, a lower melting temperature generally results in poor creep behaviour of the material. Creep in Pb-free solders and its effects on reliability of the joints are further discussed in section 4.3.4 of the report.

Table 6: Typical processing temperatures of Pb-free soldering candidates

Alloy composition	Temperature [°C]	
	Wave soldering	Reflow soldering
Sn-(3-3.9)%Ag [-(0.5-0.7)%Cu], or [-(1-3)%Bi]	250-260	235-250
Sn-57%Bi [-(0.5-1)%Ag]	N/A	180-200
Sn-(8-9%)Zn [-3%Bi]	~250	220-230
Sn-0.7%Cu [-Ag, Ni, Au]	250-260	N/A

Note: Figures in [] are the third alloying elements and their typical compositions.

4.2.5 Wetting characteristics

Wetting can be defined as the ability of a material, generally a liquid, to spread over another material, generally a solid [32]. The wetting ability of a solder is a crucial factor in the manufacturing of soldered joints in order to ensure that a proper metallurgical bond will take place between the solder and the copper lead. When discussing the wetting characteristics of Pb-free solders, three aspects of the wetting mechanism must be evaluated: wetting angle, surface tension and wetting force.

The wetting angle between a liquid droplet and solid substrate is shown in Figure 18 [2]. Generally, good wetting of the substrate is achieved when the wetting angle is between 0° and 90° and poor wetting of the substrate occurs when the wetting angle is between 90° and 180°.

Figure 18: Wetting angle diagram

The wetting angle (θ) is influenced by the surface tensions of the liquid (γ_{lg}), solid (γ_{gs}), and liquid-solid interface (γ_{ls}), and can be determined by the Young-Dupre equation:

$$\gamma_{gs} = \gamma_{ls} + \gamma_{gl} \cos \theta \quad (24)$$

Therefore, in order to evaluate the wetting characteristics of Pb-free solders, one must understand the influence of various alloying elements on the surface tension of the liquid solder and at the liquid-solid interface.

The surface tension of a liquid is a thermodynamic quantity and can be defined as the amount of work required to isothermally enlarge the surface area of the liquid [33]. The surface tensions of solders under processing conditions are not precisely known due to the many factors that can influence the system including: temperature, flux composition, and solder-substrate interaction. Although there is limited surface tension data available for Pb-free solders, some studies of simple binary systems have been performed. The results of the work performed by Vincent and Richards [34] on the surface tension of a selection of binary Pb-free alloys in both air and nitrogen (<20 ppm O₂) at 50°C over their liquidus temperature is summarized in Table 7. The resulting radius of curvature of the soldered joint due to the measured surface tension is also reported.

Table 7: Surface tension and radius of curvature of Pb-free solder alloys

Alloy	Surface tension (mN/m)		Radius of curvature (mm)	
	Air	Nitrogen	R _{air}	R _{nitrogen}
Bi-42Sn	319	349	1.93	2.02
Sn-9Zn	518	487	2.7	2.61
Sn-40Pb*	417	464	2.19	2.31
Sn-3.5Ag	431	493	2.44	2.61
Sn-0.7Cu	491	461	2.62	2.54
Sn-5Sb	468	495	2.57	2.64

*Near eutectic Sn-40Pb included as a baseline for comparison

In an effort to continually maximize the real estate for electronic components on the surface of PCBs, manufacturers are trying to reduce the pitch between the soldering contacts. From Table 7, it can be seen that only the Bi-42Sn alloy creates a natural radius smaller than the radius for Pb-Sn. Since the other listed alloys have a greater natural radius, the risk of bridging between contacts increases, particularly as the pitch between contacts is decreasing.

Wetting force is another characteristic used to describe the extent of wetting of a solder onto a substrate. A study of the wetting force balance examining the force of interaction between a solid dipped into a liquid and subsequently retracted can provide information pertaining not only to the extent of wetting but also the time required to achieve an ideal contact area. The time required to complete soldering operations is an important parameter influencing the productivity of an electronics manufacturer and can ultimately dictate the industrial acceptability of new Pb-free solders. Hence, electronics manufacturers seek soldering alloys demonstrating a high wetting force within a short wetting time.

Tojima [35] performed experiments using three Pb-free solders at processing temperatures of 62°C above their respective melting temperatures in order to determine the wetting force ($F_{\max}$) and time to wetting (T_w). The experiments were run once using an aggressive clean flux and repeated with a less aggressive no-clean flux. The results are summarized in Table 8.

Table 8: Wetting force and time to wet on bare Cu coupons, at 62°C above T_m

Alloy	T_m (°C)	$F_{max (avg)}$ (mN)	$T_w (avg)$ (s)
(a) Aqueous clean flux			
Sn-37Pb	183	4.792	0.385
Sn-3.5Ag	221	4.822	0.400
Sn-58Bi	139	3.518	0.608
Sn-9Zn	199	1.772	0.625
(b) No-clean flux			
Sn-37Pb	183	3.486	1.571
Sn-3.5Ag	221	4.013	0.785
Sn-58Bi	139	2.410	4.092
Sn-9Zn	199	-4.300	N/A

Among the three Pb-free solders tested, it appears that the Sn-3.5Ag solder demonstrated the best wetting characteristics with a wetting force slightly higher than eutectic Sn-37Pb and a comparable time to wet. However, its higher melting temperature poses challenges for the reflow process. The Sn-9Zn alloy demonstrated the poorest wetting characteristics. In fact, when used in conjunction with the less aggressive flux, its wetting force was negative indicating that the Sn-9Zn alloy did not wet the copper coupon at all.

4.3 Properties Related to In-Service Reliability

4.3.1 Solder to substrate bonding

The fundamental role of a soldered joint is to provide a bond between the solder and the copper lead. In order to understand and evaluate the quality of the bond between the solder and the copper lead, one must consider the formation of intermetallic compounds (IMCs) at the solder to substrate interface. It has been shown that the formation of extensive and rough IMCs decreases the quality of the solder to substrate bond by reducing the joint's ductility and strength [36].

Recent works by Yu et al ([37] and [38]) have focused on the growth of IMCs in specific Pb-free solders: Sn-3.5Ag, Sn-3.5Ag-0.7Cu, and Sn-3.5Ag-1.7Cu systems on both copper and nickel substrates. They found that, similarly to the Sn-Pb system, a Cu_6Sn_5 IMC forms at the solder to copper interface and a Ni_6Sn_5 IMC forms at the solder to nickel

interface. As shown in below, the $(\text{Cu,Ni})_6\text{Sn}_5$ IMCs are comprised of scallop-shaped grains. However, when using the Sn-Ag based alloys on the copper and nickel substrates, the surface of the grains is less smooth (compared to using the Sn-37Pb alloy) and small light-colored particles form on the surface of the grains during the solidification of the soldered joint. Scanning Electron Microscope (SEM) images of the morphologies described can be seen in Figure 19. The small light-colored particles consist of the Ag_3Sn and can range from about 50nm to 100nm in size.

Figure 19: Surface morphology of IMCs at the solder to substrate interface

The more surprising results of the study revealed that the surface morphology of the IMC at the solder to substrate interface varied depending on the region being observed. These results are shown in Figure 20. On top of the wetting region, the IMCs are facet-like ranging in size from about 4 to 7 μm . Higher magnification of the same region shows hundreds of nano-particles formed on the IMC surface. Adjacent to the wetting region, the IMCs are column-shaped, at about 3 μm in length, with tens of particles formed on their surface. Throughout the remainder of the interface, the IMCs are column-shaped and also around 3 μm in length. Although the morphologies shown below are different, it is clear that they are all the same compound.

Figure 20: Surface morphology of Sn-3.5Ag-0.7Cu/Ni IMC per region

Yu et al determined that the predominant mechanism of IMC growth during soldering is through grain boundary diffusion. The as-soldered microstructures of eutectic Sn-Ag

after soldering at various times are presented in Figure 21. The regions shown in the images consist of: the copper substrate, the Cu-Sn IMC layer, and the solder matrix.

Figure 21: Micrographs of the Sn-3.5Ag/Cu interface, soldered at 250°C

It appears from the figure above that the thickness of the IMC layer increases with an increase in soldering time. Another factor affecting the thickness of the IMC layer is the composition of the soldering alloy. Figure 22 shows that the IMC layer thickness increases with the quantity of Cu in the alloy composition.

Figure 22: Effect of composition on IMC thickness

It is well-known that IMCs at the solder to substrate as well as at the solder to component interfaces can reduce the reliability of the joint by providing sites for crack initiation and growth during cyclical loading. Furthermore, IMCs can also contribute to the lift-off phenomena as discussed in the following section.

4.3.2 Solidification behaviour

Though closely related to the discussion of solder to substrate bonding, the solidification behaviour of Pb-free solders must be addressed in order to assess their reliability. One particularly concerning phenomena related to solidification of the soldered joint has been noticed to date in the work dedicated to developing reliable Pb-free solders: the lift-off phenomena.

The “lift-off” defect can be described as the solidification event by which the solder fillet is peeled from a Cu land on a circuit board on cooling from soldering [39]. Particularly evident when soldering with Sn-Bi systems, this defect has been studied extensively by Suganuma et al. [39], [40]. Sn-Bi systems are important to consider in the search for an alternative to Sn-Pb solders as they possess equivalent soldering temperatures. However, the research performed by Suganuma et al. demonstrated that the Bi content in the soldering alloy had an important effect on the probability of lift-off occurring.

Figure 23 a) shows a typical micrograph of the lift-off phenomenon observed in a through hole connection using a Sn-22Bi-2Ag alloy as the solder. It can be clearly seen that about half of the edge of the solder fillet has lifted-off from the Cu land around the hole. In Figure 23 b), an enlarged micrograph of the lifted edge shows the formation of bridges between the Cu land and the solder fillet. Suganuma determined that the bridges consist of Sn and Bi and suggested that they form like icicles of the liquid solder on the lift-off face.

Figure 23: SEM photograph of lift-off solder fillet (Sn-22Bi-2Ag)

Figure 24 a) shows a micrograph of the Sn-25Bi solder to Cu land interface near the area where the lift-off occurred. It is apparent that severe segregation of Bi occurred at the interface between the Cu land and the solder fillet. A thick Cu_6Sn_5 IMC layer formed on the Cu land and voids formed between the IMC layer and the segregated Bi. The formation of the voids indicates both poor wetting at the solder/ Cu_6Sn_5 interface and the presence of a force acting vertically to the interface [40].

Figure 24 b) shows a micrograph of the same Sn-25Bi solder to Cu land interface where the lift-off occurred. It is obvious that the lift-off occurred exactly at the interface between the Cu_6Sn_5 layer and the solder, at the Bi segregation, with no solder nor Bi on the Cu_6Sn_5 surface and no Cu_6Sn_5 left in the solder. Since the surface morphology of the Cu_6Sn_5 layer is very complex, such clean separation indicated that lift-off occurred before the Sn-Bi matrix of the solder had solidified. The rapid solidification of the IMC layer through dendrite formation compared to the slower solidification of the Sn-Bi matrix instigated the lift-off phenomenon to develop.

Figure 24: SEM photograph of the Sn-25Bi/Cu interface

The basic explanation for the occurrence of lift-off is two-fold. First of all, segregation of Bi at the interface forming a liquid both slows the solidification of the Sn-Bi matrix and weakens the adhesive strength of the bond. As shown in Figure 25, the dendrite formation traps the Bi into the liquid interface region between a solder fillet and a Cu land. The substantial amount of Bi along the interface maintains the region in a liquid state. Second of all, lift-off is caused by thermal shrinkage of a Cu lead in a through-hole and by solidification shrinkage of the solder itself, as illustrated in Figure 26.

Solidification shrinkage and the mismatch in thermal expansion coefficients between the solder and the substrate can result in lift-off.

Figure 25: Mechanism of Bi segregation at liquid-solid interface

Figure 26: Illustration of lift-off by shrinkage

The methods that Suganuma [39] suggests to reduce the probability of lift-off occurring include:

1. Eliminating the microsegregation of Bi along the solder/Cu land interface on solidification by suppressing the dendrite growth through rapid cooling and/or adding a third element.

2. Reducing the lift-off force acting on the fillet by better controlling the solidification shrinkage of the solder and expansion of the Cu land.

Overall, lift-off is a serious solder defect that greatly reduces the reliability of the joint, and consequently must be overcome when designing Pb-free solders.

4.3.3 Strength

In-service, PCBs are exposed to conditions that induce both shear and tensile loading on the soldered joints. Hence, when considering alternative Pb-free alloys for soldering applications, it is important to gauge both their shear and tensile strengths.

4.3.3.1 Shear strength

Shear loading is introduced into soldered joints due to differences in the coefficient of thermal expansion between the electronic component and the PCB substrate, as shown in Figure 27, where the board expands more than the component. Although there is surprisingly little work done exclusively on the shear properties of Pb-free solders (generally, shear strength is simply calculated from experimental tensile strength), some work has been done to study the effect of temperature on the shear strength of a soldered joint. Table 9 summarizes the loss in shear strength in going from 20°C to 100°C or 25°C to 100°C in three Pb-free solders (Pb-40Sn included as a baseline).

Figure 27: Shear stress induced in a soldered joint

Table 9: Shear loading in a soldered joint

Alloy composition	Shear strength (Mpa)			Loss (%)
	20°C	25°C	100°C	
Sn-40Pb	34.0		21.0	38
In-48Sn		14.0	3.5	75
Sn-3.5Ag		27.0	14.0	48
	38.0		23.0	39
Sn-5Sb	37.0		21.0	43
	28.0		14.0	50

It can be seen from Table 9 that the total loss in shear strength over a temperature range is slightly greater in the Pb-free solders than in the Sn-40Pb solder. Hence, a tertiary alloying element may have to be added to the alloys listed above in order to minimize the effect of temperature difference of the shear strength of the Pb-free joints.

4.3.3.2 Tensile strength

Tensile loading is introduced into soldered joints through bending of the PBC substrate, as shown in Figure 28. Since the PCBs are often constrained around their perimeters and can be exposed to severe vibration environments in-service, bending of the PCBs and the ability of Pb-free solders to withstand the resulting tensile loading of the soldered joints must be evaluated.

Figure 28: Tensile loading in a soldered joint

When evaluating the tensile strength of a material, one must consider the Yield Strength (YS), Ultimate Tensile Strength (UTS) and Elastic Modulus (E). An extensive conglomeration of tensile strength properties of Pb-free solders, from various sources, has been compiled and published by Abtew and Selvaduray [2]. Their findings showed that the elastic modulus of the Pb-free solders varied from as low as 19.5GPa for the In-48Sn alloy, to as high as 50 GPa for the Sn-3.5 alloy (compared to an elastic modulus of 39GPa for the traditional Sn-37Pb eutectic solder). Generally, a lower elastic modulus is sought because the induced stress in the soldered joint is less severe for a given strain, based on Hook's law.

It is difficult to compare data on yield strength, ultimate tensile strength and ductility from different sources since these properties are largely dependent upon microstructure and strain rate which, in turn, are dependent upon testing, process and environmental parameters encountered during the experiments. However, the trend observed in the data compiled by Abtew and Selvaduray shows that the tensile strength of Pb-free solders is generally higher than that of the Sn-40Pb alloy.

4.3.4 Creep resistance

The prevailing deformation mechanism in soldered joints is through creep. As discussed in section 2.1.3.1, the creep mechanism of Pb-Sn soldered joints is dominated by diffusion while the creep mechanism of Pb-free soldered joints is dominated by dislocation climb. Many studies have shown that the creep rate of Pb-free solders is much lower than the creep rate of Pb-Sn solders indicating that, in general, Pb-free solders offer improved creep resistance over Pb-Sn solders, particularly at elevated temperatures and low stress levels. These conclusions must be kept in mind when faced with fatigue-life test data collected during accelerated testing. Many investigators are quick to report, erroneously, that fatigue-life data for Pb-free soldered joints shows improved fatigue-life over traditional Pb-Sn soldered joints. The challenge presented by accelerated test data of Pb-free soldered joint is that there isn't sufficient dwell time at each hot and cold plateau to capture the full effect of creep on the overall plastic deformation of the specimen under test. Hence, conclusions pertaining to remarkable improvements in fatigue life for Pb-free soldered joints may be superficially positive as the effect of long-term strain due to creep are not captured in accelerated testing results.

4.3.5 Thermal performance

The development of Pb-free solders has brought about a number of challenges to overcome with respect to their performance under varying thermal conditions. These challenges are due to both the allotropy and anisotropy of tin.

4.3.5.1 Tin pest

Tin and its alloys are prone to the serious temperature-related defect called tin pest, pictured in Figure 29. Tin pest consists of the formation of grey tin on the surface of a sample at temperatures below 13°C. The transition in crystallographic structure from body-centred tetragonal, bct (white tin) to a diamond cubic (grey tin) is due to the allotropy of tin. During this transformation, the sample can undergo as much as a 26% change in volume resulting in local cracking and eventual disintegration of the sample [6]. Although the metal samples shown in Figure 29 consists of pure tin, the formation of tin pest has also been observed in the Sn-0.5Cu soldering alloy [42].

Figure 29: Tin pest formation in a Sn-0.5Cu sample (aged at -18°C)

4.3.5.2 Thermal cycling induced defects

Anisotropy can be defined as a variation of material properties with respect to crystallographic direction [6]. For example, at room temperature, tin has a body centered tetragonal structure producing a two-fold change in the coefficient of thermal expansion (CTE) depending on grain direction and three-fold change in Young's Modulus. Due to these changes in properties, significant stresses can develop at grain boundaries.

Although a reduction in the net effect of the stresses can be seen when a sample contains a large number of randomly oriented grains, the effects of the stresses are much more serious in a soldered joint that may be comprised of only a few grains. Hence, repeated thermal cycling can result in surface roughening and extrusion of the soldered joint as well as eventual cracking. The thermally induced defects caused by the anisotropy of a tin are shown in Figure 30.

Figure 30: Surface damage in a Sn-3.8Ag-0.7Cu ingot due to thermal cycling

4.3.5.3 Tin whiskers

With the elimination of Pb from traditional solder alloys comes the concern of tin whisker growth in pure Sn electroplating of electronic component terminals. Although not a concern associated specifically with Pb-free solder alloys, the risk of tin whisker growth must be considered since pure Sn is being used as an inexpensive and solderable alternative to Pb-Sn electroplating of component terminals.

Tin whisker growth is a phenomenon that has been studied and documented since 1946 [45]. Illustrated in Figure 31, tin whiskers consist of spontaneously growing conductive single crystals, up to 10 mm in length, that could lead to potentially catastrophic failures of high reliability circuits. There are numerous publicly documented system failures attributed to tin whiskers, including three complete losses of commercial satellites: GALAXY IV, GALAXY VI and SOLIDARIDAD I [46]. In fact, the concern over tin whiskers in the aerospace industry is sufficiently acute that an entire team of individuals at NASA is dedicated to mitigating the risk of tin whiskers on the Space Shuttle program.

Figure 31: Whisker growth on pure tinplated components [47]

There are four failure modes associated with tin whiskers, as listed in the table below:

Table 10: Failure modes induced by tin whiskers [47]

Failure Mode	Description
1. Permanent short circuits	Whiskers can create an electrical short between finely pitched components. In low current circuits (low voltage, high impedance), the current can be sufficiently low that it does not fuse the whisker, resulting in a stable (permanent) short circuit.
2. Transient short circuits	In higher current circuits (typically above 30 mA), the circuit may only experience a transient glitch until the whisker is fused open.
3. Metal vapour (plasma) arcing in vacuum	In vacuum conditions, and high voltage (above 18V) / high current (above a few amperes) circuits, tin whiskers may vapourize creating a plasma of conductive ions, capable of conducting hundreds of amperes. The arc may be sustained until the supply of tin is depleted, causing mission-critical damage to in-service space hardware.

Failure Mode	Description
4. Debris/Contamination	Since tin whiskers are fragile structures, random vibration and mechanical shock may cause whiskers to break loose from their originating surfaces. Such free-floating conductive particles may subsequently interfere with sensitive optical surfaces, micromechanical systems, or bridge isolated conductors resulting in short circuits.

Although an abundance of literature pertaining to tin whiskers is available, there is nonetheless a lack an industry-accepted understanding of tin whisker growth mechanisms, risk factors, and/or test methods for characterizing the tin whisker growth propensity for a given component or assembly. However, many researchers agree that the driving force behind whisker growth is from compressive stresses within the electroplated tin layer. Such compressive forces may be due to a number of factors including:

- Electroplating chemistry and process
- Substrate stress from mechanical processes (cold rolling, swaging, piercing, stamping, etc.)
- Diffusion of substrate elements into the tin layer
- IMCs altering the lattice spacing in the tin plating
- Externally applied mechanical stresses from system assembly, transportation, handling, etc.
- Environmentally-induced stresses such as thermal cycling and high temperature storage
- Surface tin oxide causing specific volume change on the surface of the tin plating.

All in all, tin whiskers is a serious concern for Pb-free electronics and must be thoroughly understood before allowing the widespread use of components with pure tin plated leads in space application and other high-reliability industries.

4.3.6 Fatigue life

The mechanical fatigue life of a solder joint by the number of stress cycles it endures before a crack is initiated and propagates. Fatigue failure of a solder joint can occur due to defects and irregularities in the microstructure that could serve as crack initiation sites. Rapid crack growth is initiated by stress concentrations caused by defects in the microstructure. Such failures may even occur when the cyclic stress in the joint is well below the yield stress of the material. Since soldered joints are increasingly exposed to severe dynamic environments, it is important to understand the fatigue resistance behaviour of Pb-free solders due to mechanically induced fatigue loading. Electronic packages in space applications are exposed to mechanical fatigue load cycles during pre-delivery vibration testing, ground handling and transportation, and transportation to orbit.

Although the thermo-mechanical fatigue of soldered joints is well documented, there is not an abundance of work that has been done on the purely mechanical fatigue resistance of Pb-free alloys specifically. What information does exist is based mainly on laboratory fatigue tests, without standardized characterization of the test conditions nor in-depth investigation of the initial microstructure or failure mechanism. Nonetheless, Lea concluded that, in general, Pb-free solders demonstrated improved fatigue resistance over eutectic Sn-Pb [48]. Some Pb-free solders ranked in increasing order of fatigue resistance were: 64Sn-36In, 42Sn-58Bi, 50Sn-50In, 99.25Sn-0.75Cu, 100Sn, 96Sn-4Ag, and 95Sn-5Sb. These conclusions support earlier results of fatigue resistance work conducted by Marshall and Walter finding that Ag-containing solders were superior to both eutectic Sn-Pb and In-Sn solders [49].

4.4 Current NASA Research

In general, Pb-free solder research has been funded by the commercial electronics industry, with little focus on the particular requirements and limitations of space applications. Following the Pb-free solder trend demonstrated in the commercial electronics industry, NASA (National Aeronautics and Space Administration) has begun preparing for the possibility of making the transition to Pb-free solders in high reliability

space applications by undertaking a number of space-specific Pb-free studies. This section provides a status and summary of the findings related to four Pb-free solder studies lead by NASA, two championed by the Jet Propulsions Laboratory (JPL), a third championed by the Goddard Space Flight Centre (GSFC), and a fourth championed by the Kennedy Space Centre (KSC).

4.4.1 JPL Evaluation of Pb-free Alloys Phase I

The first phase of the JPL evaluation of Pb-free alloys, completed in 2004, dealt with determining the most feasible candidates for replacing eutectic Pb-Sn solder, while also investigating suitable processing operations in assembling Printed Wiring Boards (PWBs) [50]. Following an extensive literature review, four Pb-free solder pastes were selected for closer evaluation:

1. Sn96.5Ag3.5 (eutectic)	221°C (T_M)
2. Sn95.5Ag3.8Cu0.7	217-218°C (T_M)
3. Sn96.2Ag2.5Cu0.8Sb0.5 (Castin [®])	217-218°C (T_M)
4. Sn77.2In20.0Ag2.8 (Indalloy 227 [®])	175°C (T_S) -187°C (T_L)

Two PWBs were assembled using each of the solder types listed above, for a total of eight electronic assemblies each resembling the typical test PWB shown in Figure 32. The PWBs were assembled in the SMT laboratory at JPL using a bench-top reflow unit. Once assembled, scanning acoustic microscopy analysis was performed on each PWB (boards and components) in order to determine whether any damage was imparted to the PWBs during processing at the higher temperatures required by the four Pb-free alloys. Results showed that the boards themselves survived the higher processing temperatures, but some of the plastic BGA components experienced delamination, indicating that they must be baked prior to reflow to avoid delamination issues.

Figure 32: JPL typical PWB test specimen

4.4.2 JPL Evaluation of Pb-free Alloys Phase II

The purpose of the second phase of the JPL evaluation of Pb-free alloys is to perform thermal cycle testing of four Pb-free PWB assemblies, using a eutectic Pb-Sn PWB assembly as a control. For this phase of the evaluation, the four candidate Pb-free solders identified in Phase I were down-selected to the following two alloys:

1. Sn95.5Ag3.8Cu0.7	217-218°C (T _M)
2. Sn96.2Ag2.5Cu0.8Sb0.5 (Castin [®])	217-218°C (T _M)

The above two Pb-free solder candidates were retained based on their suitability for reflow processing. Furthermore, the indium-containing solder alloy was deemed undesirable due to its wide pasty region (non-favourable for reflow operations) coupled with scarce world-wide availability of indium [50].

For the thermal cycle tests, 12 test PWB assemblies utilized: four PWBs were assembled using each of the solders listed above, as well as four control control PWBs using eutectic SnPb solder. Each assembly was then subjected to thermal cycling over the range of -55°C to 125°C for 100 cycles. Once thermal cycling was complete, the PWB assemblies were removed from the thermal chamber and inspected for signs of failure, both visually and under 30x magnification.

Results from the Phase II tests showed that both the Sn95.5Ag3.8Cu0.7 and Sn96.2Ag2.5Cu0.8Sb0.5 solders passed the thermal cycling without signs of cracking.

4.4.3 GSFC Evaluation of Pb-free Solders

In contrast to the JPL evaluation of Pb-free solders, GSFC selected a single alloy for further investigation [51]. The selected solder, Sn96.5Ag3.5 was selected for a number of reasons:

- Eutectic binary alloy, similar to eutectic Pb-Sn
- Widely available materials
- Comparable cost to eutectic Pb-Sn

As part of the GSFC evaluation of Pb-free solders, 10 boards were hand-soldered using Sn96.5Ag3.5. Results of the soldering process concluded that Sn-Ag requires twice as long to wet when compared with eutectic Pb-Sn, and that the resulting Pb-free solder joints have a dull appearance. However, optical inspections of Sn-Ag solder ball cross-sections revealed no significant difference from Pb-Sn solder joints.

The 10 boards assembled by GSFC are currently undergoing thermal cycling to failure, over the temperature range of -55°C to 125°C . Once thermal cycle testing is complete, the results will be compared with the conclusions drawn by other companies in the commercial electronics industry.

4.4.4 KSC Evaluation of Pb-free Solders

The NASA Technology Evaluation for Environmental Risk Mitigation (TEERM) Center at KSC has undertaken an extensive evaluation of Pb-free solders through the Joint Council on Aging Aircraft (JCAA) / Joint Group on Pollution Prevention (JG-PP) Lead-Free Solder Project. The Pb-free solders selected for testing were:

- 95.5Sn3.9Ag0.6Cu (SAC)
- 92.3Sn3.4Ag1.0Cu3.3Bi (SACB)
- 99.3Sn0.7Cu, Ni-stabilized (SnCu)

As with the other NASA tests, eutectic SnPb solder was used as a control for the experiments.

The test vehicles included both PTH and SMT components including: Ceramic Leadless Chip Carriers (CLCC-20); Plastic Leaded Chip Carriers (PLCC); Thin Small Outline Packages (TSOP-50); Thin Quad Flat Packs (TQFP-144 and TQFP-208); Plastic Ball Grid Arrays (BGA-225); Plastic Dual-in-line Packages (PDIP-20); surface mount ceramic capacitors; and surface mount resistors. The components were also selected with a variety of finishes including: SnPb, SAC, SACB, nickel-palladium-gold (NiPdAu), SnCu, and Sn. A photograph of one of the test vehicles is shown in Figure 33.

Figure 33: JCAA/JG-PP Lead-free solder project test vehicle

The project also attempted to study the reliability of both newly manufactured PWB assemblies using Pb-free solders as well as PWB assemblies that were reworked using Pb-free solders. As a result, “manufactured” test vehicles were assembled using Pb-free solders and designed for Pb-free processes (using a laminate circuit board with a high glass transition temperature (T_g) of 170°C) while the “reworked” test vehicles were assembled using Pb-free solders but were not specifically designed for Pb-free soldering

processes (using a laminate circuit board with a T_g of 140°C). The “reworked” test vehicles thus represented legacy PWBs that may be repaired using Pb-free solders.

In order to capture all aspects of solder joint reliability, a variety of tests were performed on the test vehicles, as listed below:

1. Random mechanical vibration
2. Thermal shock
3. Low stress thermal cycling
4. High stress thermal cycling
5. Combined environments testing (vibration and thermal cycling)
6. Mechanical shock
7. Salt fog
8. Humidity
9. Surface insulation resistance
10. Electrochemical migration resistance

General conclusions drawn from this study suggest that Pb-free solders are as reliable as eutectic SnPb solder for some component types and environments, but can also fail before SnPb solder for with component types and environments. However, it was also shown that component type has a greater effect on solder reliability than solder type, particularly for thermal cycling and combined environments. While an executive summary of all testing results and conclusions was published, in draft format, in July 2007 [52], the results of both the low and high stress thermal cycling tests are captured below.

The low stress thermal profile cycled between -20°C and +80°C with dwell times of 30 minutes (hot dwell) and 10 minutes (cold dwell) and ramp rates of approximately 9.5°C/minute (cooling) and 7.2°C/minute (heating). A 30 minute hot temperature dwell

time, which is longer than a typical 10 minute dwell time, was selected in order to capture the damaging effect of creep. The thermal cycle profile is shown in Figure 34.

Figure 34: Low stress thermal cycle profile, -20°C to +80°C [52]

Only “manufactured” test vehicles were evaluated during the low-stress thermal cycling tests. Although the test is on-going, at last report, the test vehicles had undergone 11,100 thermal cycles with an expected test completion of 15,000 cycles. All of the solder attachments of CLCCs and TSOP-50s have failed (SnPb and Pb-free), while the majority of the BGA components remain intact. For most of the different component types, it was found that the reliability of SACB meets or exceeds the reliability of SnPb when exposed to low stress thermal cycling while the reliability of SAC solder was, generally, only slightly more reliable than SnPb solder. Reliability results for each component type are presented in 2-parameter Weibull plots, as shown in Figure 35 and Figure 36. Test results also showed that small amounts of lead contamination (3%) resulted in a large decrease in the reliability of SACB and a small decrease in the reliability of SAC. As such, SACB solder should not be used where a risk of Pb contamination is present in order to maximize reliability.

Figure 35: Weibull plot of CLCC data for low-stress thermal cycling [53]

Figure 36: Weibull plot of TSOP data for low-stress thermal cycling [53]

The high stress thermal profile cycled between -55°C and +125°C with dwell times of 30 minutes (hot dwell) and 10 minutes (cold dwell) and a maximum temperature ramp rate of approximately 10°C/minute. A 30 minute hot temperature dwell time was once again selected in order to capture the damaging effect of creep. The thermal cycle profile is shown in Figure 37.

Figure 37: High stress thermal cycle profile, -55°C to +125°C [54]

Both “manufactured” and “reworked” test vehicles were subjected to 4743 thermal cycles during the high-stress thermal cycling tests and Weibull plots were generated once again for each component type. In general, results showed that Pb-free solders (SAC and SACB) used with CLCC and TSOP components (with the exception of the combination of SACB solder and SACB component finish) demonstrated lower reliability than the SnPb soldered controls while Pb-free solders used with other components demonstrated equivalent reliability to the controls. However, all Pb-free soldered components on the “reworked” test vehicles demonstrated higher failure rates than the PbSn controls. Sample Weibull plots generated from the high-stress thermal cycling test results are shown in Figure 38 and Figure 39.

Figure 38: Weibull plot of CLCC data for high-stress thermal cycling (“manufactured” test vehicle) [54]

Figure 39: Weibull plot of CLCC data for high-stress thermal cycling (“reworked” test vehicle) [54]

4.5 Space Readiness of Pb-free Solders

Since the emergence of Pb-free solders, the commercial and academic communities have taken the lead on research and testing of the proposed substitutes to the eutectic SnPb alloy. With the space industry representing less than 1% of the overall electronics market, space-specific research and testing of Pb-free solders has been largely lacking. Although a handful of Pb-free solder reliability testing programs have been undertaken by governmental space agencies, there is not a sufficiently large compilation of information to begin using Pb-free solders in high-reliability applications without incurring large risk.

Two specific areas require particular attention in order to improve the space-readiness of Pb-free solders. The first area that must be addressed is the collection of long-term reliability test data along with test-verified reliability predictive models for Pb-free solders suitable for the long-duration and extreme environments of space missions. The second area that must be addressed is the generation of suitable quality control processes for manufacturing, handling, and inventory management.

4.5.1 Long-term Reliability Data

Thermal cycling damage in a soldered joint is due mainly to creep occurring during the thermal plateaux. The majority of all Pb-free solder reliability data collected to date has been performed according to accelerated testing requirements such as IPC-SM-785, where the recommended dwell time at thermal plateaux is approximately 10 minutes in duration. However, such a short dwell time does not allow for the effect of creep to damage the soldered joint resulting in artificially long life results. Only a handful of thermal cycling tests have opted for extending the dwell times at thermal plateaux, such as the JCAA / JG-PP Lead-Free Solder Project which used a 30 minutes dwell time at the hot thermal plateau, in order to capture the effect of creep. It is important that more thermal cycling tests be performed with extended hot temperature dwell times, especially since thermal cycles in space applications can potentially be quite long, depending on the duration and orientation of the spacecraft orbit.

In addition to thermal cycling testing with extended dwell times, the space industry should also attempt to perform more system-level thermal cycling testing of PWB assemblies in order to establish system reliability rather than focussing exclusively on the reliability of the soldered joint. By performing system-level testing, the reliability of electrical components assembled using the higher manufacturing temperatures mandated by the use of Pb-free solders may also be captured. An ideal method of testing a PWB is to assemble a lead-free PWB assembly, acting as a shadow to an equivalent PbSn assembly, and perform in-situ monitoring of the Pb-free board until failure while the PWBs are assembled into the flight article and sent to orbit. Such in-situ testing would capture the combined effects of Pb-free solder and component reliabilities while also providing an actual thermal cycle for a given space craft orbit, and mission duration.

Finally, since studies have shown that solder reliability depends not only on solder composition but also on the component being soldered, material of the board, and severity of the thermal range, it is important that all permutations of reliability risk factors be studied when developing reliability test plans for Pb-free solders. The space industry must have a better understanding of the effect of each parameter mentioned above prior to accepting the use of Pb-free solder on “new” flight assemblies.

As the space industry works on increasing the amount of thermal cycling test data for Pb-free solders, a parallel effort of developing an analytical model for predicting the thermal cycle life of Pb-free assemblies must also be investigated. An ideal Pb-free solder reliability prediction model must be developed, and verified by test results. The ideal reliability predictive model should be derived based on the physical mechanism by which damage accumulates in the soldered joint, and supported/corrected with empirical test results.

The space community should also develop a better understanding of the effect of chemical composition tolerances on solder joint reliability. Although Pb-free candidates contain small amounts of some elements (ex: 0.7%Cu), manufacturing processes can only control the chemical composition of the soldered joint to +/- 0.1%. Fluctuations in chemical composition of Pb-free solder alloys could increase the propensity of IMC formation. A larger number and volume of IMCs near the solder joint to substrate and

component interfaces may reduce the solder joint reliability. As it is not yet clear how small variations in solder compositions affect reliability, testing must be performed in order to quantify the effect of composition variations on overall solder joint reliability.

To close, the space industry should strive for greater collaboration on Pb-free solder investigations and test programs, both within the space community itself as well as with the commercial electronics industry. At the moment, space-specific Pb-free solder publications suggest that a number of unique focus groups are working on improving NASA's body of knowledge with respect to Pb-free solders, but the focus groups are failing to collaborate on accumulating a common repository of Pb-free test data and results. Other benefits of a more collaborative effort include: learning from others' errors, greater teamwork when faced with a challenging problem, and an opportunity to ensure that each test program is striving for the common goal of collecting sufficient solder reliability test data to accept or reject the use of Pb-free solders in high-reliability circuits.

4.5.2 Quality Control Processes

In order to meet and control the high-reliability requirements imposed on space hardware, exhaustive manufacturing process controls are in place for traditional soldering techniques and manufacturing datasheets certifying compliance to the processes are collected for every component going into space. Any repairs to soldered joints occurring during the final assembly stage by the contract integrator must be documented. Once in space, the operation of every component must be continuously tracked.

4.5.2.1 Standard soldering techniques

Currently, the manufacturing process for all soldered joints aboard hardware being delivered to NASA must meet the Soldered Electrical Connections standard, NASA-STD-8739.9 [55]. This standard outlines the soldering process that electronics manufacturers must comply with for hand soldering, wave soldering and reflow soldering. The NASA-STD-8739.9 is presently tailored to soldering processes involving eutectic and near-eutectic Sn-Pb alloys. Typically, NASA's technical standards are extremely detailed documents leaving no room for the manufacturer's interpretation.

Process details such as soldering temperature, soldering time, environmental conditions, solder contaminant levels, etc., are all clearly outlined. In order to one day allow for the use of Pb-free solders in space applications, NASA's Soldered Electrical Connections standard will have to be updated to include optimized soldering processes for each Pb-free alloy deemed acceptable for space applications. This is an enormous and costly task as Pb-free solder candidates must be evaluated for compatibility with the space environment and alloy-specific soldering processes will have to be developed.

4.5.2.2 Component tracking

Should the aerospace industry embark upon the transition from Sn-Pb solders to Pb-free solders, it will be important to track exactly what solder alloy composition was used to create each joint. This will be particularly critical for repair soldering during final assembly of the deliverable unit. All technicians performing the assembly and repair of space hardware will have to be educated about the new soldering processes and the consequences of repairing a soldered joint with the wrong alloy. For example, the reliability of many Pb-free solders can be greatly reduced if contaminated with a small amount of lead.

During the transition phase, space hardware manufacturers will have to maintain inventory of all the soldering alloys they use in their assemblies. All in all, the space community must put in place a system to manage the added planning and logistics involved with stocking, using and tracking a wide range of Pb-free soldering alloys.

5 Conclusion

Although soldered joints are seemingly trivial structures due to their small stature, they are often the limiting factor when it comes to evaluating the reliability of an electronic package. Although a number of factors play a role in solder joint reliability, the most critical parameter to consider is thermo-mechanical fatigue life. The reliability of traditional SnPb soldered joints is a well-documented subject and, as such, many constitutive and fatigue life models are presented in existing literature. The application of such models, in order to determine the thermo-mechanical fatigue life of a soldered joint, must be limited to similar circumstances (solder composition, type of assembly, and expected service environment) to those used in the development and validation of the models.

However, due to existing and pending government legislations worldwide restricting the use of lead and other hazardous substances, the commercial microelectronics industry has been developing Pb-free replacements to traditional SnPb solder. A large number of candidate soldering alloy replacements have been proposed so far, each with their own strengths and weaknesses. Although research on the proposed Pb-free solders is still ongoing, some manufacturers have begun to phase out SnPb solders in an attempt to reduce the burden of maintaining both SnPb and Pb-free manufacturing lines and inventory. However, this poses a risk to high-reliability industries, such as the space industry, as there isn't yet sufficient Pb-free solder joint reliability data available to ensure that Pb-free solders will meet the stringent reliability requirements imposed on space applications. Therefore, the space industry must make a concentrated effort to ensure the space readiness of Pb-free solders before traditional SnPb solders are no longer available.

A number of areas must be addressed in order to improve the space-readiness of Pb-free solders, including:

- Performing extensive thermo-cycle testing, with various combinations of Pb-free solder types, components, and flux
- Developing a test-verified predictive reliability model for Pb-free solders, which can be used over the entire range of space service environments

- Attempting in-situ testing of non-critical boards assembled using Pb-free solders in actual service conditions
- Updating quality control processes related to manufacturing, inspection, inventory management, and repair of Pb-free soldered joints

Although conclusions drawn from limited Pb-free solder research performed specifically for space applications are encouraging, there is still a long road ahead in the preparation for transitioning from SnPb solders to Pb-free solders in the space industry.

6 References

- [1] H.H. Manko, Solder and Soldering, 2nd Edition, McGraw-Hill, New York, 1979.
- [2] Abtew, M. and Selvaduray G., Lead-free Solders in Microelectronics, *Journal of Materials Science and Engineering*, 2000, vol. 27, pp. 95-141
- [3] http://www.uyemura.com/solder_joint_reliability.htm
- [4] Engelmaier, W., Solder Joints in Electronics: Design for Reliability
- [5] Abdul-Baqi, A. *et al*, Fatigue damage modeling in solder interconnects using a cohesive zone approach, *International Journal of Solids and Structures*, 2005, vol. 42, pp. 927-942
- [6] Plumridge, W.J, Long term mechanical reliability with lead-free solders, *Soldering and Surface Mount Technology*, 2004, vol. 6, pp. 13-20
- [7] J.S. Hwang, Solder Paste in Electronic Packaging, Van Nostrand Reinhold, New York, 1989
- [8] Clech, J.P., Review and analysis of lead-free solder material properties, *NEMI-NIST-NSF-TMS workshop: Modeling and Data Needs for Lead-Free Solders*, 2001.
- [9] Kang, S. *et al*, Microstructure and mechanical properties of leaf-free solders and solder joints used in microelectronic applications, *IBM Journal of Research and Development*, 2005, vol. 49, pp. 607-620
- [10] Nachlas, J.A., Reliability Engineering: Probabilistic Models and Maintenance Methods, Boca Raton: Taylor & Francis, 2005
- [11] Villain, J. *et al.*, Creep behaviour of lead free and lead containing solder materials at high homologous temperatures with regard to small solder volumes, *Sensors and Actuators A: Physical*, 2002, vol. 99, pp. 194-197

- [12] Ridout, S. and Bailey, C., Review of methods to predict solder joint reliability under thermo-mechanical cycling, *Fatigue and Fracture of Engineering Materials and Structures*, vol. 0, no. 0, pp. ???-???
- [13] Dorn, J.E., *Some fundamental experiments on high temperature creep*, J. Mech Phys. Solids, 1954, vol. 3, pp. 85-116
- [14] IPC, IPC-SMT-785: Guidelines for Accelerated Reliability testing of Surface Mount Technology, 1992.
- [15] Darveaux, R. et al., Reliability of plastic ball grid array assemblies, Chap. 13, *BallGrid Array Technology*, ed. J.H. Lau, McGraw-Hill, 1995, pp. 379-442.
- [16] Knetch, S., Fox, L., Constitutive relation and creep-fatigue life model for eutectic tin-lead solder, *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, 1990, vol. 13, no. 2, pp. 424-433.
- [17] Wong, B. et al., A creep rupture model for two-phase eutectic solders, *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, 1998, vol 2, no 3, pp. 284-290.
- [18] Clech, J.P., Lead-free and mixed assembly solder reliability trends, APEX Designers Summit, 2004, IPC, Anaheim, California.
- [19] IPC, IPC-D-279: Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies, 1996.
- [20] Clech, J.P., Solder Reliability Solutions: A PC-based Design-for-Reliability Tool, *Surface Mount International Conference Proceedings*, Sept. 8-12, 1996, San Jose, CA, Vol. I, pp. 136-151.
- [21] Suganuma, K., Advances in Lead-Free Electronics Soldering, *Current Opinion in Solid State and Materials Science*, 2001, vol. 5., pp. 55-64
- [22] T.P. Vianco, Development of Alternatives to Lead-Bearing Solders, *Proceedings of the Technical Program on Surface Mount International*, 19 August to 2 September 1993, San Jose, CA.

- [23] R.E. Reed-Hill, Physical Metallurgy Principles, PWS Publishing Company, Massachusetts, 1994, pp. 306-307.
- [24] Wood, E.P., and K.L. Nimmo In search of new lead-free electronic solders, *Journal of Electronics Materials*, 1994, vol. 23, no. 8, pp.709-713.
- [25] European Parliament, Proposal for a Directive of the European Parliament and of the Council on Waste Electrical and Electronic Equipment and on the restriction of the use of certain hazardous substances in electrical and electronic equipment. COM, 2000, p.347
- [26] NCMS, Lead-free solder project final report, NCMS Report 0401RE96, Michigan: National Center for Manufacturing Sciences, 1997
- [27] Harrison MR, Vincent JH., IDEALS: Improved design life and environmentally aware manufacturing of electronics assemblies by lead-free soldering, *Proc 12th Microelectronics and Packaging Conference*, Cambridge: IMAPS Europe, 1999, pp. 98–104
- [28] JEIDA, Report on research and development on lead-free soldering, Tokyo: Japan Electronic Industry Development Association, 2000
- [29] N.I. Sax, R.J. Lewis, Sr., Dangerous Properties of Industrial Materials, 7th Edition, Van Nostrand Reinhold, New York, 1989, p. 2067
- [30] N.I. Sax, R.J. Lewis, Sr., Dangerous Properties of Industrial Materials, 7th Edition, Van Nostrand Reinhold, New York, 1989, p. 1985
- [31] N.I. Sax, R.J. Lewis, Sr., Dangerous Properties of Industrial Materials, 7th Edition, Van Nostrand Reinhold, New York, 1989, p. 277
- [32] Wassink, R.J.K and M.M.F. Verguld, Manufacturing Techniques for Surface Mounted Assemblies, Electrochemical Publications Ltd., 1995, GB-Port Erin, British Isles, p. 17
- [33] Wassink, R.J.K, Soldering in Electronics, 2nd Edition, Electrochemical Publications Ltd., 1989, GB-Port Erin, British Isles, pp. 36-37

- [34] Vincent, J.H. and B.P. Richards, Alternative solders for electronics assemblies, *Circuit World*, 1993, vol. 19, no. 3, p. 33
- [35] Tojima, K., Wetting Characteristics of Lead-free Solders, Senior Project Report, Materials Engineering Department, San Jose State University, May 1999.
- [36] Lee, H.T. and M.H. Chen, Influence of intermetallic compounds on the adhesive strength of solder joints, *Journal of Materials Science and Engineering*, 2002, vol. A333, pp. 24-34
- [37] Yu, D.Q et al, Intermetallic compounds growth between Sn-3.5Ag lead-free solder and Cu substrate by dipping method, *Journal of Alloys and Compounds*, 2005, vol. 392, pp. 192-199
- [38] Yu, D.Q et al, The formation of nano-Ag₃Sn particles on the intermetallic compounds during wetting reaction, *Journal of Alloys and Compounds*, 2005, vol. 389, pp. 153-155
- [39] Suganuma, K. et al., Lift-off phenomenon in wave soldering, *Acta mater.*, 2000, vol. 48, pp. 4475-4481
- [40] Suganuma, K., Microstructural features of lift-off phenomenon in through-hole circuit soldered bi Sn-Bi alloy, *Scripta Materialia*, 1998, vol. 38, no. 9, pp. 1333-1340
- [41] Plumridge, W.J, Long term mechanical reliability with lead-free solders, *Soldering and Surface Mount Technology*, 2004, vol. 6, pp. 13-20
- [42] Kariya, Y., C.R Gagg and W.J. Plumridge, Tin pest in solder alloys, *Soldering and Surface Mount Technology*, 2001, vol. 13, pp. 39-40
- [43] J.S. Hwang, Solder Paste in Electronic Packaging, Van Nostrand Reinhold, New York, 1989
- [44] Villain, J. et al., Creep behaviour of lead free and lead containing solder materials at high homologous temperatures with regard to smaller volumes, *Sensors and Actuators*, 2002, vol. A99, pp.194-197

- [45] Verdi, Fred W., *Electroplated Tin and Tin whiskers in Lead Free Electronics*, American Competitive Institute, Philadelphia, PA, 2004
- [46] NASA Goddard Tin whisker Home Page: <http://nepp.nasa.gov/whisker/>
- [47] Brusse, Jay A., et al, *Tin Whiskers: Attributes and Mitigation*, presented at *CARTS 2002: 22nd Capacitor and Resistor Technology Symposium*, March 2002, pp. 67-80.
- [48] Lea, C., *A Scientific Guide to Surface Mount Technology*, Electromechanical Publications Ltd., GB-Port Erin, British Isles, 1988
- [49] Marshall, J.L and S.R. Walter, *International Journal of Hybrid Microelectronics*, 1987, vol. 10, pp.11-17
- [50] Shapiro, Andrew A., et al, *implications of Pb-free Microelectronics Assembly in Aerospace Applications*, *IEEE Transactions on Components and Packaging Technologies*, vol. 29, no. 1, March 2006, pp. 60-70.
- [51] Kadesch, J., et al, *Technical Readiness Overview: Pb-Free Solder Alloy Investigation*, NASA Electronic Parts and Packaging Program, 2006.
<http://nepp.nasa.gov/>
- [52] JCAA/JG-PP Lead-Free Solder Project, *Joint Test Report, Executive Summary Draft*, July 2007.
http://teerm.nasa.gov/projects/LeadFreeSolderTestingForHighReliability_Proj1.html
- [53] Woodrow, T., JCAA/JG-PP Lead-Free Solder Project: -20°C to +80°C Thermal Cycle Test, *Proceedings of SMTA International Conference*, September 2006.
- [54] JCAA/JG-PP Lead-Free Solder Project, -55°C to +125°C Thermal Cycle Testing Final Report, rev B, May 2006.
http://teerm.nasa.gov/projects/LeadFreeSolderTestingForHighReliability_Proj1.html

[55] NASA Technical Standard, NASA-STD-8739.3, Soldered Electrical Connections, 1997

Appendix A: Sample Solder Joint Fatigue Analysis

A practical thermo-mechanical fatigue analysis of soldered joints on an electronics board used in a space application is presented in this appendix.

A.1 *Problem Description*

The most recent mission to Mars is the Phoenix lander (shown in Figure 40), launched in August 2007. Phoenix is specifically designed to measure volatiles (especially water) and complex organic molecules in the arctic plains of Mars, where the Mars Odyssey orbiter has discovered evidence of ice-rich soil very near the surface. The Phoenix mission is an international affair; space agencies from around the world are taking part in the outfitting of the lander with scientific equipment in which to carry-out this task. The Canadian Space Agency (CSA) is contributing the meteorological station (MET) on Pheonix. The MET is composed primarily of three instruments, a lidar to measure the degree of dust circulation in the atmosphere, a pressure sensor to measure atmospheric pressure at the landing sight, and a series of thermal couples to measure the temperature gradient at various elevations above the ground. Among these instruments, the most complex is the lidar, whose engineering model unit is shown in Figure 41 during payload integration testing.

Figure 40: Phoenix Lander on the surface of Mars

Figure 41: Engineering model of the Phoenix MET station

The conditions for the MET on Mars require operation throughout a large temperature variation for one sol duty cycle, where one sol corresponds to one Martian day. This large temperature difference can quickly cause fatigue degradation of the life the solder joint and eventually result in electrical failure. The Phoenix mission can be categorized as a NASA Category C mission, identified as a mission in which components are subjected to extreme thermal cycling and an overall short mission duration. The lifetimes of the solder joints between the electronic packages and the circuit boards due to thermal cycling had to be determined to give confidence that the MET would operate continuously throughout the 90 sol mission. The lifetime model developed by J.P. Clech [20] and implemented in the software package Solder Reliability SolutionsTM (SRS) was used for this analysis.

A.1.1 Analysis Inputs

A shape factor of six was used in the calculation of component lifetime, based on a Weibull analysis. This value is indicative of a controlled process and has been verified with the model's author as a conservative yet reasonable value to use when details of the actual manufacturing process are not known.

As previously mentioned, the SRS model has been validated against over 30 accelerated tests for test vehicles covering several generations of component assembly and circuit board technologies. These test vehicles included perimeter leaded assemblies, castellated leadless ceramic chip carriers (LCCC), chip scale packages, small outline transistors, and ball grid arrays (BGA). There are in total seven circuit boards used in the MET station. The electrical components that were selected for analysis are located on any of these boards. The selected components included a perimeter leaded package, an LCCC, and a BGA. They were selected as worst-case components either due to short leads or large overall package dimensions, both of which would reduce fatigue life. As such, these analyses present the worst-case scenarios, which would envelope all the other components used on the MET circuit boards.

A.1.2 Thermal Cycle

The thermal duty cycle for the circuit boards was determined through a detailed thermal analysis, the details of which are outside the scope of this report. The typical duty cycle is shown in Figure 42. As can be clearly seen in the figure below, the temperature change is caused by four temperature spikes creating overall temperature extremes of -28 °C to 42 °C (for a temperature differential of 70 °C) in this case. The local spikes are created as the MET station comes to life and takes measurements. The MET records the environment conditions four times each Sol.

Figure 42: Typical thermal duty cycle for electronic components over one sol

A.1.3 Component Details

Three components were chosen to represent the families of components used on the circuit boards; these were: a perimeter leaded assembly with J-leads, a BGA, and an LCCC. The components are bonded to the circuit board substrate using near-eutectic Sn-Pb solder. These components have been identified along with their corresponding temperature extremes in Table 11. For each temperature range, the three sub-cycles were scaled from the above figure. The dwell times were inputted as 15 minutes at the elevated temperature and 2 hours at the lower temperature. The overall temperature cycle loading was broken down into four separate thermal cycles for input into SRS. It was assumed that the three sub-cycles were equal in magnitude and evenly spanned the range from the lowest to highest temperature extreme of the main cycle. For example, the four cycles for the leaded assembly and LCCC are shown in Table 12.

Table 11: Electronic packages evaluated for thermal fatigue

Component Type	Thermal Extremes	Reference
Perimeter Leaded Assembly	-40 to 80 °C	Figure 43
Ball Grid Array	-40 to 92 °C	Figure 44
Leadless Ceramic Chip Carrier	-40 to 80 °C	Figure 45

Figure 43: Perimeter leaded component studied for thermal fatigue

Figure 44: BGA studied for thermal fatigue

Figure 45: LCCC studied for thermal fatigue

Table 12: Thermal cycles using the Rainflow method

Cycle Name	Temp. Hot (°C)	Temp. Cold (°C)	Dwell Hot (min)	Dwell Cold (min)
Main	80.0	-40.0	15.0	120.0
Sub-Cycle 1	8.0	-16.0	15.0	120.0
Sub-Cycle 2	32.0	8.0	15.0	120.0
Sub-Cycle 3	56.0	32.0	15.0	120.0

The circuit boards are made from a 19 layer laminate with a total thickness of 1.5951 mm (0.0628 in.). Table 13 lists the properties for the materials used to form each layer of the laminate. The stiffness property for the copper layers (“signal”, “thermal/ground” and “power/voltage”) has been estimated as:

$$E_{eq} = E_{Cu} \cdot \%Cu + E_{polyimide} \cdot (1 - \%Cu) \quad (25)$$

For stiffness calculation purposes, the copper content has been assumed to be 0% and 90% for the signal and ground/voltage layers respectively.

Table 13: Laminate board layer material properties

Material	E (Pa)	ν	α (m/m/ °C)	ρ (kg/m ³)
copper_0%	1.379E+010	0.30	1.49E-005	1660.8
polyimide	1.379E+010	0.30	1.49E-005	1660.8
copper	1.172E+011	0.30	1.69E-005	8940.6
copper_90%	1.0687E+011	0.30	1.69E-005	8940.6
Kovar	1.38E+011	0.317	5.5E-006	8360.0

Finally, a MET circuit board is shown in Figure 46, where each type of component discussed above is identified.

Figure 46: Phoenix MET station circuit board

A.1.4 Reliability Requirements

The NASA requirement for a Category C mission (short duration, extreme temperature variation) is to multiply the number of mission cycles by 3 and to add an additional 20 cycles to account for life consumption during ground tests. The Phoenix mission is 90 Sols or 90 thermal duty cycles. Following the guidelines, the electrical components for the MET circuit boards were evaluated for 290 thermal cycles ($3 \times 90 + 20$). The factor of 3

on life is intended to account for the scatter that is inherently present when evaluating fatigue life.

Due to the nature of the statistical data used to determine the fatigue life there is uncertainty. The SRS model predicts a reliability level for a given number of cycles. The evaluation criterion for reliability is not explicitly defined in the Phoenix System Requirements Definition (SRD). A typical reliability level used in industry for space bound hardware is a 1 in 100,000 failure rate. In other words, after the expected design duty cycle life, one would expect 0.001% of the population of components to have failed; conversely 99.999% of the population will have survived. The three components described above were evaluated at this reliability level.

A.2 Results

The analysis results are presented in two sections. The first part of the results consists of interim results (hysteresis curves) computed by SRS. The hysteresis curves are then used to compute the final reliability result for the electronic package.

A.2.1 Hysteresis Loops

The first set of results, shown below in Figure 47 through Figure 55, is comprised of the hysteresis curves and damage summary for the quad flatpack assembly.

It can be seen that the hysteresis curves representing damage in the solder joint due to the global CTE mismatch (refer to Figure 47 through Figure 50) actually consist of straight lines, indicating that no plastic strain (and hence no plastic strain energy) is developed in the soldered joint due to the global CTE mismatch between the component and the substrate. This can be justified by the fact that the flexibility in the leads of the assembly provide sufficient compliance to accommodate the difference in thermal expansion / compression between the component and the substrate without inducing plastic strain into the solder material.

Figure 47: Flatpack global mismatch hysteresis curve, main cycle

Figure 48: Flatpack global mismatch hysteresis curve, sub-cycle #1

Figure 49: Flatpack global mismatch hysteresis curve, sub-cycle #2

Figure 50: Flatpack global mismatch hysteresis curve, sub-cycle #3

Conversely, the hysteresis curves representing damage in the solder joint due to the local CTE mismatch (refer to Figure 51 through Figure 54) consist of closed hysteresis loops, indicating that plastic strain (and hence plastic strain energy) is indeed developed in the soldered joint due to the local CTE mismatch between the lead and the substrate. Each closed hysteresis loop shows a segment of plastic strain accumulation due to the thermomechanically applied load, as well as stress relaxation / creep lines on both the hot and cold side of the plot, during the dwell period of each thermal cycle. This can be justified

by the fact that the solder material plastically deforms in order to accommodate the difference in thermal expansion / compression between the leads and the board.

Figure 51: Flatpack local mismatch hysteresis curve, main cycle

Figure 52: Flatpack local mismatch hysteresis curve, sub-cycle #1

Figure 53: Flatpack local mismatch hysteresis curve, sub-cycle #2

Figure 54: Flatpack local mismatch hysteresis curve, sub-cycle #3

From the eight plots shown above, it can be concluded that the driving force behind damage accumulation due to thermo-mechanically applied loads is due to the local CTE mismatch rather than the global CTE mismatch.

Finally, the pie-chart shown in Figure 55 summarizes the damage contribution of each thermal cycle undergone by the quad flatpack assembly. As expected, the largest damage contribution is from the main thermal cycle (85.7%), with the greatest thermal extremes.

The damage contribution from each mini sub-cycle decreases as the mean temperature of the mini sub-cycle decreases. This can be explained by the fact that there is less creep strain developed in the solder as the temperature at the hot and cold dwell plateaux decreases.

Figure 55: Flatpack total damage summary

The second set of results, shown below in Figure 56 through Figure 64, is comprised of the hysteresis curves and damage summary for the BGA assembly.

Contrary to the results shown for the quad flatpack, it can be seen that the hysteresis curves representing damage in the BGA solder joint due to the global CTE mismatch (refer to Figure 56 through Figure 59) consist of narrow hysteresis loops, indicating that plastic strain (and plastic strain energy) is developed in the soldered joint due to the global CTE mismatch between the component and the substrate. This is justified by the lack of flexible leads in the assembly, which can accommodate the difference in thermal expansion / compression between the component and the board. As a result, the relative displacement between the component and the board is accommodated by plastic deformation of the solder balls in the BGA.

Figure 56: BGA global mismatch hysteresis curve, main cycle

Figure 57: BGA global mismatch hysteresis curve, sub-cycle #1

Figure 58: BGA global mismatch hysteresis curve, sub-cycle #2

Figure 59: BGA global mismatch hysteresis curve, sub-cycle #3

Furthermore, the hysteresis curves representing damage in the solder joint due to the local CTE mismatch (refer to Figure 60 through Figure 63) consist of closed hysteresis loops, indicating that plastic strain (and hence plastic strain energy) is also developed in the soldered joint due to the local CTE mismatch between the component pad and the substrate. As for the quad flatpack assembly, each closed hysteresis loop shows a segment of plastic strain accumulation due to the thermo-mechanically applied load, as well as stress relaxation / creep lines on both the hot and cold side of the plot, during the

dwell period of each thermal cycle. Once again, this can be justified by the fact that the solder material plastically deforms in order to accommodate the difference in thermal expansion / compression between the component pad and the board.

Figure 60: BGA local mismatch hysteresis curve, main cycle

Figure 61: BGA local mismatch hysteresis curve, sub-cycle #1

Figure 62: BGA local mismatch hysteresis curve, sub-cycle #2

Figure 63: BGA local mismatch hysteresis curve, sub-cycle #3

From the eight plots shown above, it can be concluded that the driving force behind damage accumulation due to thermo-mechanically applied loads is due to the local CTE mismatch rather than the global CTE mismatch since area of the hysteresis curves for the local CTE mismatch results is much larger than the area of the hysteresis curves for the global CTE mismatch results.

Finally, the pie-chart shown in Figure 64 summarizes the damage contribution of each thermal cycle undergone by the BGA assembly. As expected, the largest damage contribution is from the main thermal cycle (88.2%), with the greatest thermal extremes.

Once again, the damage contribution from each mini sub-cycle decreases as the mean temperature of the mini sub-cycle decreases since there is less creep strain developed in the solder as the temperature at the hot and cold dwell plateaux decreases.

Plastic BGA BG728 Package

Figure 64: BGA total damage summary

Finally, although not reported herein, the hysteresis loops for the LCCC assembly are computed in much the same manner by the SRS software, however the process must be repeated twice: once for damage accumulated in the thin solder layer between the component and the substrate and a second time for damage accumulated in the filleted toe of the soldered joint (refer to Figure 9 for an image of the two areas of damage accumulation in a filleted soldered joint). The total strain energy in the system is then computed by simply adding the areas of the hysteresis loops generated for each portion of the soldered joint.

A.2.2 Fatigue Life

The results of the fatigue analysis of the electrical components are shown in Figure 65. The graphic shows the failure rate of the population of components versus time to failure. In addition, the 290 sol design life and the 90 sol mission life are shown as well. The component life curve, to have an acceptable reliability level, should cross the 290 design cycle curve to the left of the vertical blue line representing a reliability level of 99.999% (failure rate of 0.001%). As can be seen from the curve, the leaded assembly and the

LCCC meet this requirement; however, the BGA does not. After 290 cycles, the reliability level of the BGA is roughly 98.3%.

Figure 65: Fatigue analysis results for solder joints in electronic packages

As mentioned previously, the beta factor describing the variability of the population was chosen to be 6 based on a best estimate (refer to equation 23). Industry data has shown that much higher beta factors have been achieved for BGA assemblies. This higher beta is mainly due to the fact that the BGA soldering process is performed robotically which tends to produce highly repetitive, low variation solder joints. However, since no data is available at this time concerning the board supplier's process, a conservative estimate for beta was used. Only a slight change to beta, or the confidence in the soldering process, has a significant effect on fatigue life.

A.3 Conclusion

Under predicted operational temperatures, it was shown that the leaded assembly and the LCCC both met the required reliability level for space applications. However, the reliability determined for the BGA was below the required reliability level, likely due to

the conservative beta factor chosen for generating the Weibull plot. Nonetheless, the results demonstrate a common contradiction encountered in the design of electronic packages: design features chosen for improved reliability of a component are often detrimental to the efficiency (size and capacity) of the end product. For example, the desire for miniaturization of electronic components with increasing numbers of input and output ports is driving designers towards BGA and flip chip construction. In BGAs and flip chips, a high density of input and output ports can be achieved over the whole area of the chip. However, in order to improve the fatigue life of a component, a leaded assembly is preferred in order to accommodate the global CTE mismatch in the flexibility of the leads. Unfortunately, leaded assemblies cannot provide an equivalent number of input and output ports to a BGA or a flip chip as the leads only surround the perimeter of the chip rather than the chip area.