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System-Wide Enhancement Of Distribution System Voltage Stability Operations

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SYSTEM-WIDE ENHANCEMENT OF DISTRIBUTION SYSTEM VOLTAGE STABILITY OPERATIONS

by

Alexander Hamlyn

Bachelor of Engineering, Ryerson University, 2007

A thesis

presented to Ryerson University

in partial fulfillment of the

requirements for the degree of

Master of Applied Science

in the Program of

Electrical and Computer Engineering

Toronto, Ontario, Canada, 2008

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SYSTEM-WIDE ENHANCEMENT OF DISTRIBUTION SYSTEM VOLTAGE STABILITY OPERATIONS

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Toronto, Ontario, Canada, 2008

ABSTRACT

To take on the challenge for improving the distribution system voltage stability, this thesis research carried out an extensive study of the stability issues and available technology dealing with the stability problems. Load shedding, Load reduction through transformer tap changing, reactive power compensation, and DG control are investigated in detail. The new strategies proposed, and formulations presented, in this thesis research, are designed for carrying out the corrective actions against voltage instability with a great degree of feasibility to achieve optimal operations. A new concept of composite power was developed in this thesis research, for prediction of the trend of voltage stability, and a novel prediction of voltage stability and consequently determination of corrective actions was formulated. A detailed hardware/software based development of the algorithm and strategy for voltage stability enhancement was presented. A detailed set of case studies for verification of the voltage stability enhancement was developed.

CONTENTS

CHAPTER 1	INTRODUCTION	1
1.1	MOTIVATIONS	1
1.2	VOLTAGE STABILITY ISSUES AND RESEARCH CHALLENGES	3
1.3	REVIEW OF AVAILABLE FACILITIES FOR VOLTAGE STABILITY CONTROLS	5
1.4	TRADITIONAL APPROACH VERSUS NEW STRATEGIES FOR STABILITY CONTROLS	7
1.5	BACKGROUND INFORMATION	9
1.5.1	DISTRIBUTED GENERATIONS	9
1.5.2	VOLTAGE SAGS: PROBLEMS AND SOLUTIONS	10
1.5.3	UNDER LOAD TAP CHANGERS	12
1.5.4	REACTIVE POWER COMPENSATION	15
1.5.5	A NOVEL MONITORING AND CONTROL SCHEME	17
1.6	THESIS OVERVIEW	19
CHAPTER 2	NEW METHOD OF VOLTAGE STABILITY ENHANCEMENT AND VOLTAGE INSTABILITY CORRECTIVE ACTIONS FOR DISTRIBUTION SYSTEMS	21
2.1	BASIC VOLTAGE STABILITY CHALLENGING CONDITIONS INSTABILITY MECHANISM, AND FORMULATIONS	23
2.1.1	VOLTAGE STABILITY CONDITIONS OF A FEEDER LINE IN A RADIAL DISTRIBUTION NETWORK	24
2.1.2	TRADITIONAL PV CURVES	27
2.1.3	ILLUSTRATION OF BASIC MECHANISM FOR DEVELOPMENT OF INSTABILITY CONDITIONS	28
2.2	FORMULATION OF CORRECTIVE ACTIONS FOR VOLTAGE INSTABILITY CONDITIONS ON DISTRIBUTION FEEDER LINES	30
2.2.1	ULTC CORRECTIVE ACTIONS AT THE LOAD END OF THE FEEDER	30
2.2.2	ULTC CORRECTIVE ACTIONS AT THE SOURCE END OF THE FEEDER	31
2.2.3	RPC AT THE LOAD END OF THE FEEDER	32
2.2.4	RPC AT THE SOURCE END OF THE FEEDER	32
2.2.5	SHEDDING AT THE LOAD END OF THE FEEDER	33

2.3	NEW STRATEGIES FOR LOCALIZED VOLTAGE INSTABILITY CORRECTIVE ACTIONS	34
2.3.1	NEW STRATEGIES VERSUS TRADITIONAL APPROACH	34
2.3.2	LOAD SHEDDING FOR LOCALIZED INSTABILITY CORRECTIVE ACTION	35
2.3.3	LOAD REDUCTION THROUGH ULTC FOR LOCALIZED INSTABILITY CORRECTIVE ACTION	37
2.3.4	REACTIVE POWER COMPENSATION FOR LOCALIZED INSTABILITY CORRECTIVE ACTION	39
2.3.5	INCREASED GENERATION FROM DGS FOR LOCALIZED INSTABILITY CORRECTIVE ACTION	41
2.4	NEW STRATEGIES FOR NETWORK-WIDE VOLTAGE INSTABILITY CORRECTIVE ACTIONS	44
2.4.1	NETWORK-WIDE VERSUS LOCALIZED STRATEGIES FOR STABILITY ENHANCEMENT AND INSTABILITY CORRECTION	44
2.4.2	STRATEGIES FOR NETWORK-WIDE STABILITY ENHANCEMENT OR INSTABILITY CORRECTION	45
2.5	FORMULATIONS FOR NEW STABILITY CONTROL STRATEGIES – PART 1: COMPUTATION OF DISTRIBUTION NETWORK PERFORMANCE	48
2.5.1	FORMULATION OF SYSTEM ADMITTANCE MATRIX	48
2.5.2	FORMULATION OF NETWORK PERFORMANCE	49
2.6	FORMULATIONS FOR NEW STABILITY CONTROL STRATEGIES – PART 2: NEW COMPUTATION OF PREDICTION OF COMPOSITE POWER AND VOLTAGE STABILITY	51
2.6.1	NEW CONCEPT OF COMPOSITE POWER FOR PREDICTION OF VOLTAGE STABILITY TREND	51
2.6.2	NEW FORMULATION FOR PREDICTION OF CHANGES OF LOAD POWERS	52
2.6.3	PREDICTION OF VOLTAGE STABILITY AND DETERMINATION OF CORRECTIVE ACTIONS	53
CHAPTER 3	IMPLEMENTATION OF VOLTAGE STABILITY ENHANCEMENT AND CORRECTIVE ACTIONS FOR DISTRIBUTION SYSTEMS	55
3.1	DEVELOPMENT OF THE POWER SYSTEM DATA TEST-BED	58
3.2	DEVELOPMENT OF THE MONITORING UNITS, CONTROL UNITS AND NETWORK	61
3.3	ENABLING OF NETWORK DATA ACQUISITION AT THE VOLTAGE STABILITY ENHANCEMENT CONTROLLER	68

3.4	DEVELOPMENT OF THE LOAD-FLOW SOFTWARE	71
3.5	DEVELOPMENT OF THE VOLTAGE STABILITY ENHANCEMENT STRATEGY.....	74
CHAPTER 4	VERIFICATION OF VOLTAGE STABILITY ENHANCEMENT AND CORRECTIVE ACTIONS FOR DISTRIBUTION SYSTEMS	75
4.1	MATLAB/SIMULINK VERIFICATION	76
4.1.1	VOLTAGE INSTABILITY SCENARIOS IN SIMULINK	76
4.1.2	VERIFICATION OF PREDICTOR	83
4.2	HARDWARE VERIFICATION	87
4.2.1	THE SIMULINK-DSP INTERFACE	87
4.2.2	THE DSP-CONTROLLER INTERFACE	89
4.2.3	THE LOAD-FLOW SOFTWARE	94
4.3	COMPARISON OF PV-CURVES	99
CHAPTER 5	CONCLUSIONS	107
5.1	MAJOR RESEARCH WORK COMPLETED	108
5.2	MAJOR RESEARCH CONTRIBUTIONS	110
5.3	FUTURE WORK.....	111
	REFERENCES	113
APPENDIX A	SOURCE CODE AND SIMULATION MODEL FOR VOLTAGE STABILITY ENHANCEMENT SYSTEM.....	117
A.1	SOURCE-CODE FOR PREDICTOR PROGRAM, VOLTAGE STABILITY ANALYSIS, AND VOLTAGE STABILITY CORRECTIVE ACTIONS.....	117
A.2	SOURCE-CODE/DIAGRAMS FOR MATLAB-TO-DSP COMMUNICATION.....	125
A.3	SOURCE-CODE/DIAGRAMS FOR DSP-TO-CONTROLLER COMMUNICATION.....	129
A.4	SOURCE-CODE/DIAGRAMS FOR LOAD-FLOW SOFTWARE.....	139

LIST OF FIGURES

Figure 1-1: Traditional PV curves	7
Figure 1-2: One-line diagram illustrating the Power System Structure.....	10
Figure 1-3: Circuit for illustrating Voltage Sags	12
Figure 1-4: Variable Transformer Action Illustration	13
Figure 1-5: Benefit of ULTC Action	14
Figure 1-6 Typical SVC System	17
Figure 2-1: A single load connected at the end of a feeder line	25
Figure 2-2: Traditional PV curves	27
Figure 2-3: Illustration of basic mechanism involved in development of instability conditions.....	29
Figure 2-4: ULTC corrective actions	31
Figure 2-5: RPC corrective actions	33
Figure 2-6: Illustration of instability corrective action using load shedding	37
Figure 2-7: Illustration of instability corrective action using ULTC load reduction	39
Figure 2-8: Illustration of instability corrective action using RPC	41
Figure 2-9: Illustration of instability corrective action using DG.....	43
Figure 2-10: Regions of stability conditions.....	47
Figure 3-1: IEEE 30-Bus Test System Implemented in SIMULINK	60
Figure 3-2: RTDX Library Initialization and Data Acquisition	61
Figure 3-3: Voltage Magnitude Computation Routine	62
Figure 3-4: Computation of Three-Phase Voltages and Currents	63
Figure 3-5: DSignT DSK91C111 Ethernet Daughter-Card.....	63
Figure 3-6: Connection of DSK91C111 Ethernet Card and 6416T DSK Board	64
Figure 3-7: DSP Configuration Code for Networking	65
Figure 3-8: Auto-Negotiation Subroutine	66
Figure 3-9: Network Request Handling Routine	66
Figure 3-10: Network Interface Configuration Using Winsock API	69
Figure 3-11: Subroutine for handling Network Requests	70

Figure 3-12: Checking Convergence of the Active Power Vector	71
Figure 3-13: Checking Convergence of the Reactive Power Vector.....	72
Figure 3-14: maxVector Routine	73
Figure 3-15: MATLAB program for computation of future bus loading	74
Figure 4-1: One-line diagram of the IEEE 30-bus Test System	76
Figure 4-2: Voltage at Bus 19 is acceptable, but is decreasing slightly due to a slow increase in loading.....	79
Figure 4-3: Voltage at Bus 19 drops below -5% tolerance limit due to slow increase of loading, load shedding action is taken.....	80
Figure 4-4: Voltage Profile at Bus 19 during a contingency and the resulting voltage instability	81
Figure 4-5: Heavy load and static-var compensator actions.....	82
Figure 4-6: ULTC action and load shedding	83
Figure 4-7: Measured and predicted power for	
$P = 0.5 + 0.00001*t + 0.01*\sin(0.01*t)$	84
Figure 4-8: Measured and predicted power for	
$P = 0.5 + 0.00001*t + 0.01*\sin(0.01*t)$	85
Figure 4-9: Response during a sudden rapid drop in loading	86
Figure 4-10: A Photograph of the DSP to Host-PC interface.....	88
Figure 4-11: Real-Time measurements of Bus 19 Voltage, from Code-Composer Studio	88
Figure 4-12: Real-Time measurements of Bus 19 Voltage, from SIMULINK	89
Figure 4-13: Output from centralized processor	93
Figure 4-14: Load-Flow Program Output.....	95
Figure 4-15: PSAT Model of the Modified 30-Bus Test System	96
Figure 4-16: One-Line Diagram for PV Curve Comparison	100
Figure 4-17: Standard PV Curve for Line Connecting Bus 19 and Bus 20.....	100
Figure 4-18: One-Line Diagram Illustrating ULTC Placement.....	101
Figure 4-19: PV Curve With ULTC on Load Side.....	102
Figure 4-20: PV Curve with ULTC on Source Side.....	103
Figure 4-21: One-Line Diagram Illustrating RPC Placement	104
Figure 4-22: PV Curves with RPC on the Load Side	105
Figure 4-23: PV Curves with RPC on the Source Side	106
Figure A1-1: Source Code For Predictor Program in Figure 4-7	117
Figure A1-2: Source Code for Predictor Program in Figure 4-8	118

Figure A1-3: Source Code For Predictor Program in Figure 4-9	119
Figure A1-4: Source Code for Standard PV Curve Generation	120
Figure A1-5: Source Code for PV Curve Generation with ULTC on Load Side	121
Figure A1-6: Source Code for PV Curve Generation with ULTC on Source Side ...	122
Figure A1-7: Source Code for PV Curve Generation with RPC on Load Side.....	123
Figure A1-8: Source Code for PV Curve Generation with RPC on Source Side	124
Figure A2-1: Source Code for execute_CCS.m file	125
Figure A2-2: Source Code for initialization.m	126
Figure A2-3: Source Code for simcont_dsp.m	126
Figure A2-4: SIMULINK Block Diagram for bus30_dsp.mdl.....	127
Figure A2-5: DSP Source Code for RTDX Data Acquisition	128
Figure A3-1: Source Code for execute_CCS.m file	129
Figure A3-2: Source Code for initialization.m	130
Figure A3-3: Source Code for simcont_dsp.m	130
Figure A3-4: SIMULINK Diagram	131
Figure A3-5: DSP Source Code for DSP-to-Controller Communication	135
Figure A3-6: Source Code for Controller Program	138
Figure A4-1: Source Code for Load Flow Program	143
Figure A4-2: SIMULINK PSAT Block Diagram for Verification.....	144

CHAPTER 1

INTRODUCTION

1.1 MOTIVATIONS

Recently, electricity utilities have been under tremendous pressure from their governments as well as the public to allow connections of distributed generators (DGs), powered by renewable energy resources such as wind and sunlight, to their existing distribution systems. This pressure has compelled utilities to search for solutions to the technical issues caused by allowing the connection of DGs to their distribution grids [1, 2, 3, 4, 5].

It is obvious that DGs has a major benefit of providing an additional source of electrical power for the industrial and public uses, and this source of energy is environment-friendly if the DGs are powered from renewable resources. This benefit is definitely very welcome at the present time of energy tightness and the future of foreseeable energy crises. It is also obvious that DGs, being a relative new equipment of the power systems or a new member of the electricity generation utilities, brings in a fair amount of uncertainty and concerns to the utilities particularly in the operation aspects because the DGs have to connect to and operate simultaneously with the power systems. Activities in several recent large IEEE conferences have shown significant concerns from the utilities and research institutes. The questions of "Is DG an enemy or a friend from the distribution system operation

perceptively?” and “Is DG a threat or an assistance to the distribution network operations?” as well as the interest and excitement of finding the answers start motivating this thesis research.

As this thesis research proceeds to find answers, with a focus on the distribution system operation stability, several key technical difficulties and challenges have been encountered and then overcome, and finally the DG is turned into a “friend” that assists to enhance the distribution system stability, after key technical issues have been overcome by this thesis research.

This thesis research then diverged to the investigation of a generic distribution operation issue on voltage stability. Through voltage stability issue is not new and in fact it has been studied for a few decades and many solutions are known, the practices however are often too costly and too much adverse impact on the quality of service to the users because of cutting off the electricity supply too much and too often [6, 7]. The challenge of finding a better and more effective solution to this already intensively studied stability issue is tremendous. The excitement of attempting to overcome this challenge turns into the main motivation of this thesis research.

1.2 VOLTAGE STABILITY ISSUES AND RESEARCH CHALLENGES

The section introduces the issues of voltage stability in the distribution system as the demand for “quality” supplies of electricity is continuously increasing in today’s hi-tech world that could not tolerate any substantial interruption of electricity supply due to operation problems such as voltage stability issues [6].

The challenge, that this thesis research has been facing, for finding a better and more effective control of voltage stability in the distribution system is tremendous, because voltage stability has been continuously studied for a few decades and many sound solutions have been proposed and some are used in daily operations. In addition, power distribution system is one of the key infrastructures of a country and the reliability of its operation is paramount. Any initiation, change of practices, or new development in distribution system operation must respect the practical environment and restrictions. Otherwise, a minor overlook in the small change of operations, such as for implementing a new voltage stability control algorithm, if not satisfying all practical limitations and restrictions, could jeopardize electricity supply to customers, and consequently could cause tremendous financial lost.

To take on the challenge for improving the distribution system voltage stability, this thesis research carried out an extensive study of the stability issues and available technology dealing with the stability problems. It is astonishing to realize that so many good techniques and equipments have been developed for the control of power system stability at the high-voltage transmission level. At the same time, it is quite surprising to find out that the voltage stability control in the distribution system level has not progressed as much. Even though sound practices have been established. These practices however may be too costly and have

too much adverse impacts on the quality of service to the users because of cutting off the electricity supply too much and too often.

To explain this phenomenon, a brief concluding remark is drawn from this thesis extensive study as follows. First, the transmission system handling bulk power cannot tolerate any substantial instability without causing tremendous financial lost and adverse impacts of many aspects in our society that draws much more efforts for both research and engineering to address the stability issues. Second, the transmission networks are equipped with much more controlling devices per line than the distribution networks, and the transmission lines and transformers impedances are lower than the distribution impedances, therefore the stability issues on the transmission level are better controlled. Furthermore, connections of recently developed DGs of relatively unfamiliar operating characteristics on the distribution network cause an impression of adding difficulty to the control of distribution system voltage stability [8].

The above-mentioned information of revealing insufficient existing practices actually provides a great opportunity for this thesis work to carry out research and development in the area of voltage stability enhancement as well as instability corrective actions in the distribution network with or without DGs connections. However, this area of research and development does not provide as much freedom as other engineering fields due to the practical environment and restrictions as the distribution systems being one of the key infrastructures of the country. On the other hand, lots of sound practices exist in the systems and it is strongly recommended to learn them first prior to creating new ones, as does this thesis research.

1.3 REVIEW OF AVAILABLE FACILITIES FOR VOLTAGE STABILITY CONTROLS

Though areas of improvement have been identified in this thesis, there are many sound practices that exist in the distribution system and some are being used in the daily operations. The typical ones are load shedding, load reduction through transformer tap changing, reactive power compensation.

Load shedding: This means cutting off the load that is obvious to be capable of restoring the voltage stability fast and effectively. However the load shedding can cause adverse impact on the quality of customer service, and is recommended as the last resort for restoring the instability conditions.

Load reduction through transformer tap changing: This means reducing the load voltage that is effective for impedance loads by reducing the load voltage to reduce the load power burden on the feeder as power versus square of voltage. However, this reduction is not effective for the constant power type of loads, of which the reduction of voltage causes correspondingly an increase of current, resulting in no release of power burden on the feeder.

Reactive power compensation: This means adding capacitors, that is effective for loads of low power factor and the compensator provides reactive power to reduce the reactive power demand from the load. However, this compensation is not effective for load of close to unity power factor such as the residential loads and the compensation is limited by the availability of capacitor banks connected on the system.

The above provides a comprehensive view of the available sound methods of voltage stability control. These methods will be adopted by this thesis. In attempt to make contributions to voltage stability, this thesis is focused on: how to best use these methods but

avoiding or reducing the impact of their limitations, how to determine the amount of load shedding, transformer load reduction, and reactive compensation to avoid over-compensation and reduce impact on the customer loads, where to apply the facilities if they are available in more than one locations, what are the possible effects on other loads while improving the voltage stability of the feeder node of interest, when to apply the facilities, etc.

1.4 TRADITIONAL APPROACH VERSUS NEW STRATEGIES FOR STABILITY CONTROLS

The traditional approach to voltage stability can be typically represented by the well-known PV curves, of which the power P is restricted to the power of the load connected to a feeder node where the voltage stability is under investigations due to its critical location, or concerns being caused. This restriction severely limits the operational feasibility of corrective actions [6,9]. For example, the load can be shedded/cut not on the feeder location under investigation, but on the neighboring circuit or on circuits upstream or downstream. This would be most likely the situation where the voltage stability of the critical loads are of interest and need to be monitored and controlled, but they cannot be cut without serious consequences. The traditional approach could not handle these conditions.

Figure 1-1: Traditional PV curves

The new strategies, proposed in this thesis research, are designed for carrying out the corrective actions against voltage instability with a great degree of feasibility to achieve optimal operations. In particular, the new strategies expand the traditional concept significantly, for example, by defining the power P as a *composite power* including all neighboring load powers that influencing the voltage stability of the feeder location under investigation.

However, credits should be given to the creation of these PV curve. The curves in Figure 1.1 are sketched merely to show conceptually the basic relationship of the feeder line voltage at the location where the load is connected versus the amount of power drained by the load from the feeder line. The top part of the curves with negative slope is the stable region of operation, and the following discussion is referred to this part. It is obvious that as the load power increases, the feeder/load voltage drops. Also when there is a contingency occurring on the distribution system, the effective PV curve will reduce with small maximum power available to the load, i.e. the curves of smaller size and more to the left. As the contingency is usually due to loss of a line, a transformer, etc. this increases the equivalent impedance of the source and makes the curves less horizontal that means for the same load power drawn from the feeder, the voltage drop is relatively more [10].

1.5 BACKGROUND INFORMATION

1.5.1 DISTRIBUTED GENERATIONS

Chapter 2 outlines the strategies of using DG for enhancing the voltage stability of distribution systems, instead of a common impression that DG is bad for power system stability, if proper use of DG is implemented according to the new strategy proposed in Chapter 2. The following provides information about this newly available resource of power.

Electricity utilities, like Ontario Hydro the previous province-wide sole electricity utility in Ontario of Canada, have been under tremendous pressure, from governments to deregulate their control of electricity supplies. The traditional large-size utility was responsible for the generation, transmission, distribution and sale of electricity. This type of utility was monopolistic, and was recently discouraged by the governments [11]. As a result of drives from the governments, utilities of monopolized enterprise were forced to split into several smaller companies. For example, Ontario Hydro was split into Ontario Power Generation (OPG) and Hydro One, of which OPG handles generation and Hydro One handles transmission and several distributions. The sale of electricity is managed by the so-called Independent Market Operator (IMO). Only generation, distribution, and sale of electrical energy can make a profit, and transmission is run by the government-operated utility, with the goal of minimizing cost, not maximizing profits [11]. Under this new deregulated environment, generation can be preformed with a profit by other companies, independent of the transmission and distribution companies. This greatly improves the appeal of distributed generations (DGs).

1.5.2 VOLTAGE SAGS: PROBLEMS AND SOLUTIONS

To recognize the voltage sag problem in distribution systems, we must first clearly understand the power system's physical structure. A diagram illustrating the typical structure is shown in Figure 1-2 [12]. At the top of the figure is a centralized generating station that produces bulk electrical power at the 10's of kV level. This electrical power is stepped up to the transmission level of 100's of kV for energy-efficient transmission over long distances. The power is then stepped-down to the sub-transmission level of around 100kV in a switchyard. Through the sub-transmission system, the power is further stepped down at a substation, where it is converted to lower voltage levels of 10's of kV, before finally being stepped down to the service entry levels of 600V or 208V, the typical voltages for end uses in North America [12, 13].

Figure 1-2: One-line diagram illustrating the Power System Structure

With an understanding of the power system structure, we can now describe the voltage sag phenomena using a simple electric circuit with an equivalent circuit representation of the power system, as shown in Figure 1-3 [6]. First, it is noted that this circuit is a one-line diagram representation of a power system. In other words, it represents just one phase of the

typical 3-phase electric power systems. Also, it is noted that the per-unit system is adopted to simplify the analysis, whereby an impedance of $R+jX$ and a voltage source E represent the total impedance and the source of the power supplies from the generation, transmission, and distribution systems. With respect to Figure 1-3, voltage V at the load can simply be expressed as:

$$\bar{V} = \bar{E} - (R + jX)\bar{I} \quad (1-1)$$

Also P and Q represent the active and reactive load demands at the service level, respectively. We can now derive V as a function of P , Q , R , X and E as [6]:

$$V = \sqrt{E^2/2 - QX} + \sqrt{E^4/4 - X^2P^2 - XE^2Q} \quad (1-2)$$

This expression shows that if either P or Q increases, the voltage decreases. Alternatively, we could say that as the load demand increases, then the current supplying the load increased, then the voltage drop across the equivalent impedance also increases, which makes the voltage at the service level decreases. In other words, as the load, either real or reactive power, increases, the service level voltage decreases. This consequently results in voltage sag at the load that could cause tremendous application problems and associated costs. The voltage drop across the system equivalent impedance is unavoidable, but the voltage sag at the load has to be avoided, eliminated, or effectively controlled, in order to maintain high quality of power supplied to the utility customers.

Figure 1-3: Circuit for illustrating Voltage Sags

Continuously using the very simple equivalent circuit of Figure 1-3, we can illustrate some possible solutions to the voltage sag problem, explain which ones are feasible, and how the system presented in this thesis can enhance the feasible solutions for maintaining the desired “constant” service-level voltage.

The first, and the most intuitive option for increasing V is to increase E . This is evident from (1-1), that when E increases, V increases as well. However, increase of E could have a significant drawback. First, increasing E will result in all voltages throughout the power system increasing, including those at the transformer terminals and transmission lines. It has been shown in [13] that increasing the terminal voltage of a transformer requires a significant increase in insulating material, which increases both the cost and size of transformer. Similarly, increasing the voltage level of a transmission line will require greater ground clearance, wire clearance, and more insulating material at the wire-tower interface.

1.5.3 UNDER LOAD TAP CHANGERS

A second option for increasing V is to adjust taps of the transformer supplying the load at the distribution substation. This is commonly referred as Under-Load Tap-Changers

(ULTCs). This adjustment in fact effectively decreases the system equivalent impedance $R+jX$, and therefore with the same system equivalent voltage E , the service-level voltage V could be maintained constant even during the period of heavy load. Figures 1-4 and 1-5 will be utilized to explain the ULTC's action. The tap-changing transformer operates by rotating the mechanism in the right side of Figure 1-4 to connect the various internal terminals. For example, rotating the mechanism in Figure 1-4 from an initial connection 1-2 to connection 2-3 will result in a larger turns ratio.

Figure 1-4: Variable Transformer Action Illustration

Figure 1-5 is now used to illustrate how a tap-changing transformer can be used to improve voltage sags. Reflecting E , R and X , to the load side of the transformer as:

$$E' = \frac{E}{r}, R' = \frac{R}{r^2}, X' = \frac{X}{r^2} \quad (1-3)$$

Substituting (1-3) into (1-1) results in the following expression:

$$V = \sqrt{E^2/2r^2 - Q\frac{X}{r}} + \sqrt{E^4/4r^4 - \left(\frac{X}{r}\right)^2 P^2 - \frac{X}{r^3} E^2 Q} \quad (1-4)$$

From this expression, it is clear that as r decreases, then V increases, thus illustrating how tap-changing transformers can be utilized to implement a ULTC, with the goal of maintaining V , the voltage at the load constant.

Figure 1-5: Benefit of ULTC Action

ULTCs have been utilized by utilities for many years to adjust the distribution system voltage, and thus the service level voltage. However, they do have a number of limitations. First, ULTCs have an adjustment limit. In other words, there is a maximum and minimum turns ratio that the ULTC can operate between. Therefore, if the load is particularly heavy at a given time, then $r_{\min}$ may not be small enough to support the nominal voltage at the service level. The minimum turns ratio for a transformer is part of the manufacturer design considering the current that the transformer can handle. Second, ULTCs are in general slow-acting equipment, in that they may take many seconds to make a transformer adjustment, and each adjustment results in a voltage change of about 0.5% [9].

In the existing power distribution control, most of the time for transformer adjustment is required for determining whether the ULTC should be operated and how many taps should be moved based on the system information processed from measurements as well as the decisions of the human operators. Therefore, when the load is increasing rapidly, ULTCs will

be insufficient to maintain a stable voltage. The monitoring and control system developed in this thesis will drastically improve the effectiveness of ULTC adjustments through a powerful prediction and control mechanism operating in full automatic high-speed digital signal processing environment, without the need of any assistance from human operators.

1.5.4 REACTIVE POWER COMPENSATION

Another major tool that can be employed in the battle against rapidly developing voltage sags is the compensation device. Compensation devices take on two broad forms, the series and shunt forms, whereby the device is connected in series with the transmission line, or alternatively, in shunt with the system buses. The series compensation devices serve to reduce the effective reactance of the transmission, sub-transmission, and distribution circuits. In contrast, the shunt compensation device serves to supply some or all of the reactive load demand, which is equivalent to saying that some of the reactive load demand is met locally, rather than being supplied by the centralized generator shown in Figure 1-3. This is beneficial to the load voltage profile, because some or all of the reactive power does not have to travel through the generation, transmission and distribution equipments, resulting in a lower voltage drop across the system, and thus a higher voltage at the distribution and service levels.

Series compensation devices are usually capacitors that are permanently installed on the transmission and distribution towers, so that there is little that can be done from a control perspective to improve distribution system operations using these devices [14]. This obviously results in a limitation in maintaining constant voltage for a dynamic load environment. The most practical difficulty imposed by series compensation is the protection

of the compensating devices during faults on the load side of the devices, and proper short circuit mechanism must be implemented for preventing any damage of the devices.

The shunt compensation offers more opportunities for better voltage regulations, particularly during conditions of dynamic load changing with fast and wide variations, or when the requirements for voltage regulations are very strict for certain critical and sensitive loads. This thesis is therefore focused on the optimal controls of shunt compensation devices. Now a brief comparison of the different shunt compensation technologies is presented. The simplest shunt compensation technology is the one using switched capacitors. The Bushing is utilized to connect the capacitor bank to the distribution system, the discharge resistor is used to discharge the capacitor when the capacitor bank is disconnected for maintenance, etc. In the implementation of shunt compensation, silicon-controlled rectifiers (SCRs) are usually used as switches to connect or disconnect shunt capacitors from the utility distribution circuit at the point of coupling.

The switched capacitor implementation has the advantage of being the simplest to control, i.e., a change of capacitance can be achieved by opening or closing the SCR switches. However, the switched capacitor can only provide capacitance in discrete amounts (either on or off). Also, switched capacitors are operated fairly infrequently, and are thus not tailored to rapidly changing load characteristics. A more modern approach to shunt compensation is using power electronic-based Flexible Alternating Current Transmission Systems (FACTS) devices. These compensation devices, referred to in the literature as Static Compensators (STATCOM) typically feature a DC capacitor and energy storage device (battery), connected to a three-phase inverter, where the gating signals of the inverter are varied to create a variable capacitor as seen from the AC side. The device is connected to a step-up

transformer, which allows the inverter and capacitor to be rated at a lower voltage level. A schematic of STATCOM is shown in Figure 1-6 [15].

Figure 1-6 Typical SVC System

1.5.5 A NOVEL MONITORING AND CONTROL SCHEME

The goal of this thesis is to develop a novel monitoring and control scheme, that employs state-of-the-art DSP technology, in conjunction with high-speed computer networking technology [16, 17, 18]. This system will be utilized for improving and maintaining a stable voltage profile and system frequency, in power distribution systems that feature dispersed generations.

The system will feature a monitoring architecture that monitors the voltage, current, active power and reactive power at all major distribution system buses. This information will be available to all networked devices in the system through a secure Ethernet-based TCP/IP computer network, which is robust and constructed using inexpensive off-the-shelf hardware, and thoroughly tested software.

In terms of improving distribution system operations, the proposed system will utilize a first-of-its-kind prediction scheme, to compute the optimal control parameters for all DGs, compensation devices, and ULTCs connected in the distribution system. The prediction scheme utilizes industry-proven analysis techniques to provide accurate predictions of the voltage profile at all system buses, based upon global measurements, and collected measurement data.

1.6 THESIS OVERVIEW

This thesis consists of five chapters. The following provides an overview of the remaining chapters.

Chapter 2 First, present basic voltage stability challenging conditions and instability mechanism. Second, present formulation of corrective actions for voltage instability conditions on distribution feeder lines. Third, present new strategies for carrying out corrective actions to improve the voltage stability margin for stable network conditions, to maintain stability for the network conditions prone to instability, or to restore stability for unstable network conditions. Fourth, present new strategies for carrying out network-wide voltage instability corrective actions and network-wide voltage stability enhancement. Fifth present formulations for computation of distribution network performance. Sixth, presents a new concept of composite power for prediction of the trend of voltage stability at the feeder node of interest, and present new computation of prediction of composite power and voltage stability.

Chapter 3 First, present the development of a test-bed to generate the real-time power-system data, by accurate simulation of the real-time performance of a modern power system. Second, presents the development of the hardware, and software monitoring network, including the DSP-based measurement units, and the network infrastructure to support network-enabled monitoring of power system voltage, current and, active and reactive demand. Third, present the development of the software for acquiring data from the monitoring, and system configuration/control networks, for the voltage stability enhancement

strategy. Fourth, present the development of a load-flow software to enable the prediction functions. Fifth, present the development of the prediction software. This function requires the processing of vast amounts of data.

Chapter 4 First, present verification in the MATLAB/SIMULINK test bed. Second, presents the hardware verifications. Third present the verification of the comparison of the PV curves.

Chapter 5 First, present the conclusion of this thesis research. Second, summarize major tasks accomplished in this thesis research. Third, list the major contributions from this thesis research. Fourth, recommend future work in this thesis research area.

CHAPTER 2

NEW METHOD OF VOLTAGE STABILITY ENHANCEMENT AND VOLTAGE INSTABILITY CORRECTIVE ACTIONS FOR DISTRIBUTION SYSTEMS

This chapter presents a new concept and a new method for voltage stability enhancement and voltage instability corrective actions for distribution systems with or without connections of distribution generators (DGs). First this chapter reviews the basic principle and mechanism of voltage stability in the distribution system. Second, this chapter reviews all the technologies available for the control of voltage stability in a distribution system. Third, this chapter identifies the weakness or insufficiencies of existing technologies. Fourth, this chapter proposes a new method for enhancement of distribution system voltage stability. Finally and most importantly, this chapter presents the formulation of the new method.

The following lists the sections in this chapter:

- Section 2.1 presents basic voltage stability challenging conditions, instability mechanism, and formulations.
- Section 2.2 presents formulation of corrective actions for voltage instability conditions on distribution feeder lines.

- Section 2.3 presents new strategies for carrying out corrective actions to improve the voltage stability margin for stable network conditions, to maintain stability for the network conditions prone to instability, or to restore stability for unstable network conditions.
- Section 2.4 presents new strategies for carrying out network-wide voltage instability corrective actions and network-wide voltage stability enhancement.
- Section 2.5 presents formulations for new stability control strategies – Part 1: Computation of distribution network performance.
- Section 2.6 presents a new concept of composite power for prediction of the trend of voltage stability at the feeder node of interest, and presents formulations for new stability control strategies – Part 2: New computation of prediction of composite power and voltage stability.

2.1 BASIC VOLTAGE STABILITY CHALLENGING CONDITIONS, INSTABILITY MECHANISM, AND FORMULATIONS

This section describes the basic voltage stability challenging conditions, the elementary formulation for stability studies, the elemental mechanism involved in general voltage instability conditions, and the basic traditional corrective actions for voltage instability in the utility power distribution systems.

This thesis research identifies challenging conditions for maintaining voltage stability in the distribution network and defines the focus of voltage instability investigations. Basically, the stability challenging conditions can be identified from several points of view, typically from the practical networks and operations standpoint, from standard recommended practices judgment, from the customer quality services perspective, or even from political impacts viewpoint. Each challenging condition may impose specific technical obscurity in addition to general technical difficulty that needs to be conquered in order to maintain voltage stability if the network condition is prone to instability or to restore voltage stability if the network condition is unstable. For example, from the practical network and operations standpoint, it would be fairly challenging to maintain good voltage stability condition at the end of a long weak line connected to a big single load with randomly switching in/out operations, without imposing adverse effects on the source end of the line by certain stability corrective actions.

The following presents a typical voltage stability condition and its formulation, the well-known PV curves, illustration of basic mechanism for development of instability conditions, and four typical corrective actions.

2.1.1 VOLTAGE STABILITY CONDITIONS OF A FEEDER LINE IN A RADIAL DISTRIBUTION NETWORK

This section describes the voltage stability conditions at the end of a feeder line in a traditional radial distribution network. This condition is used to illustrate the basic mechanism involved in the formation of voltage instability condition in a distribution network. In the following, the condition is formulated, and then analyzed. In the literature, this limit is also referred to as the loadability limit [19].

a) Formulate the condition for voltage stability study

Figure 2-1 shows a single load connected at the end of a feeder line. This figure also shows an equivalent circuit. The voltage $\bar{V}_L$ at the feeder end can be expressed as:

$$\bar{V}_L = \bar{V}_S - j(X_S + X_F)\bar{I}_L \quad (2-1)$$

where the source voltage $\bar{V}_S$ and source impedance jX_S is the equivalent circuit of the distribution network, jX_F is the feeder impedance, and $\bar{I}_L$ is the load current.

Figure 2-1: A single load connected at the end of a feeder line

Assuming $\bar{V}_S = V_S \angle 0^\circ$, $\bar{V}_L = V_L \angle -\theta$, and $X = X_S + X_F$, the active power P_L and the reactive power Q_L absorbed by the load can be expressed as:

$$P_L + jQ_L = \bar{V}_L \cdot \bar{I}_L^* = \bar{V}_L \cdot \frac{\bar{V}_S^* - \bar{V}_L^*}{jX} \quad (2-2)$$

$$\therefore P_L + jQ_L = \frac{j}{X} (V_S V_L \cos \theta - j V_S V_L \sin \theta - V_L^2)$$

Therefore, the load active power P_L and reactive power Q_L are:

$$P_L = \frac{V_S V_L}{X} \sin \theta \text{ and } Q_L = -\frac{V_L^2}{X} + \frac{V_S V_L}{X} \cos \theta \quad (2-3)$$

Eliminating θ in (2-3) gives:

$$(V_L^2)^2 + (2Q_L X - V_S^2)(V_L^2) + X^2(P_L^2 + Q_L^2) = 0 \quad (2-4)$$

The condition for (2-4) to have a solution is:

$$(2Q_L X - V_S^2)^2 - 4X^2(P_L^2 + Q_L^2) \geq 0$$

$$\therefore P_L^2 + \frac{V_S^2}{X} Q_L - \frac{V_S^4}{4X^2} \leq 0 \quad (2-5)$$

The equality of (2-5) defines the locus of all maximum power points.

Assuming that (2-5) is satisfied, the voltage at the load can be expressed as:

$$V_L = \sqrt{\frac{V_S^2}{2} - Q_L X \pm \sqrt{\frac{V_S^4}{4} - X^2 P_L^2 - X V_S^2 Q_L}} \quad (2-6)$$

$$\therefore V_L = \sqrt{\frac{V_S^2}{2} - Q_L (X_S + X_F) \pm \sqrt{\frac{V_S^4}{4} - (X_S + X_F)^2 P_L^2 - (X_S + X_F) V_S^2 Q_L}}$$

b) Analyze the voltage stability condition

It is obvious from (2-6) that if either the active power P_L or the reactive power Q_L of the load increases, the load voltage V_L decreases. Also, the longer the feeder line, that is the higher the line impedance X_F , the lower the load voltage V_L becomes.

A voltage instability condition would be formed at the load or at the end of the feeder line when the active power P_L and the reactive power Q_L of the load increase so much that causes a substantial decrease of the load voltage V_L beyond an acceptable minimum level. Equation (2-6) shows that the reactive power Q_L of the load has much higher influential impact on the drop of the load voltage V_L resulting in a voltage instability condition.

It is obvious as shown in (2-6) that if the source impedance X_S and the feeder line impedance X_F are zero, then the load voltage $\bar{V}_L$ is the same as the source voltage $\bar{V}_S$ that is usually controlled very well, and therefore there is no voltage stability problem. However, this is not practically possible. The smaller the source impedance X_S and feeder line impedance X_F , the higher the cost to build the distribution system.

2.1.2 TRADITIONAL PV CURVES

Figure 2-2 shows the traditional graph of the PV curves that are sketched, according to the relationship of the load voltage $\bar{V}_L$ and the load power $\bar{S}_L = \bar{P}_L + jQ_L$ as given in (2-6). Each curve is drawn for the load voltage $\bar{V}_L$ versus the load active power

P_L with a selected ratio defined as $\tan \phi = \frac{Q_L}{P_L}$ (2-7)

Figure 2-2: Traditional PV curves

The curves in Figure 2.2 are sketched merely to show conceptually the basic relationship of the feeder line voltage at the location where the load is connected versus the amount of power drained by the load from the feeder line. This is a simple conceptual display of (2-6), of which it is obvious that as the load power increases, the feeder/load voltage drops.

2.1.3 ILLUSTRATION OF BASIC MECHANISM FOR DEVELOPMENT OF INSTABILITY CONDITIONS

Figure 2.3 is provided to illustrate the basic mechanism for the development of an instability condition in the distribution network, after a contingency has occurred in the network. This figure shows that under a normal distribution network operation condition, the operating point of a feeder node of interest is at point *A* that is the intersection point of the load characteristic *curve 1* and the pre-contingency network power-voltage PV *curve 2*. At point *A*, the voltage of the feeder node is V_A and the power supplied by the feeder to its load is P_A .

When a contingency occurs, the network PV curve changes to *curve 3*. This curve shows that the maximum power that can be supplied by the distribution network is P_{max} , as shown in Figure 2-3. During the contingency, the operating point of the feeder node moves from point *A* to point *B*. Afterwards, whether the operating point will stay or move depends on the characteristics of the load. There are two possible cases.

Case 1: For the load of impedance type represented by *curve 1*, the operating point will not move any more but stay at point *B*. The feeder node voltage at this operating point is V_B . Whether there is an instability condition will depend on the limit of the stability tolerance set for that feeder node, and this limit setting is dependent on the application. If the value of V_B is lower than the minimum limit of stability tolerance, then an instability condition will be established if no corrective action is taken.

Case 2: For the load of constant power type that tries to maintain constant output power (i.e. P_A shown in Figure 2-3), the operating point continuously moves from point *B*

downward along the post-contingency network PV curve, because the post-contingency maximum-available power P_{max} is less than the pre-contingency load power P_A . As a consequence, the voltage of the feeder node will pass point M and continue downwards and collapse because the demand power by the load P_A is greater than the post-contingency maximum-available power P_{max} . In this case, it is obvious that an instability condition is established, if no corrective action is taken.

Figure 2-3: Illustration of basic mechanism involved in development of instability conditions [20]

The basic corrective actions for improving a distribution feeder voltage stability condition or restoring stability from an instability condition, after a contingency occurred in the distribution network are: load shedding, load reduction through under load tap changing (ULTC) operation, reactive power compensation (RPC), and newly available distributed generation (DG). These actions are discussed in the following sections.

2.2 FORMULATION OF CORRECTIVE ACTIONS FOR VOLTAGE INSTABILITY CONDITIONS ON DISTRIBUTION FEEDER LINES

This section presents three common corrective actions (i.e. ULTC, RPC, and load shedding) for restoring voltage stability from an instability conditions on a long feeder. The following presentation assumes that these corrective actions are available in the location of the voltage instability conditions, and the distribution network can be modeled using an equivalent circuit with a constant source of voltage $\bar{V}_s$ and a constant impedance of reactance jX_s . The use of this equivalent circuit is for simplicity in expression the basic concept of voltage stability. However, the suitability of this equivalent circuit for voltage stability study, and consequently for corrective actions, will be discussed.

2.2.1 ULTC CORRECTIVE ACTIONS AT THE LOAD END OF THE FEEDER

The following carries out the formulation for the ULTC voltage instability corrective action. If an ULTC is available at the end of the feeder, as shown in Figure 2-4(a), and the turns ratio of the ULTC is 1:n, then the circuit condition can be formulated as follows:

$$\begin{aligned}\bar{V}_s &= \frac{\bar{V}_L}{n} + j(X_s + X_F)n\bar{I}_L \Rightarrow n\bar{V}_s = \bar{V}_L + jn^2(X_s + X_F)\bar{I}_L \\ \therefore \bar{V}_L &= n\bar{V}_s - jn^2(X_s + X_F)\bar{I}_L\end{aligned}\quad (2-8)$$

Comparison of (2-8) with (2-1) shows that if $n\bar{V}_s$ replaces $\bar{V}_s$, and $jn^2(X_s + X_F)$ replaces $jX_s + jX_F$ in (2-6). Then the voltage at the feeder end can be expressed as:

$$V_L = \sqrt{\frac{(nV_s)^2}{2} - Q_L n^2 (X_s + X_F) \pm \sqrt{\frac{(nV_s)^4}{4} - (n^2 (X_s + X_F))^2 P_L^2 - n^2 (X_s + X_F) (nV_s)^2 Q_L}} \quad (2-9)$$

2.2.2 ULTC corrective actions at the source end of the feeder

If a ULTC is available at the source end of the feeder, as shown in Figure 2-4(b), then the circuit condition can be formulated as follows:

$$\begin{aligned} \bar{V}_s &= \frac{\bar{V}_L + jX_F \bar{I}_L}{n} + jX_s n \bar{I}_L \Rightarrow n \bar{V}_s = \bar{V}_L + j(n^2 X_s + X_F) \bar{I}_L \\ \therefore \bar{V}_L &= n \bar{V}_s - j(n^2 X_s + X_F) \bar{I}_L \end{aligned} \quad (2-10)$$

Comparison of (2-10) with (2-1) shows that if $n \bar{V}_s$ replaces $\bar{V}_s$, and $n^2 X_s + X_F$ replaces $X_s + X_F$ in (2-6). Then the voltage at the feeder end can be expressed as:

$$V_L = \sqrt{\frac{(nV_s)^2}{2} - Q_L (n^2 X_s + X_F) \pm \sqrt{\frac{(nV_s)^4}{4} - (n^2 X_s + X_F)^2 P_L^2 - (n^2 X_s + X_F) (nV_s)^2 Q_L}} \quad (2-11)$$

Figure 2-4: ULTC corrective actions

2.2.3 RPC AT THE LOAD END OF THE FEEDER

If a RPC is available at the load end of the feeder to carry out the voltage instability corrective action, as shown in Figure 2-5(a), then the circuit condition can be formulated as follows:

$$\bar{S}_C = jQ_C = \bar{V}_L \bar{I}_C^* = \bar{V}_L \left(\frac{\bar{V}_L}{1/jX_C} \right)^* = \bar{V}_L (jX_C \bar{V}_L)^* = -jX_C V_L^2 \Rightarrow Q_C = -X_C V_L^2 \quad (2-12)$$

Substituting (2-12) into (2-6) gives:

$$V_L = \sqrt{\frac{V_S^2}{2} - (Q_L - Q_C)(X_S + X_F) \pm \sqrt{\frac{V_S^4}{4} - (X_S + X_F)^2 P_L^2 - (X_S + X_F) V_S^2 (Q_L - Q_C)}} \quad (2-13)$$

2.2.4 RPC AT THE SOURCE END OF THE FEEDER

If a RPC is available at the source end of the feeder to carry out the voltage instability corrective action, as shown in Figure 2-5(b), then the circuit condition can be formulated as follows:

$$\begin{aligned} \bar{V}_S &= jX_S(\bar{I}_L + \bar{I}_C) + jX_F \bar{I}_L + \bar{V}_L = jX_S(\bar{I}_L + jX_C(jX_F \bar{I}_L + \bar{V}_L)) + jX_F \bar{I}_L + \bar{V}_L \\ &= j(X_S + X_F - X_C X_F) \bar{I}_L + (1 - X_S X_C) \bar{V}_L \\ \therefore \bar{V}_L &= \frac{\bar{V}_S}{1 - X_S X_C} - j \frac{X_S + X_F - X_C X_F}{1 - X_S X_C} \bar{I}_L = K_1 \bar{V}_S - jK_2 \bar{I}_L \end{aligned} \quad (2-14)$$

Comparison of (2-14) with (2-1) shows that if $K_1 \bar{V}_S$ replaces $\bar{V}_S$, and K_2 replaces $X_S + X_F$ in (2-6). Then the voltage at the feeder end can be expressed as:

$$V_L = \sqrt{\frac{(K_1 V_S)^2}{2} - Q_L K_2} \pm \sqrt{\frac{(K_1 V_S)^4}{4} - K_2^2 P_L^2 - K_2 (K_1 V_S)^2 Q_L} \quad (2-15)$$

Figure 2-5: RPC corrective actions

2.2.5 Shedding at the load end of the feeder

If the load voltage is collapsing and there is no ULTC or RPC available, then load shedding at the load end of the feeder is an option, though this is the most undesirable corrective action. If the amount of load to be cut is:

$$\Delta \bar{S} = \Delta P + j\Delta Q \quad (2-16)$$

then the voltage at the feeder end can be expressed as:

$$V_L = \sqrt{\frac{V_S^2}{2} - (Q_L - \Delta Q)(X_S + X_F)} \pm \sqrt{\frac{V_S^4}{4} - (X_S + X_F)^2 (P_L - \Delta P)^2 - (X_S + X_F) V_S^2 (Q_L - \Delta Q)} \quad (2-17)$$

2.3 NEW STRATEGIES FOR LOCALIZED VOLTAGE INSTABILITY CORRECTIVE ACTIONS

This section presents new strategies for carrying out corrective actions to improve the voltage stability margin for stable network conditions, to maintain stability for the network conditions prone to instability, or to restore stability for unstable network conditions.

2.3.1 NEW STRATEGIES VERSUS TRADITIONAL APPROACH

The traditional formulations for voltage instability corrective actions given in Section 2.3 have serious limitations, because these formulations are derived based on an equivalent circuit with the assumption that the equivalent voltage $\bar{V}_s$ and the equivalent reactance jX_s are constant and known. However, this assumption is not correct in a real-time operating distribution system, since the electricity source and the load are continuously changing.

The traditional approach to voltage stability can be typically represented by the well-known PV curves, of which the power P is restricted to the power of the load connected to a feeder node where the voltage stability is under investigations due to its critical location, or concerns being caused. This restriction severely limits the operational feasibility of corrective actions. For example, the load can be shedded on the neighboring circuit or on circuits upstream or downstream, but not on the feeder location

under investigation. This would be most likely the situation where the voltage stability of the critical loads are of interest and need to be monitored and controlled, but they cannot be cut without serious consequences. The traditional approach could not handle these conditions.

The new strategies, proposed in this thesis research, are designed for carrying out the corrective actions against voltage instability with a great degree of feasibility to achieve optimal operations. In particular, the new strategies expand the traditional concept significantly, for example, by defining the power P as a *composite power* including all neighboring load powers that influencing the voltage stability of the feeder location under investigation. The new strategies are grouped into two parts: Part 1: Strategy for localized voltage instability corrective actions, and Part 2: Strategy for system-wide voltage instability corrective actions. Part 1 is presented in this section. Part 2 is presented in the next section.

The following presents the new strategies of using load shedding, load reduction through ULTC, RPC, and newly available DG as “localized” voltage instability corrective actions for improving a distribution feeder voltage stability condition or restoring voltage stability from an instability condition, during a contingency occurring in the distribution network.

2.3.2 LOAD SHEDDING FOR LOCALIZED INSTABILITY CORRECTIVE ACTION

The most effective and fast voltage-restoring action to avoid the collapse of the feeder node voltage is load shedding. However, the instability corrective action using

load shedding, that is load cutting, is most costly and has the most adverse impact on the load and the quality of utility customer services. The choice of the voltage-restoring actions depends on the type of loads connected to the feeder node and the operating condition of the distribution system. Figure 2-6 is utilized to illustrate the basic mechanism involved in load shedding for restoring the feeder network from collapsing. For illustration, the instability condition discussed in Section 2.1.3, as well as the two types of loads, the impedance load and the constant power load, are used in the following presentation.

Case 1: For the load of impedance type, the operating point moves from point A to point B , and will stay at B if no corrective action is taken place. However, the feeder node voltage at point B is V_B that may be too low for a lot of applications and may be viewed as voltage instability. Assume that corrective action using load shedding is requested. After a load shedding is implemented, the load characteristic curve changes from *curve 1* to *curve 4*. While the contingency is still going on, the feeder node voltage has improved from an unacceptable voltage V_B to an acceptable voltage V_D .

Case 2: For the load of constant-power type, assumed that after a load shedding is implemented, the demand of load power is reduced from the amount of P_A to P_C . Then the feeder node voltage is improved from the value of V_B to V_C . If V_C is not acceptable, then more loads have to cut. The load shedding is required to be carried out fast enough before the voltage collapses. Figure 2-6 is used to illustrate this requirement as follows.

Recall that the contingency causes the operating point to move from point A to point B . For constant power type of loads, the operating point will be continuously moving downwards along the post-contingency network PV *curve 3* if no corrective

action is taken place because the load demand P_A is higher than the maximum available power from the network P_{max} in curve 3. As long as the operation of the corrective action of load shedding is carried out before the operating point passes point F , there is restoring power in the network to move the operating point back to point C . The restoring power is the power available from the network on curve 3 subtracting the power P_C , the demanded load power after load shedding.

Figure 2-6: Illustration of instability corrective action using load shedding [20]

2.3.3 LOAD REDUCTION THROUGH ULTC FOR LOCALIZED INSTABILITY CORRECTIVE ACTION

The load reduction through under load tap change (ULTC) can be used to improve the voltage condition if the network is still stable after a contingency or to avoid the collapse of the feeder node voltage if the network is prone to instability. Figure 2-7 is utilized to illustrate the basic mechanism involved in ULTC load reduction for improving the voltage condition or restoring the feeder network from collapsing during post

contingency. For convenience of comparison, the instability condition discussed in the previous section is used in the following presentation.

Case 1: Carry out a substantial transformer tap change. Recall that after the contingency occurred, the operating point moves from point A to point B , and will stay at B if the load is of impedance type and if no corrective action is taken place. However the feeder node voltage at point B is V_B that may be too low for a lot of applications and may be viewed as a voltage instability. Assume that corrective action using ULTC load reduction is requested. After the ULTC load reduction is implemented, the load characteristic curve changes from *curve 1* to *curve 4*. While the contingency is still going on, the feeder node voltage has improved from an unacceptable voltage V_B to an acceptable voltage V_D .

Case 2: If a large portion of the load is of constant power type, the operating point moves from point A to point B and will continue moving downwards, and finally the feeder voltage will collapse. In addition, assuming a substantial ULTC operation is unacceptable, because either it cannot be implemented practically or it causes serious impact on the load. Then this thesis proposes to carry out enough transformer tap change to prevent voltage from collapsing as well as to avoid serious impact on the load. After an appropriate ULTC load reduction is implemented, the load characteristic curve changes from *curve 1* to *curve 5*. The new operating point is point C and the corresponding voltage is V_C . This operating point is low and therefore is not desirable, but the ULTC operation does rescue the feeder voltage from collapsing, and it is the optimal operation because a substantial ULTC either cannot be implemented practically or causes serious impact on the load. This ULTC operation must be carried out fast

enough before the operating point reaches the failure point F . On the other hand, for a longer-term quality performance, this low voltage condition needs to be improved by using other corrective actions or by restoring the system from contingency.

Figure 2-7: Illustration of instability corrective action using ULTC load reduction [20]

2.3.4 REACTIVE POWER COMPENSATION FOR LOCALIZED INSTABILITY CORRECTIVE ACTION

The reactive power compensation (RPC) can be used to improve the voltage condition if the network is still stable after a contingency, or to avoid the collapse of the feeder node voltage if the network prone to instability. Figure 2-8 is utilized to illustrate the basic mechanism involved in RPC operation for improving the voltage condition or restoring the feeder network from collapsing during post contingency. For convenience of comparison, the instability condition discussed in the previous sections is used in the following presentation.

Case 1: For the load of impedance type, the operating point moves from point A to point B , and will stay at B if no corrective action is taken place. However, the feeder node voltage at point B is V_B that may be too low for a lot of applications and may be viewed as voltage instability. Assume that corrective action using RPC is requested. After a RPC operation is implemented, Figure 2-8 shows two network curves: curve 5 and curve 6, where the amount of RPC available for the corrective actions in curve 5 is less than that in curve 6. The final operating point after the RPC operation is either on point C or point D depending on the amount of RPC available. Similarly, the final feeder voltage is either V_C or V_D . The feeder voltage is improved compared with the voltage initially at point B . If more RPC is available, the feeder voltage could be further improved.

Case 2: For the load of constant-power type, if no corrective action is implemented or if the RPC is not sufficient, then the feeder voltage could collapse. After the contingency, the operating point moves from point A to point B , and then it will continuously move downwards along curve 3 to point M and point F , and consequently the feeder voltage collapses, because there is no power available from the network along curve 3 is greater or equal to the power P_A demanded by the load. Similar condition will occur if the RPC is not sufficient. For example, the RPC operation does improve the network characteristic from curve 3 to curve 5, but the maximum power available from the network of curve 5 is P_{C-max} that is smaller than P_A , the power demanded by the load of constant type. On the other hand, when there is sufficient RPC available for the instability corrective action as shown in curve 6, the RPC operation does improve the voltage stability of the distribution network, as shown in Figure 2-8. After this RPC

operation of curve 6, the feeder voltage is improved to V_E , and at the same time the load demand of P_A is satisfied.

Figure 2-8: Illustration of instability corrective action using RPC [20]

2.3.5 INCREASED GENERATION FROM DGs FOR LOCALIZED INSTABILITY CORRECTIVE ACTION

Increased generation for DGs, if available, can improve the voltage condition if the network is still stable after a contingency or to avoid the collapse of the feeder node voltage if the network is prone to unstable. Figure 2-9 is utilized to illustrate the basic mechanism involved in increased DG output for improving the voltage condition or restoring the feeder network from collapsing during post contingency. For convenience of comparison, the instability condition discussed in the previous sections is used in the following presentation.

Case 1: For the load of impedance type, the operating point moves from point A to point B, and will stay at B if no corrective action is taken. However, the feeder node

voltage at point B is V_B that may be too low for a lot of applications and may be viewed as voltage instability. Assume that corrective action with increased DG output is requested. After an increased DG operation is implemented, Figure 2-9 shows the operating point improves from point B to C and D as the DG output increases assuming the increase of DG output first is available and second it does not cause adverse effect on other part of the distribution network.

Case 2: For the load of constant-power type, if no corrective action is implemented or if the DG output is not sufficient, then the feeder voltage could collapse. After the contingency, the operating point moves from point A to point B , and then it will continuously move downwards along curve 3 to point M and point F , and consequently the feeder voltage collapses, because there is no power available from the network along curve 3 is greater or equal to the power P_A demanded by the load. A similar condition will occur if the DG output is not sufficient. For example, the RPC operation does improve the network characteristic from curve 3 to curve 4, but the maximum power available from the network of curve 4 is P_{C-max} that is smaller than P_A , the power demanded by the load of constant type. On the other hand, when there is sufficient DG output available for the instability corrective action as shown in curve 5, the increased DG operation does improve the voltage stability of the distribution network, as shown in Figure 2-8. After this increased DG operation of curve 5, the feeder voltage is improved to V_E , and at the same time the load demand of P_A is satisfied. If more DG output is available and the increased DG output does not cause adverse impact on other part of the distribution network, then the operating point can be further improved and may be even

better than the original point A before contingency such as to the operating point G shown in Figure 2-9.

Figure 2-9: Illustration of instability corrective action using DG [20]

2.4 NEW STRATEGIES FOR NETWORK-WIDE VOLTAGE INSTABILITY CORRECTIVE ACTIONS

This section presents new strategies for carrying out network-wide corrective actions to improve the voltage stability margin for stable network conditions, to maintain stability for the network conditions prone to instability, or to restore stability for unstable network conditions.

2.4.1 NETWORK-WIDE VERSUS LOCALIZED STRATEGIES FOR STABILITY ENHANCEMENT AND INSTABILITY CORRECTION

The strategies presented in Section 2.3 are designed to fully utilize the advantages that the facilities required for the corrective actions are available in close proximity of the feeder location under investigation. However, the facilities available for implementing the instability corrective actions may not be close to the feeder location, of which maintaining the voltage stability for the critical loads is of the greatest importance, such as the financial centers, hospitals, control centers, etc. Very often, these critical loads are located in busy developed areas where there is hardly any economical space available for installation of the corrective action facilities.

This thesis research has developed new strategies for carrying out network-wide voltage stability enhancement and voltage instability corrective actions. The new strategies utilize the modern computer networking technology for distribution network-

wide acquisition of data for enhancing or restoring voltage stability, and state-of-the-art digital signal processing technology for real-time execution of voltage instability corrective actions or voltage stability enhancement operations. These network-wide strategies have two aspects: micro-operations and macro-operations. The micro-operation strategies are based on those given in Section 2.3, of which the characteristics of each practical facility for instability corrective actions are specifically utilized. The strategies for the macro-operations are presented in the following.

2.4.2 STRATEGIES FOR NETWORK-WIDE STABILITY ENHANCEMENT OR INSTABILITY CORRECTION

When a feeder location of interest, most likely connected with critical loads, is experiencing voltage instability condition, there could be many factors contributing to it and it may not be possible to identify each one in a real-time operation, particularly the critical condition leading to voltage collapse. The strategies developed in this thesis research involve several operations.

First, identify the regions of stability conditions, as shown in Figure 2-10. The stability conditions are classified into four regions: region of stability enhancement, region of instability correction, region of critical operation, and region of intensive care.

Second, determine the available resources of corrective actions at the time when the voltage instability condition is experiencing. In order to achieve an accurate and fast determination of the availability of resources, it is important to keep an active database using the computer network system developed in this thesis research to constantly

monitor the status and operating states of the resources such as whether the reactive compensator is working or not (example of active status), if it has already been operating, how much unused capacity is available for immediate use (example of current operating states), etc.

Third, select and execute available resources appropriate for the identified region of stability condition.

With a focus on the four instability corrective action resources presented in the previous sections, i.e. load shedding, ULTC load reduction, RPC, and DG, the following outlines the strategies for the selection of the resources for each region of stability conditions.

In the region of stability enhancement, moderate corrective actions are required, and therefore ULTC load reduction, moderate-speed RPC and moderate-speed DG would be appropriate.

In the region of instability correction, fast corrective actions are required, and therefore high-speed RPC, high-speed ULTC load reduction, moderate load shedding would be appropriate.

In the region of critical operation, very fast corrective actions are required, and therefore load shedding, and very high-speed RPC and ULTC load reduction would be appropriate.

In the region of intensive care, load shedding is probably the only effective action that can save this feeder voltage from collapsing.

Figure 2-10: Regions of stability conditions

2.5 FORMULATIONS FOR NEW STABILITY CONTROL STRATEGIES – PART 1: COMPUTATION OF DISTRIBUTION NETWORK PERFORMANCE

This section provides the formulation of new strategies, developed in this thesis research, for voltage stability enhancement and for voltage instability corrective actions. The new strategies presented in Section 2.3 and Section 2.4 basically consist of two basic processes: 1) identify the region of stability conditions to select the corrective actions, and 2) assess the performance of the selected corrective actions and the network response to determine if additional corrective actions are needed, or if the course of actions need to be changed. Both processes require accurate, high-speed, real-time computations of the network performance during the course of voltage stability enhancement and voltage instability corrective actions. The network computations are based on real-time data collected from the monitoring system installed in the distribution network. Therefore, the key formulation of the new strategies designed in this thesis research is composed of two parts: Part 1 is network performance computation, and Part 2 is voltage stability enhancement and voltage instability corrective action computation.

2.5.1 FORMULATION OF SYSTEM ADMITTANCE MATRIX

The system admittance matrix is formed by considering the feeder lines one by one. If a line (say no. k) interconnecting two feeder nodes i and j has a series impedance

of $\bar{Z}^{(k)}$ and a total shunt admittance of $\bar{Y}^{(k)}$, then the entries of the system admittance matrix, due to this line, are:

$$\begin{aligned}\bar{y}_{ii}^{(k)} &= \bar{y}_{jj}^{(k)} = \frac{\bar{Y}^{(k)}}{2} + \frac{1}{\bar{Z}^{(k)}}, \\ \bar{y}_{ij}^{(k)} &= -\frac{1}{\bar{Z}^{(k)}}\end{aligned}\quad (2-18)$$

The elements of the admittance matrix can be expressed as:

$$\begin{aligned}\bar{y}_{ii} &= \sum_k \bar{y}_{ii}^{(k)} + jb_i, \\ \bar{y}_{ij} &= \sum_k \bar{y}_{ij}^{(k)}, \quad i \neq j\end{aligned}\quad (2-19)$$

where b_i is the susceptance of the static compensation at feeder node i . Applying (2-19) for each feeder node in the distribution system will yield the system admittance matrix:

$$[Y] = \begin{bmatrix} \bar{y}_{11} & \bar{y}_{12} & \cdot & \cdot & \bar{y}_{1m} \\ \bar{y}_{21} & \bar{y}_{22} & \cdot & \cdot & \bar{y}_{2m} \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \bar{y}_{m1} & \bar{y}_{m2} & \cdot & \cdot & \bar{y}_{mm} \end{bmatrix} \quad (2-20)$$

2.5.2 FORMULATION OF NETWORK PERFORMANCE

First, formulate the network equation. Assume the feeder node voltage and elements of the admittance matrix are:

$$\bar{V}_i = V_i \angle \delta_i, \quad \bar{y}_{ij} = y_{ij} \angle \theta_{ij} \quad (2-21)$$

The feeder node injected current and power can be expressed as follows:

$$[\bar{I}] = [Y] \cdot [\bar{V}] \Rightarrow \bar{I}_i = \sum_j \bar{y}_{ij} \bar{V}_j \quad (2-22)$$

$$\begin{aligned}
\bar{S}_i &= \bar{V}_i \bar{I}_i^* = \bar{V}_i \sum_j \bar{y}_{ij} V_j^* = V_i \sum_j V_j y_{ij} e^{j(\delta_i - \delta_j - \theta_{ij})} \\
\therefore P &= V_i \sum_j V_j y_{ij} \cos(\delta_i - \delta_j - \theta_{ij}) \\
Q &= V_i \sum_j V_j y_{ij} \sin(\delta_i - \delta_j - \theta_{ij})
\end{aligned} \tag{2-23}$$

Second, formulate the power flow. The incremental power is expressed as the difference between the calculated powers and the specified power as:

$$\Delta P_i = P_i - P_{is} \rightarrow 0, \quad \Delta Q_i = Q_i - Q_{is} \rightarrow 0 \tag{2-24}$$

where P_{is} and Q_{is} are the expected active and reactive powers injections at bus i. Using the Fast Decoupled Load Flow technique, the incremental feeder node voltage can be expressed as [21,22]:

$$\begin{aligned}
[\Delta \delta] &= -[B_p]^{-1} \cdot \left[\frac{\Delta P}{V} \right], \\
[\Delta V] &= -[B_Q]^{-1} \cdot \left[\frac{\Delta Q}{V} \right]
\end{aligned} \tag{2-25}$$

where the elements for the Jacobian matrices $[B_p]$ and $[B_Q]$ are obtained from:

$$\begin{aligned}
\frac{\partial \Delta P_i}{\partial \delta_j} &\approx -y_{ij} \sin \theta_{ij} = -B_{ij}, \quad \frac{\partial \Delta P_i}{\partial V_j} \approx 0 \\
\frac{\partial \Delta Q_i}{\partial V_j} &\approx -y_{ij} \sin \theta_{ij} = -B_{ij}, \quad \frac{\partial \Delta Q_i}{\partial \delta_j} \approx 0
\end{aligned} \tag{2-26}$$

Third, formulate the iteration. Update the feeder voltage, angle and magnitude as follows:

$$\begin{aligned}
\delta^{k+1} &= \delta^k + \Delta \delta, \\
V^{k+1} &= V^k + \Delta V
\end{aligned} \tag{2-27}$$

Perform the iteration until the following condition is satisfied:

$$\max \left(\left[\frac{\Delta P}{V} \right] \right) \leq \varepsilon_p, \quad \max \left(\left[\frac{\Delta Q}{V} \right] \right) \leq \varepsilon_q \tag{2-28}$$

2.6 FORMULATIONS FOR NEW STABILITY CONTROL STRATEGIES – PART 2: NEW COMPUTATION OF PREDICTION OF COMPOSITE POWER AND VOLTAGE STABILITY

This section presents new concept of composite power, developed in this thesis research, for prediction of the trend of voltage stability at the feeder node of interest. Also this section presents new formulation of computation for prediction of composite power and voltage stability.

2.6.1 NEW CONCEPT OF COMPOSITE POWER FOR PREDICTION OF VOLTAGE STABILITY TREND

The new strategies, proposed in this thesis research, are designed for carrying out the corrective actions against voltage instability with a great degree of feasibility to achieve optimal operations. In particular, the new strategies expand the traditional concept significantly by defining the power P in the PV curves as a *composite power* including network-wide all load powers that influencing the voltage stability of the feeder location under investigation. This thesis research develops the new concept of the composite power. This power is not necessary to be expressed explicitly, but it is expressed indirectly as a composite effect of the changes of network-wide all load powers on the voltage stability of the feeder nodes of interest, being monitored, or under investigation.

2.6.2 NEW FORMULATION FOR PREDICTION OF CHANGES OF LOAD POWERS

This section presents a new formulation for prediction of changes of load powers using a simple second order polynomial for extrapolation of load powers based on previous monitored data. The following provides the derivation of the formulation.

The second order polynomial of extrapolation can be expressed as:

$$P = at^2 + bt + c \quad (2-29)$$

The monitoring system collects and stores data of network-wide load powers. Assume that the period of prediction is T , and the current load power and the load power of the previous two periods of a feeder node are:

$$P_{t=0} = P_1, \quad P_{t=T} = P_2, \quad P_{t=2T} = P_3 \text{ (current power)} \quad (2-30)$$

Substituting (2-30) into (2-29) gives:

$$\begin{aligned} P_1 &= a(0)^2 + b(0) + c \\ P_2 &= a(T)^2 + b(T) + c \\ P_3 &= a(2T)^2 + b(2T) + c \end{aligned} \quad (2-31)$$

Solving (2-31) for the coefficients of the polynomial gives:

$$a = \frac{P_3 - 2P_2 + P_1}{2T^2}, \quad b = \frac{4P_2 - P_3 - 3P_1}{2T}, \quad c = P_1 \quad (2-32)$$

The prediction of the load active power on the next period can be expressed as:

$$P_4 = a(3T)^2 + b(3T) + c = P_1 - 3P_2 + 3P_3 \quad (2-33)$$

Express (2-33) in the following comprehensive form:

$$P_{next} = 3P_{current} - 3P_{previous-T} + P_{previous-2T} \quad (2-34)$$

Similarly for the prediction of the load reactive power on the next period can be expressed as:

$$Q_{next} = 3Q_{current} - 3Q_{previous-T} + Q_{previous-2T} \quad (2-35)$$

The prediction of load power expressed in (2-34) and (2-35) is very simple and tremendously efficient in real-time digital signal processing.

2.6.3 PREDICTION OF VOLTAGE STABILITY AND DETERMINATION OF CORRECTIVE ACTIONS

This section presents new method of computation for prediction of voltage stability and consequently determination of corrective actions. The computation for stability prediction utilizing the formulations derived in Section 2.5.2 and equations (2-34) and (2-35).

Substituting (2-34) and (2-35) into (2-24) gives:

$$\begin{aligned} \Delta P_i &= P_i - P_{i,next} \rightarrow 0, \\ \Delta Q_i &= Q_i - Q_{i,next} \rightarrow 0 \end{aligned} \quad (2-36)$$

The computation of the feeder node voltages using (2-25), (2-27) and (2-36) is expressed as:

$$\begin{aligned} [\Delta \delta] &= -[B_p]^{-1} \cdot \left[\frac{\Delta P}{V} \right], \\ [\Delta V] &= -[B_Q]^{-1} \cdot \left[\frac{\Delta Q}{V} \right] \end{aligned} \quad (2-25)$$

$$\begin{aligned} \delta^{k+1} &= \delta^k + \Delta \delta, \\ V^{k+1} &= V^k + \Delta V \end{aligned} \quad (2-27)$$

The computation is by method of iteration until the following condition is satisfied:

$$\max\left(\left[\frac{\Delta P}{V}\right]\right) \leq \varepsilon_p, \quad \max\left(\left[\frac{\Delta Q}{V}\right]\right) \leq \varepsilon_q \quad (2-28)$$

Based on the predicted voltage of the feeder node under investigation or being monitored, the determination of the corrective actions can be preceded according to the characteristics of the four stability-improvement options, i.e. load shedding, ULTC load reduction, RPC, and DG, given in Sections 2.3 and 2.4.

CHAPTER 3

IMPLEMENTATION OF VOLTAGE STABILITY ENHANCEMENT AND CORRECTIVE ACTIONS FOR DISTRIBUTION SYSTEMS

In Chapter 2, a detailed development of the algorithm and strategy for voltage stability enhancement was presented. This strategy utilizes real-time power system measurements to obtain information about the current system state, such as whether the system is in the region of stability enhancement, critical operation, etc. This information stems from prediction data about the power demands in the system to provide detection, prediction, and mitigation of voltage instabilities. The prediction is enabled through the use of a power flow program, as well as an algorithm to search for voltage problems existing, or that may exist in the system, in the future, etc. This Chapter 3 will describe the detailed development of the strategy for voltage stability enhancement described in Chapter 2. The implementation of such a system involves overcoming 5 major challenges. They are as follows:

1. Development of a test-bed to generate the real-time power-system data, by accurate simulation of the real-time performance of a power system.
2. Development of the hardware, and software monitoring network, including the DSP-based measurement units, and the network infrastructure to support network-enabled monitoring of power system voltage as well as, active and

reactive power demand. In addition, the development of the hardware, and software system to acquire the current states of the power system equipments, such as the voltage and power set-points of Distributed Generations (DGs), the tap settings of under-load tap changers (ULTCs), the currently enabled amount of reactive compensation, and the status of circuit breakers (CBs) and bus disconnects.

3. Development of the software for acquiring data from the monitoring, and system configuration/control networks, for the stability enhancement strategy.
4. Development of a load-flow software to enable the prediction functions.
5. Development of a voltage stability enhancement software, that detects existing voltage problems, and predicts future voltage problems. This function requires the processing of vast amounts of data, and careful selection of control commands. It is this software that determines the appropriate actions for voltage stability enhancement.

The following lists the sections in this chapter:

- Section 3.1 Presents the development of a test-bed to generate the real-time power-system data, by accurate simulation of the real-time performance of a modern power system
- Section 3.2 Presents the development of the hardware, and software monitoring network, including the DSP-based measurement units, and the network infrastructure to support network-enabled monitoring of power system voltage, current and, active and reactive demand

- Section 3.3 Presents the development of the software for acquiring data from the monitoring, and system configuration/control networks, for the voltage stability enhancement strategy.
- Section 3.4 Presents the development of a load-flow software to enable the prediction functions.
- Section 3.5 Presents the development of the prediction software. This function requires the processing of vast amounts of data.

3.1 DEVELOPMENT OF THE POWER SYSTEM DATA TEST-BED

Detailed and accurate modeling of modern power systems remains one of the most challenging problems in power engineering to date. Before the advent of modern computer technology, and robust software to run on these computers, accurate simulation of the power system was nearly impossible. In the past, laboratory models of AC power systems were constructed utilizing miniature discrete components, such as resistors, capacitors, inductors, transformers, etc, to build a DC equivalent power system. These models were accurate enough for basic system construction and planning purposes [14]. However detailed testing must still be conducted on a real power system, but many preliminary studies cannot be carried out in the real power system due to safety and equipment damage concerns. In this situation, the only viable option for the development of a novel system, such as will be presented in this section, requires a computer software package for testing. Many software packages, such as the Power System Computer Aided Design (PSCAD™) [23], Power Systems Analysis Toolbox (PSAT™) [24], and Electrical Transient Analyzer Program (ETAP™) [25], are available for power system analysis. However, available time-domain analysis softwares, which are necessary for the development of a real-time control system, are either not computationally efficient enough for real-time controller verification in the power system environment, or too financially costly, or both [26]. Instead, the SIMULINK® software package, produced by the MATHWORKS® company, can be utilized to provide accurate simulation of the time-domain characteristics of the modern power system [27]. This will be the approach

utilized in this thesis, that is, to utilize the SIMULINK® package to produce the real-time data for the monitoring and control networks.

SIMULINK® system design utilizes “blocks”, specifically their parameters and interconnections, to represent the behavior of systems. This Graphical User Interface (GUI) structure allows for the rapid development of large power systems simulators. A sample SIMULINK diagram, showing the structure of, and the components within the IEEE 30-bus test system [28], is shown in Figure 3-1. A detailed treatment of all the blocks, and how they function is beyond the scope of this thesis, but the curious reader is encouraged to consult the literature [29]. What is important about this system, is that it shows how the SIMULINK® package can be utilized to construct an accurate model of the power system, which will be verified in Chapter 4. As a final note, reading measurement data, or sending control data from/to a simulation can be accomplished via the output and input blocks, respectively [29]. Thus, any system that can be built in SIMULINK® can be monitored and controlled externally from the SIMULINK® environment, allowing for the development of algorithms and hardware systems, which do not require the MATLAB® framework for voltage stability enhancement. This will be elaborated upon in the sequel.

Warning!
do not sample
frequency

Figure 3-1: IEEE 30-Bus Test System Implemented in SIMULINK

3.2 DEVELOPMENT OF THE MONITORING UNITS, CONTROL UNITS AND NETWORK

The monitoring units and network are utilized to enable the real-time voltage stability enhancement strategy proposed in this thesis. This section will first discuss the DSP hardware implementation for data acquisition. A description of the processing software, to determine the voltage and current magnitude will be presented. Thereafter, the networking hardware will be discussed, and the application of a DSP-based networking library will be discussed.

To acquire the real-time voltage and current data from the SIMULINK® simulation as discussed in Section 3.1, the RTDX library functions are utilized. A detailed description of the RTDX libraries is in [30]. A sample code to initialize the RTDX libraries, acquire a single floating point data, store it in the variable *double data_host*, and return a receipt acknowledgment data to the data sender stored in the variable *double data_target*, is shown in Figure 3-2.

```
#include <rtdx.h>
RTDX_CreateOutputChannel(ochan);
RTDX_CreateInputChannel(ichan);
void main( void ) {
    unsigned int status_host, status_target;
    unsigned int i,j;
    double data_host,data_target=10.0;
    TARGET_INITIALIZE();
    RTDX_enableOutput(&ochan);
    RTDX_enableInput(&ichan);
    while ( RTDX_read( &ichan, &data_host, sizeof(data_host) ) != sizeof(data_host) );
    status_target = RTDX_write( &ochan, &data_target, sizeof(data_target) );
}
```

Figure 3-2: RTDX Library Initialization and Data Acquisition

The calculation of voltage magnitude, is performed using the relationship in Equation (3-1).

$$|\tilde{X}| = 1.4142 \sqrt{\frac{1}{T} \left(\sum_{i=1,2,\dots,\lfloor T/T_s \rfloor} (x[i])^2 \right)} \quad (3-1)$$

In the subroutine *double mag(unsigned int)* shown in Figure 3-3, the signal $x(t)$ has been acquired from the SIMULINK® test-bed described in Section 3.1, and is stored in the buffer *buff[bufNum]*. The summation under the radical sign in Equation (3-1) is taken over three fundamental periods, to avoid inconsequential deviations that may occur in any given period.

```
double mag(unsigned int bufNum) {
    double sum=0;
    int i;
    for (i=0; i<(DataSize*3); i++)
        sum+=buff[bufNum][i]*buff[bufNum][i]*Ts;
    return (1.4142*sqrt(sum*f/3));
}
```

Figure 3-3: Voltage Magnitude Computation Routine

The computation of three-phase voltage and current signals can be accomplished using successive calls to the *double mag(unsigned int)* subroutine. This is illustrated in the subroutine *double calcMags()* shown Figure 3-4, where the voltage signal $v_{ab}(t)$ is stored in *buff[0]*, $v_{bc}(t)$ is stored in *buff[1]*, $v_{ca}(t)$ is stored in *buff[2]*. Similarly, the signals $i_a(t)$, $i_b(t)$, and $i_c(t)$ are stored in *buff[3]*, *buff[4]* and *buff[5]*, respectively.


```

double calcMags()
{
    vab = mag(0);
    vbc = mag(1);
    vca = mag(2);
    ia = mag(3);
    ib = mag(4);
    ic = mag(5);
}

```

Figure 3-4: Computation of Three-Phase Voltages and Currents

To enable the networking for the network-enabled monitoring functions described in this thesis, the DSK91C111 Ethernet Daughter-card is utilized. A picture of this daughter-card is shown in Figure 3-5. This daughter-card fits gluelessly into the External Peripheral Interface and the External Memory Interface on the TMS320C6416T Digital signal processor Starter Kit (DSK) manufactured by Spectrum Digital Inc [31], as shown in Figure 3-6. The daughter-card provides TCP/IP and UDP network connectivity for connections, negotiated at 10Mbps, or 100Mbps. The parameters of the connection are determined by configuration of the dsknet library, developed by the DSignT Inc. [32].

Figure 3-5: DSignT DSK91C111 Ethernet Daughter-Card

Figure 3-6: Connection of DSK91C111 Ethernet Card and 6416T DSK Board

The DSP code to initialize the daughter-card for network auto-negotiation is shown in Figure 3-7, where the function pointer *void link_status (unsigned char mode)* is utilized for the auto-negotiation functions, and the network requests are handled by the function pointer *int32_t tcp_call_back (SOCKET *so, void *data, u_int32_t len, u_int32_t ec)*.

```
#include "csl.h"                /* chip support library */
#include "csl_irq.h"
#include "csl_timer.h"
#include "csl_cache.h"
#include "dsknet.h"             /* network support */
#include "dskemif.h"           /* EMIF setting */
#include "netconfig.h"          /* network configuration */
unsigned int dsp_clock = 1000000000;
SOCKET *tcp_server;
static char tcp_rx[16];        /* buffer for TCP requests */
static char tcp_tx[] = "this is the DSP response\n";
int InitializeNetwork (void)
{
    u_int16_t ret;

    ret = dsk_init ( network_mode, dsp_clock, link_status);

    if ( ret == 0 )
```

```

{
    return (1);
}
printf(".");
if ( !net_init (dsp_ip_addr, dhcp_setting, dns_server_ip, dns_setting))
    return (2); // out of memory
printf(".");
if ( install_icmp_socket (1024) == NULL )
{
    return (3);
}
printf(".");
tcp_server = socket_open (ANY_ADDRESS,
                          ANY_PORT,
                          1061,
                          DATATYPE_CHAR,
                          TCP_INIT_FUNC);
if ( tcp_server == NULL )
{
    exit (5);
}
printf(".");
socket_define_callback (tcp_server, tcp_call_back, tcp_rx, sizeof(tcp_rx));
printf(".");
return (0);
}

```

Figure 3-7: DSP Configuration Code for Networking

From the discussion so far, the two important aspects of the network connection are, the auto-negotiation function, and the network request handling functions. Figure 3-7 shows the DSP code for handling the auto-negotiation functions. Whenever a network connection is dropped, or a new network connection is established by the DSK91C111 card, then this subroutine is automatically called. This was configured with the *dsk_init (network_mode, dsp_clock, link_status)* function call shown in Figure 3-7.

```

void link_status (unsigned char mode)
{
    printf("\r\n Link status changed: ");

    switch (mode)

```

```

{
    case 0xff:
        printf("No Link\n");
        break;

    default:
        printf("Linked at %dMbit %s duplex\n",
            (mode & SPEED_100) ? 100:10,
            (mode & FULL_DUPLEX) ? "full":"half");
        break;
}
}

```

Figure 3-8: Auto-Negotiation Subroutine

The network request handling function is enabled by the `socket_define_callback` (`tcp_server`, `tcp_call_back`, `tcp_rx`, `sizeof(tcp_rx)`) function call in Figure 3-6. The function for handling network requests is called whenever a network data is sent to the DSK91C111 daughter-card. The function `int32_t tcp_call_back (SOCKET *so, void *data, u_int32_t len, u_int32_t ec)` for this purpose is shown in Figure 3-7. This function simply transmits the character string that is in the variable `static char tcp_rx[16]`.

```

int32_t tcp_call_back (SOCKET *so, void *data, u_int32_t len, u_int32_t ec)
{
    switch (ec)
    {
        case 0:
            net_send (so, tcp_tx, strlen(tcp_tx));
            break;
        default:
            printf("socket error : %s\n", error_tab[so -> error_code]);
            break;
    }
    return (1);
}

```

Figure 3-9: Network Request Handling Routine

Thus, by varying the content of the variable `tcp_tx` to the message, a message can be transmitted through the network. In particular, the routine in Figure 3-9 will be utilized for sending monitoring data to the voltage stability controller proposed in this thesis, as well as receiving control commands from the voltage stability controller for updating the operation of the test-bed described in Section 3.1.

3.3 ENABLING OF NETWORK DATA ACQUISITION AT THE VOLTAGE STABILITY ENHANCMENT CONTROLLER

Section 3.2 has discussed the development of the DSP-based monitoring units, as well as the network to support the network-enabled monitoring. In this Section, the challenge of acquiring the data from many network-enabled monitoring units will be solved. To accomplish this task, the C++-based Winsock library will be utilized. This library was developed in the early 1990s, to allow the development of robust C/C++ based applications that require networking capabilities. The latest version of the Winsock Application Programming Interface (API) is the Winsock 2 API [33]. The Winsock API simply provides software-based access to the data that is received through a network card installed on a host PC. The initialization of the Winsock network programming interface is accomplished with the C++ code shown in Figure 3-9. This code allows the computer network card to connect to the device with the IP address "192.168.168.200", which is the IP address for the DSP-based network monitoring unit developed in Section 3.2. The approach allows connection to as many as 256 DSP-based monitoring and/or control units, which are each assigned a unique, but arbitrary, IP addresses in the range 192.168.168.0 to 192.168.168.255.

```

include <winsock.h>
nRet = WSAStartup(wVersionRequested, &wsaData);
printf("\nClient connecting to server: %s on port: %d\r\n", "192.168.168.200", 1061);

// Find the server
LPHOSTENT lpHostEntry;
lpHostEntry = gethostbyname("192.168.168.200");
if (lpHostEntry == NULL)
{
    PRINTERROR("gethostbyname()");
    return;
}
//
// Create a TCP/IP stream socket
//
SOCKET theSocket;
theSocket = socket(AF_INET,          // Address family
                  SOCK_STREAM,       // Socket type
                  IPPROTO_TCP);      // Protocol
if (theSocket == INVALID_SOCKET)
{
    PRINTERROR("socket()");
    return;
}
u_long* dataSize;
long blockingMode = 1;

SOCKADDR_IN saServer;
saServer.sin_family = AF_INET;
saServer.sin_addr = *((LPIN_ADDR)*lpHostEntry->h_addr_list); // ^ Server's
address
saServer.sin_port = htons(1061); // Port number

// Establish connection
int nRet;
nRet = connect(theSocket, (LPSOCKADDR)&saServer, sizeof(struct sockaddr));
if (nRet == SOCKET_ERROR)
{
    PRINTERROR("socket()");
    closesocket(theSocket);
    return;
}

```

Figure 3-10: Network Interface Configuration Using Winsock API

The network requests on the voltage stability enhancement server side are handled by the *void networkManagement()* routine defined in Figure 3-10. The winsock API function *send*, is used to send the contents of the character string *sBuf* over the network, using the network connection defined by the Winsocket *theSocket*, which was initialized in Figure 3-9. The *sBuf* variable is thus utilized to send control commands through the network, to the DSP-based control unit at the IP address defined by *theSocket*. Similarly, the Winsock API function *recv* is utilized to receive network data, and store it in the character string *rBuf*. The network connection for this data transmission is defined by the Winsocket *theSocket*. So, the *rBuf* variable is used hold the data received from the monitoring unit. This data will be the real-time measurements taken by the DSP-based monitoring unit developed in Section 3.2.

```
void networkManagement() {
    nRet = send(theSocket, sBuf, sizeof(sBuf), 0);
    if (nRet == SOCKET_ERROR)
    {
        PRINTERERROR("send()");
        closesocket(theSocket);
        return;
    }
    printf("message sent successfully, waiting for reply\n");
    nRet = recv(theSocket, rBuf, sizeof(rBuf), 0);
    if (nRet == SOCKET_ERROR)
    {
        PRINTERERROR("recv()");
        closesocket(theSocket);
        return;
    }
}
```

Figure 3-11: Subroutine for handling Network Requests

3.4 DEVELOPMENT OF THE LOAD-FLOW SOFTWARE

The key software for implementation of the voltage stability enhancement system, as proposed in this thesis, is the load flow routine. Load flow is utilized to determine the predicted voltage and phase angle at all buses of interest in a power system of arbitrary size. This routine is broken up into two distinct parts, namely, the portion that checks the convergence of the real power injection vector, and the part that checks the convergence of the reactive power injection vector. The software to check the convergence of the active power vector is shown in Figure 3-12.

```

for (numIts=0 ; numIts<20 ; numIts++) {
    for (i=(numGen+numTx) ; i<(numGen+numTx+numLoad) ; i++) {
        tempsum = 0;
        for (j=0 ; j<(numGen+numTx+numLoad) ; j++) {
            tempsum += Vbus[i]*Vbus[j]*magY[i][j]*cos(thetabus[i] - thetabus[j] -
angY[i][j]);
        }
        delP[i] = (Pbus[i] + tempsum)/Vbus[i];
    }

    // Step 3: Check convergence of active Power
    if (maxVector(delP) < ep) {
        KP=1;
        if (KQ==1)
            break;
    }

    // If P doesn't converge...
    else {
        // solve 8 and update thetaV
        for (i=(numGen+numTx) ; i<(numGen+numTx+numLoad) ; i++) {
            tempsum=0;
            for (j=(numGen+numTx) ; j<(numGen+numTx+numLoad) ; j++)
                tempsum -= Binv[i][j]*delP[j];
            thetabus[i] -= tempsum;
        }
        KQ=0;
    }
}

```

Figure 3-12: Checking Convergence of the Active Power Vector

The software shown in Figure 3-12 is based upon the load-flow algorithm presented in Section 2.6. Similarly, the software to check the convergence of the reactive power vector is shown in Figure 3-13. Both of the routines for checking converge of the active and reactive power vectors, utilized the helper subroutine, shown in Figure 3-14.

```

for (numIts=0 ; numIts<20 ; numIts++) {
//Step 4, calculate deltaQ
for (i=(numGen+numTx) ; i<(numGen+numTx+numLoad) ; i++) {
    tempsum =0;
    for (j=0 ; j<(numGen+numTx+numLoad) ; j++) {
        tempsum += Vbus[i]*Vbus[j]*magY[i][j]*sin(thetabus[i] - thetabus[j] -
angY[i][j]);
        delQ[i] = (Qbus[i] + tempsum)/Vbus[i];
    }
}
// Step 5: Check convergence of reactive power
if (maxVector(delQ) < eq)
{
    KQ=1;
    if (KP==1)
    {
        break;
    }
}

// If Q doesn't converge
else
{
    // solve 9 and update V
    for (i=(numGen+numTx) ; i<(numGen+numTx+numLoad) ; i++)
    {
        tempsum=0;
        for (j=(numGen+numTx) ; j<(numGen+numTx+numLoad) ; j++)
            tempsum -= Binv[i][j]*delQ[j]/Vbus[j];
        Vbus[i] -= tempsum;
    }
}
} // loop back to beginning

```

Figure 3-13: Checking Convergence of the Reactive Power Vector

The algorithm for checking the maximum value of a vector is quite simple. A variable called *double max*, which will contain the maximum value in the vector *double *x* when the routine is completed, is initialized to the first value in the vector. Then, the value of *max* is compared with each subsequent value in the vector, and *max* is reinitialized to be the maximum value of *max* and *x[i]*, until all elements have been analyzed.

```
double maxVector(double* x)
{
    double max;
    max = x[1];
    for (int i=1 ; i<sizeY ; i++)
        if (max < x[i])
            max = x[i];
    return max;
}
```

Figure 3-14: maxVector Routine

3.5 DEVELOPMENT OF THE VOLTAGE STABILITY ENHANCEMENT STRATEGY

A key contribution to this thesis is a novel power flow predictor. This power flow predictor utilizes Equation (2-34) developed in Section 2.6. This equation is repeated in Equation (3-2) for convenience.

$$P_{next} = 3P_{current} - 3P_{previous-T} + P_{previous-2T} \quad (3-2)$$

The MATLAB code for computation of the predictor output (P_{next}) is shown in Figure 3-15.

```
% Clear workspace and command window
clear; clc;
% Generate test waveform
w=0.01;
tp = 0.01;
tend=2400;
t=0:tp:tend;
P = (0.5 + 0.00001*t + 0.01*sin(w*t)) ;

% Sample waveform
Ts=5;
for k=1:floor((tend/Ts))
    tk3(k) = t((k-1)*Ts/tp + 1);
    Pk3(k) = P((k-1)*Ts/tp + 1);
end;
% initialize prediction parameters
Pm3(1) = 0;
Pm3(2) = 0;
% Calculate the next voltage output
for i=2:(floor((tend/Ts))-1)
    Pm3(i+1) = 3*Pk3(i) - 3*Pk3(i-1) + Pk3(i-2);
end;
% Generate graphs
plot(t/60,P,tk3(:)/60,Pm3(:));
axis([0 2400/60 0.45 0.55]);
xlabel('t [min]');
ylabel('P [pu]');
legend('P_{measured}', 'P_{predicted, T_s=5s}');
grid on;
```

Figure 3-15: MATLAB program for computation of future bus loading

CHAPTER 4

VERIFICATION OF VOLTAGE STABILITY ENHANCEMENT AND CORRECTIVE ACTIONS FOR DISTRIBUTION SYSTEMS

In this chapter, a detailed set of case studies for verification of the voltage stability enhancement strategy proposed in this thesis, will be presented. First, in Chapter 4.1, SIMULINK environment will be utilized to illustrate the strategy. Results will show that the strategy is successful. Thereafter, in Chapter 4.2, a detailed hardware investigation will be described. The results from this investigation will verify that the strategies and softwares developed in this thesis were successful, and may enhance the voltage stability of the distribution system.

The following lists the sections in this chapter:

- Section 4.1 Presents verification in the MATLAB/SIMULINK testbed.
- Section 4.2 Presents the hardware verifications.
- Section 4.3 Presents the verification of the comparison of the PV curves.

Table 4-1: Bus Data for the 30-Bus Test System

Bus Number	V (pu)	Theta	Pload (pu)	Qload (pu)	Base v (kV)
1	1.06	0	0	0	132
2	1.045	-5.48	0.217	0.127	132
3	1.01	-14.37	0.942	0.19	132
4	1.01	-12.1	0.3	0.3	132
5	1.082	-14.39	0	0	11
6	1.071	-15.24	0	0	11
7	1.021	-7.96	0.024	0.012	132
8	1.012	-9.62	0.076	0.016	132
9	1.01	-11.34	0	0	132
10	1.002	-13.12	0.228	0.109	132
11	1.051	-14.38	0	0	1
12	1.045	-15.97	0.058	0.02	33
13	1.057	-15.24	0.112	0.075	33
14	1.042	-16.13	0.062	0.016	33
15	1.038	-16.22	0.082	0.025	33
16	1.045	-15.83	0.035	0.018	33
17	1.04	-16.14	0.09	0.058	33
18	1.028	-16.82	0.032	0.009	33
19	1.026	-17	0.095	0.034	33
20	1.03	-16.8	0.022	0.0077	33
21	1.033	-16.42	0.175	0.112	33
22	1.033	-16.41	0	0	33
23	1.027	-16.61	0.032	0.016	33
24	1.021	-16.78	0.087	0.067	33
25	1.017	-16.35	0	0	33
26	1	-16.77	0.035	0.023	33
27	1.023	-15.82	0	0	33
28	1.007	-11.97	0	0	132
29	1.003	-17.06	0.024	0.009	33
30	0.992	-17.94	0.106	0.019	33

Table 4-2: Line Data for 30-Bus Test System

Tap Bus	Z bus	Rseries(PU)	Xseries(PU)
1	2	0.0192	0.0575
1	7	0.0452	0.1652
2	8	0.057	0.1737
7	8	0.0132	0.0379
2	3	0.0472	0.1983
2	9	0.0581	0.1763
8	9	0.0119	0.0414
3	10	0.046	0.116
9	10	0.0267	0.082
4	9	0.012	0.042
9	11	0	0.208
9	12	0	0.556
5	11	0	0.208
11	12	0	0.11
8	13	0	0.256
13	6	0	0.14
13	14	0.1231	0.2559
13	15	0.0662	0.1304
13	16	0.0945	0.1987
14	15	0.221	0.1997
16	17	0.0524	0.1923
15	18	0.1073	0.2185
18	19	0.0639	0.1292
19	20	0.034	0.068
12	20	0.0936	0.209
12	17	0.0324	0.0845
12	21	0.0348	0.0749
12	22	0.0727	0.1499
21	22	0.0116	0.0236
15	23	0.1	0.202
22	24	0.115	0.179
23	24	0.132	0.27
24	25	0.1885	0.3292
25	26	0.2544	0.38
25	27	0.1093	0.2087
27	28	0	0.396
27	29	0.2198	0.4153
27	30	0.3202	0.6027
29	30	0.2399	0.4533
4	28	0.0636	0.2
9	28	0.0169	0.013

This thesis will now utilize this model to build a number of significant case studies. In these case studies, bus 19 will be considered the bus of interest. In other words, for the case studies, the voltage stability enhancement system proposed in this thesis will be interested in improving the operation of bus 19, through control of the compensation devices at bus 18, and 20, through the control of the ULTC connected between buses 6 and 10, and through shedding the non-critical loads at system buses.

CASE 1: NO VOLTAGE SAG EXISTING OR PREDICTED AT CRITICAL BUS 19

In this case, it is assumed that a small increase in load at bus 19 will not result in voltage instabilities. The voltage stability enhancement strategy proposed in this thesis takes no action. The resulting slowly decreasing voltage profile is shown in Figure 4-2.

Figure 4-2: Voltage at Bus 19 is acceptable, but is decreasing slightly due to a slow increase in loading.

CASE 2: VOLTAGE SAG PREDICTED AT CRITICAL BUS 19

In this scenario, the voltage stability enhancement strategy proposed in this thesis must take immediate actions to improve the voltage profile. Specifically, the strategy sheds many of non-critical loads in the system. This case verifies that load shedding is a successfully means to mitigate voltage instabilities, which is consistent with the theory presented in Section 2.3.2

Figure 4-3: Voltage at Bus 19 drops below -5% tolerance limit due to slow increase of loading, load shedding action is taken at $t = 42$ minutes

CASE 3: CONTINGENCY CAUSES SIGNIFICANT VOLTAGE INSTABILITY

In this case, it is assumed that there has been a steady increase in loading at all buses in the system, resulting in a slowly decreasing voltage profile at the critical bus. At $t=23\text{min}$, a severe contingency forces line 10-20 out of service, which results in a substantial voltage drop. Load shedding after the fault results in only a small increase in voltage, due to the crippling nature of losing one of the two main lines feeding bus 19. The fault is cleared and load service is restored by the voltage stability enhancement strategy proposed in this thesis.

Figure 4-4: Voltage Profile at Bus 19 during a contingency and the resulting voltage instability

CASE 4: HEAVY LOADING AND VAR COMPENSATION ACTIONS

In this case, there is a large increase in loading at all buses in the system, which results in the voltage dropping below the -5% tolerance. The voltage stability enhancement system proposed in this thesis utilizes switched capacitor compensation at neighboring buses to increase the voltage profile at the critical bus 19. This case shows that RPC is an excellent strategy to mitigate voltage instabilities, according to the theory presented in Section 2.3.4.

Figure 4-5: Heavy load and static-var compensator actions.

CASE 5: ULTC AND LOAD SHEDDING ACTION COMBINED DURING A SIGNIFICANT VOLTAGE INSTABILITY

A rapid increase in loading begins at $t=8\text{min}$. At $t=24\text{min}$, the voltage drops below the 5% tolerance region. ULTC action begins increasing the voltage at $t=26\text{min}$, and successfully increases the voltage to slightly above the 1pu set-point. This action sets into action a serious voltage instability, which results in a rapid decrease in voltage at $t=28\text{min}$. Load shedding action is taken, restoring the system to an acceptable voltage profile. This case shows that ULTC adjustment coupled with load shedding is an effective means to mitigate voltage instabilities, according to the theory presented in Sections 2.3.2, and 2.3.3.

Figure 4-6: ULTC action and load shedding

4.1.2 VERIFICATION OF PREDICTOR

A key development of this thesis research is the novel load demand predictor developed in Section 2.6.2. In these examples, the performance of the predictor will be examined under varying power demand profiles, and under variety sampling frequencies. This is an effective means of verification of the predictor proposed in this thesis research. Figure 4-7 shows the actual and predicted powers for an arbitrary power waveform, having the form: $P = 0.5 + 1 \cdot 10^{-5} * t + 0.01 * \sin(0.01 * t)$, where t is the time in seconds. The prediction mechanism's results show excellent agreement with the actual measured waveform. This is possible due to the selection of a sampling frequency that is much higher than the frequency variation of the power waveform being measured. In this application, a low sampling frequency can be afforded because power systems, except during major events like contingencies, are very stiff and show small such variations.

Figure 4-7: Measured and predicted power for $P = 0.5 + 0.00001*t + 0.01*\sin(0.01*t)$

The next examples shows the affect that sampling frequency can have on the predictor's performance. Figure 4-8 illustrates the relationship between the prediction formulation's ability to follow the measured waveform, and the sampling period. The predicted waveforms for $T_s=5s$, $T_s=20s$, and $T_s=40s$ are shown in the Figure, as well as the original measured waveform. The measured waveform and the predicted waveform sampled at $T_s=5s$, and $T_s=20s$ are indistinguishable. The waveform sampled at $T_s=40s$ shows only small variations, particular at the local peaks when the waveform's slope changes significantly. From this figure, it is clear that increasing the sampling period, i.e. decreasing the sampling frequency, does reduce the ability of the predictions to track the actual measurements. However, using modern digital-signal processing technology, sampling periods of only few seconds are to be expected. Next we will explore the

ability of the prediction mechanism to follow steep changes in the power waveform, such as those that occur during a contingency, or during load shedding operations as described in Section 2.3.2.

Figure 4-8: Measured and predicted power for $P = 0.5 + 0.00001*t + 0.01*\sin(0.01*t)$

Figure 4-9 illustrates the response of the predictor to a sudden drop in measured power. This power drop could be due to a contingency, or load shedding following an approaching voltage instability. All source code for the predictor program is available in the Appendix A1.

Figure 4-9: Response during a sudden rapid drop in loading

4.2 HARDWARE VERIFICATION

In this section, a detailed investigation of the hardware implementation of the voltage stability enhancement strategy proposed in this thesis will be presented. First, a detailed investigation of the interface between the DSP and SIMULINK test-bed will be presented. This interface simulates the performance of the DSP-based monitoring and distributed processor unit. Thereafter, a detailed investigation of the communication interface between the DSP, and the voltage stability enhancement system. This interface simulates the communication link between a single monitoring and distributed processor unit, and the centralized controller. In a real-time power system monitoring and control application, there will be many such links. This section will conclude with a detailed investigation and verification of the load-flow software.

4.2.1 THE SIMULINK-DSP INTERFACE

Figure 4-10 shows a photograph of the DSP to Host-PC interface, where the host PC in this example is conducting time-domain simulations of the power system through the SIMULINK test-bed. Verification of this interface is equivalent to transmitting the real-time data from the SIMULINK test-bed through a RTDX channel, and to the RTDX buffer on the DSP. The configuration software to accomplish this task was presented in Section 3.2. Figure 4-11 shows the plots of the real-time measurements of the bus 19 voltage in the SIMULINK environment, and in the DSP's Code Composer Studio Environment. The source code and simulation models for this portion of the verification

is available in Appendix A.2. The waveforms were identical. This is due to the high reliability of modern computer and digital signal processor architecture.

Figure 4-10: A Photograph of the DSP to Host-PC interface

Figure 4-11: Real-Time measurements of Bus 19 Voltage, from Code-Composer Studio

Figure 4-12: Real-Time measurements of Bus 19 Voltage, from SIMULINK

4.2.2 THE DSP-CONTROLLER INTERFACE

In this example, the host PC is conducting time-domain simulations of the power system through the SIMULINK test-bed, transmitting the data through the RTDX channel to the DSP. The DSP then prepares this information for network transmission, and transmits this data to the voltage stability enhancement controller. In this example, the IEEE 30-bus simulation will be used to generate a set of real-time voltage magnitude, voltage angle, as well as power and reactive power flow through each of the 30 buses. This information will then be transmitted through the RTDX channel to the DSP, and the DSP will transmit all 120 pieces of data through the network, to the voltage stability enhancement controller. Table 4-1 shows the data generated by the SIMULINK, Table 4-2 shows the data received by the DSP, and Table 4-3 shows the data received by the centralized controller, through the network connection. Finally, Figure 4-13 shows the

output from the centralized controller's execution. The source code and simulation models for this portion of the verification are available in Appendix A.3.

Table 4-1: Power System Monitoring Data for 30-Bus System from MATLAB

Bus	V	theta	P	Q
1	1.0600	0.0000	7488.3520	3635.4970
2	1.0450	-5.4800	1021.0550	-1433.4540
3	1.0100	-14.3700	3070.7280	818.3247
4	1.0100	-12.1000	2732.5930	857.9235
5	1.0820	-14.3900	-8.0222	-2.8115
6	1.0710	-15.2700	-17.4979	-12.4858
7	1.0289	-6.5152	-4.0668	-6.1578
8	1.0217	-8.0666	-142.4347	-181.4559
9	1.0138	-10.2838	-2842.8380	-1250.2070
10	1.0013	-12.6094	596.0862	868.0281
11	1.0715	-10.6758	7.7473	3.2931
12	1.0715	-10.6758	45.9321	-247.3209
13	1.0898	-8.8976	-93.1818	-120.9814
14	1.0651	-10.4906	-21.7905	-20.5947
15	1.0522	-10.9115	-16.8420	-18.0083
16	1.0803	-9.9221	12.8138	18.3385
17	1.0675	-10.7472	-1.5805	-10.2443
18	1.0241	-12.8090	22.0213	19.5593
19	1.0119	-13.7124	-53.5959	-58.8353
20	1.0257	-13.0173	-4.1599	-4.8238
21	1.0117	-15.4239	-25.4452	-49.0720
22	1.0423	-12.4874	-8.0540	-22.6895
23	1.0333	-11.9428	11.1212	10.6151
24	1.0197	-12.8855	-0.1946	-17.0859
25	1.0107	-13.6911	7.8379	4.9013
26	0.9888	-14.2291	4.7949	9.4844
27	1.0162	-13.8681	21.5173	29.0468
28	1.0117	-10.4184	20.2941	31.1586
29	0.9918	-15.4002	-4.1658	-5.0564
30	0.9780	-16.4930	20.4591	17.2502

Table 4-2: Power System Monitoring Data for 30-Bus System from CCS

Bus	V	theta	P	Q
1	1.06	0	7488.352	3635.4968
2	1.045	-5.48	1021.0545	-1433.4545
3	1.01	-14.37	3070.7275	818.3247
4	1.01	-12.1	2732.5926	857.9235
5	1.082	-14.39	-8.0222	-2.8115
6	1.071	-15.27	-17.4979	-12.4858
7	1.0289	-6.5152	-4.0668	-6.1578
8	1.0217	-8.0666	-142.4347	-181.4559
9	1.0138	-10.2838	-2842.8383	-1250.2073
10	1.0013	-12.6093	596.0862	868.0281
11	1.0715	-10.6757	7.7473	3.2931
12	1.0715	-10.6757	45.9321	-247.3209
13	1.0898	-8.8976	-93.1818	-120.9814
14	1.0651	-10.4906	-21.7905	-20.5947
15	1.0522	-10.9115	-16.842	-18.0083
16	1.0803	-9.9221	12.8138	18.3385
17	1.0675	-10.7472	-1.5805	-10.2443
18	1.0241	-12.809	22.0213	19.5593
19	1.0119	-13.7124	-53.5959	-58.8353
20	1.0257	-13.0173	-4.1599	-4.8238
21	1.0117	-15.4239	-25.4452	-49.072
22	1.0423	-12.4874	-8.054	-22.6895
23	1.0333	-11.9428	11.1212	10.6151
24	1.0197	-12.8855	-0.1946	-17.0858
25	1.0107	-13.6911	7.8379	4.9013
26	0.9888	-14.2291	4.7949	9.4844
27	1.0162	-13.8681	21.5173	29.0468
28	1.0117	-10.4184	20.2941	31.1586
29	0.9918	-15.4002	-4.1658	-5.0564
30	0.978	-16.493	20.4591	17.2502

Table 4-3: Power System Monitoring Data for 30-Bus System from Controller

Bus	V	theta	P	Q
1	1.06	0	7488.352051	3635.496826
2	1.045001	-5.48	1021.054504	-1433.454468
3	1.01	-14.370001	3070.72754	818.324708
4	1.01	-12.1	2732.59253	857.923524
5	1.082	-14.390001	-8.022236	-2.811493
6	1.071	-15.270001	-17.497897	-12.485793
7	1.028863	-6.515194	-4.066753	-6.157773
8	1.021724	-8.066579	-142.434663	-181.455873
9	1.01385	-10.28379	-2842.840332	-1250.205322
10	1.001251	-12.609349	596.086182	868.028137
11	1.071507	-10.67575	7.747349	3.29311
12	1.071507	-10.675746	45.932073	-247.320847
13	1.089763	-8.897555	-93.181817	-120.981361
14	1.065076	-10.490592	-21.790506	-20.594664
15	1.052205	-10.911522	-16.841972	-18.00827
16	1.080255	-9.922057	12.813806	18.338482
17	1.067488	-10.747199	-1.580508	-10.244275
18	1.024059	-12.809006	22.02127	19.559253
19	1.011908	-13.712428	-53.595913	-58.835258
20	1.025707	-13.017314	-4.15991	-4.823815
21	1.01174	-15.423881	-25.445219	-49.072044
22	1.042304	-12.487369	-8.054045	-22.689545
23	1.033314	-11.94278	11.121209	10.61511
24	1.01965	-12.885504	-0.194607	-17.085848
25	1.010689	-13.691074	7.837947	4.901318
26	0.988838	-14.229083	4.794869	9.484352
27	1.016245	-13.868069	21.517282	29.046765
28	1.011733	-10.418436	20.294181	31.15858
29	0.991831	-15.400162	-4.165842	-5.05641
30	0.977953	-16.493042	20.459114	17.250242

Client connecting to server: 192.168.168.200 on port: 1061

Bus 1: V = 1.060000 pu, theta = 0.000000 deg, P = 7488.352051 pu, Q = 3635.496826 pu
Bus 2: V = 1.045001 pu, theta = -5.480000 deg, P = 1021.054504 pu, Q = -1433.454468 pu
Bus 3: V = 1.010000 pu, theta = -14.370001 deg, P = 3070.727540 pu, Q = 818.324708 pu
Bus 4: V = 1.010000 pu, theta = -12.100000 deg, P = 2732.592530 pu, Q = 857.923524 pu
Bus 5: V = 1.082000 pu, theta = -14.390001 deg, P = -8.022236 pu, Q = -2.811493 pu
Bus 6: V = 1.071000 pu, theta = -15.270001 deg, P = -17.497897 pu, Q = -12.485793 pu
Bus 7: V = 1.028863 pu, theta = -6.515194 deg, P = -4.066753 pu, Q = -6.157773 pu
Bus 8: V = 1.021724 pu, theta = -8.066579 deg, P = -142.434663 pu, Q = -181.455873 pu
Bus 9: V = 1.013850 pu, theta = -10.283790 deg, P = -2842.840332 pu, Q = -1250.205322 pu
Bus 10: V = 1.001251 pu, theta = -12.609349 deg, P = 596.086182 pu, Q = 868.028137 pu
Bus 11: V = 1.071507 pu, theta = -10.675750 deg, P = 7.747349 pu, Q = 3.293110 pu
Bus 12: V = 1.071508 pu, theta = -10.675746 deg, P = 45.932073 pu, Q = -247.320847 pu
Bus 13: V = 1.089763 pu, theta = -8.897555 deg, P = -93.181817 pu, Q = -120.981361 pu
Bus 14: V = 1.065076 pu, theta = -10.490592 deg, P = -21.790506 pu, Q = -20.594664 pu
Bus 15: V = 1.052205 pu, theta = -10.911522 deg, P = -16.841972 pu, Q = -18.008270 pu
Bus 16: V = 1.080255 pu, theta = -9.922057 deg, P = 12.813806 pu, Q = 18.338482 pu
Bus 17: V = 1.067488 pu, theta = -10.747199 deg, P = -1.580508 pu, Q = -10.244275 pu
Bus 18: V = 1.024059 pu, theta = -12.809006 deg, P = 22.021270 pu, Q = 19.559253 pu
Bus 19: V = 1.011908 pu, theta = -13.712428 deg, P = -53.595913 pu, Q = -58.835258 pu
Bus 20: V = 1.025707 pu, theta = -13.017314 deg, P = -4.159910 pu, Q = -4.823815 pu
Bus 21: V = 1.011740 pu, theta = -15.423881 deg, P = -25.445219 pu, Q = -49.072044 pu
Bus 22: V = 1.042304 pu, theta = -12.487369 deg, P = -8.054045 pu, Q = -22.689545 pu
Bus 23: V = 1.033314 pu, theta = -11.942780 deg, P = 11.121209 pu, Q = 10.615110 pu
Bus 24: V = 1.019650 pu, theta = -12.885504 deg, P = -0.194607 pu, Q = -17.085848 pu
Bus 25: V = 1.010689 pu, theta = -13.691074 deg, P = 7.837947 pu, Q = 4.901318 pu
Bus 26: V = 0.988838 pu, theta = -14.229083 deg, P = 4.794869 pu, Q = 9.484352 pu
Bus 27: V = 1.016245 pu, theta = -13.868069 deg, P = 21.517282 pu, Q = 29.046765 pu
Bus 28: V = 1.011733 pu, theta = -10.418436 deg, P = 20.294181 pu, Q = 31.158580 pu
Bus 29: V = 0.991831 pu, theta = -15.400162 deg, P = -4.165842 pu, Q = -5.056410 pu
Bus 30: V = 0.977953 pu, theta = -16.493042 deg, P = 20.459114 pu, Q = 17.250242 pu

Figure 4-13: Output from centralized processor

4.2.3 THE LOAD-FLOW SOFTWARE

Figure 4-14 shows the output of the load flow program run for a modification of the IEEE 30-Bus system. For the sake of comparison, the SIMULINK-based PSAT model shown in Figure 4-15 was constructed to be consistent with the modified model of the 30-bus test system. The results from the PSAT simulation is shown in Table 4-4, and the results from the developed load-flow program are shown in Table 4-5. The results show excellent agreement due to the accuracy and robustness of the developed load flow program. The source code and simulation models for this portion of the verification are available in Appendix A.4.

Power Flow converged in 8 iterations

Bus 1: V = 1.0600 pu ang = 0.0000 deg Pi = 2.6560 pu Qi = -0.1678 pu
Bus 2: V = 1.0450 pu ang = -5.4800 deg Pi = 0.1837 pu Qi = 0.5270 pu
Bus 3: V = 1.0100 pu ang = -14.3700 deg Pi = -0.9484 pu Qi = 0.2157 pu
Bus 4: V = 1.0100 pu ang = -12.1000 deg Pi = -0.3618 pu Qi = 0.1488 pu
Bus 5: V = 1.0820 pu ang = -14.3900 deg Pi = 0.0009 pu Qi = 0.3104 pu
Bus 6: V = 1.0710 pu ang = -15.2400 deg Pi = 0.0290 pu Qi = 0.3517 pu
Bus 7: V = 1.0223 pu ang = -7.6728 deg Pi = -0.0240 pu Qi = -0.0120 pu
Bus 8: V = 1.0147 pu ang = -9.4744 deg Pi = -0.0760 pu Qi = -0.0160 pu
Bus 9: V = 1.0093 pu ang = -11.2828 deg Pi = 0.0000 pu Qi = 0.0000 pu
Bus 10: V = 1.0009 pu ang = -13.0604 deg Pi = -0.2280 pu Qi = -0.1090 pu
Bus 11: V = 1.0223 pu ang = -14.3991 deg Pi = 0.0000 pu Qi = 0.0000 pu
Bus 12: V = 0.9989 pu ang = -16.0691 deg Pi = -0.0580 pu Qi = -0.0200 pu
Bus 13: V = 1.0250 pu ang = -15.4520 deg Pi = -0.1120 pu Qi = -0.0750 pu
Bus 14: V = 1.0072 pu ang = -16.3818 deg Pi = -0.0620 pu Qi = -0.0160 pu
Bus 15: V = 1.0002 pu ang = -16.4026 deg Pi = -0.0820 pu Qi = -0.0250 pu
Bus 16: V = 1.0060 pu ang = -15.9660 deg Pi = -0.0350 pu Qi = -0.0180 pu
Bus 17: V = 0.9959 pu ang = -16.2817 deg Pi = -0.0900 pu Qi = -0.0580 pu
Bus 18: V = 0.9870 pu ang = -17.0365 deg Pi = -0.0320 pu Qi = -0.0090 pu
Bus 19: V = 0.9825 pu ang = -17.2070 deg Pi = -0.0950 pu Qi = -0.0340 pu
Bus 20: V = 0.9857 pu ang = -16.9827 deg Pi = -0.0220 pu Qi = -0.0077 pu
Bus 21: V = 0.9854 pu ang = -16.5203 deg Pi = -0.1750 pu Qi = -0.1120 pu
Bus 22: V = 0.9858 pu ang = -16.4935 deg Pi = 0.0000 pu Qi = 0.0000 pu
Bus 23: V = 0.9833 pu ang = -16.6738 deg Pi = -0.0320 pu Qi = -0.0250 pu
Bus 24: V = 0.9719 pu ang = -16.7325 deg Pi = -0.0870 pu Qi = -0.0670 pu
Bus 25: V = 0.9726 pu ang = -16.2875 deg Pi = 0.0000 pu Qi = 0.0000 pu
Bus 26: V = 0.9541 pu ang = -16.7474 deg Pi = -0.0350 pu Qi = -0.0230 pu
Bus 27: V = 0.9820 pu ang = -15.7244 deg Pi = 0.0000 pu Qi = 0.0000 pu
Bus 28: V = 1.0051 pu ang = -11.4292 deg Pi = 0.0000 pu Qi = 0.0000 pu
Bus 29: V = 0.9612 pu ang = -17.0622 deg Pi = -0.0240 pu Qi = -0.0090 pu
Bus 30: V = 0.9492 pu ang = -18.0252 deg Pi = -0.1060 pu Qi = -0.0190 pu

Figure 4-14: Load-Flow Program Output

Figure 4-15: PSAT Model of the Modified 30-Bus Test System

Table 4-4: Load-Flow Results from PSAT

Bus	V	theta	P	Q
1	1.060	0.000	2.656	-0.168
2	1.045	-5.480	0.184	0.527
3	1.010	-14.370	-0.948	0.216
4	1.010	-12.100	-0.362	0.149
5	1.082	-14.390	0.001	0.310
6	1.071	-15.240	0.029	0.352
7	1.022	-7.673	-0.024	-0.012
8	1.015	-9.474	-0.076	-0.016
9	1.009	-11.283	0.000	0.000
10	1.001	-13.060	-0.228	-0.109
11	1.022	-14.399	0.000	0.000
12	0.999	-16.069	-0.058	-0.020
13	1.025	-15.452	-0.112	-0.075
14	1.007	-16.382	-0.062	-0.016
15	1.000	-16.403	-0.082	-0.025
16	1.006	-15.966	-0.035	-0.018
17	0.996	-16.282	-0.090	-0.058
18	0.987	-17.037	-0.032	-0.009
19	0.982	-17.207	-0.095	-0.034
20	0.986	-16.983	-0.022	-0.008
21	0.985	-16.520	-0.175	-0.112
22	0.986	-16.494	0.000	0.000
23	0.983	-16.674	-0.032	-0.025
24	0.972	-16.733	-0.087	-0.067
25	0.973	-16.288	0.000	0.000
26	0.954	-16.747	-0.035	-0.023
27	0.982	-15.724	0.000	0.000
28	1.005	-11.429	0.000	0.000
29	0.961	-17.062	-0.024	-0.009
30	0.949	-18.025	-0.106	-0.019

Table 4-5: Load-Flow Results from Load-Flow Software Developed

Bus	V	theta	P	Q
1	1.060	0.000	2.656	-0.168
2	1.045	-5.480	0.184	0.527
3	1.010	-14.370	-0.948	0.216
4	1.010	-12.100	-0.362	0.149
5	1.082	-14.390	0.001	0.310
6	1.071	-15.240	0.029	0.352
7	1.022	-7.673	-0.024	-0.012
8	1.015	-9.474	-0.076	-0.016
9	1.009	-11.283	0.000	0.000
10	1.001	-13.060	-0.228	-0.109
11	1.022	-14.399	0.000	0.000
12	0.999	-16.069	-0.058	-0.020
13	1.025	-15.452	-0.112	-0.075
14	1.007	-16.382	-0.062	-0.016
15	1.000	-16.403	-0.082	-0.025
16	1.006	-15.966	-0.035	-0.018
17	0.996	-16.282	-0.090	-0.058
18	0.987	-17.037	-0.032	-0.009
19	0.982	-17.207	-0.095	-0.034
20	0.986	-16.983	-0.022	-0.008
21	0.985	-16.520	-0.175	-0.112
22	0.986	-16.494	0.000	0.000
23	0.983	-16.674	-0.032	-0.025
24	0.972	-16.733	-0.087	-0.067
25	0.973	-16.288	0.000	0.000
26	0.954	-16.747	-0.035	-0.023
27	0.982	-15.724	0.000	0.000
28	1.005	-11.429	0.000	0.000
29	0.961	-17.062	-0.024	-0.009
30	0.949	-18.025	-0.106	-0.019

4.3 COMPARISON OF PV-CURVES

In this thesis research, the use of the PV curves has been identified as integral to the prediction, detection and mitigation of voltage instabilities. A detailed discussion of the significance, and the application of, the PV-curves is presented in Section 2.1.2, and again in Section 2.4.2. Thus, it is essential to construct the PV-curve at the critical bus in the IEEE 30-bus test system, to further verify the voltage stability enhancement strategy proposed in this thesis. To this end, a detailed investigation of three cases of PV-curves will be presented. Specifically, the original PV-curves, the PV-curves under ULTC actions, as well as the PV-curves under RPC, will now be developed and analyzed.

a) Standard PV Curves

In this example, the load at bus 19 is assumed to be demanding the power factor as dictated in the standard of $\cos(\arctan(0.034/0.095))$. The source impedance and feeder impedance in this example are lumped together to meet the specification according to the standard of $X=0.068\text{pu}$. The one-line diagram of this scenario is shown in Figure 4-16. The equation (4-1) is utilized to form the graph shown in Figure 4-17. The MATLAB source code to produce the curve shown in Figure 4-17 is in Appendix A.1.

$$V_L = \sqrt{\frac{V_S^2}{2} - Q_L(X_S + X_F)} \pm \sqrt{\frac{V_S^4}{4} - (X_S + X_F)^2 P_L^2 - (X_S + X_F)V_S^2 Q_L} \quad (4-1)$$

Figure 4-16: One-Line Diagram for PV Curve Comparison

Figure 4-17: Standard PV Curve for Line Connecting Bus 19 and Bus 20

b) PV Curves under ULTC Influence

Case 1: ULTC on Load Side

To see the effect that a ULTC would have on the PV curve connecting Bus 19 and Bus 20, it is assumed that there is a ULTC connected to the Bus 19 (load) side of Line 19-20. This scenario is depicted in Figure 4-18 (a). The resulting PV curve is shown in Figure 4-17, alongside the original PV curve. This new curve is formed based upon Equation (2-9), which is repeated as Equation (4-2) for convenience. The turns ratio (n) of the ULTC is assumed to 1.05. The results are in Figure 4-19. The MATLAB source

code to produce the curves shown in Figure 4-19 is in Appendix A.1. In this example, the maximum power is observed not to increase. This is due to assuming a constant PQ load in the formulation of Equation (4-2). What is instructive about this figure is that at a given load demand, the voltage profile at the bus 19 has been improved. For large ULTC actions, a greater voltage increase is expected. This is consistent with the formulations developed in Section 2.3.3.

Figure 4-18: One-Line Diagram Illustrating ULTC Placement

$$V_L = \sqrt{\frac{(nV_s)^2}{2} - Q_L n^2 (X_s + X_F)} \pm \sqrt{\frac{(nV_s)^4}{4} - (n^2 (X_s + X_F))^2 P_L^2 - n^2 (X_s + X_F) (nV_s)^2 Q_L} \quad (4-2)$$

Figure 4-19: PV Curve With ULTC on Load Side

Case 2: ULTC on Source Side

Similarly, we will now assume that there is a ULTC connected to the Bus 20 (source) side of Line 19-20. This scenario is depicted in Figure 4-18(b). The resulting PV curve is shown in Figure 4-20, alongside the original PV curve. This new curve is formed based upon Equation (4-3). The turns ratio (n) of the ULTC is assumed to 1.05. In this example, the maximum load power is observed to increase with respect to the original PV curve. In addition, the load voltage at maximum power is also observed to increase. The MATLAB source code to produce the curves shown in Figure 4-20 is in Appendix A.1.

$$V_L = \sqrt{\frac{(nV_s)^2}{2} - Q_L(n^2X_s + X_F)} \pm \sqrt{\frac{(nV_s)^4}{4} - (n^2X_s + X_F)^2 P_L^2 - (n^2X_s + X_F)(nV_s)^2 Q_L} \quad (4-3)$$

Figure 4-20: PV Curve with ULTC on Source Side

c) PV Curves under RPC Influence

Case 1: RPC is on Load Side

To see the effect that RPC would have on the PV curve connecting Bus 19 and Bus 20, it is assumed that there is a RPC is connected to the Bus 19 (load) side of Line 19-20. This scenario is depicted in Figure 4-21 (a). The resulting PV curve is shown in Figure 4-22, alongside the original PV curve. This new curve is formed based upon Equation (4-4). In this figure, the reactive power supplied by the compensator is

designed to compensate 25% of the reactive demand of the load. The MATLAB source code to produce the curves shown in Figure 4-21 is in Appendix A.1.

Figure 4-21: One-Line Diagram Illustrating RPC Placement

$$V_L = \sqrt{\frac{V_S^2}{2} - (Q_L - Q_C)(X_S + X_F)} \pm \sqrt{\frac{V_S^4}{4} - (X_S + X_F)^2 P_L^2 - (X_S + X_F)V_S^2(Q_L - Q_C)} \quad (4-4)$$

Figure 4-22: PV Curves with RPC on the Load Side

Case 2: RPC is on Source Side

To see the effect that RPC would have on the PV curve connecting Bus 19 and Bus 20, it is assumed that there is a RPC is connected to the Bus 20 (source) side of Line 19-20. This scenario is depicted in Figure 4-21 (b). The resulting PV curve is shown in Figure 4-23, alongside the original PV curve. This new curve is formed based upon which repeated in Equation (4-5). In this figure, the RPC reactance is assumed to be -

0.2Ω. This implies that
$$K_1 = \frac{1}{1 - \left(\frac{0.0628}{2}\right)(-0.2)} = 1.009, \quad \text{and}$$

$$K_2 = \frac{0.0628 - (-0.265) \left(\frac{0.0628}{2} \right)}{1 - \left(\frac{0.0628}{2} \right) (-0.265)} = 0.0595. \quad \text{The resulting PV curves are shown in}$$

Figure 4-23. These curves illustrate the RPC significantly increases the voltage profile, and the maximum power at the load end. This is consistent with the formulations developed in Section 2.3.4. The MATLAB source code to produce the curves shown in Figure 4-23 is in Appendix A.1.

Figure 4-23: PV Curves with RPC on the Source Side

$$V_L = \sqrt{\frac{(K_1 V_s)^2}{2} - Q_L K_2} \pm \sqrt{\frac{(K_1 V_s)^4}{4} - K_2^2 P_L^2 - K_2 (K_1 V_s)^2 Q_L} \quad (4-5)$$

CHAPTER 5

CONCLUSIONS

This thesis research has been successfully completed, with several contributions to the field of voltage stability in the electricity power distribution systems. This thesis presents a new concept and a new method for voltage stability enhancement and voltage instability corrective actions for distribution systems. This chapter presents a summary of the completed major research work, a list of major research contributions, and several recommended future work.

5.1 MAJOR RESEARCH WORK COMPLETED

The following presents a summary of major tasks accomplished in this thesis research.

- Developed formulation of corrective actions for voltage instability conditions on distribution feeder lines.
- Developed new strategies for carrying out corrective actions to improve the voltage stability margin for stable network conditions, to maintain stability for the network conditions prone to instability, or to restore stability for unstable network conditions.
- Developed new strategies for carrying out network-wide voltage instability corrective actions and network-wide voltage stability enhancement.
- Developed formulations for computation of distribution network performance.
- Developed a new concept of composite power for prediction of the trend of voltage stability at the feeder node of interest, and developed formulations for new stability control strategies.
- Developed a new Power System Data Test-bed for real-time simulation of power systems. Developed the DSP-based software for data acquisition from the Test-bed, and network communication between the DSP-based monitoring units and voltage stability enhancement strategy.
- Developed the windows-based software for network data acquisition of real-time post-processed data from the DSP-based monitoring units utilizing the WINSOCK API.
- Developed a robust and efficient load-flow computation software for prediction future feeder node voltages in the power system, based upon the fast-decoupled load-flow method. Developed the software for the feeder node loading predictor.

- Developed 5 detailed case studies based upon the IEEE 30-bus test system, which showcase the key actions the voltage stability enhancement strategy will utilize for voltage stability mitigations. Described a detailed set of 3 cases to verify the performance of the predictor.
- Developed a detailed test case to verify the performance of the SIMULINK-to-DSP interface. This interface simulates the link between the power system, and the DSP-based monitoring devices. RTDX data transmission was successful.
- Developed a detailed test case to verify the performance of the DSP-to-stability enhancement strategy controller. Network data transmission was successful.
- Developed a detailed test case, based upon a modified IEEE 30-bus configuration, to verify the robust performance of the developed load-flow software. A PSAT power flow simulation was utilized for the sake of comparison.
- Developed 5 detailed case studies to showcase the effect of ULTC and RPC actions on the PV-curves of the critical bus 19 in the IEEE 30-bus test system

5.2 MAJOR RESEARCH CONTRIBUTIONS

The following lists the major contributions from this thesis research.

1. ***New strategies for corrective actions to improve the voltage stability:*** Developed new strategies for carrying out corrective actions to improve the voltage stability margin for stable network conditions, to maintain stability for the network conditions prone to instability, or to restore stability for unstable network conditions.
2. ***New strategies for network-wide voltage instability corrective actions:*** Developed new strategies for carrying out network-wide voltage instability corrective actions and network-wide voltage stability enhancement.
3. ***New concept of composite power for prediction of voltage stability trend:*** Developed a new concept of composite power for prediction of the trend of voltage stability at the feeder node of interest, and developed formulations for new stability control strategies.
4. ***New power system data test-bed for real-time power distribution simulation:*** Developed a new Power System Data Test-bed for real-time simulation of power systems, and developed the DSP-based software for data acquisition from the Test-bed, and network communication between the DSP-based monitoring units and voltage stability enhancement strategy.
5. ***New real-time power flow computation software for loading prediction:*** Developed a robust power flow computation software for prediction future feeder node voltages in the power system, based upon the fast-decoupled load-flow method, and developed the software for the feeder node loading predictor.

5.3 Future Work

The following presents recommended future work with a focus on field tests for the feasibility and effectiveness of the strategies presented in this thesis for voltage stability enhancement and voltage instability corrective actions in power distribution systems. More specifically,

Field tests of formulation for real-time computation of distribution system performance:

This thesis strongly recommends to carrying out field tests to verify the correctness of the formulation and software algorithm for real-time computation of distribution system performance.

Field tests of formulation for predictions of loading and their effects on voltage stability: This thesis also strongly recommends to conducting field test to validate the effectiveness of the real-time loading prediction in the live operating distribution system.

Additional cases studies: This thesis recommends to carrying out additional cases studies for severe voltage instability conditions that requires a combination of corrective actions for restoring the instability conditions.

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APPENDIX A

SOURCE CODE AND SIMULATION MODEL FOR VOLTAGE STABILITY ENHANCEMENT SYSTEM

APPENDIX A1: SOURCE-CODE FOR PREDICTOR PROGRAM, VOLTAGE STABILITY ANALYSIS, AND VOLTAGE STABILITY CORRECTIVE ACTIONS

```
% Clear workspace and command window
clear; clc;
% Generate test waveform
w=0.01;
tp = 0.01;
tend=2400;
t=0:tp:tend;
P = (0.5 + 0.00001*t + 0.01*sin(w*t)) ;

% Sample waveform
Ts=5;
for k=1:floor((tend/Ts))
    tk3(k) = t((k-1)*Ts/tp + 1);
    Pk3(k) = P((k-1)*Ts/tp + 1);
end;
% initialize prediction parameters
Pm3(1) = 0;
Pm3(2) = 0;
% Calculate the next voltage output
for i=3:(floor((tend/Ts))-1)
    Pm3(i+1) = 3*Pk3(i) - 3*Pk3(i-1) + Pk3(i-2);
end;
% Generate graphs
plot(t/60,P,tk3(:)/60,Pm3(:));
axis([0 2400/60 0.45 0.55]);
xlabel('t [min]');
ylabel('P [pu]');
legend('P_{measured}', 'P_{predicted, T_s=5s}');
grid on;
```

Figure A1-1: Source Code For Predictor Program in Figure 4-7

```

% Clear workspace and command window
clear; clc;
% Generate test waveform
w=0.01; tp = 0.01; tend=2400; t=0:tp:tend;
P = (0.5 + 0.00001*t + 0.01*sin(w*t)) ;
% Sample waveform
Ts=40;
for k=1:floor((tend/Ts))
    tk1(k) = t((k-1)*Ts/tp + 1);
    Pk1(k) = P((k-1)*Ts/tp + 1);
end;
% initialize prediction parameters
Pm1(1) = 0;
Pm1(2) = 0;
% Calculate the next voltage output
for i=3:(floor((tend/Ts))-1)
    Pm1(i+1) = 3*Pk1(i) - 3*Pk1(i-1) + Pk1(i-2);
end;
% Sample waveform
Ts=20;
for k=1:floor((tend/Ts))
    tk2(k) = t((k-1)*Ts/tp + 1);
    Pk2(k) = P((k-1)*Ts/tp + 1);
end;
% initialize prediction parameters
Pm2(1) = 0;
Pm2(2) = 0;
% Calculate the next voltage output
for i=3:(floor((tend/Ts))-1)
    Pm2(i+1) = 3*Pk2(i) - 3*Pk2(i-1) + Pk2(i-2);
end;
% Sample waveform
Ts=5;
for k=1:floor((tend/Ts))
    tk3(k) = t((k-1)*Ts/tp + 1);
    Pk3(k) = P((k-1)*Ts/tp + 1);
end;
% initialize prediction parameters
Pm3(1) = 0;
Pm3(2) = 0;
% Calculate the next voltage output
for i=3:(floor((tend/Ts))-1)
    Pm3(i+1) = 3*Pk3(i) - 3*Pk3(i-1) + Pk3(i-2);
end;
% Generate graphs
plot(t/60,P,tk1(:)/60,Pm1(:),tk2(:)/60,Pm2(:),tk3(:)/60,Pm3(:));
axis([0 2400/60 0.45 0.55]);
xlabel('t [min]');
ylabel('P [pu]');
legend('P_{measured}', 'P_{predicted, T_s=40s}', 'P_{predicted, T_s=20s}', 'P_{predicted, T_s=5s}');
grid on;

```

Figure A1-2: Source Code for Predictor Program in Figure 4-8


```

% Clear workspace and command window
clear; clc;
% Generate test waveform
w=0.01; tp = 0.01; tend=2400; t=0:tp:tend;
P = (0.5 + 0.00001*t + 0.01*sin(w*t)).*(t<1200) + (-0.01.*(t-1200) +
0.506).*(t>=1200);
% Sample waveform
Ts=40;
for k=1:floor((tend/Ts))
    tk1(k) = t((k-1)*Ts/tp + 1);
    Pk1(k) = P((k-1)*Ts/tp + 1);
end;
% initialize prediction parameters
Pm1(1) = 0;
Pm1(2) = 0;
% Calculate the next voltage output
for i=3:(floor((tend/Ts))-1)
    Pm1(i+1) = 3*Pk1(i) - 3*Pk1(i-1) + Pk1(i-2);
end;
% Sample waveform
Ts=20;
for k=1:floor((tend/Ts))
    tk2(k) = t((k-1)*Ts/tp + 1);
    Pk2(k) = P((k-1)*Ts/tp + 1);
end;
% initialize prediction parameters
Pm2(1) = 0;
Pm2(2) = 0;
% Calculate the next voltage output
for i=3:(floor((tend/Ts))-1)
    Pm2(i+1) = 3*Pk2(i) - 3*Pk2(i-1) + Pk2(i-2);
end;
% Sample waveform
Ts=5;
for k=1:floor((tend/Ts))
    tk3(k) = t((k-1)*Ts/tp + 1);
    Pk3(k) = P((k-1)*Ts/tp + 1);
end;
% initialize prediction parameters
Pm3(1) = 0;
Pm3(2) = 0;
% Calculate the next voltage output
for i=3:(floor((tend/Ts))-1)
    Pm3(i+1) = 3*Pk3(i) - 3*Pk3(i-1) + Pk3(i-2);
end;
% Generate graphs
plot(t/60,P,tk1(:)/60,Pm1(:),tk2(:)/60,Pm2(:),tk3(:)/60,Pm3(:));
axis([0 2400/60 0.45 0.55]);
xlabel('t [min]');
ylabel('P [pu]');
legend('P_{measured}', 'P_{predicted, T_s=40s}', 'P_{predicted, T_s=20s}', 'P_{predicted, T_s=5s}');
grid on;

```

Figure A1-3: Source Code For Predictor Program in Figure 4-9

```

Vs=1;
Xs=0;
Xf=0.068;

% PF = 0.9415 lagging
tanPHI = 0.034/0.095;

% Solving the inequality in Equation (2-5) to find the maximum power
a = 1;
b = Vs^2*tanPHI/(Xs+Xf);
c = -Vs^4/4/(Xs+Xf)^2;
Plmax = (-b + sqrt(b^2 - 4*a*c))/2/a;
Pl = 0:0.00001:Plmax;
Ql = tanPHI*Pl;

% Upper Portion of Curve
Vlu = sqrt( Vs^2/2 - Ql.*(Xs+Xf) + sqrt( Vs^4/4 - (Xs+Xf)^2*Pl.^2 -
(Xs+Xf)*Vs^2.*Ql));

% Lower Portion of Curve
Vll = sqrt( Vs^2/2 - Ql.*(Xs+Xf) - sqrt( Vs^4/4 - (Xs+Xf)^2*Pl.^2 -
(Xs+Xf)*Vs^2.*Ql));
plot(Pl/Plmax,Vlu);
hold on;
plot(Pl/Plmax,Vll);
ylabel('V_l / V_s [pu]');
xlabel('P_l / P_{l,max} [pu]');
grid on;

```

Figure A1-4: Source Code for Standard PV Curve Generation

```

Vs=1;
Xs=0.068/2;
Xf=0.068/2;

% PF = 0.9415 lagging
tanPHI = 0.034/0.095;

% Solving the inequality in Equation (2-5) to find the maximum power
a = 1;
b = Vs^2*tanPHI/(Xs+Xf);
c = -Vs^4/4/(Xs+Xf)^2;
Plmax = (-b + sqrt(b^2 - 4*a*c))/2/a;

Pl = 0:0.005:Plmax;
Ql = tanPHI*Pl;

% Upper Portion of original curve
Vlu = sqrt( Vs^2/2 - Ql.*(Xs+Xf) + sqrt (Vs^4/4 - (Xs+Xf)^2*Pl.^2 -
(Xs+Xf)*Vs^2.*Ql));

% Lower Portion of original curve
Vll = sqrt( Vs^2/2 - Ql.*(Xs+Xf) - sqrt (Vs^4/4 - (Xs+Xf)^2*Pl.^2 -
(Xs+Xf)*Vs^2.*Ql));

Vs=1.05;
Xs=1.05^2*Xs;
Xf=1.05^2*Xf;

% Solving the inequality in Equation (2-5) to find the maximum power
a = 1;
b = Vs^2*tanPHI/(Xs+Xf);
c = -Vs^4/4/(Xs+Xf)^2;
Plmaxm = (-b + sqrt(b^2 - 4*a*c))/2/a;

Plm = 0:0.005:Plmaxm;
Qlm = tanPHI*Plm;

% Upper Portion of modified curve
Vlmu = sqrt( Vs^2/2 - Qlm.*(Xs+Xf) + sqrt (Vs^4/4 - (Xs+Xf)^2*Plm.^2 -
(Xs+Xf)*Vs^2.*Qlm));
% Lower Portion of modified curve
Vlml = sqrt( Vs^2/2 - Qlm.*(Xs+Xf) - sqrt (Vs^4/4 - (Xs+Xf)^2*Plm.^2 -
(Xs+Xf)*Vs^2.*Qlm));

plot(Pl/Plmax,Vlu,Plm/Plmax,Vlmu);
hold on;
plot(Pl/Plmax,Vll,Plm/Plmax,Vlml);
ylabel('V_l / V_s [pu]');
xlabel('P_l / P_{l,max} [pu]');
grid on;
axis([0 1.05 0 1.05]);

```

Figure A1-5: Source Code for PV Curve Generation with ULTC on Load Side

```

Vs=1;
Xs=0.068/2;
Xf=0.068/2;
% PF = 0.9415 lagging
tanPHI = 0.034/0.095;

% Solving the inequality in Equation (2-5) to find the maximum power
a = 1;
b = Vs^2*tanPHI/(Xs+Xf);
c = -Vs^4/4/(Xs+Xf)^2;
Plmax = (-b + sqrt(b^2 - 4*a*c))/2/a;

Pl = 0:0.005:Plmax;
Ql = tanPHI*Pl;

% Upper Portion of original curve
Vlu = sqrt( Vs^2/2 - Ql.*(Xs+Xf) + sqrt (Vs^4/4 - (Xs+Xf)^2*Pl.^2 -
(Xs+Xf)*Vs^2.*Ql));

% Lower Portion of original curve
Vll = sqrt( Vs^2/2 - Ql.*(Xs+Xf) - sqrt (Vs^4/4 - (Xs+Xf)^2*Pl.^2 -
(Xs+Xf)*Vs^2.*Ql));

Vs=1.05;
Xs=1.05^2*Xs;
Xf=1.05^2*Xf;
% Solving the inequality in Equation (2-5) to find the maximum power
a = 1;
b = Vs^2*tanPHI/(Xs+Xf);
c = -Vs^4/4/(Xs+Xf)^2;
Plmaxm = (-b + sqrt(b^2 - 4*a*c))/2/a;

Plm = 0:0.005:Plmaxm;
Qlm = tanPHI*Plm;

% Upper Portion of modified curve
Vlmu = sqrt( Vs^2/2 - Qlm.*(Xs+Xf) + sqrt (Vs^4/4 - (Xs+Xf)^2*Plm.^2 -
(Xs+Xf)*Vs^2.*Qlm));

% Lower Portion of modified curve
Vlml = sqrt( Vs^2/2 - Qlm.*(Xs+Xf) - sqrt (Vs^4/4 - (Xs+Xf)^2*Plm.^2 -
(Xs+Xf)*Vs^2.*Qlm));

plot(Pl/Plmax,Vlu,Plm/Plmax,Vlmu);
hold on;
plot(Pl/Plmax,Vll,Plm/Plmax,Vlml);

ylabel('V_l / V_s [pu]');
xlabel('P_l / P_{l,max} [pu]');
grid on;
axis([0 1.05 0 1.05]);

```

Figure A1-6: Source Code for PV Curve Generation with ULTC on Source Side

```

clear; clc;
Vs=1;
Xs=0.068/2;
Xf=0.068/2;
% PF = 0.9415 lagging
tanPHI = 0.034/0.095;

% Solving the inequality in Equation (2-5) to find the maximum power
a = 1;
b = Vs^2*tanPHI/(Xs+Xf);
c = -Vs^4/4/(Xs+Xf)^2;
Plmax = (-b + sqrt(b^2 - 4*a*c))/2/a;

Pl = 0:0.005:Plmax;
Ql = tanPHI*Pl;

% Upper Portion of original curve
Vlu = sqrt( Vs^2/2 - Ql.*(Xs+Xf) + sqrt (Vs^4/4 - (Xs+Xf)^2*Pl.^2 -
(Xs+Xf)*Vs^2.*Ql));

% Lower Portion of original curve
Vll = sqrt( Vs^2/2 - Ql.*(Xs+Xf) - sqrt (Vs^4/4 - (Xs+Xf)^2*Pl.^2 -
(Xs+Xf)*Vs^2.*Ql));

% Solving the inequality in Equation (2-5) to find the maximum power
a = 1;
b = Vs^2*tanPHI/(Xs+Xf);
c = -Vs^4/4/(Xs+Xf)^2;
Plmaxm = (-b + sqrt(b^2 - 4*a*c))/2/a;

Plm = 0:0.005:(Plmaxm*2.5);
Qlm = tanPHI*Plm;
Qlc = 0.25*Qlm;

% Upper Portion of modified curve
Vlmu = sqrt( Vs^2/2 - (Qlm-Qlc).*(Xs+Xf) + sqrt (Vs^4/4 -
(Xs+Xf)^2*Plm.^2 - (Xs+Xf)*Vs^2.*(Qlm-Qlc)));

% Lower Portion of modified curve
Vlml = sqrt( Vs^2/2 - (Qlm-Qlc).*(Xs+Xf) - sqrt (Vs^4/4 -
(Xs+Xf)^2*Plm.^2 - (Xs+Xf)*Vs^2.*(Qlm-Qlc)));

plot(Pl/Plmax,Vlu,Plm/Plmax,Vlmu);
hold on;
plot(Pl/Plmax,Vll,Plm/Plmax,Vlml);

ylabel('V_l / V_s [pu]');
xlabel('P_l / P_{l,max} [pu]');
grid on;
axis([0 1.09 0 1.05]);

```

Figure A1-7: Source Code for PV Curve Generation with RPC on Load Side

```

clear; clc;
Vs=1;
Xs=0.068/2;
Xf=0.068/2;
% PF = 0.9415 lagging
tanPHI = 0.034/0.095;
% Solving the inequality in Equation (2-5) to find the maximum power
a = 1;
b = Vs^2*tanPHI/(Xs+Xf);
c = -Vs^4/4/(Xs+Xf)^2;
Plmax = (-b + sqrt(b^2 - 4*a*c))/2/a;
Pl = 0:0.005:Plmax;
Ql = tanPHI*Pl;
% Upper Portion of original curve
Vlu = sqrt( Vs^2/2 - Ql.*(Xs+Xf) + sqrt( Vs^4/4 - (Xs+Xf)^2*Pl.^2 -
(Xs+Xf)*Vs^2.*Ql));

% Lower Portion of original curve
Vll = sqrt( Vs^2/2 - Ql.*(Xs+Xf) - sqrt( Vs^4/4 - (Xs+Xf)^2*Pl.^2 -
(Xs+Xf)*Vs^2.*Ql));

Xc=0.265;
K1 = 1/(1-Xs*Xc);
K2 = (Xs+Xf-Xc*Xf)/(1-Xs*Xc);
Vs = K1*Vs;

% Solving the inequality in Equation (2-5) to find the maximum power
a = 1;
b = Vs^2*tanPHI/(Xs+Xf);
c = -Vs^4/4/(Xs+Xf)^2;
Plmaxm = (-b + sqrt(b^2 - 4*a*c))/2/a;

Plm = 0:0.005:(Plmaxm*2.5);
Qlm = tanPHI*Plm;

% Upper Portion of modified curve
Vlmu = sqrt( Vs^2/2 - (Qlm).*(K2) + sqrt( Vs^4/4 - (K2)^2*Plm.^2 -
(K2)*Vs^2.*(Qlm)));

% Lower Portion of modified curve
Vlml = sqrt( Vs^2/2 - (Qlm).*(K2) - sqrt( Vs^4/4 - (K2)^2*Plm.^2 -
(K2)*Vs^2.*(Qlm)));

plot(Pl/Plmax,Vlu,Plm/Plmax,Vlmu);
hold on;
plot(Pl/Plmax,Vll,Plm/Plmax,Vlml);

ylabel('V_l / V_s [pu]');
xlabel('P_l / P_{l,max} [pu]');
grid on;
axis([0 1.16 0 1.05]);

```

Figure A1-8: Source Code for PV Curve Generation with RPC on Source Side

APPENDIX A2: SOURCE-CODE/DIAGRAMS FOR MATLAB-TO-DSP COMMUNICATION

```
% Open CCS and make visible
target = ccstdsp();
target.visible(1);

% Load Project
target.cd('C:\CCStudio_v3.1\MyProjects\dsptest\dsp_test');
target.open('DSP_TEST.pjt');

target.build();

% % Load Program into DSP memory
target.cd('C:\CCStudio_v3.1\MyProjects\dsptest\dsp_test\Debug');
target.load('DSP_TEST.out');

% % Initialize RTDX channels
rx = target.rtdx;
configure(rx,1024,4,'continuous');
rx.enable;

% % Open Host and Target Channels
open(rx, 'ochan', 'r' );
open(rx, 'ichan', 'w' );

% Clear Channel Buffers
flush(rx,'ochan');
flush(rx,'ichan');

% Execute DSP Code
target.run();
```

Figure A2-1: Source Code for execute_CCS.m file

<pre> Ts=1e-3; n=30; Vbase=33e3; Sbase=100e6; fbase=60; wbase=2*pi*fbase; Zbase=Vbase*Vbase/Sbase/80; Rbase=Zbase; Lbase=Zbase/wbase; Cbase=1/(Zbase*wbase); P2 = 21.7*Sbase; P3 = 94.2*Sbase; P4 = 30*Sbase; P7 = 2.4*Sbase; P8 = 7.6*Sbase; P10 = 22.8*Sbase; P12 = 5.8*Sbase; P13 = 11.2*Sbase; P14 = 6.2*Sbase; P15 = 8.2*Sbase; P16 = 3.5*Sbase; P17 = 9*Sbase; P18 = 3.2*Sbase; P19 = 9.5*Sbase*3; P20 = 2.2*Sbase; P21 = 17.5*Sbase; P23 = 3.2*Sbase; P24 = 8.7*Sbase; P26 = 3.5*Sbase; P29 = 2.4*Sbase; </pre>	<pre> P30 = 10.6*Sbase; Q2 = 12.7*Sbase; Q3 = 19*Sbase; Q4 = 30*Sbase; Q7 = 1.2*Sbase; Q8 = 1.6*Sbase; Q10 = 10.9*Sbase; Q12 = 2*Sbase; Q13 = 7.5*Sbase; Q14 = 1.6*Sbase; Q15 = 2.5*Sbase; Q16 = 1.8*Sbase; Q17 = 5.8*Sbase; Q18 = 0.9*Sbase; Q19 = 3.04*Sbase*3; Q20 = 0.77*Sbase; Q21 = 11.2*Sbase; Q23 = 1.6*Sbase; Q24 = 6.7*Sbase; Q26 = 2.3*Sbase; Q29 = 0.9*Sbase; Q30 = 1.9*Sbase; t1215s=1000; mP=1.6; mQ=1.6; t1020=1000; t1020s=1000; t1215=1000; tcomp = 1000; execute_CCS; </pre>
--	--

Figure A2-2: Source Code for initialization.m

```

clear;
clc;
% Initialize Variables
initilization;
nsamps=1000;
[T,X,Y] = sim('bus30_dsp');
for i=1:nsamps
    writemsg(rx, 'ichan', single(V(i,19)) );
end;
plot(t,V(:,19));
xlabel('t [s]');
ylabel('V19 [pu]');

```

Figure A2-3: Source Code for simcont_dsp.m

Figure A2-4: SIMULINK Block Diagram for `bus30_dsp.mdl`

```

#include <stdio.h>
#include <stdlib.h>
#include <rtdx.h>
#include "target.h"
#define numvalues 1000

RTDX_CreateOutputChannel(ochan);    // Output Channel
RTDX_CreateInputChannel(ichan);    // Input Channel

float buff[numvalues];    // Storage for recieved data
float indata;

void main( void )
{
    unsigned int outdata=10; // Handshaking value, arbitrary
    int i;                  // Loop Counter

    TARGET_INITIALIZE(); // Initialize C6416T DSP Board

    printf("Target Initialization Successfu\r\n");
    /* Enable the output channel, "ochan" */
    RTDX_enableOutput(&ochan);
    RTDX_enableInput(&ichan);
    printf("Channel Initialization Successfu\r\n");
    printf("Getting ready to send data...\r\n");
    for (i = 0 ; i < numvalues ; i++) {
        // Receive Bus 19 Data from host
        while ( RTDX_read( &ichan, &indata, sizeof(indata) ) != sizeof(indata) );
        printf("data received from host %i\r\n",indata);
        buff[i] = indata;
        // Send Handshake data back to host
        RTDX_write( &ochan, &outdata, sizeof(outdata));
        printf("data sent to host\r\n"); }
    /* Disable the output channel, "ochan" */
    RTDX_disableOutput(&ochan);
    RTDX_disableInput(&ichan);
    printf("\r\nDone, see waveforms in buff ");
}

```

Figure A2-5: DSP Source Code for RTDX Data Acquisition

APPENDIX A3: SOURCE-CODE/DIAGRAMS FOR DSP-TO-CONTROLLER COMMUNICATION

```
% Open CCS and make visible
target = ccstdsp();
target.visible(1);

% Load Project
target.cd('C:\CCStudio_v3.1\MyProjects\dsptest');
target.open('DSP_TEST.pjt');

target.build();

% Load Program into DSP memory
target.cd('C:\CCStudio_v3.1\MyProjects\dsptest\Debug');
target.load('DSP_TEST.out');

% Initialize RTDX channels
rx = target.rtdx;
configure(rx,1024,4,'continuous');
rx.enable;

% Open Host and Target Channels
open(rx, 'ochan', 'r' );
open(rx, 'ichan', 'w' );

% Clear Channel Buffers
flush(rx,'ochan');
flush(rx,'ichan');

% Execute DSP Code
target.run();
```

Figure A3-1: Source Code for execute_CCS.m file

<pre> Ts=1e-3; n=30; Vbase=33e3; Sbase=100e6; fbase=60; wbase=2*pi*fbase; Zbase=Vbase*Vbase/Sbase/80; Rbase=Zbase; Lbase=Zbase/wbase; P2 = 21.7*Sbase; P3 = 94.2*Sbase; P4 = 30*Sbase; P7 = 2.4*Sbase; P8 = 7.6*Sbase; P10 = 22.8*Sbase; P12 = 5.8*Sbase; P13 = 11.2*Sbase; P14 = 6.2*Sbase; P15 = 8.2*Sbase; P16 = 3.5*Sbase; P17 = 9*Sbase; P18 = 3.2*Sbase; P19 = 9.5*Sbase*3; P20 = 2.2*Sbase; P21 = 17.5*Sbase; P23 = 3.2*Sbase; P24 = 8.7*Sbase; P26 = 3.5*Sbase; P29 = 2.4*Sbase; P30 = 10.6*Sbase; Q2 = 12.7*Sbase; </pre>	<pre> Q3 = 19*Sbase; Q4 = 30*Sbase; Q7 = 1.2*Sbase; Q8 = 1.6*Sbase; Q10 = 10.9*Sbase; Q12 = 2*Sbase; Q13 = 7.5*Sbase; Q14 = 1.6*Sbase; Q15 = 2.5*Sbase; Q16 = 1.8*Sbase; Q17 = 5.8*Sbase; Q18 = 0.9*Sbase; Q19 = 3.04*Sbase*3; Q20 = 0.77*Sbase; Q21 = 11.2*Sbase; Q22 = 0*Sbase; Q23 = 1.6*Sbase; Q24 = 6.7*Sbase; Q25 = 0*Sbase; Q26 = 2.3*Sbase; Q29 = 0.9*Sbase; Q30 = 1.9*Sbase; mP=1.6; mQ=1.6; t1020=1000; t1020s=1000; t1215=1000; t1215s=1000; tcomp = 1000; execute_CCS; </pre>
--	---

Figure A3-2: Source Code for initialization.m

<pre> clear; clc; % Initialize Variables initilization; nsamps=1000; [T,X,Y] = sim('bus30_dsp1'); for i=1:30 writemsg(rx, 'ichan', single(V(length(V),i))); writemsg(rx, 'ichan', single(theta(length(theta),i)-30)); writemsg(rx, 'ichan', single(P(length(P),i))); writemsg(rx, 'ichan', single(Q(length(Q),i))); while msgcount(rx,'ochan') == 0 end readmsg(rx, 'ochan', 'int16'); end; </pre>

Figure A3-3: Source Code for simcont_dsp.m

Warning:
Direct access
power

Figure A3-4: SIMULINK Diagram

```

#include <stdio.h>
#include <stdlib.h>
#include <rtdx.h>
#include "target.h"
#ifndef CHIP_6416
#define CHIP_6416
#endif
#include "csl.h"          /* chip support library */
#include "csl_irq.h"
#include "csl_timer.h"
#include "csl_cache.h"
#include "dsknet.h"       /* network support */
#include "dskemif.h"      /* EMIF setting */
#include "netconfig.h"    /* network configuration */
#define numvalues 1000
RTDX_CreateOutputChannel(ochan);    // Output Channel
RTDX_CreateInputChannel(ichan);     // Input Channel
float V[numvalues];                // Storage for recieved voltage
float theta[numvalues];            // Storage for recieved angle
float P[numvalues];                // Storage for recieved active demand
float Q[numvalues];                // Storage for recieved reactive demand
float indata;
unsigned int dsp_clock = 1000000000;
SOCKET *tcp_server;
char tcp_rx[16];                  /* buffer for TCP requests */
char tcp_tx[32];
unsigned int i=0;
int32_t tcp_call_back (SOCKET *so, void *data, u_int32_t len, u_int32_t ec)
{
    switch (ec)
    {
        case 0:
            printf("Message Received\r\n");

            sprintf(tcp_tx,"%f",V[i]);
            printf("\r\nMessage to send is %s\r\n",tcp_tx);
            net_send (so, tcp_tx, strlen(tcp_tx));
            sprintf(tcp_tx,"%f",theta[i]);
            printf("\r\nMessage to send is %s\r\n",tcp_tx);
            net_send (so, tcp_tx, strlen(tcp_tx));
            sprintf(tcp_tx,"%f",P[i]);
            printf("\r\nMessage to send is %s\r\n",tcp_tx);
            net_send (so, tcp_tx, strlen(tcp_tx));
            sprintf(tcp_tx,"%f",Q[i]);
            printf("\r\nMessage to send is %s\r\n",tcp_tx);
            net_send (so, tcp_tx, strlen(tcp_tx));
    }
}

```

```

        if (i==29)
            i=0;
        else
            i++;
        break;

    default:
        printf ("socket error : %s\r\n", error_tab[so -> error_code]);
        break;
    }
    return (1);
}

void link_status (unsigned char mode)
{
    printf ("\r\n Link status changed: ");
    switch (mode)
    {
        case 0xff:
            printf ("No Link\r\n");
            break;
        default:
            printf ("Linked at %dMbit %s duplex\r\n",
                (mode & SPEED_100) ? 100:10,
                (mode & FULL_DUPLEX) ? "full":"half");
            break;
    }
}

int InitializeNetwork (void)
{
    u_int16_t ret;
    initialize smc91c111
    possible values
    mode: FDX_100, FDX_10, HDX_100, HDX_10, AUTO_NEG
    ret = dsk_init ( network_mode, dsp_clock, link_status);
    if ( ret == 0 )
    {
        return (1);
    }

    printf (".");
    if ( !net_init (dsp_ip_addr, dhcp_setting, dns_server_ip, dns_setting))
        return (2); // out of memory
    printf (".");
    if ( install_icmp_socket (1024) == NULL )
    {

```

```

    return (3);
}
printf (".");
tcp_server = socket_open (ANY_ADDRESS,
                          ANY_PORT,
                          1061,
                          DATATYPE_CHAR,
                          TCP_INIT_FUNC);
if ( tcp_server == NULL )
{
    exit (5);
}
printf (".");
socket_define_callback (tcp_server, tcp_call_back, tcp_rx, sizeof(tcp_rx));
printf (".");
return (0);
}
void main( void )
{
    unsigned int outdata=10; // Handshaking value, arbitrary
    int i;// Loop Counter
    TARGET_INITIALIZE(); // Initialize C6416T DSP Board
    printf("Target Initialization Sucessful\r\n");
    /* Enable the output channel, "ochan" */
    RTDX_enableOutput(&ochan);
    RTDX_enableInput(&ichan);
    prprintf("Channel Initialization Sucessful\r\n");
    init_emif (dsp_clock);
    printf("External Memory Interface Initialization Sucessful\r\n");
    CSL_init();
    printf("Chip Support Library Enabled\r\n");
    if ( InitializeNetwork () )
    {
        printf("Error initialilizing networking, exiting\r\n");
        exit (1);
    }
    else
        printf("Network enabled sucessfully\r\n");
    printf("Getting data from testbed...\r\n");
    for (i = 0 ; i < 30 ; i++)
    {
        // Receive Bus 19 Data from host
        while ( RTDX_read( &ichan, &indata, sizeof(indata) ) != sizeof(indata) );
        printf("data received from host %i\r\n",indata);
        V[i] = indata;
        while ( RTDX_read( &ichan, &indata, sizeof(indata) ) != sizeof(indata) );
    }
}

```



```

printf("data received from host %i\r\n",indata);
theta[i] = indata;
while ( RTDX_read( &ichan, &indata, sizeof(indata) ) != sizeof(indata) );
printf("data received from host %i\r\n",indata);
P[i] = indata;

while ( RTDX_read( &ichan, &indata, sizeof(indata) ) != sizeof(indata) );
printf("data received from host %i\r\n",indata);
Q[i] = indata;
// Send Handshake data back to host
RTDX_write( &ochan, &outdata, sizeof(outdata));
printf("data sent to host\r\n");
}
RTDX_disableOutput(&ochan);
RTDX_disableInput(&ichan);
printf("\r\nDone, see data in V, theta, P, and Q buffers ");
while (1)
{
    net_isq();
}
}

```

Figure A3-5: DSP Source Code for DSP-to-Controller Communication

```

#include <stdio.h>
#include <stdlib.h>
#include <winsock.h>
#include "math.h"
#define M_PI 3.14159265
#define w 2.0*M_PI*60
#define omega 376.99
#define PRINTERROR(s) fprintf(stderr, "\n%: %d\n", s, WSAGetLastError());

// Function prototype
void networkManagement();
static double V[30];
static double theta[30];
static double P[30];
static double Q[30];
FILE *outfile;
void main()
{
    // Thread Data
    char ch;
    int status;
    WORD wVersionRequested = MAKEWORD(1,1);
    WSADATA wsaData;

```

```

int nRet;
short nPort;
// Initialize WinSock
nRet = WSAStartup(wVersionRequested, &wsaData);
if (wsaData.wVersion != wVersionRequested)
{
    fprintf(stderr, "\n Wrong version\n");
    return;
}
outfile = fopen("out.txt", "w");
networkManagement();
WSACleanup();
fclose(outfile);
}

void networkManagement()
{
    printf("\nClient connecting to server: 192.168.168.200 on port: 1061\n\n");
    fprintf(outfile, "\nClient connecting to server: 192.168.168.200 on port: 1061\n\n");

    LPHOSTENT lpHostEntry;

    lpHostEntry = gethostbyname("192.168.168.200");
    if (lpHostEntry == NULL)
    {
        PRINTERROR("gethostbyname()");
        return;
    }

    SOCKET theSocket;
    theSocket = socket(AF_INET,                // Address family
                      SOCK_STREAM,            // Socket type
                      IPPROTO_TCP);           // Protocol
    if (theSocket == INVALID_SOCKET)
    {
        PRINTERROR("socket()");
        return;
    }

    u_long* dataSize;
    long blockingMode = 1;
    SOCKADDR_IN saServer;
    saServer.sin_family = AF_INET;
    saServer.sin_addr = *((LPIN_ADDR)*lpHostEntry->h_addr_list); // ^ Server's
address
    saServer.sin_port = htons(1061);                // Port number
    int nRet;
    nRet = connect(theSocket, (LPSOCKADDR)&saServer, sizeof(struct sockaddr));

```

```

if (nRet == SOCKET_ERROR)
{
    PRINTERROR("socket()");
    closesocket(theSocket);
    return;
}
char sBuf[16];
char rBuf[32];
strcpy(sBuf, "Start");
for (int i=0 ; i<30 ; i++)
{
    nRet = send(theSocket, sBuf, sizeof(sBuf), 0);
    if (nRet == SOCKET_ERROR)
    {
        PRINTERROR("send()");
        closesocket(theSocket);
        return;
    }
    printf("Bus %d: ",i+1);
    fprintf(outfile,"Bus %d: ",i+1);
    nRet = recv(theSocket, rBuf, sizeof(rBuf), 0);
    if (nRet == SOCKET_ERROR)
    {
        PRINTERROR("recv()");
        closesocket(theSocket);
        return;
    }
    V[i] = (double)atof(rBuf);
    printf("V = %lf pu", V[i]);
    fprintf(outfile,"V = %lf pu", V[i]);
    nRet = recv(theSocket, rBuf, sizeof(rBuf), 0);
    if (nRet == SOCKET_ERROR)
    {
        PRINTERROR("recv()");
        closesocket(theSocket);
        return;
    }
    theta[i] = (double)atof(rBuf);
    printf(" theta = %lf deg",theta[i]);
    fprintf(outfile," theta = %lf deg",theta[i]);
    nRet = recv(theSocket, rBuf, sizeof(rBuf), 0);
    if (nRet == SOCKET_ERROR)
    {
        PRINTERROR("recv()");
        closesocket(theSocket);
        return;
    }
}

```

```

    }
    P[i] = (double)atof(rBuf);
    printf(" P = %lf pu,",P[i]);
    fprintf(outfile," P = %lf pu,",P[i]);
    nRet = recv(theSocket, rBuf, sizeof(rBuf), 0);
    if (nRet == SOCKET_ERROR)
    {
        PRINTERROR("recv()");
        closesocket(theSocket);
        return;
    }
    Q[i] = (double)atof(rBuf);
    printf(" Q = %lf pu\r\n",Q[i]);
    fprintf(outfile, " Q = %lf pu\r\n",Q[i]);
}
closesocket(theSocket);
return;
}

```

Figure A3-6: Source Code for Controller Program

APPENDIX A4: SOURCE-CODE/DIAGRAMS FOR LOAD-FLOW SOFTWARE

```
#include <stdio.h>
#include <math.h>
#include <stdlib.h>
#define M_PI 3.14159265
#define ep 1e-3
#define eq 1e-3
int sizeY = 30;
int numLoad = 24;
int numTx=6;
int numGen=0;
using namespace std;
FILE *myfile;
FILE *outfile;
// Current Data
double** Binv;
double** magY;
double** angY;
void storeArray(double** x, int bounds);
void storeVector(double* x, int bounds);
double *Vbus,*thetabus,*Pbus,*Qbus;
// Return 1 if convergent, 0 if not
int loadFlow(int numGen, int numTx,int numLoad, double** magY, double** angY,
double** Binv, double* Vbus, double* thetabus, double* Pbus, double* Qbus);
double maxVector(double* x, int start, int end);
void init();
int main()
{
    init();
    printf("\r\n Hello World\r\n");
    loadFlow(numGen,numTx,numLoad,magY,angY,Binv,Vbus,thetabus,Pbus,Qbus);
    printf("\r\n Done Loadflow\r\n");
    fclose(outfile);
    system("pause");
    return 0;
}
int loadFlow(int numGen, int numTx, int numLoad, double** magY, double** angY,
double** Binv, double* Vbus, double* thetabus, double* Pbus, double* Qbus)
{
    int KP,KQ;
    int i=0, k=0,j=0, numIts;
    double tempsum;
    double *delP, *delQ;
    int sizeY=numGen+numTx+numLoad;
```

```

delP = (double *)malloc(numLoad*sizeof(double));
delQ = (double *)malloc(numLoad*sizeof(double));
//Step 1: Initialization
KP = 0;    // P Has not converged yet
KQ = 0;    // Q Has not converged yet
numIts = 0; // Number of iterations
// Begin Load Flow Calculations
do
{
    //Step 2: Calculate delP
    for (i=0 ; i<numLoad ; i++)
    {
        tempsum = 0;
        if (Pbus[i+numTx+numGen] != 0)
        {
            for (j=0 ; j<sizeY ; j++)
                tempsum +=
Vbus[i+numTx+numGen]*Vbus[j]*magY[i+numTx+numGen][j]*cos(thetabus[i+num
Tx+numGen] - thetabus[j] - angY[i+numTx+numGen][j]);
            delP[i] = (Pbus[i+numTx+numGen] + tempsum)/Vbus[i+numTx+numGen];
        }
        else
        {
            delP[i] = 0;
        }
    }
    // Step 3: Check convergence of active Power
    if (maxVector(delP,0,numLoad) < ep)
    {
        KP=1;
        if (KQ==1)
            break;
    }

    // If P didn't converge yet...
    else
    {
        // solve for delta_theta and update thetaV
        for (i=0 ; i<numLoad ; i++)
        {
            tempsum=0;
            for (j=0 ; j<numLoad ; j++)
                tempsum -= Binv[i][j]*delP[j];
            thetabus[i+numTx+numGen] -= tempsum;
        }
        KQ=0;
    }
}

```

```

}

//Step 4, calculate deltaQ
for (i=0 ; i<numLoad ; i++)
{
    tempsum =0;
    if (Qbus[i+numTx+numGen] != 0)
    {
        for (j=0 ; j<sizeY ; j++)
            tempsum +=
Vbus[i+numTx+numGen]*Vbus[j]*magY[i+numTx+numGen][j]*sin(thetabus[i+num
Tx+numGen] - thetabus[j] - angY[i+numTx+numGen][j]);
        delQ[i] = (Qbus[i+numTx+numGen] + tempsum)/Vbus[i+numTx+numGen];
        delP[i] = (Pbus[i+numTx+numGen] + tempsum)/Vbus[i+numTx+numGen];
    }
    else
    {
        delQ[i] = 0;
    }
}

// Step 5: Check convergence of reactive power
if (maxVector(delQ,0,numLoad) < eq)
{
    KQ=1;
    if (KP==1)
        break;
}
// If Q doesn't converge
else
{
    // solve delta_v and update V
    for (i=0 ; i<numLoad ; i++)
    {
        tempsum=0;
        //fprintf(outfile, "\r\n%lf", Vbus[j+numTx+numGen]);
        for (j=0 ; j<numLoad ; j++)
            tempsum -= Binv[i][j]*delQ[j]/Vbus[j+numTx+numGen];
        Vbus[i+numTx+numGen] -= tempsum;
    }
}
} while ( (numIts++)<21); // loop back to beginning
if (numIts == 22)
{
    printf("\r\nPower Flow did not converge, exiting\r\n");
    return 0;
}

```

```

}
//Find the unknown Powers
else
{
    // Find power flows of Tx buses
    for (i=0 ; i<(numTx+numGen) ; i++)
    {
        tempsum =0;
        for (j=0 ; j<sizeY ; j++)
            tempsum -= Vbus[i]*Vbus[j]*magY[i][j]*cos(thetabus[i] - thetabus[j] -
angY[i][j]);
        Pbus[i] = tempsum;
        tempsum=0;
        for (j=0 ; j<sizeY ; j++)
            tempsum -= Vbus[i]*Vbus[j]*magY[i][j]*sin(thetabus[i] - thetabus[j] -
angY[i][j]);
        Qbus[i] = tempsum;
    }

    printf("\r\nPower Flow converged in %d iterations\r\n",numIts);
    for (i=0 ; i<sizeY; i++)
    {
        printf("Bus %3d: ",i+1);
        printf("V = %3.3lf pu ",Vbus[i]);
        printf("ang = %3.3lf deg ",thetabus[i]*180.0/M_PI);
        printf("Pi = %3.3lf pu ",-Pbus[i]);
        printf("Qi = %3.3lf pu\r\n",-Qbus[i]);
        fprintf(outfile,"Bus %3d: ",i+1);
        fprintf(outfile,"V = %3.3lf pu ",Vbus[i]);
        fprintf(outfile,"ang = %3.3lf deg ",thetabus[i]*180.0/M_PI);
        fprintf(outfile,"Pi = %3.3lf pu ",-Pbus[i]);
        fprintf(outfile,"Qi = %3.3lf pu\r\n",-Qbus[i]);
    }
}
return 1;
}
void init()
{
    Binv = (double **)malloc(numLoad*sizeof(double *));
    magY = (double **)malloc(sizeY*sizeof(double *));
    angY = (double **)malloc(sizeY*sizeof(double *));
    Vbus = (double *)malloc(sizeY*sizeof(double));
    thetabus = (double *)malloc(sizeY*sizeof(double));
    Pbus = (double *)malloc(sizeY*sizeof(double));
    Qbus = (double *)malloc(sizeY*sizeof(double));
}

```



```

for (int i=0 ; i<sizeY ; i++)
{
    magY[i] = (double *)malloc(sizeY*sizeof(double));
    angY[i] = (double *)malloc(sizeY*sizeof(double));
}
for (int i=0 ; i<numLoad ; i++)
{
    Binv[i] = (double *)malloc(numLoad*sizeof(double));
}
myfile = fopen("data.txt", "r");
outfile = fopen("out.txt", "w");
storeArray(magY,sizeY);
storeArray(angY,sizeY);
storeArray(Binv,numLoad);
storeVector(Vbus,sizeY);
storeVector(thetabus,sizeY);
storeVector(Pbus,sizeY);
storeVector(Qbus,sizeY);
fclose(myfile);
}
void storeArray(double** x, int bounds)
{
    for (int i=0 ; i < bounds ; i++)
        for (int j=0 ; j < bounds ; j++)
            fscanf(myfile,"%lf",&x[i][j]);
}
void storeVector(double* x, int bounds)
{
    for (int i=0 ; i<bounds ; i++)
        fscanf(myfile,"%lf",&x[i]);
}
double maxVector(double* x, int start, int end)
{
    double max;
    max = x[start];
    for (int i=start ; i<end ; i++)
        if (max < x[i])
            max = x[i];
    return max;
}

```

Figure A4-1: Source Code for Load Flow Program

Figure A4-2: SIMULINK PSAT Block Diagram for Verification

④ Bn-73-23