FREQUENCY CALIBRATION OF THE SYSTEM CLOCK OF PASSIVE WIRELESS MICROSYSTEMS

by

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ABSTRACT

FREQUENCY CALIBRATION OF THE SYSTEM CLOCK OF PASSIVE WIRELESS MICROSYSTEMS

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Master of Applied Science, Electrical and Computer Engineering, Ryerson University, 2017

This thesis presents a theoretical and simulated study of frequency calibration of the system clock of passive wireless microsystems.

The proposed frequency calibration technique achieves ultra-low power, high frequency accuracy, and fast calibration of the frequency of a local oscillator in a passive wireless microsystem using a frequency-locked loop (FLL). A new integrating frequency difference detector (iFDD) that senses the frequency difference between the local oscillator and a reference clock is also proposed. The iFDD is implemented using a switched-capacitor network with two integrating paths. The FLL is composed of a logic-control block for generation of clock signals, the iFDD, and a relaxation voltage-controlled oscillator. A detailed analysis of the characteristics of the iFDD in the time and frequency domains is presented. The loop dynamics of the FLL is also investigated. The proposed FLL is implemented in IBM 0.13-μm, 1.2 V CMOS technology and is validated through simulations using Spectre APS.

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List of Abbreviations

CDS	Cadence Design Systems
ADC	Analog-to-Digital Converter
*AND*2	2-input AND logic gate
APS	Accelerated Parallel Simulator
ASK	Amplitude-Shift Keying
*BSIM*4*v*4	Berkeley Short-Channel IGFET Model 4 version 4
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital-to-Analog Converter
dBm	Decibel power with respect to 1 Milliwatt
DC	Direct Current
DCO	Digitally-Controlled Oscillator
DFF	Data (D) Flip-Flop
DFLL	Digital Frequency-Locked Loop
EPC	Electronic Product Code
*EPCC*1*G*2	Class-1 Generation-2 EPC standard
ERP	Equivalent Radiated Power
FF	(NMOS)Fast-(PMOS)Fast
FLL	Frequency-Locked Loop

FS	(NMOS)Fast-(PMOS)Slow
FVC	Frequency-to-Voltage Converter
$iFDD$	Integrating Frequency Difference Detector
ILD	Injection-Locked Divider
$IL-PLL$	Injection-Locked Phase-Locked Loop
IoT	Internet-of-Things
LCB	Logic-Control Block
IIR	Infinite-Impulse-Response
$MIM-cap$	Metal-Insulator-Metal Capacitor
$2:1MUX$	2-input, 1-ouput Multiplexer
$NAND2/3$	2/3 input Not-AND logic gate
$NMOS$	N-channel Metal-Oxide Semiconductor
PFD	Phase-Frequency Detector
PIE	Pulse-Interval-Encoding
PLL	Phase-Locked Loop
$PMOS$	P-channel Metal-Oxide Semiconductor
PVT	Process, Voltage, and Temperature
$reltol$	Relative Tolerance
RF	Radio Frequency
$RFID$	Radio Frequency Identification System
$RTcal$	Read-to-Transponder calibration
SAR	Successive-Approximation-Register
SF	(NMOS)Slow-(PMOS)Fast

S/H	Sample-and-Hold
SNR	Signal-to-Noise Ratio
$SR-latch$	Set-Reset latch
SS	(NMOS)Slow-(PMOS)Slow
$TSPC$	True-Single-Phase-Clocking
TT	(NMOS)Typical-(PMOS)Typical
TVC	Time-to-Voltage Converter
UHF	Ultra High Frequency
VCO	Voltage-Controlled Oscillator

Chapter 1

Introduction

Automatic identification procedures have become a popular method to supply information about animals, people, goods and products that are in transit and are now very important in the service, logistics, and manufacturing industries to name a few [2]. Although barcodes are stilled used to this day to provide information on products because they are very inexpensive, their low storage capacity and inability to be reprogrammed prevents them from being used in identification systems that require storage of large amounts of data and the ability to be reprogrammed [2].

Of the various types of identification systems-barcode, optical character recognition, voice recognition, smart card, and Biometry-radio frequency identification (RFID) systems are becoming popular alternatives because of their various distinct advantages, such as not being able to be interfered with while reading/writing data, their operation not being influenced by external objects like dust/dirt, and being able to have large distances ($\gg 1$ m) between the reader and the data-carrying device [2]. Currently, they are finding extensive use in tap-to-pay systems for the goods and services industry as well as public transit payment systems. RFID systems consist of two intrinsic parts:

- the *transponder* (located on the item to be analyzed),
- the *reader/interrogator*.

The reader reads data from or writes data to the transponder and is usually composed of a transmitter/receiver module, a control block, and a coupling component to the transponder [2]. Similarly, the transponder also has a coupling element in addition to a

microchip which processes and stores the data to be retrieved by the reader, provided it is within the reading distance of the reader [2].

1.1 Characterization of Radio Frequency Identification (RFID) Systems

RFID systems are typically characterized by the operating frequency of the reader, the coupling method between the reader and transponder, and the operating distance between the reader and transponder [2].

1.1.1 Close-Coupling RFID Systems

RFID systems that have an operating range up to 1 cm are known as *close-coupling* systems [2]. Such systems have transmission frequencies in the range of 0-30 MHz and the coupling between the reader and transponder is achieved through both electric and magnetic fields, thus requiring the transponder to either be physically inserted into the reader or positioned on or very near to it [2]. Since close-coupling systems operate at very small distances, then their operating power can be greater than RFID systems that function at larger distances. Typically close-coupling RFID systems are used in applications that require rigid security between the reader and transponder as well as small operating distances between them, such as electronic door-locking systems and smart card systems with tap-to-pay functions [2].

1.1.2 Remote-Coupling RFID Systems

RFID systems that operate at distances up to 1 m are termed *remote-coupling* systems [2]. Most remote-coupling systems use magnetic coupling between the reader and transponder, operate at frequencies less than 135 kHz or 13.56 MHz, and have applications in animal tracking and industrial automation [2].

1.1.3 Long-Range RFID Systems

RFID systems with read-to-transponder ranges $\gg$ 1 m are collectively known as *long-range* systems [2]. These systems operate in the ultra-high frequency (UHF) range (860-960 MHz) and microwave region (2.5 GHz and 5.8 GHz) in Canada, use electromagnetic coupling between the reader and transponder (thus they require antennas for coupling) and the majority of such systems operate using the *backscattering* technique to communicate data from the transponder to the reader [2, 3, 4]. Long-range RFID systems are further distinguished by how their transponders are energized. *Active* long-range transponders have an on-board power supply/battery, whereas *passive* long-range transponders do not have a power supply but rather use the energy contained in the magnetic or electromagnetic field that is emitted by the reader when communicating with the transponder, provided the transponder is within the reader's interrogation zone [2]. In particular, if the transponder is in the interrogation zone of the reader, then it will provide the transponder with power through its emitted RF wave, which is stored on a large capacitor on the transponder [5]. The power-up procedure begins the reader-transponder communication process and it takes some time to complete, since the capacitor must be charged to a level that will allow the transponder to operate [2]. Another distinguishing factor between active and passive transponder is the field of the received RF wave from the reader. Since the magnetic or electromagnetic field of the emitted RF wave from the reader does not power active transponders, then it can be much weaker than the field that is emitted for passive transponders [2]. Passive transponders cannot generate enough power to create an RF signal on their own and, therefore, they rely on modulating the electromagnetic field that is emitted by the reader to be able to transmit data from the transponder to the reader [4]. In particular, passive transponders must be activated by the reader prior to communicating with it, whereas active transponders do not need to be activated by the reader prior to communication. Apart from the way active and passive transponders are powered, another major distinction between them is their operating distance. Active transponders have operating ranges of 15 m and above, while passive transponders typically have operating distances up to 3 m, although some authors haved reported operating distances of 9.25 m [2, 6].

1.2 Background on Passive Wireless Microsystems (PWMs)

RFID systems that operate using passive transponders are known as *passive wireless microsystems (PWMs)*. Attributive to their miniaturization, wireless accessibility, programmability, and maintenance-free operation, PWMs have found a broad range of emerging applications including implantable bio-MEMS pressure sensors [7], retinal prosthetic devices [8], multi-site pressure sensors for wireless arterial flow characterization [9], and wireless temperature sensors [10, 11, 12], to name just a few, and are the main focus of this thesis work.

1.2.1 Architecture

The architecture of an RF powered transponder consists of an antenna for receiving the RF signal, a power generation circuit, a signal front-end block, and a baseband processing block, as shown in Fig.1.1.

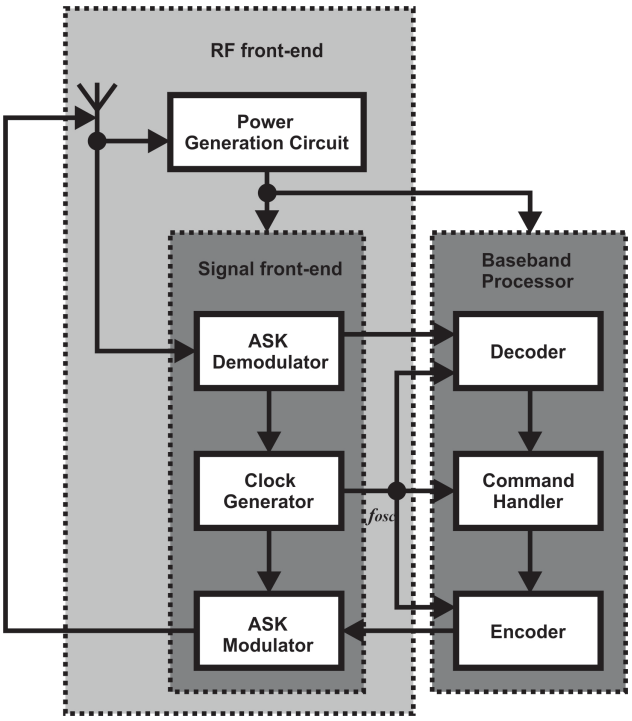

Figure 1.1: Simplified block diagram of a typical UHF RFID transponder.

RF Front-End

The first major layer of the transponder of the PWM is the RF front-end, which consists of an antenna for receiving the RF signal, a power generation circuit, an amplitude-shift-keying (ASK) demodulator for recovering the data, a clock generator for extracting the clock from the ASK demodulator, and an ASK modulator for transmitting the data from the transponder to the reader through backscattering. The RF front-end is thus responsible for supplying power to the transponder and interfacing with the reader.

Sub-components within the RF front-end that are critical to the correct operation of the transponder are the antenna matching network and the RF-to-DC converter. The antenna matching network is responsible for matching the impedance of the antenna to that of the transponder, in order to provide maximum power transfer from the RF signal to the chip [5]. The RF-to-DC converter is responsible for providing the required, stable DC voltage to power the transponder [5]. The efficiency of the matching network and the RF-to-DC converter are still major design challenges in these areas. However, the study of these important blocks are beyond the scope of this thesis and will not be discussed here.

Baseband Block

The baseband processing block consists of circuits that process, generate and/or store data, such as quantizing the sensor readings of the PWM through analog-to-digital converters (ADCs) or microprocessors for signal processing [5]. Since PWMs are powered by the incoming RF signal, then such signal processing units will have a very limited power budget. Consequently, the design of low power baseband processing circuits is the major challenge in this field, but is beyond the scope of this thesis and will not be discussed further.

System Clock

Another crucial element for PWMs is the clock signal itself. The operation of both the RF signal front-end and baseband procesing blocks of a PWM is administered by its system clock, as seen in Fig.1.1. It is responsible for decoding the downlink data from the reader to the transponder, clocking the command handler, and encoding the uplink data from the transponder to the reader [13]. Further details on the requirements of the system

clock and challenges in designing it will be explored in Section 1.3, followed by a review of the state-of-the art in clock generation and calibration for PWMs in Chapter 2.

1.2.2 Applications

Passive wireless microsystems have applications in various areas that range from supply chain management for automation of the storing and distribution of goods, tracking items, and better inventory-control management; electronic access control into buildings and secure locations for storing equipment; tap-to-pay fare collection for transit systems; tracking livestock for animal health and disease control; and healthcare for tracking hospital equipment and supplies, to name a few [4]. Furthermore, the market for PWMs is expected to be worth $14.9 billion by the year 2022, up from $11.2 billion in 2017 [14]. Therefore, PWMs not only have applications in areas that either directly or indirectly affect our lives, but their economic impact is also very significant.

1.3 Motivation

The primary motivation of this thesis was overcoming the dominant challenges in the design of a clock generation technique for PWMs in UHF applications, which will be discussed next.

1.3.1 Challenges in the Design of the System Clock for PWMs

Due to the lack of a power source in PWMs, the transponder typically cannot allot any of its DC power to generate its own RF signal to communicate with the reader. Rather, PWMs communicate with the reader through backscatter load modulation, whereby a fraction of the received RF signal from the reader is reflected back to the reader by the transponder's antenna [2, 5]. The total power that is reflected back by the antenna is set by its input impedance. Therefore, by varying the impedance/load of the antenna, the amount of reflected power can be varied. The impedance of the antenna can be varied by modulating it with the data that is being transmitted by the transponder. The frequency of the data and, consequently, the frequency of the modulation of the antenna impedance is determined

by the clock of the PWM. A diagram to illustrate the concept is presented in Fig.1.2. The switch varies the impedance of the antenna and is controlled by the baseband data, which controls the change in the antenna impedance. Backscatter load modulation significantly eases the power constraint on PWMs, since the transponder does not have to generate its own an RF signal thus greatly increasing its power budget.

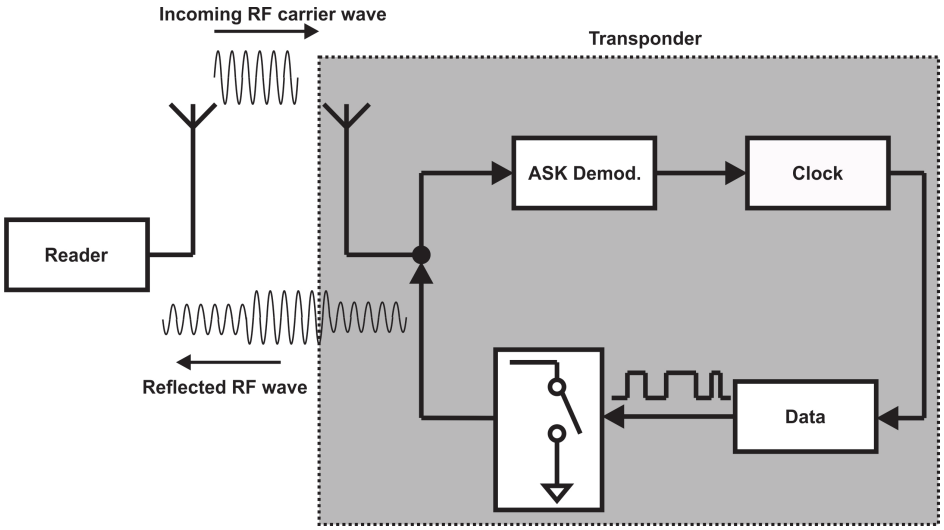

Figure 1.2: Simplified block diagram example of backscatter load modulation.

Modulating the data of the transponder by a carrier signal, namely the system clock of the PWM, generates sub-carriers which allows easier detection of the backscatterd signal by the reader [5]. This is shown in Fig.1.3. The reader can recover the carrier signal by filtering out the signal at the sub-carrier frequency f_c+f_{clk} using a low-pass filter. Fig.1.1 and Fig.1.3 show that the bandwidth of the backscattered transponder signal is set by the frequency of the transponder's clock signal. Therefore, a very accurate clock frequency is required to ensure proper transponder-to-reader communication. For the EPC radio-frequency class-1 generation-2 (EPC C1G2) UHF RFID protocol, the frequency variation of the uplink data must be bounded by $\pm 2.5\%$ in environments that contain a single reader [3].

In addition to the frequency accuracy constraint, the power consumption of the clock generation technique must be low due to the limited power budget of a PWM. Additionally,

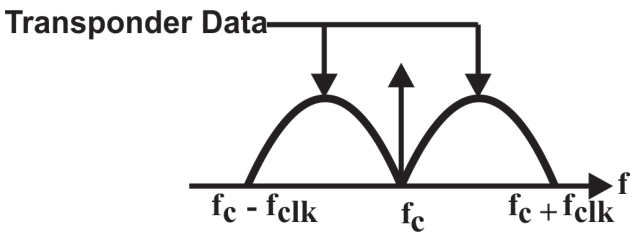

Figure 1.3: Spectrum of backscattered data signal from the transponder.

the larger the power consumption of a PWM the smaller the reader-to-transponder distance which limits the PWM to short-range applications [2]. Furthermore, the received power to a transponder decreases as its distance from the reader increases, further restricting the power budget of the PWM [2]. Therefore, for a PWM to operate at large ($\gg$ 1 m) reader-to-transponder distances its power consumption must be ultra-low and the supply voltage it operates from should also be very low, since the amplitude of the received RF signal will be very small and its power decreases with increasing distance [2].

Including the power constraint and strict frequency accuracy requirement of the backscattered data, the calibration time of the reader-to-transponder can also be very strictly confined. For example, for EPC C1G2 UHF RFID protocol the reader-to-transponder calibration time can be as short as 56.25 μs with a maximum calibration time of 300 μs, depending on local radio regulations [3]. This places an extra constraint on the generation of the system clock.

To summarize, the following major challenges in the design of the system clock for PWMS are:

1. Ultra-low power clock generation due to the restricted power budget of the PWM.
2. Frequency variation of the backscattered data must be bounded by $\pm$2.5% for single reader environemnts.
3. Short calibration times ($\leq$56.25 μs or $\leq$300 μs).
4. Ability to operate at low supply voltages for large reader-to-transponder distances ($>$3 m) for UHF applications.

1.4 Objective

The objective of this thesis is the design of a frequency calibration technique that can meet the requirements described in Section 1.3.1. Our particular goal was to design a frequency calibration technique using a frequency difference detector that integrates the frequency difference between a reference clock that is provided by the reader and the local oscillator of a PWM, thereby providing zero steady-state frequency error for the system clock of the PWM after calibration, while also achieving very fast frequency calibration and an ultra-low power consumption so that the system can be used in long-range PWM applications, such as supply-chain management or healthcare.

1.5 Contributions

The following original contributions made by this thesis are outlined as follows:

- An ultra-low power, highly accurate, and fast frequency calibration method using a frequency-locked loop (FLL) that is embedded with frequency difference detector that integrates the frequency error between a reference clock sent by the reader and the local oscillator of the PWM, as discussed in Section 1.4. The calibration technique provides zero steady-state frequency error between a timing reference from the reader and the local oscillator of the transponder, while also achieving ultra-low power and a very short calibration time. Compared to previous clock generation techniques reported in [15, 16, 17, 18, 13, 19] our proposed design significantly improves on both the calibration time and the frequency accuracy of the system clock for PWMs.

- An ultra-low power integrating frequency difference detector (iFDD) that integrates the frequency difference between two signals and can operate at very low supply voltages. The iFDD provides fine frequency resolution and fast frequency calibration by detecting the duty-cycle and period difference between two signals through a switched-capacitor network. The importance of the iFDD design is that it uses only a single current source and switched-capacitor network to detect a frequency difference between two

signals, thereby reducing mismatch-induced frequency error present in dual-frequency-to-voltage (FVC) designs [20, 21].

1.6 Thesis Organization

This thesis is organized as follows:

- Chapter 1 provides an overview of the characterization of the various forms of RFID systems, background on the architecture of PWMs, and a brief discussion on the operation of each block within a PWM. This chapter also presents the challenges in designing the system clock for PWMs. The main objective of the thesis is derived from these design challenges. The contributions that the research presented in this thesis has achieved in realizing the main objective is also provided.

- Chapter 2 presents a literature review that examines and compares the state-of-the-art in clock generation techniques for PWMs based on the major design challenges presented in Chapter 1.

- Chapter 3 introduces the proposed method for calibration of the system clock of PWMs. The proposed integrating frequency difference detector is presented and analyzed in detail in this chapter. The loop dynamics of the FLL embedded with the frequency difference detector is also investigated.

- Chapter 4 presents the simulation environment that was set up to test the performance of the FLL as well as the simualtion results that were obtained from the set up. Comparison of our results to previous state-of-the-art works is also presented.

  Chapter 5 summarizes the thesis and outlines possible directions for future work in this area.

1.7 Chapter Summary

This chapter presented a brief characterization of the difference types of RFID systems as well as basic background on PWMs. We acquainted ourselves with the basic architecture

of a passive transponder and concisely discussed its critical circuit blocks, such as the RF front-end and baseband processing units. The specified tasks and design challenges of the signal front-end block, baseband block, and system clock of passive transponders were briefly discussed. Challenges with respect to the design of system clock for the transponder of PWMs were addressed in detail. From these challenges, it was concluded that the most pressing problems in the area of clock generation for PWMs are ultra-low power consumption, high frequency accuracy, and a fast calibration time. Motivated by these design challenges, the objective of this thesis was outlined and the contributions of a new frequency calibration technique using an integrating frequency difference detector were summarized.

Chapter 2

A Review of State-of-the-Art for Clock Generation and Calibration of PWMs

The operation of both the RF front-end and baseband processing blocks of PWMs is conducted by its system clock. As discussed in Chapter 1, there are demanding requirements on the system clock. A few methods have been developed to generate the clock for PWMs and they can be split into two categories:

1. Clock recovery from the incoming data sent by the reader.
2. Frequency calibration of a local oscillator in the PWM.

This chapter will review the advantages and disadvantages of previous works in each of these areas.

2.1 Clock Recovery Method

2.1.1 Clock Recovery from an ASK-Modulated Carrier

A PWM with ASK data links with its reader can directly extract the clock from the ASK-modulated carrier by using an ASK-demodulator, as shown in Fig.2.1 [22]. This approach yields a very simple design, since only a comparator and a chain of frequency dividers is needed. However, it suffers from a few notable drawbacks for UHF RFID systems. First, the high frequency of the carrier results in significant power consumption from the clock recovery circuit. This is because the baseband processors of PWMs operate in the high-kHz to low-MHz range, so frequency dividers are required to bring down the high frequency of

the carrier to a baseband frequency [1]. Second, the clock signal is unavailable when the input RF signal is weak, which occurs when the read-to-transponder distance is large, or when transmitting a data-0 with a 100% modulation-index. Finally, a very stable voltage reference accross process, voltage, and temperature (PVT) variations is required to ensure reliable recovery of the clock signal from the RF carrier wave.

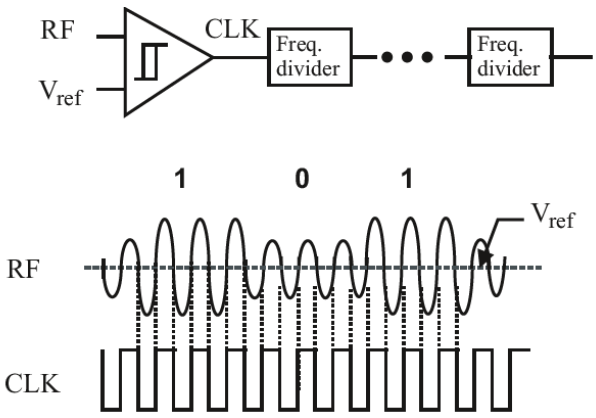

Figure 2.1: Clock recovery from the ASK-modulated carrier wave [1].

2.1.2 Clock Recovery using Injection-Locked Dividers

To overcome the issue presented in Section 2.1.1, Leung and Luong proposed a method that uses an injection-locked divider (ILD) to reduce the power consumption of the frequency divider circuit as shown in Fig.2.2 [15]. The idea behind this approach is to first recover a clock at the frequency of the RF carrier when the RF signal is strong and then use low power injection-locked frequency dividers to bring the recovered clock frequency down further. True-Single-Phase-Clocking (TPSC) frequency dividers are used because of their low power consumption to further lower the frequency. This method resulted in a total average power consumption of 7 μW from a power supply of 0.5 V and -12 dBm (63 μW) input power to the transponder. Thus, the clock recovery circuit consumes 11% of the total received power. With this input power, a reading distance of around 3 m can be achieved (assuming a dipole antenna with 0 dB gain at 500 mW effective radiated power (ERP))[2]. However, as

the reading distance increases and the amplitude of the received RF signal becomes smaller, the received input power decreases significantly [2]. Consequently, the majority of the power consumption of the transponder in this case would be from the clock generator circuit. Leung *et al.* resolve this issue by switching to a low-power oscillator circuit that consumes 1.5 μW when the received RF signal is weak. However, the frequency accuracy of the local oscillator cannot be guaranteed because of PVT variations and since no frequency calibration of the local oscillator is done.

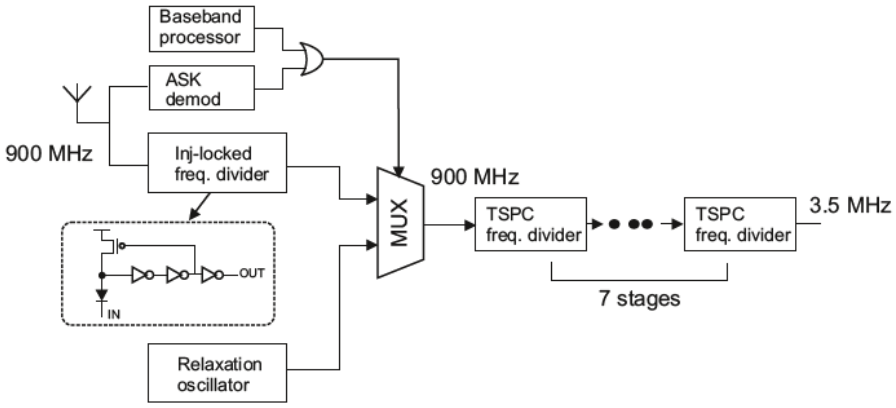

Figure 2.2: Clock recovery from the RF carrier wave using injection-locked dividers [1].

2.1.3 Clock Recovery from the Envelope of the Carrier

The system clock of a PWM can also be extracted from the envelope of the received RF signal, as shown in Fig.2.3 [16, 23]. This method uses an envelope detection circuit to extract the envelope signal of the modulated RF carrier and a comparator to compare the amplitude of the recovered envelope signal with a reference value. The output of the comparator is then used to generate the clock signal. Compared with clock generation from the carrier, this method has a much lower power consumption because the clock that is extracted from the envelope is at a much lower frequency than the carrier signal and thus does not require frequency dividers, so it can be used for basedband operation of the transponder's processor. For example, Ma, Wu, Zhang, and Zhang achieved a static power consumption

for the clock generator circuit less than 1 μW at a 1.8 V supply [16]. However, the dynamic power consumption of the clock generator circuit was 3.38 μW. Another disadvantage of this approach is that a stable voltage reference across PVT is required for the comparator in order to accurately recover the clock signal. This increases the complexity and silicon area of the circuit, since compensation circuitry would be required for the reference voltage. Furthermore, any deviation in the reference voltage will result in reduced frequency accuracy of the recovered clock signal.

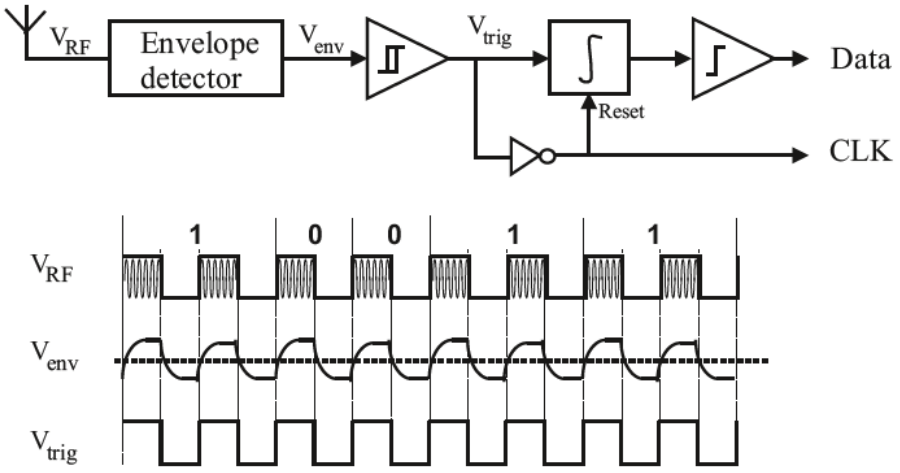

Figure 2.3: Clock generation from the envelope of the ASK-modulated carrier [1].

2.2 Remote Frequency Calibration of a Local Oscillator

The second method of creating the system clock for the transponder in a PWM involves generating the clock locally by tuning the frequency of a VCO. However, the impact of PVT uncertainty greatly affects the frequency accuracy of the local oscillator. For example, a VCOs free-running frequency can vary by as much as $\pm 20\%$ owing to process, voltage, and temperature (PVT) effects [13]. Given the stringent frequency accuracy requirement of EPC C1G2 UHF RFID protocols of $\pm 2.5\%$ for the backscattered data, the frequency of the VCO must be corrected prior to any operation of the PWM to reduce its frequency error.

Compensation circuitry can be used to offset the effect of supply voltage and temperature variations [24, 25]. However, such techniques become difficult to implement in PWMs because of their limited power budget [26, 27]. Furthermore, such techniques cannot mitigate the effect of process variations, so additional circuitry for process effects would be required. Another approach to correcting the VCO frequency prior to the commencement of the passive transponder's operations is to calibrate the VCO frequency with respect to a reference signal provided by the reader. This approach is termed *remote frequency calibration.*

2.2.1 Remote Frequency Calibration using Digital Trimming

The frequency of the local oscillator is often calibrated using digital trimming, shown in Fig.2.4 [17, 28, 29, 30, 31]. In this approach, the frequency of the local VCO is calibrated with respect to a calibrating signal sent from the reader in a calibration phase by using a counter to count the number of oscillation cycles of the oscillator during this phase. The value of the counter at the end of the calibration phase is then used as a threshold value for a successive-approximation-register (SAR), with which the frequency of the oscillator after the calibration phase is compared. Although this approach features a large frequency tuning range and excellent robustness in the presence of PVT variations, the need for a SAR, a digit-to-analog-converter (DAC), and other logic makes it rather difficult to lower the power consumption and shorten the calibration time. Additionally, since the frequency accuracy of digital trimming is set by the number of bits of the SAR, then improving the frequency accuracy will result in an increase in both the power consumption and the calibration time. For example, the power consumption of the frequency calibration block in [17] was 31 μW while a calibration time of 928 μs was required to set all of the bits of the 8-bit SAR.

2.2.2 Remote Frequency Calibration using a Phase-Locked Loop

The local oscillator of a PWM can also be calibrated using a phase-locked loop (PLL), as shown in Fig.2.5 [18]. This approach uses a clock recovery and calibration circuit to calibrate the frequency of a VCO. An envelope detector detects the envelope of the received RF signal and a clock extractor generates a square wave clock signal with a frequency that is the same as the carrier frequency. Once the clock has been generated, a PLL is used to tune

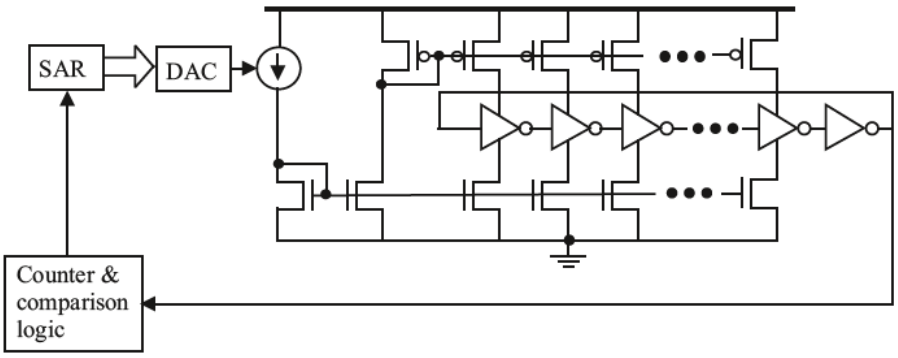

Figure 2.4: Frequency calibration of a local oscillator by digital trimming [1].

the frequency of the VCO to the recovered clock signal. After the PLL has locked to the reference clock, a local system clock for the transponder of the PWM is generated. Fan, Dai, Zhang, and Lu implemented a PLL remote frequency calibration system that operated at a frequency of 13.56 MHz [18]. The total power consumption of Fan *et. al*'s clock generation and calibration system was 17 μW during the locking state and 3 μW in the locked state. However, this is simply a result of the carrier frequency that was used in their design. For UHF carrier signals, the power consumption of this approach would be very large since the VCO would operate at a much higher frequency. Furthemrore, when no carrier is available, which occurs when a large modulation index is used, the frequency of the local oscillator drifts since no reference clock is present. Fan *et. al* get around this problem by implementing a detector and logic block that turns the phase-frequency detector (PFD) off so that it holds it previous value, thus preventing the VCO frequency from differenting too much. However, the VCO frequency will drift by some amount due to stray capacitances in the loop filter of the PLL. Apart from the above drawbacks, since a PLL is used to calibrate the VCO, then the calibration time will be long since the PLL will lock the phase and frequency of the VCO to the recovered clock signal.

2.2.3 Remote Frequency Calibration using a Digital Frequency-Locked Loop

Chan, Pun, Leung, Guo, Lincoln, and Choy proposed a remote frequency calibration technique that uses a digital frequency-locked loop (DFLL), as shown in Fig.2.6 [13]. This

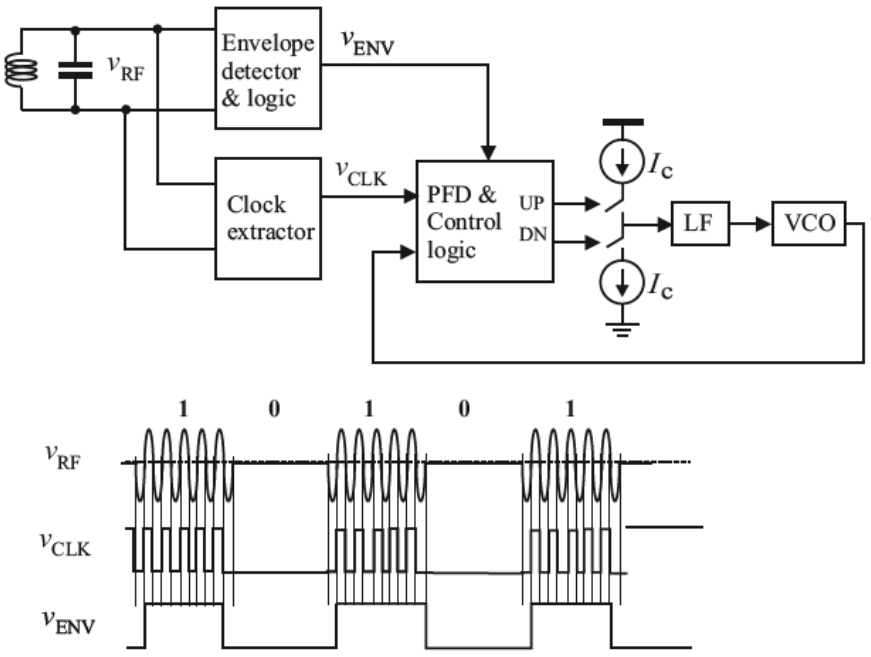

Figure 2.5: Frequency calibration of a VCO using a PLL [1].

approach uses a counter that stores the number of oscillation cycles of a reference VCO during the transmission of a binary-0 or a binary-1, since in pulse-interval-encoding (PIE) a binary-0 and binary-1 have different pulse-widths [1]. A preset threshold value is used as a reference to compare the number of oscillation cycles of a digitally-controlled oscillator (DCO) that is stored in the counter. The threshold value is determined by the baseband processor of the transponder during the reader-to-transponder calibration (RTcal) phase. In particular, if the pulse-width of the transmitted symbol from the reader during RTcal is greater than RTcal/2, then the baseband processor decides that a binary-1 has been received. Otherwise, a binary-0 has been received. The DFLL compares the difference between the preset threshold value determined by the baseband processor and the value stored in the counter, such that their difference is used to control a DCO. Chan *et al.* were able to achieve a very low power consumption of 1.8 μW and a frequency accuracy of -3.2$\sim$1.2% at a clock frequency of 2.56 MHz [13]. Another distinct advantage of this approach is that the DCO will be continuously calibrated so long as there is communication between the reader and transponder. However, a drawback of this approach is the limited frequency accuracy of the

local DCO, since a counter is used to store the number of oscillation cycles of the DCO. As a result, quantization error will always exist and fine frequency accuracy ($<\pm 2.5\%$) cannot be achieved without increasing the power consumption of the transponder. A second drawback of this approach is that the reference value used to compare the number oscillation cycles of the DCO to is obtained from a second VCO that is not calibrated and thus is subject to PVT effects. Another limitation of this approach is its long calibration time of 16 PIE downlink data symbols in nominal conditions in the worst case and 6 PIE symbols in the best case [13]. Since a PIE symbol is determined by the length of a data-0 symbol plus a data-1 symbol, which can have pulse-widths between 25 μs and 50 μs and 6.25 μs and 7.8125 μs, respectively, then even in the best case scenario the calibration time of this technique is 84.375 μs.

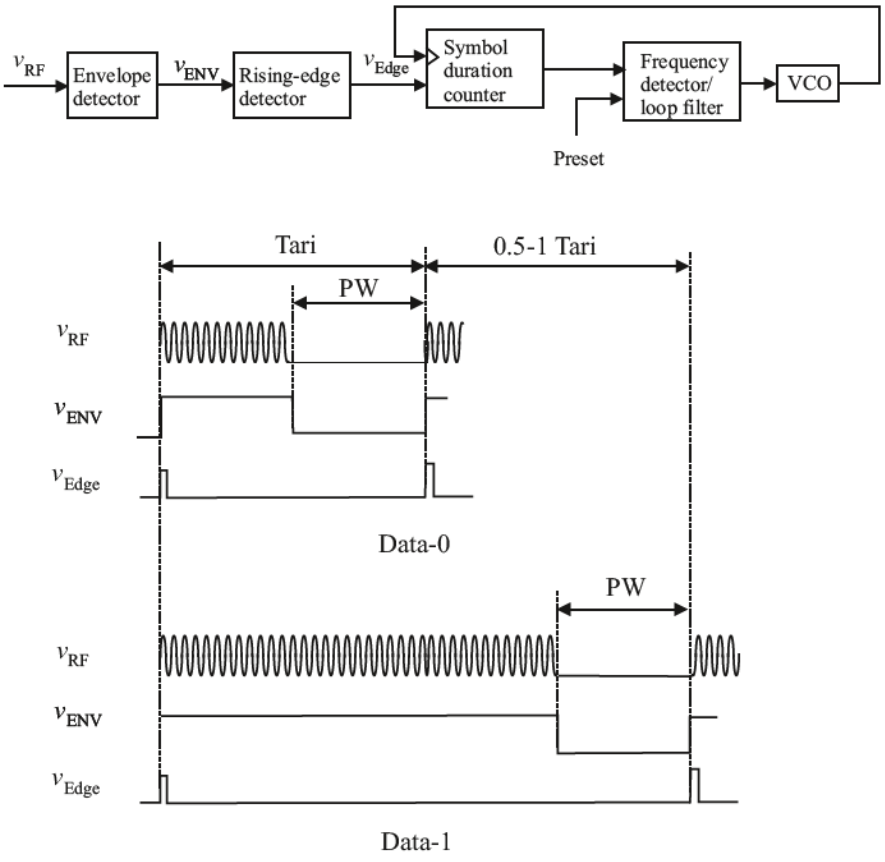

Figure 2.6: Frequency calibration of a VCO using a DFLL [1].

2.2.4 Remote Frequency Calibration using an Injection-Locked Phase-Locked Loop

A remote frequency calibration technique based on injection-locking to the envelope of the received RF input signal was proposed in [19] and is shown in Fig.2.7. This approach utilizes the fact that the baseband processor of passive transponders operates in the kHz-to-low-MHz range and that ASK-modulation schemes are often used for PWMs. Therefore, the envelope of the received RF signal can be extracted and then used as an injection-locking signal for the local oscillator that is embedded in a PLL. The injection-locked PLL (IL-PLL) utilizes integrating feedback to extend its lock range. This greatly reduces the power consumption of the remote frequency calibration system of the transponder by operating the local oscillator at a low frequency and by eliminating the need for frequency dividers. Furthermore, high frequency accuracy can be achieved through injection-locking of the local oscillator to the frequency of the envelope signal. Thus, this approach can achieve both a low power consumption and excellent frequency accuracy. The power consumption of this technique when using a 10-mV-amplitude injection signal at a frequency of 1 MHz was 0.96 μW at a power supply of 1.2 V [19]. However, there are a few drawbacks to this technique. First, the lock range of the IL-PLL is limited to only 0.43 MHz, so if the VCO free-running frequency varies by more than this amount, the IL-PLL will be unable to lock the VCO to the injection signal. To increase the lock range, the charge-pump current in the integrating feedback loop has to be increased, thus increasing the power consumption. Second, the IL-PLL suffers from a relatively long calibration time of 150 μs and 30 μs in the worst and best cases, respectively, thus being unable to meet the EPC C1G2 RFID protocol for the calibation time in reader-to-transponder communication across PVT.

2.3 Chapter Summary

A review of the state-of-the-art in clock recovery and remote frequency calibration techniques for generating the system clock of the transponder in PWMs was presented. We found that clock recovery methods that extract the clock signal from either the carrier or envelope signal can suffer from high power consumption and are unable to operate correctly

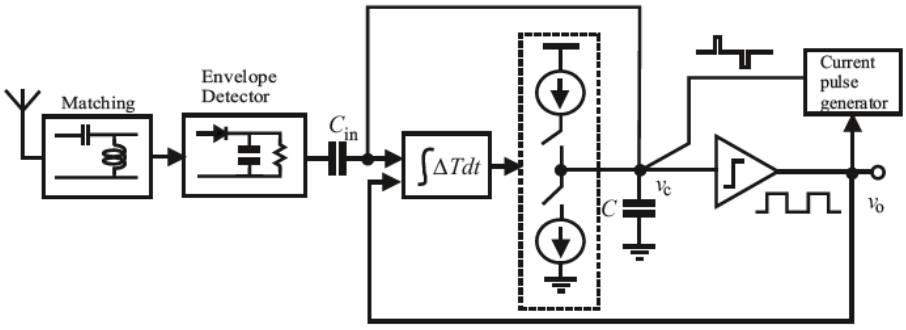

Figure 2.7: Frequency calibration of a VCO using an IL-PLL [1].

when a large modulation index is used for the ASK-modulated carrier. This also limits the reading range of the PWM. Remote frequency calibration techniques that calibrate the frequency of a local oscillator through digital trimmming, PLLs, DFLLs, and IL-PLLs were presented. The digital trimming technique was found to be the most popular calibration approach due to its large tuning range and robustness in the presence of PVT effects. However, it was determined that digital trimming suffers from long calibration times and significant power consumption. Remote frequency calibration using a PLL that locks to the carrier signal frequency was found to have a much lower power consumption than the digital trimming technique, but still experiences a large power consumption when a UHF carrier is used. A remote frequency calibration technique that uses a DFLL to compare the number of oscillation cycles of a reference VCO to that of a DCO was presented and found to have a very low power consumption, but long calibration times and a non-zero frequency error in steady-state. Finally, an IL-PLL that uses envelope injection-locking and integrating feedback to tune a VCO was presented. This method achieved both ultra-low power consumption and excellent frequency accuracy through injection-locking. However, noteable limitations to this design are its relatively long calibration time, high supply voltage, and small lock range.

Chapter 3

Sub-Microwatts Integrating Frequency Difference Detector for Frequency Calibration of PWMs

3.1 Introduction

The operation of both the RF front-end and baseband blocks of a PWM is controlled by its system clock. Successful communication between the reader and transponder of a PWM thus depends on the accuracy of its system clock, which is strongly dependent on changes in the local environment that the passive transponder is in. Variations in power supply, temperature, pressure, and the strength of the local electric/magnetic field can result in a subsequent deviation in the desired free-running frequency of the local oscillator that generates the system clock of the PWM. Regular calibration of the frequency of the local oscillator to a defined reference value can mitigate these effects and keep the oscillator's frequency at a constant, pre-defined value.

In this chapter, we propose a frequency calibration scheme that fine-tunes the frequency of the local oscillator of a PWM to a desired reference frequency using a frequency-locked loop (FLL). Additionally, a new ultra-low power integrating frequency difference detector (iFDD) that detects fine frequency differences is proposed. Similar to the dual frequency-to-voltage conversion (FVC) scheme in [20, 21], the iFDD uses a switched-capacitor network to sense and then integrate the difference between the frequency of the local oscillator and that of the reference. However, unlike the designs in [20, 21], the proposed iFDD does not use an error amplifier to amplify the frequency difference and uses only a single switched-capacitor network, thereby eliminating the need to design a low power and high-

gain error amplifier and the effect of FVC-mismatch-induced frequency error as a result of the use of two FVCs in [20, 21]. In addition, the stability of the FLL with the proposed iFDD does not depend on the stability of an error amplifier, unlike the designs in [20, 21]. Finally, the proposed iFDD is also capable of detecting duty-cycle error between the reference signal and the local oscillator, as opposed to the designs [20, 21] which require both signals to have the same duty-cycle.

The remainder of this chapter is organized as follows: Section 3.2 presents the basic concept of the the iFDD, including a time-domain and duty-cycle mismatch analysis. The frequency-domain behavior of the iFDD and FLL is explored in Section 3.3. Nonidealities such as duty-cycle variation and the effect of noise generated by the sampling capacitors on the operation of the FLL is also considered. The chapter is summarized in Section 3.4.

3.2 Integrating Frequency Difference Detector

To overcome the previously mentioned challenges in [20, 21], we propose a new integrating frequency difference detector that is capable of detecting fine frequency differences using a single FVC without an error amplifier. To develop an understanding of the iFDD, first a simple conceptual analysis of the iFDD is performed, followed by detailed derivations of its time-domain behaviour, an analysis of the effect of duty-cycle variation, and then finally an investigation into its maximum frequency of operation.

3.2.1 Concept of the iFDD

The simplified block diagram of the iFDD is shown in Fig.3.1. It consists of a logic control block (LCB), a time-to-voltage converter (TVC), a sample-and-hold (S/H) circuit, and a bridge circuit. The LCB converts the input frequencies, f_{ref} and f_{osc}, to two time intervals denoted by Δt_{C_1} and Δt_{C_2} for the charging intervals of two capacitors C_1 and C_2, respectively, in addition to generating clocks for sampling and charge redistribution. A dual TVC that consists of a constant current source, I, and two capacitors, C_1 and C_2, converts Δt_{C_1} and Δt_{C_2} to two voltages, v_{C_1} and v_{C_2}. The charging time intervals are obtained from the following equations

$$v_{\Delta t_{C_1}} = v_{osc} \wedge \overline{v_{ref}}, \tag{3.1}$$

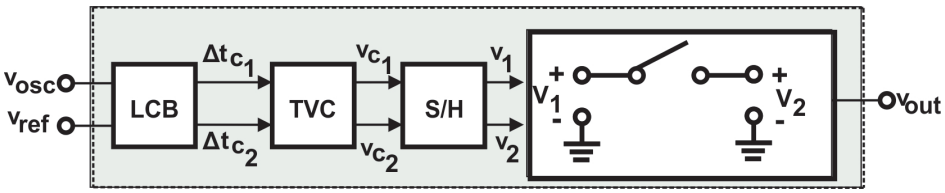

Figure 3.1: Simplified block diagram of the proposed iFDD.

$$v_{\Delta t_{C_2}} = \overline{v_{osc}} \wedge v_{ref}, \tag{3.2}$$

where $v_{\Delta t_{C_1}}$ and $v_{\Delta t_{C_2}}$ are the voltage waveforms of Δt_{C_1} and Δt_{C_2}, respectively. Expressions (3.1) and (3.2) show that the time intervals Δt_{C_1} and Δt_{C_2} determine the length of time for which v_{osc} is high and v_{ref} is low and v_{osc} is low while v_{ref} is high, respectively, as shown in Fig.3.2. In addition, Fig.3.2 shows that the iFDD senses fine frequency differences by measuring the time intervals formed by the rising and falling edges of v_{osc} and v_{ref}. As a result, Δt_{C_1} and Δt_{C_2} are related to the frequencies of the oscillator and reference signals via

$$0 \leq \Delta t_{C_1} \leq d_{osc} T_{osc}, \tag{3.3}$$

$$0 \leq \Delta t_{C_2} \leq d_{ref} T_{ref}, \tag{3.4}$$

where d_{osc} and d_{ref} represent the duty-cycle factors for the oscillator and reference signal, respectively. In the case that both waveforms are 50% duty-cycle, then d_{osc}=d_{ref} =2. From (3.3) and (3.4), a 1:1 mapping between T_{osc} and T_{ref} and v_{C_1} and v_{C_2} of the TVC exists and is given by

$$0 \leq v_{C_1} \leq \left(\frac{I}{C_1}\right) d_{osc} T_{osc}, \tag{3.5}$$

$$0 \leq v_{C_2} \leq \left(\frac{I}{C_2}\right) d_{ref} T_{ref}. \tag{3.6}$$

Cases (i)-(vi) in Fig.3.2 show that the time intervals Δt_{C_1} and Δt_{C_2} determine which signal is operating at a higher frequency. In particular, if $\Delta t_{C_1} > \Delta t_{C_2}$ (cases (ii), (iv),

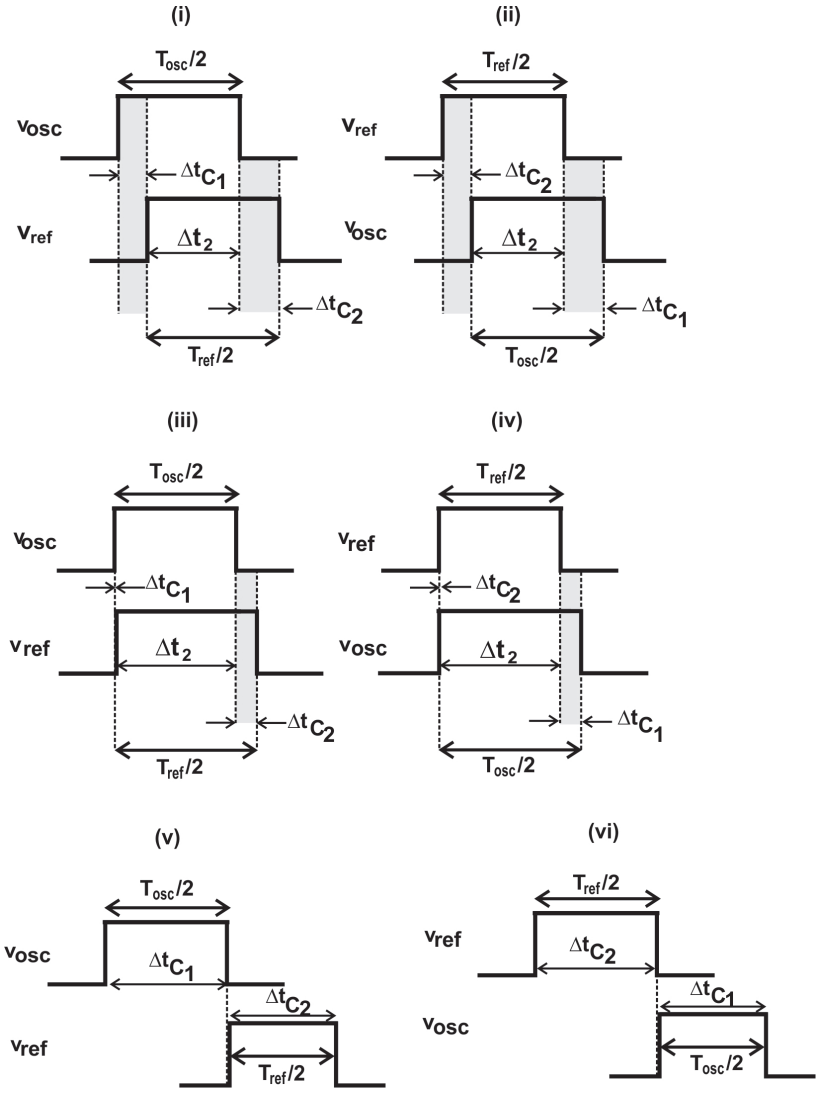

Figure 3.2: Waveforms of v_{osc} and v_{ref} for fine frequency difference ($0 < f_{osc} < f_{ref}$ or $f_{ref} < f_{osc} < 2f_{ref}$) showing the definition of Δt_{C_1} and Δt_{C_2}, in addition to their intermediate and extreme values in (i)-(vi). This is for the ideal case that both waveforms are 50% duty-cycle signals.

and (v)) then $f_{osc} < f_{ref}$, and if $\Delta t_{C_1} < \Delta t_{C_2}$ (cases (i), (iii), and (vi)) then $f_{osc} > f_{ref}$. Furthermore, assuming both waveforms are 50% duty-cycle, then we can write

$$\Delta t_{C_1} + \Delta t_2 = \frac{T_{osc}}{2}, \tag{3.7}$$

$$\Delta t_2 + \Delta t_{C_2} = \frac{T_{ref}}{2}. \tag{3.8}$$

Notice in (3.8) that since $\frac{T_{ref}}{2}$ is constant, then $\Delta t_2 + \Delta t_{C_2}$ is constant in every cycle which implies that if Δt_2 is increasing, then Δt_{C_2} must be decreasing and vice-versa. Subtracting (3.8) from (3.7) and defining the period error as $\Delta T_{err} = T_{osc} - T_{ref}$, we have

$$\Delta t_{C_1} - \Delta t_{C_2} = \frac{\Delta T_{err}}{2}. \tag{3.9}$$

Equation (3.9) shows that both the magnitude and sign of the frequency error between v_{osc} and v_{ref} is contained in the time intervals Δt_{C_1} and Δt_{C_2}. If $\Delta t_{C_1} > \Delta t_{C_2}$, then from (3.9) $\Delta T_{err} > 0$ and thus the frequency of the oscillator must increase. Otherwise, $\Delta T_{err} < 0$ and the frequency of the oscillator must decrease. Finally, If $\Delta t_{C_1} = \Delta t_{C_2}$, then $\Delta T_{err} = 0$. This implies that $v_{C_1} = v_{C_2}$ so that $v_1 = v_2$ after the S/H circuit. Consequently, the bridge is balanced when $\Delta t_{C_1} = \Delta t_{C_2}$ (when both waveforms are 50% duty-cycle) so that $T_{osc} = T_{ref}$. Otherwise, the bridge isn't balanced and the circuit will continue to operate until the bridge is balanced, assuming the iFDD is in a closed-loop system with negative feedback.

3.2.2 Time-Domain Behaviour of the iFDD

To develop a quantitative understanding of the iFDD, the circuit will be analyzed very close to steady-state conditions, so as to develop time-domain (and later on z-domain) equations of the output of the iFDD. Since the iFDD circuit contains switched-capacitors, then we can treat the output voltage of the iFDD as as a discrete-time signal, where the sampling rate in steady-state is set by the reference clock. Fig.3.3 shows the schematic of the proposed iFDD on the left and the waveforms of v_{osc}, v_{ref}, and the clocks that control switches ϕ_{C_1}, ϕ_{sa1}, ϕ_{r1}, ϕ_{C_2}, ϕ_{sa2}, ϕ_{r2}, and ϕ_f on the right. Clock signals ϕ_{sa1}, ϕ_{r1}, ϕ_{sa2}, and ϕ_{rst2} are generated from signals ϕ_{C_1} and ϕ_{C_2}, respectively, whereas clock signal ϕ_f is the delayed version of either ϕ_{r1} or ϕ_{r2} depending on if the falling edge of v_{osc} lags or leads the the falling edge of v_{ref}, as shown on the right of Fig.3.3. The falling edges of both v_{osc} and v_{ref} are detected by two rising edge DFFs, as shown on the left in Fig.3.3. If the falling edge of v_{osc} leads the falling edge of v_{ref}, then Q_{ref} goes high and ϕ_{r2} is selected by the wired-OR 2:1 MUX so that ϕ_f=ϕ_{r2}. On the other hand, if the falling edge of v_{osc} lags v_{ref}, then Q_{osc} goes high and ϕ_{r1} is selected by the wired-OR 2:1 MUX so that ϕ_f=ϕ_{r1}. The delay τ that is used to create clock signals ϕ_{sa1}, ϕ_{sa2}, ϕ_{r1} and ϕ_{r2} is generated by a chain of inverters.

Note that the order of operation of the switches varies when the circuit is not operating in or near steady-state or is not operating in a closed-loop system. In particular, the order of ϕ_{C_1} and ϕ_{C_2} will vary so that either ϕ_{C_1} or ϕ_{C_2} occurs first, and, consequently, the order of switches ϕ_{sa1}, ϕ_{r1}, ϕ_{sa2}, and ϕ_{r2} will vary. However, clock signal ϕ_f will always occur after either ϕ_{r1} or ϕ_{r2}. The start and end of each cycle is defined when the rising edge of ϕ_{C_1} or ϕ_{C_2} occurs first and when the falling edge of ϕ_f occurs, respectively. A buffer is added after the wired-OR so as to restore ϕ_f to V_{DD}.

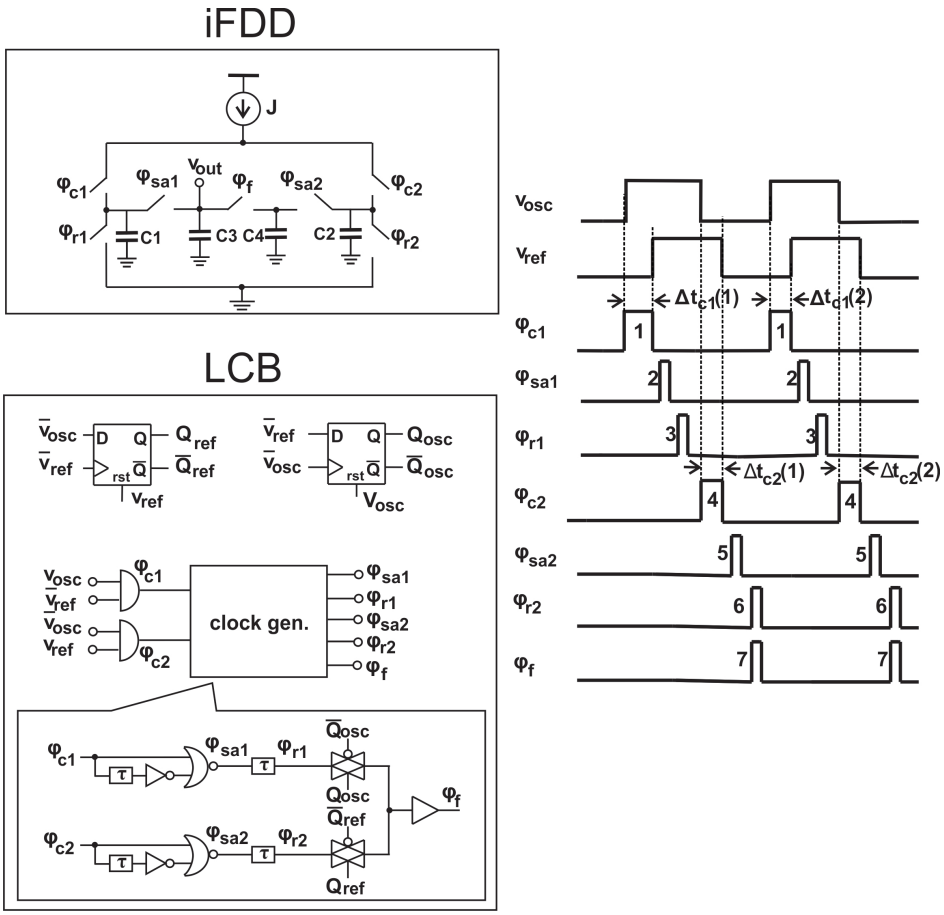

Figure 3.3: Proposed iFDD and its logic control block (LCB) (left) and waveforms (right) of v_{osc}, v_{ref}, ϕ_{C_1}, ϕ_{sa1}, ϕ_{r1}, ϕ_{C_2}, ϕ_{sa2}, ϕ_{r2}, and ϕ_f. The order of operation of the switches are included in the waveform for ease of understanding. The number inside the brackets of $\Delta t_{C_1}(j)$ and $\Delta t_{C_2}(j)$ indicates their jth sample number.

Consider the first cycle of operation, as shown in the waveform on the right of Fig.3.3, and assume that all capacitors are initially at rest, so that $v_{C_{1,2,3,4}}(t = 0^-) = v_{C_{1,2,3,4}}(t = 0^+) = 0$. The first operation in this cycle of the iFDD will be time-to-voltage conversion. Since time interval $\Delta t_{C_1}(1)$ occurs first, then switch ϕ_{C_1} will close and capacitor C_1 will be charged so that $\Delta t_{C_1}(1)$ is converted to a voltage, given by

$$v_{C_1}(1) = \Big(\frac{I}{C_1}\Big)\Delta t_{C_1}(1), \tag{3.10}$$

where $v_{C_1}(1)$ represents the first sample of v_{C_1}. After switch ϕ_{C_1} opens, the second operation of the iFDD, sampling-and-holding, will occur. In this particular case, switch ϕ_{sa1} closes so that charge redistribution between C_1 and C_3 occurs. Assuming that charge redistribution between C_1 and C_3 completes before switch ϕ_{sa1} opens, then by the principle of conservation of charge we have

$$(C_1 + C_3)v_{C_3}(1) = C_3 v_{C_3}(0) + C1 v_{C_1}(1), \tag{3.11}$$

where $v_{C_3}(1)$ represents the first sample value of the the voltage across C_3 and $v_{C_3}(0)$ is the initial voltage across C_3. Since $v_{C_3}(0) = 0$ and $v_{C_3} = v_{out}$, then solving for $v_{C_3}(1)$ yields

$$v_{out}(1) = \Big(\frac{C_1}{C_1 + C_3}\Big)v_{C_1}(1). \tag{3.12}$$

Define $\alpha_1 = \frac{C_3}{C_1}$, then substituting α_1 and (3.10) into (3.12) yields

$$v_{out}(1) = \Big(\frac{\frac{I}{C_1}}{1 + \alpha_1}\Big)\Delta t_{C_1}(1). \tag{3.13}$$

The third operation of the iFDD will be resetting capacitor C_1 by discharging it to ground when ϕ_{r1} closes so that $v_{C_1} = 0$. Next, switch ϕ_{C_2} will close so that the fourth operation of the iFDD will be time-to-voltage conversion of $\Delta t_{C_2}(1)$ to a voltage given by

$$v_{C_2}(1) = \Big(\frac{I}{C_2}\Big)\Delta t_{C_2}(1), \tag{3.14}$$

where $v_{C_2}(1)$ represents the first sample of v_{C_2}. After switch ϕ_{C_2} opens, switch ϕ_{sa2} closes to commence the fifth operation, which is sampling-and-holding of the voltage $v_{C_2}(1)$. Assuming

that charge redistribution between C_2 and C_4 completes before switch ϕ_{sa2} opens, then by the principle of conservation of charge we have

$$(C_2 + C_4)v_{C_4}(1) = C4v_{C_4}(0) + C2v_{C_2}(1), \tag{3.15}$$

where $v_{C_4}(0)$ is the initial voltage across capacitor C_4. Since $v_{C_4}(0) = 0$ then solving for $v_{C_4}(1)$ in (3.15) yields

$$v_{C_4}(1) = \Big(\frac{C_2}{C_2 + C_4}\Big)v_{C_2}(1). \tag{3.16}$$

Define $\alpha_2 = \frac{C_4}{C_2}$, then substituing α_2 and (3.14) into (3.16) yields

$$v_{C_4}(1) = \Big(\frac{\frac{I}{C_2}}{1 + \alpha_2}\Big)\Delta t_{C_2}(1). \tag{3.17}$$

In order to compare v_{out} and v_{C_4} equally, we must have $\frac{I}{C_1} = \frac{I}{C_2}$. Therefore, let $C_1 = C_2 = C$ and define $K_{TVC} = I/C$ as the gain of the TVC. Then equations (3.13) and (3.17) become

$$v_{out}(1) = K_{TVC}\Big(\frac{1}{1 + \alpha_1}\Big)\Delta t_{C_1}(1), \tag{3.18}$$

$$v_{C_4}(1) = K_{TVC}\Big(\frac{1}{1 + \alpha_2}\Big)\Delta t_{C_2}(1). \tag{3.19}$$

After switch ϕ_{sa2} opens, capacitor C_4 is reset after clock signal ϕ_{r2} goes high. The next operation is comparing $v_{out}(1)$ with $v_{C_4}(1)$ through the bridge after switch ϕ_f closes. Again, assuming that charge redistribution between C_3 and C_4 completes before switch ϕ_f opens, then by the principle of charge conservation,

$$(C_3 + C_4)v_{out}(2) = C_3v_{out}(1) + C_4v_{C_4}(1), \tag{3.20}$$

where $v_{out}(2)$ is the second sample value of v_{out}. Solving for $v_{out}(2)$ in (3.20) yields

$$v_{out}(2) = \Big(\frac{C_3}{C_3 + C_4}\Big)v_{out}(1) + \Big(\frac{C_4}{C_3 + C_4}\Big)v_{C_4}(1). \tag{3.21}$$

Define $\alpha_3 = \frac{C_4}{C_3}$, then (3.21) can be written in the form

$$v_{out}(2) = \Big(\frac{1}{1+\alpha_3}\Big)v_{out}(1) + \Big(\frac{1}{1+\alpha_3{}^{-1}}\Big)v_{C_4}(1). \tag{3.22}$$

Substituting (3.18) and (3.19) into (3.22) gives

$$v_{out}(2) = K_{TVC}\Big[\Big(\frac{1}{1+\alpha_1}\Big)\Big(\frac{1}{1+\alpha_3}\Big)\Delta t_{C_1}(1) + \Big(\frac{1}{1+\alpha_2}\Big)\Big(\frac{1}{1+\alpha_3{}^{-1}}\Big)\Delta t_{C_2}(1)\Big]. \tag{3.23}$$

Subtracting (3.18) from (3.23) and defining $\Delta v_{out}(2) = v_{out}(2) - v_{out}(1)$ as the second sample value of the change in the output voltage (since $\Delta v_{out}(1) = v_{out}(1) - v_{out}(0) = v_{out}(1)$) gives

$$\Delta v_{out}(2) = K_{TVC}\Big(\frac{\alpha_3}{1+\alpha_3}\Big)\Big[\Big(\frac{1}{1+\alpha_2}\Big)\Delta t_{C_2}(1) - \Big(\frac{1}{1+\alpha_1}\Big)\Delta t_{C_1}(1)\Big]. \tag{3.24}$$

Choosing $\alpha_1 = \alpha_2 = \alpha$ yields

$$\Delta v_{out}(2) = K_{TVC}\Big[\frac{\alpha_3}{(1+\alpha_3)(1+\alpha)}\Big]\Big(\Delta t_{C_2}(1) - \Delta t_{C_1}(1)\Big). \tag{3.25}$$

Substituting (3.9) into (3.25) yields

$$\Delta v_{out}(2) = -K_{TVC}\Big[\frac{\alpha_3}{(1+\alpha_3)(1+\alpha)}\Big]\Big(\frac{\Delta T_{err}(0)}{2}\Big), \tag{3.26}$$

where $\Delta T_{err}(0)$ is defined as the initial sample value of the difference between the periods of v_{osc} and v_{ref}. Since $v_{out}(2) = v_{out}(1) + \Delta v_{out}(2)$, then from (3.26) we can write

$$v_{out}(2) = v_{out}(1) - K_{TVC}\frac{\alpha_3}{(1+\alpha_3)(1+\alpha)}\frac{\Delta T_{err}(0)}{2}. \tag{3.27}$$

Repeating this process for the second cycle, it can be shown that

$$v_{out}(4) = \frac{K_{TVC}}{1+\alpha}\Big[\Delta t_{C_1}(2) + \Big(\frac{\alpha}{1+\alpha}\Big)\Delta t_{C_1}(1) - \frac{\alpha_3}{2(1+\alpha_3)}\Big(\Delta T_{err}(1) + \Big(\frac{\alpha}{1+\alpha}\Big)\Delta T_{err}(0)\Big)\Big], \tag{3.28}$$

and

$$v_{out}(4) = v_{out}(3) - K_{TVC}\frac{\alpha_3}{(1+\alpha_3)(1+\alpha)}\frac{\Delta T_{err}(1)}{2}. \tag{3.29}$$

Continuing in this manner, we have

$$v_{out}(2n) = \frac{\beta K_{TVC}}{\alpha}\left[\sum_{k=0}^{n-1}\beta^k \Delta t_{C_1}(n-k) - \frac{\alpha_3}{2(1+\alpha_3)}\sum_{k=1}^{n}\beta^{k-1}\Delta T_{err}(n-k)\right], \tag{3.30}$$

as the $2n$th-sampled value of the output voltage, where $\beta = \frac{\alpha}{1+\alpha}$. Furthermore, from (3.27) and (3.29) we can write, in general,

$$v_{out}(2n) = v_{out}(2n-1) - K_{TVC}\frac{\alpha_3}{2(1+\alpha_3)(1+\alpha)}\Delta T_{err}(n-1), \tag{3.31}$$

for $n \geq 1$. Equation (3.29) represents the iterative form of $v_{out}(2n)$ or rather the final value of v_{out} at the end of each cycle, whereas (3.31) represents the difference-equation form of $v_{out}(2n)$. Equation (3.30) shows that $v_{out}(2n)$ will converge only if the two sums in (3.31) are bounded, where the first sum represents a sum of weighted values of Δt_{C_1} and the second sum is a sum of the weighted period difference. Furthermore, note that α_3 determines the contribution that the sum of the error terms makes to $v_{out}(2n)$. To make the contribution of the error term larger, then α_3 must be made large and since $\alpha_3 = \frac{C_4}{C_3}$, then this means that either C_4 should be large or C_3 should be small. However, since $C_1 = C_3$ and $C_2 = C_4$, then adjusting C_3 or C_4 will invariably change C_1 and C_2. Consequently, the gain term K_{TVC} will be split into two terms: $K_{TVC,1}$ for the capacitor pair C_1 and C_3, and $K_{TVC,2}$ for the capacitor pair C_2 and C_4. In turn, this will prevent the direct measurement of the frequency error. Therefore, to be able to measure the frequency error, we must have $C_3 = C_4$ and thus $C_1 = C_2 = C_3 = C_4 = C$. Therefore, $\alpha_3 = 1$ so that (3.31) becomes

$$v_{out}(2n) = \frac{\beta K_{TVC}}{\alpha}\left[\sum_{k=0}^{n-1}\beta^k \Delta t_{C_1}(n-k) - \frac{1}{4}\sum_{k=1}^{n}\beta^{k-1}\Delta T_{err}(n-k)\right], \tag{3.32}$$

In order for the iFDD to be stable, we must have $|\beta| < 1$. Since $C_1 = C_2 = C_3 = C_4$, then $\alpha = 1$ so that $\beta = 1/2$, which ensures the stability of the iFDD. With $\beta = 1/2$ (3.32) becomes

$$v_{out}(2n) = \frac{K_{TVC}}{2}\left[\sum_{k=0}^{n-1}\left(\frac{1}{2}\right)^k \Delta t_{C_1}(n-k) - \frac{1}{4}\sum_{k=1}^{n}\left(\frac{1}{2}\right)^{k-1}\Delta T_{err}(n-k)\right]. \tag{3.33}$$

Equation (3.33) shows that the output voltage of the iFDD is proportional to the frequency error ΔT_{err} (since $\Delta T_{err} \propto \Delta f_{err}$). Indeed, (3.26) shows that $\Delta v_{out}(2n) \propto \Delta T_{err}(n)$ so that the change in the output voltage at the end of each cycle depends on the frequency error between v_{osc} and v_{ref}. If $\Delta T_{err}(n) < 0$ so that $f_{osc} > f_{ref}$, then $\Delta v_{out}(2n) > 0$ and vice-versa according to (3.26). Note that the second sum will converge when $\Delta T_{err}(n-k) = 0$ $\forall k \geq N$ for some $N \in \mathbb{Z}^+$, which occurs when $f_{osc} = f_{ref}$.

3.2.3 Convergence

Note that in order for the two sums in (3.33) to converge, if the terms $\Delta t_{C1}(n-k)$ in the first sum are increasing then the terms $\Delta T_{err}(n-k)$ in the second sum must be increasing as well, but from negative values. Similarly, when the terms $\Delta t_{C1}(n-k)$ in the first sum are decreasing, the terms $\Delta T_{err}(n-k)$ in the second sum must be decreasing. Thus the terms $\Delta t_{C1}(n-k)$ and $\Delta T_{err}(n-k)$ in the two sums given in (3.33) must be in-phase with each other in order for (3.33) to be bounded. This can be better understood by writing (3.33) in vector form as

$$v_{out}(2n) = \mathbf{a} \cdot (\mathbf{b} + \mathbf{c}), \tag{3.34}$$

where

$$\mathbf{a} = \frac{K_{TVC}}{2} \begin{bmatrix} 1 & 1/2 \cdots 1/2^{n-1} \end{bmatrix}^T, \tag{3.35}$$

$$\mathbf{b} = \begin{bmatrix} \Delta t_{C1}(n) & \Delta t_{C1}(n-1) \cdots \Delta t_{C1}(1) \end{bmatrix}^T, \tag{3.36}$$

$$\mathbf{c} = \frac{1}{4} \begin{bmatrix} \Delta T_{err}(n) & \Delta T_{err}(n-1) \cdots \Delta T_{err}(1) \end{bmatrix}^T, \tag{3.37}$$

where vectors $\mathbf{b}$ and $\mathbf{c}$ represent the sample vectors for the sampled values of $\Delta t_{C1}(n-k)$ and $\Delta T_{err}(n-k)$, respectively. Expanding (3.34) yields

$$v_{out}(2n) = \|\mathbf{a}\| \, \|\mathbf{b}\| \cos\theta + \|\mathbf{a}\| \, \|\mathbf{c}\| \cos\phi. \tag{3.38}$$

where θ and ϕ are the angles between vectors $\mathbf{a}$ and $\mathbf{b}$, and $\mathbf{a}$ and $\mathbf{c}$, respectively. Comparing (3.38) to (3.33) yields $\theta = 0$ and $\phi = \pi$, so that

$$v_{out}(2n) = \|\mathbf{a}\| \, (\|\mathbf{b}\| - \|\mathbf{c}\|). \tag{3.39}$$

Therefore, $\|\mathbf{b}\| \neq \|\mathbf{c}\|$ and $\mathbf{a}$ is in-phase with $\mathbf{b}$ and 180° out-of-phase with $\mathbf{c}$ in steady-state. Let $L \in \mathbb{R}^+$ be the steady-state value of $v_{out}(2n)$, then from (3.39) we can write

$$\|\mathbf{b}\| - \|\mathbf{c}\| = \frac{L}{\|\mathbf{a}\|}. \tag{3.40}$$

Squaring (3.40) yields

$$\|\mathbf{b}\|^2 - 2\|\mathbf{b}\|\|\mathbf{c}\| + \|\mathbf{c}\|^2 = \frac{L^2}{\|\mathbf{a}\|^2}, \tag{3.41}$$

which can be written in the form

$$(\mathbf{b}-\mathbf{c})\cdot(\mathbf{b}-\mathbf{c}) = \frac{L^2}{\|\mathbf{a}\|^2}. \tag{3.42}$$

Expanding the left side of (3.42) gives

$$\|\mathbf{b}\|^2 - 2\|\mathbf{b}\|\|\mathbf{c}\|\cos\psi + \|\mathbf{c}\|^2 = \frac{L^2}{\|\mathbf{a}\|^2}, \tag{3.43}$$

where ψ is the angle between the vectors $\mathbf{b}$ and $\mathbf{c}$. Comparing (3.41) to (3.43) shows that $\psi = 0$ so that the vectors $\mathbf{b}$ and $\mathbf{c}$ are in-phase with each other in steady-state.

Therefore, the iFDD reaches a steady-state value only when the vectors $\mathbf{b}$ and $\mathbf{c}$ are in-phase and the difference between their magnitudes is given by (3.40). The above derivations agree with our earlier observation regarding the sums in (3.33). Consequently, if the terms $\Delta t_{C1}(n-k)$ and $\Delta T_{err}(n-k)$ in the two summations in (3.33) are out-of-phase, then $v_{out}(2n)$ will not reach a steady-state value.

3.2.4 Effect of Duty-Cycle Variation

The previous derivations presented in Section 3.2.2 are based on the assumption that v_{osc} and v_{ref} are both 50% duty-cycle waveforms. In practice, however, this may not occur as one of the waveforms may have a 50% duty-cycle while the other waveform does not. Therefore, an analysis of the effect of duty-cycle variation is warranted. Let d_{osc} and d_{ref} represent the duty-cycle factors for v_{osc} and v_{ref}, respectively, defined by

$$d_{osc} = \frac{T_{osc,H}}{T_{osc}}, \tag{3.44}$$

$$d_{ref} = \frac{T_{ref,H}}{T_{ref}}, \tag{3.45}$$

where $T_{osc,H}$ and $T_{ref,H}$ represent the time duration for which v_{osc} and v_{ref} are high, respectively. Therefore, we can write $T_{osc,H} = d_{osc}T_{osc}$ and $T_{ref,H} = d_{ref}T_{ref}$. Following the same order of operations presented in Section 3.2.2, we have

$$v_{C_1}(1) = \frac{I}{C}\Delta t_{C_1}(1), \tag{3.46}$$

after charging of C_1, where we have set C_1=C_2=C_3=C_4=C. Then after charge-sharing between C_1 and C_3 we have,

$$v_{out}(1) = \frac{I}{2C}\Delta t_{C_1}(1). \tag{3.47}$$

Similarly, for capacitors C_2 and C_4 we have for the charging and charge-sharing operations

$$v_{C_2}(1) = \frac{I}{C}\Delta t_{C_2}(1), \tag{3.48}$$

$$v_{C_4}(1) = \frac{I}{2C}\Delta t_{C_3}(1). \tag{3.49}$$

Next, after the clock signal ϕ_f goes high, charge-sharing between C_3 and C_4 occurs so that

$$v_{out}(2) = \frac{I}{4C}\left(\Delta t_{C_1}(1) + \Delta t_{C_2}(1)\right). \tag{3.50}$$

Consequently, the change in the output voltage is

$$\Delta v_{out}(2) = v_{out}(2) - v_{out}(1) = \frac{I}{4C}\left(\Delta t_{C_2}(1) - \Delta t_{C_1}(1)\right). \tag{3.51}$$

But,

$$\Delta t_{C_1}(1) - \Delta t_{C_2}(1) = d_{osc}T_{osc}(1) - d_{ref}T_{ref}. \tag{3.52}$$

Therefore, we can write $v_{out}(2)$ in the form

$$v_{out}(2) = \frac{I}{2C}\Delta t_{C_1}(1) - \frac{I}{4C}\left(d_{osc}T_{osc}(1) - d_{ref}T_{ref}\right). \tag{3.53}$$

However, since $0 < d_{osc}, d_{ref} < 1$ and $d_{osc}, d_{ref} \in \mathbb{R}^+$, then we can write

$$d_{osc} = 1 - d'_{osc}, \tag{3.54}$$

$$d_{ref} = 1 - d'_{ref}, \tag{3.55}$$

where $d'_{osc}, d'_{ref} \in \mathbb{R}^+$. Therefore, (3.53) becomes

$$v_{out}(2) = \frac{I}{2C}\Delta t_{C_1}(1) - \frac{I}{4C}\left(T_{osc}(1) - d'_{osc}T_{osc}(1) - T_{ref} + d'_{ref}T_{ref}\right). \tag{3.56}$$

However, since $\Delta T_{err} = T_{osc} - T_{ref}$, then

$$v_{out}(2) = \frac{I}{2C}\Delta t_{C_1}(1) - \frac{I}{4C}\left(\Delta T_{err}(0) - \Delta T_{duty}(0)\right), \tag{3.57}$$

where $\Delta T_{duty} = d'_{osc}T_{osc} - d'_{ref}T_{ref}$. Continuing in this manner, it can be shown that

$$v_{out}(2n) = \frac{K_{TVC}}{2}\left[\sum_{k=0}^{n-1}\left(\frac{1}{2}\right)^k \Delta t_{C_1}(n-k) - \sum_{k=1}^{n}\left(\frac{1}{2}\right)^{k-1}\left(\frac{\Delta T_{err}(n-k)}{2} - \frac{\Delta T_{duty}(n-k)}{2}\right)\right], \tag{3.58}$$

where in the second summation the firsrt term is the period difference and the second term is the duty-cycle difference. In the case that $d'_{osc} = d'_{ref} = 0.5$, (3.58) reduces to the 50% duty-cycle case. Therefore, the iFDD can detect duty-cycle variations.

3.2.5 Maximum Frequency of Operation

The maximum frequency of operation of the iFDD is set by the widths of clocks ϕ_{sa1} and ϕ_{rst1} or ϕ_{sa2} and ϕ_{rst2}, since their widths are identical. In particular,

$$f_{max} \leq \frac{1}{2(\tau_{sa1} + \tau_{rst1})}, \tag{3.59}$$

where τ_{sa1} and τ_{rst1} are the widths of clocks ϕ_{sa1} and ϕ_{rst1}, respectively. However, since the widths of ϕ_{sa1} and ϕ_{rst1} are set by the delay τ in Fig.3.3, then $\tau_{sa1} = \tau_{rst1} = \tau$ so that

$$f_{max} \leq \frac{1}{4\tau}. \tag{3.60}$$

Therefore, a smaller τ yields are larger frequency of operation. However, a smaller τ requires a smaller capacitance in order for the charge-sharing operation between C_1/C_2 and

C_3/C_4 and C_3 and C_4 to complete successfully. This would result in larger thermal noise from the capacitors since the power of the thermal noise from a capacitor is given by

$$\overline{v_n^2} = \frac{kT}{C}, \tag{3.61}$$

where k is Boltzmann's constant and T is temperature in Kelvin's. Thus, a smaller capacitance results in larger kT/C noise, whereas a larger capacitance reduces it. Therefore, a tradeoff exists between choosing the size of the capacitors and the maximum frequency of operation.

3.3 Design of the FLL

To design the frequency-locked loop (FLL), first a model of the iFDD must be obtained. Note that since the input signals to the iFDD are frequencies, then the VCO can be modelled as a constant gain block with a gain of K_{VCO}.

3.3.1 Model of the iFDD

To determine a model of the iFDD, consider (3.31) with $\alpha_3 = 1$, $\alpha = 1$. Since the two charge-sharing operations between C_1 and C_3 and C_3 and C_4 occur within one cycle of the reference signal, then we can write (3.31) in the following form

$$v_{out}(nT_{ref}) \approx v_{out}(nT_{ref} - \gamma T_{ref}) + K_{iFDD}\Delta f(nT_{ref} - \gamma) \tag{3.62}$$

where γT_{ref} represents the time from the first charge-sharing operation between C_1 and C_3 to the second charge-sharing operation between C_3 and C_4, $K_{iFDD} = -\frac{K_{TVC}}{8f_{ref}^2}$, and we have assumed that $f_{ref}f_{osc} \approx f_{ref}^2$ in simplifying (3.62). Therefore, performing the $\mathcal{Z}$-transform on (3.62) yields the following transfer function of the iFDD

$$\begin{aligned} H_{iFDD}(z) &\equiv \frac{V_{out}(z)}{\Delta f(z)} \approx \frac{K_{iFDD} z^{-\gamma}}{1 - z^{-\gamma}} \\ &\approx \frac{K_{iFDD}}{z^{\gamma} - 1} \end{aligned} \tag{3.63}$$

Since $z = e^{sT_{ref}}$, then performing a Maclaurin series expansion on z^{γ} gives

$$z^{\gamma} = e^{s\gamma T_{ref}} = 1 + (\gamma T_{ref})s + \frac{(\gamma T_{ref})^2 s^2}{2} + \cdots. \tag{3.64}$$

Since $0 < \gamma < 1$, then ignoring terms greater than second-order in (3.64) and substituting the result into (3.62) yields

$$H_{iFDD}(s) \approx \frac{K_{iFDD}}{s\left[\gamma T_{ref} + \frac{(\gamma T_{ref})^2 s}{2}\right]}. \tag{3.65}$$

Equation (3.65) shows that the iFDD has a pole at $s = 0$ and another pole at $s = -2/(\gamma T_{ref})$. The pole at the origin allows the iFDD to integrate the frequency error. Indeed, the accumulation operation performed in (3.31) illustrates the integration performed by the iFDD. In addition, (3.31) shows that the iFDD behaves as a first-order, low-pass IIR filter. To illustrate this, replace z^{γ} in (3.63) with $z^{\gamma} = e^{j\gamma\omega}$, then we have

$$H_{iFDD}(e^{j\omega}) \approx \frac{K_{iFDD}}{e^{j\gamma\omega} - 1}, \tag{3.66}$$

from which we obtain the following magnitude and phase responses of the iFDD

$$\left\| H_{iFDD}(e^{j\omega}) \right\| \approx \frac{|K_{iFDD}|}{\sqrt{2}} \frac{1}{\sqrt{1 - \cos\gamma\omega}}, \tag{3.67}$$

$$\angle H_{iFDD}(e^{j\omega}) \approx -\tan^{-1}\left(\frac{\sin\gamma\omega}{1 - \cos\gamma\omega}\right). \tag{3.68}$$

Equation (3.67) shows that the magnitude response of the iFDD has poles that are located at $\omega = 0, 2k\pi/\gamma$ for $k \in \mathbb{Z}$, whereas (3.68) shows that the iFDD has a non-linear

phase delay. The magnitude and phase response of (3.67) and (3.68) shown in Fig.3.4 and Fig.3.5 demonstrate that the iFDD behaves as a low-pass IIR filter, thus confirming our earlier observation.

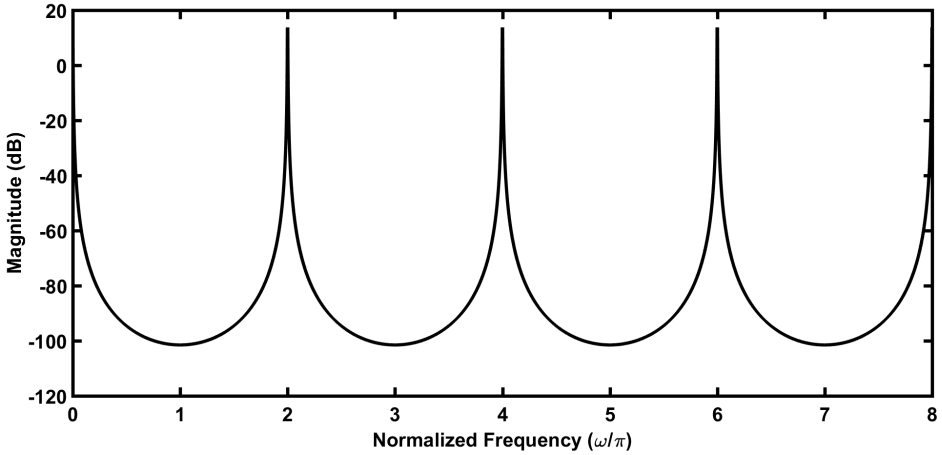

Figure 3.4: Magnitude response of the iFDD with respect to normalized frequency.

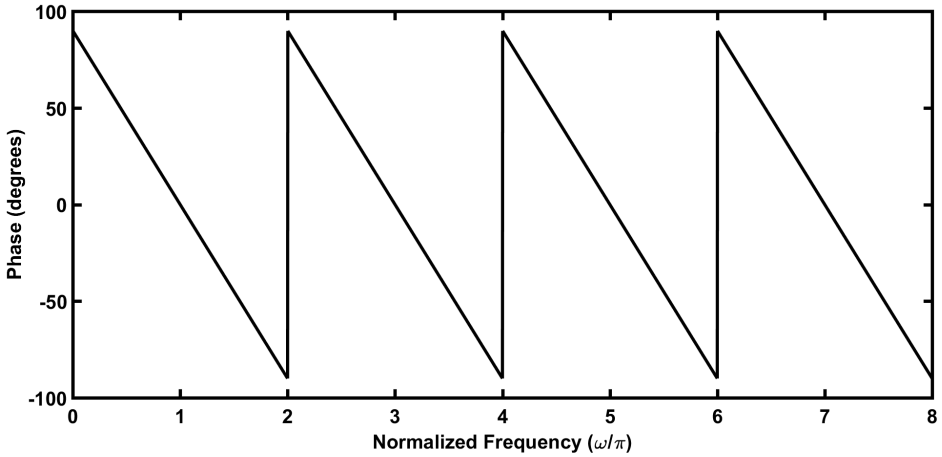

Figure 3.5: Phase response of the iFDD with respect to normalized frequency.

3.3.2 Model of the FLL

Fig.3.6 shows the model of the FLL in the discrete-time domain. Note that the VCO is modelled as a constant gain, as mentioned earlier. From Fig.3.6 and using the transfer function of the iFDD given by (3.65), then the open-loop transfer function of the FLL in the s-domain, $H_{ol}(s)$, is

$$H_{ol}(s) \approx \frac{K}{\frac{(\gamma T_{ref})^2}{2}s^2 + (\gamma T_{ref})s}, \tag{3.69}$$

where $K = K_{iFDD}K_{VCO}$ is the loop gain factor. From (3.69) it can be shown that the phase margin, PM, of the open-loop system is given by

$$PM = \pi + \tan^{-1}\left(\sqrt{\frac{2}{\sqrt{1+K^2}-1}}\right), \tag{3.70}$$

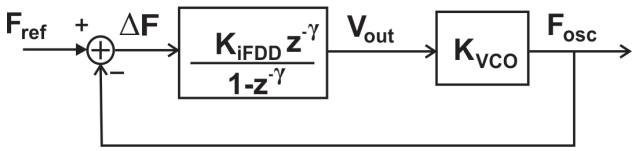

Figure 3.6: Discrete-time model of the FLL.

From Fig.3.6 and (3.69), it can be shown that the closed-loop transfer function, $H_{cl}(s) \equiv F_{osc}(s)/F_{ref}(s)$, is given by

$$H_{cl}(s) \approx \frac{2K/(\gamma T_{ref})^2}{s^2 + \frac{2}{\gamma T_{ref}}s + \frac{2K}{(\gamma T_{ref})^2}}. \tag{3.71}$$

Equation (3.71) can be written in standard second-order form as

$$H_{cl}(s) \approx \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{3.72}$$

where

$$\omega_n = \frac{\sqrt{2K}}{\gamma T_{ref}}, \tag{3.73}$$

$$\zeta = \frac{1}{\sqrt{2K}}, \tag{3.74}$$

are the natural frequency and damping factor of the closed-loop system, respectively. From (3.71), the closed-loop error transfer function, $H_e(s)$, is given by

$$\begin{aligned} H_e(s) &= 1 - H_{cl}(s) \\ &\approx \frac{s\left(s + 2\zeta\omega_n\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \end{aligned} \tag{3.75}$$

Therefore, by the final value theorem, the steady-state frequency error when a unit-step in the reference frequency occurs is

$$\begin{aligned} \Delta f_{err,ss} &= \lim_{s\to 0}(s\Delta F_{err}(s)) \\ &= \lim_{s\to 0}\left(\frac{s\left(s + 2\zeta\omega_n\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2}\right) \\ &= 0. \end{aligned} \tag{3.76}$$

Thus the FLL has zero steady-state frequency error. From (3.70) and $K = -\frac{IK_{VCO}}{8Cf_{ref}^2}$, an optimal value of C can be found. However, I and C cannot be chosen independently. Since the value of C effects both the gain and consequently the stability of the system as well as the noise contributed by the iFDD, then I was fixed at 100 nA to provide a low power consumption, while still providing a large enough charging current for capacitors C_1 and C_2. Next, the VCO was designed to have a tuning range that at least covers 20% above and below f_{ref}, which in our design is 1 MHz. Through simulations in SpectreRF, the gain of the VCO, K_{VCO}, that met the requirement was found to be -8.2 MHz/V. Plots of equation (3.70) and C versus K are shown in Fig.3.7 and Fig.3.8.

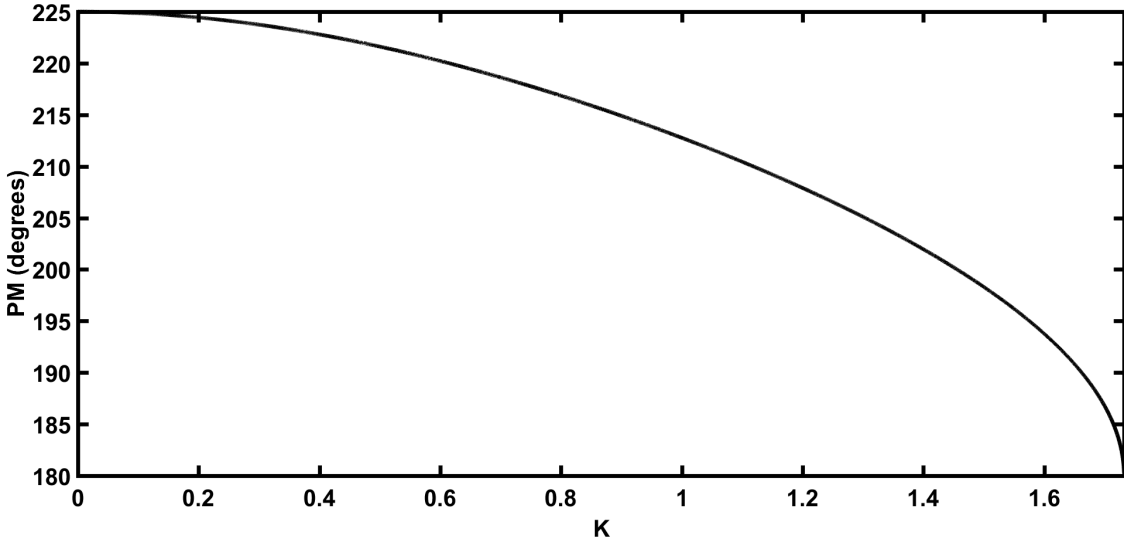

Figure 3.7: Pot of phase margin (PM) vs. loop gain factor, K.

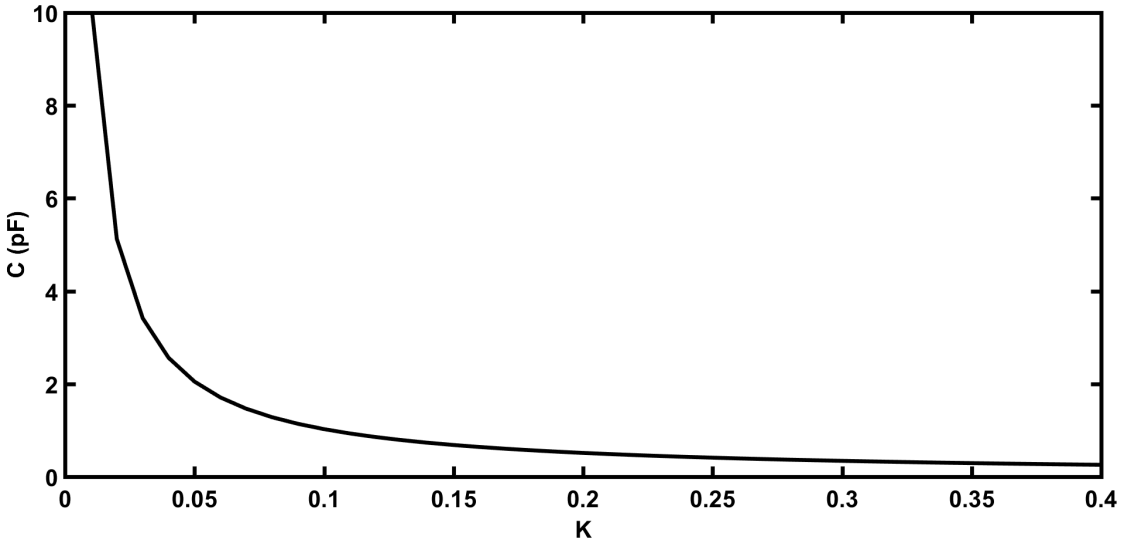

Figure 3.8: Plot of C vs. loop gain factor, K, with $I = 100$ nA.

From the plots in Fig.3.7 and Fig.3.8 we see that as K increases the phase margin decreases. Thus the stability of the system degrades as K increases and since $K \propto 1/C$, where C is the value of the capacitor in the TVC, then decreasing C reduces the stability of the system as seen in Fig.3.7. This also comes at the expense of increased thermal noise from the capacitors in the iFDD, according to (3.61). Therefore, good stability and low thermal noise can be achieved by making C large. However, this comes at the expense

of an increased damping factor, ζ, and a longer transient response according to (3.74). Furthermore, increasing C will increase the dynamic power consumption of the circuit, since $P_{dynamic} \propto C$. To ensure good stability by providing large phase margin, from Fig.3.7 we choose $K \approx 0.1$, which corresponds to $C \approx 1$ pF from Fig.3.8.

3.3.3 Speed and Noise Considerations

From (3.18) and (3.19) we can see that the proportion of Δt_{C_1} and Δt_{C_2} that is contributed to the sample-and-hold capacitors, C_3 and C_4, can be increased by making α ($=\alpha_1=\alpha_2$) small. Doing so will increase the step-size of v_{out} and v_{C_4} and thus improve the speed of the transient response of the FLL. Increasing the fraction of Δt_{C_1} and Δt_{C_2} to be shared with C_3 and C_4 can be achieved by either increasing C_1 and C_2 or decreasing C_3 and C_4. However, increasing C_1 and C_2 will decrease K_{TVC} and consequently result in a more over-damped transient response by reducing K, whereas decreasing C_3 and C_4 will not effect the gain of the TVC. Therefore, the lock-time of the FLL can be made shorter by decreasing the size of the sample-and-hold capacitors C_3 and C_4, without effecting the gain term K_{TVC}. This comes at the expense of degraded SNR at the output of the iFDD, since

$$SNR = \frac{(V^2/2)\,C}{kT}, \tag{3.77}$$

is the SNR for a sampling capacitor, where $V^2/2$ is the input signal power relative to a 1 Ω load and C is the value of the sampling capacitor. Since the noise from the output of the iFDD is coupled to the VCO, then a reduced SNR at the output of the iFDD will subsequently degrade the spectrum of the VCO. Therefore, a tradeoff exists between the lock-time of the FLL and the quality of the spectrum of the VCO around the desired frequency.

3.4 Chapter Summary

A new integrating frequency difference detector (iFDD) that senses the frequency difference between the local oscillator of the PWM and the input reference clock signal to generate an output voltage that is proportional to the frequency error between the oscillator

and reference clock was proposed. The iFDD utilizes a single current source to reduce the mismatch between its two integrating paths. A detailed analysis of the characteristics of the iFDD in the time and frequency domains was presented. The analysis demonstrated that the iFDD integrates the frequency error between a reference signal and the VCO. It was also shown that the iFDD is able to detect duty-cycle differences between the reference signal and the VCO signal. Further analysis showed that a trade-off exists between the maximum frequency of operation of the iFDD and thermal noise power generated by its capacitors. Additionally, it was shown that the iFDD can be modelled as a low-pass, IIR filter. Furthermore, the loop dynamics of the FLL were also investigated. It was found that the FLL achieves zero steady-state frequency error. Finally, an investigation into the relationship between the lock-time of the FLL and the SNR of the iFDD demonstrated that the lock-time of the FLL can be improved at the expense of a degraded spectrum of the VCO around the desired frequency of operation.

Chapter 4

Results

4.1 Simulation Environment Set Up

To verify the results presented in this study and quantify the performance of the proposed iFDD, a FLL with the proposed iFDD as shown in Fig.3.3 in Chapter 3 was designed in IBM 0.13-μm, 1.2 V CMOS technology and analyzed using the simulator Spectre APS (Accelerated Parallel Simulator) from Cadence Design Systems (CDS) with BSIM4v4 device models and reltol set to 1e^{-}2 to speed up the simulator without sacrificing accuracy. Metal-insulator-metal capacitors (MIM-caps) were used for capacitors $C_1 \sim C_4$. The transistor-level schematic of the iFDD is shown in Fig.4.1.

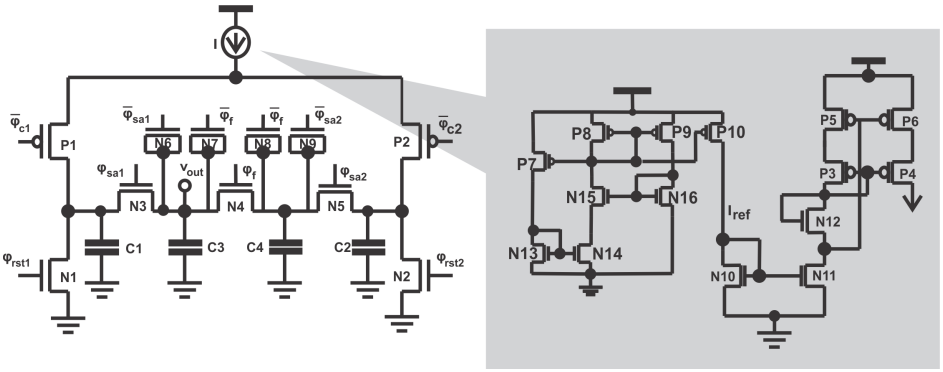

Figure 4.1: Schematic of the iFDD. Transistor sizes are: $W_{N1,N2}$ = 0.320 μm, W_{N3-N5} = 1 μm, $W_{P1,P2}$ = 0.640 μm, W_{N6-N9} = 0.5 μm, $W_{N10-N12}$ = 0.480 μm, $W_{P3,P5}$ = 0.960 μm, $W_{P4,P6}$ = 1.55 μm, $W_{N13-N16}$ = 0.480 μm, W_{P7-P9} = 0.960 μm, W_{P10} = 6 μm, $L_{N1-N12,P1,P2,P3,P5}$ = 0.120 μm, $L_{N13-N16}$ = 0.240 μm, and $L_{P4,P6-P10}$ = 0.480 μm.

A low-swing cascode current mirror circuit is used to generate the current I for the iFDD to ensure I is constant across varying load conditions and so that the iFDD can be operated at a low power supply. NMOS transistors were used as the charge-sharing switches instead of transmission gates to (1) reduce clock feedthrough, (2) minimize the parasitic capacitance contributed by the transistors to the capacitors, and (3) to minimize the silicon area consumed by the iFDD. Transistors $N6 - N9$ are dummy switches to reduce charge injection onto capacitors C_3 and C_4 when clock signals $\phi_{sa1,sa2}$ and ϕ_f are low. The transistors $N3 - N5$ are the charge-sharing switches, so they operate in the deep triode region near steady-state. Therefore, their on-resistances in steady-state are given by

$$R_{ON} \approx \frac{1}{K_N \left(\frac{W}{L}\right) (V_{GS} - V_{th,N})}. \tag{4.1}$$

Through simulations, the pulse-widths of the clock signals ϕ_{sa1}, ϕ_{sa2}, ϕ_{rst1}, ϕ_{rst2}, and ϕ_f that allowed capacitors C_1 and C_3 and C_2 and C_4 (where all capacitors were set to 1 pF) to complete charge redistribution before the clock signals went to logic-0 was found to be ≈ 50 ns. Therefore, the time constant of the switches must be (50ns/5 =) 10 ns and the maximum on-resistance of the charge-redistribution switches is $R_{ON,max}$ (50ns/1pF =) 10 kΩ. Thus, $0 < R_{ON} \leq 10\text{k}\Omega$. From the previous inequality and (4.1) and using $K_N = 500$ μA/V^2 and $V_{th,N} = 0.36$ V as obtained from DC simulations using SpectreRF, we have $\frac{W}{L} \geq 2$. Using minimum-length transistors of $L = 120$ nm, the minimum-width of the switches is $W_{min} = 240$ nm. Therefore, to ensure a low on-resistance for the charge-redistribution switches throughout their operation, their widths were set to 1 μm and their lengths were all set to the minimum channel length of 0.120 μm, so that $\frac{W}{L} \approx 8.3$.

The logic control block (LCB) in Fig.3.3 in Chapter 3 used NAND2 and NAND3 logic gates to implement the rising-edge DFFs rather than the TSPC approach to lower their power consumption. The AND2 logic gates used to generate clock signals ϕ_{C_1} and ϕ_{C_2} were implemented using a low-skew design to help ensure that the clock signals ϕ_{C_1} and ϕ_{sa1}, and ϕ_{C_2} and ϕ_{sa2} do not overlap. The inverters in the clock generator circuit were implemented using minimum average delay sizing to reduce their delay.

A relaxation VCO with a pair of current-starved inverters, two comparators, and an SR-latch was used to generate v_{osc}. The schematic of the VCO is shown in Fig.4.2. Capacitors C_r are tuning capacitors that allow easier tuning of the VCO tuning curve and were set to 1.75 pF to obtain the desired tuning curve of the VCO. The PMOS load transistor, $P7$, was used to give the required negative tuning curve of the VCO. The bias voltages, V_{bias} were set 330 mV to operate the comparators, formed by transistors $N3 - N4$ and $P3 - P4$, and $N5 - N6$ and $P5 - P6$, in subthreshold.

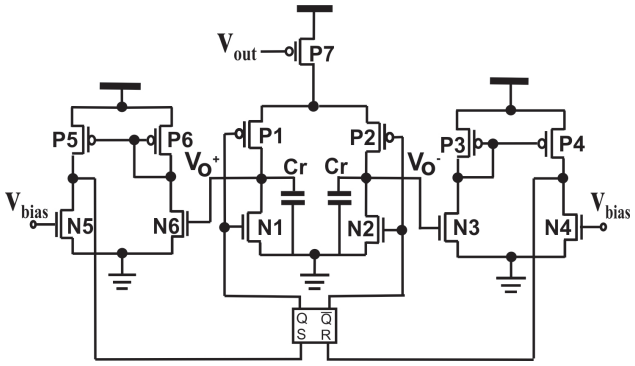

Figure 4.2: Schematic of the relaxation VCO that was used to generate v_{osc}. Transistor sizes are: $W_{N1-N6} = 0.350$ μm, $W_{P1-P7} = 0.700$ μm, and $L_{N1-N6,P1-P7} = 0.120$ μm. The value of the tuning capacitors, C_r, was set 1.75 pF.

The power supply was set to 0.5 V in our design to provide an ultra-low power consumption, while still allowing the VCO to operate at the required frequency of 1 MHz. A plot of the free-running VCO frequency versus V_{DD} is shown in Fig.4.3. This graph shows that operating the VCO at a power supply of 0.5 V allows it to have a free-running frequency near 1 MHz. Consequently, this allows for the tuning capacitors, C_r, to be small which further reduces power consumption from the VCO.

A plot of the tuning curve of the VCO across all five process corners is shown in Fig.4.4. From Fig.4.4 we see that the free-runnung frequency of the VCO varies significantly across the ff, fs, sf, and ss process corners. Additionally, Fig.4.5 and Fig.4.6 show that the free-running frequency of the VCO can vary by $\pm 20\%$ for a $\pm 20°$C temperature change and

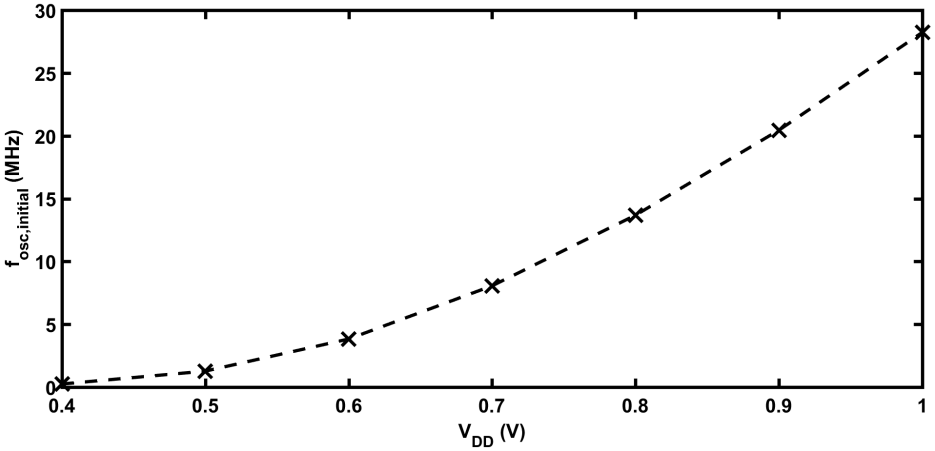

Figure 4.3: Free-running frequency of VCO versus V_{DD}.

by $\pm 20\%$ for a ± 15 mV change in V_{DD}. Thus the free-running frequency of the VCO is very sensitive to PVT variations, hence the need for frequency calibration.

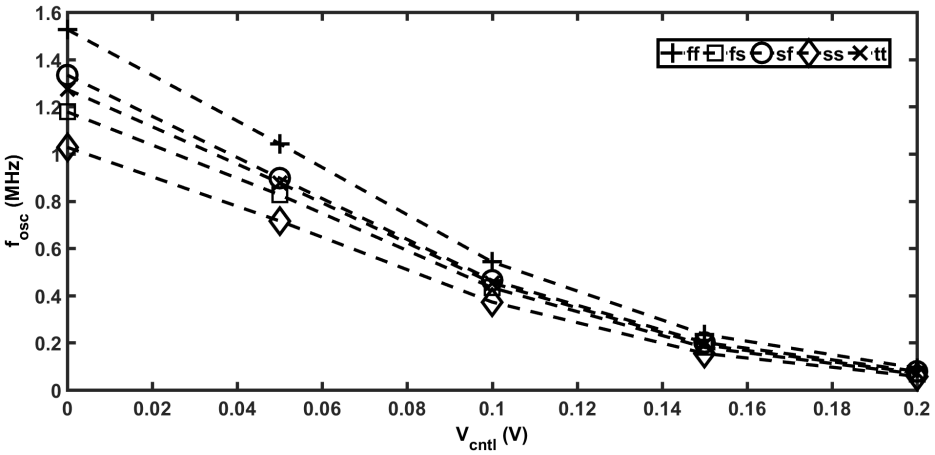

Figure 4.4: VCO tuning curve across tt, ff, fs, sf, and ss process corners.

4.2 Simulation Results

An open-loop test was performed on the iFDD to obtain the graph of Δv_{out} versus Δf_{err} and demonstrate its linearity. Two 50% duty-cycle square-waves were used as input signals to the iFDD. The frequency error, Δf_{err}, was swept from -0.2 MHz to 0.2 MHz in 0.05

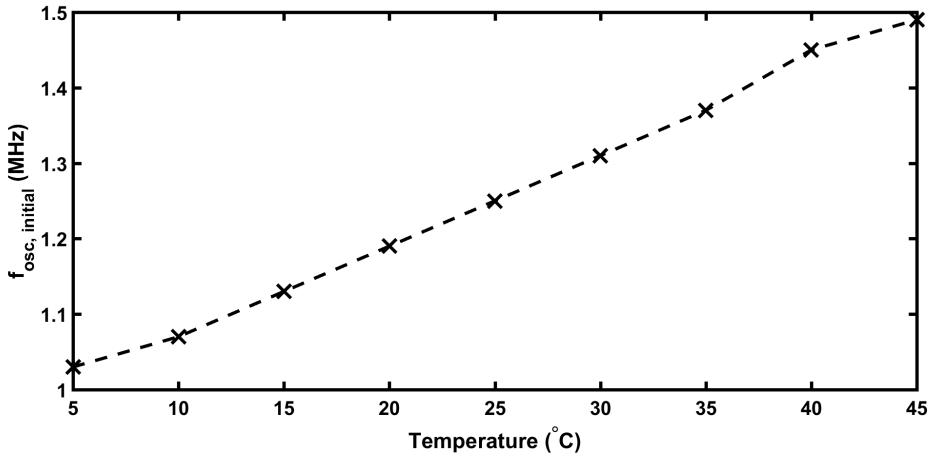

Figure 4.5: Free-running VCO frequency $\sim$ temperature relation.

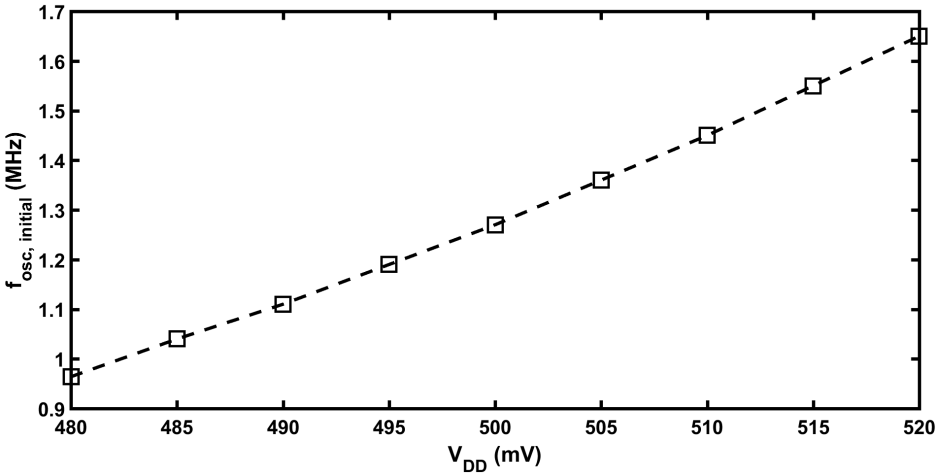

Figure 4.6: Free-running VCO frequency $\sim V_{DD}$ relation.

MHz steps. The frequency error was only swept in this range since the VCO free-running frequency can vary by as much as $\pm 20\%$ from its desired frequency as seen from Fig.4.5 and Fig.4.3. Since the targeted frequency in our design is 1 MHz, then $\pm 20\%$ corresponds ± 0.2 MHz around 1 MHz. A plot of Δv_{out} versus Δf_{err} is shown in Fig.4.7, which shows that the simulation results agree well with the theory. However, a slight deviation between the simulation and theoretical results exists because it was found that the current source that was implemented in Cadence had a value of 95 nA, as opposed to the 100 nA used in the

calculations. This would result in a slightly smaller gain obtained from simulations, which is evident in Fig.4.7.

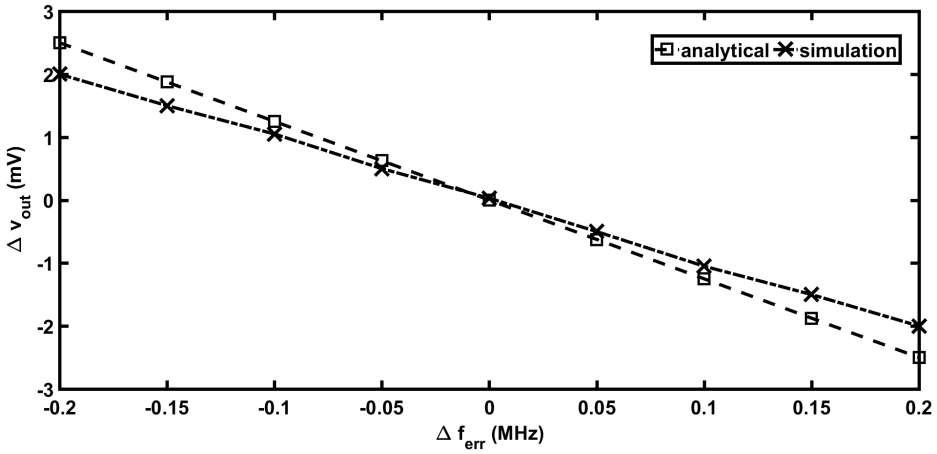

Figure 4.7: $\Delta v_{out} \sim \Delta f_{err}$ relation.

Transient simulations of the FLL were performed using a 1 MHz, square-wave signal as the reference clock that is provided by the reader as a timing signal for calibation. The FLL was simulated across all process corners, as well as fast and slow corners to test its stability in the presence of PVT variations. In addition, the duty-cycle of the reference signal was varied from 38%, 50%, and 63% to test the FLL's ability to detect and operate correctly in the presence of duty-cycle variations from the reference signal. Additionally, the FLL was simulated for different α ($=\alpha_1=\alpha_2$) values to examine their effect on the lock-time of the FLL and the spectrum of the VCO. The results are shown in Fig.4.8, Fig.4.9, Fig.4.10, Fig.4.11, Fig.4.12, Fig.4.13, Fig.4.14, Fig,4.15, and Fig.4.16.

The plot of the transient response of v_{out} shown in Fig.4.8 illustrates that the output voltage consists of two steps within any cycle of operation, where the first, larger step is from the Δt_{C_1} terms and the second, smaller step is the corrective term from ΔT_{err}. This agrees well with our earlier observations. The transient response of f_{osc} to a 1 MHz, 50% duty-cycle frequency step shown in Fig.4.9 demonstrates that the VCO locks to the 1 MHz reference signal within 14 μs. The transient response of Δf_{err} in Fig.4.10 shows that there is zero steady-state frequency error, which agrees with our earlier prediction in (3.76). Fig.4.11

shows that the FLL can still lock to the 1 MHz clock signal even if the signal does not have a 50% duty-cycle, as predicted from our earlier analysis. The transient response of f_{osc} to an input frequency step of 1 MHz across the ff, fs, sf, and ss process corners shown in Fig.4.12 demonstrates the stability of the FLL across all process corners. Finally, the transient response of f_{osc} at fast and slow corners shown in Fig.4.13 validates the stability of the FLL in the presence of PVT variations.

Table 4.1 summarizes the power consumption of each block of the FLL across all process corners. The results from this table show that (1) the total power consumption of the FLL is < 1.7 μW across all process corners, (2) the iFDD consumes the least amount of power of all the blocks, and (3) the VCO consumes more than 50% of the total power of the FLL. Therefore, a much lower power consumption can be achieved by using a VCO with ultra-low power consumption. Fig.4.14 shows that the lock-time of the FLL is shortened by making α smaller, as predicted earlier. In particular, the lock-time (within $\pm 1\%$ of f_{ref}) for α=$\{0.25, 0.5, 1\}$ was found to be 8.76 μs, 9.27 μs, and 13.53 μs, respectively. This result is further illustrated in Fig.4.16, which shows the relationship between the lock-time of the FLL and α. However, decreasing α comes at the cost of a degraded spectrum for the VCO, as seen in Fig.4.15. Fig.4.15 shows that as α decreases, the magnitude of the second-order harmonic increases and the spectrum of the VCO around 1 MHz gets wider, which implies that the power of the VCO signal at 1 MHz is becoming less concentrated at that desired frequency. This result also agrees with our earlier observation in Section 3.3.3, since decreasing α reduces the SNR at the output capacitor C_3. Table 4.2 summarizes the lock-time simulation results across all process corners, which shows that the FLL can achieve lock with the 1 MHz reference signal within 20 μs across all process corners. Table 4.3 compares this work to previous state-of-the-art designs for clock recovery and calibration techniques for PWMs. Note that the works presented in the table are all from post-fabrication measurements. From Table 4.3 we see that the frequency accuracy of our work meets the minimum requirement of $\pm 2.5\%$ for the frequency variation of the backscattered data, as required by EPC C1G2 UHF RIFD protocols [3]. In addition, the results presented in Table 4.3 show that our proposed frequency calibration technique achieves the best calibration time and frequency accuracy compared to previous works. Furthermore, since the FLL can operate at a low supply voltage,

then it can be implemented in PWMs that operate at large read-to-transponder distances, since such PWMs typically operate at power supplies < 1 V [2].

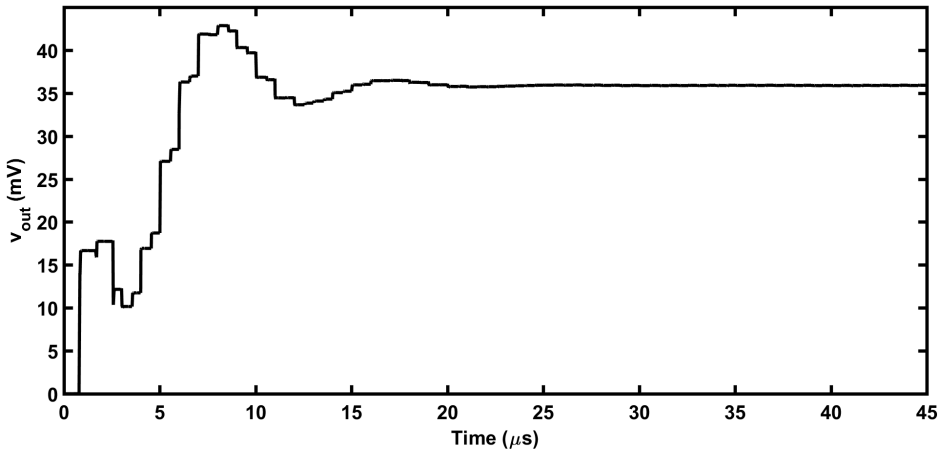

Figure 4.8: Control voltage of relaxation oscillator in response to an input frequency step of 1 MHz with 50% duty-cycle.

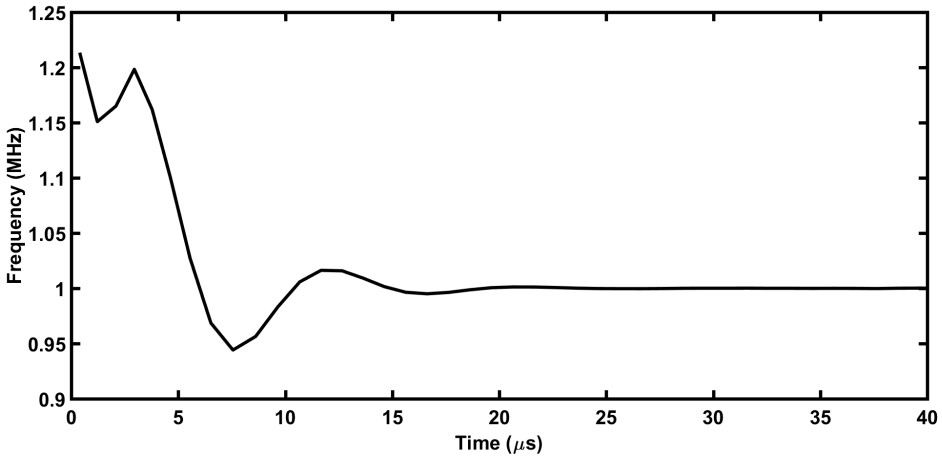

Figure 4.9: Transient response of the frequency of the relaxation oscillator, f_{osc}, with a 1 MHz, 50% duty-cycle reference clock input.

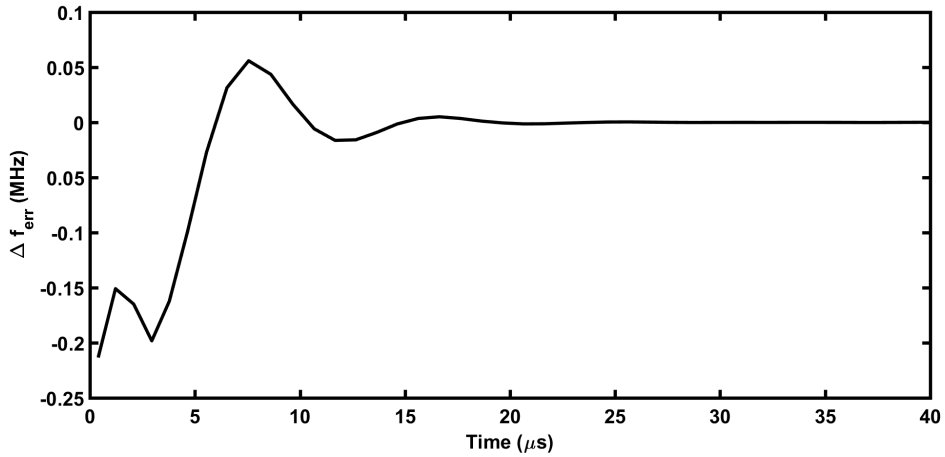

Figure 4.10: Transient response of the frequency error, Δf_{err}, in response to an input frequency step of 1 MHz with 50% duty-cycle.

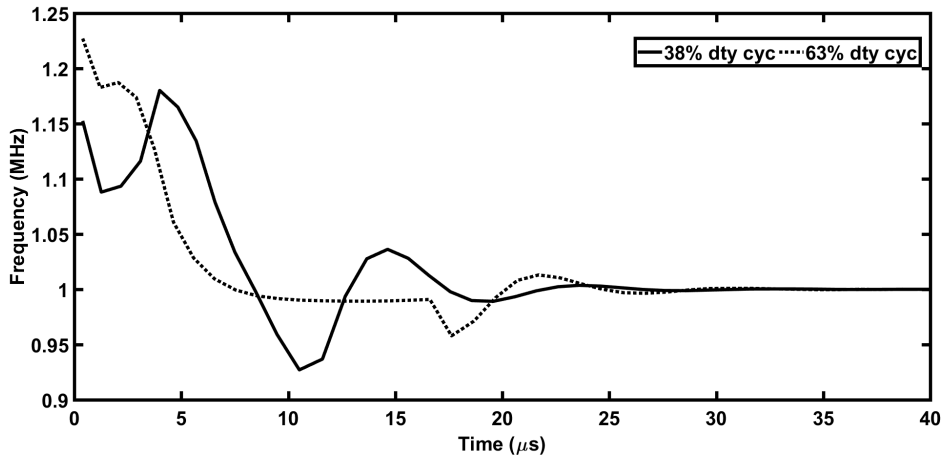

Figure 4.11: Transient response of f_{osc} to an input frequency step of 1 MHz with duty-cycles of 38% and 63%.

Table 4.1: Simulation Results of Power Consumption of FLL (Unit: μW).

Block	tt	ff	fs	sf	ss
LCB	0.482	0.5384	0.5247	0.4621	0.4698
iFDD	0.0909	0.2695	0.1286	0.0739	0.0235
VCO	0.6955	0.8396	0.7637	0.6763	0.6638
Total	1.27	1.651	1.42	1.214	1.16

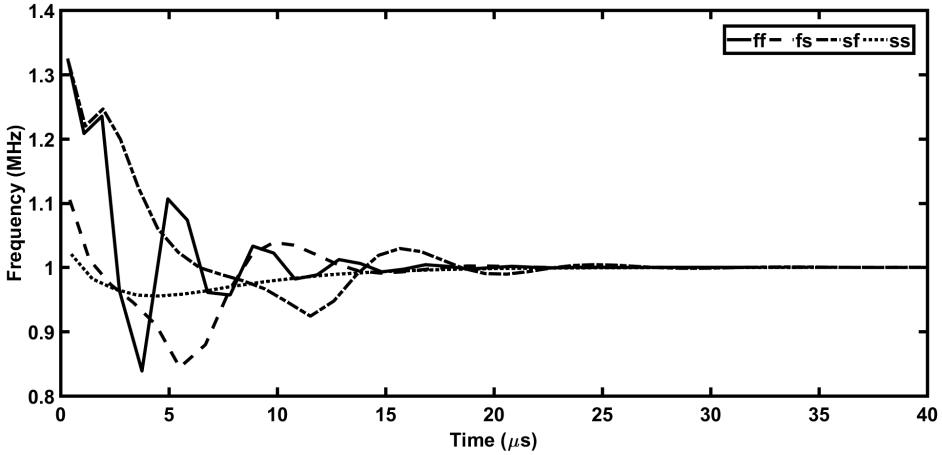

Figure 4.12: Transient response of f_{osc} to an input frequency step of 1 MHz with 50% duty-cycle across ff, fs, sf, and ss process corners.

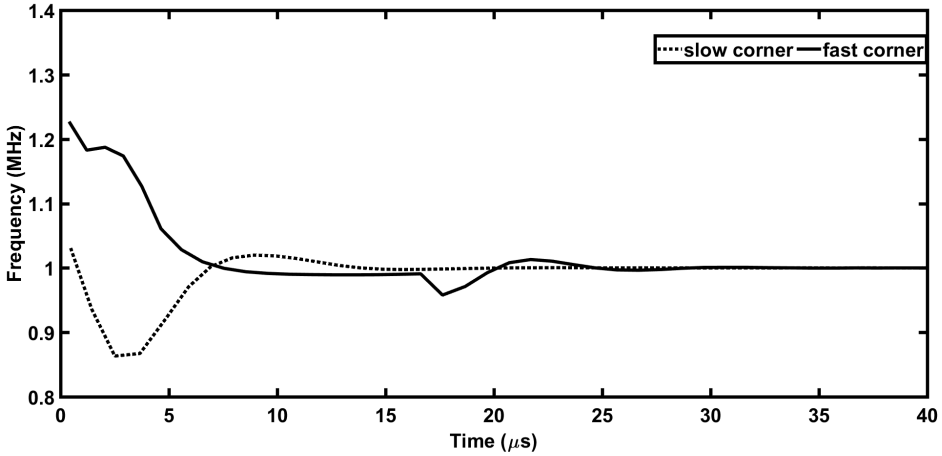

Figure 4.13: Transient response of f_{osc} to an input frequency step of 1 MHz with 50% duty-cycle at fast (V_{DD} = 535 mV, T = -25°C, ff process) and slow (V_{DD} = 465 mV, T = 85°C, ss process) corners.

4.3 Chapter Summary

A frequency calibration technique that allows for accurate tuning of the frequency of a local oscillator in a PWM using an ultra-low power, fast-locking frequency-locked (FLL) that is embedded with an integrating frequency difference detector (iFDD) has been proposed. A relaxation oscillator with a current-starved inverter pair with a PMOS load was employed as the VCO of the FLL to realize the required negative tuning curve of the VCO for stable FLL operation. The power consumption of the proposed FLL was effectively reduced by

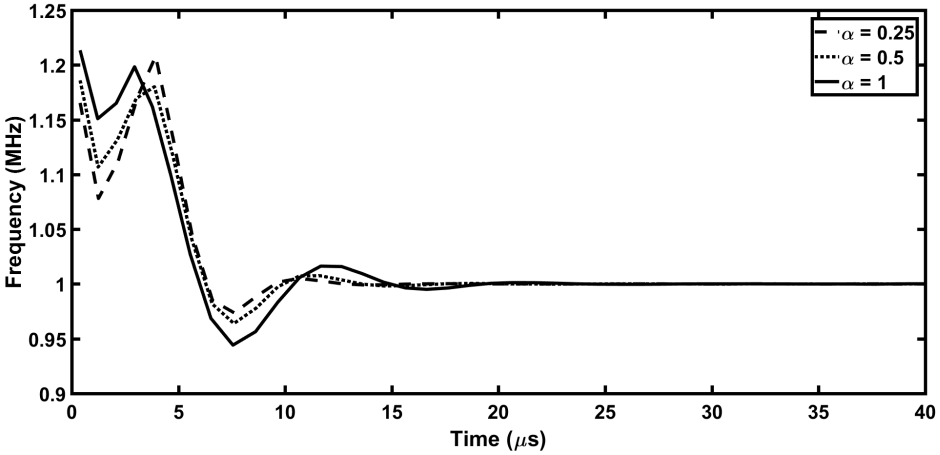

Figure 4.14: Transient response of f_{osc} to an input frequency step of 1 MHz with 50% duty-cycle with $\alpha = \{0.25, 0.5, 1\}$. Lock-time (within $\pm 1\%$ of f_{ref}) for α=$\{0.25, 0.5, 1\}$: 8.76 μs, 9.27 μs, and 13.53 μs, respectively

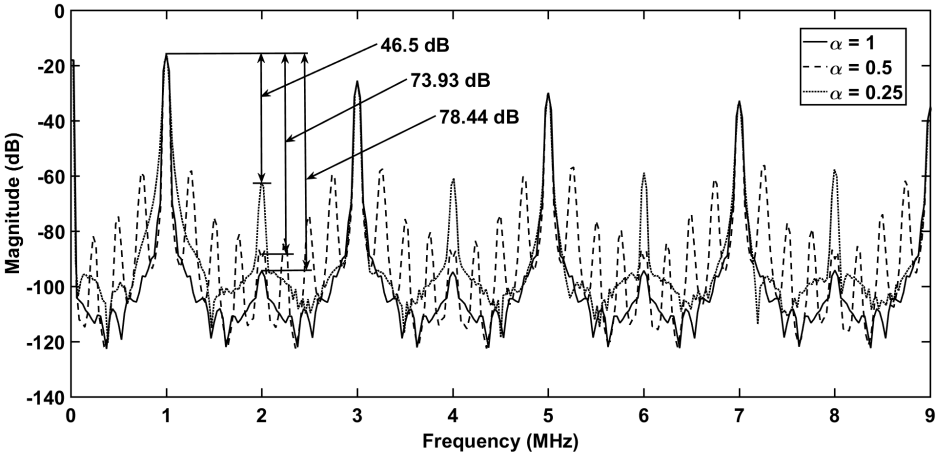

Figure 4.15: Spectrum of VCO for $\alpha = \{0.25, 0.5, 1\}$.

Table 4.2: Simulation Results of Lock-time of FLL to a 1 MHz, 50% Duty-Cycle Reference Signal with $\alpha = 1$.

Process Corner	Lock-time (μs) ($\pm 1\%$)
tt	13.53
ff	13.18
fs	12.42
sf	20.74
ss	13.22

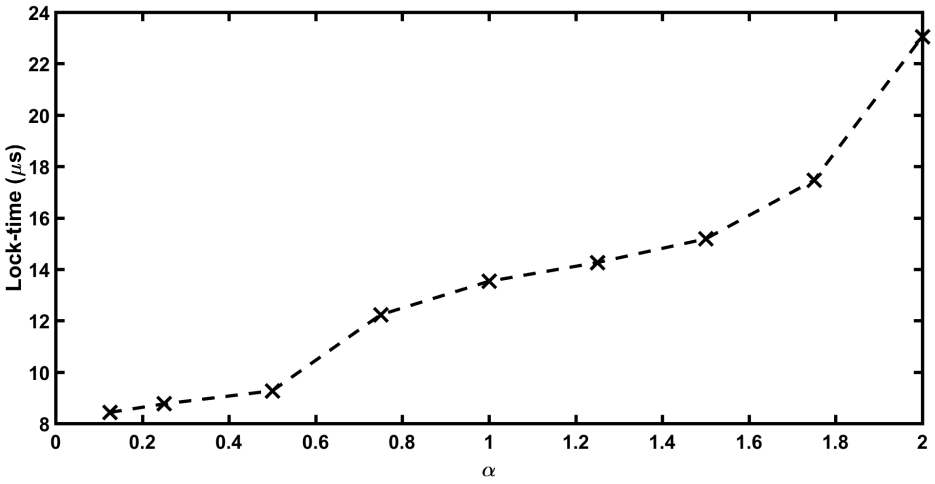

Figure 4.16: Simulated lock-time (within ±1% of f_{ref}) versus α.

Table 4.3: Comparison with Prior Clock Recovery and Clock Calibration Technigues for PWMs*.

Ref.	Tech.	V_{DD} (V)	Clock freq. (MHz)	Power (μW)	Clock accuracy	Calib. time	Lock range (MHz)
[15][1]	0.18μm	0.5 and 1	3.5	7	164 ps peak-to-peak jitter	-	525
[16][1]	0.18μm	1.1	902-928	4.12	-	-	-
[17][1]	0.35μm	1.5	2.2	31	0.91%	-	-
[18][1]	0.35μm	3.3	6.78	17	7.5 %	<200μs	
[13][2]	0.18μm	1	2.56	2	-3.2% to +1.2%	<16 PIE	2
[19][2]	0.18μm	1.2	1	0.96	-	<100μs	0.430
This work[2]	0.13μm	0.5	1	1.27	<0.01%	<21μs	1.2

1 Clock recovery method
2 Clock calibration method
* Results from previous works are from post-fabrication measurements

operating the LCB, iFDD, and relaxation oscillator in subthreshold. The proposed FLL was implemented in IBM 0.13-μm, 1.2 V CMOS technology with BSIM4v4 device models. The theoretical results of the proposed FLL were evaluated using simulation results obtained from Spectre APS in CDS with reltol set to 1e^{-}2. The proposed FLL could operate at a power supply as low as 0.5 V and consumed a total power of 1.27 μW, while achieving a calibration <9μs, a lock range of 1.2 MHz, and a frequency variation < 0.01% in the lock-state, thus meeting the stringent frequency accuracy requirement of ±2.5% for the clock in the EPC C1G2 UHF RFID protocol. Of the 1.27 μW, the proposed iFDD consumed only 90 nW, accounting for only 7% of the total power. The FLL also exhibits excellent robustness in the presence of PVT variations and has zero steady-state frequency error. Compared to previous

clock generation techniques in [13, 15, 16, 17, 18, 19], our proposed frequency calibration techniques achieves the fastest calibation time and one of the best frequency accuracies after calibration, thus easily meeting the calibration time and frequency variation requirements for the system clock in the EPC C1G2 UHF RFID protocol.

Chapter 5

Conclusions and Future Work

5.1 Summary

This thesis contributed to the area of remote frequency calibration of passive wireless microsystems. The focus of the design was on minimizing the power consumption of the system clock of passive wireless microsystems, while achieving a fast calibration time, a high frequency accuracy of the the system clock for a passive transponder, and being able to operate at low supply voltages. The design proposed in this thesis is summarized as follows.

A remote frequency calibration technique that allows a passive wireless mircrosystem to tune the frequency of its local oscillator to a required frequency using a low power frequency-locked-loop (FLL) has been proposed. A new integrating frequency difference detector (iFDD) that uses a switched-capacitor network with two integrating paths and a single current source to minimize mismatch between the two arms, consequently reducing mismatch-induced frequency error. The iFDD integrates the frequency error between a reference signal provided by the reader and the local oscillator of the passive wireless microsystem, thereby yielding zero steady-state frequency error. The power consumption of the proposed FLL is effectively reduced by operating the frequency detector and the local oscillator in subthreshold. A detailed analysis of the time-domain and frequency-domain behaviour of the iFDD was presented, as well as an investigation of the loop dynamics of the FLL. The theoretical conclusions of the proposed FLL were assessed using simulation results obtained from Spectre APS in CDS. The proposed FLL operated at a supply voltage of 0.5 V and achieved a low power consumption of 1.27 μW, while achieving a calibration time of 13.53 μs,

a lock range of 1.2 MHz, thus easily covering the ±20% variation in the center frequency of the local oscillator due to PVT effects, and a frequency variation of <0.01% in the lock state. The FLL was also found to be robust againt PVT variations. Since the proposed FLL could operate at a supply voltage of 0.5 V, while also achieving low power consumption, then it is capable of being implemented in PWMs with large reader-to-transponder distances. The proposed frequency calibration technique also achieved the fastest calibation times and best frequency accuracy in comparison to the works in [13, 15, 16, 17, 18, 19]. Therefore, our proposed frequency calibration technique improved on the calibation time and the frequency accuracy of the system clock of PWMs.

5.2 Future Work

The design introduced in this thesis was aimed at further advancing the creation of low power passive wireless microsystems that can operate at large reading distances, while achieving very fast calibration times and very high frequency accuracy. The direction of future work in this area will be toward the development of smaller passive wireless microsystems that can achieve ultra-low power consumption and larger reading distances, while still being able to provide all of the necessary sensor measurements, storage, and signal processing required of them regardless of their surrounding environment. This is especially true with the concurrent developement of the internet-of-things (IoT). One of the most significant barriers to the deployment of UHF RFID transponders in IoT and other areas that have dense reader environments, is the requirement of an ultra-low power system clock with very fine frequency resolution and fast calibration time.

The remote frequency calibration technique presented in this thesis can be implemented as a fundamental unit in a passive wireless microsystem that operates at a large reader-to-transponder distance with ultra-low power, but still requires a system clock that has excellent frequency accuracy, can be calibrated quickly, and is robust against variations in the supply voltage and temperature of the PWM that result from changes in its surrounding environment, which will be critical for RFID systems that are to be used in applications such as supply-chain management, environmental monitoring, and certain areas in healthcare.

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