A 100 MHz - 1 GHz ON-CHIP-PROGRAMMABLE PHASE-LOCKED-LOOP

by

Haleh Vahedi
BSc. Isfahan University of Technology, Isfahan, Iran, 1985

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I would like to dedicate this thesis to my mother

Jaleh Vahedi

whose unlimited love, caring, and compassion never left me alone.

Abstract

A 100 MHz - 1 GHz On-Chip- Programmable Phase-Locked-Loop
Master of Applied Science, 2004
Haleh Vahedi
The Department Electrical and Computer Engineering
Ryerson University

A programmable wide-range PLL has been designed that can provide 100-MHz to 1-GHz rail-to-rail digital clock signal from a 50-MHz reference clock. The architecture is appropriate for low-power design and is also power-efficient. The system is robust against temperature changes so that the stability of the system is guaranteed. Because of the differential configuration of the sub-blocks and using a voltage-controlled oscillator with a low gain and a linear transfer function the system has an acceptable noise rejection.

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Chapter1

Introduction

Microelectronics advances has led to numerous circuits in a single chip working at high clock frequency to provide different capabilities, such as computation and communication. The demand for high performance and low costs in electronic systems dictated the use of on-chip phase locked loops (PLLs) and clock recovery circuits (CRC). Advances of integrated –circuit (IC) technologies in terms of speed and complexity made this dream possible. These blocks find wide application in areas such as communication, wireless systems, and digital circuits and disk drive electronics [1].

Research on the topic goes back to as early as 1919 [24]. Vincent [24] and Appelton [25] experimentally researched and analyzed, respectively, the practical synchronization of oscillators. After these initial papers, research and development continued up until 1940s.

In 1935, Travis published a paper entitled "Automatic Frequency Control", [26] which suggested two reasons for controlling the local oscillator of a receiver. "Oscillator drift, if not corrected by more or less frequency manual readjustment, is capable of mistuning the signal by many channels in the course of a few hours run"[23, p.1].. His second reason for oscillator control is more interesting: " it seems to be quite true that the average listener does not tune his set well enough to obtain the best quality it is capable of giving, partly from negligence, and partly from lack of the necessary skill, in which case the mechanical design of the set is a possible contributing factor" [23, p.2].

In 1939, Vincent Rideout described a servo-mechanical automatic frequency control circuit [27]. At this time the DC stability of amplifiers was poor, and maintaining a constant control voltage was difficult.

About 1953, phase-locked loop designers began studying the nonlinear operation of the circuits. Color television would not have been possible without the advancement of phase-locked loop technology [23].

In the early 1950s, a "good" phase-locked loop would adjust the television's color within a second. A "fair" phase-locked loop would adjust the color within 10 seconds. The phase-locked loop in the color sub-carrier circuit was originally to replace a phase-control "knob" that the consumer would adjust manually as a new station was tuned [23].

By 1959, analog phase-locked loop theory and design was approaching maturity. The wider applicability of the phase-locked loops resulted from the acceptance of the PLL as a low pass filter for FM inputs and a high-pass filter to the output oscillator. McAleer [18] wrote that there were three uses for phase-locked loops: 1) in a receiver to increase the power level and attenuate the noise of a weak FM signal, 2) can be used to reduce the jitter or frequency noise of a high-powered oscillator, 3) as a narrow band-width filter [23].

While the concept of phase locking has been in use for more than half a century, monolithic implementation of PLLs and CRCs has become possible only in the last twenty-five years, and popular in the last fifteen years [1].

1.1 Applications

PLLs are used for jitter reduction, skew suppression, frequency synthesis and clock recovery. In the following, a brief explanation will be provided for each of these functions.

1.1.1 Jitter Reduction

Any variation in the period of a periodic signal is called jitter. Signals often experience timing jitter as they travel through a communication channel or as they are retrieved from a storage medium. This type of corruption cannot be removed by amplification and clipping even if the signal is binary. A PLL can be used to reduce the jitter. Timing jitter is shown in Fig. 1.1[1].

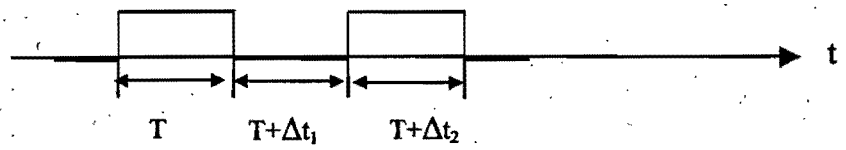

Fig. 1.1 Timing jitter.

1.1.2 Skew Suppression

Skew suppression is a critical problem in high-speed digital systems. Fig. 1.2 shows this problem. In these circuits a clock, CLK_{ref}, enters a chip from outside and is buffered (in several stages) to sharpen its edges in order to drive the capacitance load with minimal delay. The problem is that the on-chip clock, CLK_{in}, typically drives several nano-farads of capacitive loads, exhibiting significant delay with respect to the reference clock. The resulting skew reduces the timing budget for on-chip and inter-chip operation [1].

In order to reduce the skew, CLK_{ref} and CLK_{in} could be aligned through a PLL.

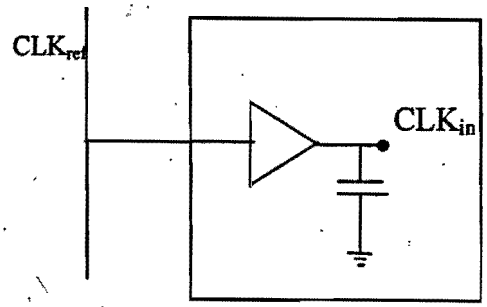

Fig. 1.2 Clock skew in a digital system.

1.1.3 Frequency Synthesis

In many systems we need frequency multiplication of periodic signals. For example, sometimes the bandwidth limitation of PC (printed circuits) boards constrains the reference clock, that is CLK_{ref} , while the on-chip clock frequency may need to be much higher. Frequency multiplication can be implemented by PLLs [1].

1.1.4 Clock Recovery

It is a common practice in communication systems to embed clock information into the transmitted data signal to make data transfer more efficient and economical. Therefore, at the receiver end there must be a means for recovering the timing information and synchronizing the data with the incoming data. Most clock recovery circuits employ phase locking [1].

In addition, increased integration and clock rates in systems-on-a-chip (SOC) create a demand for special management of clock distribution networks, primarily based on phase-locked loops. With the addition of clock dividers and in-circuit programmability, clock managers are capable of performing functions beyond simple clock skew reduction or static clock multiplication.

In many cases, managers for clock distribution networks are capable of adjusting phase and duty cycle, synchronizing several components in a system, reducing skew

and synthesizing variable frequencies. These qualities are favorable when several independent elements are integrated into a system-on-a-chip. An SOC can incorporate a microprocessor, a system bus, compact flash interface, a universal serial bus host controller, serial data ports, and digital to analog converters. Each element operates independently, thus creating a demand for a wide range of clock rates. With the advancement of multi-speed microprocessors and higher operating frequencies, this operating range expands [8].

Also, programmability offers a dimension to clock managers that expands its applications to areas such as power management. By making clock frequency a function of the demand on the system, the direct relationship between power and frequency can be exploited to reduce the power consumption [8].

As PLL will continue to be one of the main blocks of many chips, the purpose of this study is to build a general-purpose wide-range (for order of ten, that is 100MHz to 1GHz) programmable PLL which can be used in both analog and digital chips. It benefits from a voltage-controlled oscillator (VCO) with a low gain and linear operation. The architecture is power efficient and suitable for low power design. It is robust against temperature changes and has good noise rejection.

Many outstanding PLLs have been designed to date. Some of them have used GaAs and bipolar transistor (BJT) technologies. However, sub-micron CMOS technology is now dominant in design of novel high-frequency PLLs. CMOS technology has the advantages of low cost, low power consumption, and the ability to integrate digital and analog circuits together on the same chip. For all these reasons CMOS technology has been used for this design.

1.2 Main Features Achieved in the Designed PLL

- One of the main issues in PLL design is noise, which comes from many different sources. They could be thermal and flicker noises of the devices or the noise induced through supply and ground of the system. Some of them, such as thermal and flicker noises are inevitable, however normally they are not dominant. The dominant one is the supply noise, which could be severe in a PLL because of the mixed mode nature of the design (i.e. both digital and analog blocks are used in this system). Some of the blocks that work with switching logic could induce switching noise on the supply.

As the differential architecture has common-mode noise rejection feature, differential architecture has been used for all sub-blocks of the PLL. Also, by separating the supply of the sensitive blocks from the supply of the switching blocks, attempt is done to minimize the effect of supply noise on sensitive blocks. In addition, in the method used for programmability, the required wide frequency range (that is order of ten) is partitioned into several smaller ranges so that, as it will be shown later, the system is less prone to noise and also it is appropriate for low-power design.

- The high-performance of the proposed PLL is because of a new architecture proposed for one of its main block, that is VCO (voltage controlled oscillator). As it will be shown later, the proposed architecture uses fast switching in order to reduce noise. Also, it has low gain, which helps better noise rejection. The transfer function is linear and robust against temperature changes and guaranties the stability of the system.
- Also, the reliable performance of proposed PLL is due to a method used for fixing the common-mode problem of another sub-block of the PLL: charge-pump.

With this feature, when the system is locked, there won't be any undesired deviation of this condition.

- In the method used for programmability an extra feature is added to the system: in smaller partitioned ranges twenty percent overlap has been considered between two successive ranges in order to make the system even more robust against temperature change.
- The design is suitable for system level programmability. This is achieved with a VCO capable of shifting operating ranges by automatically changing the driving capability. This adds a coarse control feature to the VCO architecture, which has also the fine control feature of a conventional VCO.
- The method used for programmability is power efficient and all sub-blocks are suitable for low power design.
- The method is also expandable and the range could be even wider. Also the range could be shifted to the upper part of the frequency range or the lower part of the frequency range with changing the driving capabilities
- The proposed PLL produces a rail-to-rail clock output, which makes it appropriate as a general-purpose PLL that could be used in all applications. Also, six clocks with different phases are brought as outputs in order to be used in data-clock recovery circuits.
- As our goal is to build a PLL that could be accompanied with both digital and analog process technologies, all capacitors required are built with transistors and no MIM (metal-insulation-metal) capacitor is used in this design.
- As a general-purpose PLL, buffers are considered at the output to sharpen the PLL outputs. In this case PLL could drive higher output capacitive load and can be used for skew reduction.

- The proposed PLL is a programmable wide-range PLL that can be provided 100-MHz to 1-GHz rail-to-rail digital clock signal from a 50-MHz reference clock. The architecture is appropriate for low-power design and it is also power efficient. The system is robust against temperature changes so that the stability of the system is guaranteed. Because of the differential configuration of the sub-blocks and using a voltage- controlled oscillator with a low gain and linear transfer function the system has a good noise rejection.

1.3 Outline of the Thesis

In the Chapter 2 the basic concepts of the PLL will be discussed, linear models are introduced for basic PLL and Charge-pump PLL and the advantages of charge-pump PLL are described. Also, the closed –loop transfer function of the basic PLL and the charge-pump PLL will be covered in Chapter 2.

Chapter 3 is a literature review on PLL design. This chapter shows advantages of the previous works and improvements achieved in the proposed design.

In Chapter 4 the top level design of the system is introduced. Next, the circuit design of sub-blocks is introduced at transistor level and discussed in-detail. After getting familiar with the whole blocks, the transfer function of the proposed PLL is derived.

Chapter 5 is dedicated to the simulation results and the procedures used for calculating the required results. Layout challenges and sizes of different blocks in the layout are also discussed.

Finally, Chapter 6 deals with conclusions and suggestions for the future works.

Chapter 2

Basic Concepts of PLL

2.1 Introduction

A phase-locked loop (PLL) is basically an oscillator whose frequency is locked onto some frequency component of an input signal. It is a feedback system that operates on the excess phase of nominally periodic signals. The basic architecture of a PLL is shown in Fig. 2.1[1]. It consists of a phase detector (PD), a low-pass filter (LPF), and a voltage-controlled oscillator (VCO). Phase detector is a circuit that shows the phase difference between two input signals and produces a voltage based on this phase difference; i.e. the output of PD is linearly proportional to the phase difference. The low-pass filter smoothes the output pulses of the phase detector and the resulting DC component is the input for voltage-controlled oscillator. Finally, VCO is an oscillator whose output frequency is a function of a control input, usually a voltage.

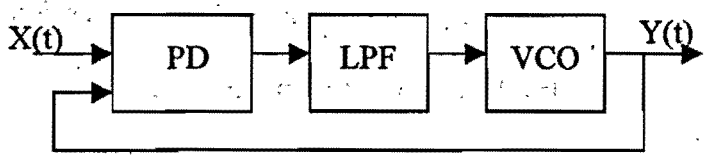

Fig. 2.1 Basic architecture of PLL.

2.2 System Operation

Phase detector (PD) has an output voltage with an average value proportional to the phase difference between the input signal and the output of the VCO. The low-pass filter removes high-frequency components in the PD output and is used to extract the average value from the output of the PD. This average value is used to drive the VCO.

The negative feedback of the loop results in the output of the VCO being synchronized with the input signal.

It should be mentioned that PLL is a dynamic system, i.e., its response depends on the past values of the input and output. Therefore, an understanding of the loop dynamics is necessary.

2.3 Terms and Definitions

It is timely to give a brief description of some of the terms which are vastly used hereafter in this work in order to clarify the concepts.

Phase Locking: The task of aligning the output phase of VCO with the phase of the reference input. When the loop is locked, $\varphi_{out} - \varphi_{in}$ (that is the difference between output and input phases) does not change with time. Therefore, $d\varphi_{out}/dt - d\varphi_{in}/dt$ is equal to zero which means $\omega_{in} - \omega_{out} = 0$.

Jitter: Any random variation in the period of a periodic signal.

Acquisition Time: The amount of time a PLL takes to converge with a certain phase error of the input signal.

Acquisition Range: The frequency range that PLL can acquire lock.

2.4 Loop Dynamics

Transient response of a phase-locked loop is nonlinear and cannot be easily formulated. However, a linear approximation can be used for gaining an intuition and understanding trade-offs in PLL design.

We can introduce the VCO characteristic as a linear function of the VCO frequency, ω_o, with respect to the control voltage, v_{cont}. The linear model is

$$\omega_o = \Delta\omega_o + \omega_i = K_{VCO}(v_{cont}) + \omega_i,$$

K_{VCO} is the VCO gain, ω_o and ω_I are output and input frequency respectively. In simple examples, K_{VCO} has a well-defined value because the VCO characteristic has

been linear. In practice, this is only an approximation at best. There is obviously a tradeoff between range and linearity [19]. By considering the last equation, the excess phase is

$$\varphi_{out}(t) = K_{VCO} \int v_{cont}\, dt.$$

So, the transfer function of the linear model of the VCO will be:

$$\varphi_{out}(s)/v_{cont}(s) = K_{VCO}/s.$$

The linear model for PD is

$$V_{cont} = (\omega_o - \omega_1)/K_{VCO} = K_{PD}.\theta_e.$$

where K_{PD} is the PD gain and θ_e is the phase error of the VCO output relative to the input signal. As V_{cont} is inversely proportional to K_{VCO} in order to minimize the phase error, $K_{PD}K_{VCO}$ should be maximized. Also, note that the phase error is a function of output frequency [2].

Fig. 2.2 [2] shows a linear model of the PLL with the transfer function of each block. The goal is to derive the overall transfer function for the phase, $\phi_{out}(s)/\phi_{in}(s)$. The PD is represented by a subtractor whose output is amplified by K_{PD}. The low-pass filter transfer function is considered as $V_{out}(s)/V_{in}(s) = 1/(1+s/\omega_{LPF})$, because if V_{in} varies rapidly, V_{out} cannot fully track the input variations. Note that ω_{LPF} denotes the 3-dB bandwidth. Therefore, the open-loop transfer function of the PLL is

$$H(s)/_{open} = \phi_{out}(s)/\phi_{in}(s),$$

$$H(s)/_{open} = K_{PD}.1/(1+s/\omega_{LPF}).(K_{VCO}/s). \qquad (2.1)$$

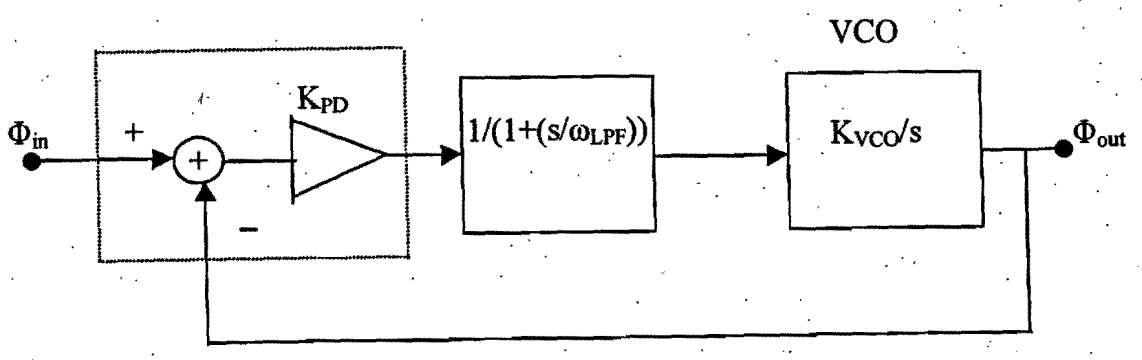

Fig. 2.2 Linear model of basic PLL.

Equation (2.1) shows that the system is of second order, with one pole contributed by the VCO and another by the LPF. The closed loop transfer function can be written as

$$H(s)/_{closed} = (K_{PD}.K_{VCO})/(s^2/\omega_{LPF} + s + K_{PD}.K_{VCO}). \tag{2.2}$$

The frequency of a waveform is the time derivative of the phase: $\omega = d\phi/dt$. Since the frequency and the phase are related by a linear operator, the above transfer function also applies to the input and output frequencies,

$$\omega_{out}(s)/\omega_{in}(s) = (K_{PD}.K_{VCO})/(s^2/\omega_{LPF} + s + K_{PD}.K_{VCO}).$$

The familiar form of the second order system in control theory is

$$H(s) = \omega_n^2/(s^2 + 2\xi\omega_n s + \omega_n^2). \tag{2.3}$$

If, the transfer function is compared with this familiar form used in control theory, ξ, the "damping ratio" and ω_n, the natural frequency, are

$$\omega_n = \sqrt{\omega_{LPF}.K_{PD}.K_{VCO}}, \tag{2.4}$$

$$\xi = 1/2\sqrt{\omega_{LPF}/(K_{PD}.K_{VCO})}.$$

(2.5)

The two poles of the system are

$$s_{1,2} = -\xi\omega_n \pm \sqrt{(\xi^2 - 1)\omega_n^2},$$

$$s_{1,2} = (-\xi \pm \sqrt{\xi^2 - 1})\omega_n.$$

Thus, if $\zeta > 1$, both poles are real. The system is over-damped and the transient response contains two exponentials with time constants $1/S_1$ and $1/S_2$. On the other hand, if $\zeta < 1$, the poles are complex and the response to a unit step input $\omega_{in} = \Delta\omega\, u(t)$ is equal to:

$$\omega_{out}(t) = \{1 - e^{-\xi\omega_n t}[\cos(\omega_n\sqrt{1-\xi^2}t) + (\xi/\sqrt{1-\xi^2})\sin(\omega_n\sqrt{1-\xi^2}t)]\}\Delta\omega u(t),$$

$$\omega_{out}(t) = [1 - (1/\sqrt{1-\xi^2})e^{-\xi\omega_n t}\sin(\omega_n\sqrt{1-\xi^2}t + \theta)]\Delta\omega u(t),$$

where ω_{out} denotes the change in the output frequency and $\theta = \sin^{-1}\sqrt{1-\xi^2}$. Thus, the step response contains a sinusoidal component that decays with a time constant $(\zeta\ \omega_n)^{-1}$, which determines the settling speed of PLL. The system exhibits the same response if a phase step is applied to the input and the output phase is observed.

The settling speed of PLL is important and should be maximized.

This result reveals a critical trade-off between the settling speed and the ripple on the VCO control line: when we decrease ω_{LPF} in order to have better suppression of the high-frequency components produced by the PD, the settling time constant (which determines the acquisition time) will be longer.

The value of ζ is also important. For a stable second-order system ζ should be greater than 0.5, preferably $\sqrt{2}/2$ or even 1 to avoid excessive ringing. With these limitations we will have more trade-offs. Eq. (2.5) shows that as ω_{LPF} is reduced to

minimize the ripple of the control voltage, the stability degrades. Also, as mentioned earlier phase error is inversely proportional to $K_{VCO}K_{PD}$. Since ζ is inversely proportional to $K_{VCO}K_{PD}$, lowering the phase error makes the system less stable. Moreover, this type of the PLL has another drawback, namely a limited acquisition range. The acquisition range is on the order of ω_{LPF}; that is, the loop locks only if the difference between ω_{in} and ω_{out} is less than roughly ω_{LPF}. So if ω_{LPF} is reduced in order to suppress the ripple on the control voltage, the acquisition range will be decreased [2]. These problems encourage designers to use phase-frequency detector accompanied with a charge-pump PLL.

2.5 Phase-Frequency Detector and Charge-Pump PLL

For resolving acquisition problem, in new designs of PLLs designers use a phase-frequency detector (PFD): a circuit that can detect both frequency and phase differences. Three-state PFD, with one realization suggested by Shahriary *et. al.* [18] is widely used by designers, because it is simple and has a linear range of $\pm 2\pi$ radians. The conceptual operation of this PFD is shown in Fig. 2.3. The circuit creates three states and responds to the rising (or falling) edges of the two inputs. If initially $Q_A = Q_B = 0$, then a rising transition on A leads to $Q_A = 1$ and Q_B remains zero. This state will remain until the rising edge of B appears. At this point both Q_A and Q_B return to Zero.

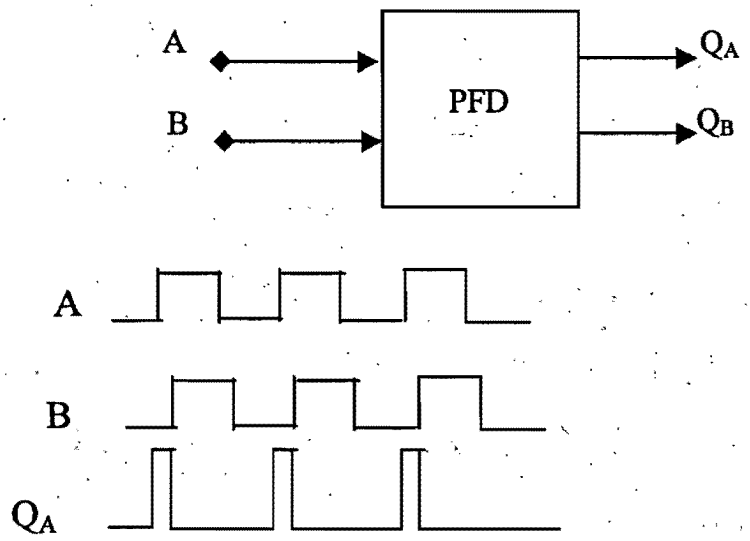

Fig. 2.3 Conceptual operation of PFD.

Fig. 2.4 shows a basic implementation for PFD. The inputs, A and B, are the clocks of the Flip-Flops. If Q_A=Q_B=0 and A goes high, Q_A rises. This state is remained until the rising transition on B appears. At this moment Q_B goes high and the AND gate resets both Flip-Flops.

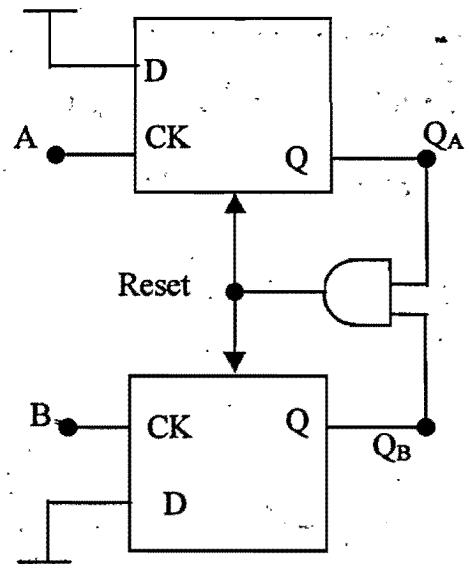

Fig. 2.4 Basic implementation of PFD.

For using the PFD in a phase-locked loop, normally a "charge-pump" is inserted between the PFD and the loop filter. Charge-pump consists of two switched current sources which source or sink charge into or out of the loop filter according to the two outputs of the PFD.

Fig.2.5 shows a charge-pump which is driven by a PFD and drives a capacitor. If Q_A=Q_B=0, then the switches are off and the output remains constant. If Q_A is high and Q_B is low, I_1 charges C_P and the output will increase. If Q_A is low and Q_B is high, then I_2 discharges C_P and the output will decrease.

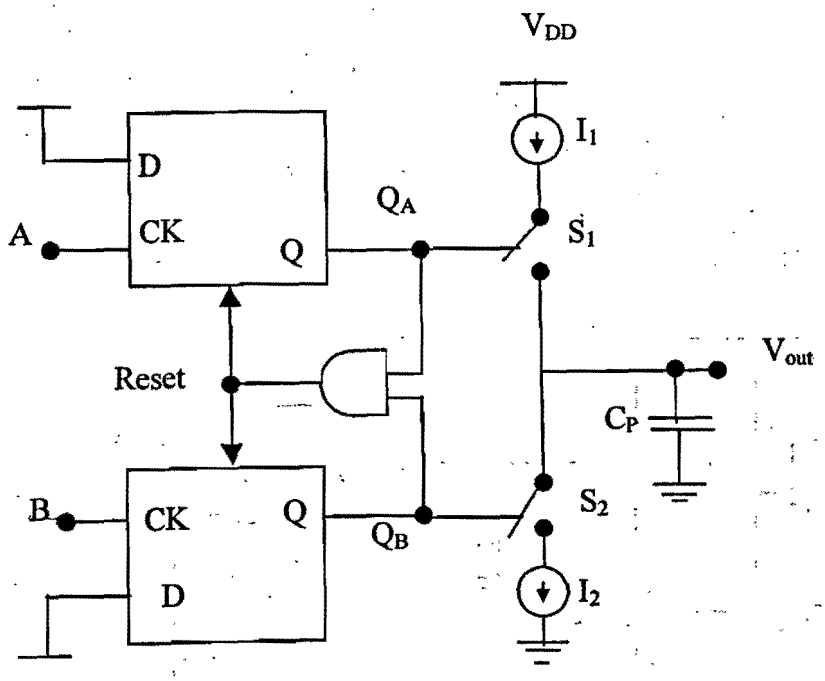

Fig. 2.5 PFD with charge-pump.

This circuit has an interesting property. For example, if A leads B by a finite amount, then Q_A produces pulses indefinitely, allowing the charge pump to inject I_1 into C_P and forcing V_{out} to rise steadily. In other words, for a finite input error the output eventually goes to $+\infty$ or $-\infty$. It means the gain of the circuit is infinity.

Fig. 2.6 shows a basic charge-pump PLL. When the loop is activated, ω_{out} may be far from ω_{in}. The PFD and the charge-pump change the control voltage such that ω_{out} approaches ω_{in}. When the input and the output frequencies are sufficiently close, the PFD acts as a phase detector. The loop locks when the phase error is zero and in this case the charge pump doesn't work any more.

As observed here, the gain of the PFD/CP combination is infinite. On the other hand when the loop is locked V_{out} is finite, and the input phase error should be zero. This is in contrast to basic PLL in which the phase error is a function of the output frequency.

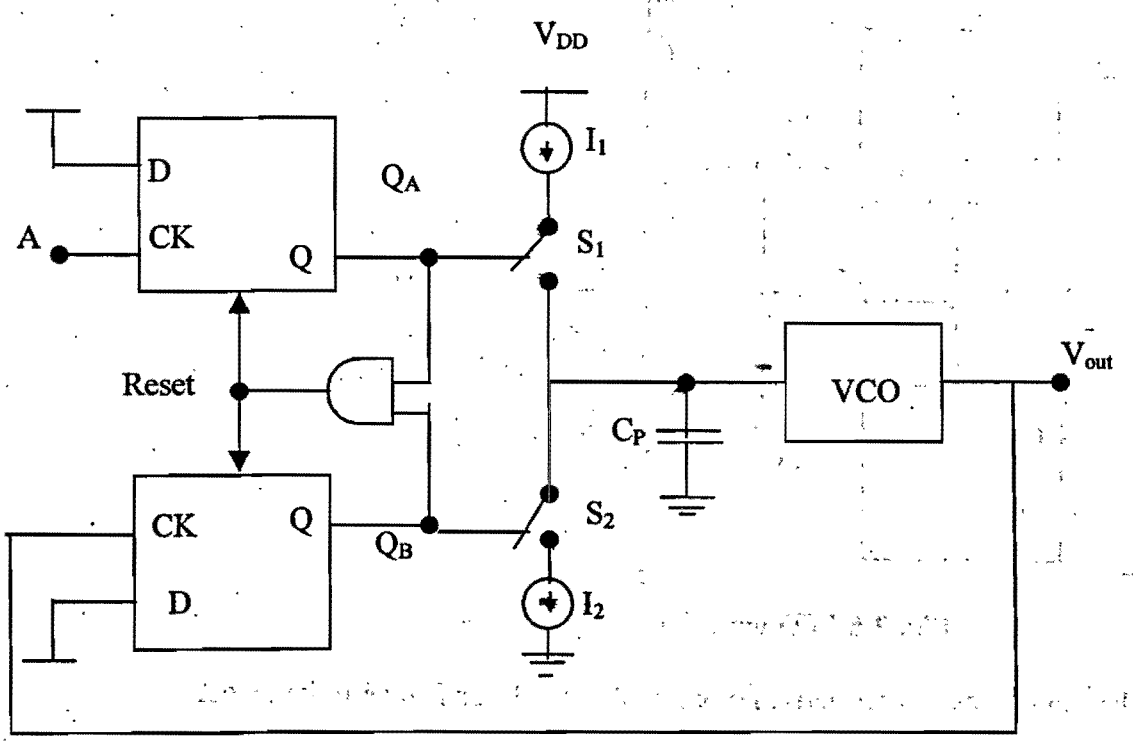

Fig. 2.6 Basic charge pump PLL

2.6 Dynamics of the Charge-Pump PLL

For deriving the dynamics of charge-pump PLL a linear model should be derived for the PFD, the charge pump and the low pass filter. In fact, the combination of PFD/CP/LPF is not a linear system. Actually, the output of this combination is discrete because while the $Q_A = Q_B = 0$, the output is constant and increases or decrease if there is any phase difference. However, the output waveform is approximated by a ramp, a linear relationship between V_{out} and $\Delta\phi$. In a sense, our discrete-time system is approximated by a continuous-time model.

For deriving the transfer function of this combination, a phase difference impulse is applied and V_{out} is calculated. As a phase-difference impulse is difficult to visualize, a phase difference step is applied, V_{out} is obtained and the result is differentiated with respect to time. Fig. 2.7 shows a step response of PFD/CP/LPF combination.

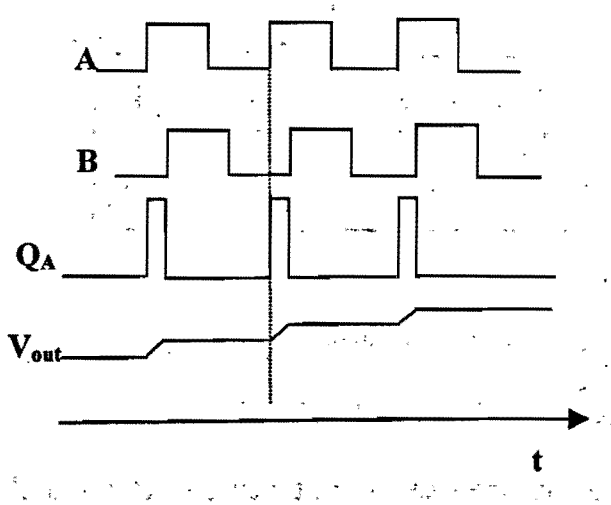

Fig. 2.7 Step response of PFD/CP/LPF combination [2].

Q_A continues to produce pulses that are $\phi_0 T_{in}/2\pi$ seconds wide, raising the output voltage by $(I_P/C_P)(\phi_0 T_{in}/2\pi)$ in every period. Approximated by a ramp, V_{OUT} exhibits a slope of $(I_P/C_P)(\phi_0/2\pi)$ and can be expressed as

$$V_{out}(t) = (I_P/(2\pi.C_P)).t.\phi_0 u(t).$$

The impulse response is therefore given by

$$h(t) = (I_P/2\pi.C_P)u(t).$$

Therefore, the transfer function will be

$$V_{out}/\Delta\phi(s) = (I_P/2\pi.C_P).(1/s).$$

Now we construct a linear model of charge-pump PLL. This linear model is shown in the Fig. 2.8. The open-loop transfer function of the model is

$$\Phi_{out}(s)/\Phi_{in}(s)|_{open} = (I_p/(2\pi C_p))(K_{VCO}/s^2).$$

This loop gain has two poles at the origin. The closed-loop transfer function, H(s) is

$$H(s) = (I_P K_{VCO})/(2\pi C_p)/(s^2 + (I_P K_{VCO})/(2\pi C_p))).$$

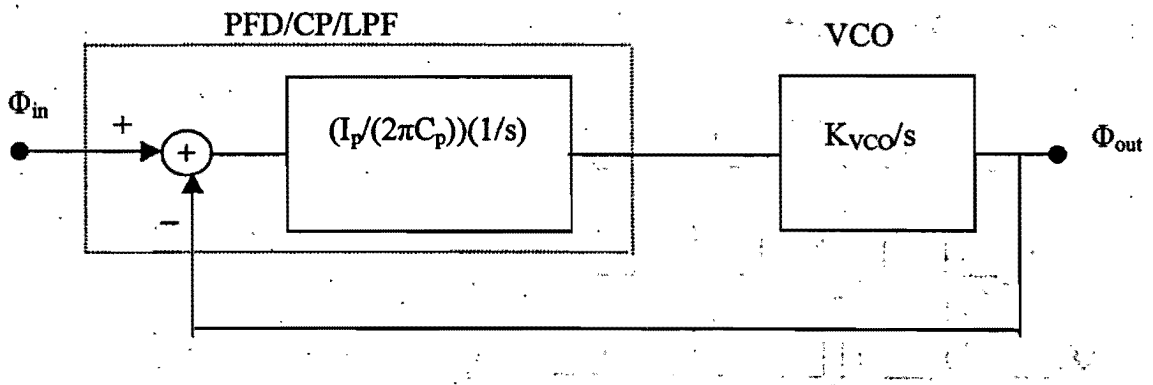

Fig.2.8 Linear model of basic charge-pump PLL.

This result shows the system is not stable because the closed-loop system contains two imaginary poles. In order to stabilize the system, the transfer function should be modified. That is, a zero should be added in the loop gain to keep the phase margin in the safe range for stability. This will be realized by adding a resistor in series with the loop filter capacitor (Fig. 2.9). It can be shown [2] that the PFD/CP/LPF transfer function is

$$V_{out}(s)/\Delta\phi(s) = (I_P/2\pi)(R_P + (1/(C_P.s))).$$

The PLL open-loop transfer function is

$$\phi_{out}(s)/\phi_{in}(s)|_{open} = (I_P/2\pi).(R_P + 1/(C_P s)).(K_{VCO}/s),$$

and

$$H(s) = (I_P.K_{VCO}/(2\pi.C_P))(R_P.C_P.s+1)/(s^2 + (I_P/2\pi).K_{VCO}.R_P.s + (I_P/(2\pi C_P)).K_{VCO})$$

If this transfer function is compared with the familiar form of second order system, transfer function shown in Eq. (2.3), the natural frequency and the damping factor are respectively

$$\omega_n = \sqrt{(I_P.K_{VCO})/(2\pi.C_P)},$$

$$\xi = (R_P/2)\sqrt{(I_P.C_P.K_{VCO})/2\pi}.$$

This architecture has a drawback: since the charge-pump drives a capacitor and a resistor in series, each time a current is injected into the loop filter the control voltage experiences a large jump [2]. This may produce a ripple in controlling voltage. To fix this problem, a second capacitor is usually added in parallel with R_P and C_P to suppress the initial step. Fig. 2.9 shows this modified configuration. Now the loop filter is of second order. However, in order to keep the transfer function unchanged, the capacitance of the second capacitor is about one-fifth to one-tenth of C_P.

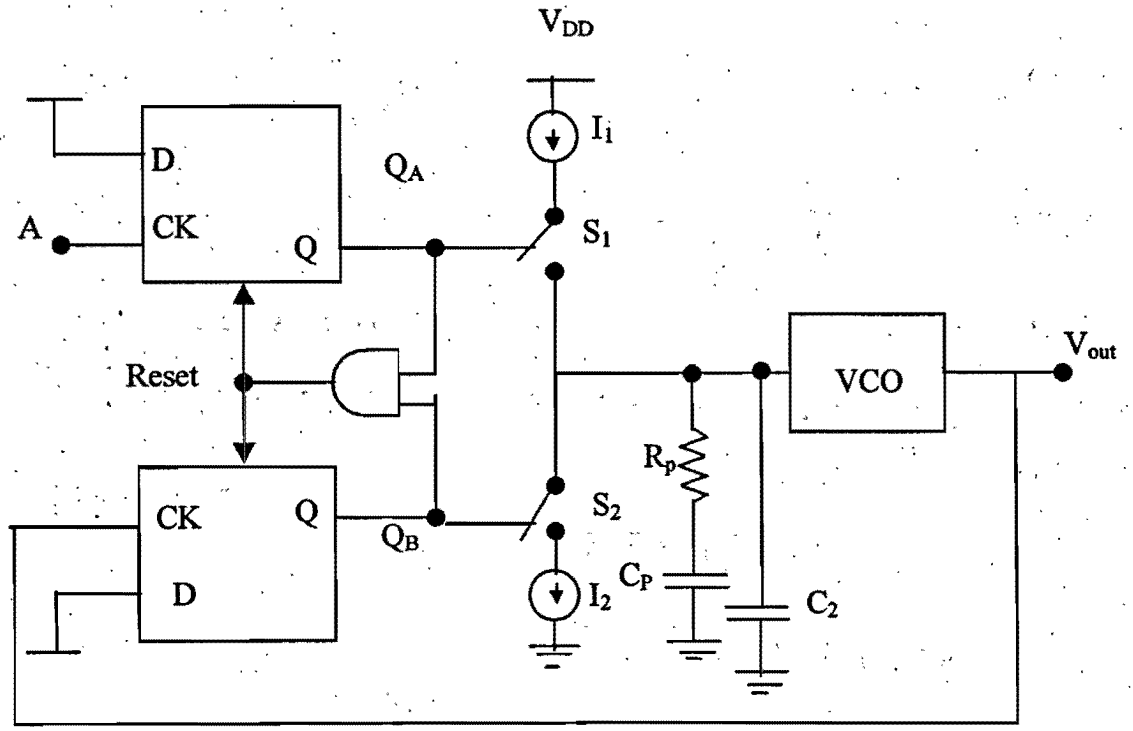

Fig. 2.9 The charge-pump PLL architecture used a resistor in series with C_p and the second capacitor.

By comparing the loop dynamics of basic PLLs (section 2.4) and charge-pump PLLs, it is clear that interrelated attributes such as noise suppression, acquisition time, phase error and stability, as well as limited acquisition range are disadvantages of the basic PLL over the charge-pump PLL and this justifies our choice of charge-pump type for the proposed PLL.

Chapter 3

Literature Review

3.0 A Summary of Previous Works

The result of an investigation in the recent works on wide-range and/or programmable PLL has been summarized in the Table 3.1 and shows the various features of the major works.

Author	Programming style	On-chip Program mability	VCO Frequency range	VCO gain	VCO transfer function	Power dissipation	Supply V	Process um	Chip Area (mm^2)
Rhee[5] (VCO only)	Programming loading capacitors	No	54M-1G	430M/V worst case(Diagr am)	Linear ,but variable	3.5mW (VCO only)	2.5	0.35	-------
Sutoh[10]	Programming NO. of inverter stages	yes	5M-400M	-------	nonlinear	13.7mW	2	0.25	0.14
Sung[4]	Using circuitry	Yes	75M-1G	430M/V	Linear and constant	92mW	3.3	0.6	1.05
Chen[20]	Programming driving capabilities	No	103M-1.02G	271M/V	nonlinear	4.52mW	1.8	0.35	0.16
Brynjolfs -on[8]	Programming number of inverters	yes	1.5M-1.8G	370 M/V(worst case - diagram)	Linear, but variable	8.9mw @330M	1.8	0.18	-------
Joe-shin Lee[9]	Using circuitry	yes	150M-740M	460M/V (diagram)	linear	53mW	2.5	0.25	-------

Table 3.1 Features of main works on wide-range and /or programmable PLLs.

3.1 Different Methods for Getting Wider Range

Looking at the system-level design, the first major question is how to reach a wide range PLL. Normally, in getting a wide-range frequency output in the PLL the bottleneck is VCO. Therefore, the main block to be considered is VCO (voltage controlled oscillator).

Ring oscillators are the most popular architecture used for wide-range and/or programmable PLL's [1,5,6]. However, as observed later, the range of frequency that a ring oscillator could cover is at most of order of two to three. This range is hardly enough for temperature and process change coverage. So, the first issue in the system-level design is how to increase the frequency range of the VCO.

Researchers have tried to increase the frequency range of an oscillator by increasing the linearity of the VCO transfer function [4,9], programming the driving capabilities [3], programming loading capacitors in a relaxation oscillator [5], or number of inverter stages for changing the delays [8, 10].

Sung *et. al.* [4] and Joe Shin Lee *et. al.* [9] tried to reach to a wide-range PLL. They tried to make the transfer function of the VCO linear and getting wider frequency range by adding some circuitry. However, since the wide-range frequency should be achieved within a voltage range that supply voltage permits (i.e. maximum swing between ground and supply), the resulting VCO gain is high and the system is susceptible to noise and hence the jitter performance is not good. Also, the design is not appropriate for low supply voltage.

Rhee [5] tried to reach to a wide range VCO by programming floating capacitor in a relaxation VCO. He reached a linear transfer function for VCO. However, this design also suffers from high VCO gain problem and it is susceptible to noise leading to a

worse jitter performance. Also, in this method a good area of the chip will be occupied by the capacitors.

Although these two methods could increase the output frequency range of the VCO and achieve linear transfer function for the VCO, the gain of the VCO should be large. Large VCO gain makes the VCO sensitive to noise, therefore the jitter performance will not be acceptable.

In the designs proposed by Sutoh *et. al.* [6] and Brynjolfson *et. al* [8], the programmable wide frequency range of the VCO is achieved by changing the number of inverters. Therefore, the total delay of all inverter stages, which determines the output frequency of the VCO, will change. In this case, the larger the number of inverter stages utilized, implies_the smaller output frequency of VCO. Therefore, more hardware is required for wider range.

Brinjolfson et al [8] have suggested a logic circuit for on-chip programmability and they tried to use the linear part of the VCO transfer function. However, their diagram shows that the VCO gain is not constant for different ranges. In other words, for high frequencies, when one inverter or two inverters are used, the gain is high (about 370M/V) and there is a problem for achieving the required overlapping while for the lower ranges the VCO gain is low and there is too much overlapping.

Oscal *et al.* [20] also have tried to divide the wide frequency range into many small portions that are individually controlled by the control voltages. The proposed approach uses many parallel inverter chains that can be viewed as programming the driving capabilities of inverter chains. In this case, a fairly low hardware complexity is needed. In particular, the power consumption can be reduced when VCO operates at a low oscillation frequency. The proposed range-programmable VCO can be applied in low supply voltage applications with a power efficient operation.

However, in this paper there was no emphasis on linearity of VCO transfer function. Also, no logic has been considered for on-chip programmability. Therefore, the problems of on-chip programming of partitioning the wide range into smaller ranges have not been investigated. One of the problems is the temperature change effect. If the temperature changes the frequency of the system will also change. So, if the system works in upper or lower part of a particular range (determined with the number of chains), the system may leave that particular range due to temperature change and come back to that range again and this may happen frequently. So, the system is no longer stable. Overlapping of different ranges may fix the problem; however, for proper operation of the PLL, the VCO should withstand temperature changes.

These problems had to be in mind while designing a new PLL.

Table 3.2 summarizes the comparison between different methods for getting VCO with wide range frequency.

Method	Using circuitry For making the VCO transfer function linear and getting wider range	Programming loading capacitor	Programming the number of inverter stages	Programming driving capabilities
VCO gain	high	variable	variable	low
Suitable for low supply voltage	no	yes	yes	yes
Area	large	large	medium	medium
Power dissipation	large	medium	medium	Small/medium

Table 3.2 Comparison of the features of different methods for VCO with wide-range frequency.

3.2 Different Architectures for Delay Cell

VCO has the main role in jitter performance of the PLL and is the most power consuming circuit. Therefore, from the circuit design point of view, the most critical block in a PLL is the voltage-controlled oscillator (VCO). The following parameters are important in investigating VCO blocks performance:

1. Tuning range, that is the range between the minimum and maximum values of the VCO frequencies. Taking into account frequency changes due to process, temperature and supply variation, this range should cover the required frequency range.
2. Output amplitude over the range, which should not have large variation.
3. Supply and substrate noise rejection should be kept at acceptable levels. Since these blocks are normally built along with other digital circuit and share the same substrate, noise is always an important issue.
4. VCO gain variation, which is undesirable across the tuning range.
5. Power dissipation is also very important because VCO is most current starving block in the PLL.

In this survey the most common architectures were considered and the performance of each architecture was investigated by simulation. Finally, the performances of the simulated architectures are compared.

As mentioned before, ring-oscillator – type VCOs are widely used in PLLs, because they occupy a small chip area and could produce high-frequency signals with large amplitude suitable for digital systems. In the ring oscillator architecture a chain of N delay cells, with a total phase shift of 180 degrees, are placed in a feedback loop (Fig. 3.1). The simplest delay cell is an inverter block. As each inverter has approximately 90 degrees phase shift at its unity-gain frequency, if there are at least three inverters in

the loop, it is guaranteed that the loop gain will still be greater than unity when the phase shift around the loop becomes greater than 180 degrees. Therefore, the circuit is unstable and will oscillate. In each half period, the signal will propagate around the loop with an inversion. So if the delay of each inverter is shown with τ_{inv}, and we have n inverters, we can write [3]:

$$T/2 = n\tau_{inv}.$$

Therefore, we have

$$f_{osc} = 1/2n\tau_{inv},$$

where T is the period and f_{osc} is frequency of oscillation.

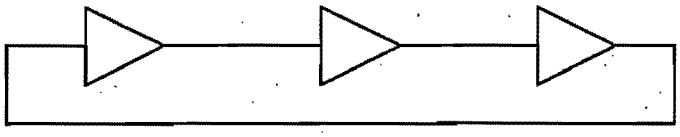

Fig. 3.1 Ring oscillator with least number of delay cells

Therefore, by changing the delay of the delay cell we can change the frequency of the oscillator. The delay could be controlled in two different ways: external and internal techniques

3.2.1 Architectures with the External Control

In the external control type, the control is done outside the delay cell. Therefore the delay cell could be a simple inverter and the control of the oscillator can be implemented by varying the capacitance or the resistance seen at the output node.

In capacitance tuning method, shown in Fig. 3.2a, a voltage-dependent capacitor (e.g. a reverse-biased p-n junction diode) loads the output node and its capacitance is adjusted by V_{cont}. The drawback of this circuit is that the minimum value of the capacitor still loads the circuit, limiting the maximum frequency of operation.

Another circuit used for capacitance tuning is shown in Fig. 3.2b. In this circuit the capacitor is constant, but a MOS device operates as a voltage–dependent resistor and thereby changes the effective capacitance seen at the output node.

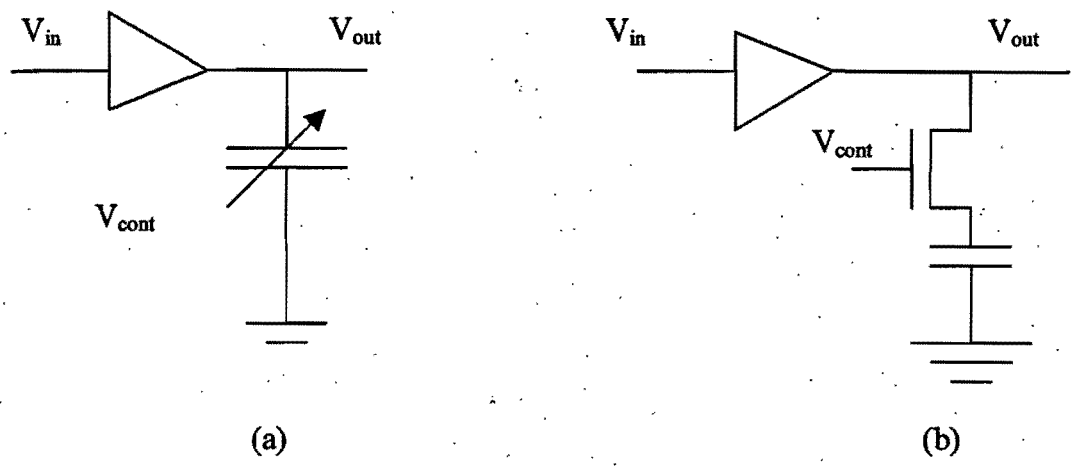

Fig. 3.2 Configurations with capacitance tuning load.

The second configuration was simulated. The schematic of the circuit is shown in Fig. 3.3. This delay cell is very fast and the output swing is rail to rail. However, as the transistor can't be kept in the triode region for a wide range, we don't have a linear resistor for a wide tuning range and the tuning range will be limited. Also, since the inverter is not immunized against supply voltage noise, some designers have tried to fix this problem by adding a regulator [17, 11,12]. But, since the regulator limits the headroom, this modification could not be a good choice when the supply voltage is low. This architecture is fast and has a rail to rail output swing, but the tuning range is limited and it has supply noise issue.

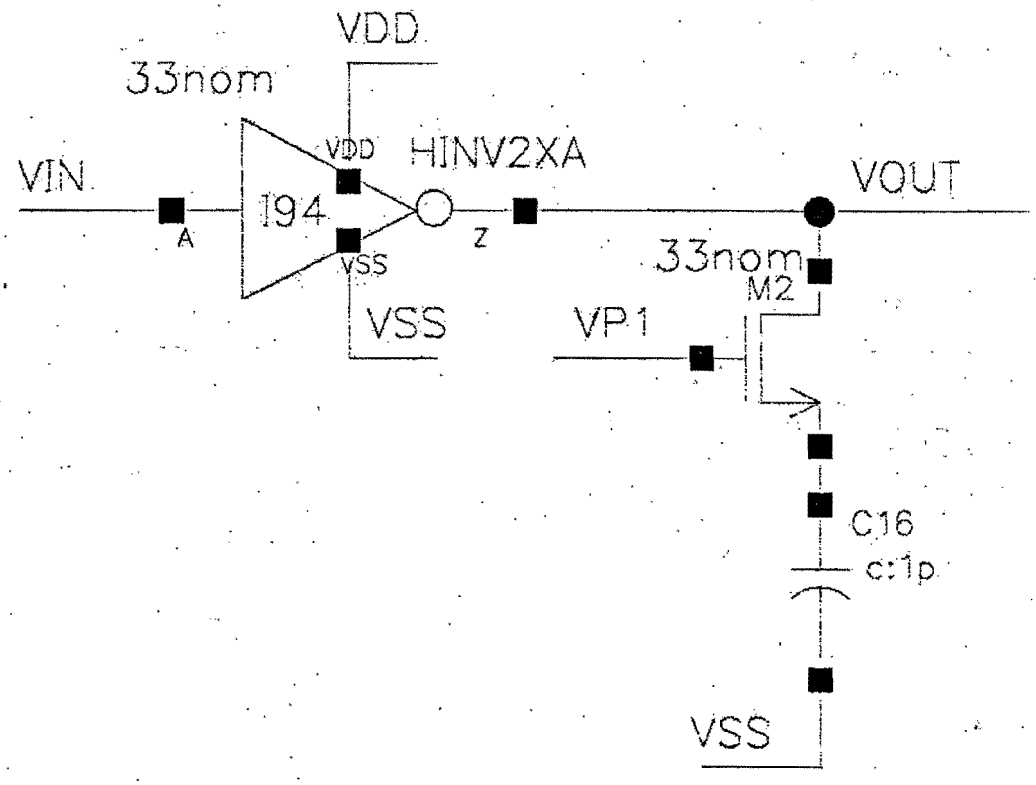

Fig. 3.3 External control.

3.2.2 Architectures with Internal Control

In this type of control, the control of the frequency takes place inside the delay cell. Although the architectures used with this type of control could be both single-ended and differential, as the differential architecture is immunized against supply noise we only discuss the differential configurations here. Consider the differential pair shown in Fig. 3.4.

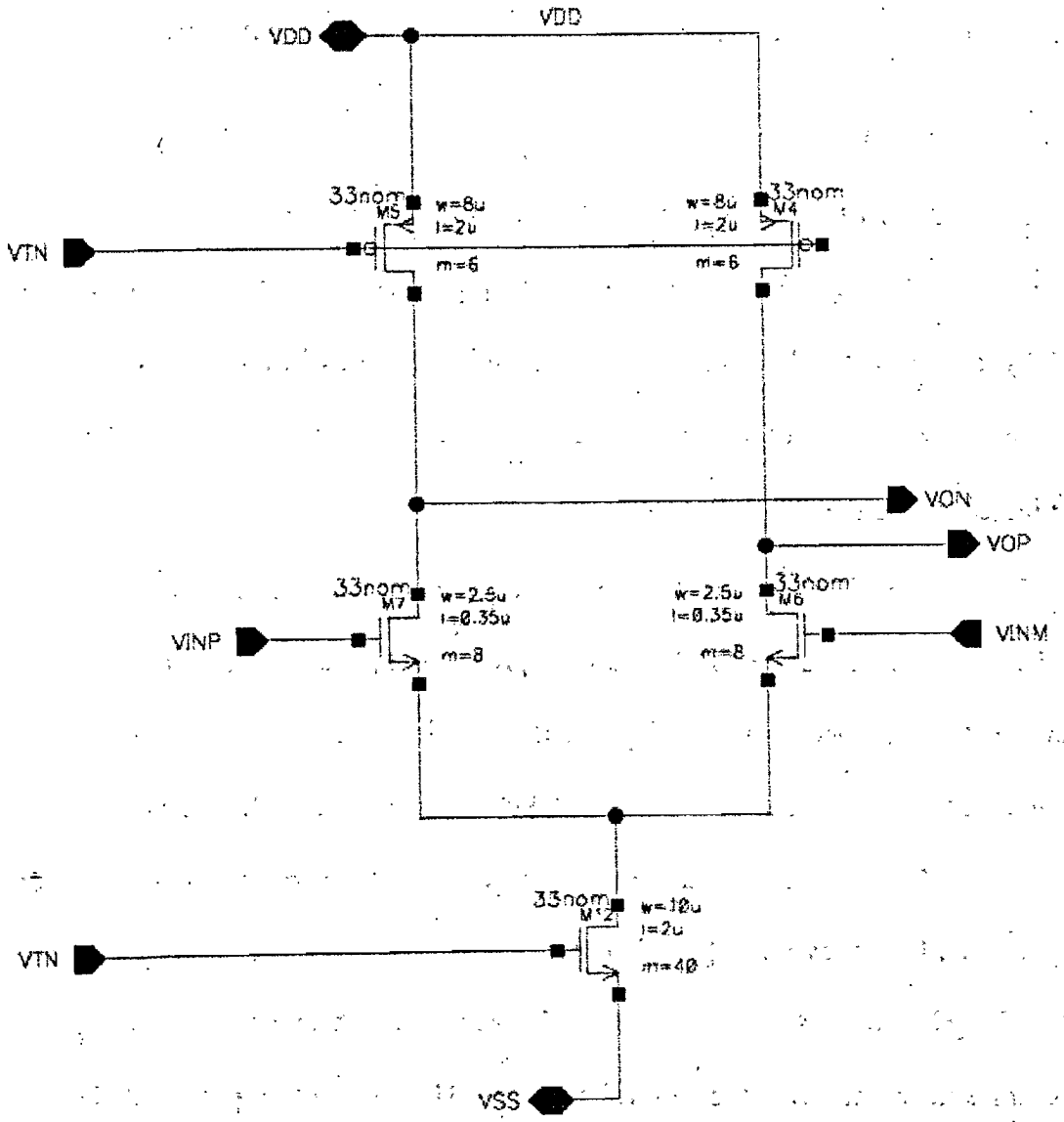

Fig. 3.4 Differential configuration with internal control

As it is shown in the circuit, the control in the delay cell (VTN) could be applied to the load or to the current. So, we can categorize this type of control to load control and current control.

3.2.2.1 Load Control

In this category two architectures will be discussed: resistive load and symmetric load.

3.2.2.1.1 Resistive Load

The basic architecture of this type of control is a tunable resistive load. This resistor can be implemented by a transistor in the triode region so that its resistance is controlled by changing the bias voltage. As shown in Fig. 3.4, when V_{cont} becomes more positive the resistance of the load transistors increases thus the time constant at the output increases and the f_{osc} will decrease.

If we can keep the resistor of the resistive load linear in a reasonable range, these linear resistor loads are desirable for dynamic supply noise rejection. As they provide differential–mode resistance that is independent of common-mode voltage carrying the supply noise, the delay of buffer is not affected by this common-mode noise.

However, with MOS transistors these devices cannot maintain linearity while generating a broad frequency range [13]. In other words, the transistors cannot be kept in the triode region for a wide range. The other problem is that the output voltage level is small and varies with the control voltage. Therefore the output should be amplified and converted for the full-swing output in order to be able to drive the next stage [14].

3.2.2.1.2 Symmetric Load

Maneatis and Horowitz [13] tried to fix the problem of range limitation in the resistive load architecture by devising a symmetric load. A half circuit of a block of their architecture is shown in Fig. 3.5.

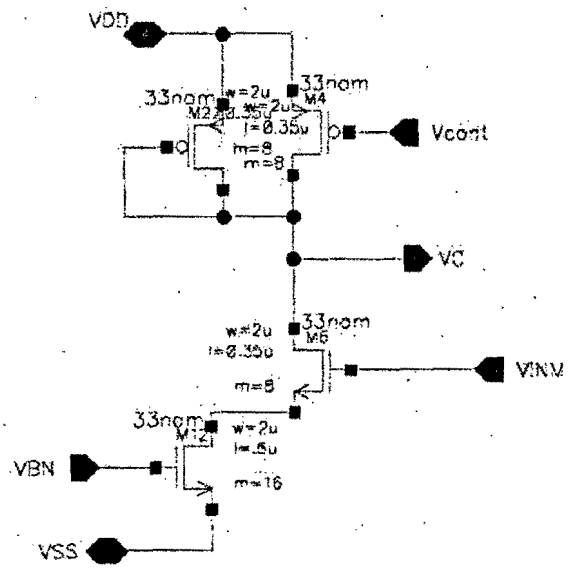

Fig. 3.5 Symmetric load idea [13].

In this architecture a diode-connected transistor will be connected in series with the resistive load. These transistors operate as follows: when $V_c > V_{cont} + V_{th}$ transistor M_4 operates in triode region and transistor M_{22} is off. When $V_c < V_{cont} + V_{th}$ transistor M_4 operates in saturation region and transistor M_{22} is on. The resulting current versus voltage is shown in Fig. 3.6.

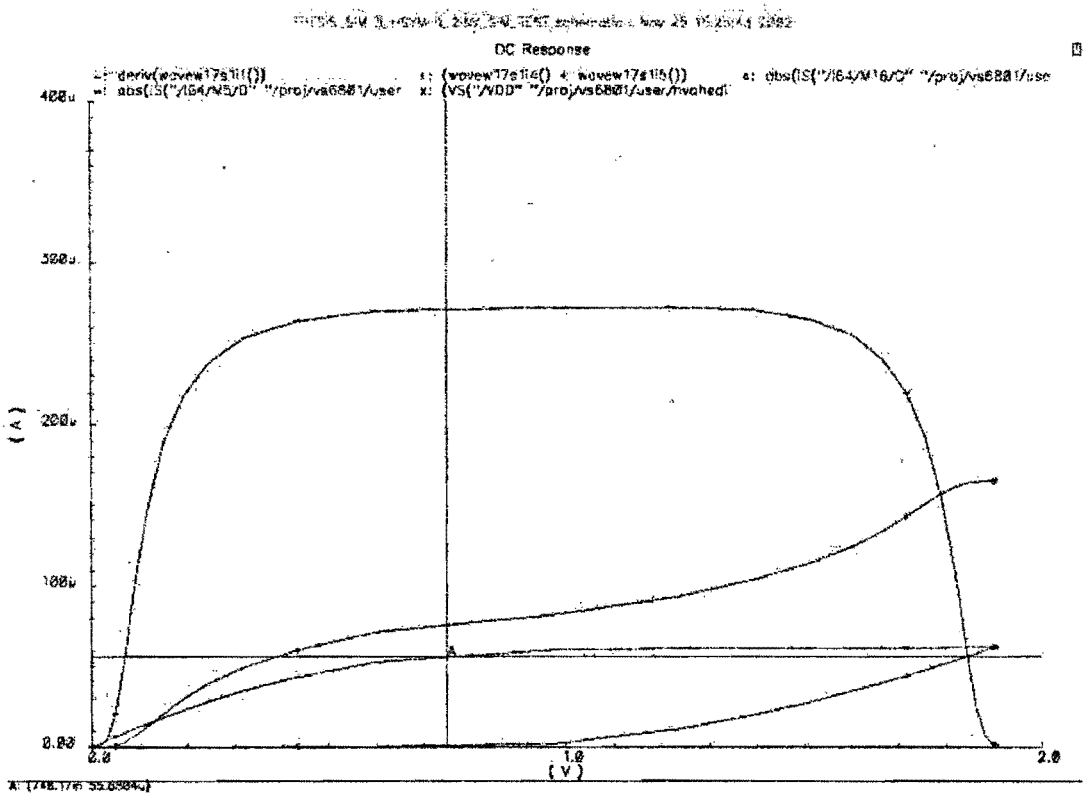

Fig. 3.6 Current of the symmetric load architecture.

As it can be seen in Fig. 3.6, the resulting resistor will be symmetric around the common mode. As the current in the two legs of Fig. 3.7 are symmetric and the load shows symmetric resistance around the common mode, the resistors seen at the two output nodes will have the same value. So, as shown in the curve of Fig. 3.7, the terms of outputs related to the noise will be cancelled. Ku Kang [14] and Lee [15] have used the cell of Fig. 3.7 in their PLLs.

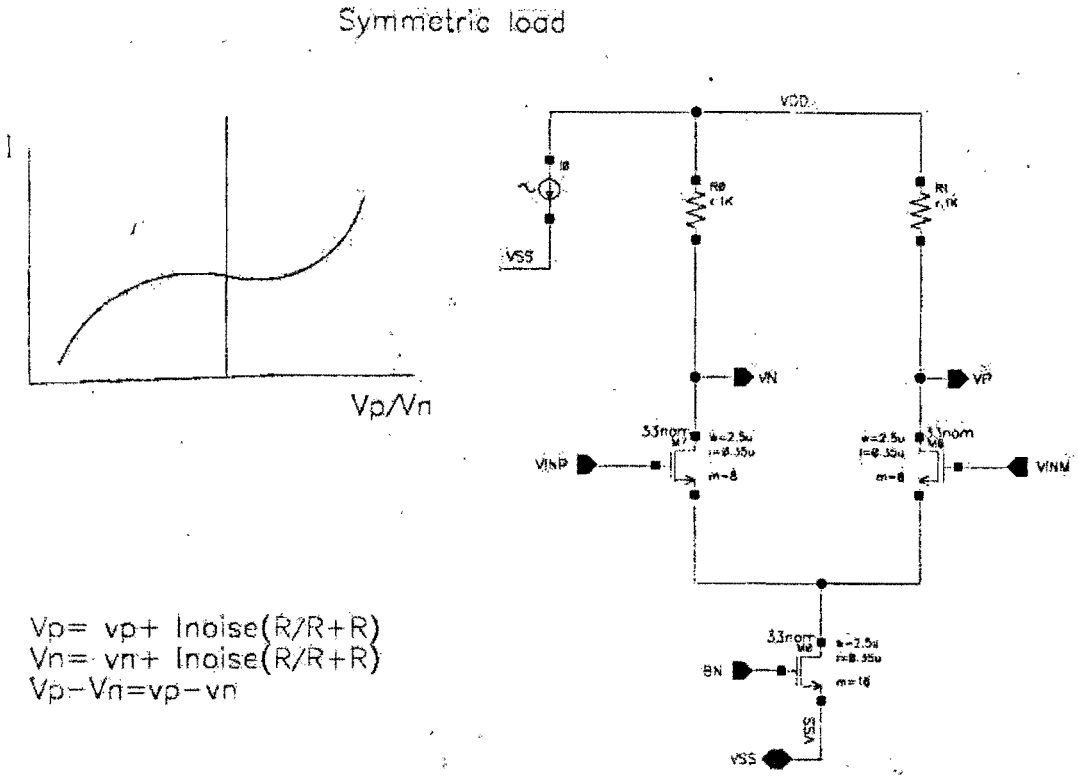

Fig. 3.7 Noise cancellation in symmetric load architecture.

3.2.2.2 Current Control

In this category two main architectures are discussed: diode-connected load and modified current control cell.

3.2.2.2.1 Diode-Connected Load

Diode-connected load is the basic architecture of this category. The circuit is shown in Fig. 3.8. In this circuit two diode-connected transistors are used as loads and the frequency is controlled by the tail current. The linear tuning range of this circuit is limited, because the frequency is determined by the g_m of the differential pair and the g_m is proportional to the square root of the current.

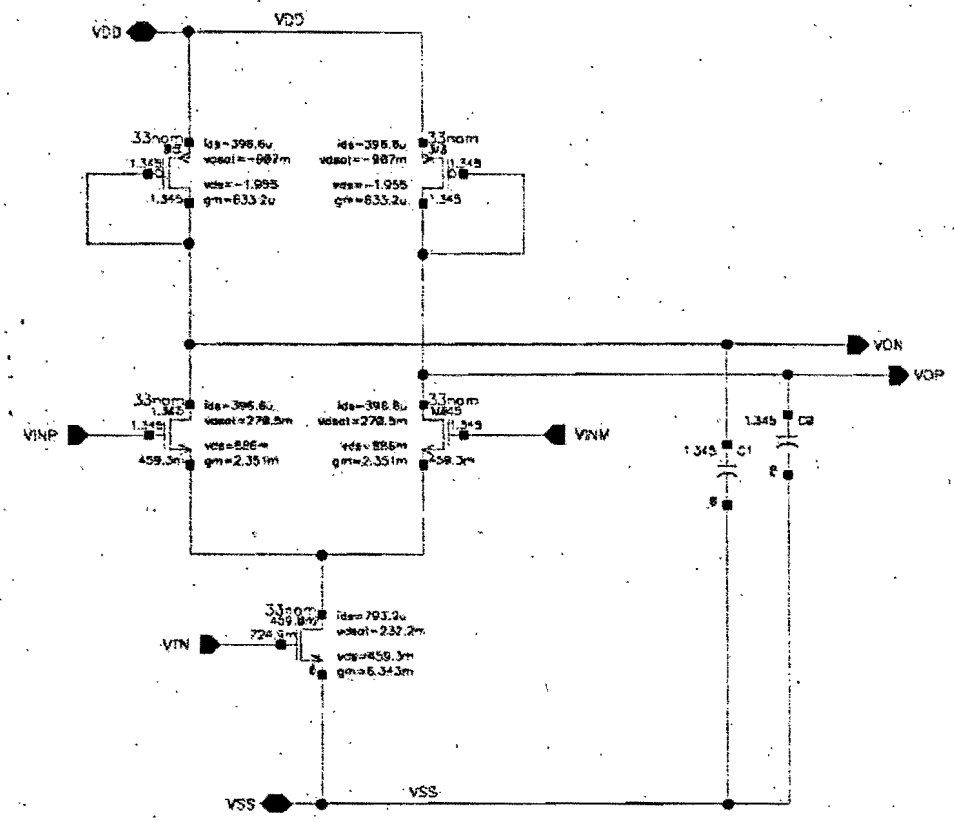

Fig. 3.8 Current control architecture with diode-connected load.

Also, the output swing is limited here. This architecture has been modified to have a better output swing [2]. But the main problem is that the nature of the differential pair doesn't allow both fast response and rail to rail swing. That is because changing the situation in each leg results in going through a linear transition. Therefore, a modified cell, as explained next, is adopted in the proposed technique.

3.2.2.2 Modified-Current-Control Cell

In the modified cell the differential pair is replaced by two inverters. The circuit is shown in Fig. 3.9. As the transition between "on" and "off" conditions in the inverter is much faster than the transition in a differential pair, this cell could reach higher frequencies. Another advantage of this cell is its almost rail to rail output. The circuit can cover a wide linear range. The supply noise rejection of the circuit is very good

because the circuit is isolated from the supply and substrate through the current sources. Djemouai *et al.* [16] have used this cell in their PLL.

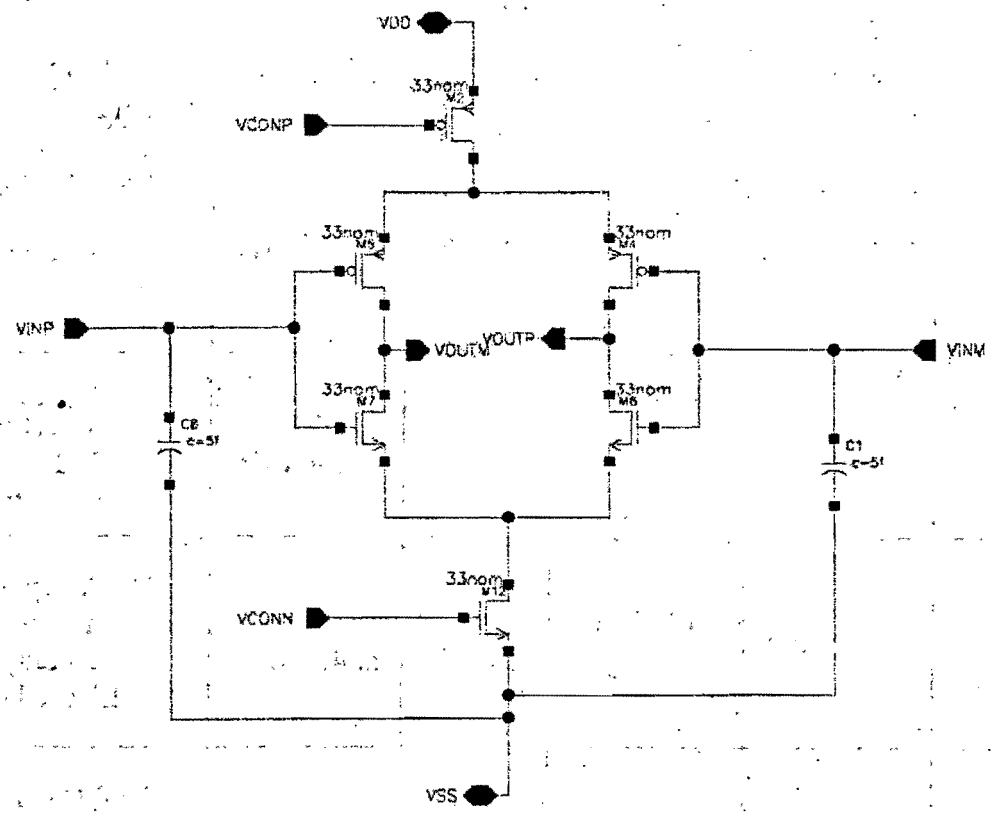

Fig. 3.9 Modified-control-current cell.

The characteristics of the discussed delay cells are compared in the Table 3.3. Through this comparison it can be concluded that:

- Symmetric load configuration is recommended when a limited output swing is required or the output swing variations could be fixed in the next stage.
- The modified current control configuration is recommended if a rail to rail fast swing is required.
- The architectures of these two configurations allow working with 1.8V supply.
- Power dissipation for these two cells are close to each other and the circuit consumes around 1mA in 100MHz.

Table 3.3 Comparison of different delay cells for VCO.

Architecture	Range	Output swing	Noise rejection	Power dissipation	Comments
Resistive load	Less than factor of 1.5	Variable with Controlling voltage	Weak	1.39mA at 200MHz	-Weak supply noise rejection -Variable output swing -Limited linear range
Symmetric load	Factor of 3	Variable with controlling voltage	Good	975u at 150MHz	-Good supply noise rejection -Wide swing -Variable output swing
Differential pair with diode connected load	Factor of 2	Limited swing	Weak	6.25mA at 400MHz	-Weak supply noise rejection -Limited output swing -Limited range
Differential inverters with two current sources	Factor of 3	Rail to Rail	Good	2.1mA at 450MHZ	-Good supply noise rejection -Wide swing - Rail to rail output swing

The last structure, i.e. modified current control cell, has some limitation on the speed. due to the upper and lower current sources. The challenge could be going for a higher speed delay cell by letting the upper and lower transistors work in the triode region. However, at the same time the supply noise issue should be resolved because with the transistors working in the triode region the delay cell is not immunized against noise. The goal is to have a fast delay-cell with a linear characteristic, while optimizing the jitter performance and having a robust delay-cell against temperature change.

All these reasons led us to devise a new architecture for VCO which is fast enough to work in GHz area and at the same time provides a symmetric rail-to-rail output. Due to the pseudo-differential arrangement and using fast switching and non-clipping method, this block has a good supply noise power rejection. A compensating block will be accompanied with this VCO, which helps us have a linear transfer function for the VCO. Also, the compensating circuit helps have a VCO which is robust against temperature changes. In addition the compensating circuit adds a mechanism for rejecting the supply noise up to certain frequencies. These attributes are elaborated in Chapter 4 which gives a somewhat detailed description of the delay cell.

Chapter 4

The Proposed PLL

In this Chapter the designed PLL will be described in two different levels: system level and circuit level.

4.1 System Level of the Design

The following decisions were made in order to implement the top-level system. First, due to the advantages mentioned in Chapter 2, a charge-pump configuration. has been chosen for achieving a programmable wide-range frequency, i.e. 100MHz to 1GHz, by a 50 MHz reference clock.

Programmable driving capability method [20] is used for achieving the wide frequency range. As described in Chapter 3, the frequency range is partitioned into smaller ranges and adding the driving capability of the VCO will provide us with different ranges. Also attempt has been made to use the idea of the method that uses some circuitry [9] to make the VCO transfer function more linear in order to have a wider range frequency. For this purpose, a novel compensating circuit has been added to the VCO block. As the reference frequency is much lower than the output frequency, a divider is used for bringing down the output signal frequency in order to be compared with the input frequency.

In addition to the basic sub-blocks used in a conventional charge-pump PLL - i.e. phase frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO) - a programmable divider, two comparators, a reference voltage block and a logic circuit are added to provide the programmability capability. The top level of the design is shown in Fig. 4.1.

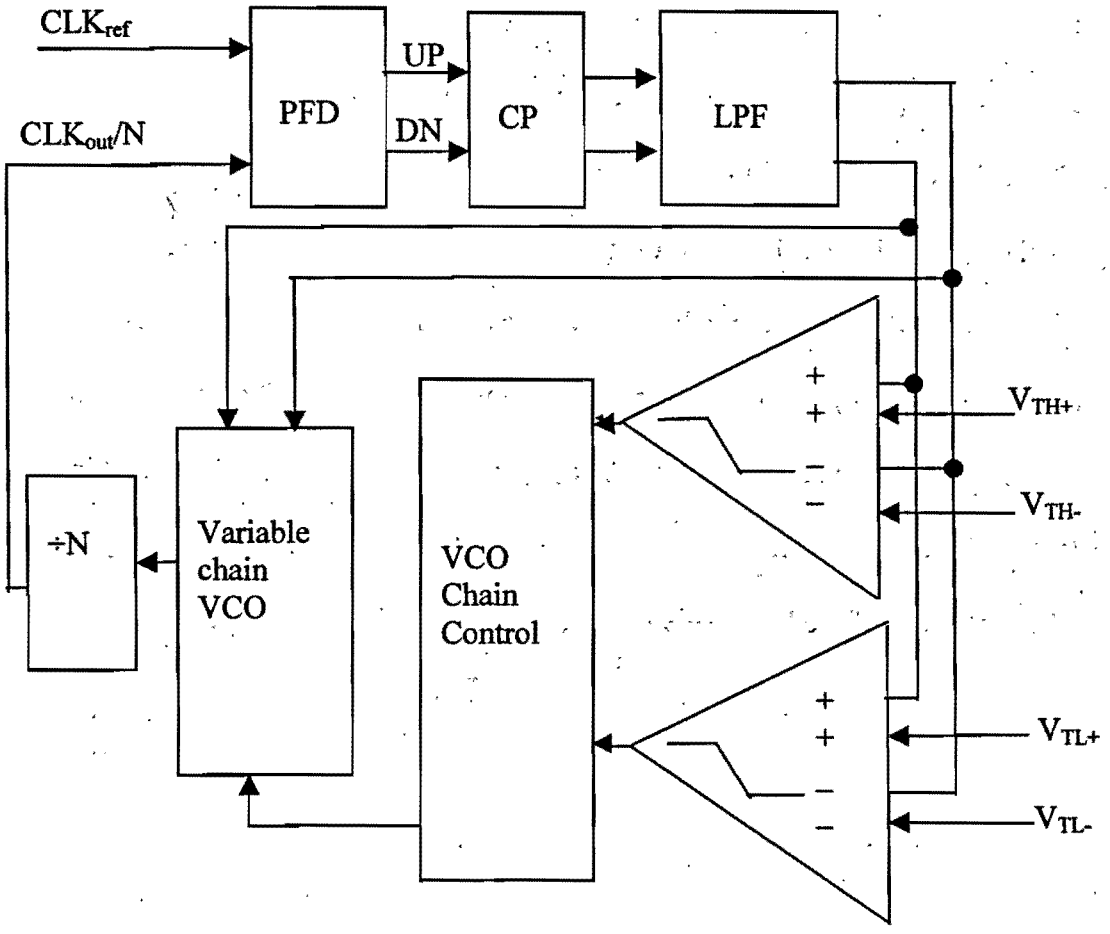

Fig. 4.1 The block diagram of the proposed PLL.

4.1.1 The Operation of the System

The output of the PLL (divided by N) is compared to the reference clock in a phase-frequency detector. The output of the phase frequency detector is fed to the charge-pump followed by a low-pass filter. The latter combination provides a control voltage for the VCO. Using a voltage-reference block, two thresholds are specified for this control voltage. Two comparators compare the control voltage with these two thresholds. The outputs of the comparators are fed to a logic circuit. If the comparators show the control voltage exceeds one of these thresholds, the logic circuit will decide to change the driving capability of the VCO by changing the

number of chains. This change will be transferred to the VCO using a translator called "MUX" block. The "MUX" block, which is a combination of several multiplexers, determines the driving capability of the VCO according to what the logic circuit has dictated. This is how the range of VCO is changed.

The top level of the design has been built using AHDL blocks and the functionality of the system was verified. These are the blocks that are designed with Analog Hardware Design Language (AHDL) to implement the desired functions. Fig. 4.2 shows the top level of the system using AHDL blocks. Also, the system level was implemented in MATLAB by SIMULINK. This was done in order to check the dynamics of the system and the stability of the loop. This implementation will be shown later.

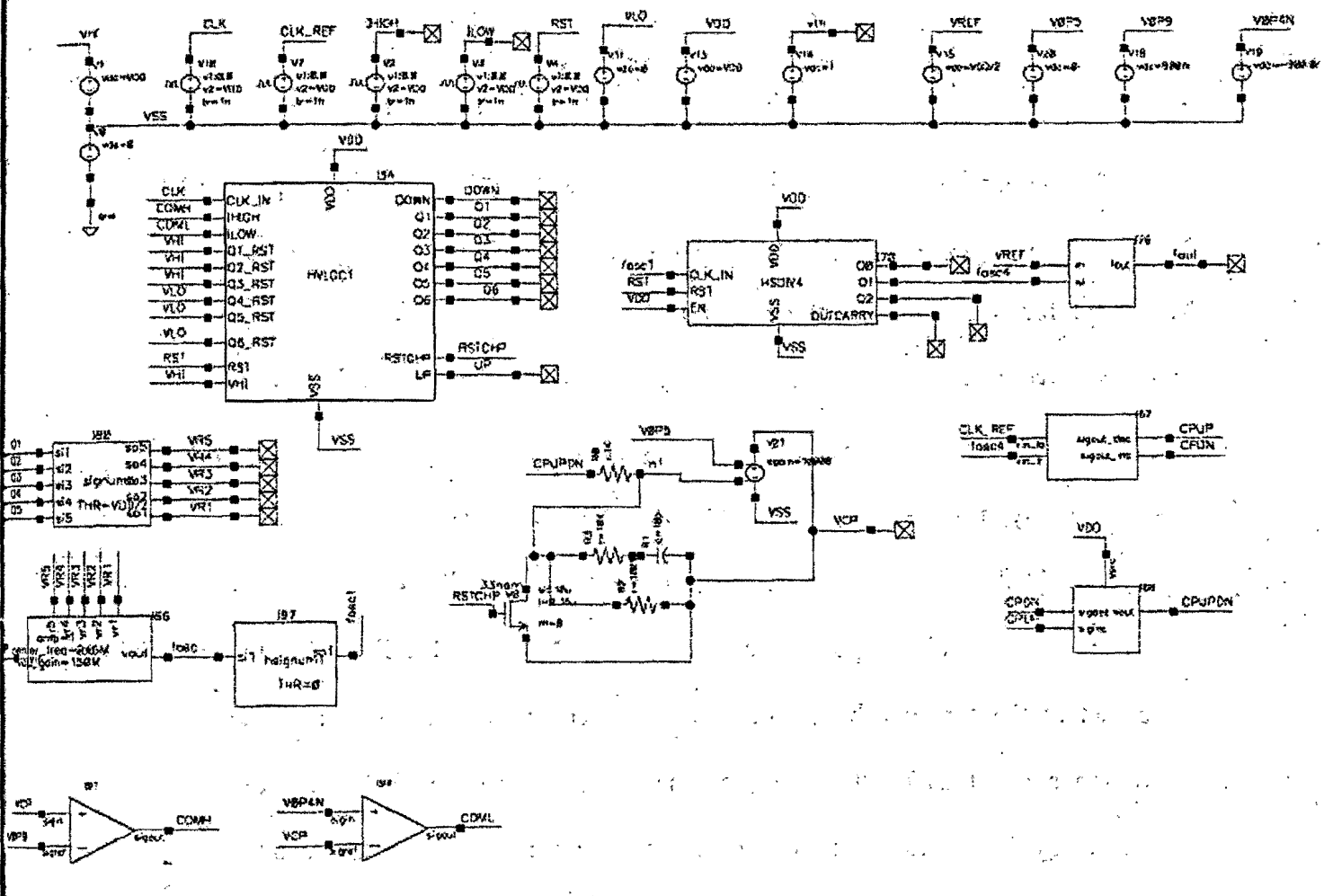

Fig. 4.2 Implementation of the top-level system with AHDL blocks.

4.2 Circuit-Level Design of PLL Blocks

Design and simulations have been done using CADENCE tool and HSPICE simulator. In this section the circuits designed for the delay cell, VCO, charge-pump, frequency-phase detector, and low-pass filter are described. The blocks that implement the programmability are covered in the next section. The most important block in this PLL is the VCO which is a ring oscillator which has three delay cells in its chain.

4.2.1 VCO Delay Cell

A new fast delay-cell with a linear transfer function and suitable for high speed, wide-range applications is used for the VCO. The proposed delay-cell is shown in Fig. 4.3. The trend for designing a fast delay-cell is an inverter based one [20,11,12]. A modified inverter-based delay cell is used. The following are the modifications made to improve the performance of the delay cell.

- Normally, the frequency of VCO is controlled outside of the delay-cell. It was decided to control the frequency inside the delay cell in order to reduce the noise. For this purpose, two transistors (M0 and M1 in Fig. 4.3) were added at the top and bottom of the inverter. These transistors work in triode region and act as resistor. By changing the value of these resistors the VCO frequency is fine-tuned. In this case we have a rail to rail output and the symmetry of the circuit helps get undistorted output waveform.
- As seen in Chapter 3, the differential configuration makes the delay-cell slow. Therefore, the single-ended configuration was chosen. However, to take advantage of a pseudo-differential configuration, two single-ended legs (i.e the circuit of Fig. 4.3) are bound through two inverters in order to be synchronized as if they are differential (Fig. 4.4). In this pseudo-differential configuration the common-mode noise is rejected: It can be seen that if the IN+ and IN- are increased, V_{out+} and V_{out-} will decrease while the inverters which bind the two outputs dictate opposite directions for two outputs. This fight keeps the common mode constant. They keep the zero crossing at mid-supply and cause the two outputs to be symmetric.

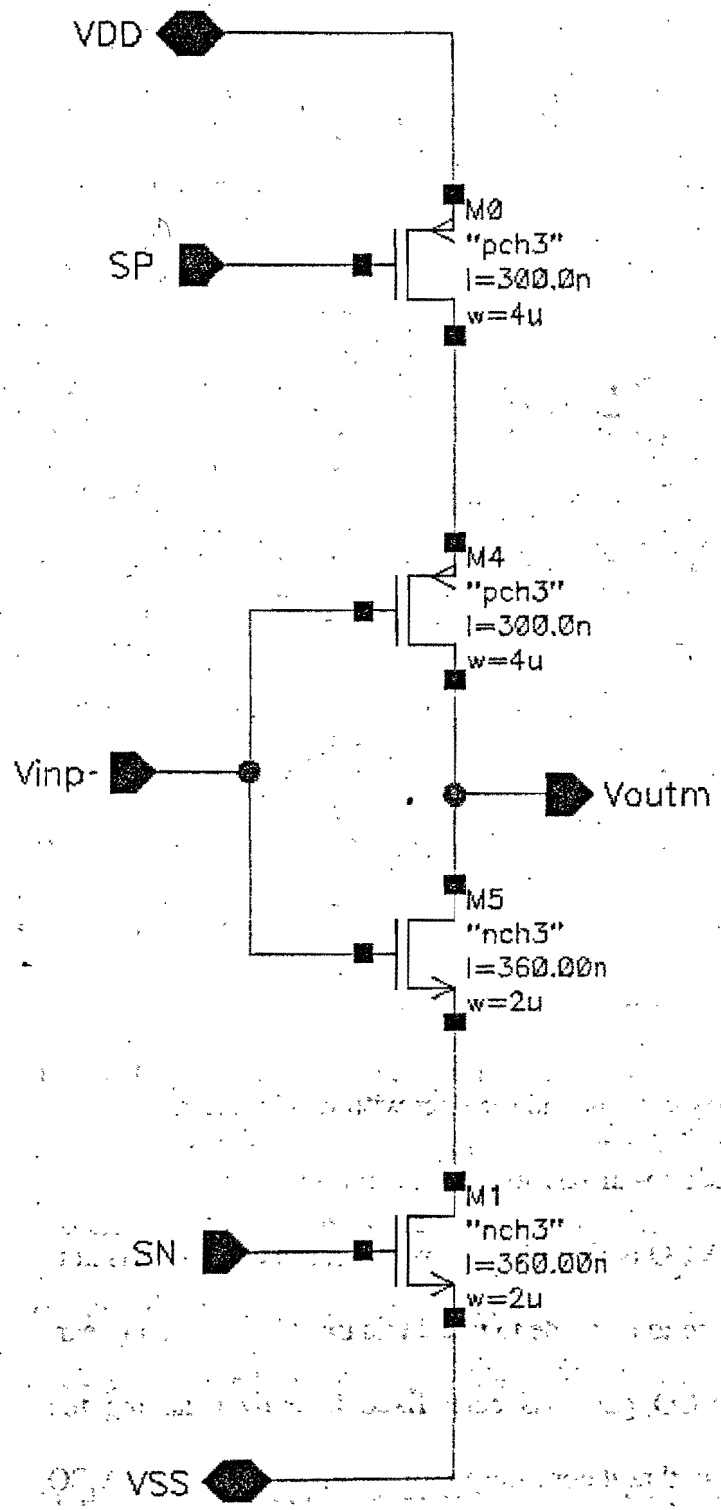

Fig. 4.3 Delay cell architecture with upper and lower controlled resistor.

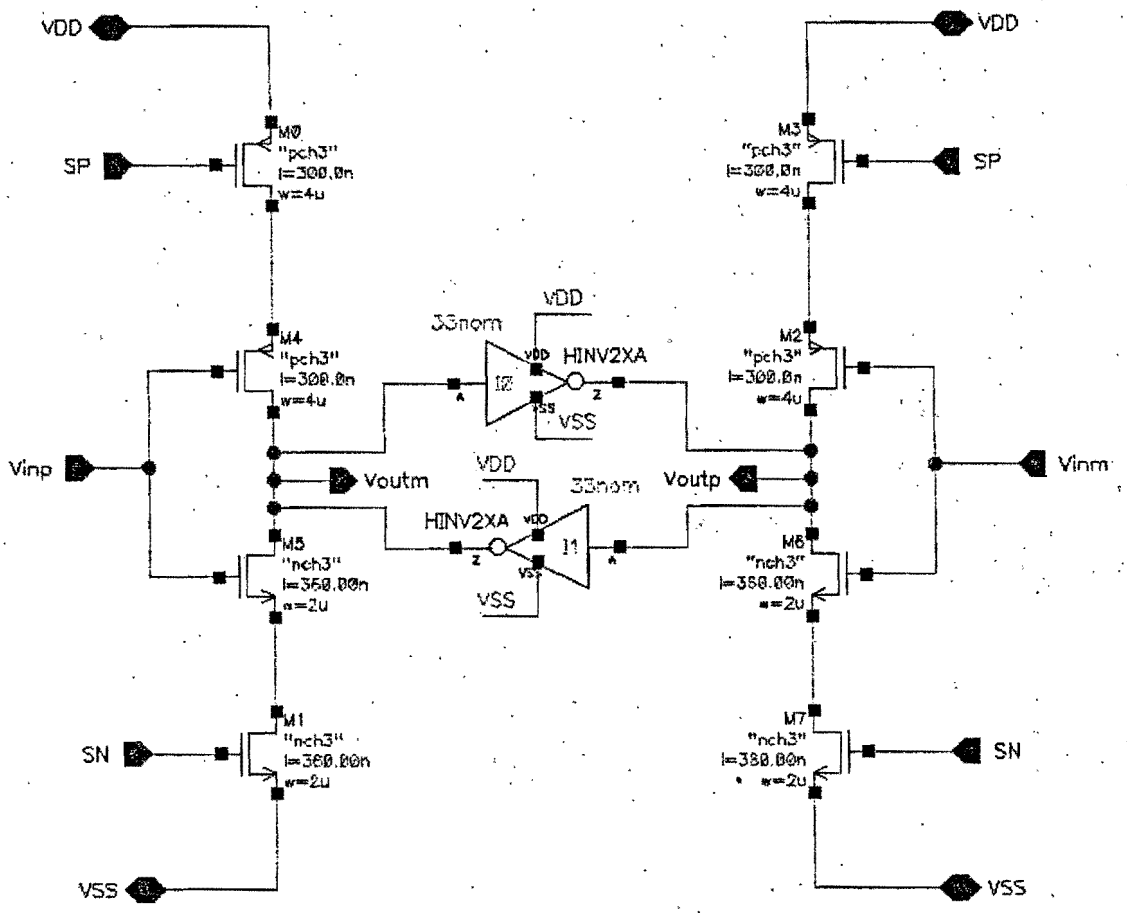

Fig. 4.4 Two single-ended delay-cells bound together with two inverters in order to make a pseudo- differential configuration.

- The transfer function of the VCO built with the inverter-based delay-cell is not linear. Another modification had to be made to make this transfer function linear. The problem of nonlinear VCO gain has been fixed here by changing the controlling voltage in such a way that it compensates the nonlinearlity of the VCO gain. This circuit, shown in Fig. 4.5, is called mapper and consists of a V/I (voltage to current) converter and an I/V (current to voltage) converter. Here is how mapper works: the differential outputs of the charge-pump are fed to this

circuit. First, these outputs are converted to a current through the V/I block. Then the current is converted to two controlling voltages, but now the controlling voltages are reshaped so that they compensate the non-linearity of the delay-cell gain and therefore the VCO transfer function will be linear.

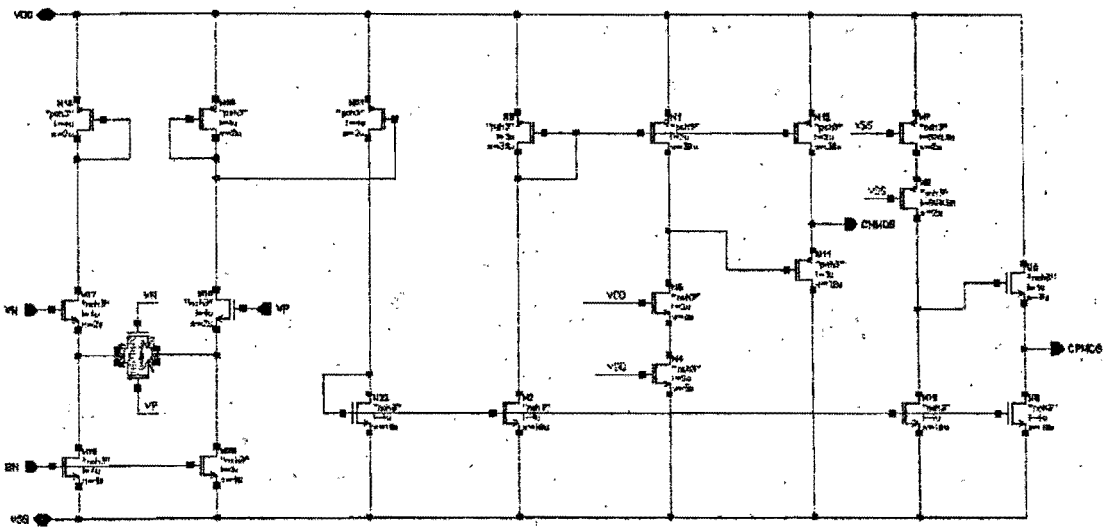

Fig. 4.5 The circuit of mapper.

- For the method of programmability utilized in this design, the VCO should be insensitive to the temperature change. This function is also realized in the mapper. The voltages provided in mapper are insensitive to temperature changes: Fig. 4.6 is a partial schematic of the mapper accompanied by the transistor which acts as a resistive load in the delay cell (transistor M2). Here is how g_{ds} of transistor M2 is calculated. The transistor works in triode region. As $V_{DS} << 2(V_{GS}-V_{th})$, we have:

$$g_{ds2} = dI_D/dV_{DS} = [\mu_n C_{ox}(W_2/L_2)(V_{GS2} - V_{tn})] \cong 1/[\mu_n C_{ox}(W_2/L_2)V_{GS2}] . \quad (4.1)$$

On the other hand, for the transistors in the deep triode region, i.e. transistors M4 and M5, we have:

$$V_{DS5}=I_D/[\mu_n C_{ox}(W_5/L_5)(V_{DD} - V_{tn})] \cong I_D/[\mu_n C_{ox}(W_5/L_5)(V_{DD})]. \quad (4.2)$$

From Fig. 4.6 we have

$$V_{GS2} = 2V_{DS5} + V_{GS11} \qquad (4.3)$$

But transistor M11 is a level shifter and V_{GS2} is mainly determined by V_{DS5}. Combining equations (4.1), (4.2) and (4.3) will yield

$$g_{ds2} \cong \mu_n C_{ox}(W_2/L_2)[(2 I_D/(\mu_n C_{ox}(W_5/L_5)(V_{DD}))], \qquad (4.4)$$

$$g_{ds} \cong (2 I_D W_2/L_2)/((W_5/L_5)(V_{DD})) .$$

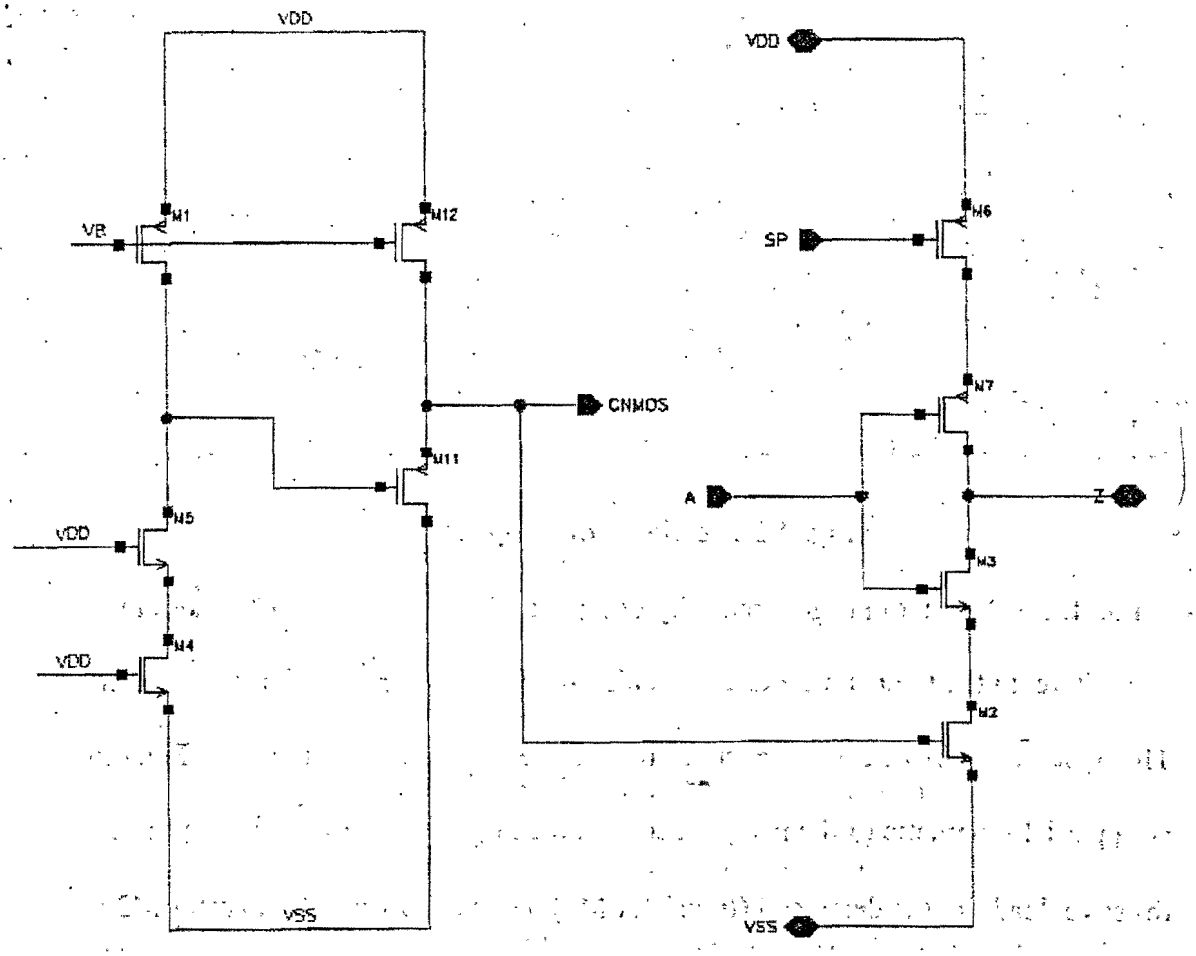

Fig. 4.6 A partial schematic of the mapper accompanied by the transistor which acts as a resistive load.

If V_{DD} is considered constant:

$$g_{ds} = KI_{bias},$$

where K is a constant and I_{bias} is insensitive to temperature.

- The other important point in the delay-cell is the supply noise rejection. The mapper provides good supply noise rejection for certain frequencies, that is up to around 200MHz: In Fig. 4.7, which is a partial schematic of the mapper and the delay cell, we can write for transistor M0

$$V_G=V_{DD}-2V_{DS}-V_{GS9}.$$

From this equation, when V_{DD} changes, this change will appear in V_G. Therefore, we can write:

$$\Delta V_G= \Delta V_{DD}.$$

On the other hand we can see from Fig. 2.7 that the change in V_{DD} directly appears on source of Transistor M0 and we can write

$$\Delta V_S= \Delta V_{DD}.$$

Therefore, V_{GS} of transistor M0 is independent of V_{DD} change and hence insensitive to supply noise. Researchers have shown that the inverter-based delay-cells have good supply noise rejection because of the fast switching [6].

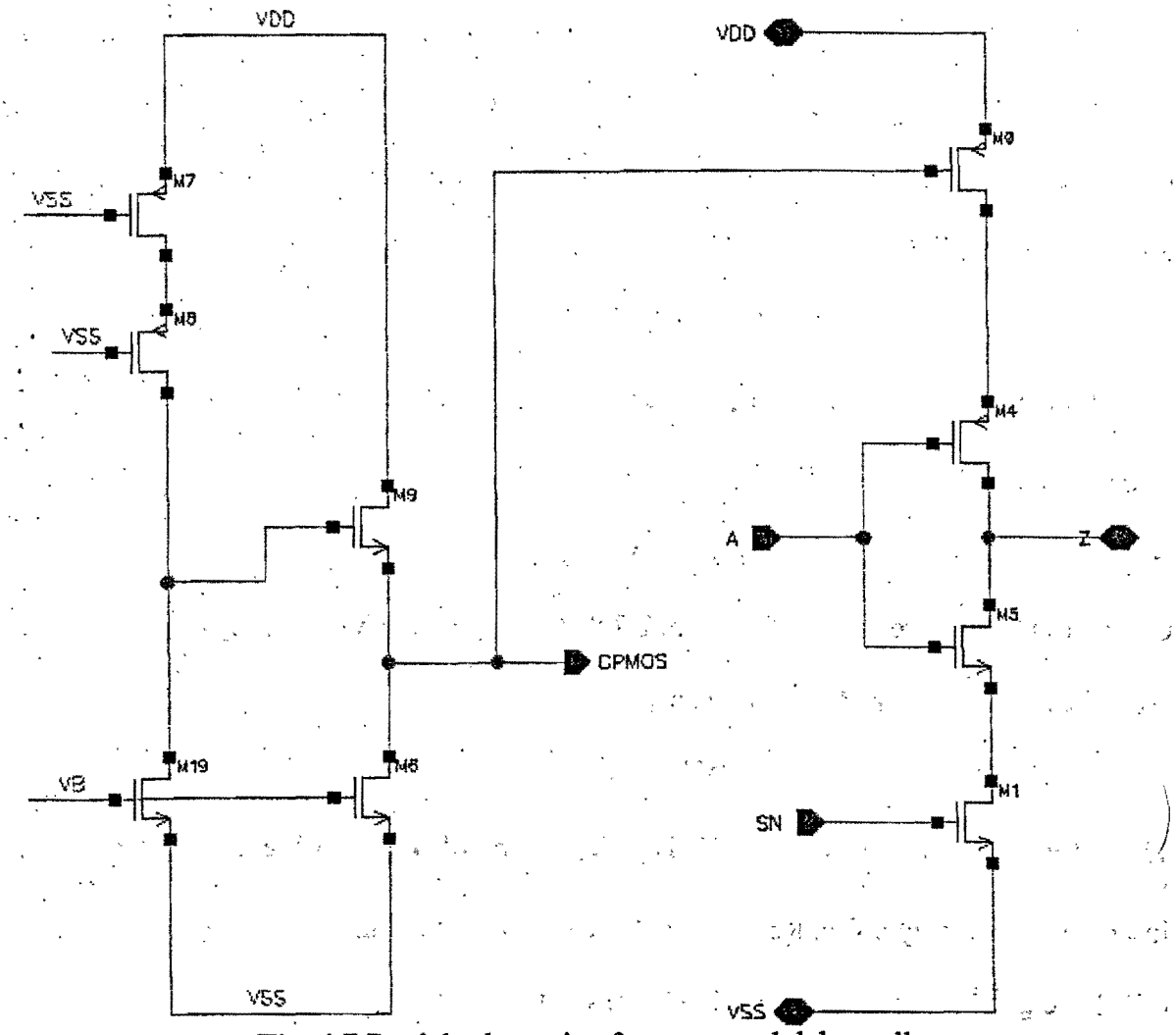

Fig. 4.7 Partial schematic of mapper and delay cell.

4.2.2 VCO

The proposed VCO is a ring oscillator which has three delay cells in its chain. Fig. 4.8 shows the basic architecture of the VCO. Seven parallel chains have been provided For providing programmable driving capability.

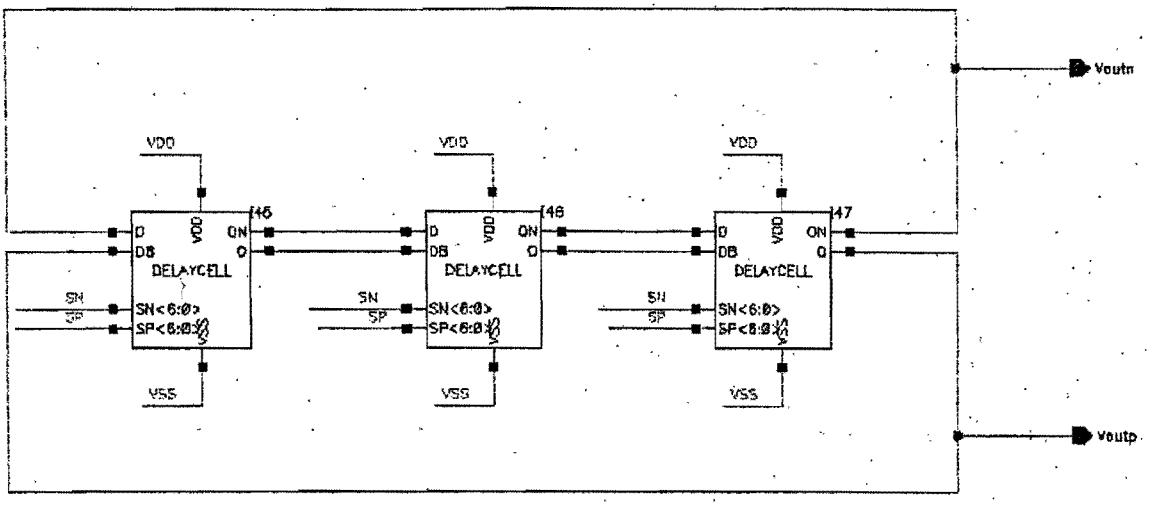

Fig. 4.8 Basic architecture of the VCO.

Fig. 4.9 shows the schematic diagram of circuits inside each of the blocks of Fig. 4.8 (for simplicity only four chains out of the seven chains have been shown.) As mentioned in Chapter 3, the frequency range of the ring oscillator VCO is at most a factor of three, which is hardly enough for the temperature and process variation coverage. In order to attain the desired frequency range, seven chains of such a ring have been put in parallel so that we can split our wide range into seven different smaller ranges. The ranges have about 20% overlap and a proper number of chains will be in operation in any desired range. A logic circuit will decide the number of required chains. When a chain is not in operation, it is turned off so that the power dissipation is optimized.

In order to have enough driving capability at the output of the VCO, a block consisting of a chain of inverters is used to bring out the output of the VCO. This block, called TAP, is suitable for driving 2pF capacitive load at the output of the VCO. Fig. 4.10 shows the TAP architecture.

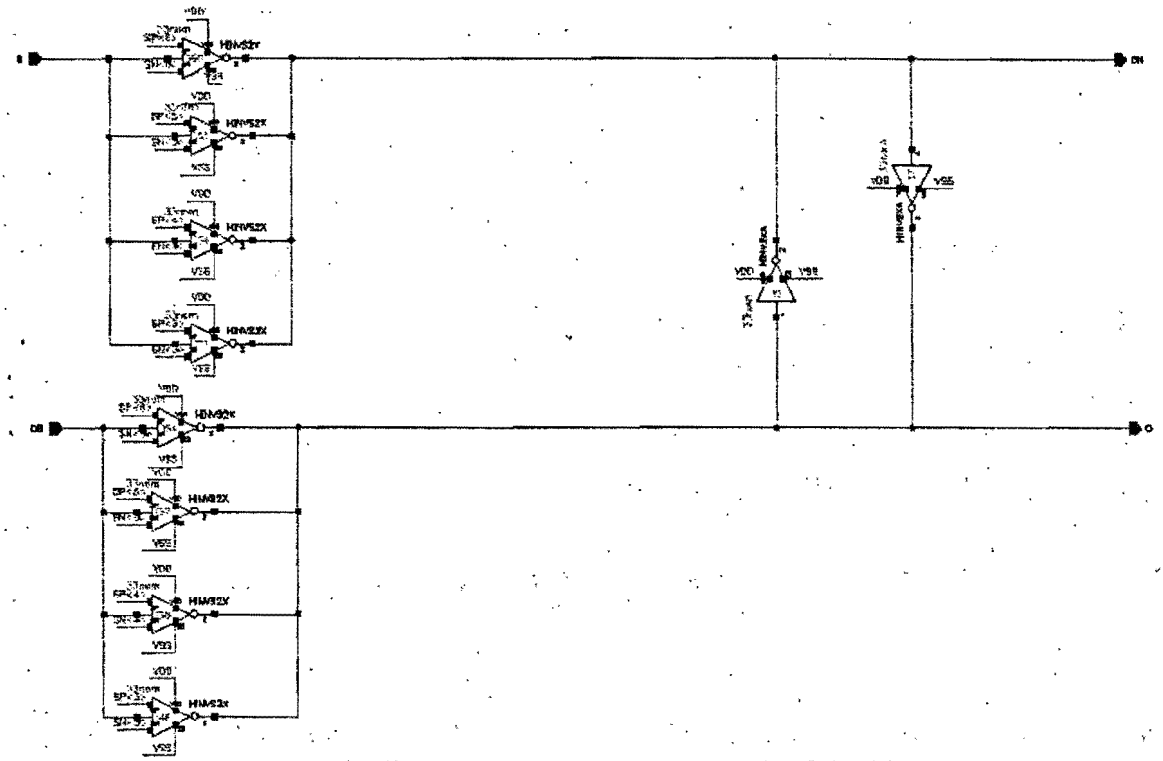

Fig. 4.9 The schematic diagram of circuits inside each of the blocks of Fig. 4.8.

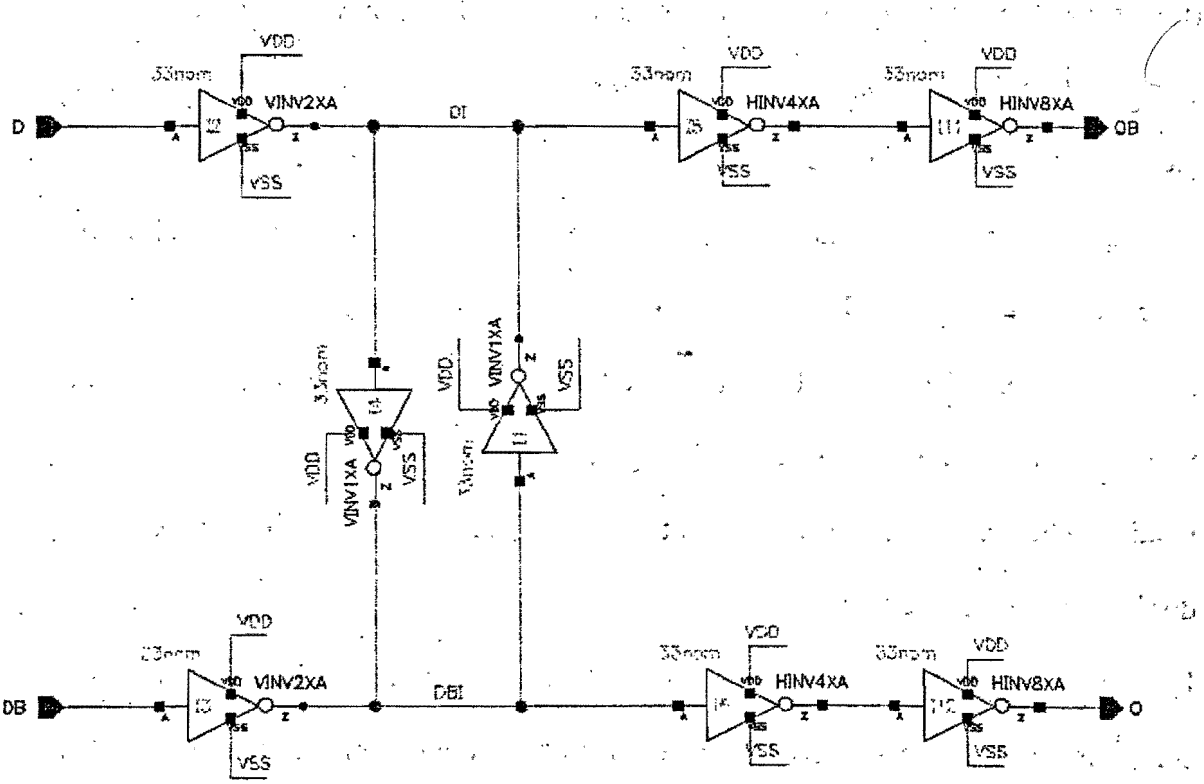

Fig. 4.10 TAP architecture.

4.2.3 Charge-Pump

For choosing the appropriate charge-pump architecture, different charge-pumps were studied. A simplified version of the final architecture is shown in Fig. 4.11. In this architecture the switches M8 and M12 control the current flow to the charge-pump's output. These switches are placed on the source side of the current-source devices, i.e. M7 and M13, in order to attenuate any switching errors that may appear at the sensitive output node. In other words the output nodes are isolated from the switches in order to avoid switching ripples appear on outputs.

The dummy devices M49-M52 are employed to reduce both charge injection and clock feed-through errors [3]. These transistors introduce capacitors that cancel the switches C_{gd} effects [11]. Transistors M41 and M44 are used to ensure a fast turn-off of the current sources.

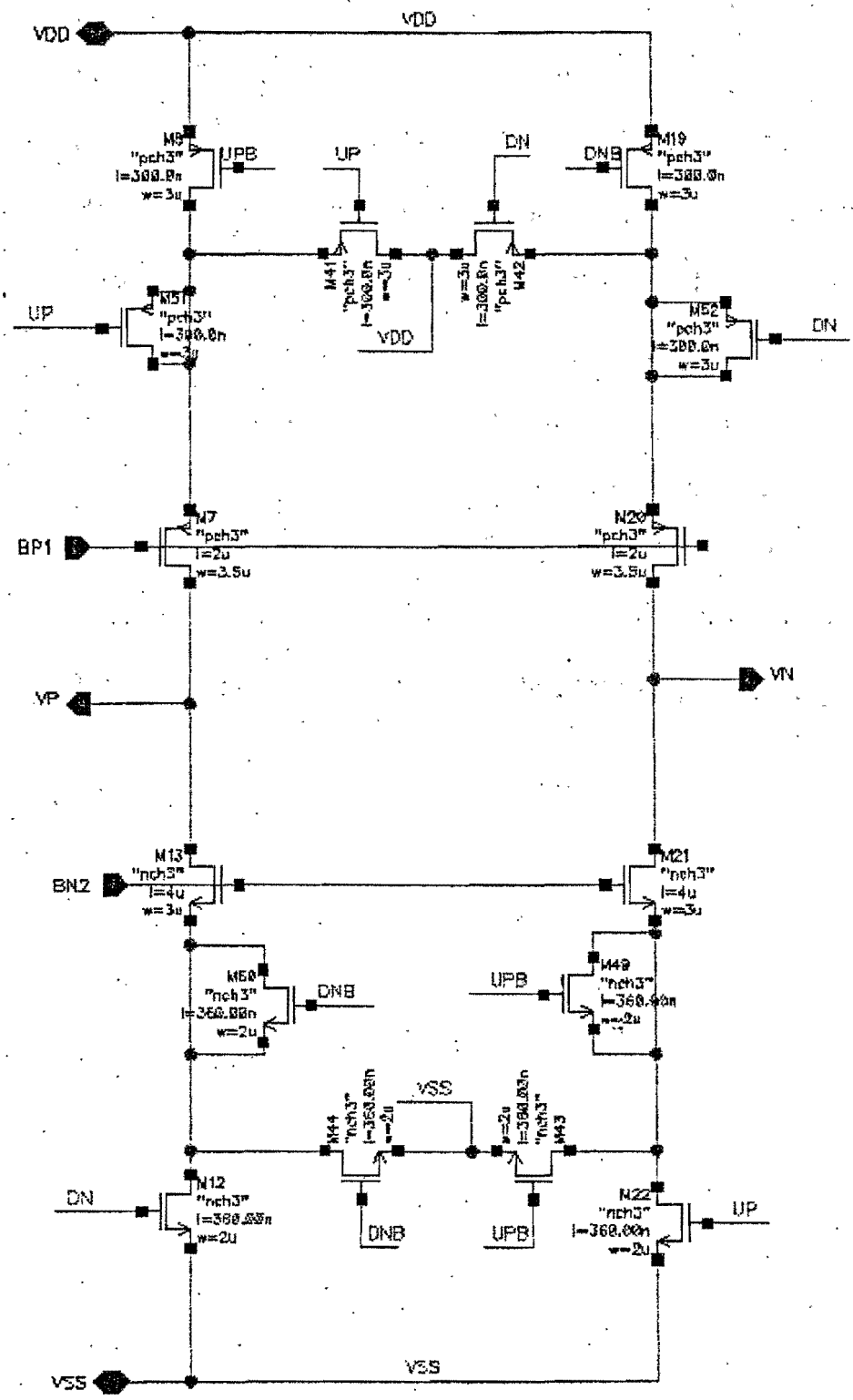

Fig. 4.11 The Basic architecture of the chosen charge-pump.

The challenge in charge-pump design was to make the common-mode voltage constant. Usually, a conventional common-mode feedback (CMFB) circuit accompanies the charge-pump. In the CMFB circuit, Fig. 4.12, the difference of the differential outputs of the charge-pump is compared with the reference voltage in a differential pair and a bias current is made which forces the common-mode voltage to be constant. However, when the charge-pump doesn't sink or source charges, e.g. when it is in locked condition, the switches are open and the bias current cannot keep the common-mode voltage constant. To resolve this issue, a dummy circuit was added to have constant common-mode voltage at all time, see Fig. 4.13.

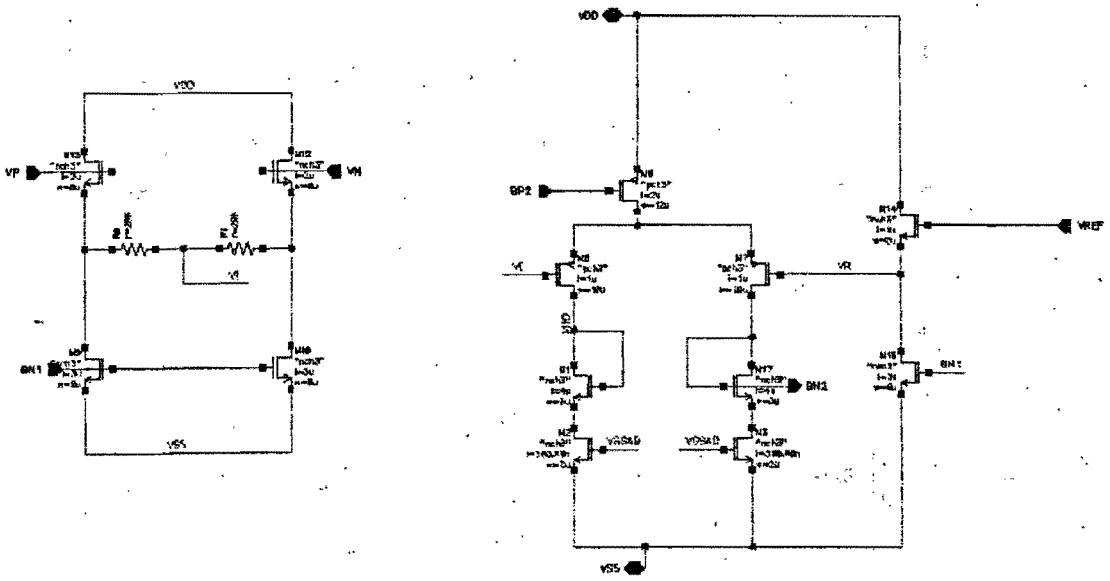

Fig. 4.12 The CMFB circuit for the charge-pump.

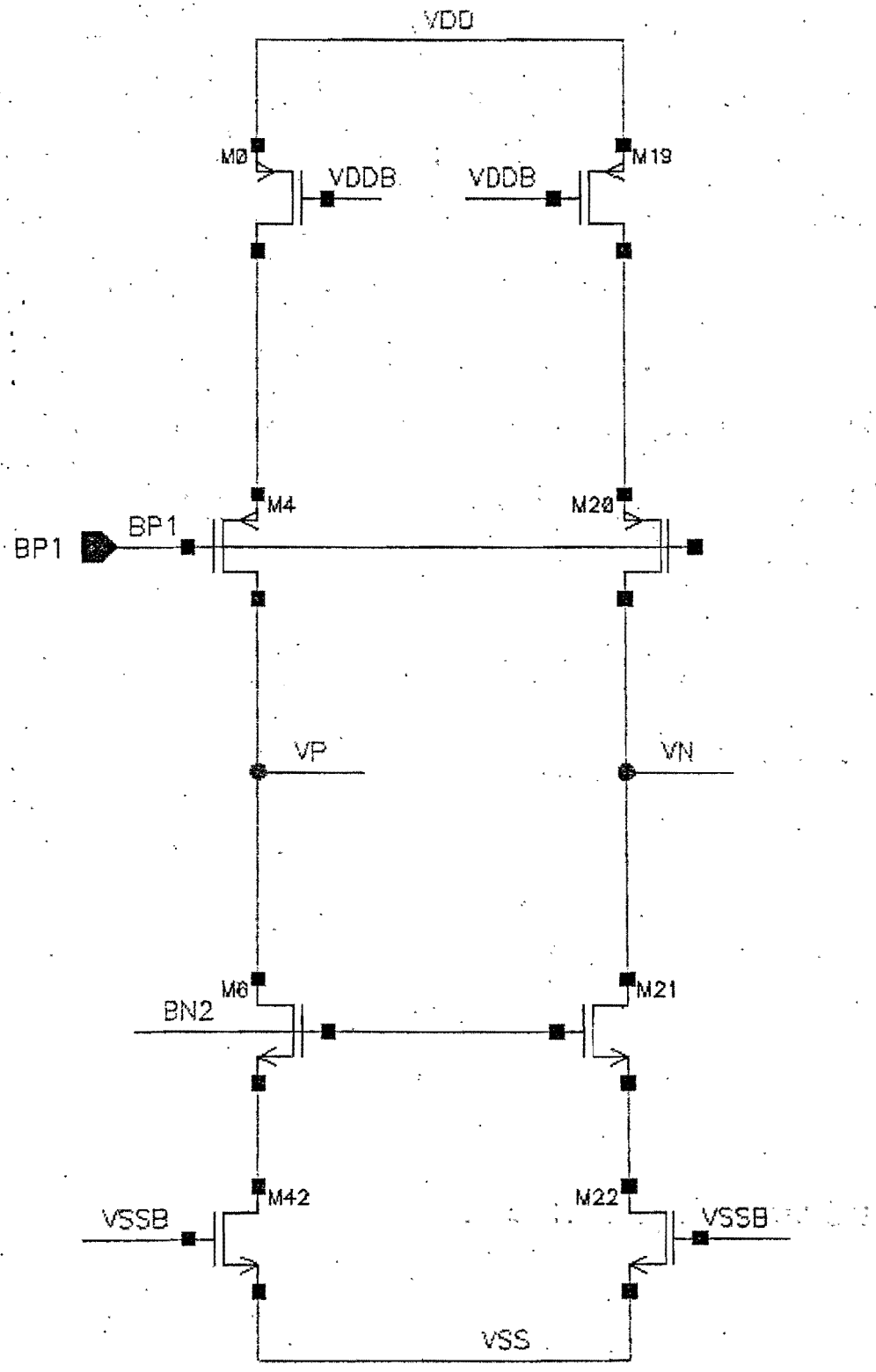

Fig. 4.13 Dummy circuit added to the charge-pump.

4.2.4 Phase-Frequency Detector

The phase frequency detector (PFD) is a robust tri-state detector. The basic configuration of the PFD is shown in Fig. 4.14. The configuration is close to the one described in Chapter 2. Two main signals are fed to two Flip-Flops as clock signals. When the rising edge of the leading signal appears, the output of the relevant Flip-Flop will be logic one and this output will be maintained in logic one until the rising edge of the other signal appears. At this time the reset signal will be logic one and both outputs will go to logic zero.

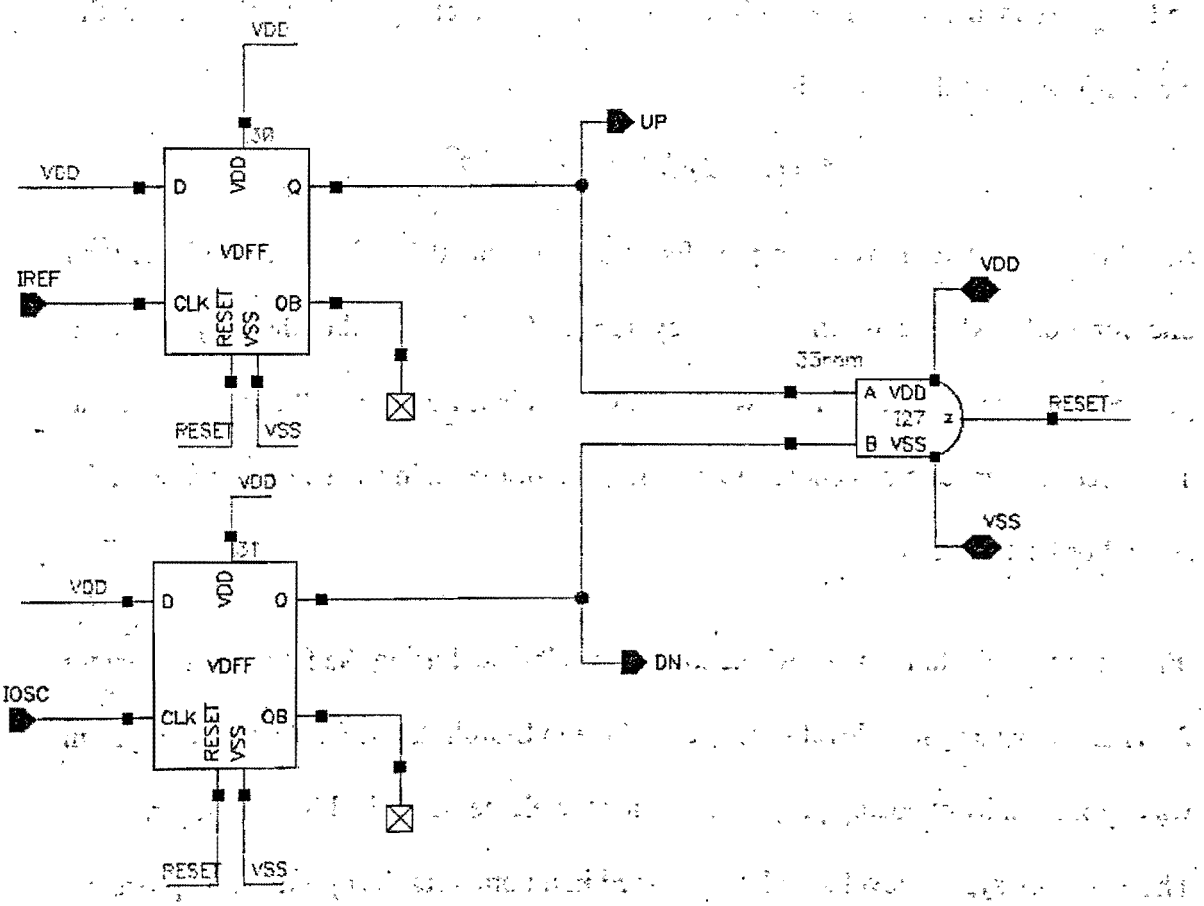

Fig. 4.14 Basic architecture of the phase-frequency detector.

The simulation result shows that this circuit functions properly up to 200MHz.

No challenge has been made for removing the narrow pulses appearing in reset time in both outputs, because these small outputs assures that there is no dead zone in the charge pump [2]. The phase difference could be as small as zero.

4.2.5 Low-Pass Filter

As discussed in Chapter 2 and shown in Fig. 2.9, a proper low-pass filter is a resistor and a capacitor in series, in parallel with a small capacitor. The bandwidth of the low-pass filter has an important role in stability of the whole loop. The sizes of the resistor and capacitors are chosen as follows. As we have a charge-pump architecture, the damping factor of the system is

$$\xi = (R_P / 2)\sqrt{(I_P . C_P . K_{VCO}) / 2\pi} .$$

Stability dictates to have a damping factor greater than 0.5 and not much bigger than one for both extreme of the frequency range. In this formula, the only unknown parameters are R_p and C_p. These values are chosen in a way to fulfill this requirement. The second capacitors is chosen to be one tenth of the main capacitor to maintain the second order configuration.

First, the transfer function of whole loop was calculated using the formulas of chapter 2. Then using a system level simulation, done in Simulink, the stability of the system was optimized by choosing proper values for the elements of the low-pass filter. The Simulink system level simulation helped in automating the optimization process. Fig. 4.15 shows the low-pass filter architecture.

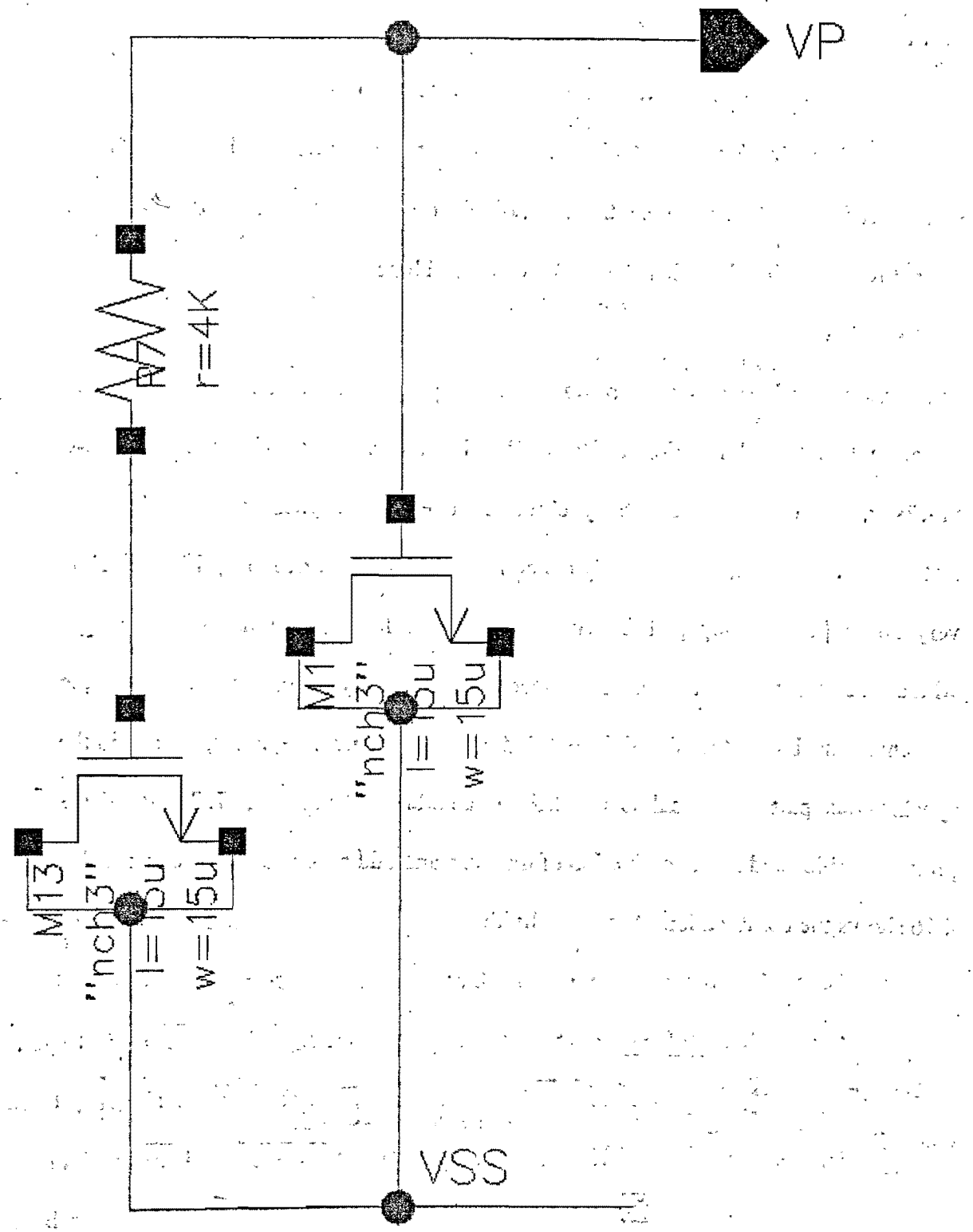

Fig. 4.15 The low-pass filter architecture.

4.3 Programmability and Utility Devices

In this section the blocks used for achieving on-chip programmability, such as programmable divider, logic circuit, comparator are described. The circuits for voltage reference block (to set the threshold for programmability) and bandgap, and current reference block (utility devices) are covered here.

4.3.1 Divider

The divider used in this system was a challenging one, because we needed a fast divider which could function up to 1GHz. Therefore, the divider was split to two blocks, an asynchronous and a synchronous one. In the asynchronous block, or the fast part of division, we are only concerned with the delay of D-Flip-Flop which is very small [about 200ps]. The synchronous block follows the asynchronous one, where the frequency has been reduced by the asynchronous divider. In the asynchronous block the signal is divided by an even number, say 2,4,8, and in the synchronous part the signal is divided by an odd number, say 3,5,7. The divider is programmable and any combination of the even and odd numbers can be chosen. Fig. 4.16 shows the combination of the two dividers

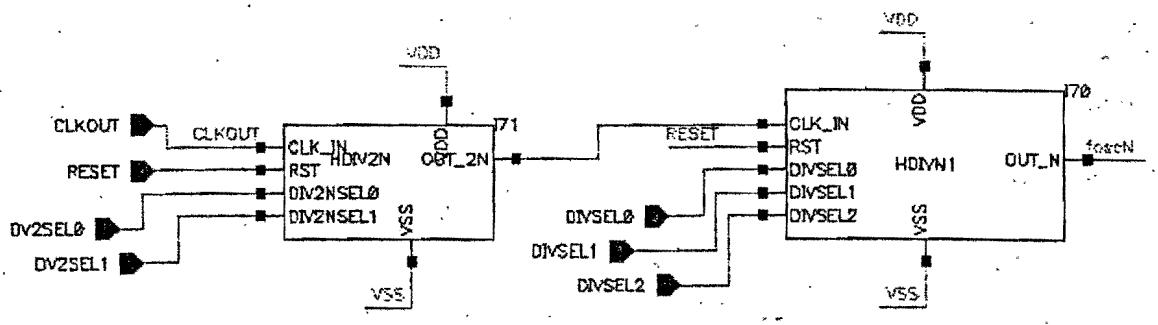

Fig. 4.16 Combination of two dividers (synchronous and asynchronous).

4.3.1.1 Asynchronous Divider

The asynchronous divider is a combination of D Flip-Flops. The main signal to be divided is fed as a clock signal to the first Flip-Flop. The output of each Flip-Flop, i.e. Q, is fed as a clock to the following Flip-Flop and the inverted output of each Flip-Flop is fed as an input to itself. Fig. 4.17, shows the architecture of the asynchronous divider. The output of the first Flip-Flop is a divided-by-two signal, the output of the second Flip-Flop is a divided-by-four signal and the output of the third Flip-Flop is a divided-by-eight signal.

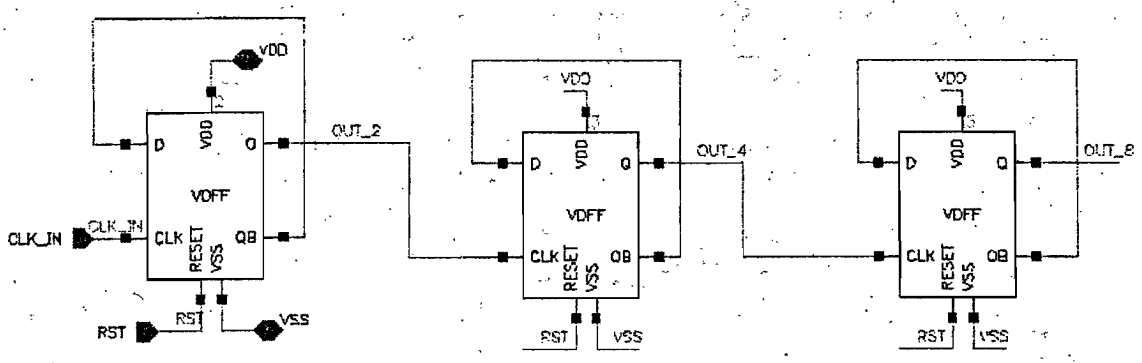

Fig. 4.17 Asynchronous divider.

4.3.1.2 Synchronous Divider

Fig. 4.18 shows the synchronous divider. In this circuit the signal to be divided is the input of the first flip-flop. All the flip-flops have the same clock and the output of each flip-flop is the input of the succeeding stage. When the division by N is done, the system is reset. The value of N, which could be 3,5,7 and 9, is determined by a decoder.

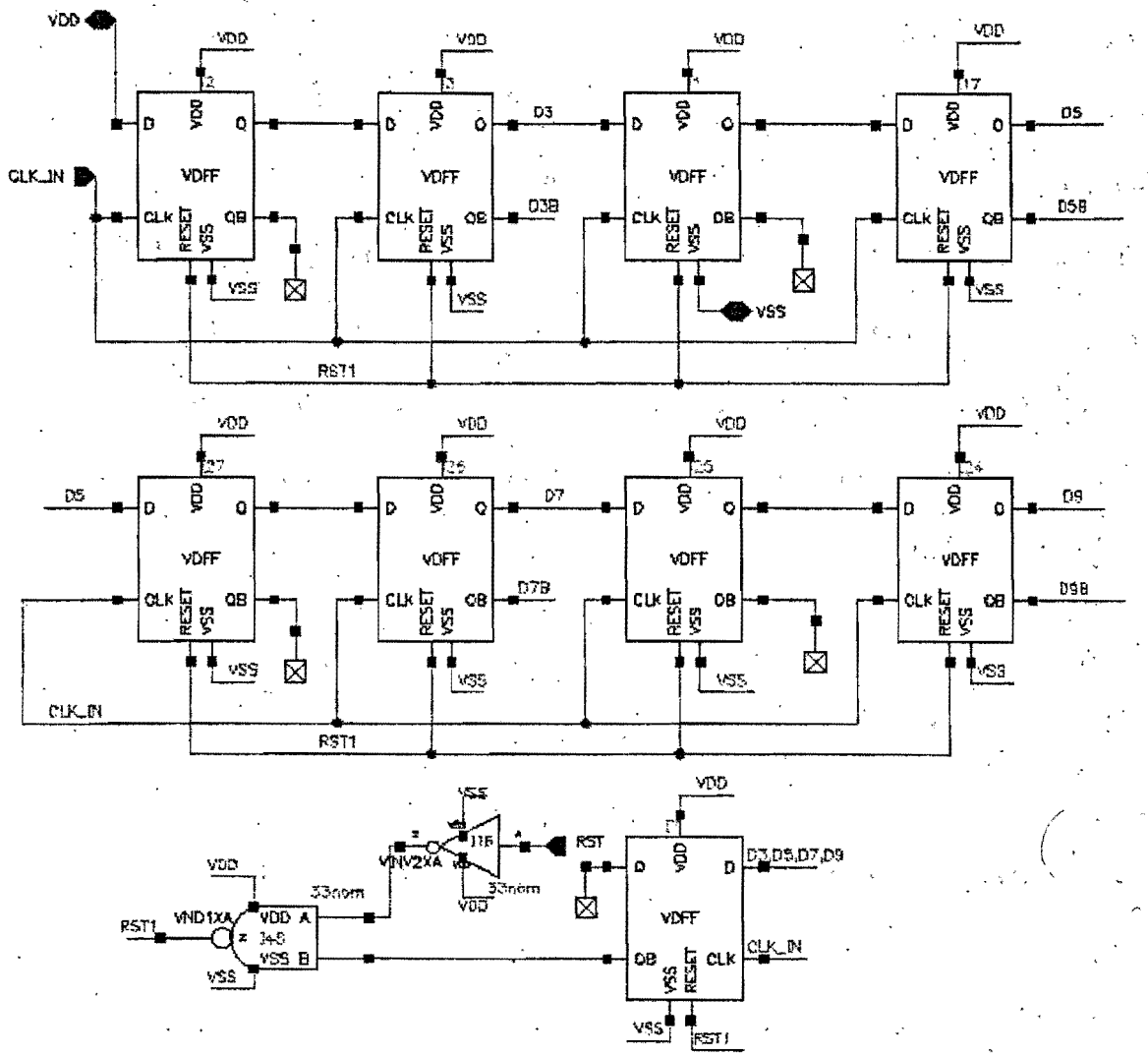

Fig. 4.18 Synchronous divider.

4.3.2 Logic Circuit

The logic circuit is a digital circuit that decides how many chains of delay-cells are in operation. This decision is made by using the outputs of two comparators. Fig. 4.19 shows the core of logic circuit. When the output of one of the comparators changes to logic one, it shows that the controlling voltage has exceeded the absolute value of threshold. Therefore, the number of delay-cell chains should be changed accordingly. Then, the logic circuit checks the number of existing chain and brings in or takes out a chain. At this moment a reset signal is built which brings the controlling voltage to its

common-mode value. Also, a feature has been provided that overrides the number of chains manually. This feature could be used at start-up or for testing the chip.

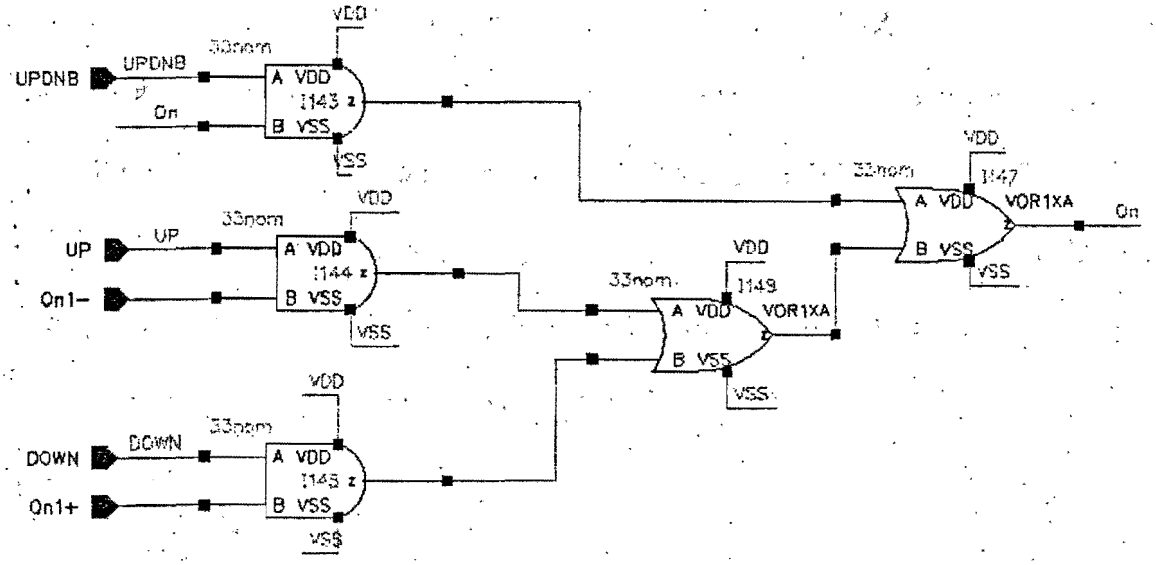

Fig. 4.19 Core of logic circuit.

4.3.3 Comparator

Two comparators are used for determining the points where the controlling voltage exceeds the upper or lower thresholds. Fig. 4.20 shows the basic top-level architecture of the comparator. It consists of a bias circuit, a pre-amplification stage, a track and latch stage and an R-S latch.

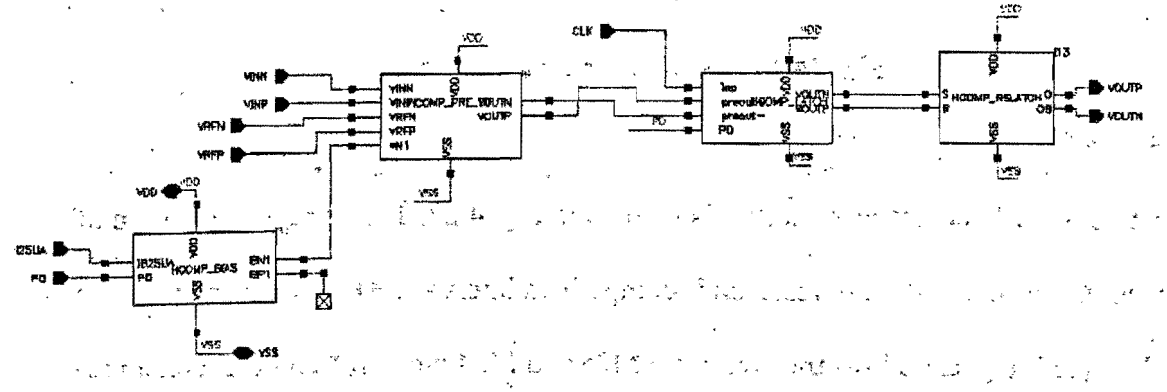

Fig. 4.20 Basic architecture of the comparator.

Shown in Fig. 4.21, is the pre-amplifier configuration. The input signal is fed differentially. The pre-amplifier is used to obtain higher resolution and to minimize the effects of kickback. Kickback refers to the charge transfer either into or out of the inputs when the track and latch stage goes from track mode to latch mode [3].

The output of the pre-amplifier, although larger than the comparator input, is still much smaller than the voltage required to drive digital circuitry. The track and latch stage further amplifies it again during the latch phase, when positive feedback is enabled.

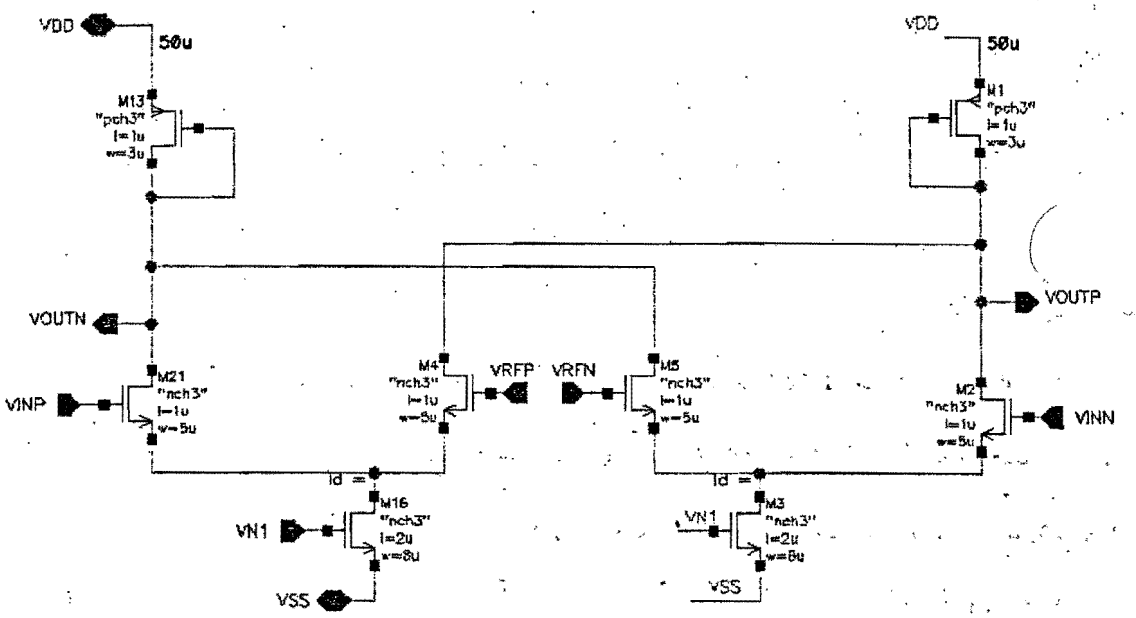

Fig. 4.21 Pre-amplifier configuration.

The track-and-latch stage circuitry is shown in Fig. 4.22. The dynamic operation of this circuit is divided into reset and comparison intervals. At the reset interval, the clock ("inc" signal) is low, transfer gates M25 and M24 are "off " and p-channel pre-charge transistors M18 and M21 are "on". Therefore, both the p-channel flip-flop nodes, formed by M19 and M20, are charged up to power-supply voltage level and n-

channel Flip-Flop nodes, formed by M24 and M25, are discharged to ground level through n-channel discharge transistors. When the clock goes high, charging current starts to flow from the p-channel side to the n-channel Flip-Flop. A part of the current is discharged through discharge transistors M26 and M27, whose gates are controlled by the differential amplifier. Since these two discharge transistors have different currents, a large voltage difference is obtained when the n-channel flip-flop drain voltages exceed the threshold voltage. The amplified difference is transferred to the p-channel flip-flop, and is amplified to a voltage swing nearly equal to the power supply voltage [21].

The output of the track-and-latch circuit is fed to the R-S latch during the clock period. Fig. 4.23 shows the R-S latch.

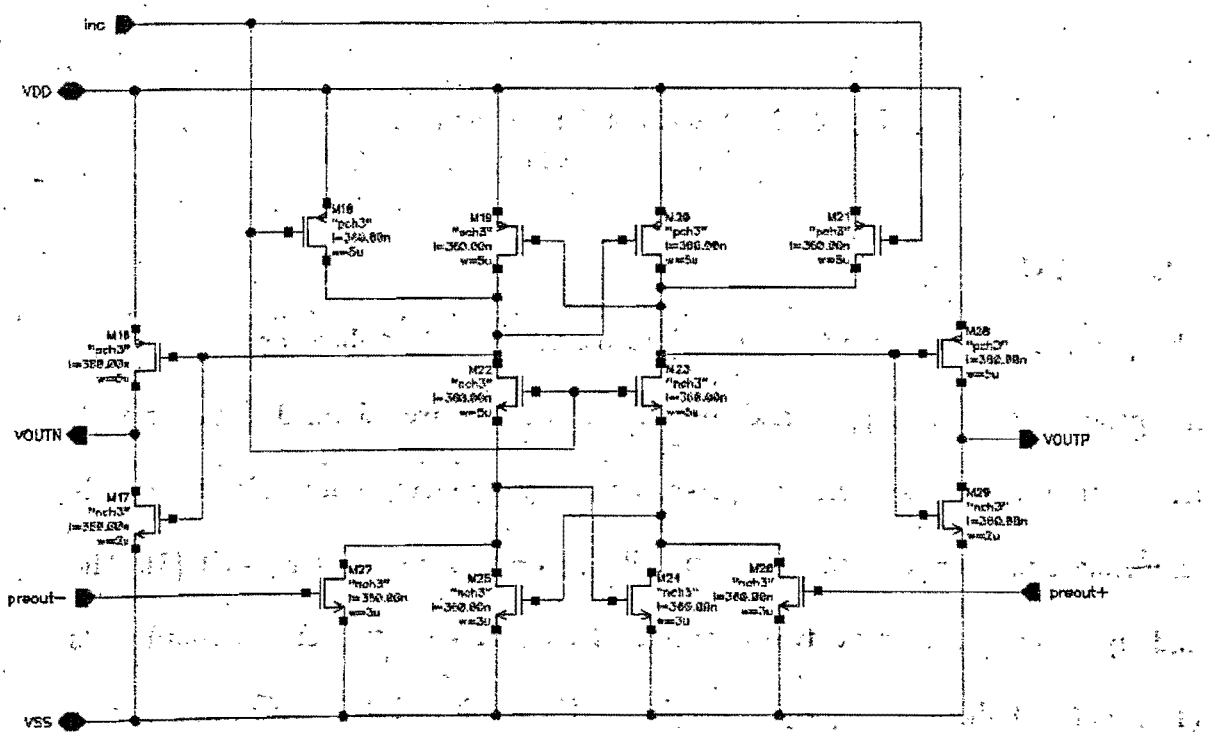

Fig. 4.22 Track-and-latch stage.

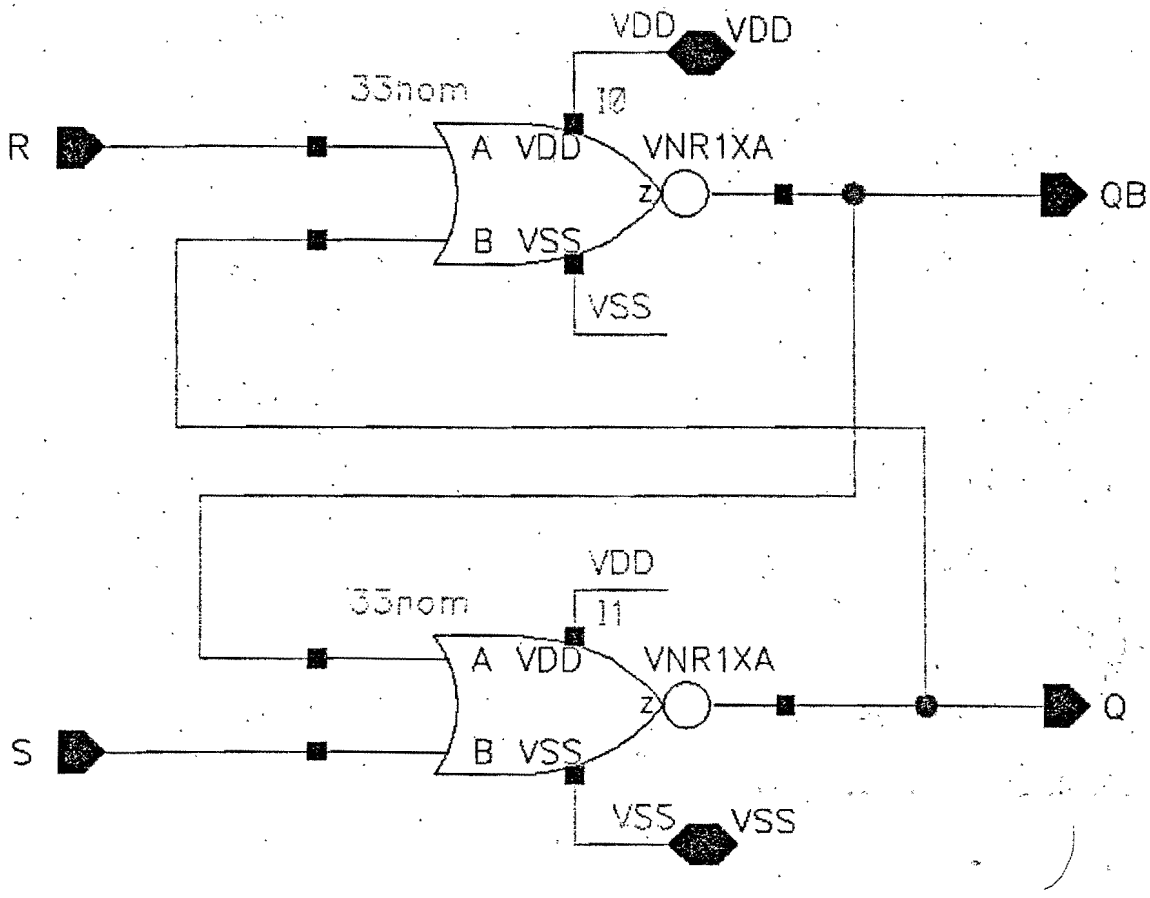

Fig. 4.23 R-S latch of the comparator.

4.3.4 Band-Gap Circuit

The purpose of reference voltage circuit is to establish a DC voltage or current that is independent of the supply and process and has a well-defined behavior with temperature. Since most process parameters vary with temperature, if a reference is temperature-independent, then it is usually process independent as well [3]. The underlying idea is to have two quantities having opposite temperature coefficients (TC) and add them with proper weighting. The result will show a zero temperature coefficient.

Bipolar transistors have proven to provide the most reproducible and well-defined quantities that can provide positive and negative TCs. Even though many parameters

of MOS devices have been considered for the task of reference generation, bipolar operation still forms the core of such circuits [3].

The base-emitter voltage of bipolar transistors or, more generally, the forward voltage of a pn-junction diode exhibits a negative TC. For a bipolar device we can write:

$$I_C = I_S \exp(V_{BE}/V_T),$$

where $V_T = KT/q$.

It can be shown that with $V_{BE} \cong 750mV$ and $T = 300°$ K, $dV_{BE}/dT \cong -1.5mV/°$ K [3].

It was recognized that if two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages is directly proportional to the absolute temperature [3]. As shown in Fig. 4.24, if two identical transistors ($I_{S1} = I_{S2}$) are biased at collector currents of nI_0 and I_0 and their base currents are negligible, then:

$$\Delta V_{BE} = V_{BE1} - V_{BE2},$$

$$\Delta V_{BE} = V_T \ln (nI_0/I_{S1}) - V_T \ln (I_0/I_{S2}),$$

$$\Delta V_{BE} = V_T \ln (n).$$

Therefore, the V_{BE} difference has a positive temperature coefficient;

$$dV_{BE}/dT = K/q \ln (n).$$

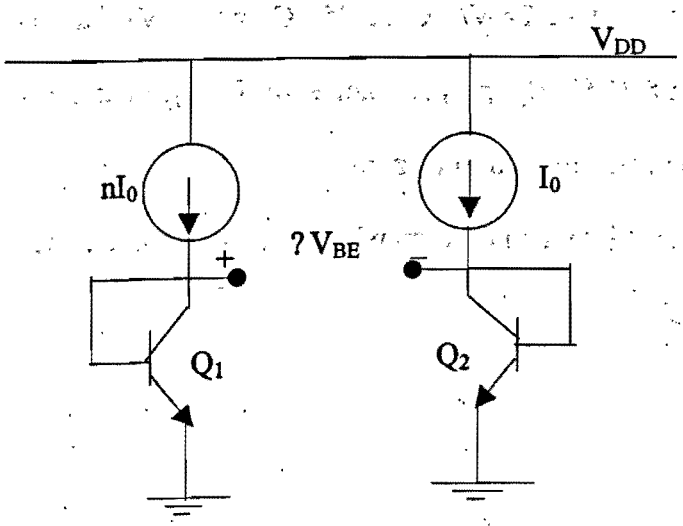

Fig. 4.24 Generation of positive temperature coefficient [3].

The core of the band-gap circuit is shown in Fig. 4.25 [22]. The low-temperature coefficient of the bandgap voltage is obtained by addition of a negative temperature coefficient (TC) base-emitter voltage of a bipolar transistor, with a positive TC voltage obtained from the difference of two base-emitter voltages biased at different current densities.

The supply independence as well as the temperature independence are achieved by a feedback mechanism that forces node 2 in Fig. 4.25 to be at the same potential as node 1. This simultaneously ensures that I_{M2} is an accurate copy of I_{M1}.

From Fig. 4.25 we can write

$$V_{BG} = V_{BE2} + NI * R_2. \tag{4.1}$$

Since nodes 1 and 2 are at the same potential, we can write:

$$V_{BE1} + I*R_1 = V_{BE2},$$

$$V_T \ln (I/(M*I_0)) + I*R_1 = V_T \ln ((N+1)I/I_0),$$

$$V_T \ln (1/(M*(N+1)) = -I*R_1. \tag{4.2}$$

Deriving "I" from Eq.(4.2) and substituting it in Eq. (4.1) yields

$$V_{BG} = V_{BE2} + N*V_T \ln [1/(M*(N+1))*(R_2/R_1)].$$

V_{BE2} has a temperature coefficient of –2.2mV/° C at 25° C, while V_T has a temperature coefficient of +0.085 mV/° C. By proper choice of R_2/R_1, M and N, temperature coefficient of V_{BG} can be compensated to be zero.

The band-gap core circuit is accompanied with an op-amp which is used to force node 1 to be at the same potential as node 2.

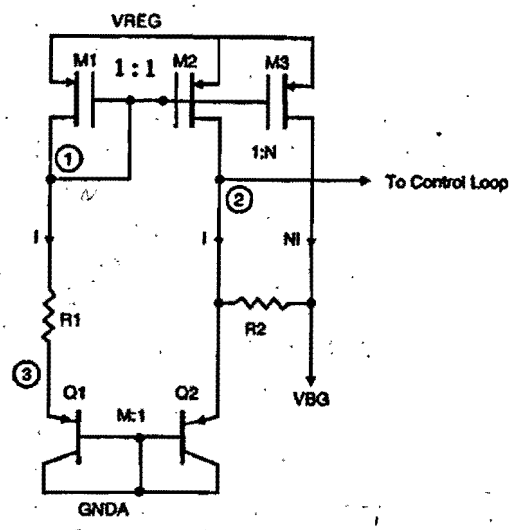

Fig. 4.25 Core of the band-gap circuit [22].

4.3.5 Voltage Reference Circuit

In order to provide thresholds of controlling voltages of the VCO a voltage reference block is needed. These threshold voltages are fed to the comparators. Fig. 4.26 shows the top-level circuit of the voltage reference block.

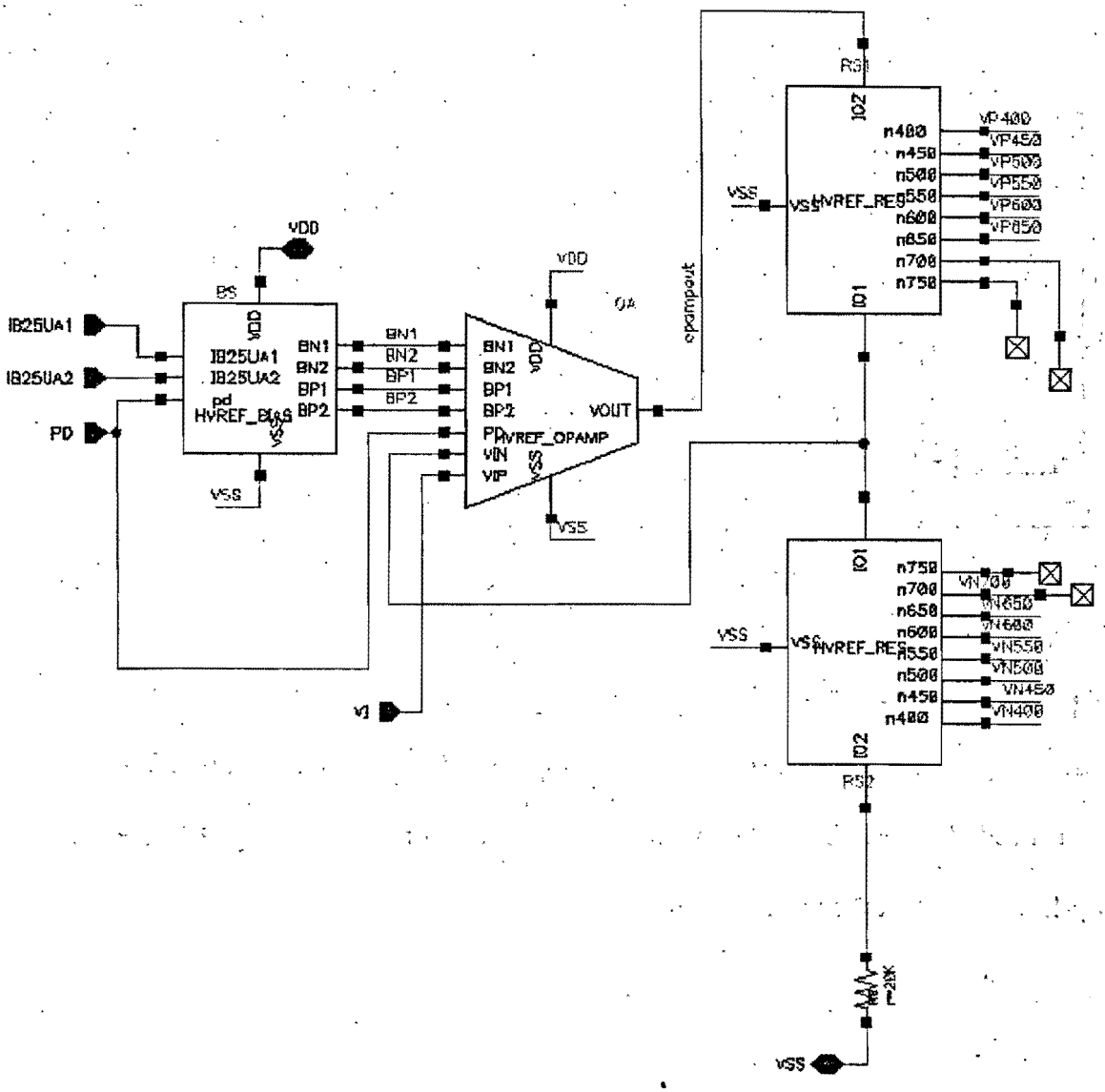

Fig. 4.26 Top-level of the voltage reference block.

This block is made of a bias circuit, a folded-cascode op-amp, and a string of the resistors. The reference voltage built in the band-gap circuit is fed to the positive input of the folded-cascode op-amp. A negative feedback dictates a constant voltage at the resistor based voltage divider. This voltage divider, the string of the resistors, allows us to have specified quantized reference voltages.

A combination of a multiplexer and a decoder is used to add programmability to the threshold voltages, in order to be able to check the functionality of the system with different threshold voltages during the test mode of the chip.

4.3.6 Current Reference Circuit

We need a precise 25-uA current for different parts of the circuit, such as bias circuits. This current is made available in a current reference block. Fig. 4.27 shows the top-level circuit of this block.

This block is self biased and consists of a two-stage op-amp (a p-type differential op-amp followed by a common-source output stage) and a feedback loop which forces a constant current to flow in an external resistor. This constant current is mirrored in several branches to be used in different parts of the system.

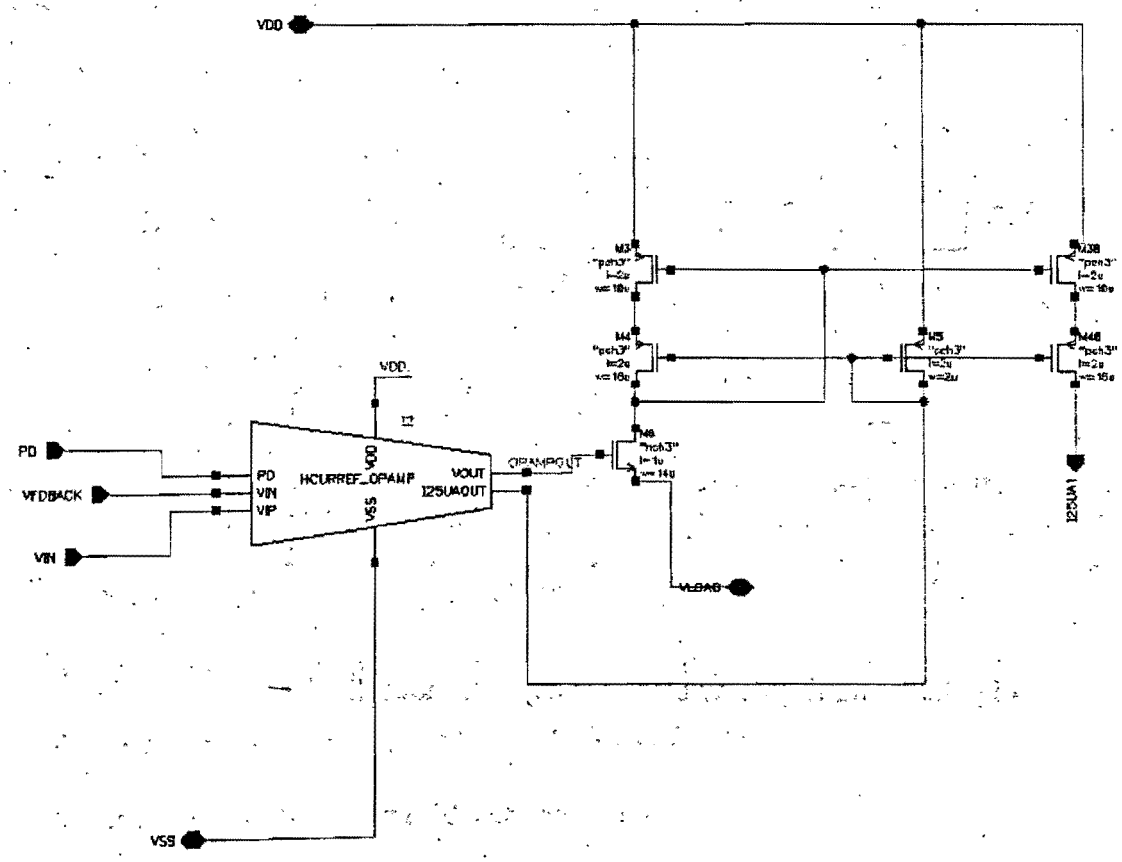

Fig. 4.27 Top-level circuit of the current reference block.

4.3.7 Aligning Delay Blocks

As the output frequency is divided by N in the divider, before being compared with the input reference clock, we have to consider the delay resulted from this division in order to align the input reference clock and the output. For this purpose, two delay cells have been built, in order to copy the delays applied by the asynchronous and the synchronous dividers. Figs. 4.28 and 4.29 show the circuits which copy the delay applied by the asynchronous divider and the synchronous divider respectively. This block, titled "HINDELAY" in the diagram, copies the delay of a Flip-Flop.

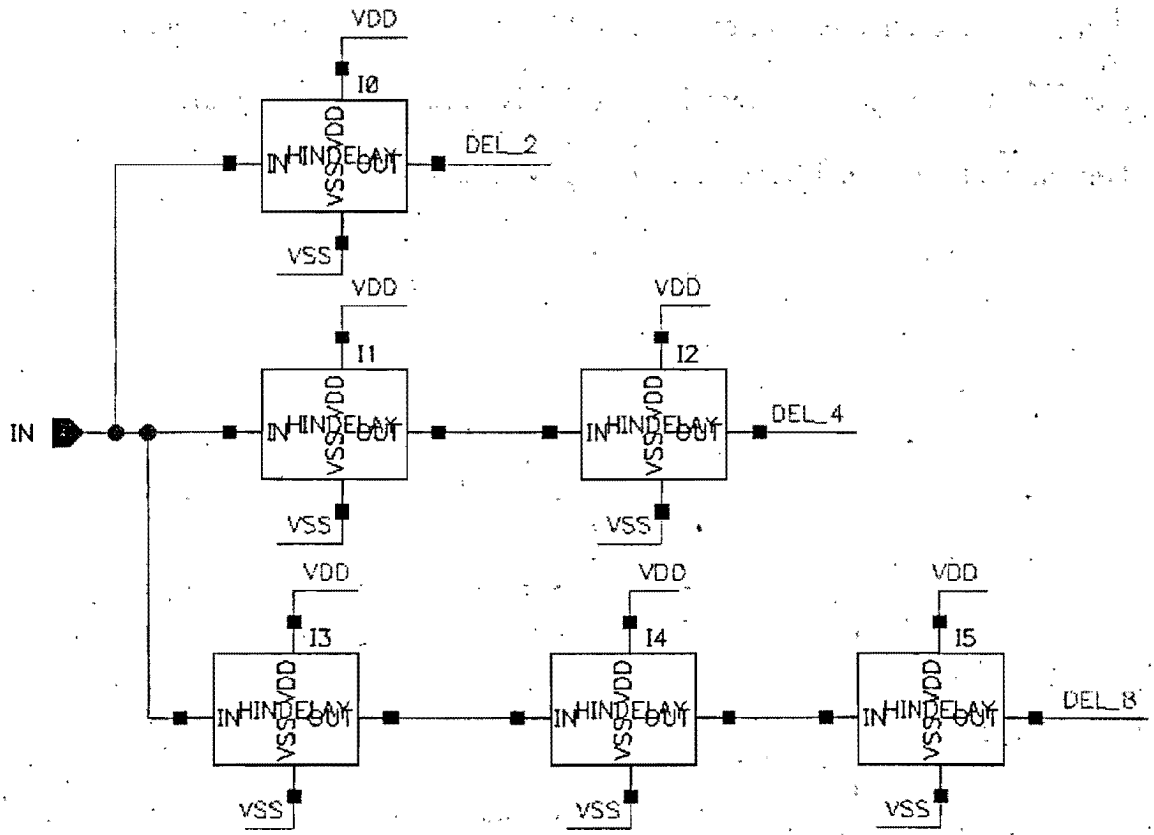

Fig. 4.28 Aligning delay block for asynchronous divider.

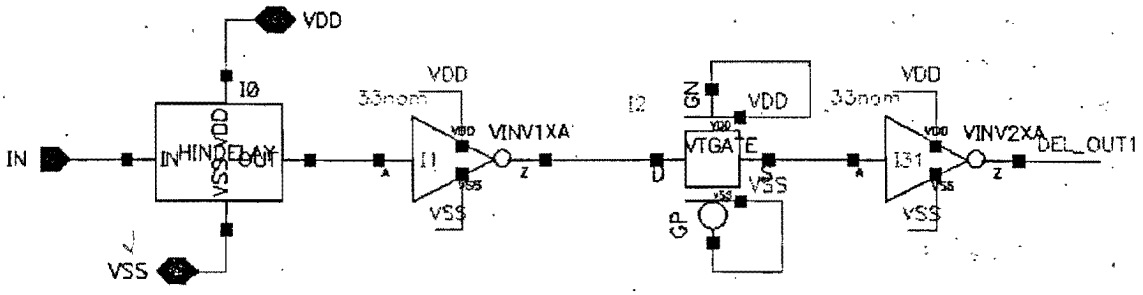

Fig. 4.29 Aligning delay block for synchronous divider.

4.4 Testability of the Chip

In order to improve the testability of the design, it is required to be able to force different blocks from outside and look at the output of different nodes. In this way, in the test mode we can see how the performance of each block in the real chip measures up with the desired specifications defined in the design

The following features have been added to the system to facilitate the testability of the chip:

1. Forcing signals from outside to the inputs of the PFD: It is possible to feed the PFD from outside. Therefore, if there is any problem in the loop, the loop can be broken and two inputs will be forced from outside to the PFD and the functionality of a part of the loop will be checked.
2. Manual control on the number of delay cell chains: The number of delay cell chains can be determined from outside the chip. This feature is used either at the initial point of operation or for the test purposes.
3. Forcing signals from outside to the inputs of the charge-pump.
4. Forcing the controlling voltage of the VCO from outside.
5. Bringing out the output of the charge pump
6. Bringing out the six clocks with different phases.
7. Bringing out the clock and the inverted clock.

8. Power down feature for the whole loop.

4.5 Extra Features of the Design

The followings are some extra features provided in making the designed PLL as general-purpose and as testable.

1. Since no MIM capacitor has been considered in digital technology, all capacitors required in the design for low-pass filter and for compensation of different op-amps have been built with transistors and no MIM capacitors has been used. This is consistent with our goal to build a PLL that can be fabricated with both digital and mixed-mode technology.

2. An option has been provided so that the chip could also use the 25uA current built by the band-gap as the reference-current. By using this option the system doesn't need any external component. This is also another feature that makes the PLL appropriate for any design when there is no chance for adding external component.

3. As already mentioned in Section 4.3.5, four options have been considered for the controlling voltage thresholds.

4. There are three options for the resistors used in the low-pass filter. The default is R=4K. However, we have two other options: we can make the resistor half size or double it in order to test the functionality of the circuit in different situations.

5. Three options have been considered for providing the reference DC current (25uA): (a) The precise current generated by our reference current circuit, (b) The current generated by the band-gap reference, or (c) A reference current from outside. The third option is for the situation that the PLL comes along with another block that already has a reference current. Therefore, the PLL can use the same reference current that the other block does.

Chapter 5

Simulation Results and Layout

The results of simulation for some of the major blocks of the chip are shown and discussed in this chapter. Layout issues of the chip are also explained.

5.1 Simulation Results for Some Major Blocks

5.1.1 VCO Simulation

VCO was the first block to be designed. VCO transfer function over the whole range is shown in Fig. 5.1. It can be seen that there is 20% overlap between each two successive sub-ranges.

The threshold voltages are considered to be –500mv to +600mv (though it is programmable and can be changed during testing) so that only the linear part of the range will be used. As it can be seen in the Fig. 5.1 the gain is constant for all sub-ranges. Let us compare this result with the result that Brynjolfson and Zilic [8] have reported (Fig. 5.2) for programmability by changing the number of inverters. One can see that in their diagram the VCO gain doesn't remain constant when the number of inverters is changed. This change in VCO gain will affect the dynamics of the loop. Moreover, for high frequencies the VCO gain is high and the system is prone to noise. The proposed design, therefore, has advantage in this respect over theirs.

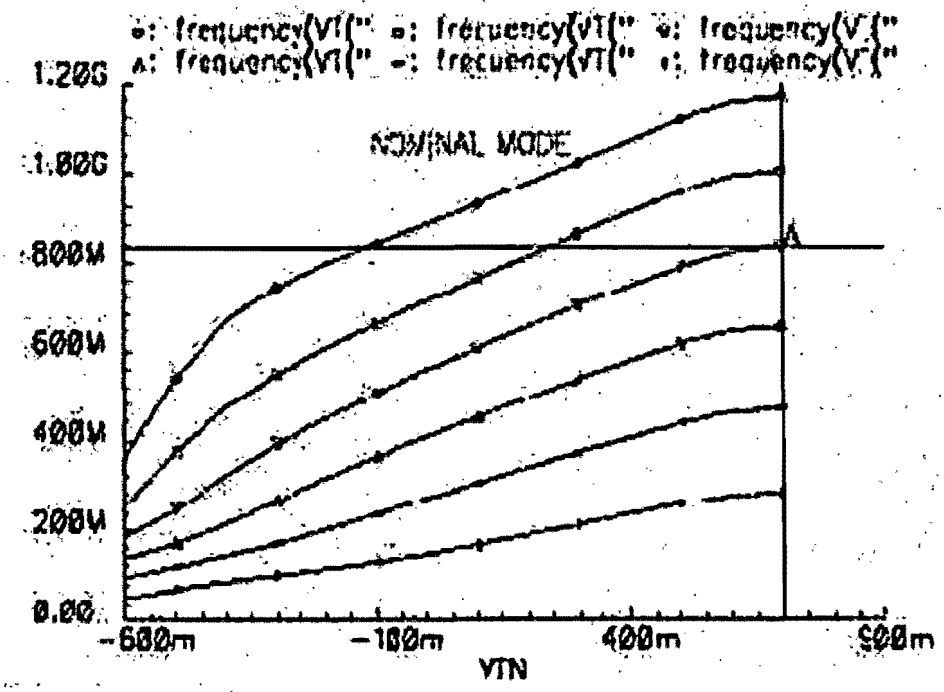

Fig. 5.1 Transfer function of the VCO over the whole range (frequency versus controlling voltage in mV).

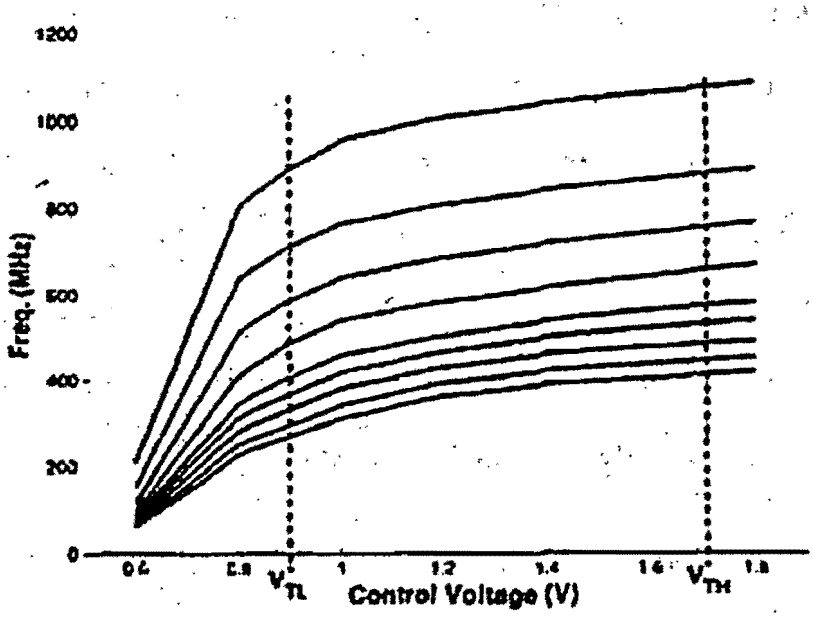

Fig. 5.2 The transfer function of the VCO suggested by Brynjolfson and Zilic [8].

5.1.2 Phase-Frequency Detector

Fig. 5.3 shows the result of the simulation for phase-frequency detector circuit. This result is for the situation that the oscillator frequency is ahead of the reference frequency. Therefore, at the rising edge of this signal the "DOWN" signal becomes logic one and shows that the output frequency should be lowered to match the reference frequency. This signal will stay high until the rising-edge of the reference frequency appears. At this time both " DOWN" and "UP" signal will reset.

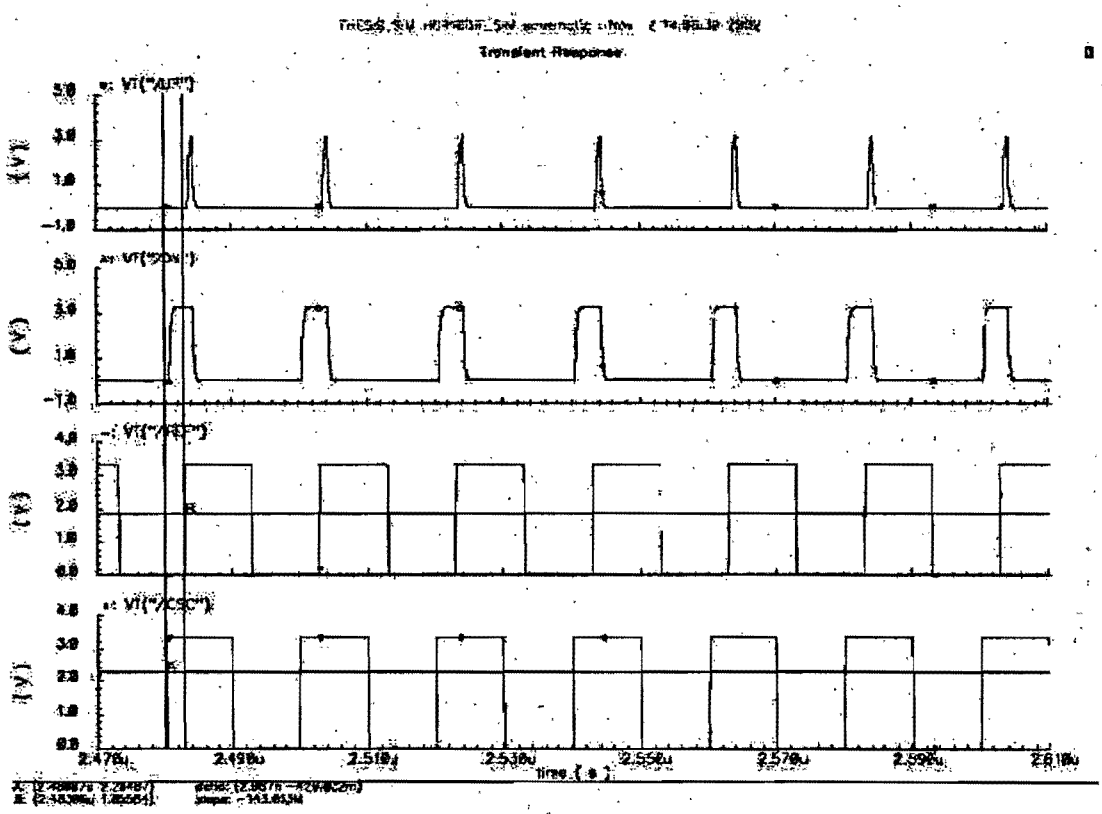

Fig. 5.3 Phase-frequency detector simulation.

5.2 MATLAB Simulation Result

After simulating each single block the whole loop was simulated in MATLAB with Simulink in order to optimize the filter components and check the stability of the loop for both extremes of the ranges. Fig. 5.4 shows the diagram of the system in Simulink. Shown in Fig. 5.5 is the loop behavior for dividing factor N=4. Calculations based on the loop transfer function derived in Chapter 2 shows that for N=4 and with charge-pump current of 50 uA the damping ratio is equal to 1.1 and hence the system is stable. The number of rings in the simulation result of Fig. 5.5 confirms the stability of the designed system.

The frequency response of the PLL was derived in MATLAB. Figs. 5.6 and 5.7 show the transfer function of the PLL for N=4 and N=20 respectively. The ω_{-3dB} and, hence, the bandwidth of the PLL for these two dividing factors are $3*10^6$ and $6*10^6$

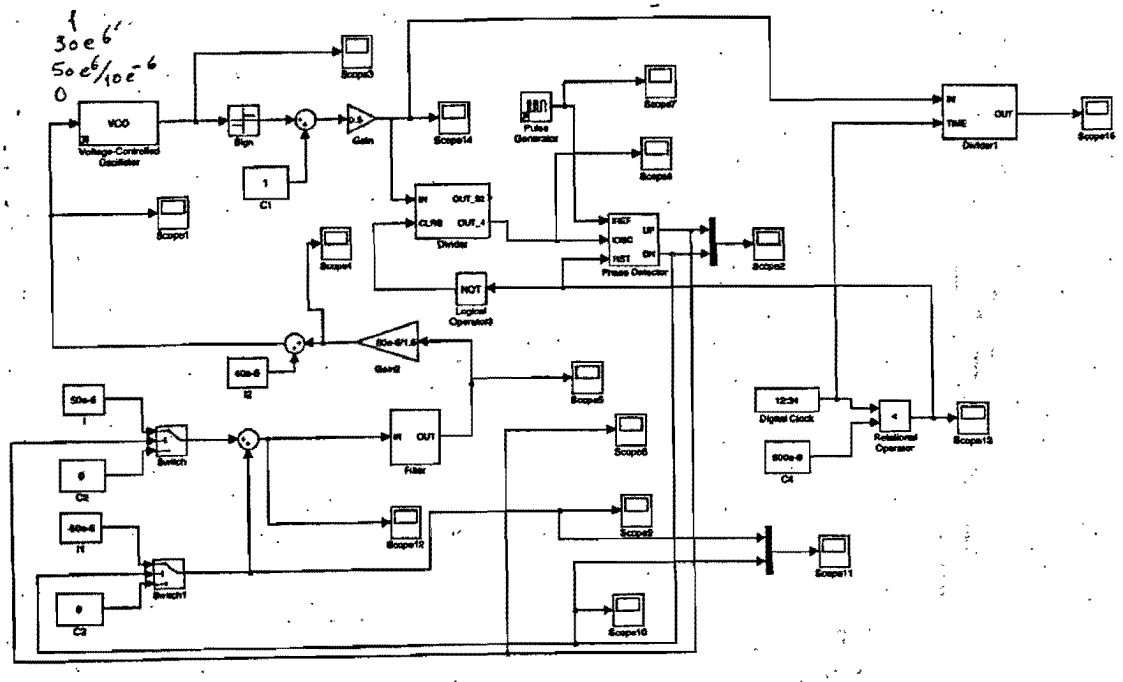

Fig. 5.4 System level schematic in Simulink.

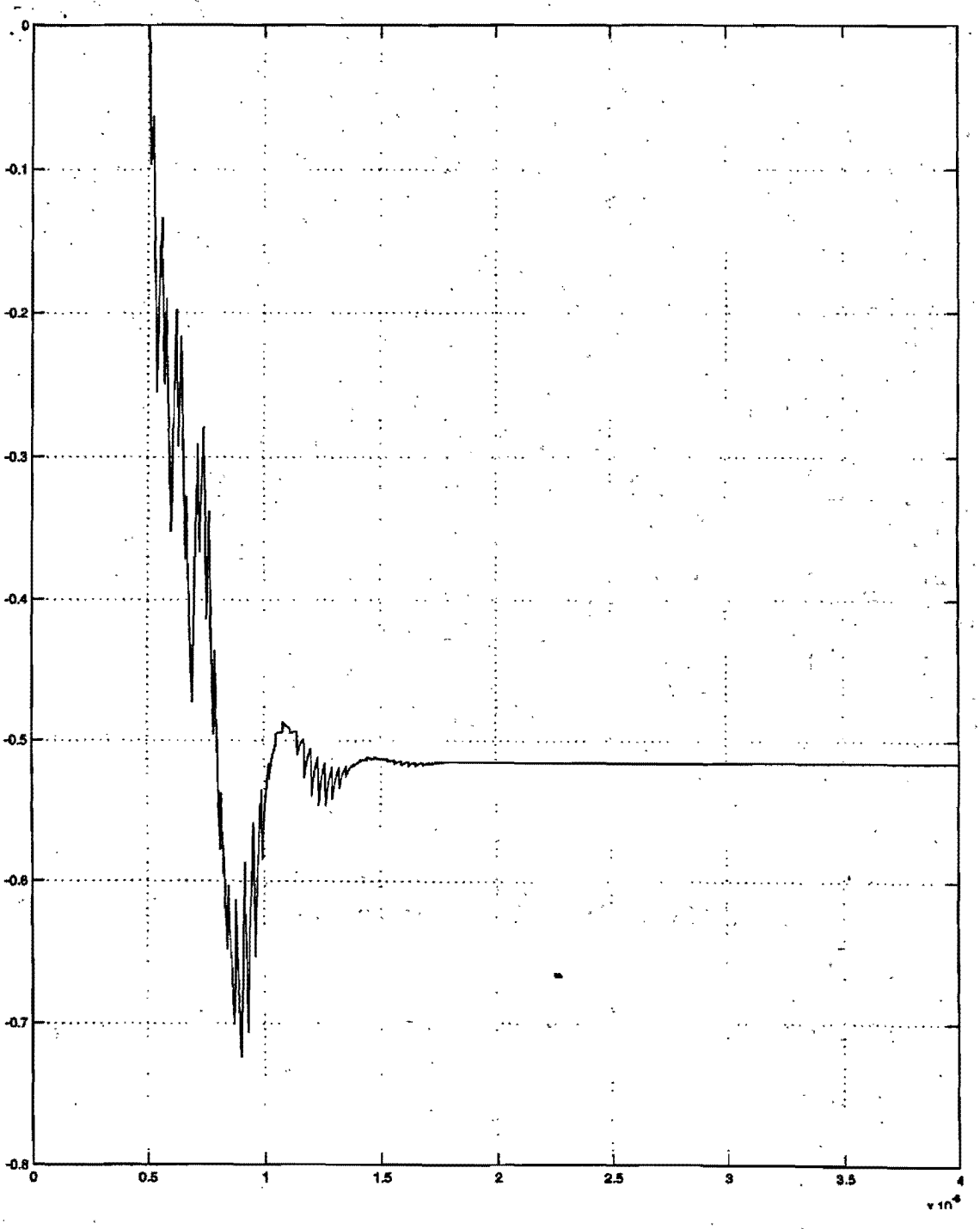

Fig. 5.5 Loop behavior in Simulink for the dividing factor N=4 Low-pass output voltage (V) versus time (us).

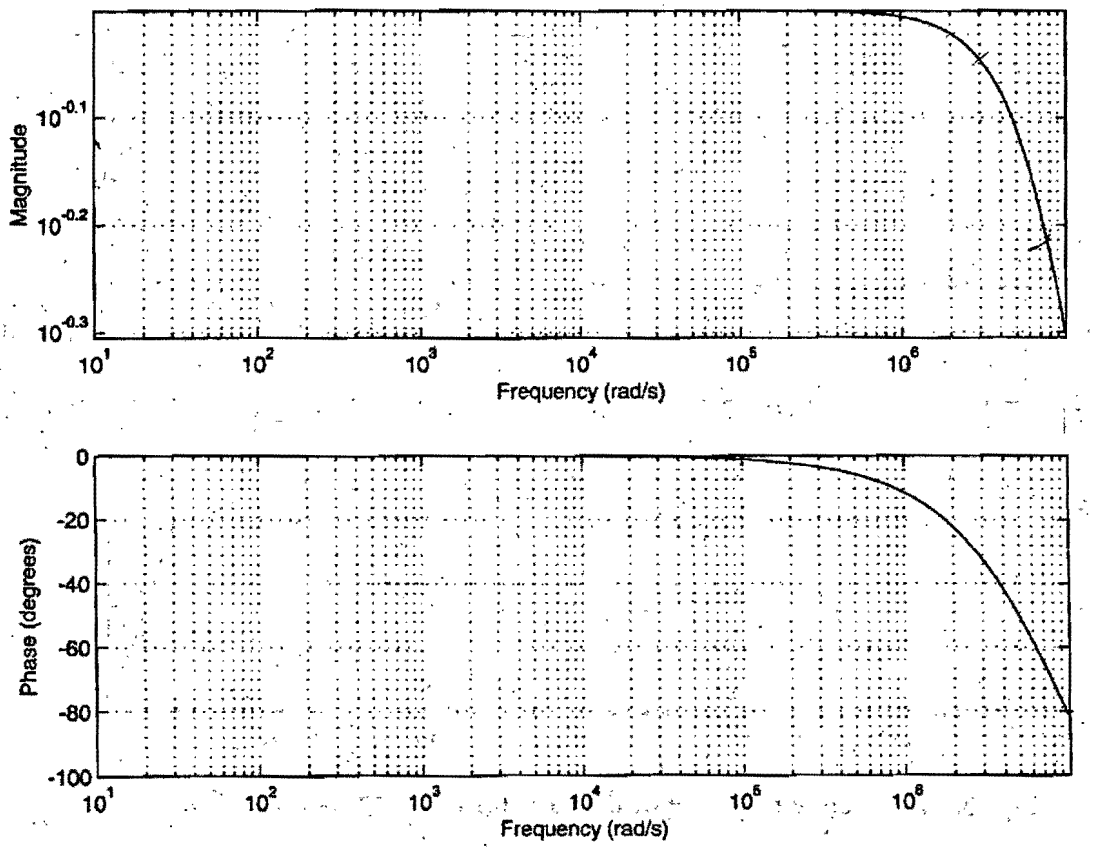

Fig. 5.6 Frequency response of the PLL for dividing factor N=4.

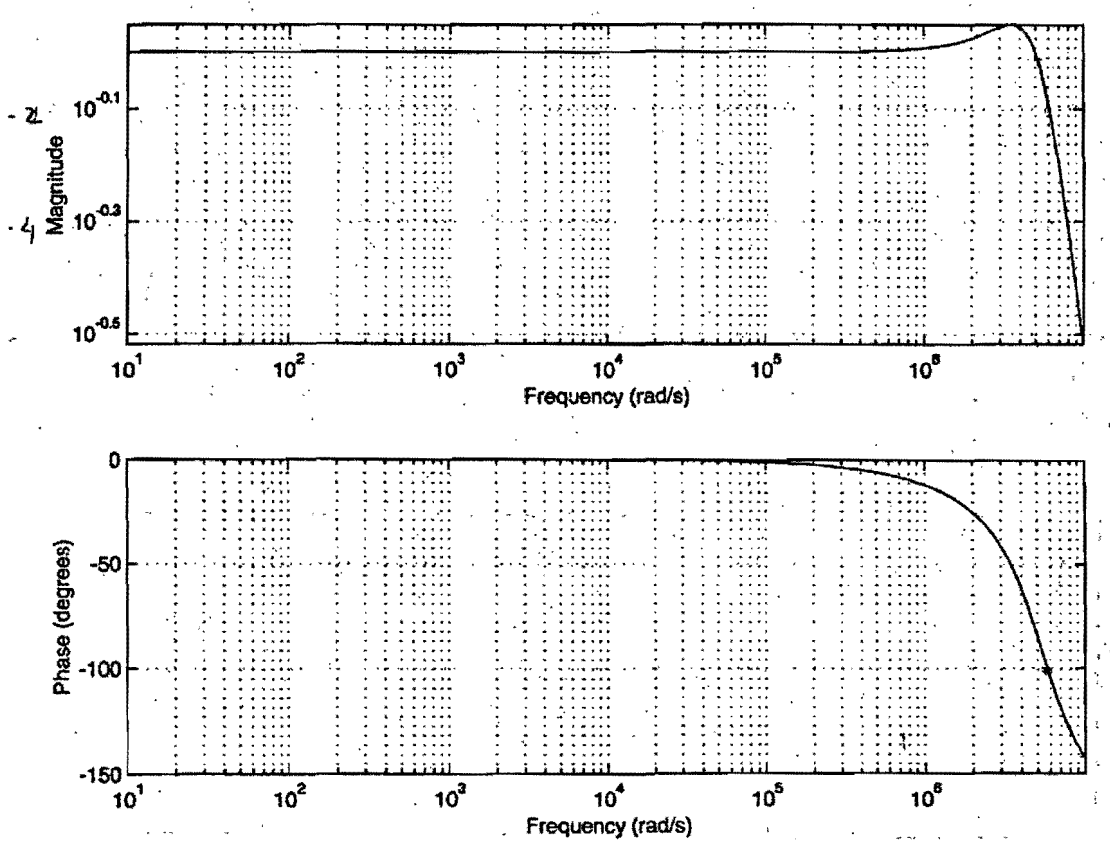

Fig. 5.7 Frequency response of the PLL for dividing factor N=20.

5.3 PLL Loop Simulation

The whole loop was simulated in CADENCE environment for both extremes of the range and for the frequencies in between. A 2pF capacitive load has been considered at the output of the PLL in order to consider the output load effects in the simulation. A15fF capacitor has been added for simulating the routing capacitance effect. The results of the simulation are discussed next.

Figure 5.8 shows the VCO output. We can see that the output, as expected, is a rail-to-rail signal. Figure 5.9 is the output of the charge-pump and the low-pass filter. This voltage is the base of comparison. We can see that the system decides on the number of delay-cells chains twice before the system reached to a lock condition.

Fig. 5.10 shows the output signal of PLL for 1GHz frequency. Shown in Fig. 5.11 is the dividers response. One can see that the duty cycle of the synchronous divider

output is not 50%. However, as the PFD responds to the rising edge this imperfect duty cycle doesn't cause any problem.

Fig. 5.12 shows the jitter of the system for 10mV (rms) random supply noise. It is attained by sweeping the output by a sawtooth signal generator. For 1GHz frequency the amount of jitter is seen to be 1ps peak-to-peak.

Finally, Fig. 5.13 shows the phase difference between input and output signals in the lock condition. It should be mentioned that the input pad delay has not been considered in this measurement.

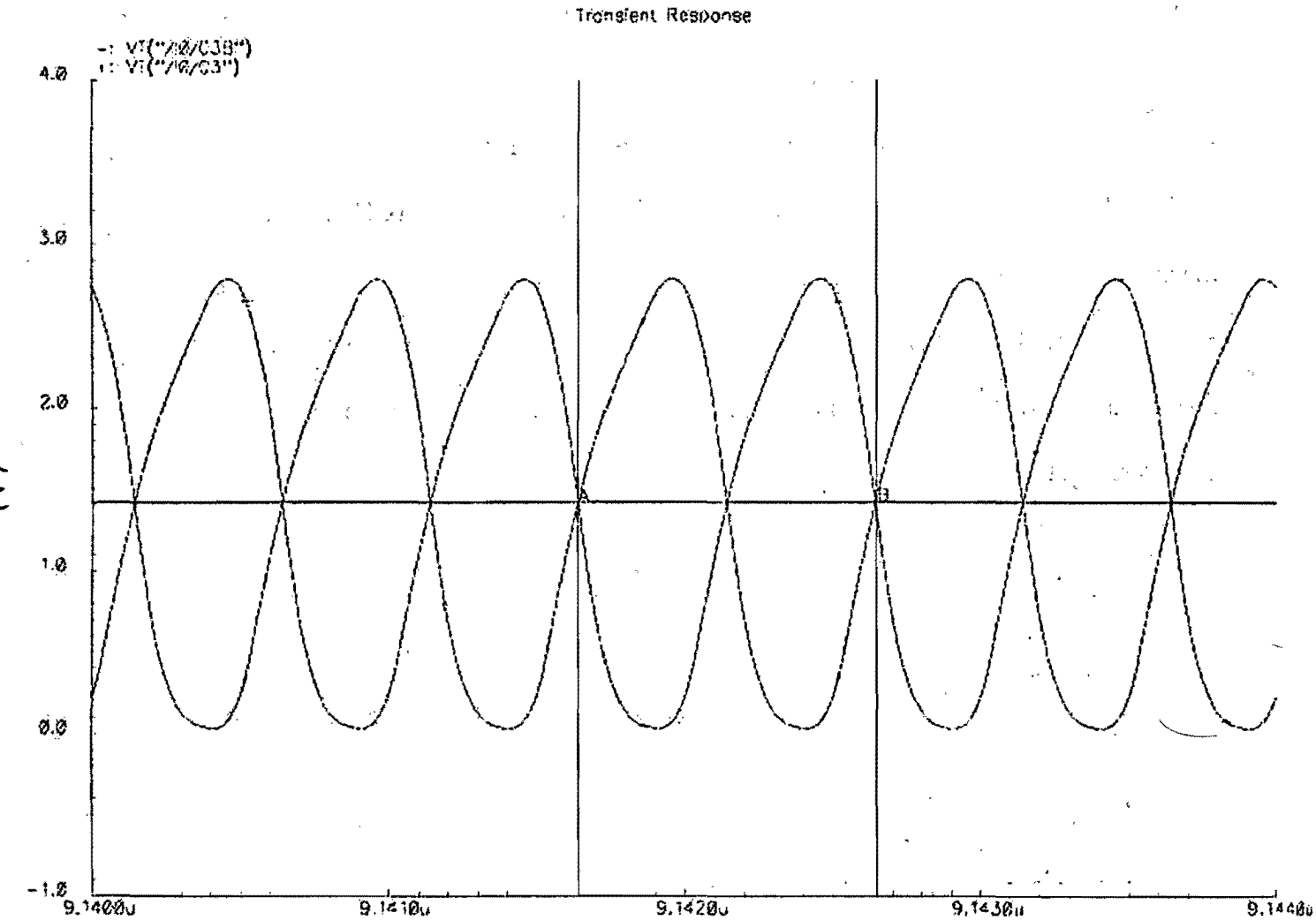

Fig. 5.8 VCO output signal.

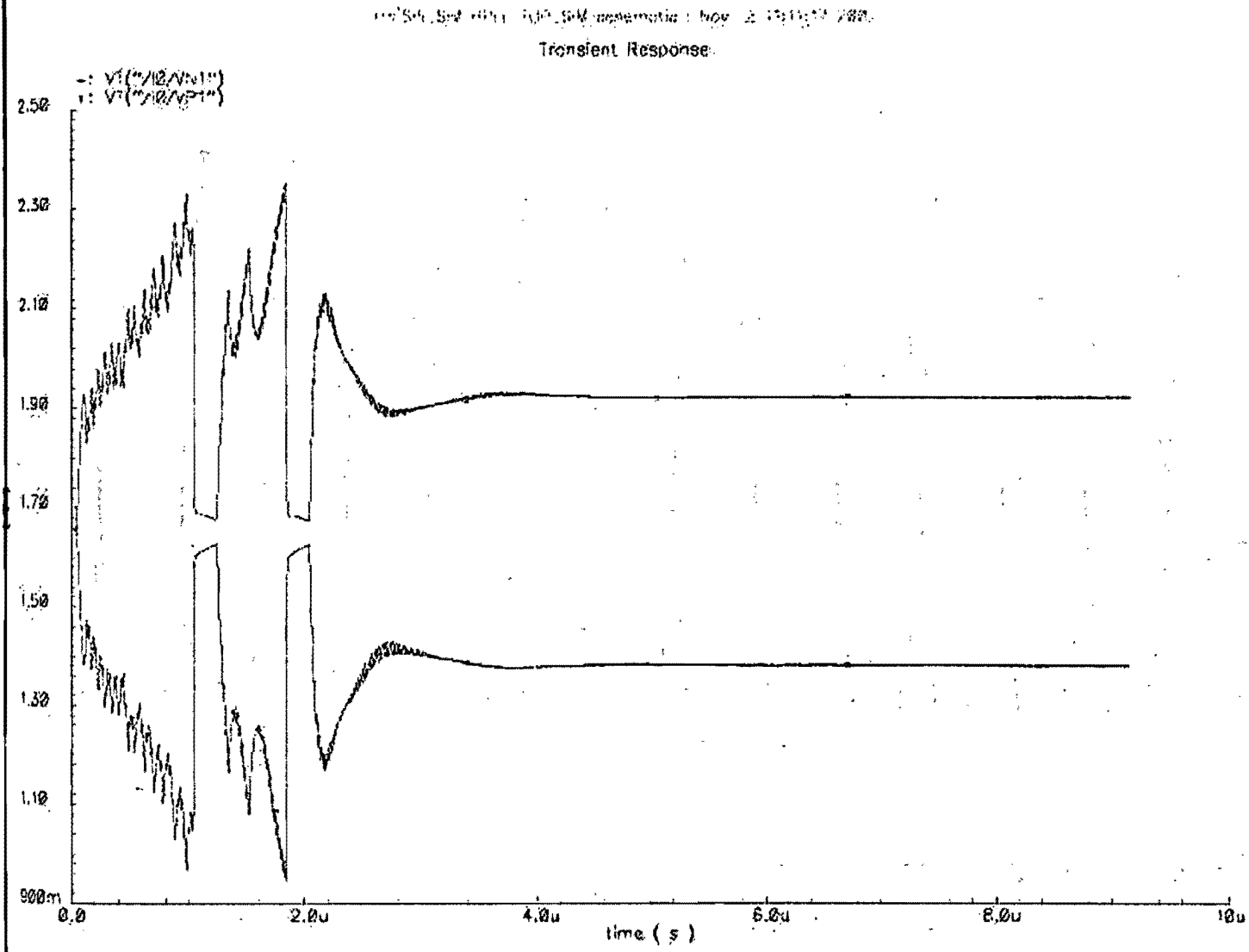

Fig. 5.9 The output of the charge-pump and the low-pass filter.

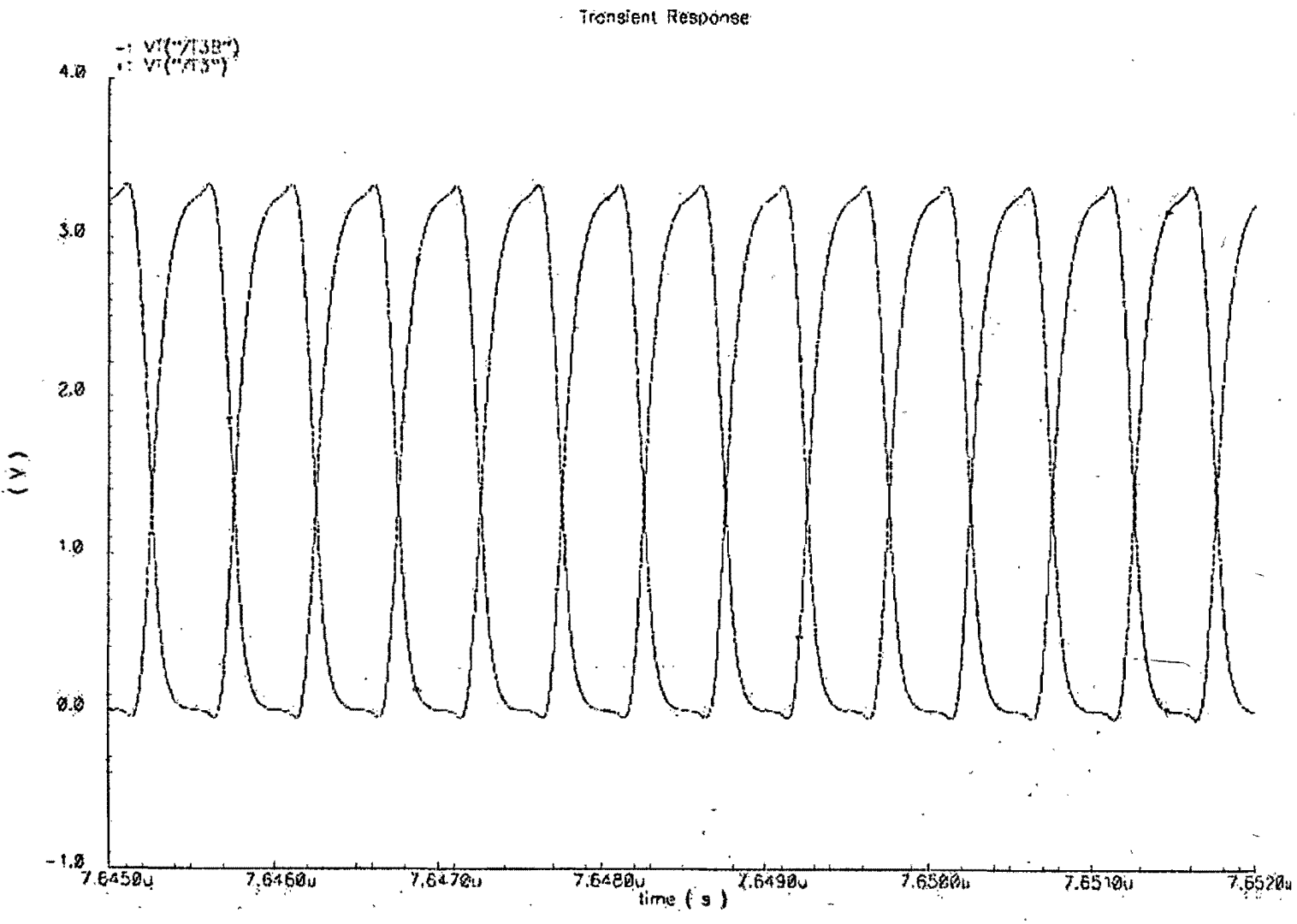

Fig. 5.10 The output signal of PLL for 1GHz.

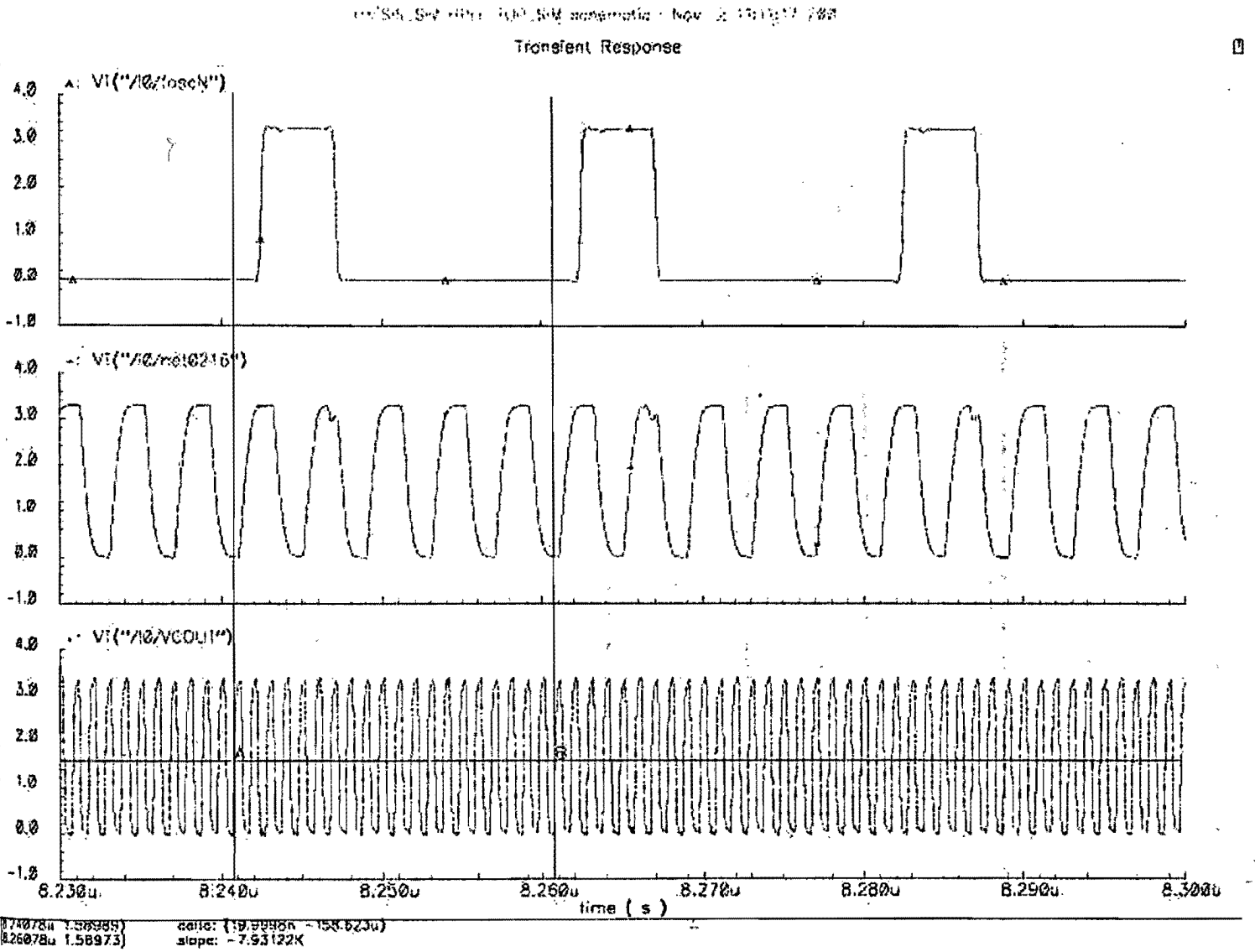

Fig. 5.11 The dividers response.

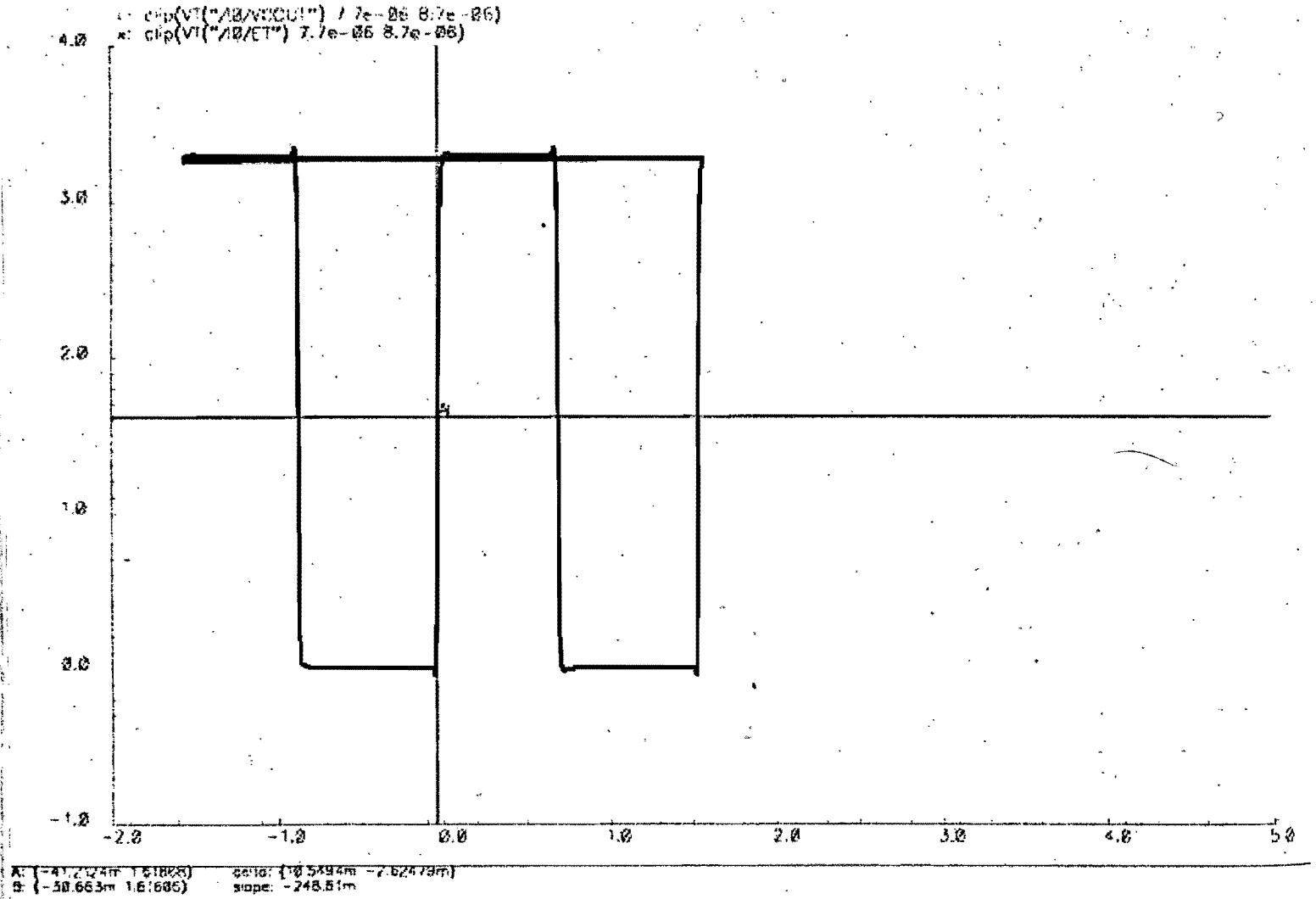

Fig. 5.12 The jitter of the system for 10mV (rms) random supply noise.

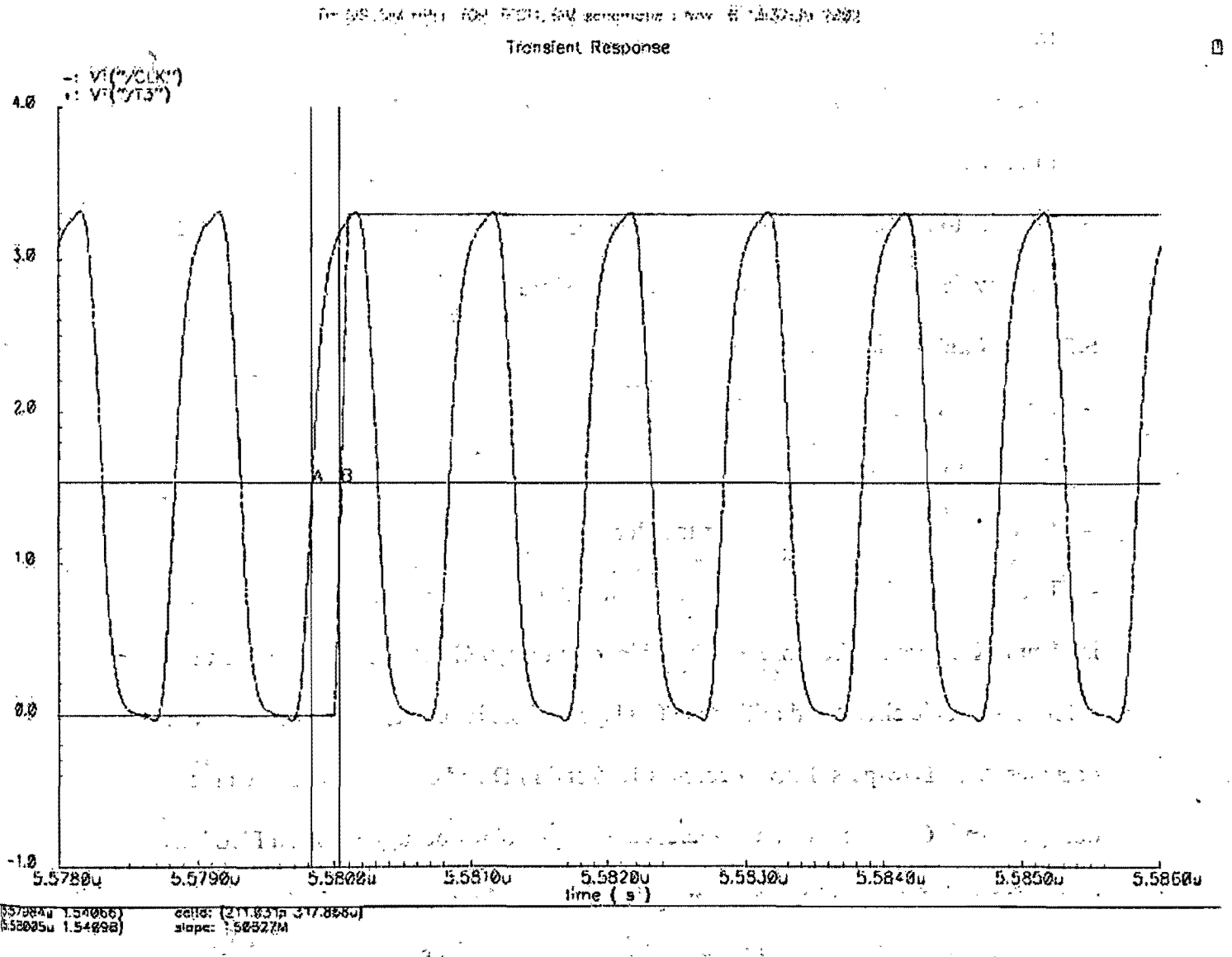

Fig. 5.13 The phase difference between input and output signals in the lock condition.

5.4 Layout Considerations

PLL has been laid out in 0.18u technology. In layout design following aspects have been considered:

- In floor planning stage the blocks were arranged in such a way that the routings between different blocks were minimized.

- Analog blocks and digital blocks were separated and two different supplies were used for them.
- In choosing the width of the routings of signals and supplies the maximum current (or the worst case) was considered.
- Shielding was considered for the VCO and PFD in order to immune these blocks to the noise of other blocks (especially digital blocks).
- In order to minimize mismatching between the transistors that should be matched, dummy devices were added to isolate matched transistors.

5.5 Pads, Package and Chip Size

- I/O buffers and Pads of TSMC library "tpz973g" have been used for connecting the core to the output.
- Package no. 68PGA was used for the chip.
- The chip has 52 pins (13 pins in each side) and its total area (including pads) is1.5mm X1.5 mm. The core of the chip occupies 0.6X0.6 um^2 from which 9% belongs to logic circuit and utilities. VCO layout occupies 0.2%, charge pump layout occupies 8%, Low-pass filter occupies 10% and PFD and dividers and delay blocks occupies 7%. Comparators and reference voltage block occupy 13% and PLL bias circuit occupies 16% of the chip area. Testability and programmability blocks have occupied the remaining space. Figure 2.10 shows the layout of the chip.

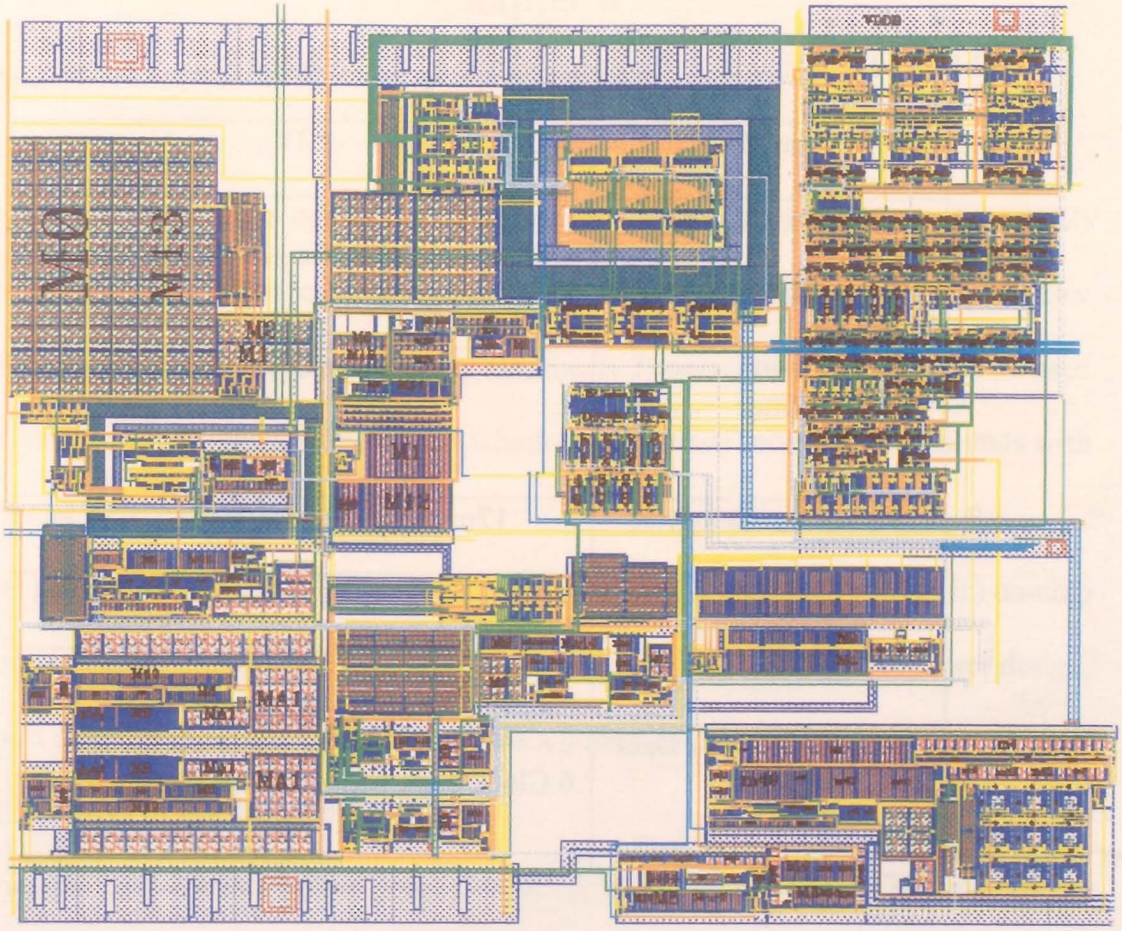

Fig. 5.14 Layout of the PLL core.

5.6 PLL Specifications

The noise of devices has been measured using RF Spectre analysis. The analysis shows the noise is 0.56% p-p

An AHDL block power meter inserted in the route of the main supply has measured power dissipation. The simulation shows 11 mW power dissipation for 100MHz and 17 mW power dissipation for 1GHz. Main figures in specification of the PLL are summarized in Table 5.1

Table 5.1 Main figures in the specification of the designed PLL.

Supply	3.3V
Frequency Tuning Range	100MHz –1GHz
Jitter	Less than1.5 ps P-P (with 10mVrms random noise)
Power Consumption	17mW for 1GHz at V_{DD}= 3.3 V
Output Signal	Rail-to-Rail digital clock
VCO Gain	250 MHz/V
Extra Outputs for Data Recovery	6 Clock Taps with different Phase Offsets

Chapter 6

Conclusion

Phase-locked-loops are one of the main blocks in many system on-a chip (SOC) communication and /or computation blocks. They are used for jitter reduction, skew reduction, data recovery and frequency synthesis. Programmable PLLs could be used for clock management in the chips which include many independent elements with different clock rates.

The goal was to build a general-purpose wide-range (100MHz – 1GHz) on-chip programmable CMOS PLL which is power-efficient, suitable for low-power design, robust against temperature changes and has a good noise rejection.

6.1 Features of the Designed PLL

A simple and robust method was chosen for programmability. In this method the wide-range frequency is partitioned to smaller ranges and these smaller ranges are achieved by changing the driving capability of the voltage-controlled oscillator (VCO). For making the system stable against any temperature change twenty percent overlap has been considered between different partitioned ranges. Any sub-circuit that is not in use will be disabled in order to make the system power-efficient. The design is suitable for low-power applications when there is limitation on supply voltage.

A logic circuit has been added for providing on-chip programmability. Using this method, the system could decide how much driving capability is required for the desired frequency.

Quality performance of the system is due to the novel architecture chosen for the VCO. This architecture along with a compensating circuit (mapper) provides a VCO with a linear transfer function with a constant low-gain for all frequency ranges. This

makes the system less prone to noise. Also, this architecture benefits from fast switching for reducing the noise [6]. The compensating circuit adds an extra advantage which makes the system more robust against temperature changes.

Choosing differential architectures for all sub-blocks (except for the VCO which has a pseudo-differential architecture) provided better noise rejection.

The designed system is a general-purpose PLL which provides a rail-to-rail digital clock signal from a 50-MHz reference clock. The design is implemented with 3.3V supply, while the system is capable of handling 1.8V. The output jitter came out to be 1ps P-P for 1GHz output when 10mVrms random noise was injected in the supply line. The power consumption was 11mW for 100MHz and 17mW for 1GHz.

This PLL is suitable for both analog and digital technology because the required capacitors were built with transistors and no MIM capacitor has been used.

The supply of the digital sub-blocks is separated from the supply of the analog sub-blocks in order to block the switching noise to the analog circuits.

6.2 Layout and Post-Layout Simulation

The PLL was laid out in CMOS 0.18u technology and was verified for design rules and matching with schematics. The total area was 0.6X 0.6 um^2 out of which 48% was for programmability and utility blocks. The results of post-layout simulations were in reasonable consistency with those found in the design process.

6.3 Comparison

Table 6.1 shows the simulation results of the implemented PLL along with the results reported for some of the recent wide-range and/or programmable PLLs. The table shows the advantages of the proposed PLL over its counterparts: VCO low gain which is constant over the whole range, VCO linear transfer function, on-chip programmability and small area.

Author	Programming style	On-chip Program -mability	VCO Frequency range	VCO gain	VCO transfer function	Power Dissipation mW	Supply	Process um	Chip Area mm^2
Rhee [5] (VCO only)	Programming loading capacitors	No	54M-1G	430M/V worst case(Diagram)	Linear ,but variable	3.5 (VCO only)	2.5V	0.35	--------
Sutoh [10]	Programming NO. of inverter stages	yes	5M-400M	400M/V (diagram)	nonlinear	13.7	2V	0.25	0.14
Sung [4]	Enlarging driving capability	Yes	75M-1G	430M/V	Linear and constant	92	3.3V	0.6	1.05
Chen [20]	Programming driving capabilities	No	103M-1.02G	271M/V	nonlinear	4.52	1.8V	0.35	0.16
Brynjolfs-on [8]	Programming number of inverters	yes	1.5M-1.8G	370 (worst case)	Linear, but variable	8.9 @330M	1.8V	0.18	--------
Joe-shin Lee [9]	Enlarging Driving capabilities	yes	150M-740M	460M/V (diagram)	linear	53	2.5V	0.25	----------
Proposed PLL	Programming driving capabilities	yes	100MHz-1GHz	250MH/V	Linear and constant	17@ 1GHz	3.3V	0.18	0.18 + 0.18 (programmability and testability)

Table 6.1 Main works on wide-range and /or programmable PLLs and the proposed PLL.

6.4 Suggestions for Future Works

The following suggestion could be considered for the next version of the chip.

- A band-gap could be designed for 1.8 volt so that the whole system could be implemented with 1.8V supply.

- A regulator could be added to the VCO architecture, as shown in Ingino and Von Koenel work [17], in order to have a better noise rejection.
- Investigation should be carried out to see if it is possible to have less power consumption without losing the frequency range.

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