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Steady-state modeling and analysis of PWM current source drives

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STEADY-STATE MODELING AND ANALYSIS OF PWM CURRENT SOURCE DRIVES

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Abstract

Steady State Modeling and Analysis of PWM Current Source Drive
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Current source converter based ac motor drives are increasingly used in medium voltage high power applications due to their simple converter topology, inherent four-quadrant operation, reliable short circuit protection and motor friendly waveforms.

The behavior of the current source drive system in the steady state condition is studied in this thesis. The main objective of this investigation is to optimize the dc link inductance, which is one of the most expensive components of the drive system.

The first research focus of this thesis is to model the current source drive system in steady state condition. Different parts of the drive system such as the induction motor, mechanical load and the complicated field oriented control (FOC) scheme are simplified for the steady state operation mode. This model has two main features: 1) substantially reduced simulation time, and 2) simplified control loop design without any control parameter tuning and control instability problem.

Secondly, the characteristic of the dc link circuit is investigated using the developed steady state drive system model in MATLAB Simulink. The effect of the dc link inductance on the input LC resonant frequency is studied. The value of the dc current ripple is calculated under different conditions, and the effects of different system parameters on the ripple value is investigated. Furthermore, a user-friendly simulation software is developed for the dc choke optimization.

Experiments are conducted on a low-voltage (30hp, 480V) current source drive system test setup at Rockwell Automation Canada, with which the developed simulation model is verified.

Acknowledgments

The work presented in this thesis was carried out in the Laboratory of Electric Drive Application and Research (LEDAR) at Ryerson University.

I would like to express my gratitude to my supervisor, Professor Bin Wu, for his skillful guidance and continuous support throughout my graduate studies at Ryerson. His valuable advice directed this research project in a professional manner. I am also grateful to Dr. Navid Zargari, MV R&D manager at Rockwell Automation Canada, for his precious assistance and practical insights on this thesis.

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Last and not least I would like to thank Nazanin for her boundless encouragement and beautiful friendship.

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Chapter 1

Introduction

1.1 Introduction

1.1.1 High Power Medium Voltage Drives

High power medium voltage (MV) drives are increasingly used in industry, where speed and torque control of high power induction and synchronous motors are required . The advent of medium voltage controllable switches such as gate turn off thyristors (GTOs) initiated the development of these drive systems in mid 80's. The switching device technology has been improved over time, and insulated gate bipolar transistors (IGBTs) and gate commutated thyristors (GCTs) have become the standard switches for the MV drive systems nowadays. At the medium voltage level from 2.3KV to 13.8KV, the power rating of the MV drives varies from 0.4MW to 40MW. It can also be further increased to 100MW in some special applications [1].

A major market for the MV drives in industry is the retrofit applications, where the drive systems are used for the existing fixed speed MV motors for speed and torque control. Among the various MV drive applications, speed control of fan and pump type loads account for more than 70% of the installed MV drives as shown in Fig.1.1.

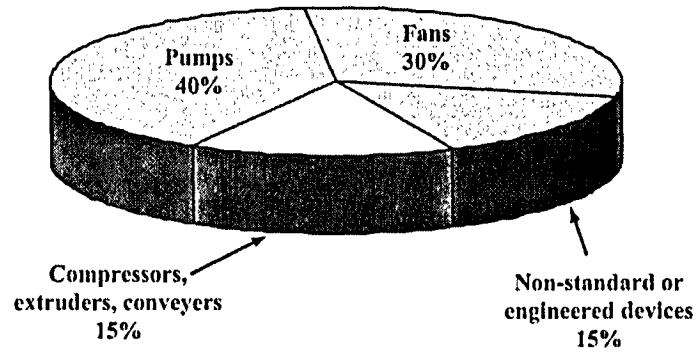

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Figure 1.1: Load types for MV drives

A main reason of the wide implementation of MV drives is to minimize the system total energy loss. With a fixed speed motor for fans or pumps, mechanical devices such as dampers and valves are normally used to control air and liquid flow. These mechanical methods introduce considerable energy losses in high power applications. When the MV drives are employed to control the motor speed according to the load requirement, the need for mechanical equipments can be eliminated. As a result, the total system efficiency can be increased substantially.

In addition, the use of MV drives can improve product quality. In metal industry, for instance, fast and accurate speed and torque control of rolling mills is required to achieve proper material thickness, flatness and tension [2]. Furthermore, the system downtime due to mechanical equipment maintenance can be reduced when electric drives are employed, which leads to a significant increase in overall productivity.

1.1.2 Configuration of MV Drives

Fig. 1.2 illustrates a simplified block diagram of the MV drive system. The main objective of this configuration is to convert a three-phase input voltage with fixed amplitude and frequency to a three-phase voltage with adjustable magnitude and frequency at the drive's output. As shown in Fig. 1.2, the input ac voltage is first converted to dc voltage/current through the rectifier (ac-dc converter). The dc link filter serves as an energy buffer and reduces the ripple on the rectifier's output voltage/current. This dc voltage/current is then fed to the inverter (dc-ac converter), and is converted to an adjustable three-phase voltage. Depending on the converter and dc link topologies, the drive system can be classified into two categories: 1)Voltage Source Inverter(VSI) fed drives, and 2) Current Source Inverter (CSI) fed drives.

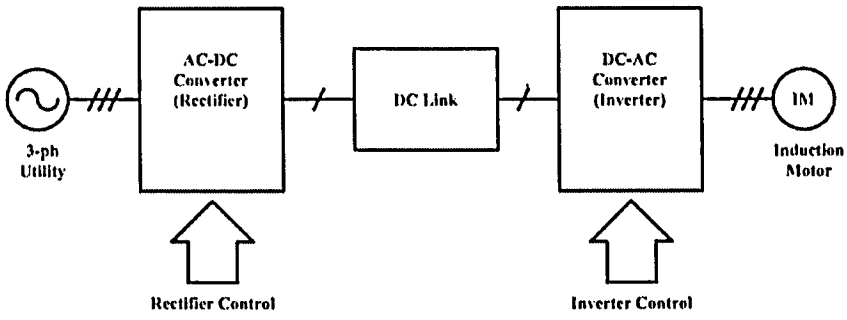
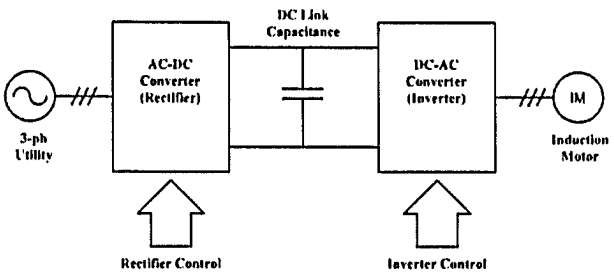


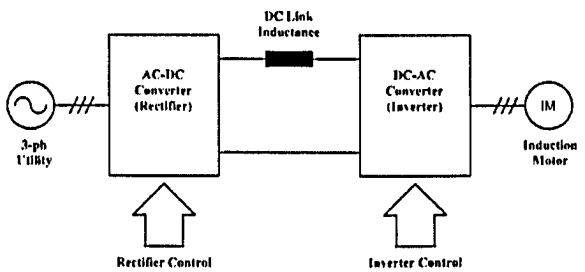
Figure 1.2: MV drive block diagram

1. **VSI-fed MV drives**

   A simplified block diagram of the VSI-fed drive system is shown in Fig 1.3(a), where a large capacitor bank is used in the dc link to reduce the voltage ripples. This dc voltage is then fed to the inverter and is converted to a three-phase voltage with adjustable amplitude and frequency.



(a) VSI-fed drive configuration



(b) CSI-fed drive configuration

Figure 1.3: MV drive configurations

Multi-pulse diode rectifier is mostly used to convert the input voltage to a dc voltage. In this case, a phase shifting transformer is usually employed to eliminate low order harmonics and reduce line current total harmonics distortions (THD) [1]. In some applications, controllable switches with pulse width modulation (PWM) scheme can be used as an active front-end to replace the diode rectifier [3].

On the inverter side, various topologies such as cascaded H-bridge multilevel inverters, diode clamped multilevel inverters and neutral point clamped inverters can be employed [1]. The output voltage of the inverter is a chopped waveform, where the rate of rise of the output voltage dv/dt is determined by the dc voltage, inverter configuration and the switching pattern. In order to reduce the output voltage dv/dt, voltage levels in a multilevel inverter should be increased.

The drive's output voltage is applied to the motor (normally an MV induction motor) and the output current is determined according to the motor parameters and operating conditions. Since motor inductances serve as a low pass filter, the motor current waveform will be close to sinusoidal.

2. **CSI-fed MV drives**

In the CSI-fed drive system shown in Fig 1.3(b), a large inductance is employed in the dc link to smooth the dc current. Fully controllable switching devices such as GTOs and GCTs are utilized for the PWM rectifier and inverter bridges. In some high power synchronous motor applications, SCR thyrsitors are used in the inverter bridge, where the commutation of the switches is assisted by the load's leading power factor and the topology is called load commutated inverter (LCI) [4].

The output current of a current source inverter is a defined chopped waveform. Its amplitude is equal to the amplitude of the dc current. At the drive output, a three-phase capacitor is connected to eliminate high order harmonics in the output current. Due to the presence of the output capacitor, the drive output voltage would not change instantaneously. As a result, the value of dv/dt of the output voltage in a CSI-fed drive is substantially reduced compared to that in a VSI drive system, which makes the CSI-fed drive more suitable to operate an MV induction motor [1].

Due to their significant advantages, such as simple converter configurations, dynamic braking, four-quadrant operation, reliable short circuit protection and motor friendly waveforms with low dv/dt, CSI-fed drives have gained great popularity in various industrial applications in recent years especially in medium voltage range [1]. Therefore, CSI-fed drive system is therefore the main focus of this research.

1.2 Current Source Drive System

1.2.1 Typical Circuit Diagram

Fig.1.4 illustrates the circuit diagram of a current source drive system. It consists of an isolation transformer, input filter circuit, a PWM current source rectifier, dc link circuit, a PWM current source inverter and an output filter. The current source drive system is connected to a high power MV induction motor.

A single-bridge configuration is used for both rectifier and inverter, where the switching devices are normally symmetric GCTs (SGCTs) and therefore antiparallel freewheeling diodes are not required. With this configuration the drive system can be used for higher voltage applications simply by connecting more switching devices in series in each leg. The minimum number of the series connected switching devices depends on the voltage and power ratings of the system. Another way to achieve higher power ratings is to use multi-bridge CSR or multilevel CSI with more than one bridges connected in parallel [5, 6].

As shown in Fig. 1.4, the drive system is connected to the supply through a three-phase Y/Δ isolation transformer. The main objective of this transformer is to block the common mode voltage that would otherwise appear on the motor windings. The common mode voltage is introduced by the rectification and inversion process and appears on the neutral point of the stator winding [7]. This voltage could cause premature failure of the winding insulation system. However, the isolation transformer may not be required in some configurations, where the common mode voltage is suppressed by a special dc choke [8].

The input line inductance L_{in} on the ac side of the rectifier represents the total inductance between the utility supply and the rectifier. It includes the equivalent inductance of the utility supply, leakage inductances of the isolation transformer if any, and the inductance of

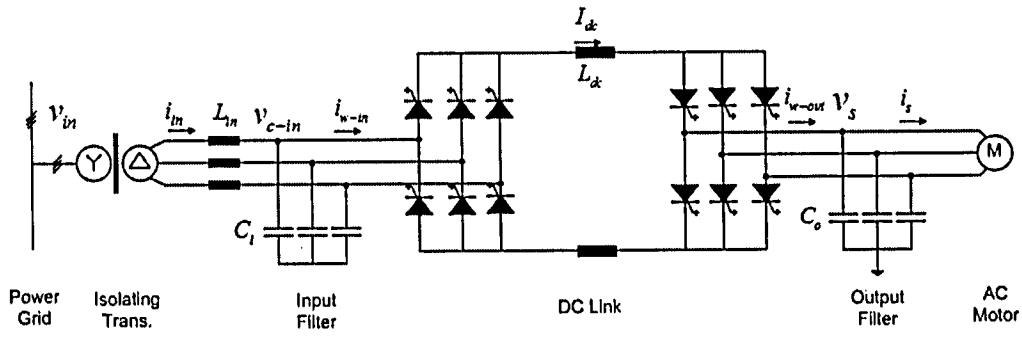


Figure 1.4: MV Current Source Drive System

the line reactor that might be added in practice for the line current THD reduction. The value of L_{in} is normally in the range of 0.1 to 0.15 (pu)[1].

In a PWM current source drive system, three-phase filter capacitors are necessary at the rectifier input and the inverter output (C_i and C_o). These capacitors assist the commutation of the switching devices. For instance, when one of the switches turns off, the current of that phase suddenly drops to zero. The capacitor C_i or C_o provides a path for the energy stored in the line side or load side inductance and prevents high voltage spikes which can be otherwise induced. Moreover, those capacitors also act as harmonic filters that improve the rectifier input current i_{w-in} and inverter output current i_{w-out}. The size of the capacitors is determined by different factors such as the input power factor, resonant frequency, the required current THD and the rectifier and inverter switching frequencies [9]. For high power drives with the switching frequency around a few hundred Hertz, the value of the filter capacitors at both sides is normally be in the range of 0.3 to 0.6 pu [1].

Between the CSR and CSI bridges, a dc choke L_{dc} is required to smoothen the dc current. Therefore, if a short circuit fault occurs on the motor side, the dc choke prevents the sudden rise of current and provides enough time for the protection circuit to function and therefore eliminates the need for fuses. However an open circuit in the dc current flow path would induce damaging high voltage at the dc link, and special care needs to be paid to the drive's

modulation scheme to avoid this. The dc choke is usually arranged with two coils, one connected to the positive bus and the other to the negative bus, to reduce the motor common mode voltage [1]. Since the dc inductance highly affects the drive system's overall size, cost and dynamic performance [10], optimal design of the dc inductance is very important and it is one of the main objectives in this work.

1.2.2 Modulation and Control Schemes

Different CSI-fed drive topologies and modulation schemes have been introduced and developed over time. In the mid 1980's, capacitor assisted current source inverter was introduced [11], which used SCR thyristors as the switching devices. A large output capacitor had to be employed to assist the SCR commutation. Today, the SCR devices are replaced by GCTs, and PWM scheme is used for both the rectifier and the inverter circuit. As a result, the output filter capacitor and dc link inductance can be reduced [12, 13].

The modulation scheme of the current source converter bridge is required to satisfy an important constraint: at any instant of time, two and only two switches should be turned on, one connected to the positive bus and the other connected to the negative bus. This assures that the output current is always defined and there is always a path for the dc link current to flow. For PWM modulation of a CSI-fed drive, different schemes such as selective harmonic elimination (SHE), trapezoidal pulse width modulation (TPWM) and space vector modulation (SVM) are available. For high power drives, SHE scheme is of more interest due to its desirable harmonic content with low switching frequency [14, 15].

Different control schemes can be employed for CSI-fed drives. The simplest control method for a CSI drive is the traditional V/f control, where the ratio of the output voltage to frequency is kept constant to ensure a constant motor flux. However with the V/f control method, the drive system's dynamics and stability would be limited [16].

In order to achieve superior dynamic performance, two advanced control schemes, field oriented control (FOC) and direct torque control (DTC), are developed, which have recently become the standard for high power medium voltage drives. As the name implies, the DTC scheme directly controls the electromagnetic torque by regulating the stator flux vector with hysteresis PWM band. Unlike the DTC scheme, the FOC scheme, also known as vector control, transforms the measured three phase stator current into two axis (d-q), leading to two orthogonal stator current components i_{ds} and i_{qs}. The rotor flux and the electromagnetic torque can then be controlled independently by controlling i_{ds} and i_{qs}. If the d-q axis is rotating with the synchronous speed, i_{ds} and i_{qs} become dc values and can be controlled in the same manner as a dc machine [17].

Due to its numerous advantages such as defined switching behavior, four quadrant operation capability [18] and improved dynamic performance [19], the FOC scheme is widely adopted for CSI-fed drive control. However the FOC scheme is very sophisticated with numerous time consuming mathematical calculations. Moreover, the tuning of the controller parameters, which is dependant on the motor and load parameters, is very challenging [20]. The operating principle of the FOC scheme will be elaborated in Chapter 2.

1.3 Simulation Techniques

In order to study the overall performance of the current source drive system, simulation models should be first developed. The simulation models can be used to illustrate the system's behavior from standstill to steady state condition. The results are then analyzed and used for further experimental investigation and finally the improvement of the drive's design.

For the modeling of power electronic circuits, there are many software packages commer-

cially available, such as MATLAB Simulink, PSpice, SABER, PSCAD and PSIM. Each of them has some advantages and disadvantages, mostly regarding to their accuracy, simulation time and mathematical calculation abilities. Matlab Simulink features rich power electronic library (which contains models for most of the power electronic components) and the capability to generate customized modules according to specific requirements. Its efficiency in control system design and simulation is also very desirable. Moreover, a MATLAB m-file program can be used together with the simulink model for more convenient simulation. For those reasons, MATLAB Simulink has been chosen in this work for the modeling of a CSI-fed drive [21, 22].

However, it is worth mentioning that the CSI-fed drive system is very complicated. Without a feedback control loop, the system will lose its stability. A sophisticated control schemes, such as FOC scheme, has to be used in the current source drive systems, resulting in numerous mathematical calculations in each simulation iteration [23]. The existence of these controllers in the model substantially increases the model's simulation time.

As mentioned previously, the main objective of this thesis is to optimize the value of the dc link inductor used in CSI-fed drives. For this purpose, dc current ripple value should be calculated in different conditions and its relationship with the dc choke and other system parameters should be investigated. Since the ripple of the dc current is defined in the steady state condition, the dynamic performance of the system is not considered in this thesis.

To investigate the system steady state performance, a detailed dynamic time-domain simulation model of the CSI-fed drive system, including all the dynamic models and the feedback control schemes, is not required. This is especially true for the dc link inductance design, where the model should be examined iteratively for different conditions and the dc current ripple value should be calculated for each trial. To reduce the simulation time and avoid control parameters tuning for a CSI drive system, a simplified model with the ability

of illustrating the steady state performance for a given drive operating condition is highly desirable.

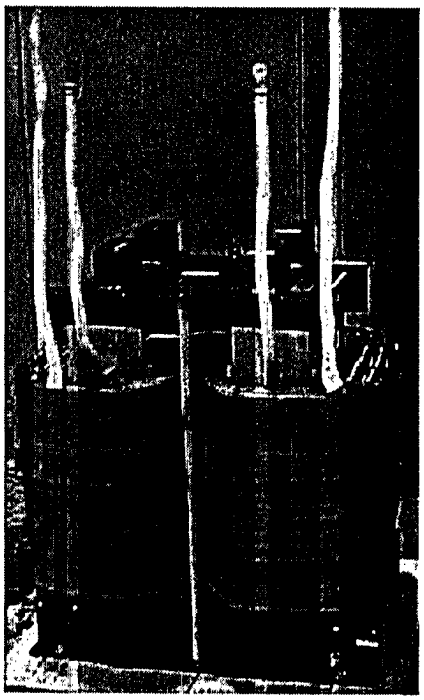
1.4 Motivation and Objectives

Considering the competitive market for drive systems, there is an urgent need for the drive manufacturers to improve product performance and increase profit. This can be achieved by two approaches. The first approach is to enhance the performance of the drive system by improving the line and motor current harmonic profiles, system dynamic response and energy efficiency. To achieve this, new topology and control schemes for the drive system should be developed. Secondly, the reduction in size and cost of the system is desirable, as the market prefers a drive system of lower price and smaller size.

This thesis deals with the second approach, i.e. to reduce the size and the cost of the drive system. Since the dc link inductor is one of the most expensive components in a PWM current source drive, this research focuses on the optimization of the dc choke value based on the simulation investigation of drive's steady state performance. The main objectives of this research can be summarized as follows.

1.4.1 Optimization of DC Choke Value for Cost Reduction

An obvious solution to attenuate the ripple on the dc current is to select a large value for the dc link inductance in the current source drive system. However, a large dc choke would lower the dc link current response and subsequently affect the drive system dynamic performance. More importantly, the overall cost and size of the drive system will increase with a larger dc choke. Therefore, it is necessary to address the tradeoff between the dc link current ripples and drive size, cost and dynamic performance. The proposed approach is to minimize dc link



(Courtesy of Rockwell Automation)

Figure 1.5: Typical dc link inductor used in CSI-fed drive system

inductance that could satisfy the dc ripple requirements. This research work was inspired by Rockwell Automation Canada, one of the leading manufacturers of the current source drive system. Fig. 1.5 shows a typical dc link inductor used in Rockwell's drive products.

It is worth noting that current source drive is a very complex system with many components and control parameters. Its dc current is a function of many system parameters, such as dc link inductance, output frequency, converter switching frequency and phase angle, input/output filter values, and switching scheme. Finding a general and all-encompassing equation for the ripple current calculation is almost impossible. Therefore, proper simulation model should be used to investigate the dc current and calculate the steady state current ripple under different operating conditions.

1.4.2 Development of Closed-form Simulation Algorithm

As mentioned previously, the complete dynamic simulation model for a CSI-fed drive system has two major drawbacks for system steady state performance investigation:

- In a CSI-fed drive system, a complicated FOC scheme is normally used. The drive controller design and switching techniques are dependant on the motor parameters and loading conditions. The control parameter tuning is therefore very challenging. If the controller is not properly designed, the drive will become unstable and cannot operate under steady state condition.

- Due to the complexity of a detailed dynamic drive system model, a considerable amount of time (between 90 to 120 minutes) is required to simulate the drive starting from standstill to reach the steady state operation. For dc choke optimization, where many iterations are required, the dynamic drive model cannot be used.

Since the dc link inductance design is based on the steady state waveforms, an alternative simulation model with the ability to provide steady state results without going through transient process is desirable. With such a steady state model, the drive starting from standstill is no longer required and the steady state results can be directly obtained at any drive operating conditions. Consequently, the dc link inductance optimization can be carried out more effectively.

1.5 Thesis Organization

This thesis contains five chapters. The first chapter provides general background on high power MV current source drives. Motivations and objectives of this thesis are also presented. The rest of the thesis are organized as follows:

Chapter2 focuses on the development of a steady state model for the CSI MV drive. After an introduction of the dynamic model with the FOC control scheme, steady state models for different parts of the drive system are developed. The FOC scheme is simplified to generate only the steady state gating signals for the CSR and CSI at different operating conditions.

Chapter3 conducts the study on the dc link circuit and the optimization of the dc choke value. The developed simulation model is employed to investigate the effect on the dc current ripple under different drive parameters and operating conditions. A user friendly software package is developed to assist dc link inductance optimization.

Chapter4 presents the verification of the steady state model developed in Chapter 2. Both simulation results from a dynamic induction motor model and experimental results obtained from Rockwell's MV drive product are provided to verify the developed steady state drive system model.

Chapter5 summarizes the conclusions and contributions of this thesis.

Chapter 2

Steady State Modeling of CSI drives

2.1 Introduction

As discussed in Chapter 1, current source converter based ac motor drives are increasingly used in medium voltage high power applications. Compared to voltage source converter fed drives, current source approach offers simple converter topology, inherent dynamic braking, inherent four-quadrant operation, reliable fuseless short circuit protection and motor friendly waveforms with low output voltage dv/dt [1].

In a current source drive system, the dc link inductor is a bulky and expensive component. In order to reduce the system's size and overall cost, this thesis focuses on the optimization of the dc choke value based on the simulation investigation of drive steady state performance. Due to the complexity of a detailed drive system dynamic model, it takes a long time to simulate the drive starting from standstill to the interested steady state speed.

Different commercial simulation packages, such as Matlab simulink, PSIM and SABER, can be employed for modeling of the drive system. The complexity of the system makes these models fairly slow. For instance, the simulation time of drive startup process using the dynamic model in Matlab Simulink would typically take 90 to 120 minutes. Therefore, a fast and simplified model for investigation of steady state performance of the drive system

in any given load speed is highly desirable.

This chapter focuses on the development of a steady state model of a current source drive system. After a brief introduction of the dynamic simulation model of CSI-fed drive with field oriented control (FOC), a simplified steady state model of the drive system is developed. The most time consuming functional blocks in the dynamic simulation model, such as the induction motor and its mechanical load are replaced with their equivalent steady state models. Furthermore, FOC control scheme is also simplified to generate only steady state gating signals for the rectifier and inverter bridges.

2.2 CSI Drive with FOC Scheme

Fig. 2.1 shows a simplified block diagram of the dynamic model of a current source drive system. The drive system model is composed of a rectifier, an inverter, an induction motor, input and output filters, a dc link inductance and a control block that regulates the motor flux and speed and generates the gating signals for the switching devices.

Different control schemes can be employed in the CSI drive. The controller receives the feedback signals such as motor stator voltage and current, and generates gating signals for the rectifier and inverter to properly control the motors speed and its mechanical torque.

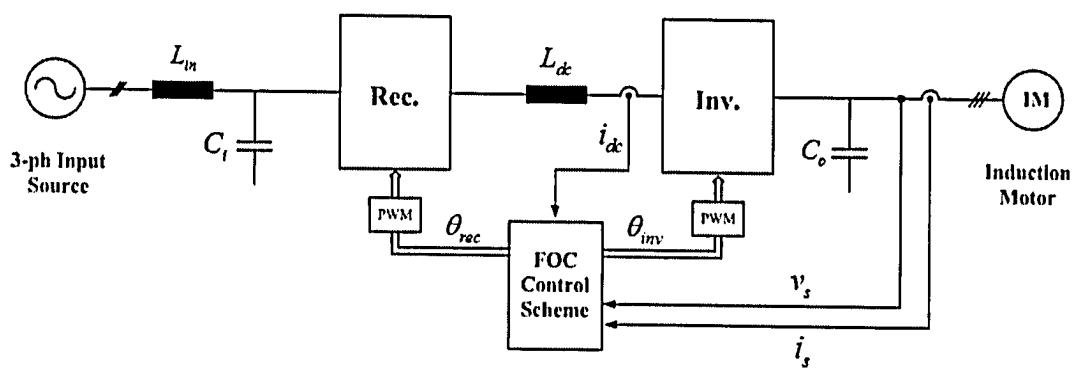


Figure 2.1: Block diagram of current source drive system dynamic model

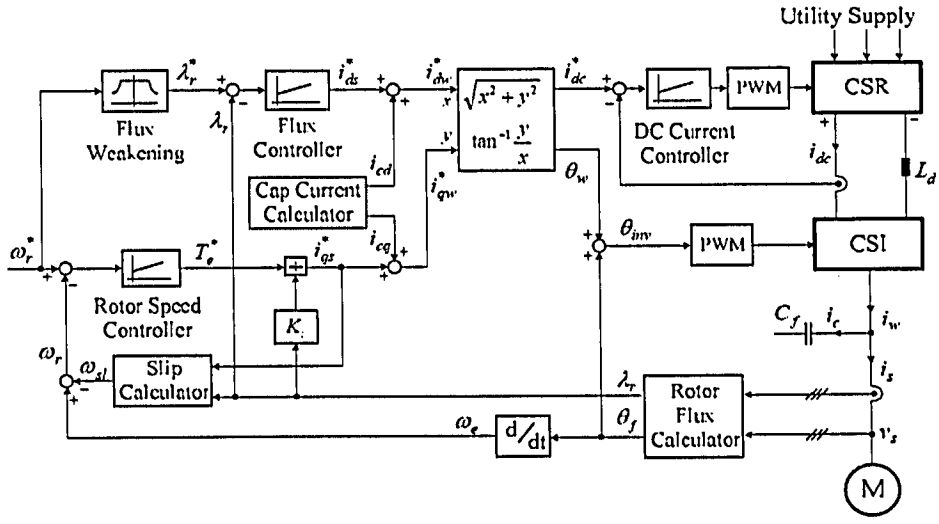


Figure 2.2: Simplified block diagram for FOC control scheme used for CSI fed drive

The controller should be designed according to the motor and load parameters and dynamic requirements. **Field oriented control (FOC)** (also known as vector control) is the commonly used control scheme with high dynamic performance [1, 24].

Fig. 2.2 shows a simplified block diagram of the FOC scheme used for CSI fed drive. The concept of field oriented control is to decompose the motor current into flux-producing and torque-producing components and control these two components separately. To facilitate the motor flux and torque control, the flux-producing and torque-producing components of motor current are usually transformed into dc quantities by choosing proper reference frames. The FOC scheme can be generally classified into rotor flux, air-gap flux and stator flux orientations. Since the rotor flux orientation is extensively adopted for ac drives, it is considered in this thesis.

As shown in Fig. 2.2, the motor stator voltage and current i_s and v_s as well as the dc link current i_{dc} are feedback variables of the controller. Through complex calculations, the phase angles ,θ_{rec} and θ_{inv}, used for rectifier and inverter modulation are obtained and proper gating

signals are generated. The torque and flux producing components of the output current i_{ds} and i_{qs} are derived as dc quantities with rotor flux orientation. The rotor flux and torque are controlled according to the motor speed requirement. FOC scheme will be discussed later in this chapter in details.

2.3 Steady-State Modeling of the CSI Drive System

As previously described, it is technically challenging to design an FOC control to satisfy both dynamic and steady state requirements of a drive system. In addition, to simulate the drive start up process using drive dynamic models, the simulation time is very long. Since the steady state condition is of interest for the dc link inductance design, a simplified steady state model is proposed for the analysis of the drive steady state performance. A block diagram of the steady state simulation model is depicted in Fig. 2.3. There are no feedback control loops in this model and hence its simulation time is substantially reduced. Moreover, the proposed steady state model does not have system instability problem caused by improperly tuned FOC parameters. Detailed discussion of the steady state modeling is presented below.

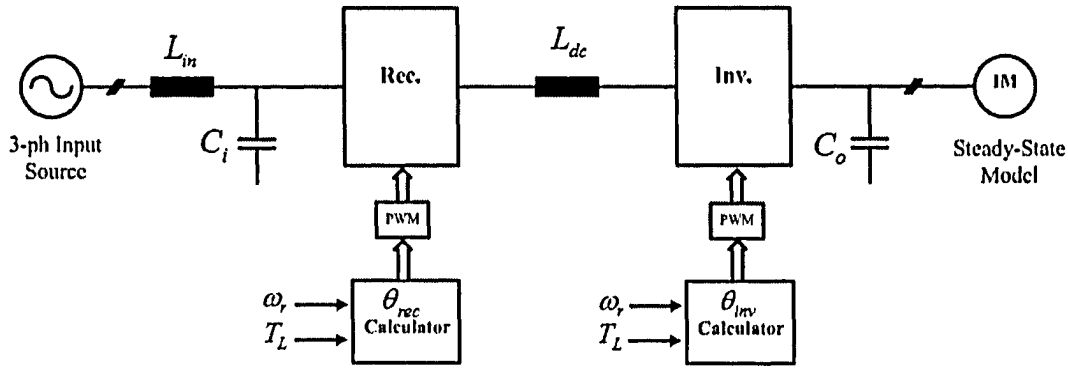


Figure 2.3: Block diagram of current source drive system steady state model

2.3.1 Induction Motor Model

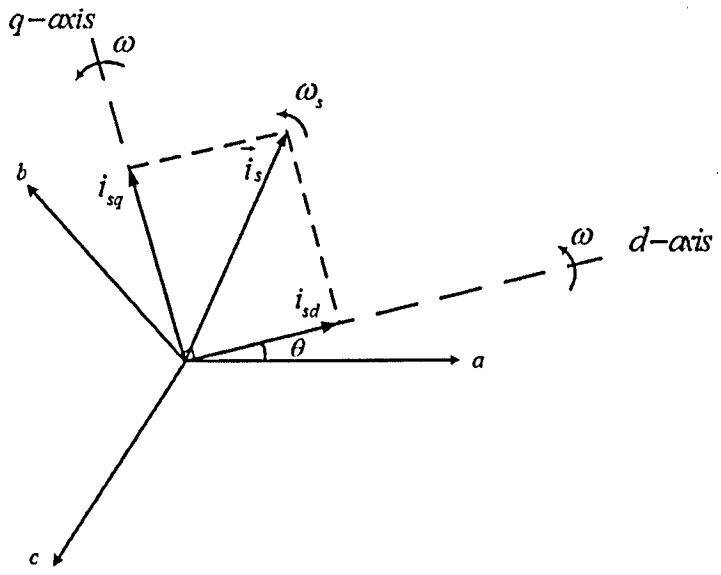


Figure 2.4: Vector diagram of the motor stator current in both abc and d-q frames

Induction motors are widely used in industry due to their features such as simple structure, easy maintenance and low cost. To simulate the performance of induction motors, different models have been developed [25, 26, 27]. For instance, the two-phase **dq** reference frame model is commonly employed for dynamic analysis of the motor.

In the **dq** model, all variables in the three-phase abc frame (x_a, x_b and x_c) are transformed to their d-q frame counterparts (x_d and x_q) by

$$\begin{pmatrix} x_d \\ x_q \end{pmatrix} = 2/3 \begin{pmatrix} \cos\theta & \cos(\theta - 2\pi/3) & \cos(\theta - 4\pi/3) \\ -\sin\theta & -\sin(\theta - 2\pi/3) & -\sin(\theta - 4\pi/3) \end{pmatrix} \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} \tag{2.1}$$

where θ is the angle between the d-axis and a-aixs of the two-phase and three-phase reference frames as shown in Fig. 2.4, and it is related to the rotating speed of the d-q frame as

$$\omega = \frac{d\theta}{dt} \tag{2.2}$$

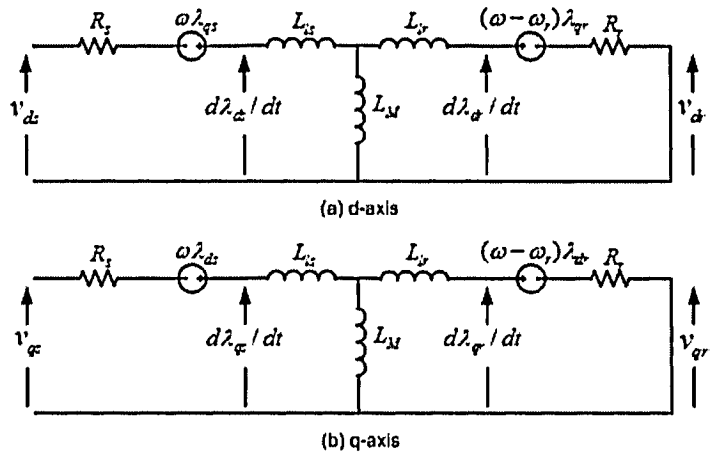


Figure 2.5: Induction motor dq model

A vector diagram of the motor stator current in both abc and d-q frames is shown in Fig. 2.4. In this figure, $\vec{i}_s$ is the space vector of the stator current, whose rotational speed is equal to its synchronous speed ω_s. **d** and **q** axes are perpendicular to each other and rotate in space with a defined speed ω. If ω is set to zero, the d-q frame is called **stationary frame.** i_s in this case is rotating in the d-q frame and hence its d-q components ,i_{ds} and i_{qs} vary with time. When the frame's rotating speed is equal to the synchronous speed ω_e, the frame is referred to as the **synchronous frame.** The synchronous frame and the current's space vector rotate at the same speed and therefore the values of i_{ds} and i_{qs} are constant in steady state operation.

The circuit diagram of an induction motor's d-q model is shown in Fig. 2.5. In this model R_s and L_{ls} are the stator resistance and the stator leakage inductance, R_r and L_{lr} are the rotor resistance and rotor leakage inductance, and L_m is the magnetizing inductance. λ_d and λ_q are the d-q components of the stator and rotor fluxes, and ω_r is the rotor speed. The rotor winding of the induction motor is shorted, and therefore the rotor voltage v_r is equal to zero. This model is suitable for investigating the dynamic behavior of the induction motor.

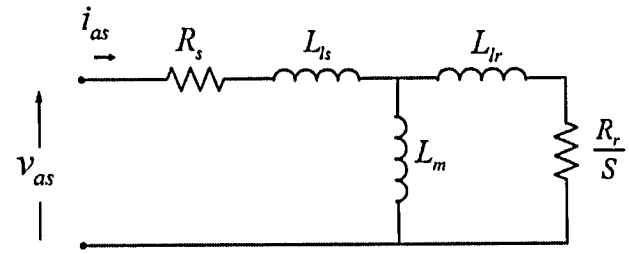


Figure 2.6: Steady state induction motor model (per phase circuit diagram)

On the other hand, the steady state model of the induction motor is preferred when the steady state condition is of interest. Fig. 2.6 shows the per phase circuit diagram of a commonly used steady state model, where v_{as} is the phase voltage of the stator while R_s, R_r, L_{ls}, L_{lr} and L_m have the same definition as those in the dynamic model of the motor [28]. The motor slip S can be calculated by

$$S = \frac{N_s - N_r}{N_s} = \frac{f_s - f_r}{f_s} = \frac{f_{sl}}{f_s} \tag{2.3}$$

where N_s and N_r are the synchronous and rotor speeds (rpm), f_s and f_r are the stator and rotor frequencies, and f_{sl} is the slip frequency, which is the difference between the synchronous and rotor frequencies. Moreover, in an induction motor with P poles the relationship between the synchronous speed and stator frequency is given by

$$N_s = \frac{120 f_s}{P} \tag{2.4}$$

To ensure that rated torque can be produced at different speeds, the rotor flux is normally kept at its rated value. Since the rotor flux is proportional to the ratio of the stator voltage V_s to the synchronous frequency f_s, $\frac{V_s}{f_s}$ should be kept constant. This method is known as **constant flux** or constant **Volt/Hertz** control scheme [16, 28]. Similarly, FOC scheme regulates the rotor flux at its rated value by controlling the flux-producing current. With a constant rotor flux, the stator voltage at different output frequencies can be found from

$$V_s = K f_s \tag{2.5}$$

where

$$K = \frac{V_{rated}}{f_{rated}} \tag{2.6}$$

The electromagnetic torque of the motor can be expressed as [29]

$$T_e = 3(\frac{P}{2})\frac{R_r}{S\omega_s}\frac{V_{th}^2}{(R_{th} + R_r/S)^2 + \omega_s^2(L_{th} + L_{lr})^2} \tag{2.7}$$

where V_{th}, R_{th} and L_{th} are the parameters in the **thevenin equivalent circuit** of the induction motor and can be calculated from:

$$\begin{cases} V_{th} = K_{th}.V_s \\ R_{th} = K_{th}^2.R_s \\ L_{th} = L_{ls} \\ R_{th} = K_{th}^2.R_s \\ K_{th} = \frac{L_m}{L_{ls}+L_m} \end{cases} \tag{2.8}$$

The values of electromechanical torque T_e and rotor speed ω_r are known for each operating condition. Using equations 2.3, 2.5 and 2.8, and solving equation 2.7, the value of the synchronous frequency f_s can be found. Motor slip S and stator voltage V_s are calculated correspondingly. These values complete the induction motor model; thus the motor model can be used in the steady state modeling of the drive system.

Fig. 2.7 shows the three-phase circuit diagram of the induction motor model. Providing a three phase system, the output of the inverter should be connected to a three phase motor model. For this purpose, three single phase induction motor steady state models are connected in Y connection.

It should be mentioned that the inverter output current waveforms include the fundamental component along with higher order harmonics. The steady state model is capable to show the results for the fundamental component. The slip value is calculated for the

fundamental component. However, due to the existence of large output filter capacitors, the higher order harmonics are highly reduced in the motor current and their effect on the results is negligible. Hence, the motor model can be used in the modeling of PWM CSI drives with high accuracy.

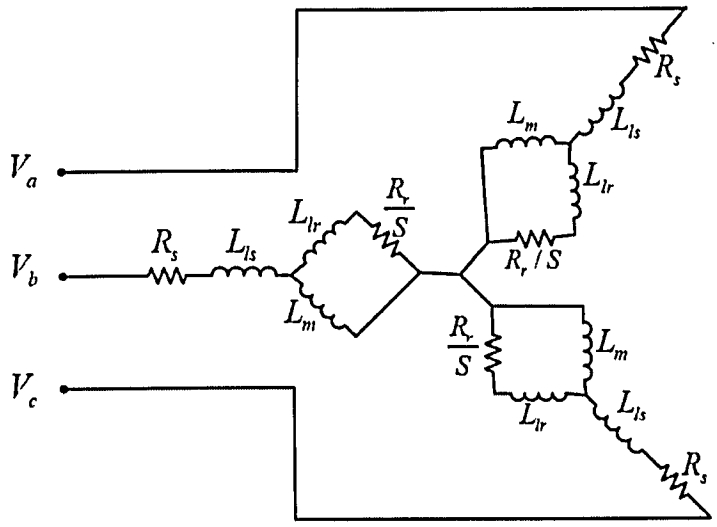


Figure 2.7: Steady state induction motor model (three phase diagram)

2.3.2 Load Model

The majority of MV drives are installed to control the speed of fans and pumps. Although fan/pump type loads do not require high dynamic performance, a proper speed control of these loads is an important issue since it highly affects the total energy loss as well as the quality of the product.

Due to their wide industrial application, the fan/pump type of loads are selected as the mechanical load connected to the induction motor in the proposed steady state modeling of the drive system. The relationship between the load mechanical torque T_L and speed ω_L for fan/pump type loads is

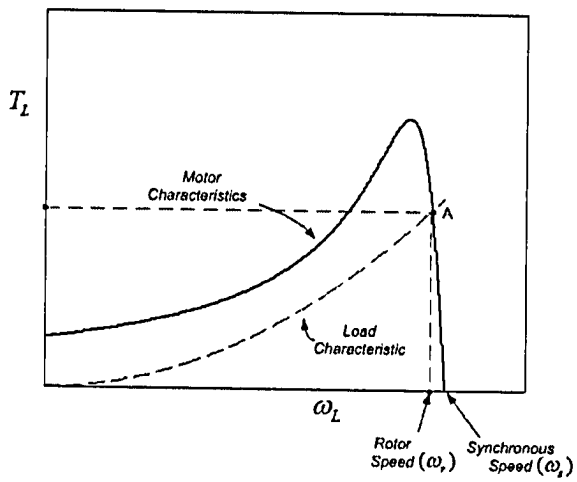


Figure 2.8: Load and motor torque-speed characteristics

$$T_L = k\omega_L^2 \tag{2.9}$$

where, k is determined by the load's characteristics. Assuming the load is directly connected to the motor rotor, the values of the rotor speed ω_r and motor's electromagnetic torque T_e are equal to the respective load speed and mechanical torque. A diagram of the torque-speed characteristics of a fan type load and an induction motor is shown Fig. 2.8.

The steady state operating point (A in Fig. 2.8) is the intersection of the load and the induction motor's speed-torque profiles. At this point, the mechanical torque produced by the motor is equal to the torque required by the load to operate at certain speed. The operating speed can be controlled by regulating the synchronous speed ω_s. When ω_s changes, the motor's torque characteristic shifts, resulting in a new steady state operating speed. Note that although fan/pump loads are considered here, other types of loads can also be implemented in the model by defining their torque-speed characteristics.

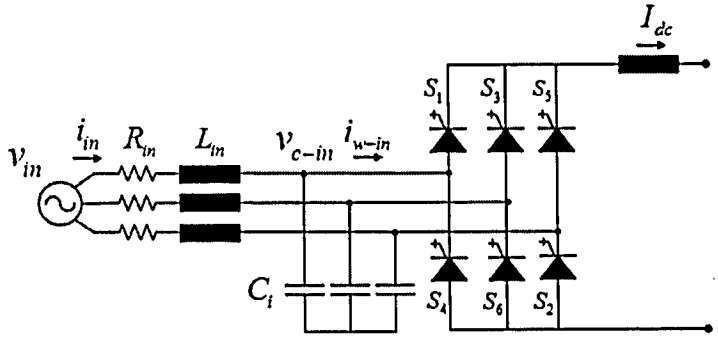


Figure 2.9: Circuit diagram of the PWM CSR

2.3.3 Rectifier Model

The main function of a PWM current source rectifier (CSR) is to convert a three-phase ac supply to an adjustable dc current source. The circuit diagram of the rectifier is shown in Fig. 2.9, where R_{in} and L_{in} are the line side total resistance and inductance. As discussed before, a three-phase filter capacitor C_i is necessary on the input side of the rectifier to assist GCT device commutation as well as to filter switching harmonics. On the dc side, a dc link inductance is used to smooth the rectifier dc output current.

Modulation Scheme

Selective harmonic elimination (SHE) PWM scheme can be employed to control the switching devices in the rectifier. SHE is an off-line modulation scheme where the switching angles are precalculated and stored in a lookup table [1]. These angles are derived such that certain low order harmonic components in the rectifier's input current i_{w-in} are eliminated. The higher order harmonics can then be easily filtered out by the input filter [30].

There are two constrains for the switching pattern on the current source converter. First, the dc current I_{dc} should be continuous. Open circuit of the dc current loop will induce a

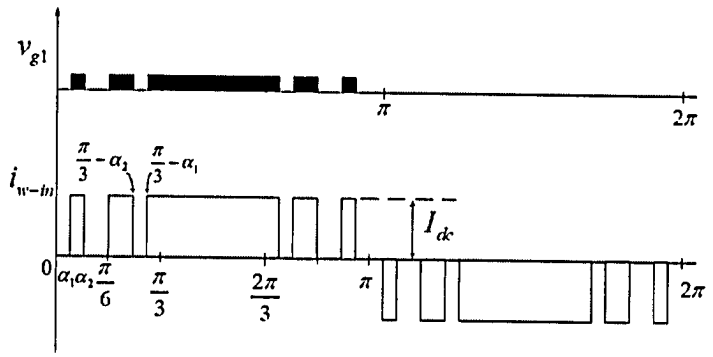


Figure 2.10: SHE line current for 2 harmonic elimination

huge voltage spike on the dc link, which will damage the switching devices. The second constraint is that i_{w-in} should be defined. These two limitations can be combined into one general rule: two and only two switches, one in the bottom half and the other in the top half, should be turned on at any instant of time [1].

Fig. 2.10 shows a typical input current waveform of the rectifier along with the gating signal v_{g1} for switch S_1. There are five pulses per half cycle. Among the ten switching angles , only two of them are independent (α_1 and α_2). The rest could be calculated accordingly as indicated in Fig. 2.10. The rectifier input current i_{w-in} can be expressed by its Fourier series:

$$i_{w-in}(\omega t) = \sum_{n=1}^{\infty} a_n \sin(n\omega t) \tag{2.10}$$

and its coefficients for different harmonics can be found from

$$a_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} i_{w-in}(\omega t)\sin(n\omega t)d(\omega t) \tag{2.11}$$

where n is the order of the current harmonics.

The desired switching angles to eliminate certain harmonic components can be calculated by equating the corresponding coefficients to zero. Therefore, the number of independent switching angles should be equal to the number of harmonics to be eliminated. Two harmonic

components can be canceled for the waveform in Fig. 2.10 by choosing proper switching angles (α_1 and α_2).

In order to calculate the switching angles to eliminate different combinations of harmonics, numerical methods (e.g. Newton-Raphson) can be employed. It should be noted that the lowest order harmonics should have the first priority to be eliminated in practice.

In a practical drive system, the rectifier input frequency is normally 60Hz. With seven pulses per half cycle, the SHE scheme can eliminate the 5^{th}, 7^{th} and 11^{th} harmonic components with a switching frequency of 420Hz for the GCT switches.

Rectifier Firing Angle (θ_{rec})

In a CSI-fed drive system, the modulation index of the inverter is usually fixed and the amplitude of the output current i_{w-out} is determined by the dc current I_{dc}. The dc current I_{dc} can be adjusted by the PWM current source rectifier through its firing angle θ_{rec}, which is the phase angle between the phase voltage across the input capacitor v_{c-in} and the fundamental component of the rectifier input current i_{w-in_1}. Note that it is also possible to compensate the rectifier input power factor using this firing angle control method and the modulation index m_a control scheme simultaneously [31]. By this means, the rectifier input active power and therefore its output dc power and dc link current can be regulated.

The value of the rectifier firing angel can be calculated in each steady state operating condition from the drive's output frequency and output voltage. To simplify the calculations, the following assumptions are made.

- The power loss in the rectifier and inverter circuits is negligible, which implies that their input and output power is equal:

$$P_{dc} = P_{ac} \tag{2.12}$$

- There is no modulation index control for the rectifier and the inverter. The value of the modulation index m_a of the rectifier and the inverter is the same and set at its maximum value. The modulation index is defined by

$$m_a = \frac{\widehat{I}_{w-in_1}}{I_{dc}} \tag{2.13}$$

where $\widehat{I}_{w-in_1}$ is the amplitude of the fundamental component on rectifier's input or inverter's output and I_{dc} is the dc current.

m_a has been calculated for different modulation schemes and the results are summarized in Table 2.1. It can be noted the number of pulses of the modulation scheme has little effect on the value of m_a.

Table 2.1: Modulation index for different number of pulses

Modulation Scheme	*SHE,5P*	*SHE,7P*	*SHE,9P*	*SHE,11P*	*SHE,13P*
m_a	1.028	1.022	1.029	1.027	1.026

- The winding resistance of the dc link choke R_{dc} is zero. Therefore, there is no voltage drop across the dc choke and the average dc voltage at the rectifier output is equal to that at the inverter input

$$V_{dc-rec} = V_{dc-inv} = V_{dc} \tag{2.14}$$

Considering the above assumptions, the active power of the inverter is

$$\sqrt{3}V_s\frac{\widehat{I}_{w-out_1}}{\sqrt{2}}\cos(\theta_Z) = V_{dc}I_{dc} \tag{2.15}$$

where V_s is the inverter output line-line voltage, V_{dc} is the average dc voltage, $\widehat{I}_{w-out_1}$ is the amplitude of the inverter output fundamental current and θ_Z is the phase angle between the output voltage and current. This angle is determined by the total impedance including the output filter capacitor and the impedance of the induction motor model. It should be

noted that to keep the rotor flux constant, V_s is proportional to the drive output frequency. Considering the modulation index in 2.13, Equation 2.15 can be expressed as

$$V_{dc} = \sqrt{1.5} V_s m_a \cos(\theta_Z) \tag{2.16}$$

Similarly, the dc voltage equation for the rectifier side can be derived as

$$V_{dc} = \sqrt{1.5} V_{in} m_a \cos(\theta_{rec}) \tag{2.17}$$

Substituting 2.16 into 2.17 the value of the rectifier firing angle can be calculated as

$$\theta_{rec} = \cos^{-1}\left(\frac{V_s \cos(\theta_Z)}{V_{in}}\right) \tag{2.18}$$

In summary, the rectifier firing angle θ_{rec} can be calculated according to motor parameters, slip frequency, inverter output filter capacitance and the output voltage. In the steady state simulation model, this angle is obtained with reference to the zero crossing point of v_{c-in} and the proper gate signals for the CSR switches can be generated accordingly.

2.3.4 Inverter Model

The circuit diagram of the PWM CSI is shown in Fig. 2.11. Its input dc current is converted to three-phase currents with adjustable frequency at the output. To assist GCT

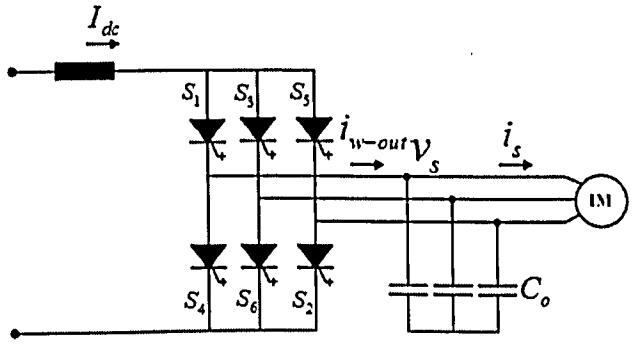


Figure 2.11: Circuit diagram of the CSI

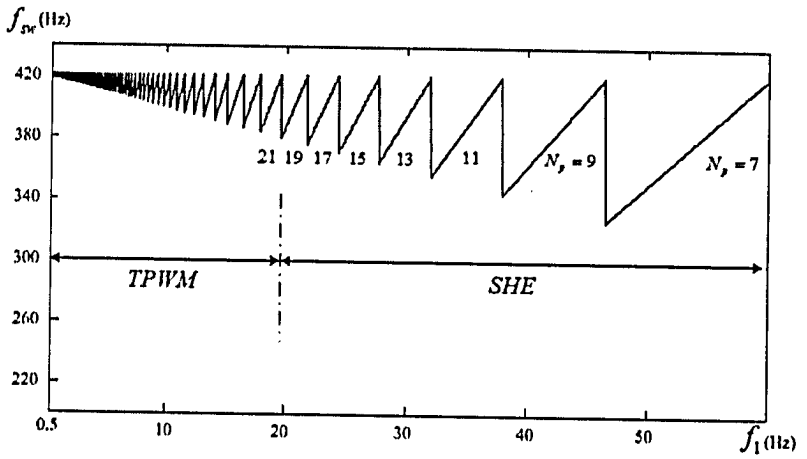


Figure 2.12: Inverter switching pattern

device commutation and switching harmonics elimination, a three-phase filter capacitor is connected at the output of the inverter.

Similar to the PWM CSR, the switching devices of a PWM CSI are GTOs or GCTs. At medium voltage high power level, the device's switching frequency is usually around a few hundred Hertz to limit the switching loss [1].

Modulation Scheme

There are three main PWM schemes for a CSI: selective harmonic elimination (SHE), trapezoidal pulse width modulation (TPWM) and space vector modulation (SVM). For the current source drive system presented in this chapter, SHE and TPWM schemes are employed. The switching pattern is designed in such to keep the switching frequency close to a certain value (i.e. 420Hz) as shown in Fig. 2.12. The device switching frequency can be calculated from

$$f_{sw} = N_p \times f_1 \tag{2.19}$$

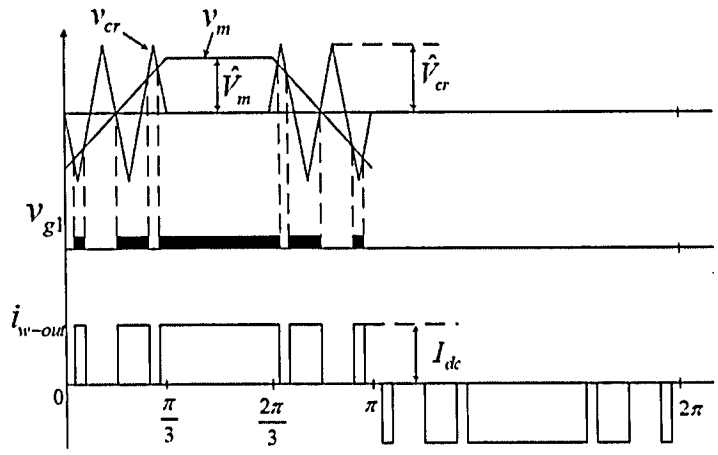


Figure 2.13: Trapezoidal modulation scheme

where N_p is the number of pulses per cycle of the inverter output fundamental frequency f_1. Therefore, in order to keep f_{sw} within a defined range, N_p should be increased with the decrease of f_1.

SHE PWM scheme is usually preferred over TPWM due to its better harmonic profile. However, it is difficult, if not impossible, to find all the switching angles when the number of pulses N_p is high. In practice, SHE scheme is employed for the output fundamental frequency above 20Hz with $N_p \leq 19$, where the maximum switching frequency of the GCT devices is limited to 420Hz. The TPWM scheme is used for lower fundamental frequencies with $N_p > 19$ as shown in Fig. 2.12.

Fig. 2.13 shows the principle of TPWM scheme, where the gating signal v_{g1} is produced by comparing a trapezoidal modulating waveform v_m with a triangular carrier waveform v_{cr}. The amplitude of the inverter output current i_{w-out} is equal to the dc link current I_{dc}.

The modulation index of the TPWM scheme is defined as

$$m_a = \frac{\hat{V}_m}{\hat{V}_{cr}} \tag{2.20}$$

where $\widehat{V}_m$ is the amplitude of the modulating waveform and $\widehat{V}_{cr}$ is the amplitude of the carrier waveform. The modulation index is usually fixed at 0.85, at which the THD of the inverter output current reaches its minimum value [1]. With a fixed modulation index, the inverter output current amplitude is proportional to I_{dc}.

The SHE scheme has been discussed in the previous sections, and therefore is not repeated here.

Inverter Firing Anlge (θ_{inv})

As discussed in Section 1.2.2, an FOC scheme with rotor flux orientation is used in the current source drive. In this scheme, the value of the inverter firing angle θ_{inv}, the angle between the inverter's output current i_{w-out} and the stationary reference frame, can be calculated.

The vector diagram of the FOC scheme with rotor flux orientation is shown in Fig. 2.14, where the rotor flux vector λ_r is aligned with the d-axis of the reference frame. With the d-q frame rotating at the synchronous speed ω_s, the d- and q-axis components of the rotor flux can be written as

$$\lambda_{dr} = \lambda_r, \ \ \lambda_{qr} = 0 \tag{2.21}$$

The main objective of the FOC scheme is to control the electromagnetic torque and magnetic flux of the induction motor separately. The electromagnetic torque can be expressed as

$$T_e = \frac{3PL_m}{2L_r}(i_{qs}\lambda_{dr} - i_{ds}\lambda_{qr}) \tag{2.22}$$

where P is the number of poles, L_m and L_r are the magnetizing and rotor self inductances, and λ_{dr} and λ_{qr} are the d- and q-axis components of the rotor flux, respectively. With λ_{qr}=0

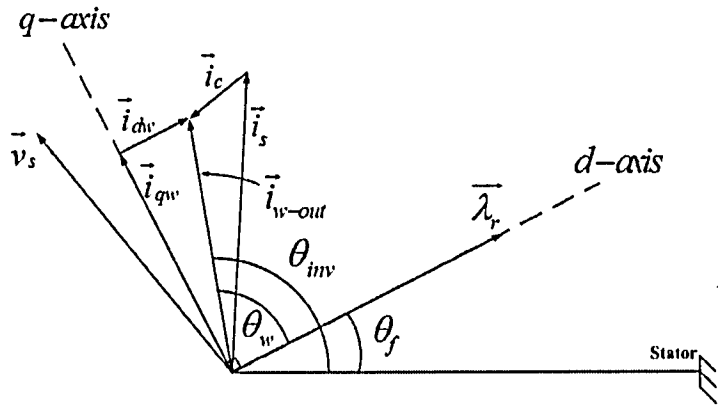


Figure 2.14: Vector diagram for CSI rotor flux orientation

for the rotor flux orientation, the torque equation can be simplified as

$$T_e = \frac{3PL_m}{2L_r}\lambda_{dr}i_{qs} \tag{2.23}$$

Therefore, by keeping λ_{dr} to its rated value, the developed torque can be independently controlled by i_{qs}, which is a dc quantity in the synchronous frame. To align the rotor flux vector with the d-axis, a proper inverter firing angle θ_{inv} should be calculated, based on which the gate signals will be generated. Considering Fig. 2.14, we have

$$\theta_{inv} = \theta_f + \theta_w \tag{2.24}$$

where θ_f is the rotor flux angle which is the angle between the d-axis and the stator reference frame. This angle can be calculated from

$$\theta_f = \int \omega_s dt \tag{2.25}$$

In order to calculate the inverter firing angle θ_{inv}, an angle θ_w between i_{w-out} and the d-axis should first be found. Therefore purpose the d- and q-axis components of i_{w-out} should be obtained.

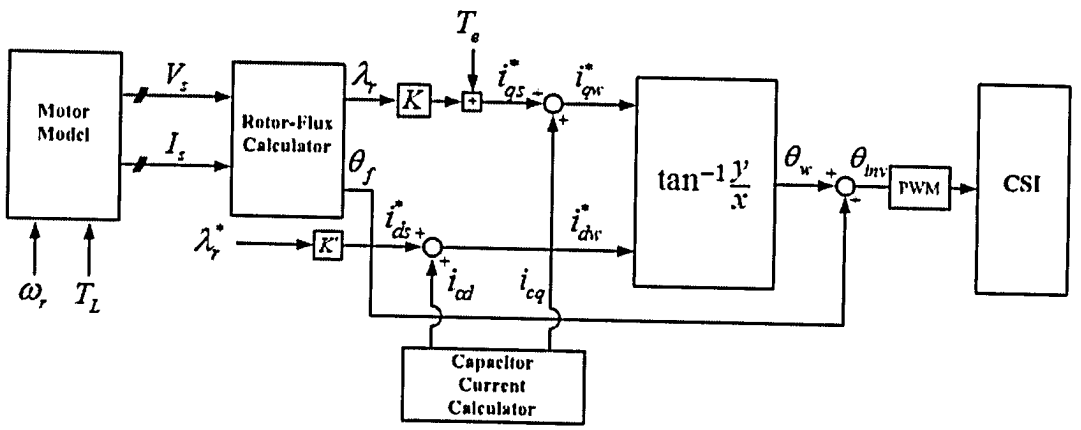


Figure 2.15: Simplified steady state block diagram of FOC scheme for CSI inverter

Fig. 2.15 shows the simplified block diagram of the FOC scheme in steady state condition. The values of the rotor speed ω_r and the mechanical torque T_L are defined by the given load condition. T_L is equal to the electromagnetic torque T_e generated by the induction motor. The reference value for the rotor flux λ_r^* is equal to its rated value in steady state and can be calculated from

$$\lambda_r^* = \frac{V_{base}}{4.44 f_{base}} \tag{2.26}$$

where V_{base} and f_{base} are the base values for the voltage and frequency.

Knowing the values of ω_r and T_L and considering the motor model discussed in Section 2.3.1, the values of the drive output voltage V_s and motor current I_s can be calculated. The rotor flux λ_r and its angle with respect to stator θ_f are then found through rotor-flux calculation, which is discussed in Appendix A.

In FOC scheme with rotor flux orientation, the flux-producing current component's reference value i_{ds}^* is related to λ_r^* as [1]:

$$i_{ds}^* = \frac{(1 + p\tau_r)}{L_m} \lambda_r^* \tag{2.27}$$

where τ_r is the rotor time constant and p is the derivative operator (d/dt). Since the rotor flux (λ_r^*) is normally kept constant $(p\lambda_r^*{=}0)$ in steady state, equation 2.27 can be simplified

to

$$i_{ds}^{*} = \frac{1}{L_m}\lambda_r^{*} \tag{2.28}$$

To calculate the torque-producing current component i_{qs}^{*}, the torque equation (2.23) should be considered, from which i_{qs}^{*} can be found from

$$i_{qs}^{*} = \frac{2L_r}{3PL_m}\frac{T_e}{\lambda_r} \tag{2.29}$$

The d- and q-axis inverter output currents can be calculated by

$$\begin{cases} i_{dw}^{*} = i_{ds}^{*} + i_{cd} \\ i_{qw}^{*} = i_{qs}^{*} + i_{cq} \end{cases} \tag{2.30}$$

where i_{cd} and i_{cq} are the d-q axis components of the capacitor currents, which can be derived from

$$\begin{cases} i_{cd} = -\omega_s v_{qs} C_o \\ i_{cq} = \omega_s v_{ds} C_o \end{cases} \tag{2.31}$$

where v_{qs} and v_{ds} are the d-q axis components of the inverter output voltage in the synchronous frame and ω_s is the synchronous speed.

Finally, θ_w can be calculated by

$$\theta_w = \tan^{-1}(i_{qw}^{*}/i_{dw}^{*}) \tag{2.32}$$

θ_w is a fixed value which is calculated for each operating condition and rating. Once θ_w is calculated and using equation 2.24, the inverter's firing angle θ_{inv} can be determined. It is worth noting that the initial rotor flux angle θ_f is assumed to be zero, which means the d-axis initially rests on the stator axis (see Fig. 2.14). This assumption does not affect the accuracy of the steady state drive system model and is validated by the systems experimental verification in Chapter 4.

2.4 Conclusion

In this chapter, a simplified model for the steady state analysis of the current source drive system is developed. Steady state models are used to represent different function blocks of the drive system such as the induction motor, mechanical load, rectifier and inverter, and the FOC control scheme. Mechanical load is assumed to be fans/pumps since they are widely used in industry. The detailed analysis of CSR and CSI gate signals generation under different steady state operating conditions are presented. Compared to the dynamic simulation model, the developed steady state model has the following features :

- No motor start-up process. To investigate the steady state performance of the drive, the motor is not required to start from standstill. The simulation model is developed such that it can directly provide the steady state simulation results under any motor speeds. Therefore, the simulation of the drive start-up process is avoided.

- Simple simulation algorithm. The effort has been made to simplify high order differential equations for the FOC control into a number of simple algebraic equations for steady state modeling of the drive. The complexity of the simulation algorithm is greatly reduced.

- No system stability problem. In a CSI fed drive system, improper tuning of controller parameters causes system instability. This problem is completely eliminated in the steady state simulation model developed in this chapter.

- Substantial reduction in simulation time. Since the simulation algorithm developed in the chapter neither involves motor start-up process, nor controller parameter tuning, nor system stability problem, the simulation time is substantially reduced for the steady state analysis of the drive.

Chapter 3

Analysis and Design of DC Link Circuit

3.1 Introduction

The dc link inductance in a CSI-fed drive is used to reduce the dc current ripple and to provide a stiff current for the inverter. The magnitude of the dc current ripple, which is defined and calculated in the steady state operating conditions, affects the harmonic distortions of the drive's input and output currents. As the dc current becomes closer to ideal (i.e. ripple free), the harmonic profile of the input and output currents can be improved.

The dc current ripple can be reduced by increasing the dc link inductance. However, the dc inductance cannot be too high, as a large inductance substantially increases the size and cost of the drive. In addition, the drive dynamic performance will be degraded as well with a larger dc choke [10]. Therefore, the dc choke optimization is essential in finding a minimum possible inductance that could satisfy the dc current ripple requirements.

The dc current ripple can be affected by a variety of factors in a current source drive such as the inverter output frequency, filter capacitors, converter switching frequencies, and the switching firing angles. Finding an analytical equation for the ripple value calculation is therefore almost impossible. To solve the problem, the steady state simulation model

developed in Chapter 2 can be used to analyze the behavior of the drive and to calculate the dc current ripple under different operating conditions.

In this chapter, the characteristics of the dc link current are studied. Effects of the system parameters on the dc current ripple are then investigated using the developed steady state system model. Moreover, to assist the calculation of the dc current ripple and the selection of proper dc inductance for a given ripple constraint, a user-friendly computer software package is developed.

3.2 System Overview

Fig. 3.1 shows a typical circuit diagram of a high power current source drive system. The rectifier input fundamental frequency is fixed and equal to the frequency of the utility supply (60Hz). The selective harmonic elimination (SHE) scheme with seven pulses per half cycle is used to control the switching devices in the rectifier. As mentioned before, the switching angles in this scheme are chosen in order to eliminate the 5^{th}, 7^{th} and 11^{th} harmonics of the input current i_{w-in}. The higher order harmonic components waveform are attenuated by the input filter capacitor C_i. As a result, the input line current waveform i_{in} is close to sinusoidal as shown in Fig. 3.17(a).

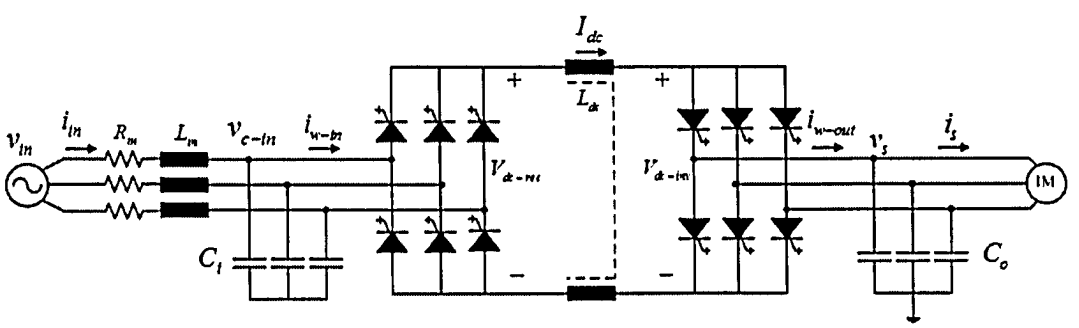
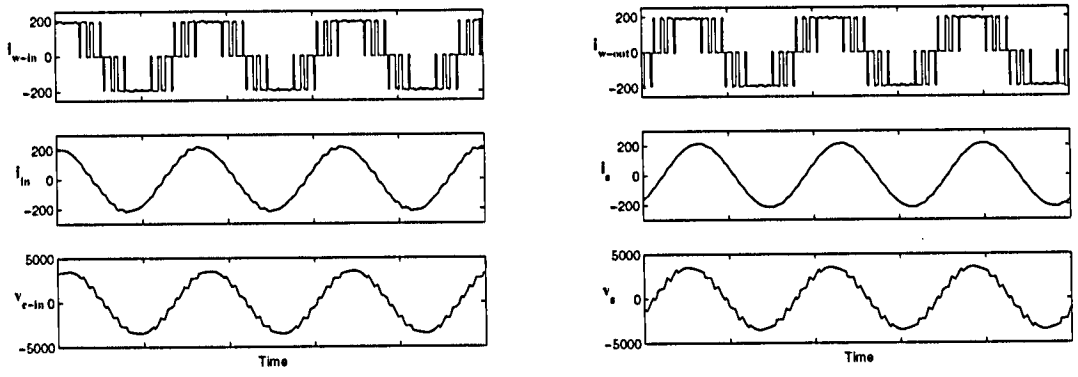


Figure 3.1: CSI drive circuit diagram



(a) input waveforms (b) output waveforms

Figure 3.2: Typical waveforms of a CSI drive system

SHE and TPWM schemes are employed in the inverter. The fundamental frequency of the inverter output current controls the motor speed. The number of pulses of the modulation scheme is adjusted such that the switching frequency is kept in the 300 to 420Hz range. Typical waveforms of the input and output currents and voltages of a CSI-fed drive system are shown in Fig. 3.15(b). The inverter output frequency in this example is 60Hz.

Fig. 3.3 shows the waveforms of the rectifier output dc voltage v_{dc-rec} and the inverter input dc voltage v_{dc-inv}. The phase displacement between these two dc voltages depends on the rectifier and inverter firing angles, θ_{rec} and θ_{inv}. The number of pulses per cycle of the fundamental frequency in these dc voltages depends on the number of pulses of the rectifier and inverter PWM modulation schemes. The dc link current i_{dc} contains a certain amount of ripple caused by switchings of the rectifier and inverter as well.

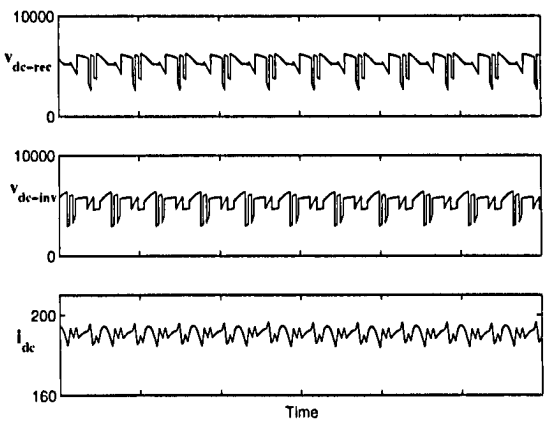


Figure 3.3: DC link waveforms of CSI drive system

3.3 DC Link Analysis

In this section, general information about the dc current and the definition of the ripple value are presented. The effect of the dc link inductance on the drive input resonant frequency is discussed in detail.

3.3.1 DC Link Current

The dc current ripple is calculated in the steady state operation mode. Its value is mainly limited by the dc link inductance, and hence proper dc choke should be chosen to satisfy the ripple constraint.

The dc current ripple and its relationship to the dc link inductance and the voltage drop across the inductance can generally be expressed as:

$$\Delta i_{dc} = \frac{v_{dc-rec} - v_{dc-inv}}{L_{dc}} \Delta t \tag{3.1}$$

where Δt is the time interval. The dc current ripple in percentage is defined by

$$Ripple(\%) = \frac{\Delta I_{dc_{max}}}{I_{rated}} \tag{3.2}$$

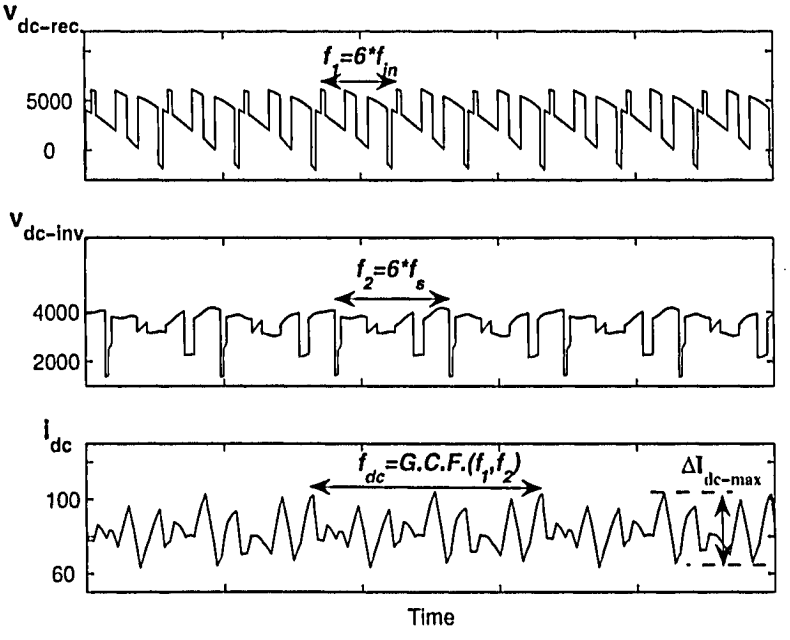


Figure 3.4: Dc link current frequency

where $\Delta I_{dc_{max}}$ is the maximum dc current ripple and I_{rated} is the rated dc current.

The maximum dc current ripple $I_{dc_{max}}$ is equal to the difference between the maximum peak and the minimum peak of the dc current as shown in Fig. 3.4.

As shown in this figure, the frequencies of the dc link voltages, v_{dc-rec} and v_{dc-inv}, are six times of the fundamental frequencies of the drive's ac input and output voltages, respectively. Considering the displacement of dc voltages at both sides of the dc choke, the frequency of the dc link current can be calculated, which is equal to the **Greatest Common Factor** (G.C.F) of the frequencies of the dc link voltages. The input fundamental frequency is normally fixed, thus the dc current frequency is only related to the output frequency. In Fig. 3.4, the input and output frequencies are equal to 60Hz and 40Hz, resulting in a dc link current frequency of 120Hz.

The shape and the frequency of the dc link current affect the input and output current

harmonic profiles. Due to dc current ripple, low order harmonics in the rectifier input and inverter output currents are not completely eliminated by the SHE scheme. The current ripples introduce some non-integer (non-characteristic) harmonics to the rectifier input and inverter output current waveforms.

3.3.2 Effect of DC Circuit on Input Resonant Frequency

The input resonant frequency f_{res} in a current source drive system is one of the important technical issues. To avoid any possible LC resonance, f_{res} should not fall into the harmonic frequencies introduced by the drive system. The LC resonance may cause high voltage oscillations on the rectifier's input side, which might damage the system components.

Neglecting the input equivalent resistance R_{in} (due to its small value), the input LC cut-off frequency can be calculated by

$$f_{cut-off} = \frac{1}{2\pi\sqrt{L_{in}C_i}} \tag{3.3}$$

where L_{in} is the total input line inductance and C_i is the input filter capacitance. $f_{cut-off}$ is equal to the input resonant frequency when the effect of the dc link circuit of the drive is not considered. While in reality the resonant frequency is affected by the dc circuit. Note that the LC filter cutoff frequency $f_{cut-off}$ is only related to the input LC filter circuit and it is not affected by the dc link circuit.

Fig. 3.5 shows a three-phase current source rectifier used to investigate the effect of dc link circuit on the input resonance. The inverter and the motor are replaced by an equivalent load resistance R_d.

Depending on the rectifier switching conditions, two switching states can be considered for each phase. When neither of the switches in phase-a, S_1 or S_4, is turned on, the input

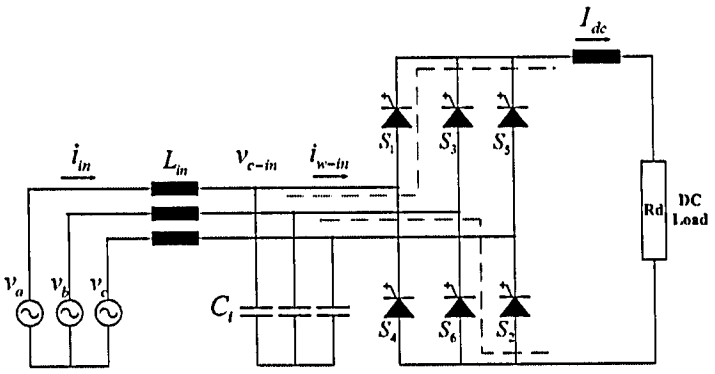
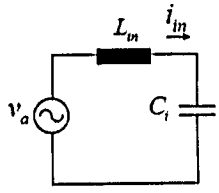
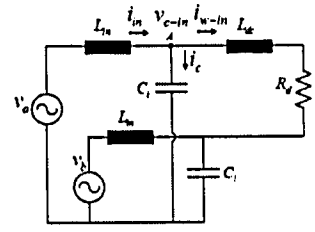


Figure 3.5: Current source rectifier



(a) S_1 and S_4 are open



(b) S_1 or S_4 are closed

Figure 3.6: Equivalent rectifier circuit of phase a

LC circuit in this phase is completely detached from the dc link (Fig. 3.6(a)). Assuming that the SHE modulation index in a CSR bridge is unity (no short through of one leg) and all of the devices are used evenly, the state in Fig. 3.6(a) occurs for 1/3 of the fundamental period, as it is two out of six possible switching states in this case.

Fig. 3.6(b) shows a circuit diagram where S_1 and S_6 are conducting. This condition occurs for 2/3 of the fundamental period. Note that in a three-phase balance system the neutral points of the three-phase input voltage and the filter capacitor have equal potential, thus they are connected together in this figure.

It should be mentioned that the sources of LC resonances in this case are the harmonics in the rectifier's input current i_{w-in}. The input voltage is considered as a purely sinusoidal

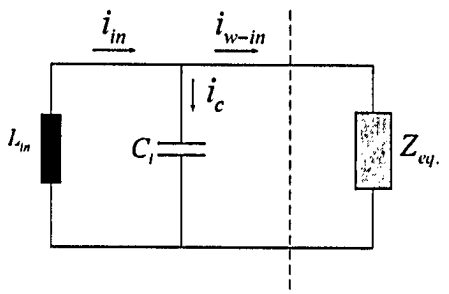


Figure 3.7: Equivalent resonant circuit

voltage source and hence it is shorted for the resonant mode analysis.

Consequently, the equivalent circuit diagram over one fundamental period can be shown in Fig. 3.7, where Z_{eq} represents an equivalent impedance seen from the rectifier's input terminal into the dc link circuit in one period of the fundamental frequency. This equivalent impedance is affected by the dc link inductance L_{dc}, equivalent dc load resistance R_d and the rectifier's switching patterns. It can be concluded from the equivalent circuit that the input LC resonant mode is influenced by both the input LC filter and the dc link circuit.

In order to precisely calculate the value of Z_{eq}, a proper approach is required to transform the dc circuit to the ac side, with consideration of the equivalent circuits shown in Fig. 3.6 and the rectifier switching pattern. Accurate mathematical derivation of the value of Z_{eq} is beyond the scope of this work. Instead, the simulation model of a current source rectifier is used in this section to investigate the effect of the dc link inductance on the input resonant frequency f_{res}.

The simulation investigation is based on the input line current harmonics. As has mentioned, due to the existence of the dc ripple, the rectifier input current i_{w-in} contains small 5^{th} order harmonic. When the rectifier's input resonant frequency (determined by both the input LC filter circuit and the dc link circuit) is equal to 5pu (300Hz), the 5^{th} harmonic in i_{w-in} will be notably amplified, which will in turn distort the input line current i_{in}.

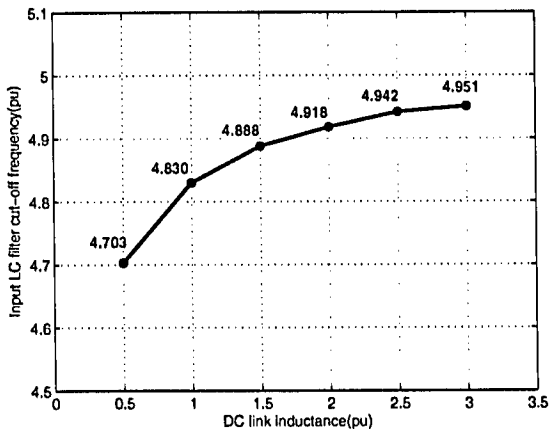


Figure 3.8: Relationship between the dc choke and the input LC filter cut-off frequency (input resonant frequency is kept at 300Hz)

In this investigation, the dc link inductance is varied from 0.5pu to 3pu. The resonant mode is found by finding the corresponding value of the input filter capacitance (L_{in} is kept unchanged), which gives rise to the maximum 5^{th} harmonic in i_{in}. As a result, the rectifier input LC resonant frequency is fixed at 5pu (i.e. 300Hz), while the LC filter cutoff frequency $f_{cut-off}$ is changed by the variation of input filter capacitance. In other words, to maintain a input resonant frequency at 300Hz, the input LC filter cutoff frequency has to change with the variation of dc link inductance.

Fig. 3.8 shows the results from this investigation. The LC cutoff frequency increases when the dc choke becomes larger. Some conclusions can be made from these results:

- The input resonant frequency is not solely defined by the input LC filter circuit. Under the variation of dc link inductance, the rectifier input filter parameters and therefore the filter cutoff frequency $f_{cut-off}$ has to change to maintain a input resonant frequency at 300Hz.

- To keep the input resonant frequency at 5pu, the input LC filter cutoff frequency

changes from 4.703pu for L_{dc}=0.5pu to 4.95pu for L_{dc}=3pu. This implies that due to the presence of dc link inductance, the effective input resonant frequency becomes higher than the LC filter cutoff frequency. As the dc link inductance increases, its effect on the input resonance decreases and $f_{cut-off}$ approaches 5pu.

Finally, the effect of the dc link inductance on the input resonance should be considered while designing the input LC filter. For instance, with an input LC filter designed with a cutoff frequency of 4.703pu and a dc choke of 0.5pu, the input resonant frequency would be equal to 5pu, which would amplify the 5^{th} harmonic of i_{w-in} and would introduce high voltage and larger current ripple into the system.

3.4 DC Current Ripple Analysis

3.4.1 Effect of L_{dc} on DC Current Ripple

In this section, the effect of the dc link inductance on the dc current and its ripple is studied using the developed steady state drive system model. Parameters and ratings of the CSI-fed drive and the induction motor are summarized in Tables 3.1 and 3.2. These values represent the practical parameters for Rockwell Automation's medium voltage drive system (Powerflex7000) and will be used for all system studies presented in this thesis. A 1250hp centrifugal fan is used as a mechanical load of the drive, whose rated speed is the same as the induction motor.

Fig. 3.9 shows the dc current ripple with different values of dc link inductance, where the CSI output frequency is kept at 60Hz. As expected, the dc current ripple is reduced by the increase of dc link inductance. It can also be seen that the effect of the dc link inductance on the ripple is not linear. There is 8% reduction in the ripple value when L_{dc} is increased

Table 3.1: CSI drive ratings and parameters

Rated Power	1MVA
Rated voltage (line-to-line,rms)	4160V
Rated line current (rms)	138
DC link inductance L_{dc}(rms)	0.8pu
Total line inductance L_{in}	0.1pu
Input filter capacitor C_i	0.5pu
Equivalent series resistance R_{in}	0.005pu
Output filter capacitor C_o	0.4pu

Table 3.2: Motor Nameplate and parameters

Motor Ratings		Motor Parameters	
Rated Output Power	1250hp	Stator Resistance, R_s	0.01pu
Rated Line-to-Line Voltage	4160V	Stator Leakage Inductance, L_{ls}	0.125pu
Rated Stator Current	138A	Rotor Leakage Inductance, L_{lr}	0.125pu
Rated Speed	1192 rpm	Rotor Time Constant, τ_r	1.5 sec
Rated Torque	7466N.m	Magnetizing Inductance, L_m	4.5pu
		Moment of Inertia, J	20 kg.m^2

from 0.5pu to 0.6pu, whereas the variation from L_{dc}=0.6pu to L_{dc}=1pu can only reduce 6% of the dc current ripple.

Fig.3.10 shows the effect of the dc link inductance on the ripple value when the drive operates at different output frequencies. The motor speed varies from 0.5pu to 1 pu. Therefore the range of the output frequency is from 30Hz to 60Hz. At each output frequency the dc current ripple with different dc choke values (ranging from 0.5pu to 1.2pu) is calculated. It can be observed that the ripple value decreases for larger dc link inductances in each output frequency and the maximum value of the ripple occurs at frequencies around 40 to 45 Hz. This is mainly due to the input LC resonant mode, which will be discussed in the following subsections.

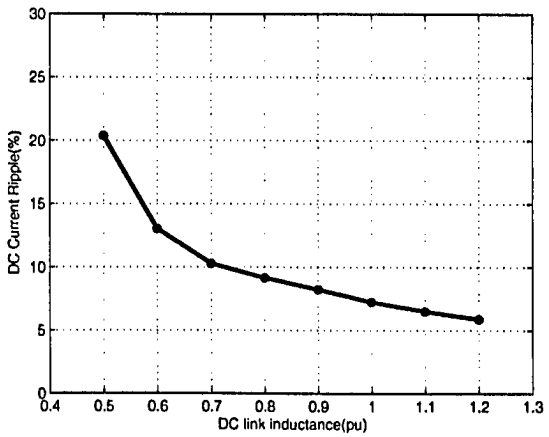


Figure 3.9: Effect of dc link inductance on dc current ripple, f_s=60Hz

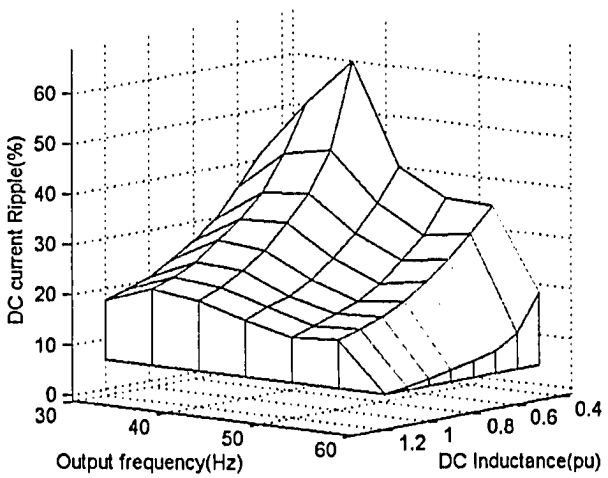


Figure 3.10: Effect of dc link inductance on dc current ripple, f_s=30~60Hz

3.4.2 Effect of Filter Capacitors on DC Current Ripple

The design of the input and output filter capacitors in a current source drive system is an important issue, as they directly affect the system performance. For instance, the input filter should be designed in such a way to reduce the unwanted harmonics to a certain degree [9]. The input power factor of the drive should also be considered in the filter design [32].

As previously mentioned, the SHE scheme will introduce some low order harmonics in the drive input and output currents due to the dc current ripples. An improperly designed filter capacitor could excite LC resonances and degrade the ac and dc current waveforms. Therefore, understanding the effects of filter capacitors on the dc link current can assist in the dc link inductance design and the overall system performance improvements.

1) Input filter capacitor

The developed steady state simulation model of the CSI drive system can be utilized to investigate the effects of the input filter capacitor on the dc current ripple. For this purpose, the dc current ripple is calculated under different input capacitance (from 0.35pu to 0.55pu), while other system components are kept constant.

Fig. 3.11 shows the relationship between the input filter and the dc current ripple with the drive output frequency as a parameter. It can be seen that at each output frequency, the dc current ripple stays relatively constant over the input capacitance variation, except at C_i=0.45pu, where the ripple reaches its maximum value. This change in the ripple value is because at this point the rectifier input LC resonance is excited by the 5^{th} harmonic of the rectifier input current i_{w-in}.

The input line current waveform i_s along with its FFT analysis are shown in Fig. 3.12, where two different values of the input filter capacitor (C_i=0.4pu and 0.45 pu) are used and

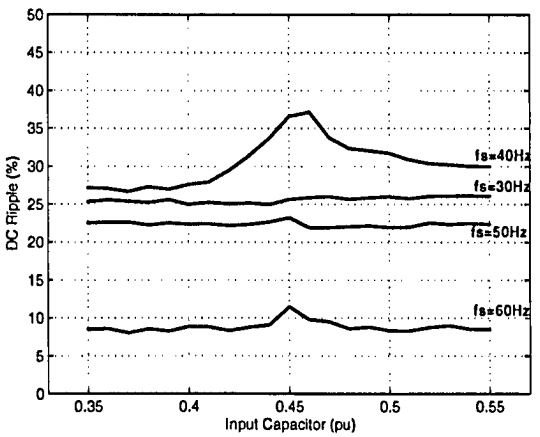


Figure 3.11: Effect of input filter capacitor on the dc current ripple

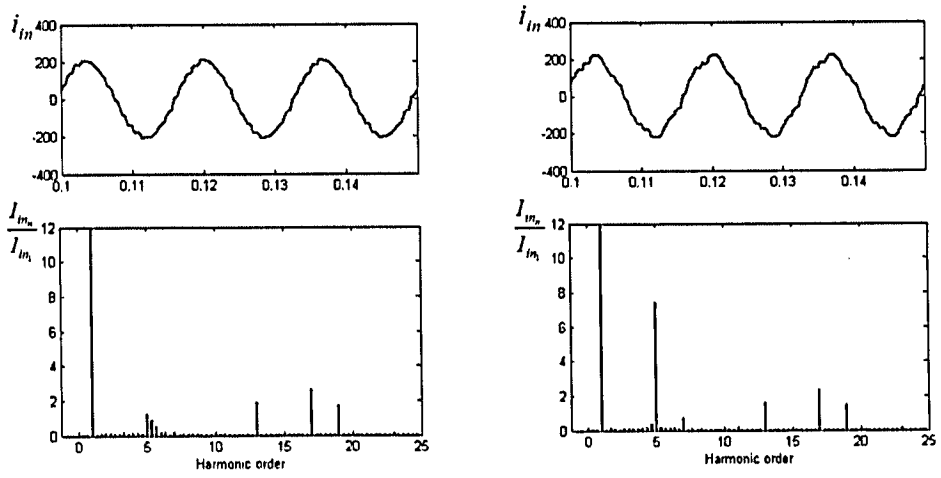
the motor is operated at its rated speed. It can be observed that the 5^{th} harmonic is highly excited when the input filter capacitor is equal to 0.45pu.

In summary, the input filter capacitor does not have a considerable effect on the dc ripple value provided that the input filter resonant mode is not excited. The input capacitor value should be designed to avoid the input LC resonance with consideration of the resonant frequency variation caused by the dc inductance.

2) Output filter capacitor

In this section, the effect of the output capacitor on the dc current ripple is investigated. For this purpose, the capacitance is varied in the range of 0.35 to 0.55pu. Using the developed steady state simulation model, the value of the dc ripple is calculated correspondingly.

The investigation is conducted under different output frequencies to observe the ripple at different motor speeds. The output frequency f_s is selected to be equal to 30, 40, 50 and 60Hz. For each operating condition and output filter capacitor value, the rectifier and the inverter firing angles, θ_{rcc} and θ_{inv}, are calculated and applied to the model.



(a) C_i=0.4pu (b) C_i=0.45pu

Figure 3.12: Input line current FFT analysis , f_s=60Hz

Fig. 3.13 shows the results of this investigation. The curves of dc current ripple versus the input capacitance are relatively smooth, and do not reflect the possible LC resonance caused by the output capacitor and motor inductances. This is because the induction motor's equivalent resistance provides damping into the system.

Although the variation of the current ripple for different output capacitors is limited, the results show no consistent relationship between the filter capacitance and the dc current ripple for different output frequencies. This inconsistency is due to the fact that the phase displacement between the dc link voltages, v_{dc-rec} and v_{dc-inv}, varies regarding to θ_{rec} and θ_{inv}, which changes the shape of the voltage across the dc link inductance.

3.4.3 Effect of Output Frequency on DC Current Ripple

As can be noted from previous investigations, the dc link current ripple is affected by the drive output frequency. In order to further study this effect , the drive system is examined for

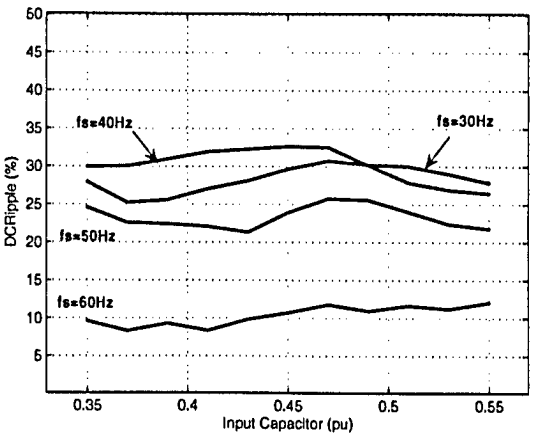


Figure 3.13: Effect of output filter capacitor on the dc current ripple

different loading conditions with different output frequencies. The speed of the motor varies from 0.5pu to 1 pu by varying the inverter output frequency from 30Hz to 60Hz accordingly.

The inverter PWM scheme is shown in Fig. 2.12, where the SHE modulation technique is used. The maximum switching frequency is 420Hz. The inverter firing angle θ_{inv} is calculated from the FOC scheme as was discussed in Chapter 2. On the rectifier side SHE scheme with seven pulses is used and the switching frequency is constantly kept at 420Hz. The rectifier firing angle θ_{rec} varies according to the inverter output frequency such that the voltage to frequency ratio V_s/f_s is kept constant.

Fig. 3.14 illustrates the calculated values for the dc ripple under different output frequencies. It can be revealed that the dc current ripple generally increases with the decrease of output frequency. This is caused by the increased peak voltage across the dc inductance at lower inverter output frequency. Although the average dc voltages at both sides of the dc inductance, V_{dc-rec} and V_{dc-inv}, are equal, the dc current ripple is related to their instantaneous values. Since the input line voltage is fixed, the peak of v_{dc-rec} remains the same. While the peak value of v_{dc-inv} decreases proportionally to the output frequency. As a result, the peak voltage drop across the dc inductance increases, leading to a larger dc

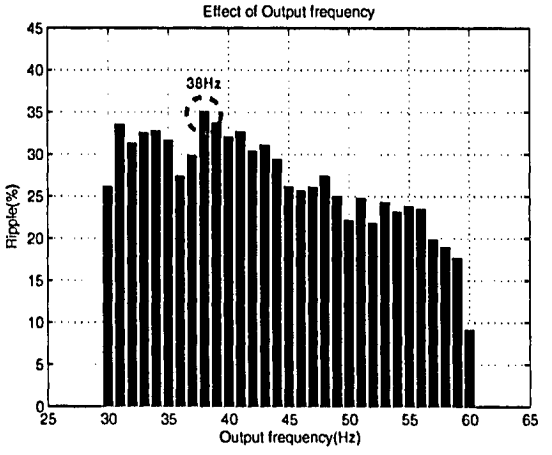


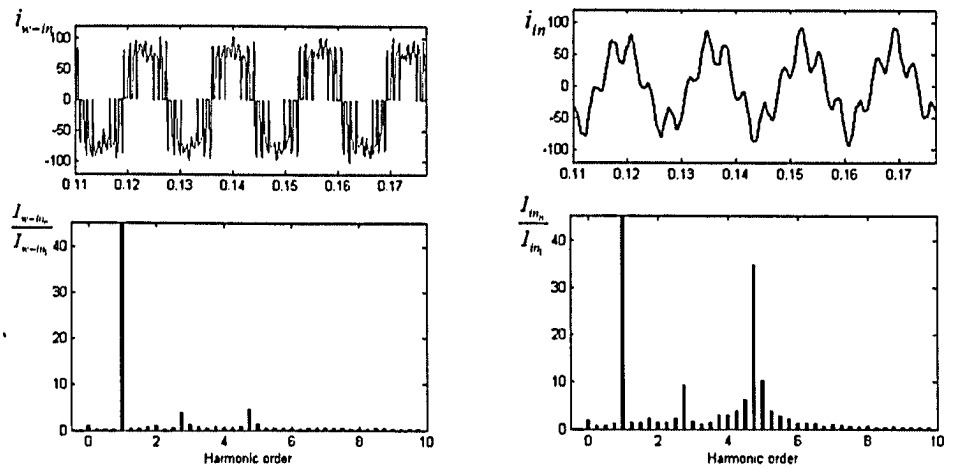
Figure 3.14: Dc ripple at different inverter output frequencies (C_i=0.5pu,L_{in}=0.1pu,L_{dc}=0.8pu)

current ripple.

The dc current ripple in Fig. 3.14 is also related to other factors. As mentioned previously, the rectifier and the inverter firing angles change under different output frequencies, which in turn changes the dc voltages phase displacement. In addition, by varying the output frequency, the number of pulses in the inverter switching pattern alters which also affects the shape of the dc link current.

The maximum ripple value in Fig. 3.14 occurs at the output frequency of 38Hz. This is mainly caused by the drive input LC resonance. Due to the dc ripples, some non-integer harmonics will be introduced to the input side. If the input LC resonant frequency is close to one of these harmonics, the input LC resonance will be excited. At the inverter output frequency of 38Hz, the harmonic current with a frequency of 290Hz (4.83pu) is amplified by the rectifier input LC resonance. The input current waveforms and their harmonic components are shown in Fig. 3.15, where it verifies that the input resonant frequency is around 290Hz.

Varying the input resonant frequency will affect the frequency at which the maximum



(a) Rectifier input current (i_{w-in}) (b) Input line current (i_{in})

Figure 3.15: Input Current waveforms, f_s=38Hz

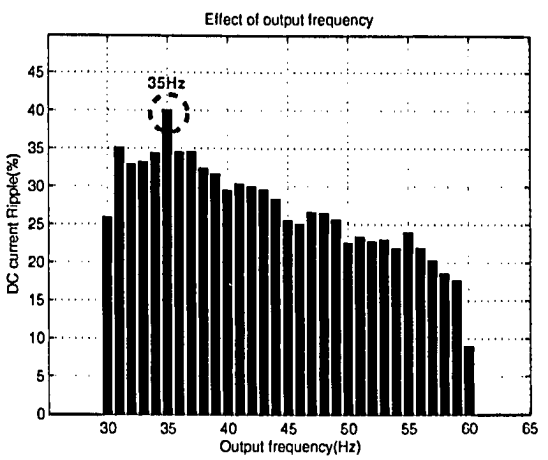
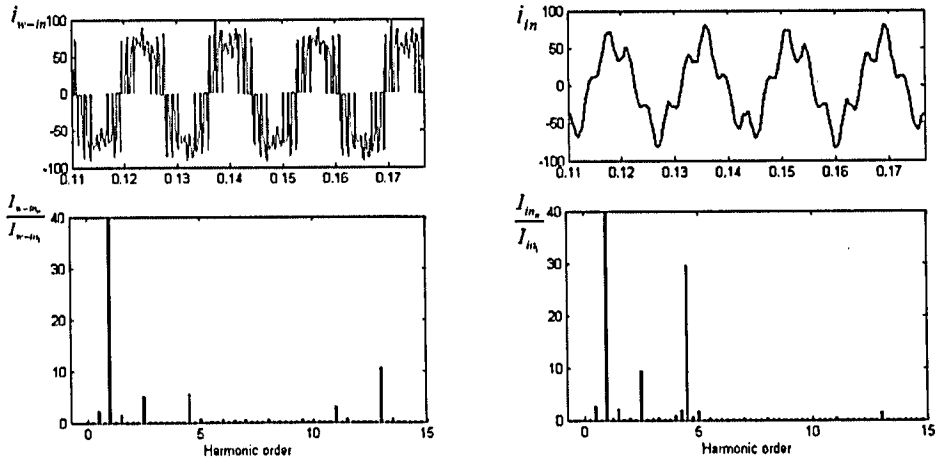


Figure 3.16: Dc ripple at different inverter output frequencies (C_i=0.5pu,L_{in}=0.12pu, L_{dc}=0.8pu)



(a) Rectifier input current (i_{w-in})

(b) Input line current (i_{in})

Figure 3.17: Input Current waveforms, f_s=35Hz

ripple occurs. For instance, Fig. 3.16 shows the simulation results where the input line inductance L_{in} is 0.12pu instead of 0.1pu in the previous case. The maximum dc ripple current happens at 35Hz. The input resonant frequency, which is excited in this case, is equal to 4.5pu (270Hz). This is verified by the FFT analysis of the input current is shown Fig. 3.17.

3.5 DC Choke Selection

To design the dc choke, the calculation of dc current ripple is necessary. However, due to the complexity of the drive system, deriving an accurate and general equation for the dc ripple calculation seems unfeasible.

In this section, a user friendly software simulation package is developed to assist the design of the dc link inductance. The drive and motor parameters, the output frequency range and the maximum acceptable dc current ripple are defined by the user. The software package then uses these input values and automatically runs the developed steady state

model to find the minimum dc link inductance that satisfies the specified ripple constraint.

3.5.1 Simulation Block Diagram

The block diagram of the simulation package is shown in Fig. 3.18. The simulation package is base on Matlab Simulink, which loads the parameters of the drive system and then calculates the ripple value under various operating condition. The maximum acceptable value for the dc current ripple and the range of the drive output frequency are also given to the program as its input.

In each operating condition, all the required variables in the drive system, such as the motor slip, inverter and rectifier switching patterns and their phase angles are calculated by the Matlab program and applied to the simulation model automatically.

Fig. 3.19 shows the user interface of this software package. The computer program runs the steady state simulation model for all the specified output frequencies with a preset value of the dc link inductance. The corresponding values of the dc ripple are calculated and the frequency at which the maximum ripple occurs will be identified.

Different values of the dc link inductance will then be tested in the simulation program, where the output frequency is set to the frequency found in the first part (the frequency

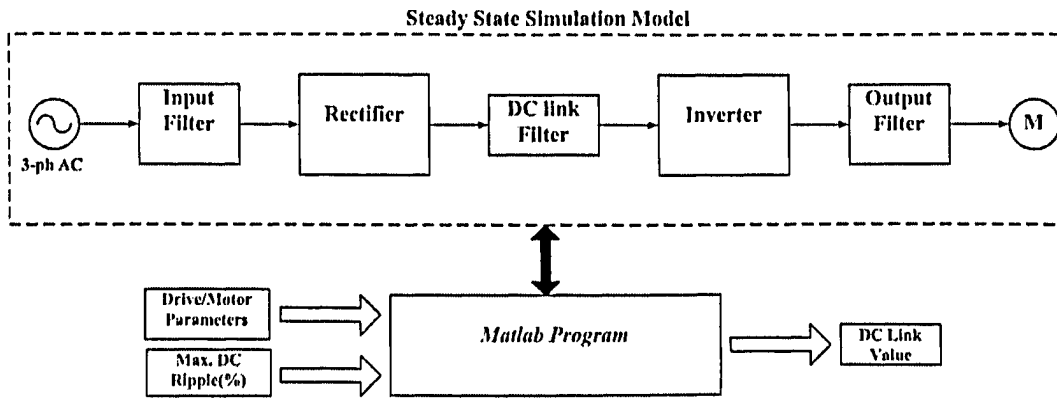


Figure 3.18: Block diagram of the developed computer program

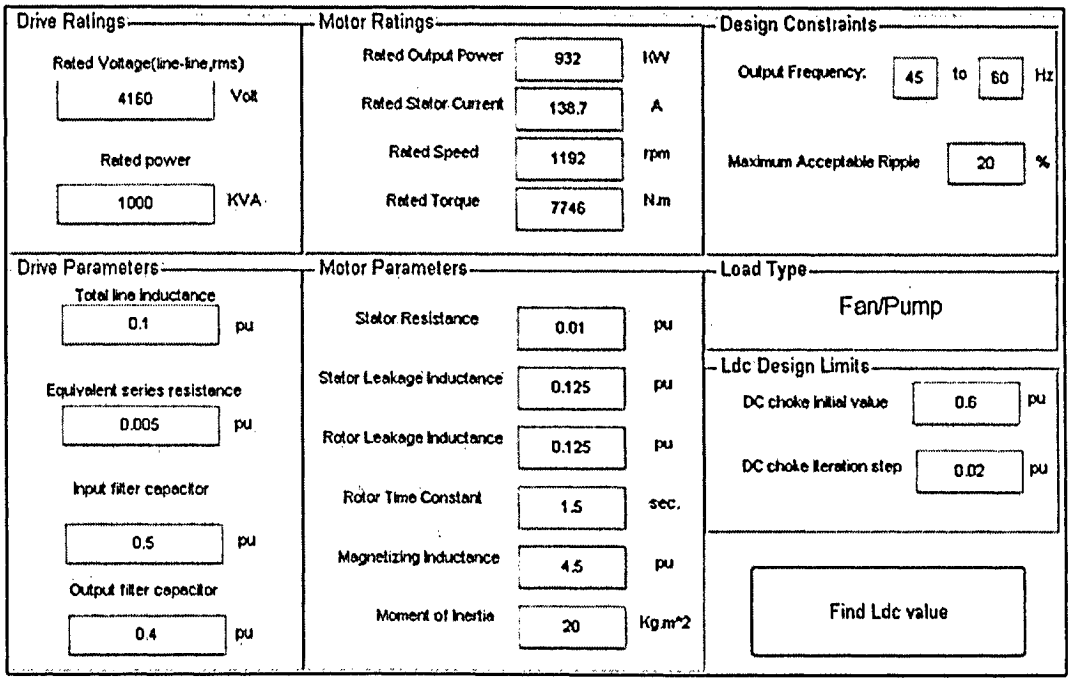


Figure 3.19: Computer package user interface

that the maximum dc current ripple occurs). The preset value of the dc inductance and its increment step in each iteration can be defined by the user. The dc current ripple is obtained in each iteration and the minimum dc choke which satisfies the ripple constraint will be the output of the program.

3.5.2 Design Example

In this section, the developed software package is employed to find out the optimized value of the dc inductance in the drive system with parameters given in Tables 3.1 and 3.2.

The drive output frequency is programmed to vary from 45Hz to 60Hz. This range is selected because the normal operating condition of the drive system for fans and pumps is from 80% to 100% of the rated speed. The drive would operate at lower speeds only for a very short period during the start-up process. The acceptable maximum ripple value Rip_{max}

is set to 20%, and the initial dc inductance is chosen as 0.6pu with a iteration step of 0.02pu.

The program runs the Simulink model with the initial dc inductance at the defined output frequency range. The ripple is calculated at each frequency and the largest ripple is found to happen at 48Hz. This operating speed is then chosen, under which the simulation model will be run with different dc choke values. The minimum L_{dc} that satisfies the maximum ripple limit (Rip_{max}<20%) is the output of the program, which is equal to 1.09pu in this case.

In order to better illustrate the proper dc link inductance in a wider range of operating speed, the minimum dc choke is calculated for output frequencies from 30Hz to 60Hz. Fig 3.20 illustrates the results. It can be seen that the designed dc choke in the rated condition (f_s=60Hz) to satisfy the maximum ripple constraint (Rip_{max}<20%) is fairly small and equal to 0.51pu. As expected, this value increases for lower operating frequencies. The maximum dc choke required over the frequency range is increased to 1.32pu at f_s=37Hz (compared to the 1.09pu with output frequency range of 45-60Hz). Considering the fact that the drive would operate in this frequency for only a short period of time, choosing this value as the dc choke results in an over designed inductance.

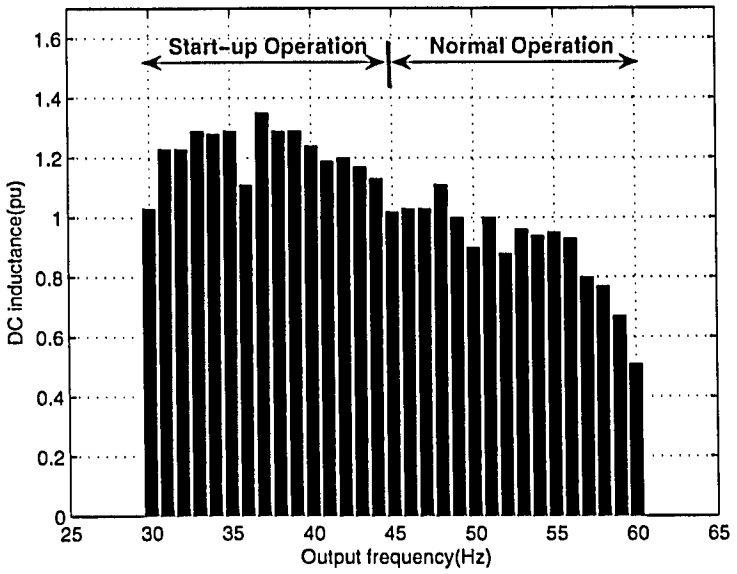


Figure 3.20: Designed dc link choke at inverter output frequency range from 30Hz to 60Hz

3.6 Conclusion

The developed steady state model of a CSI-fed drive has been used in this chapter for a thorough investigation on the characteristics of the dc current ripple and its relationship with different system parameters and loading conditions. In order to optimize the dc choke value, a user-friendly simulation package is developed, which can be used to determine the minimum possible dc inductance that satisfies the dc ripple requirements. The work in this chapter can be summarized as follows:

- The characteristics of the dc link current and its ripple are introduced. Relationships between the dc current frequency and the drive input and output fundamental frequencies are discussed. Moreover, the effect of the dc link inductance on the input resonant frequency is investigated.

- The steady state simulation model is used to study the dc link current ripple under

different drive operating conditions. Effects of input, output and dc link filters on the dc current ripple are studied. The dc current ripple under different motor speeds is also investigated.

- A user friendly computer software package is developed to facilitate the dc choke optimization. Parameters of the drive and induction motor are loaded to the package as inputs. According to the user defined maximum dc current ripple value and the drive output frequency range, the program can automatically find the minimum dc link inductance.

Chapter 4

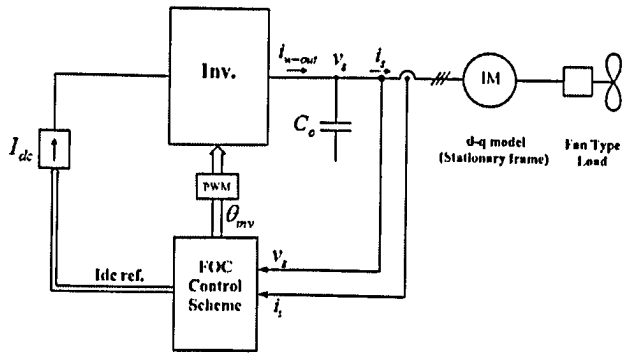
Experimental Verification

4.1 Introduction

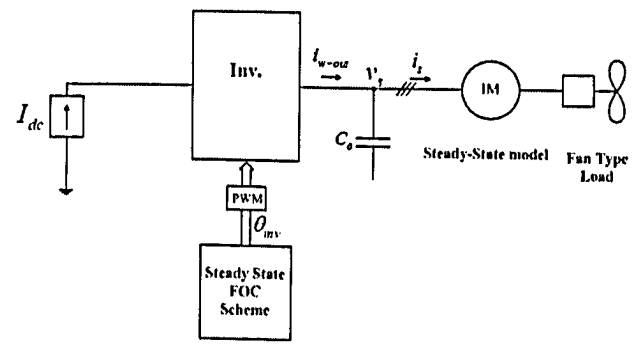
In this chapter the steady state models developed in Chapter 2 are verified. First, the steady state simulation model including the simplified steady state FOC scheme and a steady state induction motor model is compared to a dynamic simulation model, where a d-q axis dynamic induction motor model and the entire FOC control loops are used. Secondly, a low voltage current source drive system test setup is used for experimental verification. The results obtained from the experiments are compared with those simulated by the developed steady state drive system model.

4.2 Verification of Induction Motor Model and FOC Scheme

To investigate the accuracy of the developed steady state model for the induction motor and the simplified steady state FOC scheme, both dynamic and steady state models of the induction motor are controlled by a current source inverter with FOC control scheme and the results are compared in different operating conditions. Fig. 4.1 shows the block diagrams of these two simulation models.



(a) CSI dynamic model



(b) CSI steady state model

Figure 4.1: CSI simulation models

In Fig. 4.1(a), the dynamic model of the induction motor (of Fig.2.5) is connected to a current source inverter. The FOC scheme is employed for proper motor speed control. The inverter output voltage and current are the control system feedback variables and the dc current reference and the inverter firing angle θ_{inv} are the FOC scheme outputs.

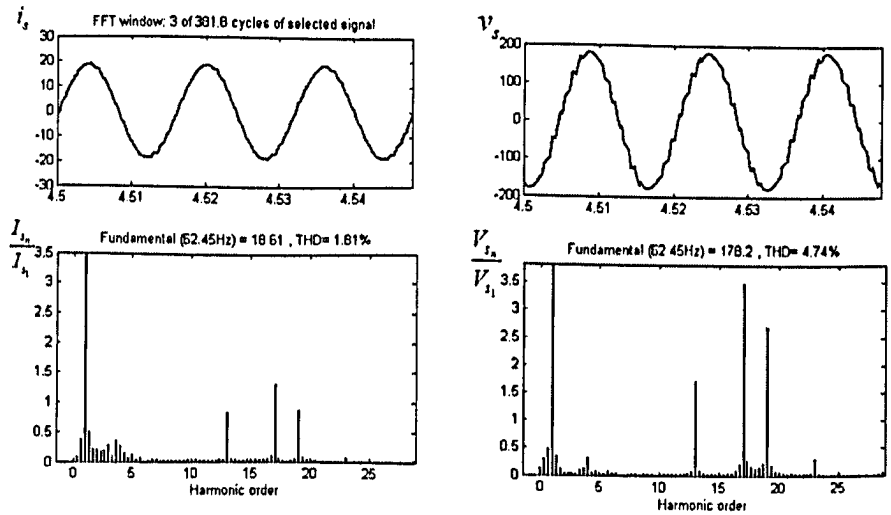
In the steady state simulation model shown in Fig. 4.1(b), the steady state induction motor model (Fig. 2.7) is used. The developed simplified steady state FOC scheme is also employed, where the dc current and inverter firing angle θ_{inv} are directly calculated at each operating condition as discussed in Chapter 2. In both models, SHE modulation scheme is used for the inverter, and the mechanical load is of a fan/pump type load.

To compare the two models, the motor speed n_r is set to 25%, 50%, 75% and 100% of the rated speed. The corresponding mechanical torque T_L is applied at the respective speeds. The inverter output current i_{w-out} and voltage v_s from both models at each speed are compared. The resultant rms values are summarized in Table 4.1. As expected, V_s and I_s become smaller as the motor speed and mechanical torque decreases. This is because the required drive output power is decreased. The two sets of results obtained from the two models match very well, which verifies the accuracy of the developed steady state induction motor model and the simplified FOC control scheme.

Figs. 4.2 and 4.3 show the drive output voltage and current waveforms as well as their FFT analysis at the rated operating condition (f_s=60Hz). As can be seen from these figures, the SHE PWM scheme can eliminate the 5^{th}, 7^{th} and 11^{th} harmonic components in the inverter output current. The higher order current harmonics are attenuated by the inverter output filter, which makes the output current close to sinusoidal. This low THD current waveform in turn ensures the near sinusoidal inverter output voltage. Considering the closely matched results from both models, the steady state model of the induction motor and the simplified steady state FOC scheme can be reliably used in the modeling of the drive system in the steady state condition.

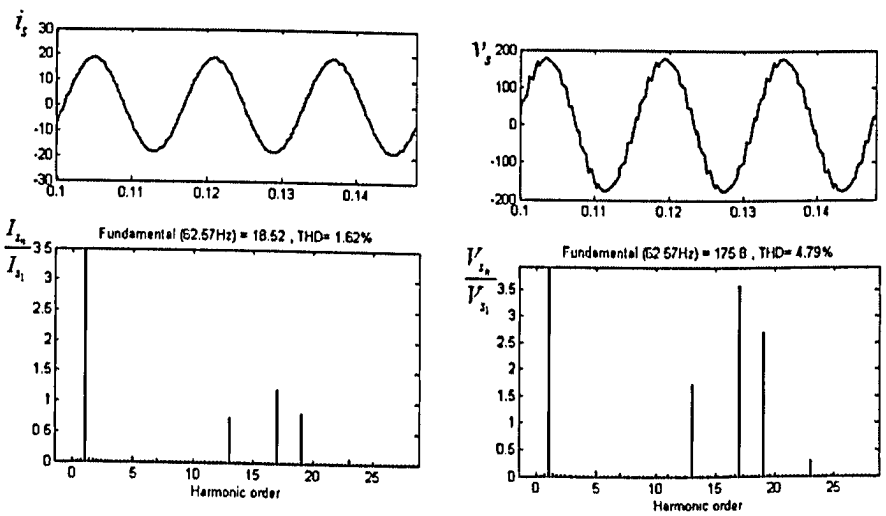
Table 4.1: Simulation verification results

n_r%	T_L%	θ_{inv}%	Dynamic model			Steady-State model		
			I_{w-out}(A)	V_s(V)	I_s(A)	I_{w-out}(A)	V_s(V)	I_s(A)
100	100	87.7°	15.6	178.2	18.67	15.55	175.8	18.52
70	50	59°	9.42	120.3	11.88	9.42	122.2	11.94
50	25	31.43°	7.89	84.03	9.49	7.88	84.72	9.51
25	6.25	52.42°	13.03	50.6	13.42	13	48.5	13.36



(a) Motor line current (b) Inverter output voltage

Figure 4.2: The simulation results using dynamic model ($f_s = 60Hz$)



(a) Motor line current (b) Inverter output voltage

Figure 4.3: The simulation results using steady state model ($f_s = 60Hz$)

4.3 Drive Model Verification

Experimental investigation is also carried out to verify the proposed steady state simulation model. The experiments are conducted on a low voltage current source drive system setup at Rockwell Automation Canada. In the experiment, the drive input, output and dc link circuit waveforms are measured and compared with the ones obtained from the proposed steady state simulation model.

4.3.1 Test Setup Configuration

The block diagram of the drive system under test is shown in Fig. 4.4, where the same system configuration as the simulation model used in previous chapters is employed. The input voltage of the drive is 480V, which is provided by a distribution transformer. This transformer also serves as a isolation transformer for motor common mode voltage elimination as discussed in Chapter 1.

The input filter consists of the filter inductance L_{in} and the filter capacitor C_i. The filter inductance is added to the system for input current THD reduction, while the input filter capacitor is required by the current source drive as discussed in previous chapters. The dc link inductance L_{dc} is responsible for limiting the dc current ripple. At the drive's output, a

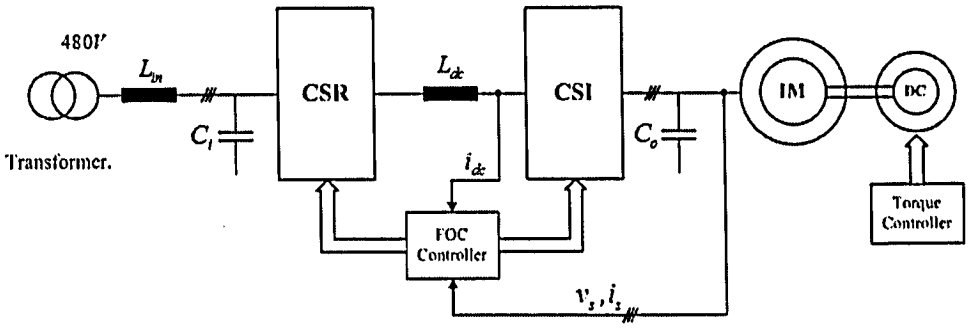


Figure 4.4: 30hp test setup block diagram

Table 4.2: Experimental drive setup parameters

Drive Ratings: 36 A, 480 V, 60 Hz		
R_{in}	Input Line Resistance	0.01 pu
L_{in}	Input Line Inductance	0.12 pu
C_i	Input Filter Capacitor	0.568 pu
L_{dc}	DC Choke	0.846 pu
C_o	Output Filter Capacitor	0.467 pu

three phase filter capacitor C_o is connected between the inverter and the low voltage (460V, 30hp) induction motor. The ratings and parameters of the low voltage drive system setup and the induction motor are given in Tables 4.2 and 4.3, respectively.

A load with adjustable torque T_L is applied to the induction motor. This load torque is provided by a dc generator, which is mechanically coupled to the induction motor. The desired mechanical torque is applied to the induction motor by adjusting the generator's armature current.

In order to control the speed of the induction motor, FOC scheme is employed for the current source drive system. With the reference drive output frequency, the FOC scheme generates proper gate signals for the switching devices in the rectifier and the inverter. The drive input fundamental frequency is 60Hz, and the rectifier is controlled with 7-pulse SHE scheme. On the inverter side, SHE and TPWM modulation schemes are used, where the maximum switching frequency is limited to 420Hz as shown in Fig. 2.12.

4.3.2 Experimental Results and Comparisons

1) PWM Rectifier Test

The PWM current source rectifier of the drive system is investigated experimentally in this section. The block diagram of this experiment is shown in Fig. 4.5. In order to operate

Table 4.3: Induction motor parameters

Name Plate Data: 30 Hp, 460 V, 36 A, 60 Hz		
R_s	Stator Resistance	0.0349 pu
L_{ls}	Stator Inductance	0.15 pu
L_{lr}	Rotor Inductance	0.15 pu
τ_r	Rotor time constant	0.6 sec
L_m	Magnetizing Inductance	3.46 pu
n_r	Rated Speed	1775 rpm

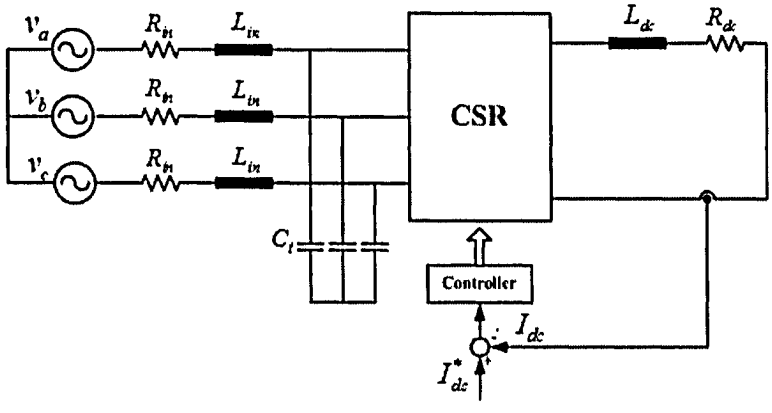
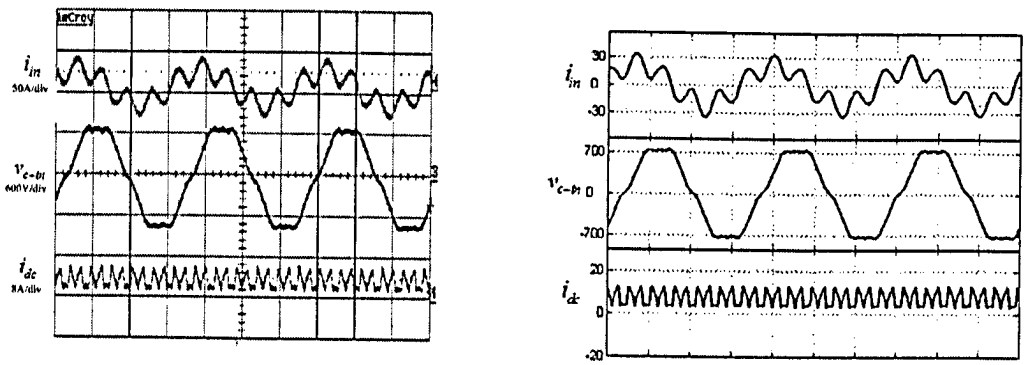


Figure 4.5: Rectifier test block diagram

the drive system only as a PWM rectifier, the dc link circuit is shorted through by inverter bridge (e.g. turn on S_1 and S_4 at the same time).

To examine the PWM rectifier and its control scheme, different reference values are manually set for the dc link current (i.e. I_{dc}=0.2,0.3 and 0.4pu) in the experiment. The controller regulates the dc current to the desired value by adjusting θ_{rec}. The input current, voltage and dc link current waveforms are then captured.

Similar investigation with the same dc current reference is carried out in the simulation using the developed steady state drive system model. The rms values of the results taken



(a) experimental results (b) simulation results

Timebase:5ms/div

Figure 4.6: Rectifier test results from a 30hp drive with $I_{dc} = 0.2$pu

from both the experimental test setup and the simulation model are summarized in Table 4.4. It can be seen that under each dc current reference, the fundamental component of the rectifier input current I_s, input voltage V_{c-in} and the rectifier firing angle θ_{rec} from both simulation and experiment are almost the same. Note that due to the absence of dc load in the rectifier test (the dc link circuit is shorted), the rectifieroutput power in the simulation and experiment is relatively small. As a result, small input power is required which makes the values of θ_{rec} close to 90° as shown in Table 4.4.

Fig. 4.6 shows the measured and simulated waveforms of rectifier input current i_{in}, input capacitor voltage v_{c-in} and dc link current i_{dc}. It can be noticed from Fig. 4.6(a) that the

Table 4.4: Rectifier test results

I_{dc}		θ°_{rec}		I_{in_1}(A)		V_{c-in_1}(V)	
(pu)	(A)	Experiment	Simulation	Experiment	Simulation	Experiment	Simulation
0.2	7.2	89.3	89.4	15	16	497	500
0.3	10.8	89.1	89.2	11	12	496	499
0.4	14.4	89	88.9	7	9	497	497

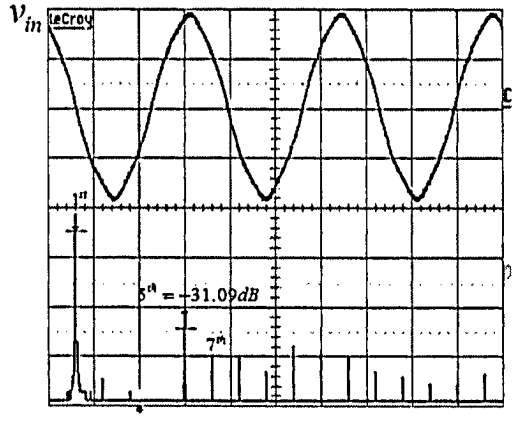


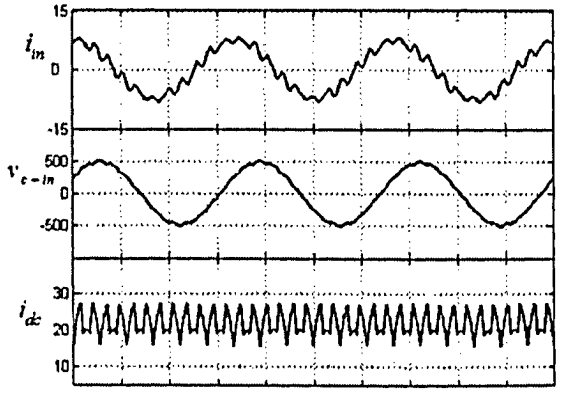
Figure 4.7: Input voltage source of the experimental test setup

drive input current i_{in} is oscillatory, and it contains some low order harmonic components. This is due to the fact that the source voltage v_s is not purely sinusoidal, and its harmonic components are amplified by the drive input LC filter in the experiment. The experimental source voltage has been measured and shown along with its FFT analysis in Fig. 4.7, where the largest harmonic (the 5th harmonic) has a value of -30dB (3.16% of fundamental).

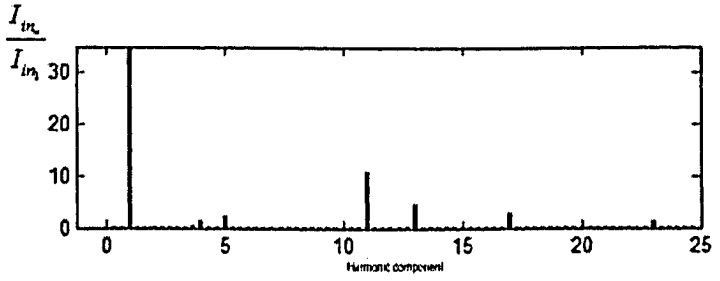
In order to examine the simulation model and to fairly compare its results with the ones from the experimental setup, similar 5^{th} order harmonic ($\sim$ -30dB) is added to the input source in the simulation. As shown in Fig. 4.6(b), almost identical input line current and capacitor voltage are obtained in the simulation. The matched current and voltage waveforms result in closely matched dc link current ripple in both the simulation and experiment as shown in Figs. 4.6 (a) and (b). This indicates that the developed steady state model can accurately calculate the dc current ripple, which is important for the dc choke design.

Finally, the simulation model is also examined with a pure sinusoidal input source and the results are shown in Fig. 4.8. As expected, without the source voltage harmonics, there is no noticeable low order harmonic components in the input line current, as the SHE modulation scheme has eliminated the low order harmonics introduced by the rectifier

switching waveform.



(a) waveforms



(b) FFT analysis of i_s

Figure 4.8: Rectifier results without input voltage harmonic

2) Complete Drive System Test

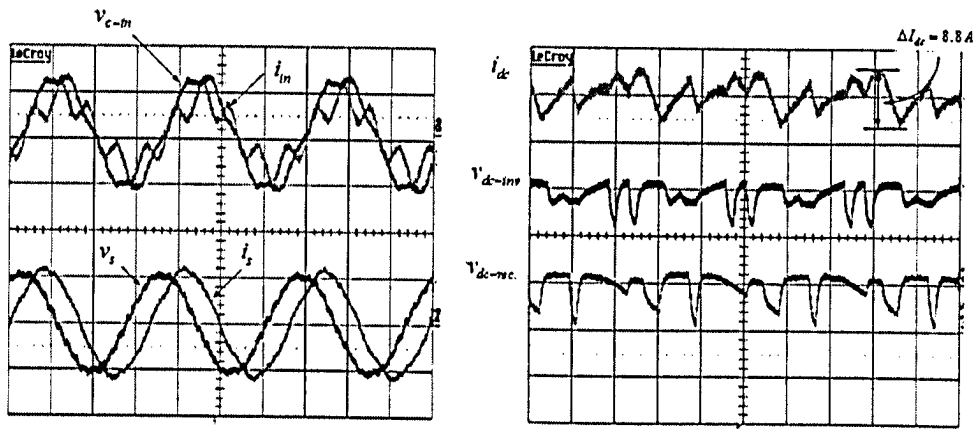
The complete drive system, including the rectifier, the inverter and the FOC control scheme is also investigated in the experiment. As shown in Fig. 4.4, the drive system is connected to an induction motor operating at different speeds. The mechanically coupled dc generator applies adjustable torque to the motor in each operating condition.

The drive setup is tested at the output frequencies of 30,45 and 60Hz with corresponding mechanical torque of 0.9, 0.87 and 0.86pu, respectively. Under each operating condition, the waveforms on the line side, motor side and on the dc link are measured. For the purpose of comparison, the steady state simulation model is also run under the same conditions. The results from the experiment and the simulation at rated output frequency of 60Hz are compared in Figs. 4.9 and 4.10. The waveforms from other operating conditions are shown in Appendix B.

As shown in Figs. 4.9 and 4.10, the drive input line current contains large percentage of the 5^{th} harmonic component. This distortion is introduced by the non-ideal input source voltage as discussed earlier. Due to SHE modulation and the filtering effect between the CSI output capacitors C_o and the motor leakage inductance, the drives output voltage v_s and current i_s are very close to sinusoidal with low THD. The phase shift between i_s and v_s is caused by the motor lagging power factor. The shape of the dc link current is related to the shape of the dc link voltages and their relative instantaneous values.

Comparing Figs. 4.9 and 4.10, a close match between the experimental measurement and the simulation results is obtained. The nearly identical dc current ripple values from both the experiment and steady state model simulation indicate the accuracy of the ripple calculations in Chapter 3.

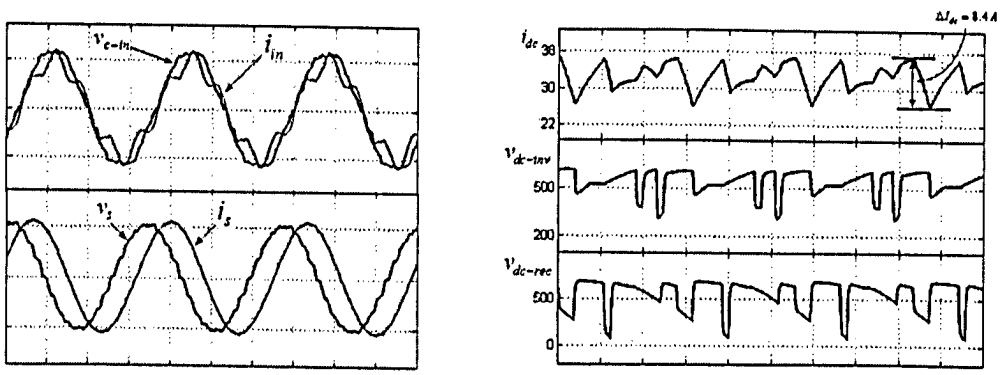
Experiment and simulation results under all three operating conditions are summarized in Table 4.5, where the rms values of the drive input and output current/voltage as well as the rectifier and inverter phase angles are listed. Note that θ_{rec} in Table 4.5 is calculated with respect to the voltage across the input capacitor v_{c-in}. As mentioned before, the rectifier switching pattern is fixed to 7-pulse SHE, whereas different number of pulses are used in the inverter side in order to control the switching frequency. As shown in Table 4.5, the rms value of v_{c-in} is almost constant in all conditions, while the output voltage changes



(a) Input/Output current and voltage (b) DC link current and voltages

i_s:40A/div,i_{in}:50A/div,i_{dc}:8A/div,Voltage traces:600V/div,Timebase:5ms/div

Figure 4.9: Experimental results from a 30hp drive ($f_s = 60Hz$)



(a) Input/Output current and voltage (b) DC link current and voltages

i_s:40A/div,i_{in}:50A/div,v_{in}:600V/div,v_s:600V/div,Timebase:5ms/div

Figure 4.10: Simulation results ($f_s = 60Hz$)

Table 4.5: Drive test results

f_s(Hz)	T_L(pu)	*Inv. Pattern*	$\theta^\circ_{rec.}$	θ°_w	Simulation Results:				Experimental Results:			
					V_{c-in} (V)	I_{in} (A)	V_s (V)	I_s (A)	V_{c-in} (V)	I_{in} (A)	V_s (V)	I_s (A)
60	0.9	SHE,N_p=7	30	106	492	24	434	29	489	26	439	32
45	0.87	SHE,N_p=9	50.4	91	484	17.5	340	28	492	19	336	31
30	0.86	SHE,N_p=13	65.1	81	475	12	223	27.5	494	14	227	31

proportional to the output frequency. Once again, a close match between the steady state model simulation and the experimental measurement is obtained in Table 4.5.

As a final note, the dc link voltage waveforms, v_{dc-rcc} and v_{dc-inv}, are chopped due to the rectifier and the inverter switching action. However, in the experimental results, these waveforms are measured through a low pass filter in order to eliminate the measurement noises; thus their rising and falling edges are not as sharp as expected. The time constant of this low pass filter is close to $20\mu sec$. A similar filter has been placed in the simulation model to achieve matching results.

4.4 Conclusion

In this chapter, the steady state drive system model developed in Chapter 2 and the dc current ripple analysis provided in Chapter 3 have been verified by dynamic model simulations and experiments on a 30hp laboratory drive system. The verification can be summarized as follows:

- Verification of proposed steady state motor model and simplified FOC control by system dynamic simulation. The developed steady state induction motor model and the simplified steady state FOC control scheme is examined. The results are compared

with those obtained from the complete dynamic simulation model. A close match is achieved.

- Verification of proposed steady state drive system model by experiment. Experimental results obtained in a 30hp CSI-fed drive system setup further verify the accuracy of the proposed steady state drive system model and the dc current calculation. Two different experiment tests, the rectifier test and the complete drive system test, are performed at different motor speeds and loading conditions. A close match between the steady state simulation results and the experimental measurement is obtained.

Considering the consistency of results from the steady state simulation model and those from the practical system measurements, the accuracy of the developed steady state drive model is verified. Moreover, the dc current ripple values from the simulation and experiment in different conditions are well matched. This indicates that the developed steady state drive system model can be reliably used for the dc link inductance design.

Chapter 5

Conclusion

This thesis is devoted to study and investigate the behavior of the current source drive system operating under the steady state conditions. The main objective of this investigation is to optimize the dc link inductance, which is one of the most expensive components in the current source drive system. The thesis can be divided into two parts:

The first part concentrates on the modeling of the drive system in steady state operation mode. Different functional blocks of the system, such as field oriented control (FOC) schemes, induction motor, and mechanical load are simplified, and their steady state simulation models are developed.

The second part of this thesis is focused on the investigation of the dc link circuit and the optimization of dc link inductance using the developed steady state drive system model. Effects of the dc link inductance on the drive input LC resonances is first investigated. The dc current ripple value is then calculated in different operating conditions. The effects of various components of the drive system, such as the dc link inductance, input and output filter capacitors and drive output frequency, on the dc current ripple are studied. The dc choke optimization is achieved by determining the minimum possible dc inductance that satisfies the dc current ripple requirement using a developed software package.

The main contributions of this thesis is summarized as follows:

The complicated closed-loop FOC scheme of the CSI-fed drive system is avoided for the developed steady state drive system model. With the developed steady state model, the challenging and time consuming task of FOC control parameters tuning for different operating conditions is not required. Moreover, the instability problem of the dynamic drive model caused by the ill-tuned control parameters is completely avoided with the steady state model.

The simulation time of the drive system model has been substantially reduced. To investigate the steady state performance, the motor is not required to start from standstill. Instead, the steady state results can be directly derived from the developed model at any given motor speed. In addition, without the feedback control blocks and their complex mathematical calculations in each time step, the simulation time of the developed steady state model is further reduced.

The effects of the dc circuit on the drive input resonant frequency has been investigated. It is revealed that the rectifier input LC resonance is not only defined by the input LC filter, but it is also affected by the dc link circuit. Due to the existence of dc inductance, the input resonance frequency is higher than the LC filter cutoff frequency. For drive system design, the effect of the dc inductance on input LC resonances must be considered.

The effects of different operating conditions and various system components on the dc current ripple has been studied. It has been found that the dc current ripple is related to various components of the drive system such as the dc link inductance, input and output filter capacitors, and drive output frequency. The dc link inductance, the rectifier input resonance and the inverter output frequency are three major factors that influence the dc current ripple.

A user friendly simulation software is developed in order to optimize the dc link inductance. The simulation software is developed using the steady state model developed in this thesis. The software features very short simulation time, no system stability problems, no controller parameter tuning, and no motor start-up process. For a given dc current ripple, the software will automatically find the minimum value of dc link inductance that can satisfy the dc ripple requirements. In the developed software package, the motor and drive parameters, the motor operating speed range and the dc current ripple requirement are the user inputs, and the optimized dc link inductance is the output.

Following are several topics recommended for **future study:**

- Further studies on the steady state behavior of the system. Besides the dc current ripple, effects of the system components on other parameters such as the drive input and output THD can be studied. This can be carried out using the steady state system model developed in this thesis.

- Improvement on the computer simulation package. The design of other system components such as the input and output filter values and the most efficient PWM switching scheme can be programmed into the simulation package based on the certain design criteria such as minimum harmonic distortions at drive input and output.

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Appendix A

Rotor-Flux Calculation

The objective of the Rotor-Flux Calculation is to calculate the rotor flux vector $\vec{\lambda}_r$ so that the it can be aligned with the d-axis. Since θ_f is calculated and measured with respect to the stationary frame, the stationary model for the induction motor is used for the calculation:

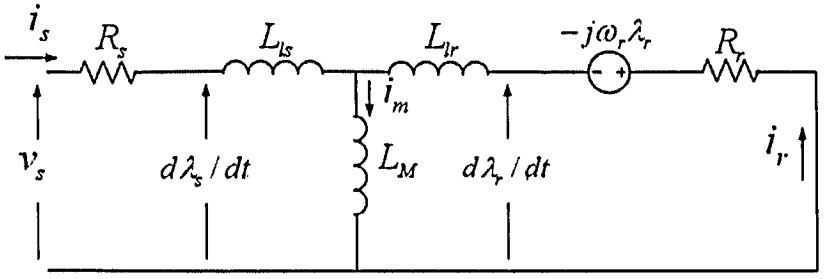


Figure A.1: Induction Motor model in stationary frame

Stator flux λ_s can be calculated using the input voltage and current d-q components and the motor parameters:

$$\begin{cases} \lambda_{ds} = \int(\vec{v}_{ds} - R_s\vec{i}_{ds})dt \\ \lambda_{qs} = \int(\vec{v}_{qs} - R_s\vec{i}_{qs})dt \end{cases} \tag{A.1}$$

from the flux linkage equations, the rotor flux can be calculated as:

$$\begin{cases} \lambda_{dr} = \frac{L_r}{L_m}(\vec{\lambda}_{ds} - \sigma L_s\vec{i}_{ds}) \\ \lambda_{qr} = \frac{L_r}{L_m}(\vec{\lambda}_{qs} - \sigma L_s\vec{i}_{qs}) \end{cases} \tag{A.2}$$

where $\sigma = 1 - (L_m^2/L_sL_r)$ and L_s, $L_r$and L_m are stator and rotor self-inductance and magnetizing inductance respectively.

Considering equation A.2, the value of the flux amplitude and it angle can be calculated:

$$\begin{cases} \lambda_r = & \sqrt{\lambda_{dr}^2 + \lambda_{qr}^2} \\ \theta_f = & \tan^{-1} \frac{\lambda_{qr}}{\lambda_{dr}} \end{cases} \tag{A.3}$$

Fig. A.2 shows the vector diagram of current and flux vectors used in rotor flux calculation. When the rotor vector λ_r and stator current i_s rotate one revolution in space, their d-q components in stationary frame change one cycle over time.

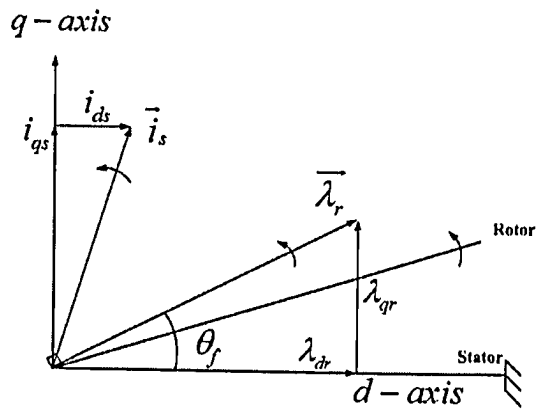


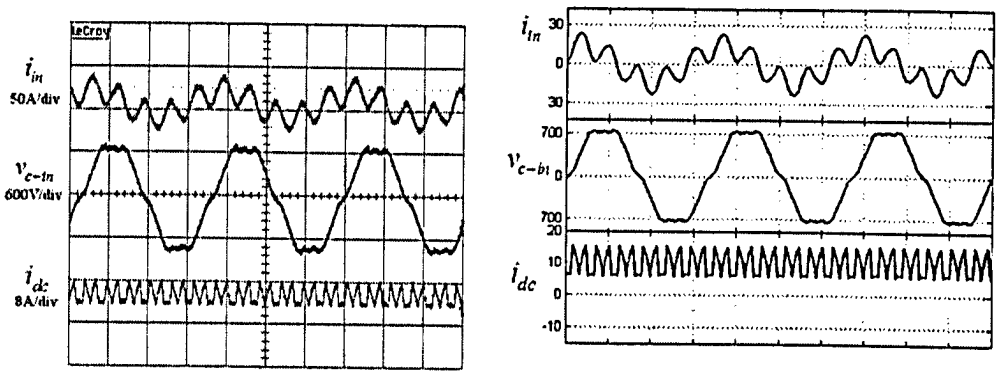
Figure A.2: Stationary frame vector

Appendix B

Experimental test results

The waveforms appended here are to compare the results taken from the experimental test setup and the ones from the simulation model. Figs. B.1-B.2 show the results for the rectifier test with the dc link circuit being shorted. The reference value for the dc current are equal to 0.3 and 0.4pu respectively.

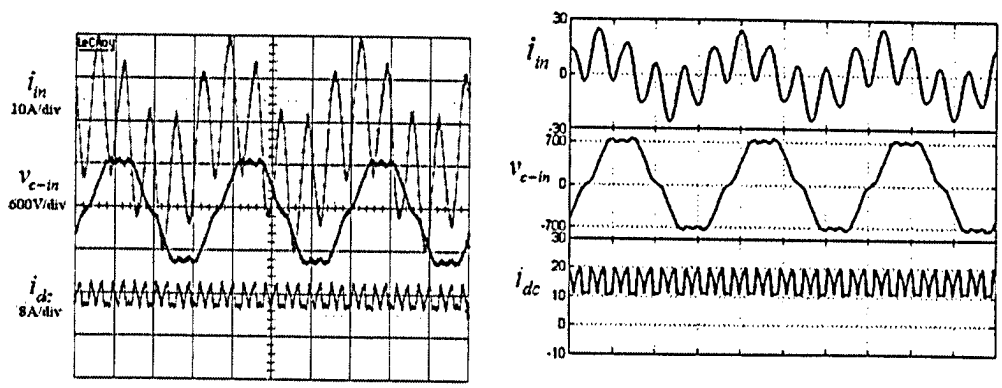
The results from the drive test are illustrated in Figs. B.3-B.6. This test has been performed in three different operating conditions: f_s=60Hz,,45Hz,30Hz. The results from the first test were discussed in Chapter 4. The results from the other two are shown here. The ripple value is also shown in both conditions. Considering the results, the accuracy of the simulation model can be concluded.



(a) experimental results

(b) simulation results

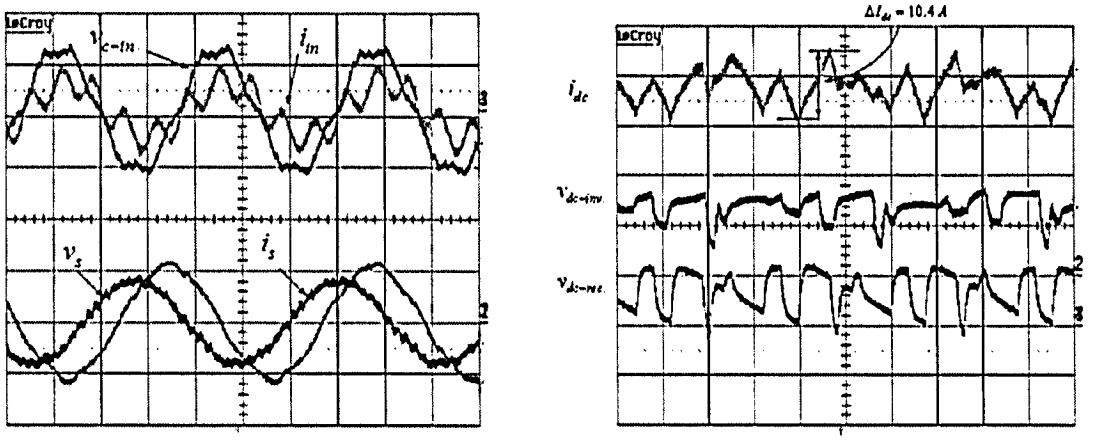
Figure B.1: Rectifier Test results for $I_{dc} = 0.3$pu



(a) experimental results

(b) simulation results

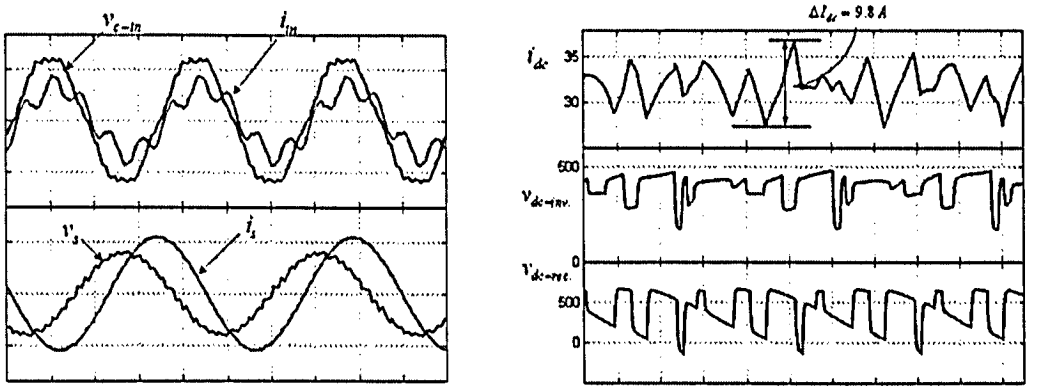
Figure B.2: Rectifier Test results for $I_{dc} = 0.4$pu



(a) Input/Output current and voltage (b) DC link current and voltages

i_s:40A/div,i_{in}:50A/div,i_{dc}:8A/div,Voltage traces:600V/div,Timebase:5ms/div

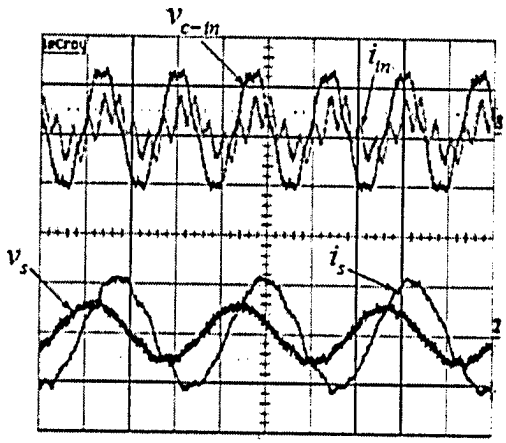
Figure B.3: Drive test experimental results ($f_s = 45Hz$)



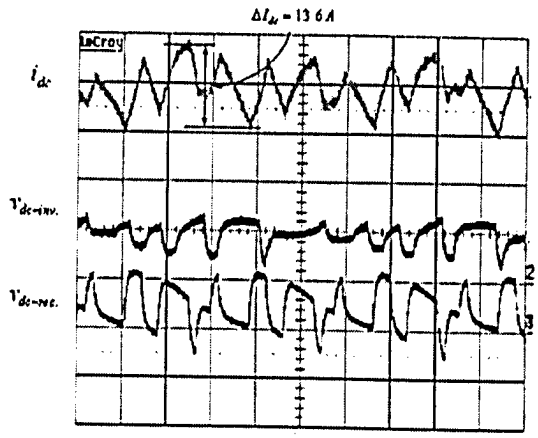
(a) Input/Output current and voltage (b) DC link current and voltages

i_s:40A/div,i_{in}:50A/div,v_{in}:600V/div,v_s:600V/div,Timebase:5ms/div

Figure B.4: Drive test simulation results ($f_s = 45Hz$)



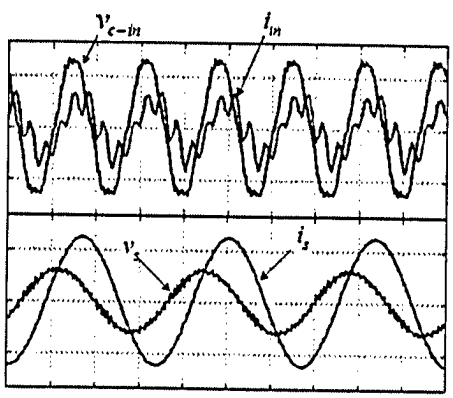
(a) Input/Output current and voltage
(Timebase:10ms/div)



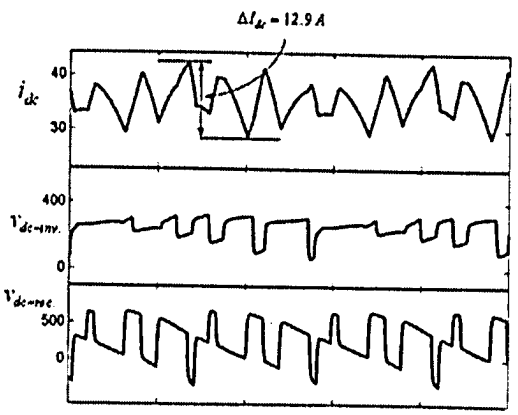
(b) DC link current and voltages
(Timebase:5ms/div)

i_s:40A/div,i_{in}:50A/div,Voltage traces:600V/div

Figure B.5: Drive test experimental results ($f_s = 30Hz$)



(a) Input/Output current and voltage
(Timebase:10ms/div)



(b) DC link current and voltages
(Timebase:5ms/div)

i_s:40A/div,i_{in}:50A/div,v_{in}:600V/div,v_s:600V/div

Figure B.6: Drive test simulation results ($f_s = 30Hz$)