HIGH-POWER MODULAR MULTILEVEL CONVERTERS: MODELING, MODULATION, AND CONTROL

By

Apparao Dekka

B. Tech., Jawaharlal Nehru Technological University, Hyderabad, India, 2007
M. Tech., Indian Institute of Technology, Bombay, India, 2010

A dissertation
presented to Ryerson University
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy
in the program of
Electrical and Computer Engineering

Toronto, Ontario, Canada, 2017

The best work is not what is most difficult for you;
it is what you do best.

— Jean-Paul Sartre

AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this dissertation. This is a true copy of the dissertation, including any required final revisions, as accepted by my examiners.

I authorize Ryerson University to lend this dissertation to other institutions or individuals for the purpose of scholarly research.

I further authorize Ryerson University to reproduce this dissertation by photocopying or by other means, in total or in part, at the request of other institutions or individuals for the purpose of scholarly research.

I understand that my dissertation may be electronically available to the public.

High-Power Modular Multilevel Converters: Modeling, Modulation, and Control

Apparao Dekka
Doctor of Philosophy
Electrical and Computer Engineering
Ryerson University, Toronto, 2017

ABSTRACT

THIS dissertation addresses the technical challenges associated with the operation and control of high-power modular multilevel converters. To improve the performance of modular multilevel converter (MMC), a generalized three-phase mathematical model with common-mode voltage (CMV) is proposed. By using the proposed mathematical model, the magnitude of circulating currents, capacitors voltage ripple, and the ripple in DC-link current during balanced and unbalanced operating conditions can be minimized.

The modulation scheme and switching frequency are directly affected the output power quality and the performance of the converter and control method. In this dissertation, a novel sampled average and space vector modulation scheme is proposed. These modulation schemes are suitable to control the MMC with any number of submodules (without modifications), operates at low switching frequency, minimizes the ripple in output current

and voltage harmonic distortion, and reduces the output filter size.

For reliable operation of MMC, the voltage balancing among submodules is mandatory. This dissertation proposes a generalized single-stage balancing approach with reduced current sensors to control the MMC. The proposed balancing approach is suitable to implement with both phase-shifted and level-shifted pulse width modulation schemes. With the proposed approach, it is also possible to control the MMC with half-bridge and three-level flying capacitor submodules. Also, an improved balancing approach often referred as the dual-stage balancing approach is proposed to minimize the voltage harmonic distortion and device power losses.

This dissertation also proposes a direct model predictive control (D-MPC) approach to minimize the ripple in submodule capacitors voltage. To implement D-MPC approach, a discrete-time model of MMC with CMV is proposed. With the use of proposed model, the D-MPC approach does not require a cost function to minimize the circulating currents.

The computational complexity is one of the major issues in the implementation of D-MPC approach for MMC. In this dissertation, a novel reduced computational MPC approaches named as dual-stage D-MPC and indirect model predictive control (I-MPC) approach are proposed. These approaches significantly minimize the computational complexity and, improve the voltage and current waveform quality while operating at the low switching frequency.

Finally, the simulation and experimental studies are presented to validate the dynamic and steady-state performance of proposed methodologies.

Index Terms

- Modular Multilevel Converters.
- Capacitors Voltage Balancing.
- Pulse Width Modulation Schemes.
- Circulating Currents.
- Capacitors Voltage Ripple.

- Direct Model Predictive Control.
- Dual-Stage Direct Model Predictive Control.
- Indirect Model Predictive Control.
- Total Harmonic Distortion.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude and heart-felt thanks to my supervisor Professor Bin Wu for his exceptional guidance and constant encouragement throughout this course of work. Without his continuous motivation and valuable suggestions, this work may not have been completed. It has been a true privilege to have worked with him, and I am very glad that I have pursued my doctoral studies under his excellent supervision.

I am grateful to Dr. Navid Zargari, Dr. David Xu and Dr. Amir Yazdani for their kind suggestions and helpful tips during the early stage of my research. I am thankful to my friend and fellow researcher Dr. Ricardo Lizana (Universidad Católica de la Santisima Concepción, Chile) and Prof. Marcelo Perez (Universidad Técnica Federico Santa Maria, Chile) for their valuable suggestions and collaborative research work on Modular Multilevel Converters.

I would also like to extend my thanks to my all colleagues at LEDAR and CUE during the past years, for their support and friendship. I would like to especially mention Sebastian Rivera, Venkata Yaramasu, Srinivas Karanki, Sivaprasad Jaldanki, Bhanu, Mehadi Narimani, Kai Tian, Longcheng Tan and Sixing Du for memorable times and fruitful discussions.

I express my respect and intense gratitude to my parents who were the source of inspiration and support all through my life. Special thanks to my brother Venkata Muni who supported me in every possible way to see the completion of this work. My research would not have been possible without

his support and encouragement.

I am very grateful to Dr. Abdul Beig for his tremendous help during the early stage of my research. He encouraged me to pursue higher studies abroad and showed me the way around this fantastic city.

Financial support from Prof. Bin Wu, Department of ELCE, Center for Urban Energy (CUE), Connect Canada program, IESO and Ryerson University is greatly acknowledged.

Toronto, Ontario, Canada
June, 2017.

Dedicated to My Mother

— Lakshmi

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

LV	Low voltage
MV	Medium voltage
HV	High voltage
DC	Direct current
AC	Alternating current
IGBT	Insulated-gate bipolar transistor
GTO	Gate turn-off thyristor
GCT	Gate commutated thyristor
IGCT	Integrated gate-commutated thyristor
SGCT	Symmetrical gate-commutated thyristor
CHB	Cascaded H-bridge
CNPC	Cascaded neutral-point clamped
FC	Flying capacitor
NPC	Neutral point clamped
ANPC	Active neutral point clamped
NNPC	Nested neutral point clamped
MMC	Modular multilevel converter
SM	Submodule
HB	Half-bridge
FB	Full bridge or H-bridge
CH	Cascaded half-bridge
CD	Double clamp
BM	Blocking mode

HVDC	High-voltage direct current
STATCOM	Static synchronous compensator
VSC	Voltage source converter
VSI	Voltage source inverter
VSR	Voltage source rectifier
CSC	Current source converter
CSI	Current source inverter
CSR	Current source rectifier
CCV	Cycloconverter
THD	Total harmonic distortion
RMS	Root mean square
VOC	Voltage oriented control
FOC	Field oriented control
DTC	Direct torque control
PWM	Pulse width modulation
PSC-PWM	Phase-shifted carrier pulse width modulation
LSC-PWM	Level-shifted carrier pulse width modulation
SHE	Selective harmonic elimination
NLM	Nearest level modulation
2L	Two-level
3L	Three-level
5L	Five-level
PD	Phase-disposition
POD	Phase-opposition disposition
APOD	Alternate phase-opposition disposition
CMV	Common-mode voltage
PI	Proportional-integrator
PR	Proportional-resonant
PIR	Proportional-integral-resonant
VPI	Vector proportional-integrator
HPF	High-pass filter

MPC	Model predictive control
D-MPC	Direct model predictive control
I-MPC	Indirect model predictive control
SVM	Space vector modulation
SAM	Sampled average modulation
DSAZE	Decoupled sampled average zero sequence voltage elimination
CPWM	Carrier pulse width modulation
DT	Discrete-time
CT	Continuous-time

LIST OF SYMBOLS

Superscript

p	Predicted quantity
m	Measured quantity
k	Submodule index number
n	Normalized quantity
$\widehat{\ }$	Extrapolated quantity
$*$	Reference quantity
$\rightarrow$	Vector quantity

Subscript

h	Capacitor index number
$x \in \{a, b, c\}$	AC output quantities
$y \in \{u, l\}$	Arm side quantities
z	Circulating current component
e	Estimated quantity
t	total value
dev	Device quantity
d	Diode quantity
tc	Transistor conduction state
ton	Transistor on-state
$toff$	Transistor off-state
dc	Diode conduction state
dr	Diode recovery state

System Quantities

m_a	Amplitude modulation index
f_o	Fundamental frequency (Hz)
f_c	Carrier frequency (Hz)
f_{sw}	Switching frequency (Hz)
ϕ	Phase angle between phases (rad)
ϕ_c	Phase angle between carriers (deg)
ϕ_{ci}	Interleave angle between carriers (deg)
φ	Power factor angle (deg)
R	Number of capacitors in each converter leg
N	Number of submodules in each arm
D	Direction of current
D_{xy}	Normalized arm voltage waveform
S_{xyh}	Submodule switching states
G_{xyh}	Submodule gating signals
E	Submodule energy (J)
p	Submodule instantaneous power (W)
T_s	Sampling time (sec)
g	Cost function
op	Optimal quantity
j	Switching state
λ_o	Weighting factor for output current control
λ_c	Weighting factor for capacitor voltage control

Current Quantities

i_{dc}	DC-link current (A)
i_u, i_l	Upper and lower DC-link currents (A)
i_s	DC current component (A)
i_{cm}	Common-mode current (A)
i_{au}, i_{bu}, i_{cu}	Three-phase upper arm currents (A)
i_{al}, i_{bl}, i_{cl}	Three-phase lower arm currents (A)
i_a, i_b, i_c	Three-phase AC output currents (A)
i_B	Base current (A)

Voltage Quantities

V_{dc}	DC-link voltage (V)
V_u, V_l	Upper and lower half DC-link voltage (V)
v_{au}, v_{bu}, v_{cu}	Three-phase upper arm voltages (V)
v_{al}, v_{bl}, v_{cl}	Three-phase lower arm voltages (V)
v_{H}	Output voltage of half-bridge (V)
v_{F}	Output voltage of full-bridge (V)
v_{FC}	Output voltage of flying capacitor (V)
v_{CH}	Output voltage of cascaded half-bridge (V)
v_{CD}	Output voltage of double clamp (V)
v_{C}	Submodule capacitor voltage in HB-SM (V)
v_{C1}, v_{C2}	Submodule capacitors voltage in FC-SM (V)
v_{cm}, v_{no}	Common-mode voltage (V)

Passive Elements

L_{dc}	DC-line inductor (H)
r_{dc}	DC-line resistor (Ω)
L_o	Load inductor (H)
r_o	Load resistor (Ω)
L	Arm inductor (H)
r	Arm resistor (Ω)
R_c	Pre-charging resistor (Ω)
S_c	Contactor switch
C	Submodule capacitance in HB-SM (F)
C_1, C_2	Submodule capacitance in FC-SM (F)

CHAPTER 1

INTRODUCTION

POWER converters are well known in industry and academia as one of the preferred choices for efficient power conversion systems [1]. In the past decade, several power converters are developed and commercialized in the form of standard and customized products that power a wide range of industrial applications [2]. The standard power converter topologies are available for an operating voltage of 2.3-13.8 kV only [3]. These topologies require either a step-up transformer or high-voltage (HV) semiconductor devices for HV operation. The former solution is costly and, increases the size and volume of the converter system. The new solution is difficult to implement due to the lack of HV semiconductor devices [4]. The available semiconductor devices and their voltage and current ratings are shown in Table 1.1 [5]. The semiconductor devices are available in medium-voltage (MV) range and cannot block the high operating voltages.

Alternatively, MV devices are connected in series to increase the operating voltage of power converters. The series-connected devices and their gate drivers may not exhibit similar static and dynamic performance. These devices may not equally share the total voltage during blocking mode and switching transients. This approach requires equalization circuit to achieve equal voltage sharing during blocking mode [6]. The additional voltage shar-

Table 1.1. Market overview of power semiconductor devices

Rating	Power Diode	Thyristor	GTO	GCT/IGCT/ SGCT	LV–IGBT/ HV–IGBT
Max. Voltage	8.5 kV at 1.2 kA	12 kV at 1.5 kA	6 kV at 6 kA	10 kV at 1.7 kA	6.5 kV at 0.75 kA
Max. Current	9.6 kA at 1.8 kV	5 kA at 0.4 kV	6 kA at 6 kV	5 kA at 4.5 kV	2.4 kA at 1.7 kV

ing circuit increases the power losses in power converters. The series connection of devices does not improve the output voltage and current waveform quality [7].

A modular approach has been developed to overcome the limitation of semiconductor devices and their series connection to reach high-voltage operation [8]. In a modular approach, identical low-voltage submodules are connected in series to reach high voltages [9]. With this approach, it is easy to scale the voltage and power rating of the power converter, reduces the complexity of assembly and maintenance of power converters, and can be operate with reduced capacity during submodule failure. Therefore, the modular power converters become popular for high-voltage, high-power applications. The modular power converters are also referred as cascaded power converters or multi-cell power converters [10].

The cascaded H-bridge (CHB), cascaded neutral-point clamped (CNPC) converters, and modular multilevel converter (MMC) belongs to the multi-cell converter family [11]. The CHB and CNPC topologies require phase-shifting transformer with multiple secondary windings to generate isolated DC sources, which increases the overall size and cost of the converter. These topologies are not cost effective for regenerative applications [12]. Recently, the MMC has been developed to address the problems associated with the existing CHB and CNPC topologies. The main features of MMC are modular construction, high reliability, cost effective due to the use of low-voltage, insulated gate bipolar transistor (LV-IGBT) technology to reach high-voltage

(HV) operation, does not require isolated DC sources and direct connection to the high-voltage networks without line frequency transformer [13]. The MMC is commercialized in medium-voltage motor drives, high-voltage direct current (HVDC) transmission systems, multi-terminal HVDC systems and static synchronous compensators (STATCOM) [14, 15].

Each leg of MMC has formed with a cascade connection of low-power submodules. The standard submodules such as half-bridge (HB) and full-bridge (FB) topologies are employed in commercially available MMC systems [16]. These submodules have a simple construction and easy to control. Alternatively, the multilevel submodules such as flying-capacitor (FC), neutral-point clamped (NPC) and twin modules are investigated in place of standard submodules [17]. These submodules reduce the foot-print size and improve the efficiency of MMC. However, it requires a control scheme with complex structure and functions to manage several control objectives simultaneously [17].

In this dissertation, novel linear and model predictive control methods have been proposed aimed at standard and multilevel submodule based modular multilevel converter system. The proposed approaches are more generic in nature, operate at the low switching frequency and produce high-quality voltage and current waveforms with lowest harmonic distortion. Also, the steady-state and dynamic performance of MMC is significantly improved. Furthermore, these approaches minimize the computational burden of the real-time implementation.

This chapter is organized as follows: an overview of high-power converters is presented in Section 1.1. Among them, the voltage source converters (VSCs) have the highest market share and widely used in industry applications. The recent development of VSCs is discussed in Section 1.2. The fundamental details and technical challenges associated with the operation and control of MMC are presented in section 1.3. The background overview of control methods for MMC is presented in Section 1.4 and 1.5, respectively. The dissertation objectives are given in Section 1.6. In Section 1.7, the outline

of the dissertation is summarized.

1.1 Overview of High-Power Converters

High-power converters are categorized into two groups as shown in Figure 1.1. The first group consists of power converters with an intermediate DC-link (DC energy storage element). This group of converters performs the power conversion in two stages of AC-DC and DC-AC between the AC-grid and machine. This group is further categorized into voltage source converters (VSCs) and current source converters (CSCs), depending on the nature of the DC energy storage element [18]. VSCs normally employ DC capacitors as DC energy storage element, whereas CSCs employ DC inductors in the DC-link. VSCs are referred as voltage source rectifiers (VSR) in the AC-DC conversion stage, and voltage source inverters (VSI) in the DC-AC conversion stage [18]. Similarly, CSCs are referred as CSR and CSI, depending on the functionality [19, 20].

The second group consists of power converters without an intermediate DC-link (DC energy storage element). This group of converters performs direct AC-AC conversion between the AC-grid and machine. Cycloconverters (CCVs) and matrix converters belong to this group. CCV is a widely used

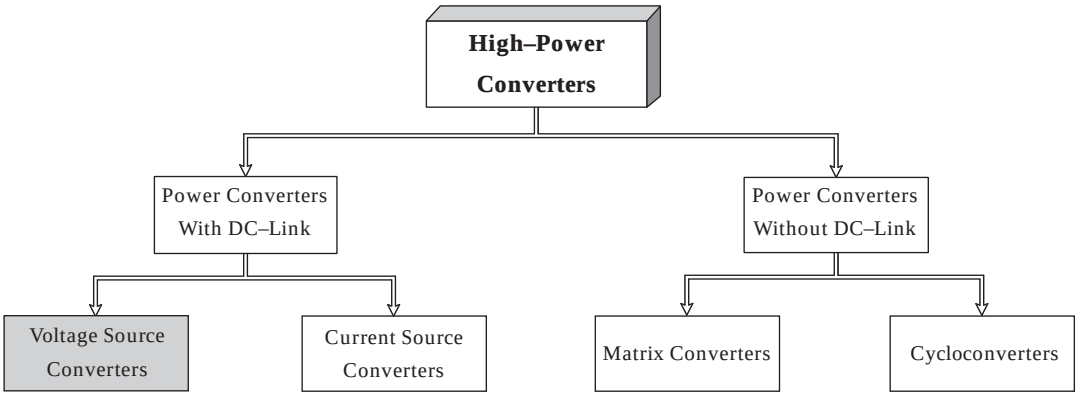


Figure 1.1. Classification of high-power converters.

topology in high-power applications, which use an array of thyristors for the direct connection of the AC-grid to a machine [21]. CCV allows efficient power flow in both directions. However, CCVs have poor dynamic performance, limited operating voltage and frequency range, and low-power factor at low-speed of operation [21]. Matrix converter is a new topology capable of direct AC-AC conversion without DC energy storage. The main features of matrix converters include sinusoidal input or output waveforms, controllable input power factor, wide range of output voltages and frequency control, and light-weight design unlike CCVs [22, 23].

1.2 Voltage Source Converters

Over the past decade, VSCs exhibited higher market penetration and more evident developments compared with CSCs and matrix converters. The most prominent developments in VSCs are shown in Figure 1.2. Two-level converters are limited to low-voltage (LV), low-power applications. For high-power applications, two-level converters require either device in parallel to carry high-current at LV operation or devices in series to reach MV operation with low current carrying capacity [24]. The parallel and series connection of devices do not introduce any additional benefits regarding power quality (reduction of voltage and current harmonic distortions) and $\frac{dv}{dt}$ reduction. Power losses and voltage blocking is uneven in series connected devices. Thus, the two-level converters are not very popular for high-power applications [25].

New converter topologies with low-cost semiconductor technology are developed for high-power applications. These converters are referred as multilevel converters. The multilevel converters have significant advantages compared with two-level converters, which includes low $\frac{dv}{dt}$ and harmonic distortion, near sinusoidal currents, the smaller size of input and output filters (if necessary), high-efficiency, low common-mode voltage, and possible fault tolerant operation in certain cases [25–27]. Multilevel converters are

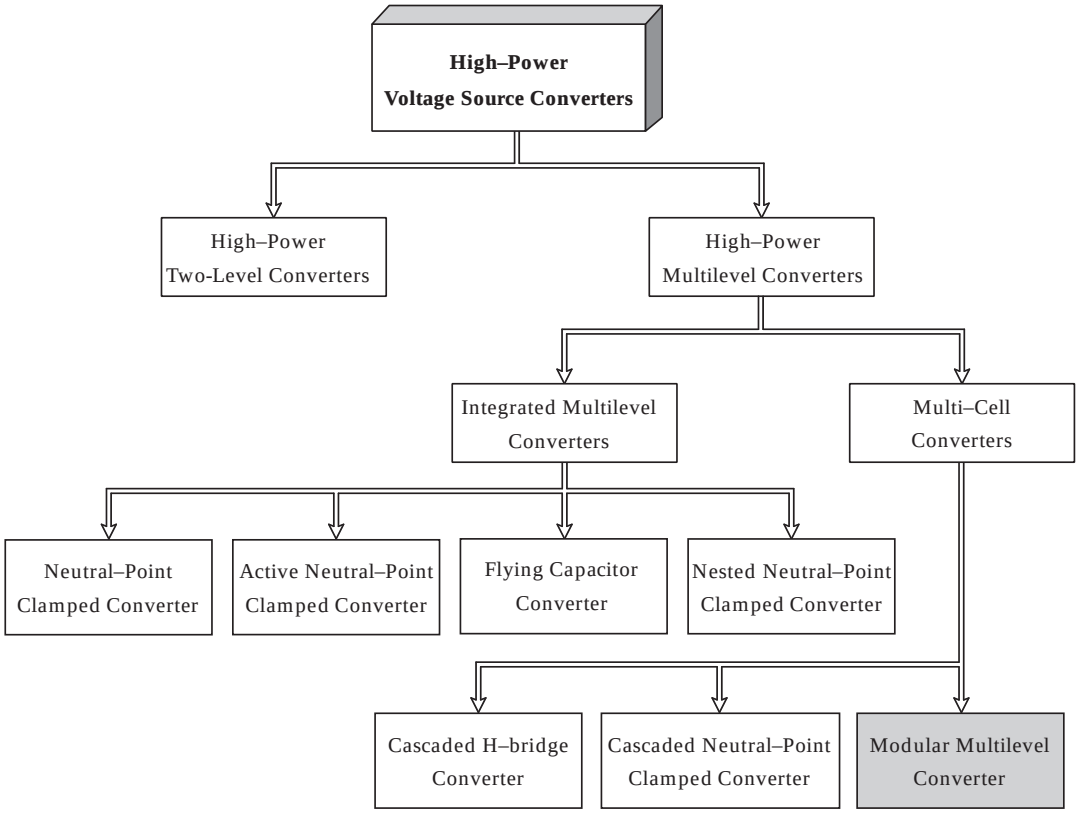


Figure 1.2. Classification of voltage source converters.

composed with an array of LV or MV devices and DC capacitors. These converters generate a stepped voltage waveform with proper arrangement of devices, capacitive voltage sources, and control methods [25–27].

Several multilevel converter topologies are established in the past years, and very few succeeded in the industry as shown in Figure 1.2. Neutral-point clamped (NPC), active neutral-point clamped (ANPC), flying capacitor (FC) and nested neutral-point clamped (NNPC) converters can handle a voltage of 2.3-4.16 kV [25–27]. These converters require significant modifications to increase the operating voltage and the number of voltage levels, which is not cost-effective. These converters are shut down during faults and other failures, leading to a significant loss of production in various industrial processes.

Aforementioned problems can overcome with the cascaded converter topologies, also referred as multi-cell converters. The CHB and CNPC converters are constructed with a cascade connection of low-power submodules with an isolated DC source in each phase. These topologies have modular construction and, can reach an operating voltage higher than 6 kV upto 13.8 kV. The cascaded converters can operate with reduced capacity during faults as well [25–27]. The number of submodules in each phase is increased to reach a high voltage. However, CHB and CNPC requires a phase-shifting transformer with multiple secondary windings to generate isolated DC sources, which increases the cost of the converter and limits the number of submodules in each phase [25–27]. Recently, MMC has been developed to address the problems associated with the existing cascaded converter topologies.

1.3 Fundamentals of Modular Multilevel Converter

The voltage and power capacity of MMC is naturally increased by adding the submodules in each arm. The submodule (SM) is a building block of MMC, configured in various forms with IGBTs and DC capacitors. Unlike CHB and CNPC, any power converter circuit such as full-bridge or H-bridge, flying capacitor, and neutral-point clamped converters can be utilized as a submodule in MMC [28, 29]. The type and number of submodules in each arm vary with the application, operating voltage and the rating of IGBT devices [30]. For example, medium-voltage motor drives with 3.3-13.8kV operating voltage require 5-20 SM / arm [31], high-voltage direct current (HVDC) transmission system needs 200-400 SM / arm to reach $\pm$ 320 kV (DC) voltage [32] and static synchronous compensators employ 15-200 SM / arm to reach 13.8-220 kV operating voltage [33]. The three-phase MMC can be extended to multi-phase applications because of its modular construction.

Figure 1.3 shows the generalized circuit configuration of three-phase modular multilevel converter. The DC system is often referred as a DC-bus or

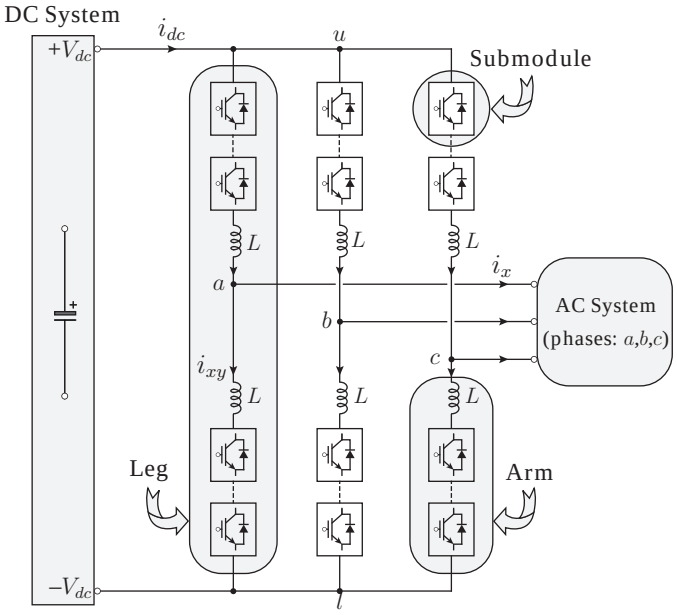


Figure 1.3. Configuration of modular multilevel converter

DC-link, connected to the positive and negative bars of the converter legs. The three-phase AC system is connected to the mid-point of each leg (a, b, c). Each leg of MMC is divided into two arms. The arms connected to the positive bar is referred as upper arms (u) and the arms connected to the negative bar are referred as lower arms (l). Each arm consists of a group of submodules and an inductor (L). The arm inductor is connected in series with each group of submodules to limit the current due to the instantaneous voltage difference of the arms [34].

The main features of MMC are as follows:

- It has modular construction with an ability to scale the voltage and power rating,
- It can generate an output voltage and current waveforms with reduced $\frac{dv}{dt}$ and ripple. Typically, a very low total harmonic distortion (THD) can be obtained,
- Since MMC can produce an output voltage waveform with very large

number of voltage levels, it is possible to operate at very low switching frequency while achieving high efficiency,

- It can employ redundancy submodules in each arm to operate during faults.

1.3.1 Configuration of Submodules

The submodule (SM) is a simple DC-AC power conversion circuit. Usually, low-voltage IGBT devices (1200-1700 V) and DC capacitors are used to configure a submodule. Most widely used submodule configurations in MMC are as follows [35–37]:

- Half-bridge (HB) submodule
- Full-bridge (FB) submodule
- Cascaded half-bridge (CH) submodule
- Double clamp (CD) submodule

Among them, the half-bridge (HB) submodule is most popular and widely used in the commercial products. The HB-SM is often referred as a chopper cell, and its circuit configuration is shown in Figure 1.4. It's simple construction (two semiconductor devices and one floating capacitor) results in simple control and design. During normal operation, only one device (either S_1 or $\overline{S}_1$) will be in "ON" state. Therefore, the HB-SM has low power losses and high efficiency [35–37]. The output voltage of half-bridge submodule has positive levels only, and can not support the bipolar operation and DC fault current blocking in MMC.

The full bridge (FB) submodule is referred as H-bridge, which consists of four semiconductor devices and one DC capacitor as shown in Figure 1.5. The number of semiconductor devices becomes double as that of the HB-SM for the same voltage rating. However, the control and design complexity

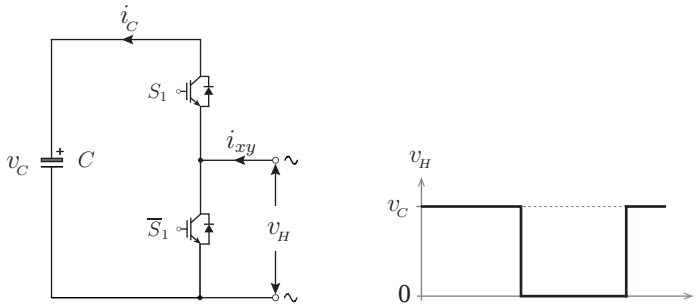


Figure 1.4. Half-bridge submodule and output voltage

are same as that of HB-SM. During normal operation, two devices in a conduction state results in higher power losses and low efficiency [35–37]. The negative voltage levels in FB-SM are used to limit the current during DC-side faults.

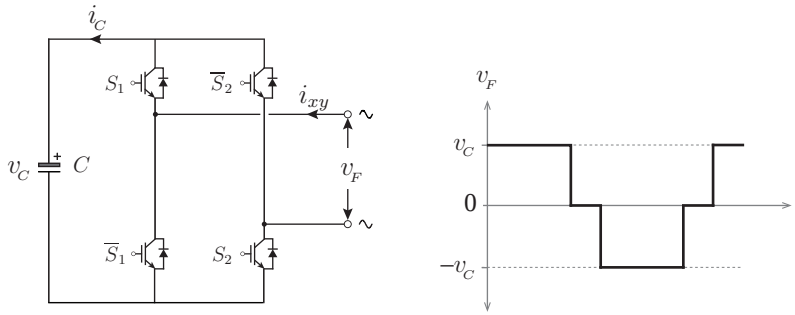


Figure 1.5. Full-bridge submodule and output voltage

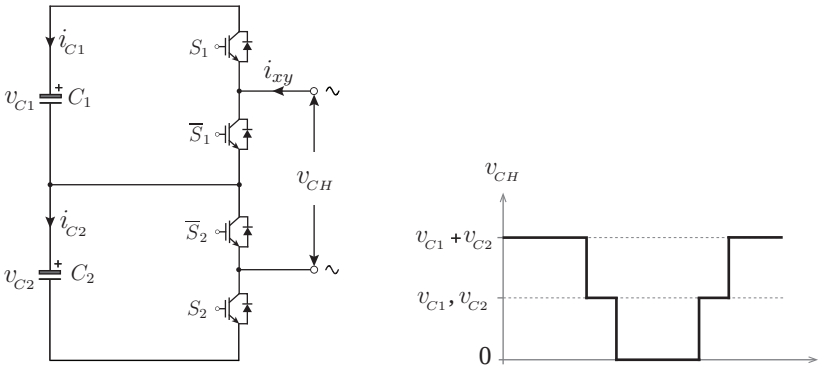


Figure 1.6. Cascaded half-bridge submodule and output voltage

The cascaded half-bridge (CH) submodule is formed using two HB-SMs connected in series, resulting in three-level operation as shown in Figure 1.6. It requires simple control and low design complexity, low power losses and high efficiency similar to HB-SM [35–37]. The CH-SM cannot block the DC-side faults and does not support bipolar operation.

Table 1.2. Comparison of submodules

Performance Index	HB-SM	FB-SM	CH-SM	CD-SM
No. of output voltage levels	2	3	3	4
Max. blocking voltage of SM	v_C	v_C	$2v_C$	$2v_C$
Max. No. of DC capacitors normalized to v_C	1	1	2	2
No. of devices normalized to v_C	2	4	4	7
Max. No. of devices in conduction path	1	2	2	3
Power losses	Low	Moderate	Moderate	High
Bipolar operation	No	Yes	No	Yes
SM design complexity	Low	Low	Low	High
SM control complexity	Low	Low	Low	Low
DC fault blocking	No	Yes	No	Yes

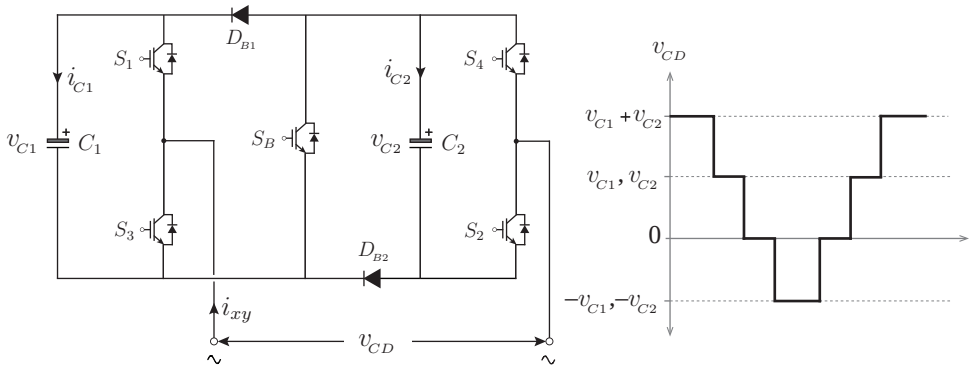


Figure 1.7. Double clamp submodule and output voltage

The double clamp (CD) submodule is also formed using two HB-SMs along with three additional devices as shown in Figure 1.7. This topology limits the DC-side fault currents by generating the negative voltage levels

during blocking mode (BM) of operation. However, the power losses, efficiency and design complexity are significantly high due to the additional devices [35–37]. A summary of submodule comparison in terms of rating, operation, control and design complexity, losses, and DC fault blocking capability is presented in Table 1.2 [35–37].

1.3.2 Principle of Operation

In this section, the operation of MMC with HB-SM is presented. The structure of three-phase MMC is shown in Figure 1.8(a), where the DC system is modeled as a split DC source of voltage $\frac{V_{dc}}{2}$, in series with an inductor L_{dc} and a resistor r_{dc}. The three-phase AC system is connected to a passive load of an inductor L_o and a resistor r_o. As the name suggested, the MMC is configured using multiple HB-SMs with an identical construction in each arm to generate the multilevel stepped waveform at the output.

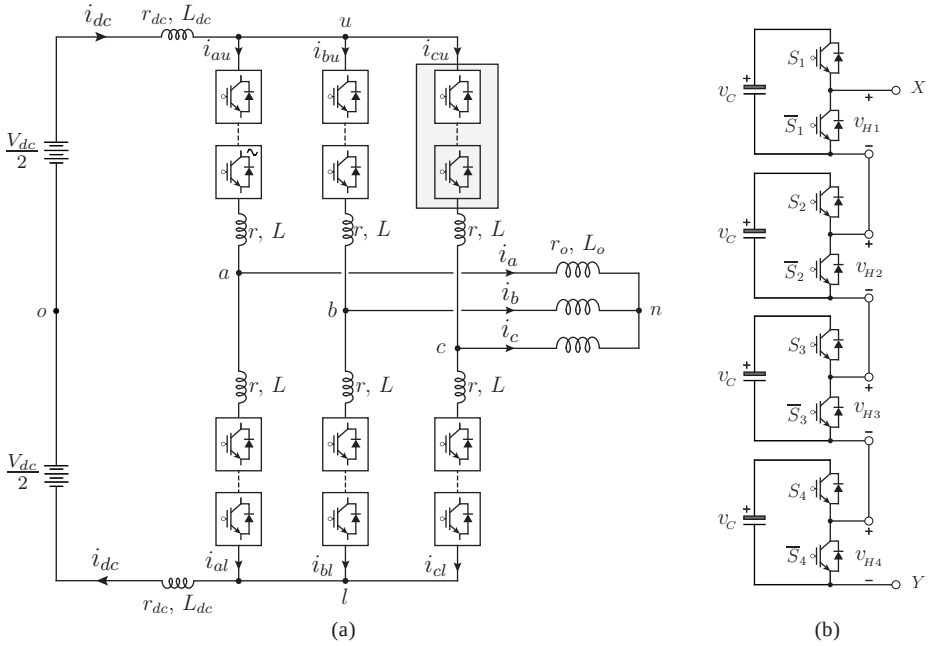


Figure 1.8. Converter and arm configuration: (a) MMC with passive load, (b) Connection diagram of HB-SMs in an arm

For easy of understanding, In each arm, four half-bridge submodules are considered, and their connection diagram is shown in Figure 1.8(b). Each submodule capacitor voltage is rated for v_C, and its output voltages are named as v_{H1}, v_{H2}, v_{H3} and v_{H4}. The submodule output terminals are connected in series and give an arm voltage.

Table 1.3. Switching states and voltage levels

S_1	S_2	S_3	S_4	v_{H1}	v_{H2}	v_{H3}	v_{H4}	v_{XY}	Voltage Level
0	0	0	0	0	0	0	0	0	0
1	0	0	0	v_C	0	0	0	v_C	
0	1	0	0	0	v_C	0	0	v_C	1
0	0	1	0	0	0	v_C	0	v_C	
0	0	0	1	0	0	0	v_C	v_C	
1	1	0	0	v_C	v_C	0	0	$2v_C$	
1	0	1	0	v_C	0	v_C	0	$2v_C$	
1	0	0	1	v_C	0	0	v_C	$2v_C$	2
0	1	1	0	0	v_C	v_C	0	$2v_C$	
0	1	0	1	0	v_C	0	v_C	$2v_C$	
0	0	1	1	0	0	v_C	v_C	$2v_C$	
1	1	1	0	v_C	v_C	v_C	0	$3v_C$	
1	1	0	1	v_C	v_C	0	v_C	$3v_C$	3
1	0	1	1	v_C	0	v_C	v_C	$3v_C$	
0	1	1	1	0	v_C	v_C	v_C	$3v_C$	
1	1	1	1	v_C	v_C	v_C	v_C	$4v_C$	4

The switching states, the output voltage of submodules, and arm voltage are shown in Table 1.3. With four submodules, the arm voltage has five voltage levels "0, v_C, $2v_C$, $3v_C$, and $4v_C$". The highest voltage level "$4v_C$" is generated by turning "ON" S_1, S_2, S_3, and S_4. Similarly, the lowest voltage level "0" is generated by turning "OFF" all the submodules. Table 1.3 shows that the intermediate voltage levels are generated using multiple switching combinations (redundancy switching states). The redundancy switching states

are often used to control the submodule capacitors voltage in MMC. The arm voltage equation, which represents the operation of an arm is given by

$$v_{XY} = v_{H1} + v_{H2} + v_{H3} + v_{H4} = S_1\, v_C + S_2\, v_C + S_3\, v_C + S_4\, v_C \tag{1.3.1}$$

The arm voltage is equal to the summation of submodules output voltage. Each submodule output voltage is equal to the product of submodule capacitor voltage and corresponding submodule switching state. The above philosophy can be easily extended to any number of submodules per arm. The multilevel voltage waveform across the load is generated by controlling the submodules in upper and lower arms of MMC.

1.3.3 Technical Challenges

The operation and control of MMC involve several technical challenges, which are summarized as follows:

1) **Mathematical Model:** The design and performance of control scheme are greatly depends on the mathematical model of the system. Due to the modular construction, the per-phase modeling is used to control the MMC. These models are approximate in nature and affect the performance of MMC [38]. Hence, the accurate mathematical models are necessary to improve the performance of MMC.

2) **Pulse Width Modulation (PWM) Schemes:** The PWM schemes require significant modifications, depending on the number of submodules, converter configuration, and type of submodule. Also, the output voltage and current waveform quality vary with the number of submodules and switching frequency. Hence, a generalized low switching frequency PWM scheme which can generate high-quality output voltage and current waveforms is required to control the MMC.

3) **Submodule Capacitor Pre-Charging Process:** Each submodule is designed with IGBT devices and floating capacitors. These floating capac-

itors have zero initial voltage and must be charged to its nominal voltage level before starting the normal operation. However, the charging process of submodule capacitors during startup leads to a large inrush current due to the small equivalent impedance of the converter [39]. The pre-charging of submodule capacitors without inrush current is one of the major challenges in MMC.

4) **Submodule Capacitor Voltage Control:** The control of submodule capacitors voltage at the given reference voltage value is mandatory to generate a multilevel stepped waveform at the output of MMC. The MMC has several submodules in each arm. A complex control structure is required to control these submodules [40]. Also, a significant number of current and voltage sensors is required to implement the submodule capacitor voltage control. Hence, a control scheme with reduced computational complexity and sensors is required to reduce the system cost.

5) **Submodule Capacitor Voltage Ripple:** The interaction between arm current and arm voltage causes voltage ripple in submodule capacitors [41,42]. These voltage ripples increase the device voltage stress and effect the reliability of the converter. Each submodule requires large capacitance value to suppress the voltage ripple, thus increases the converter cost [41, 42]. Hence, the suppression of voltage ripple without using large capacitors is one of the challenging tasks.

6) **Circulating Current:** Circulating currents originate from the voltage difference between the arms in each converter leg [41,42]. The circulating currents does not affect the AC output voltages and currents. However, it increases the peak and RMS value of the arm current which consequently increases the converter power losses and the ripple in submodule capacitors voltage [41, 42]. Therefore, the suppression of circulating currents is mandatory for a reliable and efficient operation of MMC.

Several control methods have been developed to address the above challenges. The overview and limitations of existing methodologies are discussed in the following sections.

1.4 Overview of Classical Control Methods for MMC

The digital control schemes enable safe, reliable, and efficient operation of MMC. These control schemes provide superior dynamic and steady state performance. The control of MMC is quite challenging and involves multiple control objectives as shown in Figure 1.9. The MMC control objectives are divided into two categories of primary and secondary. The output currents and submodule (SM) capacitors voltage control are primary objectives, associated with the operation of MMC. The control of circulating currents and submodule capacitor voltage ripple belongs to the secondary objectives. These objectives affect the size, reliability, and efficiency of MMC. These objectives are achieved using classical control methods. The classical control methods require an independent controller for submodule capacitor voltage, output current and circulating currents. Also, the pulse width modulator is required to generate the gate signals for each submodule. The background overview and limitations of classical control methods are discussed in the following sections.

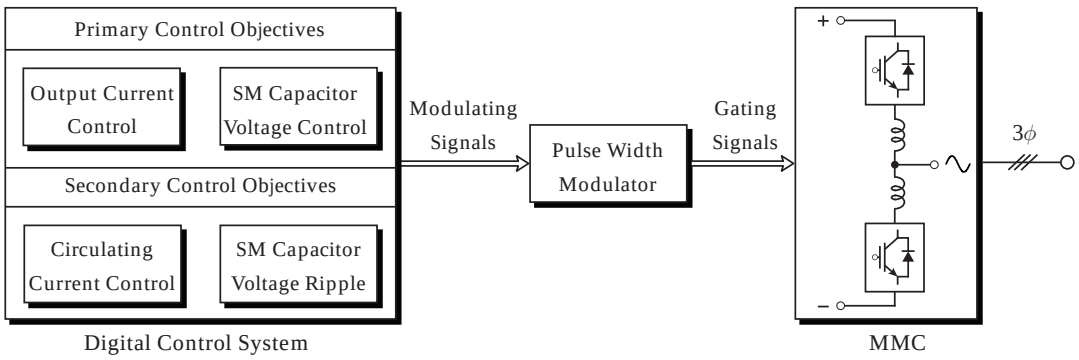


Figure 1.9. Block diagram of classical control system

1.4.1 Pulse Width Modulation Schemes

The pulse width modulation (PWM) is widely used to control the AC output voltage of a power converter. The duty cycle of switching devices varies to generate the targeted (reference) AC output voltage. The PWM schemes are designed to reduce the output voltage harmonic distortion and increase the magnitude of the output voltage at a given switching frequency [43–45]. Based on the switching frequency, the PWM schemes for modular multilevel converter are categorized into high-switching frequency and fundamental switching frequency modulation schemes as shown in Figure 1.10 [43–45].

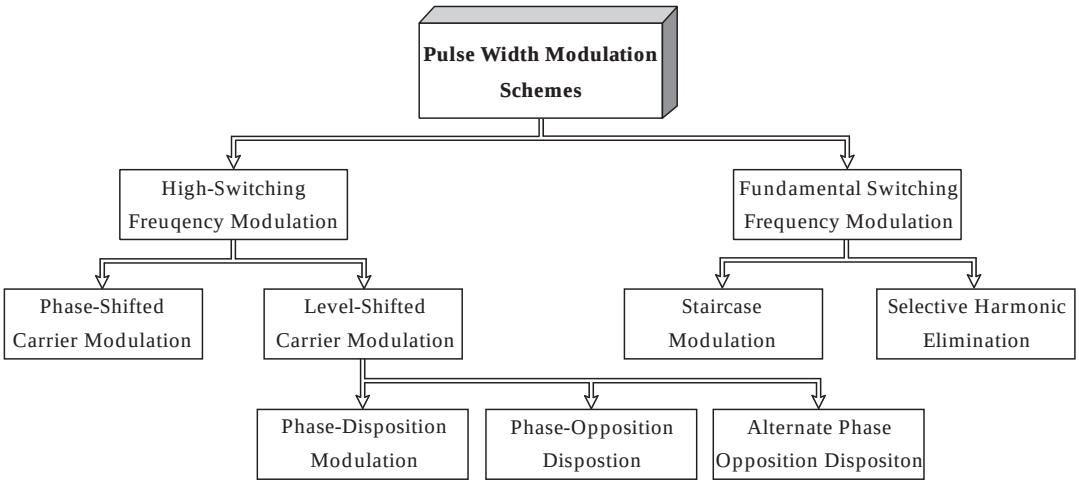


Figure 1.10. Pulse width modulation schemes for MMC.

The carrier modulation scheme is often referred as sine-triangular modulation, which is well established for two-level power converters. In carrier modulation, the modulating signals are compared with a single triangular carrier signal to generate the gating signals for the switching devices of the two-level converter. The carrier modulation schemes are extended to multilevel converters, where multiple triangular carrier signals are compared with phase modulating signals to generate the gating signals. This approach is referred as multi-carrier modulation scheme [43–45]. Depending on the type of carrier arrangement, the multi-carrier modulation schemes are categorized into phase-shifted (PSC-PWM) and level-shifted (LSC-PWM) carrier modu-

lations [43–45].

The natural balancing of submodule capacitors voltage in MMC can be achieved with high-carrier frequency based PSC-PWM scheme [46]. The high-switching frequency operation causes higher switching losses, which is not desirable for high-power applications [46]. Therefore, an additional voltage balancing algorithm is used with lower carrier frequency based PSC-PWM scheme, provided that the number of submodules is high [47]. The PSC-PWM is investigated with and without interleaving angle, and the results show that carrier interleaving improves the total harmonic distortion of the output voltage at the expense of higher ripple and RMS (root mean square) value of arm current [48, 49].

The LSC-PWM is further categorized into phase-disposition (PD-PWM), phase-opposition disposition (POD-PWM), and alternate phase-opposition disposition (APOD-PWM) schemes [50]. Among them, the PD-PWM generates output voltage with lowest harmonic distortion compared to POD-PWM and APOD-PWM schemes [50]. The control of MMC with PD-PWM is presented in [51] and its performance is compared with the PSC-PWM scheme. The results show that the LSC-PWM scheme produces a large ripple in submodule capacitors voltage and large magnitude of circulating currents compared with the PSC-PWM scheme [52–54]. Also, the change in the number of submodules affects the arrangement of carrier signals. Hence, the carrier PWM modulator needs to be redesigned by the converter configuration and affects the flexibility in extending the existing MMC system to the higher operating voltage levels.

The staircase or nearest level modulation (NLM) method is easy to implement and studied for MMC based HVDC systems [55]. In this approach, each submodule is switched at the fundamental frequency, which significantly reduces the switching losses. Also, the MMC generates an output voltage with very low harmonic distortion (THD $<$1%) due to the large number of submodules (200-400 SMs) in each arm, which is the case for MMC based HVDC systems [55]. However, this approach requires higher sampling frequency

to reduce the harmonic distortion by triggering the submodules as quickly as possible [56]. A modified NLM method generates output voltage levels equivalent to the carrier PWM with the interleaving angle and is presented in [57].

The selective harmonic elimination (SHE) scheme is also operated at fundamental switching frequency [58, 59]. The implementation of SHE scheme involves the calculation switching angles [58, 59]. The number of switching angles drastically increase with the number of voltage levels. Also, it is difficult to obtain the solution for such a large number of switching angles. Therefore, the SHE scheme is not an ideal solution for MMC. Other hand, the staircase modulation approach is easy to implement and does not involve any complicated calculations like SHE scheme.

In [60], several fundamental switching frequency modulation schemes are presented for MMC. In these schemes, optimized pulse-pattern or switching angles are calculated in real-time and, applied to the submodules based on their capacitors voltage and the direction of arm current. The fundamental switching frequency modulation schemes are suitable for MMC with a large number of submodules in each arm [60]. There are no other modulation schemes in literature, which can operate at the low switching frequency and suitable for MMC with a smaller number of submodules. The development of low switching frequency modulation schemes for MMC is another interesting research topic.

1.4.2 Output Current Control

The MMC is used in high-voltage direct current (HVDC) transmission, medium-voltage motor drives, and static synchronous compensator (STATCOM) applications [61–64]. Each application requires a different technique to control their output currents. For example, voltage oriented control (VOC) is used in HVDC application [61] and field oriented control (FOC) or direct torque control (DTC) is applied to motor drive systems [62]. In the case of STATCOM, the output currents are controlled to meet the reactive power or

power factor requirement [63, 64]. These control techniques are well established and implemented in stationary-abc, stationary-$\alpha\beta$ and synchronous-dq reference frames [65].

1.4.3 Submodule Capacitors Voltage Control

The MMC has several low-voltage submodules in cascade to reach the required operating voltage. The number of floating capacitors per submodule varies with its configuration. For example; three-level submodules have two floating capacitors, while the four-level submodules have three floating capacitors. During normal operation of MMC, these floating capacitors voltage need to be regulated at their nominal value. At the same time, the total average leg voltage of MMC should be equal to the DC-link voltage. These objectives are achieved by using a leg voltage control and submodule voltage balancing approach.

The simplest way to balance the voltage of the capacitor is, by the periodical rotation of gating signal pattern based on the phase-voltage switching state redundancy [66, 67]. However, this method is difficult to apply for MMC with a large number of submodules per arm. In [68–70], a balancing controller is presented for capacitor voltage balancing between the submodules. In this approach, each submodule has a dedicated balancing controller and its output is added to the corresponding submodule reference modulating signal [68–70]. However, the designing of multiple balancing controllers is difficult and increases the complexity of control scheme. This method can achieve good balancing and current controllability when the switching frequency is sufficiently high. Other hand, the capacitors voltage balancing is achieved by adjusting the duration of PWM gating pulses in real-time [71,72]. These approaches are studied for half-bridge based MMC with phase-shifted carrier pulse width modulation (PSC-PWM) scheme only.

Alternatively, the sorting based voltage balancing approaches are developed to control the MMC with level-shifted carrier pulse width modulation (LSC-PWM), selective harmonic elimination (SHE) schemes and nearest level

modulation (NLM) methods [73–76]. In this approach, the submodules in the arm are sorted in either ascending or descending order for each PWM period based on the instantaneous value of capacitor voltage and the direction of arm current. When the arm current is positive, the submodules with the lowest voltage is chosen to be inserted to let them charge and avoid any overcharging of those capacitors with highest voltages, and vice–versa [73–76]. This approach mainly involves logical functions and implemented after the modulation stage [73–76]. These approaches are further extended to control the multilevel submodule (3L-FC, 3L-NPC) based MMC system, and verified its performance with PSC-PWM and LSC-PWM schemes [77].

The sorting based voltage balancing algorithms are custom designed according to the type of modulation scheme and submodule. There is no unique solution in the literature, which can be used to control the MMC irrespective of the type of modulation scheme.

The direction of arm current is widely used in the implementation of voltage balancing methods. The three-phase MMC has total six arms and requires six current sensors to measure the arm currents. The system cost can be reduced by eliminating or reducing the number of arm current sensors. In [78], the charging and discharging of submodule capacitors is analyzed based on the pulse width duration of gating signals. The optimum gating signal is applied to the submodule, which requires extreme charge transfer. This approach eliminates the arm current sensors and improves the reliability of the system by reducing the number of components that can potentially fail [78]. This approach is only applicable for fundamental switching frequency modulation schemes and difficult to apply for MMC with a large number of submodules per arm. The design of generalized voltage balancing algorithm without measuring arm currents and suitable to implement with any modulation scheme needs to be addressed.

It is also possible to achieve voltage balancing among submodules by controlling the submodules energy rather than their voltages. In [79], a simple open-loop energy estimation approach is presented for half-bridge based

MMC system. The energy balancing methods effectively control the submodule capacitors voltage at their nominal value even under submodule fault conditions [80]. The voltage or energy based balancing approaches show identical performance in the case of half-bridge based MMC [81, 82]. However, there is no definite answer in the case of multilevel submodule based MMC. The design and study of energy balancing approach for multilevel submodule based MMC is one of the challenging and interesting research topics.

1.4.4 Minimization of Submodule Capacitors Voltage Ripple

Submodule capacitors voltage ripple is one of the major issues in an MMC based motor drive systems under constant-torque, low-speed operation [83, 84]. Low-frequency voltage ripple, particularly second and fourth-order harmonic components can be observed in submodule capacitors voltage. The voltage ripple generates the circulating current on the arm side corresponding to the ripple frequency [85]. The circulating current increases the peak value of arm current, thereby increasing the voltage stress on devices and introducing additional conduction losses. The ripple in submodule capacitors voltage can be reduced at the system level by selecting the proper size of submodule capacitors, which increases the cost and size of the converter [86, 87].

The classical control methods are designed to minimize the low-frequency voltage ripple components by using two additional degrees freedom, i.e., common-mode voltage (CMV) on the AC-side and a circulating current between the converter legs [88–90]. In [88], a zero-sequence voltage at twice the output frequency is injected to compensate the double line frequency components in the capacitors voltage. In [89], an injection of the second harmonic circulating current component is presented to shape the capacitors voltage ripple. The second-and fourth-order harmonic circulating current components are also used to minimize the voltage ripple in MMC [90].

The voltage ripple can be minimized by using either proper PWM scheme or by adding the CMV to the modulation signals [91, 92]. In [91], discontinu-

ous-PWM scheme is presented for ripple minimization in MMC. This approach includes the CMV in the modulation stage itself. In [92], an improved PSC-PWM is presented to minimize the submodule capacitors voltage ripple. This scheme improves the total harmonic distortion of output voltage compared to the conventional PSC-PWM scheme. Alternatively, several CMV injection methods such as sinusoidal, third-order harmonic, and square-wave CMVs are studied in [93]. Among them, the square-wave CMV injection method significantly minimizes the voltage ripple without increasing the peak-value of arm current (50% smaller than that of other methods) and has low conduction losses.

A combination of high-frequency CMV and circulating current is used to reduce the voltage ripple further [94–96]. CMV and circulating current can be injected at the same frequency or different frequencies. Among these methods, the CMV at three-times the output frequency and circulating current at twice the output frequency are highly effective in minimizing the voltage ripple [96]. However, these methods require complex analysis and off-line optimization techniques to generate the reference CMV and circulating currents. In [97, 98], a simplified decoupled current model is presented for online generation of reference CMV and circulating current. The decoupled model is simple and highly effective with a ripple reduction capability of 60%. These methods increase the RMS value of arm current and, the voltage stress on motor windings and bearings.

Alternatively, the converter configuration can be modified to operate at low-frequency region without increasing the ripple in capacitors voltage. Several new topologies such as passive cross-connected, active cross-connected arm based MMCs, and modified MMC are presented [99–101]. The cross-connected arm topologies consist of a cross-connected branch between upper and lower arms. This cross connected branch absorbs the power fluctuations in upper and lower arms during low-frequency operation [100, 101].

The off-line and online methods are studied with the classical control methods, where proportional-integral (PI) regulators, resonant regulators,

and synchronous PI regulators are used to control the reference signals. The parameters in the classical controller are difficult to tune, and their bandwidths are limited, which significantly affects the performance and controllability of classical control methods.

1.4.5 Circulating Current Control

Another major issue in MMC is the circulating currents among the converter legs. These currents originate from the voltage difference between the upper and lower arms of the converter legs. This current mainly consists of negative sequence component at twice the fundamental frequency during balanced operation [102]. The circulating current does not have any impact on the AC side voltages and currents. However, the improper control of circulating currents increase the peak / RMS value of the arm current, which consequently increases the rating of devices, device power losses, and ripple in submodule capacitors voltage [103]. By proper sizing of arm inductors, the magnitude of circulating currents can be suppressed to an extent [104]. However, a closed-loop control technique is required to eliminate the circulating currents from the converter legs.

In [105, 106], the open-loop methods are presented for the circulating current control and harmonic suppression. These methods are very sensitive to the parameters variation. The synchronous reference frame based control approach is widely used for the complete elimination of circulating currents. In this approach, the circulating currents in the stationary-abc frame are transformed into the synchronous-dq frame rotating at twice the fundamental frequency [107, 108]. In the synchronous-dq frame, the double line frequency circulating current component becomes DC signals. The DC signals are easily controlled using a simple PI-regulators [107, 108].

The resonant regulators are employed to control the circulating currents in the stationary-abc frame. In this approach, the resonant regulators are designed to eliminate the specific dominant harmonic frequency component such as second and fourth-order harmonic components from the circulating

currents [109–111]. In [112], a parallel combination of repetitive and PI regulator is used to eliminate multiple harmonics in the circulating currents. The parallel combination imposes a limitation on the PI regulator performance and complicates the design of the repetitive controller. To overcome these problems, a cascade structure of repetitive controller and PI regulator is presented [113]. The repetitive controller improves the bandwidth and dynamic performance of circulating current control, and total harmonic distortion of output voltage.

During unbalanced operating conditions, the circulating current consists of positive and zero sequence components besides negative sequence components at the double the line frequency [114]. The positive and negative sequence components flow through the converter legs. On the contrary, the zero sequence circulating current flows through the DC-link and converter legs, leading to a ripple in DC-link power. These ripples appear in DC-link current, considering that the DC-link voltage is stiff [114]. The DC-link current ripple increases the ripple in submodule capacitors voltage and the magnitude of arm current, which has a cascade effect on the device voltage stress and conduction losses.

In [114], the proportional+integral+resonant (PIR) regulator is employed to control the positive, negative and zero sequence circulating currents. In [115], the proportional+resonant (PR) regulator based on the instantaneous power theory is designed to suppress the zero sequence circulating currents. Thereby, the power fluctuations on DC side are minimized. In [116], a control method to suppress the circulating currents in the stationary-$\alpha\beta 0$ frame is presented. In this approach, the high-pass filter (HPF) is used to extract the double line frequency components from the circulating currents, which effect the dynamic performance of the controllers [116]. A non-ideal PR regulator is presented to adapt the grid frequency variation and minimize the circulating currents during unbalanced conditions [117]. In [118], the circulating currents are controlled using a PR regulator, where the PR regulator is designed to control the fundamental and double frequency components.

Alternatively, the circulating currents are separated into positive, negative and zero sequence components in synchronous-$dq0$ frame and controlled using a simple PI regulators [119]. In [120], decoupled double synchronous-$dq0$ frame based current control is presented to control the sum and differential energies of each converter leg. The stationary-abc frame based control method is presented in [121], where the combination of PI regulator and VPI (vector proportional integral) regulator is used in the current control. Other hand, the DC-link current or submodule capacitors voltage ripple is directly controlled by using PR regulators. Therefore, the magnitude of zero sequence circulating currents is minimized [122]. These controllers generate zero sequence voltage command, which is added to the reference modulating signals. The performance of classical control methods is greatly limited by the parameters of current controller, switching frequency, and type of PWM scheme.

1.4.6 Pre-Charging of Submodule Capacitors

Conventionally, the MMC consists of HB-SMs in series to handle the required operating voltage. Each HB-SM has single floating capacitor with zero initial voltage. These floating capacitors are pre-charged to its nominal value during start-up process and maintained at their nominal value during normal operation. However, the capacitor charging process leads to a large inrush current due to very low equivalent impedance of the converter. These currents threatening the safe operation of MMC during the start-up process.

Several uncontrolled and controlled charging methods are presented to achieve the smooth charging of floating capacitors during start-up process [123–126]. The simplest method is to include a resistor in series with an arm inductor for a short period to limit the inrush current [123]. The external resistor, arm inductor, and submodule capacitor form an RLC damping circuit. These RLC elements are designed such that it has over damping response to avoid the oscillations in DC-link current and results in large response time [123]. In [124, 125], the charging of submodule capacitors is

achieved using a staggering switching sequence, where each submodule capacitor is inserted in the arm one after another to charge them. In this approach, the DC-link voltage is maintained at the rated voltage of submodule capacitor by using an auxiliary voltage source [126]. It is also possible to achieve the charging of submodule capacitors using a low-voltage auxiliary voltage source [127]. This method is cost-effective and easy to implement. In this method, the submodule capacitors can be charged simultaneously or one after another.

The controlled charging methods have a fast dynamic response and able to limit the inrush current during the start-up process. In [128], a closed-loop current controller is used to control the magnitude of charging current flowing through the submodule capacitors. The current controller also maintains the average DC voltage of each converter leg at their nominal value during normal operation. In [129], the pre-charging of submodule capacitors without auxiliary voltage source is presented. The DC-link voltage of MMC is obtained from the AC-DC converter (passive rectifier). In this method, the submodule capacitors in each arm are simultaneously charged to its nominal value. The charging current is controlled by swapping the working state of submodules and duty cycle of submodule operated in PWM mode. These methods are studied for half-bridge based MMC system only.

1.5 Overview of Model Predictive Control Methods

The model predictive control (MPC) has emerged as a powerful tool to control the power converter systems. The main advantages of MPC are fast dynamic response, simple design, flexibility to include multiple constraints and non-linearities, ease of handling control delays, and robustness against system parameter variations [130–134]. MPC eliminates the use of PI-regulators and modulation stage, thereby significantly improves the dynamic response and controllability [130–134]. The generalized block diagram of MPC approach is shown in Figure 1.11. This approach requires a discrete-time model

of the system to predict the future behavior of the control variables for each valid switching state of the converter. The reference control variables ($\mathbf{x}^*(k)$) are extrapolated to $(k+1)^{\text{th}}$- sampling instant. The predicted ($\mathbf{x}(k+1)$) and the extrapolated ($\widehat{\mathbf{x}}^*(k+1)$) variables are included in a cost function. The cost function consists of multiple control objectives, which are optimized with weight factors to reach the desired system behavior [135–137]. The resulting switching states are applied to the converter.

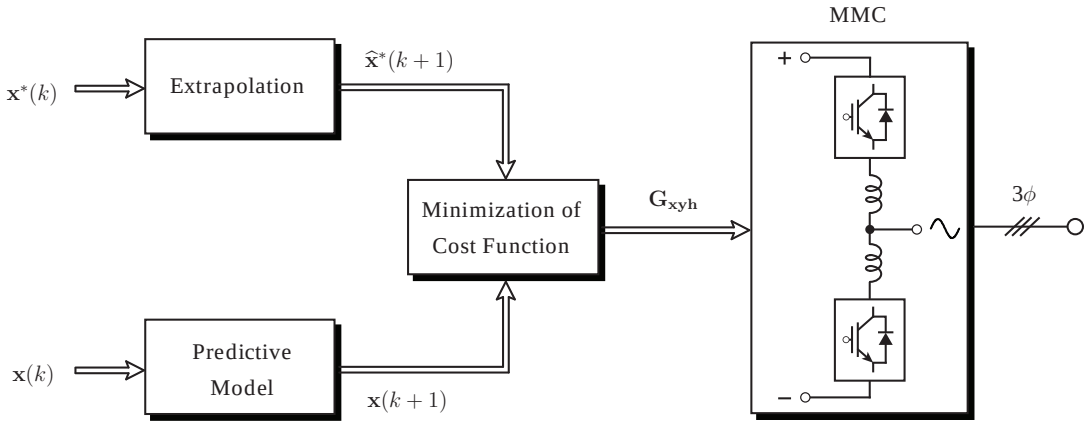


Figure 1.11. Block diagram of model predictive control

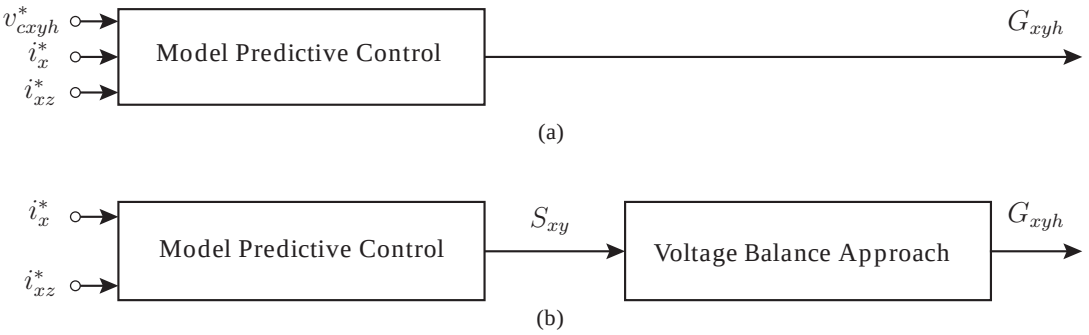


Figure 1.12. MPC schemes for MMC: (a) direct MPC, and (b) indirect MPC

The MPC approach is rigorously investigated for multilevel converters, such as neutral-point clamped (NPC) [138, 139], active NPC [140], flying capacitor [141], cascaded H-bridge [142], matrix converters [143], and hybrid converter topologies [144, 145]. MPC is further extended to the MMC [146].

Based on the design procedure, the MPC approach is categorized into direct model predictive control (D-MPC) and indirect model predictive control (I-MPC) approach as shown in Figure 1.12. In D-MPC, the control goals are achieved using single cost function. In case of I-MPC, the voltage balance strategy is used along with the predictive strategy to achieve the required control objectives.

1.5.1 Direct Model Predictive Control

The direct model predictive control (D-MPC) is one of the model predictive approach, which allows the simultaneous control of output current, circulating currents and submodule capacitors voltage in MMC. These control objectives are included in a cost function and evaluated for all possible switching states [147–149]. The number of switching states drastically increases with the number of submodules, which increases the computational burden on the digital controller.

The per-phase MPC strategy is adopted to control the MMC and to reduce the computational complexity of the real-time implementation [147–149]. Therefore, the D-MPC approach requires to evaluate 2^{2N} switching states per phase to control the MMC with N submodules per arm. The effectiveness of D-MPC is studied under balanced conditions only, where the negative sequence circulating currents are effectively controlled using a cost function [148, 149]. During unbalanced conditions, the zero sequence circulating current causes large ripple in DC-link current and there are no studies about the minimization of ripple in DC-link current using MPC approach.

The per-phase MPC approach is studied for MMC-HVDC systems and not suitable for motor drive systems, where the control of common-mode voltage is one of the primary objectives. The mathematical model of CMV involves the three-phase voltages, which are required simultaneously during the prediction process. Therefore, the three-phase modeling and control is required for motor drive systems. Also, the minimization of ripple in submodule capacitors voltage is also an important aspect in MMC fed motor

drive systems.

1.5.2 Indirect Model Predictive Control

The computational complexity of D-MPC is reduced by using either multiple cost functions to achieve the control objectives or use the voltage balancing strategy with the predictive algorithm. This approach is referred as indirect model predictive control (I-MPC) approach [150–152]. The voltage balancing strategy is used to achieve the voltage balancing between submodules in an arm, while the predictive control algorithm is used to control the output and circulating currents. The predictive algorithm requires $(N+1)^2$ switching states to optimize the cost function, but the dynamic response becomes sluggish [152]. In [153], the submodules in each arm is divided into several groups and sorted them based on the direction of current and their voltages.

In [154], the fast-MPC is presented to improve the dynamic performance of MMC. These approaches evaluate only $3(N+1)$ voltage levels in a three-phase system. The work in [155], analyzed a reduced switching state based MPC approach, where each control objective is achieved through an independent MPC algorithm. However, a further deeper analysis is required to study the dependency of each MPC strategy and their impact on the converter performance. The existing I-MPC approaches operate at high switching frequency and generates an output voltage and current waveforms with higher harmonic distortion, and large ripple in output current.

1.6 Dissertation Objectives

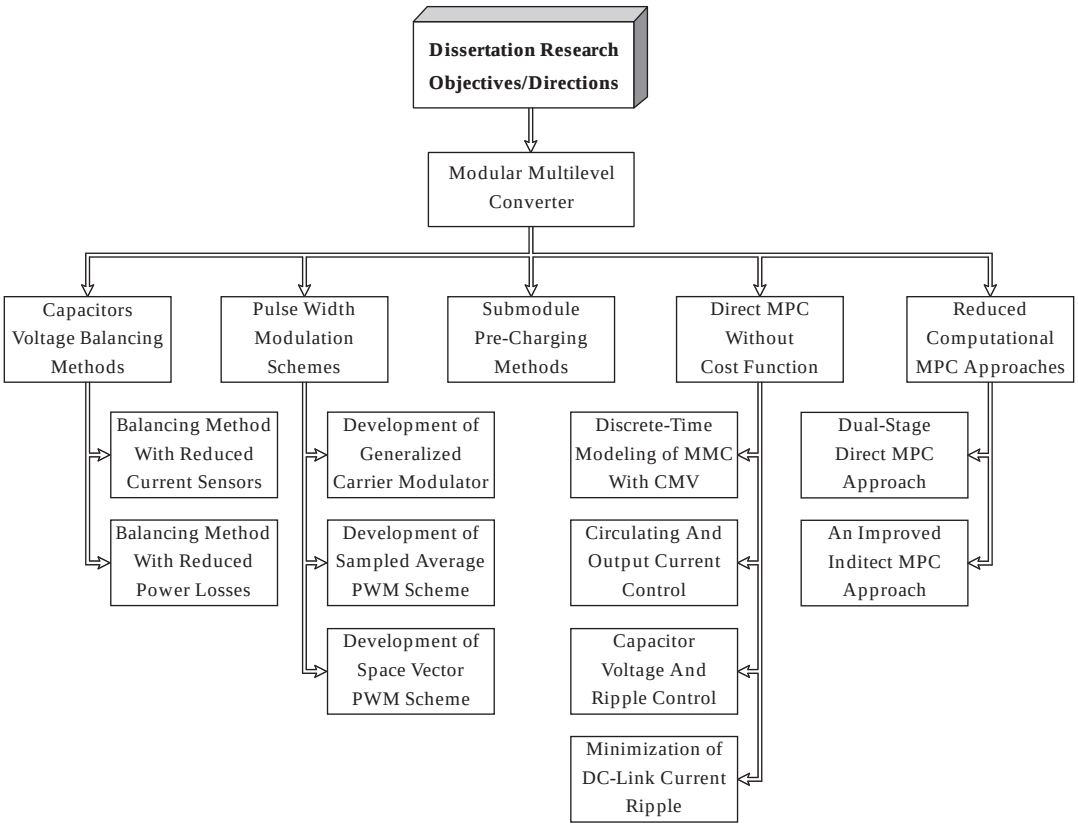


Figure 1.13. Summary of dissertation research.

Aforementioned technical challenges of MMC are addressed in this dissertation. The research objectives and contributions of this dissertation are summarized in Figure 1.13. The first problem addressed in this dissertation is capacitors voltage balancing among submodules with reduced current sensors, power losses and harmonic distortion. The second important aspect is generalized and reduced computational pulse width modulation schemes with improved harmonic performance. Particularly, the development, implementation and submodule capacitors voltage balancing with sampled average and space vector modulation schemes are discussed. The third aspect discussed in this dissertation is pre-charging method for flying capacitor sub-

module based MMC. The next target of this dissertation is to address the capacitors voltage ripple minimization and circulating currents using model predictive control without cost function. Finally, the computational complexity of model predictive control is addressed through novel indirect and dual-stage model predictive control approaches. The main contributions of this dissertation are as follows:

1) **Research on Submodule Capacitors Voltage Balancing Method with Reduced Current Sensors**

The existing voltage balancing methods are customized according to the type of submodule configuration and type of pulse width modulation scheme. Also, the balancing methods require arm current direction for the selection of submodules. The three-phase MMC has six arms and requires six current sensors to measure the arm currents. The system cost can be reduced by eliminating or reducing the number of current sensors.

Considering the above issues, a generalized single-stage voltage balancing method with reduced current sensors is proposed in this dissertation. The proposed approach reduces the required number of current sensors by 50% and is suitable to control both half-bridge and three-level flying capacitor submodule based MMC without any modifications. The proposed approach is also suitable to implement with any pulse width modulation scheme including the fundamental switching frequency schemes.

2) **Research on Submodule Capacitors Voltage Balancing Method With Reduced Power Losses and Harmonic Distortion**

The improper design of balancing method causes uneven submodule switchings in MMC. These additional switchings increase the harmonic distortion of arm currents and output voltages. The harmonic current components and unwanted switchings increase the submodule power losses, which will affect the efficiency of MMC. Also, the total power losses should be equally

distributed between the submodules in each arm. Hence, identical thermal and cooling systems can be used in MMC.

To address these issues, an improved balancing method is proposed in this dissertation. The proposed approach is specifically designed to control the flying capacitor submodule based MMC. This approach is implemented in two stages unlike the existing single stage balancing method and minimizes the voltage harmonic distortion and submodule power losses.

3) Research on Generalized, Reduced Computational Pulse Width Modulation Schemes With Improved Harmonic Performance

As summarized in Figure 1.10, several high and fundamental switching frequency modulation schemes are presented in the literature. Among them, the PSC-PWM and LSC-PWM schemes have very good control capability, when the switching frequency is sufficiently high. However, any change in the number of submodules (i.e., adding new submodules to increase the power rating and output voltage levels or bypassing faulty submodules) effect the arrangement of triangular carrier signals. Hence, the carrier modulator needs to be redesigned by the converter configuration. Other hand, the NLM requires either higher sampling frequency or higher number of submodules in each arm to generate high-quality voltage and current waveforms. Also, an external common-mode voltage (CMV) is added to the modulation signal to minimize the internal unbalance between upper and lower arm submodule capacitors voltage.

In this dissertation, a sampled average PWM and a space vector PWM is proposed to address the above problems. The proposed modulation schemes are generic in nature, computationally less complex and directly applied to MMC with any number of submodules without any modifications. These modulation schemes inherently generate CMV along with the fundamental frequency component across the arms. The magnitude of CMV is controlled by selecting the proper switching vector. The proposed modulation schemes minimize the ripple in output current, output filter size and total harmonic

distortion.

4) Research on Minimization of Submodule Capacitors Voltage Ripple and Circulating Currents Using Direct MPC Approach Without Cost Function

The per-phase methodology is employed to develop the mathematical model of MMC and in the implementation of direct model predictive control (D-MPC) approach. In D-MPC approach, the cost function is used to minimize the circulating currents among the converter legs. The circulating current control ensures the arm voltage balancing and minimizes the submodule capacitors voltage ripple, but its effectiveness is limited.

In this dissertation, a new direct model predictive control with common-mode voltage (CMV) injection is proposed to address the above issues. An accurate discrete-time model of three-phase MMC which includes the common-mode voltage (CMV) is presented to implement the proposed approach. The injection of CMV not only minimizes the capacitors voltage ripple but also significantly reduces the magnitude of circulating currents in the converter legs. The proposed approach also guarantees arm voltage balancing without circulating current control.

5) Research on Reduced Computational MPC Approaches With Improved Harmonic Performance

In direct MPC approach, the control objectives of MMC are included in single cost function and evaluated for all possible switching states. The number of switching states drastically increases with the number of submodules, which further increases the computational complexity of real-time implementation. The reduced computational MPC approach often referred as indirect MPC or fast MPC is presented in the literature. These approaches adopt the classical balancing method with a predictive strategy to achieve the control objectives of MMC. The indirect or fast MPC operates at high-switching frequency,

which is not feasible for high-power applications. Also, the output voltage and current waveform quality is deteriorated due to the unwanted switchings.

In this dissertation, an improved indirect MPC and novel dual-stage direct MPC approaches are proposed. These approaches significantly minimize the computational complexity, harmonic distortion in output voltage and ripple in output current while operating at the lowest switching frequency.

1.7 Dissertation Outline

The research presented in this dissertation is organized in six chapters. The research outline of the dissertation is summarized in Figure 1.14. The work carried out in each chapter is summarized as follows:

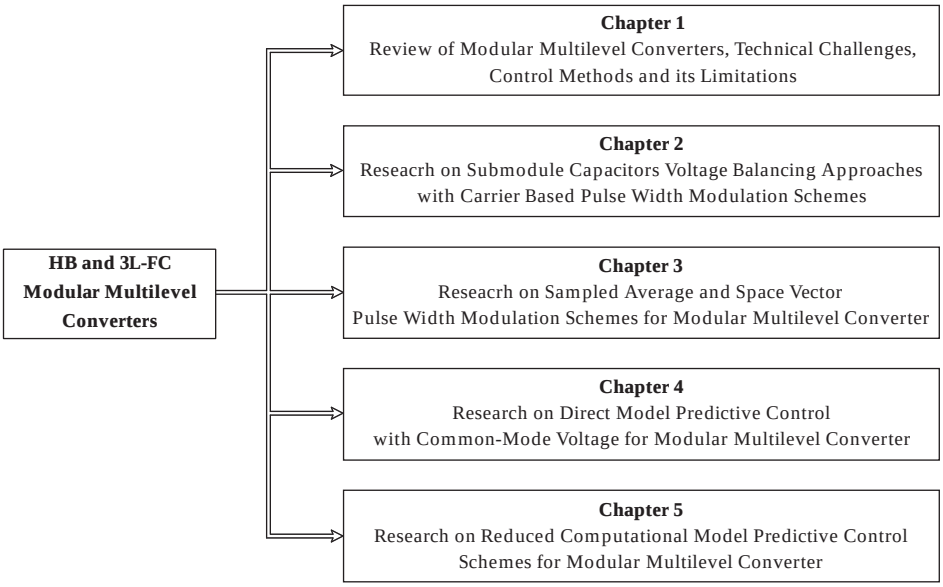


Figure 1.14. Summary of Dissertation Outline.

- **Chapter-1:** In this chapter, the review of the modular multilevel converter and associated technical challenges are presented. Also, the existing control methods and their limitations are discussed. Finally, the research objectives and outline of this dissertation are presented.

- **Chapter-2:** In this chapter, a novel single-stage balancing approach along with a simple pulse width modulator structure is proposed. The dynamic and steady-state performance of single-stage balancing approach are verified on an HB and 3L-FC based MMC with PSC-PWM and LSC-PWM schemes.

  Also, a novel dual-stage balancing approach is proposed for 3L-FC based MMC system. The performance comparison of single and dual-stage balancing approaches are presented in terms of total harmonic distortion, submodule power losses under different modulation indices and power factors. Finally, the pre-charging of submodule capacitors in 3L-FC based MMC system is presented.

- **Chapter-3:** In this chapter, a generalized sampled average pulse width modulation scheme along with voltage balancing approach is proposed. The development and implementation of a modulation scheme and balancing approach are discussed in detail. Simulation and experimental results are presented to validate the dynamic and steady-state performance of the proposed approach. The performance comparison between the sampled average modulation and PSC-PWM schemes are presented in terms of total harmonic distortion and output current ripple.

  Also, a dual space vector modulation scheme is proposed for MMC. In addition, a simple voltage balancing approach with reduced current sensors is proposed to control the submodule capacitors voltage. The step-by-step design procedure of modulation scheme and balancing approach is presented. The dynamic and steady-state performance of proposed methodology are validated through simulations and dSPACE-DS1103 experiments on a three-phase 3L-FC based MMC.

- **Chapter-4:** In this chapter, a novel D-MPC with CMV is proposed. The generalized continuous- and discrete-time modeling of three-phase MMC is presented and analyzed. The step-by-step design procedure of proposed strategy is presented. The regulation of output current, submodule capacitors voltage, minimization of ripple in submodule capacitors voltage, circulating currents and ripple in DC-link current during balanced and unbalanced operating conditions, is discussed in detail. Simulation and experimental results are presented to validate the proposed methodology.

- **Chapter-5:** In this chapter, a reduced computational D-MPC approach, also referred as dual-stage D-MPC approach is proposed. The step-by-step design procedure of dual-stage D-MPC is presented. The performance of proposed approach is evaluated in terms of dynamic response, total harmonic distortion, output current ripple, and computational complexity.

  In addition, an improved I-MPC approach is proposed. The design steps of I-MPC approach are presented. The regulation of output current and submodule capacitors voltage is discussed in detail. The performance comparison of proposed strategy with the existing methodology is presented in terms of dynamic response, switching frequency, total harmonic distortion, output current ripple, and computational complexity. The performance of reduced computational MPC schemes is validated through MATLAB simulations and dSPACE-DS1103 experiments on a three-phase HB-MMC.

- **Chapter-6:** The main contributions and conclusions of this dissertation are summarized in this chapter. The possible extensions and future directions to the research presented in this dissertation are also suggested.

CHAPTER 2

SUBMODULE CAPACITORS VOLTAGE BALANCING METHODS

MODULAR multilevel converters (MMCs) are equipped with low-voltage submodules in cascade to reach the required operating voltage. The number of floating capacitors per submodule vary with the configuration and number of output voltage levels. These floating capacitors are pre-char-ged to their nominal value during a start-up operation and maintained at their nominal value during normal operation. The control of submodule capacitors voltage involves three main objectives such as (i) maintaining the average DC voltage of each converter leg equal to the DC-link voltage, (ii) realize the equal DC voltages between upper and lower arm submodule capacitors, and (iii) maintaining the voltage balancing among submodules in an arm. The first two objectives are achieved using standard closed-loop controllers, while the final objective is realized using either closed-loop controller or balancing algorithm.

This chapter proposes a generalized single-stage voltage based balancing approach to control the half-bridge (HB) and three-level flying capacitor (3L-FC) submodule based MMC. Also, a simple carrier pulse width modulator is presented to implement the balancing approach with PSC-PWM and LSC-PWM schemes. The performance of proposed approach is verified through

simulation and experimental studies on a 3L-FC based MMC. The proposed balancing approach is further extended to control the HB-SM based MMC without any modifications. Also, a dual-stage balancing approach is proposed to improve the performance of MMC. The performance comparison of single-stage and dual-stage balancing approaches are presented in terms of total harmonic distortion and submodule power losses at different load displacement factors and modulation indices. Finally, the step-by-step design procedure to pre-charge the submodule capacitors in 3L-FC based MMC is presented.

2.1 Modular Multilevel Converter and Submodule Configuration

The detailed configuration of MMC and 3L-FC submodule is discussed in the following subsections.

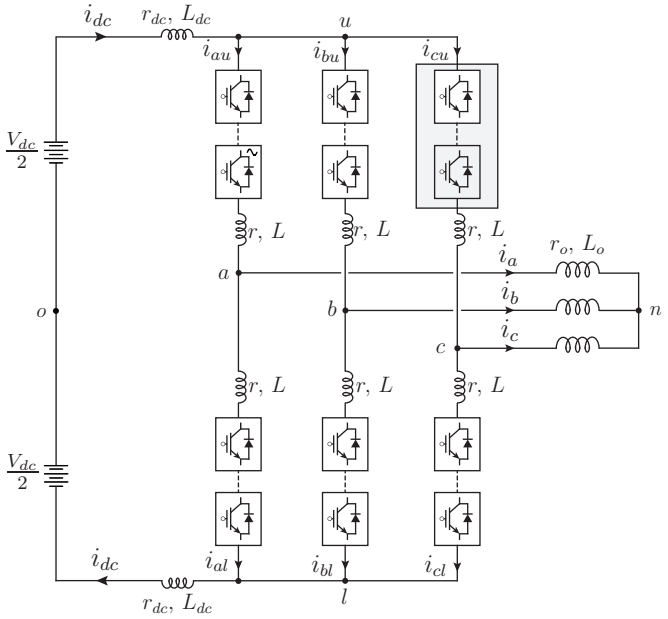


Figure 2.1. Three-phase MMC with passive load

2.1.1 Converter Configuration

The configuration of three-phase MMC with passive load is shown in Figure 2.1. The DC-link voltage is divided into two equal parts with a voltage of $\frac{V_{dc}}{2}$. The DC-line is represented with an equivalent inductance "L_{dc}" and resistance "r_{dc}". Each arm consists of several submodules in series with an inductor "L". The inductor power losses are represented by resistance "r". The three-phase upper and lower arm currents are represented with i_{au}, i_{bu}, i_{cu} and i_{al}, i_{bl}, i_{cl}, respectively. The difference between upper and lower arm current gives the output current flowing through the load. The three-phase output currents are represented with i_a, i_b, i_c.

2.1.2 Three-Level Flying Capacitor Submodule

Figure 2.2(a) shows the configuration of 3L-FC submodule. It is composed of four IGBT devices with antiparallel diodes (S_1, $\overline{S}_1$ and S_2, $\overline{S}_2$) and two DC capacitors (C_1 and C_2). The voltage of DC capacitors C_1 and C_2 is given by

$$\begin{aligned} v_{C1} &= \frac{1}{C_1}\int_{0+}^{t} i_{C1}(\tau)d\tau \\ v_{C2} &= \frac{1}{C_2}\int_{0+}^{t} i_{C2}(\tau)d\tau \end{aligned} \tag{2.1.1}$$

The outer and inner capacitors current (i_{C1} and i_{C2}) is given in terms of device switching states and AC current as follows:

$$\begin{aligned} i_{C1} &= S_1\, i_{xy} \\ i_{C2} &= (S_2 - S_1)\, i_{xy} \end{aligned} \tag{2.1.2}$$

The device switching states (S_1 and S_2) of 3L-FC submodule are shown in Table 2.1. There are total four switching combinations, generates three voltage levels of "0", "$v_{C1} - v_{C2}$" or "v_{C2}", and "v_{C1}" as shown in Figure 2.2(a). The DC capacitor voltage v_{C1} is regulated at twice that of the DC capacitor voltage "v_{C2}", resulting in symmetrical steps in output voltage and reverse

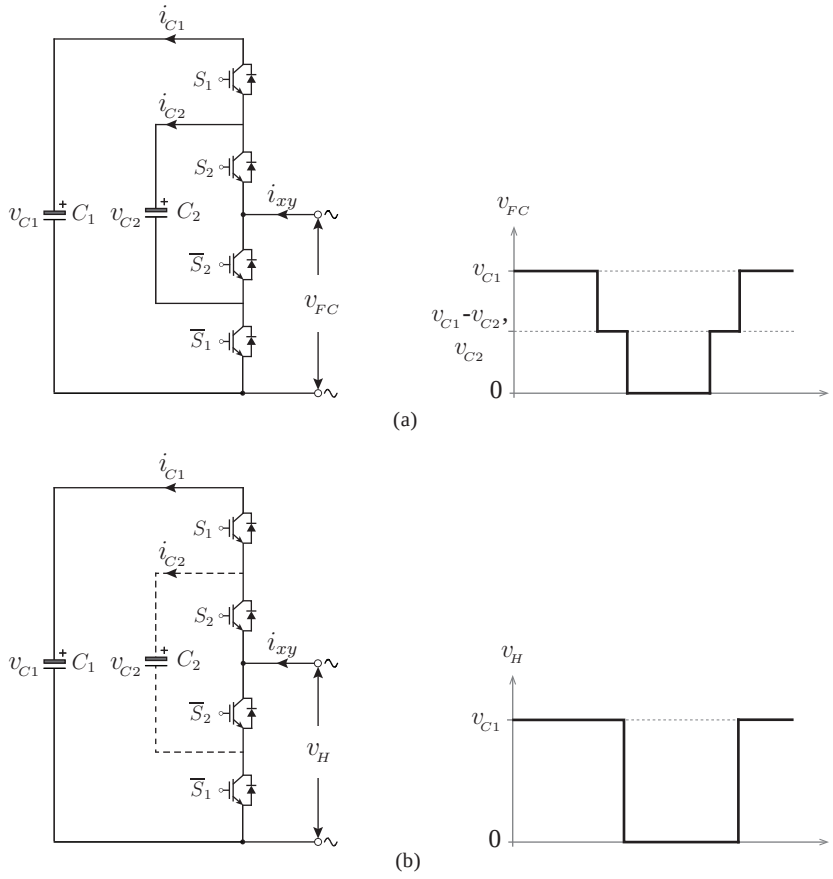


Figure 2.2. 3L-FC submodule and output voltage: (a) three-level operation (b) two-level HB operation

Table 2.1. Switching states of 3L-FC submodule

State	S_1	S_2	v_{FC}	$i_{xy} > 0$	$i_{xy} \leq 0$
⓪	0	0	0	$v_{C1}\approx$,$v_{C2}\approx$	$v_{C1}\approx$,$v_{C2}\approx$
①	0	1	v_{C2}	$v_{C1}\approx$,$v_{C2}\uparrow$	$v_{C1}\approx$,$v_{C2}\downarrow$
②	1	0	$v_{C1} - v_{C2}$	$v_{C1}\uparrow$,$v_{C2}\downarrow$	$v_{C1}\downarrow$,$v_{C2}\uparrow$
③	1	1	v_{C1}	$v_{C1}\uparrow$,$v_{C2}\approx$	$v_{C1}\downarrow$,$v_{C2}\approx$

blocking voltage of IGBT devices. When the devices S_1, S_2 are "ON", the AC output voltage is equal to "v_{C1}". In this mode, the DC capacitor voltage "v_{C1}" increases during the positive direction of current and decreases during the

negative direction. The DC capacitor voltage "v_{C2}" remains constant.

The AC output voltage will be "$v_{C1} - v_{C2}$" for a switching state S_1–"ON", S_2–"OFF". In this mode, the DC capacitor voltage v_{C1} increases and v_{C2} decreases for the positive direction of current, and vice versa. Similarly, for a switching state S_1–"OFF", S_2–"ON", the AC output voltage is equal to v_{C2}. In this mode, the DC capacitor voltage v_{C2} will change, while the DC capacitor voltage v_{C1} remains constant. When the switching state $S_1,\ S_2$ are "OFF", the AC voltage level is "0". The AC output voltage of 3L-FC submodule is given by,

$$v_{FC} = S_1\, v_{C1} + (S_2 - S_1)\, v_{C2} \tag{2.1.3}$$

The 3L-FC submodule requires four semiconductor devices with a voltage rating of v_C and three DC capacitors (rated at v_C), which is three times the capacitors in the full-bridge submodule. The capacitors have different nominal voltages, which results in complex design and control complexity. During normal operation of 3L-FC submodule, maximum two devices carry the current. Efficiency and power losses are comparable to that of FB submodule. The flying capacitor submodule generates only positive voltage levels and can not limit the current during DC-side faults.

The HB-SM operation can be obtained from the 3L-FC submodule. Figure 2.2(b) shows the equivalent operation of HB submodule with 3L-FC submodule. The switching combinations corresponding to the states ② and ⓪ are used to generate the two voltage levels "0" and "v_{C1}" at the output. The DC capacitor C_2 is completely bypassed in this mode of operation. The output voltage of half-bridge submodule is equal to

$$v_H = S_1\, S_2\, v_{C1} \tag{2.1.4}$$

2.2 Phase-Shifted Carrier Modulation Scheme

The triangular carrier signals can be disposed in either horizontally or vertically within the linear modulation range. The modulation scheme with

horizontally disposition of identical triangular carrier signals is referred as phase-shifted carrier modulation (PSC-PWM). In PSC-PWM, all triangular signals have the same frequency and peak-to-peak amplitude, but there is a phase-shift between the adjacent triangular signals. The main features of PSC-PWM are [156]:

- It provides natural balancing of submodule capacitors voltage at high switching frequency (carrier frequency),
- The semiconductor device stress and power handled by each submodule are evenly distributed,
- Eliminates the DC-bus current ripple.

The implementation of PSC-PWM scheme for MMC is mainly consists of the following steps:

2.2.1 Generation of Modulating Signals

Each leg of MMC is divided into two arms, named as upper and lower arms. The submodules in upper and lower arm are modulated to generate the reference output phase voltage. The modulating signals for upper and lower arms are obtained from phase modulating signals. The simplified per-phase equivalent representation of MMC is shown in Figure. 2.3. The submodules in upper and lower arm are modeled as a controlled AC voltage source. The DC system is modeled as a battery source with a voltage V_{dc} and split into two halves. From equivalent circuit, the voltage equations of upper and lower arm are given by [77],

$$\begin{aligned} v_{xu} &= \frac{V_{dc}}{2} - v_{xo} - L\,\frac{di_{xu}}{dt} - r\,i_{xu} \\ v_{xl} &= \frac{V_{dc}}{2} + v_{xo} - L\,\frac{di_{xl}}{dt} - r\,i_{xl} \end{aligned} \tag{2.2.1}$$

where $x \in \{a, b, c\}$ represents the phase. The arm inductor (L) is designed to limit the magnitude of circulating currents flowing through the

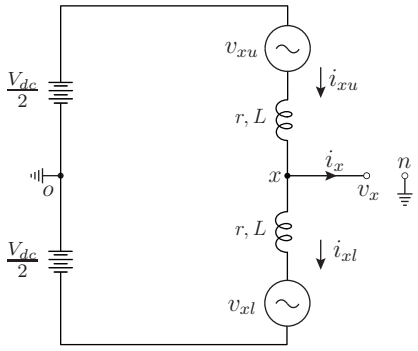


Figure 2.3. Per-phase equivalent circuit

arms. These circulating currents mainly exist due to the switching mismatch between upper and lower arm submodules and ripple in submodule floating capacitors voltage. These circulating currents are controlled using a circulating current control. To simplify the analysis, the submodule capacitors are replaced with ideal battery sources. The delay in switching between the upper and lower arms are also neglected. From equation (2.2.2), the arm modulating signals at steady-state are given as follows:

$$\begin{aligned} v_{xu} &= \frac{V_{dc}}{2} - v_{xo} - v_{xz} - v_{dct} \\ v_{xl} &= \frac{V_{dc}}{2} + v_{xo} - v_{xz} - v_{dct} \end{aligned} \tag{2.2.2}$$

where v_{xu}, v_{xl} represents the upper and lower arm modulating signals, i_{xu}, i_{xl} represents the upper and lower arm currents, v_{xo} represents the phase-modulating signal, v_{xz} represents the voltage component corresponding to the converter internal unbalance, and v_{dct} represents the voltage component corresponding to the total DC-link voltage control.

Depending on the type of application, the phase modulating signals are generated by using either closed-loop or open-loop control methods. In grid connected systems, voltage oriented control (VOC) and the field oriented control (FOC) method in motor drive systems are used to generate the phase modulating signals. In this study, the MMC is connected to a passive load. The phase modulating signals are generated by using an open-loop approach.

The phase modulating signal is defined as follows:

$$v_{xo} = m_a \times \frac{V_{dc}}{2} \sin(\omega_o t + \phi) \tag{2.2.3}$$

where m_a is the amplitude modulation index of range 0 to 1, ω_o is fundamental angular frequency and $\phi \in \left\{0, -\frac{2\pi}{3}, -\frac{4\pi}{3}\right\}$ represents the phase angle in rad.

2.2.2 Generation of Triangular Carrier Signals

To apply the PSC-PWM for MMC with N submodules per arm (R number of capacitors) requires R triangular carrier signals. These R triangular carrier signals are disposed of with a phase angle shift of ϕ_c. The phase shift (ϕ_c) between the carrier angles is given by [77]:

$$\phi_c = \frac{360^\circ}{R} \tag{2.2.4}$$

where $R = N$ for HB-SM and $R = 2N$ for 3L-FC submodule. The upper and lower arm triangular signals are displaced with an interleave angle (ϕ_{ci}) of

$$\phi_{ci} = \frac{360^\circ}{2R} \tag{2.2.5}$$

With an interleave angle between upper and lower arms, the MMC generates an output voltage with $2R + 1$ voltage levels. It is also possible to use the similar triangular carrier signals for upper and lower arms (i.e., ϕ_{ci}=0), resulting an output voltage with $R + 1$ voltage levels. The reduction in voltage levels increases the total harmonic distortion (THD) of the output voltage.

2.2.3 Pulse Width Modulator

The pulse width modulator is designed to generate the gating pattern for submodules in MMC. Figure 2.4 shows the structure of proposed pulse width modulator, which is suitable for any carrier modulation scheme. In this approach, the upper arm modulating signal (v^*_{xu}) is compared with carrier signals $T_1 \ldots T_R$. The output of each comparator is added together to obtain a

normalized voltage waveform (D_{xu}), which resembles the actual output voltage waveform of the upper arm. Similarly, the normalized voltage waveform of lower arm (D_{xl}) is generated by comparing the lower arm modulating signal (v^*_{xl}) with lower arm carrier signals $T_{R+1} \ldots T_{2R}$ and their outputs are added together. The normalized voltage waveform (D_{xu} and D_{xl}) has voltage levels of $0, 1, 2 \ldots, R$ ($R = 2N$ for 3L-FC and $R = N$ for HB-SMs). The normalized voltage waveform represented the required number of ON-state submodules in each arm and given to the voltage balancing approach. Similarly, the proposed modulator can be used with other carrier arrangements such as PD-PWM, POD-PWM, and APOD-PWM schemes.

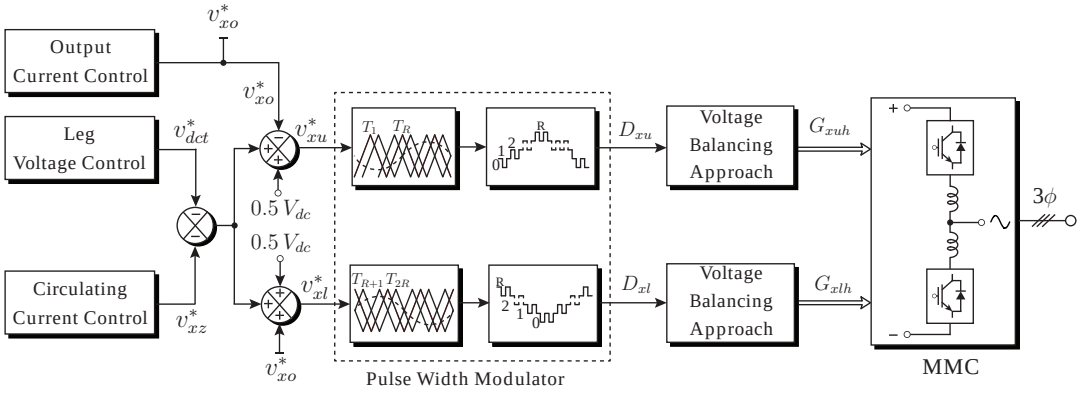


Figure 2.4. Block diagram of pulse width modulator

2.3 Single-Stage Voltage Balancing Approach

The basic principle of voltage balancing approach is to control the charging and discharging of submodule capacitors, depending on the direction of arm current and the instantaneous value of capacitors voltage. For the positive direction of current, capacitors with the lowest voltage and for the negative direction, the capacitors with the highest voltage are inserted in the arm to achieve the voltage balancing. The closed-loop controllers are employed for the robust control of capacitors voltage. However, the complexity of closed-loop controllers increases with the number of submodules per

arm. Alternatively, the redundancy switching states are used to achieve the voltage balancing among submodules. The redundancy switching states are also increases with the number of submodules. For the selection of required switching state from such a high redundancy is difficult and requires sophisticated method.

2.3.1 Design Procedure

The design steps of proposed voltage balancing approach are shown in Figure 2.5(a) and summarized as follows:

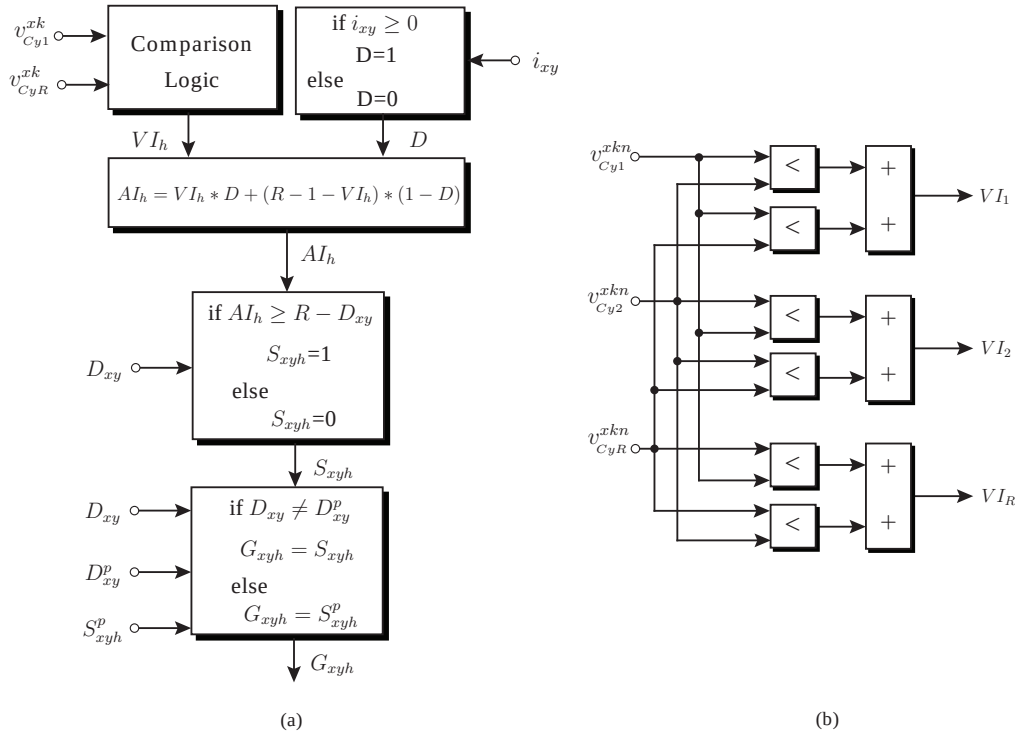


Figure 2.5. Voltage balancing approach: (a) design steps of balancing approach, (b) comparison logic

- **Step-I: Selection of Submodule Capacitors Voltage**

The capacitors voltage comparison logic is shown in Figure 2.5(b) and is utilized for the selection of submodule capacitors voltage in each arm. The comparison logic requires normalized submodule capacitors voltage as input. The normalized capacitors voltage is obtained by dividing the actual capacitors voltage with the rated value. Each 3L-FC submodule has two floating capacitors and their normalized voltages are given by,

$$\begin{aligned} v_{Cy1}^{xkn} &= \frac{v_{Cy1}^{xk}}{V_{C1}} \\ v_{Cy2}^{xkn} &= \frac{v_{Cy2}^{xk}}{V_{C2}} \end{aligned} \tag{2.3.1}$$

where v_{Cy1}^{xkn} and v_{Cy2}^{xkn} are the normalized submodule capacitors voltage, v_{Cy1}^{xk} and v_{Cy2}^{xk} are the actual capacitors voltage, and V_{C1} and V_{C2} are the rated capacitors voltage.

Each normalized submodule capacitor voltage is compared with other normalized capacitors voltage. The output of each comparator is added together and resulting in a virtual index number VI_h. The range of virtual index number is $VI_h \in \{0, 1, \ldots, R-1, R\}$ and $h \in \{1, 2 \ldots, R-1, R\}$. Similarly, the comparison between other capacitors voltage is executed, and their index numbers are obtained. These index numbers are rearranged in either ascending or descending order, depending on the direction of arm current. A simple mathematical expression is presented below to arrange the submodule index numbers.

$$AI_h = VI_h * D + (R - 1 - VI_h) * (1 - D). \tag{2.3.2}$$

where D represents the direction of arm current and is given by

$$D = \begin{cases} 1 & i_{xy} \geq 0 \\ 0 & i_{xy} < 0 \end{cases} \tag{2.3.3}$$

where i_{xy} represents the arm current and, $x \in \{a, b, c\}$ and $y \in \{u, l\}$.

- **Step-II: Generation of Reference Index Number**

The reference index number is generated from the difference between number of submodule capacitors (R) and the normalized voltage waveform (D_{xy}). The reference index number represents the required number of ON-state submodules in each arm to generate the output voltage level. The reference index number is given by

$$\Re = R - D_{xy}. \tag{2.3.4}$$

- **Step-III: Generation of Submodule Switching State**

The switching state of each submodule is generated by comparing the actual index number (AI_h) with the reference index number ($\Re$). If the actual index number is greater than or equal to the reference index number, then the corresponding IGBT device is ”ON” else it will be ”OFF”.

- **Step-IV: Generation of Gating Pattern**

The submodule switching states (S_{xyh}) are applied to the selected IGBT devices (G_{xyh}) for a duration of the normalized voltage level (D_{xy}). If there is a change in the normalized voltage level, then the balancing approach generates new switching state to meet the control objectives. To avoid the intermediate and uneven switchings, the present voltage level (D_{xy}) is compared with the past voltage level (D^p_{xy}). If the present and past voltage levels are equal then the balancing approach apply the switching state corresponding to the past voltage level (S^p_{xyh}) during the present sampling interval.

2.3.2 Comparison of HB and 3L-FC based MMC

In this section, the performance comparison of HB-MMC and 3L-FC MMC systems are presented. The HB and 3L-FC MMC systems are designed with identical system parameters to handle a voltage of 6 kV and power of 2.5 MW.

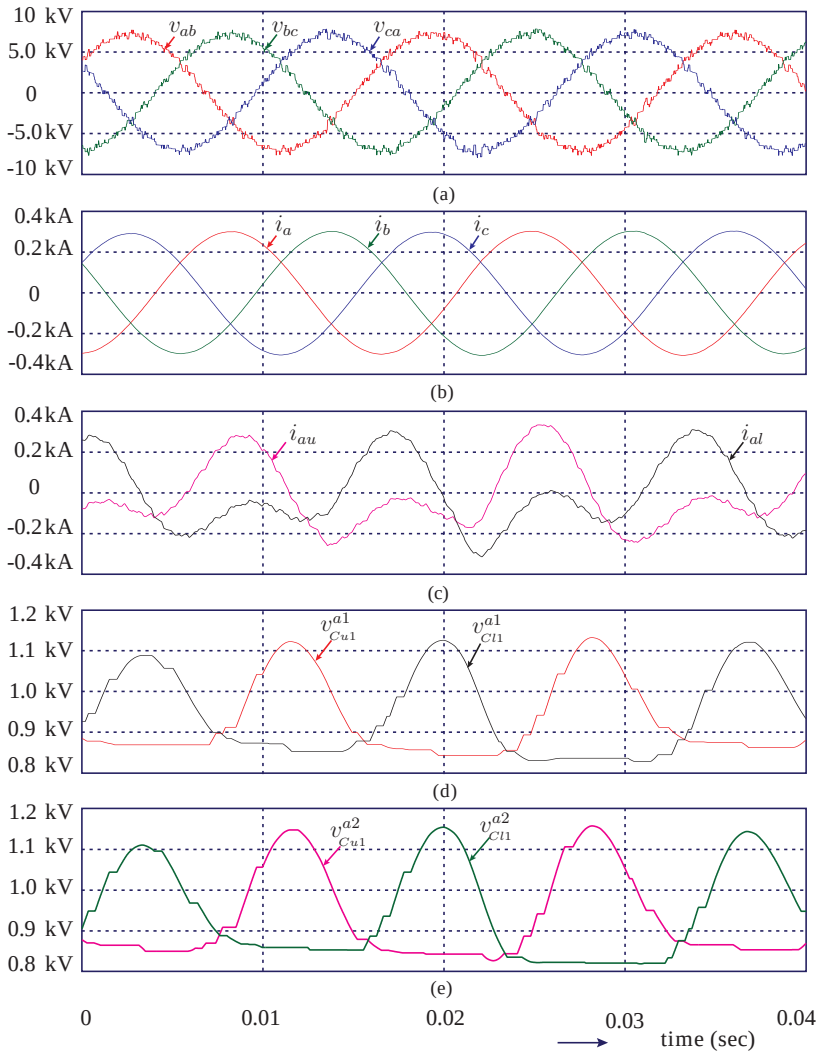


Figure 2.6. Simulation results: (a) output line voltages (b) output line currents (c) upper and lower arm current of phase-a (d) upper and lower arm SM^1 capacitor voltage (e) upper and lower arm SM^2 capacitor voltage

The performance of HB-MMC with $m_a = 0.9$, $f_o = 60$Hz and PF=0 is shown in Figure 2.6. In this study, each arm of HB-MMC consists of ten SMs to generate 21-levels in the line voltage. Each SM capacitor is designed with a capacitance of 2200μF and a nominal voltage of 1 kV. The three-phase line voltages are very close to sinusoidal signal as shown in Figure 2.6(a). The

output voltage has a harmonic distortion of 5.53% as shown in Table 2.2. Figure 2.6(b0 shows the three-phase output currents, which are sinusoidal in nature and has a distortion of 0.59% only. The upper and lower arm current has a dominant second harmonic current of 88.66 A as shown in Figure 2.6(c). The upper and lower arm submodule capacitors voltage is maintained at an average value of 1 kV as shown in Figure 2.6(d)-(e). These capacitors have a peak-peak ripple of 300 V, which is around 30% of nominal voltage.

The 3L-FC based MMC consists of five SMs in each arm to generate 21-levels in the line voltage as that of HB-MMC. Each 3L-FC has two floating capacitors C_1 and C_2, which are designed with a capacitance of 2200μF. The nominal voltage of floating capacitors C_1 and C_2 is 2 kV and 1kV, respectively. The performance of 3L-FC MMC with m_a = 0.9, f_o = 60Hz and PF=0 is shown in Figure 2.7. The three-phase line voltages are very close to sinusoidal signals and have a harmonic distortion of 5.44% as shown in Figure 2.7(a). The three-phase output currents have harmonic distortion of 0.4% as shown in Figure 2.7(b). The second harmonic component in upper and lower arm current is reduced by 45.91% as shown in Figure 2.7(c). The submodule outer and inner capacitors have a peak-peak voltage ripple of 200 V and 84 V, respectively. These ripples are 9% and 8.4% of their nominal voltage as shown in Figure 2.7(d)-(e).

Table 2.2. Comparison of HB and 3L-FC based MMC

Performance Indices	Zero PF (Lag)		Unity PF	
	HB-MMC	3L-FC MMC	HB-MMC	3L-FC MMC
V_{THD}	5.53%	5.44%	3.72%	2.66%
I_{THD}	0.59%	0.4%	3.05%	2.74%
CC (RMS)	88.66 A	40.71 A	52.79 A	22.77 A
V_{C1} Ripple (p-p)	269 V	200 V	180 V	140 V
V_{C2} Ripple (p-p)	300 V	84 V	187 V	80 V

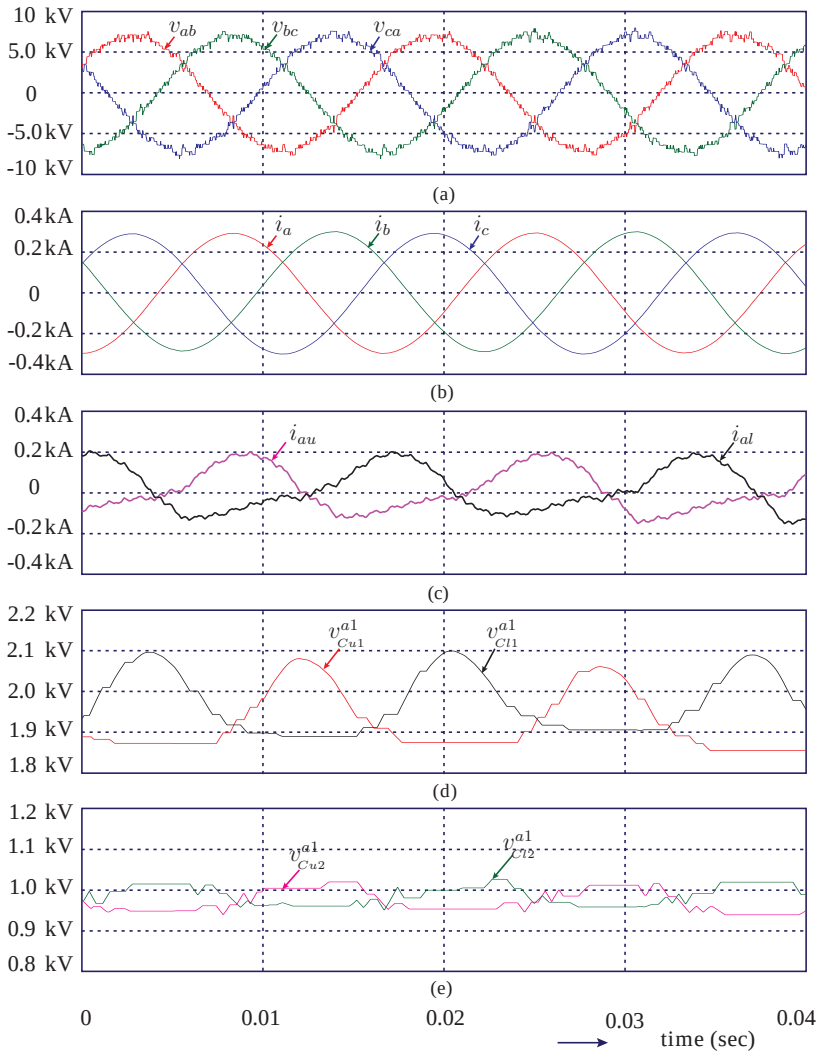


Figure 2.7. Simulation results: (a) output line voltages (b) output line currents (c) upper and lower arm current of phase-a (d) upper and lower arm SM^1 outer capacitor voltage (e) upper and lower arm SM^1 inner capacitor voltage

The performance comparison of HB-MMC and 3L-FC MMC under unity power factor operation is summarized in Table 2.2. With 3L-FC MMC, the V_{THD} and I_{THD} is reduced by 28.49% and 10.16%, respectively. The magnitude of the second harmonic component in the arm current is reduced by 57.82%. Also, the ripple in the outer and inner capacitors voltage is reduced

by 61.11% and 57.2%, respectively. Considering the above advantages, the 3L-FC submodule is a suitable candidate for MMC based motor drive applications.

2.3.3 Dynamic Performance of Single-Stage Voltage Balancing Approach

The simulation studies are conducted on a three-phase MMC with 3L-FC system to validate the effectiveness of proposed voltage balancing approach. The MMC consists of five 3L-FC submodules in each arm to handle a voltage of 6 kV and 2.5 MW power level. The submodule outer and inner capacitors rated voltage are V_{C1} = 2 kV and V_{C2} = 1 kV. The MMC requires a total DC-link voltage of 10 kV to generate an output voltage of 6 kV at unity modulation index.

The dynamic performance of balancing approach is presented with PSC-PWM scheme. Each 3L-FC submodule requires two triangular carrier signals and twenty triangular carrier signals are required to control ten submodules in a converter leg. These triangular carrier signals are disposed of with a phase shift of 18°. The triangular carrier signals belong to the same arm are arranged with a phase shift of 36°. With the above carrier arrangement, the MMC generates an output voltage with 21-levels. The frequency of each triangular carrier signal is selected as 180 Hz, and the average switching frequency (f_{sw}) of the converter is equal to 3600 Hz.

- **Dynamic Performance With Step Change in Modulation Index**

The dynamic performance of balancing approach is presented with a step change in the modulation index (m_a), and corresponding results are shown in Figure 2.8. Initially, the converter is operating at steady-state with a modulation index of m_a = 0.5 and frequency f_o = 60 Hz. The submodule outer and inner capacitors voltage is maintained at 2 kV and 1 kV, respectively as shown in Figure 2.8(a)-(b). The outer and inner capacitors have peak-peak voltage ripple of 3.95% and 4.2%, respectively.

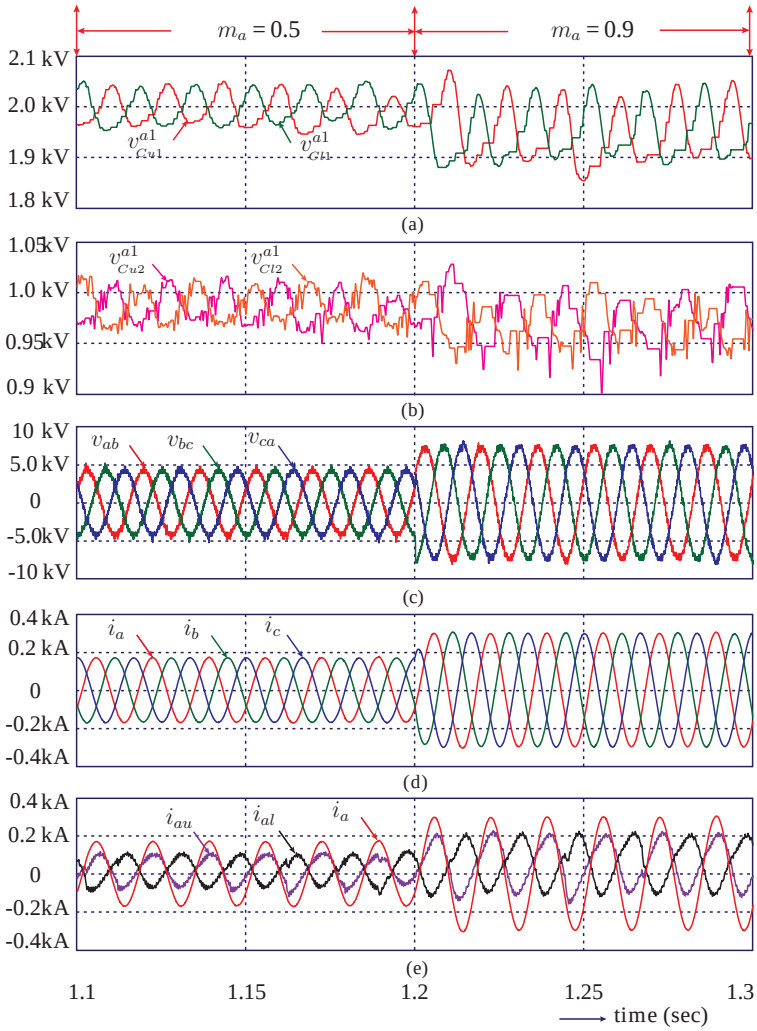


Figure 2.8. Simulation results for dynamic performance: (a) upper and lower arm SM^1 outer capacitor voltage (b) upper and lower arm SM^1 inner capacitor voltage (c) three-phase line-line voltages (d) three-phase line currents (e) upper, lower arm and phase-a line current

The converter generates 12-level output voltage waveform across the load, corresponding to a modulation index as shown in Figure 2.8(c). The three-phase currents are sinusoidal in nature and has a peak value of 190 A as shown in Figure 2.8(d). The output fundamental frequency current component is equally distributed between upper and lower arms as shown in Figure

2.8(e). Also, the arm current consists of DC current component along with the second harmonic current component.

At t = 1.2 s, the modulation index is changed from 0.5 to 0.9 and frequency kept constant. Even though there is an external disturbance, the balancing approach is effectively maintaining the capacitors voltage at their rated value as shown in Figure 2.8(a)-(b). The magnitude of the output voltage and current flowing through the load is proportionally increased with the modulation index as shown in Figure 2.8(c)-(d). The increased number of levels in the output voltage significantly minimizes its harmonic distortion. Due to the increment in load current, the outer and inner capacitors peak-peak voltage ripple are increased by 7.15% and 8.5%, respectively. Figure 2.8(e) shows that the shape of the arm current waveform at m_a = 0.5 and m_a = 0.9 are very close except its magnitude.

- **Dynamic Performance With and Without Balancing Approach**

The converter performance with and without voltage balancing approach is shown in Figure 2.9 and Figure 2.10. At t = 0 s, the voltage balancing approach is activated. The converter is operating with m_a = 0.9 and f_o = 60 Hz. The balancing approach maintains the upper and lower arm submodule outer capacitors voltage at 2 kV as shown in Figure 2.9(a)-(b). The upper and lower arm submodule inner capacitors voltage is maintained at 1 kV as shown in Figure 2.9(c)-(d). Therefore, the reverse blocking voltage across each device is equal to 1 kV. The converter generates a balanced output voltage and sinusoidal currents across the load as shown in Figure 2.10(a)-(b). The output currents are equally distributed between upper and lower arm as shown in Figure 2.10(c)-(d).

At t = 0.07 s, the balancing approach is disabled. During this period, the converter is controlled with open loop PWM scheme. The submodule outer and inner capacitors voltage are diverging from their nominal value as shown in Figure 2.9. The increment (or) decrement in the submodule capacitors voltage depends on their duty cycles. The uneven submodule capacitors

voltage affects the device reverse blocking voltages and, output voltage and current waveform quality as shown in Figure 2.10(a)-(b). In addition, the magnitude of arm current exceeds the rated value, which affects the reliability and performance of the converter as shown in Figure 2.10(c)-(d). At $t = 0.1$ s, the voltage balancing approach is enabled. The balancing approach can bring back the submodule capacitors voltage to their nominal value.

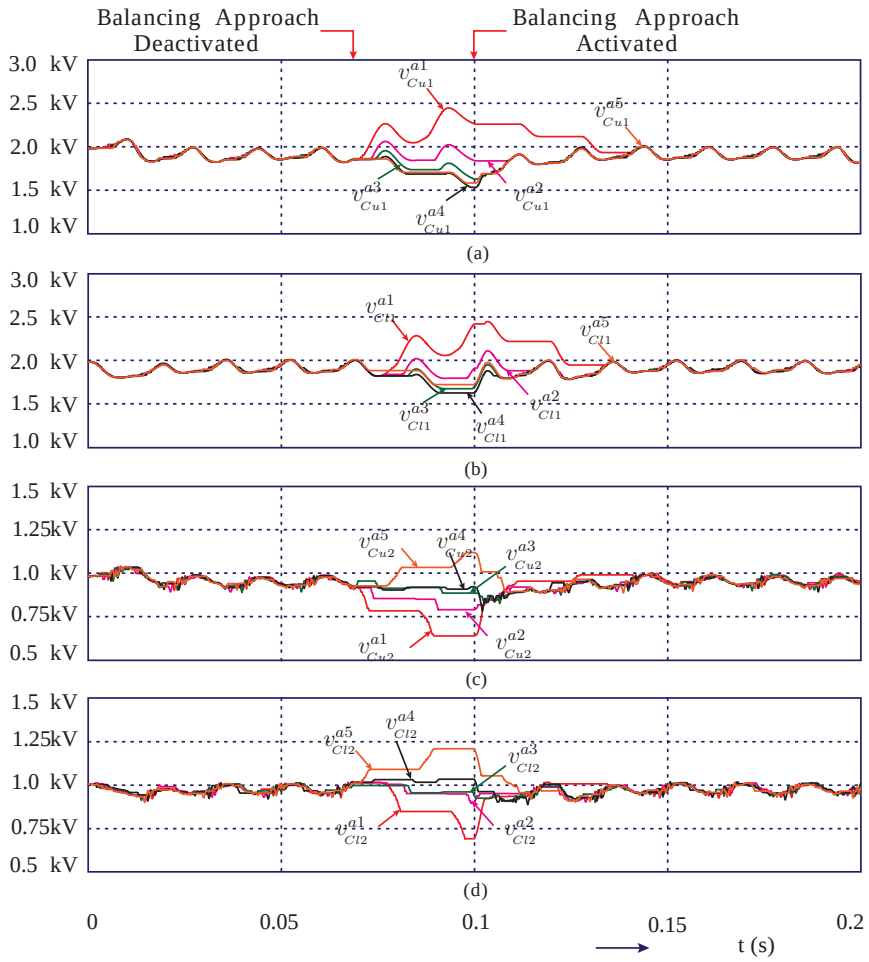


Figure 2.9. Simulation results: (a) upper arm submodule outer capacitors voltage (b) lower arm submodule outer capacitors voltage (c) upper arm submodule inner capacitors voltage, and (d) lower arm submodule inner capacitors voltage

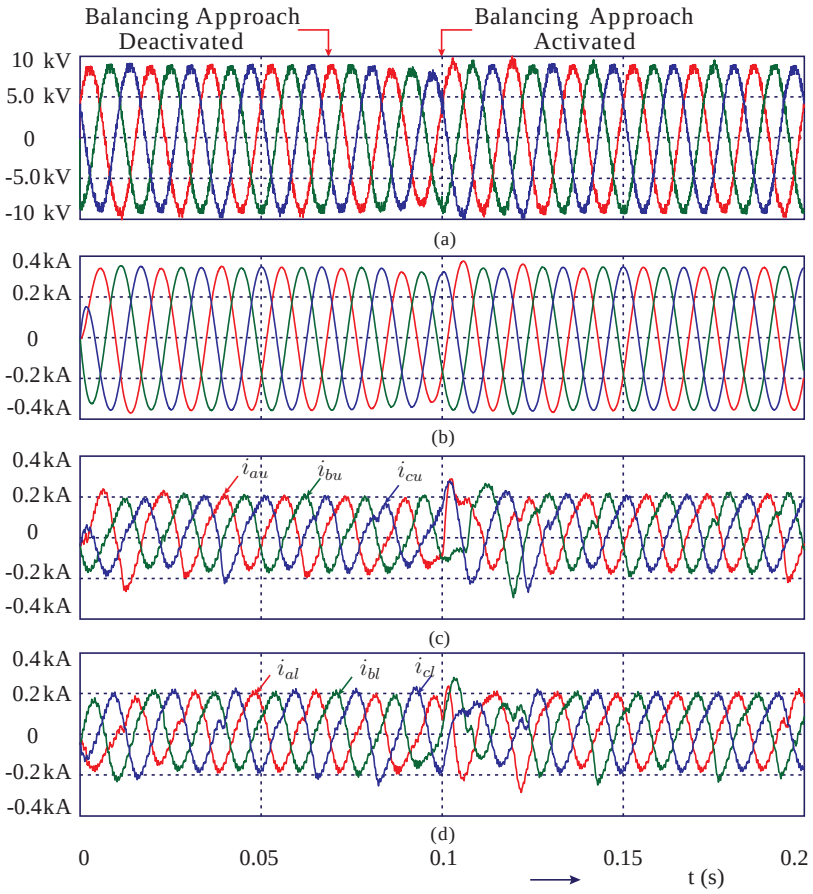


Figure 2.10. Simulation results: (a) three-phase line-line voltages (b) three-phase line currents (c) three-phase upper arm currents (d) three-phase lower arm currents

- **Performance With Different Submodule Capacitances**

The submodule capacitors voltage ripple increases with the reduction in the size of the capacitor. These voltage ripples affect the shape of arm current, circulating current, and output voltage harmonic distortion of MMC. The half-bridge submodule consists of a single floating capacitor and any variation in its size has a direct impact on the AC side performance. In contrast, the 3L-FC submodule has two floating capacitors. These capacitors are referred as outer capacitor (C_1) and inner capacitor (C_2). In this study, the effect

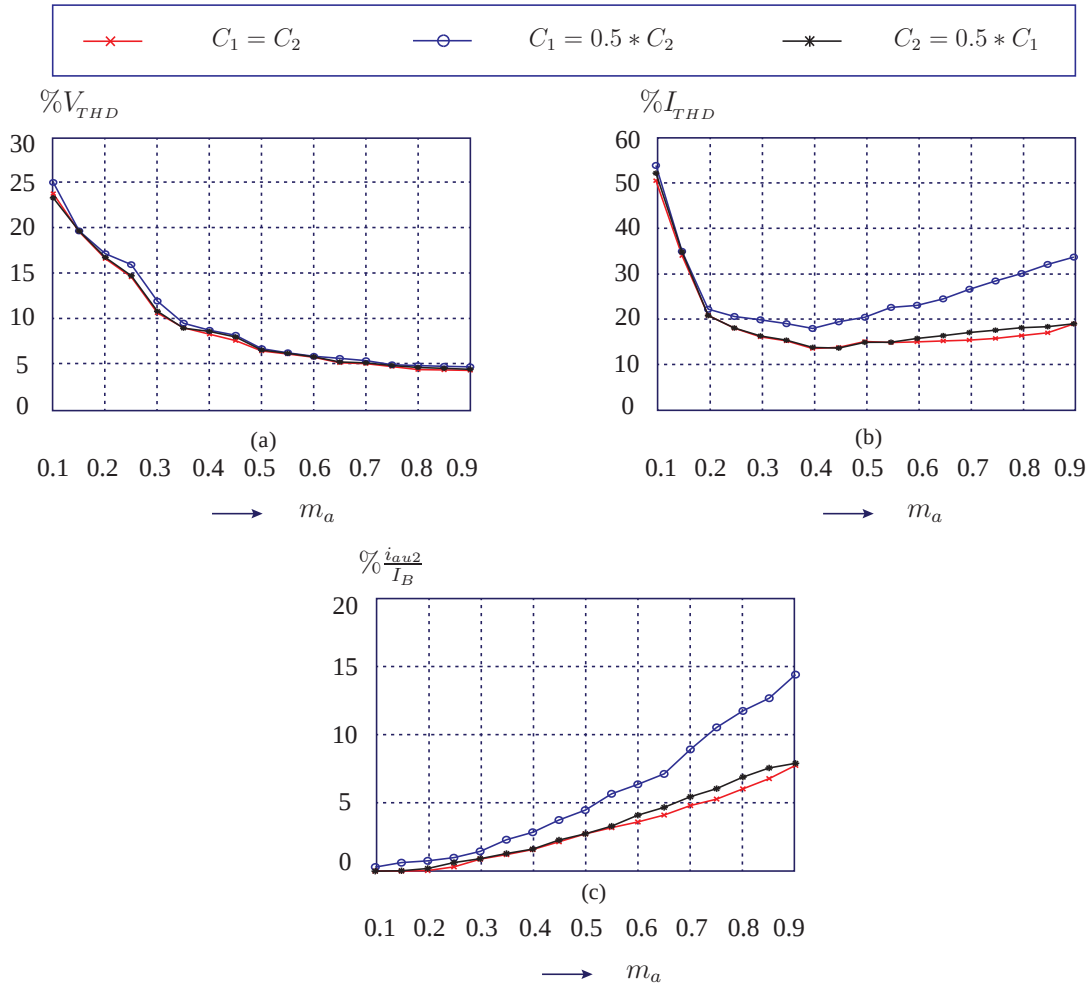


Figure 2.11. Simulation results: (a) output line voltage harmonic distortion (b) arm current harmonic distortion (c) second harmonic current component

of outer and inner capacitors size on the converter performance is analyzed. The 50% variation in outer capacitor size is selected such that the stored energy is equal to the energy stored in half-bridge submodule.

The simulation results are presented for the following three cases.

- Case-I : outer and inner capacitors size is equal ($C_1 = C_2$)
- Case-II : outer capacitor is 50% smaller than the inner capacitor ($C_1 =$

$0.5 * C_2$)

- Case-III: inner capacitor is 50% smaller than the outer capacitor ($C_2 = 0.5 * C_1$)

In this study, the case-I is used as a reference to compare the case-II and case-III performances. In case-I, the harmonic distortion of the output voltage and arm current is 4.33% and 19.38%, respectively. The circulating current mainly consists of a second harmonic component of 0.18 pu. In case-II, The output voltage and arm current harmonic distortions are increased by 9% and 75.33%, respectively. In case-III, the harmonic distortion and magnitude of the second harmonic current component are very close to the value obtained in case-I. The analysis is conducted at different modulation indices, and their performance is shown in Figure 2.11. These results show that the case-I and case-II performances are very close in the complete operation range. Also, the magnitude of the second harmonic current component increases with the reduction in outer capacitor size. In overall, the outer capacitor size has a dominant effect on the AC side performance compared with the inner capacitor size.

2.3.4 Experimental Validation

To validate the performance of proposed balancing approach, a low power experimental prototype of 208 V, 3 kVA rated three-phase modular multilevel converter (MMC) with 3L-FC submodule is developed. Each 3L-FC submodule is constructed by using Semikron dual pack SKM100GB12T4 IGBT / diode modules of 1200 V, 100 A capacity, SKHI22-B dual-core IGBT gate drivers, and EPCOS DC capacitors. The submodule is designed such that the laboratory prototype can be easily extended to higher operating voltage and output voltage levels by connecting the submodules in cascade. The MMC is controlled by using dSPACE / DS1103 research and development control platform. The capacitors voltages and current feedback signals are measured by LEM LV25-P and LA55-P sensors, respectively. The measurements are sent

to the controller through a CP1103 I/O connector. The input DC-link voltage is generated by using Xantrex DC power source of 600 V, 20 A capacity.

The prototype consists of two 3L-FC submodules per leg and requires four triangular carrier signals. The four triangular carrier signals are arranged with a phase-shift of 90° and carrier signals belong to the same arm are arranged with a phase-shift of 180°. With the above carrier arrangement, the MMC generates line voltage with a maximum nine voltage levels. The carrier signals are generated with a frequency of 540 Hz and the average switching frequency of MMC is equal to 2160 Hz. The submodule outer and inner capacitors voltage are rated to V_{C1}=350 V and V_{C2}=175 V.

- **Dynamic Performance**

The dynamic performance of proposed voltage balancing approach is presented with a step change in the modulation index (m_a). Initially, the MMC is operating with m_a=0.5 and f_o=60 Hz. The three phase line-line voltages and line currents are shown in Figure 2.12(a) and Figure 2.12(b), respectively. The line voltages (v_{ab}, v_{bc}, v_{ca}) have five levels with a voltage step of 87.5 V and output currents (i_a, i_b, i_c) have a peak value of 5 A.

The phase-a, upper and lower arm SM_1 outer and inner capacitors voltage (v_{Cu1}^{a1}, v_{Cu2}^{a1}, v_{Cl1}^{a1}, v_{Cl2}^{a1}) is presented in Figure 2.12(c). The results show that the outer and inner capacitors voltage is regulated at $346V$ and $173V$, respectively. The steady-state voltage error can be eliminated by using leg and arm voltage balancing controller. The upper and lower arm current of phase-a (i_{au} and i_{al}) is shown in Figure 2.12(d) and their difference is equal to the current flowing through the load. After some time, the modulation index is changed from m_a=0.5 to m_a=0.9 and frequency kept constant. The voltage balancing approach is perfectly maintaining the submodule capacitors voltage at its rated value. The number of levels in the line voltage is increased from five to nine. The output current has a magnitude of 10 A, which is also proportionally increased with the modulation index.

Further, the converter operation is presented with and without voltage

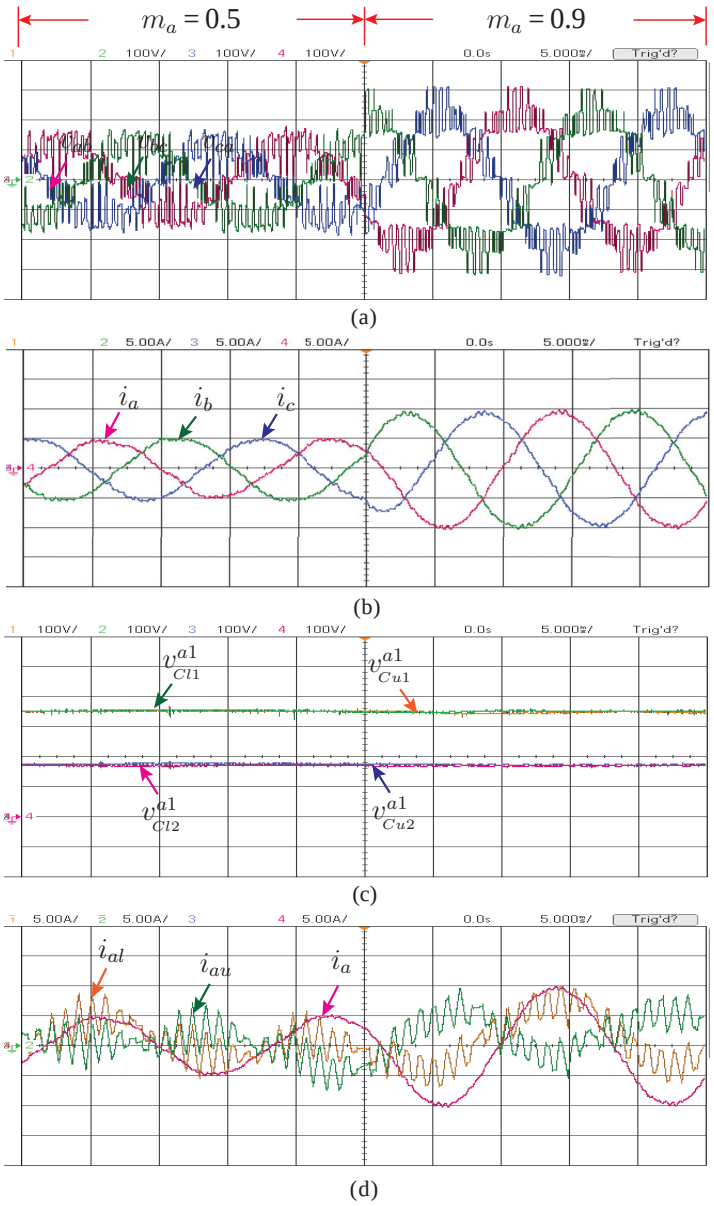


Figure 2.12. Experimental results with step change in modulation index: (a) three-phase output line voltages, (b) three-phase output currents, (c) upper and lower arm submodule capacitors voltage, and (d) upper, lower arm and output current

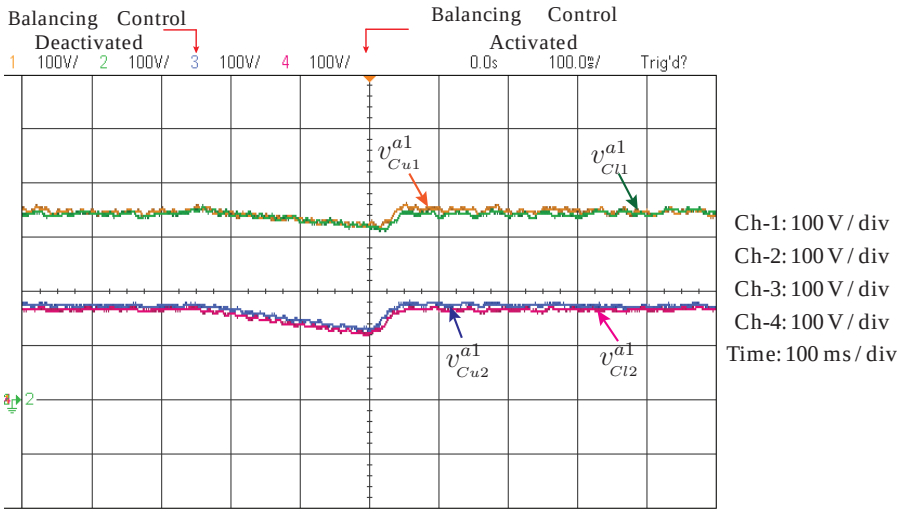


Figure 2.13. Submodule capacitors voltage with and without balancing approach

balancing approach and their results are shown in Figure 2.13. Initially, the converter is operating with the balancing approach at m_a=0.9 and f_o=60 Hz. With the help of proposed approach, the submodule capacitors voltage is maintained at the rated value. At t=250 ms, the voltage balancing algorithm is deactivated. During this period, the gating signals are directly generated based on the intersection of the carrier and modulating signals. The results show that the diverging of submodule capacitors voltage towards zero value. If the converter continues to operate without voltage balancing approach, then the submodule capacitors voltage becomes zero. Instead, the voltage balancing approach is reactivated at t=500 ms. The balancing approach can bring back the submodule capacitors voltage to its rated value. In overall, the proposed voltage balancing approach is successfully maintaining the submodule capacitors voltage at their nominal value under external disturbance as well.

- **Performance With LSC-PWM Scheme**

The proposed pulse width modulator and balancing approach can be extended to the LSC-PWM scheme without any modifications. Particularly,

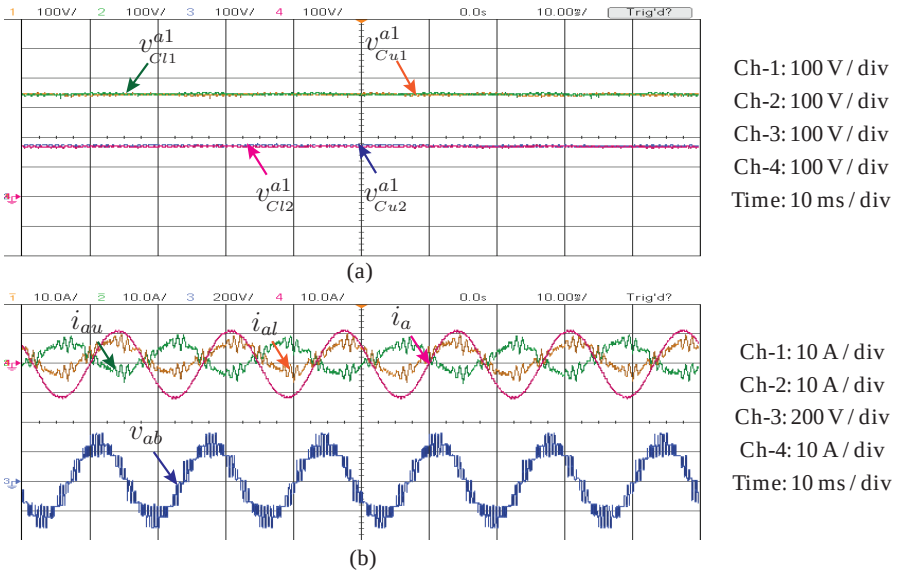


Figure 2.14. Experimental results with for PD-PWM scheme: (a) upper and lower submodule capacitors voltage and (b) output voltage and current waveforms

the phase-disposition PWM (PD-PWM) scheme is considered to control the MMC with 3L-FC submodules. Only, the triangular carrier signals are re-arranged according to the requirement of PD-PWM scheme. The performance of the MMC-3L-FC system with PD-PWM scheme is shown in Figure 2.14. The results are presented for m_a=0.9, f_o=60 Hz, and carrier frequency f_c=1080 Hz. The results show that the phase-a, upper and lower arm outer and inner capacitors voltage (v_{Cu1}^{a1}, v_{Cu2}^{a1}, v_{Cl1}^{a1}, v_{Cl2}^{a1}) is maintained at their rated value as shown in Figure 2.14(a). The converter generates line voltage (v_{ab}) with nine levels and output current (i_a) with 10 A peak value as shown in Figure 2.14(b). The upper and lower arm current (i_{au} and i_{al}) has less switching ripples compared to the PSC-PWM scheme as shown in Figure 2.14(b).

- **Extended Operation With Half-Bridge Submodule**

The proposed balancing approach is extended to the MMC with half-bridge submodules as well. In this system, each arm consists of two half-bridge submodules with identical nominal voltages. Each submodule capacitor voltage

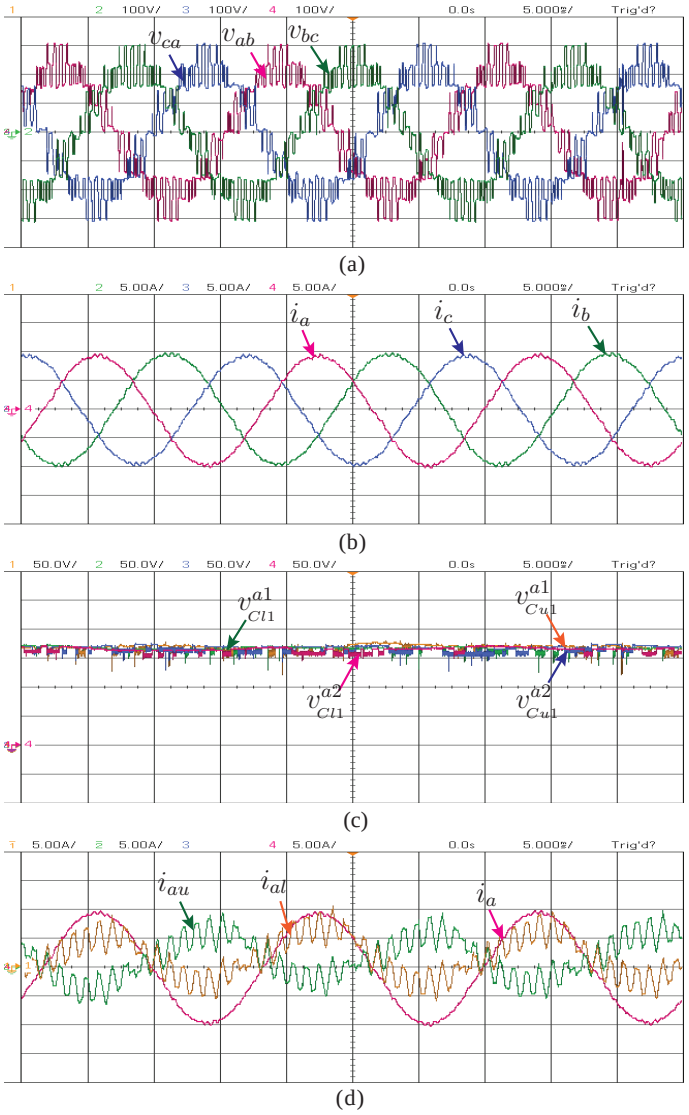


Figure 2.15. Experimental results for MMC with HB-SM: (a) three-phase output line voltages, (b) three-phase output currents, (c) upper and lower arm submodule capacitors voltage, and (d) upper, lower arm and output current

is rated for 175 V. The performance of HB based MMC system with PSC-PWM scheme is shown in Figure 2.15. The results are presented for m_a=0.9, f_o=60 Hz and carrier frequency f_c=540 Hz. The three-phase output voltages and currents are perfectly balanced as shown in Figure 2.15(a)-(b). The

phase-a, upper and lower arm SM^1 and SM^2 capacitors voltage (v_{Cu1}^{a1}, v_{Cu1}^{a2}, v_{Cl1}^{a1}, v_{Cl1}^{a2}) is maintained at their nominal value of $175V$ as shown in Figure 2.15(c). The upper and lower arm current has similar shape and ripple as that of 3L-FC based MMC as shown in Figure 2.15(d). In overall, the proposed approach can be easily implemented with any CPWM scheme to control the MMC (2L-HB and 3L-FC submodules) without any major modifications.

2.4 Dual-Stage Voltage Balancing Approach

The dual-stage voltage balancing approach is proposed to improve the performance and reduce the computational complexity of single-stage balancing approach. The single-stage approach requires $2N \times (2N-1)$ comparisons to implement the sorting technique for an MMC with N-3L-FC submodules per arm ($2N$ submodule capacitors). Other hand, the dual-stage approach requires $0.5 \times N \times (N-1)$ comparisons, which are quite low in comparison to the single-stage methods.

2.4.1 Submodule Energy Distribution

The energy stored in the phase-x, outer and inner capacitor of k^{th}-SM is given by

$$E_{Cy1}^{xk} = \frac{C_1}{2}(v_{Cy1}^{xk})^2,\ E_{Cy2}^{xk} = \frac{C_2}{2}(v_{Cy2}^{xk})^2. \tag{2.4.1}$$

where E_{Cy1}^{xk} and v_{Cy1}^{xk} represents the energy and voltage of k^{th}-SM, outer capacitor, and E_{Cy2}^{xk} and v_{Cy2}^{xk} represents the energy and voltage of k^{th}-SM, inner capacitor. The total energy stored in the k^{th}-SM is obtained from the equation (2.4.1) as follows:

$$E_y^{xk} = E_{Cy1}^{xk} + E_{Cy2}^{xk}, \tag{2.4.2}$$

where k represents the SM index number. Each arm of MMC has N-SMs in cascade. The total arm energy (E_{xy}) is equal to the sum of energy stored in

N-SMs as follows:

$$E_{xy} = \sum_{k=1}^{N} E_{Cy}^{xk}. \tag{2.4.3}$$

The total arm energy is equally distributed between the SMs in each arm as follows:

$$E_y^{x1} = E_y^{x2} = \ldots = E_y^{xN}. \tag{2.4.4}$$

The relationship between the AC and DC side SM power is given by,

$$\frac{dE_{xy}}{dt} = p_{xy}. \tag{2.4.5}$$

The instantaneous AC power of each arm (p_{xy}) is given by,

$$p_{xy} = v_{xy}\, i_{xy}, \tag{2.4.6}$$

where $x \in \{a, b, c\}$ represents the phase, $y \in \{u, l\}$ represents the arm and, v_{xy} and i_{xy} represents the arm voltage and arm current. From equation (2.4.3) and (2.4.5), the symmetrical energy distribution ensures identical power handling capability on AC side of the SM and given as follows:

$$p_y^{x1} = p_y^{x2} = \ldots = p_y^{xN}. \tag{2.4.7}$$

The instantaneous value of SM output power is given by,

$$p_y^{xk} = v_y^{xk}\, i_{xy}. \tag{2.4.8}$$

2.4.2 Principle of Operation

The proposed approach is implemented in two-stages to handle the objectives of 3L-FC based MMC such as voltage balancing among submodules and internal capacitors voltage balancing of 3L-FC submodule (i.e., maintaining the 50% voltage difference between outer and inner capacitors voltage).

- **Stage-I: Energy Balancing Among Submodules**

In this stage, the SMs are arranged in either ascending or descending order based on their energy and the direction of arm current. The SM energy is calculated using the equations (2.4.1) and (2.4.2). Each arm has N-SMs and their energies are stored in an array of $E_y^{xk} = \{E_y^{x1}, E_y^{x2}, \ldots, E_y^{xN}\}$. The direction of arm current (D) is obtained from

$$D = \begin{cases} \text{Ascending} & i_{xy} \geq 0 \\ \text{Descending} & i_{xy} < 0 \end{cases} \tag{2.4.9}$$

The SMs energy is sorted using a sorting algorithm and corresponding indices are given by:

$$I^k = \text{sort}\,(E_y^{xk}, D), \tag{2.4.10}$$

where I^k is an array, which contains the indices of SMs energy. These energies are arranged in ascending order for the positive direction of arm current. Therefore, the SMs with the lowest energy is inserted in the arm to charge them. Similarly, the SMs with the highest energy is inserted to discharge them during the negative direction of arm current. The number of inserted SMs vary with the required voltage level, which is obtained from the modulation stage.

The modulation stage gives the information of required voltage level and is distributed symmetrically between the submodules. The distribution of voltage levels between the submodules is presented for N=3 per arm in Table 2.3. For example, the required voltage level of $L_v = 2$ is generated using two submodules with a voltage of v_C and one submodule is turned off. Similarly, the output voltage level $L_v = 5$ is generated using two submodules with a voltage of $2v_C$ and one submodule with a voltage of v_C. These voltage levels are assigned to the submodules based on their energy as follows:

$$SM(I^k) = M_L^k \tag{2.4.11}$$

where SM represents the array of submodule output voltage levels.

Table 2.3. Assignment of voltage level to SMs

L_v	M_L^1	M_L^2	M_L^3
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	2	1	1
5	2	2	1
6	2	2	2

- **Stage-II: Internal Capacitors Voltage Balancing of 3L-FC Submodule**

Once the voltage level has been assigned to the submodules, the next step is to generate the gating pulses. From Table 2.4, the voltages levels ”0” and ”2” are generated by using the states ⓪ and ③, respectively. However, the voltage level ”1” can be generated by using the states either ① or ②. These states are referred as redundancy states. The redundancy states are selected based on the error between outer and inner capacitor voltage.

Table 2.4. Switching table of 3L-FC SM

state	S_1	S_2	v_{xy}/V_C	i_{C1}/i_{xy}	i_{C2}/i_{xy}
⓪	0	0	0	0	0
①	0	1	1	0	1
②	1	0	1	1	-1
③	1	1	2	1	0

The normalized voltage error of k^{th}-SM is defined as follows:

$$\Delta V_y^{xk} = \frac{v_{Cy1}^{xk}}{V_{C1}} - \frac{v_{Cy2}^{xk}}{V_{C2}} \tag{2.4.12}$$

where V_{C1} and V_{C2} are the nominal voltage of capacitors C_1 and C_2, respectively.

Table 2.5. Selection of redundancy switching states

	$i_{xy} > 0$	$i_{xy} \leq 0$
$v_{Cy1}^{xk}/V_{C1} > v_{Cy2}^{xk}/V_{C2}$	①	②
$v_{Cy1}^{xk}/V_{C1} < v_{Cy2}^{xk}/V_{C2}$	②	①

From Table 2.5, the variation of capacitors voltage for state ① is given as

$$\begin{aligned} \Delta v_{Cy1}^{xk} &= 0 \\ \Delta v_{Cy2}^{xk} &= \frac{T_s}{C_2} i_{xy} \end{aligned} \tag{2.4.13}$$

where T_s is the sampling time. The voltage error for switching state ① is given by

$$\Delta V_y^{xk①} = D_y^{xk} - T_s \frac{1}{C_2\, V_{C2}}\, i_{xy} \tag{2.4.14}$$

The voltage variation for switching state ② is given by,

$$\begin{aligned} \Delta v_{C1}^{xk} &= \frac{T_s}{C_1} i_{xy} \\ \Delta v_{C2}^{xk} &= -\frac{T_s}{C_2} i_{xy} \end{aligned} \tag{2.4.15}$$

Hence, the voltage error for switching state ② is given as follows:

$$\Delta V_y^{xk②} = D^{xk} + T_s \left(\frac{1}{C_1\, V_{C1}} + \frac{1}{C_2\, V_{C2}} \right) i_{xy} \tag{2.4.16}$$

From equations (2.4.14) and (2.4.16), it is observed that the voltage error depends on the switching state, initial voltage error (D_y^{xk}) and the direction of arm current. From equation (2.4.12), if $\frac{v_{Cy1}^{xk}}{V_{C1}} > \frac{v_{Cy2}^{xk}}{V_{C2}}$ then the voltage error becomes $\Delta V_y^{xk} > 0$. To minimize the voltage error, the state ① is applied for $i_{xy} > 0$. If the direction of arm current is negative ($i_{xy} \leq 0$), then the state ② is applied to the submodule.

2.4.3 Design Procedure

The implementation of proposed balancing approach mainly involves the logical functions corresponding to the Tables described in the Section 2.4.2. The design steps of dual-stage voltage balancing approach are shown in Figure 2.16 and are summarized as follows:

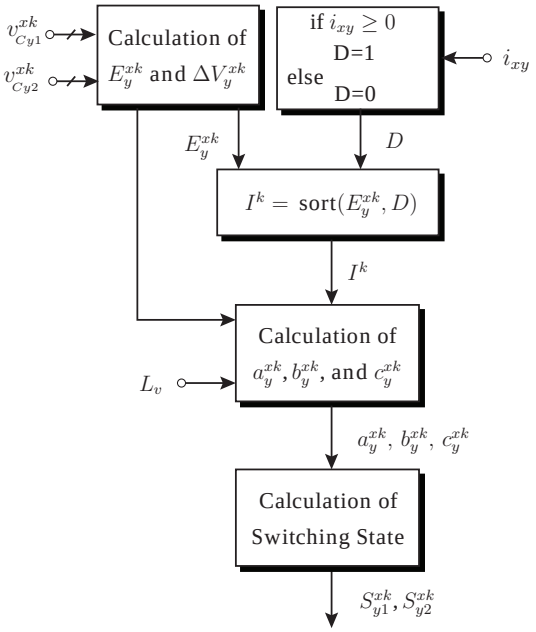


Figure 2.16. Dual-stage voltage balancing approach

- Define the parameters C_1 and C_2, normalized SM capacitors voltage v_{Cy1}^{xkn} and V_{Cy2}^{xkn}, and the number of SMs per arm N inside the argument,
- Measure the SM capacitors voltage v_{Cy1}^{xk} and v_{Cy2}^{xk}, and arm current i_{xy},
- Calculate the SMs energy using the equations (2.4.1) and (2.4.2),
- Calculate the voltage error using the equation (2.4.12),
- Obtain the direction of arm current using the equation (2.4.9),

- Arrange the SMs in either ascending or descending order based on the SMs energy and the direction of arm current using the sorting technique given in the equation (2.4.10),
- Obtain the voltage level L_v from the modulation stage,
- Assign the voltage levels to the SMs (M_L^k), which is given as

$$M_L^k = a_y^{xk} + b_y^{xk}, \tag{2.4.17}$$

The constants a_y^{xk} and b_y^{xk} are obtained from the comparison between voltage level (L_v) and SM energy indices as follows:

$$\begin{aligned} a_y^{xk} &= \begin{cases} 1 & L_v \geq I^k \\ 0 & L_v < I^k \end{cases} \\ b_y^{xk} &= \begin{cases} 1 & L_v \geq (I^k + N) \\ 0 & L_v < (I^k + N) \end{cases} \end{aligned} \tag{2.4.18}$$

- According to the Table 2.5, if the product between the sign of the arm current and the voltage difference is positive, then the state ① is applied to the converter. On the contrary, if the product is negative, then the state ② must be applied. Hence, the logical function c_y^{xk} is defined based on the voltage error (ΔV_y^{xk}) and the direction sign of arm current as follows:

$$c^{xk} = \begin{cases} 1 & (\Delta V_y^{xk} * \text{sign}(i_{xy})) \leq 0 \\ 0 & (\Delta V_y^{xk} * \text{sign}(i_{xy})) > 0 \end{cases} \tag{2.4.19}$$

- The possible switching state of devices S_{y1}^{xk} and S_{y2}^{xk} are given in Table 2.6. These switching states are mathematically represented using the logical variables given in (2.4.18) and (2.4.19) as follows:

$$\begin{aligned} S_{y1}^{xk} &= a_y^{xk}\,(b_y^{xk}\,\overline{c_y^{xk}} + c_y^{xk}) \\ S_{y2}^{xk} &= a_y^{xk}\,(b_y^{xk}\,c_y^{xk} + \overline{c_y^{xk}}) \end{aligned} \tag{2.4.20}$$

Table 2.6. Generation of gating signals

a_y^{xk}	b_y^{xk}	c_y^{xk}	S_{y1}^{xk}	S_{y2}^{xk}
0	0	0	0	0
0	0	1	0	0
0	1	0	-	-
0	1	1	-	-
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	1	1

2.4.4 Dynamic Performance of Dual-Stage Voltage Balancing Approach

The main objective is to verify the energy balancing between the SMs in one arm and the control of capacitors voltage in each SM. Therefore, the per-phase structure of MMC with three 3L-FC SMs per arm is considered. Each SM has two floating capacitors with a nominal voltage of V_{C1}=120 V and V_{C2}=60 V. The two floating capacitors are designed with a capacitance of 1000 μF. The nominal value of energy stored in the outer capacitor is E_{C1} = 7.2 J and the inner capacitor are E_{C2} = 1.8 J. The total energy stored in each SM is equal to the sum of outer and inner capacitors energy of E = 9 J.

- **Dynamic Performance With Step Change in Modulation Index**

The dynamic performance of proposed approach is validated with the step change in the modulation index. Initially, the converter is operating at a modulation index of m_a = 0.5 and frequency of f_o = 60 Hz. The converter generates 7-level voltage waveform with a voltage step of 30 V across the load as shown in Figure 2.17(a). The magnitude of arm and load currents is proportionally generated with the modulation index as shown in Figure 2.17(b).

The peak value of load current is around 6 A, corresponding to the modulation index 0.5. The balancing approach maintains upper arm SMs energy at 9 J as shown in Figure 2.17(c). The SM outer capacitors voltage is regulated

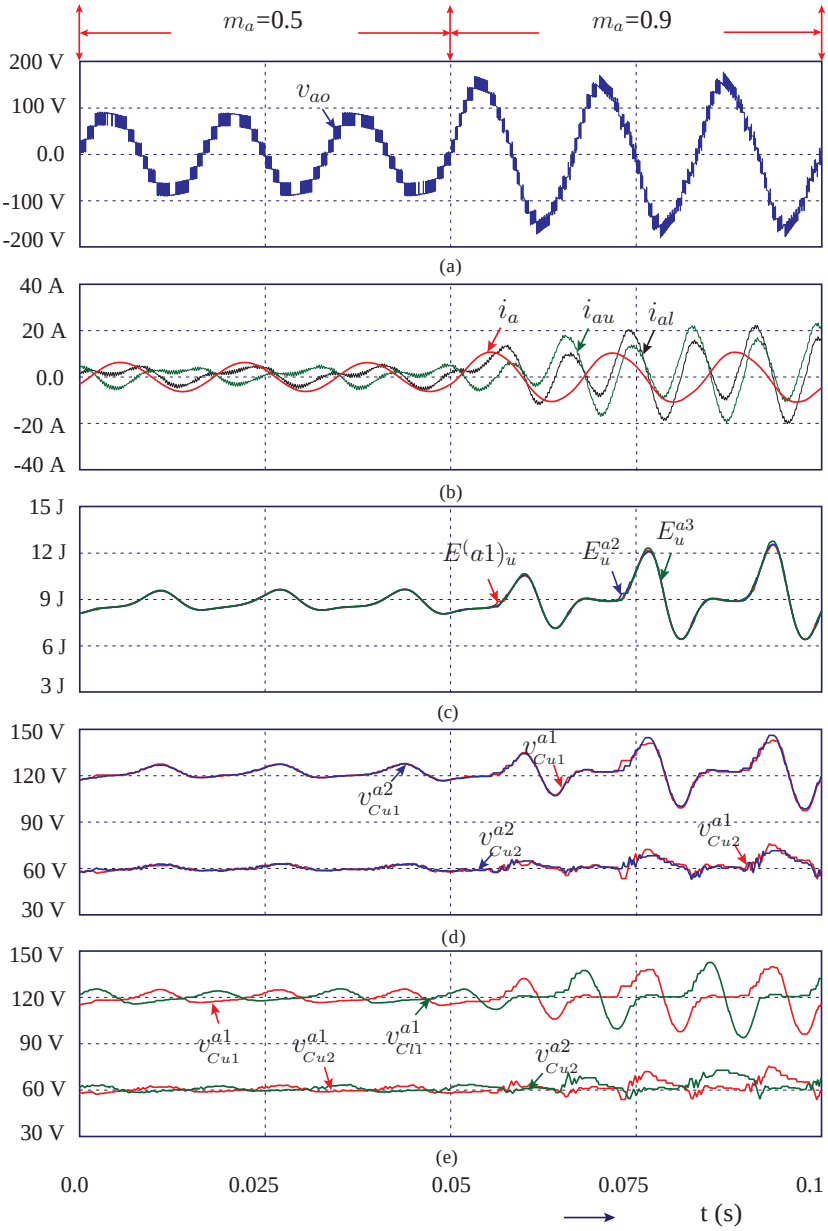


Figure 2.17. Dynamic performance: (a) output voltage, (b) upper, lower arm and output currents, (c) upper arm SMs energy, (d) upper arm SM^1 and SM^2 capacitors voltage, and (e) upper and lower arm SM^1 capacitors voltage.

at 120 V and corresponding SM inner capacitors voltage is regulated at 60 V as shown in Figure 2.17(d). Similarly, the lower arm SM capacitors voltage is regulated at their nominal value as shown in Figure 2.17(e). At $t = 0.05$ s, a step change in modulation index from $m_a = 0.5$ to $m_a = 0.9$ is applied. The magnitude of output current and output voltage levels is proportionally increased with the modulation index. The balancing approach maintains all the SMs energy and corresponding capacitors voltage at their nominal values. The ripple in SMs energy and capacitors voltage increases proportionally with the magnitude of load current.

- **Dynamic Performance With and Without Balancing Approach**

In this study, the two capacitors in each SM is designed with a capacitance value of 1000 μF. The nominal value of energy stored in outer capacitor is 7.2 J and the inner capacitor are 1.8 J. The total energy stored in each SM is equal to the sum of outer and inner capacitors energy, which is equal to 9 J. The dynamic performance of proposed energy balancing approach is shown in Figure 2.18. Initially, the balancing approach is enabled with a modulation index of $m_a = 0.9$ and frequency of $f_o = 60$ Hz. The balancing approach maintains all the SMs energy at their nominal value of 9 J as shown in Figure 2.18(a). The SM outer capacitors are regulated at 120 V and inner capacitors at 60 V as shown in Figure 2.18(b). Similarly, the lower arm SM capacitors voltage is regulated at their nominal value as shown in Figure 2.18(c).The converter generates a symmetrical sinusoidal output voltage waveform of 120 V peak with voltage steps of 15 V as shown in Figure 2.18(d). The output load current is equal to the difference of upper and lower arm currents as shown in Figure 2.18(e).

From $t = 0.05$ s to $t = 0.1$ s, the balancing approach is disabled. The SM capacitor voltages and corresponding energies are diverging from their nominal value. During this process, the converter generates highly distorted voltage and current waveforms across the load. At $t = 0.1$ s, the balancing approach is enabled again, and the system returns to the normal operation.

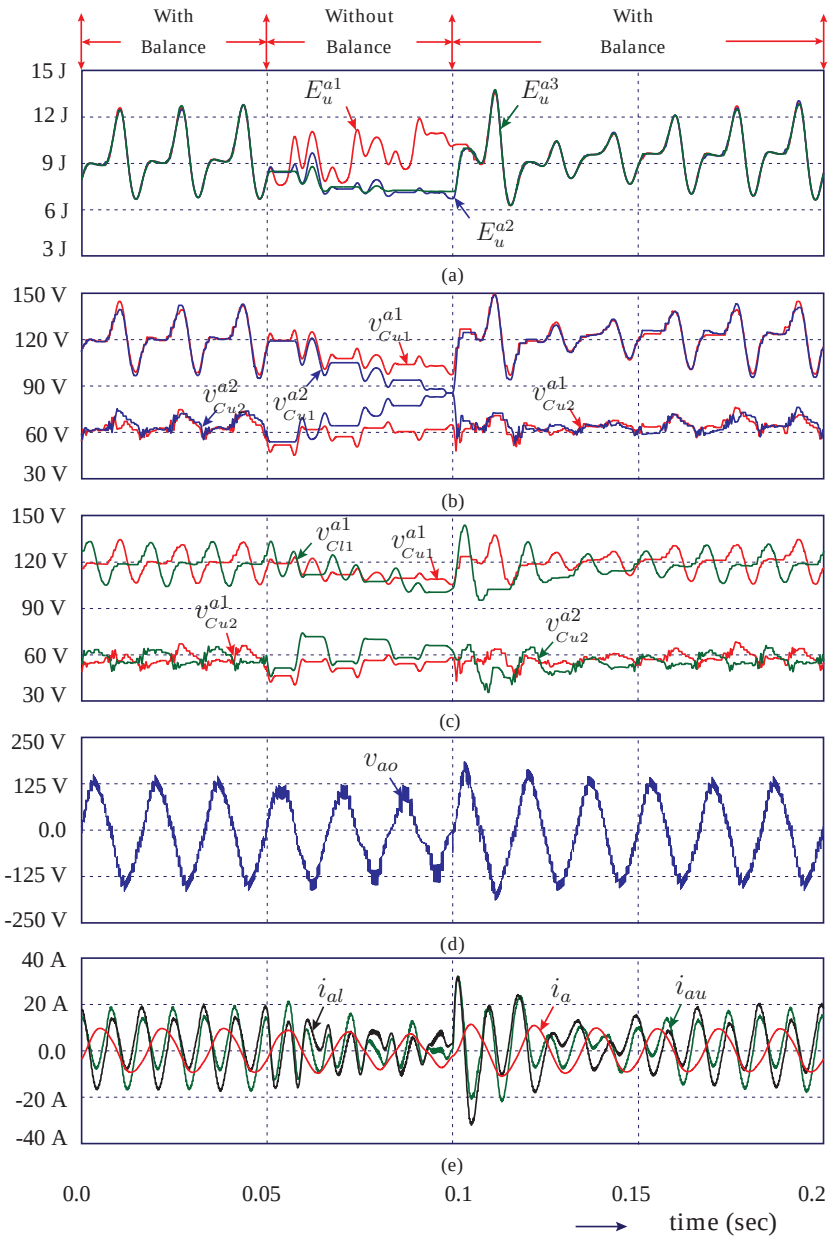


Figure 2.18. Dynamic performance: (a) upper arm SMs energy, (b) upper arm SM^1 and SM^2 capacitors voltage, (c) upper and lower arm SM^1 capacitors voltage, (d) output voltage, and (e) upper, lower arm and output currents.

During the disabling of balance approach, the performance of load is significantly deteriorated. Therefore, the balancing approach is required to achieve better converter and load performance.

- **Submodule Power Losses**

The submodule power losses are evaluated at different load power factors with the curve fitting techniques. Each 3L-FC submodule consists of four IGBT devices with anti-parallel diodes. The device power losses (P_{dev}) are given by

$$P_{dev} = P_t + P_d \tag{2.4.21}$$

where P_t represents the power losses in the transistor and P_d represents the power losses in the diode. The losses in the transistor consist of conduction losses (P_{tc}, on-state (P_{ton}) and off-state (P_{toff}) losses as follows:

$$P_t = P_{tc} + P_{ton} + P_{toff} \tag{2.4.22}$$

The power losses in the diode is given by,

$$P_d = P_{dc} + P_{dr} \tag{2.4.23}$$

where P_{dc} and P_{dr} represents the conduction and reverse recovery losses of the anti-parallel diode in IGBT.

The loss distribution between the SMs in each arm with dual-stage balancing approach at zero power factor is shown in Figure 2.19(a). The submodules in upper arm have identical power losses ($P_{_{SM^1}}$, $P_{_{SM^3}}$, $P_{_{SM^3}}$) and proportionally increases with the modulation index. The power loss analysis is further extended to other load power factors. The SM^1 power losses at zero and unity power factors are shown in Figure 2.19(b). The submodules have higher power losses at zero power factor operation compared with the unity power factor. At zero power factor, the submodule capacitors voltage has large second harmonic voltage ripple. These voltage ripples increase the magnitude of circulating currents and thereby the power losses in the submodules.

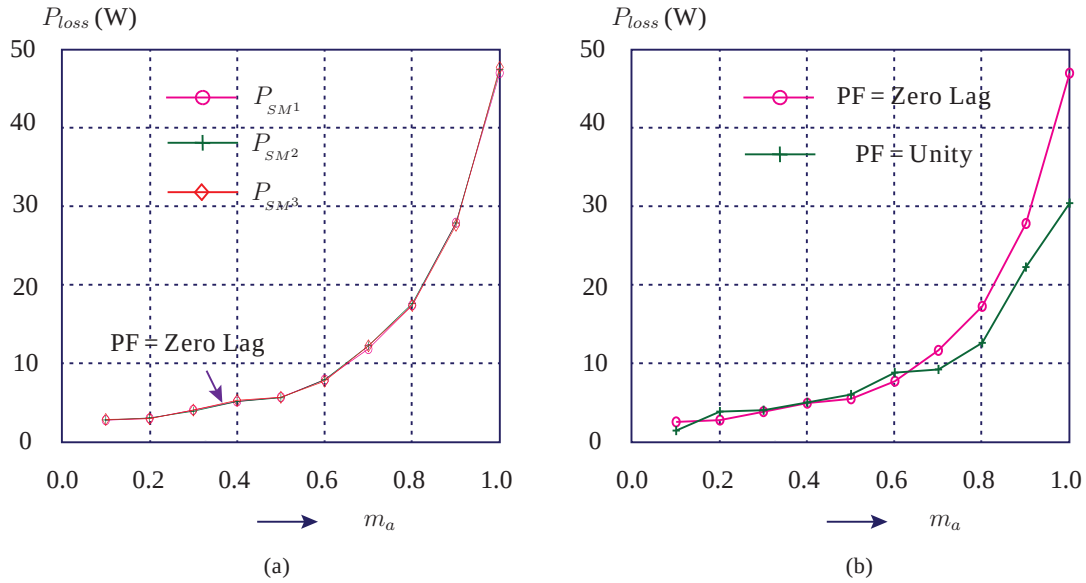


Figure 2.19. Analysis of submodule power losses: (a) upper arm submodule power losses, and (b) submodule power losses at different power factors

2.4.5 Experimental Validation

To validate the simulation study, a low power 3L-FC based MMC laboratory prototype is developed. Due to the limitations of control platform, the per-phase structure of MMC is considered to validate the performance of proposed approach. Each arm consists of three 3L-FC SMs per arm with a total DC bus voltage of 360 V.

- **Dynamic Performance**

The dynamic performance of the dual-stage approach is shown in Figure 2.20. Initially, the balancing approach is enabled with m_a=0.9 and f_o=60 Hz. The balancing approach maintains the energy of SM^1, SM^2 and SM^3 in the upper arm (E_u^{a1}, E_u^{a2}, E_u^{a2}) at their nominal value of 9 J as shown in Figure 2.20(a). The SM outer capacitors are regulated at 120 V and inner capacitors at 60 V as shown in Figure 2.20(b). Similarly, the lower arm SM capacitors voltage is regulated at their nominal value as shown in Figure 2.20(c). The

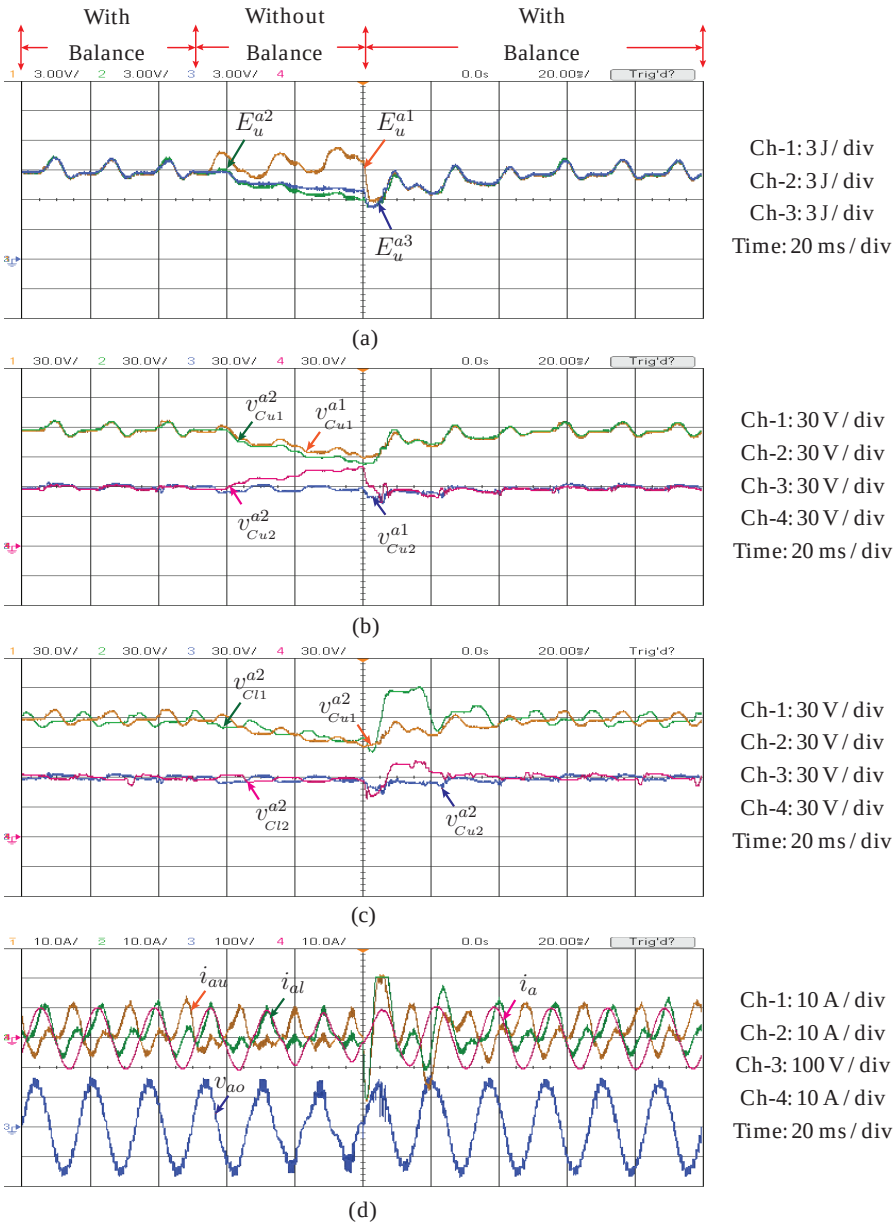


Figure 2.20. Experimental results with and without balancing approach: (a) upper arm submodules energy, (b) upper arm submodule capacitors voltage, (c) upper and lower arm submodule capacitors voltage, and (d) output voltage and current waveforms

converter generates a symmetrical sinusoidal output voltage (v_{ao}) waveform of 160 V peak with voltage steps of 25 V as shown in Figure 2.20(d). The output load current (i_a) is equal to the difference of upper and lower arm currents as shown in Figure 2.20(d).

From t=0.05 s to t=0.1 s, the balancing approach is disabled. The SM capacitor voltages and corresponding energies diverging from their nominal value. During this process, the converter generates highly distorted voltage and current waveforms across the load. The magnitude of arm current exceeds the rated current, which may damage the semiconductor devices as shown in Figure 2.20(d).

At t=0.1 s, the balancing approach is enabled, and the system returns to the normal operation. During the disabling of balance approach, the load performance is significantly deteriorated. Therefore, the balancing approach is required to achieve better converter and load performance. From the above results, it is observed that the proposed approach is effectively balancing the SMs energy even under external disturbance.

- **Performance at Low-Switching Frequency**

The voltage balancing at the low switching frequency is another major challenge in 3L-FC based MMC. At low switching frequency operation, either large size of submodule capacitors or higher number of submodules per arm is required to ensure the perfect balancing with smaller capacitor voltage ripple. In MMC-HVDC system, each arm is designed with 200-400 SMs and switched at a frequency of less than 200 Hz. Therefore, the power losses can be significantly minimized without affecting the output power quality. In this study, the performance of dual-stage approach with the average submodule switching frequency of 180 Hz as shown in Figure 2.21, where m_a is set to 0.9, f_o=60 Hz and load power factor 0.85 (lag). Figure 2.21(a) shows the stair case voltage waveform with a step of 30 V. The arm currents have a higher ripple, due to the low-switching frequency operation and a smaller number of submodules in each arm. Other hand, the dual-stage balancing

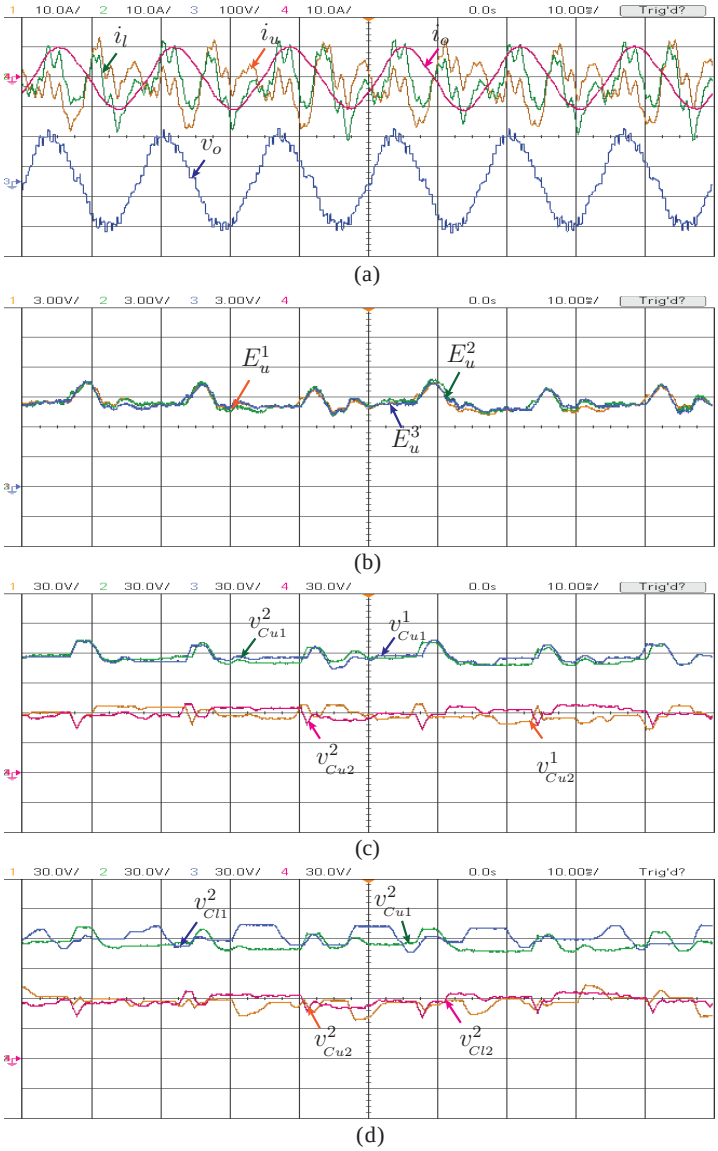


Figure 2.21. Experimental results at low-switching frequency: (a) output voltage and current waveforms, (b) upper arm submodules energy, (c) upper arm submodule capacitors voltage, and (d) upper and lower arm submodule capacitors voltage

approach effectively balancing the SMs energy and corresponding capacitors voltage at their nominal value as shown in Figure 2.21(b)-(c). The upper

and lower arm SMs outer and inner capacitors voltage are regulated at 120 V and 60 V, respectively as shown in Figure 2.21(d).

2.5 Comparison of Single and Dual-Stage Approaches

The performance comparison of single-stage and dual-stage balancing approach is presented in terms of switching frequency, voltage harmonic distortion and power losses under different load displacement factors and modulation indices.

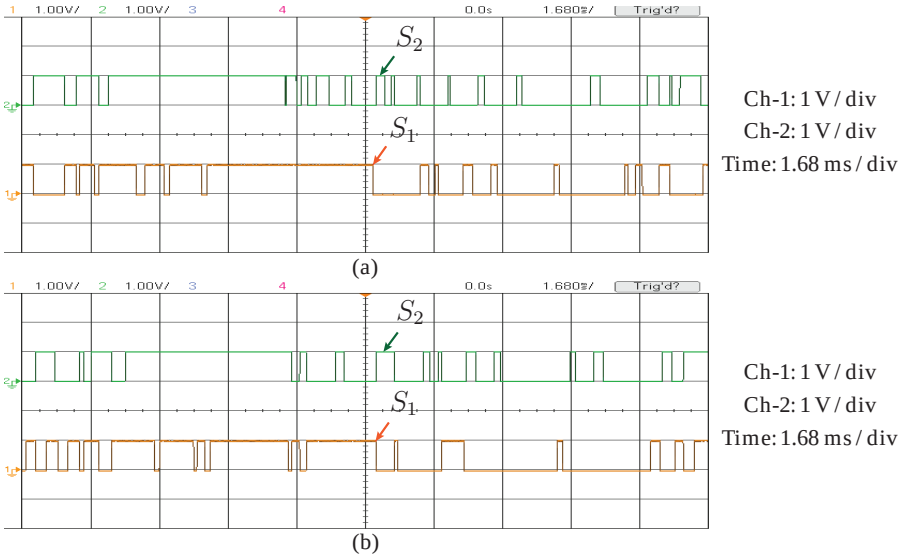


Figure 2.22. Submodule switching frequency: (a) dual-stage approach, and (b) single-stage approach

2.5.1 Switching Frequency

To analyze the switching frequency of dual-stage and single-stage balancing approaches, the gating pulse of devices S_1 and S_2 in SM^1 for one fundamental cycle is presented in Figure 2.22. In dual-stage balancing approach, the devices S_1 and S_2 are switched at 17 and 16 times in one fundamental cycle, which is equivalent to the frequency of 1020 Hz and 960 Hz, respectively

as shown in Figure 2.22(a). The average submodule switching frequency is 990 Hz. Similarly, the SM^1 gating signals with the single-stage balancing approach are shown in Figure 2.22(b). The switching frequency of devices S_1 and S_2 is around 900 Hz and 960 Hz, respectively. The average submodule switching frequency is 930 Hz. From the above results, it is observed that the dual-stage and single-stage approaches have similar operation value.

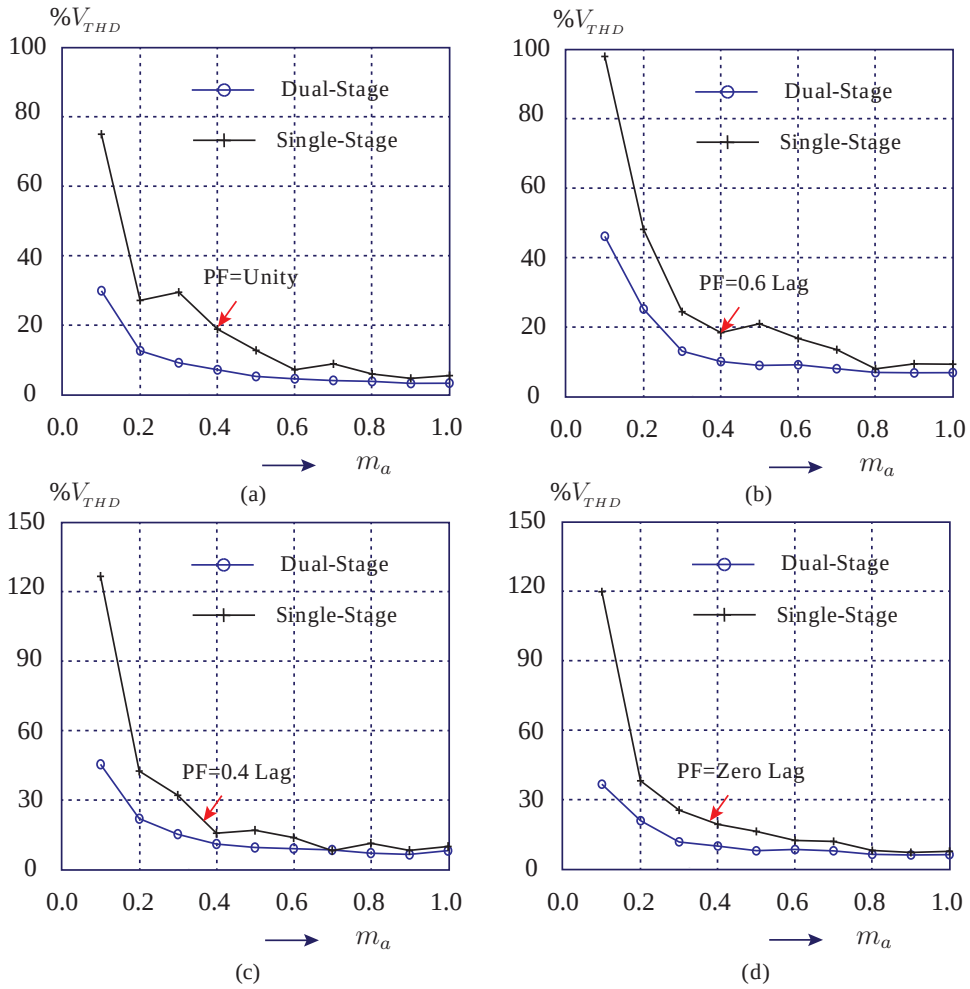


Figure 2.23. Experimental analysis of V_{THD} at different power factors: (a) unity, (b) 0.6 lagging, (c) 0.4 lagging, and (d) zero lagging

2.5.2 Total Harmonic Distortion

The performance comparison between dual and single-stage balancing methods at different power factors is shown in Figure 2.23. The results show that the dual-stage approach has lowest voltage harmonic distortion compared with the single-stage approach. When $m_a \geq$0.7, the voltage harmonic distortion obtained from the dual and single-stage methods are very close. At lower modulation indices, the single-stage method has very poor performance irrespective of the load power factor. The above results prove the superiority of the dual-stage balancing approach over the single-stage balancing approach.

2.5.3 Submodule Power Losses

The loss comparison between dual and single-stage balancing approach is shown in Figure 2.24. The results show that the submodules have low power losses with dual-stage balancing approach compared with that of the single-stage balancing approach. At lower modulation indices, the performance of dual and single-stage balancing approaches is very close.

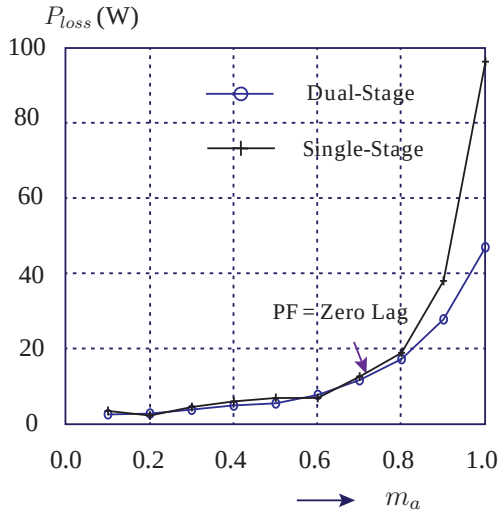


Figure 2.24. Submodule power losses at zero power factor (lag).

2.6 Start-Up Operation of 3L-FC based MMC

The three-level flying capacitor (3L-FC) submodule consists of two floating capacitors with unequal rated voltage capacity. These floating capacitors have zero initial voltage and must be charged to its nominal value during converter start-up process. However, the direct start-up process leads to a large inrush current due to the very low equivalent impedance of the converter. These inrush currents may damage the IGBT devices, capacitors and, effects the reliability and operation of MMC. From safety and reliability perspective, a systematic procedure is required for smooth pre-charging of submodule capacitors in MMC.

2.6.1 Principle of Start-up Operation

During submodule pre-charging process, the AC output voltage (v_{xo}) is set to zero. Therefore, the AC output current (i_x) and circulating current (i_{xz}) component becomes zero. The upper and lower arm current mainly consists of DC current component and is given as

$$\begin{aligned} i_{xu} &= i_s \\ i_{xl} &= i_s \end{aligned} \tag{2.6.1}$$

The DC current component is given by

$$i_s = \frac{i_{xu} + i_{xl}}{2} \tag{2.6.2}$$

Substitute $v_{xo} = 0$ and equation (2.6.2) in (2.2.1), which results in

$$0 = \frac{1}{2}[v_{xl} - v_{xu}] \tag{2.6.3}$$

From equation (2.2.1), the DC-side dynamics are given as

$$L\,\frac{di_s}{dt} + r\,i_s = \frac{1}{2}(V_{dc} - v_{xu} - v_{xl}) \tag{2.6.4}$$

The upper and lower arm reference voltage commands during start-up process are given as

$$\begin{aligned} v_{xu} &= \frac{V_{dc}}{2} - v_{dct} \\ v_{xl} &= \frac{V_{dc}}{2} - v_{dct} \end{aligned} \tag{2.6.5}$$

where $v_{dct} = L\,\frac{di_s}{dt} + r\,i_s$ is the voltage component corresponding to the current drawn from the DC-link. The magnitude of the DC-current component depends on the active power demanded by the load and, the difference between DC-link voltage and the sum of submodule capacitors voltage in each leg. The smooth pre-charging of submodule capacitors is achieved by controlling the DC-current component i_s.

The start-up process of 3L-FC based MMC system is divided into three stages. In each stage either outer (or) inner capacitor of 3L-FC submodule is charged by using passive (or) active current control technique. The three-stages of start-up operation are as follows:

- **Stage-I: Uncontrolled Charging Process of Submodule Outer Capacitor**

The equivalent circuit of stage-I start-up operation is shown in Figure 2.25(a). In this process, the pre-charging of submodule capacitors is achieved by using the main DC-link voltage (V_{dc}). When the DC-source (V_{dc}) is connected to the MMC terminals, the submodule outer capacitors are automatically charged in an uncontrolled manner. In this stage, the switching state ③ is applied to all the submodules in each leg. Thus, the submodule inner capacitors C_{u2} and C_{l2} in upper and lower arms are completely bypassed, and their voltages are maintained at zero value. The submodule outer capacitors C_{u1} and C_{l1} are charged through an antiparallel diode of the IGBT devices to a maximum voltage of

$$v_{_{Cu1}} = v_{_{Cl1}} = \frac{V_{dc}}{2N} \tag{2.6.6}$$

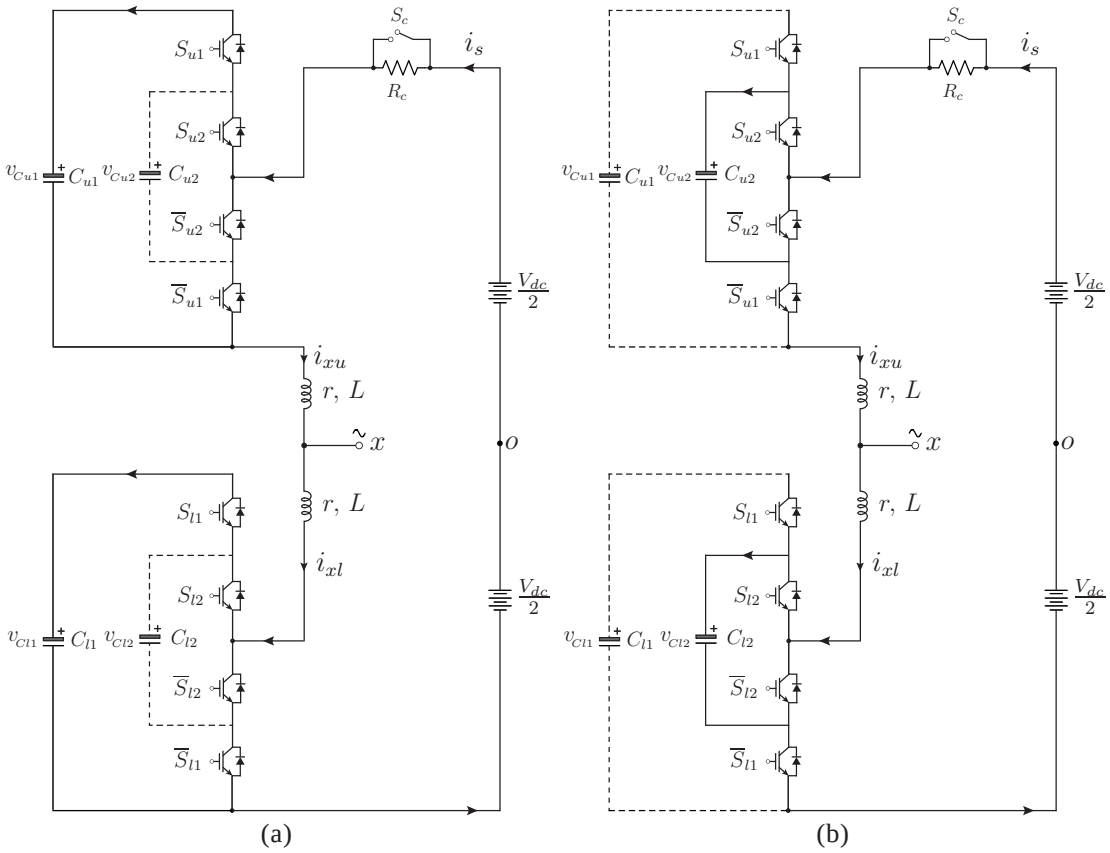


Figure 2.25. Start-up operation of 3L-FC based MMC: (a) stage-I and stage-III (b) stage-II

To limit the magnitude of charging current, an external pre-charging resistor (R_c) with a by-pass contactor (S_c) is connected in series with main DC-source. The magnitude of charging current is given by

$$i_s = \frac{V_{dc} - v_{Cu1} - v_{Cl1}}{R_c} \tag{2.6.7}$$

For normal operation of MMC, the outer capacitors (C_{u1} and C_{l1}) in upper and lower arms should be charged to a voltage of

$$v_{Cu1} = v_{Cl1} = \frac{V_{dc}}{N} \tag{2.6.8}$$

but, the uncontrolled charging process is only able to charge the submodule outer capacitors to 50% of its nominal voltage.

- **Stage-II: Uncontrolled Charging Process of Submodule Inner Capacitor**

The equivalent circuit of stage-II start-up operation is shown in Figure 2.25(b). In this process, the switching state ① is applied to all the submodules in each leg. Thus, the submodule inner capacitors are charged in an uncontrolled manner. During this process, the antiparallel diode of devices S_{u1} and S_{l1} is reverse biased, and there is no effect on the submodule outer capacitors voltage (C_{u1} and C_{l1}). The inner capacitors C_{u2} and C_{l2} are slowly charged through the antiparallel diode of S_{u2} and S_{l2} to a maximum voltage of

$$v_{Cu2} = v_{Cl2} = \frac{V_{dc}}{2N} \tag{2.6.9}$$

The magnitude of charging current is given as

$$i_s = \frac{V_{dc} - v_{Cu2} - v_{Cl2}}{R_c} \tag{2.6.10}$$

and it is controlled by using pre-charging resistor (R_c). For normal operation of MMC, the submodule inner capacitors should be charged to a value of

$$v_{Cu2} = v_{Cl2} = \frac{V_{dc}}{2N} \tag{2.6.11}$$

which is equal to the capacitors actual voltage given in equation (2.6.6) during uncontrolled charging process.

- **Stage-III: Controlled Charging Process of Submodule Outer Capacitor**

In flying capacitor submodules, the outer capacitor can not fully charge to its nominal value through the uncontrolled charging process. It further requires a control method to charge the outer capacitors to its nominal value. The equivalent circuit of stage-III operation is similar to the stage-I operation as shown in Figure 2.25(a). The pre-charging resistor (R_c) is bypassed by using the contactor (S_c). In this stage, the outer capacitors are slowly charged to its

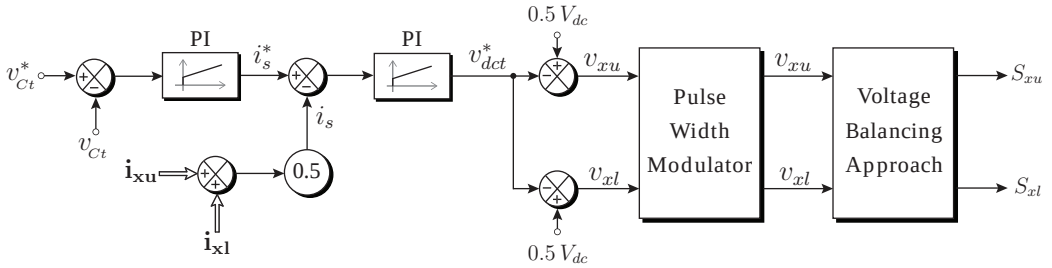


Figure 2.26. Start-up current controller

nominal value by controlling the magnitude of charging current using closed loop controller as shown in Figure 2.26. The closed-loop control system has an outer voltage and an inner current control loop. The voltage control loop regulates the average DC-voltage per leg and provides a reference charging current per leg (i^*_s). The reference charging current is given by

$$i^*_s = k_{pv}\,(v^*_{Ct} - v_{Ct}) + k_{iv}\int (v^*_{Ct} - v_{Ct})dt \tag{2.6.12}$$

where v^*_{Ct} represents the reference average DC-voltage per leg, v_{Ct} represents the actual average DC-voltage per leg and, k_{pv} and k_{iv} are the gains of voltage PI-controller. The reference charging current per leg (i^*_s) is compared with the actual charging current flowing through each leg (i_s). The current error is controlled by using current PI-controller, and its output is equal to the reference voltage command (v^*_{dct}). The reference voltage command is given by

$$v^*_{dct} = k_{pi}\,(i^*_s - i_s) + k_{ii}\int (i^*_s - i_s)dt \tag{2.6.13}$$

where i_s is the actual charging current flowing through each leg. The reference voltage command v^*_{dct} is added to the feed-forward DC-voltage component to obtain the upper and lower arm reference voltage commands. These voltage commands are used with a pulse width modulator and voltage balancing approach to achieve the equal charging of the submodule outer capacitors in each leg.

2.6.2 Experimental Validation

The start-up performance of 3L-FC based MMC is shown in Figure 2.27. Initially, all the submodule capacitors have zero voltage. From t=0 to 2 s, the switching state ③ is applied to all the submodules. The submodule outer capacitors are charged to a voltage of 175 V through the anti-parallel diodes of IGBT devices as shown in Figure 2.27(a). During stage-I, the inner capacitor of each submodule is completely bypassed, and their voltage is maintained at zero value. During this period, the charging current is controlled by using an external pre-charging resistor of R_c=100Ω. The magnitude of upper and lower arm current (i_{au} and i_{al}) is slowly decreased and eventually reaches to zero value when the sum of submodule outer capacitors voltage in each leg is equal to the voltage of main DC-link voltage as shown Figure 2.27(b). The magnitude of the output current is equal to the difference between upper and lower arm current, which is equal to zero. During start-up process, the reference output voltage component v^*_{xo} in arm modulating signals is set to zero. Therefore, the output voltage across the load is close to zero as shown in Figure 2.27(b).

At t= 2s (stage-II), the switching state ① is applied to all the submodules. In this stage, the outer capacitor is bypassed, and the inner capacitor is connected to the main DC-link through a pre-charging resistor and antiparallel diodes of IGBT devices. The charging current flowing through the inner capacitor becomes zero, when the inner capacitor of each submodule is charged to a voltage of 175 V as shown in Figure 2.27(a)-(b).

At t=4 s (stage-III), the pre-charging resistor is bypassed, and the closed-loop start-up controller is activated. In this stage, the closed-loop current controller is used along with the balancing approach to boost the outer capacitor voltage from 175 V to 350 V as shown in Figure 2.27(a). In this approach, the reference command is slowly varied at a rate of $0.0035V/sample$ (i.e. the outer capacitor voltage should reach to 350 V from 175 V within 2 sec period). During this period, the inner capacitor voltage has slightly reduced due to the delay in switching of IGBT devices and device loss, etc. Ideally,

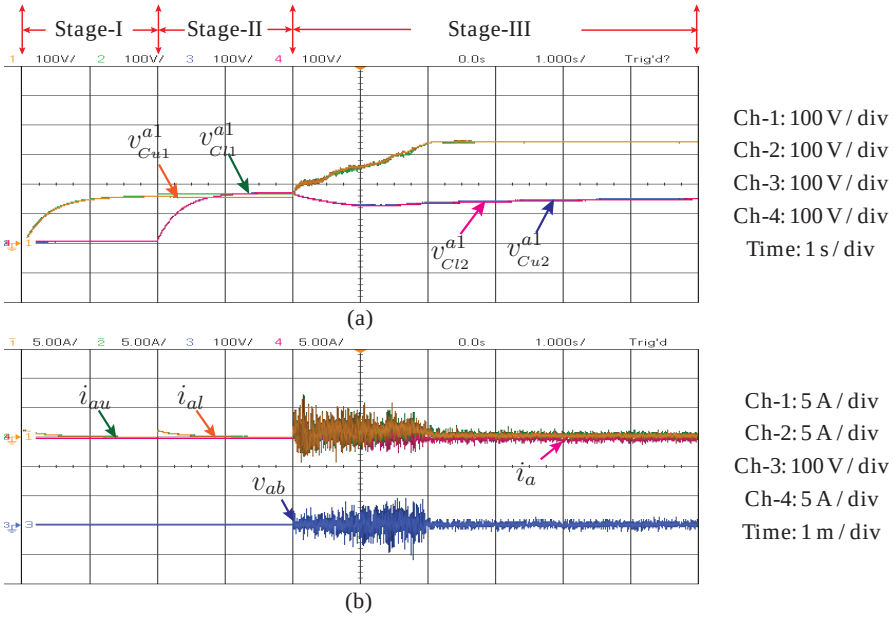


Figure 2.27. Experimental results for MMC start-up process: (a) upper and lower arm submodule capacitors voltage, and (b) output voltage and current waveforms

the output voltage and an output current flowing through the load should be zero. However, it consists of switching ripple corresponding to the voltage component v_{dct}^{*} as shown in Figure 2.27(b). The magnitude of switching ripples vary with the number of submodules in each arm.

2.7 Summary

In this chapter, a novel single-stage balancing approach along with a simple pulse width modulator is proposed for half-bridge and three-level flying capacitor submodule based MMC. The performance of HB-MMC is compared with 3L-FC MMC under identical operating conditions and system parameters. The 3L-FC MMC has smaller circulating current component and capacitors voltage ripple compared with HB-MMC system. The performance of flying capacitor submodule is analyzed under different submodule outer and

inner capacitors size. The size of inner capacitor has least significant effect on the converter performance compared with the outer capacitor size. Also, the dynamic and steady-state performance of balancing approach is presented with PSC-PWM and LSC-PWM schemes. The LSC-PWM scheme generates arm current with less switching ripple compared to PSC-PWM. Finally, the balancing approach is extended to control the half-bridge submodule based MMC and their performance is experimentally validated.

To improve the performance and reduce the computational complexity, a dual-stage balancing approach is proposed for flying capacitor submodule based MMC. The principle of operation and design procedure of dual-stage balancing approach is presented. The dynamic and steady-state performance of dual-stage approach is presented under high and low-switching frequency operating conditions. The performance comparison of single-stage and dual-stage balancing approaches are presented in terms of switching frequency, voltage harmonic distortion and submodule power losses under different operating conditions. The results show that the dual-stage approach has superior performance over the single-stage approach. Finally, the start-up process of flying capacitor submodule based MMC is presented. The simulation and experimental results are in a close relationship and thus validate the proposed methodology.

CHAPTER 3

PULSE WIDTH MODULATION SCHEMES WITH IMPROVED HARMONIC PERFORMANCE

THE carrier modulation schemes require significant modifications if there is any change in the system configuration or a number of submodules in each arm. These modulation schemes require either high sampling frequency or a large number of submodules to generate high-quality output voltage and current waveforms. In addition, a common-mode voltage (CMV) signal is added to the modulation signals to minimize the internal unbalance between upper and lower arm submodule capacitors voltage.

In this chapter, two novel modulation schemes named as sampling average modulation (SAM) and space vector modulation (SVM) schemes are proposed. The sampled average modulation approach independently modulates each leg of MMC. This approach can be directly applied to an MMC with any number of submodules without any modifications. The three-phase equivalent of sampled average modulation results in (i) the elimination of average zero sequence voltage in each sampling interval, (ii) reduces the ripple in output current, and (iii) minimizes the harmonic distortion in output voltage and current. In addition, a simple balancing approach is proposed to achieve the voltage balancing among submodules. The experimental studies are presented to validate the performance of sampled average modulation

and voltage balancing approach.

The second approach is dual space vector modulation (SVM) scheme, which has more freedom to select the switching vectors with different magnitudes of common-mode voltage (third-harmonic voltage component). In this approach, the upper and lower three-phase arms are independently controlled using space vector philosophy. The proposed approach is implemented in abc-coordinate system, which reduces the computational complexity and, easy to obtain the switching vectors and corresponding dwell times. Also, a balancing approach with reduced current sensors is proposed. The experimental studies are presented to validate the performance of proposed approach. The performance comparison of balancing approach with and without a reduction in current sensors is also presented.

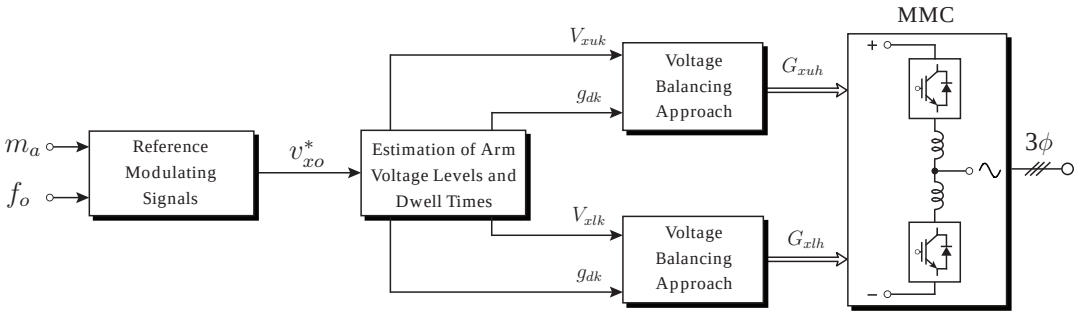


Figure 3.1. Control block diagram of MMC with sampled average modulation

3.1 Sampled Average Modulation

The control block diagram of MMC with sampled average modulation scheme is shown in Figure 3.1. The reference modulating signals (v^*_{xo}) are generated with required modulation index (m_a) and frequency (f_o). These modulating signals are given to the sampled average modulator, in which the two nearest phase voltage levels and corresponding duty cycles are calculated. From phase voltage levels, the upper and lower arm voltage levels are estimated. The voltage balancing approach generates gating signal to the

submodules based on the voltage levels, the direction of arm current and submodule capacitors voltage. The implementation of sampled average modulation and submodule capacitors voltage balancing approach is discussed in the following subsections.

3.1.1 Implementation of Sampled Average Modulation

The sampled average modulation scheme directly controls the phase voltage of the MMC allows to generate the line-to-line voltage implicitly. This approach is computationally less complex and easy to apply for MMC with any number of submodules without any modifications. In this method, the reference phase voltage is generated by averaging the two nearest voltage levels in each sampling interval. This approach eliminates the volt-sec error in the staircase or nearest voltage level modulation. The volt-sec balance of reference phase voltage expressed in terms of two nearest voltage levels and corresponding dwell times as,

$$\begin{aligned} v^{n}_{rxo}\, T_s &= V_{x1}\, T_{x1} + V_{x2}\, T_{x2} \\ T_s &= T_{x1} + T_{x2}. \end{aligned} \tag{3.1.1}$$

where v^{n}_{rxo} represents the normalized reference phase voltage, V_{x1} and V_{x2} represents the nearest phase voltage levels, and T_{x1} and T_{x2} represents the dwell times of phase voltage levels, respectively, and T_s represents the sampling time, which is equal to the summation of dwell times T_{x1} and T_{x2}. The implementation of sampled average modulation scheme involves three major steps as follows:

- **Step-I: Identification of Two Nearest Voltage Levels**

The total DC-link voltage of each arm is expressed in terms of number of SMs and rated SM capacitor voltage as,

$$V_{dc} = R \times V_C \tag{3.1.2}$$

where $R = N$ for HB submodule and $R = 2N$ for 3L-FC submodule. The two nearest phase voltage levels are obtained from the normalized reference phase voltage in each sampling interval. The reference phase voltage is given in terms of number of submodules and its capacitor voltage as,

$$v_{xo} = \frac{R\,V_C}{2} \times m_a \sin(\omega_o t + \phi) \tag{3.1.3}$$

The normalized reference phase voltage is obtained by dividing the equation (3.1.3) with submodule rated capacitor voltage as,

$$v_{xo}^n = \frac{R}{2} \times m_a \sin(\omega_o t + \phi) \tag{3.1.4}$$

The sampled average modulation requires nearest voltage levels, which are positive integers only. Therefore, an offset value of $\frac{R}{2}$ is added to the equation (3.1.4) and results in

$$v_{rxo}^n = \frac{R}{2} \times [1 + m_a \sin(\omega_o t + \phi)] \tag{3.1.5}$$

where v_{xo}^n represents the normalized reference phase voltage, v_{rxo}^n represen-ts the normalized reference phase voltage with offset, m_a represents the amplitude modulation index of range 0 to 1, and ω_o is the fundamental angular frequency in rad/sec. The phase voltage levels are obtained from the equation (3.1.5), where the lower voltage level (V_{x1}) is obtained from the operator $floor(v_{rxo}^n)$ and the upper voltage level (V_{x2}) is equal to $1 + V_{x1}$.

$$\begin{aligned} V_{x1} &= floor\,(v_{rxo}^n) \\ V_{x2} &= 1 + V_{x1}. \end{aligned} \tag{3.1.6}$$

- **Step-II: Calculation of Dwell Times**

The voltage levels V_{x1} and V_{x2} are applied for a time duration of T_{x1} and T_{x2}, respectively over a sampling interval T_s. From the volt-sec balance principle given in equation (3.1.1), the dwell times T_{x1} and T_{x2} are given by

$$\begin{aligned} T_{x2} &= \frac{v_{rxo}^n - V_{x1}}{V_{x2} - V_{x1}} \times T_s \\ T_{x1} &= T_s - T_{x2} \end{aligned} \tag{3.1.7}$$

These dwell times are compared with a symmetrical triangular waveform to generate the pulses g_{d1} and g_{d2} as shown in Figure 3.2. The pulse g_{d1} is applied to the submodules in upper and lower arms of the corresponding phase to generate the phase voltage level V_{x1}. Similarly, the voltage level V_{x2} is obtained by modulating the submodules in upper and lower arms for a pulse duration of g_{d2}.

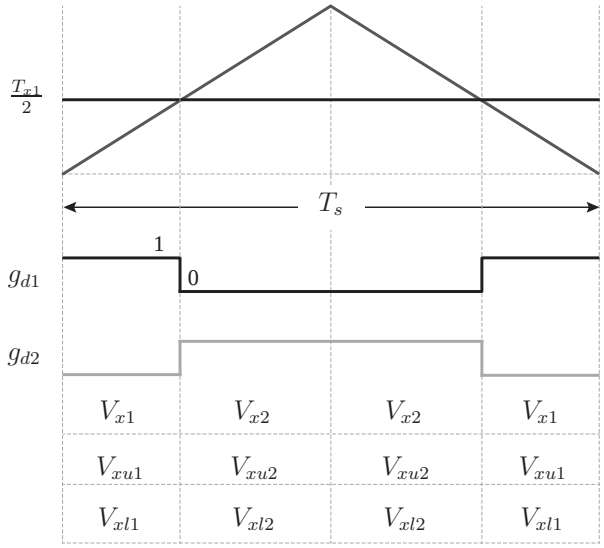


Figure 3.2. Dwell times of voltage levels

- **Step-III: Calculation of Arm Voltage Levels**

The phase voltage levels V_{x1} and V_{x2} are generated by using the submodules from the upper and lower arms together. In each sampling interval, the upper and lower arms are controlled such that R-number of submodule capacitors out of $2R$ submodule capacitors from each leg are used to generate the required phase voltage level (i.e., the number of on-state submodule capacitors is maintained constant and equal to R in each sampling interval).

According to this criteria, the upper and lower arm voltage levels are given by

$$\begin{aligned} V_{xuk} + V_{xlk} &= R \\ V_{xlk} &= V_{xk} \\ V_{xuk} &= R - V_{xlk} \end{aligned} \tag{3.1.8}$$

where $k \in \{1, 2\}$ represents the voltage levels, V_{xuk} and V_{xlk} represents the upper and lower arm voltage levels.

3.1.2 Capacitors Voltage Balancing Approach

The sampled average modulation scheme has an ability to maintain the voltage balancing between arms. However, the additional balancing approach is required to achieve the voltage balancing among submodules. The basic principle of voltage balancing approach is to control the charging and discharging of submodule capacitors, depending on the direction of the current and the instantaneous value of the capacitor voltage [49, 51, 61, 71, 73, 75, 76, 93, 156]. The implementation of proposed approach involves various stages as shown in Figure 3.3(a). The design steps of voltage balancing approach are as follows:

- **Stage-I: Selection of Submodule Capacitors Voltage**

The comparison logic is shown in Figure 3.3(b), which is utilized for the selection of submodule capacitors voltage. It requires normalized submodule capacitor voltage as input. Particularly, the 3L-FC submodule has two floating capacitors with different rated voltages, which are normalized to their rated value and applied to the comparison logic. The normalized outer and inner capacitors voltage of 3L-FC submodule is

$$\begin{aligned} v_{Cy1}^{xkn} &= \frac{v_{Cy1}^{xk}}{V_{C1}} \\ v_{Cy2}^{xkn} &= \frac{v_{Cy2}^{xk}}{V_{C2}} \end{aligned} \tag{3.1.9}$$

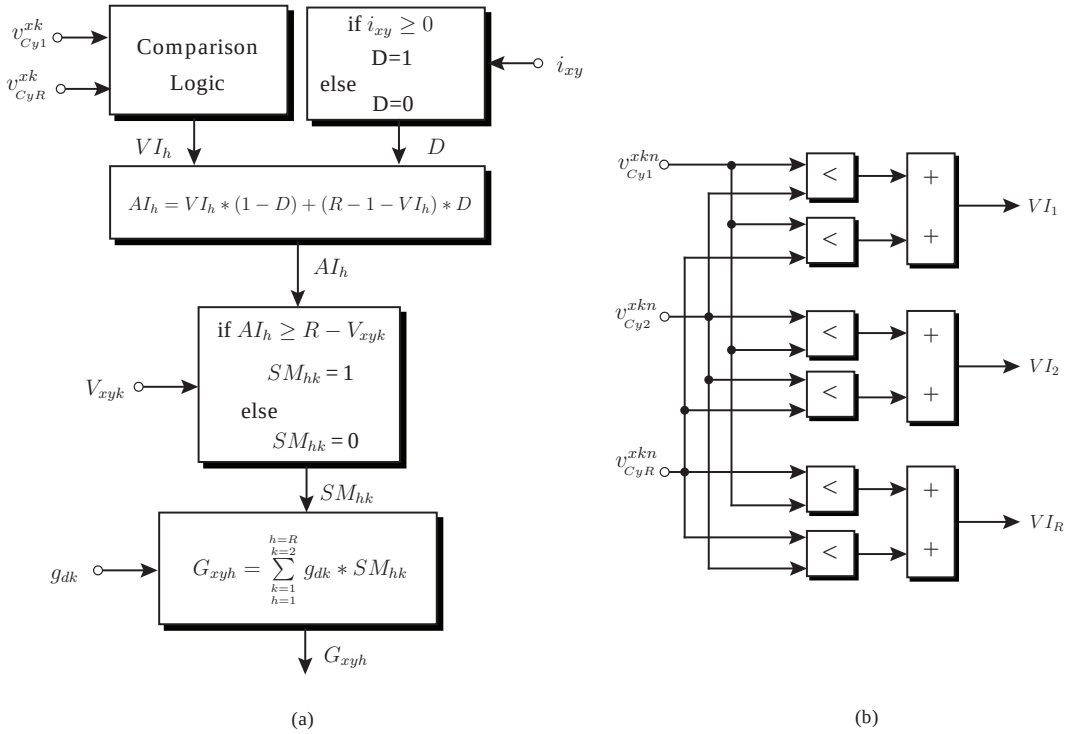


Figure 3.3. Voltage balancing approach: (a) design steps of balancing approach, (b) comparison logic

Each normalized capacitor voltage is compared with other capacitors voltage as shown in Figure 3.3(b). The output of each comparator is added together and the resultant output becomes a virtual index number of the capacitor voltage (VI_h). The range of virtual index number is $VI_h \in \{0, 1.....R-1\}$ and $h \in \{1, 2.....R-1, R\}$. The actual index number of the capacitor voltage is obtained based on the direction of the arm current and the virtual index number. Equation (3.1.10) gives the actual index number of each capacitor voltage (AI_h),

$$AI_h = VI_h * (1-D) + (R-1-VI_h) * D \tag{3.1.10}$$

where D represents the direction of the arm current and is given as

$$D = \begin{cases} 1 & i_{xy} \geq 0 \\ 0 & i_{xy} < 0 \end{cases} \tag{3.1.11}$$

where i_{xy} represents the arm current, $x \in \{a, b, c\}$ represents the leg and $y \in \{u, l\}$ represents the arm.

- **Stage-II: Generation of Submodule IGBT Status**

Stage-II requires the two nearest voltage levels of either upper and lower arm (V_{xyk}), where k represents the voltage levels $k \in \{1, 2\}$. These voltage levels are compared with the actual index number (AI_h) to generate the IGBT status (SM_{hk}) of the corresponding capacitor voltage. If $SM_{hk} = 1$, then the IGBT device corresponding to that particular capacitor voltage should be turned-on; otherwise, it should be turned off for a duration of either d_1 or d_2.

- **Stage-III: Generation of Gating Pattern**

After the determination of IGBT status SM_{hk}, the final step is to generate the gating pattern for the IGBT devices of each 3L-FC submodule. The generalized equation for the gating pattern of IGBT device is given as

$$G_{xyh} = \sum_{\substack{k=1 \\ h=1}}^{\substack{h=R \\ k=2}} g_{dk} * SM_{hk} \tag{3.1.12}$$

Equation (3.1.12) is expanded for single IGBT device of G_{xy1} as,

$$G_{xy1} = g_{d1} * SM_{11} + g_{d2} * SM_{12} \tag{3.1.13}$$

3.1.3 Three-phase Equivalent Approach

The per-phase philosophy of sampled average modulation scheme is extended to a three-phase MMC system, which results in (i) elimination of average-zero sequence voltage in each sampling interval, (ii) minimization of ripple in output current. These features are similar to the conventional decoupled sampled average zero sequence voltage elimination scheme (DSAZE-PWM) [157, 158]. Therefore, the three-phase approach is also referred as DSAZE-PWM.

The three-phase normalized reference output voltages are defined as follows:

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \frac{R}{2} \begin{bmatrix} 1 + m_a\, sin(\omega_o\, t) \\ 1 + m_a\, sin(\omega_o\, t - \frac{2\pi}{3}) \\ 1 + m_a\, sin(\omega_o\, t - \frac{4\pi}{3}) \end{bmatrix} \tag{3.1.14}$$

The nearest output phase voltage levels are given as

$$\begin{aligned} V_{a1} &= floor(v_a(t)),\ V_{a2} = 1 + V_{a1} \\ V_{b1} &= floor(v_b(t)),\ V_{b2} = 1 + V_{b1} \\ V_{c1} &= floor(v_c(t)),\ V_{c2} = 1 + V_{c1} \end{aligned} \tag{3.1.15}$$

The duty cycle corresponding to each voltage level is given as:

$$\begin{aligned} d_{a1} &= 1 - d_{a2},\ d_{a2} = v_a(t) - V_{a1} \\ d_{b1} &= 1 - d_{b2},\ d_{b2} = v_b(t) - V_{b1} \\ d_{c1} &= 1 - d_{c2},\ d_{c2} = v_c(t) - V_{c1} \end{aligned} \tag{3.1.16}$$

These duty cycles are converted into time durations and corresponding gating pulses as shown in Figure 3.2. The upper and lower arm voltage levels are obtained from equations (3.1.14) and (3.1.15). These voltage levels are generated by using upper and lower arm submodules. In this study, the upper and lower arm submodules are equally modulated in each sampling interval. This approach is also known as equal-duty DSAZE-PWM approach [157, 158]. The voltage levels and duty cycles are applied to a voltage balancing approach shown in Figure 3.3(a). The voltage balancing approach generates the final gating pattern to meet the required control objective. In DSAZE-PWM scheme, the average-zero sequence voltage in a sampling interval becomes zero. The zero sequence voltage is given as

$$v_{cm} = \frac{1}{3}[v_{ao} + v_{bo} + v_{co}] \tag{3.1.17}$$

Equation (3.1.17) is expressed in terms of upper and lower arm voltages [38]:

$$v_{cm} = \frac{1}{6}\ [(v_{al} + v_{bl} + v_{cl}) - (v_{au} + v_{bu} + v_{cu})] \tag{3.1.18}$$

The proposed DSAZE-PWM scheme is analyzed with a simple example given in Table 3.1.

Table 3.1. Example with N=3, R=6, m_a=0.8 and f_o=60 Hz

Phase	at t=4.1667 ms	(V_1, V_2)	(V_{u1}, V_{l1})	(V_{u2}, V_{l2})	(d_1, d_2)
$v_a(t)$	5.4	(5,6)	(1,5)	(0,6)	(0.6,0.4)
$v_b(t)$	1.8	(1,2)	(5,1)	(4,2)	(0.2,0.8)
$v_c(t)$	1.8	(1,2)	(5,1)	(4,2)	(0.2,0.8)

The average-zero sequence voltage for one sampling interval is given as

$$\begin{aligned} v_{cm(average)} &= \frac{1}{6}\left[(5\times 0.6 + 6\times 0.4 + 1\times 0.2 + 2\times 0.8\right. \\ &\quad + 1\times 0.2 + 2\times 0.8) - (1\times 0.6 + 0\times 0.4 \\ &\quad \left. + 5\times 0.2 + 4\times 0.8 + 5\times 0.2 + 4\times 0.8)\right] \\ &= \frac{1}{6}[(5.4 + 1.8 + 1.8) - (0.6 + 4.2 + 4.2)] \\ v_{cm(average)} &= 0 \end{aligned} \tag{3.1.19}$$

Equation (3.1.19) shows the average value of zero sequence voltage becomes zero in each sampling interval. In other words, the dynamic balancing of the zero sequence voltage is achieved, which results in the dynamic balancing of zero sequence current.

The equivalence between the proposed and conventional space vector modulation (SVM) approach is shown in Figure 3.4. In the multilevel-SVM approach, the reference space vector is decomposed into an offset and two-level space vector. From the offset vector, the origin of the two-level space vector diagram formed by the eight possible switching vectors (V_{a1}, V_{b1}, V_{c1}), (V_{a2}, V_{b1}, V_{c1}), (V_{a1}, V_{b2}, V_{c1}), (V_{a1}, V_{b1}, V_{c2}), (V_{a2}, V_{b2}, V_{c1}), (V_{a1}, V_{b2}, V_{c2}), (V_{a2}, V_{b1}, V_{c2}), and (V_{a2}, V_{b2}, V_{c2}) are located [159–162]. From the position of the two-level

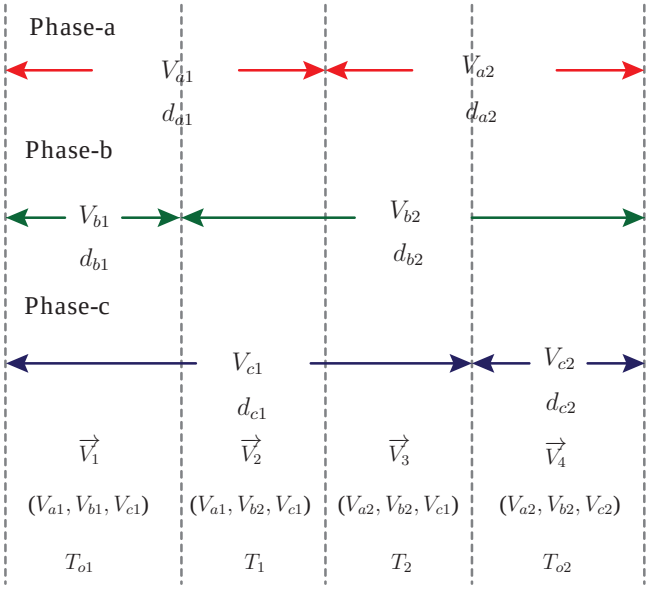


Figure 3.4. Three-phase equivalent switching sequence

space vector, the nearest four vectors are selected to realize the reference space vector. The four vectors (on sequence) $\vec{V_1}$-$\vec{V_2}$-$\vec{V_3}$-$\vec{V_4}$ are applied for time durations of T_{o1}-T_1-T_2-T_{o2}, respectively. The time durations T_{o1} and T_{o2} are equally distributed in the conventional SVM approach. In the proposed approach, the three-phase voltage levels together represent the nearest four vectors, similar to the switching sequence of the conventional SVM approach as shown in Figure 3.4. However, the proposed approach does not require the sector identification procedure, which is one of the major differences between the proposed and conventional SVM approach. In addition, the time durations T_{o1} and T_{o2} are not equally distributed in the proposed approach. The T_{o1} and T_{o2} are proportionally varied with the instantaneous value of three-phase modulating signals.

3.2 Dynamic Performance of Sampled Average Modulation

The performance of proposed modulation scheme and voltage balancing approach is validated on a per-phase MMC system by using MATLAB software.

In per-phase MMC system, the load is connected between the midpoint of DC-link and the AC output terminal. Each arm of MMC has a single buffer inductor and three 3L-FC submodules. Each 3L-FC submodule has two floating capacitors with a rated voltage of V_{C1} = 120 V and V_{C2} = 60 V. The sampling frequency of proposed modulation scheme is 1080 Hz, and the average device switching frequency is equal to 180 Hz.

3.2.1 Dynamic Performance

The performance of proposed modulation scheme and balancing approach is validated with the step change in load. The simulation results with a step change in load is shown in Figure 3.5. The converter is operating at a modulation index of m_a = 0.9, frequency of f_o = 60 Hz, and a half-load condition. The upper arm submodule outer and inner capacitors voltage is perfectly maintained at 120 V and 60 V, respectively as shown in Figure 3.5(a). The lower arm submodule outer and inner capacitors voltage are also maintained at the same value of upper arm submodule capacitors voltage. The charging and discharging of upper and lower arm capacitors voltage is in-phase opposition as shown in Figure 3.5(b). The output voltage has seven levels with a step of 53.33 V as shown in Figure 3.5(c). The voltage levels are perfectly clamped and there is no intermediate switchings in the output voltage. The load current has a peak value of 5 A and is equally distributed between upper and lower arms as shown in Figure 3.5(d).

At t = 0.1 s, the load is suddenly (step) changed from half-load to full-load condition. The modulation index and frequency are kept constant at 0.9 and 60 Hz, respectively. The magnitude of the load current is increased with the load. However, the balancing approach perfectly maintaining the submodule capacitors voltage from the upper and lower arms at their nominal values. But, the ripple in submodule capacitors voltage is increased with the load current. At full-load condition, the output voltage has a similar number of voltage levels as that of the half-load condition.

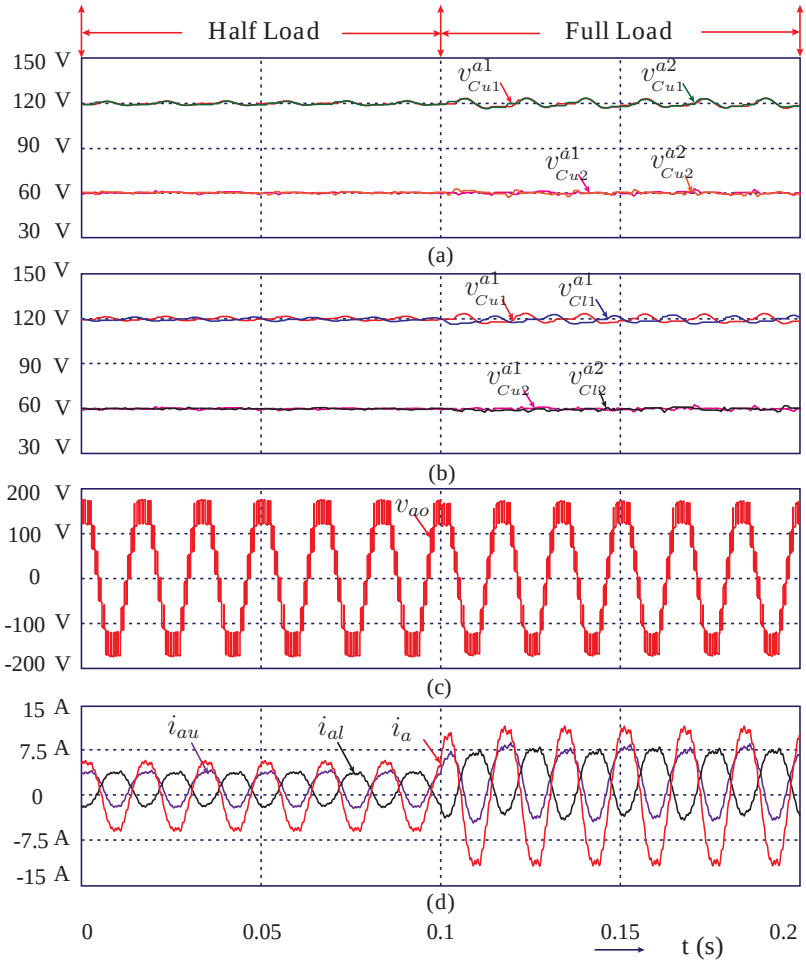


Figure 3.5. Dynamic performance with step change in load: (a) upper arm SM^1 and SM^2 outer and inner capacitors voltage, (b) upper and lower arm SM^1 outer and inner capacitors voltage, (c) output voltage, and (d) upper, lower arm, and load current waveforms.

3.2.2 Total Harmonic Distortion

The harmonic spectrum of the output voltage with PSC-PWM and proposed modulation schemes are shown in Figure 3.6(a) and Figure 3.6(b), respectively. With proposed approach, the output voltage harmonic distortion is 38.84%, which is smaller than the harmonic distortion of 66.34% produced

by the conventional PSC-PWM scheme. In addition, the percentage of harmonics around the switching frequency is 75% smaller than the PSC-PWM method. Hence, the ripple in output current is significantly minimized and requires smaller output filter, which is low cost. Overall, there is a 50% reduction in the voltage harmonic distortions with the proposed modulation scheme as compared to the conventional PSC-PWM method.

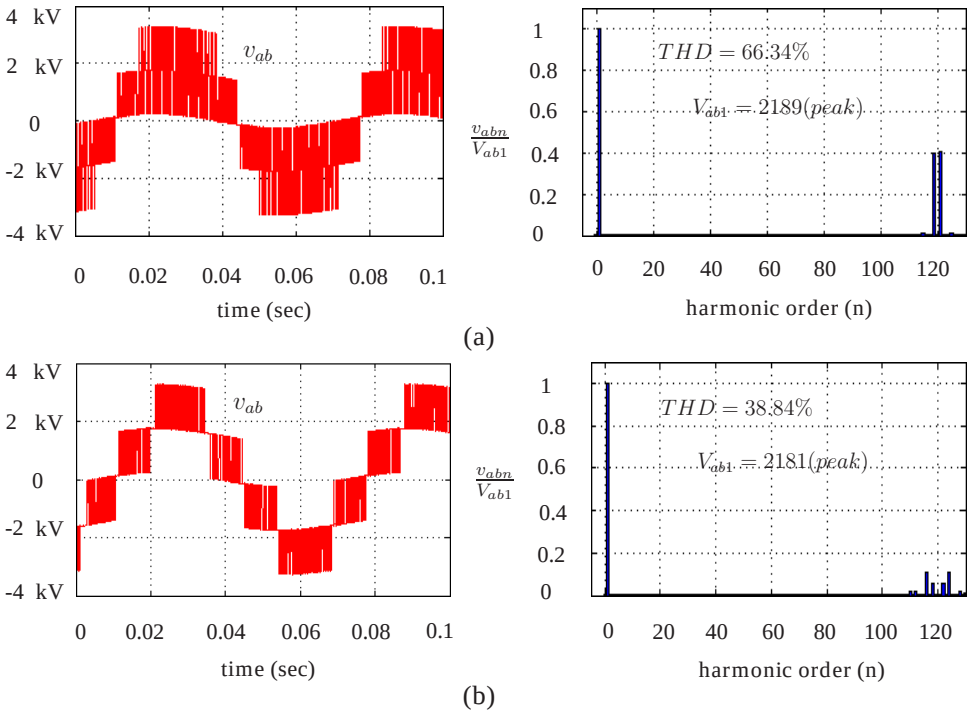


Figure 3.6. Harmonic spectrum of output voltage: (a) PSC-PWM scheme (b) SAM scheme at m_a=0.25 and f_o=15 Hz

3.3 Experimental Validation

The effectiveness of the proposed methodology is validated on a low-power MMC laboratory prototype with 3L-FC submodule. The total DC-link voltage of 360 V is equally distributed between the submodules in each arm. Each arm consists of three 3L-FC submodules with a rated capacitor voltage of V_{C1}=120 V, and V_{C2}=60 V. The sampling frequency set to 1080 Hz.

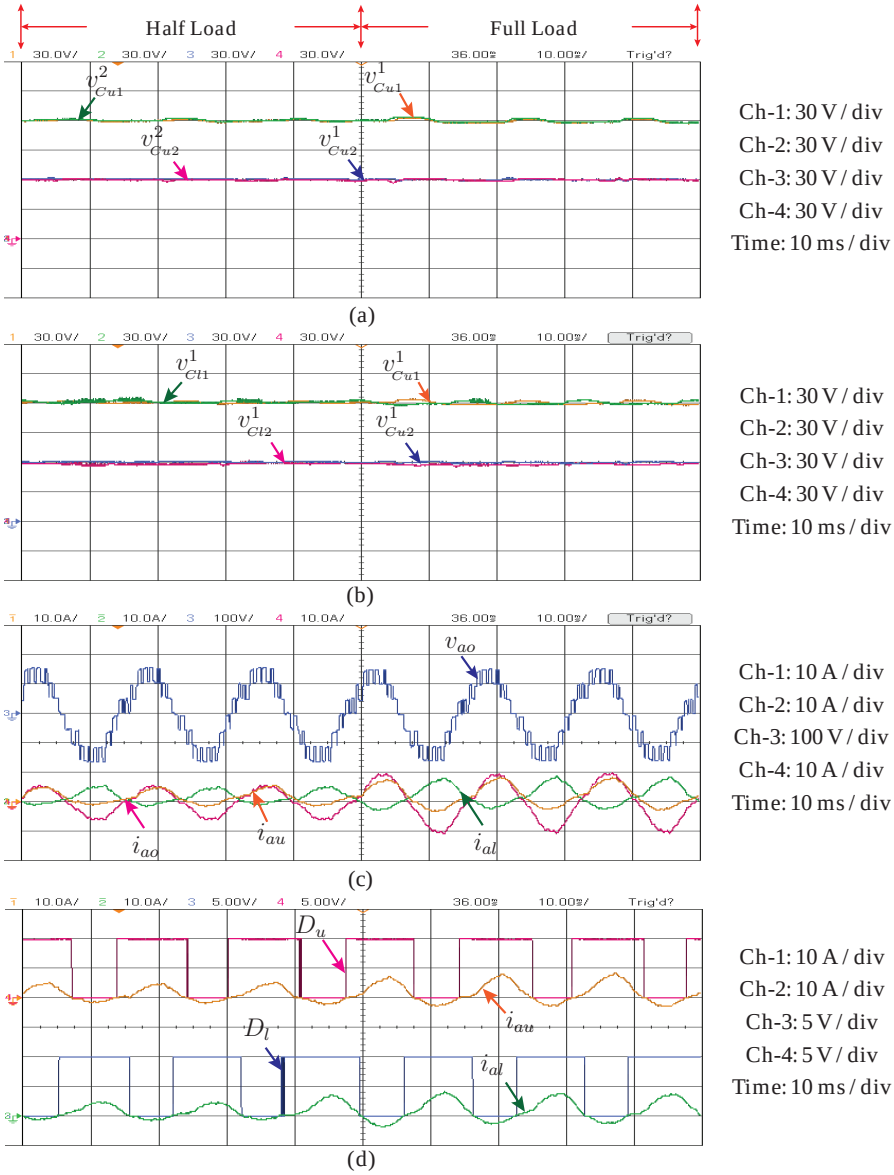


Figure 3.7. Experimental results with step change in load: (a) upper arm submodule capacitors voltage, (b) upper and lower arm submodule capacitors voltage, (c) output voltage and current waveforms, and (d) arm currents and its direction

3.3.1 Dynamic Performance

The transient performance of proposed modulation scheme and voltage balancing approach with a step change in the load is shown in Figure 3.7. Ini-

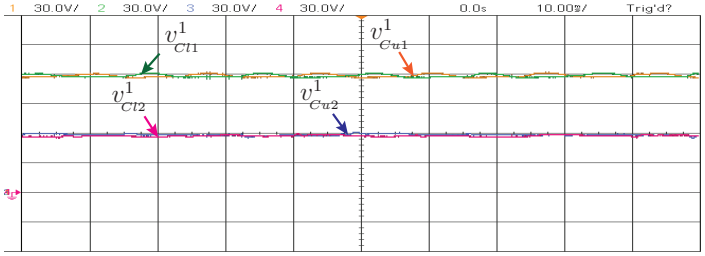
tially, the converter is operating at a modulation index of 0.9, frequency of 60 Hz, and half-load condition. The submodule outer and inner capacitors voltage of upper and lower arm is shown in Figure 3.7(a)-(b). The outer and inner capacitors voltage is maintained at 120 V and 60 V, respectively. The converter output has seven level voltage waveform as shown in Figure 3.7(c).

After some time, the load is suddenly changed from half-load to full-load condition (i.e., the value of load resistance is decreased). The magnitude of the fundamental output voltage is maintained constant. According to Ohm's law, the variation in the magnitude of the load current is inversely proportional to the value of the load resistance. The upper and lower arm current and its direction (D_u and D_l) is shown in Figure 3.7(d). According to the proposed voltage balancing approach, D=1 (analog equivalent of 10 V) for the positive direction and D=0 (analog equivalent of 0 V) for the negative direction of the arm current. The variable D is sent to the D / A converter and captured by using DSO-2024A oscilloscope.

3.3.2 Performance With Different Size of Arm Inductor

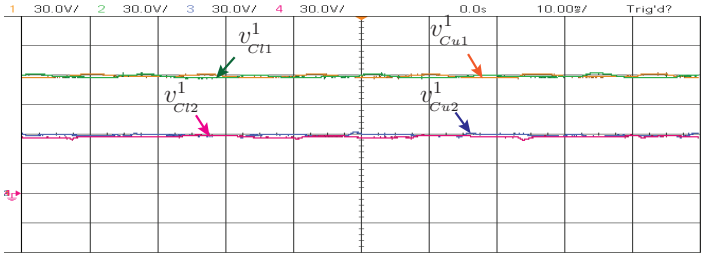
The performance of proposed methodology is investigated with a different size of buffer inductor. Typically, the size of the buffer inductor is selected based on the arm current ripple, short circuit current capability, circulating current limit, and submodule capacitance [29, 104]. The buffer inductor also helps to minimize the magnitude of switching frequency circulating current components. The smaller buffer inductor with high switching frequency (or) slightly larger size with lower switching frequency is preferred [68, 163].

The experimental results with a buffer inductor size of L=5 mH and L=1 mH are shown in Figure 3.8 and Figure 3.9. The outer and inner capacitors voltage is perfectly regulated at 120 V and 60 V irrespective of the buffer inductor size as shown in Figure 3.8 and there is no impact on the output voltage and current as shown in Figure 3.9. However, the upper and lower arm current waveforms have higher distortion with the reduction in buffer inductor size as shown in Figure 3.9. The peak value of the arm current also



Ch-1: 30 V / div
Ch-2: 30 V / div
Ch-3: 30 V / div
Ch-4: 30 V / div
Time: 10 ms / div

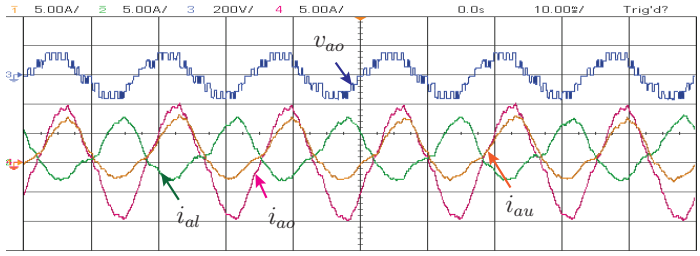
(a)



Ch-1: 30 V / div
Ch-2: 30 V / div
Ch-3: 30 V / div
Ch-4: 30 V / div
Time: 10 ms / div

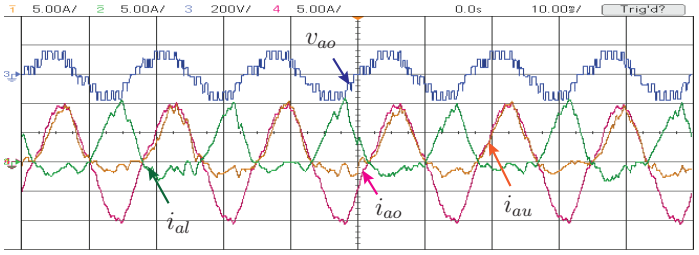
(b)

Figure 3.8. Experimental results with different size of buffer inductors: (a) L=5 mH and (b) L=1 mH [Scope: upper and lower arm submodule capacitors voltage]



Ch-1: 5 A / div
Ch-2: 5 A / div
Ch-3: 200 V / div
Ch-4: 5 A / div
Time: 10 ms / div

(a)



Ch-1: 5 A / div
Ch-2: 5 A / div
Ch-3: 200 V / div
Ch-4: 5 A / div
Time: 10 ms / div

(b)

Figure 3.9. Experimental results with different size of buffer inductors: (a) L=5 mH and (b) L=1 mH [Scope: output voltage and current waveforms]

increased due to the increment in the magnitude of circulating current, and the device power loss is affected.

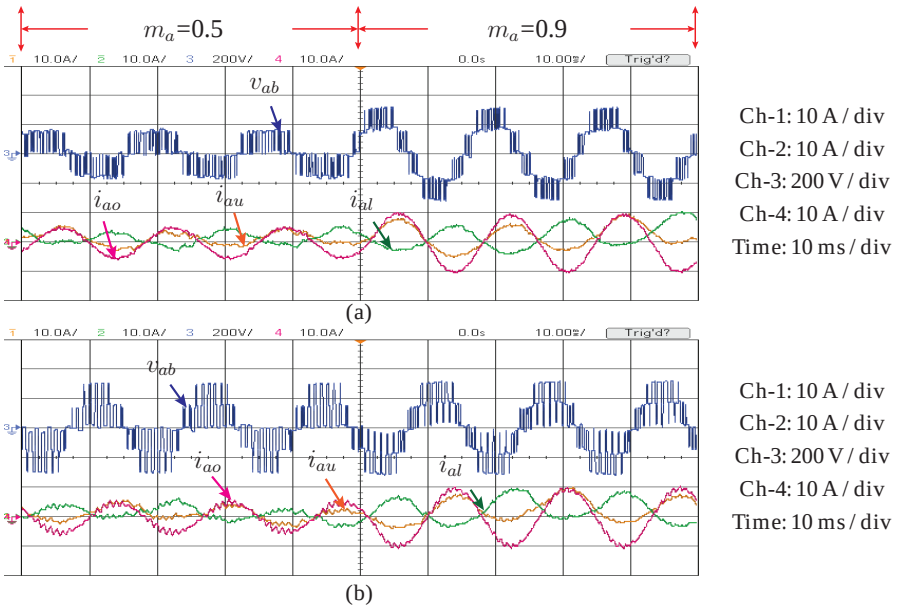


Figure 3.10. Experimental results for dynamic performance: (a) SAM scheme (b) PSC-PWM scheme [Scope: output voltage and current waveforms]

3.3.3 Performance Comparison With PSC-PWM

The dynamic performance of the DSAZE-PWM is experimentally validated on a three-phase MMC system with a single 3L-FC submodule per arm. The three-phase converter is designed for a 208 V, 3 kW rated capacity. The main DC-link voltage of 360 V is generated by using the Xantrex DC-power source of 600 V, 20 A capacity. The submodule outer and inner capacitor rated voltages are approximately 360 V and 180 V respectively. The sampling frequency of 1080 Hz is selected. The experimental results with a step change in the modulation index are shown in Figure 3.10. Initially, the converter is operating at a m_a=0.5, f_o=60 Hz, and full-load condition. The output voltage and current waveforms are shown in Figure 3.10(a). The converter output has two-level line-line voltage waveform. The output and arm currents have

less switching ripple.

At t=50 ms, the modulation index is changed from 0.5 to 0.9. The output line-line voltage waveform has three voltage levels with a step of 180 V as shown in Figure 3.10(a). The magnitude of output and arm currents increased with the modulation index. The experimental results with conventional PSC-PWM are shown in Figure 3.10(b). The output voltage is shown in Figure 3.10(b), which represents the three-level equivalent operation of MMC. However, the harmonic distortion with PSC-PWM is much higher than the DSAZE-PWM scheme. The ripple in the output current is also higher compared with the DSAZE-PWM scheme.

3.4 Dual Space Vector Modulation

The control block diagram of MMC with dual space vector modulation scheme is shown in Figure 3.11. The reference phase modulating signals are generated with the required modulation index (m_a) and frequency (f_o). The upper and lower arm modulating signals are derived from the phase modulating signals. The nearest switching vectors and dwell times are obtained from the reference arm modulating signals. Each switching vector represents the required number of SMs that should be turned on in three-phases. The switching vectors and dwell times are applied to the voltage balancing approach. The balancing approach generates gating signals to the selected SMs, depending on the submodule capacitors voltage and direction of arm current.

The space vector modulation (SVM) is one of the low switching frequency modulation approach applied to the high-power multilevel converters. The SVM approach is flexible in the selection of best switching vectors among the redundancy switching vectors to enhance the DC-link utilization, better harmonic performance, and regulation of common-mode voltage magnitude, etc. In spite of its significant advantages, SVM for more than three-level converter is difficult to implement, due to the large number of switching vectors

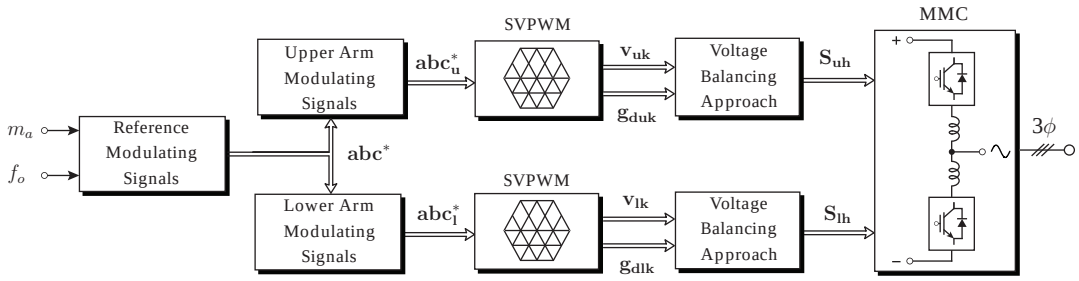


Figure 3.11. Control block diagram of MMC with dual-SVM scheme

and switching sequences that accompany the higher number of voltage levels. The space vector diagram of m-level converter consists of m^3 switching vectors and $6(m-1)^2$ triangles. In SVM scheme, the determination of redundant switching vectors and switching sequences is a more challenging task.

The implementation of SVM scheme in $\alpha - \beta$ and $\alpha - \beta - 0$ coordinate system involves coordinate transformation, trigonometric functions and look-up tables, which increases the computational load of the modulation stage [160]. The implementation of SVM in abc-coordinate system overcomes the above drawbacks and easy to obtain the switching vectors and duty cycles as it were an equivalent of two-level SVM [158, 164, 165]. This approach has the following features:

- switching states, duty cycles, and switching sequences are obtained by simple calculations; thus, no look-up table is required.
- computationally less complex and extendable to the modular multilevel converter with any number of voltage levels without any modifications.

3.4.1 Design Procedure

The upper and lowers arms of three-phase MMC system are controlled using an independent SVM scheme. This approach is referred as dual SVM

approach. The three-phase upper and lower arm reference voltages are obtained from the reference phase voltages. The nearest switching vectors and corresponding duty cycles are calculated by decomposing the multilevel space vector into several two-level space vectors in abc-coordinate system. The implementation of dual SVM approach mainly consists of following three steps:

- **Step-I: Synthesis of Reference Arm Voltage Vectors**

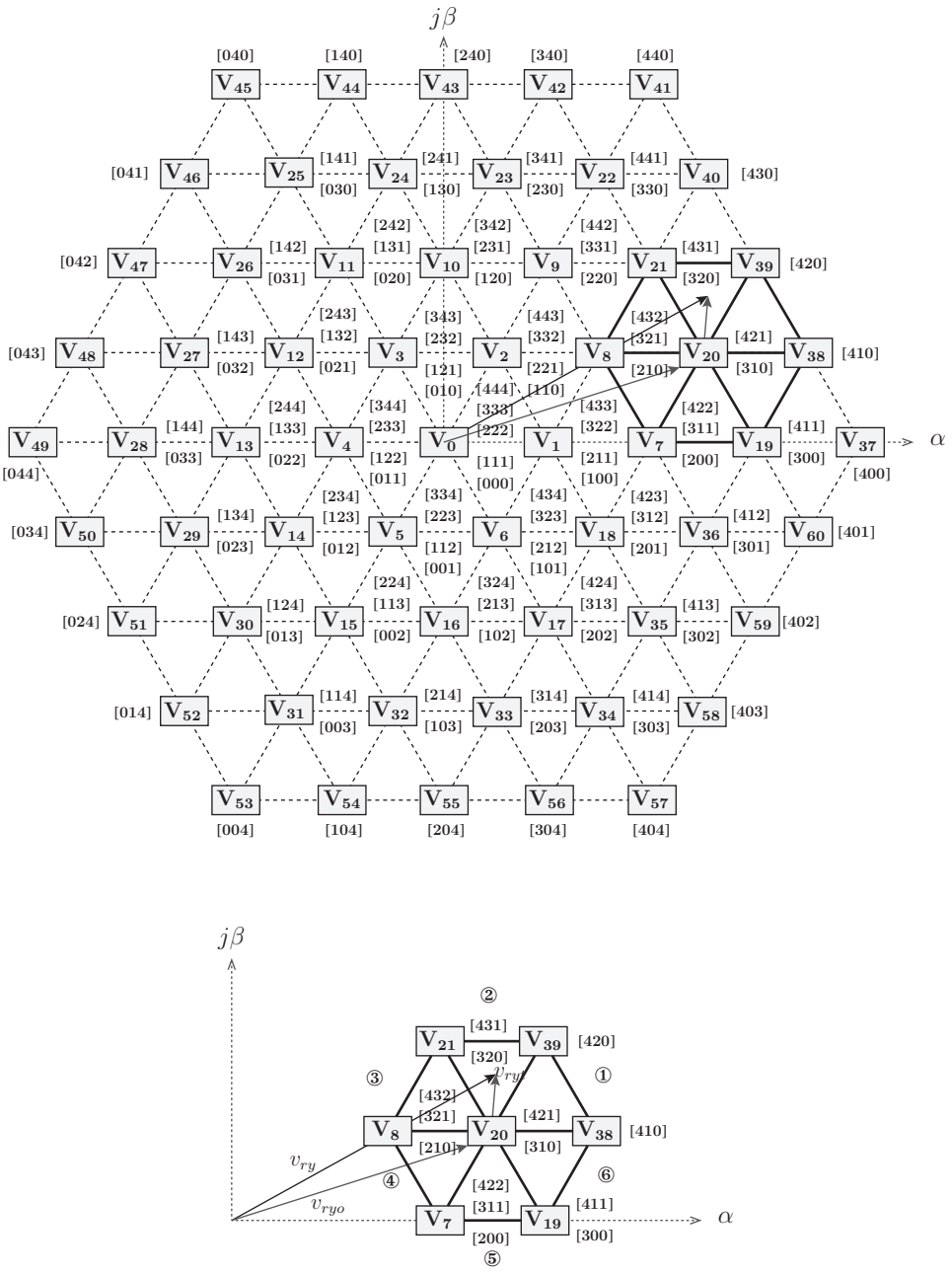
The normalized reference output vector ($\overrightarrow{v}_r$) for an m-level modular multilevel converter is defined as follows:

$$\overrightarrow{v}_r = \begin{bmatrix} a^* \\ b^* \\ c^* \end{bmatrix} = \frac{m-1}{2} \begin{bmatrix} m_a \sin(\omega_o t) \\ m_a \sin(\omega_o t - \frac{2\pi}{3}) \\ m_a \sin(\omega_o t - \frac{4\pi}{3}) \end{bmatrix} \tag{3.4.1}$$

The upper and lower arm reference vectors are obtained from the normalized reference output vector and expressed as follows:

$$\begin{aligned} \overrightarrow{v}_{ru} &= \begin{bmatrix} a_u^* \\ b_u^* \\ c_u^* \end{bmatrix} = \frac{m-1}{2} \begin{bmatrix} 1 - m_a \sin(\omega_o t) \\ 1 - m_a \sin(\omega_o t - \frac{2\pi}{3}) \\ 1 - m_a \sin(\omega_o t - \frac{4\pi}{3}) \end{bmatrix} \\ \overrightarrow{v}_{rl} &= \begin{bmatrix} a_l^* \\ b_l^* \\ c_l^* \end{bmatrix} = \frac{m-1}{2} \begin{bmatrix} 1 + m_a \sin(\omega_o t) \\ 1 + m_a \sin(\omega_o t - \frac{2\pi}{3}) \\ 1 + m_a \sin(\omega_o t - \frac{4\pi}{3}) \end{bmatrix} \end{aligned} \tag{3.4.2}$$

where m_a is the number of output voltage levels, m_a is the modulation index in the range of $0 \leq m_a \leq 1$, and ω_o is the fundamental angular frequency.



Two-Level Space Vector Hexagon

Figure 3.12. Space vector diagram for a 5L-MMC

The generalized five-level space vector diagram is shown in Figure 3.12. The normalized arm reference vector ($\overrightarrow{v}_{ry}$) is decomposed into an offset voltage vector ($\overrightarrow{v}_{ryo}$) and a two-level voltage vector ($\overrightarrow{v}_{ryt}$) as follows:

$$\overrightarrow{v}_{ry} = \overrightarrow{v}_{ryo} + \overrightarrow{v}_{ryt} \tag{3.4.3}$$

The offset voltage vector represents the origin of the two-level space vector diagram, and their coordinates (a_{y0}, b_{y0}, c_{y0}) are given by,

$$\begin{aligned} a_{y0} &= floor(a_y^*) \\ b_{y0} &= floor(b_y^*) \\ c_{y0} &= floor(c_y^*) \end{aligned} \tag{3.4.4}$$

The two-level voltage vector ($\overrightarrow{v}_{ryt}$) is located in one of the six sectors of the two-level space vector diagram as shown in Figure 3.12. The switching vectors, which forms the two-level space vector diagram are obtained from the coordinates (a_{y0}, b_{y0}, c_{y0}) and (a_{y1}, b_{y1}, c_{y1}). The coordinates (a_{y1}, b_{y1}, c_{y1}) are given by,

$$\begin{aligned} a_{y1} &= 1 + a_{y0} \\ b_{y1} &= 1 + b_{y0} \\ c_{y1} &= 1 + c_{y0} \end{aligned} \tag{3.4.5}$$

The switching vectors, which forms the two-level space vector diagram are (a_{y0}, b_{y0}, c_{y0}), (a_{y1}, b_{y0}, c_{y0}), (a_{y1}, b_{y1}, c_{y0}), (a_{y0}, b_{y1}, c_{y0}), (a_{y0}, b_{y1}, c_{y1}), (a_{y0}, b_{y0}, c_{y1}), (a_{y1}, b_{y0}, c_{y1}), and (a_{y1}, b_{y1}, c_{y1}).

- **Step-II: Determination of Switching Vectors**

In abc-coordinate system, the normalized reference vector is synthesized by using the nearest four switching vectors. The volt-sec balance of the reference vector is given by,

$$\begin{aligned} \overrightarrow{v}_{ry}\, T_s &= \overrightarrow{v}_{y1}\, T_{y1} + \overrightarrow{v}_{y2}\, T_{y2} + \overrightarrow{v}_{y3}\, T_{y3} + \overrightarrow{v}_{y4}\, T_{y4} \\ T_s &= T_{y1} + T_{y2} + T_{y3} + T_{y4} \end{aligned} \tag{3.4.6}$$

Table 3.2. Switching Vectors in each Sector

sector	$\overrightarrow{v}_{y1}$	$\overrightarrow{v}_{y2}$	$\overrightarrow{v}_{y3}$	$\overrightarrow{v}_{y4}$
①	(a_{y0}, b_{y0}, c_{y0})	(a_{y1}, b_{y0}, c_{y0})	(a_{y1}, b_{y1}, c_{y0})	(a_{y1}, b_{y1}, c_{y1})
②	(a_{y0}, b_{y0}, c_{y0})	(a_{y0}, b_{y1}, c_{y0})	(a_{y1}, b_{y1}, c_{y0})	(a_{y1}, b_{y1}, c_{y1})
③	(a_{y0}, b_{y0}, c_{y0})	(a_{y0}, b_{y1}, c_{y0})	(a_{y0}, b_{y1}, c_{y1})	(a_{y1}, b_{y1}, c_{y1})
④	(a_{y0}, b_{y0}, c_{y0})	(a_{y0}, b_{y0}, c_{y1})	(a_{y0}, b_{y1}, c_{y1})	(a_{y1}, b_{y1}, c_{y1})
⑤	(a_{y0}, b_{y0}, c_{y0})	(a_{y0}, b_{y0}, c_{y1})	(a_{y1}, b_{y0}, c_{y1})	(a_{y1}, b_{y1}, c_{y1})
⑥	(a_{y0}, b_{y0}, c_{y0})	(a_{y1}, b_{y0}, c_{y0})	(a_{y1}, b_{y0}, c_{y1})	(a_{y1}, b_{y1}, c_{y1})

These switching vectors are identified based on the location of the normalized reference vector in two-level space vector diagram. The location of the normalized reference vector is obtained from the coordinates (a_{y0}, b_{y0}, c_{y0}) and (a_{y1}, b_{y1}, c_{y1}). The nearest four switching vectors in different sectors are shown in Table 3.2. The vectors $\overrightarrow{v}_{y1}$ and $\overrightarrow{v}_{y4}$ are located at the origin of the two-level space vector diagram. The distribution of the duty cycles between the vectors $\overrightarrow{v}_{y1}$ and $\overrightarrow{v}_{y4}$ will affect the common-mode voltage component only. In this study, the duty cycles between the vectors $\overrightarrow{v}_{y1}$ and $\overrightarrow{v}_{4}$ are equally distributed.

- **Step-III: Calculation of Dwell Times**

Once the switching vectors are identified, the next step is to calculate the dwell times of each switching vector. These dwell times are calculated from

the reference arm voltages. The dwell times of each arm are given by,

$$\begin{aligned} T_{ay} &= (a_y^* - floor(a_y^*)) \times T_s \\ T_{by} &= (b_y^* - floor(b_y^*)) \times T_s \\ T_{cy} &= (c_y^* - floor(c_y^*)) \times T_s \end{aligned} \tag{3.4.7}$$

The dwell time of each switching vector is expressed as follows:

$$\begin{aligned} T_{y1} &= 1 - max(T_{ay}, T_{by}, T_{cy}) \\ T_{y2} &= max(T_{ay}, T_{by}, T_{cy}) - med(T_{ay}, T_{by}, T_{cy}) \\ T_{y3} &= med(T_{ay}, T_{by}, T_{cy}) - min(T_{ay}, T_{by}, T_{cy}) \\ T_{y4} &= min(T_{ay}, T_{by}, T_{cy}) \\ T_{y0} &= T_{y1} + T_{y4} \end{aligned} \tag{3.4.8}$$

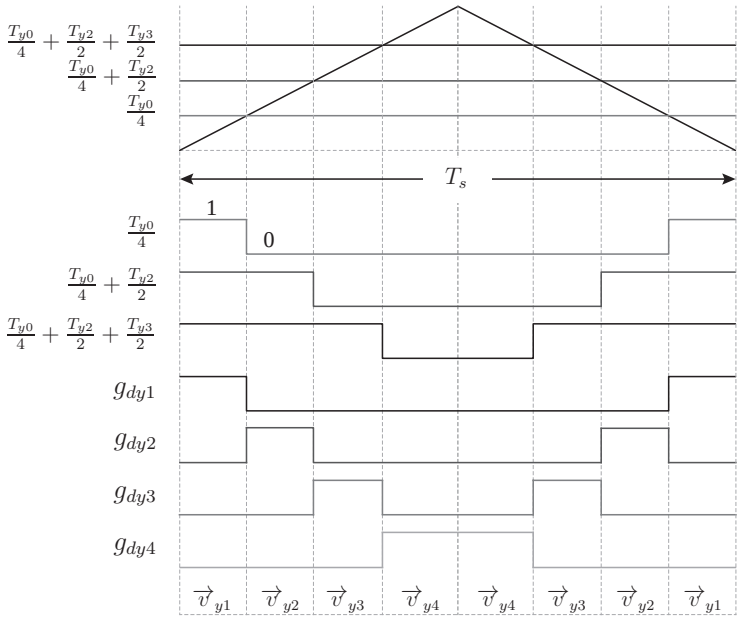


Figure 3.13. Dwell times of the switching vectors

These duty cycles are compared with the symmetrical triangular waveform shown in Figure 3.13, to obtain the pulses g_{dy1}, g_{dy2}, g_{dy3}, and g_{dy4} corresponding to the switching vectors $\vec{v}_{y1}$, $\vec{v}_{y2}$, $\vec{v}_{y3}$, and $\vec{v}_{y4}$, respectively.

After the switching vectors and duty cycles are calculated, the final output of the modular multilevel converter is determined by selecting the appropriate sequence of switching vectors. The symmetrical switching sequence is extensively used to achieve the lowest voltage harmonic distortion and current ripple. The symmetrical switching sequence $\overrightarrow{v}_{y1} \rightarrow \overrightarrow{v}_{y2} \rightarrow \overrightarrow{v}_{y3} \rightarrow \overrightarrow{v}_{y4} \rightarrow \overrightarrow{v}_{y4} \rightarrow \overrightarrow{v}_{y3} \rightarrow \overrightarrow{v}_{y2} \rightarrow \overrightarrow{v}_{y1}$ is applied over a sampling time (T_s).

3.4.2 Capacitors Voltage Balancing Approach With Reduced Current Sensors

The voltage balancing approach requires the direction of arm current, which is obtained from the direct measurement of arm currents using hall sensors. The three-phase MMC requires six current sensors to obtain the direction of arm current. However, the number of current sensors can be reduced by estimating the arm currents. The arm current consists of the following current components: AC circulating current (i_{xz}), DC current component (i_s), and AC output current (i_x). The AC circulating currents are mainly presents due to the voltage difference between upper and lower submodule capacitors voltage. These circulating currents affect the efficiency and reliability of MMC only. Therefore, the circulating currents can be neglected during the capacitors voltage balancing among submodules. Hence, the DC current and AC output current components only exist in the arm current. The magnitude of DC current component varies with the active power demanded by the load and is estimated by using the following equation [90]:

$$i_s = \frac{m_a\, I \cos\varphi}{4} \tag{3.4.9}$$

where I represent the root mean square (RMS) value of load current and $\cos\varphi$ represents the load power factor. The AC output current is directly measured by using three current sensors and its magnitude equally distributed between upper and lower arms. By doing so, the number of current sensors is reduced by 50% compared with the existing balancing approaches.

The flow chart of proposed voltage balancing approach is shown in Figure 3.14(a). The implementation of proposed voltage balancing approach mainly consists of three stages, as follows:

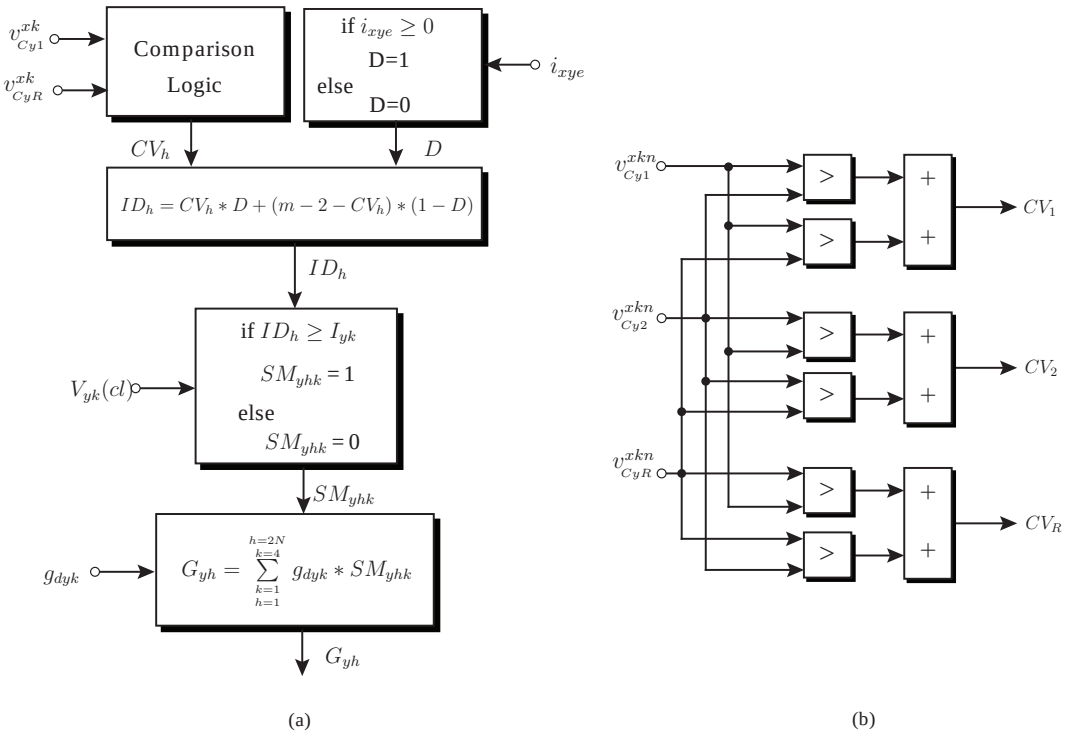


Figure 3.14. Voltage balancing approach: (a) design steps of balancing approach, (b) comparison logic

- **Stage-I: Generation of Index Number for Submodule Capacitors**

In proposed approach, the SM capacitor with the lowest voltage is inserted in the arm during the positive direction of the current. Similarly, the SM capacitors with the highest voltage are chosen to be inserted to let them discharge during the negative direction of the current. Achieving this objective requires a relative comparison logic with the normalized capacitor voltage as shown in Figure 3.14(b).

The normalized capacitor voltage of the 3L-FC module is expressed as follows:

$$\begin{aligned} v_{Cy1}^{xkn} &= \frac{v_{Cy1}^{xk}}{V_{C1}} \\ v_{Cy2}^{xkn} &= \frac{v_{Cy2}^{xk}}{V_{C2}} \end{aligned} \tag{3.4.10}$$

Each capacitor voltage is compared with other capacitor voltages, as shown in Figure 3.14(b), and their outputs are added together. The final output becomes an index number (CV_h). The range of index numbers is $CV_h \in \{0, 1.....m-2\}$ and $h \in \{1, 2.....2N-1, 2N\}$. The output of comparison logic can be directly used to generate the SM IGBT status in stage-II for the positive direction of the current. However, these index numbers should be rearranged for the negative direction of the current. The direction of current is incorporated into the process of index number generation to meet this objective and maintain the compatibility between the stage-I and stage-II variables. The actual index number (ID_h) for each capacitor voltage is obtained using Equation (3.4.11)

$$ID_h = CV_h * D + (m - 2 - CV_h) * (1 - D) \tag{3.4.11}$$

where D is the direction of estimated arm current and is expressed as follows:

$$D = \begin{cases} 1 & i_{xye} \geq 0 \\ 0 & i_{xye} < 0 \end{cases} \tag{3.4.12}$$

Based on the equations (3.4.11) and (3.4.12), the relative comparison logic in stage-I assigns the highest priority index number to the highest capacitor voltage during the positive direction of the current (D=1 and $ID_h = CV_h$). In the negative direction of the current, the highest priority index number is assigned to the lowest capacitor voltage (D=0 and $ID_h = m - 2 - CV_h$). Index number generation is further explained in the example shown in Table 3.3. In this example, two 3L-FC (N=2) modules per arm are considered. Table 3.3 shows that the highest priority index number is assigned to SM^2

inner capacitor (v_{Cu3}^{an}) in the positive direction of the current. In the negative direction of the current, the highest priority index number is assigned to the SM^2 outer capacitor with the lowest voltage (v_{Cu4}^{an}).

Table 3.3. Index number generation for N=2, m=2N+1=5

Normalized Cap. Voltage	CV_h	ID_h for $i_{xye} \geq 0$ & D=1	ID_h for $i_{xye} < 0$ & D=0
$v_{Cu1}^{an} = 0.95$	CV_1=2	ID_1=2	ID_1=1
$v_{Cu2}^{an} = 0.93$	CV_2=1	ID_2=1	ID_2=2
$v_{Cu3}^{an} = 0.92$	CV_3=0	ID_3=0	ID_3=3
$v_{Cu4}^{an} = 0.98$	CV_4=3	ID_4=3	ID_4=0

- **Stage-II: Determination of Submodule IGBT Status**

Stage-II requires the nearest switching vectors from the modulation stage. Each vector has three elements, which represent the required number of SMs that should be turned on in three phases. These elements are extracted from the switching vectors and processed by using the voltage balancing approach. The term $\overrightarrow{v}_{yk}(cl)$ represents the elements of the switching vector (upper and lower arm), where $y \in \{u, l\}$ represents the arm, $k \in \{1, 2, 3, 4\}$ represents the switching vectors, and $cl \in \{1, 2, 3\}$ represents the elements in each switching vector. These elements are used to generate the reference index number (I_{yk}), which is given by,

$$\begin{aligned} I_{yk} &= R - \overrightarrow{v}_{yk}(cl) \\ R &= m - 1 \end{aligned} \tag{3.4.13}$$

The reference index number (I_{yk}) dynamically varies with the switching vectors. The reference index number is compared with the actual index num-

ber of the capacitor voltage (ID_h) to determine the IGBT status (SM_{yhk}) corresponding to that capacitor voltage, that is, ON (1) / OFF (0). If $SM_{yhk} = 1$, then the IGBT device corresponding to that particular capacitor should be turned on. Otherwise, it should be turned off.

The implementation of stage-II is explained by using the example shown in Table 3.4. In this example, the switching vectors $\overrightarrow{v}_{y1}$=(3,2,2), $\overrightarrow{v}_{y2}$=(4,2,2), $\overrightarrow{v}_{y3}$=(4,3,2) and $\overrightarrow{v}_{y4}$=(4,3,3) are considered. The switching states corresponding to phase-a is extracted from the switching vectors and are expressed as $\overrightarrow{v}_{y1}(1)$=3, $\overrightarrow{v}_{y2}(1)$=4, $\overrightarrow{v}_{y3}(1)$=4 and $\overrightarrow{v}_{y4}(1)$=4. Based on the equation (3.4.13), the reference index numbers for each switching vector are expressed as I_{y1}=1, I_{y2}=0, I_{y3}=0, and I_{y4}=0. The actual index number (ID_h) of the SM is compared with the reference index number. The IGBT status of the corresponding SM capacitor voltage is shown in Table 3.4.

Table 3.4. Determination of IGBT status N=2, m=5, R=4 and D=1

ID_h	I_{yk}	SM_{yhk}
ID_1=2	I_{y1}=1	SM_{y11}=1, SM_{y12}=1, SM_{y13}=1, SM_{y14}=1
ID_2=1	I_{y2}=0	SM_{y21}=1, SM_{y22}=1, SM_{y23}=1, SM_{y24}=1
ID_3=0	I_{y3}=0	SM_{y31}=0, SM_{y32}=1, SM_{y33}=1, SM_{y34}=1
ID_4=3	I_{y4}=0	SM_{y41}=1, SM_{y42}=1, SM_{y43}=1, SM_{y44}=1

- **Stage-III: Generation of Gating Pattern**

After determining the IGBT status, the final step is to generate the gating pattern for the IGBT devices of each 3L-FC module. Stage-III requires the gating pulses (g_{dy1}, g_{dy2}, g_{dy3}, and g_{dy4}) corresponding to the nearest switching vectors ($\overrightarrow{v}_{y1}$, $\overrightarrow{v}_{y2}$, $\overrightarrow{v}_{y3}$, and $\overrightarrow{v}_{y4}$), respectively. These gating pulses are obtained from the modulation stage. The IGBT status (SM_{yhk}) from stage-II

is used along with the pulses to generate the final gating pattern (G_{yh}). The generalized gating of the IGBT device is defined as follows:

$$G_{yh} = \sum_{\substack{k=1 \\ h=1}}^{\substack{h=2N \\ k=4}} g_{dyk} * SM_{yhk} \tag{3.4.14}$$

Equation (3.4.14) is expanded and presented for single IGBT device of G_{y1}, as follows:

$$\begin{aligned} G_{y1} = g_{dy1} * SM_{y11} + g_{dy2} * SM_{y12} \\ + g_{dy3} * SM_{y13} + g_{dy4} * SM_{y14} \end{aligned} \tag{3.4.15}$$

Similarly, the equations for the gating patterns of other IGBT devices in an arm can be obtained by using the equation (3.4.14). Stage-III of the proposed approach is explained by the example shown in Table. 3.5. The devices $Gy1$ and G_{y2} belong to SM^1, whereas G_{y3} and G_{y4} belong to SM^2. We observed that SM^1 is inserted, whereas the SM^2 is operated in the PWM mode. In one sampling interval, only one device changes its state to either "ON-OFF" or "OFF-ON". In this example, the devices G_{y1}, G_{y2} and G_{y4} are inserted, and G_{y3} is operated in PWM mode over a sampling interval. The proposed approach mainly involves simple comparisons only. The digital implementation of these comparison logics is easy and can be easily extended to the large number of SMs per arm without any difficulty.

Table 3.5. Gating pattern generation

G_{yh}
$G_{y1} = g_{dy1} + g_{dy2} + g_{dy3} + g_{dy4}$
$G_{y2} = g_{dy1} + g_{dy2} + g_{dy3} + g_{dy4}$
$G_{y3} = g_{dy2} + g_{dy3} + g_{dy4}$
$G_{y4} = g_{dy1} + g_{dy2} + g_{dy3} + g_{dy4}$

3.5 Dynamic and Steady-State Performance of Dual-Space Vector Modulation

The performance of the proposed SVM scheme and capacitor voltage balancing approach is verified on a three-phase MMC system by using the MATLAB / SIMULINK software. The three-phase MMC system consists of three 3L-FC modules per arm. The rated voltage of outer and inner capacitors is V_{C1} = 3.33 kV and V_{C2} = 1.66 kV, respectively. The sampling frequency of the proposed modulation scheme is 1200 Hz.

3.5.1 Dynamic Performance

The simulation results with the step change in modulation index are shown in Figure 3.15. From t = 0 s to t = 0.1 s, the converter operates at a modulation index of m_a = 0.5 and frequency of f_o = 60 Hz. At t = 0.1 s, the modulation index is changed from 0.5 to 0.9 and frequency is kept constant. The upper and lower arm submodule outer and inner capacitors voltage are maintained at 3.33 kV and 1.66 kV, respectively as shown in Figure 3.15(a)-(b). The ripple in capacitors voltage is increased with the modulation index. Unlike CPWM, the SVM approach perfectly maintaining the upper and lower arm submodule capacitors voltage at an identical average value during the external disturbance. The three-phase output voltages and currents are balanced. The output voltage steps and the magnitude of the output current are increased with the modulation index as shown in Figure 3.15(c)-(d). With SVM, the ripple in arm current and output current is significantly reduced as shown in Figure 3.15(e). Hence, the smaller output filter is required to eliminate the switching frequency harmonics.

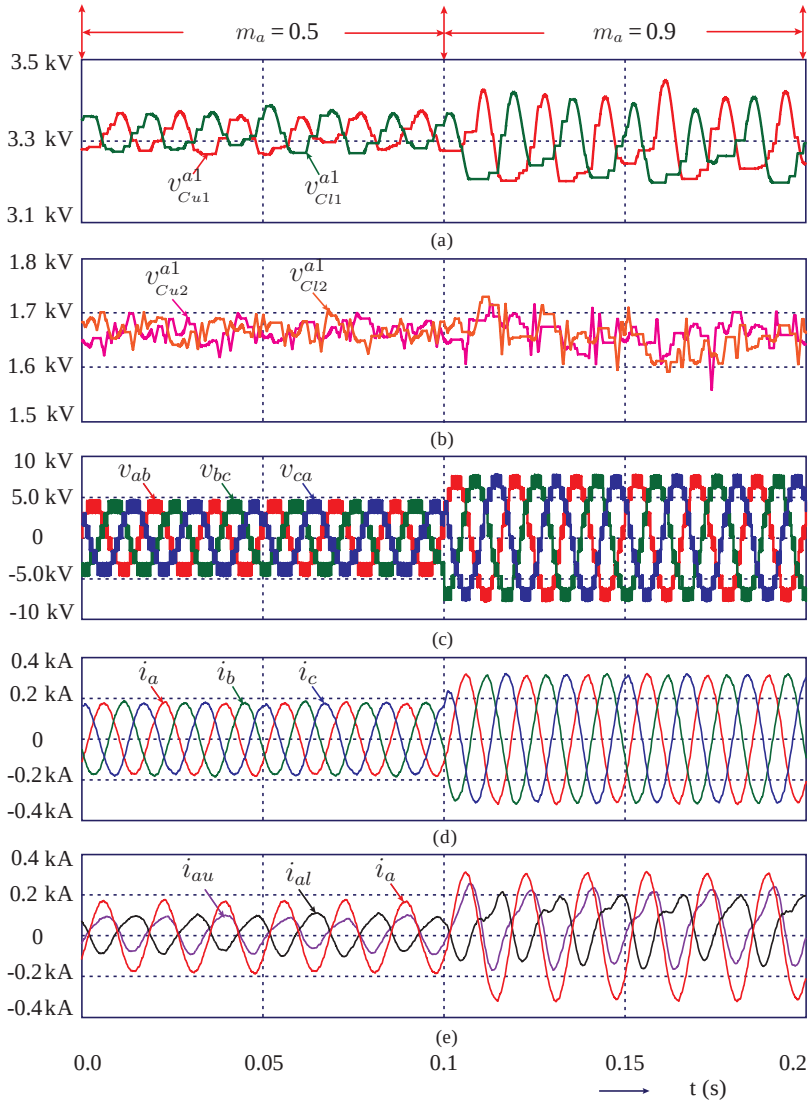


Figure 3.15. Transient operation: (a) phase-a, upper and lower arm SM^1 outer capacitors voltage, (b) phase-a, upper and lower arm SM^1 inner capacitors voltage, (c) three-phase line voltages, (d) three-phase line currents and (e) upper, lower arm and phase-a current waveforms

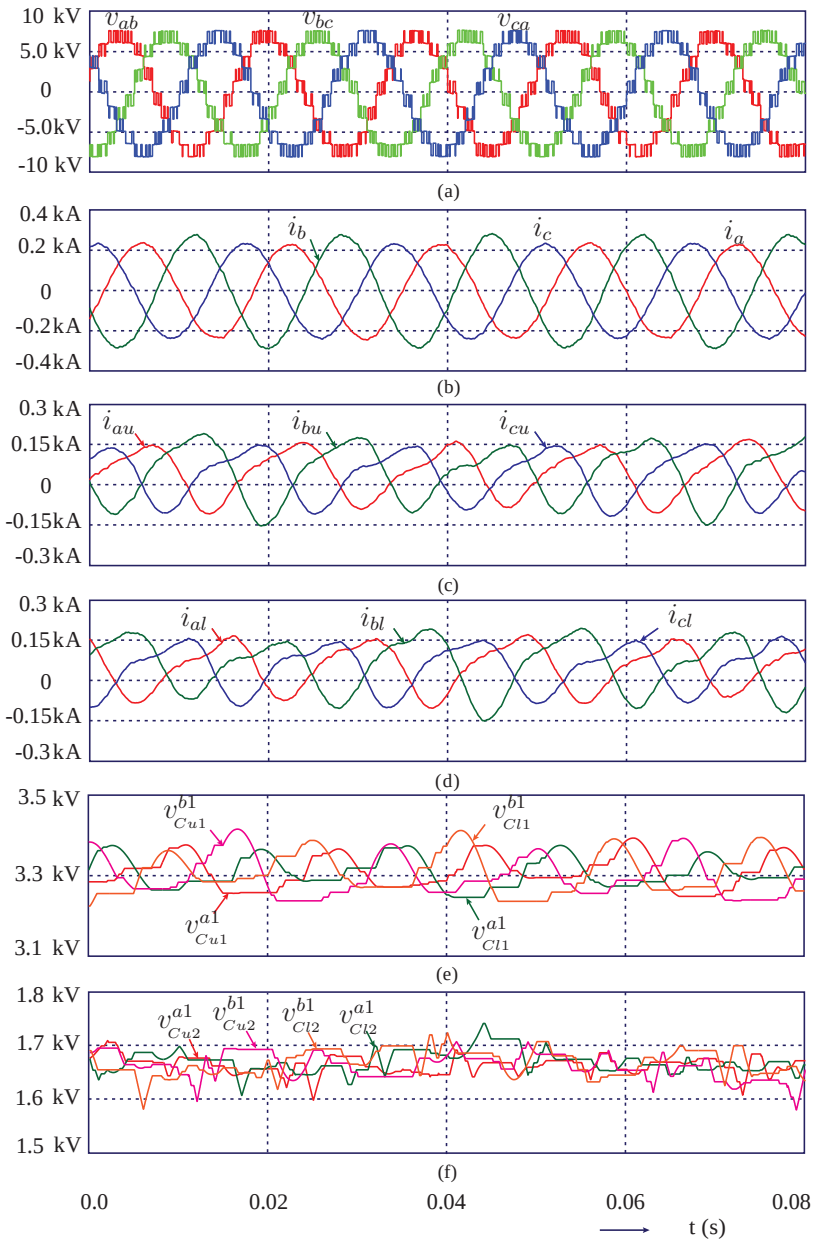


Figure 3.16. Simulation results of unbalanced operation: (a) three-phase line voltages, (b) three-phase line currents, (c) three-phase upper arm currents, (d) three-phase lower arm currents, (e) phase-a, -b, upper and lower arm SM^1 outer capacitors voltage, and (f)phase-a, -b, upper and lower arm SM^1 inner capacitors voltage

3.5.2 Unbalanced Operation

The performance of proposed approach with the unbalanced load is shown in Figure 3.16. In this case, the load parameters of phase-b are different from those of phases-a and c. The converter output has the balanced three-phase output voltages corresponding to a modulation index of $m_a = 0.9$ and frequency of $f_o = 60$ Hz as shown in Figure 3.16(a). During the unbalanced operation, the three-phase output currents are sinusoidal and unbalanced in nature as shown in Figure 3.16(b). The output currents are equally distributed between upper and lower arms as shown in Figure 3.16(c)-(d). The unbalanced operation causes positive and zero sequence circulating currents along with the negative sequence circulating current component at double the frequency. These additional circulating currents contribute additional device stress and conduction losses [117, 118]. The phase-a and -b submodule outer and inner capacitors voltage is maintained at their nominal value as shown in Figure 3.16(e)-(f). The submodule capacitors in unbalanced phase-b have higher voltage ripple compared with other phases.

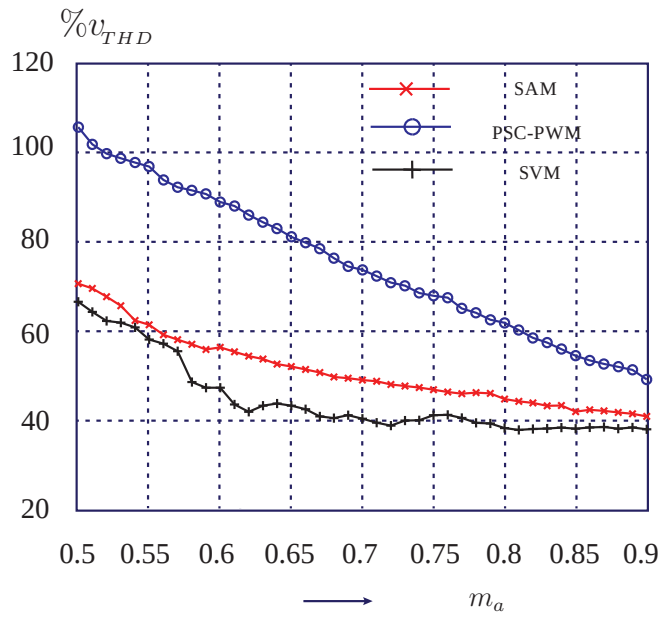


Figure 3.17. THD analysis

3.5.3 Total Harmonic Distortion

The performance comparison of PSC-PWM, DSAZE-PWM and SVM strategies in terms of total harmonic distortion (THD) at different modulation indices is shown in Figure 3.17. The results show the DSAZE-PWM scheme has less harmonic distortion compared with the PSC-PWM scheme. However, it has a slightly higher THD compared with the SVM strategy owing to the asymmetrical distribution of time duration for zero vectors. The asymmetrical distribution of zero vectors generate sub-harmonics, which leads to higher harmonic distortion.

3.6 Experimental Validation

The performance of dual space vector modulation and submodule capacitors voltage balancing approach is verified on a 3 kVA, 208 V rated prototype of three-phase MMC with 3L-FC SMs. Each arm has single 3L-FC SM with two floating capacitors of 350 V and 175 V rated capacity.

3.6.1 Dynamic Performance

The transient operation of proposed voltage balancing approach is shown in Figure 3.18. These results are presented for a lagging load power factor of 0.85. Initially, the converter is operated at m_a=0.5 and f_o=60 Hz. The phase-a, upper and lower arm submodule outer and inner capacitors voltage are maintained at 350 V and 175 V, respectively as shown in Figure 3.18(a). The output line-voltage has two levels corresponding to a modulation index of 0.5 as shown in Figure 3.18(b). The load current has a magnitude of 5 A, which is equally distributed between the upper and lower arms as shown in Figure 3.18(b).

The modulation index is suddenly changed from 0.5 to 0.9, and the frequency is maintained constant. The balancing approach effectively maintains the upper and lower arm submodule capacitors voltage at their nomi-

nal value. The number of output voltage levels is increased with modulation index. At m_a=0.9, the output voltage has three-levels equivalent to three-level operation. The magnitude of the output current is increased to 10 A, as shown in Figure 3.18(b). The arm currents have low ripple compared to the PSC-PWM scheme.

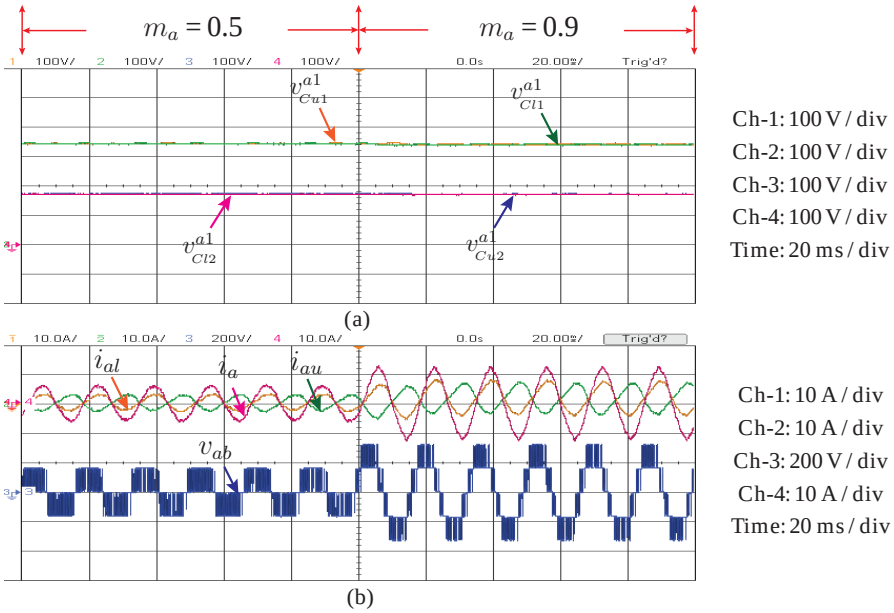


Figure 3.18. Experimental results for step change in the modulation index: (a) upper and lower arm submodule capacitors voltage, and (b) output voltage and current waveforms

3.6.2 Unbalanced Operation

During this operation, the three-phase modulating signals are generated with a modulation index of m_a=0.7 and frequency of f_o=60 Hz. Initially, the load is perfectly balanced, and converter generates balanced three-phase voltages across the load as shown in Figure 3.19(a). These voltages generate balanced currents with a magnitude of 5 A as shown in Figure 3.19(b). The upper and lower arm currents of phase-a and b are balanced and equal in magnitude shown in Figure 3.19(c). The three-phase upper and lower arm submodule

outer and inner capacitors voltage perfectly maintained at 350 V and 175 V, respectively as shown in Figure 3.20(a)-(c).

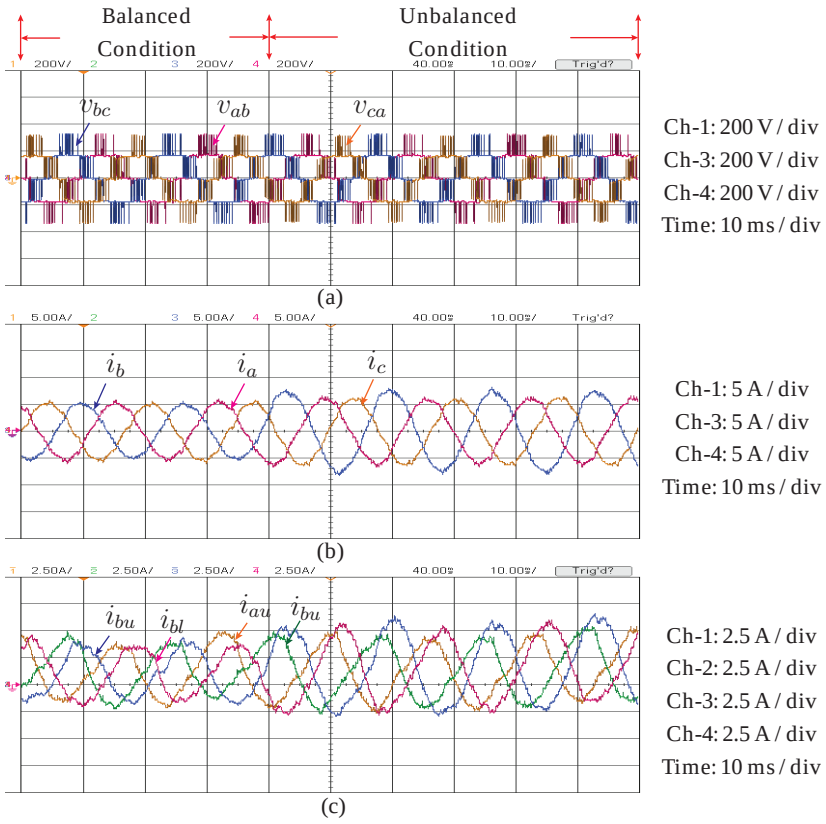


Figure 3.19. Experimental results with unbalanced load at m_a=0.7 and f_o=60 Hz: (a) three-phase output line voltages, (b) three-phase output currents, and (c) upper and lower arm currents

Subsequently, the impedance of phase-b is changed, resulting in unbalanced operation of MMC. The converter generates balanced voltages across the load due to balanced modulating signals as shown in Figure 3.19(a). However, the load currents are unbalanced in nature due to the unbalanced load as shown in Figure 3.19(b). The unbalanced nature of load currents reflects in the arm currents as shown in Figure 3.19(c). Due to the unbalanced operation, the circulating currents consist of zero sequence components along with the positive and negative sequence double frequency com-

ponents. These additional current components increase the device stress and power losses. Minimizing the circulating currents by using circulating current controller is necessary to improve the performance of MMC. However, the circulating current does not have any negative affect on the submodule capacitors voltage balancing approach. The three-phase submodule outer and inner capacitor voltages from the upper and lower arms are shown in Figure 3.20(a)-(c). The balancing approach is effectively maintaining the SM capacitor voltages by using the estimated arm currents.

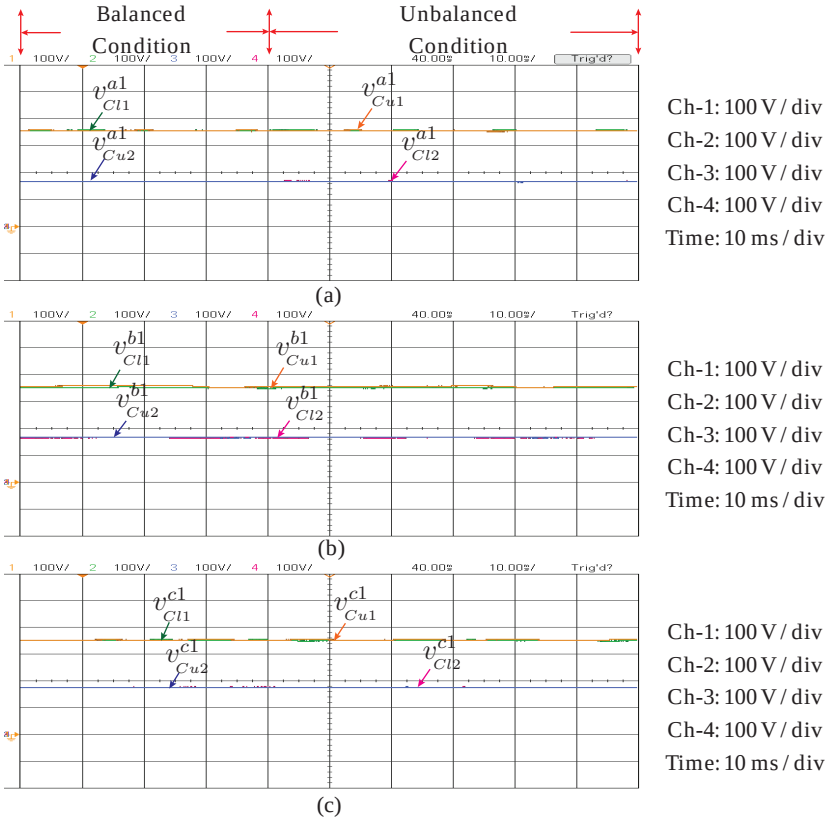


Figure 3.20. Experimental results with unbalanced load at m_a=0.7 and f_o=60 Hz: (a) phase-a submodule capacitors voltage, (b) phase-b submodule capacitors voltage, and (c) phase-c submodule capacitors voltage

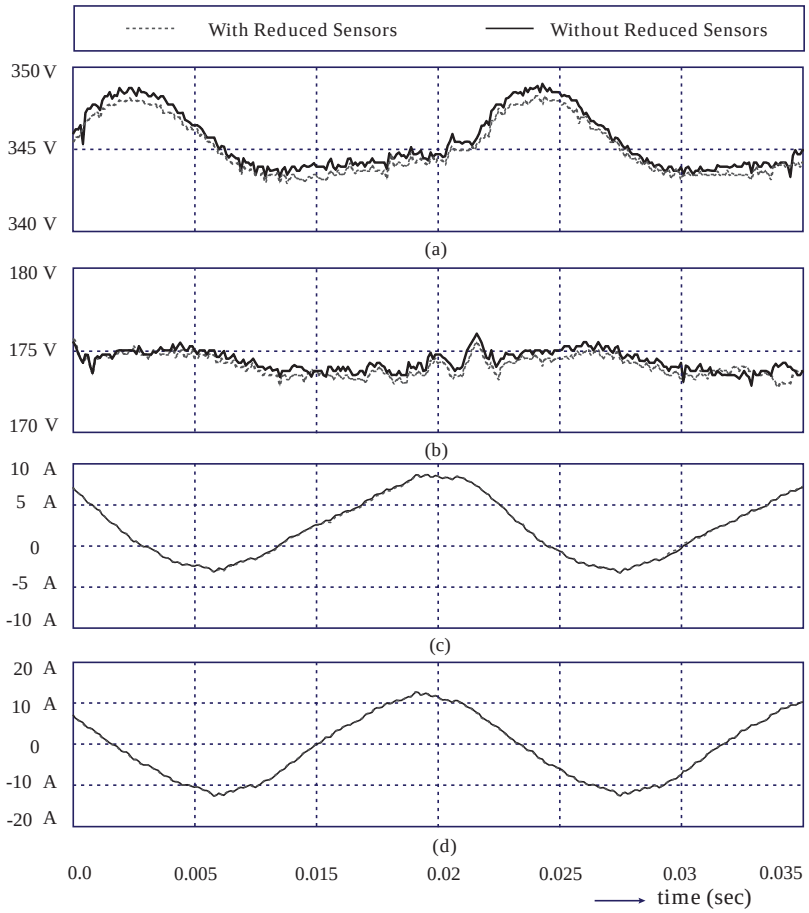


Figure 3.21. Experimental results: (a) submodule outer capacitor voltage, (b) submodule inner capacitor voltage, (c) upper arm current, and (d) phase-a line current

3.6.3 Comparison of Balancing Approach With and Without Current Sensors Reduction

The performance of voltage balancing approach with the direct measurement of arm currents is compared with the balancing approach with the estimated arm currents. The experimental results of this comparison are shown in Figure 3.21. The voltage variation of submodule outer and inner capacitors is very close in a relationship as shown in Figure 3.21(a)-(b). However, there is

a marginal error in their average voltages. The current flowing through the arm and load is identical in shape as shown in figure 3.21(c)-(d). Overall, the results show that the performance of balancing approach with direct measurement and estimated arm currents are very close and identical. As such, using the estimated arm current for voltage balancing in the MMC is possible. With this approach, the required number of current sensors is effectively reduced by 50% in a three-phase system.

3.7 Summary

In this chapter, two novel modulation schemes named as sampled average modulation and dual space vector modulation schemes are proposed. These modulation schemes are equivalent to the sinusoidal modulation with third-order harmonic injection. The injected third-order harmonic component minimizes the internal converter unbalance (i.e., voltage balancing between arms).

The sampled average modulation approach follows the per-phase philosophy, computationally less complex and easy to apply for MMC with any number of phases and submodules. The three-phase equivalent of sampled average modulation is named as DSAZE-PWM and generates an output voltage with lowest harmonic distortion, output current with the lowest ripple and reduces the magnitude of switching frequency harmonics compared with the PSC-PWM. In addition, a simple voltage balancing approach is proposed to achieve the voltage balancing among submodules. The experimental and simulation studies are conducted, and results show the satisfactory performance.

The SVM controls the three phases together and is flexible in the selection of switching vectors from redundancy vectors. The implementation of SVM in abc-coordinates significantly reduces the computational complexity, easy to obtain the switching vectors and their dwell times, and extendable to higher number of voltage levels without any modifications. In SVM approach, the zero vectors are equally distributed, which results in output volt-

age with lowest harmonic distortion. Finally, a submodule capacitors voltage balancing approach with reduced current sensors is presented. This approach uses estimated arm current, which reduces the number of current sensors to 50% compared with the conventional balancing approach. The performance of balancing approach with estimated and direct measurement of arm current is presented. The results are very close in a relationship and thus validate the proposed methodology.

CHAPTER 4

MINIMIZATION OF SUBMODULE CAPACITORS VOLTAGE RIPPLE USING DIRECT MODEL PREDICTIVE CONTROL

MINIMIZATION of submodule (SM) capacitor voltage ripple is one of the main technical challenges in an MMC [84]. Low-frequency voltage ripple, particularly second and fourth-order harmonic ripple components, can be observed in submodule capacitor voltages. Capacitor voltage ripple generates the circulating current on the arm side with corresponding ripple frequency [42]. The circulating current increases the peak value of the arm current, thereby increasing the voltage stress on devices and introducing additional conduction losses [104]. These circulating currents are controlled using either proportional-integral (PI) or resonant regulators in classical control methods [90,108,111,117]. In direct model predictive control (D-MPC), the objective of circulating current control is included in a cost function [146–149]. The circulating current control ensures the voltage balancing between upper and lower arms and minimizes the ripple in submodule capacitors voltage as well.

In this chapter, a direct model predictive control without cost function is proposed to minimize the circulating currents and ripple in submodule ca-

pacitors voltage. To implement the proposed approach, a three-phase mathematical model of MMC in the discrete-time domain is presented. The proposed three-phase equivalent model of MMC includes the common-mode voltage (CMV), which minimizes the power fluctuations in the arm. Hence, the ripple in submodule capacitors voltage is reduced. The injected CMV also guarantees the voltage balancing between arms, minimizes the magnitude of circulating currents and eliminates the need for the cost function. During unbalanced operation, the injected CMV effectively minimizes the second harmonic fluctuations in DC-link current, considering that the DC-link voltage is stiff. The simulation and experimental studies are conducted on a laboratory prototype to validate the performance of proposed approach during balanced and unbalanced operating conditions.

4.1 Mathematical Modeling of 3L-FC Based MMC

For the digital implementation of direct model predictive control (D-MPC) approach, a discrete-time model of the MMC is required. The discrete-time (DT) model is obtained from the discretization of continuous-time (CT) model. In this Section, the continuous-time and discrete-time model of MMC connected to a passive load are presented.

The configuration of three-phase MMC connected to a simple passive load is shown in Figure 4.1. Each leg of MMC is composed of two arms, namely upper and lower ($y \in \{u, l\}$). Each arm consists of N-submodules in series with an inductor (L). The power losses in each arm are represented with an equivalent resistance (r). The DC system is represented by a split DC source of V_u and V_l, where $V_u = V_l = \frac{V_{dc}}{2}$. The DC source output is connected to the upper and lower DC bus bars of each leg in MMC through a DC-line. The DC-line is modeled as an inductor (L_{dc}) and a series resistance (r_{dc}). The passive load consists of an inductor (L_o) and a resistor (r_o) connected in between mid-point of each leg ($x \in \{a, b, c\}$) and neutral point (n), which forms a star configuration. The potential difference between the

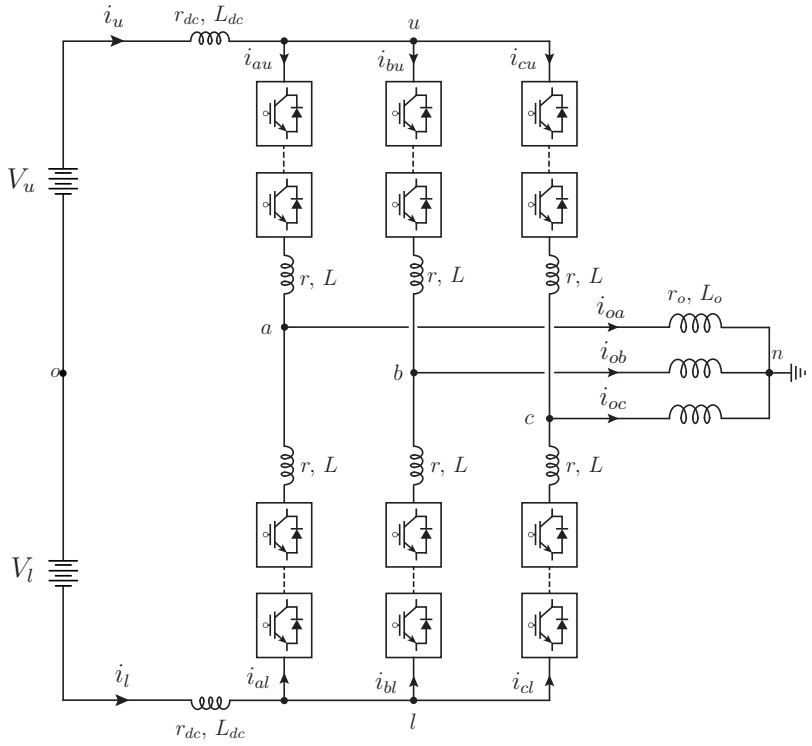


Figure 4.1. Three-phase MMC.

star point of passive load (n) and the mid-point of DC source (o) is considered in the modeling of MMC. The submodules in each arm are modeled as a controlled voltage source with a value equal to the sum of N submodule capacitor voltages as shown in Figure 4.2.

To analyze the dynamic behavior of the MMC, the arm current (i_{xy}) is decomposed into various current components, which includes the DC current component (i_s), AC output current (i_x), and AC circulating current (i_{xz}). From the equivalent model shown in Figure 4.2, the upper and lower arm current of phase-a is given by,

$$\begin{aligned} i_{au} &= i_a + i_s + i_{az} \\ i_{al} &= i_a - i_s - i_{az}. \end{aligned} \tag{4.1.1}$$

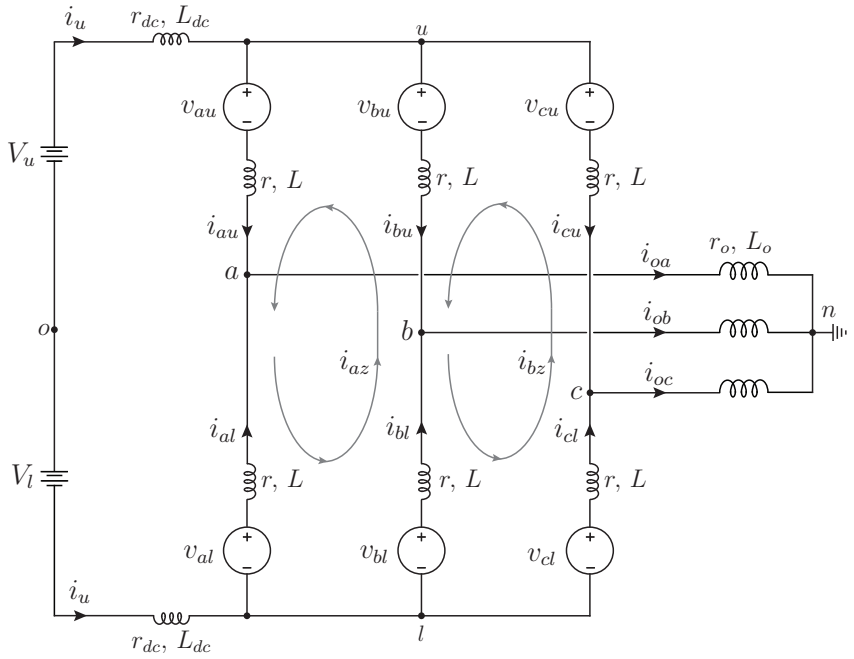


Figure 4.2. Equivalent model of MMC.

The current flowing through the upper and lower DC-link of MMC is given by

$$\begin{aligned} i_u &= i_{au} + i_{bu} + i_{cu} = 3\, i_s \\ i_l &= i_{al} + i_{bl} + i_{cl} = -3\, i_s. \end{aligned} \tag{4.1.2}$$

Similarly, the AC output current flowing through the phase-a of the passive load is formulated as follows:

$$i_{oa} = 2\, i_a. \tag{4.1.3}$$

From the equivalent model shown in Figure 4.2, the voltage equations of phase-a, upper and lower arms are given as,

$$\left.\begin{aligned} V_u &= L_{dc}\frac{d\, i_u}{dt} + r_{dc}\, i_u + v_{au} + L\frac{d\, i_{au}}{dt} + r\, i_{au} + L_o\frac{d\, i_{oa}}{dt} + r_o\, i_{oa} + v_{no} \\ -V_l &= L_{dc}\frac{d\, i_l}{dt} + r_{dc}\, i_l - v_{al} + L\frac{d\, i_{al}}{dt} + r\, i_{al} + L_o\frac{d\, i_{oa}}{dt} + r_o\, i_{oa} + v_{no}. \end{aligned}\right\} \tag{4.1.4}$$

Substraction of lower arm voltage in equation (4.1.4) from the upper arm voltage results in,

$$V_{dc} = L_{dc}\frac{d\,(i_u - i_l)}{dt} + r_{dc}\,(i_u - i_l) + v_{au} + v_{al} + L\frac{d\,(i_{au} - i_{al})}{dt} + r\,(i_{au} - i_{al}). \tag{4.1.5}$$

Similarly, the summation of phase-a, upper and lower arm voltages in equation (4.1.4) gives the following equation,

$$0 = L_{dc}\frac{d\,(i_u + i_l)}{dt} + r_{dc}\,(i_u + i_l) + v_{au} - v_{al} + L\frac{d\,(i_{au} + i_{al})}{dt} + r\,(i_{au} + i_{al}) + 2L_o\frac{d\,i_{oa}}{dt} + 2r_o\,i_{oa} + 2v_{no}. \tag{4.1.6}$$

4.1.1 Modeling of DC Current Component

The DC current component flows from the DC system through the converter legs, and its magnitude varies proportionally to the active power demanded by the load. From equation (4.1.2), the DC current component is given by

$$i_s = \frac{i_u - i_l}{6}. \tag{4.1.7}$$

The equations (4.1.1) and (4.1.7) are substituted in equation (4.1.5), which results in

$$V_{dc} = 6L_{dc}\frac{d\,i_s}{dt} + 6r_{dc}\,i_s + v_{au} + v_{al} + 2L\frac{d\,i_s}{dt} + 2r\,i_s + 2L\frac{d\,i_{az}}{dt} + 2r\,i_{az}. \tag{4.1.8}$$

Similarly, the phase-b and -c voltage equations are obtained as follows:

$$\left.\begin{aligned} V_{dc} &= 6L_{dc}\frac{d\,i_s}{dt} + 6r_{dc}\,i_s + v_{bu} + v_{bl} + 2L\frac{d\,i_s}{dt} + 2r\,i_s + 2L\frac{d\,i_{bz}}{dt} + 2r\,i_{bz} \\ V_{dc} &= 6L_{dc}\frac{d\,i_s}{dt} + 6r_{dc}\,i_s + v_{cu} + v_{cl} + 2L\frac{d\,i_s}{dt} + 2r\,i_s + 2L\frac{d\,i_{cz}}{dt} + 2r\,i_{cz}. \end{aligned}\right\} \tag{4.1.9}$$

The dynamic model of DC current component is obtained by adding the equations (4.1.8) and (4.1.9):

$$\frac{d\,i_s}{dt} = \frac{1}{3L_{dc}+L}\left[\frac{V_{dc}}{2} - \sum_{x=a,b,c}\frac{v_{xu}+v_{xl}}{6} - (3r_{dc}+r)\,i_s\right]. \tag{4.1.10}$$

The continuous-time model of DC current component given in equation (4.1.10) is transformed into discrete-time domain by using forward Euler approximation,

$$\begin{aligned}\frac{i_s^p(k+1)-i_s^m(k)}{T_s} = \frac{1}{3L_{dc}+L}&\left[\frac{V_{dc}^m}{2}(k) - \sum_{x=a,\,b,\,c}\frac{v_{xu}^p(k)+v_{xl}^p(k)}{6}\right]\\ &- \frac{3r_{dc}+r}{3L_{dc}+L}\,i_s^m(k).\end{aligned} \tag{4.1.11}$$

which is simplified and its equivalent discrete-time model is given by,

$$\begin{aligned}i_s^p(k+1) = \Gamma_s&\left[\frac{V_{dc}^m(k)}{2} - \sum_{x=a,b,c}\frac{v_{xu}^p(k)+v_{xl}^p(k)}{6}\right]\\ &+ \Phi_s\,i_s^m(k),\end{aligned} \tag{4.1.12}$$

where superscript "p" denotes the predicted variable, "m" denotes the measured variable, and T_s represents the sampling time. The discrete-time parameters are defined by,

$$\Gamma_s = \frac{T_s}{3L_{dc}+L}, \quad \Phi_s = 1 - \frac{(3r_{dc}+r)\,T_s}{3L_{dc}+L}. \tag{4.1.13}$$

4.1.2 Modeling of AC Circulating Current

The circulating current flows among the converter legs due to the difference between the upper and lower arm voltages. This current mainly consists of even order harmonic components corresponding to the multiples of twice the fundamental frequency. These circulating currents are controlled to achieve arm voltage balance, voltage ripple, and power loss reduction. The upper

and lower arm currents given in equation (4.1.1), are added together and formulated as,

$$i_{az} = \frac{i_{au} - i_{al}}{2} - i_s. \tag{4.1.14}$$

The dynamic model of phase-a, AC circulating current is obtained by solving the equations (4.1.8), (4.1.10), and (4.1.14) as follows:

$$\frac{d\, i_{az}}{dt} = \frac{1}{L}\left[\sum_{x=a,b,c} \frac{v_{xu} + v_{xl}}{6} - \frac{v_{au} + v_{al}}{2} - r\, i_{az}\right]. \tag{4.1.15}$$

From equation (4.1.15), the generalized representation of three-phase AC circulating currents is given by

$$\frac{d\, \mathbf{i_{xz}}}{dt} = \frac{1}{L}\left[\sum_{x=a,b,c} \frac{v_{xu} + v_{xl}}{6} - \frac{\mathbf{v_{xu}} + \mathbf{v_{xl}}}{2} - r\, \mathbf{i_{xz}}\right], \tag{4.1.16}$$

where,

$$\mathbf{i_{xz}} = \begin{bmatrix} i_{az} \\ i_{bz} \\ i_{cz} \end{bmatrix},\ \mathbf{v_{xu}} = \begin{bmatrix} v_{au} \\ v_{bu} \\ v_{cu} \end{bmatrix},\ \mathbf{v_{xl}} = \begin{bmatrix} v_{al} \\ v_{bl} \\ v_{cl} \end{bmatrix}. \tag{4.1.17}$$

With the forward Euler approximation, the discrete-time model of three-phase AC circulating currents is formulated as,

$$\begin{aligned} \mathbf{i^p_{xz}}(k+1) = \Gamma_z & \left[\sum_{x=a,b,c} \frac{v^p_{xu}(k) + v^p_{xl}(k)}{6} - \frac{\mathbf{v^p_{xu}}(k) + \mathbf{v^p_{xl}}(k)}{2}\right] \\ & + \Phi_z\, \mathbf{i^m_{xz}}(k), \end{aligned} \tag{4.1.18}$$

where,

$$\Gamma_z = \frac{T_s}{L}, \quad \Phi_z = 1 - \frac{r\, T_s}{L}. \tag{4.1.19}$$

4.1.3 Modeling of AC Output Current

The magnitude of DC current component equally flows among the three-phase, upper and lower arms. The three-phase arm currents are added together and results in,

$$i_u + i_l = 0. \tag{4.1.20}$$

The AC output current is equally distributed among the upper and lower arms. From equation (4.1.1), the magnitude of phase-a, AC output current is given by

$$i_a = \frac{i_{au} + i_{al}}{2}. \tag{4.1.21}$$

Substitution of equations (4.1.3), (4.1.20) and (4.1.21) into equation (4.1.6) results in,

$$v_{au} - v_{al} + 2L\,\frac{d\,i_a}{dt} + 2r\,i_a + 4L_o\,\frac{d\,i_a}{dt} + 4r_o\,i_a + 2v_{no} = 0. \tag{4.1.22}$$

Similarly, the phase-b and -c voltage equations are given by

$$\left.\begin{aligned} v_{bu} - v_{bl} + 2L\,\frac{d\,i_b}{dt} + 2r\,i_b + 4L_o\,\frac{d\,i_b}{dt} + 4r_o\,i_b + 2v_{no} = 0 \\ v_{cu} - v_{cl} + 2L\,\frac{d\,i_c}{dt} + 2r\,i_c + 4L_o\,\frac{d\,i_c}{dt} + 4r_o\,i_c + 2v_{no} = 0. \end{aligned}\right\} \tag{4.1.23}$$

From equations (4.1.22) and (4.1.23), the common-mode voltage (v_{no}) is given by:

$$v_{no} = \sum_{x=a,b,c} \frac{v_{xl} - v_{xu}}{6}. \tag{4.1.24}$$

The dynamic model of phase-a, AC output current is obtained by solving the equations (4.1.22), (4.1.23), and (4.1.24):

$$\frac{d\,i_a}{dt} = \frac{1}{L + 2L_o}\left[\frac{v_{al} - v_{au}}{2} - \underbrace{\sum_{x=a,b,c} \frac{v_{xl} - v_{xu}}{6}}_{\text{Common-Mode Voltage}} - (r + 2r_o)\,i_a\right]. \tag{4.1.25}$$

From equation (4.1.25), the generalized dynamic model of three-phase AC output current is developed as,

$$\frac{d\,\mathbf{i_x}}{dt} = \frac{1}{L + 2L_o}\left[\frac{\mathbf{v_{xl}} - \mathbf{v_{xu}}}{2} - \underbrace{\sum_{x=a,b,c} \frac{v_{xl} - v_{xu}}{6}}_{\text{Common-Mode Voltage}} - (r + 2r_o)\,\mathbf{i_x}\right]. \tag{4.1.26}$$

The continuous-time model given in equation (4.1.26) is transformed into the discrete-time domain using forward Euler approximation as follows:

$$\mathbf{i_x^p}(k+1) = \Gamma_o \left[\frac{\mathbf{v_{xl}^p}(k) - \mathbf{v_{xu}^p}(k)}{2} - \underbrace{\sum_{x=a,b,c} \frac{v_{xl}^p(k) - v_{xu}^p(k)}{6}}_{\text{Common-Mode Voltage}} \right] + \Phi_o \, \mathbf{i_x^m}(k), \tag{4.1.27}$$

where,

$$\Gamma_o = \frac{T_s}{L + 2L_o}, \quad \Phi_o = 1 - \frac{(r + 2r_o)\, T_s}{L + 2L_o}. \tag{4.1.28}$$

4.1.4 Modeling of Arm Voltage

The MMC is constructed using a three-level flying capacitor (3L-FC) submodule as shown in Figure 4.3. The 3L-FC submodule has two floating capacitors C_1 and C_2 with a voltage of v_{C1} and v_{C2}, respectively.

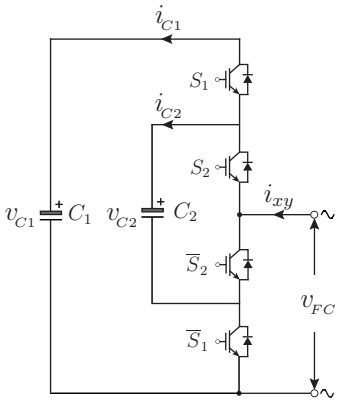


Figure 4.3. Flying capacitor submodule

The voltage equations of capacitor C_1 and C_2 in continuous-time are given as follows:

$$\left.\begin{aligned} v_{C1}(t) &= v_{C1}(0) + \frac{1}{C_1}\int_{0+}^{t} i_{C1}(\tau)\, d\tau \\ v_{C2}(t) &= v_{C2}(0) + \frac{1}{C_2}\int_{0+}^{t} i_{C2}(\tau)\, d\tau, \end{aligned}\right\} \tag{4.1.29}$$

where $v_{C1}(0)$ and $v_{C2}(0)$ represents the initial voltage of capacitors C_1 and C_2, respectively, i_{C1} and i_{C2} represents the current flowing through the capacitors C_1 and C_2, respectively. The voltage equations of capacitor C_1 and C_2 in discrete-time are given by,

$$\left.\begin{aligned} v^p_{C1}(k+1) &= v^m_{C1}(k) + \frac{T_s}{C_1} i^p_{C1}(k) \\ v^p_{C2}(k+1) &= v^m_{C2}(k) + \frac{T_s}{C_2} i^p_{C2}(k). \end{aligned}\right\} \tag{4.1.30}$$

The capacitors current in terms of switching states and arm current is given by,

$$\left.\begin{aligned} i^p_{C1}(k) &= S^p_1(k)\, i^m_{xy}(k) \\ i^p_{C2}(k) &= (S^p_2(k) - S^p_1(k))\, i^m_{xy}(k). \end{aligned}\right\} \tag{4.1.31}$$

The capacitor C_1 voltage is regulated at twice the value of capacitor C_2 voltage to generate three voltage levels at the output. The submodule output voltage is given by,

$$v^p_{SM1}(k) = S^p_1\, v^m_{C1}(k) + (S^p_2 - S^p_1)\, v^m_{C2}(k), \tag{4.1.32}$$

where $v^m_{C1}(k)$ and $v^m_{C2}(k)$ are the measured voltages.

Each arm consists of N-submodules. The summation of N-submodules output voltage gives the arm voltage,

$$v^p_{xy}(k) = v^p_{SM1}(k) + v^p_{SM2}(k) + \ldots + v^p_{SMN}(k). \tag{4.1.33}$$

4.2 Direct Model Predictive Control Approach

The direct model predictive control (D-MPC) is one of the predictive approach, which allows the simultaneous control of output current, circulating currents and submodule capacitor voltages in the modular multilevel converter (MMC). In conventional D-MPC approach, the control objectives of each phase are included in a cost function and optimized for 2^{2N} switching

states [148, 149]. In this approach, the circulating current control is required to minimize the ripple in submodule capacitors voltage and DC-link current, and voltage balancing between arms during balanced and unbalanced conditions. These objectives are achieved by using an approximate mathematical model in the implementation of conventional D-MPC. The approximate mathematical model significantly affects the performance of MMC.

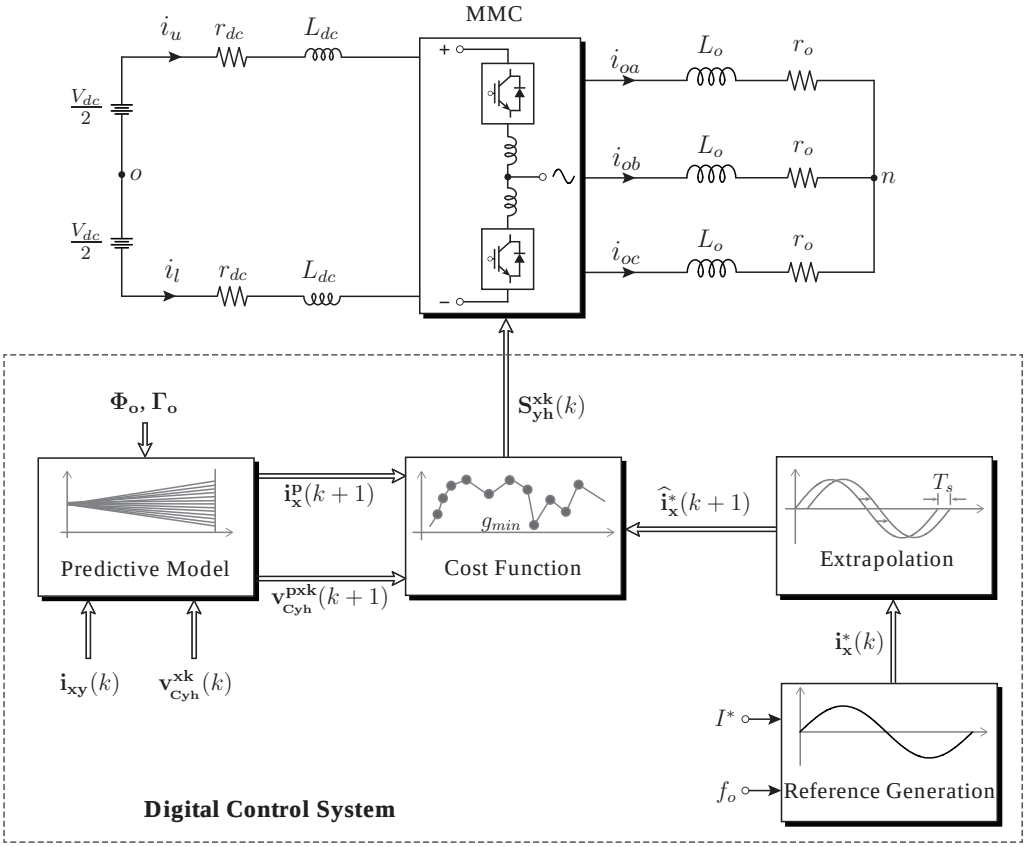


Figure 4.4. Block diagram of D-MPC with CMV injection.

The performance of D-MPC can be significantly improved by using an accurate mathematical model of MMC. The exact model includes the common-mode voltage (CMV), which minimizes the ripple in capacitors voltage and DC-link current, eliminates the cost function to control the circulating current and ensures the voltage balancing between arms. In D-MPC with CMV injection, the three-phase control objectives can be achieved using single cost

function. This approach has high computational complexity compared with the conventional D-MPC.

The block diagram of D-MPC for a simultaneous control of output current and submodule capacitor voltages in an MMC is shown in Figure 4.4. The three-phase reference output currents ($\mathbf{i}_{\mathbf{x}}^{*}(k)$) are generated with a required magnitude (I^{*}) and frequency (f_o). These currents are in alternating in nature and extrapolated to $(k+1)^{\text{th}}$-sampling instant using Lagrange extrapolation technique. Other hand, the submodule capacitors voltage are DC in nature. Hence, the extrapolation is not required for the DC signals. The reference output currents and capacitors voltage are included in a cost function. These reference signals are compared with the predicted signals. The output currents and submodule capacitors voltage are predicted to $(k+1)^{\text{th}}$-sampling instant using the system parameters, predicted voltages, and measured currents. Finally, the cost function is evaluated for all possible switching states. The switching state which minimizes the cost function is selected and applied to the converter. The implementation of D-MPC with CMV injection involves various steps, such as synthesis of feedback and reference signals, prediction of future behavior, optimization of cost function and selection of switching state. The step-by-step design procedure of D-MPC with CMV injection is presented in the following subsections.

4.2.1 Design Procedure

The design procedure of direct model predictive control (D-MPC) with CMV injection involves the following steps:

- **Measurement and Synthesis of Feedback Signals**

The three-phase output currents ($\mathbf{i_x}$), DC current component (i_s), and circulating currents ($\mathbf{i_{xy}}$) are synthesized from the measured upper ($\mathbf{i_{xu}}$) and lower arm currents ($\mathbf{i_{xl}}$) as follows:

$$\mathbf{i_x}(k) = \frac{\mathbf{i_{xu}}(k) + \mathbf{i_{xl}}(k)}{2} \tag{4.2.1}$$

and, the measured submodule capacitor voltages ($\mathbf{v}_{\mathbf{Cyh}}^{\mathbf{xk}}$) are used in the predictive block.

- **Calculation of Reference Currents**

The reference output currents are generated proportional to the required magnitude (I^*) and frequency (f_o). In the case of motor drive applications, the reference currents are obtained from the torque / speed and flux controllers [140, 166]. In grid-connected systems, the reference currents are obtained from the active and reactive powers demanded by the grid [139]. The reference output currents are defined as follows:

$$\mathbf{i}_{\mathbf{x}}^{*}(k) = I^{*}\, sin(2\pi f_o t + \theta_o) \tag{4.2.2}$$

where $\theta_o \in \left\{0, -\frac{2\pi}{3}, -\frac{4\pi}{3}\right\}$. The reference value of submodule outer and inner capacitors voltage is set to $\mathbf{V}_{\mathbf{C1}}^{*}(k) = V_{dc}/N$ and $\mathbf{V}_{\mathbf{C2}}^{*}(k) = V_{dc}/2N$, respectively.

- **Extrapolation of Reference Currents**

To minimize the steady-state tracking error, the sinusoidal reference output currents are extrapolated to $(k+1)^{\text{th}}$-sampling instant by using a third-order Lagrange extrapolation technique. The extrapolated reference currents are given by,

$$\widehat{\mathbf{i}_{\mathbf{x}}^{*}}(k+1) = 4\,\mathbf{i}_{\mathbf{x}}^{*}(k) - 6\,\mathbf{i}_{\mathbf{x}}^{*}(k-1) + 4\,\mathbf{i}_{\mathbf{x}}^{*}(k-2) - \mathbf{i}_{\mathbf{x}}^{*}(k-3) \tag{4.2.3}$$

whereas the submodule capacitors voltage is DC in nature. Therefore, the extrapolation of these signals are not required. The submodule capacitor voltages at $(k+1)^{\text{th}}$-sampling instant are equal to their values at $(k)^{\text{th}}$-sampling instant (i.e, $\mathbf{V}_{\mathbf{C1}}^{*}(k+1) = \mathbf{V}_{\mathbf{C1}}^{*}(k)$ and $\mathbf{V}_{\mathbf{C2}}^{*}(k+1) = \mathbf{V}_{\mathbf{C2}}^{*}(k)$).

- **Prediction of Future Behaviour of MMC**

By using the measured quantities and off-line computed system parameters, the future behavior of the output currents is predicted with the following discrete-time model:

$$\mathbf{i_x^p}(k+1) = \Gamma_o \left[\frac{\mathbf{v_{xl}^p}(k) - \mathbf{v_{xu}^p}(k)}{2} - \underbrace{\sum_{x=a,b,c} \frac{v_{xl}^p(k) - v_{xu}^p(k)}{6}}_{\text{Common-Mode Voltage}} \right] + \Phi_o \, \mathbf{i_x^m}(k), \tag{4.2.4}$$

where "p" denotes the predicted quantity and "m" denotes the measured quantity. These currents are expressed in terms of measured currents and predicted arm voltages. The predictive model of arm voltage is given by,

$$v_{xy}^p(k) = v_{SM1}^p(k) + v_{SM2}^p(k) + \ldots + v_{SMN}^p(k). \tag{4.2.5}$$

The predictive model of submodule output voltage is given by

$$v_{SM1}^p(k) = S_1^p \, v_{C1}^m(k) + (S_2^p - S_1^p) \, v_{C2}^m(k), \tag{4.2.6}$$

The predictive model of submodule outer and inner capacitors voltage is given by,

$$\left.\begin{aligned} v_{C1}^p(k+1) &= v_{C1}^m(k) + \frac{T_s}{C_1} i_{C1}^p(k) \\ v_{C2}^p(k+1) &= v_{C2}^m(k) + \frac{T_s}{C_2} i_{C2}^p(k). \end{aligned}\right\} \tag{4.2.7}$$

- **Minimization of Cost Function**

The converter cost function to meet the required goals is defined as follows:

$$\begin{aligned} g(k) = \lambda_o \, |\widehat{\mathbf{i}}_{\mathbf{x}}^*(k+1) - \mathbf{i_x^p}(k+1)| + \lambda_{c1} \, |\mathbf{V_{C1}^*}(k+1) - \mathbf{v_{Cy1}^{xk}}(k+1)| \\ + \lambda_{c2} \, |\mathbf{V_{C2}^*}(k+1) - \mathbf{v_{Cy2}^{xk}}(k+1)| \end{aligned} \tag{4.2.8}$$

The primary control objective is to force the actual output current to follow their reference and thus $\lambda_o = 1$. The weight factor λ_c is adjusted to achieve the desired response in secondary control objective. The value of λ_c is calculated using the per unit method. During each iteration, the cost function is evaluated over switching states of $3C_N^{2N}$. The optimal switching state which minimizes the cost function is selected and applied to the converter.

- **Calculation of Weighting Factors**

The weighting factors for the error terms given in Equation (4.2.8) are obtained by using the per-unit conversion method [145]. The current error term is divided by the rated reference current (I_B^*), and the capacitor voltage error terms are divided with the rated capacitor voltage (V_{C1}^* and V_{C2}^*). Finally, the overall cost function is multiplied with the rated reference current and given as follows:

$$g(k) = I_B^* \times \left[\frac{|\mathbf{i}_\mathbf{x}^*(k+1) - \mathbf{i}_\mathbf{x}(k+1)|}{I_B^*}\right] + I_B^* \times \left[\frac{|\mathbf{v}_{\mathbf{C1\_xy}}^*(k+1) - \mathbf{v}_{\mathbf{C1\_xy}}(k+1)|}{V_{C1}^*}\right] + I_B^* \times \left[\frac{|\mathbf{v}_{\mathbf{C2\_xy}}^*(k+1) - \mathbf{v}_{\mathbf{C2\_xy}}(k+1)|}{V_{C2}^*}\right]. \tag{4.2.9}$$

The weighting factors are obtained from Equations (4.2.8) and (4.2.9) as follows:

$$\lambda_o = \frac{I_B^*}{I_B^*},\ \lambda_{c1} = \frac{I_B^*}{V_{C1}^*},\ \lambda_{c2} = \frac{I_B^*}{V_{C2}^*}. \tag{4.2.10}$$

4.2.2 Control Algorithm

The flowchart of a direct model predictive control algorithm for MMC is shown in Figure 4.5. The arm currents and submodule capacitor voltages are measured in block ①. The $(k+1)^{\text{th}}$-sampling instant reference output currents and weight factors λ_o, λ_c are calculated in ②. The iterative loop is

performed between the blocks ④ and ⑨. In blocks ⑤ to ⑧, the MMC arm voltages $\mathbf{v}^{\mathbf{p}}_{\mathbf{xy}}[j](k)$, output currents $\mathbf{i}^{\mathbf{p}}_{\mathbf{x}}[j](k+1)$, and submodule capacitor voltages $\mathbf{v}^{\mathbf{pxk}}_{\mathbf{Cyh}}$-$(k+1)$ are predicted, and minimization of cost function $g[j](k)$ is performed for all $3C_N^{2N}$ possible switching states. An optimal switching state j_{op},

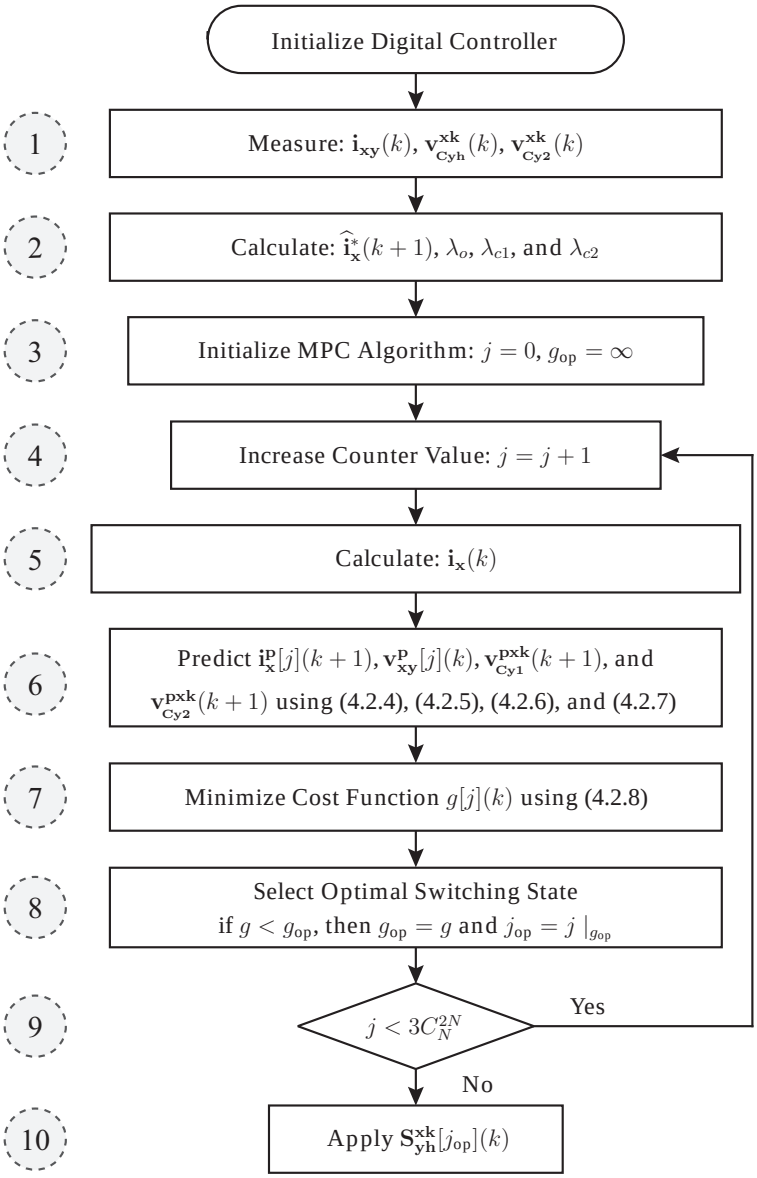


Figure 4.5. Flowchart of direct model predictive control.

and corresponding switching signals are selected and applied directly to the MMC in blocks ⑧ to ⑩. With direct model predictive control approach, the simultaneous control of output current and submodule capacitor voltages are achieved.

4.3 Dynamic and Steady-State Performance Analysis of D-MPC

The performance of proposed MPC scheme with CMV injection is verified on a three-phase MMC system with 3L-FC submodules. In this study, the DC system is replaced with an ideal DC source of V_{dc}=7.354 kV, in series with an inductor. The MMC consists of two 3L-FC submodules in each leg, and each submodule has two floating capacitors with a nominal voltage of V_{C1}=3.677 kV and V_{C2}=1.838 kV. The AC system is represented with a simple three-phase passive load of 4.16 kV / 5 MVA rated capacity.

4.3.1 Performance of D-MPC With and Without CMV Injection

The performance of MPC with CMV injection is shown in Figure 4.6. In this study, the objective of output current and submodule capacitors voltage control is included in the cost function. The MMC supplies a constant current of 0.6 pu at an operating frequency of 60 Hz to the load, as shown in Figure 4.6(a). From t=0 s to t=0.05 s, the third-order harmonic CMV is injected into the system as shown in Figure 4.6(b). With CMV injection, the upper and lower arm submodule capacitors voltage is maintained at identical average value as shown in Figure 4.6(c)-(d). In addition, the second-order harmonic ripple in submodule capacitors voltage is significantly minimized. The magnitude of circulating current is significantly reduced with CMV injection as shown in Figure 4.7(a). The magnitude of upper and lower arm current of phase-a is less than the rated value, as shown in Figure 4.7(b). Hence, the device voltage stress and power losses are within the nominal range. The output voltage levels are symmetrically distributed, which minimizes the

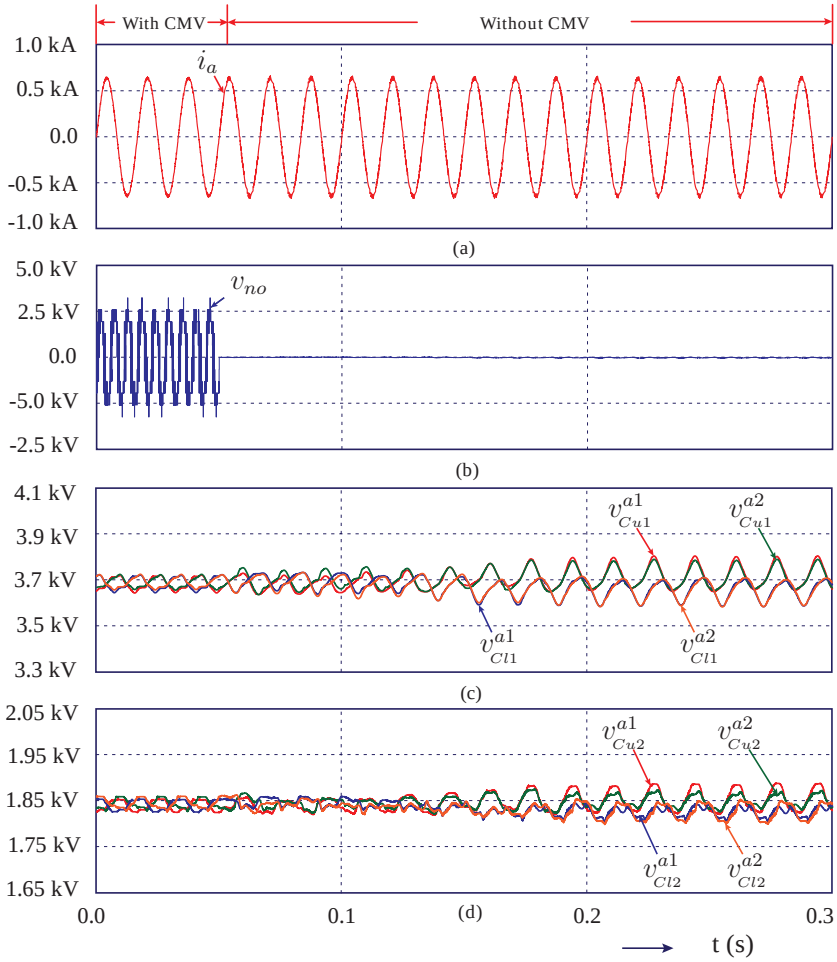


Figure 4.6. Steady-state performance of MPC with CMV injection: (a) phase-a output current, (b) CMV, (c) upper and lower arm submodules capacitor C_1 voltage in phase-a, and (iv) upper and lower arm submodules capacitor C_2 voltage in phase-a

harmonic distortion as shown in Figure 4.7(c).

At t=0.05 s, the CMV is forced to zero as shown in Figure 4.6(b). Hence, the upper and lower arm submodule capacitors voltage slowly diverging from their nominal value and settled at different average values as shown in Figure 4.6(c)-(d). This difference in arm voltages causes large circulating currents among the legs as shown in Figure 4.7(a). In addition, the ripple in

submodule capacitors voltage and RMS value of arm currents exceed their nominal value as shown in Figure 4.7(b). The output voltage has additional voltage levels caused by the unwanted switching actions as shown in Figure 4.7(c).

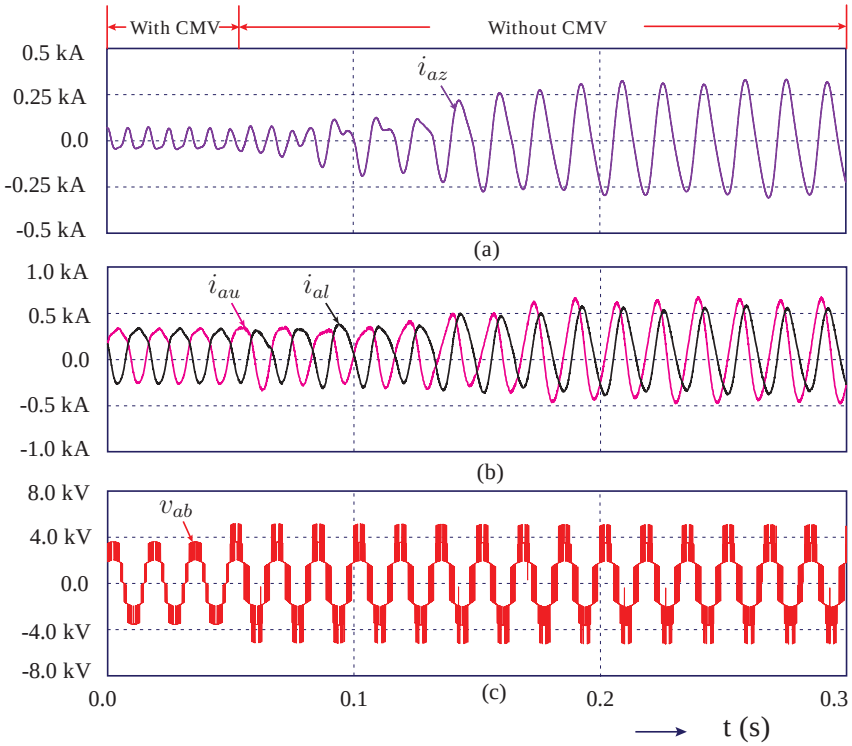


Figure 4.7. Steady-state performance of MPC with CMV injection: (a) phase-a circulating current, (b) upper and lower arm current of phase-a, and (c) output voltage

The performance of MPC with and without CMV injection is summarized in Table 4.1. The performance assessment parameters $\%V_{THD}$, $\%I_{THD}$, the peak-peak voltage ripple of V_{C1} and V_{C2}, the peak-peak value of circulating current (CC) and the peak value of CMV are considered. The voltage and current harmonic distortions are reduced by 40.51% and 44.07% with CMV injection, respectively. The capacitor C_1 and C_2 voltage ripples (p-p) are reduced by 51.22% and 21.43%, respectively. The magnitude of the circulating current is reduced by 81.25% compared with the base case (without CMV

injection). However, the increase in CMV causes voltage stress on winding insulation in case of motor drives.

Table 4.1. Simulation analysis of MPC with and without CMV

Performance Indices	Without CMV	With CMV
V_{THD}	41.20%	24.51%
I_{THD}	2.70%	1.51%
V_{C1} Ripple (p-p)	123 V	60 V
V_{C2} Ripple (p-p)	42 V	33 V
CC (p-p)	720 A	135 A
CMV (peak)	0 V	2450 V

4.3.2 Comparison of Conventional D-MPC and D-MPC With CMV Injection

The performance of the proposed MPC with CMV injection is compared with that of the conventional MPC. In conventional MPC approach, CMV is not included in the discrete-time model of the output current and demonstrated with the following model [146–148]:

$$\mathbf{i_x^p}(k+1) = \Gamma_o[\frac{\mathbf{v_{xl}^p}(k) - \mathbf{v_{xu}^p}(k)}{2}] + \Phi_o\,\mathbf{i_x^m}(k). \tag{4.3.1}$$

The dynamic performance of conventional MPC approach is shown in Figure 4.8 and Figure 4.9. The converter is controlled to supply a current magnitude of 0.4 pu to the load. At t = 0.05 s, the magnitude of the reference output current is changed from 0.4 pu to 0.8 pu. The actual output currents perfectly following their reference currents, as shown in Figure 4.8(a). However, the output voltage waveform has multiple changes in the voltage steps (i.e., unwanted additional switchings of submodules), which increases

the harmonic distortion and device switching frequency as shown in Figure 4.8(b). The MMC CMV mainly consists of switching ripples with a peak value of 600 V as shown in Figure 4.8(c).

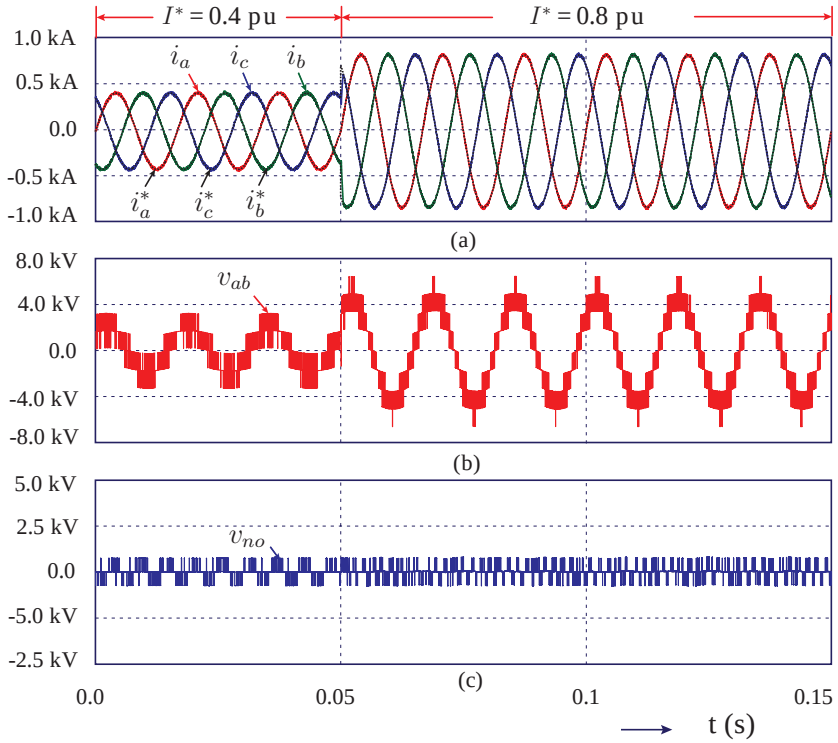


Figure 4.8. Dynamic performance of conventional MPC: (a) three-phase output currents, (b) output voltage, and (c) CMV

Given that the CMV is not included in the discrete-time model of the conventional MPC approach, the control does not have any effect on voltage ripple and circulating current reduction. The upper and lower arm submodule capacitors C_1 and C_2 voltage from phase-a are shown in Figure 4.9(a)-(b). The submodule capacitors voltage in the same arm is perfectly balanced. However, the charging and discharging of upper and lower arm submodule capacitors are not identical. The difference in the upper and lower arm submodule capacitors voltage causes phase circulating currents as shown in Figure 4.9(c). The phase circulating current increases the submodule capacitor voltage ripple and the peak value of arm current as shown in Figure 4.9(d).

It further increases the device voltage stress and power losses as well.

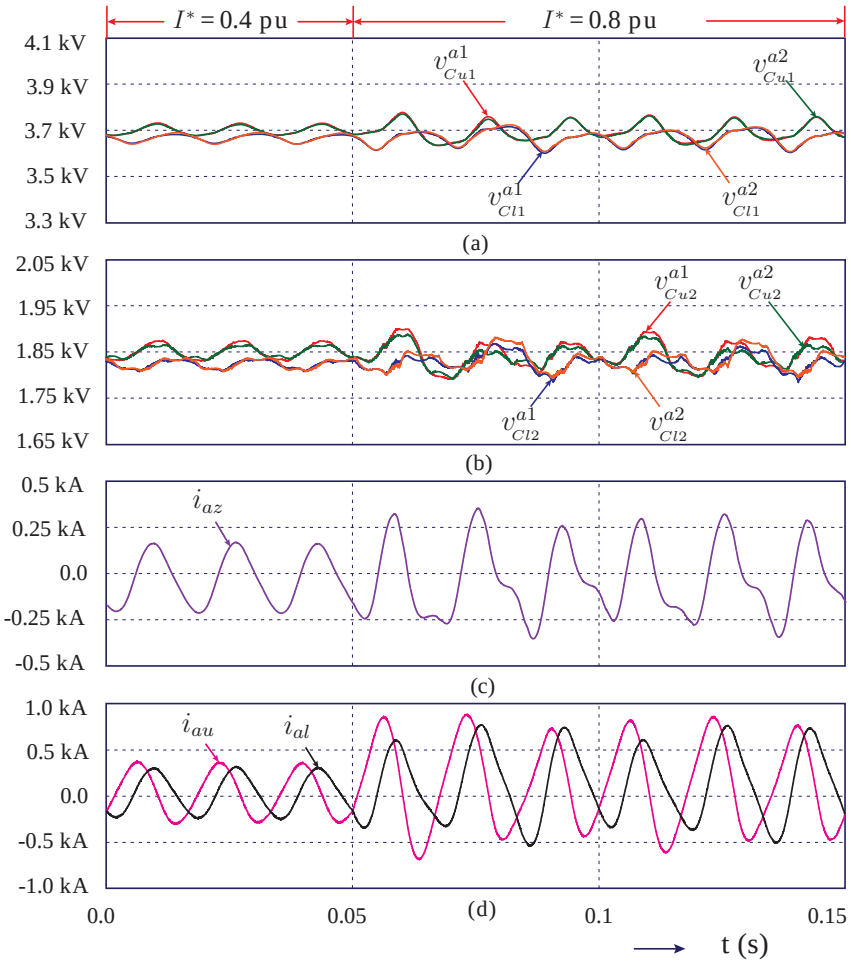


Figure 4.9. Dynamic performance of conventional MPC: (a) upper and lower arm submodules capacitor C_1 voltage in phase-a, (b) upper and lower arm submodules capacitor C_2 voltage in phase-a, (c) upper and lower arm current of phase-a, and (d) phase-a circulating current

In proposed MPC approach, the CMV is included in the discrete-time model of MMC given in equation (4.1.27). The dynamic performance of proposed MPC with CMV is shown in Figure 4.10 and 4.11. The actual output currents are perfectly following the reference currents as shown in Figure 4.10(a). The output voltage levels are symmetrically distributed as shown

Figure 4.10(b), which reduces the output voltage harmonic distortion significantly. The peak value of CMV generated by the MMC is approximately 35% of the total DC-link voltage shown in Figure 4.10(c). The upper and lower arm submodule capacitors C_1 and C_2 voltage from phase-a are maintained at 3.677 kV and 1.838 kV, respectively as shown in Figure 4.11(a)-(b). The magnitude of circulating current and the peak value of the arm current are reduced, as shown in Figure 4.11(c)-(d).

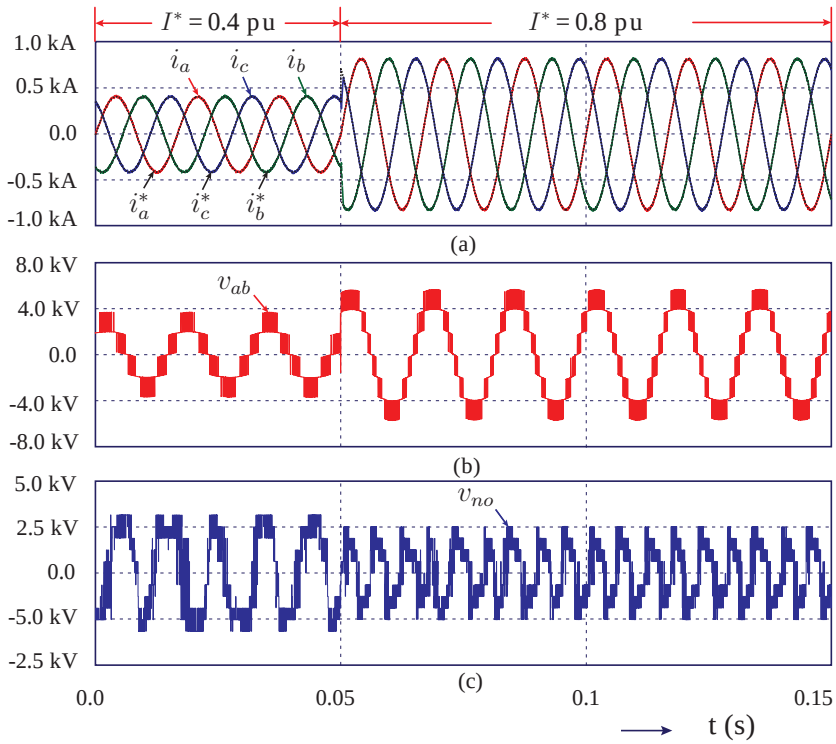


Figure 4.10. Dynamic performance of MPC with CMV: (a) three-phase output currents, (b) output voltage, and (c) CMV

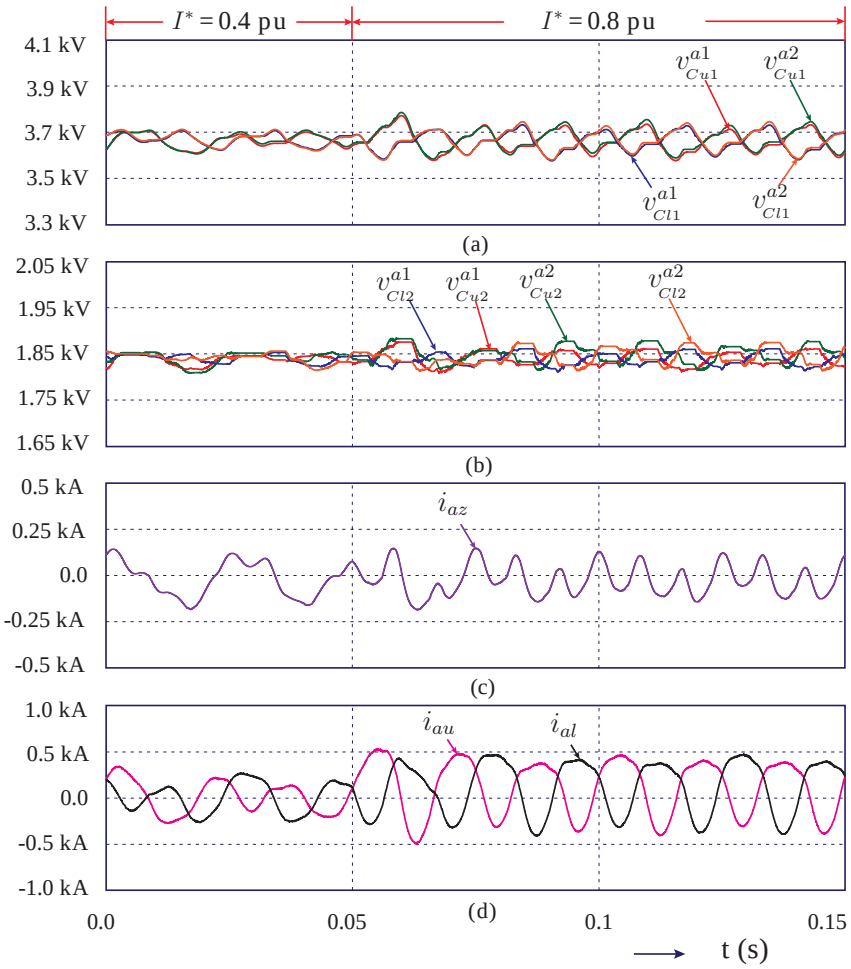


Figure 4.11. Dynamic performance of MPC with CMV: (a) upper and lower arm submodules capacitor C_1 voltage in phase-a, (b) upper and lower arm submodules capacitor C_2 voltage in phase-a, (c) upper and lower arm current of phase-a, and (d) phase-a circulating current

The performance of conventional and proposed MPC approaches is summarized in Table 4.2. With proposed MPC approach, the voltage and current harmonic distortion are reduced by 30% and 23.9%, respectively. The peak-peak value of capacitor C_1 and C_2 voltage ripple is reduced by 35.8% and 13.78%, respectively. A significant reduction of 69.28% also exists in the peak-peak value of the circulating current compared with the conventional

MPC approach. Overall, the proposed MPC with CMV injection improves the performance of MMC.

Table 4.2. Simulation analysis of conventional MPC and MPC with CMV

Performance Indices	Conventional MPC Approach	Proposed MPC Approach
V_{THD}	29.61%	20.54%
I_{THD}	1.38%	1.05%
V_{C1} Ripple (p-p)	162 V	104 V
V_{C2} Ripple (p-p)	58 V	50 V
CC (p-p)	700 A	215 A
CMV (peak)	600 V	2450 V

4.3.3 DC-link Current Ripple During Unbalanced Operation

The performance of conventional MPC during unbalanced operation is shown in Figure 4.12, where the phase-a and -c reference currents are generated with a peak value of 0.6 pu and frequency of 60 Hz. The phase-b reference current is generated with 20% unbalance in the magnitude as that of other phases. The actual output currents perfectly follow their reference currents as shown in Figure 4.12(a). The unbalanced operation generates asymmetrical AC circulating currents, which leads to asymmetrical nature of arm currents as shown in Figure 4.12(b). The AC circulating current consists of zero sequence current components along with the positive and negative sequence components as shown in Figure 4.12(c). The zero sequence circulating current at twice the fundamental frequency flows through the DC-link and causes a significant ripple in DC-link current as shown in Figure 4.12(d). The DC-bus current has a second order harmonic component of 59.31 A along with the DC current component. The ripple in DC-link current increases the magnitude of arm currents and thereby, the converter power losses.

The performance of proposed MPC with CMV is shown in Figure 4.13, under identical operating conditions as that of conventional MPC. The pro-

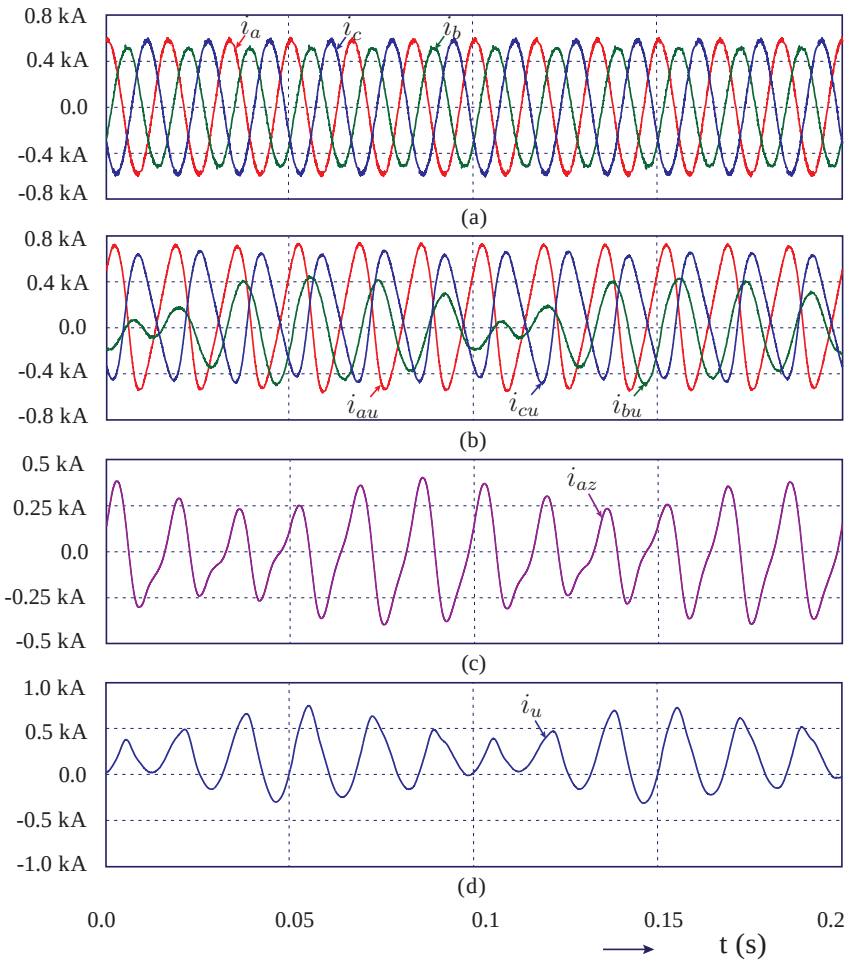


Figure 4.12. Unbalanced operation of conventional MPC: (a) three-phase output currents, (b) three-phase upper arm currents, (c) dc-link current, and (d) phase-a circulating current

posed approach uses the discrete-time model given in equation (4.1.27), which consists of CMV in the AC output current model. The proposed approach generates a CMV along with the fundamental voltage across the arm. The fundamental voltage forces the fundamental frequency current component corresponding to the reference current as shown in Figure 4.13(a). The CMV consists of third-harmonic voltage component, which generates third-harmonic current component. The third-harmonic voltage and current component

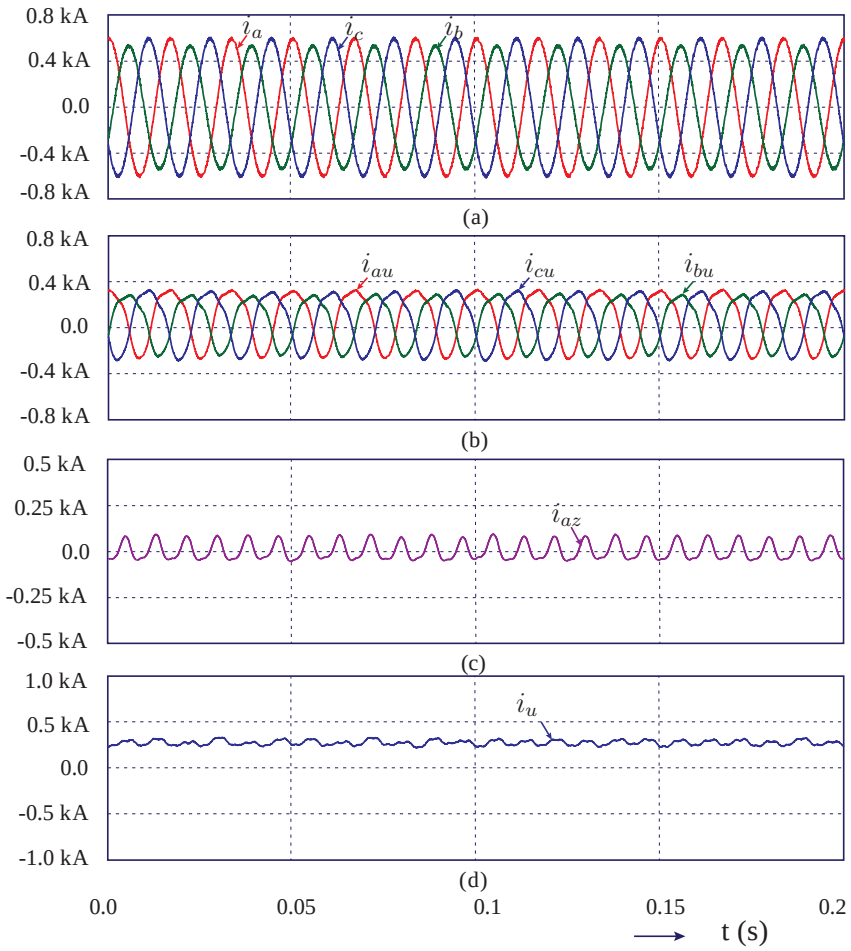


Figure 4.13. Unbalanced operation of MPC with CMV: (a) three-phase output currents, (b) three-phase upper arm currents, (c) dc-link current, and (d) phase-a circulating current

ensures the internal balance between the converter legs. The three-phase arm currents identical in nature except for a minor difference in the magnitude as shown in Figure 4.13(b). Therefore, the magnitude of AC circulating currents is within the nominal range as shown in Figure 4.13(c). In addition, the injected CMV reduces the ripple in DC-link current as shown in Figure 4.13(d). The DC-link current has a second harmonic component of 16.71 A, which is reduced by 71.8% in comparison to the conventional MPC.

4.4 Experimental Validation

The performance of the proposed MPC approach is verified on a 3L-FC-based MMC laboratory prototype with a 3 kVA / 208 V rated capacity. Each arm consists of single 3L-FC submodule with two floating capacitors. The capacitor C_1 is rated for 360 V and C_2 for 180 V.

4.4.1 Submodule Capacitors Voltage Ripple and Circulating Currents

The experimental verification of proposed MPC with CMV injection is shown in Figure 4.14. From t=0 s to t=0.08 s, a CMV of 105 V (peak) is injected into the system. The injection of CMV minimizes the magnitude of the circulating current. In particular, the current component that corresponds to twice the output frequency is minimized. At t=0.08 s, the CMV is forced to zero, as shown in Figure 4.14(a), which increases the magnitude of arm currents and corresponding circulating current component. The increase in arm current magnitude contributes to the additional power losses, which deteriorates the MMC efficiency.

In phase-a, the upper and lower arm submodule-1 capacitors C_1 and C_2 voltage are shown in Figure 4.14(b). The capacitors C_1 and C_2 voltage are perfectly maintained at 360 V and 180 V, respectively. However, capacitor C_1 and C_2 voltage ripples are increased without CMV, as shown in Figure 4.14(c). The output voltage and the current waveforms are shown in Figure 4.14(d). The actual output current perfectly following their reference current. The voltage steps in output voltage are perfectly clamped with CMV injection into the system.

The performance of comparison is summarized in Table 4.3. The output voltage and current harmonic distortion are reduced by 46.95% and 41.58%, respectively, through CMV injection. Capacitor C_1 and C_2 voltage ripples (peak-peak) are reduced by 25% and 46.15%, respectively. The magnitude of the circulating current (peak-peak) is reduced by 40.82%.

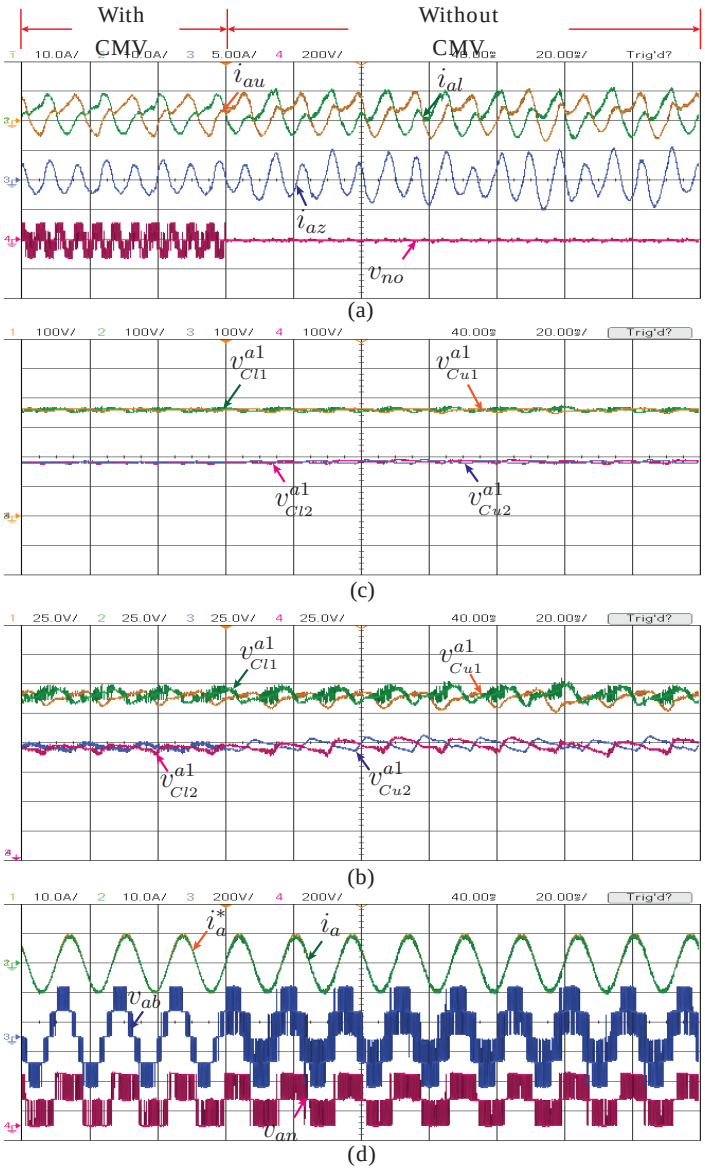


Figure 4.14. Performance of MPC with and without CMV injection: (a) upper, lower arm, circulating currents and CMV, (b) ripple in upper and lower arm submodule capacitors voltage, (c) upper and lower arm submodule capacitors voltage, and (d) output line voltage, phase voltage and output current

Table 4.3. Experimental analysis of MPC with and without CMV

Performance Indices	Without CMV	With CMV
V_{THD}	68.69%	36.44%
I_{THD}	7.07%	4.13%
V_{C1} Ripple (p-p)	16 V	12 V
V_{C2} Ripple (p-p)	13 V	7 V
CC (p-p)	9.8 A	5.6 A
CMV (peak)	0 V	105 V

4.4.2 Comparison of Conventional and Proposed D-MPC

A comparison between the conventional and proposed approaches are presented in Figure 4.15 and Figure 4.16, respectively. The dynamic performance of conventional D-MPC is shown in Figure 4.15, where the step change in the reference current 5 A to 10 A is applied. The actual output current follows the reference current. However, the output voltage levels are not symmetrically distributed. The controller chooses the switching state that has multiple changes in voltage levels to achieve the perfect current tracking, as shown in Figure 4.15(a).

The arm voltage has three levels with a peak value of 360 V. The upper and lower arm submodule capacitors voltage is perfectly balanced at full-load condition. A DC-offset voltage exists between the upper and lower arm capacitors voltage at the light-load condition as shown in Figure 4.15(b). The magnitude of arm current and circulating current is proportionally increased with the reference current as shown in Figure 4.15(c). The circulating current has dominant second-order harmonic current component, which increases the RMS value of arm current. With conventional D-MPC, the MMC generates a CMV of 60 V (peak) and does not have any effect on the converter performance as shown in Figure 4.15(c).

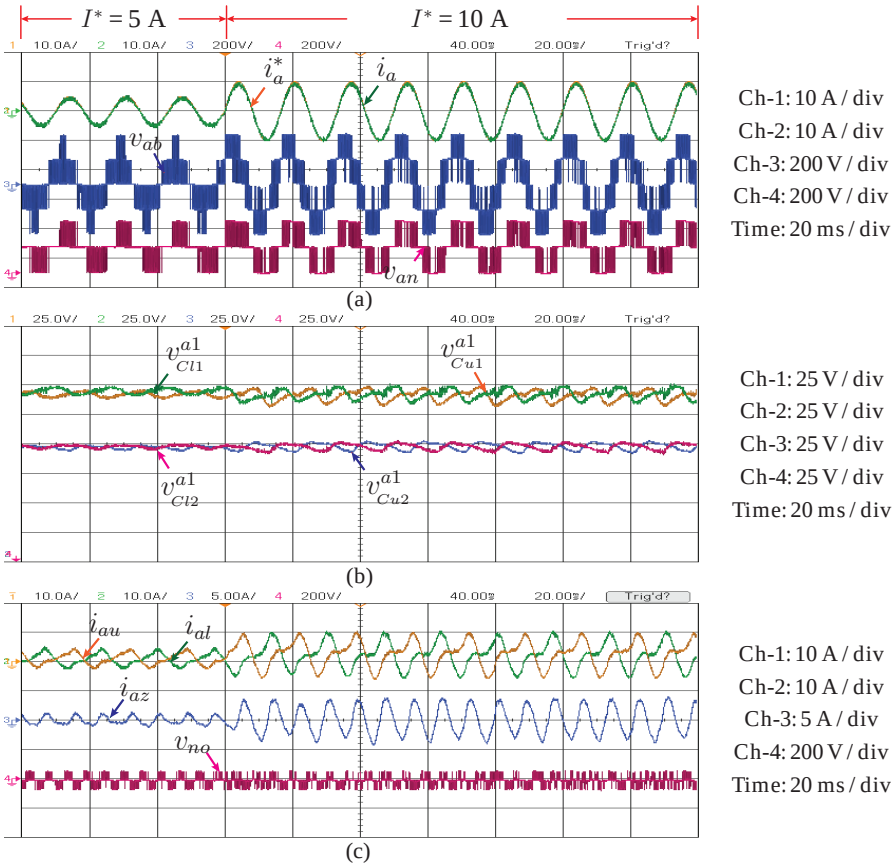


Figure 4.15. Dynamic performance of conventional MPC: (a) output line voltage, phase voltage, and output current, (b) ripple in upper and lower arm submodule capacitors voltage and (c) upper, lower arm, circulating currents, and CMV

The dynamic performance of proposed D-MPC with CMV is shown in Figure 4.16. The actual output current perfectly following their reference current during external disturbance as well. The output voltage levels are symmetrically distributed and improve the output voltage waveform quality and harmonic distortion, as shown in Figure 4.16(a). The upper and lower arm submodule capacitors voltage is perfectly balanced in the entire operating region. The capacitor voltage ripple and peak value of the circulating current are also minimized compared with those of conventional D-MPC as shown in Figure 4.16(b)-(c). In this approach, the CMV of 105 V (peak) is

injected into the system as shown in Figure 4.16(c).

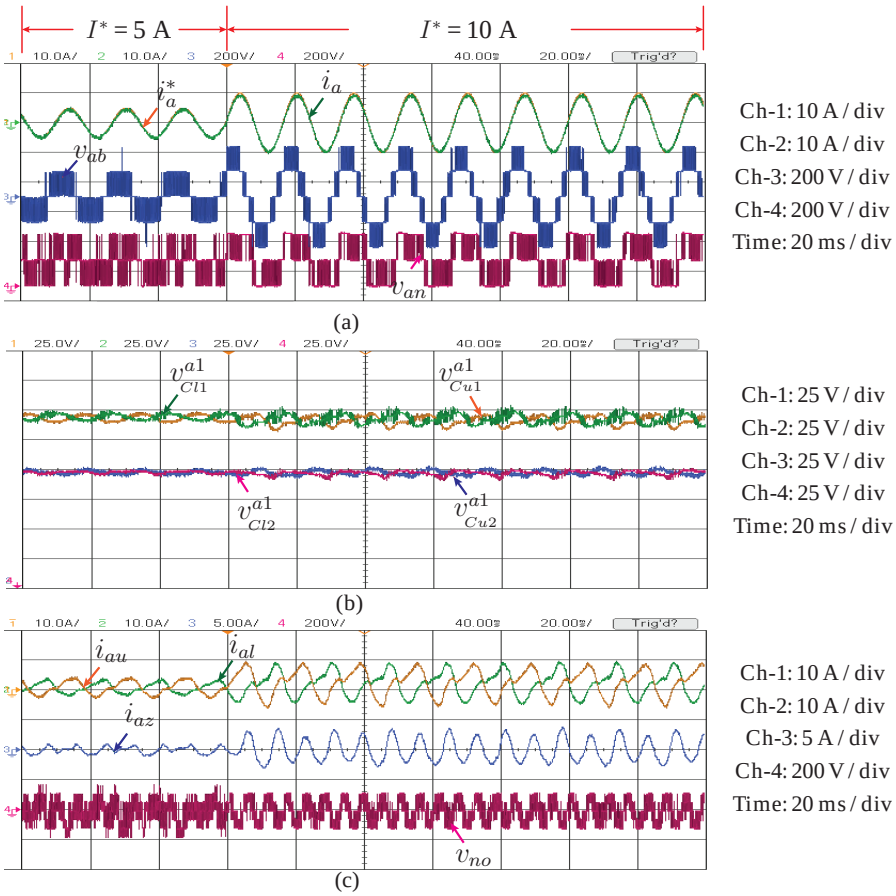


Figure 4.16. Dynamic performance of MPC with CMV injection: (a) output line voltage, phase voltage and output current, (b) ripple in upper and lower arm submodule capacitors voltage, and (c) upper, lower arm, circulating currents and CMV

A comparison between the conventional and proposed MPC approaches are summarized in Table 4.4. The proposed approach reduces the output voltage and current harmonic distortion by 37.83% and 27.79%, respectively. Capacitor C_1 and C_2 voltage ripples are reduced by 20% and 22.22%, respectively. The magnitude of circulating current (peak-peak) is reduced by 23.81%. The simulation and experimental results have a close relationship. Thus, the proposed methodology is validated.

Table 4.4. Experimental analysis of conventional and proposed D-MPC

Performance Indices	Conventional MPC Approach	Proposed MPC Approach
V_{THD}	58.62%	36.44%
I_{THD}	5.72%	4.13%
V_{C1} Ripple (p-p)	15 V	12 V
V_{C2} Ripple (p-p)	9 V	7 V
CC (p-p)	7.35 A	5.6 A
CMV (peak)	60 V	105 V

4.4.3 DC-link Current Ripple During Unbalanced Operation

The simulation study is validated on a dSPACE-DS1103 based MMC laboratory prototype. Each converter leg has two 3L-FC submodules with a nominal voltage of V_{C1}=360 V and V_{C2}=180 V. The phase-b and -c reference currents are generated for a peak value of 10 A and frequency of 60 Hz. The phase-a reference current is generated with a 20% unbalance in magnitude. With conventional MPC, the actual currents follow their reference currents as shown in Figure 4.17(a). These currents are non-sinusoidal in nature with a harmonic distortion of 4.71%. The unbalanced operation causes zero sequence circulating currents, which flows through the DC-link and converter legs. The DC-link current has a second harmonic component of 0.65 A, which increases the ripple in DC-link current and distortion in arm currents as shown in Figure 4.17(b). The submodule outer and inner capacitors voltage is maintained at 360 V and 180 V, respectively. These capacitors have a peak-peak ripple of 10 V and 8.5 V, respectively.

Due to the zero sequence currents, the charging and discharging of submodule capacitors in upper and lower arms are not in symmetry as shown in Figure 4.17(c). The difference in upper and lower arm voltage causes negative sequence circulating current, which flows among the converter legs. The phase-a circulating current (includes zero, negative and positive sequence

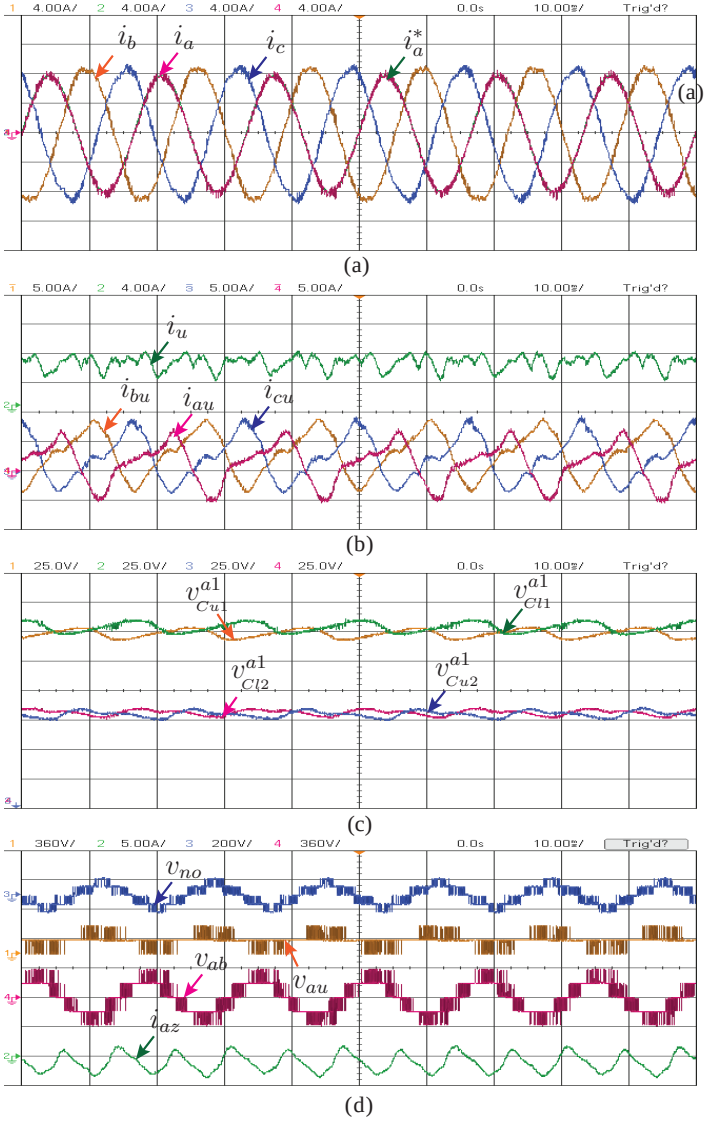


Figure 4.17. Performance of conventional MPC during unbalanced conditions: (a) three-phase line currents, (b) three-phase upper arm and DC-link current, (c) upper and lower arm submodule capacitors voltage, and (d) output line voltage, upper arm voltage, CMV and circulating current

components) has a peak-peak value of 5.35 A. The conventional MPC approach generates only fundamental frequency voltage across the arms as shown in Figure 4.17(d). Therefore, the zero sequence currents can not be

controlled with this approach. The output line voltage has a harmonic distortion of 38.27%. The voltage across the terminals n and o is 360 V.

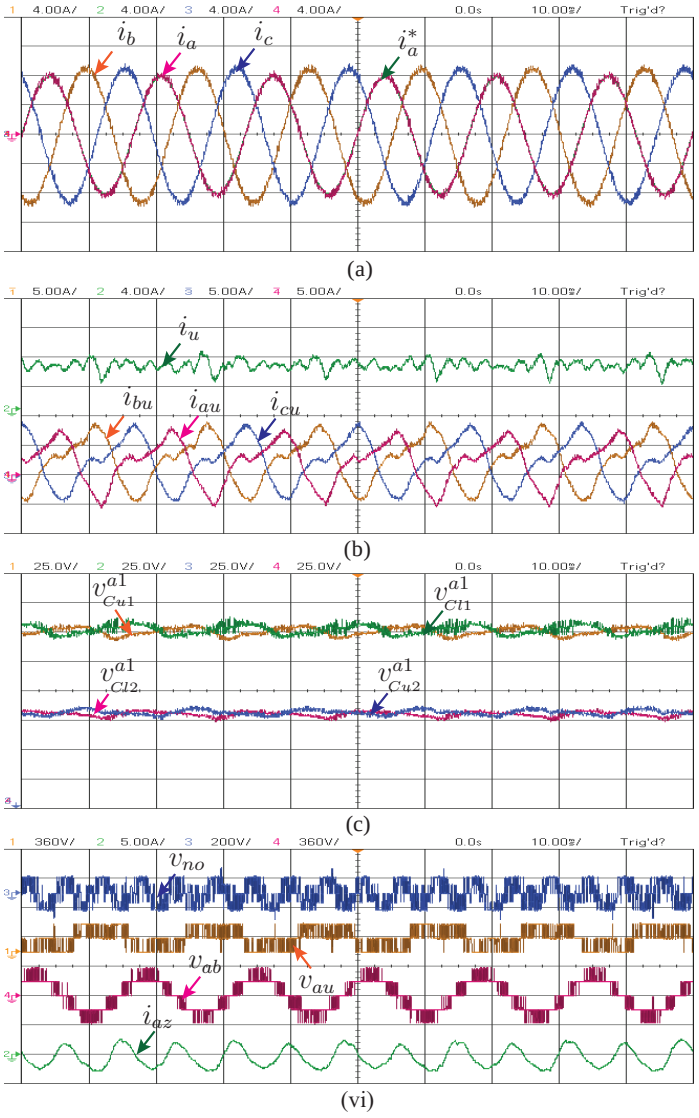


Figure 4.18. Performance of MPC with CMV during unbalanced conditions: (a) three-phase line currents, (b) three-phase upper arm, and DC-link current, (c) upper and lower arm submodule capacitors voltage, and (d) output line voltage, upper arm voltage, CMV, and circulating current

The performance of proposed approach is presented in Figure 4.18, with the above operating conditions. The proposed D-MPC perfectly generates three-phase sinusoidal currents with a harmonic distortion of 3.74% as shown in Figure 4.18(a), which is 20.59% smaller than that of the conventional D-MPC. The proposed approach reduces the ripple in DC-link current (mainly second harmonic zero sequence component) by 61.54% as shown in Figure 4.18(b), which further minimizes the distortion in arm currents. In addition, the submodule capacitors voltage in upper and lower arms are perfectly regulated at their nominal value as shown in Figure 4.18(c). The outer and inner capacitor voltage have a peak-peak ripple of 8.5 V and 6 V, respectively. This approach ensures the symmetrical charging and discharging of submodule capacitors in upper and lower arms. Therefore, the magnitude of negative sequence circulating currents can be reduced. The circulating current has a peak-peak value of 4.4 A as shown in Figure 4.18(d), which is 17.75% smaller than that of the conventional D-MPC. The proposed approach generates a voltage waveform across the arm corresponding to the fundamental and zero sequence currents as shown in Figure 4.18(d). The converter generated common-mode voltage appears across the terminals n and o. The CMV has a peak-peak value of 360 V. The inclusion of CMV in the output current model reduces the output line voltage harmonic distortion by 12.75%.

4.5 Summary

In this chapter, a direct model predictive control is proposed to minimize the magnitude of circulating currents and ripple in submodule capacitors voltage during balanced operating conditions. To implement the proposed approach, a generic three-phase mathematical model of the MMC is developed. The proposed model includes the CMV and can be applied to any MMC structure with minor modifications. The inclusion of CMV helps to achieve the voltage balancing between arms without using the cost function. In addition, the DC-link current ripple is minimized during unbalanced operating conditions. The simulation and experimental studies are presented to

validate the performance of proposed MPC with CMV injection under balanced and unbalanced conditions. Finally, the performance of proposed D-MPC is compared with the conventional D-MPC. The results show that the injection CMV minimizes the output voltage and current harmonic distortion, and current ripple along with other control objectives such as output current and submodule capacitors voltage control are successfully achieved.

CHAPTER 5

REDUCED COMPUTATIONAL MODEL PREDICTIVE CONTROL APPROACHES

THE computational complexity is one of the major issues in the implementation of model predictive control (MPC) for modular multilevel converters (MMCs). The conventional direct model predictive control (D-MPC) considers the per-phase model of MMC (approximate model) in the implementation, which significantly influences the converter performance. To reduce the computational burden of D-MPC, each phase of MMC is independently controlled using a per-phase D-MPC strategy. The per-phase D-MPC approach requires only C_N^{2N} switching states to optimize the cost function (where C represents the number of combinations) [42].

In this chapter, a novel reduced computational model predictive control approaches are proposed for MMC. The first approach is dual-stage direct model predictive approach, in which the control objectives are achieved in two stages using two cost functions. The first stage is designed to control the output and circulating currents in MMC. In this stage, the three phases are controlled together using three-phase predictive algorithm. In the second stage, the submodule capacitors voltage is controlled using a cost function. This approach reduces the voltage harmonic distortion and current ripple along with the computational complexity compared with the conven-

tional D-MPC. The dynamic and steady-state performance of dual-stage D-MPC approach is experimentally validated on a half-bridge based MMC system. The performance comparison of dual-stage D-MPC and conventional D-MPC is also presented.

The second approach is an indirect model predictive control (I-MPC) approach, in which the classical voltage balancing approach is adopted with the predictive algorithm to achieve the control objectives of MMC. The three-phase output currents and circulating currents are controlled using three-phase predictive algorithm. The capacitor voltage balancing among submodules in each arm is achieved using voltage balancing approach. The performance of proposed I-MPC approach is experimentally validated on a half-bridge based MMC system. The performance of proposed indirect MPC approach is compared with the existing fast MPC [152–154], and corresponding results are presented.

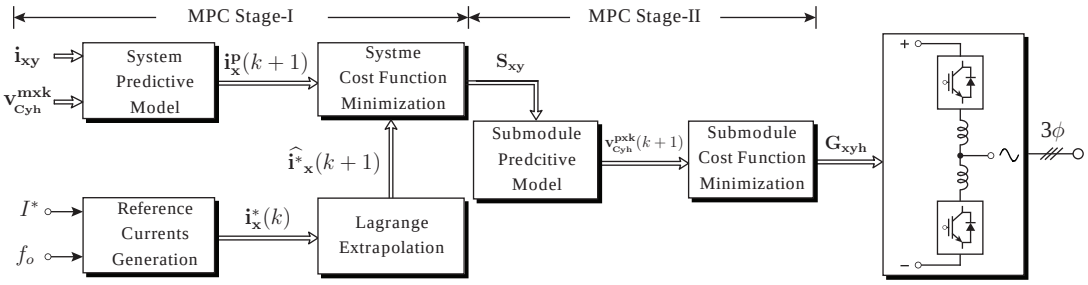


Figure 5.1. Control block diagram of dual-stage MPC

5.1 Dual-Stage Direct Model Predictive Control Approach

The control block diagram of proposed dual-stage D-MPC approach is shown in Figure 5.1. In this approach, the control objectives are categorized into two groups; namely primary and secondary. The three-phase output currents and circulating currents are included in the primary group, and the secondary group consists of submodule capacitors voltage. The primary group of control objectives is evaluated in MPC stage-I for a total of m^3 voltage vectors,

where m represents the number of output voltage levels. Each voltage vector represents the number of SMs inserted in three phases. The information of optimized voltage vector is given to the MPC stage-II, which is implemented in the local controller. In this stage, the secondary control objectives are evaluated for SMs redundancy corresponding to the optimized voltage vector. The switching state, which minimizes the cost function is selected and applied to the converter. The main features of dual-stage MPC are as follows:

- reduced computational complexity,
- less output voltage and current harmonic distortion, and
- smaller output current ripple

However, the transient response of dual-stage MPC approach is deteriorated compared with the direct MPC approach, which is one of the trade-offs.

5.1.1 Mathematical Model of MMC

The performance of model predictive control greatly depends on the mathematical model of the system. The discrete-time model of three-phase MMC is derived and presented in the chapter 4. The mathematical model is applicable to the MMC with any submodule. The output current model used in the implementation of dual-stage MPC is given below:

$$\mathbf{i_x^p}(k+1) = \Gamma_o \left[\frac{\mathbf{v_{xl}^p}(k) - \mathbf{v_{xu}^p}(k)}{2} - \underbrace{\sum_{x=a,b,c} \frac{v_{xl}^p(k) - v_{xu}^p(k)}{6}}_{\text{Common-Mode Voltage}} \right] + \Phi_o \, \mathbf{i_x^m}(k), \tag{5.1.1}$$

where,

$$\Gamma_o = \frac{T_s}{L + 2L_o}, \quad \Phi_o = 1 - \frac{(r + 2r_o)\, T_s}{L + 2L_o}. \tag{5.1.2}$$

5.1.2 Modeling of Arm Voltage

In this study, the half-bridge submodule (HB-SM) is used to configure the three-phase MMC. The HB-SM has single floating capacitor (C) and two semiconductor devices (S_1 and $\overline{S}_1$) as shown in Figure 5.2.

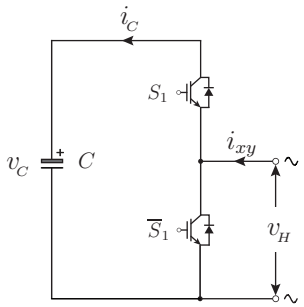


Figure 5.2. Configuration of HB-SM

The floating capacitor voltage is controlled by adjusting the duty-cycle of semiconductor devices. The devices S_1 and $\overline{S}_1$ are operated in complementary manner. Therefore, one independent gating signal is sufficient to control the HB-SM. The continuous-time model of HB-SM capacitor voltage is expressed as follows:

$$v_C(t) = v_C(0) + \frac{1}{C}\int_{0+}^{t} i_C(\tau)d\tau, \tag{5.1.3}$$

where, $v_C(0)$ represents the initial value of submodule capacitor voltage, and i_C represents the current flowing through the SM capacitor. The discrete-time model of SM capacitor voltage for one-step prediction is obtained from (5.1.3) as,

$$v_C^p(k) = v_C^m(k) + \frac{T_s}{C} i_C^p(k), \tag{5.1.4}$$

where T_s represents the sampling time, superscript m and p represents the measured and predicted quantities, respectively. The predicted SM capacitor current is given in terms of measured arm current and switching state as follows:

$$i_C^p(k) = S_1\, i_{xy}^m(k). \tag{5.1.5}$$

The predicted submodule output voltage is obtained by

$$v_{SM}^{p}(k) = S_1\, v_C^{m}(k), \tag{5.1.6}$$

where $v_{SM}^{p}(k)$ represents the predicted SM output voltage and $v_C^{m}(k)$ represents the measured SM capacitor voltage.

Each arm has N-submodules and their equivalent output voltage is expressed as follows:

$$v_{xy}^{p}(k) = \frac{S_{xy}(k)}{N} \sum_{h=1}^{N} v_{Cyh}^{m}(k), \tag{5.1.7}$$

where S_{xy}(k) represents the arm voltage level, which is also equal to the number of submodules to be inserted in an arm.

5.1.3 Implementation of Dual-Stage Predictive Algorithm

The implementation of dual-stage D-MPC scheme involves seven major steps, which are described below:

1) Measure the arm currents i_{xy}^{m} and submodule capacitors voltage $\mathbf{v_{Cyh}^{mxk}}$ at k^{th} sampling instant.

2) Generate the reference output currents. The user defines the magnitude of reference currents. However, the proposed dual-stage MPC can be applied to other power conversion applications by changing the procedure of reference current generation. The k^{th} sample of reference current is extrapolated to $(k+1)^{th}$ instant by using the third-order Lagrange extrapolation technique given below [133, 142]:

$$\widehat{i_x^*}(k+1) = 4i_x^*(k) - 6i_x^*(k-1) + 4i_x^*(k-2) - i_x^*(k-3). \tag{5.1.8}$$

3) Predict the arm voltages $v_{xy}^{p}(k)$ and output current $i_x^{p}(k+1)$ using (5.1.7) and (5.1.1).

4) The reference and predicted output currents are included in a cost function given below:

$$g_o(k) = \lambda_o \left| \widehat{\mathbf{i}}^*_{\mathbf{x}}(k+1) - \mathbf{i}^{\mathbf{p}}_{\mathbf{x}}(k+1) \right| \tag{5.1.9}$$

where λ_o is the weighting factor for output current control. The predicted output current $\mathbf{i}^{\mathbf{p}}_{\mathbf{x}}(k+1)$ for each voltage vector is compared with the extrapolated reference output current $\widehat{\mathbf{i}}^*_{\mathbf{x}}(k+1)$. The voltage vector which minimizes the cost function is selected and applied to stage-II of MPC. The m-level three-phase MMC has a total of m^3 output voltage vectors.

5) Obtain the arm voltage level from output voltage vector ($\mathbf{S_t}$). Each vector consists of three elements, which represents the lower arm voltage levels of three-phases. The upper arm voltage levels are obtained by subtracting the lower arm voltage levels from a total number of submodules per arm.

$$\begin{aligned} \mathbf{S_{xl}}(k) &= \mathbf{S_t}(k) \\ \mathbf{S_{xu}}(k) &= N - \mathbf{S_t}k \end{aligned} \tag{5.1.10}$$

The start and end memory location (S_{ts} and S_{te}) of switching states corresponding to required arm voltage level are obtained. These memory locations are used in the stage-II of MPC to retrieve the switching states.

6) Predict the submodule capacitors voltage using (5.1.4) and (5.1.5). The predicted and reference submodule capacitors voltage of each leg are included in a cost function given below:

$$g_C(k) = \lambda_C \left| V^*_C(k+1) - \mathbf{v}^{\mathbf{pxk}}_{\mathbf{Cyh}}(k+1) \right| \tag{5.1.11}$$

where λ_C is the weighting factor for capacitor voltage control and $V^*_C(k+1)$ is a reference value of the SM capacitor voltage. The cost function given in (5.1.11) is evaluated for switching states corresponding to the required arm voltage level ($\mathbf{S_{xy}}$). The switching state which minimizes the cost function is selected and applied to the converter.

5.2 Experimental Validation

To verify the performance of proposed dual-stage D-MPC approach, an experimental study is conducted on a half-bridge based three-phase MMC laboratory prototype. The MMC has two HB-SMs in each arm with a total DC-bus voltage of 150 V. This voltage is equally distributed between the SMs. The SM^1 and SM^2 in each arm are designed with a capacitance value of 1000μF and 2200μF rated for 75 V. The MMC output terminals are connected to a passive load of 108 V / 1 kW rated capacity. The dynamic performance of the proposed dual-stage MPC is compared with conventional D-MPC approach. In conventional D-MPC, the mathematical model of the output current is derived under the assumption that the DC-bus midpoint and neutral point of AC load are connected. The output current model is evaluated for total switching states of $3C_N^{2N}$. The output current model used in the conventional D-MPC is given by,

$$\mathbf{i_x^p}(k+1) = \Phi_o \mathbf{i_x^m}(k) + \Gamma_o[\mathbf{v_{xl}^p}(k) - \mathbf{v_{xu}^p}(k)]. \tag{5.2.1}$$

5.2.1 Dynamic Performance

The performance of conventional D-MPC with a step change in the reference output current is shown in Figure 5.3. The magnitude of reference output current is changed from 4 A to 8 A (peak). The actual output currents are perfectly following their reference output currents as shown in Figure 5.3(a). The output voltage represents the three-level operation of MMC, which has high $\frac{dv}{dt}$ and asymmetrical voltage steps leading to a higher harmonic distortion. The MMC generates a CMV of 30 V (peak) and circulating current of 8 A (peak-to-peak) as shown in Figure 5.3(b). The submodule capacitor voltage is rated for 75 V each. The upper and lower arm SM capacitors voltage are perfectly maintained at their rated value. The charging and discharging of SM capacitors shown in Figure 5.3(c), are not identical due to the unequal SM capacitance value.

The performance of dual-stage D-MPC with identical operating condi-

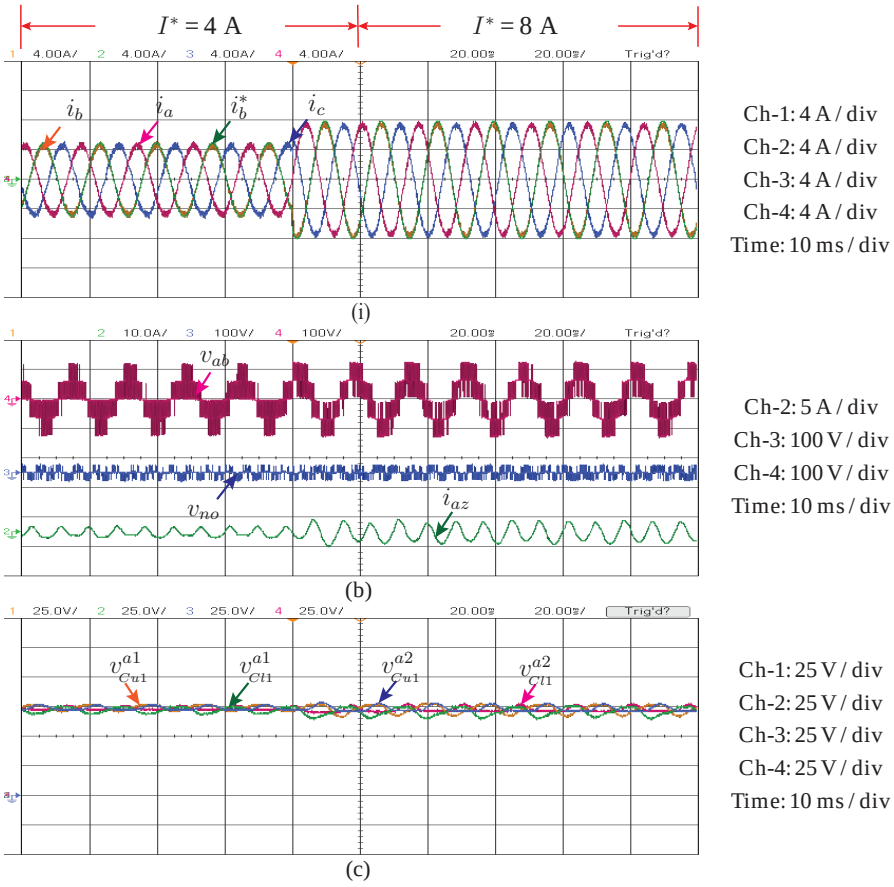
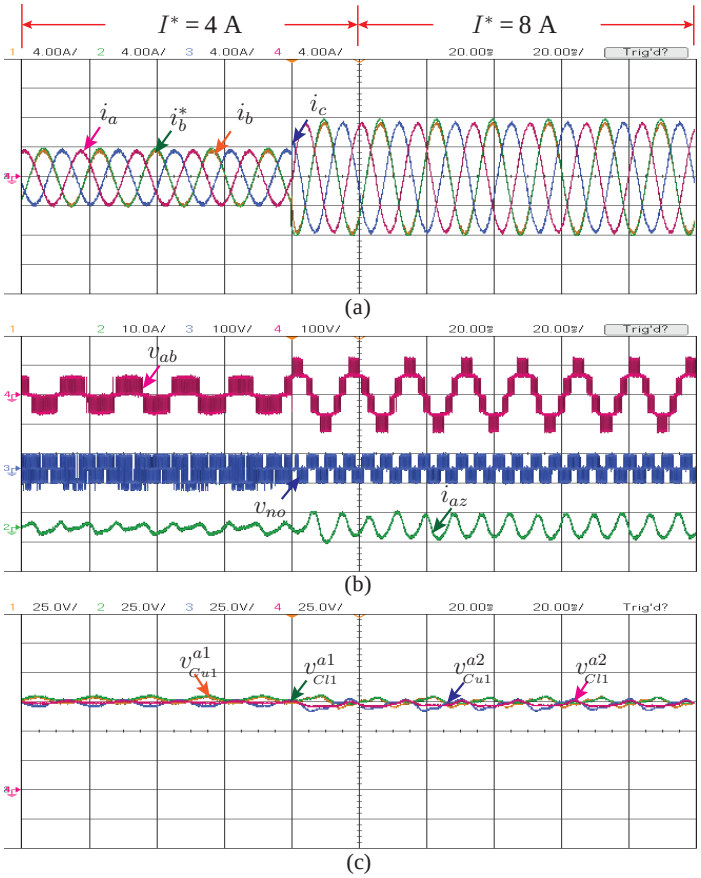


Figure 5.3. Dynamic performance of conventional MPC: (a) three-phase output currents, (b) output voltage, CMV, and circulating current, and (c) upper and lower arm submodule capacitors voltage

tions as that of conventional D-MPC is presented in Figure 5.4. The actual and reference output currents are perfectly following each other as shown in Figure 5.4(a). The number of voltage steps in output voltage waveform proportionally varies with the magnitude of output current. For example, the output voltage has two levels at 4 A and three-levels at 8 A reference current. These voltage levels are symmetrical with a step of 75 V as shown in Figure 5.4(b). The CMV is included in the discrete-time model of the MMC. That means, the SMs in upper and lower arms of MMC generates a CMV along with the fundamental voltage component to control the output current. The



Ch-1: 4 A / div
Ch-2: 4 A / div
Ch-3: 4 A / div
Ch-4: 4 A / div
Time: 10 ms / div

Ch-2: 5 A / div
Ch-3: 100 V / div
Ch-4: 100 V / div
Time: 10 ms / div

Ch-1: 25 V / div
Ch-2: 25 V / div
Ch-3: 25 V / div
Ch-4: 25 V / div
Time: 10 ms / div

Figure 5.4. Dynamic performance of dual-stage MPC: (a) three-phase output currents, (b) output voltage, CMV, and circulating current, and (c) upper and lower arm submodule capacitors voltage

fundamental voltage appears across the load, and the injected CMV appears across the DC-link midpoint and neutral point of AC load (v_{no}). The injected CMV increases the magnitude of overall CMV generated by MMC, which is around 50 V (peak). The increment in CMV increases the magnitude of circulating currents as well, in comparison to the conventional D-MPC. The circulating current has a magnitude of 10 A (peak-peak) as shown in Figure 5.4(b), which further increase the power losses and effects the efficiency of MMC. However, the effect of CMV on the circulating currents can be minimized by including the circulating current control objective in the cost func-

tion along with the output current control. By doing so, there is a significant improvement in the performance of dual-stage D-MPC. The SM capacitor voltages are perfectly balanced and maintained at a value of 75 V as shown in Figure 5.4(c).

5.2.2 Transient Response and Output Current Ripple

Figure 5.5(a) shows the instant of a step change in the reference current. The conventional and dual-stage D-MPC approaches have identical dynamic performance. However, the dual-stage D-MPC has marginal tracking error compared to conventional D-MPC. The variation in the output current ripple is shown in Figure 5.5(b). The output current generated by dual-stage D-MPC has very low switching ripple compared to the conventional D-MPC approach, which further reduces the size of output filter and harmonic distortion.

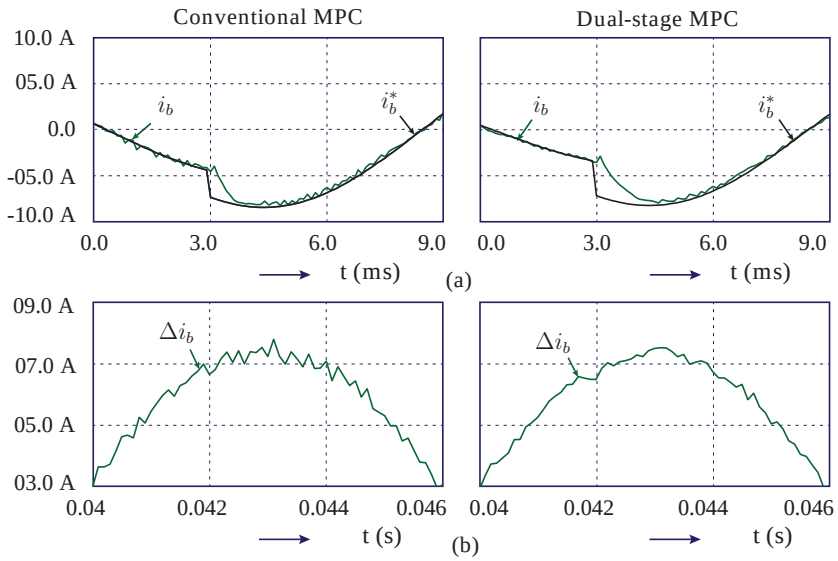


Figure 5.5. Zoomed Figure: (a) zoomed dynamic response and (b) output current ripple

5.2.3 Total Harmonic Distortion

The output voltage and current harmonic distortions are given in Table 5.1. The conventional D-MPC has an output voltage harmonic distortion of 104.-35% and current harmonic distortion of 6.93% at 4 A current reference. The voltage and current harmonic distortions are reduced by 39.29% and 40.40% respectively with the proposed dual-stage D-MPC approach. The output voltage and current harmonic distortions are further reduced with the increment in output current magnitude. At 8 A current reference, the dual-stage D-MPC approach has lowest voltage harmonic distortion of 41.56% and current harmonic distortion of 2.36% compared to the conventional D-MPC.

Table 5.1. Experiments: Performance Comparison

Performance Index	Conventional MPC		Dual-Stage MPC	
	I^* = 4 A	I^* = 8 A	I^* = 4 A	I^* = 8 A
V_{THD}	104.36%	63.35%	84%	41.56%
I_{THD}	6.93%	4.13%	4.82%	2.36%

5.2.4 Computational Complexity

The comparison of computational complexity in terms of switching states is presented in Table 5.2. For $N \leq 3$, the conventional D-MPC requires less number switching states compared to the dual-stage D-MPC approach. However, the computational complexity of dual-stage D-MPC significantly decreases with the increment in the number SMs per arm. From Table 5.2, it is observed that for $N \geq 4$, the dual-stage D-MPC requires very small number of switching states compared to the conventional D-MPC. In the conventional MPC approach, the required switching states are drastically increases with the number of SMs. For example; with N=10 SMs per arm, the conventional D-MPC requires a 554268 switching states, while the dual-stage D-

MPC requires only 2088 switching states. In overall, the dual-stage D-MPC has superior performance when the number of SMs per arm is greater than equal to 4, that is, $N \geq 4$.

Table 5.2. Comparison of Computational Complexity

Number of Submodules	Conventional D-MPC (Switching states)	Dual-Stage D-MPC With CMV (Switching states)
1	6	12
2	18	30
3	60	68
4	210	144
5	756	247
6	2774	404
7	10296	618
8	38610	940
9	145860	1379
10	554268	2088

5.3 Indirect Model Predictive Control Approach

The control block diagram of indirect model predictive control (I-MPC) approach is shown in Figure 5.6. In this approach, the classical voltage balancing approach is integrated with the predictive algorithm. The three-phase output currents and circulating currents are controlled with the predictive algorithm, which is implemented in a central controller. The control objectives are included in a cost function and evaluated for all possible output voltage vectors. The voltage vector which minimizes the cost function is selected and applied to the local controller. The optimized voltage vector represented the number of on-state submodules in each arm and given to the local controller. The submodule voltage balancing approach is implemented in a local con-

troller. The local controller selects the submodules based on their capacitors voltage, the direction of arm current and number of on-state submodules. The selected submodules are inserted in the arm.

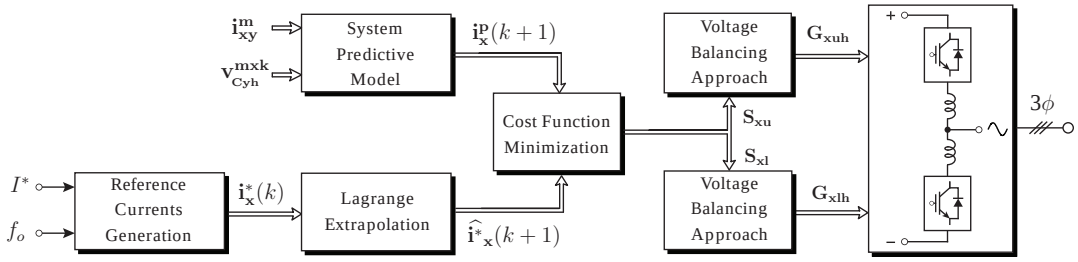


Figure 5.6. Control block diagram of indirect MPC

5.3.1 Implementation of Predictive Algorithm

The implementation of the predictive algorithm involves six major design steps given below:

1) Measure the three-phase arm currents $\mathbf{i}^{\mathbf{m}}_{\mathbf{xy}}(k)$ and SM capacitor voltages $\mathbf{v}^{\mathbf{mxk}}_{\mathbf{Cyh}}(k)$.

2) The reference output currents $\mathbf{i}^*_{\mathbf{x}}(k)$ are defined by the user. The k^{th} instant currents are extrapolated to $(k+1)^{\text{th}}$ instant by using Lagrange extrapolation as follows [167]:

$$\mathbf{i}^*_{\mathbf{x}}(k+1) = 4\mathbf{i}^*_{\mathbf{x}}(k) - 6\mathbf{i}^*_{\mathbf{x}}(k-1) + 4\mathbf{i}^*_{\mathbf{x}}(k-2) - \mathbf{i}^*_{\mathbf{x}}(k-3). \tag{5.3.1}$$

3) Using (5.1.7), estimate the future behavior of arm voltages $\mathbf{v}^{\mathbf{p}}_{\mathbf{xy}}(k+1)$ for all possible output voltage vectors. A three-phase MMC with N-SMs per arm has a total of $(N+1)^3$ output voltage vectors.

4) The predicted arm voltages and discrete-time model in (5.1.1) and (5.1.2) are used to predict the output current $\mathbf{i}^{\mathbf{p}}_{\mathbf{x}}(k+1)$ behavior.

5) A cost function is defined as follows such that predicted output current $\mathbf{i_x^p}(k+1)$ follow their corresponding references:

$$g(k) = \lambda_o * (\mathbf{i_x^*}(k+1) - \mathbf{i_x^p}(k+1))^2. \tag{5.3.2}$$

where λ_o is the weighting factor for output current control. The voltage vector which minimizes cost function is selected and applied to the local controller. Each voltage vector represents required number of on-state SMs in three-phases.

6) The weighting factors for the error terms in equation (5.3.2) are obtained from the per-unit method [145]. The weighting factor for output current control is given by,

$$\lambda_o = \frac{i_x^*}{i_B}. \tag{5.3.3}$$

where i_B represents the rated or base value of the output current.

5.3.2 Implementation of Balancing Algorithm

The balancing approach for each arm is implemented in a local controller. The flowchart of simplified balancing approach with the following design steps is shown in Figure 5.7(a):

1) Measure the SM capacitors voltage ($\mathbf{v_{Cyh}^{mxk}}$) in each arm and supply the magnitude value to "comparison logic" as shown in Figure 5.7(b).

2) In relative comparison logic, each capacitor voltage is compared with other capacitors voltage. The output of each comparator is added together to obtain an index number (VI_h). The highest index number is assigned to the submodule with the lowest capacitor voltage and vice–versa.

3) Measure the arm current (i_{xy}^m) and determine its direction (D). For positive direction D=1 is assigned, and D=0 is assigned for negative direction.

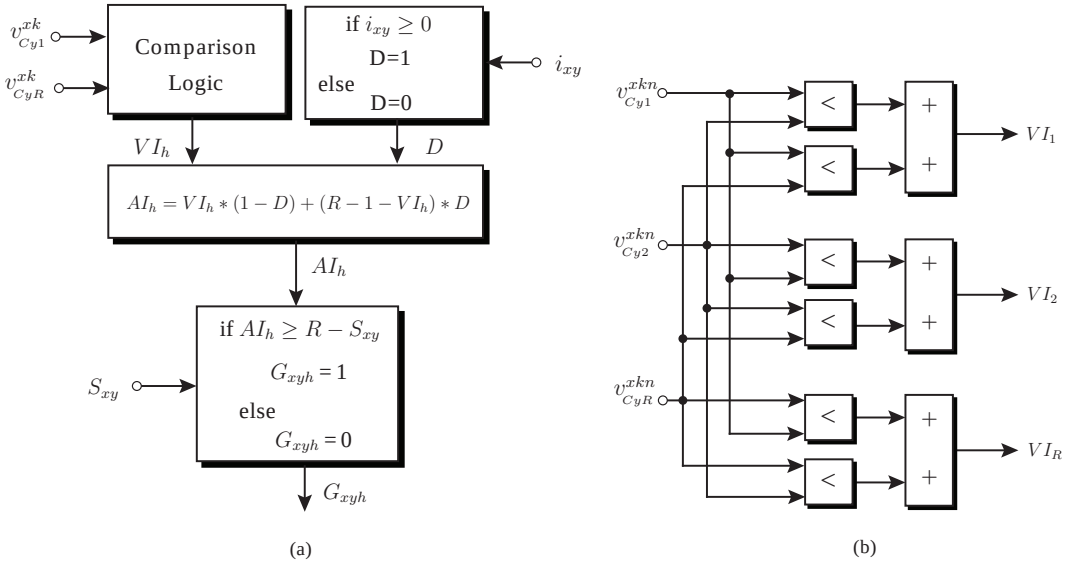


Figure 5.7. Voltage balancing approach: (a) design steps of balancing approach, (b) comparison logic

4) Arrange the SM index numbers in either ascending or descending order based on the direction of arm current. A simple mathematical expression is presented below to arrange the submodule index number.

$$AI_h = VI_h * (1 - D) + (N - 1 - VI_h) * D. \tag{5.3.4}$$

5) Compare actual index number of each submodule (AI_h) with reference index number ($N - S_{xy}$) to generate the "INSERT=1" (or) "BYPASS=0" state for each submodule (G_{xyh}).

5.4 Experimental Validation

To verify the performance of the proposed indirect MPC approach, a three-phase MMC laboratory prototype based on the HB SMs is developed. The MMC system has a total DC-bus voltage of 150 V, which can generate 105 V on AC-side. Each arm of MMC has two 2L-HB SMs with a nominal voltage of 75 V each. To emulate the deterioration of SM capacitance, the SM^1

and SM^2 are designed with a different equivalent capacitance value of 1000 μF and 2200μF, respectively. The comparison of proposed approach with fast MPC [154] is presented. The fast MPC approach follows the per-phase methodology and corresponding discrete-time model of output current is given by,

$$\mathbf{i_x^p}(k+1) = \mathbf{\Gamma_o}[\mathbf{v_{xl}^p}(k) - \mathbf{v_{xu}^p}(k)] + \mathbf{\Phi_o}\mathbf{i_x^m}(k). \tag{5.4.1}$$

From the equations (5.1.1) and (5.4.1), it is observed that the three-phase methodology includes common-mode voltage (CMV) in the mathematical model of MMC. The effect of CMV on the converter performance is presented in the following subsections.

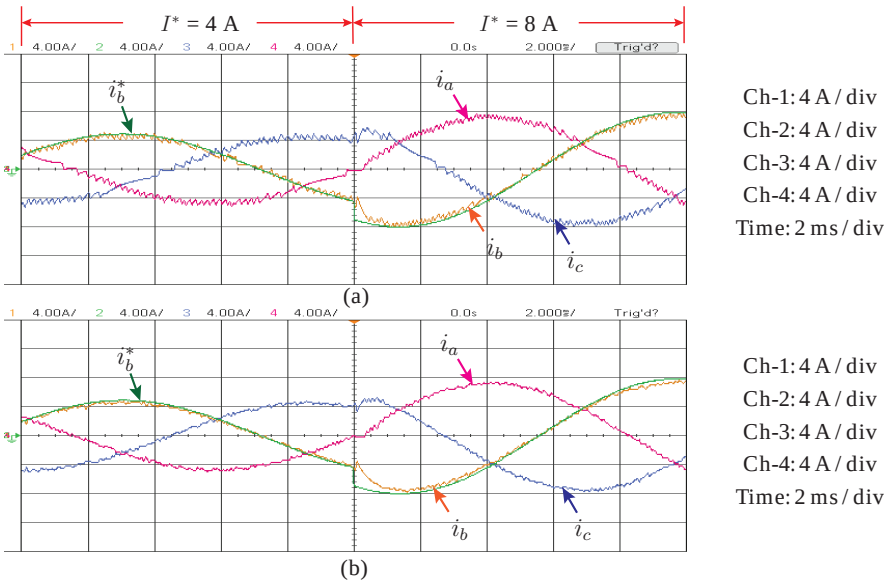


Figure 5.8. Three-phase output currents: (a) fast MPC, and (b) indirect MPC

5.4.1 Dynamic Response

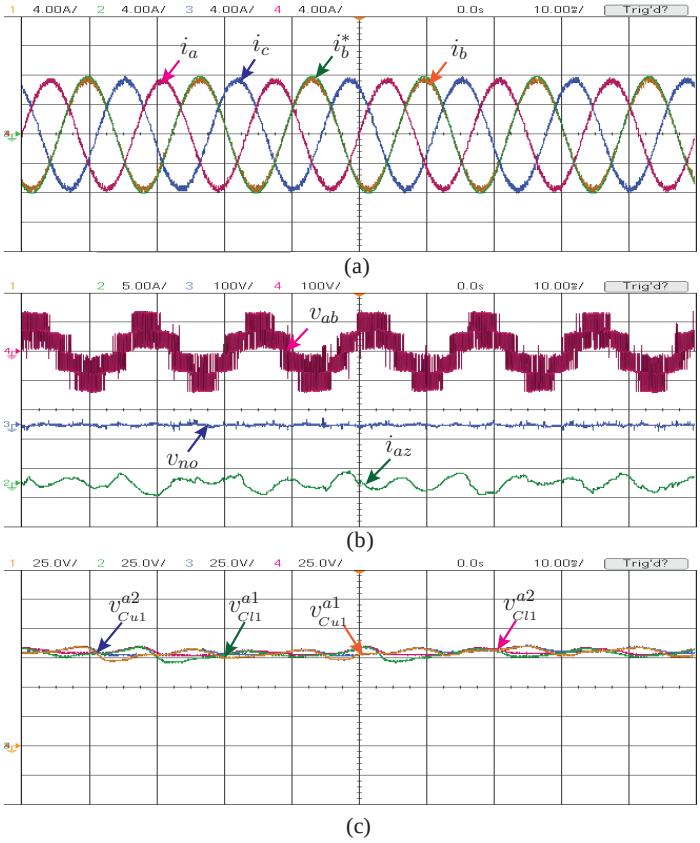
The dynamic performance comparison of fast MPC and proposed indirect MPC with a step change in the reference current is shown in Figure 5.8. In fast MPC approach, the current model given in (5.4.1) is used to control the output currents. The magnitude of reference current is changed from I^*=4

A to I^*=8 A. The three-phase output currents are perfectly balanced and, the reference and actual current of phase-b are perfectly following each other as shown in Figure 5.8(a). The fast MPC approach has a very quick response time of 0.35 ms. The dynamic response of indirect MPC is shown in Figure 5.8(b). The three-phase output currents are sinusoidal in shape and perfectly following their reference current. The indirect MPC approach has a response time of 0.55 ms, which higher than the fast MPC method. However, the switching ripple in output current is much smaller compared to the fast MPC method. Thereby, the indirect MPC requires a smaller output filter to reduce the switching ripple in the output current.

5.4.2 Balanced Operation

The steady-state performance of fast MPC under balanced operating conditions is shown in Figure 5.9. In this study, the magnitude of the reference output current is set to 8 A. The MMC generates three-phase output currents with a magnitude of 8 A reference value. These currents are perfectly balanced and sinusoidal in nature as shown in Figure 5.9(a). The output line-to-line voltage waveform resembles the three-level operation of MMC. However, the voltage waveform has high $\frac{dv}{dt}$, which increases the output voltage harmonic distortion. In fast MPC, the CMV contains only a small switching ripple as shown in Figure 5.9(b). The fast MPC approach has a circulating current of 1.5 A (p-p) at 4 A and 3 A (p-p) at 8 A of load current. The upper and lower arm SM capacitors voltage are perfectly balanced around 77 V as shown in Figure 5.9(c). The fast MPC approach has a steady-state error of 2% in capacitors voltage.

The steady-state performance of the indirect MPC is shown in Figure 5.10. The philosophy of fast MPC and proposed indirect MPC approaches are quite identical with a minor difference in the implementation of the predictive algorithm and the mathematical model of output current. In the proposed approach, the three-phase output currents are controlled using single predictive algorithm rather than the per-phase approach. The MMC is con-



Ch-1: 4 A / div
Ch-2: 4 A / div
Ch-3: 4 A / div
Ch-4: 4 A / div
Time: 10 ms / div

Ch-2: 5 A / div
Ch-3: 100 V / div
Ch-4: 100 V / div
Time: 10 ms / div

Ch-1: 25 V / div
Ch-2: 25 V / div
Ch-3: 25 V / div
Ch-4: 25 V / div
Time: 10 ms / div

Figure 5.9. Balanced operation of MMC with fast MPC: (a) three-phase output currents, (b) output voltage, CMV, and circulating current, and (c) upper and lower arm submodule capacitors voltage

trolled to generate three-phase currents with a magnitude of 8 A as shown in Figure 5.10(a). The output line-line voltage waveform has symmetrical voltage steps of 75 V and has very low harmonic distortion compared to other MPC approaches. The CMV generated by the MMC consists of a third harmonic component with a peak value of 50 V as shown in Figure 5.10(b). The indirect MPC approach generates a circulating current of 2 A (p-p) at 4 A and 4 A (p-p) at 8 A of load current as shown in Figure 5.10(b). This approach generates a slightly higher magnitude of circulating currents compared to the fast MPC approach. The inclusion of CMV in the proposed approach generates a third harmonic current component, which increases the magnitude

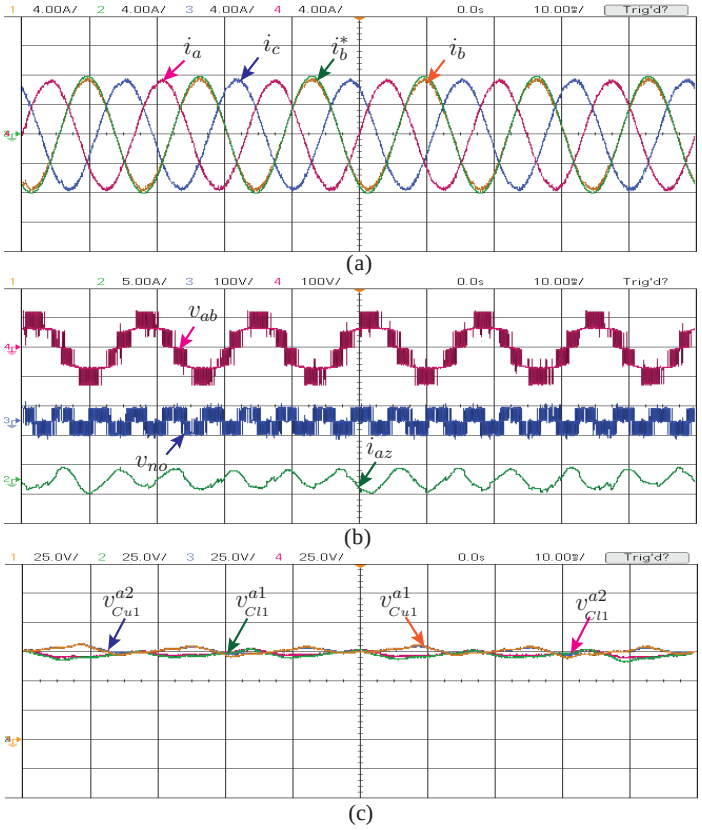


Figure 5.10. Balanced operation of MMC with indirect MPC: (a) three-phase output currents, (b) output voltage, CMV, and circulating current, and (c) upper and lower arm submodule capacitors voltage

of circulating currents. The SM capacitor voltages are perfectly balanced at their nominal value of 75 V, without any steady-state error using a voltage balancing approach as shown in Figure 5.10(c).

5.4.3 Total Harmonic Distortion

The voltage harmonic distortion (V_{THD}) and current harmonic distortion (I_{THD}) of the fast and indirect MPC approaches are summarized in Table 5.3 for a reference current magnitude of 8 A. The fast MPC has a V_{THD} of 45.07% and I_{THD} of 3.19%. Other hand, the indirect MPC generates a very high-quality output

voltage and current waveforms with a THD of 25.73% and 2.1%, respectively. The proposed MPC approach is operating at the lowest switching frequency and obtained a reduction in V_{THD} by 43% and I_{THD} by 34% in comparison to the fast MPC.

Table 5.3. Performance Comparison at Balanced Conditions

Performance Index	Fast MPC	Indirect MPC
V_{THD}	45.07%	25.73%
I_{THD}	3.19%	2.10%

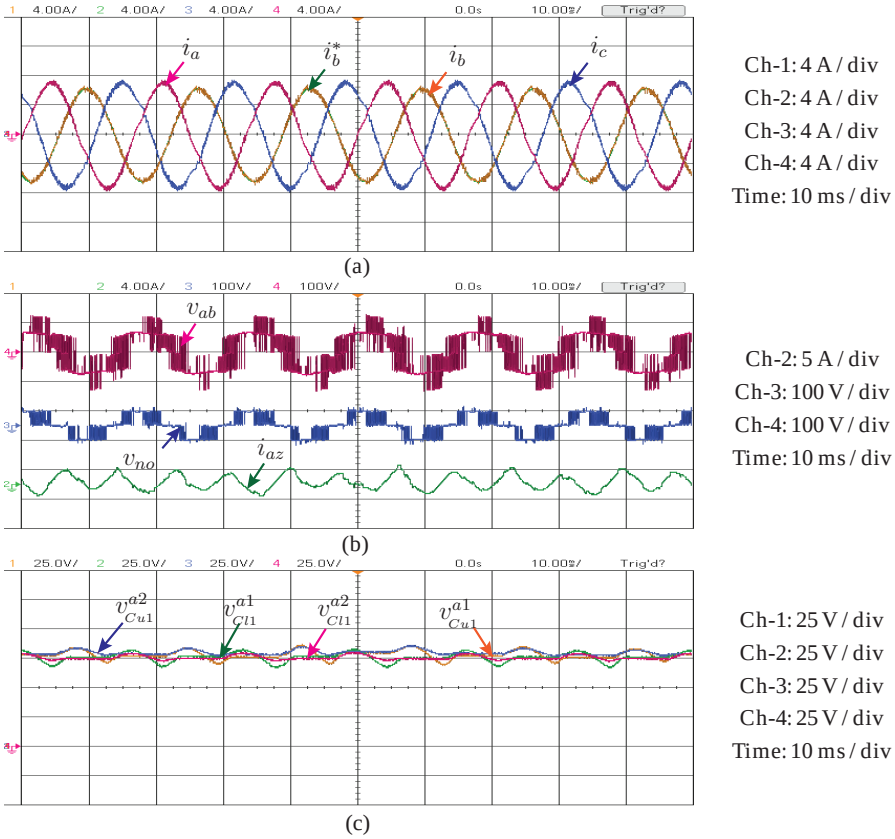


Figure 5.11. Unbalanced operation of MMC with fast MPC: (a) three-phase output currents, (b) output voltage, CMV, and circulating current, and (c) upper and lower arm submodule capacitors voltage

5.4.4 Unbalanced Operation

The performance of fast MPC approach during unbalanced operating conditions is shown in Figure 5.11. In this study, the three-phase reference currents are generated with a 20% unbalance in magnitude. The three-phase output

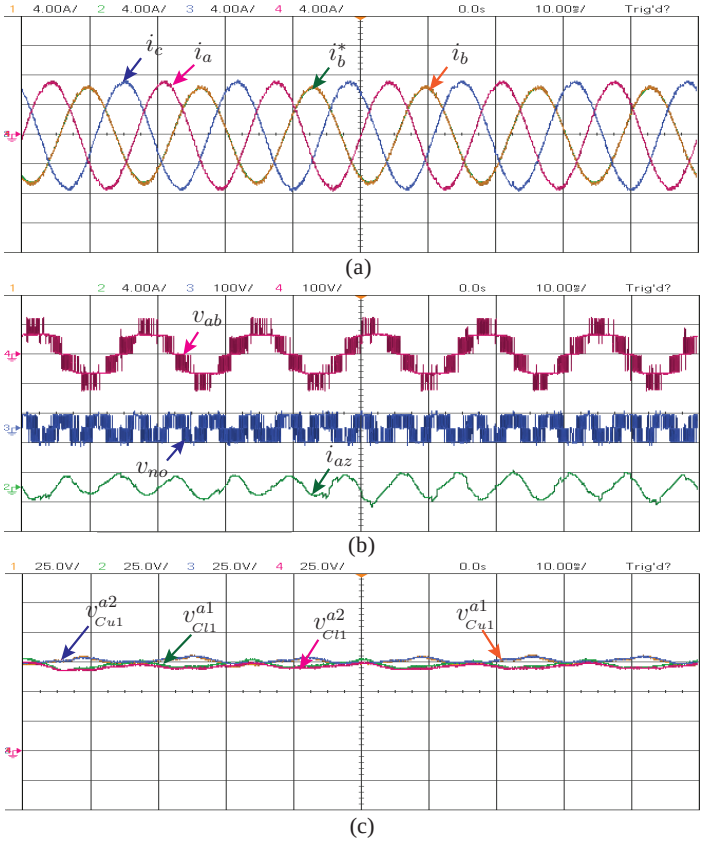


Figure 5.12. Unbalanced operation of MMC with indirect MPC: (a) three-phase output currents, (b) output voltage, CMV, and circulating current, and (c) upper and lower arm submodule capacitors voltage

currents flowing through the load are not perfectly sinusoidal in nature and have higher harmonic distortion as shown in Figure 5.11(a). The difference between line-line voltages due to the unbalanced condition appears in the form of CMV as shown in Figure 5.11(b). The CMV mainly consists of fundamental frequency component with a step of 50 V. The multilevel CMV sig-

nificantly reduces the $\frac{dv}{dt}$ stress on the load. The circulating current has a peak-peak value of 3.5 A as shown in Figure 5.11(b). The SM capacitors voltage is maintained at an average value of 73 V, which is marginally less than their nominal value of 75 V as shown in Figure 5.11(c).

The performance of indirect MPC approach is shown in Figure 5.12. The three-phase currents are very close to sinusoidal in shape and, have low ripple and harmonic distortion compared to the fast MPC approach as shown in Figure 5.12(a). The indirect MPC approach generates a line-line voltage waveform with a step of 75 V, which is quite similar to balanced operation condition as shown in Figure 5.12(b). The CMV mainly consists of third harmonic component with a peak value of 50 V. This CMV increases the magnitude of circulating currents and has a peak-peak value of 4 A as shown in Figure 5.12(b). In addition, the proposed approach perfectly balance the upper and the lower arm SM capacitors voltage at their nominal value of 75 V as shown in Figure 5.12(c).

5.4.5 Computational Complexity

The comparison of different MPC strategies in terms of computational complexity is given in Table 5.4. In direct MPC approach, the control objectives of output current, circulating current, and SM capacitor voltage balance are included in a single cost function. The cost function is evaluated for 210 switching states to control the MMC with four-submodules per arm [148]. The required number of switching states drastically increases with the number of submodules. In the case of fast MPC approach, the output and circulating current of each phase are controlled using a per-phase MPC strategy. This approach requires only 5-states for one phase (total 15-states in a three-phase system) [154]. This approach requires the least number of switching states compared to other methods. The reduced MPC strategy-I and II are presented in [155], requires 72 and 96 switching states (for N=4) to achieve the control objectives, respectively. The proposed approach requires 125 switching vectors to control the three-phase output and circulating currents, which

leads to a less computational effort in comparison to direct MPC. However, the proposed approach still requires a higher number of switching states compared to the fast and reduced MPC strategies.

Table 5.4. Computational Load on MPC

Number of Submodules	Conventional D-MPC [148]	Fast MPC [154]	Reduced MPC-I [155]	Reduced MPC-II [155]	Indirect MPC
2	18	9	30	54	27
4	210	15	72	96	125
10	554268	33	342	222	1331

5.5 Summary

In this chapter, two novel reduced computational model predictive control approaches are proposed for the modular multilevel converter. The first approach is dual-stage direct model predictive control, in which the control objectives are achieved using two cost functions. The step-by-step design procedure of dual-stage D-MPC approach is presented in this chapter. The experimental studies are presented to validate the dynamic and steady-state performance of dual-stage D-MPC approach. The performance of dual-stage D-MPC is compared with the conventional MPC. The results show that the computational complexity is significantly minimized through the dual-stage D-MPC approach. When the number of SMs $N \geq 4$, then the dual-stage D-MPC approach has superior performance and requires a lesser number of switching states compared to conventional D-MPC. In addition, a significant reduction in output voltage and current harmonic distortions are obtained. For instance, at I^*=0.8 pu, a reduction of 27.08% in current harmonic distortion and 30.85% in voltage harmonic distortion are obtained.

The second approach is indirect model predictive control (I-MPC) approach, in which the control objectives are achieved by using classical voltage balancing approach and predictive algorithm together. The implementation of I-MPC approach, which includes the voltage balancing approach and

predictive algorithm is systematically presented in this chapter. The experimental studies are presented to validate the dynamic and steady-state performance during balanced and unbalanced operating conditions. The performance of indirect MPC is also compared with the fast MPC approach. The results show that the I-MPC approach operates at lowest switching frequency and minimizes the voltage and current harmonic distortion by 43% and 34% in comparison to the fast MPC. The I-MPC approach generates output current with lowest switching ripple. Hence, the size of the output filter is minimized. However, the computational complexity is slightly higher than the fast MPC. In addition, the dynamic performance of MMC with I-MPC is marginally reduced.

CHAPTER 6

CONCLUSIONS

OVER the last few years, significant attention has been paid to the modular multilevel converters. The immense features of modular multilevel converter are attracted both academia and industry researchers, and developed several commercial products for high-voltage direct current transmission systems, medium-voltage motor drive systems and static synchronous compensators. These applications require an accurate mathematical model to develop a sophisticated control scheme with a complex structure to control the modular multilevel converter. For an efficient and reliable operation of modular multilevel converter, the control scheme must fulfill the following objectives: submodule capacitors voltage control, output current control, minimization of circulating currents, minimization of ripple in submodule capacitors voltage and DC-link current.

In this work, a novel voltage balancing methods and pulse width modulation schemes are proposed to control the modular multilevel converter. These methods are generic in nature, suitable to apply for standard and multilevel submodules based modular multilevel converters, reduces the number of current sensors and eliminates the external controllers to achieve some of the control objectives. In addition, the reduction in output voltage and current harmonic distortion, output current ripple, and device power losses

are obtained.

This dissertation also proposes a direct and reduced computational model predictive control approaches to control the modular multilevel converter. A generalized three-phase mathematical model of the modular multilevel converter, which includes the common-mode voltage is developed to implement the model predictive control approach. These methods significantly minimize the magnitude of circulating currents, a ripple in the submodule capacitors voltage and DC-link current without using a cost function during the balanced and unbalanced operating conditions. The proposed methods also reduce the computational complexity and, output voltage and current harmonic distortion while operating at the lowest switching frequency.

6.1 Main Contributions

The main contributions of this dissertation are summarized as follows:

1) **Single–stage submodule capacitors voltage balancing method with reduced current sensors**

The voltage balancing among submodules is very important objective for the reliable operation of the modular multilevel converter. In this dissertation, a generalized single–stage submodule capacitors voltage balancing method with reduced current sensors is proposed. This approach uses estimated arm currents rather than direct measurements to obtain the current direction. The single-stage approach is suitable to implement with both PSC-PWM and LSC-PWM schemes and possible to control both standard submodules (half-bridge, H-bridge) and multilevel submodules (flying capacitor, neutral-point clamp submodules) based modular multilevel converters.

2) Dual–stage submodule capacitors voltage balancing method with reduced power losses and harmonic distortion

The design and implementation of balancing approach affect the performance of the modular multilevel converter. In this dissertation, a dual-stage submodule capacitors voltage balancing approach is proposed to control the flying capacitor submodule based modular multilevel converter. This approach significantly minimizes the submodule power losses and voltage harmonic distortion compared with the single-stage balancing approach. In addition, the total power losses are equally distributed between the submodules in each arm. Hence, identical thermal and cooling systems are used to design each submodule.

3) Pulse width modulation schemes with improved harmonic performance

The performance of modular multilevel converter greatly depends on the type of pulse width modulation scheme. In this dissertation, two novel pulse width modulation schemes equivalent to the carrier pulse width modulation scheme with third harmonic injection are proposed.

- The first approach is a sampled average modulation, which modulates each leg of modular multilevel converter independently. The three-phase sampled average modulation is equivalent to space vector modulation with an asymmetrical distribution of zero voltage vectors.
- The second approach is dual space vector modulation, which modulates the three-phase upper and lower arms with a space vector philosophy. In this approach, the zero vectors are symmetrically distributed in each sampling interval.
- An external voltage balancing approach is proposed to achieve the voltage balancing among submodules with sampled average and space vector modulation schemes.

- These modulation schemes are generic in nature and directly applied to the modular multilevel converter (irrespective of a number of submodules) without any modifications.
- These modulation schemes significantly minimize the total harmonic distortion and output current ripple compared to the carrier based modulation schemes. In addition, the magnitude of switching frequency harmonics is significantly reduced. Hence, the smaller size of filter is used in the output.
- The sampled average and space vector modulation schemes generate a common-mode voltage at three-time the fundamental frequency. This common-mode voltage helps to achieve the voltage balancing between arms. Hence, the control scheme is simplified by eliminating the arm voltage balancing controller.

4) Minimization of circulating currents and, ripple in submodule capacitors voltage and DC-link current using direct model predictive control approach

The modular multilevel converter requires a control scheme to meet several control objectives simultaneously. In this dissertation, a novel direct model predictive control approach is proposed.

- To implement the proposed approach, a generalized discrete-time model of the three-phase modular multilevel converter with a common-mode voltage injection capability is developed.
- The common-mode voltage helps to achieve the voltage balancing between arms. Hence, the magnitude of circulating currents are significantly reduced without using cost function.
- The reduction in submodule capacitors voltage and DC-link current ripple during balancing and unbalanced operating conditions is obtained.

- In addition, the output voltage and current harmonic distortion is minimized.

5) Reduced computational model predictive control approaches

The computation complexity is one of the major issues in the real-time implementation of model predictive control for modular multilevel converters. In this dissertation, two novel reduced computational model predictive control approaches are proposed.

- The first approach is dual-stage direct model predictive control approach, which uses two cost functions to achieve the control objectives of modular multilevel converters.
- The second approach is indirect model predictive control approach, which integrates the voltage balancing approach with a predictive algorithm to control the modular multilevel converter.
- These approaches have less computationally complexity compared to the conventional direct model predictive control approach
- These approaches significantly minimize the harmonic distortion of output voltage and current waveforms, and output current ripple while operating at lowest switching frequency.

6) Laboratory prototype of modular multilevel converter

The simulation studies are validated through experimental studies on a low-power laboratory prototype of the modular multilevel converter. The laboratory prototype is designed to generate 208 V / 3 kVA with a total DC-link voltage 350 V. The submodules are designed to operate as either half-bridge or three-level flying capacitor submodule. Each submodule is equipped with an EPCOS DC capacitors, Semikron dual pack SKM1000GB12T4 IGBT / diode modules of 1200 V, 100 A capacity, SKHI22B dual-core IGBT gate drivers,

LEM LV25-P isolated voltage sensors and LEM LA55-P hall sensors. The DC-link voltage of the modular multilevel converter is generated by using a Xantrex DC source of 600 V, 20 A capacity. The laboratory prototype is controlled with a dSPACE / DS1103 control platform with an external CP1103 I / O interface.

6.2 Suggested Future Work

The following research works are suggested as an extension to the knowledge presented in this dissertation.

1) **Research on space vector modulation scheme to minimize the submodule capacitors voltage ripple**

The space vector modulation scheme has redundancy switching voltage vectors with different magnitudes of common-mode voltage. The use of redundancy switching vectors to minimize the submodule capacitors voltage ripple is one of the interesting research topics.

2) **Wave shaping of submodule capacitors voltage and circulating currents using direct model predictive control**

The wave shaping of submodule capacitors voltage and circulating currents using direct model predictive control with the externally generated common-mode voltage and circulating currents is another important research direction. The performance of modular multilevel converter should be investigated in terms of device power losses and capacitors voltage ripple under a different type of common-mode voltages.

3) **Research on modular multilevel converter topologies for motor drives**

The common-mode voltage injected into the system to minimize the capacitors voltage ripple in the conventional modular multilevel converter. The ex-

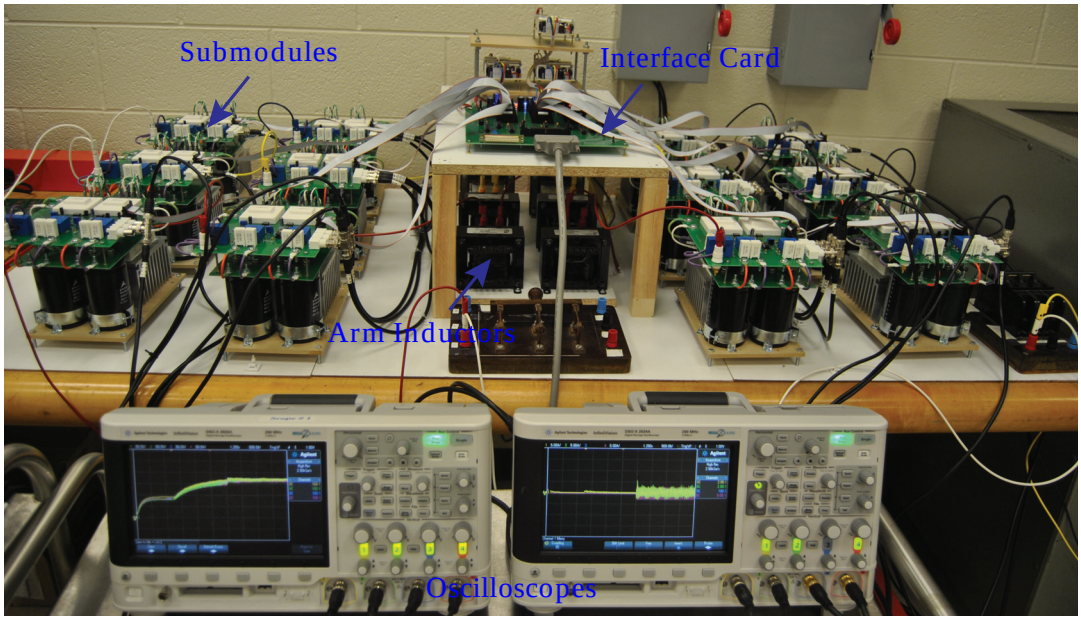
ternal injected common-mode voltage increases the magnitude of common-mode voltage generated by the converter, which is not suitable for motor drive applications. The development of new modular multilevel converter topologies, which overcomes the drawback of the conventional modular multilevel converter is another important research direction.

4) Research on submodule configurations with DC fault blocking capability

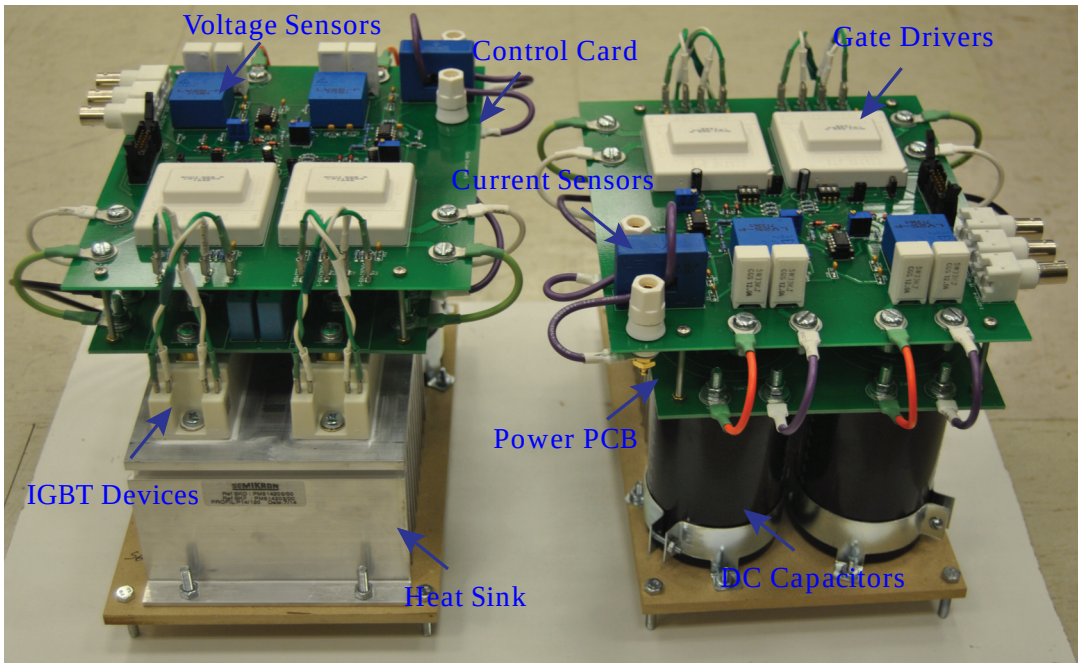
The submodule presented in this dissertation can not block the DC faults and requires a DC circuit breakers to protect the system. Hence, the development of new submodules to handle the DC faults is one of important research aspect in modular multilevel converter for HVDC applications.

APPENDIX

LABORATORY PROTOTYPES



A.1. Laboratory prototype of modular multilevel converter.



A.2. Laboratory prototype of MMC Submodule.

BIBLIOGRAPHY

[1] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun 2008.

[2] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug 2002.

[3] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May 1996.

[4] J. A. Sayago, T. Bruckner, and S. Bernet, "How to select the system voltage of mv drives-a comparison of semiconductor expenses," *IEEE Trans. Ind. Electron.*, vol. 55, no. 9, pp. 3381–3390, Sept 2008.

[5] S. Kouro, J. Rodriguez, B. Wu, S. Bernet, and M. Perez, "Powering the future of industry: High-power adjustable speed drive topologies," *IEEE Ind. Appl. Mag.*, vol. 18, no. 4, pp. 26–39, Jul 2012.

[6] B. Wu, *High-Power Converters and AC Drives*. New york: Wiley-IEEE Press, Mar. 2006.

[7] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. . M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov 2009.

[8] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters: State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug 2010.

[9] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[10] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan 1999.

[11] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (mmcc)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov 2011.

[12] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Pèrez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul 2010.

[13] H. J. Knaak, "Modular multilevel converters and hvdc/facts: A success story," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, Aug 2011, pp. 1–6.

[14] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3, Jun 2003, pp. 23–26.

[15] R. Marquardt, "Modular multilevel converter: An universal concept for hvdc-networks and extended dc-bus-applications," in *Power Electronics Conference (IPEC), 2010 International*, Jun 2010, pp. 502–507.

[16] J. Wang, R. Burgos, and D. Boroyevich, "A survey on the modular multilevel converters - modeling, modulation and controls," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, Sept 2013, pp. 3984–3991.

[17] M. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan 2015.

[18] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec 2007.

[19] K. P. Phillips, "Current-source converter for ac motor drives," *IEEE Trans. Ind. Appl.*, vol. IA-8, no. 6, pp. 679–683, Nov 1972.

[20] Y. Xiao, B. Wu, S. C. Rizzo, and R. Sotudeh, "A novel power factor control scheme for high-power gto current-source converter," *IEEE Trans. Ind. Appl.*, vol. 34, no. 6, pp. 1278–1283, Nov 1998.

[21] B. Wu, J. Pontt, J. Rodriguez, S. Bernet, and S. Kouro, "Current-source converter and cycloconverter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2786–2797, Jul 2008.

[22] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: a technology review," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 276–288, Apr 2002.

[23] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of three-phase pwm ac–ac converter topologies," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, Nov 2011.

[24] H. Stemmler, "High-power industrial drives," *Proc. IEEE*, vol. 82, no. 8, pp. 1266–1286, Aug 1994.

[25] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul 2010.

[26] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "A new nested neutral point-clamped (nnpc) converter for medium-voltage (mv) power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6375–6382, Dec 2014.

[27] M. Narimani, B. Wu, K. Tian, Z. Cheng, and N. R. Zargari, "A new h-bridge nnpc converter for 10kv class motor drives," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*.

[28] V. Dargahi, A. Sadigh, M. Abarzadeh, S. Eskandari, and K. Corzine, "A new family of modular multilevel converter based on modified flying-capacitor multicell converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 138–147, Jan 2015.

[29] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan 2015.

[30] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for hvdc-transmission," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*.

[31] J.-J. Jung, H.-J. Lee, and S.-K. Sul, "Control of the modular multilevel converter for variable-speed drives," in *Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on*.

[32] S. Teeuwsen, "Modeling the trans bay cable project as voltage-sourced converter with modular multilevel converter design," in *2011 IEEE Power and Energy Society General Meeting*.

[33] M. Pereira, D. Retzmann, J. Lottes, M. Wiesinger, and G. Wong, "Svc plus: An mmc statcom for network and grid access applications," in *2011 IEEE Trondheim PowerTech*, June 2011, pp. 1–5.

[34] Q. Tu, Z. Xu, H. Huang, and J. Zhang, "Parameter design principle of the arm inductor in modular multilevel converter based hvdc," in *Power System Technology (POWERCON), 2010 International Conference on*, Oct 2010, pp. 1–6.

[35] A. Nami, J. Liang, F. Dijkhuizen, and G. Demetriades, "Modular multilevel converters for hvdc applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan 2015.

[36] Y. Xue, Z. Xu, and G. Tang, "Self-start control with grouping sequentially precharge for the c-mmc-based hvdc system," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 187–198, Feb 2014.

[37] G. Konstantinou, J. Zhang, S. Ceballos, J. Pou, and V. G. Agelidis, "Comparison and evaluation of sub-module configurations in modular multilevel converters," in *2015 IEEE 11th International Conference on Power Electronics and Drive Systems*, June 2015, pp. 958–963.

[38] J. Wang, R. Burgos, and D. Boroyevich, "Switching-cycle state-space modeling and control of the modular multilevel converter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 4, pp. 1159–1170, Dec 2014.

[39] B. Li, Y. Zhang, D. Xu, and R. Yang, "Start-up control with constant precharge current for the modular multilevel converter," in *2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE)*, Jun 2014, pp. 673–676.

[40] S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An improved control system for modular multilevel converters with new modulation strategy and voltage balancing control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 358–371, Jan 2015.

[41] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 57–68, Jan 2012.

[42] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3702–3713, Aug 2013.

[43] X. Shi, Z. Wang, L. M. Tolbert, and F. Wang, "A comparison of phase disposition and phase shift pwm strategies for modular multilevel converters," in *2013 IEEE Energy Conversion Congress and Exposition*, Sept 2013, pp. 4089–4096.

[44] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2688–2701, May 2016.

[45] G. Konstantinou, J. Pou, S. Ceballos, R. Darus, and V. G. Agelidis, "Switching frequency analysis of staircase-modulated modular multilevel converters and equivalent pwm techniques," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 28–36, Feb 2016.

[46] W. van der Merwe, "Natural balancing of the 2-cell modular multilevel converter," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 4028–4035, Nov 2014.

[47] G. S. Konstantinou and V. G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal pwm

techniques," in *2009 4th IEEE Conference on Industrial Electronics and Applications*, May 2009, pp. 3399–3404.

[48] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, and V. G. Agelidis, "Circulating current control and evaluation of carrier dispositions in modular multilevel converters," in *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, Jun 2013, pp. 332–338.

[49] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, "An improved pulse width modulation method for chopper-cell-based modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3472–3481, Aug 2012.

[50] B. P. McGrath and D. G. Holmes, "Multicarrier pwm strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug 2002.

[51] J. Mei, K. Shen, B. Xiao, L. Tolbert, and J. Zheng, "A new selective loop bias mapping phase disposition pwm with dynamic voltage balance capability for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 798–807, Feb 2014.

[52] A. Hassanpoor, S. Norrga, H. P. Nee, and L. Ängquist, "Evaluation of different carrier-based pwm methods for modular multilevel converters for hvdc application," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Oct 2012, pp. 388–393.

[53] D. Siemaszko, A. Antonopoulos, K. Ilves, M. Vasiladiotis, L. Angquist, and H.-P. Nee, "Evaluation of control and modulation methods for modular multilevel converters," in *Power Electronics Conference (IPEC), 2010 International*, Jun 2010, pp. 746–753.

[54] R. Darus, G. Konstantinou, J. Pou, S. Ceballos, and V. G. Agelidis, "Comparison of phase-shifted and level-shifted pwm in the modular multilevel converter," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, May 2014, pp. 3764–3770.

[55] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, R. Picas, and V. Agelidis, "A modified voltage balancing algorithm for the modular multilevel converter: Evaluation for staircase and phase-disposition pwm," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4119–4127, Aug 2015.

[56] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 298–306, Jan 2011.

[57] P. Hu and D. Jiang, "A level-increased nearest level modulation method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1836–1842, Apr 2015.

[58] A. Perez-Basante, S. Ceballos, G. Konstantinou, M. Liserre, J. Pou, and I. M. de Alegria, "Circulating current control for modular multilevel converter based on selective harmonic elimination with ultra-low switching frequency," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–10.

[59] M. Moranchel, E. J. Bueno, F. J. Rodriguez, and I. Sanz, "Selective harmonic elimination modulation for medium voltage modular multilevel converter," in *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2016, pp. 1–6.

[60] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3482–3494, Aug 2012.

[61] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back hvdc system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct 2010.

[62] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel pwm inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul 2010.

[63] H. Mohammadi and M. Bina, "A transformerless medium-voltage statcom topology based on extended modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1534–1545, May 2011.

[64] M. Hagiwara, R. Maeda, and H. Akagi, "Negative-sequence reactive-power control by a pwm statcom based on a modular multilevel cascade converter (mmcc-sdbc)," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 720–729, Mar 2012.

[65] G. Bergna, A. Garcés, E. Berne, P. Egrot, A. Arzandé, J. C. Vannier, and M. Molinas, "A generalized power control approach in abc frame for modular multilevel converter hvdc links based on mathematical optimization," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 386–394, Feb 2014.

[66] G. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. Williams, and J. McDonald, "Modular multilevel inverter: Pulse width modulation and capacitor balancing technique," *IET Power Electron.*, vol. 3, no. 5, pp. 702–715, Sept 2010.

[67] Y. Zhang, G. Adam, T. Lim, S. Finney, and B. Williams, "Analysis of modular multilevel converter capacitor voltage balancing based on phase voltage redundant states," *IET Power Electron.*, vol. 5, no. 6, pp. 726–738, Jul 2012.

[68] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul 2009.

[69] S. Du, J. Liu, and T. Liu, "Modulation and closed-loop-based dc capacitor voltage control for mmc with fundamental switching frequency," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 327–338, Jan 2015.

[70] S. Du and J. Liu, "A study on dc voltage control for chopper-cell-based modular multilevel converters in d-statcom application," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2030–2038, Oct 2013.

[71] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 66–76, Jan 2014.

[72] A. Gholizad and M. Farsadi, "A novel state-of-charge balancing method using improved staircase modulation of multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6107–6114, Oct 2016.

[73] J. Mei, B. Xiao, K. Shen, L. Tolbert, and J. Y. Zheng, "Modular multilevel inverter with new modulation method and its application to photovoltaic grid-connected generator," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5063–5073, Nov 2013.

[74] D. Siemaszko, "Fast sorting method for balancing capacitor voltages in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 463–470, Jan 2015.

[75] G. Konstantinou, M. Ciobotaru, and V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *IET Power Electron.*, vol. 6, no. 1, pp. 96–107, Jan 2013.

[76] P. Meshram and V. Borghate, "A simplified nearest level control (nlc) voltage balancing method for modular multilevel converter (mmc)," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 450–462, Jan 2015.

[77] E. Solas, G. Abad, J. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts - part i: Capacitor voltage balancing method," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4525–4535, Oct 2013.

[78] F. Deng and Z. Chen, "Voltage-balancing method for modular multilevel converters switched at grid frequency," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2835–2847, May 2015.

[79] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H.-P. Nee, "Open-loop control of modular multilevel converters using estimation of stored energy," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2516–2524, Nov 2011.

[80] P. Hu, D. Jiang, Y. Zhou, Y. Liang, J. Guo, and Z. Lin, "Energy-balancing control strategy for modular multilevel converters under submodule fault conditions," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 5021–5030, Sept 2014.

[81] A. Zama, S. A. Mansour, D. Frey, A. Benchaib, S. Bacha, and B. Luscan, "A comparative assessment of different balancing control algorithms for modular multilevel converter (mmc)," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–10.

[82] A. Leon and S. Amodeo, "Energy balancing improvement of modular multilevel converters under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1–10, 2016.

[83] A. Antonopoulos, L. Angquist, S. Norrga, K. Ilves, L. Harnefors, and H.-P. Nee, "Modular multilevel converter ac motor drives with constant torque from zero to nominal speed," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1982–1993, May 2014.

[84] S. Debnath, J. Qin, and M. Saeedifard, "Control and stability analysis of modular multilevel converter under low-frequency operation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5329–5339, Sept 2015.

[85] M. Spichartz, V. Staudt, and A. Steimel, "Analysis of the module-voltage fluctuations of the modular multilevel converter at variable speed drive applications," in *Optimization of Electrical and Electronic Equipment (OPTIM), 2012 13th International Conference on*, May 2012, pp. 751–758.

[86] Y. Okazaki, H. Matsui, M. Hagiwara, and H. Akagi, "Design considerations on the dc capacitor of each chopper cell in a modular multilevel cascade inverters (mmci-dscc) for medium-voltage motor drives," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, Sept 2014, pp. 3393–3400.

[87] J. Kolb, F. Kammerer, and M. Braun, "Dimensioning and design of a modular multilevel converter for drive applications," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, Sept 2012, pp. LS1a–1.1–1–LS1a–1.1–8.

[88] Q. Tu, Z. Xu, Y. Chang, and L. Guan, "Suppressing dc voltage ripples of mmc-hvdc under unbalanced grid conditions," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1332–1338, Jul 2012.

[89] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, L. Angquist, and H.-P. Nee, "Capacitor voltage ripple shaping in modular multilevel converters allowing for operating region extension," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, Nov 2011, pp. 4403–4408.

[90] J. Pou, S. Ceballos, G. Konstantinou, V. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 777–788, Feb 2015.

[91] R. Picas, S. Ceballos, J. Pou, J. Zaragoza, G. Konstantinou, and V. Agelidis, "Closed-loop discontinuous modulation technique for capacitor voltage ripples and switching losses reduction in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4714–4725, Sept 2015.

[92] M. Huang, J. Zou, and X. Ma, "An improved phase-shifted carrier modulation for modular multilevel converter to suppress the influence of fluctuation of capacitor voltage," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7404–7416, Oct 2016.

[93] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation-suppression methods of floating capacitors in a new modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1943–1954, May 2013.

[94] M. Hagiwara, I. Hasegawa, and H. Akagi, "Start-up and low-speed operation of an electric motor driven by a modular multilevel cascade inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1556–1565, Jul 2013.

[95] A. Korn, M. Winkelnkemper, and P. Steimer, "Low output frequency operation of the modular multi-level converter," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, Sept 2010, pp. 3993–3997.

[96] M. Perez and S. Bernet, "Capacitor voltage ripple minimization in modular multilevel converters," in *Industrial Technology (ICIT), 2015 IEEE International Conference on*, March 2015, pp. 3022–3027.

[97] R. Lizana, M. Perez, D. Arancibia, J. Espinoza, and J. Rodriguez, "Decoupled current model and control of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5382–5392, Sept 2015.

[98] R. Lizana, M. Perez, S. Bernet, J. Espinoza, and J. Rodriguez, "Control of arm capacitor voltages in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1774–1784, Feb 2016.

[99] B. Li, Y. Zhang, G. Wang, W. Sun, D. Xu, and W. Wang, "A modified modular multilevel converter with reduced capacitor voltage fluctuation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6108–6119, Oct 2015.

[100] S. Du, B. Wu, N. Zargari, and Z. Cheng, "A flying-capacitor modular multilevel converter (fc-mmc) for medium-voltage motor drive," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1–9, 2016.

[101] S. Du, B. Wu, K. Tian, N. R. Zargari, and Z. Cheng, "An active cross-connected modular multilevel converter (ac-mmc) for a medium-voltage motor drive," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4707–4717, Aug 2016.

[102] S. Teeuwsen, "Simplified dynamic model of a voltage-sourced converter with modular multilevel converter design," in *Power Systems Conference and Exposition, 2009. PSCE '09. IEEE/PES*, Mar 2009, pp. 1–6.

[103] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, and V. G. Agelidis, "Controllers for eliminating the ac components in the circulating current of modular multilevel converters," *IET Power Electron.*, vol. 9, no. 1, pp. 1–8, May 2016.

[104] Y. Li and F. Wang, "Arm inductance selection principle for modular multilevel converters with circulating current suppressing control," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, Mar 2013, pp. 1321–1325.

[105] L. Ängquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H. P. Nee, "Inner control of modular multilevel converters - an approach using open-loop estimation of stored energy," in *Power Electronics Conference (IPEC), 2010 International*, Jun 2010, pp. 1579–1585.

[106] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, and H. P. Nee, "Circulating current control in modular multilevel converters with fundamental switching frequency," in *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, vol. 1, Jun 2012, pp. 249–256.

[107] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul 2011.

[108] B. Bahrani, S. Debnath, and M. Saeedifard, "Circulating current suppression of the modular multilevel converter in a double-frequency rotating reference frame," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 783–792, Jan 2016.

[109] X. She and A. Huang, "Circulating current control of double-star chopper-cell modular multilevel converter for hvdc system," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Oct 2012, pp. 1234–1239.

[110] X. She, A. Huang, X. Ni, and R. Burgos, "Ac circulating currents suppression in modular multilevel converter," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Oct 2012, pp. 191–196.

[111] Z. Li, P. Wang, Z. Chu, H. Zhu, Y. Luo, and Y. Li, "An inner current suppressing method for modular multilevel converters," *IEEE Power Electron. Lett.*, vol. 28, no. 11, pp. 4873–4879, Nov 2013.

[112] M. Zhang, L. Huang, W. Yao, and Z. Lu, "Circulating harmonic current elimination of a cps-pwm-based modular multilevel converter with a plug-in repetitive controller," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2083–2097, Apr 2014.

[113] L. He, K. Zhang, J. Xiong, and S. Fan, "A repetitive control scheme for harmonic suppression of circulating current in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 471–481, Jan 2015.

[114] J.-W. Moon, C.-S. Kim, J.-W. Park, D.-W. Kang, and J.-M. Kim, "Circulating current control in mmc under the unbalanced voltage," *IEEE Trans. Power Del.*, vol. 28, no. 3, pp. 1952–1959, Jul 2013.

[115] Y. Zhou, D. Jiang, J. Guo, P. Hu, and Y. Liang, "Analysis and control of modular multilevel converters under unbalanced conditions," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 1986–1995, Oct 2013.

[116] Z. Yuebin, J. Daozhuo, G. Jie, H. Pengfei, and L. Zhiyong, "Control of modular multilevel converter based on stationary frame under unbalanced ac system," in *Digital Manufacturing and Automation (ICDMA), 2012 Third International Conference on*, Jul 2012, pp. 293–296.

[117] S. Li, X. Wang, Z. Yao, T. Li, and Z. Peng, "Circulating current suppressing strategy for mmc-hvdc based on nonideal proportional resonant controllers under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 387–397, Jan 2015.

[118] J.-W. Moon, J.-W. Park, D.-W. Kang, and J.-M. Kim, "A control method of hvdc-modular multilevel converter based on arm current under the unbalanced voltage condition," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 529–536, Apr 2015.

[119] M. Guan and Z. Xu, "Modeling and control of a modular multilevel converter-based hvdc system under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4858–4867, Dec 2012.

[120] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzande, J.-C. Vannier, and M. Molinas, "An energy-based controller for hvdc modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2360–2371, Jun 2013.

[121] Y. Liang, J. Liu, T. Zhang, and Q. Yang, "Arm current control strategy for mmc-hvdc under unbalanced conditions," *IEEE Trans. Power Del.*, vol. PP, no. 99, pp. 1–10, 2016.

[122] X. Shi, Z. Wang, B. Liu, Y. Liu, L. M. Tolbert, and F. Wang, "Characteristic investigation and control of a modular multilevel converter-based hvdc system under single-line-to-ground fault conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 408–421, Jan 2015.

[123] A. Das, H. Nademi, and L. Norum, "A method for charging and discharging capacitors in modular multilevel converter," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, Nov 2011, pp. 1058–1062.

[124] J. Xu, C. Zhao, B. Zhang, and L. Lu, "New precharge and submodule capacitor voltage balancing topologies of modular multilevel converter for vsc-hvdc application," in *Power and Energy Engineering Conference (APPEEC), 2011 Asia-Pacific*, Mar 2011, pp. 1–4.

[125] P. Wang, X. P. Zhang, P. F. Coventry, and R. Zhang, "Start-up control of an offshore integrated mmc multi-terminal hvdc system with reduced dc voltage," *IEEE Trans. Power Syst.*, vol. 31, no. 4, pp. 2740–2751, Jul 2016.

[126] K. Li and C. Zhao, "New technologies of modular multilevel converter for vsc-hvdc application," in *Power and Energy Engineering Conference (APPEEC), 2010 Asia-Pacific*, Mar 2010, pp. 1–4.

[127] K. Tian, B. Wu, S. Du, D. . Xu, Z. Cheng, and N. R. Zargari, "A simple and cost-effective precharge method for modular multilevel converters by using a low-voltage dc source," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5321–5329, Jul 2016.

[128] B. Li, D. Xu, Y. Zhang, R. Yang, G. Wang, W. Wang, and D. Xu, "Closed-loop precharge control of modular multilevel converters during start-up processes," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 524–531, Feb 2015.

[129] K. Shi, F. Shen, D. Lv, P. Lin, M. Chen, and D. Xu, "A novel start-up scheme for modular multilevel converter," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2012, pp. 4180–4187.

[130] J. Rodriguez and P. Cortes, *Predictive Control of Power Converters and Electrical Drives*, 1st ed. Chichester, UK: IEEE Wiley press, Mar. 2012.

[131] J. Rodriguez, M. P. Kazmierkowski, J. R. Espinoza, P. Zanchetta, H. Abu-Rub, H. A. Young, and C. A. Rojas, "State of the art of finite control set model predictive control in power electronics," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 1003–1016, May 2013.

[132] J. Rodriguez, J. Pontt, C. Silva, P. Correa, P. Lezana, P. Cortes, and U. Ammann, "Predictive current control of a voltage source inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 495–503, Feb 2007.

[133] C. Xia, T. Liu, T. Shi, and Z. Song, "A simplified finite-control-set model-predictive control for power converters," *IEEE Trans. Ind. Electron.*, vol. 10, no. 2, pp. 991–1002, May 2014.

[134] S. Vazquez, J. I. Leon, L. G. Franquelo, J. Rodriguez, H. A. Young, A. Marquez, and P. Zanchetta, "Model predictive control: A review of its applications in power electronics," *IEEE Ind. Electron. Mag.*, vol. 8, no. 1, pp. 16–31, Mar 2014.

[135] V. Yaramasu, B. Wu, M. Rivera, J. Rodriguez, and A. Wilson, "Cost-function based predictive voltage control of two-level four-leg inverters using two step prediction horizon for standalone power systems," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, Feb 2012, pp. 128–135.

[136] S. A. Davari, D. A. Khaburi, and R. Kennel, "An improved fcs-mpc algorithm for an induction motor with an imposed optimized weighting factor," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1540–1551, Mar 2012.

[137] P. Cortes, S. Kouro, B. La Rocca, R. Vargas, J. Rodriguez, J. Leon, S. Vazquez, and L. Franquelo, in *Industrial Technology, 2009. ICIT 2009. IEEE International Conference on*, Feb 2009, pp. 1–7.

[138] V. Yaramasu, B. Wu, M. Rivera, M. Narimani, S. Kouro, and J. Rodriguez, "Generalised approach for predictive control with common-mode voltage mitigation in multilevel diode-clamped converters," *IET Power Electron.*, vol. 8, no. 8, pp. 1440–1450, Jul 2015.

[139] V. Yaramasu and B. Wu, "Model predictive decoupled active and reactive power control for high-power grid-connected four-level diode-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3407–3416, Jul 2014.

[140] T. Geyer and S. Mastellone, "Model predictive direct torque control of a five-level anpc converter drive system," *IEEE Trans. Ind. Appl.*, vol. 48, no. 5, pp. 1565–1575, Sept 2012.

[141] P. Lezana, R. Aguilera, and D. Quevedo, "Model predictive control of an asymmetric flying capacitor converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1839–1846, Jun 2009.

[142] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded h-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2691–2699, Aug 2010.

[143] R. Vargas, J. Rodriguez, C. Rojas, and M. Rivera, "Predictive control of an induction machine fed by a matrix converter with increased efficiency and reduced common-mode voltage," *IEEE Trans. Energy Convers.*, vol. 29, no. 2, pp. 473–485, Jun 2014.

[144] M. Perez, P. Cortes, and J. Rodriguez, "Predictive control algorithm technique for multilevel asymmetric cascaded h-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4354–4361, Dec 2008.

[145] M. Narimani, B. Wu, V. Yaramasu, and N. Reza Zargari, "Finite control-set model predictive control (fcs-mpc) of nested neutral point-clamped (nnpc) converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7262–7269, Dec 2015.

[146] J. Bocker, B. Freudenberg, A. The, and S. Dieckerhoff, "Experimental comparison of model predictive control and cascaded control of the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 422–430, Jan 2015.

[147] B. Riar, T. Geyer, and U. Madawala, "Model predictive direct current control of modular multilevel converters: Modeling, analysis, and experimental evaluation," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 431–439, Jan 2015.

[148] J. Qin and M. Saeedifard, "Predictive control of a modular multilevel converter for a back-to-back hvdc system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1538–1547, Jul 2012.

[149] L. Ben-Brahim, A. Gastli, M. Trabelsi, K. A. Ghazi, M. Houchati, and H. Abu-Rub, "Modular multilevel converter circulating current reduction using model predictive control," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3857–3866, June 2016.

[150] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Predictive sorting algorithm for modular multilevel converters minimizing the spread in the submodule capacitor voltages," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 440–449, Jan 2015.

[151] F. Zhang and G. Joos, "A predictive nearest level control of modular multilevel converter," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, Mar 2015, pp. 2846–2851.

[152] M. Vatani, B. Bahrani, M. Saeedifard, and M. Hovd, "Indirect finite control set model predictive control of modular multilevel converters," *IEEE Trans. Smart Grid*, vol. 6, no. 3, pp. 1520–1529, May 2015.

[153] P. Liu, Y. Wang, W. Cong, and W. Lei, "Grouping-sorting-optimized model predictive control for modular multilevel converter with reduced computational load," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1896–1907, Mar 2016.

[154] Z. Gong, P. Dai, X. Yuan, X. Wu, and G. Guo, "Design and experimental evaluation of fast model predictive control for modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3845–3856, June 2016.

[155] J.-W. Moon, J.-S. Gwon, J.-W. Park, D.-W. Kang, and J.-M. Kim, "Model predictive control with a reduced number of considered states in a modular multilevel converter for hvdc system," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 608–617, Apr, 2015.

[156] F. Deng and Z. Chen, "Elimination of dc-link current ripple for modular multilevel converters with capacitor voltage-balancing pulse-shifted carrier pwm," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 284–296, Jan 2015.

[157] V. Somasekhar, S. Srinivas, and K. Kumar, "Effect of zero-vector placement in a dual-inverter fed open-end winding induction-motor drive with a decoupled space-vector pwm strategy," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2497–2505, Jun 2008.

[158] B. Reddy, V. Somasekhar, and Y. Kalyan, "Decoupled space-vector pwm strategies for a four-level asymmetrical open-end winding induction motor drive with waveform symmetries," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5130–5141, Nov 2011.

[159] A. Gupta and A. Khambadkone, "A space vector pwm scheme for multilevel inverters based on two-level space vector pwm," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1631–1639, Oct 2006.

[160] N.-Y. Dai, M.-C. Wong, Y.-H. Chen, and Y.-D. Han, "A 3-d generalized direct pwm algorithm for multilevel converters," *IEEE Power Electron. Lett.*, vol. 3, no. 3, pp. 85–88, Sept 2005.

[161] N.-Y. Dai, M.-C. Wong, and Y.-D. Han, "Application of a three-level npc inverter as a three-phase four-wire power quality compensator by generalized 3dsvm," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 440–449, Mar 2006.

[162] L. Franquelo, M. Prats, R. Portillo, J. Galvan, M. Perales, J. Carrasco, E. Diez, and J. Jimenez, "Three-dimensional space-vector modulation algorithm for four-leg multilevel converters using abc coordinates," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 458–466, Apr 2006.

[163] E. Solas, G. Abad, J. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts - part ii: Experimental validation and comparison for hvdc application," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4536–4545, Oct 2013.

[164] Y. Deng, Y. Wang, K. H. Teo, and R. G. Harley, "A simplified space vector modulation scheme for multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1873–1886, Mar 2016.

[165] M. Perales, M. Prats, R. Portillo, J. Mora, J. Leon, and L. Franquelo, "Three-dimensional space vector modulation in abc coordinates for four-leg voltage source converters," *IEEE Power Electron. Lett.*, vol. 1, no. 4, pp. 104–109, Dec 2003.

[166] M. Preindl and S. Bolognani, "Model predictive direct speed control with finite control set of pmsm drive systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 1007–1015, Feb 2013.

[167] V. Yaramasu and B. Wu, "Predictive control of a three-level boost converter and an npc inverter for high-power pmsg-based medium voltage wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5308–5322, Oct 2014.