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On-chip interconnects modeling and timing driven buffer insertion

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ON-CHIP INTERCONNECTS MODELING AND TIMING DRIVEN BUFFER INSERTION

By

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ABSTRACT

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With the increasing effect of on-chip interconnects on nowadays VLSI design performance, modeling of interconnects becomes a necessity. GAM, TPN, and AWE are well known methods that are used to map an interconnect to an equivalent electrical circuit. In this thesis, a general approach that considers z-parameters is developed which allows the generation of equivalent RC, RLC, and RLCG circuits for both T and Π configurations. The performance of these generated circuits is compared to H-spice simulations by measuring the effect of interconnects on the transition times and delays under different conditions such as input transition times, interconnect lengths and capacitive loads. As a result, the a-configuration of AWE method reveals consistently an acceptable performance which makes it a good candidate to be utilized for buffer insertion.

Buffer insertion is a popular technique used to reduce the delay of a long interconnect by segmenting it and inserting buffers among these segments. Therefore, the performance of this technique depends strongly on the accuracy of the considered interconnect model. However, using a model such as the RLCG of Π-configuration which is derived from using the AWE method is not practical due to the complexity accompanied by such model which makes the derivation of closed-form expressions very complicated. To overcome this dilemma, the selected configuration has been mapped to a simple equivalent RC circuit. As a consequence, a new RC representation of on-chip interconnects is developed. Moreover, depending on the developed RC model, the proposed buffer insertion technique shows superiority over previously published works.

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In my passion, to whom (my brother Adnan) who finish his life sacrificing, supporting and encouraging me to reach this successful time, I present this work.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF APPENDICES

LIST OF SYMBOLE AND NOTATIONS

r Interconnect resistance per unit length

l Interconnect inductance per unit length

c Interconnect inductance per unit length

g Interconnect conductance per unit length

R Interconnect resistance

L Interconnect inductance

C Interconnect capacitance

G Interconnect conductance

ℓ Interconnect length

v Signal propagation speed

t_{pd} Propagation delay

Z_o Line characteristic impedance

γ Propagation constant

α Signal attenuation

β Phase constant

ω System frequency

V_{in} Input voltage

V_o Output voltage

N Number of line segments

X_n The selected grid points on the interconnect

$(\,')$ Derivative

Z_n Circuit impedance

Y_n Circuit admittance

IC   Integrated circuit

$\ell_{crt.}$ The interconnect length where the interconnect delay is in linear proportion with its

       length

R_0 Output resistance of a unit inverter

C_0 Capacitance of a unit inverter

c_g Gate capacitance of a unit inverter

c_{d0} Drain capacitance of a unit inverter

R_d The output resistance of the driver buffer

C_L The gate capacitance of the load buffer

C_N Unit capacitance of NMOS transistor

h Buffer width

VLSI   Very Large Scale Integration

SoC   System on-Chip

MOS   Metal Oxide Semiconductor

KVL Kirtchhoff's Voltage Law

KCL Kirtschhoff's Current Law

TSMC   Taiwan Semiconductor Manufacturing Company

DSM   Deep sub-micron

a_n, b_n Frames coefficients

T, Π Network configurations

GAM Global Approximation Method

TPN Two-Port Network Method

AWE Asymptotic Waveform Evaluation Method

$U.A.$ Unit area

$No.S$ Number of segments

DWB Delay with buffers

DNB Delay without buffers

$d.trns.tme.$ Different transition times

$d.Loads$ Different loads

$d.L.$ Different interconnect lengths

$(20-80)\% \, Delay$ Transition time

CHAPTER 1

Introduction

With the continued down scaling of CMOS technology to reach nanometre scale and the requirement for high speed, (SoC) interconnect emerges as one of the main performance limiting factors. As a matter of fact, it has been shown in [1] that interconnect delay is more than the logic delay and reaches 70-80% of all signal delays in a chip at 0.18μm technology. Thus, modeling and accounting for interconnect effects as early as possible in the design process becomes a major concern of VLSI designers. Modeling an interconnect expresses the characterization of the interconnect and its effects on the circuit's performance. On-chip interconnects modeling historically began in 1959 when Fairchild Semiconductor took the first step towards manufacturing an integrated circuit IC. In those days, interconnect effects were ignored because interconnects were short and circuits were simple. Therefore, an interconnect was modeled as a short circuit. With the scaling of the minimum feature size, interconnect effects started to be considerable. The first interconnect effect had to be considered when interconnect capacitances had become comparable to the gate capacitance. Thus, an interconnect was modeled as a single lumped capacitance [2-4]. With the increase in the device densities per unit area, the interconnect density has also correspondingly increased. Thus, the cross-sectional area of interconnects had been reduced to provide more interconnect per unit area [5]. Also, the global wires across the chip increased in length. So, because of the decrease in the cross-sectional area and increase in the interconnect length, the interconnect resistance could no longer be neglected and had to be considered in interconnect modeling. Therefore, the interconnect was modeled as an RC circuit [6-8]. With the demand of increasing the speed of on-chip circuits and using wider wire for distributing the clock, especially in the global wires, the inductance effect of on-chip interconnects became more important. Therefore, accounting the interconnect inductance in the interconnect modeling is crucial [9-13]. Using multi-layer techniques to increase the functionality of on-chip circuits with long wires, the effects of the dielectric loss is considered to accurately model the interconnect effects [1], [14,15].

Interconnect delay is a major concern of System on-Chip design. Basically, the interconnect delay in SoC is due to the line resistance, capacitance, inductance and dielectric conductance. These

elements are in direct proportion to the interconnect length ($R = r.\ell$, $L = l.\ell$, $C = c.\ell$, $G = g.\ell$). Elmore delay modeling for an RC interconnect [16] shows that the interconnect delay is in quadratic proportion to the interconnect length ($t_{pd} \Rightarrow r.c.l^2$). This quadratic of interconnect delay with interconnect length significantly degrades the performance of VLSI circuits with long wires. In order to reduce this quadratic increase in delay with interconnect length, repeaters (or a series of CMOS inverters separated by interconnects) are inserted along these long interconnect lines to partition the lines into shorter sections, thereby reducing the total delay of the interconnect path [17-22].

Buffer insertion technique is shown to be an effective technique for interconnect delay optimization. Buffer insertion problem can be partitioned into sizing as well as segment length and width determination. Some authors considered these two problems independently [23,24]. While others tackled both problems [25- 31].

In this thesis we derive general z-parameter models for both T and Π configurations targeting the Global Approximation Method (GAM), Two-Port Network (TPN) and Asymptotic Waveform Evaluation (AWE). The general z-parameter models allow easy and directly switching between the RC, RLC and RLCG models for both T and Π configurations for GAM, TPN and AWE modeling techniques. The interconnect RC, RLC and RLCG models were tested for different interconnect lengths, capacitive loads and input transition times and are presented in this thesis. The test results show that the RLCG model of the Π configuration which was derived from using the AWE method exhibits more acceptable, satisfactory and consistent results than other models. Thus, this model was selected as the candidate model for buffer insertion analysis. We will use this model to reduce the on-chip interconnect delay by considering the buffer insertion technique and Elmore delay modeling. By using this model, it is difficult to derive the closed-form expression for the on-chip interconnect delay based on the Elmore delay model Because of the model complexity. Therefore, modifying the model is crucial. Some modifications have been applied on the model to reduce this complexity. The first modification was eliminating the effect of the dielectric loss from the model and converting the model from RLCG model to RLC model. The second modification was mapping the interconnect RLC model into the RC model. The effect of the interconnect inductance is

compensated in the RC model. This generates an improved RC model. This model has a negative capacitance connected in the upstream of the model. We modified it to the down stream of the model and generated an equivalent RC model. This model is simple and easy to use for calculating the on-chip interconnect delay using buffer insertion technique. Moreover, this model has the simplicity of general RC model and the accuracy of the RLC model.

The thesis is organized as follows: The history of the interconnect modeling in VLSI circuits is briefly reviewed in Chapter 2. Model characterizations are also reviewed in chapter 2 which is started from the simple model represented as a short circuit and changes with time to C, RC, RLC and RLCG [2-8],[9-13],[32-35],[36-64]. Also, in Chapter 2, basic transmission line theory is briefly reviewed. The theory of transmission lines is discussed for types of transmission lines: lossless LC transmission lines, lossy RLCG transmission lines. Furthermore, brief discussions on the GAM, TPN and AWE methods are addressed.

Z-parameters of Telegraph equations are derived in Chapter 3. A general form of z-parameters of both T and Π configurations from using the GAM, the TPN and the AWE are presented respectively. Using these general z-parameter models, eighteen different RC, RLC and RLCG models are generated.

In chapter 4, the comparison for the vdd/2 and transition time between the H-spice and the RLCG models of T and Π configurations which were derived from using the GAM, TPN and AWE methods for different interconnect lengths, input transition times and capacitive loads was introduced. The comparison revealed that the RLCG model of the Π configuration which is derived from using the AWE method exhibits more acceptable and satisfactory results than other models.

The buffer insertion technique is used in Chapter 5 to reduce the on-chip interconnect delay. The equivalent RC model was considered and the Elmore delay model was used to derive closed-form expressions for the interconnect critical length, minimum buffer sizing and optimum interconnect delay. In this chapter, these closed-form expressions were compared with other studies.

Conclusions and future works are provided in Chapter 6. In Appendix A, a general z-parameter model of the T configuration is presented based on the AWE method. A general z-parameter model is derived based on the AWE method for the Π configuration in Appendix B. In Appendix C, closed-form expressions for interconnect critical length, minimum buffer sizing and optimal interconnect delay are derived.

CHAPTER 2

Background

2.1 Introduction

In VLSI, interconnect can be defined as the path, usually a metal line, that joins two or more points in the circuit. When a signal propagates through it, it exhibits some responses which affect the signal behaviour and integrity. Interconnect responses against the propagation signal such as delay, noise, reflection, etc. depends on many factors which may be grouped as interconnect and signal dependent factors. The first group includes factors such as interconnect dimensions, material, etc. The second group consists of factors such as the signal's amplitude, transition time, etc.

With the down scaling of technology, interconnects start to play a major role in determining the design performance. Thus, this chapter is dedicated for reviewing the state of the art of on-chip interconnect modeling.

2.2 Interconnect Models

On-chip interconnect modeling tries to describe the behaviour of on-chip interconnects in terms of their dimensions, materials, and propagation signal properties. Accurate models are the models which are able to characterize the interconnect behaviour accurately to reach the real behaviour. Interconnect modeling can be classified based on the signal wavelength into: lumped and distributed models.

2.2.1 Interconnect Lumped Models

Interconnects have a distributed nature and they should be modeled accordingly. However, when the signal wavelength is larger than the interconnect length, modeling interconnects as lumped elements provides good accuracy and reduce the modeling complexity. Therefore, for high-speed digital circuits, local interconnects, which is the majority of on-chip interconnects, can be safely treated as lumped models because their lengths are negligible compared to the wavelength of the traveling signals [1].

2.2.1.1 C- Lumped Models

In the 1990s, when the gate's capacitance dominated the interconnect's parasitic capacitance, interconnects were modeled as short circuits. However, with the scaling of the minimum feature, the interconnect parasitic capacitance became comparable to the gate capacitance. Thus, an interconnect was modeled as a lumped capacitance [2- 4]. As shown in Figure 2
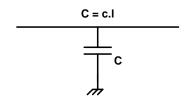
Figure 2.1: Interconnect lumped capacitive model.

In Figure 2.1, $C = c.\ell$ where C is the line capacitance, c is the line capacitance per unit length and ℓ is the interconnect length.

2.2.1.2 RC- Lumped Models

The resistance effect of on-chip interconnect is significant for global interconnects and it becomes even more prominent with the technology downscaling [5-6]. For such interconnects, modeling the resistance effect is necessary to achieve good accuracy. Figure 2.2 shows an RC-lumped interconnect modeling.
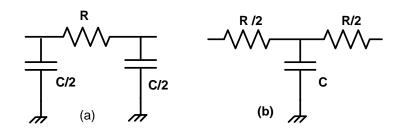
Figure 2.2: Interconnect lumped RC model (a) Π-configuration (b) T- configuration.

In Figure 2.2, $R = r.\ell$ where R is the line resistance, $C = c.\ell$ where C is the line resistance and c, r are interconnect unit capacitance and resistance respectively.

As illustrated in Figures 2.1, the C-lumped model has only one node. So, there is no voltage difference along the line whereas the RC-lumped model as shown in Figure 2.2 has two nodes in

the Π-configuration and three nodes in the T- configuration. Thus, the analysis of the RC-lumped model is more complicated than the C-lumped model due to the changes in the node voltages [7, 8], [32-35].

2.2.1.3 RLC- Lumped Models

The increased demand for faster VLSI chips pushes ASIC designers to use the wide wire upper metal layers [9- 13], [36- 55]. For global interconnects such as clock distribution, moreover, this also pushes the industry to develop low resistivity materials such as copper [42, 46] and low k materials to reduce the interconnect capacitance [42, 46]. These advance technologies allowed longer and denser interconnects which increased the inductance effect. Thus, modeling such interconnects considers their inductance effects [54]. Therefore, interconnects are modeled as lumped RLC circuits as shown in Figure 2.3.
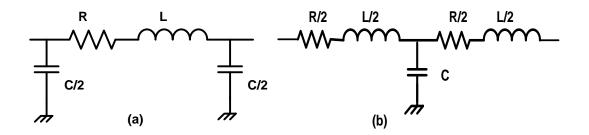
Figure 2.3: Interconnect lumped RLC model (a) Π-configuration (b) T-configuration.

In Figure 2.3, $L = l.\ell$ where L is the line inductance and l is the line inductance per unit length.

The amount of inductance effects presented in an RLC line depends on the ratio between the RC and the LC time constant of the line [55]. Hence, as inductance effects increase, the LC time constant dominates the RC time constant.

By combining all these effects with the dielectric loss G, RLCG configuration becomes necessary to characterize the behaviour of the interconnect accurately.

2.2.1.4 RLCG- Lumped Models

In VLSI circuit fabrication, G represents the conductivity of the dielectric layers such as silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) located between an interconnect and the substrate layer. Generally, there are many benefits from using dielectric layers in the chip fabrication. First of all, they are used to isolate active circuits from each other and to provide mechanical and chemical protection to the device itself. Second, dielectric layers are widely used in the fabrication of components essential to circuit functionality such as capacitors and MOS transistors. Lastly, dielectric layers are also used as masking materials during wafer fabrication. However, naturally there are no ideal dielectric materials. Thus, they reveal some conductivity. Although this conductivity is very low, it behaves as a path for the current to pass through it and cause power loss. This loss will affect the signal integrity and delay [56, 57]. This loss has to be considered in the interconnect modeling to represent the real behaviour of the interconnect. In this case, the interconnect takes another shape of configuration, which is the RLCG model as shown in Figure 2.4, where $G = g.\ell$, G is the line conductance and g is the line conductance per unit length.
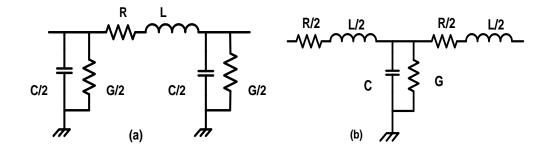
Figure 2.4: Interconnect lumped RLCG model (a) Π- configuration (b) T- configuration.

2.2.2 Distributed Transmission Line Models

When the signal transition time becomes less than or comparable to the signal traveling time on interconnects, lumped models do not characterize the behaviour of interconnects with adequate accuracy. Therefore, the distributed transmission line models are needed to fully consider this behaviour. Figures (2.5-2.10) represent the equivalent circuits of the distributed 2T and 2Π models for one lump of interconnect T and Π configurations [64].
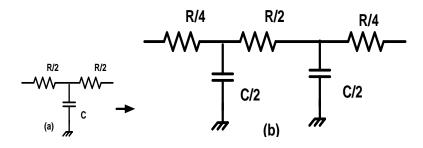
Figure 2.5: Lumped circuit approximations for distributed RC Lines (a) RC T- configuration (b) RC 2T- configuration.
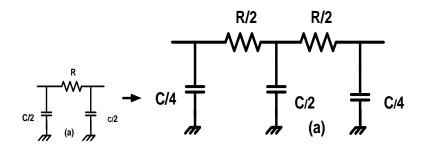
Figure 2.6: Lumped circuit approximations for distributed RC Lines (a) RC Π- configuration (b) RC 2Π- configuration.
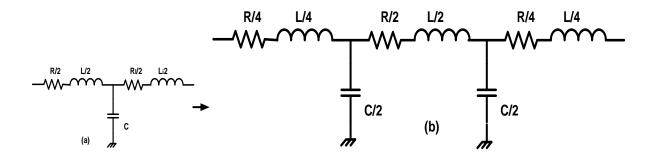
Figure 2.7: Lumped circuit approximations for distributed RLC Lines (a) RLC T- configuration (b) RLC 2T- configuration.
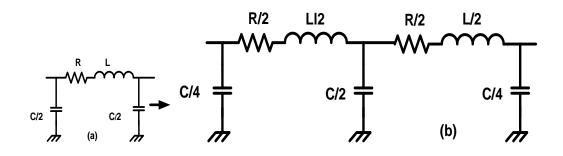
Figure 2.8: Lumped circuit approximations for distributed RLC Lines (a) RLC Π- configuration (b) RLC 2Π- configuration.
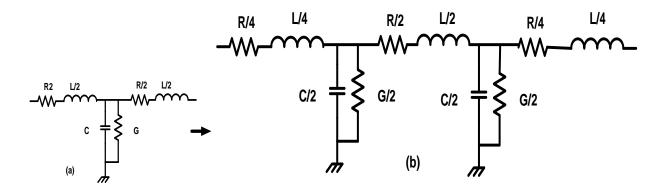
Figure 2.9: Lumped circuit approximations for distributed RLCG Lines (a) RLCG T- configuration (b) RLCG 2T- configuration.
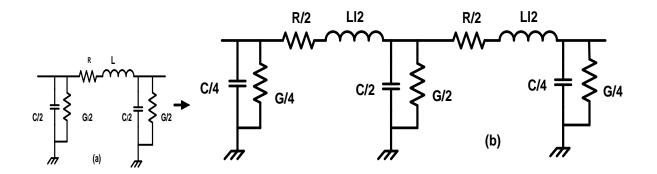
Figure 2.10: Lumped circuit approximations for distributed RLCG Lines (a) RLCG Π- configuration (b) RLCG 2Π- configuration.

2.3 Transmission Line Theory

Transmission line theory discusses the behaviour of a transmission line during signal propagation. When an electrical signal propagates through a transmission line, the voltage and current along the transmission line can vary in magnitude and phase as a function of position. Therefore, standard circuit theory cannot be employed on an electrical network; an alternative analysis must be applied to the system. As we know, transmission line theory represents a traditional topic in electrical engineering, especially in the area of power transmission. This topic received renewed attention because transmission line theory has found new and important applications in the area of high-speed VLSI circuits. Interconnect in a high-speed VLSI circuit reveals nonlinear delay effects. So, the interconnect can be modeled as a transmission line loaded with nonlinear element such as a capacitance. This nonlinearity may lead to many new effects such as instability and generation of higher order harmonics. The mathematical models of transmission lines with nonlinear loads consist of the linear partial differential equations describing the current and voltage dynamics along the lines together with the nonlinear boundary conditions imposed by the nonlinear loads connected to the lines. These nonlinear boundary conditions make the mathematical treatment very difficult. Moreover, in a high-speed VLSI circuit, the transmission line is stripped compared with the wavelength, and the transmission line can be characterized by the propagation constant and characteristic impedance.

2.3.1 Transmission Lines

The transmission line, as the name implies, is the line used to transmit an electrical signal from one point to another. When the electrical signal propagates through the transmission line, the line exhibits resistive, capacitive, inductive and conductive effects against the signal. Therefore, the line in a VLSI circuits can be modeled as a transmission line which is composed of interconnect series resistance, series inductance, shunt capacitance and shunt conductance, R, L, C and G respectively, as illustrated in Figure 2.11. The resistance R comes from the self resistance of the interconnect itself (the resistance of the materials used for interconnect); the inductance L represents the interconnect self inductance; the capacitance C is mainly due to the capacitance formed between the interconnect and the substrate layers; and the conductance G represents the conductivity of the dielectric layers located between the interconnect and the substrate layer. Interconnect parasitic impedances push the line to deviate from the ideal characteristic impedance.

11

In VLSI chips, interconnects can be modeled as micro-strips or as parallel-plate transmission lines [58- 60]. The best signal transmission from one point to another on the transmission line can be reached if the losses across the transmission are low, if the attenuation and velocity of the waves across the transmission line are frequency independent and if the characteristic impedance of the transmission line and the source and load impedances are matched to prevent reflections [61- 63].
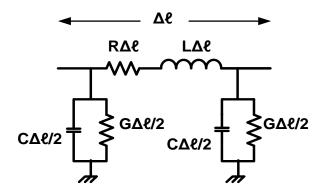
Figure 2.11: A section of an RLCG Π- configuration of transmission line.

Based on the interconnect loss, interconnects in VLSI circuits can be classified as: Lossless and Lossy transmission lines.

2.3.1.1 Lossless Transmission Lines

When the loss, which acts on the propagated signal on an interconnect in VLSI circuits due to the line elements (interconnect resistance and conductance) is ignored, the interconnect can be modeled as an LC model called a lossless transmission line model. To get a more accurate representation model, the interconnect is sampled into small pieces. Each piece represents small LC lumped circuit elements. These elements are distributed uniformly down the length of the line as shown in Figure 2.12.
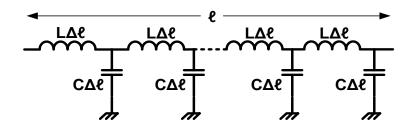
Figure 2.12: Equivalent circuit model of a lossless transmission line.

A lossless transmission line behaves as a short circuit at low frequencies because line inductance L can be represented as a short circuit whereas the line capacitance C can be represented as an open circuit. Therefore, a short circuit lossless transmission line at low frequencies represents an ideal medium for signal propagation. However, at high frequencies, the behaviour of a lossless transmission line is totally different than the short circuit representation. Delay of the propagation signal along the wire as well as the reflection is the most important two things that should be considered compared with the short circuit representation. In [64], lossless transmission line velocity, characteristic impedance and delay are calculated as illustrated in equations (2.1-2.3),

$$v = \frac{1}{\sqrt{lc}} \qquad (2.1)$$

$$Z_0 = \sqrt{\frac{l}{c}} \qquad (2.2)$$

$$t_{pd} = \frac{\ell}{v} \qquad (2.3)$$

where v is the velocity of the signal on the line, Z_0 is the line characteristic impedance and t_{pd} is the signal propagation delay.

2.3.1.2 Lossy Transmission Lines

When the loss is significant, the effects of the series resistance R and the dielectric conductance G should be included in the transmission line models. Figure 2.13 shows the equivalent circuit model of a lossy transmission line with distributed lumps of RLCG elements,
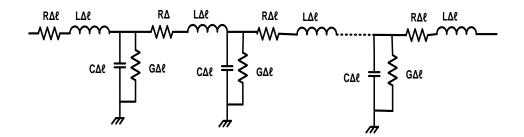
Figure 2.13: Equivalent RLCG circuit model of a lossy transmission line.

To describe Eq. (2.4), the characteristics of the wave propagation along the line (γ) is a complex number. The real part represents the signal attenuation (α) due to the line resistance and dielectric conductance. The imaginary part (β) represents the phase constant, which determines the speed of the propagation signal across the line. Thus γ can be expressed as

$$\gamma = \alpha + j\beta \tag{2.4}$$

For an RLCG lossy transmission line, the attenuation (α) can be described as in [64],

$$\alpha = \frac{r}{2Z_o} + \frac{gZ_o}{2} \tag{2.5}$$

Clearly, we can see from Eq. (2.5) that the attenuation of the lossy RLCG transmission line is directly proportional to line resistance and conductance. Also, if we neglect the effects of the line resistance and conductance, the attenuation will be zero and the line will be a lossless transmission line. The speed of the wave propagation along the transmission line for RLC and RLCG transmission lines as represented in [64] is

14

$$v = \frac{\omega}{\beta} \qquad\qquad (2.6)$$

where ω and β are the system frequency and the phase constant respectively.

From Eq. (2.6), we see that the speed of the signal across the transmission line will be frequency dependent.

2.4 Interconnects in VLSI Circuits

On-chip interconnect can be represented as series resistance R due to the line resistance and inductance L due to the interconnect inductance and shunt capacitance C due to the capacitance formed between the interconnect layer and the substrate and conductance G due to the conductivity of the dielectric layer. When a signal propagates through an interconnect, it takes a non-negligible amount of time, which is called interconnect delay or propagation delay, to travel from one end to the other. A large portion of this time is due to the time it takes to charge and discharge the capacitance of the wire and gate capacitance of the transistors through the interconnect resistance.

2.4.1 RC- Delay Models

For an RC circuit, delay can be characterized by the time constant RC. For on-chip interconnects, the delay of the signal mainly occurs due to the interconnect resistance R and the interconnect capacitance C. Interconnect resistance and capacitance are in direct proportion to the interconnect length. Based on the Elmore delay method [65], the delay of the RC line is in quadratic proportion to the interconnect length ($t_{pd} = RC \Rightarrow r.c.l^2$) as shown in Figure 2.14.
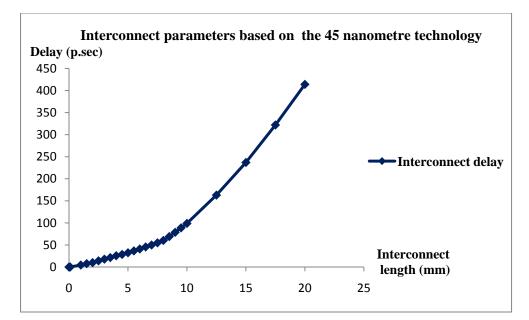
Figure 2.14: The relationship between the interconnect delay and interconnect length.

Figure 2.14 represents the changing of the interconnect delay with its length and a specific width. Clearly, we see that the interconnect delay increases nonlinearly with increasing the interconnect length. In addition, increasing interconnect length causes the delay to increase rapidly at a specific interconnect length (called critical length).

2.4.2 Elmore Delay Models

Elmore delay model [65] is widely used delay model in interconnect optimization. It is also the delay model used in this thesis. Despite its simplicity, Elmore delay model provides fairly good accuracy when compared with CAD tools such as H-spice. With an acceptable accuracy, on-chip interconnects and buffers can be replaced by an RC components. Therefore, interconnects and buffers become an RC circuit. At any point on the interconnect, the upstream resistance is equalled to the sum of the resistances from a driver (or a buffer before the point) to that point. The downstream capacitance is equalled to all capacitances from that point to a sink (or a buffer after the point). The Elmore delay model is basically a resistance-capacitance product. The Elmore delay along a signal path in the RC circuit is the sum of the delays associated with resistors in the path, where the delay is associated with a resistor is equalled to its resistance times its downstream capacitances as shown in Figure 2.15.
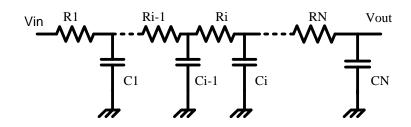
Figure 2.15: Distributed RC-model of interconnect.
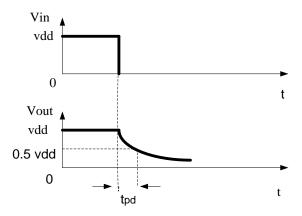
Figure 216: Delay calculation at vdd/2.

$$t_{pd} = C_N \frac{(R_1 + R_2 + ... + R_N)}{N} + ... + C_2 \frac{(R_1 + R_2)}{N-1} + C_1 R_1 \qquad (2.7)$$

For the uniform interconnect, line resistance and capacitance change with the length of the interconnect (interconnect thickness and width are constant). Then,

$$R_i = R\Delta\ell \text{ and } C_i = C\Delta\ell \qquad (2.8)$$

Eq. (2.7) can be expressed as

$$t_{p.d} = R(\Delta\ell)\frac{[C(\Delta\ell) + C(\Delta\ell) + ... + C(\Delta\ell)]}{N} \qquad (2.9)$$

$$t_{p.d} = R(\Delta\ell) \frac{[C(\Delta\ell) + C(\Delta\ell) + ... + C(\Delta\ell)]}{N+1} + ... + R(\Delta\ell)C(\Delta\ell) \qquad (2.10)$$

$$t_{p.d} = RC(\Delta\ell)^2 (1 + 2 + ... + N) \qquad (2.11)$$

$$t_{p.d} = RC(\Delta\ell)^2 \frac{N(N+1)}{2} \qquad (2.12)$$

where $\Delta\ell = \dfrac{\ell}{N}$, ($\ell$ represents the interconnect length, N represents the network sections), we have

$$t_{pd} = \frac{1}{2} RC\ell^2 \qquad (2.13)$$

Eq. 2.13 shows that the delay of the distributed RC modeled interconnect is in the quadratic proportion to the length of the interconnect.

There are many advantages and disadvantages for using the Elmore delay method. The advantages are simple closed-form expression, usefulness for interconnect optimization and good solutions compared with the H-spice delay model. However, the disadvantages are poor for slope computation and inability to handle inductance effects because it represents the first moment of the impulse response.

2.4.3 High Order Delay Models

For long interconnects where the effect of the parasitic inductance is crucial to achieve accurate modeling, many models that account for the inductance effect have been proposed [66- 69]. Zhou et al. [66] presented an analytical approach of a two-pole circuit approximation to provide a closed form solution. Kahng and Muddu [67] obtained an analytical delay model, based on first and second moments of RLC interconnection lines, that considers the effect of line inductance.

Subsequently, Tutuian et al. [68] found a stable time domain expression of the transfer function by matching the residues of the first two dominant poles with the first two moments of the transfer function. For more accurate methods, Pillage [69] proposed the asymptotic wave evaluation (AWE) method which matches the first moments of the transfer function. Later, more stable methods namely, pade via Lanczos (PVL) [70], matrix pade via Lanczos (MPVL) [71], Arnoldi algorithm

[72], block Arnoldi algorithm [73], and passive reduced order interconnect macromodeling algorithm (PRIMA) [74]. Moreover, G. Chen and Eby G. Friedman [75] have used Fourier analysis of an RLC interconnect modeling to find the transfer function, then they found the closed-form expression for the delay. These models are very accurate but need complex numerical computations.

2.5 Methodologies Used for Interconnect Modeling

In this section, we will discuss three well-known methods of characterizing on-chip interconnects: The GAM [76], TPN [77] and AWE [69] methods. The works in [78-80] have considered these three methods to find improvement models. In [78], Xu and Mazumder presented an RC macro-modeling of Π configuration using GAM and AWE methods. The work in [79] continued by presenting the RC T configuration using GAM method and also presented an RLC model for both T and Π configurations. Subsequently, Sun, et al., [80] obtained an RLC macro-modeling using TPN and AWE methods. The GAM, TPN and AWE methods will be explained briefly in the following sections.

2.5.1 Global Approximation Method (GAM)

The GAM is a method used to provide a mathematical approximation of a physical model. Depending on the range of its applicability, the mathematical approximation of a physical model can be classified as Local Approximation Method (LAM) (valid in the vicinity of a design point) or Global Approximation Method (GAM) (valid in the whole design space). LAM are usually based on Taylor series expansion at the current point using a function value and its first derivative, whereas GAM are normally based on the information taken in a series of points in the feasible design space.

The construction of a GAM relies on the sampling of the design space at X_n locations to obtain response values for the objective function. To apply this method to interconnect modeling, let us consider an interconnect of length ℓ [79] as shown in Figure 2.17, where X_n represents the selected grid points on the interconnect and V_i represents the voltages at selected grid points.
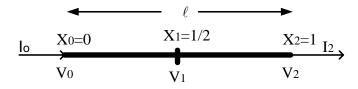
Figure 2.17: Interconnect with the assumption of the three grid points [79].

Along the line, three grid points have been selected:

$$x_0 = 0 \ , \ x_1 = \frac{1}{2} \ \text{and} \ x_2 = 1 \tag{2.14}$$

Voltages and currents at these points can be expressed in Laplace domain as follows:

$$V_0 = V(x_0,s) \ , \ V_1 = V(x_1,s) \ , \ V_2 = V(x_2,s) \tag{2.15}$$

$$I_0 = I(x_0,s) \ , \ I_1 = I(x_1,s) \ , \ I_2 = I(x_2,s) \tag{2.16}$$

To find the approximation frame for this interconnect, based on the GAM, the current differences for each two points equals the sum of the derivative currents for all branches between these two points [76].

$$I(x_2,s) - I(x_0,s) = a_1 I'(x_0,s) + a_2 I'(x_1,s) + a_3 I'(x_2,s) \tag{2.17}$$

The voltage difference between two points equals the sum of the derivative voltages of the outer points.

$$V(x_1,s) - V(x_0,s) = b_1 V'(x_0,s) + b_2 V'(x_2,s) \tag{2.18}$$

$$V(x_2,s) - V(x_1,s) = b_3 V'(x_0,s) + b_4 V'(x_2,s) \tag{2.19}$$

The approximation frame has coefficients $a_1, a_2, a_3, b_1, b_2, b_3$ and b_4 and (') denotes the derivative with respect to x ($x \in [0,1]$) where x is the normalized interconnect length. The value of these coefficients can be found by using the generalized Galerkin's method [76]. The generalized Galerkin's method assumes that interconnect currents and voltages change with interconnect length. So, to find the current response at each point, the fitting function method is used to express the current based on the location (x). The power of (x) increases with the number of derivative of the current assumed in the frame as shown below:

$$I(x,s) = x \text{ as a fitting function} \tag{2.20}$$

Using this assumption to find the coefficients a_1, a_2 and a_3 used in Eq. (2.17), we get

At $I(x,s) = x$ $\tag{2.21}$

$$x_2 - x_0 = a_1 x' \big|_{x=x_0} + a_2 x' \big|_{x=x_1} + a_3 x' \big|_{x=x_2} \tag{2.22}$$

$$1 - 0 = a_1 + a_2 + a_3 \Rightarrow a_1 = 1 - a_2 - a_3 \tag{2.23}$$

$$I(x,s) = x^2 \tag{2.24}$$

$$x_2^2 - x_0^2 = a_1 (x^2)' \big|_{x=x_0} + a_2 (x^2)' \big|_{x=x_1} + a_3 (x^2)' \big| x = x_2 \tag{2.25}$$

$$1 = a_2 + 2a_3 \Rightarrow a_2 = 1 - 2a_3 \tag{2.26}$$

$$I(x,s) = x^3 \tag{2.27}$$

$$x_2^3 - x_0^3 = a_1 (x^3)' \big|_{x=x_0} + a_2 (x^3)' \big|_{x=x_1} + a_3 (x^3)' \big| x = x_2 \tag{2.28}$$

$$1 = \frac{3a_2}{4} + 3a_3 \Rightarrow a_3 = \frac{4 - 3a_2}{12} \tag{2.29}$$

From Eqs. (2.23, 2.26 and 2.29), we get

$$a_1 = \frac{1}{6}, a_2 = \frac{2}{3} \text{ and } a_3 = \frac{1}{6} \tag{2.30}$$

In the same way, to find the voltage response at each point, the fitting function method is used to express the voltage based on the location (x). Again, the power of (x) increases with the number of derivative of the voltages assumed in the frame as shown below:

Substituting $V'(x,s) = x$ and x^2 as the fitting functions used in Eq. (2.18), yield

$$b_1 = \frac{3}{8} \text{ and } b_2 = \frac{1}{8} \tag{2.31}$$

Also, $b_3 = \frac{1}{8}$ and $b_4 = \frac{3}{8}$ can be obtained in the same way from Eq. (2.19).

The approximation frame for interconnect current and voltage differences after applying the GAM and using the generalized Galerkin's method is

$$I(x_2,s) - I(x_0,s) = \frac{1}{6}I'(x_0,s) + \frac{2}{3}I'(x_1,s) + \frac{1}{6}I'(x_2,s) \tag{2.32}$$

$$V(x_1,s) - V(x_0,s) = \frac{3}{8}V'(x_0,s) + \frac{1}{8}V'(x_2,s) \tag{2.33}$$

$$V(x_2,s) - V(x_1,s) = \frac{1}{8}V'(x_0,s) + \frac{3}{8}V'(x_2,s) \tag{2.34}$$

2.5.2 Two-Port Network (TPN)

TPN has two ports, each port is characterized by voltage and current variables as shown in Figure 2.18.
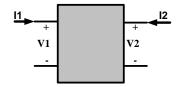
Figure 2.18: Shows the variables for a two-port network.

The subscript 1 is used to refer to the variables at the input port (at the left) and the subscript 2 to refer to the variables at the output port (at the right). At both of these ports the variables are defined so that their relative reference directions obey the usual convention (input and output current for each port should be equal). Since we now have four variables, it requires two equations to relate these variables. The general form of these equations is expressed as

$$U_1(s) = K_{11}(s)W_1(s) + K_{12}(s)W_2(s) \tag{2.35}$$

$$U_2(s) = K_{21}(s)W_1(s) + K_{22}(s)W_2(s) \tag{2.36}$$

where the quantities $U_1(s), U_2(s)$, $W_1(s)$ and $W_2(s)$ maybe any of the voltage and current variables $V_1(s), V_2(s)$ $I_1(s)$ or $I_2(s)$. Coefficients $K_{ij}(s)$ are the network functions that relate these variables. Sometimes $K_{ij}(s)$ are called *network parameters*. There are six different possible combinations that can be used to represent $U_1(s)$ and $U_2(s)$ in Eqs. (2.35-2.36). A tabulation of these six possible combinations is given in Table 2.1.

Table 2.1: Six sets of network parameters for two-port network method.

case	$U_1(s)$	$U_2(s)$	$W_1(s)$	$W_2(s)$
1	$V_1(s)$	$V_2(s)$	$I_1(s)$	$I_2(s)$
2	$I_1(s)$	$I_2(s)$	$V_1(s)$	$V_2(s)$
3	$I_1(s)$	$V_2(s)$	$V_1(s)$	$I_2(s)$
4	$V_1(s)$	$I_2(s)$	$I_1(s)$	$V_2(s)$
5	$V_1(s)$	$I_1(s)$	$V_2(s)$	$-I_2(s)$
6	$V_2(s)$	$I_2(s)$	$V_1(s)$	$-I_1(s)$

Here we may note that any one of these six sets of parameters (if it exists) has the property completely characterizes the network. Also, any set can be utilized to find other sets of parameters [77].

The general TPN configuration shown in Figure 2.19 has four individual terminals. It is theoretically possible to define four current variables rather than the two shown in the Figure 2.18. The requirement of a network port is that the current into one of the port terminals, at every instant of time, equals the current out of the other terminal of the port. This is called the *port current requirement* and it is illustrated in Figure 2.19. Most of the situations to which TPNs are applied automatically satisfy this requirement. If a port is open-circuited (i.e. if nothing is connected to it), the currents at the two terminals defining the port are zero. Thus the requirement is satisfied. When the case where any *two-terminal elements* (including a short circuit) are connected to the port, the currents into and out of the two-terminal element must be equal, the port current requirement is always satisfied in this case. The requirement is also satisfied for the case where a group of two-port networks is connected in cascade as shown in Figure 2.20. Consider the first network (on the left) in the cascade. The restriction on the currents is satisfied at the input port of this network by the open circuit. KCL now requires that the sum of the other two-terminal currents must be zero; thus the port current requirement is satisfied. Since the requirement at the output port of the first network is met, it must also be satisfied at the input port of the second network since the ports are directly connected.
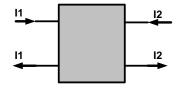
Figure 2.19: Current requirements of the ports.
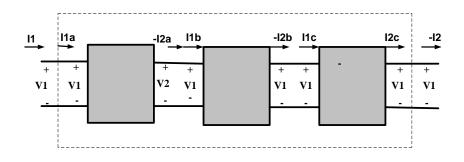
Figure 2.20: Cascade connections for two-port networks.

24

2.5.2.1 Z-Parameters in TPN Method

Table 2.1 shows that there are six ways in which the voltage and current variables of a TPN method may be selected so as to define a set of network functions. The first case in Table 2.1 will be considered to represent the z-parameter. We Choose $V_1(s)$ and $V_2(s)$ as the quantities $U_1(s)$ and $U_2(s)$ as shown in Eqs. (2.35) and (2.36) and $I_1(s)$ and $I_2(s)$ as the quantities and $W_2(s)$. Since the left members of the resulting set of equations have the dimensions of voltage, all the terms in the right members of these equations must also have the dimensions of voltage. Therefore, since the quantities $W_1(s)$ and $W_2(s)$ have the dimensions of current, this requires that coefficients $K_{ij}(s)$ have the same dimensions of impedance. Equations (2.35) and (2.36) can be written in the form of

$$V_1(s) = Z_{11}(s)I_1(s) + Z_{12}(s)I_2(s) \tag{2.37}$$

$$V_2(s) = Z_{21}(s)I_1(s) + Z_{22}(s)I_2(s) \tag{2.38}$$

Quantities $Z_{ij}(s)$ are called Z parameters. We can write equations (2.37) and (2.38) in the matrix form.

$$V(s) = \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} = \begin{bmatrix} Z_{11}(s) & Z_{12}(s) \\ Z_{21}(s) & Z_{22}(s) \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix} = Z(s)I(s) \tag{2.39}$$

Eq. (2.39) represents the z-parameter matrix where for a given set of z-parameters (shown in Eq. (2.39)), there are some commonly used network forms which may be used as circuit configurations. One of the well known methods of these forms is the " T " network configuration as show in Figure 2.21. When $Z_{12}(s)$ is equal to $Z_{21}(s)$, the network is reciprocal. Let us consider the T configuration of two-terminal impedances shown in Figure 2.21. The z-parameter matrix for this network is readily shown to be
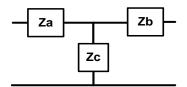
Figure 2.21: T-Configuration.

$$\begin{pmatrix} Z_{11}(s) & Z_{12}(s) \\ Z_{21}(s) & Z_{22}(s) \end{pmatrix} = \begin{pmatrix} Z_a(s) + Z_c(s) & Z_c(s) \\ Z_b(s) & Z_b(s) + Z_c(s) \end{pmatrix} \tag{2.40}$$

From the matrix above, the relations of the network elements Z_a, Z_b and Z_c as functions of the network parameters can be found from [77].

$$Z_a = Z_{11}(s) - Z_{12}(s) \tag{2.41}$$

$$Z_b = Z_{22}(s) - Z_{12}(s) \tag{2.42}$$

$$Z_c = Z_{12}(s) \tag{2.43}$$

Thus, the T-network may be redrawn with the expressions specifying the two-terminal impedances given directly in terms of z-parameters as shown in Figure 2.22.
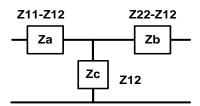
Figure 2.22: The equivalent z-parameter of T-model.

2.5.3 Asymptotic Waveform Evaluation (AWE) Method

The AWE was introduced in [69] as an efficient technique for the solution of linear circuits. It is a general method that applies to circuits consisting of all types of lumped, linear elements connected in any valid topology. The AWE method employs an efficient algorithm to compute the time moments of circuit responses. These moments are then matched via Pade approximation [70], a simple recursive formula method [106], or Maclaurin series projection [83] to reduced-order rational function models. The reduced-order models can be used to characterize the circuit's time and frequency.

In AWE, a Taylor series expression could be used to express the circuit response in a polynomial form. Then a simple recursive formula in [106] and the approaches in [83] are used to find the polynomial coefficients as illustrated below.

$$Y_{in}(s) = \frac{a_0 + a_1 s + ... + a_{2n-1}s^{2n-1}}{1 + b_1 s + ... + b_{2n-1}s^{2n}} \tag{2.44}$$

Eq. (2.44) can be expressed using a polynomial of order 2n-1, as in the Taylor series

$$Y_{in}(s) = Y_0 + Y_1 s + ... + Y_{2n-1}s^{2n-1} \tag{2.45}$$

The coefficients Y_k of Eq. (2.45) can be found by a simple recursive formula [106],

$$Y_k = a_k - \sum_{i=1}^{k} b_i Y_{k-i} \tag{2.46}$$

where $Y_{in}(s)$ is the input admittance of a circuit in s-domain, Y_k are the coefficients of the input admittance, a_k are the coefficients of the numerator of the input admittance equation, n is the number of the circuit sections , and b_i are the coefficients of the denominator of the input admittance.

2.6 Summary

In this chapter, the history of the interconnect modeling were briefly reviewed. The amendments of the interconnect modeling based on the interconnect effects in the circuits toward the accuracy are briefly addressed. Lumped and distributed interconnect models, namely C, RC, RLC, and RLCG, were addressed. A transmission line of lossy and lossless models was mentioned for RC and LC configurations respectively. Delay models based on interconnect RC configuration, Elmore method and high order delay methods were discussed. The GAM, TPN, and AWE methods were briefly reviewed. In each method, the derivation of an interconnect model is considered. These methods are fully considered in the next chapter.

CHAPTER 3

Generalizing the GAM, TPN and AWE Methods Using Z-Parameters

3. 1 Introduction

With the use of nano-meter technology, integrated circuits (ICs) have become more dense and more complex. Subsequently, interconnect delay has become the dominant factor in nano-meter design. The effects of interconnects on chip performance such as delay, crosstalk, and reflection are becoming critical factors in VLSI design [81].

In recent years also, various improvement methods have been proposed on the interconnect models [78-80]; an improved RC T-configuration based on the GAM and RC Π- configuration based on the AWE have been proposed in [78]. These models are not robust because they don't consider the effect of the interconnect inductance. In [79], improved RC and RLC models for both T and Π configurations based on the GAM have been proposed. Furthermore, improved RLC models for both T and Π configurations based on the TPN and AWE methods have been presented in [80]. Although these models exhibit good accuracy compared with H-spice, unfortunately, the complexity of using these methods prevents including the effect of the dielectric loss in their models. Therefore, generalizing these methods to find all the RC, RLC and RLCG models are crucial.

In this chapter, we generalized these methods into z-parameter models. We started to derive the Telegraph equations for the currents and voltages of a transmission line in z-parameter representation. A z-parameter of interconnect modeling for both T and Π configurations based on the GAM, TPN, and AWE is proposed. Eighteen different RC, RLC and RLCG models are easily generated from using the derived models.

3.2 Z-Parameter Representation for the Telegraph Equations

To derive the telegraph equation for the currents and voltages of a transmission line, we consider the general form using the z-parameter model where there are resistance, capacitance, inductance and/or conductance. Moreover, the distributed z-parameter model will be considered as shown in Figure 3.1.

In this section, telegraph equations for voltage and current differences of the interconnect-z-parameter model in s-domain have been derived.
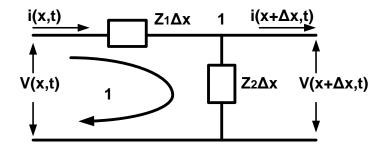
Figure 3.1: Distributed z-parameter model of a transmission line.

By applying KVL for loop1 of Figure 3.1, we get

$$v(x,t) = i(x,t)Z_1\Delta x + v(x+\Delta x,t)$$ (3.1)

$$v(x+\Delta x,t) - v(x,t) = -i(x,t)Z_1\Delta x$$ (3.2)

$$\frac{d\ v(x,t)}{dx} = \frac{\Delta v(x,t)}{\Delta x}\bigg|_{\Delta x\to 0} = -i(x,t)Z_1$$ (3.3)

Expressing Eq. (3.3) in s-domain, gives

$$\frac{dV(x,s)}{dx} = -I(x,s)Z_1$$ (3.4)

$$V'(x,s) = -Z_1 I(x,s)$$ (3.5)

By applying KCL at node1, results in

$$i(x,t) = i(x+\Delta x,t) + v(x+\Delta x,t)/Z_2\Delta x \tag{3.6}$$

$$i(x+\Delta x,t) - i(x,t) = -v(x+\Delta x,t)/Z_2\Delta x \tag{3.7}$$

$$\frac{\Delta i(x,t)}{\Delta x} = -v(x,t)/Z_2 \tag{3.8}$$

$$\frac{d(x,t)}{dx} = \frac{\Delta i(x,t)}{\Delta x}\bigg|_{\Delta x \to 0} = -v(x,t)/Z_2 \tag{3.9}$$

Expressing Eq. (3.9) in s-domain, yields

$$\frac{dI(x,s)}{dx} = -V(x,s)/Z_2 \tag{3.10}$$

$$I'(x,s) = -V(x,s)/Z_2 \tag{3.11}$$

Eqs. (3.5, 3.11) represent the Telegraph equations for voltages and currents difference of the z-parameter-transmission line in s-domain. From these equations, it is easy to get the telegraph equations of current and voltage difference for transmission line RC, RLC, or RLCG models as shown below:

For the RC distributed model, if we substitute $Z_1 = R$ and $Z_2 = \dfrac{1}{sC}$ in Eqs. (3.5, 3.11), we have

$$V'(x,s) = -RI(x,s) \tag{3.12}$$

$$I'(x,s) = -sCV(x,s) \tag{3.13}$$

For the RLC distributed model, substituting $Z_1 = R + sL$ and $Z_2 = \dfrac{1}{sC}$ in Eqs. (3.5, 3.11), we have

$$V'(x,s) = -(R+sL)I(x,s) \tag{3.14}$$

$$I'(x,s) = -sCV(x,s) \tag{3.15}$$

For the RLCG distributed model, substituting $Z_1 = R + sL$ and $Z_2 = \dfrac{1}{G + sC}$ in Eqs. (3.5, 3.11), we have

$$V'(x,s) = -(R + sL)I(x,s) \tag{3.16}$$

$$I'(x,s) = -(G + sC)V(x,s) \tag{3.17}$$

From all the results above, Eqs. (3.5, 3.11) represent the general z-parameter telegraph equations for transmission line currents and voltages. Therefore, Eqs. (3.5, 3.11) can be directly used to find RC, RLC and/or RLCG telegraph equations by replacing Z_1 and $\dfrac{1}{Z_2}$ with their actual components, where Z_1 is the impedance between the two points at which the voltages change, and $\dfrac{1}{Z_2}$ is the shunt admittance where the currents change.

3.3 Z-Parameter Modeling For Interconnect Based on GAM, TPN and AWE Methods

A general z-parameter interconnect modeling is a model which can be used to find an RC, RLC and/or RLCG interconnect model directly in both T and Π configurations. Three well known methods have been used for interconnect modeling: GAM, TPN and AWE. In this section, we will discuss all these three methods of analysing interconnects in z-parameter form and for each method, both T and Π configurations will be considered.

3.3.1 GAM Based Z-Parameter Modeling

z-parameter modeling using the GAM method is presented by deriving Telegraph equations for interconnect voltages and currents in z-parameters. The GAM method is taken for interconnect voltages and currents. Based on that, approximation frames for voltages and currents in z-parameters are obtained. The fitting function of the Galerkin's method is used to find the approximation frames coefficients. Some mathematical manipulations are applied on the frames. z-

parameter modeling for both T and Π configurations is derived. Z-parameter modeling based on the GAM method can be used easily to switch between the interconnect RC, RLC and RLCG modeling

3.3.1.1 Z-Parameters Derivation For T-Configuration

In this section, we will present the z-parameter model for an interconnect T-presentation based on the GAM. By considering Eqs. (3.5, 3.11), Eqs. (2.32-2.34), which are proposed in section 2.5.1, can be rewritten as:

$$I(x_2,s) - I(x_0,s) = -\frac{1}{6}\frac{V(x_0,s)}{Z_2} - \frac{2}{3}\frac{V(x_1,s)}{Z_2} - \frac{1}{6}\frac{V(x_2,s)}{Z_2} \tag{3.18}$$

$$V(x_1,s) - V(x_0,s) = -\frac{3}{8}I(x_0,s)Z_1 - \frac{1}{8}I(x_2,s)Z_1 \tag{3.19}$$

$$V(x_2,s) - V(x_1,s) = -\frac{1}{8}I(x_0,s)Z_1 - \frac{3}{8}I(x_2,s)Z_1 \tag{3.20}$$

Also, by considering Eqs. (2.15, 2.16) in section 2.5.1, Eqs. (3.18-3.20) above can be rewritten as

$$I_0 - I_2 = \frac{1}{6}\frac{V_0}{Z_2} + \frac{2}{3}\frac{V_1}{Z_2} + \frac{1}{6}\frac{V_2}{Z_2} \tag{3.21}$$

$$V_0 - V_1 = \frac{3}{8}Z_1I_0 + \frac{1}{8}Z_1I_2 \tag{3.22}$$

$$V_1 - V_2 = \frac{1}{8}Z_1I_0 + \frac{3}{8}Z_1I_2 \tag{3.23}$$

Eq. (3.22) can be rewritten as

$$V_1 = V_0 - \frac{3}{8}Z_1I_0 - \frac{1}{8}Z_1I_2 \tag{3.24}$$

Substituting Eq. (3.24) in equation (3.23), yields

$$V_2 = V_0 - \frac{3}{8}Z_1 I_0 - \frac{1}{8}Z_1 I_2 - \frac{1}{8}Z_1 I_0 - \frac{3}{8}Z_1 I_2 \qquad (3.25)$$

$$V_2 = V_0 - \frac{1}{2}Z_1 I_0 - \frac{1}{2}Z_1 I_2 \qquad (3.26)$$

$$V_0 - V_2 = \frac{1}{2}Z_1 I_0 + \frac{1}{2}Z_1 I_2 \qquad (3.27)$$

Depending on Eq.(3.27), the circuit can be constructed as shown in Figure 3.2.
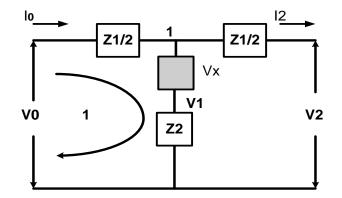
Figure 3.2: The circuit after manipulations of the voltage equations.

By applying KVL for loop 1 of Figure 3.2, we can write

$$V_0 = \frac{1}{2}Z_1 I_0 + V_1 + V_x \qquad (3.28)$$

$$V_0 - V_1 = \frac{1}{2}Z_1 I_0 + V_x \qquad (3.29)$$

Substituting Eq. (3.29) in Eq. (3.22), yields

$$\frac{1}{2}Z_1I_0 + V_x = \frac{3}{8}Z_1I_0 + \frac{1}{8}Z_1I_2 \qquad (3.30)$$

$$V_x = \frac{3}{8}Z_1I_0 - \frac{1}{2}Z_1I_0 + \frac{1}{8}Z_1I_2 \qquad (3.31)$$

$$V_x = -\frac{1}{8}Z_1(I_0 - I_2) \qquad (3.32)$$

So, from Eqs. (3.27, 3.32), the circuit can be presented as shown in Figure 3.3.
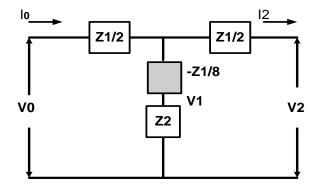
Figure 3.3: The z-parameter of T-configuration after the voltage and current equations are manipulated.

It can be seen that Eqs. (3.29, 3.32) represent the general form of the interconnect z-parameter for T-configuration based on the GAM. Figure 3.4 represents the interconnect T-configuration for RC, RLC and RLCG circuits based on the GAM as obtained from Eqs. (3.27, 3.32).
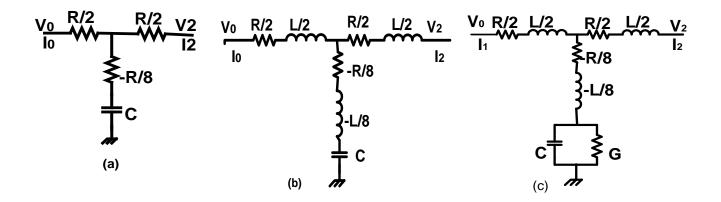
Figure 3.4: Interconnect T-configuration based on the GAM for (a) RC, (b) RLC and (c) RLCG interconnects.

In this section, we derived the z-parameter model of interconnects in T-configuration based on the GAM. In this model, the voltage differences of the line are expressed in Eq. (3.27) and the current differences are expressed in Eq. (3.32). Figures 3.4 (a, b and c) represent the result of the general z-parameter model in T-configuration based on the GAM for RC, RLC and RLCG models. Qinwei and Pinaki in [78] derived only the RC T-configuration based on GAM. They did not mention RLC and the RLCG models. Later on, the work in [79] mentioned both T and Π configurations for RC and RLC models based on the GAM but omitted RLCG models. Clearly, the revision of the z-parameter model revealed better results than the works in [78,79] because using the z-parameter model, we can easily find the T-configuration of the RC, RLC or RLCG interconnect models not only the RC or RLC model.

3.3.1.2 Z-Parameters Derivation for Π-Configuration

In this section, we derive the z-parameter model for on-chip interconnect for Π-configuration based on the GAM. Eqs. (3.5) and Eq. (3.11) represent the relationship of duality [80]. i.e., if we replace V(x, s) with I(x, s) and Z_1 with Z_2, then Eq. (3.5) and Eq. (3.11) become identical. This duality can also be applied to Eqs. (3.18-3.32) which results in another approximation frame.

$$V_0 - V_2 = \frac{1}{6} Z_1 I_0 + \frac{2}{3} Z_1 I_1 + \frac{1}{6} Z_1 I_2 \qquad (3.33)$$

$$I_0 - I_1 = \frac{3}{8}\frac{V_0}{Z_2} + \frac{1}{8}\frac{V_2}{Z_2} \qquad (3.34)$$

$$I_1 - I_2 = \frac{1}{8}\frac{V_0}{Z_2} + \frac{3}{8}\frac{V_2}{Z_2} \qquad (3.35)$$

Eqs. (3.34) can be rewritten as

$$I_1 = I_0 - \frac{3}{8}\frac{V_0}{Z_2} - \frac{1}{8}\frac{V_2}{Z_2} \qquad (3.36)$$

Substituting Eq. (3.36) in Eq. (3.35), we get

$$I_2 = I_0 - \frac{3}{8}\frac{V_0}{Z_2} - \frac{1}{8}\frac{V_2}{Z_2} - \frac{1}{8}\frac{V_0}{Z_2} - \frac{3}{8}\frac{V_2}{Z_2} \qquad (3.37)$$

$$I_0 - I_2 = \frac{1}{2}\frac{V_0}{Z_2} + \frac{1}{2}\frac{V_2}{Z_2} \qquad (3.38)$$

Based on Eq. (3.38), the circuit will be as shown in Figure 3.5.
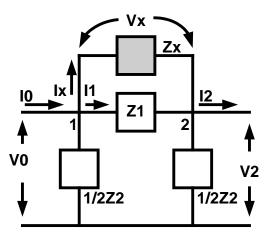
Figure 3.5: The circuit after manipulations of the current equations.

By considering KCL at node 1, we get

$$I_0 - I_1 = \frac{1}{2}\frac{V_0}{Z_2} + I_x \qquad (3.39)$$

Substituting Eq. (3.39) in Eq. (3.34), gives

$$\frac{1}{2}\frac{V_0}{Z_2} + I_x = \frac{3}{8}\frac{V_0}{Z_2} + \frac{1}{8}\frac{V_2}{Z_2} \qquad (3.40)$$

$$I_x = \frac{3}{8}\frac{V_0}{Z_2} - \frac{1}{2}\frac{V_0}{Z_2} + \frac{1}{8}\frac{V_2}{Z_2} \qquad (3.41)$$

$$I_x = -\frac{1}{8Z_2}(V_0 - V_2) \qquad (3.42)$$

So, from Eqs. (3.38) and Eq. (3.42), the circuit can be constructed as shown in Figure 3.6.
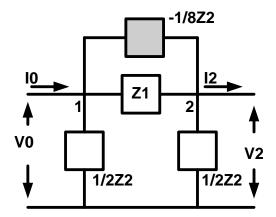
Figure 3.6: The z-parameter of Π-model after the voltage and current equations are manipulated.

It can be seen that Eqs. (3.38) and (3.42) represent the interconnect z-parameter of Π-configuration using the GAM. Figure 3.7 represents the interconnect of Π- configuration for RC, RLC and RLCG models after using Eqs. (3.38) and (3.42).
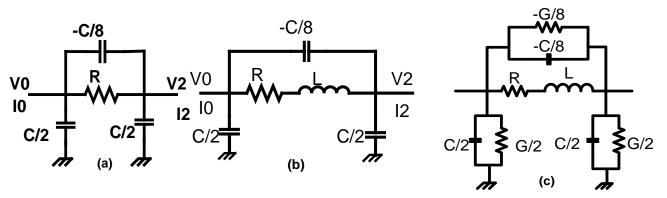
Figure 3.7: Interconnect Π- configuration based on the GAM for (a) RC, (b) RLC and (c) RLCG interconnects.

A z-parameter of interconnect modeling of Π configuration based on the GAM is derived in this section. Comparing this approach with the approaches in [78,80], a Π configuration based on the GAM is not mentioned in [78], whereas in [79], only an RC Π configuration exists. The z-parameter of the Π configuration, which is approached in this section, is better for modeling an on-chip interconnect. It is not limited to one configuration such as RC, RLC and/or RLCG configurations, but we can use it to find all interconnect models of the Π configuration as shown in Figure 3.7 (a, b and c).

3.3.2 TPN Based Z-Parameter Modeling

In the TPN method, it is possible by using Ohm's law to represent the physical circuit by parameters. This ability enables us to convert the matrix form into circuit parameters. Moreover, the TPN method enables us to use the duality between the T and Π configurations of interconnect models. In the following, we will address the z-parameter models in both T and Π configurations based on the TPN method.

3.3.2.1 Z-PARAMETER DERIVATION FOR T-CONFIGURATION

This section considers the TPN theory to find interconnect models for T-configuration. By considering Eqs. (3.21-3.23) and Eq. (3.22) can be rewritten as

$$V_1 = V_0 - \frac{3}{8} Z_1 I_0 - \frac{1}{8} Z_1 I_2 \tag{3.43}$$

Eq. (3.23) can be rearranged as

$$V_2 = V_1 - \frac{1}{8} Z_1 I_0 - \frac{3}{8} Z_1 I_2 \tag{3.44}$$

Substituting Eq. (3.43) in Eq. (3.44), we get

$$V_2 = V_0 - \frac{3}{8} Z_1 I_0 - \frac{1}{8} Z_1 I_2 - \frac{1}{8} Z_1 I_0 - \frac{3}{8} Z_1 I_2 \tag{3.45}$$

$$V_2 = V_0 - \frac{1}{2} Z_1 I_0 - \frac{1}{2} Z_1 I_2 \tag{3.46}$$

Substituting Eq. (3.43) and Eq. (3.46) in Eq. (3.23), yields

$$I_0 - I_2 = \frac{1}{6} \frac{V_0}{Z_2} + \frac{2}{3} \frac{(V_0 - \frac{3}{8} Z_1 I_0 - \frac{1}{8} Z_1 I_2)}{Z_2} + \frac{1}{6} \frac{(V_0 - \frac{1}{2} Z_1 I_0 - \frac{1}{2} Z_1 I_2)}{Z_2} \tag{3.47}$$

$$I_0 - I_2 = \frac{1}{6} \frac{V_0}{Z_2} + \frac{2}{3} \frac{V_0}{Z_2} - \frac{6}{24} \frac{Z_1 I_0}{Z_2} - \frac{2}{24} \frac{Z_1 I_2}{Z_2} + \frac{1}{6} \frac{V_0}{Z_2} - \frac{1}{12} \frac{Z_1 I_0}{Z_2} - \frac{1}{12} \frac{Z_1 I_2}{Z_2} \tag{3.48}$$

$$I_0 - I_2 = \frac{1}{6} \frac{V_0}{Z_2} + \frac{2}{3} \frac{V_0}{Z_2} - \frac{1}{4} \frac{Z_1 I_0}{Z_2} - \frac{1}{12} \frac{Z_1 I_2}{Z_2} + \frac{1}{6} \frac{V_0}{Z_2} - \frac{1}{12} \frac{Z_1 I_0}{Z_2} - \frac{1}{12} \frac{Z_1 I_2}{Z_2} \tag{3.49}$$

$$I_0 - I_2 = \frac{V_0}{Z_2} - \frac{1}{3}\frac{Z_1 I_0}{Z_2} - \frac{1}{6}\frac{Z_1 I_2}{Z_2} \tag{3.50}$$

$$V_0 = Z_2 I_0 + \frac{1}{3}Z_1 I_0 - Z_2 I_2 + \frac{1}{6}Z_1 I_2 \tag{3.51}$$

$$V_0 = \left(Z_2 + \frac{Z_1}{3}\right)I_0 - \left(Z_2 - \frac{Z_1}{6}\right)I_2 \tag{3.52}$$

Substituting Eq. (3.52) in Eq. (3.46), we get

$$V_2 = \left(Z_2 + \frac{Z_1}{3}\right)I_0 - \left(Z_2 - \frac{Z_1}{6}\right)I_2 - \frac{1}{2}Z_1 I_0 - \frac{1}{2}Z_1 I_2 \tag{3.53}$$

$$V_2 = Z_2 I_0 + \frac{Z_1}{3}I_0 - Z_2 I_2 + \frac{Z_1}{6}I_2 - \frac{1}{2}Z_1 I_0 - \frac{1}{2}Z_1 I_2 \tag{3.54}$$

$$V_2 = Z_2 I_0 - \frac{1}{6}Z_1 I_0 - Z_2 I_2 - \frac{1}{3}Z_1 I_2 \tag{3.55}$$

$$V_2 = \left(Z_2 - \frac{Z_1}{6}\right)I_0 - \left(Z_2 + \frac{Z_1}{3}\right)I_2 \tag{3.56}$$

We can write Eqs. (3.52, 3.56) as a matrix

$$\begin{bmatrix} V_0 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_2 + \dfrac{Z_1}{3}, Z_2 - \dfrac{Z_1}{6} \\ Z_2 - \dfrac{Z_1}{6}, Z_2 + \dfrac{Z_1}{3} \end{bmatrix} \begin{bmatrix} I_0 \\ -I_2 \end{bmatrix} \tag{3.57}$$

Obviously, according to the TPN theory, Eq. (3.57) represents an equivalent circuit that has negative impedance. Circuit impedances Z_{11}, Z_{12}, Z_{21} and Z_{22} can be found directly from equation (3.57) as

$$Z_{11} = Z_2 + \frac{Z_1}{3} \tag{3.58}$$

$$Z_{12} = Z_2 - \frac{Z_1}{6} \tag{3.59}$$

$$Z_{21} = Z_2 - \frac{Z_1}{6} \tag{3.60}$$

$$Z_{22} = Z_2 + \frac{Z_1}{3} \tag{3.61}$$

Considering Eqs. (2.41-2.43) in section 2.5.2.1 and Eqs. (3.58-3.61), we can write

$$Z_a = Z_2 + \frac{Z_1}{3} - Z_2 + \frac{Z_1}{6} = \frac{1}{2}Z_1 \tag{3.62}$$

$$Z_b = Z_2 + \frac{Z_1}{3} - Z_2 + \frac{Z_1}{6} = \frac{1}{2}Z_1 \tag{3.63}$$

$$Z_c = Z_2 - \frac{Z_1}{6} \tag{3.64}$$

From Eqs. (3.62-3.64), the equivalent z-parameter model of a T-configuration circuit based on the TPN theory can be described as shown in Figure 3.8.
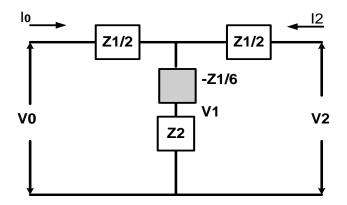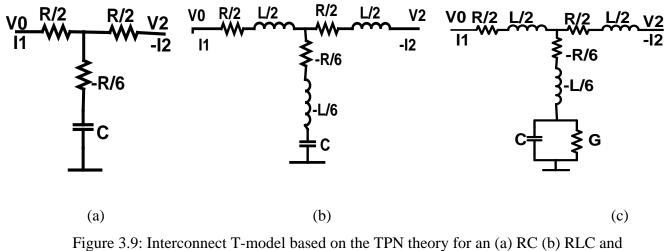
Figure 3.8: Z-parameter model of the T- configuration based on the TPN method.

Based on Eqs. (3.62-3.64), the RC, RLC and RLCG models of a T-configuration can be built as illustrated in Figure 3.9.

(a)   (b)   (c)

Figure 3.9: Interconnect T-model based on the TPN theory for an (a) RC (b) RLC and (c) RLCG interconnects.

Eqs. (3.62-3.64) represent the parameters of the interconnect T-configuration in the z-parameters form. As shown in Figure 3.9 (a, b and c), It could be easily and directly used to find the RC, RLC and/or RLCG interconnect models of the T-configuration depending on the TPN method from these equations. So, the z-parameter model, which is presented in this section, represents the general form of interconnect modeling of the T-configuration based on using the TPN method. Comparing these results to the work in [80], the work in [80] is limited by the RLC model only.

3.3.2.2 Z-Parameters Derivation for Π-Configuration

The interconnect z-parameter model of the Π-configuration based on the TPN method is presented in this section. Applying the duality principle to equations (3.43-3.64), the results are equations in the Π-model [80] as shown below

$$
\begin{bmatrix} I_0 \\ I_2 \end{bmatrix} = \begin{bmatrix} Z_1 + \dfrac{Z_2}{3}, Z_1 - \dfrac{Z_2}{6} \\ Z_1 - \dfrac{Z_2}{6}, Z_1 + \dfrac{Z_2}{3} \end{bmatrix} \begin{bmatrix} V_0 \\ -V_2 \end{bmatrix}
\tag{3.65}
$$

According to the TPN theory, equation (3.65) represents an equivalent circuit that has negative impedance. Again, circuit impedances Z_{11}, Z_{12}, Z_{21} and Z_{22} can be directly found from Eq. (3.65) as

$$
Z_{11} = Z_1 + \frac{Z_2}{3}
\tag{3.66}
$$

$$
Z_{12} = Z_1 - \frac{Z_2}{6}
\tag{3.67}
$$

$$
Z_{21} = Z_1 - \frac{Z_2}{6}
\tag{3.68}
$$

$$
Z_{22} = Z_1 + \frac{Z_2}{3}
\tag{3.69}
$$

Using the same process of Eqs. (3.58-3.64) for a T-model based on the TPN method, we get the general z-parameter of Π-model based on the TPN method as shown in Figure 3.10.
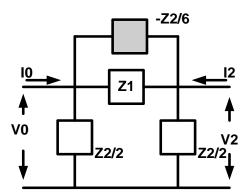
Figure 3.10: Interconnect z-parameters model of the Π- configuration based on the TPN.

From Figure 3.10, we can directly find the Π -configuration for the RC, RLC and/or RLCG models based on the TPN by replacing Z_1 and Z_2 with their actual components as shown in Figure 3.11.
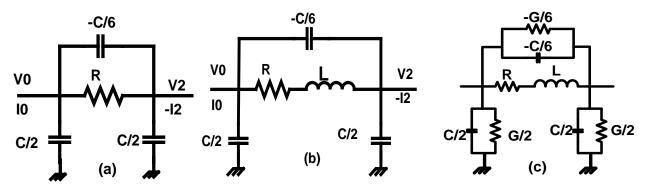
Figure 3.11: Interconnect Π -model based on the TPN theory for an (a) RC (b) RLC and (c) RLCG interconnects.

Using the derived model, we can directly find the RC, RLC and/or RLCG models of an on-chip interconnect. In contrast, [79] does not present the RLC model of the Π **-**configuration based on the TPN. Therefore, the z-parameter method used in this section is more flexible for finding all interconnect models such as RC, RLC and/or RLCG models, than the method used in [79] as shown in Figure 3.11 (a, b and c).

3.3.3   AWE Based Z-Parameter Modeling

The AWE method, a moment matching method, consists of two main parts: First, moment generation and second, moment matching. The AWE method approximates the transient response of a circuit by first expanding the system equations in moments (coefficients) of a Taylor expansion (Maclaurin Series, Pade or a Simple Recursive Formula Method) in s-domain and then matching the moments of the series as well as the initial time conditions. In the following sections, we will show the process used to find both T and Π configurations of interconnect z-parameter models based on the AWE method.

3.3.3.1 Z-Parameters Derivation for T-Configuration

The input impedance of a short-ended z-parameter interconnect with normalized length can be found as illustrated in [78-80].

$$Z_{in} = Z_o \tanh(\sqrt{\ell\lambda}) \tag{3.70}$$

Where $Z_o = \sqrt{Z_1/Z_2}$, $\ell = 1$, $\lambda = \sqrt{Z_1 Z_2}$ (3.71)

Therefore, $Z_{in} = \sqrt{Z_1/Z_2} \tanh\sqrt{Z_1 Z_2}$ (3.72)

Using Taylor series formula, we can explain the hyperbolic function as a polynomial series equation. So, the input impedance based on the Taylor series formula will be

$$Z_{in} = Z_1 - \frac{1}{3}Z_1^2 Z_2 + \frac{2}{15}Z_1^3 Z_2^2 - \frac{17}{315}Z_1^4 Z_2^3 + ----- \tag{3.73}$$

Eq. (3.73) represents the general input impedance of a short-ended interconnect in z-parameter representation. We can directly find the input impedance of a short-ended RC, RLC and/or RLCG interconnect model from Eq. (3.73) as shown below.

For an interconnect RC lumped model

$$Z_{in}(s) = R - \frac{1}{3}R^2 Cs + \frac{2}{15}R^3 C^2 s^2 - \frac{17}{315}R^4 C^3 s^3 + A \tag{3.74}$$

For an interconnect RLC lumped model

$$Z_{in}(s) = R + (L - \frac{1}{3}R^2 C)s + (-\frac{2}{3}RLC + \frac{2}{15}R^3 C^2)s^2 +$$
$$(-\frac{1}{3}L^2 C + \frac{2}{5}R^2 LC^2 - \frac{17}{315}R^4 C^3)s^3 + A \tag{3.75}$$

For an interconnect RLCG lumped model

$$Z_{in}(s) = R - \frac{1}{3}R^2G + (L - \frac{2}{3}RLG - \frac{1}{3}R^2C)s - (\frac{2}{3}RLC + \frac{1}{3}L^2G)s^2$$
$$- \frac{1}{3}L^2C + A$$

(3.76)

Let us consider the T- model illustrated in Figure 3.8.
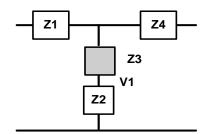
Figure 3.12: The improved T-model in the z-parameter.

Assuming Figure 3.12 has a symmetric structure. i.e. $Z_1 = Z_4$, the input impedance of the circuit shown in Figure 3.12 when short-ended is

$$Z_{in} = \frac{2Z_1Z_2 + 2Z_1Z_3 + Z_1^2}{Z_1 + Z_2 + Z_3}$$

(3.77)

Eq.(3.77) represents the general input impedance of the T-configuration in the z-parameter at a short-ended interconnect. The rational function of the input impedance for the T- configuration in the z-parameter at short-ended interconnect as illustrated in Eq.(3.77) can be expressed as a polynomial of order 2n-1. The coefficients Z_i can be computed by a simple recursive formula as shown in Eqs. (2.44-2.46). So, by using Eq. (2.45) and Eq. (2.46), we can directly find the input impedance of the models shown in Figure 3.12 for the RC, RLC and/or RLCG models after replacing Z_1, Z_2 and Z_4 with their actual components (where $Z_1 = Z_4$). By equating the first, second and third moments of Eq. (3.73) with the Eqs.(3.74-3.76) results from using the RC, RLC

and/or RLCG configuration respectively, we found the RC, RLC, and/or RLCG models of the T-configuration based on the AWE as shown in Figure 3.13. (For more details, see Appendix A.)
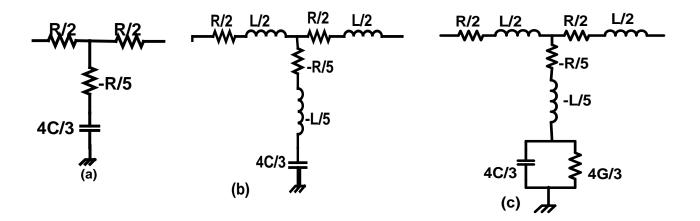
Figure 3.13: The T- configuration based on the AWE for an (a) RC, (b) RLC and (c) RLCG interconnects.

In this section, the interconnect z-parameter model of the T-configuration based on the AWE has been proposed. Comparing with the previous works such as in [78], the RC Π-configuration is only considered by using the AWE method whereas the T- configuration of an RC, RLC and/or RLCG models are not considered. However, the work in [80] considered the AWE of RLC modeling but for T-configuration only. By using the z-parameter model which is derived in this section, we can directly find the interconnect RC, RLC, and /or RLCG models of the T-configuration based on the AWE method. Thus, the z-parameter model, which is derived in this section, represents an extensive model to find the interconnect RC, RLC and/or RLCG models of the T-configuration based on the AWE method as shown in Figure 3.13 (a, b and c).

3.3.3.2 Z-Parameters Derivation for Π-Configuration

The general input admittance of the interconnect z-parameter lumped model at the open end can be obtained from the two-port parameters as in [78, 80].

$$Y_{in}(s) = \frac{\tanh \sqrt{Z_1/Z_2}}{\sqrt{Z_1 Z_2}}$$

(3.78)

Using the Taylor series formula, the hyperbolic function can be converted into the polynomial series. Therefore, for an open-ended interconnect of z-parameter, the input admittance $Y_{in}(s)$ can be expanded as follows:

$$Y_{in}(s) = \frac{1}{Z_2} - \frac{1}{3}\frac{Z_1}{Z_2^2} + \frac{2}{15}\frac{Z_1^2}{Z_2^3} - \frac{17}{315}\frac{Z_1^3}{Z_2^4} + - - -$$

(3.79)

For an open-ended interconnect, equation (3.79) represents the input admittance of a z-parameter lump-model. Thus, the admittance of an open-ended RC, RLC, and/or RLCG interconnect can be directly obtained from equation (3.79) by using the actual values of interconnect parameters as illustrated below.

For an interconnect RC lumped model, if we substitute $Z_1 = R$ and $Z_2 = \dfrac{1}{sC}$ in Eq. (3.79), this equation becomes Eq. (3.80)

$$Y_{in}(s) = sC - \frac{1}{3}RC^2 s^2 + \frac{2}{15}R^2 C^3 s^3 - \frac{17}{315}R^3 C^4 s^4 + A$$

(3.80)

For an interconnect RLC lumped model, if we substitute $Z_1 = R + sL$ and $Z_2 = \dfrac{1}{sC}$ in Eq. (3.79), this equation becomes Eq. (3.81).

$$Y_{in}(s) = sC - \frac{1}{3}RC^2 s^2 - (\frac{1}{3}LC^2 - \frac{2}{15}R^2 C^3)s^3 + (\frac{4}{15}RLC^3 - \frac{17}{315}R^3 C^4)s^4 + A$$

(3.81)

For an interconnect RLC lumped model, if we substitute $Z_1 = R + sL$ and $Z_2 = \dfrac{1}{G+sC}$ in Eq. (3.79), this equation becomes Eq. (3.82)

$$Y_{in}(s) = (G - \frac{1}{3}RG^2) + (C - \frac{1}{3}LG^2 - \frac{2}{3}RCG)s - (\frac{1}{3}RC^2 + \frac{2}{3}LCG)s^2$$

$$- \frac{1}{3}LC^2s^3 + A \tag{3.82}$$

Let us consider the Π - configuration shown in Figure 3.10,
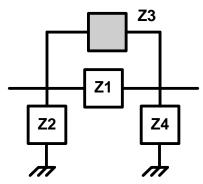
Figure 3.14: The assumption of the Π- configuration.

assuming the Π - configuration has a symmetric structure. i.e. $Z_2 = Z_4$. For an open-ended z-parameter of Π - configuration as shown in Figure 3.14, the driving point admittance can be obtained as

$$Y_{in} = \frac{Z_1Z_3 + 2Z_1Z_2 + 2Z_2Z_3}{Z_2(Z_1Z_3 + Z_1Z_2 + Z_2Z_3)} \tag{3.83}$$

Equation (3.83) represents the input admittance of a z-parameter Π - configuration at an open-ended interconnect. Using the simple recursive formula to convert the rational input admittance equation to the series equation. By matching the first, second and third moments of the Eqs. (3.80-3.82) with the results of Eq. (3.83), we can easily find the RC, RLC, and/or RLCG models of the Π -configuration based on the AWE as shown in Figure 3.15. (For more details, see Appendix B.)
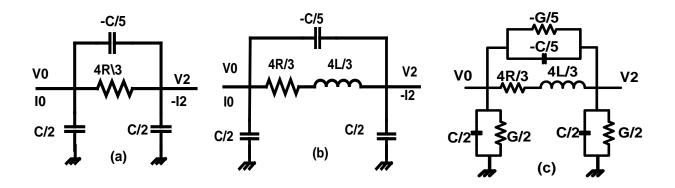
Figure 3.15: Π-configuration based on the AWE for an (a) RC, (b) RLC and (d) RLCG models.

Figure 3.15 (a, b and c) shows the results of using the z-parameter model which is derived in this section. RC, RLC and/or RLCG models are easily found from the derivative model.

3.4 Summary

Models using z-parameters for both T and Π configurations of interconnect modeling based on the GAM, TPN and AWE methods were derived in this chapter. The models provide the ability to find the RC, RLC and RLCG interconnect models easily and directly. Efficient approximation frames were obtained by using the GAM. Galerkin's method was used to find the frames coefficients. Mathematical manipulations applied on the frames lead to generate z-parameters modeling for both T and Π configurations. Another mathematical manipulations has been done on the approximation frames to convert them into a matrix form. The TPN method was used to derive another z-parameter interconnect model from the matrix in both T and Π configurations. Based on the z-parameters models derived from using the TPN method, the symmetric-structure in the z-parameter model with the AWE method was derived by matching the first three moments of the driving point admittance of an open-ended interconnect for Π-configuration and matching the first three moments of the driving point impedance of a short-ended interconnect for T-configuration. It is found that the models, which are derived from using the AWE method, have negative components called improvement elements [79]. In contrast, the derived z-parameter models represent comprehensive models for finding the RC, RLC, and /or RLCG models in both T and Π configurations based on the GAM, TPN, and AWE methods.

CHAPTER 4

Performance Comparison and Characterization of the GAM, TPN and AWE Methods

4.1 Introduction

In the previous chapter, z-parameter models of on-chip interconnect were derived. These models were used to obtain the RC, RLC, and RLCG models in both T and Π configurations based on the GAM, TPN, and AWE methods. The results of this process generate eighteen different RC, RLC, and RLCG models. To characterize an on-chip interconnect accurately, it is important to evaluate the performance of these models.

In this chapter, the RC, RLC, and RLCG models for both T and Π configurations, which were obtained from using the GAM, TPN, and AWE methods, are evaluated for different interconnect lengths, input transition times and capacitive loads. H-spice simulations show that the RLCG model of Π configuration which is derived from using the AWE method provides the best accuracy.

4.2 Verification of the Simulation Ranges

Based on our goal to find the best model response and consider the interconnect delay, choosing the accurate simulation range for different interconnect lengths, capacitive loads and input transition times is crucial to reach this goal.

4.2.1 Range of the Interconnect Length

Simply, to limit the length of the interconnect in our simulations, we will consider the critical length presented in [64] based on the RC line model and illustrated in equation (1),

$$\ell_{crt.} = \sqrt{\frac{2R_0 C_0}{RC}} \qquad\qquad (4.1)$$

where $\ell_{crt.}$ is the length of the interconnect where the delay is in linear proportion to the interconnect length, R_0 is the output resistance of the minimum buffer, C_0 is the input capacitance of the minimum buffer, R is the line resistance and C is the line capacitance.

Eq.(4.1) represents the optimum interconnect length where the interconnect delay is in linear proportion to its length. Based on the 45 nano-meter technology, the result from using Eq.(4.1) shows that the critical length is around 0.25mm. Therefore, we extend our simulations to reach 2mm to check the robustness of the models. Moreover, 2mm length is widely used and accepted [78-80].

4.2.2 Range of the Capacitive Load

Based on the 45Nano-meter technology, the input capacitance of the minimum buffer size is 0.25fF. We assume that the size of the output buffer will not exceed two-hundred times of the minimum buffer size. Therefore, we will limit our simulations of the capacitive loads for no more than 50fF.

4.2.3 Range of the Input Transition Time

The woks in [78-80] limit their simulations to10GHz. We consider this range as a satisfied and accepted range to verify the behaviour of the RLCG models which were derived based on the GAM,TPN and AWE methods for both T and Π configurations.

4.3 Models Evaluation

To evaluate the performance of the RLCG models for both T and Π configurations which were derived in the previous chapter, the output responses of on-chip interconnects under different interconnect lengths, capacitive loads, and input transition times are considered. Limiting the simulation ranges for different interconnect lengths, capacitive loads, and input-signal-transition times, we will be able to evaluate the models accurately.

4.3.1 Delay Based Comparison for the RLCG Models

In the previous chapter, sixteen different RC, RLC and RLCG models were generated for both T and Π configurations from using the z-parameter models based on the GAM, TPN and AWE

methods. The comparison among these models is important to distinguish the preferable model. We preferred to test the RLCG models for both T and Π configurations because these models represent more accurate models than others; these models consider most of the interconnect effects such as interconnect resistance, capacitance, inductance and the dielectric loss. In our perspective, we need to use the preferred model for buffer insertion technique to improve the interconnect delay in VLSI circuits. Therefore, we tested these models for the vdd/2 delay. Furthermore, we tested these models for transition time to get more robustness model.

The results of the comparison are compared with H-spice tools because these tools are widely used and their results are accurate for calculating the interconnect delay. We tested these models for different interconnect lengths, capacitive loads and input transition times. The default values are used during the simulation such as when testing the models for different capacitive loads (1fF-50fF), we have to keep the other factors (input transition times and interconnect lengths) constant.

First of all, the comparison is considered the vdd/2 delay of the output responses for T and Π configurations of the RLCG models for all methods for different interconnect lengths, capacitive loads and input transition times. Second, the best configuration response is tested for all methods to find the best model response based on vdd/2 delay calculations. In the same way, we tested the models for different transition times. Third, we compared the best models which preferred from the previous process and find the best model response.

The calculations shown in Figures 4.1-4.2 have been simulated based on the 45nano-meter technology. The default values used in these simulations are 2mm, 20p.sec and 5fF which represent the interconnect length, input transition time and capacitive load respectively. The dot line represents the line, which has slop=1, where the two values of the H-spice delay and the RLCG models delay are equalled. The simulation results appear above the slope line when the H-spice shows faster output than the RLCG models and appear below the slope line when the RLCG models show faster output responses than H-spice estimation. The ranges of the interconnect lengths, capacitive loads and input transition times we used to calculate the delay of vdd/2 is: The interconnect range we used in these simulations is from 0.25mm to 2mm, the range of the input

transition times is from 100 Pico second to 10 Pico second and the range of the capacitive loads is from 5femto farad to 50 Femto Farad.

The simulation results shown in Figure 4.1 represent the comparison of the vdd/2 delay calculations for the RLCG models of both T and Π configurations which were derived based on the GAM, TPN and AWE methods for different input transition times, capacitive loads and interconnect lengths. The simulation results show that the Π configuration is better than T configuration compared to H-spice. It is worth mentioning that the improved design tackles the upstream in Π-configuration and the down stream in T-configuration.
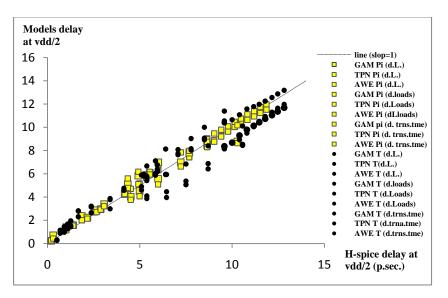
Figure 4.1: The comparison of the vdd/2 delay between the RLCG models and H-spice simulation for different interconnect lengths, capacitive loads and output transition times.

Figure 4.2 shows the comparison between the RLCG models of the Π configuration which were derived from using the GAM, TPN and AWE methods and H-spice for vdd/2 delay simulations. These models are tested for different input transition times, capacitive loads and interconnect lengths. It is clear from Figure 4.2 that the RLCG model of the Π configuration which was derived using the AWE method reveals the best output response than others.
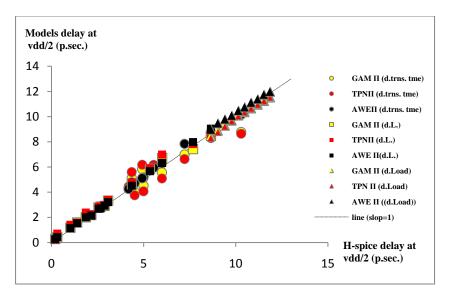
Figure 4.2: The comparison of the vdd/2 delay between the Π configuration and H-spice simulation for different interconnect lengths, capacitive loads and output transition times.

4.3.2 Output Transition Time Based Comparison for the RLCG Models

Based on the simulation results shown in Figures 4.3 and 4.4, the RLCG model of the Π-configuration which was derived from using the AWE method exhibits the best output transition time for different capacitive loads, interconnect lengths and input transition times.
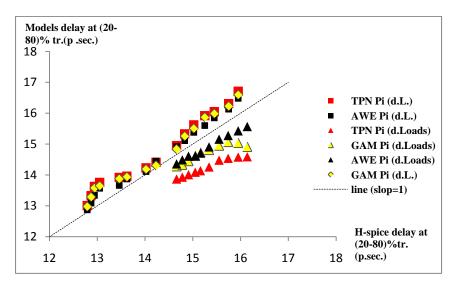
Figure 4.3: The comparison of the output transition time between the Π configuration and H-spice simulation for different interconnect lengths and capacitive loads.
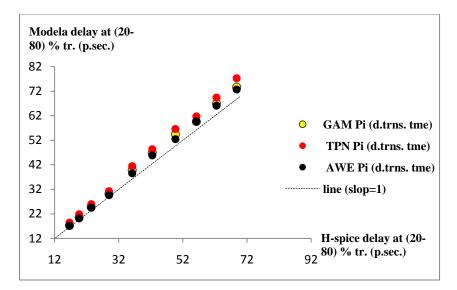
Figure 4.4: The comparison of the output transition time between the Π configuration and H-spice simulation for different output transition times.

4.4 Summary

The delay and the output transition time which are obtained from the GAM, TPN and AWE methods for both configurations T and Π are compared with H-spice in this chapter. The comparison is done for different interconnect lengths, capacitive loads and input transition times. The results from this comparison show that the RLCG model of the Π configuration which was derived from using the AWE method reveals better satisfactory and acceptable than others

CHAPTER 5

Wire Segmentation, Buffer Insertion and Buffer Sizing Techniques for Minimizing an Interconnect Delay

5.1 Introduction

With the evolution of VLSI fabrication technology, interconnect delay has become the dominant factor in deep submicron design. Buffer insertion, wire segmentation and buffer sizing have been shown to be effective techniques for interconnect delay optimization. Different studies considered these three techniques to optimize on-chip interconnect delay. However, most of the results from these studies on interconnect delay optimization, especially for some simple cases like buffer insertion alone or buffer sizing alone, are algorithmic.

Basically, sizing of inserted buffers and lengths of the segments can all be changed from source to sink in order to minimize the delay. Although some techniques are used to change buffer insertion, buffer sizing or wire segmentation alone to minimize the interconnect delay, simultaneous change techniques for buffer insertion, buffer sizing and wire segmentation are also used to reduce the interconnect delay.

For wire segmentation, [81] a uniform wire segmentation algorithm for performance optimization of distributed RLC interconnects was proposed in this paper. The optimal wire length for identical segments and buffer size for buffer insertion are obtained through computation and derivation, based on a 2-pole approximation model of distributed RLC interconnect.

Buffer sizing has been an active research area for decades. To drive a large capacitive load, [82] first proposed the tapered buffer structure, which is a series of cascaded buffers of increasing size. Immediately after that, [83] showed that the optimal tapering factor, the size-ratio between consecutive buffers in the tapered buffer structure, should be constant in order to minimize the delay. In [84], a specific algorithm is used to show that when the size of repeaters increases exponentially, the delay will be reduced. A more accurate capacitance model used to reduce the

delay showed that the optimal tapering factor should be approximately 3–5 and depend on the process parameters and the design style [85]. [86] considered the delay, power dissipation and circuit area and proposed the use of variable size-ratio between consecutive buffers. Note that all the results for the tapered buffer structure above are useful only when large capacitive loads are driven. When the resistivity of the loads cannot be ignored, as in the case of driving interconnects nowadays, buffers should be distributed throughout the interconnect.

For the case when the buffer locations in the interconnect are predetermined, and the buffers and wire segments can be sized simultaneously, an iterative algorithm can be derived. Many such algorithms published in the past few years. [87] used a sequential quadratic programming approach, [88] used a greedy approach, [89] used the Lagrangian relaxation technique, and [90] solved a recurrence relation.

For the case when the buffer locations are not predetermined (i.e., buffer insertion is considered), [91] and [92] considered the problem of driving a uniform line (i.e., wires were not sized). [93] addressed simultaneous floor planning and buffer-block planning for interconnect optimization by partition modules into super modules. [94] derived formulae of feasible regions and integrated buffer planning with floor planning to optimize area, time, noise and congestion simultaneously. [95] extended van Ginneken's buffer-insertion algorithm to simultaneously incorporate driver sizing. [96] formulated the simultaneous buffer insertion and wire sizing problem as a convex quadratic program and derived a very efficient algorithm to solve it. They also introduced an effective pruning technique to handle buffer sizing. [97] extended the dynamic programming framework by considering buffer insertion and wire sizing under the effect of process variation. [98] handled the simultaneous buffer insertion, buffer sizing and wire sizing problem by generalizing the dynamic programming algorithm for buffer insertion in [99]. The algorithm in [100] was later extended to handle power dissipation and incorporate signal slew into the buffer delay model.

5.2 Buffer Insertion (Repeaters)

A buffer insertion technique is a method used to reduce on-chip interconnect delay. When the resistance of an interconnect is comparable to or larger than the on-resistance of the driver, signal

propagation delay increases proportionally to the square of the interconnection length because both capacitance and resistance increase linearly with interconnect length. Thus, reducing the interconnect length leads reducing the interconnect delay. In buffer insertion techniques, this principal is used by sampling an interconnect into small pieces and separated them by CMOS buffers as shown in Figure 5.1
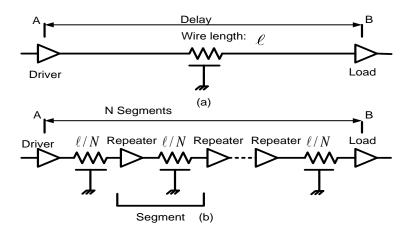
Figure 5.1: Wire (a) without repeaters, (b) with repeaters.

Figure 5.1b shows that the wire is sampled into N segments and separated by buffers. The delay is reduced by splitting the wire into N segments and increasing the number of inverters or buffers to actively drive the wire [101]. The new wire involves N segments with RC flight time $(\ell / N)^2$, for a total delay of ℓ^2 / N. If the number of segments is proportional to the length, the overall delay increases only linearly with ℓ [101].

Using inverters as repeaters gives the best performance. However, each repeater adds some delay. If the distance is too great between repeaters, the delay will be dominated by the long wires. If the distance is too small, the delay will be dominated by the large number of inverters. As usual, the best distance between repeaters is a compromise between these extremes. Suppose a unit inverter has resistance R_0 and capacitance C_0 ($C_0 \approx 3C_N$ because the inverter is composed of a unit NMOS and double-width PMOS) and a wire has both resistance r and capacitance c per unit

length. Consider inserting repeaters of h times unit size. Under the Elmore delay model, neglecting diffusion parasites, the best length of wire between two repeaters as illustrated in [101] is

$$\frac{\ell}{N} = \sqrt{\frac{2R_0C_0}{rc}} \tag{5.1}$$

The delay per unit length of a property repeated wire is

$$\frac{t_{pd}}{\ell} = (2 + \sqrt{2})\sqrt{R_0C_0rc} \tag{5.2}$$

To achieve this delay, the inverters should use an NMOS transistor width of

$$h = \sqrt{\frac{cR_0}{rC_0}} \tag{5.3}$$

5.3 Wire Segmentation

Interconnect delay is in quadratic proportion to its length. Therefore, reducing an interconnect length by cutting the interconnect into small pieces (segments) as shown in Figure 5.2 leads reducing the delay.
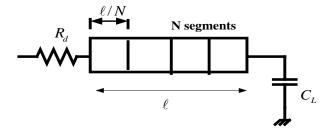
Figure 5.2: Interconnect with N segments.

Each segment can be represented as shown in Figure 5.3

$r.\ell$

$c.\ell/2$ $c.\ell/2$

(a)   (b)
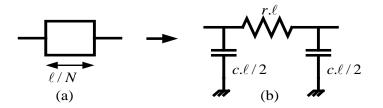
Figure 5.3: Interconnect (a) One segment, (b) RC Π-model.

Where

    r : Interconnect unit resistance

    c : Interconnect unit capacitance

ℓ/N : Segment length.

5.4 Buffer Sizing

A buffer, also called repeater, is a CMOS inverter used to separate small pieces of a line. It is modeled as a switch-level RC circuit as shown in Figure 5.4. R_0, C_0 and C_{d0} are respectively, the unit effective output resistance, the unit gate capacitance and the unit drain capacitance.

hR_0

hC_0 hC_{d0}
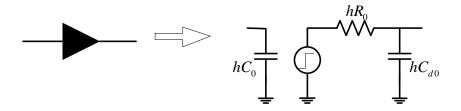
Figure 5.4: The model of a buffer has size h as a switch-level RC circuit.

Buffer insertion is widely recognized as an effective technique used to reduce the line delay [102]. To explain how the buffer insertion technique reduces the interconnect delay, let us consider the simple circuit illustrated in Figure 5.1a. The circuit has a wire without repeaters connected to a driver and load buffers. We can simply express this circuit as a Π-configuration of an RC circuit as illustrated in Figure 5.4. The circuit will be as shown in Figure 5.5b

(a)

(b)
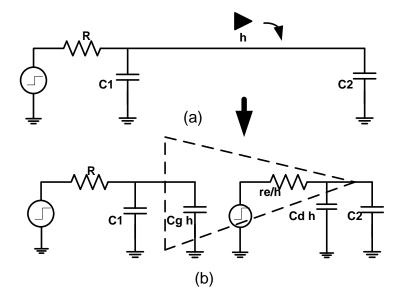
Figure 5.5: Delay reduction by buffer insertion (a) wire without a buffer (b) wire with a buffer.

Where R is the wire resistance, C_1 and C_2 are the wire capacitances . Suppose R, C_1 and C_2 are all large. Then the Elmore delay for the original circuit (Figure 5.5a) is

$$t_{pd} = R(C_1 + C_2) \qquad (5.4)$$

Where t_{pd} is the wire delay which is very large. After a buffer of size h is inserted between C_1 and C_2, the buffer isolates C_2 from the original driver. So, the original driver only needs to drive C_1 together with the gate capacitance of the inserted buffer. Therefore, the Elmore delay calculation after buffer insertion is

$$t_{p.d} = R(C_1 + C_g h) + \frac{r_e}{h}(C_d h + C_2) \qquad (5.5)$$

If the buffer is inserted appropriately, the resulting delay can be significantly smaller [88].

63

Simply, the principle behind the repeater is that when dealing with an interconnect as one piece, the time constant (RC) of the whole interconnect can be calculated by multiplying the number of units of resistance times the number of units of capacitance. For example, let us take an interconnection that has 5 units long. This means, it has 5 units of resistance and 5 units of capacitance. The Time constant will be = 5x5=25 units. When this wire is divided into five equal sections by buffers, its accumulative RC constant is reduced to 1+1+1+1+1=5 units. Of course, the additional delay due to buffers should be taken into account.

To effectively use buffer insertion technique to reduce on-chip interconnect delay, robust an interconnect model should be used. The RLCG model which is derived from the previous chapter has good accuracy compared with H-spice but it is a complex model. This complexity makes this model is difficult to be used to improve on-chip interconnect delay. Therefore, mapping this complexity is crucial to reach this target.

5.5 Mapping an RLCG Model into an RLC Model

In chapter 4, the results of the comparison show that the RLCG model of the Π-configuration which was derived from using the AWE method as shown in Figure 5.6 revealed the best response for vdd/2 delay and transition time calculations.
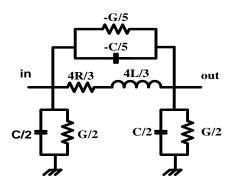
Figure 5.6: The RLCG model of the Π-configuration which was derived from using the AWE method.

The model shown in Figure 5.6 considers the interconnect resistance R, interconnect capacitance C, interconnect inductance L and dielectric conductance G. This consideration gives the model some

complexity. The complexity makes this model to be difficult to use for finding the mathematical expressions of the optimum interconnect delay, interconnect critical length and minimum buffer sizing. Modifying the model's complexity takes into our consideration to keep the same vdd/2 delay effect.

In the RLCG model, G represents the dielectric loss. It is important for long interconnect. But this loss will reduce when the interconnect be short. Because the length of the interconnect will be sampled into small pieces by using buffer insertion technique, the effect of G will be very small and we compensate this effect by the buffer sizing. Therefore, we will consider the RLC model of the Π-configuration which was derived based on using the AWE method as shown in Figure 5.7 instead of the RLCG in our simulation process.
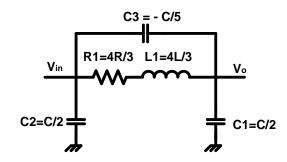
Figure 5.7: The RLC model of the Π configuration which was derived from using the AWE method.

5.6 Mapping an RLC Model into an RC Model

The model shown in Figure 5.7 has a negative capacitance is connected in parallel with the upstream components. A negative capacitance in the circuit creates some complexity [80]. This complexity is conflicted with the delay calculation. Therefore, mapping the circuit is crucial to find the closed-form expression of the line delay.

Clearly, circuit components are represented as in [80]

$$C_1 = C_2 = \frac{C}{2}, R_1 = \frac{4R}{3}, L1 = \frac{4L}{3} \text{ and } C_3 = -\frac{C}{5} \tag{5.6}$$

Where R, L and C are interconnect resistance, inductance and capacitance.

The input admittance of an open-ended circuit shown in Figure 5.7 is

$$Y_{in}(s) = \frac{(C_1 + C_2)s + (R_1C_1C_3 + R_1C_2C_3 + R_1C_1C_2)s^2 + (L_1C_1C_3 + L_1C_2C_3 + L_1C_1C_2)s^3}{1 + (R_1C_1 + R_1C_3)s + (L_1C_1 + L_1C_3)s^2}$$

(5.7)

Using the Simple Recursive Formula in [106], the input admittance can be extended as

$$Y_{in}(s) = (C_1 + C_2)s - R_1C_1^2s^2 + (R_1^2C_1^2C_3 + R_1^2C_1^3 - L_1C_1^2)s^3 + A$$ (5.8)

Let us assume that the equivalent RC circuit for Figure 5.7 is shown in Figure 5.8.
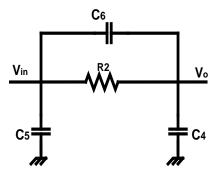
Figure 5.8: The RC equivalent circuit for the model shown in Figure 5.7.

The input admittance of an open-ended circuit shown in Figure 5.8 is

$$Y_{in}(s) = \frac{(C_4 + C_5)s + (R_2C_4C_6 + R_2C_5C_6 + R_2C_4C_5)s^2}{1 + (R_2C_4 + R_2C_6)s}$$ (5.9)

The input admittance in equation (5.9) can be extended as

$$Y_{in}(s) = (C_4 + C_5)s - R_2C_4^2s^2 + (R_2^2C_4^2C_6 + R_2^2C_4^3)s^3 + A$$ (5.10)

Using the AWE method for moments matching in [69] and we assume that the $C_1 = C_2$ and $C_4 = C_5$ as a property of the Π-configuration of an interconnect model, yields

$$C_4 = C_1 = \frac{C}{2}, R_2 = R_1 = \frac{4R}{3}, C_6 = C_3 - \frac{L_1}{R_1^2} = -\frac{C}{5} - \frac{3L}{4R^2} \qquad (5.11)$$

Eq. (5.11) represents the components of the equivalent RC circuit shown Figure 5.8. The equivalent RC circuit is similar to the RC model of the Π-configuration which was derived from using the AWE method. The difference between them is just the value of C_6 This value includes the effect of the line inductance. Therefore, this model is an RC model but considers the effect of the line inductance (an improved RC model). The comparison between the RLC model and the improved RC model have been done based on the scenarios shown in Figures (5.9) and the result is shown in Table 5.1.
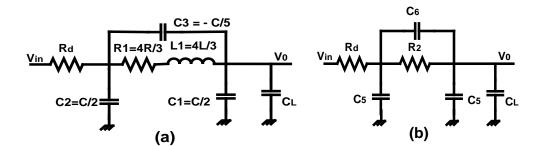
Figure 5.9: The comparison between the (a) RLC (b) Improved RC models.

Table 5.1 shows that the errors between the improved RC model RLC model mainly depend on the value of Rd. For interconnect circuit analysis, Rd represents the output resistance of the driver buffer. Therefore, increasing the driver size drives more current to an interconnect. This increases the speed of the signal and leads to reduce the error between the two responses. However, reducing the driver size leads to increasing the signal delay and this increases the error. Therefore, using optimum buffer sizing is crucial to reduce the delay. Furthermore, reducing the value of R_1, L_1 and C_3 reduces the error. These values represent the interconnect parameters. Increasing these values means increasing the length of the interconnect and leads to increasing the error. Thus, finding the critical length is important to optimize the interconnect delay.

Table 5.1: Error calculations for the vdd/2 delay between the RLC model and the improved RC model for different R1, C1 and C3.

Rd (Ω)	R_1 (Ω)	L_1 (p. h)	C_1 (f. F)	C_2 (f. F)	C_3 (f. F)	C_L (f. F)	Error at vdd/2 delay [%]
100	40	200	100	100	50	50	1.708
100	40	200	100	100	20	50	0.859
1K	40	200	100	100	50	50	0.0657
1K	40	200	100	100	20	50	0.0586
5K	20	50	50	50	25	25	0.0353
5K	20	50	50	50	10	25	0.0323
10K	20	50	50	50	25	25	0.0276
10K	20	50	50	50	10	25	0.0257

Figure 5.10 shows that the vdd/2 delays for both responses are close to each other until the interconnect reaches 1mm length. Then the difference between them starts to increase. This improvement is valid because we will not reach more than 1mm for interconnect critical length.
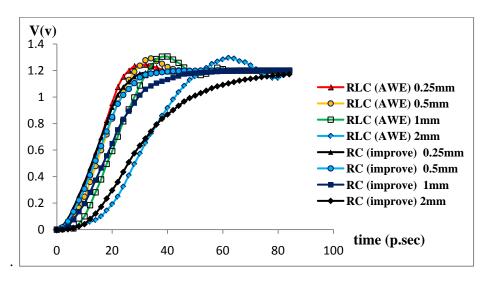
Figure 5.10: The output responses for the RLC model which was derived from using the AWE method and the RC improved for different interconnect lengths.

We see that the capacitance C_6 in Figure 5.8 is connected between the input and the output From the basic principles of capacitance charge and discharge, C_6 will charge $Q_c = C_6(V_{in} - V_{out})$. This means that the effect of the C_6 charge and discharge in the overall circuit will be the analog for the case of removing it from the upstream components and a positive C_6 is connected between the input and the ground, and the negative C_6 between the output and the ground, as shown in Figure 5.11.
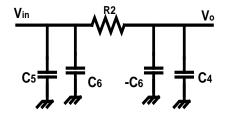
Figure 5.11: The equivalent RC circuit for the circuit shown in Figure 5.8.

$$R_{eqv.} = R_2 = R_1 = \frac{4R}{3}, C_{eqv.1} = C_5 - C_6 = C_1 + C_3 + \frac{L_1}{R_1^2} = \frac{7C}{10} + \frac{3L}{4R^2} \text{ and}$$

$$C_{eqv.2} = C_5 + C_6 = C_1 - C_3 - \frac{L_1}{R_1^2} = \frac{3C}{10} - \frac{3L}{4R^2} \tag{5.12}$$

So, the circuit shown in Figure 5.11 can be expressed as shown in Figure 5.12. The model shown in Figure 5.12 represents the equivalent RC model to the RLC model which was derived from using the AWE method. This model, is basically an RC model but it considers the effect of the interconnect inductance L. It is easy and simple to use this model to find an interconnect critical length, minimum buffer size and optimum interconnect delay. The difference between this work and the studies in [103-105] is that these studies could not find the mathematical expressions for the critical length, minimum buffer size and optimum interconnect delay because of the complexity of the RLC model used. In this work, we used a more complex RLC model and we reached the final stage of the research.
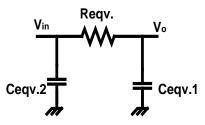
Figure 5.12: The equivalent RC circuit for the circuit shown in Figure 5.8.

To compare the two circuits (in Figure 5.8 and 5.12), let us consider an interconnect with driver and load buffers as shown in Figure 5.1a. This circuit can be represented by considering the circuits shown in Figures 5.8 and 5.11 as illustrated in Figure 5.12.
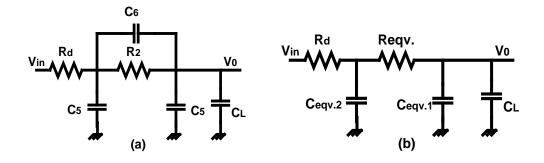
Figure 5.13: Circuit test (a) The improved RC circuit (b) The equivalent RC circuit.

Both circuits are tested for different driver and load buffer sizes and interconnect lengths. The results are shown in Table 5.2. Table 5.2 shows that the errors between the two circuits diminish when the size of the driver and load buffers and the interconnect length are reduced. This means, using the buffer insertion technique to reduce the interconnect delay due to cutting the line into small pieces separated by buffers makes the equivalent RC model more valid for modeling an interconnect.

Table 5.2: The error calculations of the vdd/2 delay for the circuits shown in Figure 5.13 (a, b) for different driver and load buffer sizes and interconnect lengths.

Rd (Ω)	R_1 (Ω)	C_1 (f. F)	C_2 (f. F)	C_3 (f. F)	C_L (f. F)	Error at vdd/2 delay [%]
100	40	100	100	50	50	5.62
100	40	100	100	20	50	2.11
1K	40	100	100	50	50	0.614
1K	40	100	100	20	50	0.228
5K	20	50	50	25	25	0.06
5K	20	50	50	10	25	0.022
10K	20	50	50	25	25	0.0297
10K	20	50	50	10	25	0.011

The simulation results shown in Figure 5.14 represent the output responses for the improved RC model equivalent RC model for different interconnect lengths. The error for vdd/2 delay between the two responses is very small. Therefore, the modification of the improved RC model into the equivalent RC model is satisfied.
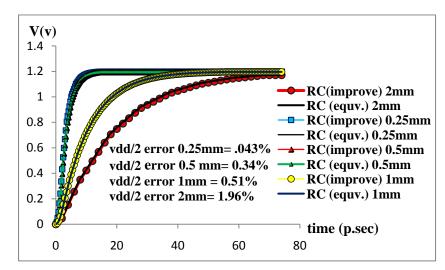
Figure 5.14: The output responses for the improved RC and equivalent RC models for different interconnect lengths.

For more robustness of the equivalent RC model, we tested this model with the RLC model as illustrated if Figure (5.15).
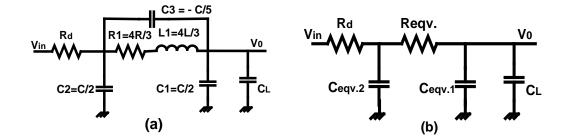
Figure 5.15: Circuit test (a) The improved RC circuit (b) The equivalent RC circuit.

In Table 5.3, the error calculations reflect the behaviour of the two circuits: the original circuit shown in Figure 5.7 and the equivalent circuit shown in Figure 5.12 at vdd/2 delay calculations for the rise time of the output responses. The results show that the error changes due to changing the original circuit component R_1, C_1, L_1 and C_3. The error calculations at vdd/2 delay are accepted especially for the interconnect length not exceeding 1mm.

Table 5.3: Error calculations for the vdd/2 delay of the RLC model and the equivalent RC model for different R1, C1 and C3.

Rd (Ω)	R_1 (Ω)	L_1 (P. h)	C_1 (f. F)	C_2 (f. F)	C_3 (f. F)	C_L (f. F)	Error at vdd/2 delay [%]
100	40	200	100	100	50	50	8.038
100	40	200	100	100	20	50	3.275
1K	40	200	100	100	50	50	1.186
1K	40	200	100	100	20	50	0.793
5K	20	50	50	50	25	25	0.294
5K	20	50	50	50	10	25	0.215
10K	20	50	50	50	25	25	0.1443
10K	20	50	50	50	10	25	0.107
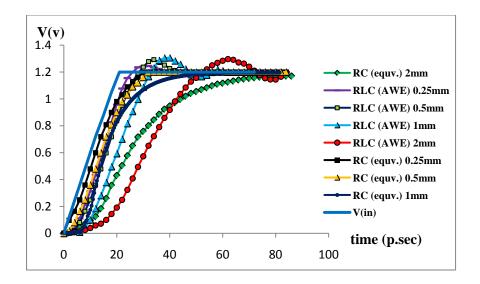
Figure 5.16: The output responses for the RLC model (AWE) and the equivalent RC models for different interconnect lengths.

5.7 Closed-Form Expression for Optimum Interconnect Delay

To calculate the interconnect delay with a buffer insertion technique, let us consider the circuit shown in Figure 5.1a. The delay of the circuit shown in Figure 5.1a is the sum of the delays for the driver buffer, interconnect and load buffer. The vdd/2 delay from point A to point B can be calculated as shown in Figure 5.17.
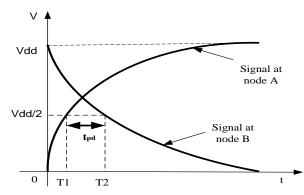
Figure 5.17: The vdd/2 delay calculation from point A to point B as illustrated in Figure 5.1a.

The delay of this circuit is due to the output resistance of the driver buffer R_d, interconnect capacitance C, resistance R and the gate capacitance of the load buffer C_L as illustrated in Figure 5.13b. Let us assume that the time taken for the signal at node A to reach 50% of its final rise time

73

is T_1 and the time taken for the signal at node B to reach 50% of its final fall time is T_2. So, the propagation delay from point A to point B at vdd/2 can be calculated as

$$t_{pd} = T_2 - T_1 \tag{5.13}$$

Figure 5.12b is the RC circuit configuration of Figure 5.1a. We can use the Elmore delay model [65] to calculate the delay of the circuit shown in Figure 5.12b as shown below

$$t_{pd} = R_d (C_{equv.2} + C_{equv.1} + C_L) + R_{equv.} (C_{equv.1} + C_L) \tag{5.14}$$

Eq. (5.14) can be expressed as

$$t_{pd} = R_d (C + C_L) + \frac{4}{3} R (\frac{7}{10} C + \frac{3}{4} \frac{L}{R^2} + C_L) \tag{5.15}$$

where RLC are the interconnect resistance, inductance and capacitance respectively.
So, Eq. (5.15) represents the delay of the circuit shown in Figure 5.13b based on the Elmore delay model.

5.8 Interconnect Critical Length and Optimum Buffer Sizing for Minimizing the Delay

To calculate the interconnect critical length and the optimum buffer sizing, we consider the method in [95] because it is a simple, an accurate and a well-known method. This method mainly considers a mathematical expression of the interconnect delay as a function of an interconnect length and buffer size. To find an interconnect critical length and optimum buffer sizing to minimize the interconnect delay, the derivation of the delay mathematical expression with respect to the interconnect length and buffer sizing is taken and the results equalized to zero. The results are the interconnect critical length and minimum buffer size. These are used to minimize the interconnect delay.

Let us assume that h is the buffer size and ℓ is an interconnect length. Therefore, Eq. 5.15 can be expressed as a function of a buffer sizing and an interconnect length as

$$t_{pd}(h,\ell) = \frac{R_0}{h}(\ell c + hC_0) + \frac{4}{3}\ell r(\frac{7}{10}\ell c + \frac{3}{4}\frac{l}{\ell r^2} + hC_0)$$

(5.16)

Where R_0 and C_0 are the unit inverter output resistance and gate capacitance and rlc are interconnect resistance, inductance and capacitance per unit length respectively.
So, the interconnect critical length can be found as

$$\frac{d(\frac{t_{pd}}{\ell})}{d\ell} = 0$$

(5.17)

Therefore,

$$\ell_{crt.} = \sqrt{\frac{15(R_0C_0 + \frac{l}{r})}{14rc}}$$

(5.18)

The interconnect critical length shown in Eq. (5.18) represents the optimum length of an interconnect in which the interconnect delay is in linear proportion to its length. Eq. (5.18) is similar to the approaches in [95]. To find the number of segments for an interconnect length ℓ, we divide the interconnect length by the critical length as shown in Eq. (5.19).

$$\text{Number of segments} = \frac{\ell}{\ell_{crt.}}$$

(5.19)

Also, the number of buffers can be calculated as shown in Eq. (5.20)

$$\text{Number of buffers} = \text{Number of segments} + 1$$

(5.20)

To find the optimum inverter size to minimize the delay, we consider both Eqs. (5.16, 5.18), yielding

$$h = \sqrt{\frac{3cR_0}{4rC_0}} \qquad\qquad (5.21)$$

Eq. (5.21) represents the optimum buffer size that can be used to minimize the interconnect delay. To find the delay per unit length of a properly repeated wire $\dfrac{t_{pd}}{\ell_{crt.}}$, we have to consider Eqs. (5.16, 5.18, 5.21). We get

$$\frac{t_{pd}(\ell)}{\ell_{crt.}}(h) = \frac{20R_0cr\sqrt{\dfrac{3R_0C_0r+3l}{c}} + 29R_0C_0c\sqrt{\dfrac{R_0cr+3l}{C_0}} + 29l\sqrt{\dfrac{R_0c}{rC_0}}}{\sqrt{\dfrac{15(R_0^2C_0r+R_0l)}{rC_0}}} \qquad (5.22)$$

(For more details, see Appendix C.)

The experimental results shown in Table 5.4 show that the interconnect delay is improved by using the proposed RC model much better than other models (columns 9, 13). Furthermore, the critical length and number of buffers which were calculated using the proposed RC method are better than others because the critical length is larger and the optimal number of buffers is less than others. The best model is that the model which presents longer critical length with minimum number of buffers because longer critical length reduces the number of buffer; reducing number of buffer means reducing the fabrication cost [101]. Therefore, the proposed RC model reveals the best simulation results than [101,103].

Where $\ell, \ell_{crt.}$ are interconnect length and critical length respectively, DNB, DWB represent the delay without buffer and with buffer respectively and NO.S, NO.B, U.A. represent the number of segments, number of buffers and unit area respectively.

Table 5.4: the performance of buffer insertion for using proposed model vs. previous published models.

The used parameters: $r= 0.29\Omega/sqr$, $c=0.21fF/sqr$, and $l=0.293pH/sqr$, $R_D=1K\Omega$ and $C_L=10fF$										
ℓ (mm)	DNB [n.s]	(Proposed RC model) h=27.38			(RC model [9]) h=31.62			(RLC model [10]) h=26.9		
		No. B.	DWB [p.s]	Area [UA]	No. B.	DWB [p.s]	Area [UA]	No. B.	DWB [p.s]	Area [UA]
0.5	0.081	3	34.4	246.4	4	51.7	379	4	46.2	322
1	0.172	5	68.9	410.7	6	86.1	569	7	73.6	564
2	0.395	10	155.1	821.4	11	172.7	1043	12	162.3	968
5	1.3	21	344.7	1724	25	413.6	2371	28	398.9	2259
8	2.7	34	558.8	2792	39	655	3699	45	602.5	3631
10	3.8	43	723.9	3532	49	827.3	4648	55	811.3	4438
12	5.1	51	861.8	4189	58	982.5	5501	66	934.6	5326
15	7.4	63	1090	5174	72	1220	6829	82	1160	6617
Average delay reduction [%]				20.5						
Average reduction of no. of buffers [%]				24						

The average delay saving are 67.66p.s than [101] and 40.22p.s than [103] and the average area saving are 768.62u.a than [101] and 654.62u.a than [103].

5.9 Summary

In this chapter, buffer insertion (repeaters), wire segmentation and buffer sizing were briefly reviewed. The RLCG model of the Π-configuration which was derived from using the AWE method was modified into an RLC model of the Π-configuration. To reduce the complexity of this model, it was mapped into an improved RC model of the Π-configuration based on using the moment matching of the AWE method. Another mapping was applied on the model to eliminate the negative capacitance. An equivalent RC model was derived. The delay of the vdd/2 of the rise time for these models was calculated for different interconnect lengths. Buffer insertion technique was used in this chapter to minimize the interconnect delay. By considering the equivalent RC model, closed-form expressions for interconnect critical length, minimum buffer size and optimum delay were derived. The simulation results as shown in Table 5.4 show that the equivalent RC model gives better results than the RC models are used in [101,103].

CHAPTER 6

Conclusions and Future Works

Interconnect closed-form expressions in z-parameter form were derived for both T and Π configurations based on the GAM, TPN and AWE methods. Telegraph equations of the transmission line were used to derive the z-parameter closed-form expressions for both transmission voltages and currents. Based on Telegraph equations of the z-parameter, the approximation frames of the transmission line voltages and currents in z-parameter configuration were proposed. Mathematical manipulations on the approximation frames were used to generate the closed-form expressions in z-parameter form for T and Π configurations based on the GAM method. These expressions were considered to derive six different RC, RLC and RLCG models in both T and Π configurations. Furthermore, other mathematical manipulations were applied on the approximation frames based on the TPN method to present the closed-form expressions in z-parameter form for both T and Π configurations. These models were used to generate another six RC, RLC and RLCG models for both T and Π configurations. By considering the models which were derived from using the TPN method, the moments matching method was used based on the AWE method to present another six different RC, RLC and RLCG models of the T and Π configurations. Therefore, eighteen different RC, RLC and RLCG models in both T and Π configurations were derived from using the z-parameter models based on the GAM, TPN and AWE methods. The RLCG models which were derived from using the GAM, TPN and AWE methods of both T and Π configurations were tested for different interconnect lengths, capacitive loads and input transition times and compared with H-spice. The results revealed that the RLCG model of the Π configuration which was derived from using the AWE method exhibits the most satisfactory and acceptable.

The RLCG model of the Π-configuration which was derived from using the AWE method was modified into an RLC model of the Π-configuration in chapter five. This model was mapped into an improved RC model based on the moment matching of the AWE method. Another mapping

process was applied to this model based on the capacitance charge and discharge to derive an equivalent RC model.

Buffer insertion technique was considered to reduce the interconnect delay. This technique was used and the equivalent RC model was considered to derive closed-form expressions for the interconnect critical length, minimum buffer size and optimum interconnect delay. These mathematical expressions were compared with an RC models in [101,103]. They show more accurate and acceptable results.

Future research could be extended to use the buffer tapering method (different buffer sizes) and different interconnect sizes. Also, capacitive load C_L and interconnect parasitic capacitances could be considered for the derivation of the mathematical expressions. Furthermore, future work could be focused on the power consumption and minimum chip area by using an equivalent RC model presented in this thesis. Another method such as a logical effort method could be used to calculate the interconnect delay instead of using the Elmore delay method. The same principle used for driving an improved RC model could be used to find an improved model from a T-Π or Π-T circuit.

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APPENDIX A

Driving Z-Parameter Modeling of the T-Configuration Based on the AWE Method

The input impedance of a short-ended z-parameter interconnect with normalized length can be found as illustrated in [64, 80].

$$Z_{in}(s) = Z_o \tanh(\sqrt{\ell\lambda}) \quad \text{Where} \quad \ell = 1 \quad, \quad Z_o(s) = \sqrt{Z_1 Z_2} \quad, \quad \lambda(s) = \sqrt{Z_1 / Z_2} \qquad \text{(A-1)}$$

So, $Z_{in}(s) = \sqrt{Z_1 Z_2} \tanh(\sqrt{Z_1 / Z_2})$ (A-2)

Using Taylor series formula, we can change the hyperbolic function into the polynomial series equation.

$$\tanh x = x - \frac{1}{3}x^3 + \frac{2}{15}x^5 - \frac{17}{315}x^7 + \ldots\ldots\ldots \text{ for } |x| < \frac{\Pi}{2} \qquad \text{(A-3)}$$

So, the hyperbolic function in z-parameter will be

$$\tanh(\sqrt{Z_1 / Z_2}) = \sqrt{\frac{Z_1}{Z_2}} - \frac{1}{3}\frac{Z_1}{Z_2}\sqrt{\frac{Z_1}{Z_2}} + \frac{2}{15}(\frac{Z_1}{Z_2})^2\sqrt{\frac{Z_1}{Z_2}} - \frac{17}{315}(\frac{Z_1}{Z_2})^3\sqrt{\frac{Z_1}{Z_2}} + \ldots\ldots \qquad \text{(A-4)}$$

The input impedance depends on the Taylor series formula will be

$$Z_{in}(s) = \sqrt{Z_1 Z_2}\, \tanh\sqrt{Z_1/Z_2} = \tanh(\sqrt{Z_1/Z_2}) = \sqrt{Z_1 Z_2}\sqrt{\frac{Z_1}{Z_2}} - \frac{1}{3}\sqrt{Z_1 Z_2}\sqrt{\frac{Z_1}{Z_2}}\frac{Z_1}{Z_2} + \frac{2}{15}\sqrt{Z_1 Z_2}\sqrt{\frac{Z_1}{Z_2}}(\frac{Z_1}{Z_2})^2 -$$

$$\frac{17}{315}\sqrt{Z_1 Z_2}\sqrt{\frac{Z_1}{Z_2}}(\frac{Z_1}{Z_2})^3 + ...$$

$$(A\text{-}5)$$

$$Z_{in}(s) = Z_1 - \frac{1}{3}\frac{Z_1^2}{Z_2} + \frac{2}{15}\frac{Z_1^3}{Z_2^2} - \frac{17}{315}\frac{Z_1^4}{Z_2^3} + ... \qquad (A\text{-}6)$$

Eq. (A-6) represents the general input impedance for interconnect z-parameter lumped model at short ended. We can easily find the input impedance for an interconnect lumped RC model as illustrated in Figure (A-1) directly from Eq. (A-6) as shown below:
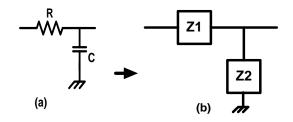

Figure A-1: Interconnect lumped model (a) RLC-model, (b) z-model.

Where $Z_1 = R$ and $Z_2 = \dfrac{1}{sC}$ then $\qquad\qquad\qquad\qquad\qquad (A\text{-}7)$

By considering equation (A-6), the input impedance for RC interconnect model will be

$$Z_{in}(s) = R - \frac{1}{3}R^2 Cs + \frac{2}{15}R^3 C^2 s^2 - \frac{17}{315}R^4 C^3 s^3 + A \qquad (A\text{-}8)$$

In the same way, we can find the input impedance for RLC and RLCG interconnect models. Now, we try to improve the improvement T-model from TPN by using AWE. Let us consider the T-model in the Figure 3.8.
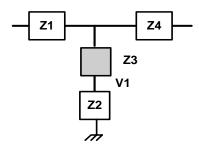
Figure A-2: Represents the improved T-model in z-parameter.

The input impedance for Figure (A-2) at short-ended is

$$Z_{in} = \frac{Z_4(Z_2 + Z_3)}{Z_2 + Z_3 + Z_4} + Z_1 \qquad \text{(A-9)}$$

$$Z_{in} = \frac{Z_1 Z_2 + Z_1 Z_3 + Z_1 Z_4 + Z_2 Z_4 + Z_3 Z_4}{Z_2 + Z_3 + Z_4} \qquad \text{(A-10)}$$

Assuming Figure (A-2) has a symmetric structure. i.e. $Z_1 = Z_4$, Eq. (A-10) can be written as

$$Z_{in} = \frac{2Z_1 Z_2 + 2Z_1 Z_3 + Z_1^2}{Z_1 + Z_2 + Z_3} \qquad \text{(A-11)}$$

Let us assume $Z_1 = Z_4 = R_1$, $Z_2 = \dfrac{1}{sC_1}$ and $Z_3 = R_3$ \qquad (A-12)

By considering these assumptions, Eq. (A-11) will be

$$Z_{in}(s) = \frac{2R_1 + (R_1^2 C_1 + 2R_1 R_3 C_1)s}{1 + (R_1 C_1 + R_3 C_1)s} \qquad \text{(A-13)}$$

By using the simple recursive formula as represented in Eqs. (2.44-2.46) of section 2.5.3,

$$Z_{in}(s) = \frac{a_0 + a_1 s + \ldots + a_{2n-1} s^{2n-1}}{1 + b_1 s + \ldots + b_{2n-1} s^{2n}} \quad (A-14)$$

Eq. (2.45) can be expressed using a polynomial of order 2n-1. As Taylor series

$$Z_{in}(s) = Z_0 + Z_1 s + \ldots + Z_{2n-1} s^{2n-1} \quad (A-15)$$

The coefficients of Eq. (A-14) can be found by using a simple recursive formula,

$$Z_k = a_k - \sum_{i=1}^{k} b_i Z_{k-i} \quad (A-16)$$

where $Z_{in}(s)$: The input impedance of a circuit in s-domain , Z_k : The coefficients of the input impedance , a_k : The coefficients of the numerator of the input impedance equation, n : The number of the circuit sections , and b_i : The coefficients of the denominator of the input impedance equation.

The rational input impedance of the model shown in Figure A-2 can be represented as a series function. So, from Eq. (A-14), the coefficients of the numerator and denominator of the input impedance can be represented as:

$$a_0 = 2R_1, \ a_1 = R_1^2 C_1 + 2R_1 R_3 C_1 \text{ and } b_1 = R_1 C_1 + R_3 C_1 \quad (A-17)$$

The series coefficients of the input impedance ($Z_1, Z_2, Z_3, Z_4, \ldots$) as illustrated in equation (A-15) can be found by considering equation (A-16). Thus

$$Z_0 = 2R_1, \ Z_1 = -R_1^2 C_1, \ Z_2 = R_1^3 C_1^2 + R_1^2 C_1^2 R_3 \quad (A-18)$$

So, the input impedance of the model shown in figure (A-2) at short-ended can be expressed as

$$Z_{in}(s) = 2R_1 + -R_1^2 C_1 s + (R_1^3 C_1^2 + R_1^2 C_1^2 R_3)s^2 \qquad \text{(A-19)}$$

We can find the circuit elements for the model shown in Figure A-2 by equating the first, second and third moments of the input impedances represented in Eqs. (A-8, A-19). Get

$$2R_1 = R \Rightarrow R_1 = \frac{R}{2}, -R_1^2 C_1 = -\frac{1}{3}R^2 C \Rightarrow C_1 = \frac{4}{3}C \text{ and} \qquad \text{(A-20)}$$

$$R_1^3 C_1^2 + R_1^2 C_1^2 R_3 = \frac{2}{15}R^3 C^2 \Rightarrow R_3 = -\frac{1}{5}R \qquad \text{(A-21)}$$

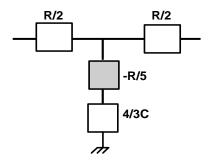The circuit of the T-model shown in the Figure (A-3) based on AWE will be

Figure A-3: Represents the RC T-model based on AWE.

In the same way, we can find the elements which represent the interconnect RLC or RLCG T-model based on the AWE.

APPENDIX B

Driving Z-Parameter Modeling of the Π-Configuration Based on the AWE Method

To explain the process of finding the general z-parameter input admittance of interconnect lumped model at open-ended as illustrated in Figure B-1, we will consider the works have been done in [64-80].
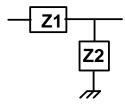

Figure B-1: Interconnect z-parameter of lumped model.

The admittance of an open-ended z-parameter interconnect can be obtained from the 2-port parameters as in [64, 80],

$$Y_{in}(s) = \frac{\tanh(\sqrt{(R+sL)Cs})}{\sqrt{(R+sL)/Cs}} = \frac{\tanh(\sqrt{Z_1/Z_2})}{\sqrt{Z_1 Z_2}} \tag{B-1}$$

where $Z_1 = R + sL$ and $Z_2 = \dfrac{1}{sC}$ then $\tag{B-2}$

Using Taylor Series formula, we can convert the hyperbolic function into the polynomial series.

$$\tanh x = x - \frac{1}{3}x^3 + \frac{2}{15}x^5 - \frac{17}{315}x^7 + ---- \quad \text{for } |x| < \frac{\Pi}{2} \tag{B-3}$$

The hyperbolic function can be expressed as a Taylor Series formula in z-parameters as

$$\tanh(\sqrt{Z_1/Z_2}) = \sqrt{\frac{Z_1}{Z_2}} - \frac{1}{3}\frac{Z_1}{Z_2}\sqrt{\frac{Z_1}{Z_2}} + \frac{2}{15}(\frac{Z_1}{Z_2})^2\sqrt{\frac{Z_1}{Z_2}} - \frac{17}{315}(\frac{Z_1}{Z_2})^3\sqrt{\frac{Z_1}{Z_2}} + ...$$ (B-4)

We can address the input admittance of z-parameter in s-domain using Taylor Series formula as

$$Y_{in}(s) = \frac{\tanh(\sqrt{Z_1/Z_2})}{\sqrt{Z_1 Z_2}} = \frac{\sqrt{\frac{Z_1}{Z_2}}}{\sqrt{Z_1 Z_2}} - \frac{1}{3}\frac{\frac{Z_1}{Z_2}\sqrt{\frac{Z_1}{Z_2}}}{\sqrt{Z_1 Z_2}} + \frac{2}{15}\frac{(\frac{Z_1}{Z_2})^2\sqrt{\frac{Z_1}{Z_2}}}{\sqrt{Z_1 Z_2}} - \frac{17}{315}\frac{(\frac{Z_1}{Z_2})^3\sqrt{\frac{Z_1}{Z_2}}}{\sqrt{Z_1 Z_2}} + ...$$ (B-5)

$$Y_{in}(s) = \frac{1}{Z_2} - \frac{1}{3}\frac{Z_1}{Z_2^2} + \frac{2}{15}\frac{Z_1^2}{Z_2^3} - \frac{17}{315}\frac{Z_1^3}{Z_2^4} + ...$$ (B-6)

Eq. (B-6) represents the general form of z-parameter input admittance for interconnect lumped model at open ended. By considering Eq. (B-2) and Eq. (B-6), the input admittance for RLC interconnect model can be expressed as

$$Y_{in}(s) = sC - \frac{1}{3}RC^2s^2 - (\frac{1}{3}LC^2 - \frac{2}{15}R^2C^3)s^3 + A$$ (B-7)

In the same way, we found the input admittance for RLC and RLCG interconnect models. Now, we will express the model shown in Figure 3.10 as a general z-parameter model.
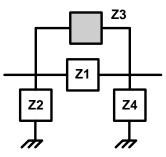
Figure B-2: Represents the improved Π-model in z-parameter.

For an open-ended z-parameter Π-model of the model as shown in Figure B-2, the deriving point admittance can be obtained as

$$Y_{in}(s) = \frac{Z_1 Z_3 + Z_1 Z_4 + Z_3 Z_4 + Z_1 Z_2 + Z_2 Z_3}{Z_2 (Z_1 Z_3 + Z_1 Z_4 + Z_3 Z_4)} \tag{B-8}$$

Eq. (B-8) represents the input admittance of a z-parameter Π-model as shown in Figure B-2 at open-ended. Assuming Π-model has a symmetric structure. i.e. $Z_2 = Z_4$. The input admittance represented in equation (B-8) can be expressed as

$$Y_{in}(s) = \frac{Z_1 Z_3 + 2Z_1 Z_2 + 2Z_2 Z_3}{Z_2 (Z_1 Z_3 + Z_1 Z_2 + Z_2 Z_3)} \tag{B-9}$$

Eq. (B-9) represents the input admittance of a general z-parameter Π-model at open-ended interconnect. We will use interconnect RLC Π-model to find the improvement of RLC Π-model using AWE. Let us assume

$$Z_1 = R_1 + sL_1, \ Z_2 = \frac{1}{sC_1}, Z_3 = \frac{1}{sC_3} \text{ and } Z_2 = \frac{1}{sC_2} \tag{B-10}$$

By considering Eqs. (B-9, B-10), the input admittance in s-domain can be expressed as

$$Y_{in}(s) = \frac{(C_1+C_2)s + (R_1C_1C_3 + R_1C_2C_3 + R_1C_1C_2)s^2 + (L_1C_1C_3 + L_1C_2C_3 + L_1C_1C_2)s^3}{1 + R_1(C_2+C_3)s + L_1(C_2+C_3)s^2} \qquad \text{(B-11)}$$

Using the simple recursive formula represented in Eqs. (30-32) of section 2.4.3,

$$Y(s) = \frac{a_0 + a_1 s + ... + a_{2n-1}s^{2n-1}}{1 + b_1 s + ... + b_{2n-1}s^{2n}} \qquad \text{(B-12)}$$

Eq. (B-12) can be expressed s Taylor series using a polynomial of order 2n-1.

$$Y(s) = Y_0 + Y_1 s + ... + Y_{2n-1}s^{2n-1} \qquad \text{(B-13)}$$

The coefficients of Eq. (B-13) can be found by using a simple recursive formula,

$$Y_k = a_k - \sum_{i=1}^{k} b_i Y_{k-i} \qquad \text{(B-14)}$$

where $Y(s)$: The input admittance of a circuit in s-domain

Y_k : The coefficients of the input admittance

n   : The number of the circuit sections

a_k : The coefficients of the numerator of the input admittance equation

b_i : The coefficients of the denominator of the input admittance equation

the rational input admittance of the model shown in Figure B-2 can be converted to a series function. So, from Eq. (B-11), the coefficients of the numerator and denominator of the input admittance can be represented as:

$$a_1 = C_1 + C_2 \,, a_2 = R_1 C_1 C_3 + R_1 C_2 C_3 + R_1 C_1 C_2 \,, a_3 = L_1 C_1 C_3 + L_1 C_2 C_3 + L_1 C_1 C_2$$
$$b_1 = R_1 C_2 + R_1 C_3 \text{ and } b_2 = L_1 C_2 + L_1 C_3 \tag{B-15}$$

We can find the coefficients of the input admittance as illustrated in Eq. (B-13) by considering the simple recursive formula in Eq. (B-14). Get

$$Y_0 = 0 \,, Y_1 = C_1 + C_2 \tag{B-16}$$

$$Y_2 = R_1 C_1 C_3 + R_1 C_2 C_3 + R_1 C_1 C_2 - \sum_{i=1}^{2}(R_1 C_2 + R_1 C_3)(C_1 + C_2) = -R_1 C_2^2 \tag{B-17}$$

$$Y_3 = L_1 C_1 C_3 + L_1 C_2 C_3 + L_1 C_1 C_2 - \sum_{i=1}^{3}(R_1 C_2 + R_1 C_3)(-R_1 C_2^2) + (L_1 C_1 + L_1 C_3)(C_1 + C_2)$$
$$Y_3 = -L_1 C_2^2 + R_1^2 C_2^3 + R_1^2 C_2^2 C_3 \tag{B-18}$$

The input admittance showed in Eq. (B-11) can be expressed as

$$Y_{in}(s) = (C_1 + C_2)s - R_1 C_2^2 s^2 + (R_1^2 C_2^3 + R_1^2 C_2^2 C_3 - L_1 C_2^2)s^3 \tag{B-19}$$

Assuming Π-model has a symmetric structure. i.e. $Z_2 = Z_4 \Rightarrow C_1 = C_2$. So, the input admittance will be

$$Y_{in}(s) = 2C_1 s - R_1 C_1^2 s^2 + (R_1^2 C_1^3 + R_1^2 C_1^2 C_3 - L_1 C_1^2)s^3 \qquad \text{(B-20)}$$

By equating the first, second and third moments of Eq. (B-7) with Eq. (B-20), get

$$C_1 = C_2 = \frac{C}{2}, \quad R_1 = \frac{4}{3}R, \quad L_1 = \frac{4}{3}L \text{ and } C_3 = -\frac{1}{5}C \qquad \text{(B-21)}$$

The RLC circuit for interconnect Π model can be build as shown in Figure B-3.
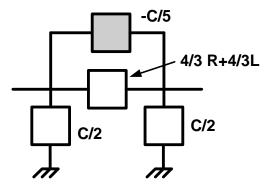

Figure B-3: Represents the interconnect RLC Π-model based on the AWE method.

In the same way, we can find the interconnect RC and RLCG Π-model based on AWE.

APPENDIX C

Closed-Form Expressions for Interconnect Critical Length, Minimum Buffer Sizing and Optimum Interconnect Delay

To calculate the interconnect critical length and optimum buffer size, let us consider the circuits shown in Figures C-1 and C-2
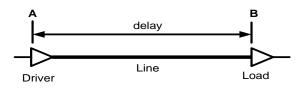

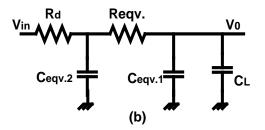Figure C-1: Interconnect with driver and load buffers.

Figure C-2: Circuit representation of Figure C-1.

The circuit shown in Figure C-2 is the representation model for the circuit shown in Figure C-1. The output resistance of the driver buffer is R_d , the gate capacitance of the load buffer is C_L and the interconnect is represented by the RC model shown in Figure 3.

To calculate the interconnect critical length and the optimum buffer size, we will consider the work in [101]. The delay of the circuit shown in Figure C-2 can be calculated using the Elmore delay [65]. Get

$$t_{pd} = R_d (C_{equv.2} + C_{equv.1} + C_L) + R_{equv.}(C_{equv.1} + C_L) \tag{C-1}$$

By considering Eqs. (1, 6, 8) and Eq. (C-1) can be expressed as

$$t_{pd} = R_d(C + C_L) + \frac{4}{3}R(\frac{7}{10}C + \frac{3}{4}\frac{L}{R^2} + C_L) \tag{C-2}$$

Where RLC are the interconnect resistance, inductance and capacitance respectively.

Eq. (C-2) can be expressed as a function of an interconnect length, get

$$t_{pd}(\ell) = R_d(\ell c + C_L) + \frac{4}{3}\ell r(\frac{7}{10}\ell c + \frac{3}{4}\frac{l}{\ell r^2} + C_L) \tag{C-3}$$

where $R = r.\ell, C = c.\ell$ and $L = l.\ell$

Dividing Eq. (C-3) on l to make the delay line is in linear proportion to the length of an interconnect. Yields

$$\frac{t_{pd}(\ell)}{\ell} = cR_d + \frac{R_d C_L}{\ell} + \frac{14}{15}\ell rc + \frac{l}{r\ell} + \frac{4}{3}rC_L \tag{C-4}$$

The optimal buffer insertion solution can be achieved by finding the optimal length l to

minimize $\dfrac{t_{pd}(\ell)}{\ell}$.

$$\frac{d(\frac{t_{pd}(\ell)}{\ell})}{d\ell} = 0 \tag{C-5}$$

$$\frac{d(\frac{t_{pd}(\ell)}{\ell})}{d\ell} = 0 = \frac{14}{15}rc - \frac{1}{\ell^2}(R_dC_L + \frac{l}{r}) \Rightarrow \ell_{crt.} = \sqrt{\frac{15(R_dC_L + \frac{l}{r})}{14rc}} \qquad \text{(C-6)}$$

This length shown in Eq.(C-6) represents the optimum length of an interconnect in which the interconnect delay is in linear proportion to its length. Eq. (C-6) is similar as the approaches in [37]. To find the number of segments for each interconnect length, we divide the interconnect length by the critical length as shown in Eq. (C-7)

$$\text{Number of segments} = \frac{\ell}{\ell_{crt.}} \qquad \text{(C-7)}$$

Also, number of buffers can be calculated as shown in Eq. (C-8)

$$\text{Number of buffers} = \text{Number of segments} + 1 \qquad \text{(C-8)}$$

To find the optimum inverter size to minimize the delay, we consider both Eqs. (C-4, C-6). Get

$$\frac{t_{pd}(\ell)}{\ell_{crt.}} = cR_d + \frac{R_dC_L}{\sqrt{\frac{15(R_dC_L + \frac{l}{r})}{14rc}}} + \frac{14}{15}rc\sqrt{\frac{15(R_dC_L + \frac{l}{r})}{14rc}} + \frac{l}{r\sqrt{\frac{15(R_dC_L + \frac{l}{r})}{14rc}}} + \frac{4}{3}rC_L$$

$$\text{(C-9)}$$

Expressing Eq. (C-9) as a function of buffer size h, get

$$\frac{t_{pd}(\ell)}{\ell_{crt.}}(h) = c\frac{R_0}{h} + \frac{R_dC_L}{\sqrt{\frac{15(R_dC_L + \frac{l}{r})}{14rc}}} + \frac{14}{15}rc\sqrt{\frac{15(R_dC_L + \frac{l}{r})}{14rc}} + \frac{l}{r\sqrt{\frac{15(R_dC_L + \frac{l}{r})}{14rc}}} +$$

$$\frac{4}{3}rC_0h$$

$$\text{(C-10)}$$

To optimize the buffer sizes to minimize the segment delay, we will drive Eq. (C-10) with respect to w and equalize it to 0.

$$\frac{d(\frac{t_{pd}(h)}{\ell_{crt.}})}{dh} = 0 \tag{C-11}$$

$$\frac{d(\frac{t_{pd}(h)}{\ell_{crt.}})}{dh} = 0 = \frac{4}{3}rC_0 - \frac{R_0 c}{h^2} \Rightarrow h = \sqrt{\frac{3R_0 c}{4rC_0}} \tag{C-12}$$

Eq. (C-12) represents the optimum buffer size can be used to minimize the interconnect delay. To find the delay per unit length of a properly repeated wire $\frac{t_{pd}}{l}$, we have to consider Eqs. (C-10, C-12). We get

$$\frac{t_{pd}(\ell)}{\ell_{crt.}}(h) = \frac{20R_0 cr\sqrt{\frac{3R_0 C_0 r + 3l}{c}} + 29R_0 C_0 c\sqrt{\frac{R_0 cr + 3l}{C_0}} + 29l\sqrt{\frac{R_0 c}{rC_0}}}{\sqrt{\frac{15(R_0^2 C_0 r + R_0 l)}{rC_0}}} \tag{C-13}$$