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CMOS RF Front-Ends For Bluetooth Applications

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CMOS RF Front-Ends for Bluetooth Applications

by

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Abstract

This project investigates the design of RF front-ends for bluetooth applications. The main objectives in each design are optimized noise figure, power consumption, gain and linearity.

The designed cascode LNA achieves 1.37 dB low noise figure through ports matching and maximizes the voltage gain to 11.5 dB. The port isolation reaches to 82 dB.

A 2 MHz low IF down-conversion mixer is developed. It employs current injection to reduce the fliker noise of MOSFETs. The total noise figure of the mixer is 17 dB and input referred IIP3 is 4.97 dB. A quadrature mixer constructed by two symmetric Gilbert mixeres is discussed.

A common-gate class E power amplifier is investigated. Through connecting a L matching network, the output power would be 17.7 dBm at 1.4 V power supply and the power added efficiency PAE and drain efficiency DE are 41% and 42.8% respectively.

To supply two LO frequencies with 90° phase difference, a quadrature voltage controlled oscillator is designed using a series coupling structure and accumulation mode PMOS varactors. The frequency tuning range is $2.304\,GHz \sim 2.54\,GHz$ when the control voltage changes from 0 to 0.7 V. The QVCO exhibits phase noise of -113 dBc/Hz at 600 kHz offset frequency and -119 dBc/Hz at 1 MHz offset frequency.

All the circuits were designed in TSMC-0.18μm 1.8 V CMOS technology and simulated using HSPICE RF simulator.

Acknowledgments

First and foremost, I would like to thank my supervisor Dr. Fei Yuan for his endless support, encouragement and patience. Without his guidance, this project would not have been possible to complete. I appreciate he directed me to the research field of RF circuit design, which broadened my knowledge and polished my design skills. His vast academic and technical expertise, endeavors and accomplishment in research have inspired and will continue to motivate me in the future.

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Abbreviations

BER	Bit Error Rate
CMOS	Complementary Metal-Oxide Semiconductors
CP	Charge Pump
DE	Drain Efficiency
FHSS	Frequency Hopping Spread Spectrum
FS	Frequency Synthesizer
GFSK	Gaussian Frequency Shift Keying
ICP1	Input Compression Point
IF	Intermediate Frequency
IIP3	Input Referred Third Order Intercept Point
ISM	Industrial, Scientific and Medical
LNA	Low Noise Amplifier
LF	Loop Filter
LPF	Low Pass Filter
LO	Local Oscillator
NF	Noise Figure
NMOS	N Type Metal-Oxide Semiconductors
OCP1	Output Compression Point
PA	Power Amplifier
PAE	Power Added Efficiency
PD	Phase Detector
PLL	Phase-locked Loop
PMOS	P Type Metal-Oxide Semiconductors

RF	Radio Frequency
RMS	Root Mean Square
SNR	Signal-to-Noise Ratio
SSB	Single Sideband
S-QVCO	Series Coupling Quadrature Voltage Controlled Oscillator
VCO	Voltage Controlled Oscillator
QVCO	Quadrature Voltage Controlled Oscillator

Chapter 1

Introduction

1.1 Background

1.1.1 An Overview of Bluetooth

The Bluetooth technology was developed to provide a wireless interconnect between small mobile devices and their peripherals. The system must fulfill the requirements of low power, low cost, high security and more integration such that its applications can be widely adopted. Bluetooth radios are designed to operate in the unlicensed ISM band, approximately $2.4 \sim 2.5$ GHz. There are many RF signals coexist in this band. In order to minimize system degradation due to outside interference, the system employs a frequency hopping spread spectrum (FHSS) scheme.

According to the Bluetooth specification v1.0. the Bluetooth technology has the following features:

- 79 frequency hopping channels covering frequency band 2.402 GHz $\sim$ 2.480 GHz, and 1 MHz channel bandwidth spacing.
- Frequency hopping scheme with 1600 hops/s, or 625 μs duration in each time slot. However, only 220 μs data processing time allowed in each channel.
- Gross symbol rate is 1 Mbits/s, and maximum data transfer rate up to 721 kbits/s for one-to-one connection.

- Gaussian frequency shift keying (GFSK) modulation with a constant envelope.
- The nominal link range is 10 centimeters to 10 meters and can be extended to 100 meters, depending on the transmit power. There are three transmission power levels in Bluetooth corresponding to the transmit distance: class3-0 dBm (1 mW), class2-4 dBm (2.5 mW) and class1-20 dBm (100 mW).

The specifications mentioned above determine the Bluetooth transceiver characteristics and architectures. They are transferred to receiver and transmitter specifications [1].

A. Receiver Specifications

- Sensitivity: The sensitivity for input signal is -70 dBm with 0.1% BER.
- Linearity: IIP_3 has to be -17 dBm in order to satisfy SNR and sensitivity.
- Gain Compression: 1 dB compression point should be -19 dBm.
- VCO phase noise: -71, -101, -111 dBc/Hz at 1 MHz. 2 MHz, 3 MHz offset.
- Noise Figure: lower than 25 dB.

B. Transmitter Specifications

- Output Power Level: Class1 20 dBm with 100 mW power output.

1.1.2 Figures-of-Merit

A. Noise

Noise is one of the most important factors to consider in RF design. Several noise sources are classified.

Thermal Noise: Thermal noise exists in resistors, lossy inductors and MOSFETs.

(1) Thermal Noise of Resistors

$$\overline{i_n^2} = \frac{4kT\,\Delta f}{R}, \tag{1.1}$$

where k is Boltzman's constant, T is the absolute temperature in Kelvins, R is the resistance and Δf is the bandwidth over which $\overline{i_n^2}$ is evaluated.

(2) Thermal Noise of MOSFETs in Saturation

$$\overline{i_{nd}^2} = 4kT\gamma g_m \Delta f, \tag{1.2}$$

where g_m is the transconductance, γ is 2.5 for MOSFETs in deep submicron region.

Flicker Noise Flicker noise shows up in ordinary resistors, however the thermal noise is dominant in resistors. MOSFETs exhibit more flicker noise than other devices. Corner frequency (1/f frequency) is defined as the frequency at which the power of the thermal noise and that of the flicker noise are equal.

The mean-square 1/f drain noise current is given by [2]

$$\overline{i_{nf}^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f, \tag{1.3}$$

where WL is the area of the channel, K is a device-specific constant and C_{ox} is the gate oxide capacitance per unit area. For a fixed transconductance g_m, the larger the gate area, the lower the fliker noise.

For NMOS devices, K is about 50 times larger than PMOS devices. In some design, PMOS is adopted when concerning 1/f noise.

Noise Figure The noise figure of a device quantifies the amount of the noise that the device contributes to the system.

$$F = \frac{Total\ equivalent\ input\ noise\ power}{Input\ noise\ power\ due\ to\ source\ only}. \tag{1.4}$$

The noise figure can also be defined by the ratio of signal-to-noise ratio(SNR)of input to that of the output.

$$F = \frac{SNR_{in}}{SNR_{out}}. \tag{1.5}$$

B. Sensitivity

Sensitivity of a receiver is the minimum input signal (S_{min}) required to produce a specified output signal for a given SNR and is defined as the minimum signal-to-noise ratio times the mean noise power.

$$S_{min} = (SNR)_{min} KTB\,(NF)\,, \tag{1.6}$$

where $(SNR)_{min}$ is the minimum SNR to detect a signal, B is the receiver bandwidth and NF is the noise figure.

If a receiver system is connected to an antenna, the sensitivity can be calculated from

$$S_{min} = (SNR)_{min} KTB\,(NF)\,/G, \tag{1.7}$$

where G is the gain of the receiver.

The Bluetooth standards specify that a -70 dBm signal (P_{in}) should be corectly demodulated with an 0.1% bit error rate (BER).

C. Gain

Voltage Conversion Gain Voltage conversion gain is the ratio of the RMS of the output voltage to that of the input voltage, and is usually expressed in decibels.

$$Voltage\,Gain = 10\log\left(\frac{V_{rms}out}{V_{rms}in}\right). \tag{1.8}$$

Power Conversion Gain Power conversion gain is the ratio of the power (P_2) delivered to the load to the power (P_1) delivered by the source.

$$Power\,Gain = 10\log\left(\frac{P_2}{P_1}\right). \tag{1.9}$$

D. Linearity

Linearity is one of the most important issues for RF circuits. For low frequency circuits, it is common to quantify the nonlinearity of a circuit by measuring the distortion in the output signal. At high frequencies, it is common to characterize the distortion produced by the circuit in terms of the 1 dB compression point and the intermodulation point. Both are needed. The former for harmonic distortion while the latter for intermodulation distortion.

1 dB Compression Point To measure the 1 dB compression point of a circuit, we apply a sinusoid to its input and evaluate the power of the fundamental of the output voltage. The 1 dB compression point (P1dB) is the point where the gain of the circuit has dropped by 1 dB from its ideal value.

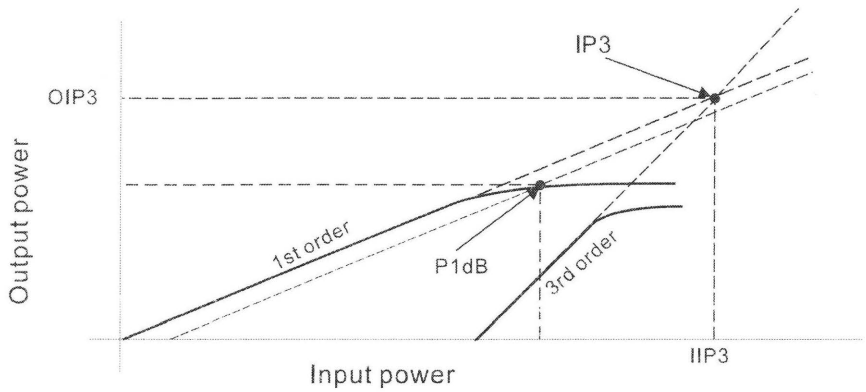

Figure 1.1: 1 dB compression point and 3rd-order intercept point.

Intercept Point Apply two closely spaced sinusoids with the same amplitude to a narrowband circuit, as shown in Fig.1.2. Their harmonics can be filtered out by a bandpass filter. However the third order intermodulation distortion existing at $2f_1 - f_2$, $2f_2 - f_1$, as shown in Fig.1.2, is very close to the frequencies of the desired signals and can not be filtered out. Hence the measurement of these distortions will help evaluate the linearity of the circuits. The third order intercept point (IP_3), is commonly used to quantify intermodulation distortion, as shown in Fig.1.1. IIP_3 is the input referred third order intercept point.

The relationship between P1dB and IIP_3 is given by [6]

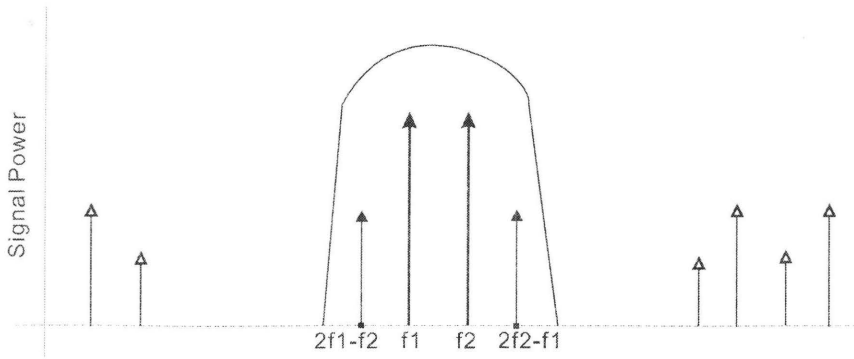

Figure 1.2: The third order intermodulation products .

$$P1dB = IIP_3 - 9.6\,dB. \tag{1.10}$$

1.1.3 RF Transceiver Architectures

A. Heterodyne System

A heterodyne system, dual conversion architecture, is employed to solve the image rejection problem [7]. In Fig.1.3, two local oscillators (LOs) are used. The first one operates at 1.6 GHz and the second one at 800 MHz. After the switch, a low noise amplifier (LNA) first amplifies the received signals (2.4 GHz). Then the first quadrature mixer down-converts the RF signal to a signal at intermediate frequency (800 MHz). The second mixer converts IF signal down to zero hertz carrier frequency. Through low pass filter (LPF) and demodulator, the baseband signal can be acquired. After the first down-conversion stage, the image frequency is reduced to 800 MHz compared to the 2.4 GHz image frequency in direct conversion architecture. The image rejection is improved.

In transmitter path, the quadrature modulated baseband signals are first up-converted to 800 MHz and then added together. In the second mixer, the result is up-converted from 800 MHz to 2.4 GHz. After two conversions, the RF signal is applied to a power amplifier (PA) to drive the antenna. The strong noisy signal at the output of the power amplifier may couple to the local oscillator (LO), causing the phenomenon known as LO pulling. This means that the frequency of the local oscillator is pulled away from the desired value if the LO frequency

is very close to the carrier frequency and the power of the noise at the output of PA is big. One of the ways to alleviate the LO pulling is moving the PA spectrum sufficiently far from the LO frequency. Since the carrier frequency in dual conversions is formed by mixing two lower LO frequencies, the LO pulling by the power amplifier is negligible compared to its counterparts direct-conversion.

The drawback of heterodyne structure is more complexity, less integration and more power consumption.

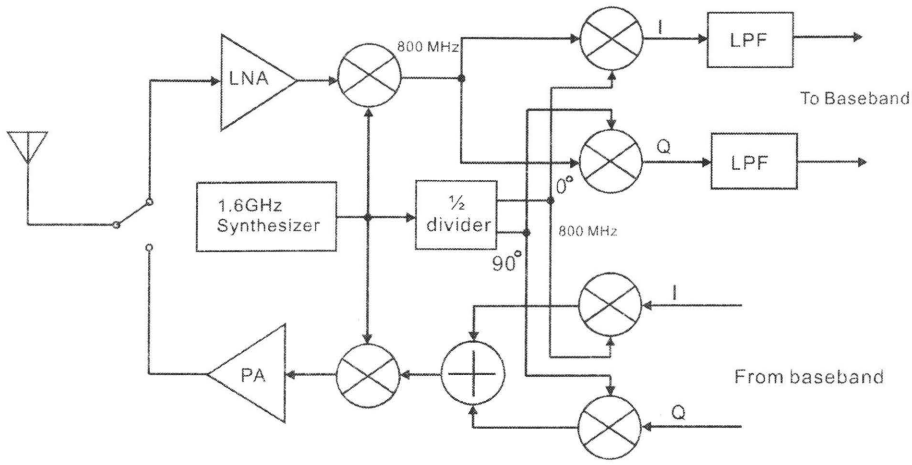

Figure 1.3: Dual conversion transceiver architecture.

B. Homodyne System

Homodyne systems, direct conversion architectures, are simpler and suitable for monolithic circuits. Only one mixer is needed in each transmitter and receiver path.

A typical direct conversion transceiver architecture is shown in Fig.1.4 [8]. Mixing is performed to down-convert the RF signals to an IF frequency at (near) zero Hertz. The image frequency is the same as the desired signal. A big advantage of direct conversion is that there are no image problems, and the IF selection filter becomes a pair of low pass filters at baseband. This allows the filter to have even greater selectivity with better gain and phase response.

However, DC offset and 1/f noise may significantly degrade the receiver performance. DC offset is caused by the LO leakage to the antenna, LNA or the input of mixer. Then the

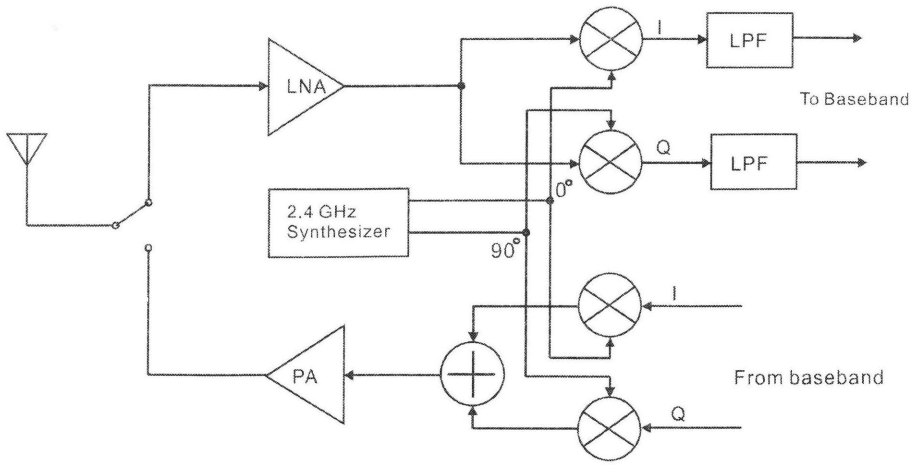

Figure 1.4: Direct conversion transceiver architecture.

leakage signal is mixed with the LO, generating DC component. The LO pulling is another concerned issue.

Low IF (2 MHz) receiver architectures are more attractive in Bluetooth transceivers [9, 10, 11]. Since the image frequency and the wanted frequency will be converted to the same IF frequency after mixing, the mixer can not distinguish the positive frequency and negative frequency. Therefore Mixer is designed to be quadrature structure such that its outputs are two signals with 90 degree phase difference. This topic will be discussed in Chapter 3 in detail.

1.2 Motivation

The rapid development and wide applications of Bluetooth transceivers introduce new design issues and challenges. Due to the scaled down power supply, the power consumption should be low to last the life of battery. Low cost requires the architectures of Bluetooth transceivers are simpler and highly integrated. Bluetooth transceivers must have high noise rejection in the interfered circumstance. These are the challenges on designing the circuit of Bluetooth transceivers by meeting all design specifications.

This project mainly investigates the design methodologies for Bluetooth tranceiver front-ends, which includs a low noise amplifier, a low IF quadrature down-conversion mixer, a

common-gate class E power amplifier and a quadrature voltage controlled oscillator. However frequency synthesizer, up-conversion mixer and IF filter are excluded. The main objectives of this project are reduce the power consumption, minimize the noise figure and increase the gain while designing all the blocks.

1.3 Project Organization

The project is organized as follows. In Chapter 2, a low noise amplifier is designed. which focuses on the impedance matches of the input and output port. Chapter 3 investigates the design of low IF (2 MHz) down-conversion mixer. It employs the current injection to reduce the 1/f noise. A quadrature mixer constructed by two symmetric Gilbert mixers is discussed in this chapter. Its performance is compared with that of Gilbert mixer. A class E power amplifier is designed in Chapter 4, which adopts the common-gate structure to increase the isolation between the ports. Chapter 5 illustrates the design of quadrature VCOs, and the design objective in this chapter is reduce the phase noise while meeting the tuning range. The conclusions and future work are presented in Chapter 6.

Chapter 2

Low Noise Amplifier

The front-ends of a receiver consist of a low noise amplifier (LNA), down-conversion mixers and an IF filter. The noise figure of the LNA will directly add to that of the system. In addition to noise figure, LNA should have relatively high gain with good linearity. Section2.1 presents the structure of a casode LNA. The impedance matches of input and output port are discussed in Section2.2. Section2.3 shows the simulation results of the performance of the LNA, including S-parameters, the impedances of input and output, the noise figure, nonlinearity and gain. This chapter is summarized in Section2.4.

2.1 Cascode LNA

The basic structure of a cascode LNA is depicted in Fig.2.1. M_1 is the input transistor, which mainly contributes the gain. M_2 acts as the cascode transistor, which provides the isolation between the input and output ports and improves the stability of the amplifier. Merging the drain of M_1 and the source of M_2 can minimize the capacitance at the drain of M_1. Inductor L_s and L_g are for impedance matching while L_d for bandwidth improvement.

2.2 Impedance Match

As shown in Fig.2.1, the input of LNA is connected to the antenna, which is modeled as a 50 Ω resistor. When the input impedance is matched to 50 Ω, the noise figure will be minimized and the power transfer will be maximized. Sometimes these two performance

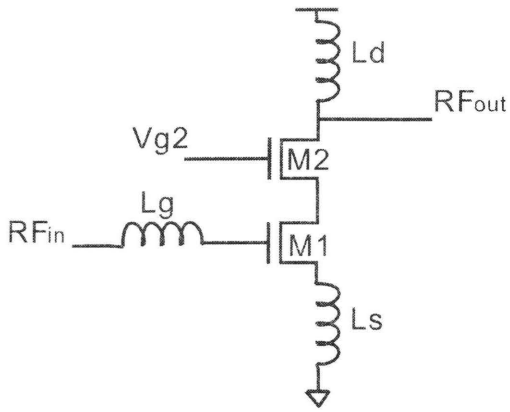

Figure 2.1: Csacode LNA.

parameters can not achieve concurrently. In this section, only noise match is discussed, since NF is most concerned.

The input impedance Z_{in} is given by [7]

$$Z_{in} = L_s \frac{g_m}{C_{gs}} + \frac{1}{C_{gs}s} + L_s s, \tag{2.1}$$

where C_{gs} is gate-source parasitic capacitance of M_1, g_m is the transconductance of M_1.

The real part of the input impedance is

$$R_{in} = L_s \frac{g_m}{C_{gs}}, \tag{2.2}$$

Inductor L_s is for the source degeneration. since it reduces the noise effect as compared with resistance degeneration. It is also the ground at DC, increasing the voltage headroom.

The imaginary part of input impedance is

$$I_m(Z_{in}) = L_s\omega - \frac{1}{C_{gs}\omega}. \tag{2.3}$$

When $L_s\omega = \frac{1}{C_{gs}\omega}$, the imaginary part vanishes and Z_{in} is real. Due to the small parasitic capacitanceC_{gs}, L_s must be very large in order to provide the needed 50 Ω input impedance. To solve this problem, L_g is used. The imaginary part of the input impedance becomes

$$I_m(Z_{in}) = L_g\omega + L_s\omega - \frac{1}{C_{gs}\omega}. \tag{2.4}$$

When $L_g\omega + L_s\omega = \frac{1}{C_{gs}\omega}$, the input impedance is purely resistive. L_g is called matching inductor.

The LNA with bias circuit is shown in Fig.2.2. The effect of DC blocking capacitors C_1 and C_2 on the resonate frequency is negligible. M_3, R_1, R_2, R_3 construct the bias circuit that creates the biasing voltages for M_1 and M_2.

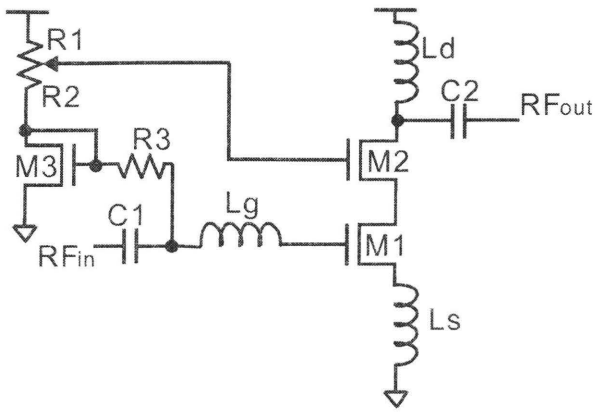

Figure 2.2: Cascode LNA with biasing circuitry.

Table.2.1 lists the component parameters of the LNA designed in TSMC-0.18μm 1.8 V CMOS technology.

Table 2.1: Parameters of LNA, the length of the transistors is 0.35 μm.

Components	Value
M1,M2	800 μm
M3	70 μm
Lg	40 nH
Ls	0.6 nH
Ld	8.2 nH
C1,C2	10 pF
R1	440 Ω
R2	2 KΩ
R3	360 Ω

2.3 Simulation Results

2.3.1 Scattering Parameters

The simulation results of S-parameters are plotted in Fig.2.3 and Fig.2.4. Around frequency 2.45 GHz, the reflection coefficients of input port s_{11} is -24.6 dB, and the output reflection coefficient s_{22} is -57.6 dB. The voltage gain reaches to 11.5 dB. The reverse isolation(s_{12}) is -82 dB.

In Fig.2.5 and Fig.2.6, the real parts of input and output resistances $R_e(Z(1,1))$ and $R_e(Z(2,2))$ are matched to 50 Ω, however the optimum source impedance for minimum noise Z_{opt} is 75.8 Ω. That means the noise figure will not be the same as the minimum noise figure.

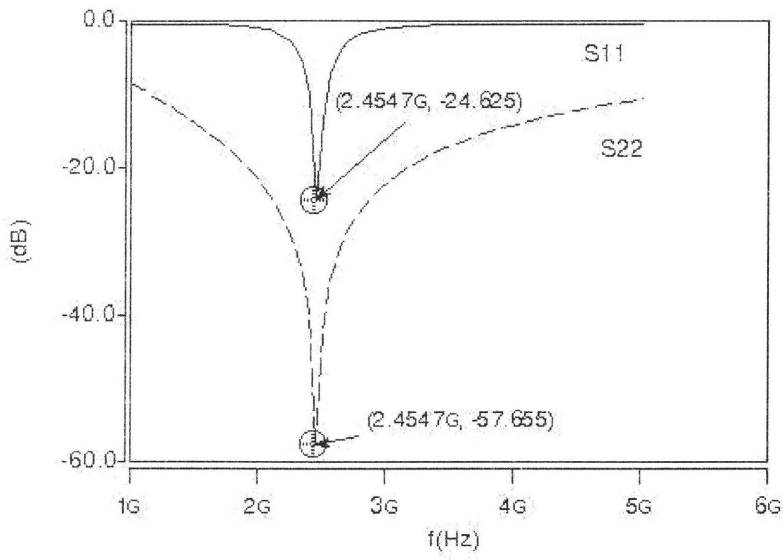

Figure 2.3: Reflection coefficients of LNA.

2.3.2 Noise Figure

The noise figure and the minimum noise figure are shown in Fig.2.7. Between the frequency 2.25 GHz and 2.38 GHz, NF equals to NFmin. NF is 1.37 dB and NFmin is 1.1

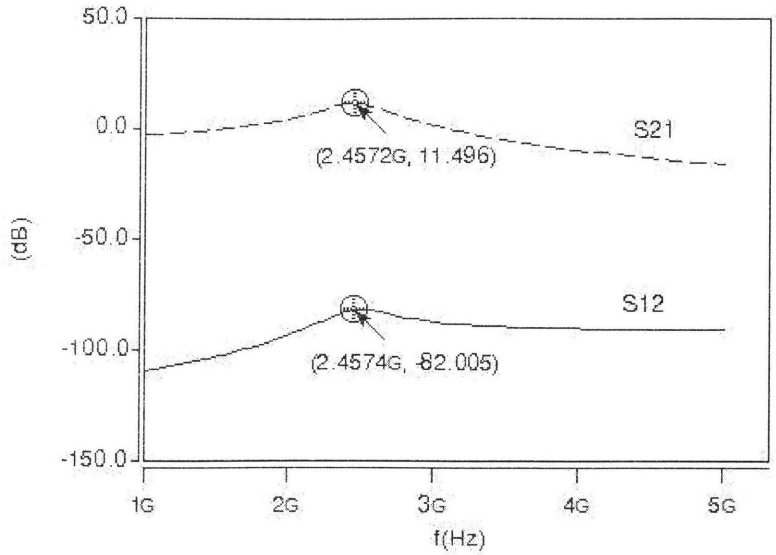

Figure 2.4: Gain of LNA.

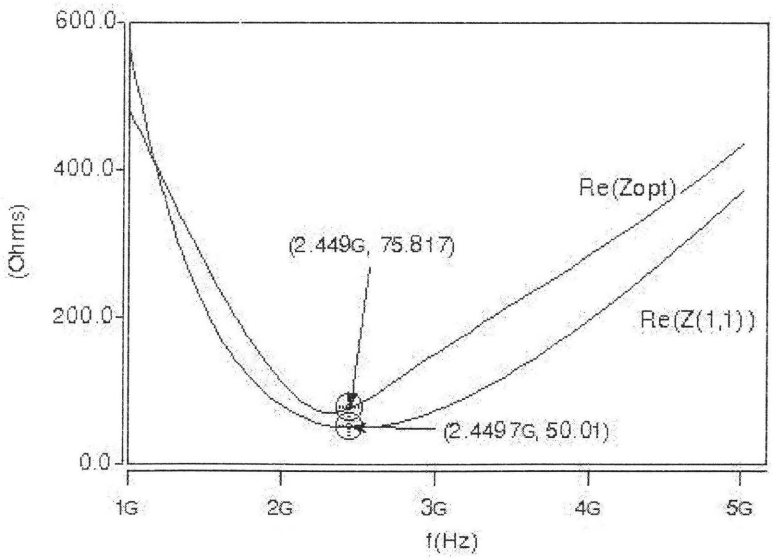

Figure 2.5: Input impedance and the optimum input impedance at the minimum noise figure.

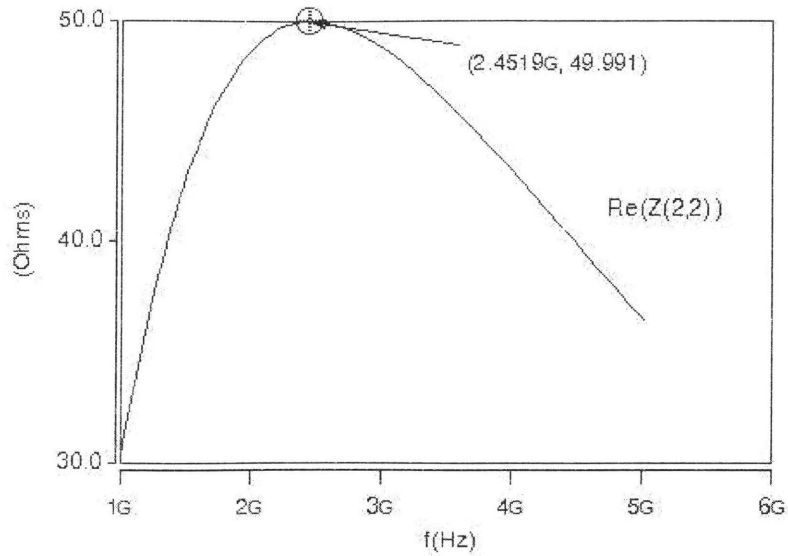

Figure 2.6: Output impedance.

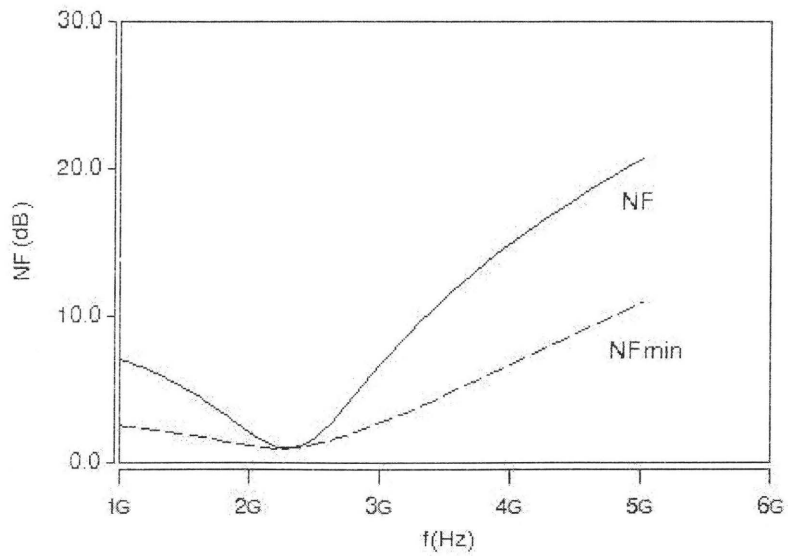

Figure 2.7: Noise figure of LNA.

dB at 2.45 GHz. Through impedance matches of input and output port, the LNA achieves relatively low NF.

2.3.3 Power Gain

The power gain is shown in Fig.2.8. Around 2.45 GHz, the maximun available power gain G_{max} is 11.5 dB. If the NFmin is obtained, the power gain will be slightly decreased. Compared to Fig.2.3, the voltage gain is almost equal to the power gain. That means the input and output network matching is good.

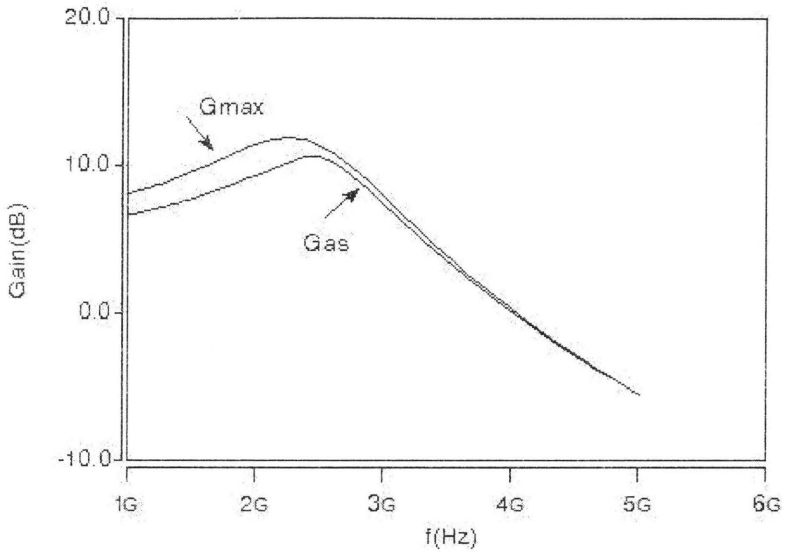

Figure 2.8: Maximum available power gain G_{max} of LNA.

2.3.4 Intercept Point

We set the fundamental frequency f_1 (2.45 GHz) and the second frequency f_2 (f_1+500 kHz) such that the third order intermodulation products fall inside the bandwidth of the desired signals . The 1 dB compression point, measured at the input power level -70 dBm, is -18.9 dBm. The LNA maintains good linearity. The third order intercept point (IIP3), as shown in Fig.2.10, is -15.2 dBm.

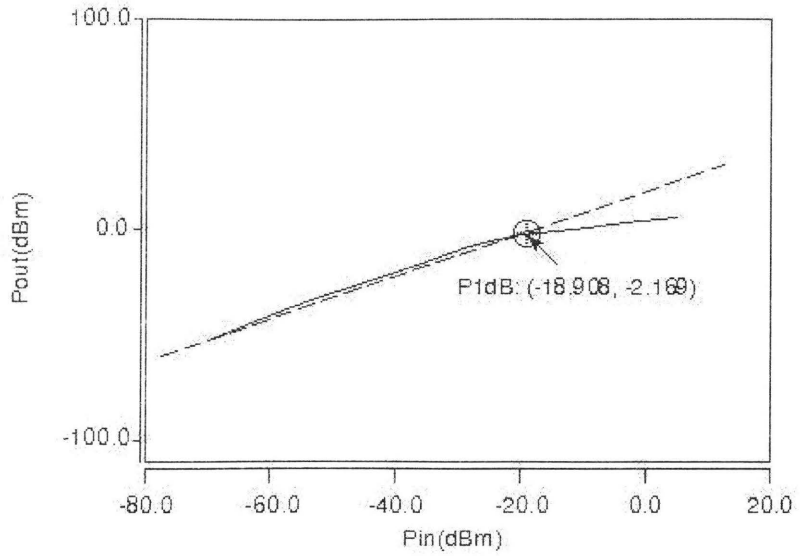

Figure 2.9: 1 dB compression point of LNA.

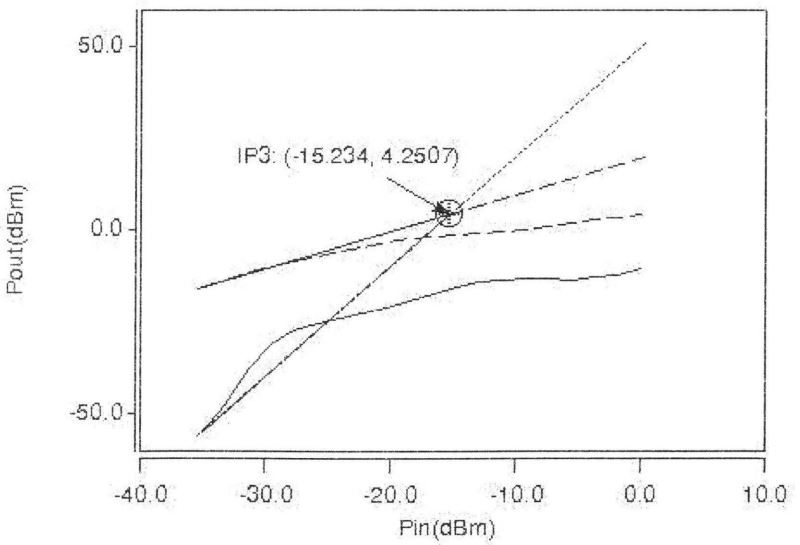

Figure 2.10: IIP3 of LNA.

The performance of LNA is summarized in Table2.2.

Table 2.2: Performance of LNA at 2.4 GHz.

Frequency	2.45 GHz
Supply Voltage	1.8 V
Current Consumption	9.7 mA
Power Dissipation	18 mW
Gain	11.5 dB
Noise Figure	1.37 dB
Reverse Isolation	82 dB
P1dB	-18.9 dBm
IIP3	-15.2 dBm

2.4 Summary

The cascode LNA with biasing circuitry has been presented in this chapter. The impedance matches of input and output port were discussed in detail. The simulation results showed that the input and output impedance were matched to 50 Ω. as well as the LNA achieved the maximum power gain. However, the noise figure of the LNA is sightly higher than the minimum noise figure. There is compromise between maximun power gain and minimum noise figure. The voltage gain reaches around 12 dB while keeping good linearity.

Chapter 3

Double-Balanced Quadrature Mixer

This chapter presents the design of down-conversion mixers. Section3.1 reviews the architectures of single-balanced mixer and double-balanced mixer (Gilbert mixer). A double-balanced mixer with current boost is designed and simulated in Section3.2. Section3.3 discusses the design of the quadrature mixer and compares its performances to that of the Gilbert mixer. This chapter is summarized in Section3.4.

3.1 Gilbet Mixers

Mixer acts as a multiplier that translates two input signals into a signal with a new frequency. The output of a mixer that has two sinusoidal inputs is given by

$$(A\cos\omega_1 t)(B\cos\omega_2 t) = \frac{AB}{2}[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t]. \tag{3.1}$$

If ω_1 is a RF signal and ω_2 is the frequency of a local oscillator (LO), the frequency of the output of the mixer contains the sum and difference of the frequencies. This principle can be used for up-conversion and down-conversion of RF input signals.

The mixers can be classified to be active mixers and passive mixers. Active mixers supply gain while mixing the frequencies. Passive mixers only employ mixing functions and has no fliker noise in theory. The mixers are also classified by their inputs and outputs as single-balanced mixers and double-balanced mixers.

3.1.1 Single-Balanced Mixer

Fig.3.1 is the schematic of a single-balanced mixer with a single-ended RF input and a differential LO input. The RF input and LO inputs are at different ports such that a better isolation of signals is obtained.

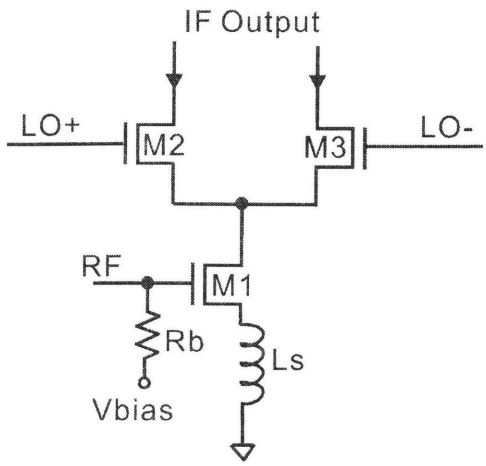

Figure 3.1: Single-balanced mixer .

M_1 is a transconductor that converts the RF voltage into a drain current, it also supplies the gain to the circuit. M_2 and M_3 are switches that steer the drain current of M_1 to obtain frequency translation. The DC currents through these switches should be zero if they totally commute. In practice, the switches may concurrently conduct for a short period of time. On the other hand, the gate sizes of switches should be made large to reduce noise. However this will increase the capacitance and consume more power.

Inductor L_s is for source degeneration. It is virtual ground at DC to increase voltage headroom and the increasing reactance of an inductor with increasing frequency helps to attenuate high frequency harmonic and intermodulation components. R_b is chosen to be large enough to reduce its noise contribution.

3.1.2 Double-Balanced Mixer

Two single-balanced mixers are connected together to produce a double-balanced mixer, as shown in Fig.3.2. It is also called Gilbert-type mixer.

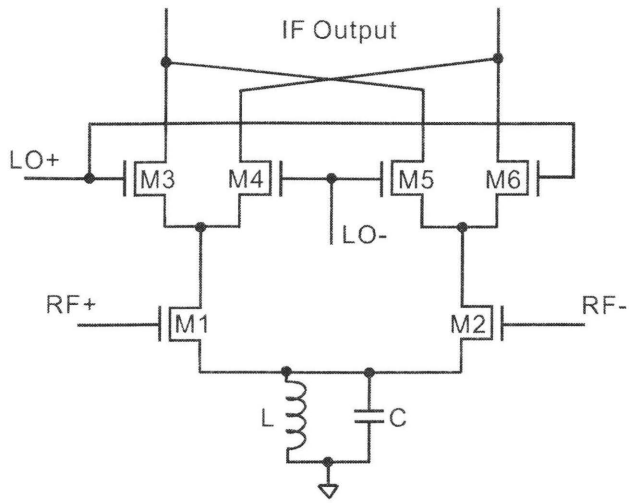

Figure 3.2: Double-balanced mixer.

The differential RF inputs improve the linearity of the mixer [2]. Due to the LO self-mixing, an unwanted DC component is generated in the output of mixer. The differential outputs of the mixer can suppress the common mode noises. The parallel LC tank source degeneration creates a zero-headroom AC current source. The resonate frequency of the tank should be chosen to provide rejection of common-mode components. This is the widely used mixer configuration.

3.2 Double-Balanced Mixer With Current Boost

3.2.1 Configuration

In Gilbert mixer, the drain current of M_1 directly feeds into the source of the switching transistors M_3 and M_4. To obtain a large gain and good linearity, the drain current of M_1 must be large. However 1/f noise performances of the mixer are primarily determined by the

switching pair devices. Minimizing the 1/f noise leads to the large area switching transistors and low biasing currents [17]. Hence, the currents of the input stage and the switching stage can be set independently to simultaneously optimize noise figure, linearity, and gain. New configurations were proposed in [18, 19, 20]. As shown in Fig.3.3, an additional current source I_{ss} is connected to the drains of the tranconductors M_1 and M_2. This technique is called current boost or current bleeding. Due to the injected current, the dc current that flows through the switching transistors is reduced.

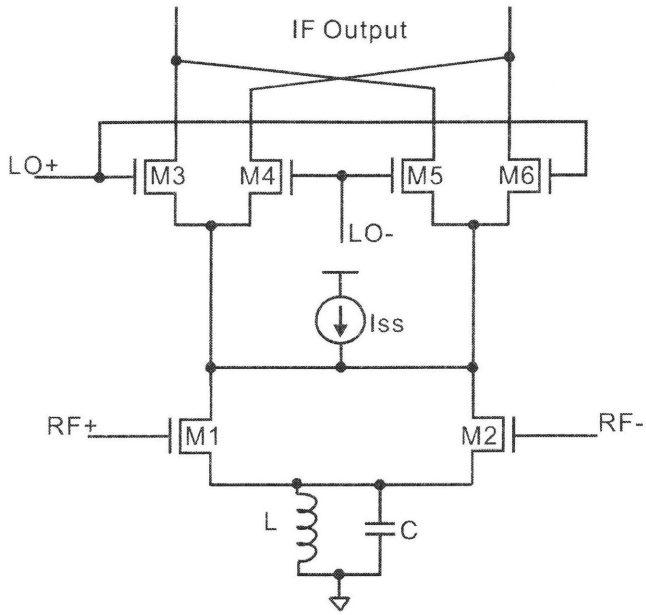

Figure 3.3: Double-balanced mixer with current boost.

In this design, the boost current source is constructed by a current mirror, shown in Fig.3.4. It is connected to the drains of M_1, M_2 through two PMOS transistors M_7, M_8, because PMOS transistors exhibit lower $1/f$ noise.

The drain current of M_9 is 3 mA, and the current injected to the drain node of M_1 is 1.5 mA.

The final circuit diagram is shown in Fig.3.5. R_1C_1 and R_2C_2 are low pass filters. L_1C_5 tank is for source degeneration. Its resonate frequency is set to be twice RF frequency to

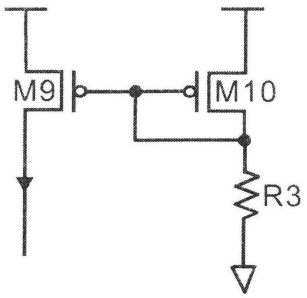

Figure 3.4: Boost current source.

reduce the second order distortion. V_g, the bias voltage for transconductors to generate biasing current, is set to be 0.9 V such that 0.2 V $\sim$ 0.3 V overdrive voltage makes M_1, M_2 work in the saturation region. R_{g1} and R_{g2} should be made large such that they do not contribute the noise performance significantly.

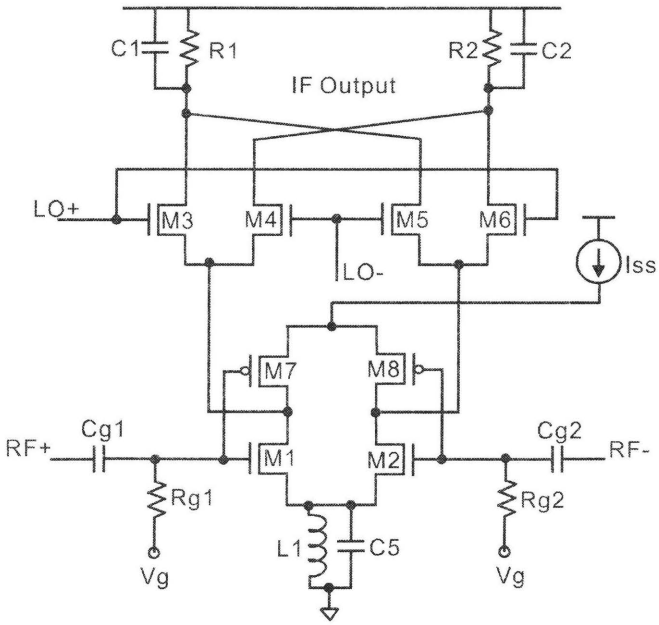

Figure 3.5: Double-balanced mixer with current injection.

Table.3.1 tabulates component parameters. The gate length of all transistors is 0.18 μm.

Table 3.1: Parameters of double-balanced mixer with current boost.

Components	Value
M1,M2	100 μm
M3,M4,M5,M6	200 μm
M7,M8	250 μm
M9	320 μm
M10	40 μm
R1,R2	500 Ω
R_3	600 Ω
$R_{g1}, Rg2$	2 KΩ
C1,C2	5.7 pF
C_{g1}, C_{g2}	10 pF
L_1	3 nH
C_5	0.35 pF

3.2.2 Simulation Results

(1) Noise Figure

The noise sources of the mixer include the thermal noise of input resistors R_{g1}, R_{g2} and load resistors R_1, R_2, the thermal noise of transistors, as well as the flicker noise of MOSFETs. The main contributors are the thermal noise of the resistors and 1/f noise of the transistors. R_{g1} generates around 4.3 dB noise to the mixer at the value of 2 $K\Omega$. The total noise figure at the output of mixer is 17 dB in Fig.3.6.

If switching of the four transistors in mixer core had been ideal, only two transistors would have been conducting in every single moment and only two transistors would have been generating noise. However, there are small intervals in which the four transistors are all on. The length of this interval depends on the LO signal, its voltage level and shape.

Hence the LO amplitude (V_{LO}) and common mode voltage should be chosen with care. Since the layout will slightly change the component parameters, in the DC steady state, the drain current of switching transistors is set to be 0.26 mA. With an additional injected current, the drain current of M_1 is 2 mA. The boost current draws away about 70% of the total drain current. The common mode voltage of LO is set to be 0.8 V and V_{LO} is 300 mV. The power level is 5 dBm and its frequency range is 2.4 GHz$\sim$ 2.48 GHz. The amplitude

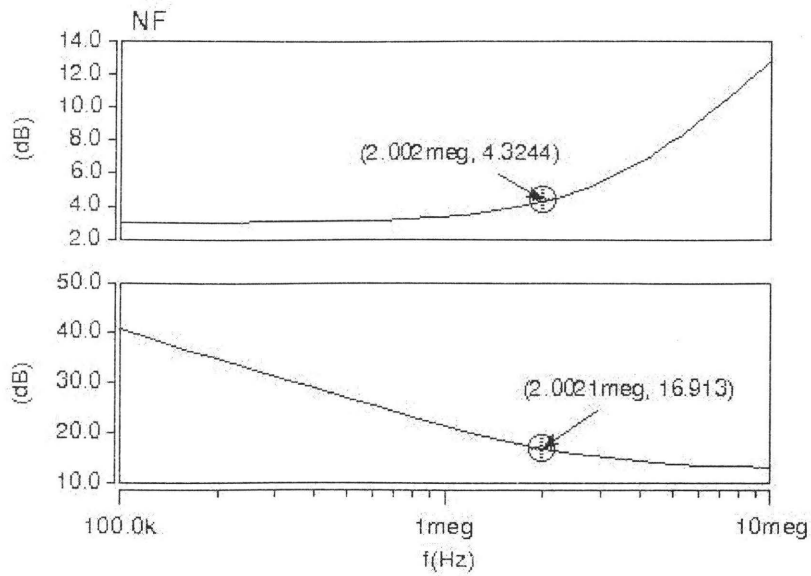

Figure 3.6: Noise figure of mixer. The upper figure is the NF contributed by R_{g1}, The lower figure is the total NF of mixer.

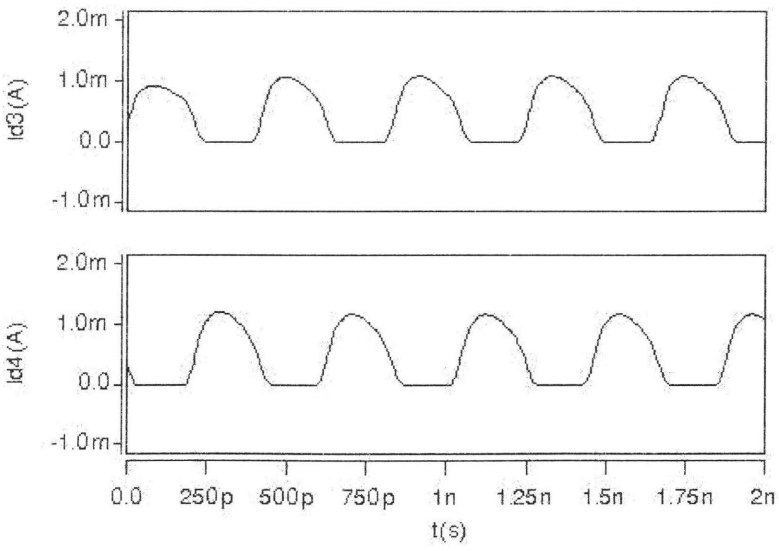

Figure 3.7: Drain currents of M_3 and M_4.

of RF input signal is set to be 10 mV, power level is -10 dBm, and the frequency range is 2.402 GHz$\sim$ 2.48 GHz.

As depicted in Fig.3.7, when M_3 is ON, M_4 is OFF. However both of them are ON for a short period of time and the conduct current is 0.26 mA.

(2) Transient Analysis

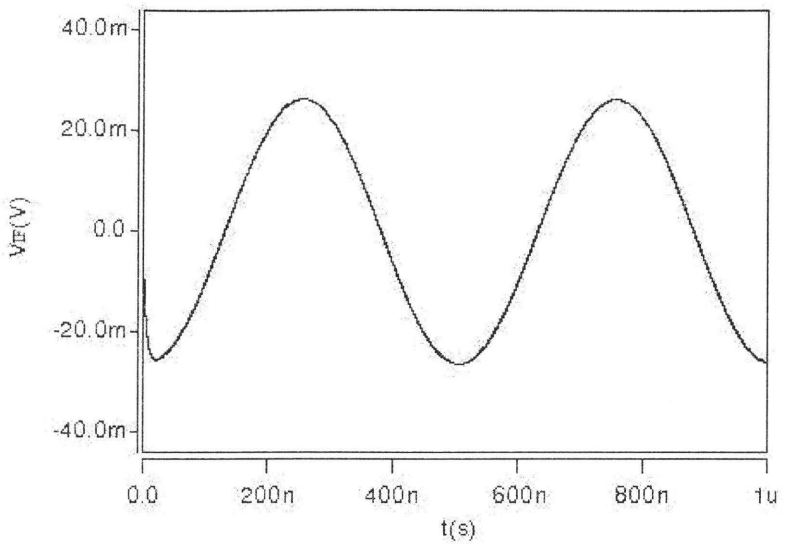

Figure 3.8: Differential output of IF port at 2 MHz.

Fig.3.8 and Fig.3.9 are the transient response of the differential IF output and that of the RF input. The mixer translates the RF signal into a low IF 2 MHz signal. Comparing these two waveforms, the voltage gain of the mixer is 4 dB. The main contributor of the voltage gain is the transconductance stage, and the drain current of M_1 and M_2 should be as large as possible. However the tradeoffs of gain and noise exist.

(3) Linearity

RF frequency f_{RF} is set to be 2.402 GHz and the LO frequency f_{LO} is 2.4 GHz. To measure IIP3, insert a second RF signal f_{RF2} (2.4022 GHz), 200 kHz apart from the first RF fundamental frequency. Using harmonic balance analysis, 1 dB compression point and

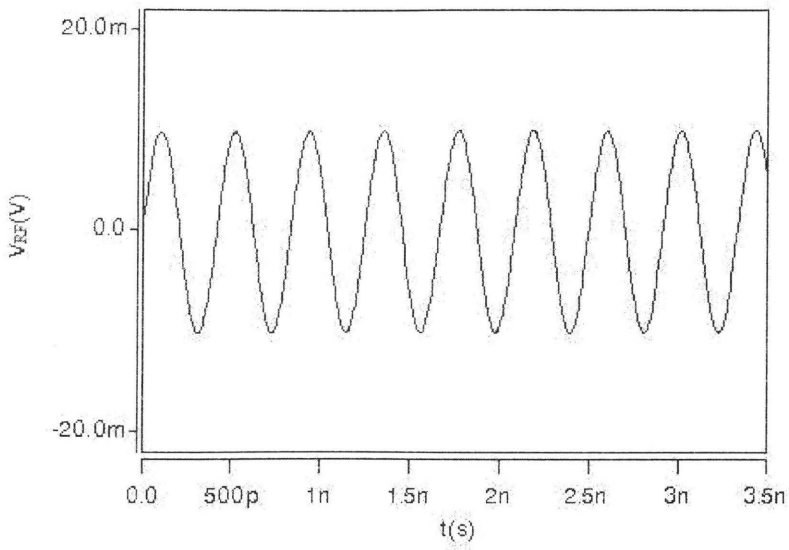

Figure 3.9: Differential input of RF port at 2.402 GHz.

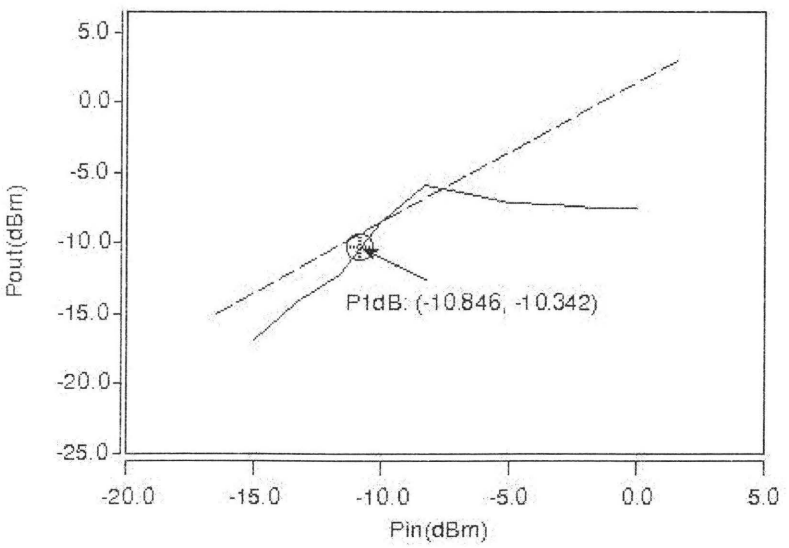

Figure 3.10: 1 dB compression point of mixer.

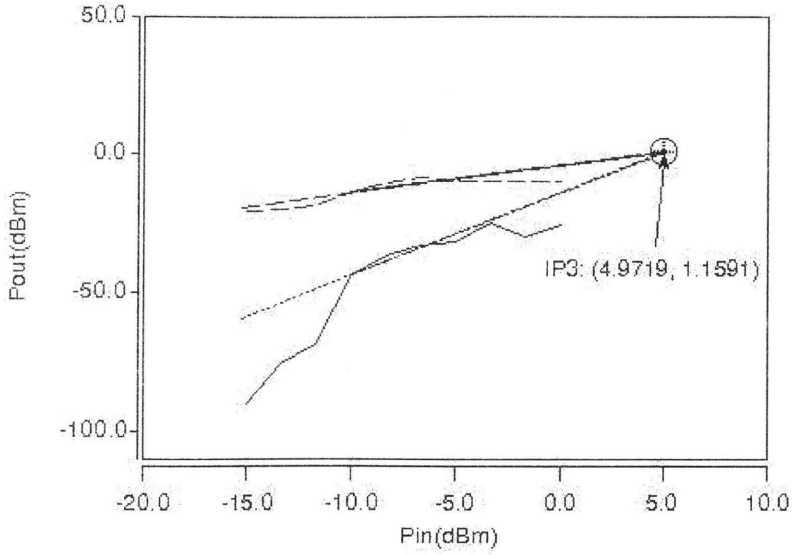

Figure 3.11: IIP3 of mixer.

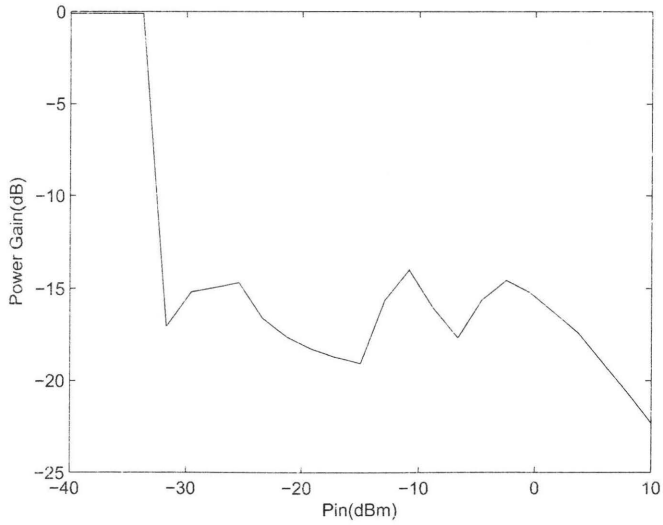

Figure 3.12: Power conversion gain of mixer.

input referred IIP3 are analyzed and the results are shown in Fig.3.10 and Fig.3.11.

Fig.3.12 shows the power conversion gain. When the power level of RF input (P_{RF}) is higher than -30 dBm, the output power at the IF port is lower than P_{RF}, and the power gain is -15 dB at -10 dBm input level. Hence this mixer will not supply power gain or called conversion loss.

Table3.2 tabulates the performance of the double-balanced mixer with current injection.

Table 3.2: Performance of double-balanced mixer with current boost.

IF Frequency	2 MHz
Supply Voltage	1.8 V
Power Dissipation	13.6 mW
Voltage Gain	4 dB
Power Gain/Loss	-15 dB
Noise Figure	17 dB
P1dB	-10.8 dBm
IIP3	4.97 dBm

3.3 Quaraure Mixer

3.3.1 Introduction

When a down-conversion occurs, the two input signals are mixed with the LO signal to the same IF frequency. One is the desired RF signal f_{RF}, the other is the frequency lower IF frequency than LO signal, called image frequency, as shown in Fig.3.13.

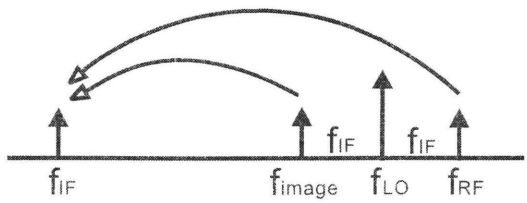

Figure 3.13: Definition of image frequency.

Suppose $f_{IF} = f_{RF} - f_{LO}$, if there is another signal $f_{image} = f_{LO} - f_{IF}$, it also mixes with the LO signal and produces the same IF frequency. The wanted and image signals are

all converted and appear at the IF port. The IF filter will not distinguish these two signals.

A common way to avoid this image problem is the use of a quadrature down-conversion mixer. There are two LO frequency signals, an in-phase (I) LO signal and a quadrature (Q) LO signal that are 90° apart. The input signals are given by $V_{RF} = A\cos(\omega_{RF}t)$, $V_{image} = A\cos((\omega_{LO} - \omega_{IF})t)$, and $V_{LO,I} = B\cos(\omega_{LO}t)$, $V_{LO,Q} = B\cos(\omega_{LO}t + 90°)$.

The RF signal multiplies the in-phase LO signal $V_{LO,I}$ to produce the desired IF signal. The image signal is mixed with the quadrature LO signal $V_{LO,Q}$ and is depicted in 3.2.

$$\begin{aligned} V_{image}V_{LO,Q} &= A\cos((\omega_{LO} - \omega_{IF})t)B\cos(\omega_{LO}t + 90°) \\ &= \frac{AB}{2}\cos((2\omega_{LO} - \omega_{IF})t + 90°) + \frac{AB}{2}\cos(-\omega_{IF}t - 90°), \end{aligned} \tag{3.2}$$

Due to down-conversion, the second term is chosen. Therefore two converted signals, the positive IF signal ω_{IF} and the negative frequency signal $-\omega_{IF}$, appear at the input of the IF filter. If the IF filter is a complex bandpass filter, the negative frequency can be detected and rejected.

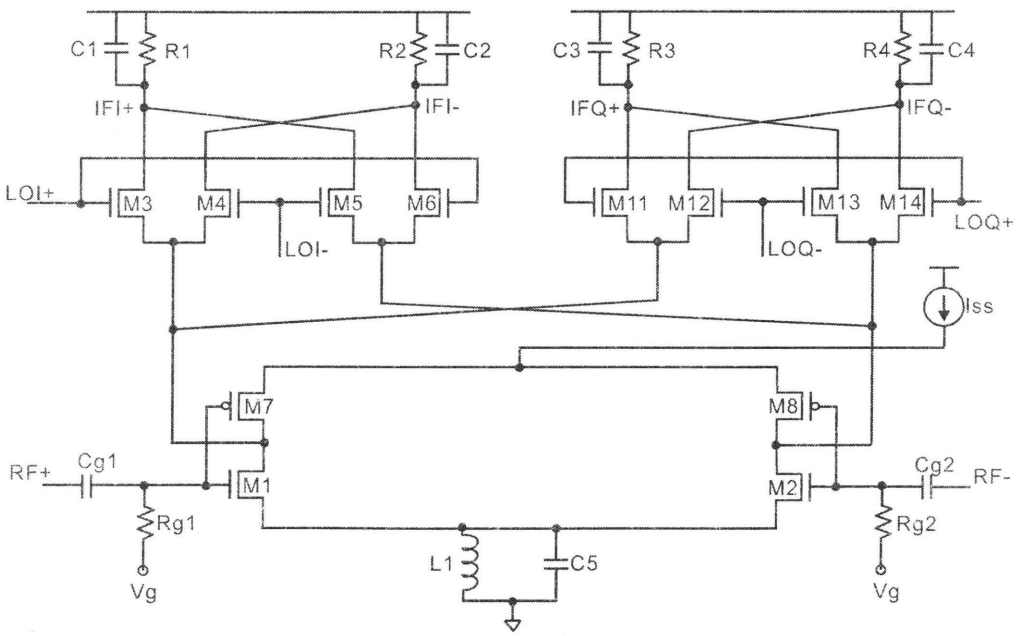

Figure 3.14: Quadrature mixer.

3.3.2 Configuration of Quadrature Mixer

Most of the quadrature mixers are constructed by two Gilbert mixers with the same RF inputs and quadrature LO signals [22, 23]. In this project, two double-balanced mixers with current boost are employed to construct a quadrature mixer, as shown in Fig.3.14. The in-phase mixer is symmetric with the quadrature mixer.

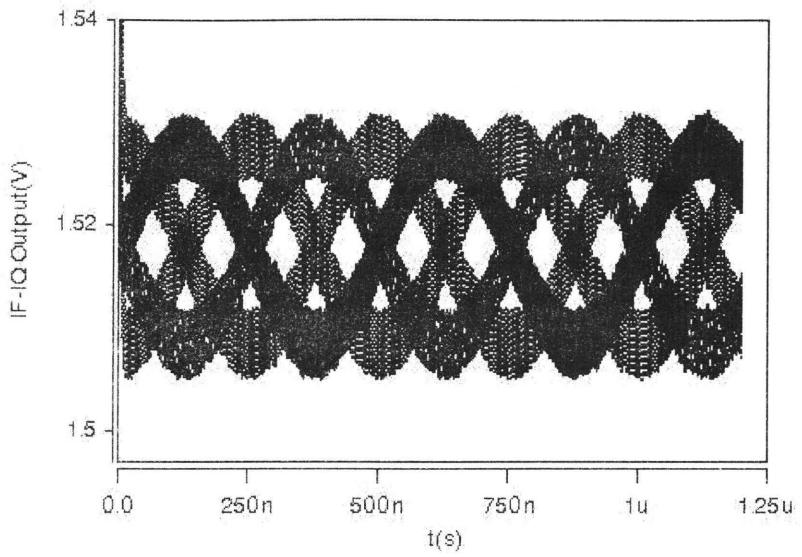

Figure 3.15: Output of quadrature mixer: IFI+, IFI-, IFQ+, IFQ-.

Fig.3.15 and Fig.3.16 show the quadrature outputs of quadrature mixer. The I and Q differential outputs exhibit the expected phase shift and the amplitude of IF output IFI and IFQ are slightly lower than the Gilbert cell, since the current of the switches flowing into the drain of the transconductors is twice that of Gilbert cell. The transconductance g_m increases and the drain voltage of M_1 decreases such that the overdrive voltage of switches M_3 and M_4 increases. Therefore the currents passing through the switches at DC increase. Fig.3.17 shows the drain current of M_3 and M_4 of quadrature mixer.

When both of the switches conduct, the current is 0.8 mA (0.26 mA in Gilbert mixer), and the conducting interval is longer than that of the single mixer. The noise figure of quadrature mixer is 21 dB, a slightly higher than that of Gilbert mixer, as shown in Fig.3.18.

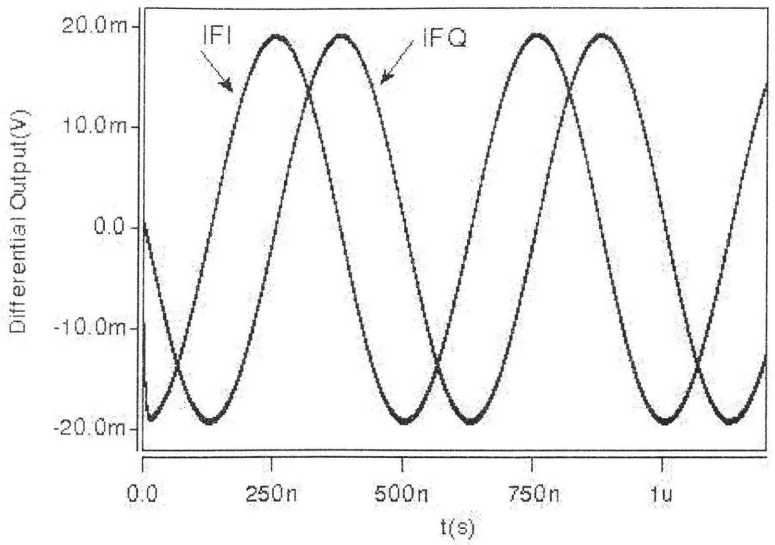

Figure 3.16: The differential output of quadrature mixer: in-phase IFI and quadrature IFQ.

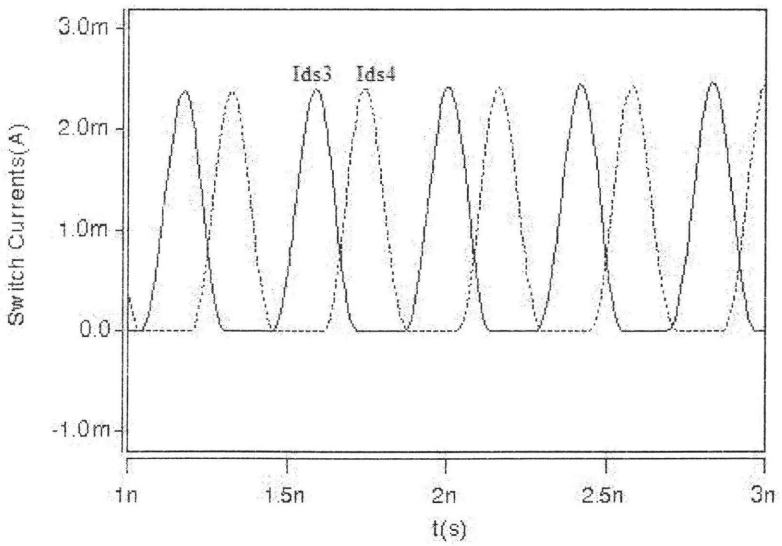

Figure 3.17: The switch currents of quadrature mixer.

In order to enhance the performance of quadrature mixer, the component parameters should be slightly adjusted, such as the amplitude of LO signal and its common mode voltage, the transistor sizes of M_1 and M_2. The overall performance of quadrature mixer is almost the same as the Gilbert mixer [22]. This project will not investigate this relative content.

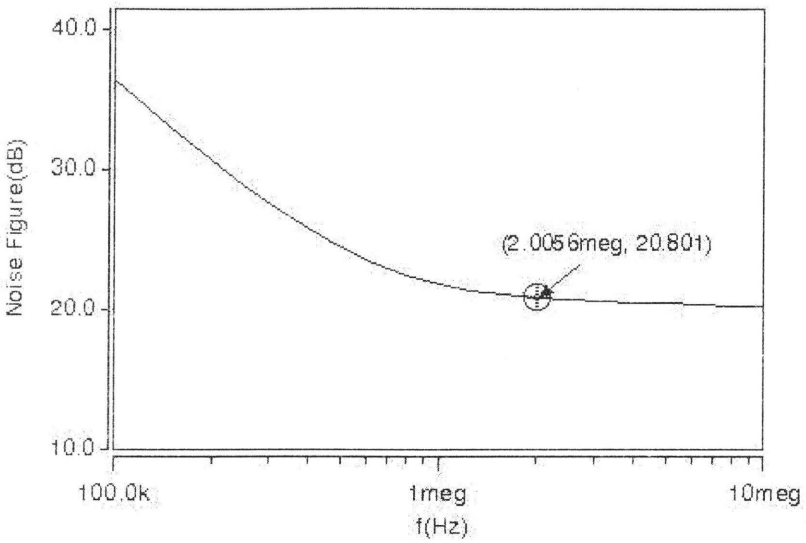

Figure 3.18: Noise figure of quadrature mixer.

3.4 Summary

A double-balanced mixer with current injection has been investigated. The amplitude and common mode voltage of the LO signal as well as the biasing voltage of transconductors, were chosen carefully to make the switches work properly while minimizing the 1/f noise. The additional circuit of injected current source may contribute to noise figure. And the input resistors of the transconductors are one of the main noise contributors. Due to the drain current of transconductors is 2 mA, the voltage conversion gain is only 4 dB. Therefore, increasing the drain current of transconductor may improve the gain and linearity. A quadrature mixer constructed by two double-balanced mixers has been illustrated. And its

performance were simulated and analyzed. The quadrature mixer yields the 90 degree phase shifts. The noise figure and the gain of quadrature mixer degrade under the same parameters of components and the same simulation conditions as the double-balanced mixer. To obtain the same performance in quadrature mixer, the parameter of transconductor, the common mode voltage and the amplitude of the LO signal must be adjusted.

Chapter 4

Power Amplifier

Power amplifier (PA) is an important block in transmitters. It amplifies the power of the modulated signal and send it to the antenna. Meanwhile, the power amplifier contributes the most in terms of the power consumption of the transceiver. The efficiency of power delivering becomes one of the crucial parameters in design of power amplifiers. Section4.1 reviews the classifications of power amplifier and the calculation of power added efficiency and drain efficiency. A configuration of common-gate Class E power amplifier is investigated in Section4.2, L matching network and its parameter calcultions are discussed in detail. All simulation results are presented in Section4.3. Section4.4 summarizes this chapter.

4.1 Classifications of Power Amplifier

There are four types of power amplifiers, distinguished primarily by bias conditions [2]. In Class A power amplifiers, where transistor operates linearly and conducts the whole duty cycle. In Class B power amplifiers, the transistor is biased to conduct 50% duty cycle to reduce power consumption. The transistor in a Class AB power amplifier turns on during 50% $\sim$ 100% duty cycle, and its performance is between Class A and Class B power amplifiers. In a Class C power amplifier, the conducting time of the transistor is less than 50% duty cycle.

Another three types of power amplifiers, Class D, E and F, use the transistor as a switch. Power consumption is ideally zero due to the different conducting duty cycle between the

drain voltage and drain current, as depicted in Fig.4.1.

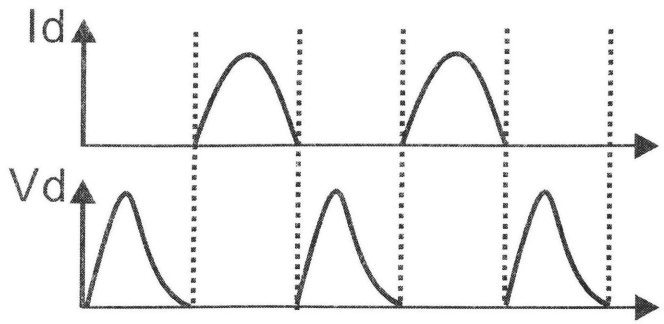

Figure 4.1: Drain voltage and current of a switching mode power amplifier.

In a Class D power amplifier, transformers are used in the input and output to force two transistors conducting half cycle respectively [2], and a series RLC network is used at the output of the amplifier. Class E power amplifiers are the same as Class D except for the transformers. A Class F power amplifier has a parallel LC tank at the output, which resonates at the carrier frequency.

Class C, D. E and F amplifiers are essentially constant envelope amplifiers [2], They do not normally provide an output that is proportional to the input and tend to perform best for constant-amplitude output. Since GFSK is adopted for bluetooth transceivers, which use constant envelope modulators, more research interests are recently focused on Class E power amplifiers for Bluetooth applications [26, 27, 28, 29, 30].

As shown in Fig.4.2, M_1 acts as a switch. When the switch turns on, the voltage across the switch should be zero. The voltage across the switch remains low when the switch turns off, as shown in Fig.4.1. Hence Class E power amplifier has no power consumption of the switch, and theoretically achieves 100% efficiency. However its linearity is poor and the the size of transistor is large.

Inductor L_d acts as a finite dc-feed inductance that resonates out the drain parasitic capacitance of switch, represented by C_o. Serial LC tank L_1 and C_1 constructs a band pass filter resonating at the carrier frequency and attenuates other harmonic signals.

The following terms are often used to evaluate the performances of power amplifiers.

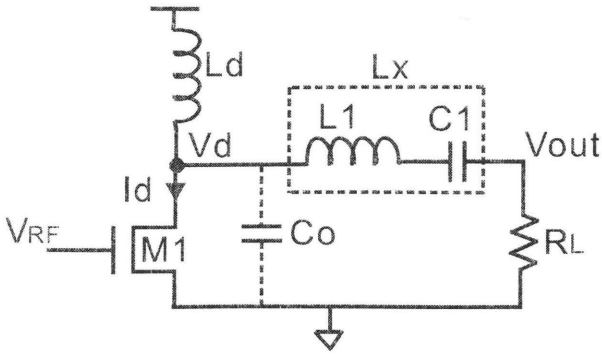

Figure 4.2: Class E power amplifier.

1. Power Added Efficiency (PAE)

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}}, \tag{4.1}$$

where

$$P_{DC} = I_{DC} V_{dd}. \tag{4.2}$$

2. Drain Efficiency (DE)

$$DE = \frac{P_{RFout}}{P_{DC}}. \tag{4.3}$$

3. Overall Power Efficiency

$$\eta = \frac{P_{RFout}}{P_{DC} - P_{RFin}}. \tag{4.4}$$

4.2 Common-Gate Class E Power Amplifier

In this project, a class 1 power amplifier is designed, its maximal output power is 20 dBm. In [28, 29], common-gate class E power amplifiers were proposed. The common gate transistor M_2 is connected in cascode with the common-source transistor M_1, as shown in Fig.4.1. The cascode structure avoids the loading effect to the input stage and increases the

isolation between the input and output of the power amplifier. The capacitance of M_1 is resonated out by the inductor L_g. R_{opt} is the optimum load, at which the power amplifier presents the desired output power with the highest efficiency.

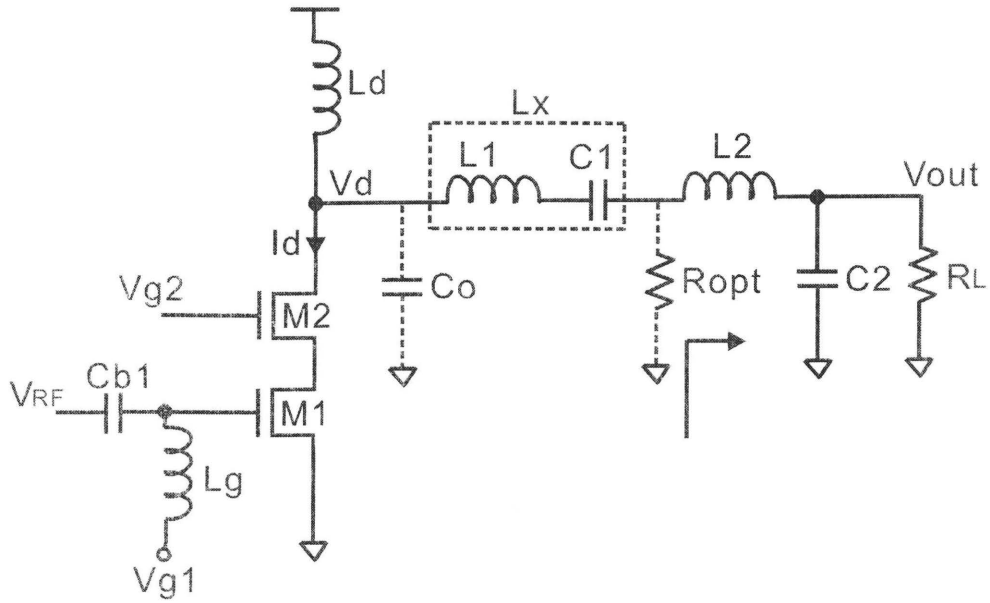

Figure 4.3: Common-gate class E power amplifier.

The dc-feed inductor L_d is calculated by the resonation frequency:

$$L_d = \frac{1}{\omega^2 C_o}. \tag{4.5}$$

The value of other components is calculated from [32].

$$L_x = \frac{\pi V_{dd}^2(\pi^2 - 4)}{2\omega P_{out}(\pi^2 + 4)}, \tag{4.6}$$

$$C_o = \frac{P_{out}}{\pi\omega V_{dd}^2}, \tag{4.7}$$

$$R_{opt} = 0.577\frac{V_{dd}^2}{P_{out}}. \tag{4.8}$$

If the supply voltage is 1.8 V and the output power is 20 dBm, R_{opt} should be 18.7 Ω. Obviously it is impossible for the power amplifier to deliver 20 dBm when directly connected

to a 50 Ω antenna. A commonly used method is add a L matching network at the output of the power amplifier to reduce the effective loading, such as L_2C_2 and R_L in Fig.4.1. The parallel L matching network can be transformed into serial connection between the capacitor and the optimum resistor in Fig.4.4.

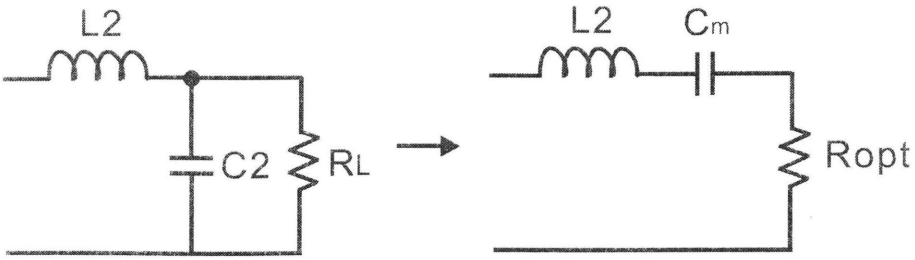

Figure 4.4: L matching network.

When inductor L_2 and capacitor C_m resonates at the carrier frequency, the input impedance of the L matching network is R_{opt}.

$$R_{opt} = \frac{R_L}{\omega_o^2 C_2^2 R_L^2 + 1}. \tag{4.9}$$

Therefore, $R_{opt} < R_L$. If the transformation ratio is

$$M = \frac{R_L}{R_{opt}}, \tag{4.10}$$

the shunt capacitance and series inductance can be computed from (4.11) and (4.12).

Shunt capacitance C_2

$$C_2 = \frac{\sqrt{M-1}}{\omega_o R_L}. \tag{4.11}$$

The series inductance L_2

$$L_2 = \frac{R_{opt}\sqrt{M-1}}{\omega_o}. \tag{4.12}$$

Table.4.1 tabulates the value of the components of the common-gate class E power amplifier. The length of M_1 and M_2 is $0.18\mu m$.

Table 4.1: Circuit parameters of common-gate class E power amplifier.

Components	Value
M1,M2	4 mm
Lg	5.2 nH
Ld	1.5 nH
L1	2.2 nH
L2	1.5 nH
C_{b1}	30 pF
C1	2 pF
C2	2 pF

4.3 Simulation Results

The class E power amplifier should operate in switch mode, the drain voltage V_d and current I_d must satisfy Fig.4.1. The supply voltage V_{dd} is 1.4 V, and the amplitude of RF input signal is 1.1 V.

Adjust the component values of L_d, L_1, L_2 and the size of transistors to ensure that the drain voltage is low when the switch turns on, as shown in Fig.4.5.

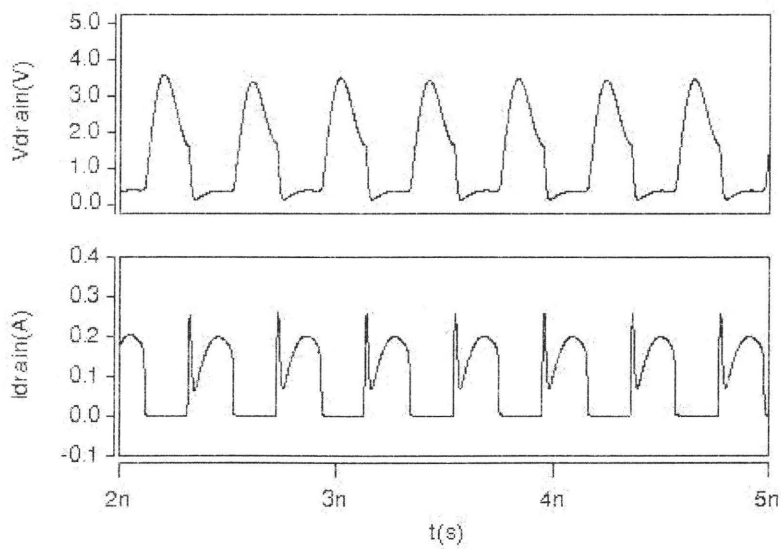

Figure 4.5: Drain voltage and current of common-gate class E power amplifier.

Due to the L matching network, the output voltage and output power are increased, as shown in Fig.4.6. However it does not mean that the power added efficiency(PAE) and drain efficiency(DE) must be high, since the input DC power changes along with the transformed resistance. Hence there are the trade-offs between the down scaled resistor and the power efficiency.

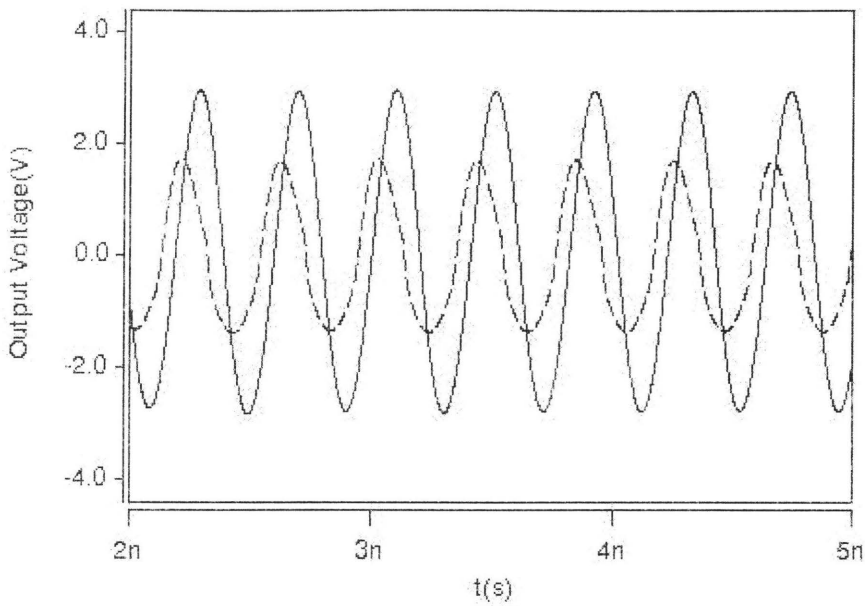

Figure 4.6: Output voltage of common-gate class E power amplifier. The dotted line: without L matching network. The solid line: with load transformation.

The output power and power gain are shown in Fig.4.7. The output power exceeds 17.7 dBm when the input power level is higher than 4 dBm. After that, the increase rate of the output power decreases along with the increase of the input power. That is why the power gain dropped afterward. The 1 dB compression point of the power amplifier, shown in Fig.4.8, is measured at the input power level 4 dBm. The linearity of the Class E power amplifier is poor.

The power added efficiency and drain efficiency are plotted in Fig.4.9. The DE is 42.8% and PAE is 41%.

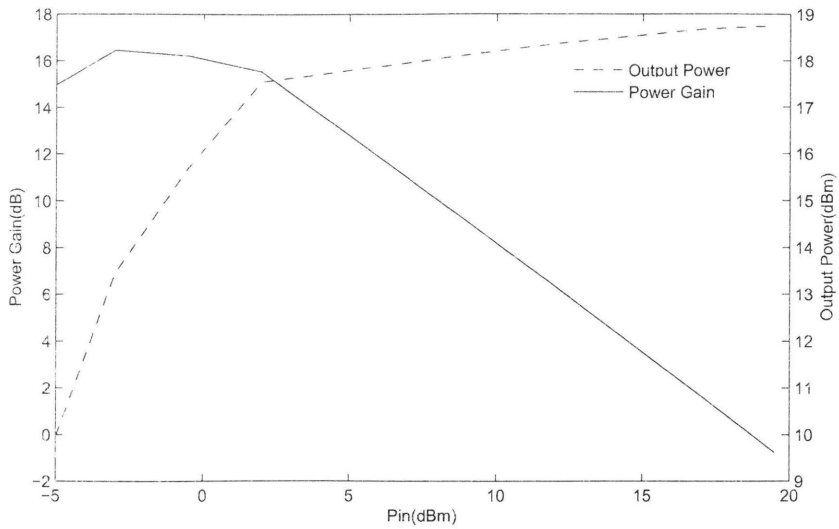

Figure 4.7: Output power and power gain of common-gate class E power amplifier.

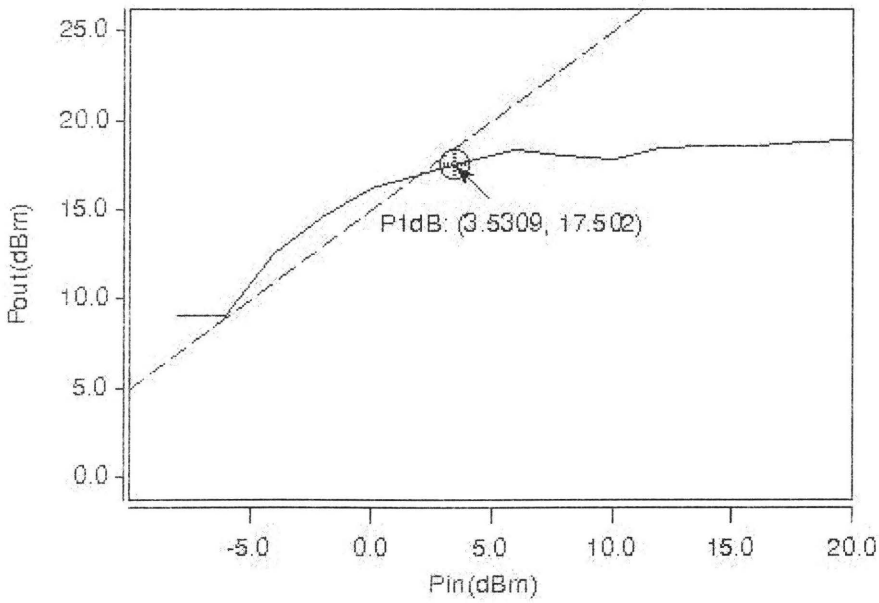

Figure 4.8: 1 dB compression point of common-gate class E power amplifier.

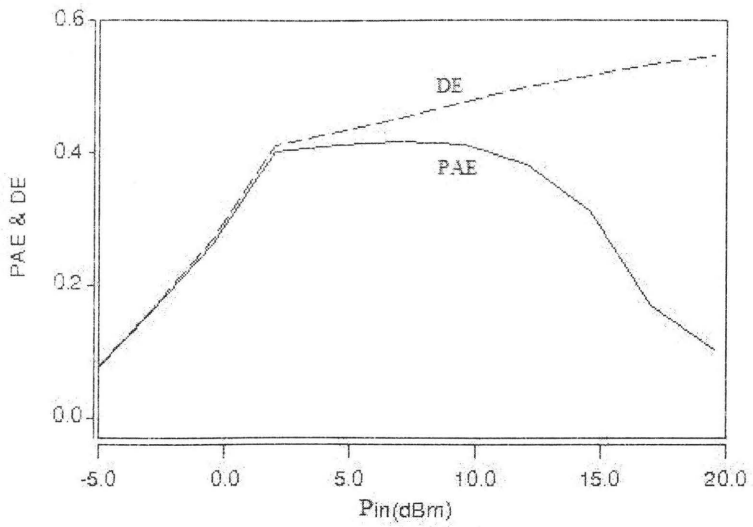

Figure 4.9: Power added efficiency and drain efficiency.

The performance of common-gate class E power amplifier is summarized in Table 4.2.

Table 4.2: Performance of common-gate class E power amplifier.

Frequency	2.45 GHz
Supply Voltage	1.4 V
Output Power	17.7 dBm
Gain	13.6 dB
P1dB	3.53 dBm
PAE	41%
DE	42.8%

4.4 Summary

A class 1 common-gate Class E power amplifier has been designed. Through connecting a L matching network at the output of PA, the optimum load resistance was reduced and the output power was increased. The common-gate transistor increases the isolation between ports. The power added efficiency PAE and drain efficiency DE were obtained over 40%. The drawbacks of Class E power amplifier are the large size of the transistors and its poor linearity.

Chapter 5

Quadrature VCOs

Design of quadrature VCOs is presented in this chapter. Section5.1 introduces the frequency synthesizer. In Section5.2, a complementary cross-coupled QVCO is investigated , and the MOS varactors and the definition of phase noise are illustrated. Steady-state behavior and phase noise of QVCOs are simulated in Section5.3. This chapter is summarized in Section5.4.

5.1 Introduction of Frequency Synthesizer

Bluetooth transceivers employ a frequency hopping spread spectrum scheme. Carrier frequency varies over a relatively large range, 2.40 GHz $\sim$ 2.480 GHz, with a pseudorandom sequence. A fixed frequency oscillator can not meet this specification. The most widely used frequency synthesizers (FS), which can generate one or more frequencies from one or several frequency references, are based on the principle of phase-locked loops (PLLs), as shown in Fig.5.1.

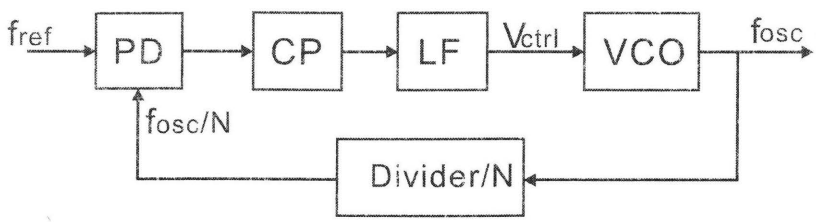

Figure 5.1: PLL-based frequency synthesizer.

Phase detector (PD), compares the phase difference between the reference frequency and the feedback frequency from the voltage controlled oscillator (VCO). When the feedback frequency is lower than the reference, PD outputs an UP signal, otherwise, a DOWN signal is asserted. The charge pump (CP) converts the UP or DOWN signal from the PD into a voltage by charging or discharging the capacitor of the downstream loop filter (LF). The loop filter generates the DC voltage V_{ctrl} that controls the frequency of VCO. The difference between a PLL and a FS is that the PLL directly feedbacks the oscillating frequency f_{osc}, but the feedback frequency of the FS is scaled down by a divider in the feedback path with a division ratio N (integer or fraction).

5.2 Quadrature VCOs

5.2.1 Architectures of Quadrature VCOs

As discussed in chapter 3, the down-conversion mixer employs the quadrature architecture. Therefore, a VCO is required to output two local oscillator signals, in-phase and quadrature. This section deals with the design of quadrature VCOs.

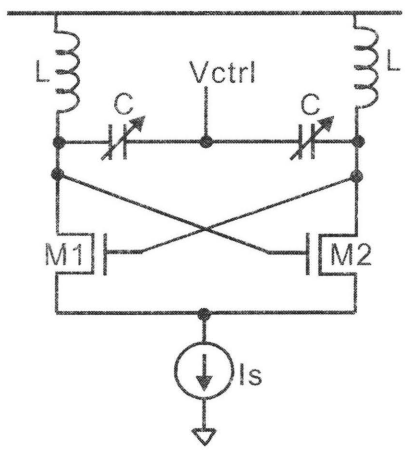

Figure 5.2: Differential LC-tank VCO.

Most of the widely used VCOs are based on LC tank VCOs with negative G_m network, as depicted in Fig.5.2 [36]. Cross-coupled transistors M_1 and M_2 constructs a negative resistance

network, C are varactors whose capacitance is controlled by the voltage V_{ctrl}. Inductors L, combined with two varactors, form LC tanks that resonate at the desired frequency.

$$f_{osc} = \frac{1}{\sqrt{LC}}. \tag{5.1}$$

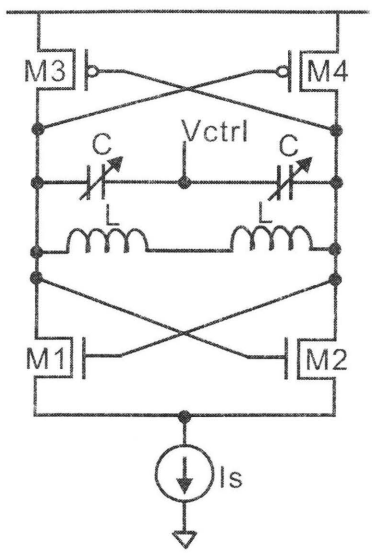

Figure 5.3: Complementary cross-coupled VCO.

Another configuration of VCOs is use two cross-coupled networks, called complementary cross-coupled VCOs, as shown in Fig.5.3. With the addition of the PMOS pair M_3 and M_4, it is possible to compensate the loss of the LC tank with less current consumption. However it is not suitable to use in low power circuits since the PMOS cross-coupled pair reduces the voltage headroom.

Quadrature VCOs consist of two symmetric differential cross-coupled VCOs. To generate quadrature phases, the switches are added to steer the currents, as shown in Fig5.4 [37].

The series coupled QVCOs (S-QVCO) were used in [37, 38, 39]. The phase error of S-QVCO is weakly dependent of the coupling strength. This characteristics allow to achieve a good phase error and phase noise at the same time.

The QVCO designed in this project is shown in Fig5.5. The QVCO has the following advantages:

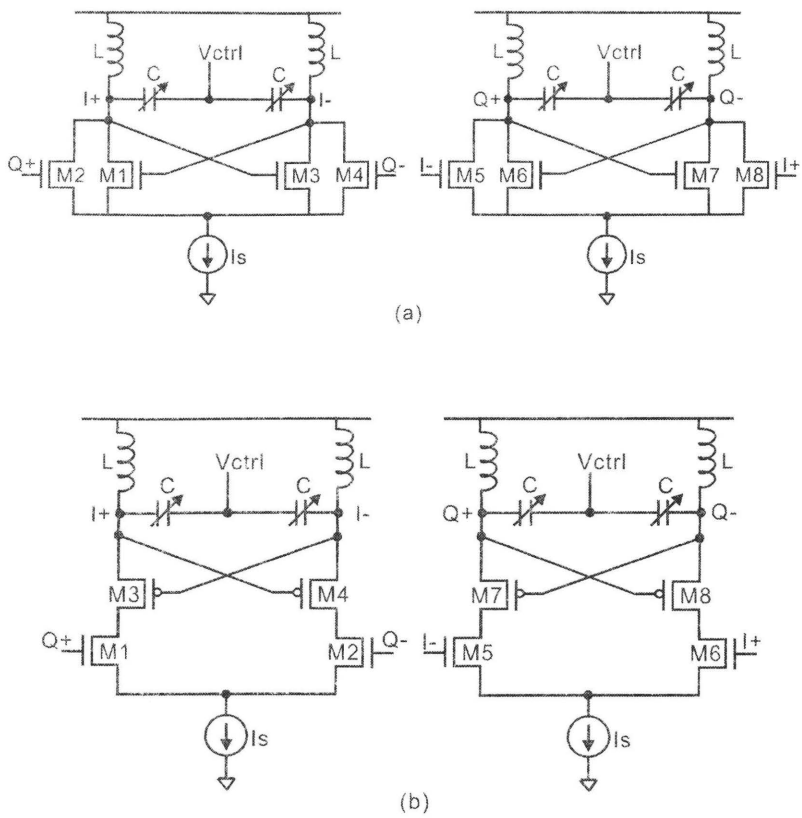

Figure 5.4: QVCOs: (a) Parallel coupled QVCOs. (b) Series coupled QVCOs

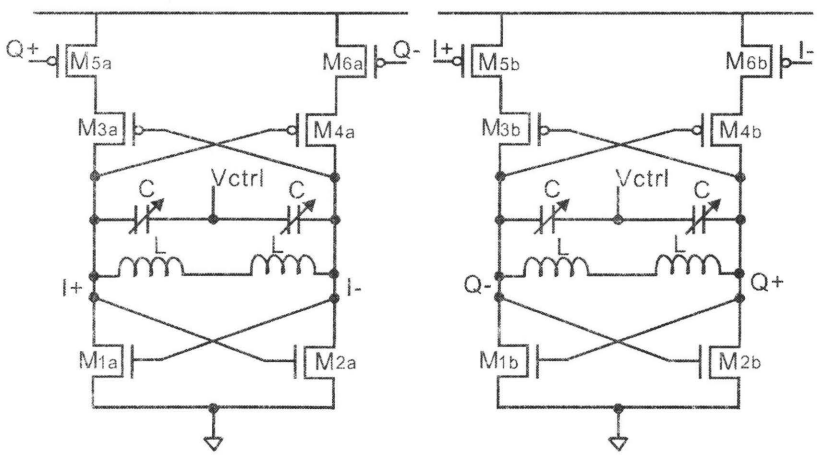

Figure 5.5: Complementary cross-coupled S-QVCO.

- Series coupling between switching transistors M_{5a}, M_{6a}, M_{5b}, M_{6b}, and cross-coupled transistors M_{3a}, M_{4a}, M_{3b}, M_{4b}.
- The switching transistors use PMOS to reduce the phase noise (low 1/f noise).
- Complementary PMOS cross-coupled pairs M_{3a}, M_{4a}, M_{3b}, M_{4b}. This complementary structure offers a large transconductance at a given current, which results in a faster switching.
- The eliminating of the tail current source increases the voltage headroom.

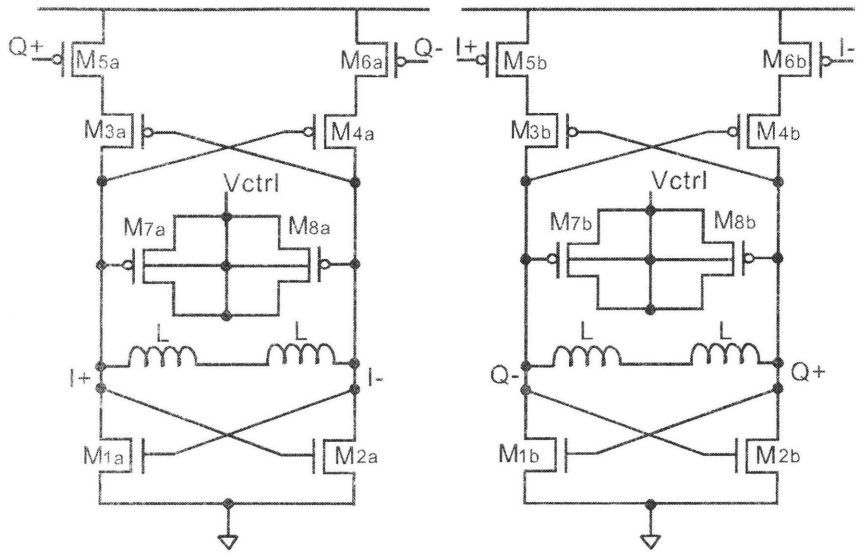

Figure 5.6: QVCO with A-mode MOS varactors.

5.2.2 MOS Varactors

In VCO design, MOS varactors are often used. MOS varactors operate in four regions, based on the biasing condition: accumulation, depletion, weak inversion, and strong inversion. Accumulation and strong inversion are two regions where most varactors are designed to operate in.

LC oscillators with accumulation-mode varactors exhibit lower power consumption and lower phase noise at large offset frequencies from the carrier, compared to those based on strong inversion varactors [43]. Therefore accumulation-mode (A-mode) PMOS varactors are used in QVCO, as shown in Fig.5.6.

5.2.3 Phase Noise

An ideal oscillator can be described as a pure sinusoidal wave

$$V(t) = V_o \sin(\omega_0 t). \tag{5.2}$$

For practical oscillators, the spectrum has power distributed around the center frequency as shown in Fig.5.7 [44]. In addition, the power is also distributed at the harmonics of the oscillation frequency. The instantaneous output of a practical oscillator can be expressed by

$$V(t) = V_o[1 + A(t)] \sin(\omega_0 t + \phi(t)), \tag{5.3}$$

where $A(t)$ and $\phi(t)$ represent amplitude and phase fluctuations of the signal, respectively. There are two types of phase terms appearing at the output spectrum of an oscillator. The first is referred to as a spurious tone due to $A(t)$. The second appears as random phase fluctuations, and is referred to as phase noise. Phase noise of an oscillator is mainly due to the internal noise sources.

Phase noise is typically quantified by the single-sideband (SSB) phase noise power, which is defined as the ratio of the noise power in a 1 Hz bandwidth at a frequency offset f_m from the oscillation frequency to the signal power. Single sideband phase noise is specified in dBc/Hz at a given frequency offset f_m from the signal frequency.

$$L(f_m) = 10 \log \left[\frac{P_{Noise}(f_m)}{P_{Signal}} \right]. \tag{5.4}$$

The parameters of the QVCO are tabulated in Table.5.1. Except the length of PMOS varactors M_{7a}, M_{8a}, M_{7b}, M_{8b}, is 0.5 μm, the length of the other transistors is minimized as

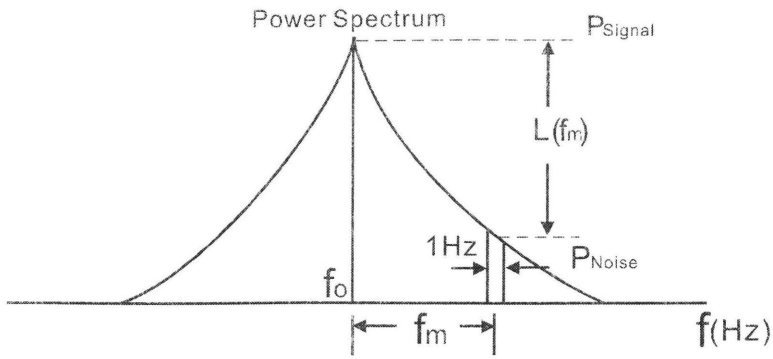

Figure 5.7: Definition of phase noise.

0.18 μm.

Table 5.1: Parameters of series coupled QVCO.

Components	Value
M1a,M2a, M1b, M2b	225 μm
M3a,M4a, M3b, M4b	150 μm
M5a,M6a, M5b, M6b	150 μm
M7a,M8a, M7b, M8b	1900 μm
L	21 nH

5.3 Simulation Results

The transient responses of the QVCO are plotted in Fig.5.8. The frequency of the four output signals are centered at 2.45 GHz when the control voltage V_{ctrl} is 0.32 V.

The relationship between control voltage V_{ctrl} and the oscillating frequency of QVCO is shown in Fig.5.9. V_{ctrl} ranging from 0$\sim$ 0.7 V achieves the frequency changing range 2.304 GHz $\sim$ 2.54 GHz. The tuning range of QVCO is around 10%.

The phase noise of QVCO is plotted in Fig.5.10. Two phase noises are measured. The first phase noise is -113 dBc/Hz at 600 kHz offset frequency, and the second one is -119 dBc/Hz at 1 MHz offset frequency. The phase noise of QVCO shown in Fig.5.6 is relatively

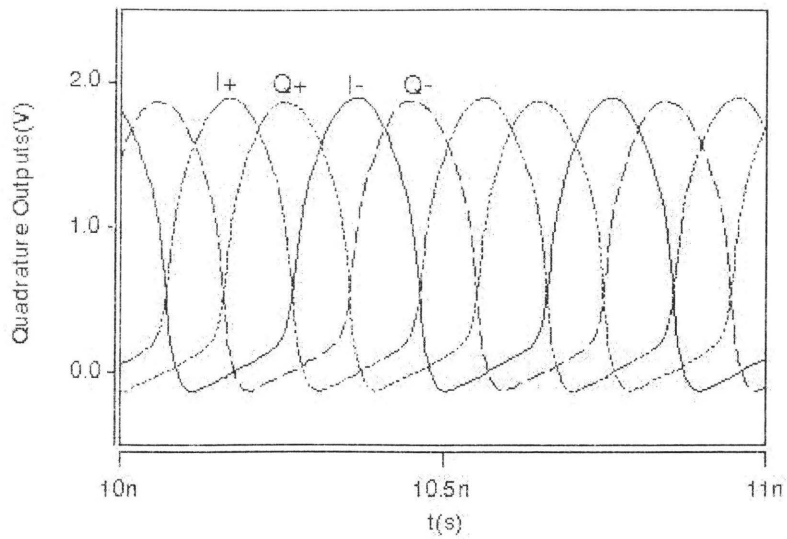

Figure 5.8: Outputs of QVCO.

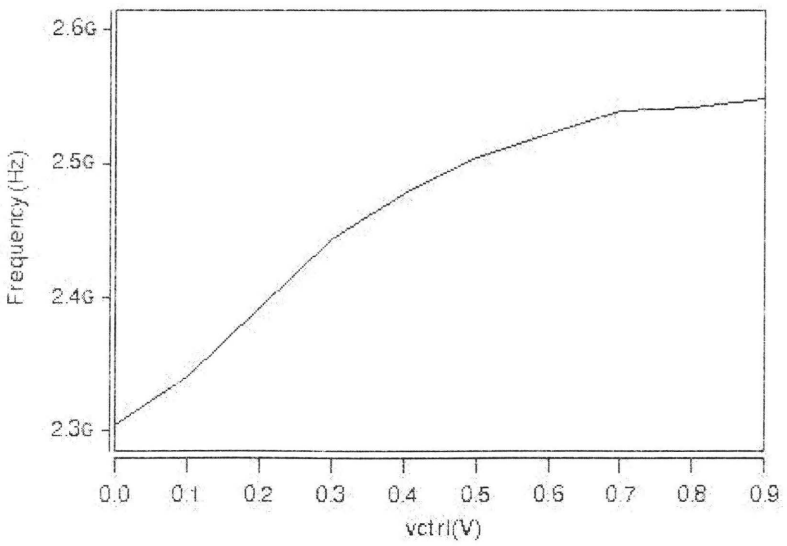

Figure 5.9: Frequency tuning range of QVCO.

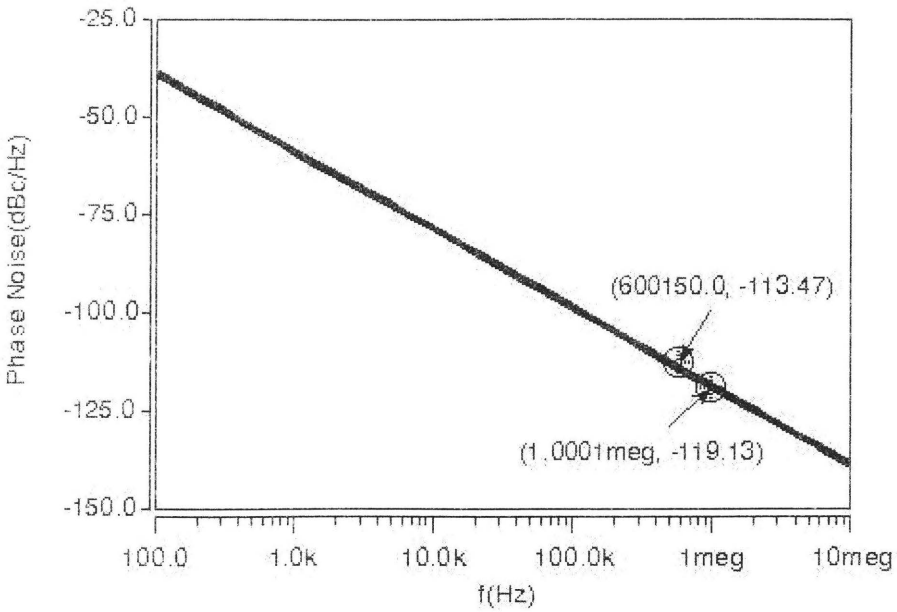

Figure 5.10: Phase noise of QVCO.

low.

The performance of the series coupled QVCO with A-mode MOS varactors is summarized in Table5.2.

Table 5.2: Performance of QVCO.

Center Frequency	2.45 GHz
Supply Voltage	1.8 V
Power Dissipation	7.2 mW
Tuning Range	2.304 GHz~2.54 GHz (10%)
Gain/Sensitivity	337 MHz/V
Phase Noise	-113 dBc/Hz(@600 kHz) -119 dBc/Hz(@1 MHz)

5.4 Summary

A complementary series cross-coupled QVCOs has been designed. The elimination of the current source tail allows the utilization of complementary configuration in low power

system. Due to the adoption of PMOS transistors in switching pairs, complementary cross-coupled pairs and MOS varactors, the low phase noises were achieved. The frequency tuning range of the QVCOs covers the frequency band of frequency hopping channels in Bluetooth transceivers. The amplitude of the oscillating signal reaches to 1.0 V, which satisfies the requirement of down-conversion mixer.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This project dealt with the design of RF transceiver front-ends for Bluetooth applications, including LNA, mixer, power amplifier and quadrature VCO.

A cascode LNA with relatively perfect impedance match of input and output port has been presented. The noise figure of the circuit is almost the same as the minimum noise figure. The cascode transistor improved the port isolation. The linearity of the LNA is good when the input power is as low as -70 dBm.

An active double-balanced down-conversion mixer has been designed, since double balance can suppress the common mode noise at input and output port. To reduce the fliker noise of switching transistors, a current source constructed by a current mirror was injected to the drain nodes of transconductors. The simulation results showed that 70% the drain current of transconductor is drew away by current bleeding. The total noise figure and the power consumption are decreased respectively. A 2 MHz differential IF signal was obtained at IF port. A quadrature mixer based on two symmetric double-balanced mixers has been investigated. The voltage gain and noise figure are slightly degraded compared to the Gilbert mixer with the same component parameters.

Common-gate Class E power amplifier has been designed. The scheme utilized a L matching network to reduce the optimum output load such that the output power was increased with the same power supply. This is suitable for the low power system. However

that doesn't mean that the lower the optimum output load, the better the performance of the power amplifier, since the PAE and DE depend on not only the output power, but the input power at DC. The compromise between output power, PAE and DE has been explored.

Finally PMOS complementary series coupling QVCO has been presented. Complementary structure increases the negative resistance with fewer current consumption and enhances the oscillation of LC tank. The A-mode PMOS varactors were chosen in LC tank, since they exhibit low power consumption and high linearity at large offset frequency. The designed and simulated QVCO achieved low phase noise at 600 kHz and 1 MHz offset frequency comparable to the configurations in the referenced literatures.

6.2 Future Work

In this project, get through the design process of RF transceiver. The main parts of the front-ends were finished. However there are still more work to do in the future.

- The input matching inductor in LNA is big, 40 nH. It is difficult to fabricate it with the other designed blocks on one chip. A better input matching network needs to be explored.
- This project excludes the up-conversion mixer. The frequency synthesizer is not designed except for the QVCO. If these two blocks are added to the project in the future, RF transceiver front-ends would keep integrity.
- Analyzing the LNA, mixer and QVCO as a system would be more valuable, since the loading effects between ports will be considered, although it is time consuming.

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