CASCADED H-BRIDGE MULTILEVEL INVERTER BASED STATCOM WITH A NOVEL DC-VOLTAGE DETECTION TECHNIQUE

by

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ABSTRACT

This thesis is dedicated to a comprehensive study of static synchronous compensator (STATCOM) utilizing cascaded H-bridge (CHB) multilevel inverter. Two challenging problems exist in the CHB-based STATCOM. Firstly, unbalanced voltages across dc capacitors of H-bridge units would occur because a large number of capacitors are utilized in the CHB inverter for high-voltage operation. The dc capacitor-voltage unbalance may result in uneven voltage stress on switches and the distortion of inverter output voltage due to the degradation of total harmonic distortion (THD). Secondly, all dc-voltages should be measured and controlled separately to perform dc capacitor-voltage balance control. In doing so, a large number of voltage sensors are required, which increases the cost and complexity of the STATCOM system. Therefore, the main objectives of this thesis are to develop new techniques for the balance of dc capacitor voltages and reduction of the number of voltage sensors used in the CHB-based STATCOM system.

A novel dc-voltage detection technique, referred to as single multiple-voltage (SMV) detector, is developed to obtain dc voltages of all H-bridges. The proposed SMV algorithm

can substantially reduce the number of voltage sensors. Only three voltage sensors are needed to obtain all dc capacitor voltages from the measured inverter output voltage. As a result, the CHB-based STATCOM with SMV detector reduces the cost and complexity of the system. The system reliability is enhanced as well. Furthermore, this technique can be extended to the STATCOM with high-level CHB inverter and suitable to high-voltage high-power applications.

A new dc-voltage balance control method is proposed to assure balanced voltages across all capacitors in the CHB inverter. This method combines the phase shifting technique and sinusoidal pulse modulation strategy for the dc-voltage control. PI regulators in all control loops can be identical due to the modular structure of CHB topology and phase-shifted PWM strategy. This feature makes the dc capacitor-voltage balance easy to be implemented.

To verify the performance of the CHB-based STATCOM and the effectiveness of the proposed methods, both computer simulations and experiments are performed. The proposed STATCOM shows superior performance in steady-state operation and can rapidly respond to the reactive power demand as well. All individual dc-voltages can be detected accurately from the SMV detector without direct dc-voltage measurement. With the detected dc-voltages, all capacitor dc-voltages can be well balanced based on the proposed dc-voltage balance control method.

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CHAPTER 1

INTRODUCTION

1.1 Overview

Over the past decades, the demands of electric power have been heavily increasing and the overall security and reliability of the electrical transmission network has become a world concern. In order to supply increased loads, improve reliability, and deliver energy at the lowest possible cost and with improved power quality, it has been widely recognized within the electric power industry that Flexible AC Transmission System (FACTS) is a superior solution from the technical, economic and environmental points of view [1].

The FACTS is a power electric based system and other static equipment that provide control of one or more ac transmission system parameters to enhance controllability and increase power transfer capability [2]. The advancements of FACTS are based on the power electronics technology to rapidly respond to dynamic system events, increase power transfer limits, and improve the quality of power delivered. In general, FACTS controllers can be divided into three categories [3, 4]:

1. Static Synchronous Compensator (STATCOM) — is a shunt-connected reactive power compensation device that is capable of generating or absorbing reactive power and the output voltage of the STATCOM can be varied to control the specific parameters of an electric power system.

2. Static Synchronous Series Compensator (SSSC) — is a static synchronous generator operated as a series compensator whose output voltage is quadrate with the line current for the purpose of increasing or decreasing the overall reactive voltage drop across the line and thereby controlling the transmitted electric power.
3. Unified Power Flow Controller (UPFC) — is a combination of STATCOM and SSSC, which is coupled via a common dc link, and is controlled to provide concurrent active and reactive power compensation.

An example of FACTS controllers controlling the power transmission capacity is shown in Figure 1-1, where a single line power system includes two ac systems 1 and 2. X_L is the impedance (assumed purely inductive) of the transmission line. FACTS controllers are to be connected to the problematic ac system through the magnetic coupling. The STATCOM or the SSSC can be shunt-connected or series-connected to the transmission line of the power system. The UPFC can be shunt- and series- connected to the power system. The power transmitted through the transmission line is given by the expression:

$$P = \frac{V_1 V_2}{X_L} \sin(\delta_1 - \delta_2) \tag{1.1}$$

where V_1 and V_2 are amplitudes, and δ_1 and δ_2 are angles of voltages of ac system 1 and 2, respectively. To control the power transmission capacity, the STATCOM controls transmission voltage through reactive power control, the SSSC controls the effective line impedance by directly controlling the voltage across the series impedance of the transmission line, and the UPFC controls, individually or in combination, all three transmission-parameters (voltage, impedance, and angle).

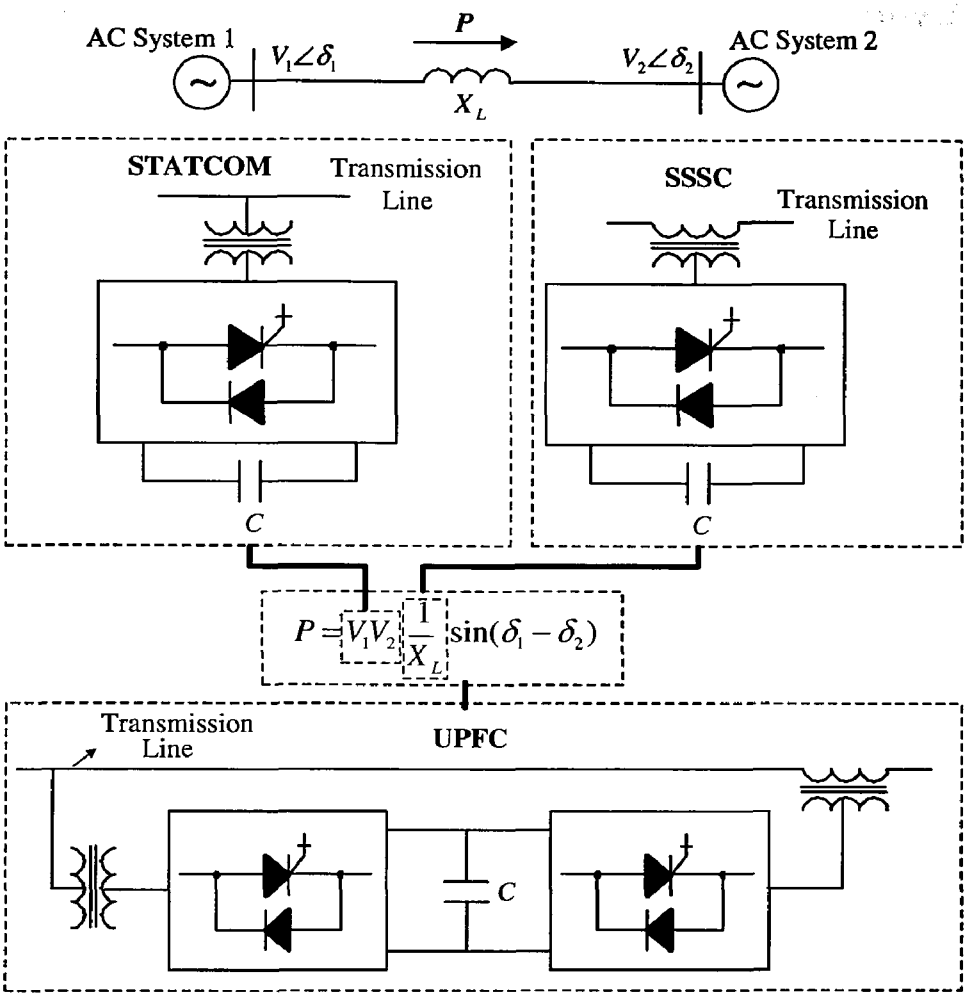


Figure 1-1. Basic family of converter-based FACTS controllers.

Among three FACTS controllers, the STATCOM has shown feasibility in term of cost effectiveness and easy shunt connection to the power system [5, 6]. The STATCOM can provide dynamic voltage support, system stabilization, increased system capacity, and enhanced power quality for transmission and distribution system applications. Using a high-speed power semiconductor switching technique, the STACOM can rapidly respond to dynamic system events. Instead of directly deriving reactive power from the energy-storage components, the STATCOM basically circulates power with connected network. The passive components used in the STATCOM, therefore, can be much smaller.

1.2 Static Synchronous Compensator (STATCOM)

The STATCOM is in general a solid-state switching inverter capable of generating or absorbing the reactive power at its output terminals without the need of large external reactor or capacitor banks. The concept of STATCOM was disclosed by Gyugyi in 1976 [2]. The first ± 100MVA STATCOM was installed at the Sullivan substation of Tennessee Vally Authority (TVA) in northeastern Tennessee in 1995. This unit is mainly used to regulate 161kV bus during the daily load cycle to reduce the operation of the tap changer of a 1.2GVA-161kV/500kV transformer. Recently, the STATCOM has been recognized as a promising FACTS controller because of its wide range of problem-solving abilities and cost effectiveness.

The single-line diagram of the STATCOM system is shown in Figure 1-2, where v_s is the voltage of the ac system which the STATCOM is connected to. v_c is the STATCOM output voltage. The STATCOM is connected to the ac system through the magnetic coupling, represented by L, which could be either an interface inductance or the leakage inductance of a coupling transformer. The key component of the STATCOM is the voltage source inverter (VSI) that uses either IGBTs or GCTs as switches. C is the energy-storage capacitor providing the dc voltage for the VSI. In principle, the output voltage of VSI is a staircase-type wave synthesized from the dc-side voltage with appropriate switching combinations of inverter switches. The inverter output voltage v_c is in phase with the system voltage v_s and the current i leads or lags v_s by 90^0 when the STATCOM provides the reactive power

compensation. The exchange of reactive power between the STATCOM and the ac system can be controlled by varying the amplitude of the inverter output voltage.

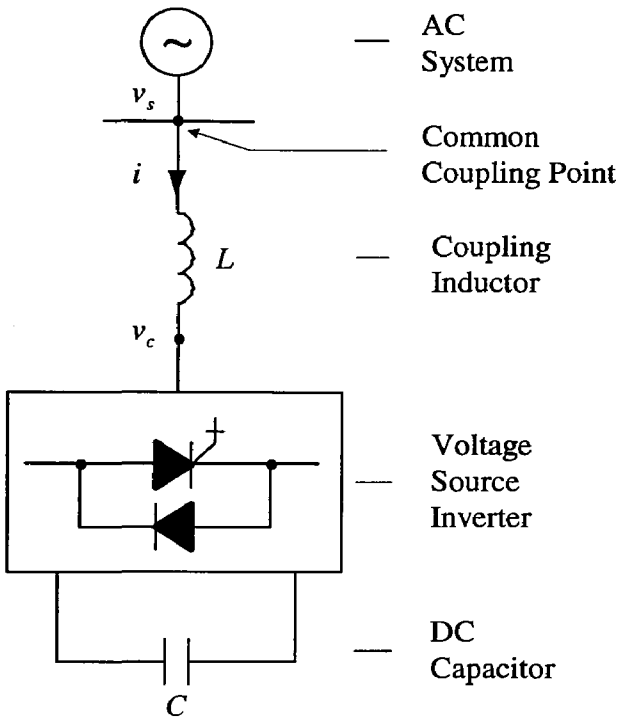
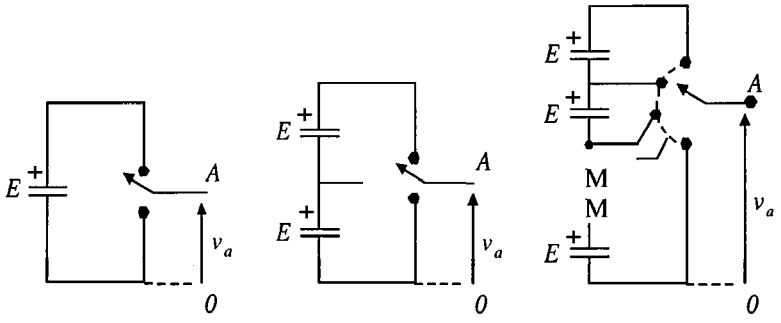


Figure 1-2. Single-line diagram of the STATCOM system.

Employing turn-off-capability semiconductor switches, switching power converters have been able to operate at high switching frequencies and to provide a faster response. This makes the voltage source inverter an important part in the STATCOM. The simplest voltage source inverter is the two-level inverter that has simple topology and modular structure. However, the two-level inverter produces high harmonic content in the inverter output voltage and high dv/dt due to fast switching. A series connection of switches is needed in high voltage applications and the problem of static/dynamic voltage sharing for series switches would occur. A new family of multilevel inverters has emerged as the solution for VSI working in high-power applications, particularly FACTS controllers [7, 8, 9].

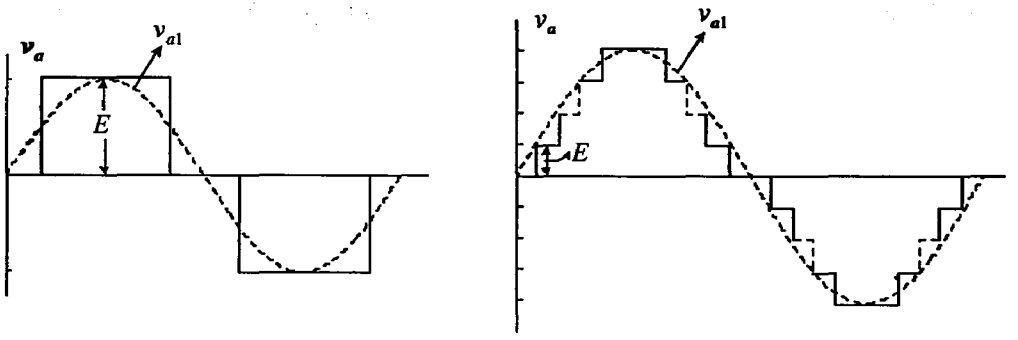
1.3 Multilevel Inverters of the STATCOM

In general, multilevel inverters include an array of switches and dc voltage sources, and can be viewed as voltage synthesizers. The output voltage of a multilevel inverter is synthesized from a number of dc voltage sources, which are typically implemented by using dc capacitors with a charge-balancing scheme maintaining the voltage constant. Figure 1-3 shows a schematic diagram of one-phase inverters with different voltage levels. The action of power switches is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two levels with respect to the point *o*, while the three-level inverter generates three voltages, and so on. Staircase-voltage waveforms of three-level and *m*-level inverters, as examples, are shown in Figure 1-4. It can be seen that by increasing the number of levels in the inverter, output voltages have more steps generating a staircase waveform with a reduced harmonic distortion.



(a) (b) (c)

Figure 1-3. One phase leg of an inverter with (a) two levels, (b) three levels, and (c) *m* levels.



(a) (b)

Figure 1-4. Staircase voltage waveforms of (a) three-level and (b) *m*-level inverter.

The attractive features of multilevel inverters are summarized as follows:

- Increasing the voltage capacity of switches without switches in series such that the static and dynamic voltage sharing problems are avoided;
- Generating output voltages with low distortion because of the low harmonic content in the inverter output voltage;
- Reducing EMI due to lower voltage steps.

In this section, three mature multilevel VSIs, diode-clamping multilevel inverter (DC) [10, 11, 12], flying-capacitor multilevel inverter (FC) [13, 14] and cascaded H-bridge multilevel inverter (CHB) [15, 16, 17], are generally discussed and compared. One of them is chosen to be the VSI of the studied STATCOM.

1.3.1 Diode-Clamped Multilevel Inverter (DC)

The diode-clamped multilevel topology, also known as neutral-point-clamped (NPC) topology, was introduced by Nabae, et al., in 1980 [10]. Figure 1-5 shows a five-level diode-clamped inverter, where the dc bus voltage is split into five levels by four series-connected dc-bus capacitors, C_1, C_2, C_3 and C_4. There are some clamping diodes in each phase, such

as $D_1 \& D_1^{'}$, $D_2 \& D_2^{'}$ and $D_3 \& D_3^{'}$ in phase A. The middle point of o is defined as the neutral point. The voltage E across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level of E through clamping diodes.

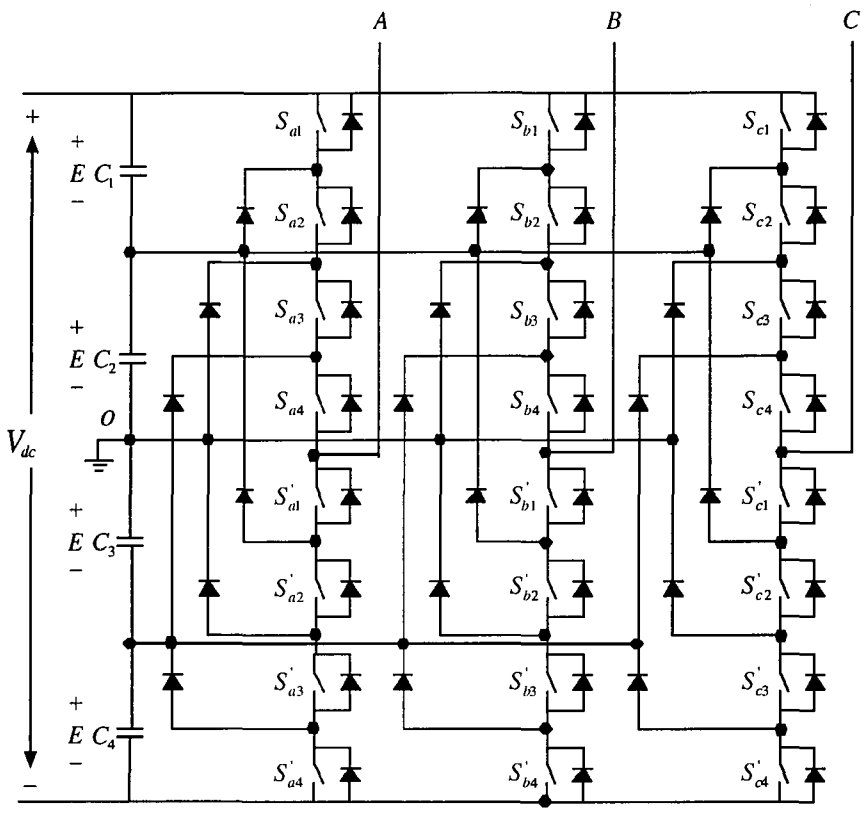


Figure 1-5. A three-phase, five-level diode-clamped inverter.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of switches will exclude the other from being turned on. The four complementary pairs, for example in phase A, are $(S_{a1}, S_{a1}^{'})$, $(S_{a2}, S_{a2}^{'})$, $(S_{a3}, S_{a3}^{'})$ and $(S_{a4}, S_{a4}^{'})$. To explain how the staircase voltage is synthesized, the neutral point o is considered as the output phase voltage reference point. The phase voltage, phase A for

example, is v_{Ao}. Five switch combinations to synthesize five level voltages across A and o are tabulated in Table 1-1.

Table 1-1 Voltage level and switching state of a five-level diode-clamped inverter

Output Voltage v_{Ao}	Switching State			
	S_{a1}	S_{a2}	S_{a3}	S_{a4}
$2E$	1	1	1	1
E	0	1	1	1
0	0	0	1	1
$-E$	0	0	0	1
$-2E$	0	0	0	0

Although each active switch has the same voltage rating of $V_{dc}/(m-1)$, where m is the number of voltage levels of the inverter, the clamping diodes must have different voltage ratings for reverse voltage blocking. Assuming that the blocking voltage rating of each diode is the same as the active switch voltage rating, the number of clamping diodes required for each phase will be $(m-1)\times(m-2)$. When m is high, the number of diodes required will make the system impractical to implement. In addition, maintaining the charge balance of capacitors is difficult for diode-clamped topologies with more than three voltage levels.

1.3.2 Flying Capacitor Multilevel Inverter (FC)

Figure 1-6 illustrates a five-level flying capacitor inverter. C_1, C_2, C_3 and C_4 are dc-bus capacitors that clamp the switch voltage to one capacitor voltage level, $E = V_{dc}/4$. C_{a1}, C_{a2} and C_{a3} in phase A, for example, are balancing capacitors. To generate an m-level staircase output voltage, m-1 capacitors in dc buses and (m-1)(m-2)/2 balancing capacitor are needed.

The complementary switch pairs in phase A are ($S_{a1}, S_{a1}^{'}$), ($S_{a2}, S_{a2}^{'}$), ($S_{a3}, S_{a3}^{'}$) and ($S_{a4}, S_{a4}^{'}$). The output voltage with respect to the neutral point o, v_{Ao}, and the switching states of a five-level flying capacitor inverter are summarized in Table 1-2.

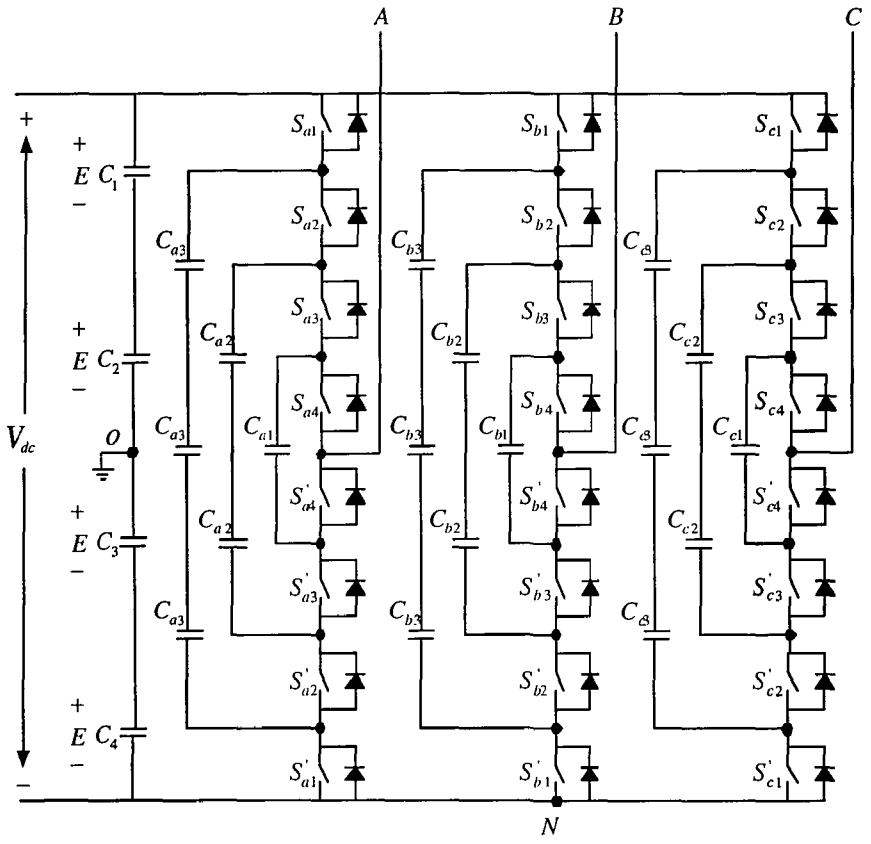


Figure 1-6. A three-phase, five-level flying capacitor inverter.

The FC topology provides more switching combination redundancies than a diode-clamped multilevel inverter. However, an excessive number of storage capacitors are required when the number of inverter levels is high. In addition, the capacitor dc-voltage control is complicated. With the required bulky capacitors, the system would be expensive and difficult to package.

Table 1-2 Voltage level and switching state of a five-level flying capacitor inverter

Output Voltage v_{Ao}	Switching State			
	S_{a1}	S_{a2}	S_{a3}	S_{a4}
$2E$	1	1	1	1
E	1	1	1	0
	0	1	1	1
	1	0	1	1
	1	1	0	1
0	1	1	0	0
	0	0	1	1
	1	0	0	1
	0	1	1	0
	1	0	1	0
	0	1	0	1
$-E$	1	0	0	0
	0	1	0	0
	0	0	1	0
	0	0	0	1
$-2E$	0	0	0	0

1.3.3 Cascaded H-Bridge Multilevel Inverter (CHB)

A relatively new inverter topology, cascaded H-bridge multilevel inverter (CHB) with separate dc source, was first introduced in 1990's and has been used for static var compensation application [17, 18, 19]. Figure 1-7 shows a configuration of wye-connected five-level cascaded inverter. The building block for the cascaded multilevel inverter is a single phase H-bridge unit, which consists of two legs with two active switches in each leg. The dc side of an H-bridge unit is a dc capacitor. Each H-bridge unit provides three voltage levels, $+V_{dc}$, 0, $-V_{dc}$. Output terminals of H-bridge units are connected in series. The output voltage is thus the summation of those H-bridge units. The CHB synthesizes a desired voltage from several dc capacitor voltages. The total number of output voltage levels per phase is defined by m=2n+1, where n is the number of H-bridge units per phase. The cascaded H-bridge inverter in Figure 1-7 can produce a phase voltage with five voltage levels. Various voltage

levels and their corresponding switching states are summarized in Table 1-3. Features of the CHB inverter are summarized in the next subsection.

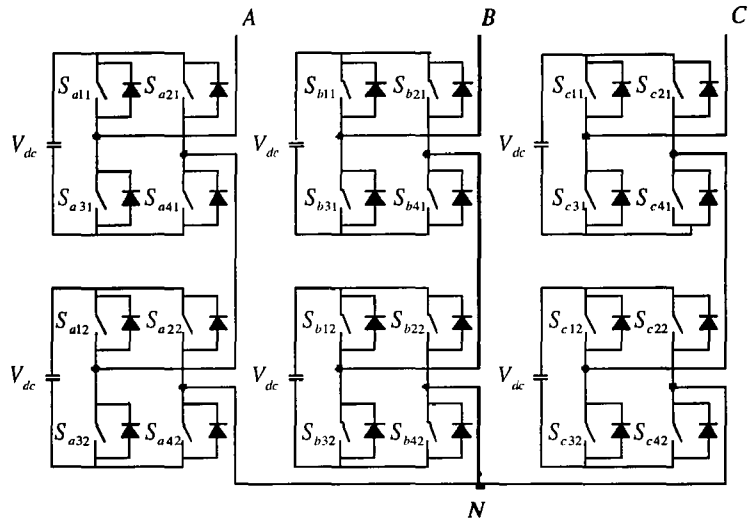


Figure 1-7. A three-phase wye-connceted five-level cascaded H-bridge inverter.

Table 1-3 Voltage level and switching state of a five-level cascaded inverter

Output Voltage v_{AN}	Switching State			
	S_{a11}	S_{a21}	S_{a12}	S_{a22}
$2E$	1	0	1	0
E	1	0	1	1
	1	0	0	0
	1	1	1	0
	0	0	1	0
0	0	0	0	0
	0	0	1	1
	1	1	0	0
	1	1	1	1
	1	0	0	1
	0	1	1	0
$-E$	0	1	1	1
	0	1	0	0
	1	1	0	1
	0	0	0	1
$-2E$	0	1	0	1

1.3.4 Comparison

Three multilevel VSIs, DC, FC and CHB, are compared in terms of the feasibility of their utilization in STATCOM applications. One consideration is the number of components used in each topology. Table 1-4 compares main power component requirements per phase leg among these three multilevel VSIs, where m is the number of voltage levels.

Table 1-4 Comparison of power component requirements per phase

Inverter Configuration	DC	FC	CHB
Main Switching Devices	$2(m-1)$	$2(m-1)$	$2(m-1)$
Main Diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping Diodes	$(m-1)(m-2)$	0	0
DC Bus Capacitors	$(m-1)$	$(m-1)$	$(m-1)/2$
Balancing Capacitors	0	$(m-1)(m-2)/2$	0
Total	m^2+2m-3	$(m^2+8m-8)/2$	$(9/2)(m-1)$

In the DC topology, a large number of clamping diodes are needed. For the more-than-three-level configuration, the voltage unbalance problem in DC topology cannot be overcome by utilizing control techniques only. Either oversized capacitors or complex balance circuits are required [11]. These make the DC topology unsuccessful in high-voltage reactive power compensation applications.

In the FC topology, an unacceptable amount of capacitors are required for high voltage levels. In the seven-level flying-capacitor inverter, for example, 15 balancing capacitors and six dc-bus capacitors are required per phase to achieve the same voltage rating yielded by

utilizing three capacitors in the CHB topology. A large number of capacitors not only make the system less cost-effective, but also introduce a severe voltage unbalance problem due to the complicated capacitor voltage control. These make the flying capacitor multilevel inverter less attractive for high-voltage STATCOM application.

Among three multilevel inverter topologies, the CHB inverter requires the least number of total main components to synthesize the same number of voltage levels because there are no extra clamping diodes or voltage-balancing capacitors in it. In addition, a cascaded inverter can reach a sufficiently high voltage level such that it can be directly connected to a medium-voltage power network, 13.8kV for example, without requiring step-up transformers. Modularised circuit layout and packaging is possible because each level has the same structure. Therefore, the CHB inverter is the promising topology for the STATCOM application and is adopted in this thesis.

1.4 Challenges of CHB-Based STATCOM

This thesis focuses on the CHB topology as the VSI module for realizing the high voltage and high MVA rating in STATCOM. Two challenging problems need to be solved in the CHB-based STATCOM system.

To be able to operate in a high-voltage application, a high level cascaded H-bridge inverter is needed and a number of dc capacitors are required. Voltages across these dc capacitors might be unbalanced due to such reasons as unequal component loss, unequal

inverter current and asymmetrical charging of the capacitor that may occur when capacitors are initially charged by ac system during starting up the STATCOM. Not only do unbalanced dc capacitor-voltages introduce uneven sharing of voltage stresses on semiconductor switches, but they also cause the distortion of the inverter output voltage due to the degradation of total harmonic distortion (THD) factor. Consequently, how to maintain and balance dc capacitor voltages with a simple and effective control method is a challenge for this thesis.

In order to control the individual dc-voltages of all H-bridge units, each dc capacitor-voltage should be measured by a voltage sensor and controlled separately. The greater number of voltage levels, the more voltage sensors are required. With a large number of voltage sensors, the system is less cost-effective and complex. The system reliability is potentially reduced as well. Therefore, another challenge is how to detect all individual dc capacitor-voltages with the least voltage sensors and make the STATCOM system cost-effective, compact and reliable.

1.5 Motivations

Motivations of the research are to provide the effective control needed for the practical realization of the CHB-based STATCOM and to solve two challenging problems mentioned in the previous section.

Main Motivations and Contributions

- Develop a novel dc capacitor-voltage detection technique for the CHB-based STATCOM to obtain all individual dc capacitor-voltages without the direct dc-voltage measurement such that the number of voltage sensors is reduced and the system is cost-effective and less complex.

- Develop a simple and effective dc capacitor-voltage balance control method to assure well-balanced voltages across all dc capacitors in the CHB inverter.

- Develop a simulation model of the medium-voltage CHB-based STATCOM system that can be used to facilitate the steady state and dynamic analysis of the CHB-based STATCOM and the proposed methods.

- Construct a low-power system prototype in the laboratory to experimentally verify the performance of the CHB-based STATCOM, the accuracy of the developed dc capacitor-voltage detection technique and the effectiveness of dc capacitor-voltage balance control.

1.6 Organization of Thesis

The contents of this thesis are divided into six chapters. A general review of FACTS controllers (specially STATCOM), comparison of three multilevel inverters, challenges in CHB-based STATCOM and motivations of the thesis are presented in the first chapter.

Chapter 2 begins with the system configuration of CHB-based STATCOM and the phase-shifted PWM switching strategy for the CHB inverter is then introduced. The operating principle of the CHB-based STATCOM is presented. The dynamic model in dq frame for the equivalent STATCOM circuit is derived. The decoupling power control scheme for power exchange between the STATCOM and the ac system is proposed, where active and reactive power can be controlled separately.

Chapter 3 presents main contributions of this thesis: dc capacitor-voltage detection technique and individual H-bridge dc-voltage balance control. The dc capacitor-voltage detection technique, single multiple-voltage (SMV) algorithm, is developed to detect individual H-bridge dc-voltages with least voltage sensors. The charging of dc capacitor and the control of dc-voltage are then presented. The balance control scheme of individual H-bridge dc-voltage is proposed to assure well-balanced voltages across all dc capacitors of the CHB inverter. The complete controller for CHB-based STATCOM system is presented in detail.

Chapter 4 presents the computer simulation and verification of the proposed STATCOM system. The simulation model of a medium-voltage seven-level CHB-based STATCOM in Matlab/Simulink environment is developed. Simulations of the proposed STATCOM on the following topics are performed: 1) steady state performance, 2) dynamic response to reactive power demand, and 3) response of dc capacitor-voltage balance control. Simulation results demonstrate that the STATCOM shows superior performance in steady state and can rapidly respond to the reactive power change. The proposed dc capacitor-voltage detection method

can detect individual H-bridge dc-voltages with the least voltage sensors and the dc capacitor-voltage balance control method can equalize individual capacitor voltages effectively.

Chapter 5 presents the experimental verification of the proposed CHB-based STATCOM. The prototype of a low-power five-level CHB-based STATCOM is built up based on the dSPACE prototyping system. The experimental set-up configuration (both hardware and software platform) is described in detail. Details of the dSPACE integrated hardware/software environment for the implementation of the proposed STATCOM are presented. Experimental results are provided to verify the steady-state performance, the accuracy of the SMV detector and the effectiveness of dc capacitor-voltage balance control.

Chapter 6 draws conclusions for this thesis and proposes future work.

CHAPTER 2
CASCADED H-BRIDGE INVERTER-BASED STATCOM

This Chapter presents the system configuration and operating principles of the cascaded H-bridge multilevel inverter (CHB) based STATCOM system. To control the active and reactive power separately, a dynamic model in the dq (two-phase synchronous) reference frame for the STATCOM equivalent circuit is derived. Based on this dq model, the decoupling power control method is proposed to control the power exchange between the ac system and the STATCOM. Phase-shifted pulse width modulation (PWM) strategy is employed in this thesis to provide gate signals for switches in the inverter.

2.1 System Configuration

In this section, the system configuration of a CHB-based STATCOM is presented. Details of the CHB inverter and phase-shifted PWM strategy are discussed. Reactive components, decoupling inductors and dc capacitors, and the STATCOM controller are introduced.

The STATCOM is a controlled reactive power source. It generates or absorbs the desired reactive power entirely by means of the action of electric switches in a voltage source inverter (VSI). The main circuit configuration of a CHB-based STATCOM system is shown in Figure 2-1. It consists of three main parts: 1) a VSI, using either IGBTs or GCTs as switches and a dc capacitor on the dc side as an energy-storage device; 2) a set of coupling inductors which

connect the STATCOM to the ac system; and 3) a controller that receives commands, measurements and feedback signals, executes control algorithms and generates gate signals for switches in the inverter. The functions of each block will be discussed in the following subsections.

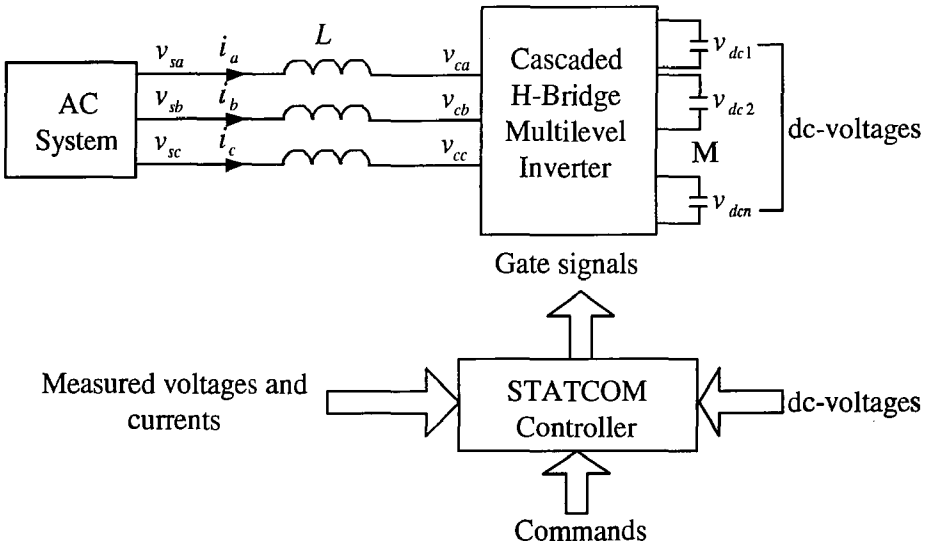


Figure 2-1. System configuration of a CHB-based STATCOM.

2.1.1 CHB Inverter and Modulation Strategy

The VSI of the STATCOM studied in this thesis is a cascaded H-bridge multilevel inverter (CHB). The diagram of a three-phase seven-level cascaded H-bridge inverter is shown in Figure 2-2. The building block of this topology is a single-phase H-bridge inverter, which includes two inverter legs with two active switches and two freewheeling diodes in each leg. The dc sides of H-bridges are dc storage capacitors. They may also be batteries or fuel cells in special applications. Each phase consists of three H-bridge units connected in series. The three-phase CHB is constructed to form a star connection.

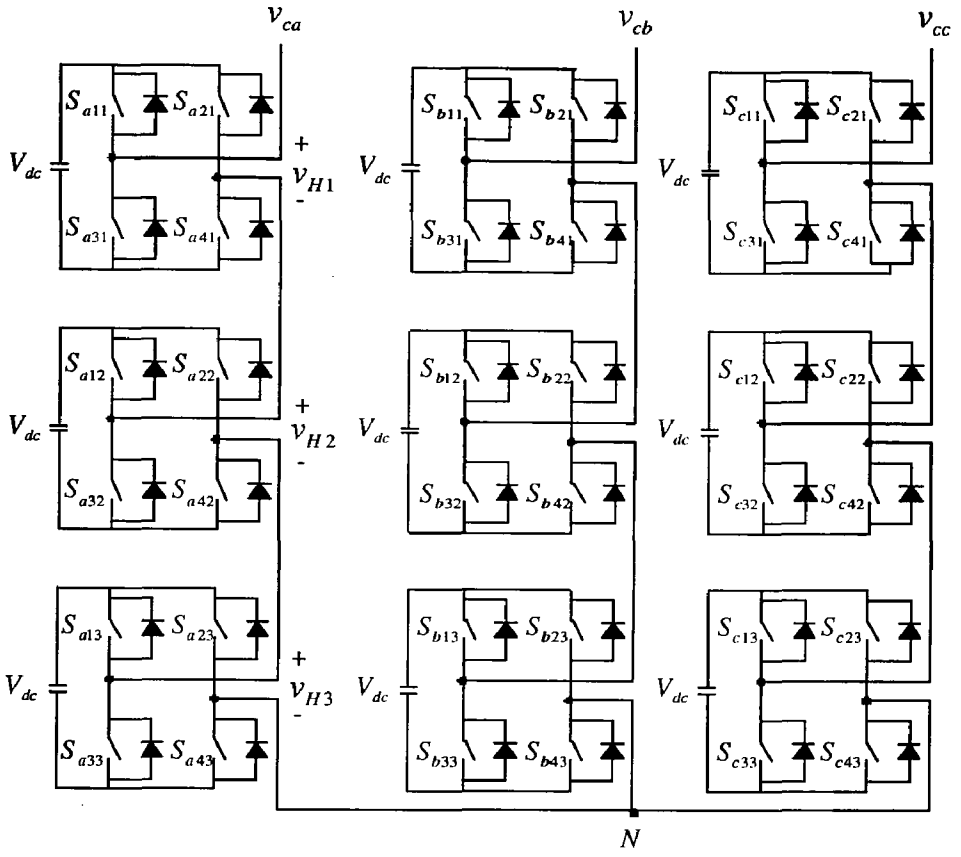


Figure 2-2. Diagram of a seven-level cascaded H-bridge inverter.

In each H-bridge unit, the upper and the lower switches in the same leg should operate in a complementary mode in case two switches in the same leg turning on or turning off simultaneously. With one switch being turned on, the other must be off, and vice versa. Therefore, switching states of an H-bridge unit can be determined only by states of the upper switches. According to the combination of switching states, the output voltage of an H-bridge has three possible levels, V_{dc} , 0, - V_{dc} . The CHB synthesizes a desired voltage from independent capacitor dc-voltages. The inverter phase voltage per phase is given by

$$v_c = v_{H1} + v_{H2} + v_{H3} \tag{2.1}$$

where v_{H1}, v_{H2} and v_{H3} are output voltages of H-bridge units H_1, H_2 and H_3, respectively. The total number of output voltage levels is defined by $m = 2n+1$, where n is the number of H-bridge units. In Figure 2-2, the 7-level cascaded inverter has three H-bridge units and the synthesized output voltage levels could be $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$.

The modulation methods used in multilevel inverters can be classified according to switching frequency, as shown in Figure 2-3 [22]. In methods working with low switching frequencies, switches generally perform one commutation during one cycle of the fundamental output voltage. The inverter output voltage is a stair-case waveform. The representative of this family is the selective harmonic elimination (SHE). In methods working with high switching frequencies, switches have many commutations in one cycle of the fundamental output voltage. Two popular methods of this family are the sinusoidal pulse width modulation (SPWM) and the space vector PWM (SVM).

In SPWM, a sinusoidal modulating wave with an adjustable amplitude and frequency is compared with a carrier (usually triangular) wave. The gate signals for switches are generated at the intersections of two waves. In this study, the phase-shifted PWM, a kind of SPWM, is used to be the modulation strategy for the switching modulator.

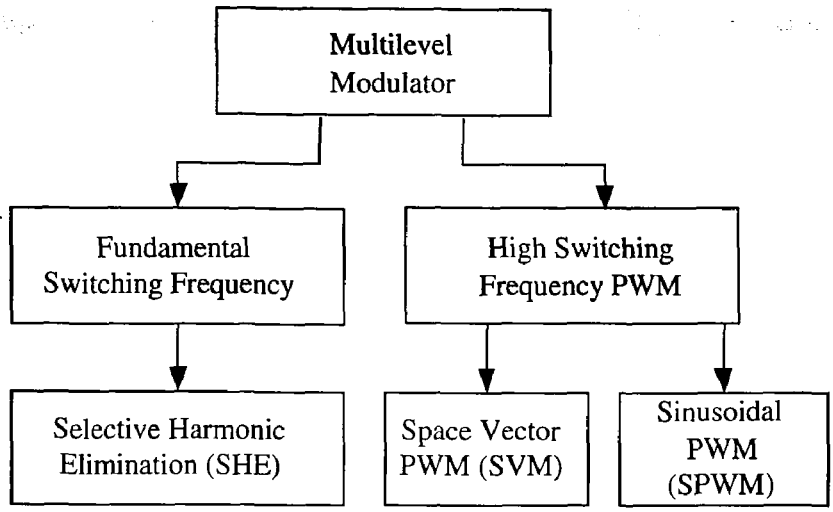


Figure 2-3. Multilevel modulation techniques.

In phase-shifted PWM, all triangular carrier waves have the same frequency and the same peak-to-peak amplitude, but there is a certain phase shift between any two adjacent carrier waves, given by

$$\Phi_{cr} = 360^0/(m-1) \tag{2.2}$$

where m is the inverter voltage level. Modulating waves are three-phase sinusoids with adjustable amplitude and frequency. Gate signals are generated at intersections of modulating wave and triangular carrier waves. Figure 2-4 shows the principle of the phase-shifted modulation of a seven-level cascaded inverter shown in Figure 2-2. Six triangular carrier waves are needed. The carriers v_{cr1}, v_{cr2} and v_{cr3} are used to generate gate signals, v_{g11}, v_{g12} and v_{g13}, for the upper switches S_{11}, S_{12} and S_{13} in left legs of H-bridge units H_1, H_2 and H_3. The other three carriers, v_{cr1-}, v_{cr2-} and v_{cr3-}, produce gate signals, v_{g31}, v_{g32} and v_{g33}, for the upper switches S_{31}, S_{32} and S_{33} in right legs of the H-bridge units. The lower switches operate in a complementary mode with respect to their corresponding upper switches. The

frequency modulation index in this example is $m_f = f_{cr} / f_m$=3 and the amplitude modulation index is $m_a = V_m / V_{cr}$=0.8, where f_{cr} and f_m are frequencies of the carrier and modulating waves, and V_{cr} and V_m are peak amplitudes of carrier and modulating waves, respectively. In phase-shifted PWM method, the amplitude and phase shift of the inverter output voltage are controlled by the modulating index m_a and phase angle, represented by α, of the modulating sinusoidal wave.

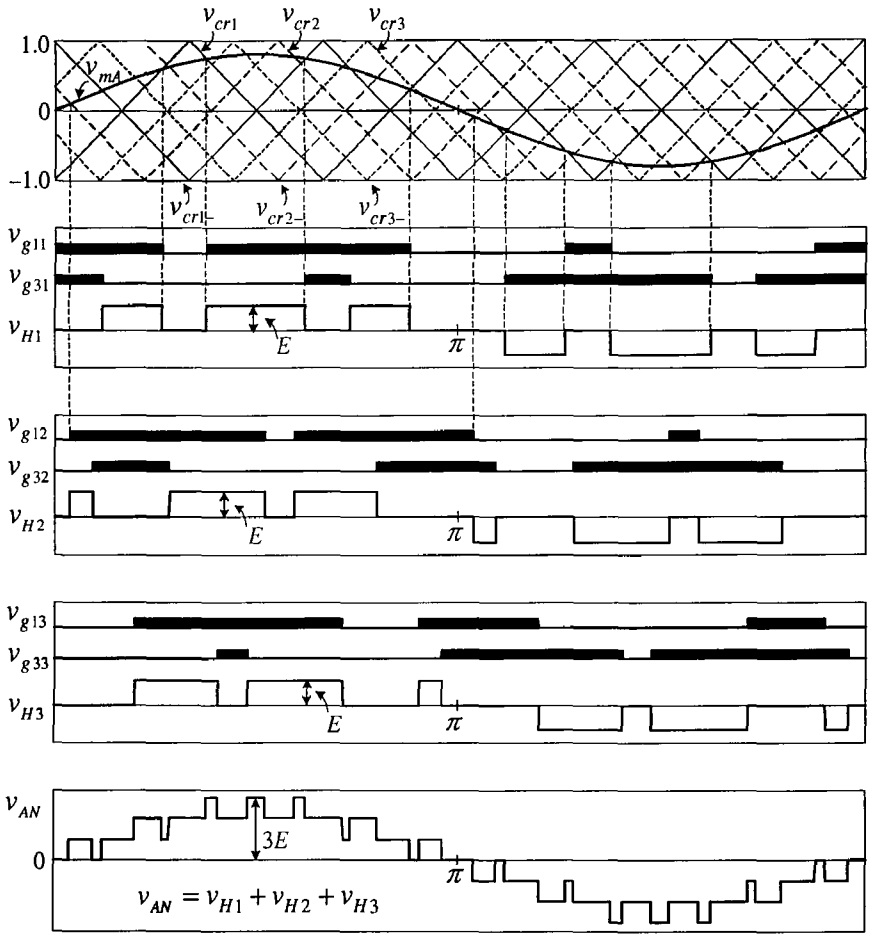


Figure 2-4. Phase shifted PWM scheme for a seven-level cascaded inverter (m_a=0.8, m_f=3) [23].

It is noted from Figure 2-4 that output voltages of H-bridge units in one phase, v_{H1}, v_{H2} and v_{H3}, have similar waveforms with a small phase displacement among them. Switching frequencies among switches are equal and stresses on all switches are balanced. No switching swap is needed. These features will make the dc-voltage balance control easy to be implemented.

2.1.2 Coupling Inductors and DC Capacitors

A set of small coupling inductors is used to connect the ac system and the STATCOM. No step-up transformer is required in the medium-voltage (4.6~13.8 kV) grid to boost the output voltage of multilevel inverter since the inverter output voltage can be enhanced with increased inverter voltage level. Another function of the coupling inductor is to filter out the line current harmonic components that are generated mainly by the pulsating output voltage of the inverter.

DC sides of the cascaded multilevel inverter are storage dc capacitors. DC voltage sources are derived from these dc capacitors charged by the rectified ac power. The primary function of the capacitor is to provide a circulating-current path as well as a voltage source.

2.1.3 STATCOM Controller

The controller of STATCOM is used to make the entire system work effectively and properly. Tasks of the STATCOM controller shown in Figure 2-5 includes:

- *Reactive Power Control* — generating or absorbing the desired reactive power to or from the ac system,

- *Total DC-Voltage Control* — controlling the active power exchanges to compensate power losses in the inverter such that the total phase dc-voltage can be regulated,
- *Individual DC-Voltage Control* — balancing all individual dc-voltages in H-bridges, and
- *Switching Modulator* — generating gate signals for switches in the inverter.

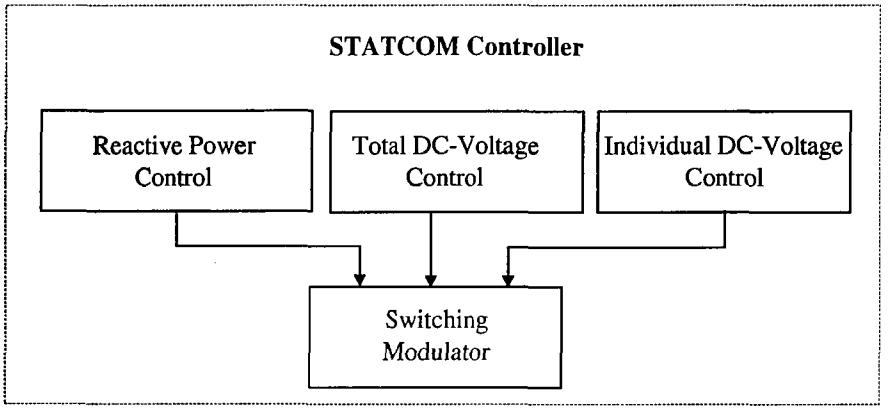


Figure 2-5. Tasks of the STATCOM controller.

In Figure 2-1, necessary voltages and currents are measured and then fed into the controller to be compared with commands. The controller then performs feed forward or feedback control and outputs a set of gate signals to drive switches of the inverter accordingly.

2.2 Operating Principles of CHB-Based STATCOM

The STATCOM provides the desired reactive power by exchanging the instantaneous reactive power among phases of the ac system. Meanwhile, a small amount of active power is needed to compensate the power loss of the inverter. Details of both active and reactive power exchanges between the STATCOM and ac system are presented in this section. Concepts of generating/absorbing the active power and leading/lagging reactive power are defined to provide references for the power control.

2.2.1 Active and Reactive Power

Expressions of active and reactive power in a STATCOM system can be derived from the equivalent circuit shown in Figure 2-6, where v_s is the phase voltage of the ac system, v_c is the generated phase voltage of the VSI and i is the line current drawn by the VSI. L is total ac inductance. Figure 2-7 is a phasor diagram of v_s and v_c, where δ is the phase difference between v_s and v_c.

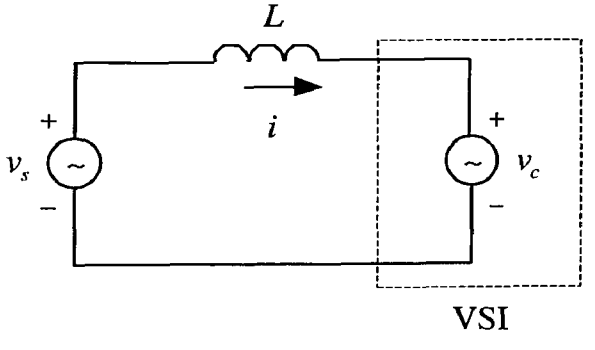


Figure 2-6. Equivalent circuit of the STATCOM.

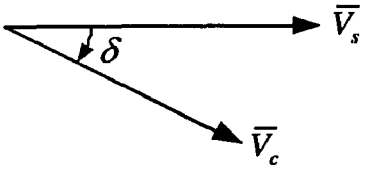


Figure 2-7. Phasor diagram of v_s and v_c

From the equivalent circuit, the current drawn by the inverter is

$$\bar{I} = \frac{\bar{V}_s - \bar{V}_c}{jX_L} = \frac{V_s \angle 0^0 - V_c \angle \delta^0}{jX_L}$$
$$= -\frac{V_c \sin\delta}{X_L} - j\left(\frac{V_s - V_c \cos\delta}{X_L}\right) \tag{2.3}$$

where V_s and V_c are rms values of the system voltage and inverter output voltage, and X_L is the equivalent impedance. The apparent power of the system is described by

$$S = \bar{V}_s \bar{I}^*$$
$$= V_s\left(-\frac{V_c \sin\delta}{X_L} + j\frac{V_S - V_c \cos\delta}{X_L}\right) \tag{2.4}$$
$$= -\frac{V_s V_c}{X_L}\sin\delta + j\frac{V_s - V_c \cos\delta}{X_L}V_s$$

From the terminal of the STATCOM, the active and reactive power are given by

$$P = \frac{V_s V_c}{X_L}\sin\delta \tag{2.5}$$

$$Q = V_s \frac{V_c \cos\delta - V_s}{X_L} \tag{2.6}$$

2.2.2 Power Exchanges between the AC System and the STATCOM

Reactive Power Exchange

The main function of a STATCOM is to generate or absorb the reactive power to or from the ac system. If the STATCOM system has no power loss and operates to supply only reactive power, no active power exchange between the STATCOM and the ac system.

Therefore, the inverter output voltage is controlled to be exactly in phase with the system voltage, i.e., $\delta = 0^0$, the reactive power becomes

$$Q = V_s \frac{V_c - V_s}{X_L} \tag{2.7}$$

From equation (2.7), the reactive power exchange between the STATCOM and the ac system can be controlled by varying the amplitude of the inverter output voltage. Figure 2-8 shows two phasor diagrams for reactive power control. In Figure 2-8 (a), the amplitude of the inverter output voltage is higher than that of the ac system voltage ($V_c > V_s$), the current flows through the inductor from the STATCOM to the ac system and leads the inverter voltage v_c by 90^0. The STATCOM generates leading reactive power for the ac system and operates in the capacitive mode ($+Q$). In Figure 2-8 (b), the amplitude of the inverter output voltage is lower than that of the ac system voltage ($V_c < V_s$), thus the reactive current flows from the ac system to the STATCOM and lags the inverter voltage v_c by 90^0. The STATCOM absorbs lagging reactive power from the ac system and operates in the inductive mode ($-Q$). If V_c is equal to V_s, the reactive power exchange is zero and the STACOM operates in the standby mode.

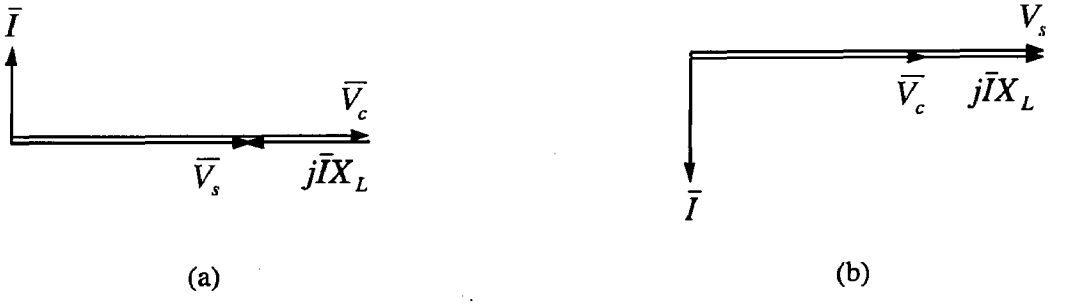


Figure 2-8. Phasor diagram for reactive power control, (a) Leading power factor, (b) Lagging power factor.

Active Power Exchange

For reactive power generation, the active power provided by the dc source as input to the inverter must be zero. Furthermore, the dc source provides no reactive power as input to the inverter and thus plays no part in the generation of reactive power by the inverter because the reactive power of zero frequency (dc) is zero. As a result, the average charge and discharge to the dc capacitor are equal [3]. In other words, dc-voltages are able to sustain in the ideal case of reactive power generation. However, switches of the inverter and passive components are not ideal and dissipative power losses exist. The energy stored in the capacitor is eventually used to compensate internal losses of the inverter. As a result, the voltage across the capacitor cannot be sustained and will eventually collapse. It is essential that the inverter itself keep the capacitor charged to the required voltage level when the STATCOM is used for reactive power generation. In order to regulate and maintain the capacitor voltage, a small amount of active power is needed to compensate component power losses.

From equation (2.5), the active power can be controlled by adjusting the phase difference δ (usually in small range) between v_s and v_c. The inverter can supply active power to the ac system if the inverter output voltage is made to lead the system voltage by a small angle ($\delta > 0$). On the other hand, it can absorb active power from the ac system if its voltage lags behind the system voltage by a small angle ($\delta < 0$). In this way, dc capacitor can be charged or discharged and the total dc-voltage can be maintained at the required level. The above analysis reveals two important laws for active and reactive power exchange in the STATCOM:

1. The amount of reactive power, Q, can be controlled by adjusting the amplitude of the inverter output voltage V_c;

2. The amount of active power, P, can be controlled by adjusting the phase difference δ of the inverter output voltage with respect to the system voltage.

The positive/negative sign of phase difference δ, active power P and reactive power Q are defined in Table2-1 to provide the reference for the power control. Power exchanges in the STATCOM system are summarized in Table 2-2, where there are four possible cases. The phasor diagrams of these cases are illustrated in four quadrants of PQ plans, as shown in Figure 2-9.

Table 2-1 Definition of signs of δ, P and Q

δ	>0	$\overline{V}_c$ lags $\overline{V}_s$
	<0	$\overline{V}_c$ leads $\overline{V}_s$
P	>0	The STATCOM absorbs the active power from the ac system
	<0	The STATCOM generates the active power to the ac system
Q	>0	The STATCOM provides the leading reactive power to the ac system
	<0	The STATCOM provides the lagging reactive power to the ac system

Table 2-2 Power exchange in the STATCOM

Condition	P	Q
I: $V_c > V_s$ and $\delta < 0$	>0	>0
II: $V_c > V_s$ and $\delta > 0$	<0	>0
III: $V_c < V_s$ and $\delta > 0$	<0	<0
IV: $V_c < V_s$ and $\delta < 0$	>0	<0

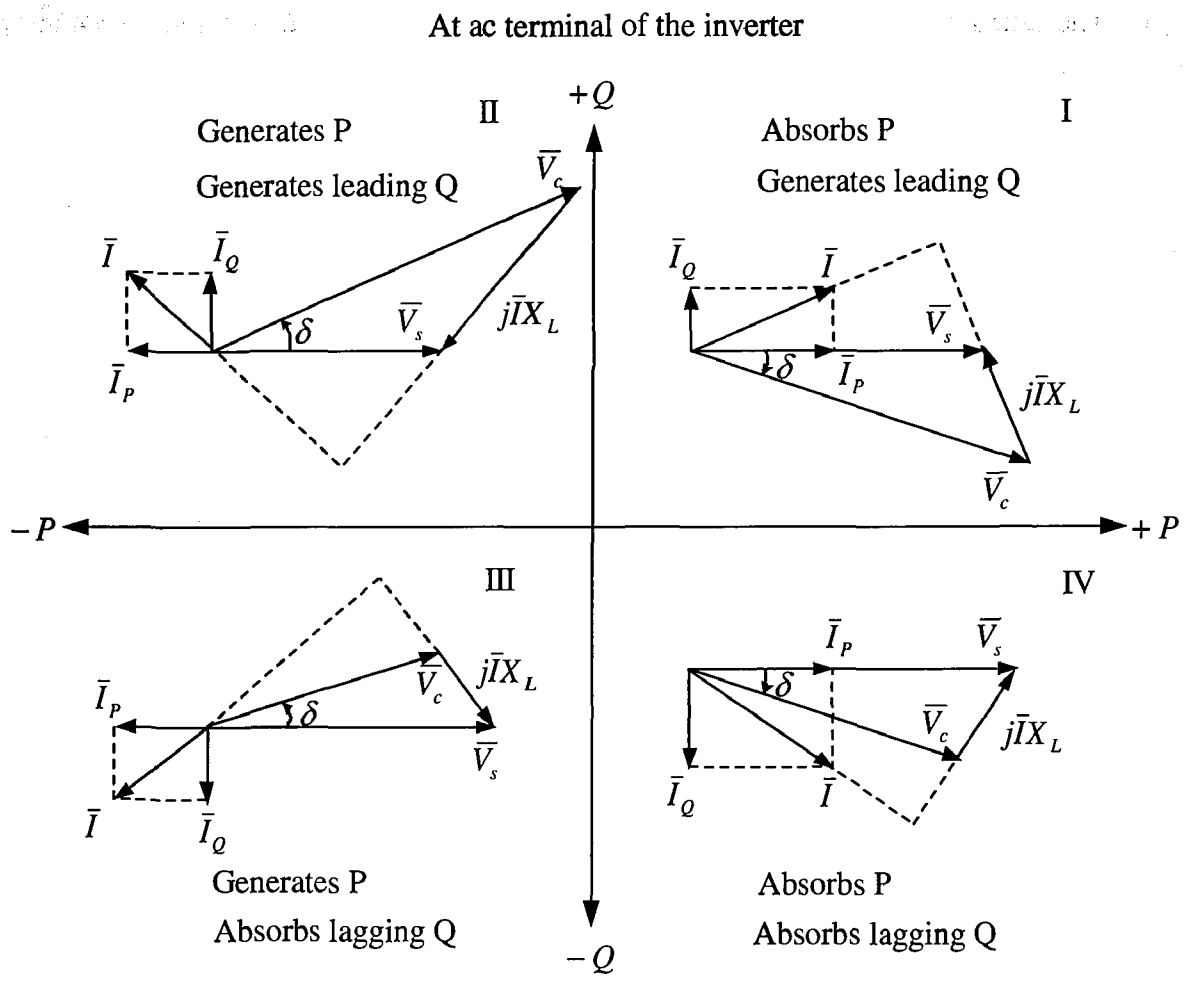


Figure 2-9. Phasor diagram for the power exchanges in the STATCOM system.

The phasor diagram of the first plane in Figure 2-9 is used as an example to explain the power exchange. The inverter output voltage $\bar{V}_c$ lags the system voltage $\bar{V}_s$ (δ<0) and the amplitude of $\bar{V}_c$ is greater than that of $\bar{V}_s$. The reactive current component I_Q leads the system voltage by 90^0, and thus the STATCOM generates leading reactive power to the ac system (Q>0). Meanwhile, the active current component I_P is in phase with the ac system voltage, and thus the STATCOM absorbs the active power from the ac system (P>0).

2.3 Reference Frame Transformation

In order to decouple the active and reactive power control, the reference frame transformation theory is used to convert the time-variant system to time-invariant system. The process of frame transformation is to transfer abc (three-phase stationary) frame to αβ (two-phase stationary) frame first, and then to dq (two-phase synchronous) frame. The transformations among reference frames are discussed in this section.

The relationship between the abc and αβ frame is shown in Figure 2-10, where the angle between abc and αβ frame (the angle between a- and α -axis) is set at 0^0 for calculation simplification. The transformation equation from abc to αβ frame is:

$$\begin{bmatrix} F_\alpha \\ F_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} F_a \\ F_b \\ F_c \end{bmatrix} \tag{2.8}$$

where Fs are variables representing voltages or currents.

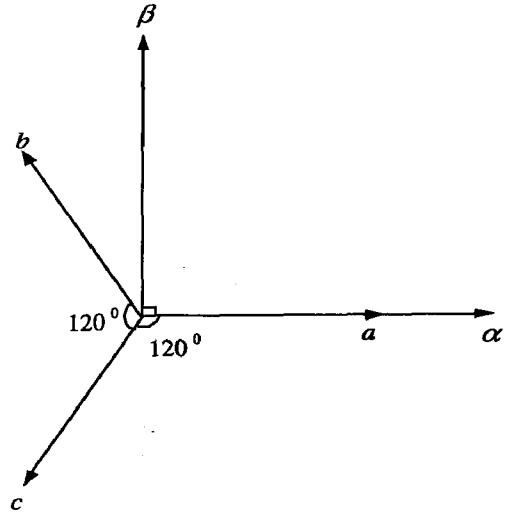


Figure 2-10. abc and αβ reference frames.

The relationship between the αβ and dq frame is shown in Figure 2-11, where the angle between αβ and dq frame (the angle between α- and d-axis) is defined as θ. The transformation equation from αβ to dq frame is:

$$\begin{bmatrix} F_d \\ F_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} F_\alpha \\ F_\beta \end{bmatrix} \tag{2.9}$$

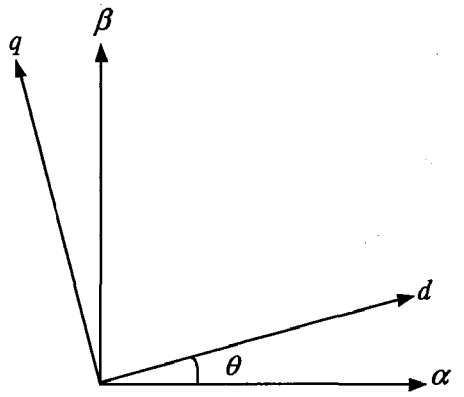


Figure 2-11. αβ and dq reference frames.

The transformation of three-phase (abc-axis) variables to the equivalent two-phase (dq-axis) variables can be performed by

$$\begin{bmatrix} F_d \\ F_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ -\sin\theta & -\sin(\theta - 2\pi/3) & -\sin(\theta + 2\pi/3) \end{bmatrix} \cdot \begin{bmatrix} F_a \\ F_b \\ F_c \end{bmatrix} \tag{2.10}$$

2.4 DQ-Frame Model of the STATCOM Equivalent Circuit

To decouple the active and reactive power control, the dynamic model in dq frame for the STATCOM equivalent circuit is derived in this section.

The first-order differential equation in abc frame for the equivalent STATCOM circuit, as shown in Figure 2-6, can be written as

$$L\frac{d\mathbf{i}_{abc}}{dt} = \mathbf{v}_{sabc} - \mathbf{v}_{cabc} \tag{2.11}$$

where $\mathbf{i}_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$, $\mathbf{v}_{sabc} = \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix}$, and $\mathbf{v}_{cabc} = \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix}$. The bold symbol represents a matrix.

After the transformation described in equation (2.10), the dynamic model in dq frame is as follows,

$$L\frac{d}{dt}\begin{bmatrix} I_d \\ I_q \end{bmatrix} + \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \cdot \begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} V_{sd} - V_{cd} \\ V_{sq} - V_{cq} \end{bmatrix} \tag{2.12}$$

where

V_{sd} and V_{sq} are the d-axis and q-axis system voltages,

V_{cd} and V_{cq} are the d-axis and q-axis inverter voltages,

I_d and I_q are the d-axis and q-axis inverter currents,

$\omega = d\theta / dt$.

Assuming that the d-axis of the synchronous frame is aligned with $\overline{V}_s$, this leads to

$$\mathbf{V}_{s\alpha\beta} = \begin{bmatrix} V_{s\alpha} \\ V_{s\beta} \end{bmatrix} = V_s \cdot \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} \text{ and} \tag{2.13}$$

$$\mathbf{V}_{sdq} = \begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot V_s \cdot \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} = \begin{bmatrix} V_s \\ 0 \end{bmatrix} \tag{2.14}$$

where V_s is the amplitude of system voltage, and $V_{s\alpha}$ and $V_{s\beta}$ are system voltage components in αβ frame. Since $V_{sd} = V_s$, and $V_{sq} = 0$, the active power, P, and reactive power, Q, can be obtained as:

$$P = V_s I_d \text{ and } Q = V_s I_q \tag{2.15}$$

where I_d and I_q represent the active and reactive current component of the STATCOM, respectively. This feature enables a decoupled control of two current components and thus decoupling the control of two power components, P and Q. Both I_d and I_q can be positive and negative. Active power flows into the inverter for positive I_d and out from the inverter for negative I_d. The STATCOM generates leading reactive power when I_q is positive and lagging reactive power when I_q is negative.

2.5 Decoupling Power Control Scheme

Based on the dq model of the STATCOM equivalent circuit, the decoupling power control scheme is proposed in this section.

It is straightforward that in order for the STATCOM to generate the desired active and reactive current components (I_d^* and I_q^*), references of inverter voltages V_{cd} and V_{cq}, V_{cd}^* and V_{cq}^*, should be given as:

$$\begin{bmatrix} V_{cd}^* \\ V_{cq}^* \end{bmatrix} = \begin{bmatrix} V_{sd} + \omega L I_q^* - L\frac{d}{dt} I_d^* \\ V_{sq} - \omega L I_d^* - L\frac{d}{dt} I_q^* \end{bmatrix} \tag{2.16}$$

Therefore, the references of V_c and δ, variables for controlling the reactive and active power, can be obtained by

$$\begin{aligned} V_c^* &= \sqrt{V_{cd}^{*2} + V_{cq}^{*2}} \\ \delta &= \tan^{-1}\left(\frac{V_{cq}^*}{V_{cd}^*}\right) \end{aligned} \tag{2.17}$$

For phase-shifted PWM scheme, the modulating index m_a is defined by

$$m_a = \frac{V_c^*}{V_{c\max}} \tag{2.18}$$

where V_c^* is the amplitude reference of the inverter output voltage, and $V_{c\max}$ is the maximum obtainable amplitude of the inverter output voltage. In cascaded multilevel inverter, when m_a=1, $V_{c\max}$=1.224V_{dc} [23], where V_{dc} is the total capacitor dc-voltage per phase.

Figure 2-12 shows the decoupling power control diagram of a seven-level CHB-based STATCOM system. V_{dc_ref} is the total phase dc-voltage reference. V_{dc} is the total dc-voltage per phase. A dc-voltage feedback control loop is used to regulate the total dc-voltage. The basic idea of this regulator is to use the error between the reference and the total dc-voltage as the feedback signal.

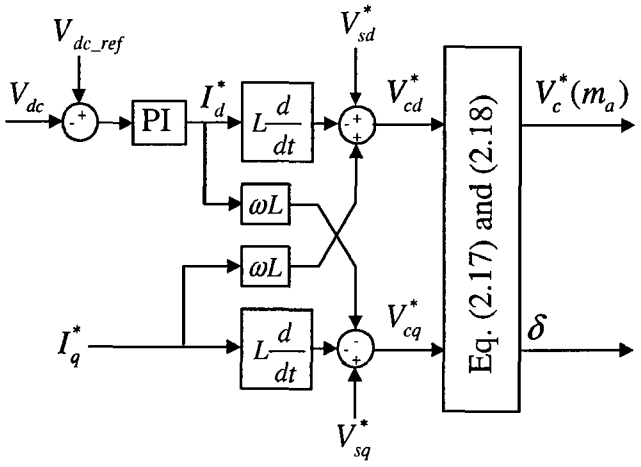


Figure 2-12. Decoupling power control diagram of a CHB-based STATCOM.

This signal is then fed to a PI regulator to produce the active current reference I_d^*. The reactive current reference, I_q^*, is given according to the command, $I_q^* = Q_{\_ref} / V_s$, where $Q_{\_ref}$

is the reference reactive power. $V_{sd}^{*}=V_s$ and $V_{sq}^{*}=0$. The amplitude reference of the inverter output voltage and the phase difference between v_s and v_c, V_c^{*} and δ, are calculated from equation (2.17). The modulation index m_a is calculated from equation (2.18).

To generate the required reactive power from the inverter, the modulation index m_a is varied. When m_a is $m_{a(\max)}$, the inverter generates the rated leading reactive power ($+Q$) and the STATCOM operates in the capacitive mode, whereas when m_a is $m_{a(\min)}$, the inverter absorbs the rated lagging reactive power ($-Q$) and the STATCOM operates in the inductive mode. The phase difference δ is used to control the active power exchange and regulate total dc-voltage to the expected value.

2.6 Summary

In this chapter, the system configuration and operating principles of the CHB-based STATCOM are presented. Phase-shifted PWM is used as the modulation strategy. To control active and reactive power separately, the dynamic model in the dq synchronous frame for the STATCOM equivalent circuit is derived. A decoupling control scheme for power exchange is proposed. The amount of reactive power can be controlled by adjusting the amplitude of the inverter output voltage. The amount of active power can be controlled by adjusting the phase difference δ of the inverter output voltage with respect to the system voltage.

CHAPTER 3
DC VOLTAGE DETECTION AND BALANCE CONTROL TECHNIQUE

This chapter focuses on the study of dc capacitor-voltage detection and balance control of the CHB-based STATCOM system. To obtain all individual H-bridge dc-voltages with the least voltage sensors, the principle of dc capacitor-voltage detection is investigated and the single multiple-voltage (SMV) detector is developed. With the detected dc capacitor-voltages as feedback signals, the feedback balance control method is proposed to ensure the balance of all individual H-bridge dc-voltages.

3.1 Introduction

It has been recognized that the CHB inverter is the promising topology for the STATCOM application due to its attractive features of the modular structure and high level output voltage without switches in series. Unfortunately, problems exist in the CHB-based STATCOM. One of the main problems is the unbalance of dc-voltages in H-bridge units. Many reasons may contribute towards unbalanced dc capacitor-voltages in CHB-based STATCOM system: unbalanced inverter current, unequal H-bridge component loss, unequal delays in switching, and asymmetrical charging of the capacitor that may occur when capacitors are initially charged by ac system during starting up the STATCOM. The dc capacitor-voltage unbalance may result in uneven voltage stress on switches and the distortion

of inverter output voltage due to the degradation of total harmonic distortion (THD) factor. For example, if there are many single-phase loads in the distribution system, the ac system voltage will be unbalanced. This disturbance of unbalanced voltages may cause unbalanced inverter current and thus the unbalance of dc capacitor-voltages arises. The voltage stress on switches will increase and the inverter voltage will become distorted as well. If the capacitor voltage drift is excessive, the switch rating may be exceeded resulting in failure [24]. Therefore, the individual H-bridge dc-voltage balance control is essential 1) to ensure the even sharing of voltage stresses in switches, and 2) to prevent the degradation of the THD in inverter output voltage.

In order to implement the individual dc capacitor-voltage balance control, every dc capacitor-voltage has to be measured by a voltage sensor and controlled separately. The per-phase diagram of an m-level CHB-based STATCOM with the traditional dc-voltage measurement is shown in Figure 3-1 (a), where the block *PT* represents a voltage sensor. v_{Hj} (j=1, 2, …, n) and v_c are H-bridge output voltage and inverter output voltage. DC-voltages v_{dcj} are measured by voltage sensors. The number of H-bridge units connected in series per phase leg is $n = \frac{m-1}{2}$, where m is the number of voltage level that the inverter can produce. For example, in a nine-level CHB-based STATCOM, there are twelve H-bridges and thus twelve voltage sensors are required. With a number of sensors in a system, the cost will be increased and the system will be complex. The reliability of the system will be weakened as well.

The dc capacitor-voltage detection technique, referred to as single multiple-voltage (SMV) detector, is developed to reduce the number of voltage sensors. The per-phase diagram of an *m*-level CHB-based STATCOM with the proposed SMV detector is shown in Figure 3-1 (b). Only one voltage sensor per phase is employed to measure the inverter phase output voltage. All individual H-bridge dc-voltages, $v'_{dc1}, v'_{dc2}, \Lambda, v'_{dcn}$, are obtained from the SMV detector. The superscript of v_{dcj} (j=1, 2, Λ, n) means that the dc capacitor-voltage is obtained from the SMV detector based on the inverter output voltage. As a result, the number of voltage sensors is substantially reduced.

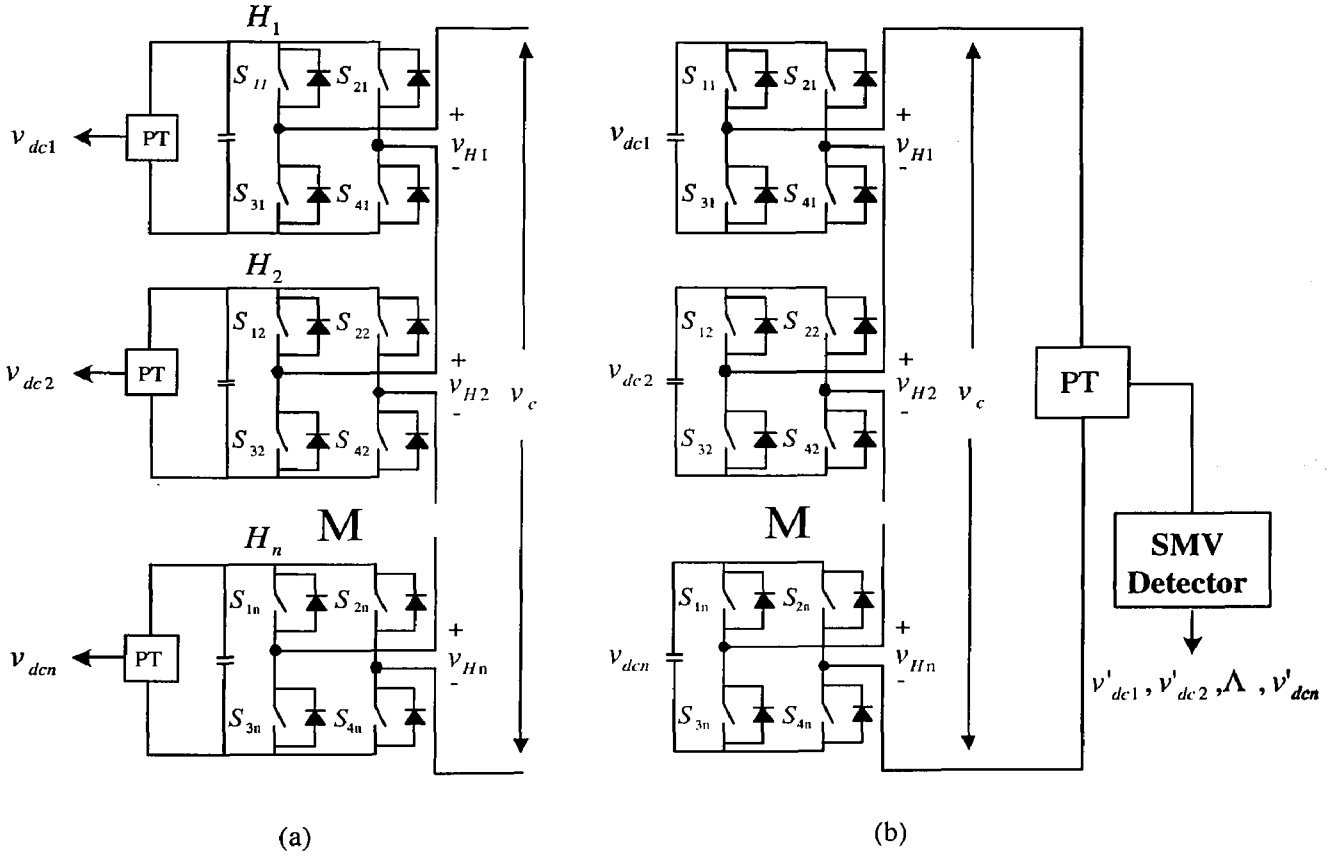


Figure 3-1. Per-phase diagram of m-level CHB-based STATCOM with
(a) traditional dc-voltage measurement method and (b) proposed dc-voltage detection method.

3.2 DC Capacitor-Voltage Detection Technique

In this section, the principle of the dc capacitor-voltage detection is investigated and the SMV algorithm is proposed to perform the dc-voltage detection. The algorithm and operating procedure of the SMV detector are presented in details.

3.2.1 Principle of DC Capacitor-Voltage Detection

To investigate the principle of dc capacitor-voltage detection technique for the CHB-based STATCOM, the single-phase H-bridge inverter is discussed first. The relationship of dc capacitor-voltage and inverter output voltage is then derived based on a seven-level CHB inverter.

The single-phase H-bridge inverter is shown in Figure 3-2, where v_H and i are H-bridge output voltage and current. v_{dc} and i_{dc} are the capacitor voltage and current. The switch pair in each leg, (S_1, S_3) or (S_2, S_4), operates complementary. The combination of possible switching states of the H-bridge is shown in Figure 3-3. The H-bridge output voltage v_H has three possible voltage levels: 1) $v_H = v_{dc}$ when S_1 is on and S_2 is off, 2) $v_H = -v_{dc}$ when S_1 is off and S_2 is on, and 3) $v_H = 0$ when S_1 and S_2 are on or off. Define SW as the switching function of the H-bridge. The relationship of switching state combination, switching function and H-bridge output voltage is illustrated in Table 3-1. In summary, the H-bridge output voltage is given by

$$v_H = SW \cdot v_{dc} \tag{3.1}$$

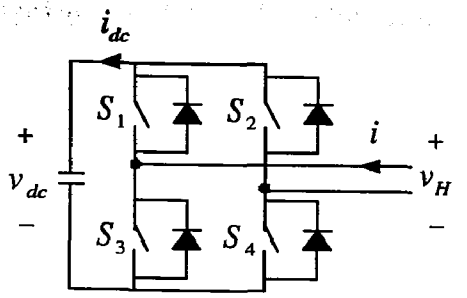
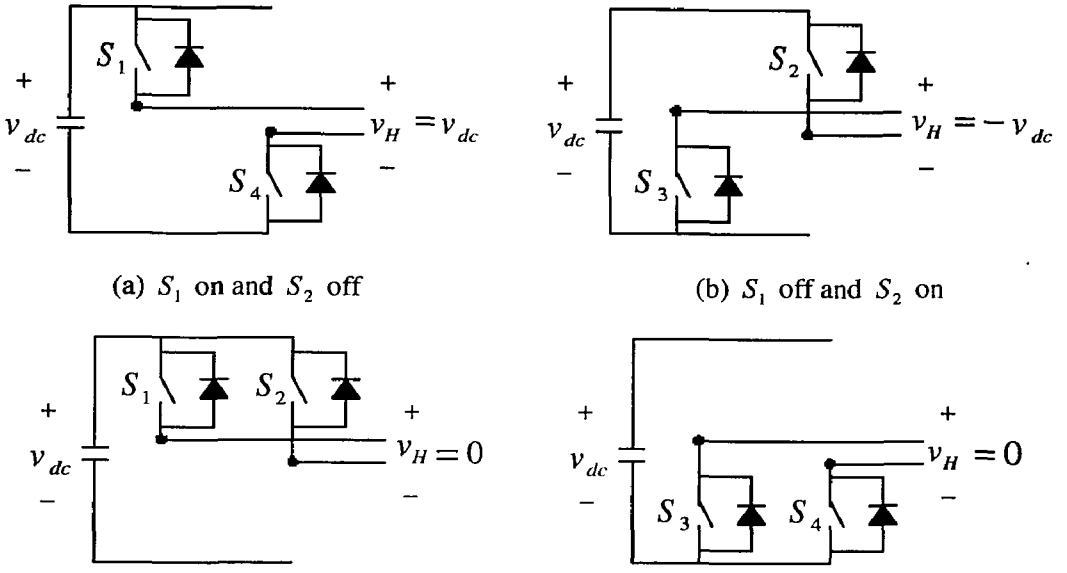


Figure 3-2. The structure of an H-bridge inverter.



(a) S_1 on and S_2 off

(b) S_1 off and S_2 on

(c) S_1 on and S_2 on

(d) S_1 off and S_2 off

Figure 3-3. Switching state combinations of an H-bridge inverter.

Table 3-1 Switch combination, switching function and output voltage of an H-bridge

S_1	S_2	SW	v_H
0	0	0	0
0	1	-1	$-v_{dc}$
1	0	1	v_{dc}
1	1	0	0

A seven-level cascaded H-bridge inverter, as shown in Figure 3-1 (b) where n=3, is used as an example to present the principle of dc-voltage detection technique. The inverter output voltage v_c is the sum of each H-bridge output voltage in one leg, i.e.,

$$v_c = v_{H1} + v_{H2} + v_{H3} \tag{3.2}$$

If the H-bridge unit H_j (j=1, 2 or 3) has an output voltage alone whereas output voltages of other units are zero, $v_c = v_{Hj} = SW_j \cdot v_{dcj}$. The condition of this case is defined as the detection condition and the inverter voltage v_c is called one-level voltage pulse. Once the detection condition is satisfied, the dc-voltage of H-bridge H_j can be obtained from the inverter output voltage as follows:

$$v'_{dcj} = \frac{v_c}{SW_j} = |v_c| \tag{3.3}$$

where the subscript of v_{dcj} means that the dc-voltage is obtained from the SMV detector, not from direct measurement.

3.2.2 Single Multiple-Voltage (SMV) Algorithm

The SMV algorithm is developed to verify the detection condition and to perform detecting dc capacitor-voltages. The basic idea of the SMV detector is to identify the time when the inverter voltage v_c is one-level and the H-bridge that has output voltage alone. If the detection condition is satisfied, the SMV detector outputs $|v_c|$ as dc-voltage of the H-bridge that has output voltage alone, v'_{dcj}. If the detection condition is not satisfied, the SMV detector does not output $|v_c|$ and keeps the previous v'_{dcj}. This method is applicable in practice because the capacitor voltage does not change instantaneously in event of rapid

change in system voltage. In doing so, multiple dc capacitor-voltages can be obtained from the single inverter voltage. A block diagram of the SMV detector is shown in Figure 3-4, where inputs of the SMV detector are three-phase inverter output voltages and outputs of the SMV detector, represented by a vector $\mathbf{v'_{dc}}$, are individual dc capacitor-voltages of all three phases. The bold symbol represents a set of individual dc-voltages.

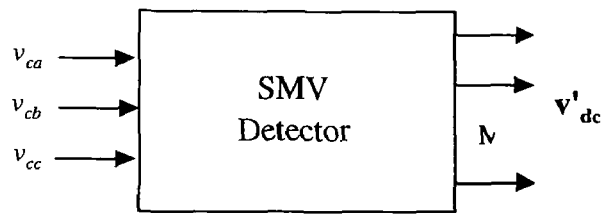


Figure 3-4. Block diagram of the SMV detector.

The operation of the SMV detector is further explained in Figure 3-5. Waveforms in Figure 3-5 (a) are sinusoidal modulating wave and six triangular carrier waves that are the same as those in Figure 2-4. v_{H1}, v_{H2}, v_{H3} and v_c in Figure 3-5 (b), (c), (d) and (e) are three H-bridge output voltages and the inverter output voltage. Each shaded area in v_c is one-level voltage pulse and corresponds to the output voltage of a certain H-bridge unit. With dc-voltage regulation and balance control, dc-voltages of different levels suppose to be identical, assumed to be E. The variable R is defined in Table 3-2. For example, the first one-level pulse of v_c in Figure 3-5 corresponds to v_{H2}, i.e., $v_c = v_{H2}$. Thus, R=2 and the dc-voltage of the second H-bridge v'_{dc2} is equal to $|v_c|$ during this one-level pulse. In the same way, the following two one-level pulses of v_c correspond to v_{H1} and v_{H3}, respectively. Accordingly, R=1 and R=3 during these two pulses. The value of R is determined by switching states and the determination rule is listed in Table 3-3.

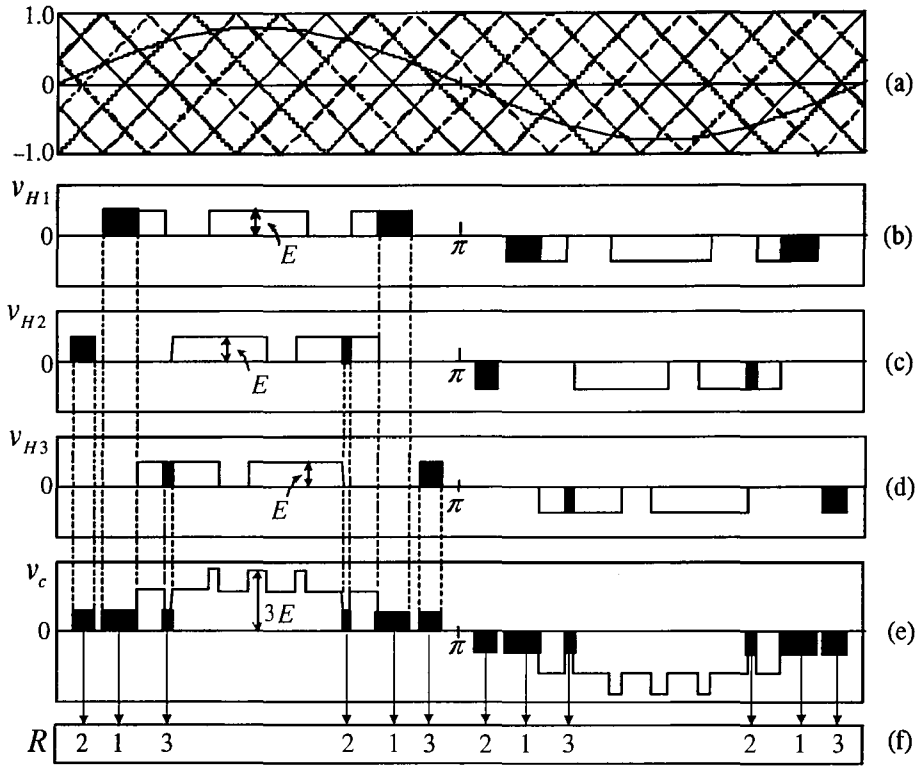


Figure 3-5. Waveform explanation of the SMV detector (phase-shifted PWM, $m_a = 0.8$ and $m_f = 3$).

Table 3-2 Definition of R

Detection condition	R
$v_c = v_{H1} = SW_1 \cdot v_{dc1}$ and $v_{H2} = v_{H3} = 0$	1
$v_c = v_{H2} = SW_2 \cdot v_{dc2}$ and $v_{H1} = v_{H3} = 0$	2
$v_c = v_{H3} = SW_3 \cdot v_{dc3}$ and $v_{H1} = v_{H2} = 0$	3
Otherwise	0

Table 3-3 Determination of R

Switching states of H- bridge cells			Output voltage of SMV detector	R
H_1	H_2	H_3		
(S_{11}=1 and S_{21}=0) or (S_{11}=0 and S_{21}=1)	(S_{12}=0 and S_{22}=0) or (S_{12}=1 and S_{22}=1)	(S_{13}=0 and S_{23}=0) or (S_{13}=1 and S_{23}=1)	$v'_{dc1} = SW_1 \cdot v_c = \lvert v_c \rvert$	1
(S_{11}=0 and S_{21}=0) or (S_{11}=1 and S_{21}=1)	(S_{12}=1 and S_{22}=0) or (S_{12}=0 and S_{22}=1)	(S_{13}=0 and S_{23}=0) or (S_{13}=1 and S_{23}=1)	$v'_{dc2} = SW_2 \cdot v_c = \lvert v_c \rvert$	2
(S_{11}=0 and S_{21}=0) or (S_{11}=1 and S_{21}=1)	(S_{12}=0 and S_{22}=0) or (S_{12}=1 and S_{22}=1)	(S_{13}=1 and S_{23}=0) or (S_{13}=0 and S_{23}=1)	$v'_{dc3} = SW_3 \cdot v_c = \lvert v_c \rvert$	3

The operation flowchart of the SMV detector for the seven-level CHB inverter is shown in Figure 3-6. According to switching states, the determination rule of R is performed. The detection condition is judged. If $R=j$ (j=1, 2 or 3), only the H-bridge H_j has output voltage and the inverter voltage is one-level. In this case, the dc-voltage of the H-bridge H_j can be obtained from the inverter voltage v_c. Therefore, the SMV detector outputs $|v_c|$ as the dc-voltage v'_{dcj}. If $R \neq j$, the inverter voltage is not one-level or does not includes the output voltage of H_j. Thus, the dc-voltage v'_{dcj} cannot be obtained from v_c and the SMV detector does not output and update v'_{dcj} with $|v_c|$. Instead, the SMV detector keeps the previous value of dc-voltage.

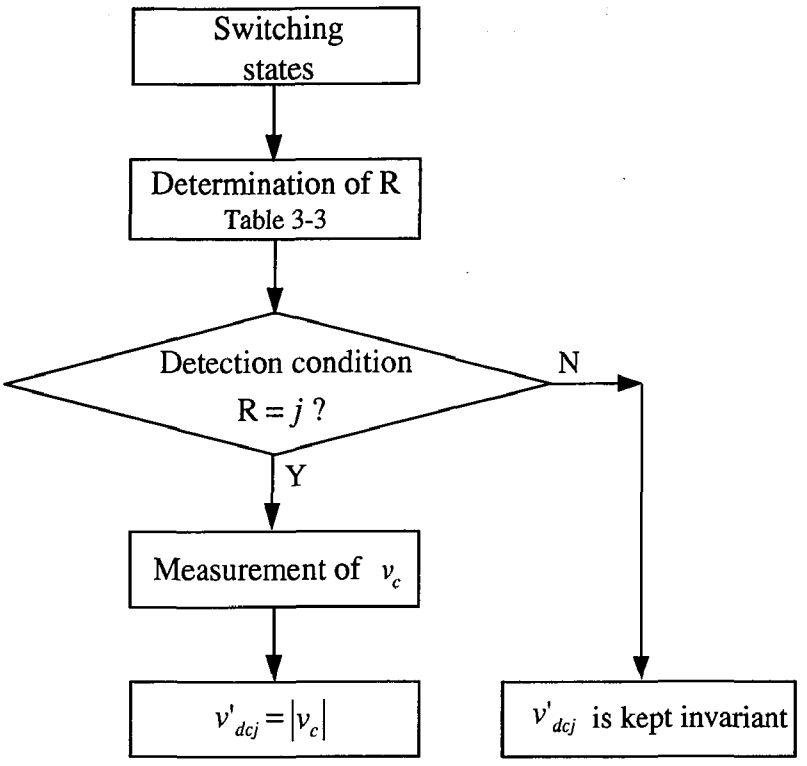


Figure 3-6. Operation flowchart of the SMV detector for the 7-level CHB inverter (j=1, 2, or 3).

In conclusion, the SMV detector works only when the inverter output voltage is one level. It outputs and updates v'_{dcj} with $|v_c|$ for the H-bridge H_j when the detection condition is satisfied. Otherwise, the SMV detector keeps v'_{dcj} invariant.

3.3 Individual DC Capacitor-Voltage Balance Control

In this section, the charging of a capacitor in an H-bridge is discussed first. The dc capacitor-voltage control method for the proposed STATCOM operating in both capacitive and inductive modes is then presented. The individual dc-voltage balance controller of CHB-based STATCOM is proposed.

3.3.1 Charging of DC Capacitor

In order to control the dc capacitor-voltage, it is necessary to investigate the charging of a capacitor in an H-bridge. The voltage of a capacitor is given by

$$v_{dc}(t) = \frac{1}{C}\int_{-\infty}^{t} i_{dc}(t)dt \tag{3.4}$$

where C is the size of capacitor and i_{dc} is the charging current of the capacitor. From equation (3.4), the voltage change on a capacitor is the combined effect of the capacitor size and the charging current. Once the capacitance is determined, the charging of a capacitor is dominated by the charging current i_{dc}. Referring to the structure of an H-bridge shown in Figure 3-2, the capacitor current is related to the switching function and the inverter ac side current as follows,

$$i_{dc} = SW \cdot i \tag{3.5}$$

where i is the inverter ac-side current and SW is the switching function of the H-bridge.

With the cascaded multilevel inverter and the coupling inductor as a filter in the STATCOM, as shown in Figure 1-2, the inverter current i could be assumed as sinusoidal. In reactive power compensation, the inverter current and the output voltage are in quadrate. It

means that the inverter current either leads or lags the voltage by $\pi/2$, depending on whether the STATCOM operates in the capacitive or inductive mode. In Figure 3-7 (a), the inverter current i leads the inverter output voltage v_H by $\pi/2$. v_{H1} is the fundamental waveform of v_H. Figure 3-7 (b) and (c) show the switching function and portions of i which are admitted by switches in the H-bridge to form i_{dc}. To simplify the analysis, the fundamental frequency switching strategy is used in Figure 3-7 to form the capacitor charging current instead of the phase-shifted PWM, which is actually used in this study. As the charging of a capacitor has certain features common to both methods, it is sufficient to examine the capacitor charging current for the case of fundamental frequency method.

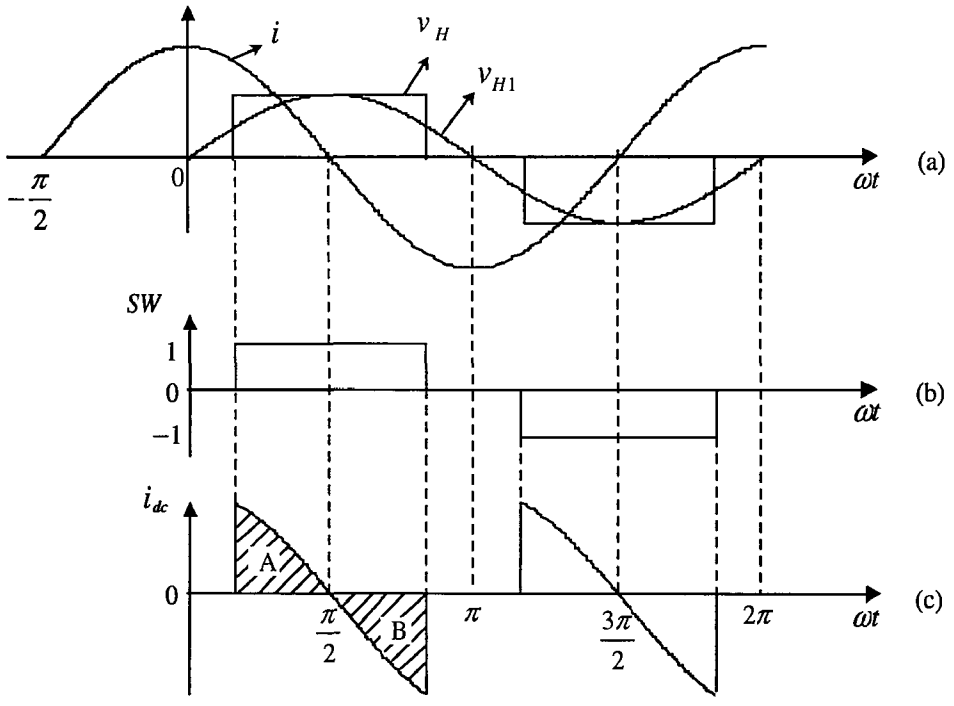


Figure 3-7. Charging of DC capacitor in an H-bridge inverter
(a) inverter current and output voltage, (b) switching function and (c) capacitor current.

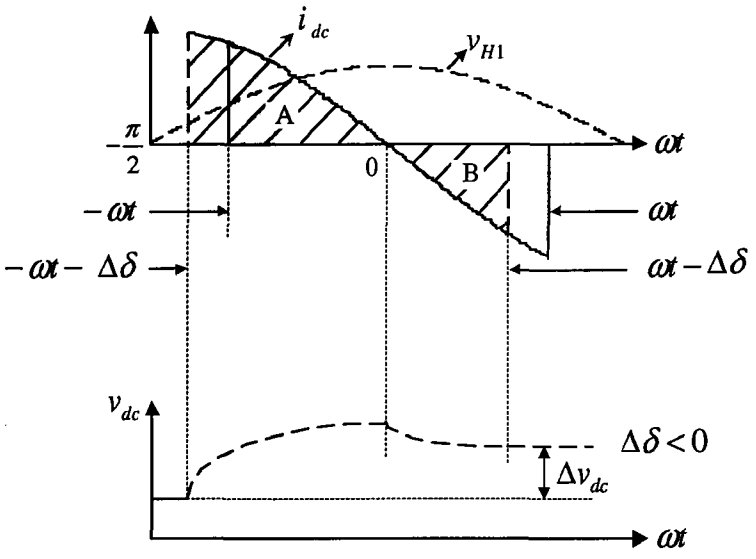
In Figure 3-7 (c), the positive area A and the negative area B are equal. It is concluded that the average charge on the dc capacitor over every half-cycle is equal to zero. Due to this symmetric charge flow, the voltage on the dc capacitor remains theoretically balanced.

3.3.2 Controlling DC Voltages

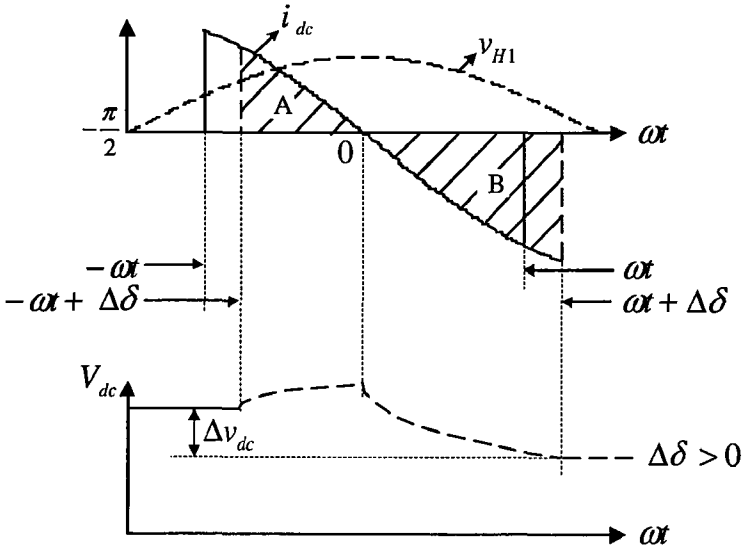
If the positive area A and the negative area B in Figure 3-7(c) are not equal, the charge and discharge of the capacitor will not be identical over the half-cycle. The dc capacitor-voltage will increase or decrease. Therefore, the average capacitor voltage can be controlled by asymmetrically displacing the charging current i_{dc}. In this subsection, the dc-voltage control method for both capacitive and inductive mode is presented.

DC-Voltage Control in the Capacitive Mode

Figure 3-8 depicts the dc capacitor-voltage control when the STATCOM operates in the capacitive mode. In Figure 3-8 (a), the inverter current i leads the fundamental inverter voltage v_{H1} by $\pi/2$. The charging current is left shifted by $\Delta\delta$ ($\Delta\delta<0$). It can be seen that the positive area A is bigger than the negative area B. Δv_{dc} is the capacitor voltage change within the half cycle. As a result, the capacitor will be charged and the dc-voltage will increase ($\Delta v_{dc}>0$). If the charging current is right shifted by $\Delta\delta$ ($\Delta\delta>0$), as shown in Figure 3-8 (b), the positive area A is smaller than the negative area B. Thus, the capacitor will be discharged and the dc-voltage will decrease ($\Delta v_{dc}<0$). If $\Delta\delta=0$, the capacitor voltage will sustain ($\Delta v_{dc}=0$).



(a)



(b)

Figure 3-8. Principle of capacitor dc-voltage control in the capacitive mode (a) i_{dc} is left shifted ($\Delta\delta<0$), (b) i_{dc} is right shifted ($\Delta\delta>0$).

The dc-voltage control scheme in the capacitive mode can be verified by the following analysis. Choose the time origin of Figure 3-8 so that the inverter current can be expressed by

$$i = -I \cdot \sin \omega t \tag{3.6}$$

Shifting the capacitor charging current slightly in the time axis, represented by Δt, the capacitor voltage change within the half cycle is

$$\begin{aligned} \Delta v_{dc} &= \frac{1}{C} \int_{-t+\Delta t}^{t+\Delta t} -I \cdot \sin \omega t dt \\ &= -\frac{2I}{\omega C} \sin \omega t \cdot \sin(\omega \Delta t) \end{aligned} \tag{3.7}$$

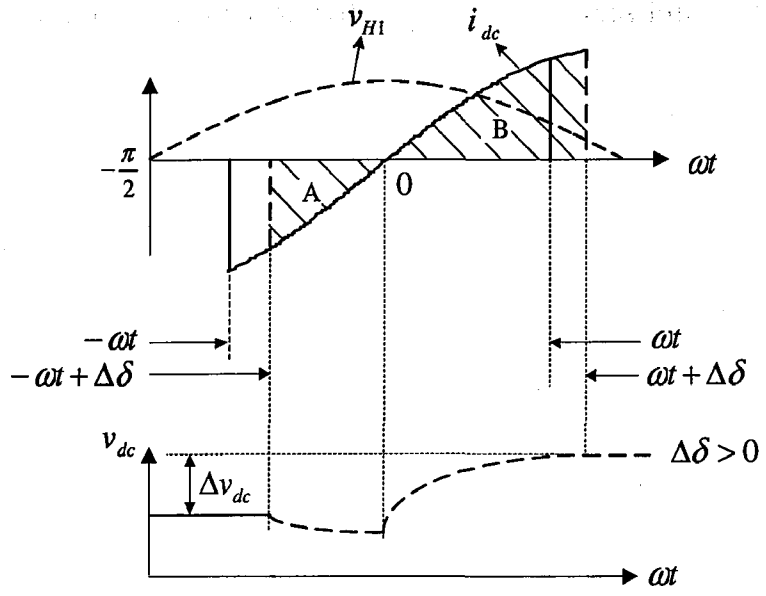
For small Δt,

$$\Delta v_{dc} = -\frac{2I}{\omega C} \sin \omega t \cdot (\Delta t) \tag{3.8}$$

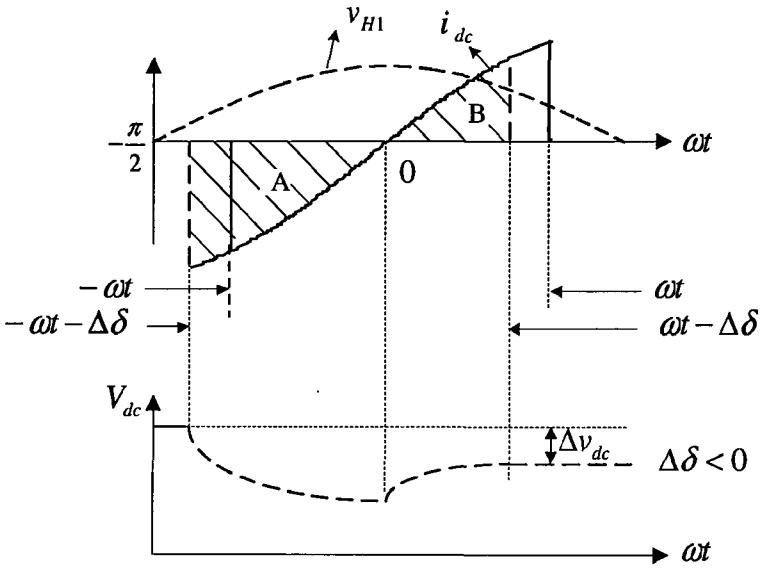
It can be proved from equation (3.8) that dc capacitor-voltage can be controlled by shifting the capacitor current an angle, $\Delta\delta = \omega\Delta t$. The dc-voltage increases, decreases or sustains when $\Delta\delta < 0$, $\Delta\delta > 0$ or $\Delta\delta = 0$, respectively.

DC-Voltage Control in the Inductive Mode

The dc-voltage control in the inductive mode is shown in Figure 3-9 where the current i_{dc} lags voltage v_{H1} by $\frac{\pi}{2}$. The control principle is opposite to that in the capacitive mode. The capacitor voltage increases, decreases or sustains when $\Delta\delta > 0$, $\Delta\delta < 0$ or $\Delta\delta = 0$, respectively.



(a)



(b)

Figure 3-9. Principle of capacitor dc-voltage control in the inductive mode (a) i_{dc} is right shifted ($\Delta\delta>0$), (b) i_{dc} is left shifted ($\Delta\delta<0$).

Likewise, the dc-voltage control method in the inductive mode can be proved by the following analysis. Choose the time origin in Figure 3-9 so that the inverter phase current can be expressed by

$$i = I \cdot \sin \omega t \tag{3.9}$$

The capacitor voltage change within the half cycle is described by equation (3.10) if the capacitor current is slightly shifted by Δt in the time axis.

$$\begin{aligned} \Delta v_{dc} &= \frac{1}{C} \int_{-t+\Delta t}^{t+\Delta t} I \cdot \sin \omega t dt \\ &= \frac{2I}{\omega C} \sin \omega t \cdot (\Delta t) \end{aligned} \tag{3.10}$$

It can be concluded from equation (3.10) that the dc-voltage can be controlled by shifting the capacitor current an angle, $\Delta\delta = \omega\Delta t$. The dc-voltage increases, decreases or sustains when $\Delta\delta < 0$, $\Delta\delta > 0$ or $\Delta\delta = 0$, respectively in the inductive mode.

3.3.3 Individual DC-Voltage Balance Control

Consequently, the voltage across each capacitor can be maintained by prolonging or shortening the current flowing through it. This can be achieved by slightly shifting the sinusoidal modulating wave of phase-shifted PWM. The direction of phase shift depends on whether the inverter is producing leading reactive power or absorbing lagging reactive power. A feedback control loop, as shown in Figure 3-10, is developed to balance the dc-voltage of an H-bridge in the CHB-based STATCOM. The error is a difference between the individual dc-voltage reference V_{dc_ref} / n (n is the number of H-bridges) and the detected individual dc-voltage v'_{dc} (could be the detected dc-voltage of any H-bridge) from the SMV detector. The direction of phase shift, represented by a variable D, depends on operating mode (capacitive,

inductive or standby mode) of the STATCOM. D is equal to 1 in the capacitive mode, -1 in the inductive mode and 0 in the standby mode. The product of the error and D is regulated by a PI controller. The output $\Delta\delta$, corresponding to $\omega\Delta t$, is the required phase shift of the sinusoidal modulating wave of phase-shifted PWM.

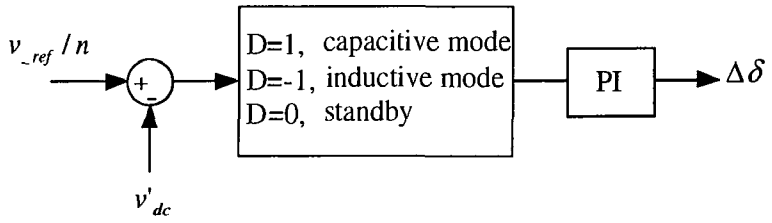


Figure 3-10. Feedback control loop for individual dc-voltage balance control.

3.3.4 Complete Controller for the CHB-Based STATCOM

Combining the proposed methods of phase-shifted PWM, decoupling power control, dc-voltage detection and individual dc-voltage balance control, the complete controller for the CHB-based STATCOM is developed and shown in Figure 3-11, where a seven-level cascaded H-bridge inverter is used as an example. The complete STATCOM controller includes four parts: the SMV detector, the decoupling power controller, the individual dc-voltage balance controller and the switching modulator. Details are described as follows.

SMV Detector

Inputs of the SMV detector are three-phase inverter output voltages, v_{ca}, v_{cb} and v_{cc}. The SMV detector detects all individual dc-voltages based on the dc-voltage detection technique discussed in Section 3.2. Outputs of the SMV detector are detected individual dc-voltages of three phases. v'_{dc_avg} is the average phase total dc-voltage and is used as feedback dc-voltage

for the decoupling power controller. For simplification, v'_{dc_avg} is the same for controllers in three phases such that only one feedback total dc-voltage control loop is used for three-phase controllers.

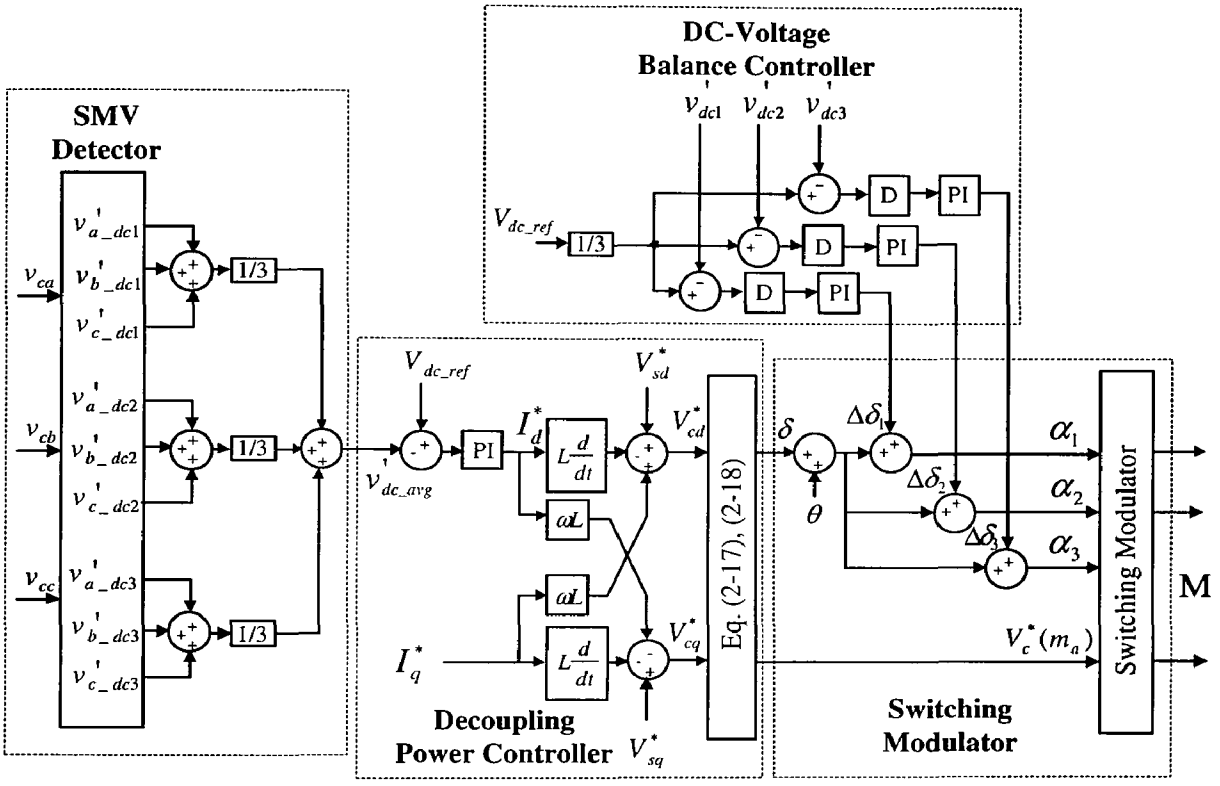


Figure 3-11. Complete control block diagram for the seven-level CHB-based STATCOM.

Decoupling Power Controller

The d-channel is the total dc-voltage regulation control loop. The detected average total dc-voltage v'_{dc_avg} is compared with the reference of one-phase total dc-voltage V_{dc_ref}. The error is inputted to the total voltage PI regulator. The output of the regulator, I^*_{cd}, is used as the reference for I_d. In q-channel, I^*_q is the desired reactive power command ($I^*_q = Q_{\_ref} / V_s$). V^*_{cd} and V^*_{cq}, the dq-component references of inverter voltages, are obtained from equation

(2.16). The amplitude reference V_c^* and the angle δ (phase angle difference of the inverter output voltage and the system voltage) are calculated from equation (2.17).

DC-Voltage Balance Controller

Three dc-voltage feedback control loops are use to balance individual dc-voltages in one phase. The individual dc-voltage of each H-bridge is compared with $V_{dc\_ref}/3$. Their errors are multiplied by D. If the STATCOM operates in the capacitive mode, D is 1; if the STATCOM operates in the inductive mode, D is -1; if the STATCOM operates in the standby mode, D is 0. Outputs after D are the desired shifting angles, $\Delta\delta_j$ (j=1, 2, or 3).

Switching Modulator

Shifting angles, $\Delta\delta_j$ (j=1, 2, or 3) are summed to θ and δ, respectively. θ is obtained from the system voltage using PLL circuit. The angle δ obtained from the decoupling power controller is the same for all individual dc-voltage balance control-loops. The angle δ adjusts the active power exchange between the STATCOM and the ac system, whereas the angles $\Delta\delta_1$, $\Delta\delta_2$ and $\Delta\delta_3$ are used to prolong or shorten the conduction of capacitors in H-bridge units H_1, H_2 and H_3, respectively. The final phase angles of three sinusoidal modulating waves, α_1, α_2 and α_3 are fed to the switching modulator, where phase-shifted PWM is used.

The complete controller shown in Figure 3-11 is one-phase based diagram. It should be emphasized that the *SMV Detector* and *Decoupling Power Controller* are the same for three phases.

3.4 Summary

In this chapter, the principle of a novel dc capacitor-voltage detection technique is investigated and the SMV detector is developed. With the detected dc capacitor-voltages as feedback signals, the feedback balance control method is proposed to ensure the balance of all individual H-bridge dc-voltages. The complete controller for the CHB-based STATCOM is presented in detail. Main contributions in this chapter are summarized as follows.

1) The novel dc-voltage detection technique, referred to as single multiple-voltage (SMV) detector, is developed to obtain dc capacitor-voltages. To balance dc capacitor-voltages, all individual H-bridge dc-voltages should be measured and controlled separately. The SMV algorithm is used to substantially reduce the number of voltage sensors. For example, in a nine-level CHB-based STATCOM, twelve voltage sensors are normally required. With the proposed SMV detection algorithm, only three voltage sensors are needed to obtain all individual H-bridge dc-voltages from measured inverter ac voltages. The CHB-based STATCOM system with the SMV detector is cost effective and less complex. The system reliability is enhanced as well. The developed dc-voltage detection technique can be extended to the STATCOM system with high level CHB inverter.

2) The new dc-voltage balance control method is proposed to assure well-balanced voltages across all capacitors in the CHB inverter. This method combines the phase shifting technique and sinusoidal pulse width modulation (SPWM) strategy for the dc-voltage balance control. PI regulators in all feedback control loops are identical. This feature makes the dc-voltage balance control easy to be implemented. With identical level of the

inverter dc-voltages, the voltage stress on switches in the inverter can be shared and the harmonic contents in the inverter output voltage can be reduced.

CHAPTER 4
COMPUTER SIMULATION

This chapter presents the computer simulation and verification of the proposed CHB-based STATCOM system. The simulation model in Simulink environment for the medium-voltage seven-level CHB-based STATCOM is developed. Extensive simulations of the STATCOM are performed to verify the proposed methods. Simulations can be classified into three categories: 1) steady-state operation of the STATCOM, 2) dynamic response to reactive power demand, and 3) response to dc-voltage balance control. To verify the effectiveness of the proposed methods for the STATCOM with high-level CHB inverter, simulations of the nine-level CHB-based STATCOM are performed and results are provided.

4.1 Simulation Model

The circuit diagram of a seven-level CHB-based STATCOM is shown in Figure 4-1, where a seven-level CHB inverter is connected to the ac system through the coupling inductor L. v_s and v_c are the system voltage and the inverter phase output voltage. i is the inverter current. v_{Hj} is the output voltage of the H-bridge H_j (j=1, 2, or 3). i_{dcj} and v_{dcj} are the capacitor current and voltage of the H-bridge H_j. A voltage sensor, represented by a block *CT*, is used to measure the inverter phase voltage and all individual dc-voltages v'_{dcj} (j=1, 2, or 3) can be obtained by the SMV detector. With the feedback signals and commands, the STATCOM controller generates gate signals for the CHB inverter. Based on the circuit diagram shown in Figure 4-1, the Simulink-based simulation model of a seven-level CHB-

based STATCOM is developed and the block diagram of simulation model is shown in Figure 4-2. The block *AC System* provides three-phase system voltage. The *CHB Inverter* block is a seven-level cascaded H-bridge inverter. The block *SMV Detector* detects all individual dc-voltages based on three-phase inverter output voltage. The *DC-Voltage Balance Controller* block functions to balance all individual dc-voltages and the *Decoupling Power Control* block controls the power exchange between the STATCOM and the ac system. The block *Switching Modulator* generates gate signals for switches in the inverter. Details of these blocks are discussed in the following subsections.

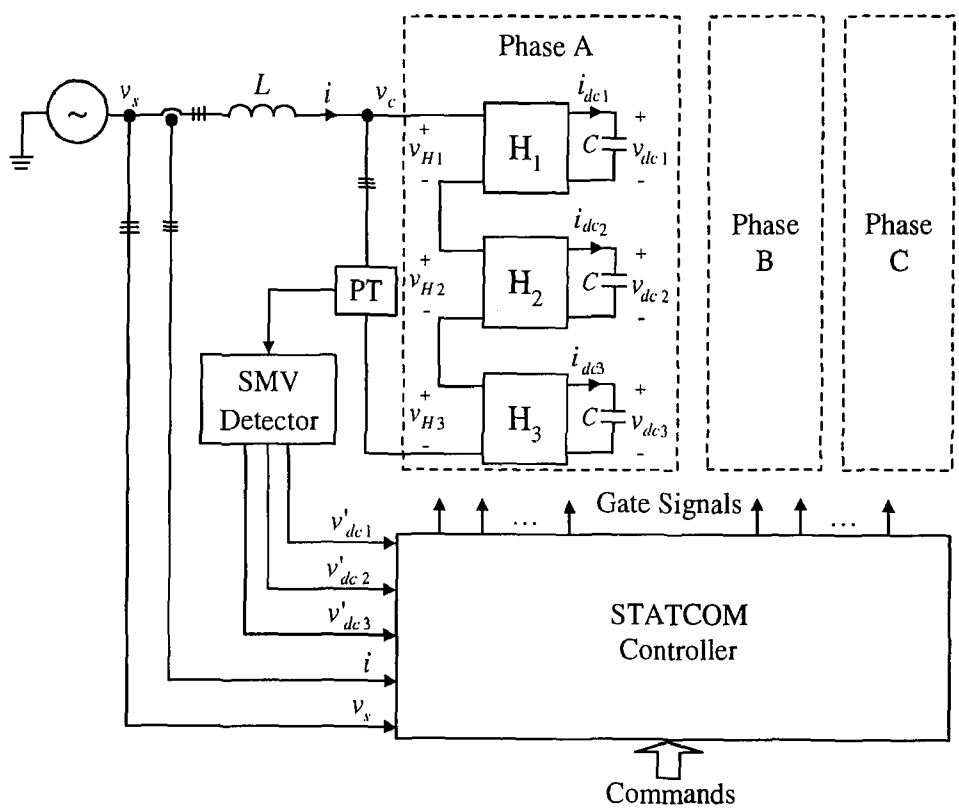


Figure 4-1. Circuit diagram of a seven-level CHB-based STATCOM.

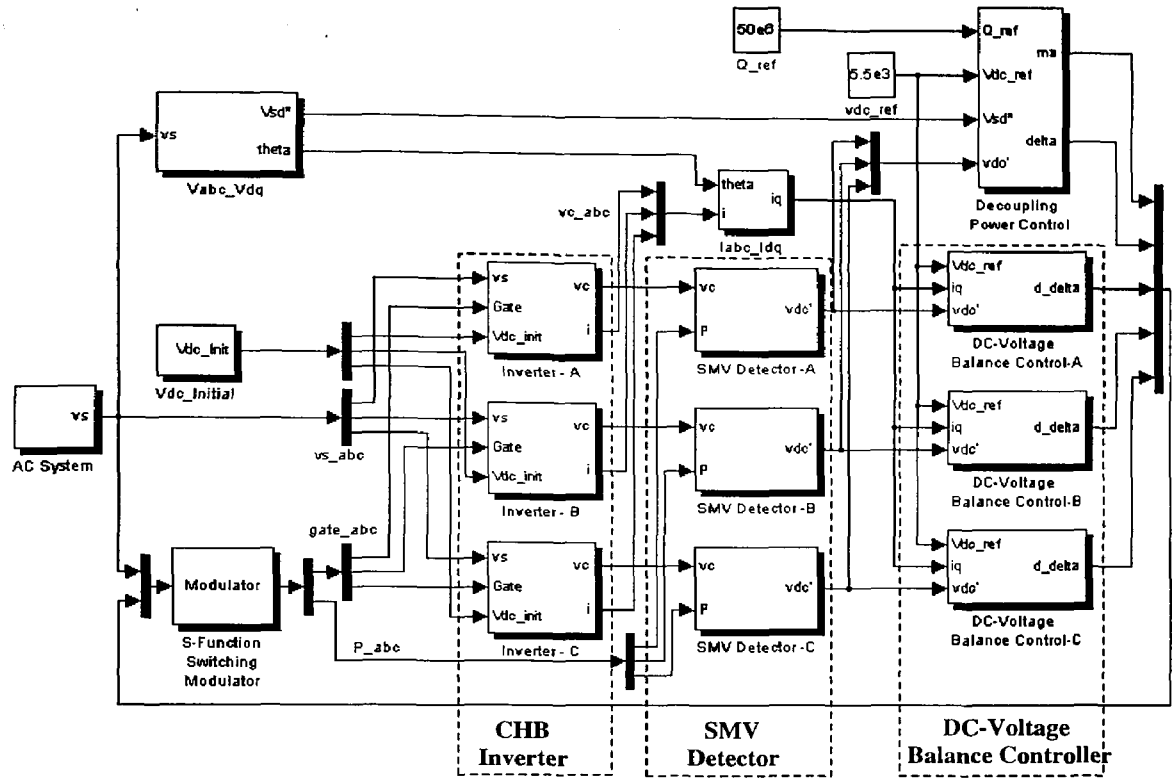


Figure 4-2. Simulink diagram of a seven-level CHB-based STATCOM.

Block Diagram of CHB Inverter

A simple way of building a CHB inverter is to drag and drop a *Universal Bridge* block and a capacitor from the Simulink Library. If doing so, the research regarding the response of unbalanced initial dc-voltage cannot be performed because the initial capacitor voltage cannot be preset. Alternatively, building a transfer-function based inverter model can solve this problem. This subsection develops a transfer-function based inverter model.

The equivalent one-phase STATCOM circuit and a seven-level CHB inverter can be described by equations (4.1) to (4.5).

$$v_s - v_c = \frac{di}{dt} \tag{4.1}$$

$$v_c = v_{H1} + v_{H2} + v_{H3} \tag{4.2}$$

$$\begin{cases} v_{H1} = SW_1 \cdot v_{dc1} \\ v_{H2} = SW_2 \cdot v_{dc2} \\ v_{H3} = SW_3 \cdot v_{dc3} \end{cases} \tag{4.3}$$

$$\begin{cases} v_{dc1} = \dfrac{1}{C}\int i_{dc1}(t)dt \\ v_{dc2} = \dfrac{1}{C}\int i_{dc2}(t)dt \\ v_{dc3} = \dfrac{1}{C}\int i_{dc3}(t)dt \end{cases} \tag{4.4}$$

$$\begin{cases} i_{dc1} = SW_1 \cdot i \\ i_{dc2} = SW_2 \cdot i \\ i_{dc3} = SW_3 \cdot i \end{cases} \tag{4.5}$$

where SW_j is the switching function of the H-bridge H_j. Based on the above equations, the simulink model of a seven-level cascaded inverter is developed and its one-phase diagram is shown in Figure 4-3. Input terminals are ac system voltage v_s, gate signals for switches and preset initial dc-voltages V_{dc_init}. Outputs are the inverter phase voltage v_c and current *i*. The switching function *SW* is obtained from a look-up table based on the gate signals.

Block Diagram of the SMV Detector

Based on the algorithm of SMV detector discussed in Section 3.3, its Simulink block is developed and shown in Figure 4-4. The first input terminal is the inverter voltage v_c and the second input is variable *R* obtained from the switching modulator. Outputs of this block are detected dc-voltages, represented by a vector $\mathbf{v'_{dc}}$.

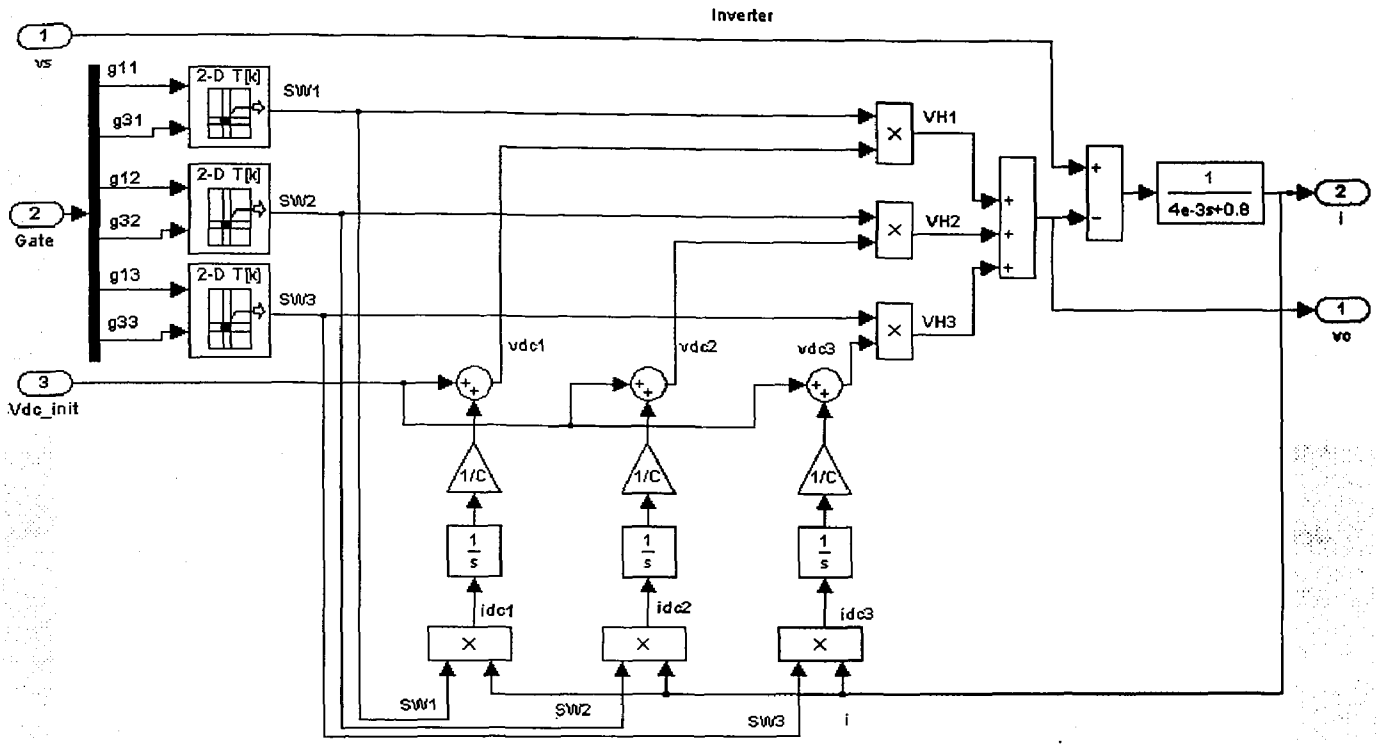


Figure 4-3. Block details of the seven-level CHB inverter.

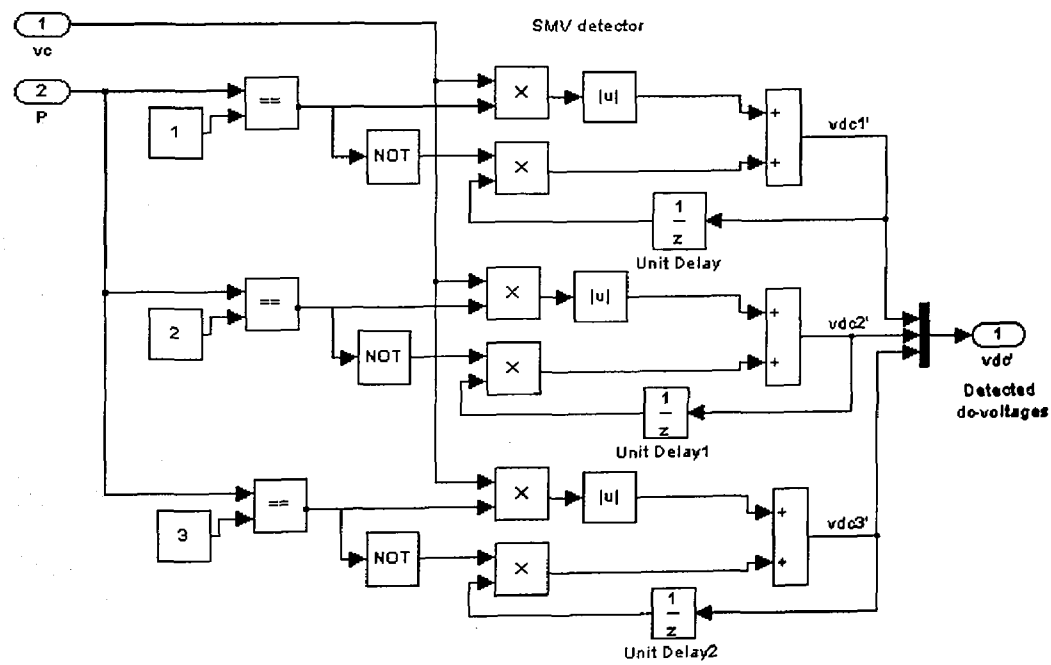


Figure 4-4. Block details of the SMV detector.

Block Diagram of the Decoupling Power Control

Based on the diagram in Figure 2-12, the Simulink block of the decoupling power control is developed and shown in Figure 4-5. The inputs of terminal $\mathbf{v'_{dc}}$ are individual dc-voltages detected from the SMV detector. The bold symbol represents a set of variables. Input terminals, V_{dc_ref} and $Q_{\_ref}$ ($I_q^* = Q_{ref} / V_s$), are references of total phase dc-voltage and reactive power. Input V_{sd}^* is the amplitude of system voltage. The block *Average Vdc* in Figure 4-5 calculates the average total dc-voltage of one phase v'_{dc_avg}. Output terminals, *delta* and m_a, are calculated from equations (2.17) and (2.18), respectively.

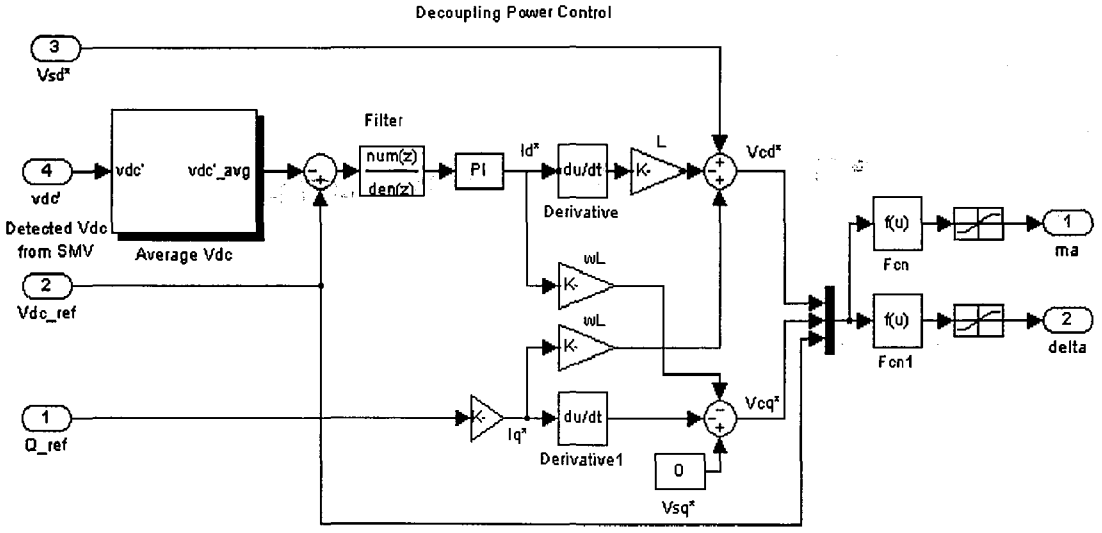


Figure 4-5. Block details of decoupling power control.

Block Diagram of DC-Voltage Balance Control

Based on the individual dc-voltage balance control scheme discussed in Section 3.2.3, the Simulink block of dc-voltage balance control is developed and shown in Figure 4-6. The input terminal, i_q, is obtained from the block *Iabc-Idq*, which converts three-phase currents to two-phase dq currents according to frame transformation equation (2.10). As discussed in Section

3.2.3, if i_q is greater than 0, the STATCOM operates in the capacitive mode and D is 1; if i_q is less than 0, the STATCOM operates in the inductive mode and D is -1; if i_q is equal to 0, the STATCOM operates in the standby mode and D is 0. Inputs of V_{dc_ref} and $\mathbf{v'_{dc}}$ are the total dc-voltage reference and detected individual dc-voltages. Outputs are the desired phase shifts of three modulating waves, corresponding to $\Delta\delta$ in Figure 3-10.

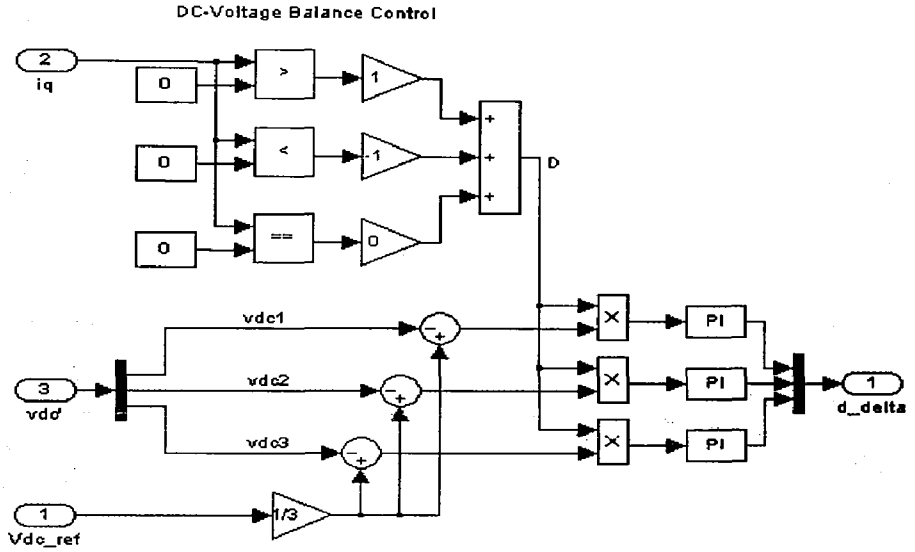


Figure 4-6. Block details of individual dc-voltage balance control.

Block Diagram of Switching Modulator

The block *Switching Modulator* in Figure 4-2 is a s-function based block developed to generate gate signals for switches in the inverter and determine the value of *R*. Inputs of this s-function block are system voltage v_s and control variables fed by the decoupling power controller and the dc-voltage balance controller, including modulating index (m_a), phase difference between the inverter voltage and system voltage (δ) and phase shift angles of modulating waves of H-bridges in three phases ($\boldsymbol{\Delta\delta}$, the bold symbol represents a shift-angle

vector). Outputs are gate signals for three-phase H-bridges and the value of R. Detailed Matlab-programming codes of this s-function block is illustrated in Appendix A.

4.2 Simulation Results of the Seven-Level CHB-based STATCOM

In this section, results obtained from the following simulations are provided: 1) steady-state operation of the proposed STATCOM, 2) dynamic response to variation of reactive power demand, and 3) response of dc-voltage balance control. Simulation system specifications of the seven-level CHB-based STATCOM are listed in Table 4-1. The term of full-capacitive mode is defined in this thesis when the STATCOM provides rated leading reactive power, $+Q$. The term of full-inductive mode is defined when the STATCOM provides rated lagging reactive power, $-Q$. Half-capacitive mode and half-inductive mode are defined when the STATCOM provides half rated leading and lagging reactive power; $\pm Q/2$. The standby mode is defined when the STATCOM provides no reactive power. All waveforms in this chapter are in per unit (p.u.).

Table 4-1 Specification of a seven-level CHB-based STATCOM

AC source voltage: $V = 13.8\,kV$	Reactive power rating : $Q = \pm 50MVar$
Current rating: $I = 2.1kA$	DC voltage reference: $V_{dc\_ref} = 5.5kV$
Coupling inductance: $L = 4mH$	DC capacitance: $C = 12mF$
Switching frequency: $f_{SW} = 600Hz$	

4.2.1 Steady-State Operation of the STATCOM

The steady-state operations of the seven-level CHB-based STATCOM in the full-capacitive mode and full-inductive mode are presented in this subsection.

Figure 4-7 shows the steady-state one-phase waveforms of system voltage v_s, inverter voltage v_c and current i, and dc-voltages v_{dcj} (j=1, 2,or 3) in the full-capacitive mode. In Figure 4-7 (a), the inverter voltage v_c shapes PWM wave with seven levels. The amplitude of v_c is maximum. The inverter current i is rated and leading the system voltage v_s by about 90^0. The invert current and the system voltage are not exactly 90^0 because of active power exchange. It is verified that the STATCOM operates steadily in the full-capacitive mode. Figure 4-7 (b) shows dc-voltages of three H-bridges, v_{dc1}, v_{dc2} and v_{dc3}. It can be seen that dc-voltages are balanced when the STATCOM operates in the full-capacitive mode. The ripple of dc-voltage in the full-capacitive mode is 0.08 p.u.

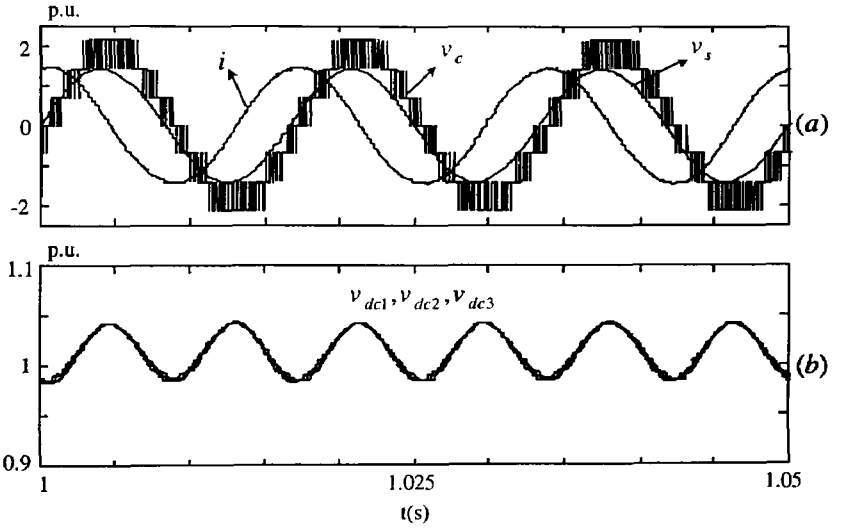


Figure 4-7. The steady state operation of seven-level CHB-based STATCOM in the full-capacitive mode.

Figure 4-8 shows the steady-state one-phase waveforms of v_s, v_c, i and v_{dcj} (j=1, 2 or 3) in the full-inductive mode. In Figure 4-8 (a), the inverter voltage v_c shapes PWM wave with five levels. The amplitude of v_c is minimum. The inverter current i is rated and lagging the system voltage v_s by about 90^0. Figure 4-8 (b) shows v_{dc1}, v_{dc2} and v_{dc3}. It is verified that dc-

voltages are balanced when the STATCOM operates in the full-inductive mode. The ripple of dc-voltage in the full-inductive mode is 0.04 p.u.

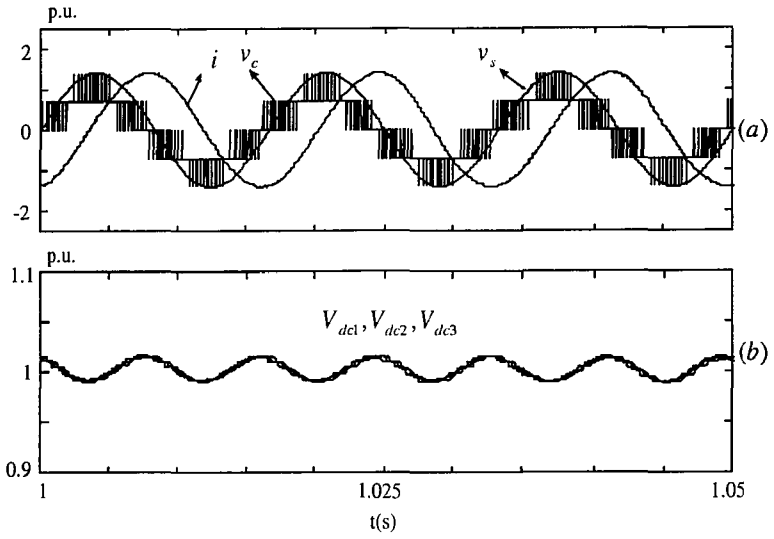


Figure 4-8. The steady state operation of seven-level CHB-based STATCOM in the full-inductive mode.

Figure 4-9 shows three-phase inverter voltages and currents of the STATCOM operating in the full-capacitive mode. It can be seen from waveforms that inverter voltages and currents are three-phase balanced.

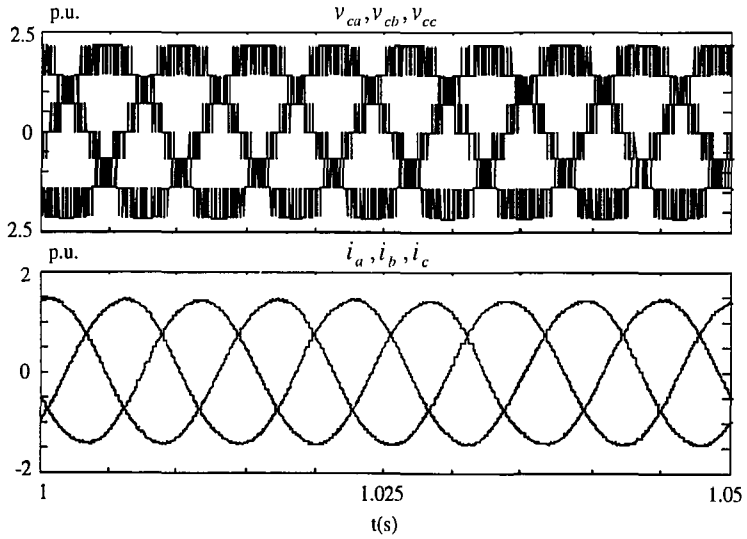


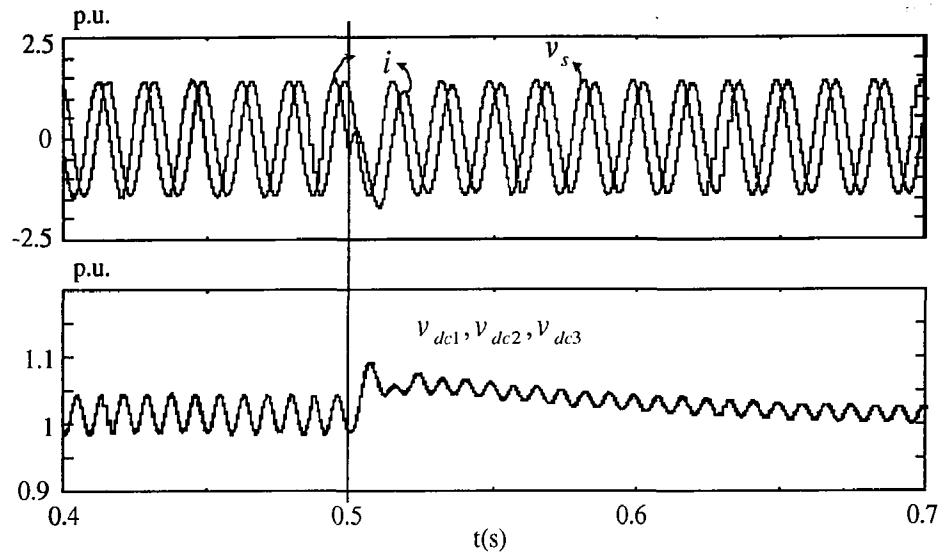
Figure 4-9. Three-phase voltages and currents of the seven-level CHB-base STATCOM.

4.2.2 Dynamic Response to Reactive Power Demand

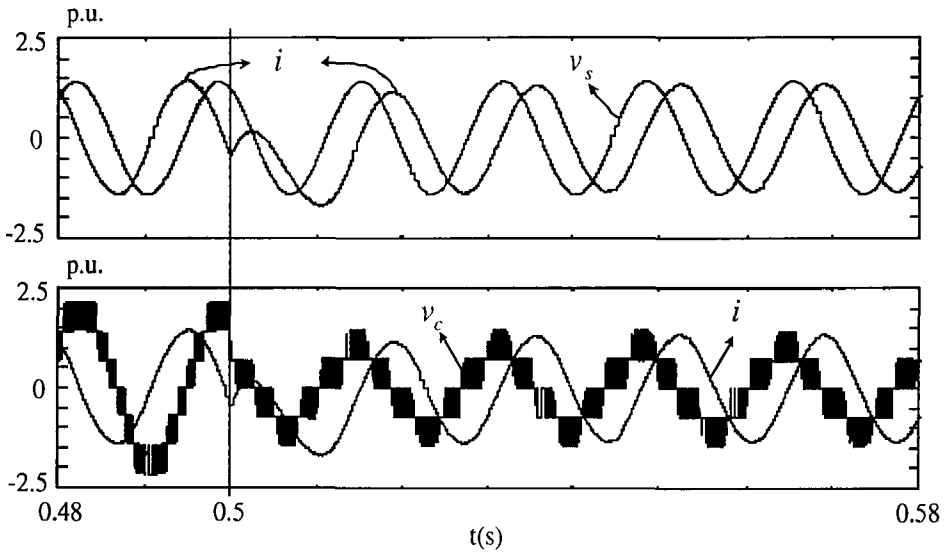
In this section, simulations of the proposed STATCOM changing among different operating modes are performed to investigate the dynamic performance of the CHB-based STATCOM. Simulation waveforms of v_s, v_c, i and v_{dc} in one phase are provided.

Figure 4-10 shows dynamic responses as the proposed STATCOM changes from full-capacitive mode to full-inductive mode at 0.5s. In Figure 4-10 (a), the inverter current i leads and lags v_s by about 90^0 before and after 0.5s. The current amplitude is 1 p.u. in both modes. It is verified that the STATCOM operates in the full-capacitive mode and then the full-inductive mode before and after the transition. Dc capacitor voltages, v_{dc1}, v_{dc2} and v_{dc3}, are balanced in two modes. Details of the transition in Figure 4-10 (a) are shown in Figure 4-10 (b). Simulation results demonstrate the extremely fast dynamic response of the proposed STATCOM. Reactive power transition can be completed within 2 cycles. Three-phase currents are shown in Figure 4-10 (c). It can be seen that the current is three-phase balanced both before and after the transition.

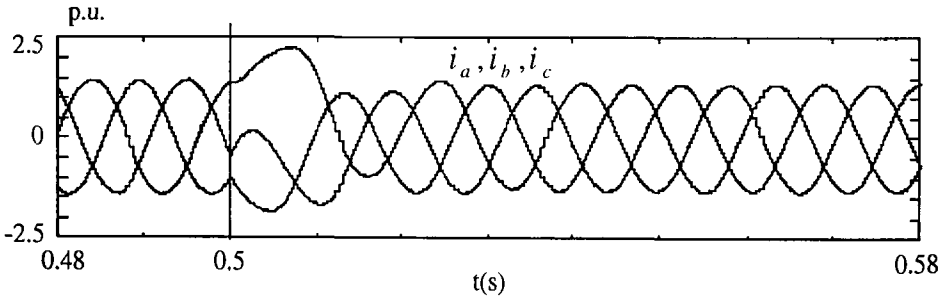
The dynamic response as the STATCOM changes from the standby mode to full-capacitive mode at 0.3s is shown in Figure 4-11, where all waveforms are the same as those in Figure 4-10. Similar conclusions can be made that the reactive power transition is completed within 2 cycles and all dc-voltages are balanced. More simulation results of dynamic response to reactive power demand are shown in Appendix C.



(a)

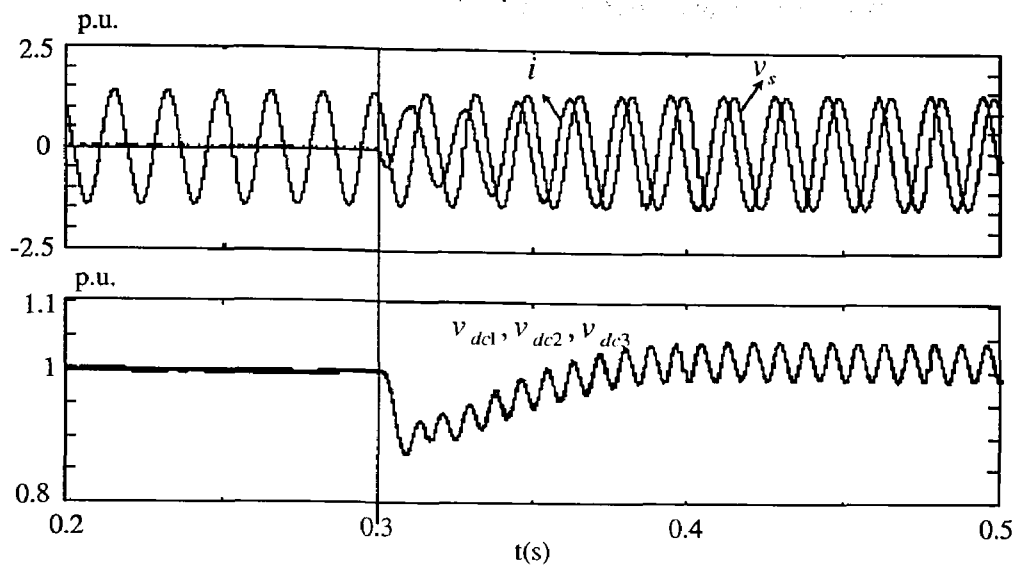


(b)

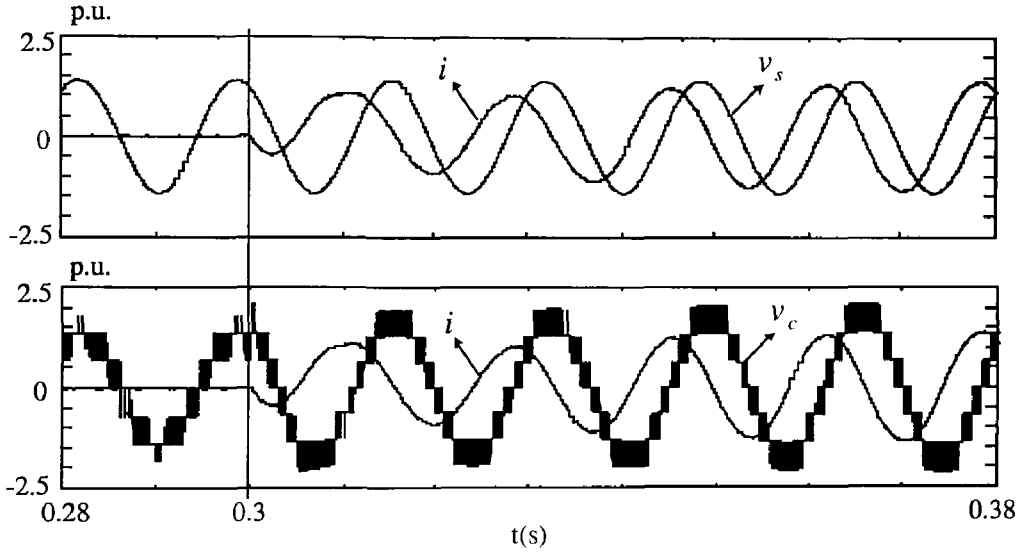


(c)

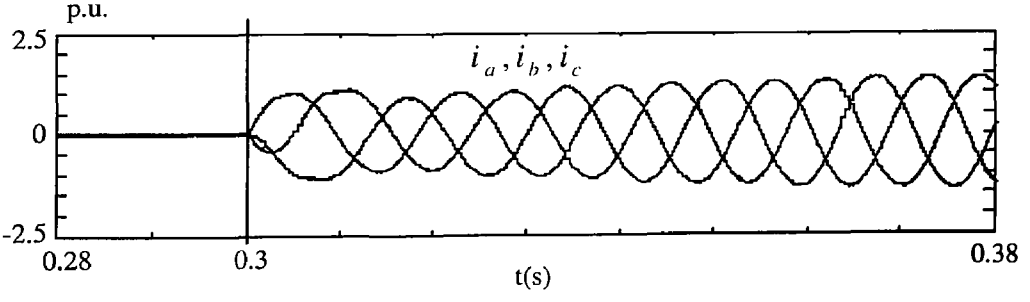
Figure 4-10. The seven-level CHB-based STATCOM responses the step change from full-capacitive mode to full-inductive mode at 0.5s, (a) i, v_s and $v_{dc1}, v_{dc2}, v_{dc3}$, (b) details of (a), (c) i_a, i_b, i_c.



(a)



(b)



(c)

Figure 4-11. The seven-level CHB-based STATCOM responses the step change from standby to full-capacitive mode at 0.3s, (a) i, v_s and $v_{dc1}, v_{dc2}, v_{dc3}$, (b) details of (a), (c) i_a, i_b, i_c.

Figure 4-12 shows three-phase inverter voltages, currents and system voltages as the STATCOM changes from full-capacitive mode to full-inductive mode at 0.5s. Results demonstrate that conclusions obtained from one-phase waveforms in Figure 4-10 are valid for three phases. Figure 4-13 shows all nine dc-voltages in the group of a) the same phase and b) the same level as the STATCOM changes from full-capacitive mode to full-inductive mode at 0.5s. With the dc-voltage control, dc capacitor-voltages of all three levels and three phases are identical as expected.

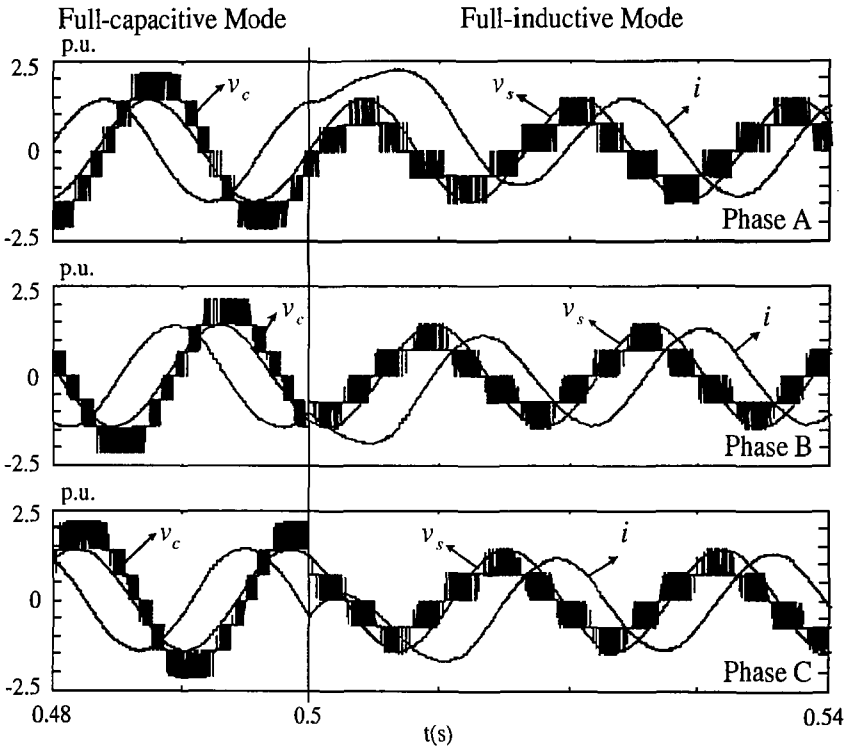
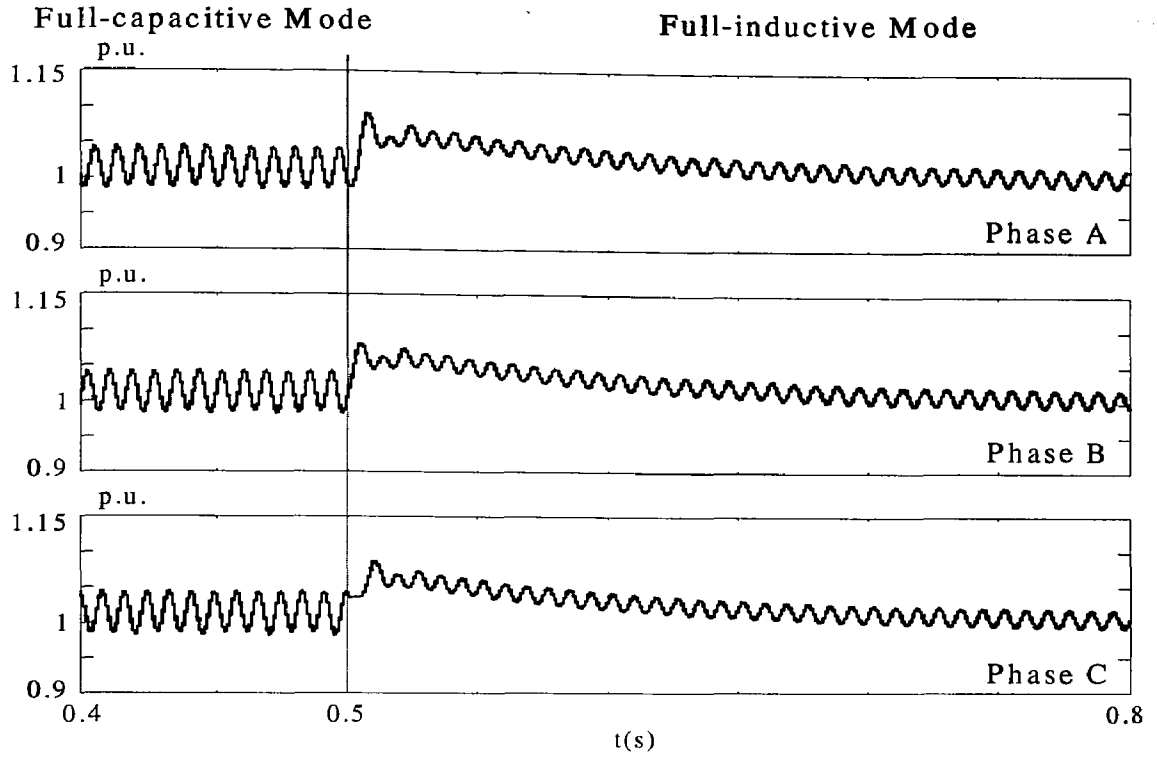
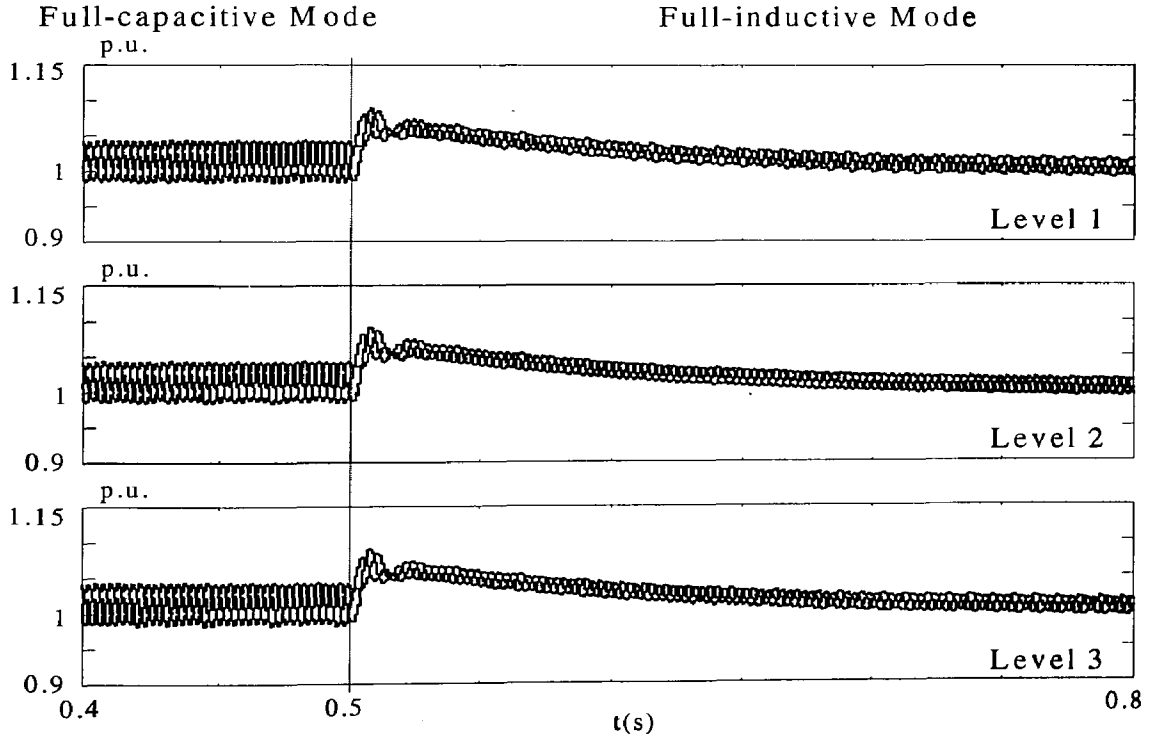


Figure 4-12. System voltage and inverter output voltage and current.



(a)



(b)

Figure 4-13. All nine capacitor dc-voltages in group of (a) the same phase and (b) the same level.

4.2.3 Response of DC-Voltage Balance Control

To verify the proposed dc-voltage balance control, simulations of the STATCOM operating under such conditions as unbalanced power losses in H-bridges, asymmetric charged initial dc-voltages and unbalanced system voltages are performed. Waveforms of all dc-voltages in groups of the same phase and the same level are provided.

Response to Unbalanced Power Losses in H-bridges

The responses of dc-voltages to the unbalanced power losses in H-bridges of one leg are shown in Figure 4-14, where there are three parts: I, II and III. Waveforms in Figure 4-14 (a), v_{dc1}, v_{dc2} and v_{dc3}, are dc-voltages of three H-bridges in phase A, and the waveform in Figure 4-14 (b) is the sum of three individual dc-voltages. Information of Figure 4-14 is tabulated in Table 4-2. The power loss of an H-bridge is realized in simulations by shunt-connecting a resistance to the dc capacitor in the H-bridge. It can be concluded that with the balance control, individual dc-voltages can be well balanced under the condition of unbalanced power loss.

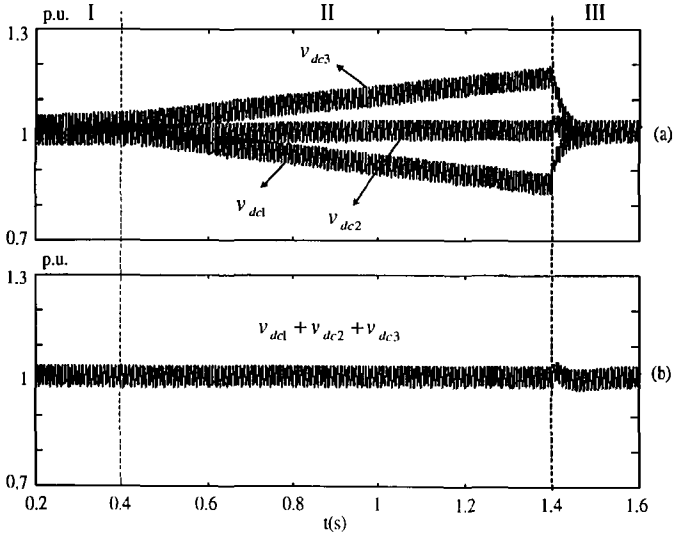


Figure 4-14. The response of the dc-voltages to the unbalanced power loss (a) individual dc-voltages, (b) sum of dc-voltages.

Table 4-2 Response of dc-voltage to unbalanced power loss in H-bridges

Part	Balance of power loss in H-bridges	Use of balance control	Balance of dc-voltages
I	Yes	Yes	Yes
II	No	No	No
III	No	Yes	Yes

Response to Asymmetric Charged Initial DC-Voltages

Figure 4-15 shows the response of dc-voltage balance control to asymmetric charging which may occur when capacitors are initially charged by ac system during starting up the STATCOM. Waveforms in Figure 4-15 (a) are dc capacitor-voltages of three H-bridges in phase A, and the waveform in Figure 4-15 (b) is the sum of three individual dc-voltages. Three initially charged dc-voltages are preset to be 1.2, 1 and 0.8 per unit, respectively. Results show that unequal dc-voltages caused by asymmetric charging can be well equalized by the individual dc-voltage balance control, while the total dc-voltage is regulated to the reference by the total dc-voltage regulation control.

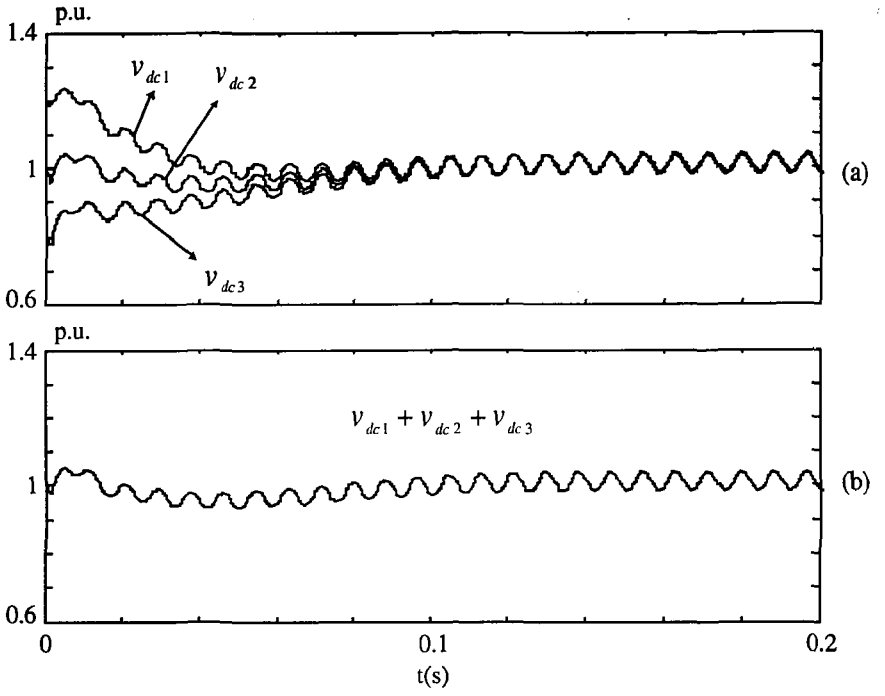
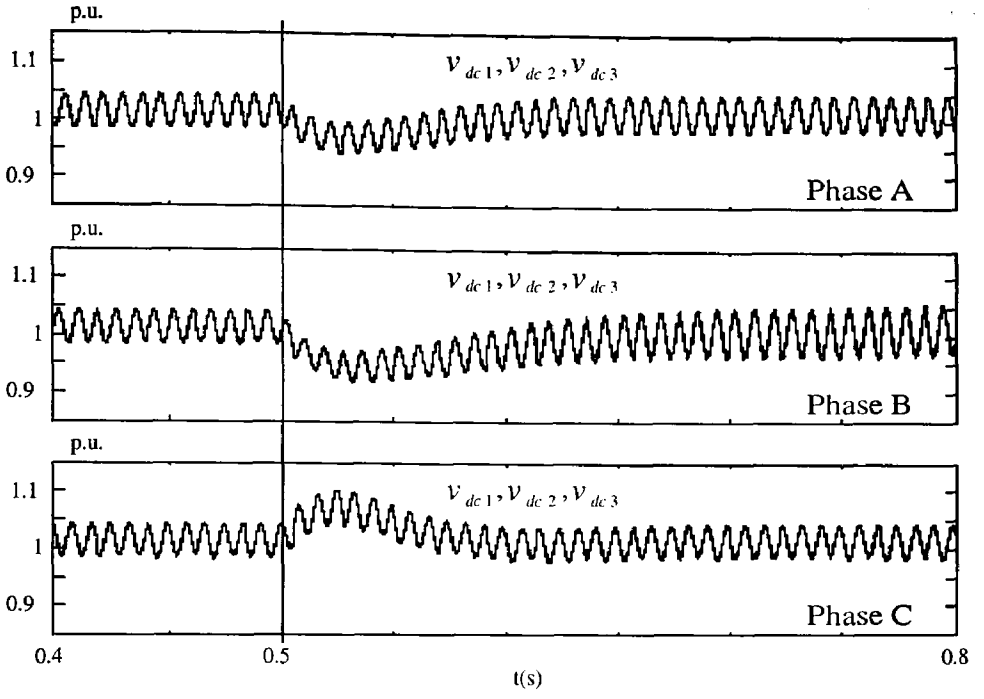


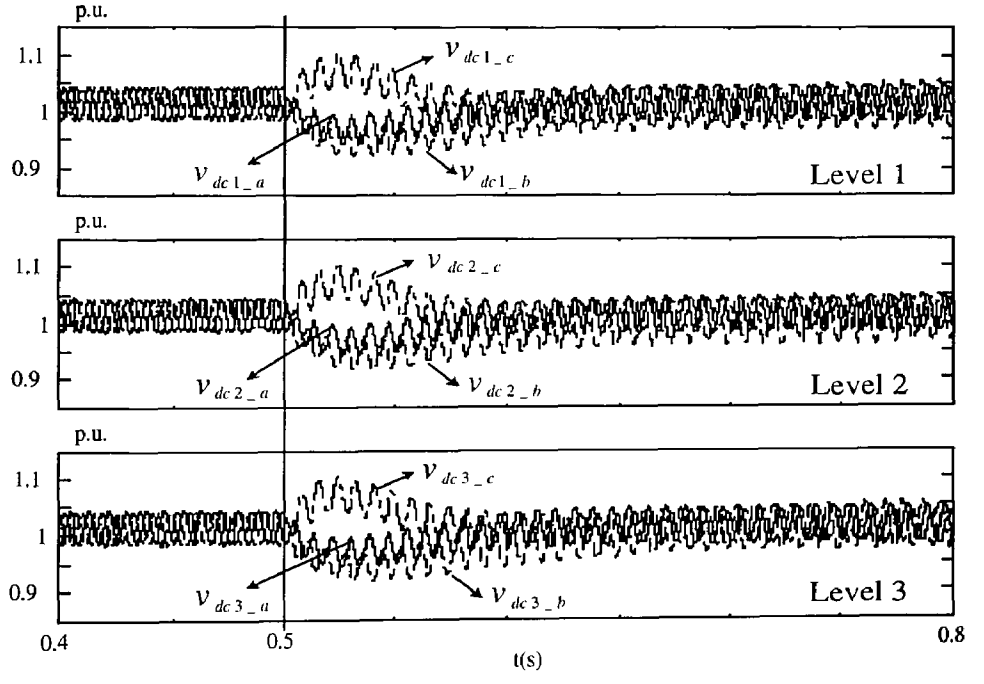
Figure 4-15. The response of the dc-voltages to the unbalanced initial charged capacitor voltages (a) individual dc-voltages, (b) sum of dc-voltages.

Response to Unbalanced System Voltages

The response of dc-voltage balance control to unbalanced system voltages is shown in Figure 4-16. The system voltage changes from balanced to unbalanced state at 0.5s. The unbalanced system voltages are: V_{sa} =1.5p.u., V_{sb} =1.87p.u. and V_{sc} =0.4p.u. Dc-voltages in Figure 4-16 are in the group of a) the same phase and b) the same level. It is verified that dc capacitor-voltages of all three levels and three phases are identical as expected.



(a)



(b)

Figure 4-16. The response of the dc-voltages to the unbalanced system voltages (a) dc-voltages in the group of phase, (b) dc-voltages in the group of level.

4.3 Conclusions

In this chapter, the performance of the CHB-based STATCOM and the proposed methods are verified by computer simulation. The simulation model in Simulink environment for the seven-level CHB-based STATCOM is developed. One of the unique features of this model lies in its ability to preset the initial dc voltage level for the H-bridge inverters. This feature allows the dc capacitor to be pre-charged to any given voltage level, which greatly facilitates the dynamic analysis of the dc capacitor voltage control for the H-bridge inverters. Based on comprehensive simulations, the following conclusions can be made:

1) The proposed STATCOM operates steadily over the full operating range of the system and responds to the leading and lagging reactive power commands rapidly.

2) Individual dc capacitor voltages can be balanced not only in each phase of the STATCOM system but also in each H-bridge unit.

3) The developed SMV detector can detect all H-bridge dc-voltages based on three-phase inverter output voltages. The technique can be extended to the STATCOM with higher-level CHB inverter.

CHAPTER 5
EXPERIMENTAL VERIFICATION

This chapter presents the experimental performance verification of the proposed CHB-based STATCOM system. A prototype of the low-power five-level CHB-based STATCOM is built up based on the dSPACE prototyping system. The configuration of the experimental set-up (both hardware and software platform) is described in detail. Details of the dSPACE integrated hardware/software implementation for the proposed STATCOM are presented. Experimental results are provided to verify the steady-state operation of the STATCOM, the accuracy of the SMV detector and the effectiveness of dc-voltage balance control.

5.1 Hardware Implementation

The dSPACE based hardware configuration of the five-level CHB-based STATCOM is shown in Figure 5-1. The *AC System* provides three-phase system voltage. The *Five-Level CHB Inverter*, the voltage source inverter of the STATCOM, is connected to the ac system through the coupling inductor. v_{dc1} and v_{dc2} are dc-voltages of H-bridges H_1 and H_2 in one phase. The coupling inductor L is used as a reactive power coupler, as well as an inverter output current filter. *CB* is the circuit breaker. The *STATCOM Controller* in this set-up is a dSPACE DS1103 board functioning the algorithm execution and the real-time control. The interface between the STATCOM controller and the CHB inverter are *CP1103 I/O Panel* and *Gate-Signal Conditioning Board*. The *CP1103 I/O Panel* provides inputs and outputs for the

STATCOM controller and easy-to-use connection for the oscilloscope. The *Gate-Signal Conditioning Board* provides ready-to-use gate signals for switches in the inverter. Details of main blocks in Figure 5-1 are presented as follows.

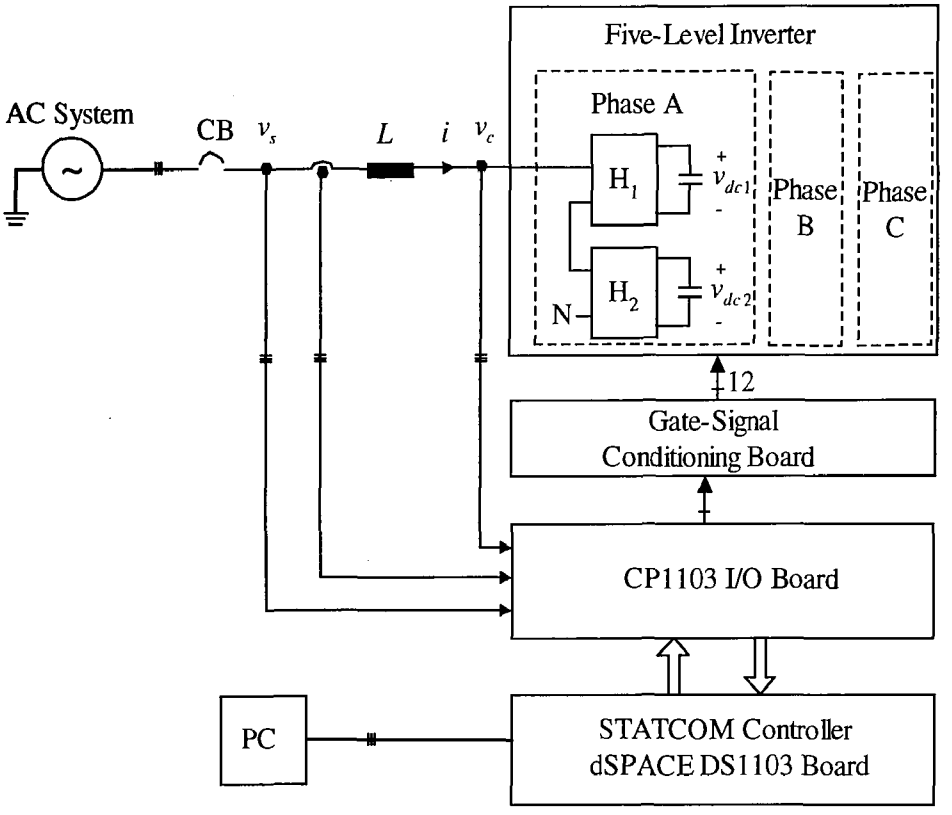


Figure 5-1. Hardware implementation of the five-level CHB-based STATCOM.

The *Five-Level CHB Inverter* consists of six H-bridge units. The schematic of an H-bridge unit is shown in Figure 3-2. Two half-bridge 600V/50A IGBTs from Siemens are combined as a single H-bridge unit. Two pieces of gate driver boards from VPT Inc. are used to drive the IGBTs in each H-bridge.

The *STATCOM Controller* is a dSPACE DS1103 board inserted in a Pentium PC. The microprocessor of DS1103 board is Motorola PowerPC 604e/333MHz, which provides a fast

processing for floating point calculations and makes real-time control possible. Control algorithms are programmed in Matlab/Simulink environment. PC compiles the software of control algorithms and downloads it into the DS1103 board. The DS1103 board executes the downloaded instructions and realizes the real-time control.

The *CP1103 I/O Board* of the set-up provides easy-to use connections between the DS1103 board and devices to be connected to it. The CP1103 panel provides inputs and outputs for the DS1103 board. The measurements are acquired via the CP1103 panel, fed into the DS1103 board and transformed to digital signals by ADCs. Digital PWM gate signals are transformed to analog ones by DACs and outputted via CP1103 panel.

The *Gate-Signal Conditioning Board* produces dead time for gate signals and sends ready-to-use gate signals to gate driver boards. Another function of gate-signal conditioning board is to shift the PWM voltage level from 10V (the voltage level of PWM signals from dSPACE DS1103 board) to 15V (the required voltage of the gate driver board).

5.2 Simulink-Based Diagram for Experiment

In this section, the software diagram of the dSPACE based implementation for the five-level CHB-based STATCOM system is described. The software platform to implement control algorithms is the commercial package Simulink. A merit of using dSPACE controller is that the dSPACE Real-Time Interface (RTI) can effectively converts MATLAB/Simulink diagrams into dSPACE assembly instructions. The off-line Simulink simulations are to be implemented on a real-time frame. All the code generation and downloading tasks are

performed automatically. In this way, the need for hand-written code is eliminated. This function provides a short cut to implement a Simulink based control algorithm and expedites the prototyping process substantially. The Simulink based diagram for the experiment is developed based on the simulation model diagram shown in Figure 4-1. Modifications to the simulation model are needed when the Simulink diagram is going to be transferred to dSPACE instructions. The implemented Simulink block diagram is shown in Figure 5-2.

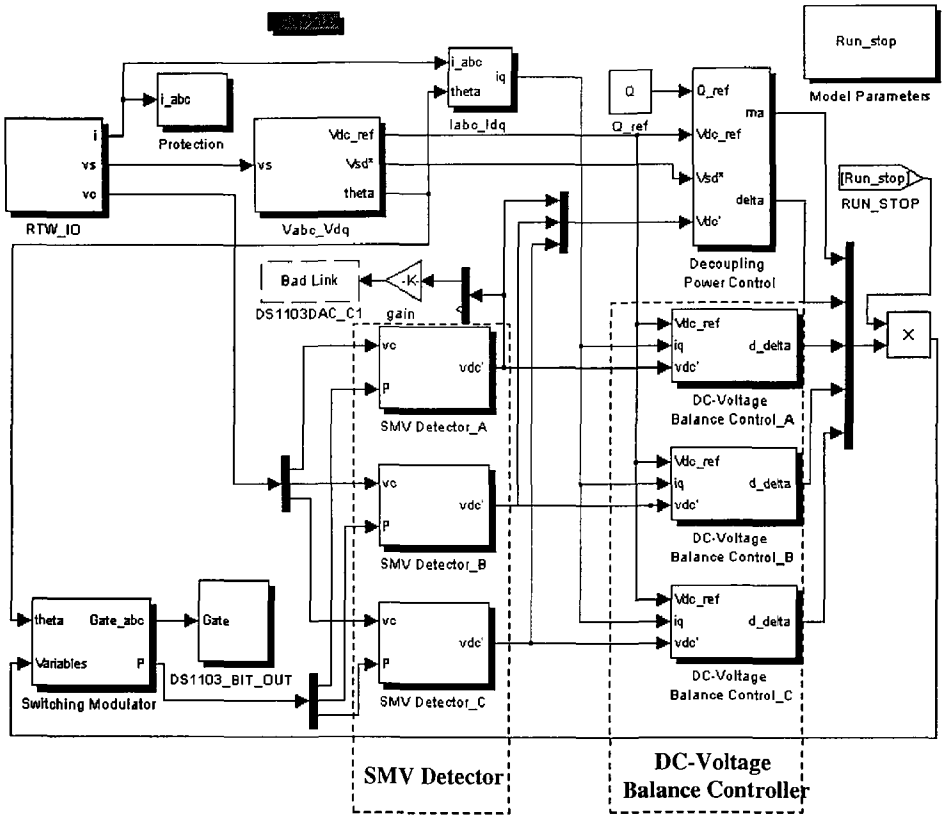


Figure 5-2. Experimental Simulink diagram of the five-level CHB-based STATCOM.

The *RTW_IO* block in Figure 5-2 is the Real-Time Workshop IOs for the STATCOM system. The *RTW_IO* block includes seven ADCs and functions of collecting three-phase system voltages v_s, line currents i, and inverter output voltages v_c.

The *Protection* block functions the current protection for the system. Once the measured current is greater than the limit value preset inside the block, the gate signals for switches will be disabled.

The *Vabc_Vdq* block is basically a PLL and provides the system voltage in d-axis ($V_{sd}^{*} = V_s$) and dc-voltage reference ($V_{dc\_ref} = 1.5 \cdot \sqrt{2} \cdot V_s$) where V_s is the rms amplitude of the system phase voltage. The *Iabc_Idq* block transforms the current components from the abc frame to dq frame and outputs reactive current component i_q to the dc-voltage balance controller. The abc-dq transformation is based on equation (2.10).

Blocks of *Decoupling Power Control*, *SMV Detector* and *DC-Voltage Balance Control* are the same as those in simulation model, as shown in Figure 4-1. The *DS1103DAC_C1* block transforms the digital-based detected dc-voltage of the first H-bridge in phase A into an analog signal that can be captured by the oscilloscope. In this way, the comparison of the actual and the detected dc-voltage can be performed and the accuracy of the developed SMV detector could be evaluated.

The *Switching Modulator* block provides gate signals for the five-level CHB inverter, and outputs the value of *R*. Details of a *Gating* sub-block are shown in Figure 5-4. Signals cr_1, cr_2, $cr_{1\_}$ and $cr_{2\_}$ are four triangular carrier waves. The input m_a is the modulation index of the sinusoidal modulating wave. The phase angle of the sinusoidal wave for each H-bridge, α_j (j=1 or 2), is the sum of inputs *theta* (θ), *delta* (δ) and *d_delta* ($\Delta\delta_j$,). The modulating

scheme is phase-shifted PWM as discussed in Section 2.2.1. Details of *Determination of R* block are shown in Figure 5-5, where H_1 and H_2 blocks generate the value of *R* for two H-bridges in one phase, respectively. The principle of determining *R* can be referred to Table 3-3.

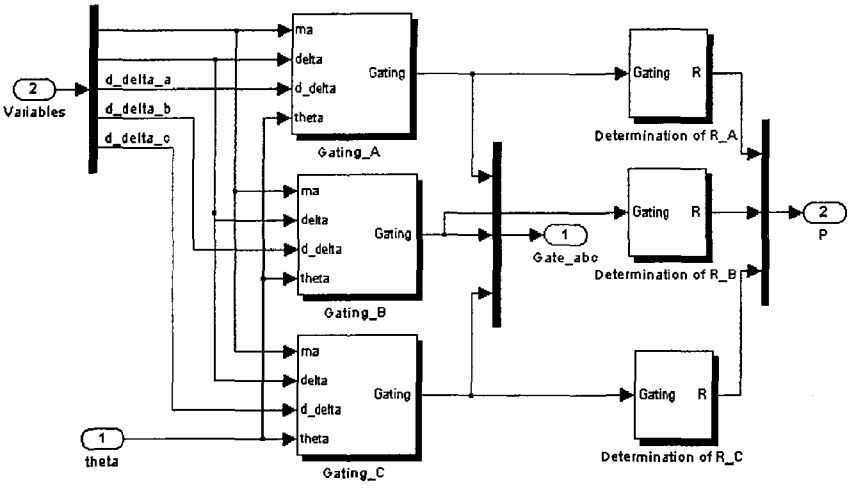


Figure 5-3. Block details of switching modulator.

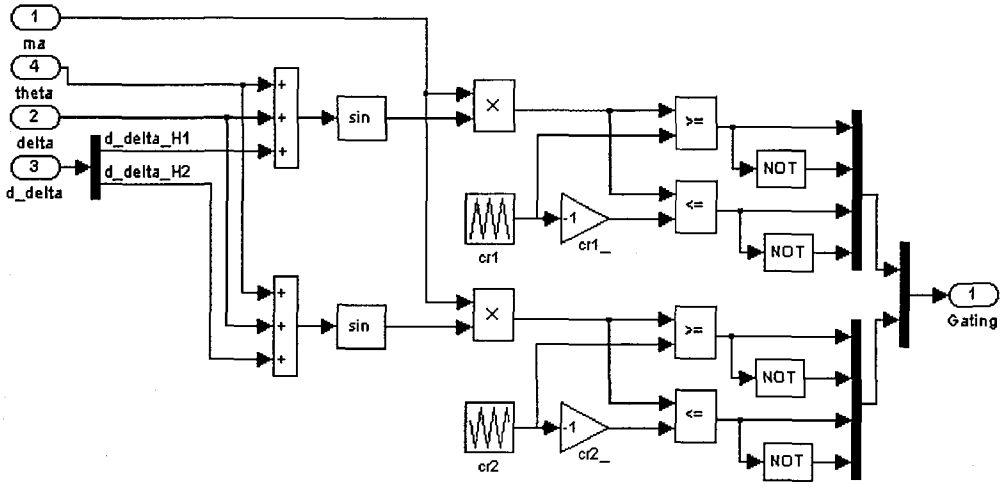


Figure 5-4. Details of *Gating* sub-block in Fig.5-3.

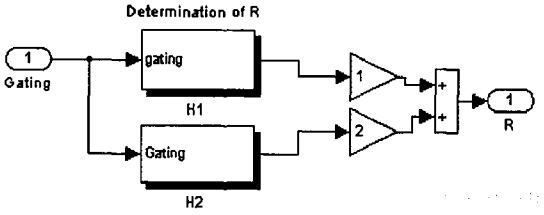


Figure 5-5. Details of *Determination of P* block in Fig.5-3.

The *DS1103_BIT_OUT* block transform the digital gating signals to analog ones and output the analog gating signals to the CP1103 I/O panel.

5.3 Experimental Results

Based on the methods proposed in this thesis, experiments are performed to verify the performance of the CHB-based STATCOM system. Experimental results are provided in this section to validate the steady-state operation of the STATCOM, the accuracy of the SMV detector and the effectiveness of dc-voltage balance control.

The experimental system specification of the five-level CHB-based STATCOM is listed in Table 5-1. The total dc-voltage reference V_{dc_ref} is selected to be 1.5 times of the peak system phase voltage. The capacitance is selected to keep the ripple dc-voltage ΔV_{dc} (peak-to-peak value of v_{dc}) within ten percent of V_{dc_ref} and small enough to assure the accuracy of the developed SMV detector. The coupling inductance is selected to be larger than the usual value in industry (0.1 p.u. of rated inductance) due to the consideration of the sensitiveness of reactive power control. The amount of reactive power exchanging between the ac system and the STATCOM, $Q = \frac{V_s \Delta V}{X_L}$, is controlled by the voltage drop ΔV across the inductor. If the coupling inductance is small, reactive power control will be too sensitive to the voltage drop. In this set-up, the coupling inductance is 0.18 per unit.

Table 5-1 Set-up specification of a five-level CHB-based STATCOM

AC system voltage: V =122V	Var rating : $Q = \pm 1.5kVar$
Current rating: I =7A	DC voltage reference: V_{dc_ref} = 150V
Coupling inductance: L=5mH	DC capacitance: C=7mF
Switching frequency: f_{SW} =600Hz	

5.3.1 Steady-State Performance of the STATCOM

The steady-state experimental results of the five-level CHB-based STATCOM in the full-capacitive mode and full-inductive mode are provided.

Figure 5-6 shows the inverter voltage and current of the STATCOM operating in the full-capacitive mode. In Figure 5-6, *Channel 1* is the inverter voltage and *Channel M1* is the inverter current. The inverter current leads the inverter voltage by about 90^0 and the peak value of leading current is rated value of 10A. Figure 5-7 shows the inverter voltage and current of the STATCOM operating in the full-inductive mode. Likewise, the *Channel 1* is the inverter voltage and *Channel M1* is the inverter current. The inverter current lags the inverter voltage by about 90^0 and the peak value of lagging current is rated value of 10A. The inverter voltage shapes in PWM waves with 5-level and 3-level, and the amplitude of the inverter voltage is maximum and minimum in the capacitive and inductive mode, respectively. It is verified from experimental results that the STATCOM can operate steadily and shows superior performance during the whole range of reactive power generation (from full-capacitive to full-inductive mode).

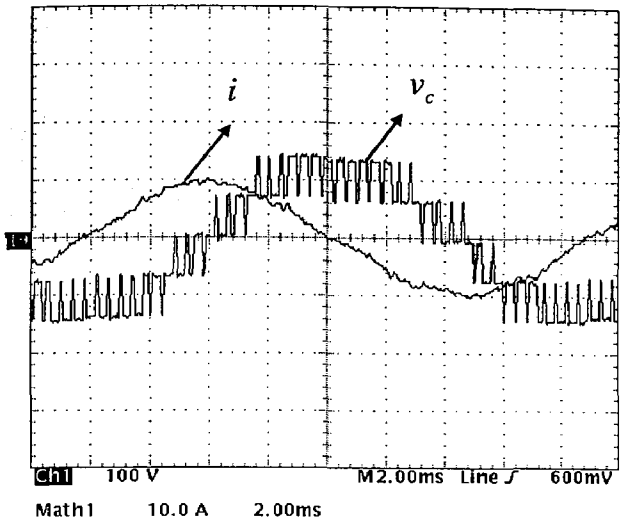


Figure 5-6. Inverter output voltage and current in the full-capacitive mode.
Ch1: Inverter voltage, v_c, 100*V*/div
M1: Inverter current, *i*, 10*A*/div

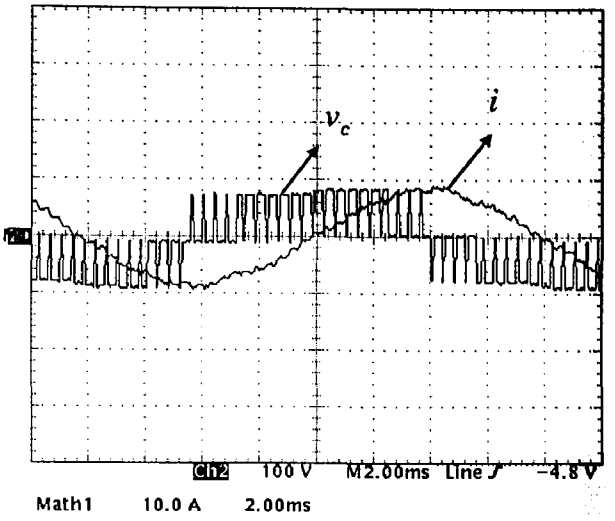


Figure 5-7. Inverter output voltage and current in the full-inductive mode.
Ch1: Inverter voltage, v_c, 100*V*/div
M1: Inverter current, *i*, 10*A*/div

5.3.2 SMV Detector Accuracy Test

The SMV detector accuracy tests for the proposed dc-voltage detection technique are presented in this subsection. The accuracy test of the SMV detector is based on the diagram shown in Figure 5-2. The dc-voltage of the first H-bridge in phase *A* from SMV detector is used as an example to be the detected dc-voltage. This signal is obtained based on the dc-voltage detection algorithm proposed in Section 3.2. The DS1103DAC_C1 block transforms the digital-based detected dc-voltage into an analog signal that could be captured by the oscilloscope connecting to the CP1103 panel. To test the accuracy of SMV detector, the dc-voltage detected from the SMV detector, actual dc-voltage and the error are captured by the oscilloscope simultaneously. Waveforms of these three signals are shown in Figure 5-8, 5-9, 5-10 and 5-11 when the STATCOM operates in the full-capacitive, half-capacitive, half-inductive and full-inductive modes, respectively. In these figures, *Channel 1* is the detected

dc-voltage v_{dc_det}, *Channel 2* is the actual dc-voltage v_{dc_act} and *Math1* is the error $v_{dc\_det} - v_{dc\_act}$ (ac component). The average steady-state dc-voltage errors in the full-capacitive, half-capacitive, half-inductive and fill-inductive modes are 1.2, 1.1, 1.5 and 2V, respectively. Above results are listed in Table 5-2, where the individual dc-voltage reference $V_{dc\_ref\_indiv}$ is 75V. The maximum error rate is 2.6% which is acceptable in most engineering applications.

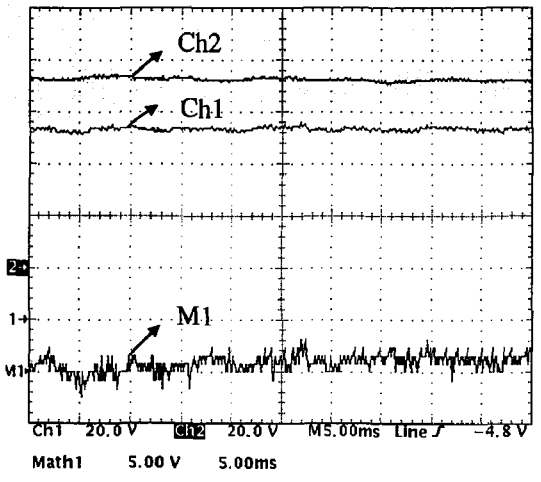


Figure 5-8. Comparison of detected and actual dc-voltages in the full-capacitive mode.
Ch1: v_{dc_det}, 20V/div
Ch2: v_{dc_act}, 20V/div
M1: $v_{dc\_det} - v_{dc\_act}$, 5V/div

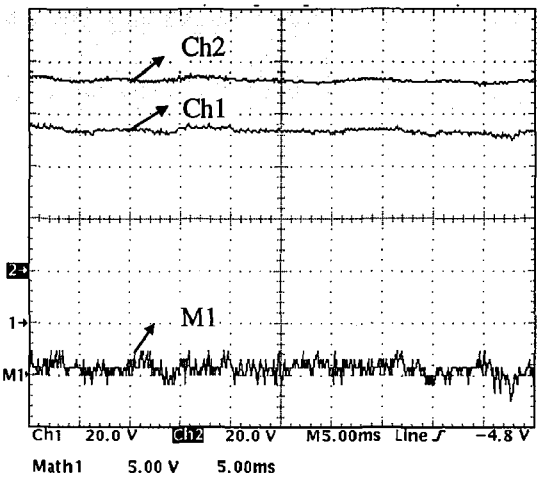


Figure 5-9 Comparison of detected and actual dc-voltages in the half-capacitive mode.
Ch1: v_{dc_det}, 20V/div
Ch2: v_{dc_act}, 20V/div
M1: $v_{dc\_det} - v_{dc\_act}$, 5V/div

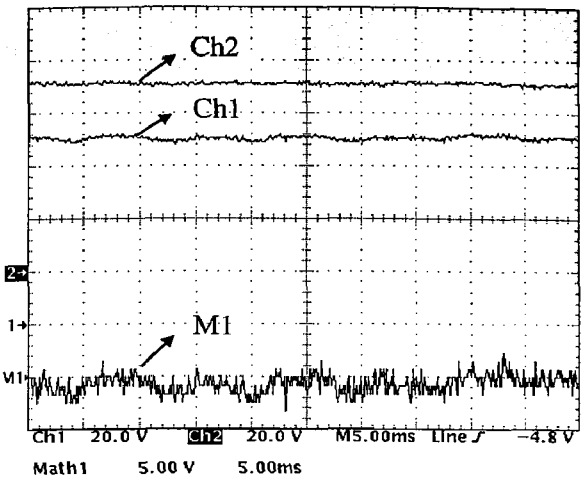


Figure 5-10. Comparison of detected and actual dc-voltages in the half-inductive mode.
Ch1: v_{dc_det}, 20V/div
Ch2: v_{dc_act}, 20V/div
M1: $v_{dc\_det} - v_{dc\_act}$, 5V/div

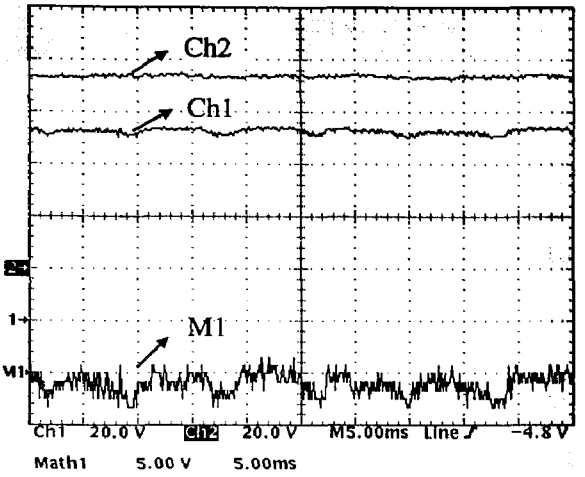


Figure 5-11 Comparison of detected and actual dc-voltages in the full-inductive mode.
Ch1: v_{dc_det}, 20V/div
Ch2: v_{dc_act}, 20V/div
M1: $v_{dc\_det} - v_{dc\_act}$, 5V/div

Table 5-2 Error analysis of dc voltage in the experiment

Operation mode	Full-capacitive mode	Half-capacitive Mode	Half-inductive mode	Full-inductive mode
Average dc-voltage error (V) $\lvert V_{dc\_act} - V_{dc\_det} \rvert$	1.2	1.1	1.5	2
Average dc-voltage error rate $\frac{\lvert V_{dc\_act} - V_{dc\_det} \rvert}{V_{dc\_ref\_indiv}} \times 100\%$	1.6	1.47	2	2.6

5.3.3 DC-Voltage Balance Test

The dc-voltage balance tests for the proposed dc-voltage balance control are presented in this subsection. Experimental results of the STATCOM operating in the full-capacitive and full-inductive modes are provided.

DC-Voltage Balance Test in the Full-Capacitive Mode

To verify the dc-voltage balancing, all six dc-voltage waveforms of the STATCOM operating in the full-capacitive mode are shown in Figure 5-12, 5-13 and 5-14, respectively. The dc-voltages in these figures are grouped in the same phase. In these three figures, *Channel 1* and *Channel 2* represent dc-voltages of the first and the second H-bridges in each phase. It is verified that all dc-voltages are balanced when the STATCOM operates in the full-capacitive mode.

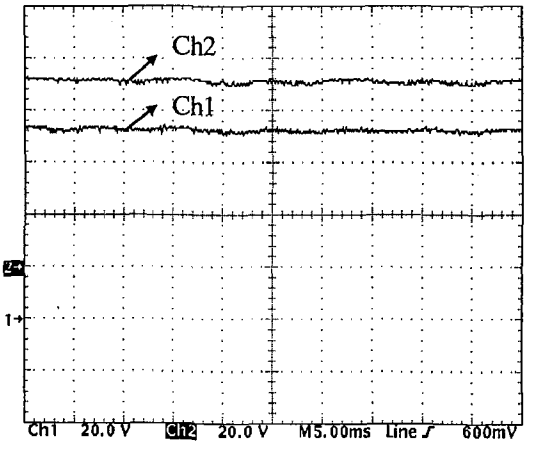


Fig.5-12 DC-voltages of phase A in the full-capacitive mode
Ch1: dc-voltage of the first H-bridge, v_{dc1}, 20V/div
Ch2: dc-voltage of the second H-bridge, v_{dc2}, 20V/div

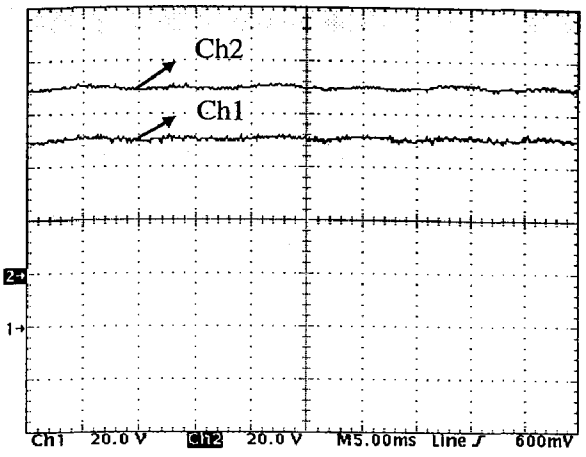


Figure 5-13. DC-voltages of phase B in the full-capacitive mode.
Ch1: dc-voltage of the first H-bridge, v_{dc1}, 20V/div
Ch2: dc-voltage of the second H-bridge, v_{dc2}, 20V/div

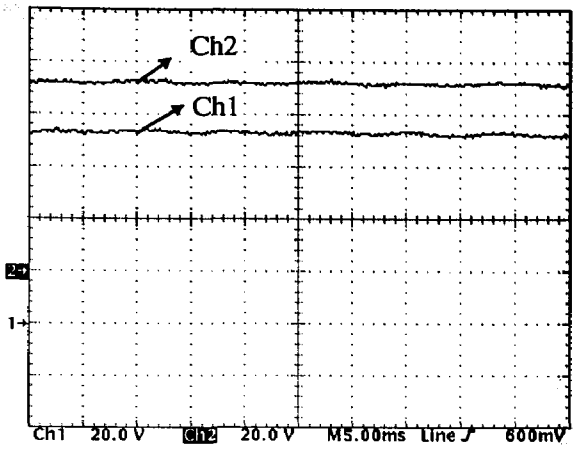


Figure 5-14. DC-voltages of phase C in the full-capacitive mode
Ch1: dc-voltage of the first H-bridge, v_{dc1}, 20V/div
Ch2: dc-voltage of the second H-bridge, v_{dc2}, 20V/div

DC-Voltage Balance Test in the Full-Inductive Mode

All six dc-voltage waveforms of the STATCOM operating in the full-inductive mode are shown in Figure 5-15, 5-16 and 5-17, respectively. Likewise, the dc-voltages in these figures are grouped in the same phase. From experimental results, all dc-voltages are balanced when the STATCOM operates in the full-inductive mode.

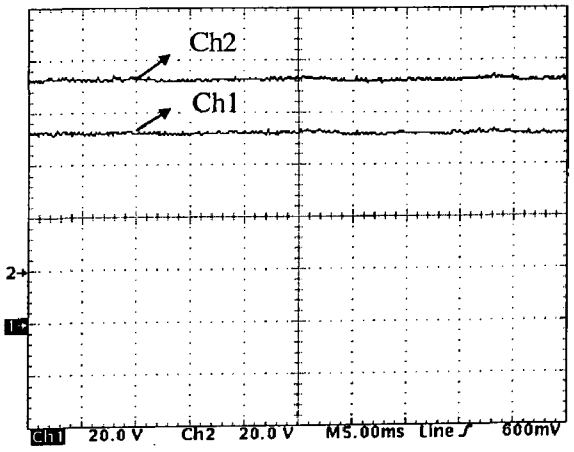


Fig.5-15 DC-voltages of phase A in the full-inductive mode
Ch1: dc-voltage of the first H-bridge, v_{dc1}, 20V/div
Ch2: dc-voltage of the second H-bridge, v_{dc2}, 20V/div

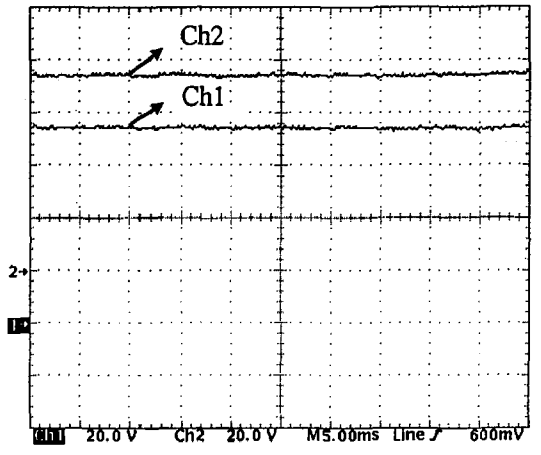


Figure 5-16. DC-voltages of phase B in the full-inductive mode.
Ch1: dc-voltage of the first H-bridge v_{dc1}, 20V/div
Ch2: dc-voltage of the second H-bridge v_{dc2}, 20V/div

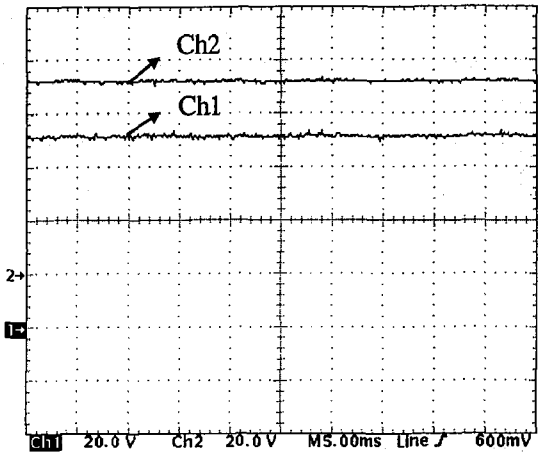


Figure 5-17. DC-voltages of phase C in the full-inductive mode
Ch1: dc-voltage of the first H-bridge v_{dc1}, 20V/div
Ch2: dc-voltage of the second H-bridge v_{dc2}, 20V/div

5.4 Conclusions

The proposed control algorithms for the CHB-based STATCOM system are experimentally verified in this chapter. The prototype of a five-level CHB-based STATCOM is constructed in the laboratory based on the dSPACE prototyping system. Experiments are classified into three categories: 1) steady-state performance of the CHB-based STATCOM system, 2) the effectiveness and the accuracy of the SMV detector, and 3) individual dc-voltage balance control. Based on the experimental results, the following conclusions can be made:

1) The proposed STATCOM system operates steadily and shows superior performance over the full operating range of the system.

2) With the proposed SMV algorithm, all individual H-bridge dc-voltages can be obtained from the measured inverter output voltage. Only three voltage sensors are needed such that the number of voltage sensors is substantially reduced. From the experimental results, the maximum error of the SMV detector with0.in the full operating range of the STATCOM is 2.6%, which is acceptable in practice.

3) Individual dc-voltages can be well balanced based on the proposed dc-voltage balance control method. Individual dc-voltages are balanced not only in each phase of the STATCOM system but also in each H-bridge inverter.

CHAPTER 6
CONCLUSIONS

It has been recognized that the transmittable power flowing through transmission lines could be increased and the voltage profile along the transmission line could be controlled by an appropriate amount of compensated reactive power. The STATCOM is a shunt-connected reactive power compensation device that is capable of generating or absorbing reactive power. In addition, the STATCOM can improve transient stability and damp power oscillations during a post-fault event. Using high-speed semiconductor switching technique, the STATCOM can rapidly respond to dynamic system events. Instead of directly deriving reactive power from the energy-storage components, the STATCOM basically circulates power with connected network. The reactive components used in the STATCOM, therefore, can be much smaller. The key component of STATCOM is voltage source inverter (VSI). Among various multilevel VSI topologies, the cascaded H-bridge (CHB) multilevel inverter is a promising topology for the STATCOM application due to its modular structure and high operating voltage without switches in series.

In this thesis, the analysis, control, simulation and experimental verification of the CHB-based STATCOM system have been presented. The system configuration and operating principle of the CHB-based STATCOM have been discussed. Decoupling power control method has been proposed to control both active and reactive power exchange between the

STATCOM and the ac system. A novel dc capacitor voltage detection technique has been developed to detect individual H-bridge dc-voltages. A new dc capacitor-voltage balance control method has been proposed to balance the voltage across all capacitors. The main contributions of the thesis are summarized as follows.

1) **A novel dc capacitor-voltage detection technique, referred to as single multiple-voltage (SMV) algorithm, has been developed.** To balance dc capacitor voltages, all individual dc-voltages should be measured and controlled separately. The proposed SMV algorithm can be used to substantially reduce the number of voltage sensors. For example, in a nine-level CHB-based STATCOM, twelve voltage sensors are normally required. With the proposed SMV detection algorithm, only three voltage sensors are needed to obtain all individual H-bridge dc-voltages from measured inverter ac voltages. The SMV algorithm can detect individual H-bridge dc-voltages accurately. The maximum error of the SMV algorithm within the full operating range of the STATCOM system is around 2.6%, which is acceptable in practice. The CHB-based STATCOM system with the SMV detector is cost effective and less complex. The system reliability is enhanced as well. The developed dc-voltage detection technique can be extended to the STATCOM system with high level CHB inverter.

2) **A new dc capacitor voltage balance control method has been proposed.** This method combines the phase shifting technique and sinusoidal pulse width modulation (SPWM) strategy for the control of H-bridge dc voltages. PI regulators in all feedback control loops can be identical. This feature makes the dc-voltage balance control easy to be

implemented. Individual dc capacitor voltages can be balanced not only in each phase of the STATCOM system but also in each H-bridge unit. With identical level of the inverter dc voltages, the voltage stress on switches in the inverter can be shared and the harmonic contents in the inverter output voltage can be reduced.

3) **Simulink model for the dynamic and steady state analysis of the CHB-based STATCOM has been established.** The Simulink model provides a useful tool to investigate the dynamic and steady state performance of the STATCOM system. One of the unique features of the model lies in its ability to preset the initial dc voltage level for the H-bridge inverters. This feature allows the dc capacitor to be pre-charged to any given voltage level, which greatly facilitates the dynamic analysis of the dc capacitor voltage control for the H-bridge inverters.

4) **The proposed control algorithms for the CHB-based STATCOM system have been experimentally verified.** A laboratory prototype of the low-power five-level CHB-based STATCOM was constructed. The prototype is controlled by the dSPACE rapid prototyping system. Experiments are performed to verify the steady-state operation of the proposed STATCOM, the accuracy of the SMV detection algorithm and the effectiveness of dc capacitor-voltage balance control.

Future Work

1) The parameters of dc-voltage controllers were manually adjusted based on trial-and-error method in this thesis. A model of the STATCOM system is required to design controller parameters.

2) This thesis presented computer simulations for the dynamic performance of the CHB-based STATCOM system. Experimental verification of the dynamic performance of the STATCOM is suggested.

APPENDIX A

S-FUNCTION CODES OF SWITCHING MODULATOR FOR SEVEN-LEVEL CHB INVERTER

```
%This s-function program generates gating signals for a 7-level H-bridge cascaded inverter.
% The modulation scheme is Phase- Shifted PWM
% The author is Yidan Li

function [sys,x0,str,ts] = sv_ref(t,x,u, flag, f_fund, fcr )
% This is for reference vector generation
% parameters:  (speed, mi)
%         f_fund--- Hz, fundamental frequency
%         ma    ---  0 ~ 1, modulation index
%         fcr   ---  carrier frequency

switch flag,
 % Initialize the states, sample times, and state ordering strings.
 case 0
  [sys,x0,str,ts]=mdlInitializeSizes(fcr);
 case 2
  sys=mdlUpdate(t,x,u,f_fund, fcr);
 case 3
  sys=mdlOutputs(t,x,u,fcr);
 case {1, 4, 9 }
  sys=[];
 otherwise
  error(['Unhandled flag = ',num2str(flag)]);
end

%=============================================================================
% mdlInitializeSizes, flag=0
%=============================================================================
function [sys,x0,str,ts] = mdlInitializeSizes(fcr)

sizes = simsizes;
sizes.NumContStates  = 0;
sizes.NumDiscStates  = 39;
sizes.NumOutputs     = 39;     % dynamically sized
sizes.NumInputs      = 13;     % inputs of s-function, dynamically sized
sizes.DirFeedthrough = 0;      %  has direct feedthrough
sizes.NumSampleTimes = 2;

sys = simsizes(sizes);
str = [];
x0  = zeros(1,39);
ts  = [0, 0; 1e-5,0];              %  inherited sample time
%=============================================================================
% mdl discrete state, flag=2
%=============================================================================
function sys=mdlUpdate(t,x,u,f_fund,fcr);
% u(1) is the modulation index ma, adjusting the inverter's output
```

```
% u(2) is the control variable for total Vdc in phase A, controlling the phase angle between Vsa and Vca .
% u(3),u(4),u(5) are control variables for Vdc1,Vdc2,Vdc3 of phase A
% u(6) is the control variable for total Vdc in phase B, controlling the phase angle between Vsb and Vcb.
% u(7),u(8),u(9) are control variables for Vdc1,Vdc2,Vdc3 of phase B
% u(10) is the control variable for total Vdc in phase C, controlling the phase angle between Vsc and Vcc.
% u(11),u(12),u(13) are control variables for Vdc1,Vdc2,Vdc3 of phase C
% u(3),...u(13) are all in radian.

ma=u(1);
a_delta =u(2);
a_delta_1=u(3); a_delta_2=u(4);  a_delta_3=u(5);
b_delta =u(6);
b_delta_1=u(7); b_delta_2=u(8);  b_delta_3=u(9);
c_delta =u(10);
c_delta_1=u(11); c_delta_2=u(12); c_delta_3=u(13);

% Modulation index
if ( ma >= 0 ) & ( ma <= 1 )
   ma = ma;
else
   ma = 1;
end

%Modulating sine wave
V_modu_A_1=ma*sin( 2*pi*f_fund*t + a_delta + a_delta_1 );
V_modu_A_2=ma*sin( 2*pi*f_fund*t + a_delta + a_delta_2 );
V_modu_A_3=ma*sin( 2*pi*f_fund*t + a_delta + a_delta_3 );

V_modu_B_1=ma*sin( 2*pi*f_fund*t - 2*pi/3 + b_delta + b_delta_1 );
V_modu_B_2=ma*sin( 2*pi*f_fund*t - 2*pi/3 + b_delta + b_delta_2 );
V_modu_B_3=ma*sin( 2*pi*f_fund*t - 2*pi/3 + b_delta + b_delta_3 );

V_modu_C_1=ma*sin( 2*pi*f_fund*t + 2*pi/3 + c_delta + c_delta_1 );
V_modu_C_2=ma*sin( 2*pi*f_fund*t + 2*pi/3 + c_delta + c_delta_2 );
V_modu_C_3=ma*sin( 2*pi*f_fund*t + 2*pi/3 + c_delta + c_delta_3 );

%Carrier triangular wave (PHASE SHIFTED SPWM)
t_in_onecycle=mod(t,1/fcr);
%V_cr1:
if t_in_onecycle < 0
   Carrier_1=0;
elseif t_in_onecycle <= 1/fcr/2
   Carrier_1=4*fcr*t_in_onecycle-1;
elseif t_in_onecycle <= 1/fcr
   Carrier_1=-4*fcr*t_in_onecycle+3;
end
%V_cr2:
if t_in_onecycle < 0
   Carrier_2=0;
elseif t_in_onecycle <= 1/fcr/3
   Carrier_2=-4*fcr*t_in_onecycle+1/3;
elseif t_in_onecycle <= 5/fcr/6
   Carrier_2=4*fcr*t_in_onecycle-7/3;
elseif t_in_onecycle <= 1/fcr
   Carrier_2=-4*fcr*t_in_onecycle+13/3;
end
```

```
%V_cr3:
if t_in_onecycle < 0
   Carrier_3=0;
elseif t_in_onecycle <= 1/fcr/6
   Carrier_3=4*fcr*t_in_onecycle+1/3;
elseif t_in_onecycle <= 2/fcr/3
   Carrier_3=-4*fcr*t_in_onecycle+5/3;
elseif t_in_onecycle <= 1/fcr
   Carrier_3=4*fcr*t_in_onecycle-11/3;
end

V_cr1  = Carrier_1;
V_cr1_f=-Carrier_1;
V_cr2  = Carrier_2;
V_cr2_f=-Carrier_2;
V_cr3  = Carrier_3;
V_cr3_f=-Carrier_3;


%Switching signal generation for phase A, B, C

[S11_a, S31_a, S12_a, S32_a, S13_a, S33_a]=Carrier_gating_7(V_modu_A_1, V_modu_A_2, V_modu_A_3,
V_cr1, V_cr2, V_cr3, V_cr3_f, V_cr2_f, V_cr1_f);
[S11_b, S31_b, S12_b, S32_b, S13_b, S33_b]=Carrier_gating_7(V_modu_B_1, V_modu_B_2, V_modu_B_3,
V_cr1, V_cr2, V_cr3, V_cr3_f, V_cr2_f, V_cr1_f);
[S11_c, S31_c, S12_c, S32_c, S13_c, S33_c]=Carrier_gating_7(V_modu_C_1, V_modu_C_2,
V_modu_C_3 ,V_cr1, V_cr2, V_cr3, V_cr3_f, V_cr2_f, V_cr1_f);

%phase a
sys(1)=S11_a; sys(2)=not(S11_a); sys(3)=S31_a; sys(4)=not(S31_a);
sys(5)=S12_a; sys(6)=not(S12_a); sys(7)=S32_a; sys(8)=not(S32_a);
sys(9)=S13_a; sys(10)=not(S13_a); sys(11)=S33_a; sys(12)=not(S33_a);

%phase b
sys(13)=S11_b; sys(14)=not(S11_b); sys(15)=S31_b; sys(16)=not(S31_b);
sys(17)=S12_b; sys(18)=not(S12_b); sys(19)=S32_b; sys(20)=not(S32_b);
sys(21)=S13_b; sys(22)=not(S13_b); sys(23)=S33_b; sys(24)=not(S33_b);

%phase c
sys(25)=S11_c; sys(26)=not(S11_c); sys(27)=S31_c; sys(28)=not(S31_c);
sys(29)=S12_c; sys(30)=not(S12_c); sys(31)=S32_c; sys(32)=not(S32_c);
sys(33)=S13_c; sys(34)=not(S13_c); sys(35)=S33_c; sys(36)=not(S33_c);

%Determinating Vdc1, Vdc2, Vdc3
%phase a
if ((S11_a==1&&S31_a==0)|(S11_a==0&&S31_a==1)) &&
((S12_a==0&&S32_a==0)|(S12_a==1&&S32_a==1)) && ((S13_a==0&&S33_a==0)|(S13_a==1&&S33_a==1))
   sys(37)=1; %Vdc1
elseif ((S12_a==1&&S32_a==0)|(S12_a==0&&S32_a==1)) &&
((S11_a==0&&S31_a==0)|(S11_a==1&&S31_a==1)) && ((S13_a==0&&S33_a==0)|(S13_a==1&&S33_a==1))
   sys(37)=2; %Vdc2
elseif ((S13_a==1&&S33_a==0)|(S13_a==0&&S33_a==1)) &&
((S11_a==0&&S31_a==0)|(S11_a==1&&S31_a==1)) && ((S12_a==0&&S32_a==0)|(S12_a==1&&S32_a==1))
   sys(37)=3; %Vdc3
else
   sys(37)=0; %error
```

```
end

%phase b
if ((S11_b==1&&S31_b==0)|(S11_b==0&&S31_b==1)) &&
((S12_b==0&&S32_b==0)|(S12_b==1&&S32_b==1)) &&
((S13_b==0&&S33_b==0)|(S13_b==1&&S33_b==1))
   sys(38)=1; %Vdc1
elseif ((S12_b==1&&S32_b==0)|(S12_b==0&&S32_b==1)) &&
((S11_b==0&&S31_b==0)|(S11_b==1&&S31_b==1)) &&
((S13_b==0&&S33_b==0)|(S13_b==1&&S33_b==1))
   sys(38)=2; %Vdc2
elseif ((S13_b==1&&S33_b==0)|(S13_b==0&&S33_b==1)) &&
((S11_b==0&&S31_b==0)|(S11_b==1&&S31_b==1)) &&
((S12_b==0&&S32_b==0)|(S12_b==1&&S32_b==1))
   sys(38)=3; %Vdc3
else
   sys(38)=0; %error
end

%phase c
if ((S11_c==1&&S31_c==0)|(S11_c==0&&S31_c==1)) &&
((S12_c==0&&S32_c==0)|(S12_c==1&&S32_c==1)) && ((S13_c==0&&S33_c==0)|(S13_c==1&&S33_c==1))
   sys(39)=1; %Vdc1
elseif ((S12_c==1&&S32_c==0)|(S12_c==0&&S32_c==1)) &&
((S11_c==0&&S31_c==0)|(S11_c==1&&S31_c==1)) && ((S13_c==0&&S33_c==0)|(S13_c==1&&S33_c==1))
   sys(39)=2; %Vdc2
elseif ((S13_c==1&&S33_c==0)|(S13_c==0&&S33_c==1)) &&
((S11_c==0&&S31_c==0)|(S11_c==1&&S31_c==1)) && ((S12_c==0&&S32_c==0)|(S12_c==1&&S32_c==1))
   sys(39)=3; %Vdc3
else
   sys(39)=0; %error
end

%=============================================================================
% mdlOutputs, flag=3
% Return the output for the S-function
%=============================================================================
function sys = mdlOutputs(t,x,u,fcr)
   sys(1:39)=x(1:39);
 %end
```

APPENDX B

SIMULATION RESULTS OF NINE-LEVEL CHB-BASED STATCOM SYSTEM

In order to verify the availability of proposed methods to the STATCOM with higher level CHB inverter, simulations of a nine-level CHB-based STATCOM system are performed and the steady-state performances of full-capacitive and full-inductive mode are illustrated in Figure B-1 and Figure B-2, respectively. In Figure B-1 (a), the inverter voltage v_c shapes PWM wave with nine levels. The amplitude of v_c is maximum. The inverter current i is rated and leading the system voltage v_s by about 90^0. Figure B-1 (b) shows dc-voltages of four H-bridges in one phase, v_{dc1}, v_{dc2}, v_{dc3} and v_{dc4}. It can be seen that dc-voltages are balanced when the STATCOM operates in the full-capacitive mode. In Figure B-2 (a), the inverter voltage v_c shapes PWM wave with five levels. The amplitude of v_c is minimum. The inverter current i is rated and lagging the system voltage v_s by about 90^0. Figure B-2 (b) shows balanced dc-voltages of four H-bridges in one phase when the STATCOM operates in the full-inductive mode.

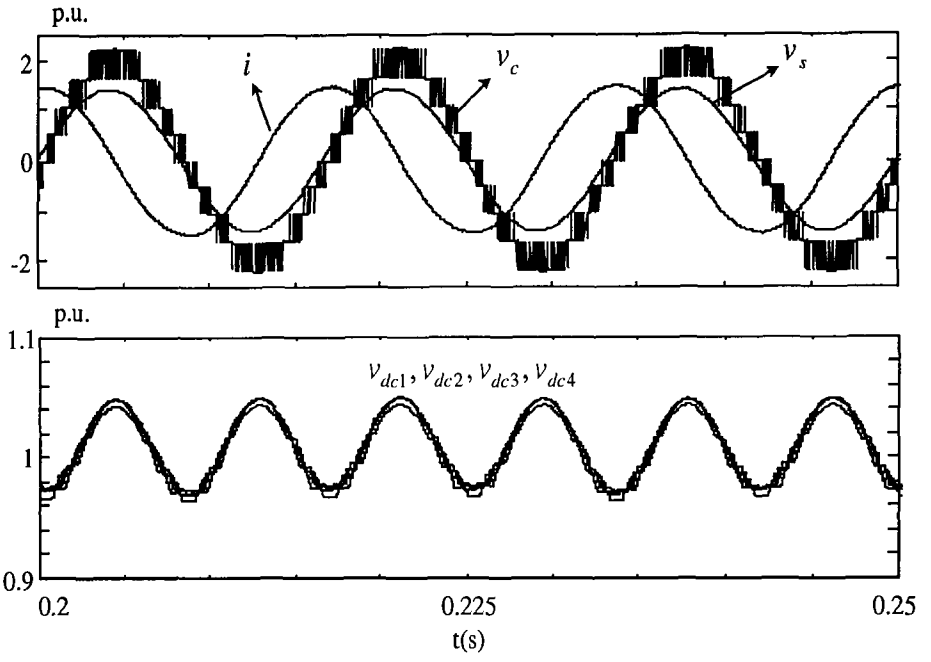


Figure B-1 The steady state performance of nine-level CHB-based STATCOM in the full-capacitive mode.

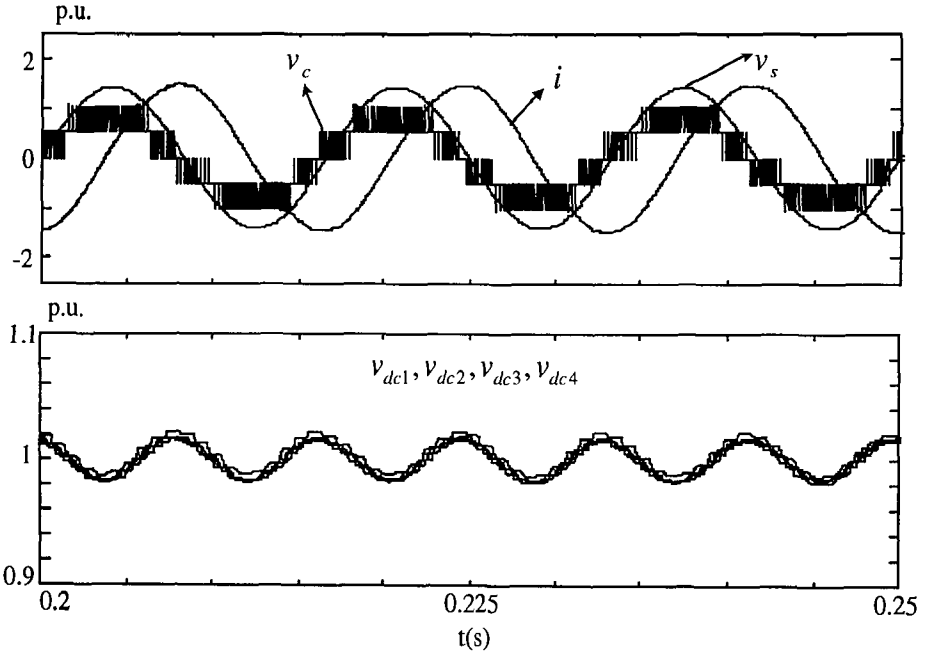
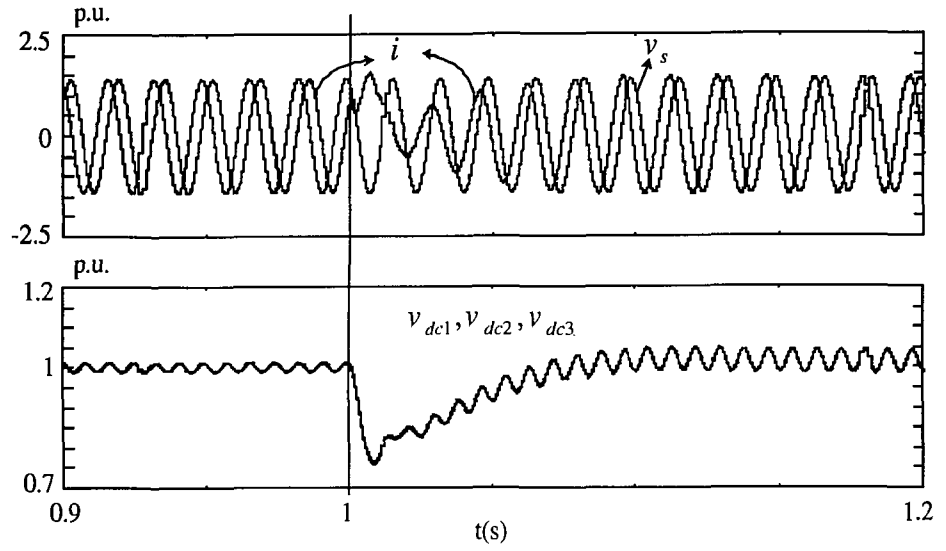


Figure B-2 The steady state performance of nine-level CHB-based STATCOM in the full-inductive mode.

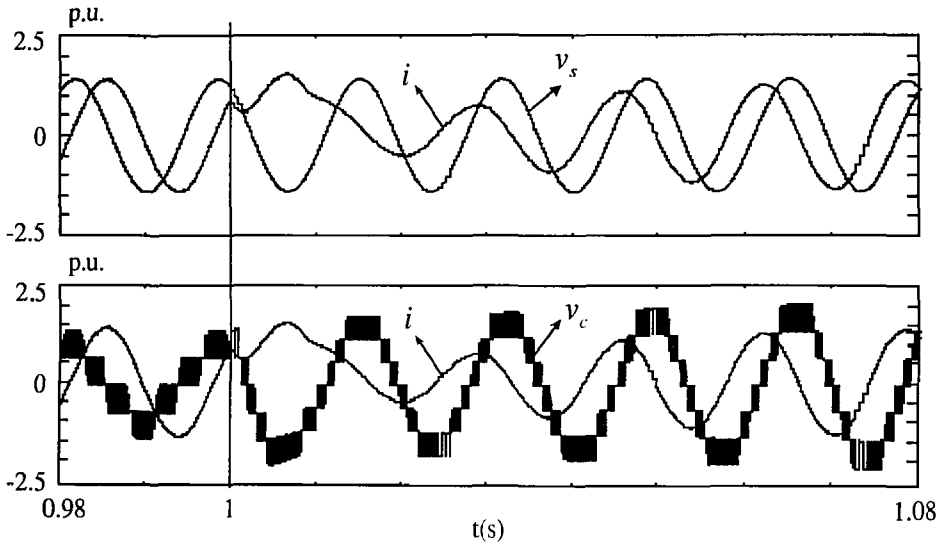
APPENDIX C

SIMULATION RESULTS OF DYNAMIC RESPONSE TO REACTIVE POWER DEMAND

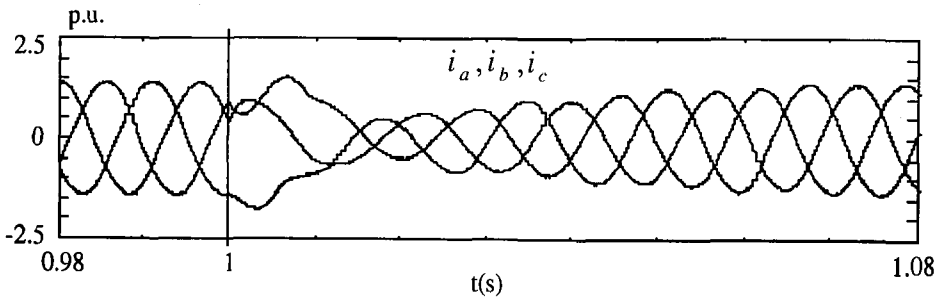
In this appendix, the simulation dynamic response waveforms of the seven-level CHB-based STATCOM are illustrated. Figure C-1, C-2 and C-3 show dynamic responses as the proposed STATCOM changes from full-inductive mode to full-capacitive mode at 1.0s, from full-capacitive mode to half-capacitive mode at 1.5s, and from half-capacitive mode to the standby mode at 2.0s, respectively. Figure C-1 (a) shows the inverter current i, system voltage v_s, and dc-voltages V_{dc1}, V_{dc2} and V_{dc3}. The inverter current i lags and leads v_s by about 90^0 before and after 1.0s. The current amplitude is 1 p.u. in both modes. Details of the transition in Figure C-1 (a) are shown in Figure C-1 (b). Simulation results demonstrate the extremely fast dynamic response of the proposed STATCOM. Reactive power transition can be completed within 2 cycles. Three-phase currents are shown in Figure C-1 (c). Inverter currents are three-phase balanced both before and after the transition. Other response waveforms in Figure C-2 and C-3 are listed in similar order.



(a)

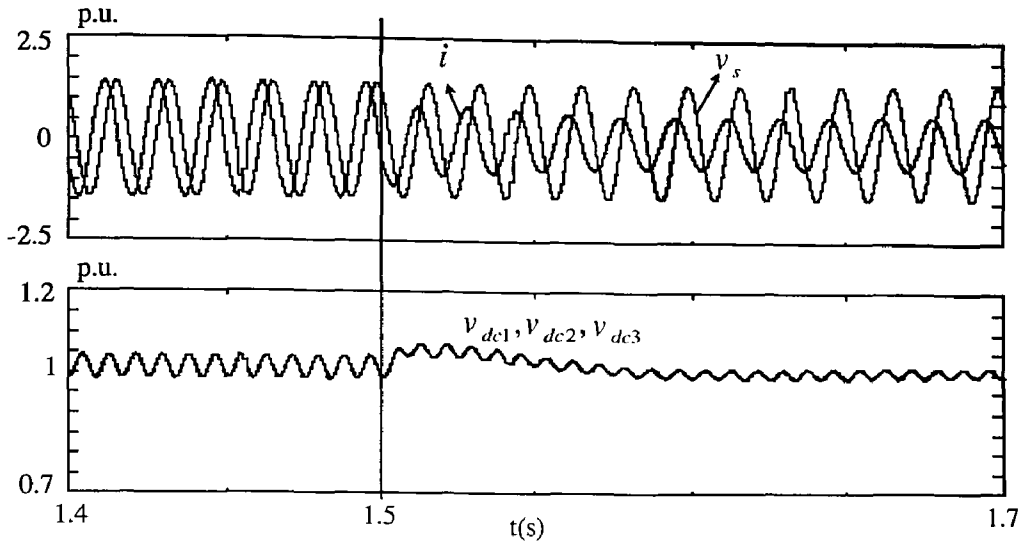


(b)

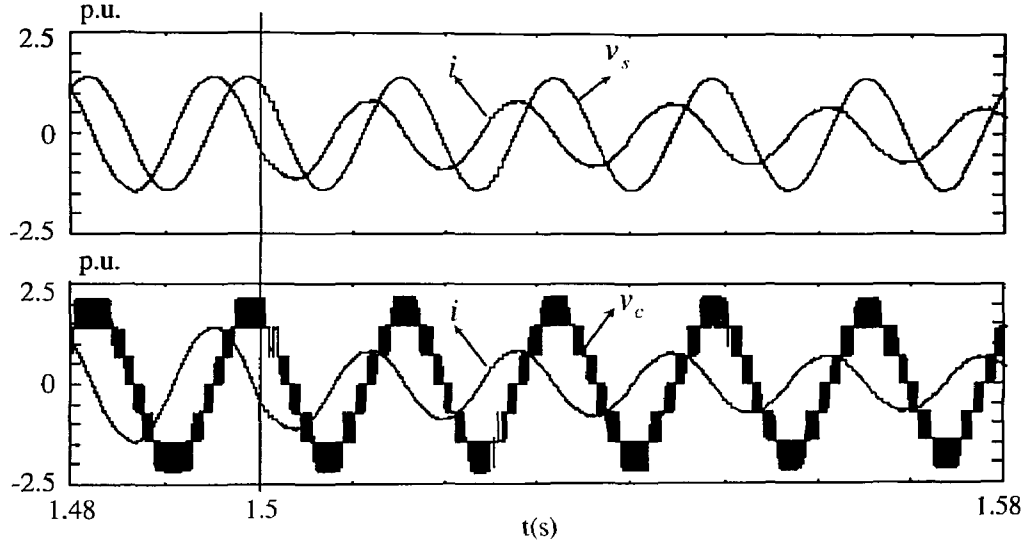


(c)

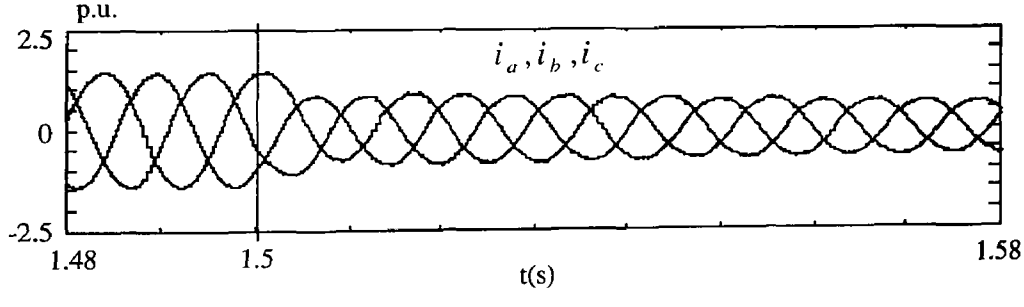
Figure C-1. The seven-level CHB-based STATCOM responses the step change from full-inductive mode to full-capacitive mode at 1.0s, (a) i, v_s and $v_{dc1}, v_{dc2}, v_{dc3}$, (b) details of (a), and (c) i_a, i_b, i_c.



(a)

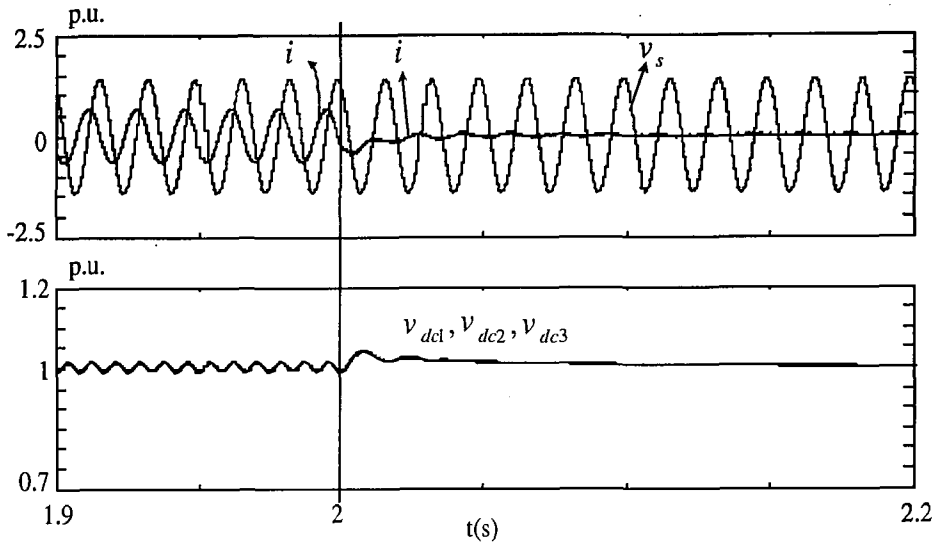


(b)

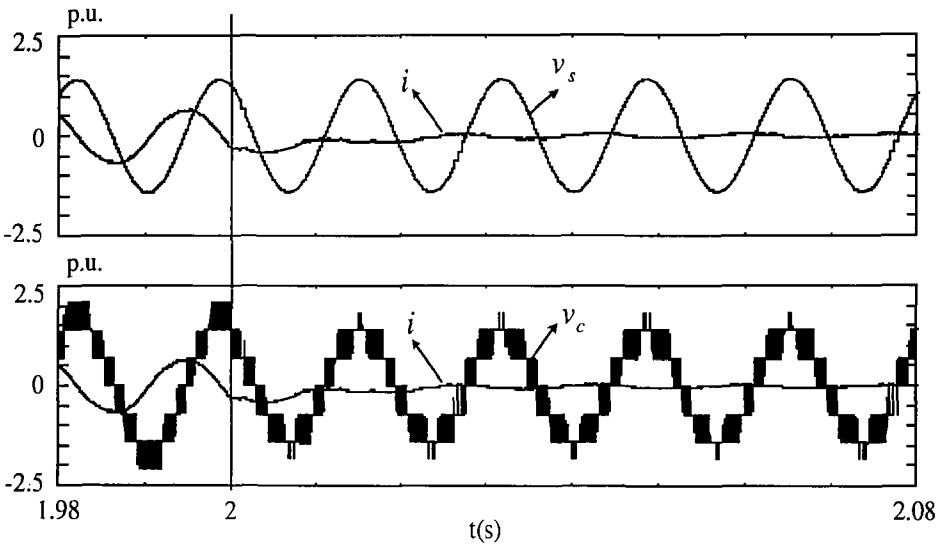


(c)

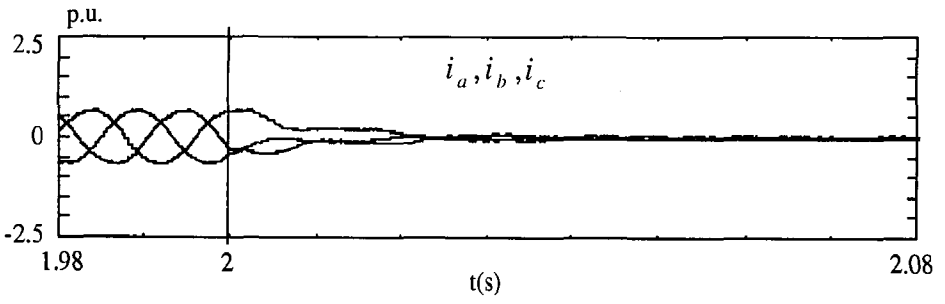
Figure C-2. The seven-level CHB-based STATCOM responses the step change from full-capacitive mode to half-capacitive mode at 1.5s, (a) i, v_s and $v_{dc1}, v_{dc2}, v_{dc3}$, (b) details of (a), and (c) i_a, i_b, i_c.



(a)



(b)



(c)

Figure C-3. The seven-level CHB-based STATCOM responses the step change from half-capacitive mode to standby at 2.0s, (a) i, v_s and $v_{dc1}, v_{dc2}, v_{dc3}$, (b) details of (a), and (c) i_a, i_b, i_c.

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