1-1-2010

Development Of A Device Characterization Curve Tracer for High Power Application

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Development of a Device Characterization Curve Tracer for High Power Application

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September 2006

A thesis

Presented to Ryerson University

in partial fulfillment of the

requirement for the degree of

Master of Applied Science

in the program of

Electrical and Computer Engineering.

Toronto, Ontario, Canada 2010

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Abstract

Due to self-heating and significant temperature rise in a power device junction, the device characterization through the DC measurement is a major issue. Short pulsed technique or Pulsed I-V (PIV) characterization is the technique which is used by commercial curve tracer and network analyzers to characterize the power devices. Although, this technique prevent excessive self-heating but doesn't guarantee that measurement will be operated in the desired accuracy range because even a moderate self heating may cause significant measurement error. In this research work, a measurement technique is introduced that results *device characterization within the desired accuracy range*. The technique is based on the stimulation of the device under test (DUT) with voltage ramps that allow for *fast transient measurement*. Because, this way of stimulation excites the parasitic impedances in the DUT, a dynamic model of the DUT is presented. This model allows determining the operating conditions that *guarantee the specified measurement accuracy*. The measurement procedure is described and the developed measurement algorithms are implemented in LabVIEW environment to obtain a *PC-based device characterization curve tracer for high power application*.

A *high current power MOSFET* is used as the DUT. The calibration and measurement phases are carried out by the developed curve tracer. During the calibration phase, the measurement condition including allowed junction temperature deviation, maximum ramp slope and maximum

allowed drain-source voltage to *guarantee 2% measurement error* is specified. The measurement phase is carried out based on these operating conditions. The result is a family of output I-V curves for different gate voltage set. This measurement technique *validated* with that of measured based on the PIV characterization technique from the device data sheet. The discrepancy between the measurement result and datasheet curve is discussed.

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Acknowledgments

Above all, I would like to sincerely thank my supervisor, Dr. Farah Mohammadi, for accepting me as her MASc. student at Ryerson University and for all of her time, effort, advice, and encouragement with my research and my entire studies. Her insights and guidance have made many research works to be done successfully and finally this dissertation remarkably better.

I would like to thank my committee members Dr. David Xu, Dr. Andy ye, and Dr. John Chen for their great advices and supports.

I would like to thank Dr. Fei Yuan and Dr. David Xu for their technical supports.

I would also like to thank my dear friends, those here and those far away, specially my dear friends Mojdeh, Maryam, Zahra and Hoda for all their kind.

I would like to thank National Science and Engineering Council of Canada (NSERC) and Ryerson University for supporting and funding my research.

I would like to thank my dear uncle Dr. Mohammad Toorani and her great family whom I love with all my heart, for all their support and the time they shared with me.

I also would like to take the opportunity to thank my parents who sacrificed so much for me to be here. Their support and guidance through my entire life has shaped me into the individual I am today. A special thank also goes to my brother, Iman. Without all of his support and encouragement I could never have accomplished any of this work.

Last but not least, I thank God for whatever I am and have right now.

To my dear parents for their love, endless support and encouragement.

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CHAPTER 1

Introduction

1.1 Motivation

When device operates at high power application, self-heating and thermal coupling are the main issues in performance and reliability of a device. Therefore, the accurate device characterization is an important topic for circuit designers. Self-heating, the process by which power dissipation causes a rise in the operating temperature of the device, causes substantial changes in the device operation. It can compromise the accuracy of device models if the operating environment of the device is not identical to one in which it was characterized. The amount of dissipated power by the circuit has direct relation with its temperature which is a crucial parameter in electrical behavior in electronic components, circuit performance and reliability of the electronic system [1-5]. Because of temperature rises that occur due to self-heating, the resulting steady-state measurements constitute a temperature-dependent characterization. In other words, since the electrical characteristics of any semiconductor device are affected by its temperature, their output characteristics obtained by conventional measurements are misleading. Attempting to fit such temperature-dependant data with models based on isothermal device operation leads to significant errors due to the temperature dependency of the semiconductor properties [6]. The magnitude of the errors will be lowest for small signal circuits, where the device current and voltage remain close to a given operating point. In this case, it is sufficient to determine model parameters at operating points close to the final circuit operating conditions; self-heating will occur, and the device temperature will rise, but the rise will be the same in characterization and in operation. Assuming the model still presents a reasonable description of the device physics at elevated temperatures, the results can be expected to be reasonably accurate with this approach. The results of large signal circuits,

where currents vary dramatically during operation, are expected to be less successful. For example, in a digital circuit, device currents often vary from a relatively low level in the off-state to a high level in the on-state; this on-state power dissipation is high enough to cause substantial self-heating [6]. Short pulsed technique or Pulsed I-V (PIV) characterization technique is used in commercial curve tracers in an attempt to eliminate this error [7]. Based on this technique, all of the measurements are performed at a low duty cycle before there is a significant change in temperature. The technique of PIV characterization was pioneered in the late 1980s and further developed during the 1990s [8-9]. This technique is still the most conventional technique to direct measurement of output characteristic of semiconductors and is used in commercial curve tracers and network analyzers [7, 10-11]. However, even a moderate self-heating may cause measurement error far above the specified accuracy. This urges designers to investigate the development of new methods to limit the measurement errors within a required accuracy.

1.2 Literature Review

In this section, different types of power transistor characterization measurement and recent advances in this area are discussed. The process of designing experiments and performing transistor measurements, for the purpose of model extraction as well as model validation, is called “transistor characterization”.

The power transistor behavior can not just described by pure electronics since it inevitably converts a significant portion of the DC power into heat. As a result, the transistor may experience a wide range of temperature gradient during the characterization measurements as well as its operation. This causes some of the electronic elements of the transistor to be very sensitive to temperature. For instance, suppose a power bipolar junction transistor (BJT) is driven to active region by applying a constant base current I_B (similarly gate voltage for a field effect transistor (FET)) and constant collector-emitter voltage V_{CE} (similarly V_{DS} for a FET); the collector current I_C (I_D for metal oxide semiconductor field effect transistor (MOSFET) slowly changes over time, to finally settle to a steady-state value. The fact that the values of V_{BE} (I_G) and I_C (I_D) change versus time can then easily be explained by the fact that the temperature of the

transistor starts changing due to self-heating as soon as the experiment starts. This can be expressed as

$$V_{BE} = F_{BE}(V_{CE}, I_B, T) \quad 1.1$$

$$I_C = F_C(V_{CE}, I_B, T) \quad 1.2$$

These phenomena can be modeled by defining temperature *(T)* as an explicit parameter in the model equations. Based on the thermodynamic concepts, thermal conductance (G_{th}) and heat capacity (C_{th}) parameters are defined to illustrate the time-varying thermal behavior of a transistor. *T (t)* can be defined as:

$$T(t) = T_0 + \Delta T_\infty \left(1 - e^{-t/\tau}\right) \quad 1.3$$

where ΔT_∞ is the difference between steady-state and room temperature and τ is the relaxation time constant. The values of these parameters for a BJT are given as [12]:

$$\Delta T_\infty = \frac{V_{CE} F_C(V_{CE}, I_B, T_0)}{G_{th} - V_{CE} \frac{\partial F_C}{\partial T}} \quad 1.4$$

and,

$$\tau = \frac{C_{th}}{G_{th} - V_{CE} \frac{\partial F_C}{\partial T}} \quad 1.5$$

From the thermal point of view, a transistor behaves as a system with a heat capacity of C_{th}, which has an apparent thermal conductance equal to $G_{th} - V_{CE} \frac{\partial F_C}{\partial T}$. So, if there is significant power dissipation in the transistor, the device behavior is a combination of thermal and electrical effects [12].

Based on the equation 1.5, if $\frac{\partial F_C}{\partial T} > 0$, like for germanium BJTs, τ becomes negative. As a result, temperature increases exponentially and never reaches a steady-state value. This unstable positive feedback phenomenon called “thermal runaway” causes damage in the transistor. One

way of breaking up the positive electro-thermal feedback cycle is to use a big enough resistor in series with the V_{CE} voltage source. The idea is that any increase in collector current automatically decreases the collector voltage. As a result, the dissipated power is decreased which leads to a decrease in the temperature rise rate. By this solution, characterizing the transistor across its entire operating span is possible without blowing it up. From the above example, it can be concluded that it is hard to build one single measurement setup that allows characterizing all possible transistor technologies.

While dealing with thermal issues, the simplest way to provide data for modeling a device would be to directly measure the temperature-dependent voltage-current relationship. This is practical if a particular couple of values ($V_{CE,}$ I_B) for BJTs or ($V_{GS,}$ V_{DS}) for FETs and a temperature T are applied, and ($V_{BE,}$ I_C) or respectively ($I_{GS,}$ I_{DS}) are measured before the temperature significantly changes. Such a measurement is referred to as isothermal. From the hardware perspective, this implies having means to control the temperature of the device under test (DUT), like a thermal chuck with the temperature of T when the experiment starts. The stimulus sources should be switched off as quickly as possible after the measurement is performed. Enough rest time should be considered before performing a subsequent measurement until the temperature returns back to T. This process is so-called Short pulsed technique or Pulsed I-V (PIV) characterization. There are many ways to perform pulsed measurements.

Figure 1.1 illustrates a pulsed I-V system which is capable of reaching any current-voltage point of three terminal devices from any arbitrary chosen DC bias points [13].

The measurement results for a GaAs metal semiconductor field effect transistor (MESFET) are shown in figure 1.2a-b. The effect of the DC bias on the output curves is considerable even when the DC dissipation and junction temperature rise is almost zero. The effect of temperature on current amplitude can be also noticed in figure 1.3a-b, when the DC dissipation in figure 1.3b is more than figure 1.3a.

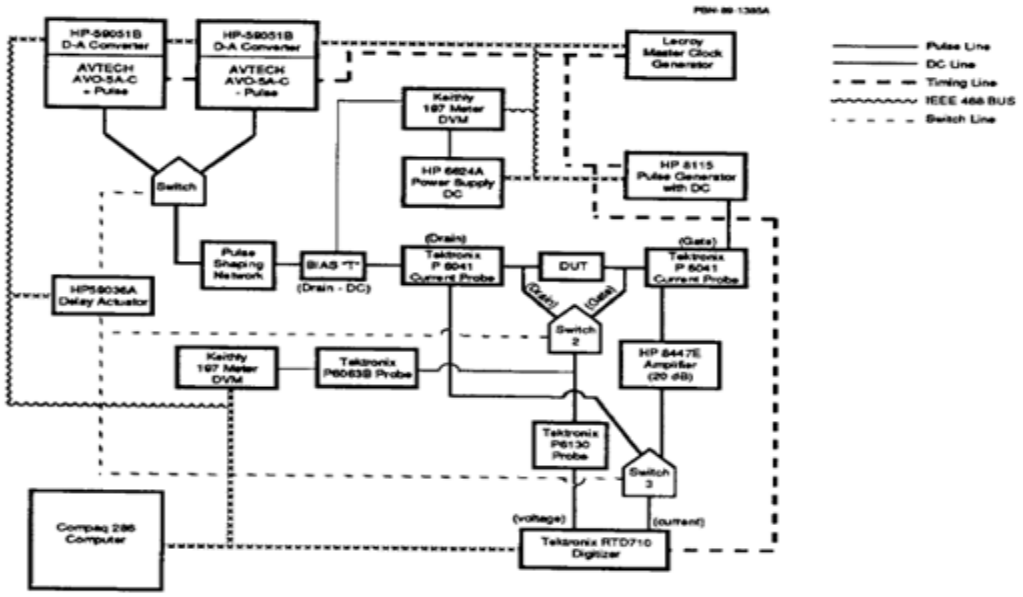
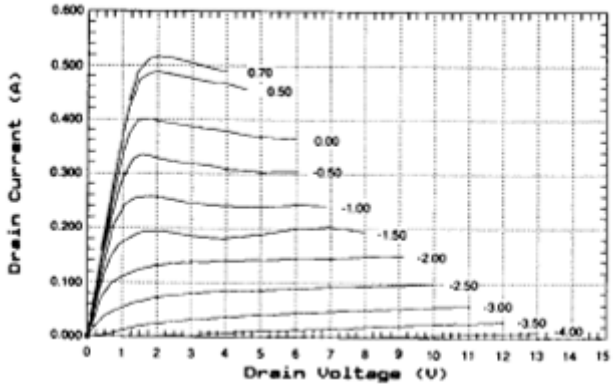
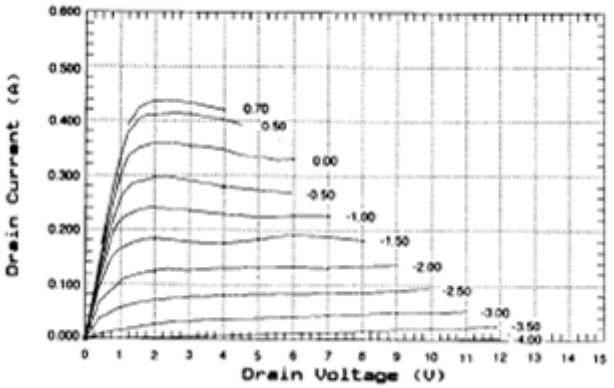


Figure 1.1: Block diagram of a PIV technique

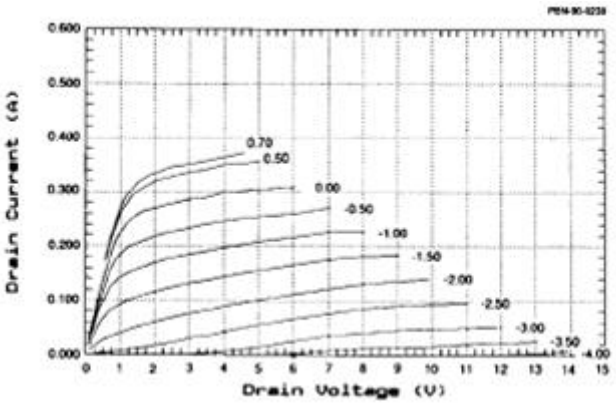


a) Vds=0V, Vgs=0V

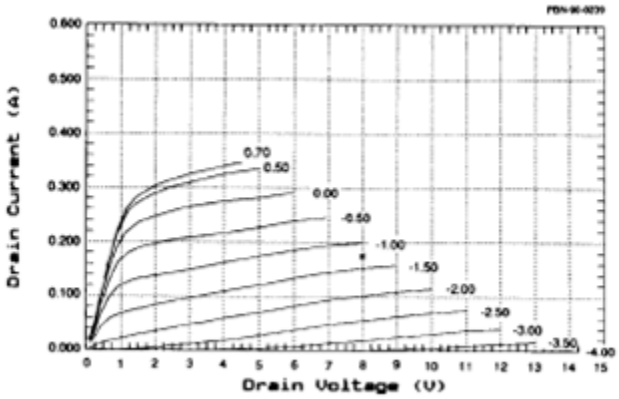


b) Vds=0V, Vgs=-4V

Figure 1.2: Effect of Different DC bias Points on PIV curves of a GaAS MESFET [13].



a) Vds=6v, Vgs=-4V



b) Vds=8V, Vgs=-1.25V

Figure 1.3: Effect of power dissipation on PIV curves of a GaAS MESFET points [13].

It can be seen that thermal behavior varies based on any change in the bias values during the pulse stimulus, as well as changing the initial bias values.

Figure 1.4 shows another example of a practical measurement performed on a 10 W GaN FET that is affected by initial biasing. The blue lines indicate the DC measurements. The red and green lines represent two pulsed measurements, where each one has a different initial bias condition. It can be observed that the IV relationship is a strong function of the initial conditions. Note that the characteristics are very different from the DC measurements. The DC measurements were performed over a much smaller bias region than the pulsed measurements. This is typically the case since DC measurements stress the device much more than pulsed measurements. Pulsed measurements can easily be performed in regions where DC measurements would cause permanent damage to the DUT (For instance, because of excessive heating) [13].

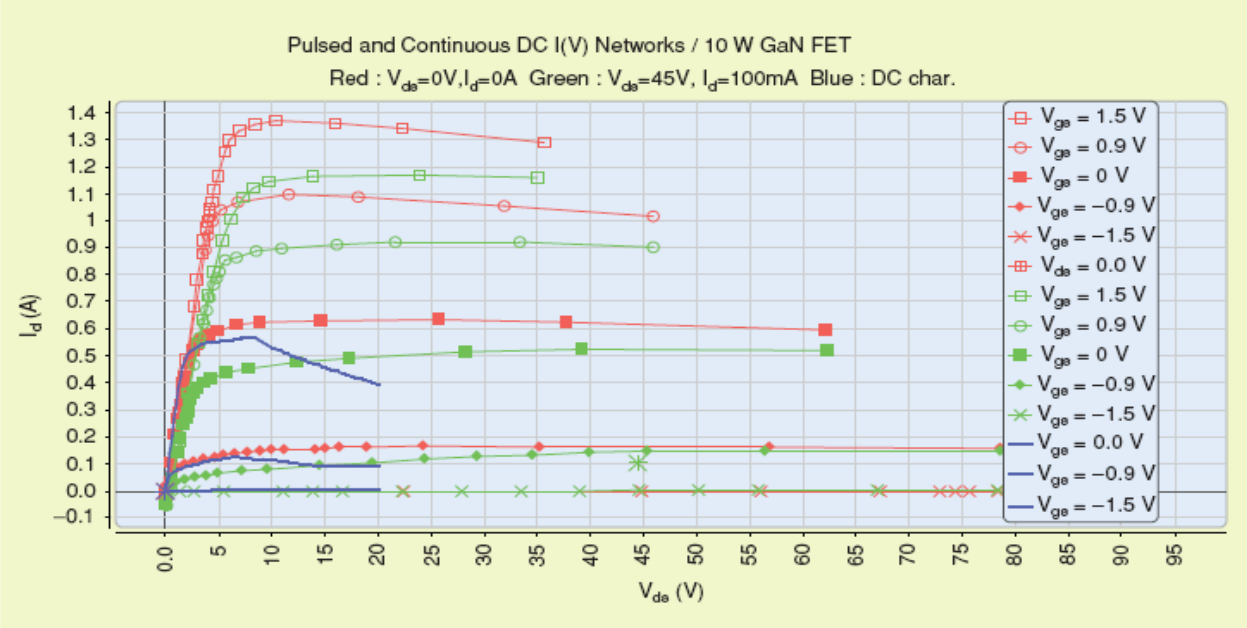


Figure1.4: Pulse and DC I-V measurement from different initial conditions for 10W GaN FET.

Another measurement method is to characterize the silicon-on-insulator (SOI) MOSFET device without self heating using short pulses with a low repetition rate and a reverse transient load-line construction. The measurement was performed on a nanosecond time scale. This method was validated based on the comparison between static measurement and pulsed excitation results for the DUT. The measured drain current is 20% higher for the static measurement as shown in figure 1.5. However, the accuracy of the pulsed I-V result has not been studied. In addition, no justification has been made for the selected time scales [14].

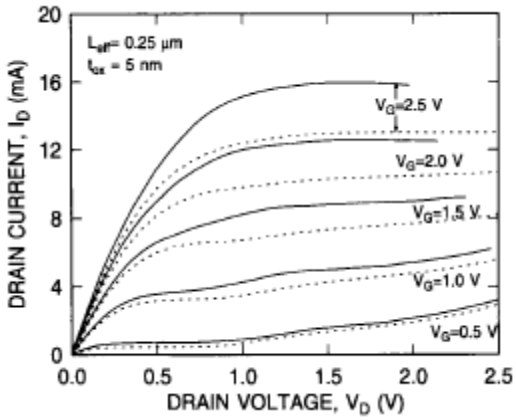


Figure 1.5: PIV (solid line) and static (dashed line) I-V curves of a SOI MOSFET [11]

As a conclusion to the above discussion, characterization of a device for both design and modeling is most effective when the DUT is excited with pulses sufficiently short and spaced. As a result, the acquired data will not be influenced by history-dependence in the device. If measurement pulses are too close together, measurement in each pulse is affected by conditions in the previous pulse. If measurement pulses are too long, measurement drifts toward its steady-state value [15-16].

The duration of stimulus pulses and their spacing is selected rather arbitrary. The measurement starts from the desired initial biasing. The output curves are affected not only by the device characteristic but also by the measurement setting.

[16-17] presents a method by which the pulsed requirements including pulse width and pulse period can be determined. Using a specific measurement set-up, the region of history-dependency error against pulse duration and separation for a sample DUT can be determined [18]. The result is a surface plotted as a 3D graph with the pulse duration t_p as the x- axe and pulse spacing t_q as the y- axe. Such a graph for a GaAs FET is given in figure 1.6.

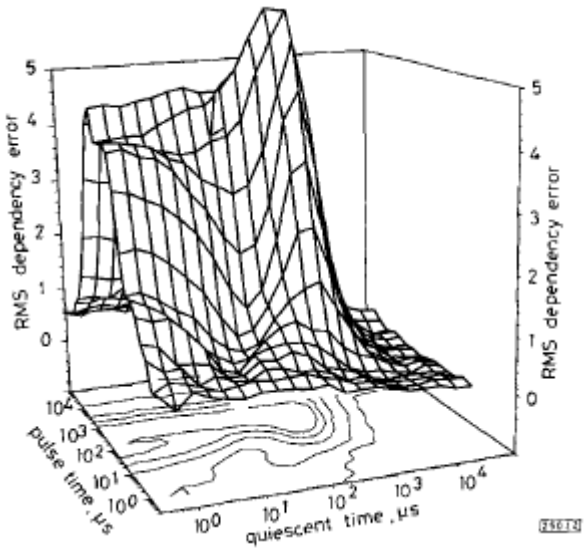


Figure 1.6: Plot of history-dependency error against pulse width and pulse spacing for a GaAs FET [13]

Time intervals vary from 100 ns to 30 ms. The surface tends toward zero error as $t_p \to 0$ and$t_q \to \infty$. It also stabilizes to a low error as $t_p \to \infty$; i.e. the pulse becomes so long that the

device settles into the thermal and trapping equilibrium during each stimulus pulse. In the vicinity of the ideal corner, there is a zone which measurement must be made within this area to minimize error. It is desirable to set the timing of a PIV measurement system in such a way that it lies in this flat zone. Outside of this zone the error is expected to grow. The optimum settings are those that produce minimum total period $(t_p + t_q)$ and thus the most rapid measurements [13].

However, there is no single measurement technique and set up for all transistors technology. The limitations mentioned earlier in this section become even worse when it comes to characterize RF transistors where high frequency and trapping effects make more difficulties [16]. More measurement set-up for PIV characterization can be found in [19-23].

1.3 Limitation of Current Methodologies

The main limitation related to PIV characterization is that stimulus pulses and their spacing are selected rather arbitrary and there is no justification for the time scaling. Method proposed in [16] presents some suggestions to select the pulsed requirements based on the low error measurement region. However, it does not necessarily provide the best pulse width and duration which are essential to minimize the self-heating and do the fast measurement. In other words, working in flat region guarantees low error but doesn't determine the error. In addition, the graph of history-dependency error (as given in figure 1.6) is not always available for all DUTs.

The other limitation is related to the dependency of output results to the initial DC biasing especially when dealing with RF power transistors.

However, a minimum self-heating always happens and causes measurement error. Therefore, it's needed to be calculated to determine the error measurement. The methodology provided in this study eliminates this limitation by calculating even minor self-heating and introduces a new operating area in which the measurement errors are limited within a desired range. Also the time scale selection is based on the instantaneous junction temperature and transient thermal impedance of the DUT which is the indicator of self-heating in semiconductors due to power dissipation.

1.4 Thesis Objective

The goal of this research is to develop a PC-based device characterization curve tracer for high power application. A technique based on the stimulation of a DUT by fast voltage ramp excitations to further minimize the power dissipation in the DUT during measurements is introduced. The objective of the developed measurement technique is to identify the operating regions of the DUT which is measurable without exceeding specified error range. This research work aimed to propose measurement technique to reduce self heating and to improve device characterization. This technique was applied to predict the characterization of a power MOSFET. The performance of the proposed measurement technique was investigated by comparing the experimental results obtained with that of available I-V characteristic of the device in datasheet which was measured based on the PIV characterization.

A ramp voltage source is designed whose slope and amplitude is controllable through the tracer circuit. This source is employed to stimulate the DUT. Transient measurement is performed during each slope. The slope and amplitude of the ramp source is selected in such a way that the maximum power dissipation does not exceed a certain value. For this purpose, the first phase of the measurement, calibration phase, is applied to identify the appropriate slope and amplitude of the ramp. The second phase is the transient measurement phase generating the static output characteristic of the DUT. The temperature rise in calibration mode is estimated through the thermal impedance response of the DUT. This estimation is employed during the measurement phase to determine the operation boundaries in which the measurement is performed without exceeding a certain error range.

1.5 Thesis Outline

In this research we have attempted to provide coverage of important subjects required for development of a PC-based device characterization curve tracer for high power application. The measurement set up and principle of operation for low power and high power devices are presented in chapter 2. In addition, the implementation of a tracer system and test board for output characterization of a transistor was briefly introduced. In Chapter 3, the tracer system as the main part of the measurement process is described. Detailed discussion on temperature

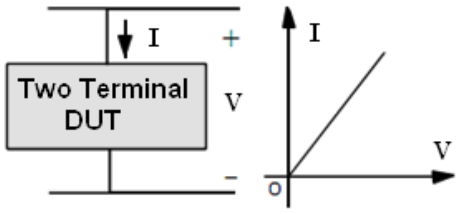
control as the main part of the trace circuit is also presented in this chapter. Chapter 4 presents the test board where the DUT (a high current power MOSFET) is located. The proposed measurement method is described in details in chapter 5. This includes characterization procedure and operational sequence. The implementation and validation of the PC-based device characterization curve tracer in LabVIEW environment are described. In addition, the main sources of measurement errors are discussed. Finally, the conclusions and suggested future works are summarized in chapter 6.

CHAPTER 2

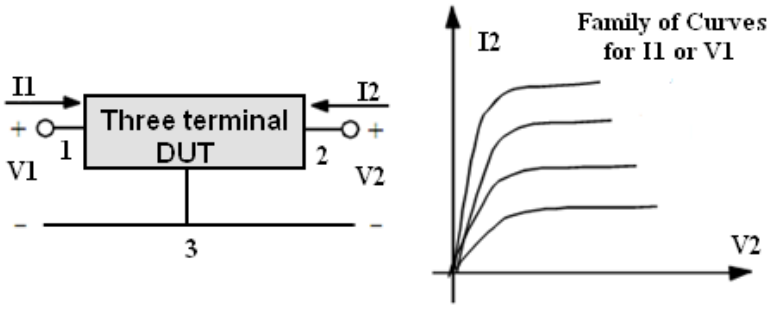
Output Characteristic Measurement of a Device

2.1 Introduction

This chapter describes the implementation procedure for a software-based curve tracer to measure the output characteristic of both low and high power devices. A curve tracer is an electronic instrument that allows monitoring the output characteristic curves of two and three terminal electronic components such as diodes, transistors, triacs, etc. The two terminal components are characterized by a single current-voltage (I-V) curve as depicted in figure 2.1a. In contrast, for a three terminal components, two I-V curves are required to characterize the device because it has two activation ports referenced to a common point. Therefore, a family of I-V characterization curves is generated. For each set of these curves, one of the activation ports is considered as a variable parameter and the other one is used as a common point [24]. Figure 2.1b depicts the I_2-V_2 characteristics of a three terminal component when I_1 or V_1 is a parameter that makes a set of I-V characterization curves.



a) Two terminals



b) Three terminals

Figure 2.1: Output characteristic of a device.

2.2 Proposed Curve Tracer

A variety of hardware and software is required to implement a curve tracer. The scope of the device characterization test itself depends on the type of the DUT and the desired results. The proposed automated set up to implement a PC-based curve tracer to conduct a typical device characterization test is shown in figure 2.2. This set up consists of four main parts as listed below.

1. *Trace Circuit:*

Trace circuit carries out the necessary signal generation and measurement.

2. *Test Board:*

The test board is a gear where the DUT and other required components for implementation of the proposed measurement method are mounted.

3. *Data Acquisition System (DAQ):*

The data is captured and analyzed using the commercially available NI PCI-6052E data acquisition hardware, supported by PC-based software [25]. The personal computer is configured with 2 NI PCI-6052E boards each with 16 analog input and 2 analog output channels for simultaneous data acquiring and recording the tests. These input channels are used for data acquisition and are capable of acquiring voltage signals from a thermocouple transmitter, a DUT and a current sensing resistor. The DAQ board acts as an interface between hardware and *LabVIEW* development environment.

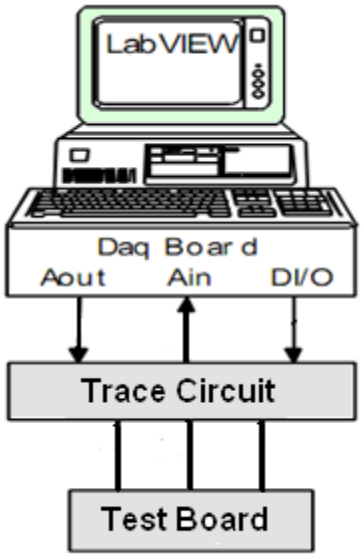


Figure2.2: Proposed Set-up for a Curve Tracer.

4. *LabVIEW Development Environment*

Laboratory Virtual Instrument Engineering Workbench (LabVIEW) development environment from National Instrument [26] is a graphically programmed computer language which is used to design algorithms and develop test and measurement control systems. In the proposed set up, it is used in different aspects. The virtual instrument capability of the LabVIEW is employed to provide analog and digital waveforms to drive and control the trace circuit. The input channels are also used to acquire measured voltage and current signals. In addition, it is used to implement the measurement algorithms and designing a proportional-integral-derivative (PID) controller as well as initializing and driving the stand-alone instruments such as power supplies and oscilloscope. The developed LabVIEW code for PID controller is described in chapter 3. The generated code for implementing the measurement algorithms and driving the stand-alone instruments are also presented in chapter 5.

2.3 Output Characteristic Measurement of Low Power Devices

The mechanism of measurement and set up is similar for two and three terminal devices. However, the trace circuit is slightly different [24, 27]. This section studies a bipolar transistor (BJT) and a field effect transistor (FET) as a DUT.

2.3.1 *Principle of Operation and Measurement Set up*

The test board houses only a DUT for low power devices. The trace circuit for a BJT is shown in figure 2.3. This circuit can also be used for two terminals and other three terminals devices. The trace circuit also includes bias resistors. The DUT was connected through three terminals inside the trace circuit. Assuming a BJT as a DUT, the emitter terminal (E) is the common point for the input and output circuit. The input circuit includes the base (B) which is stimulated by a voltage signal (V_{BB}) or current signal (I_{BB}). The stimulation generally whether for manually measurement or automated measurement is discrete values. For the assigned base value, the V_{CC} is swept in the desired range and simultaneously the V_{CE} and I_C is measured. The result is the I_{CE}-V_{CE} curve for the designated V_{BE}. The same procedure can be used for a FET just this time, the gate as an input, should be driven by a voltage source. E terminal should be connected to the source as the common source and the output signal are V_{DS} and I_D. To drive a two terminal component, only the collector sweeping is required to obtain the I-V curve.

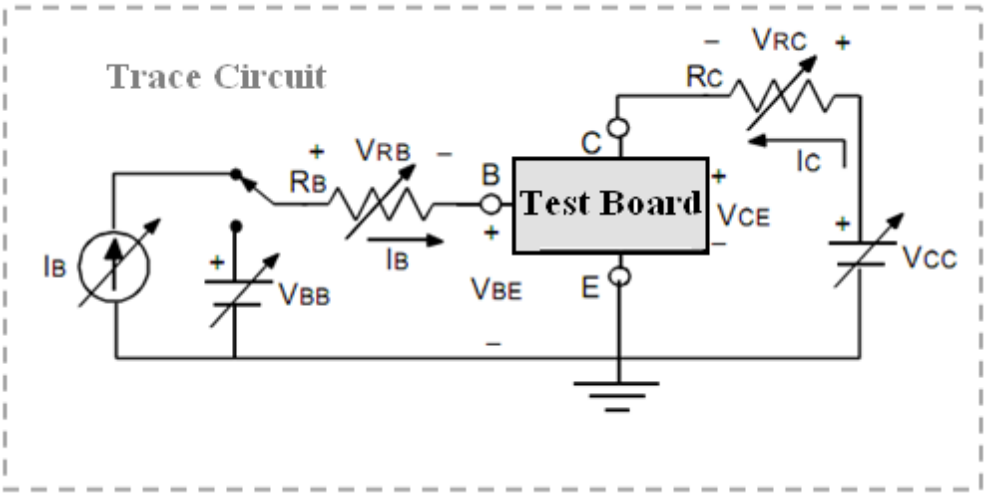


Figure 2.3: Trace circuit.

To automate the measurement as illustrated in figure 2.2, a data acquisition system is employed. PCI-6052E which is a full featured E-series DAQ from National Instrument (NI) is used in this work. However, basic DAQs such as PCI6014 are also suitable for low-power measurements.

A program is developed in LabVIEW environment to control the trace circuit while a BJT is mounted in the test board as a DUT. The developed graphic user interface is shown in figure 2.4. A user may select either a BJT or a FET as a DUT for characterization purpose. In calibration section, the user selects the initial base (gate) voltage as well as number of desired traces, that is, the number of output curves that would be generated. Also, the user has the option to change the collector resistance (*Rc*) to adjust the biasing operating points. Vcc-step implies how the user wants to sweep the output. A default value of 0.01 V was set, but the user can adjust it to desired value.

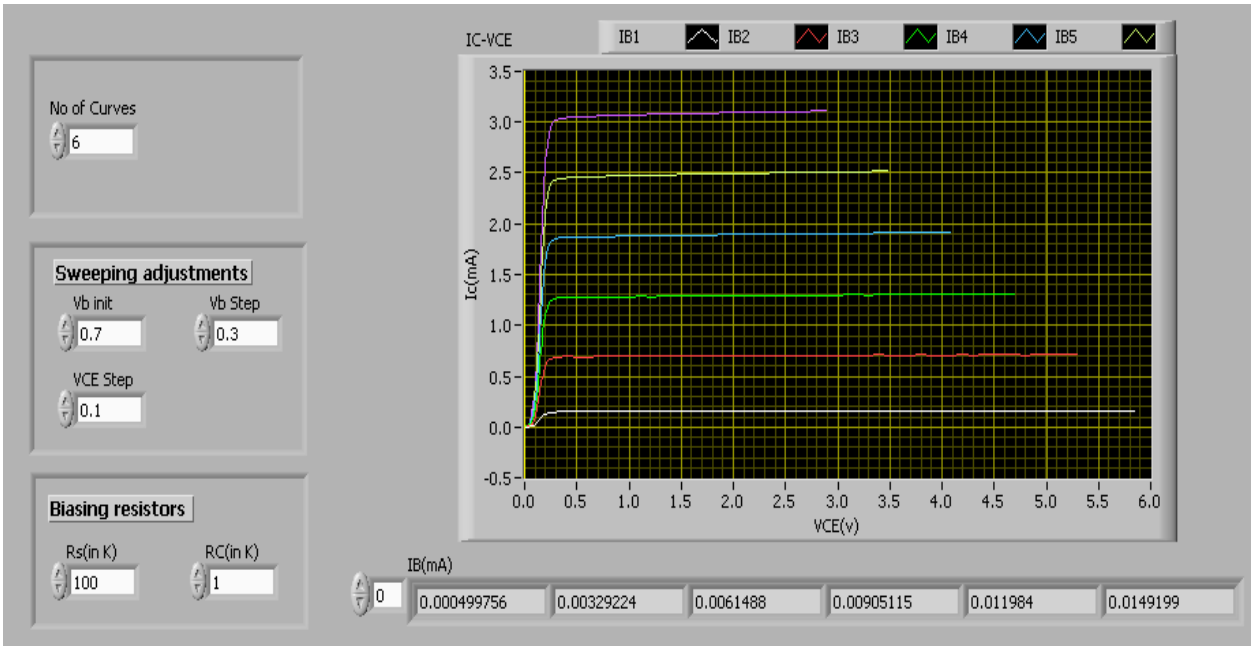


Figure 2.4: User graphical interface for a BJT and a FET curve tracer.

Figure 2.5 illustrates the developed LabVIEW program. It uses two analog output (AO) channels to generate base (gate) voltage and V_{CC}. Two analog input (AI) channels are also employed to measure the collector-emitter (drain-source) voltage, V_{CE}, and output collector (drain) current, I_C. The inside loop generates an I-V curve and the outside loop repeats the procedure to generate a family of curves based on the number of selected tracer.

It should be noted that the maximum voltage provided by the DAQ is 10V. In the case that V_{CE} exceeds ±10V an attenuator is needed. In addition, an amplifier should be added to the tracer circuit [24, 27] to provide voltage source more than 10V for $V_{CC.}$

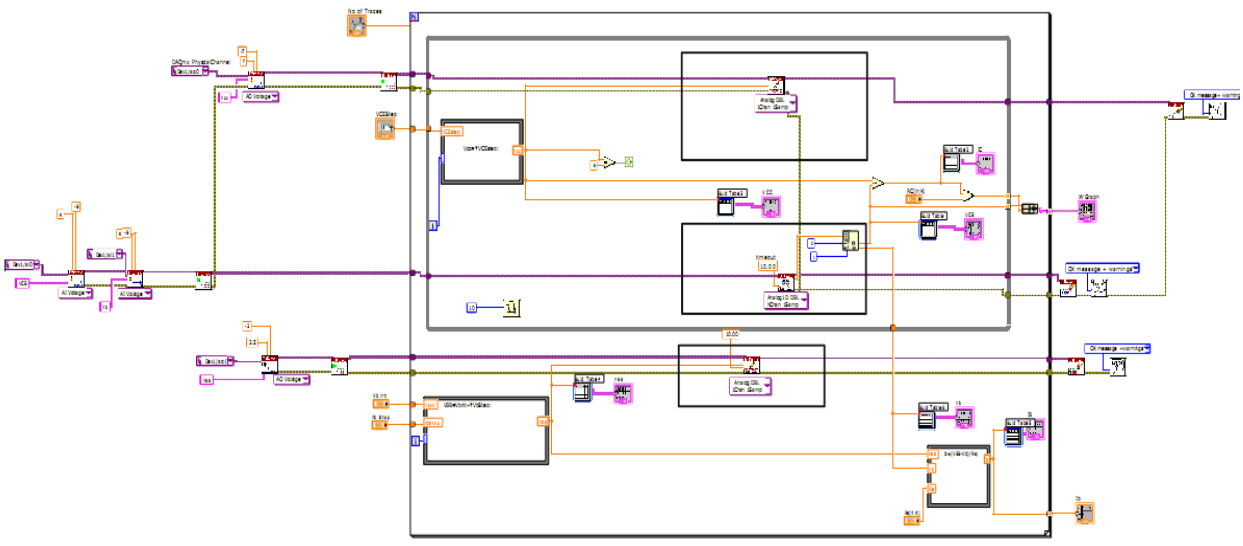


Figure 2.5: Curve tracer program in LabVIEW for a BJT and a FET.

2.3.2 Results and Discussion

Fairchild 2N3904 BJT is employed as a target device [28]. For biasing resistors, R_C and R_B, (see figure 2.3) are selected for 1KΩ and 100KΩ, respectively. Six output I-V curves are generated by the developed LabVIEW program for the base currents varying between 0.00049 to 0.0149 mA (see figure 2.4). The collector current (I_C) is limited to values below the maximum allowed current for the DAQ analog output channel which is about 5mA. The V_{CC} is limited by the program to maximum 6V. According to the I-V curves in figure 2.4, the voltage drop across the collector resistor are insignificant for smaller base currents and the most part of the voltage source (V_{CC}) drops across the transistor channel. Base current increase and consequently collector current rise leads to an increase in voltage drop across R_C. For the last curve, the voltage drop across R_C and V_{CE} is almost equal.

2.4 Output Characteristic Measurement of High Power Devices

The proposed measurement method to characterize a high power device is based on the stimulation of a DUT by voltage ramps [29].

2.4.1 *Measurement Set up*

The block diagram of the test set up to measure the static output characteristic of a high-current power MOSFET is shown in figure 2.6.

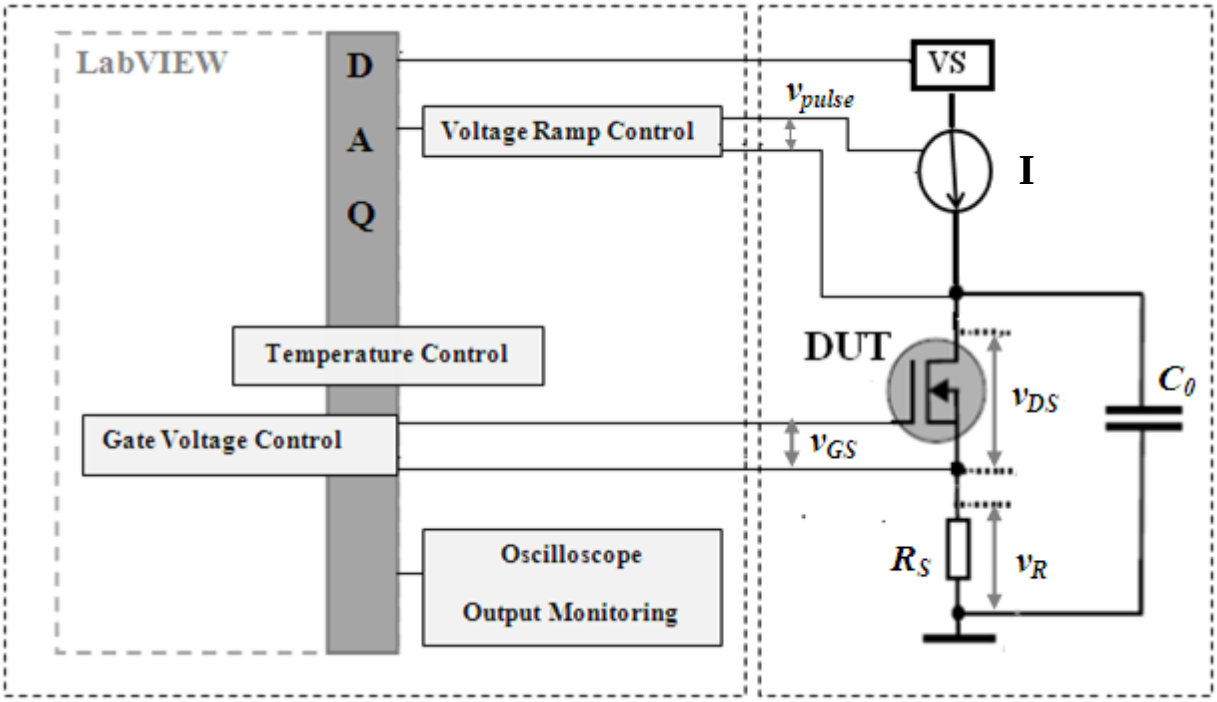


Figure 2.6: Block diagram of the proposed set up for power MOSFET I-V measurement

Trace circuit, shown in left hand side of the figure 2.6, is composed of a voltage ramp control, a temperature control, a gate voltage control and an output monitoring part. These parts are controlled by the developed LabVIEW program through a DAQ board. Detailed description of each part is provided in chapter 3.

Test board, located in right hand side of the figure 2.6, is a gear where a DUT, a voltage controlled current source, a current sensing resistor (R_S), a capacitor (C_0) and a PC-controllable voltage supply (V_S) are mounted. The specification of each component is presented in chapter 4.

2.4.2 *Principle of Operation*

The proposed measurement technique is based on the stimulation of a DUT by voltage ramps that allows for fast transient measurement. Although, self-heating is inevitable, this

approach seeks mitigating of self-heating as the main source of the measurement errors in high power semiconductors such as power MOSFETs [29].

After the gate voltage (V_{GS}) established in a DUT, the voltage controlled current source is driven for the desired constant current (I) and time (pulse width). The current source is controlled by a pulse voltage (V_{pulse}). Thus, the voltage V_{DS} across the DUT is increasing in a linear fashion as C_0 is charging with the constant current I. The drain current (V_R/R_S) of the DUT rises until it reaches saturation (I_{sat}). The current source is then turned off slowly when the voltage V_{DS} reaches the maximum allowed voltage (V_{peak}). The reverse operation is then occurs i.e. the voltage across C_0 discharges through the channel of the DUT toward zero. Repeating the described procedure for various gate voltages (V_{GS}) generates a family of I-V curves. In addition, this procedure can be repeated for various junction temperatures to characterize the operating range of the device. The described procedure is illustrated in figure 2.7.

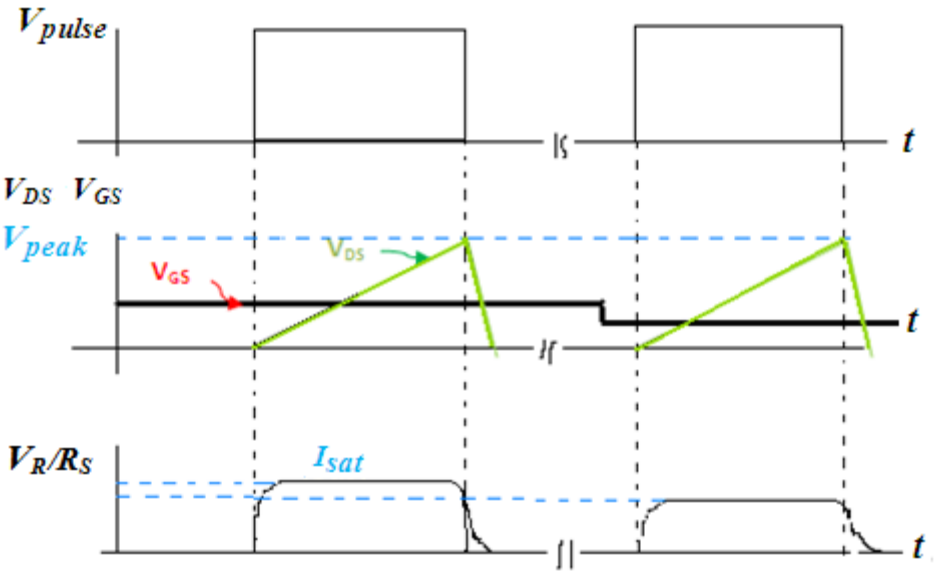


Figure 2.7: Illustration of the operation of proposed set up shown in figure 2.6.

2.5 Summary

A set up for a software-based curve tracer to conduct a typical device characterization test is introduced in this chapter. The proposed curve tracer measurement set up consists of four major components: trace circuit, test board, data acquisition system and LabVIEW development

environment. The implementation of a trace circuit and a test board for output characterization of both low and high power devices as well as their operational principal was described.

CHAPTER 3

Trace Circuit

3.1 Introduction

This chapter introduces the main parts of the curve tracer set up. It also describes the implementation of each part. Figure 3.1 depicts the block diagram of the trace circuit.

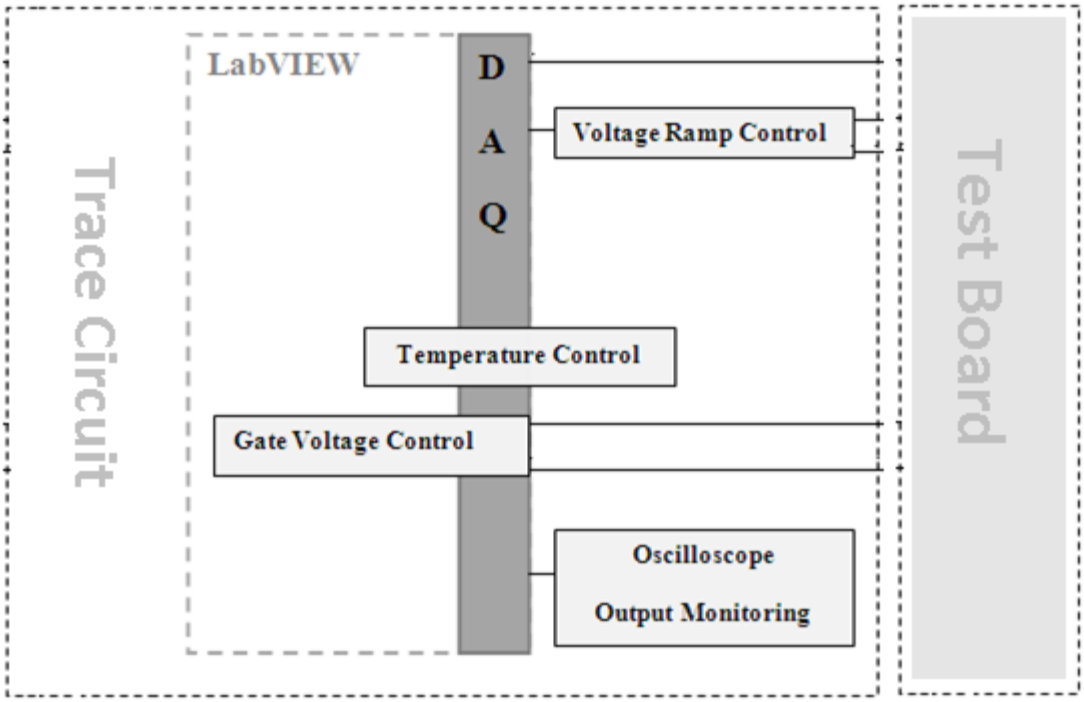


Figure 3.1: Block diagram of the trace Circuit.

The trace circuit is composed of five main parts as follows:

1. *CPU/PC* : is used as a platform for the LabVIEW development environment to automate the measurement system;

2. *Voltage ramp control unit*: is used to set the slope and pulse width of the voltage ramp;

3. *Temperature control unit*: is employed to monitor and maintain the junction of the DUT at a constant temperature;

4. *Gate voltage control unit*: is used to set the gate voltage of the DUT;

5. *Oscilloscope*: is used to monitor and measure the voltage and current of the DUT.

3.2 Voltage Ramp Control Unit

The main reason of having a voltage ramp control unit is to implement a voltage-controlled current source to charge a capacitor in an almost linearly fashion for transient measurement. A power MOSFET is employed as a current source. It is driven to active region to guarantee a near-ideal current source. Note that any other voltage current source can be used as long as the current can be set within a few hundred of nanoseconds. This short period of time for source driving is a necessary requirement for the suggested methodology described in chapter 2. A control FET gate driver with the capability of ultrafast rise and fall times was required to achieve this goal. It should also be able to provide short minimum pulse widths in few hundreds of micro seconds as described in chapter 2.

3.2.1 MOSFET Driver

An ultrafast MOSFET driver, IXDD415SI [30] is utilized to implement the driver circuitry. This 28 pin IC, as shown in figure 3.2, is a dual CMOS high-speed, high-current gate driver. It has been designed to drive the MOSFETs in class D and E, as well as other applications requiring short minimum pulse widths. Each output pin provides 4nF drive in less than 5ns, as well as up to 15 amperes source and sink peak current. By paralleling, the outputs can provide even higher current up to 30 amperes. Wide operating range of 8V to 30V is a great advantage of IXDD415SI over other drivers. Very short rise and fall times of less than 3ns along with the capability of providing short pulse width of 6ns introduces IXDD415SI as a good candidate for the proposed application. A typical performance characteristic for this 28 pin IC is shown in figure 3.3.

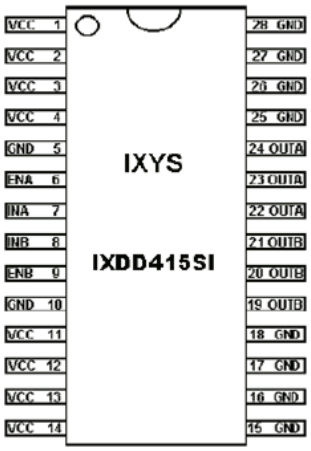
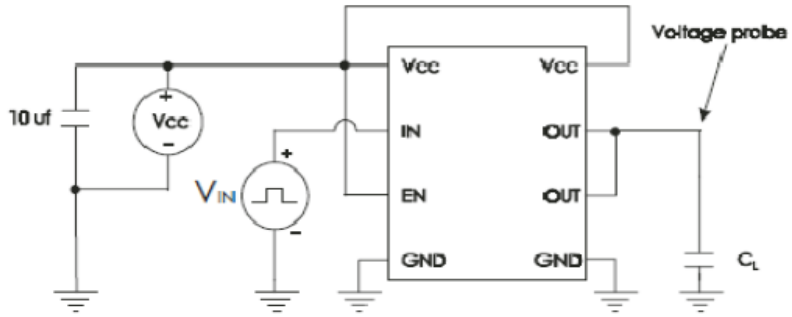
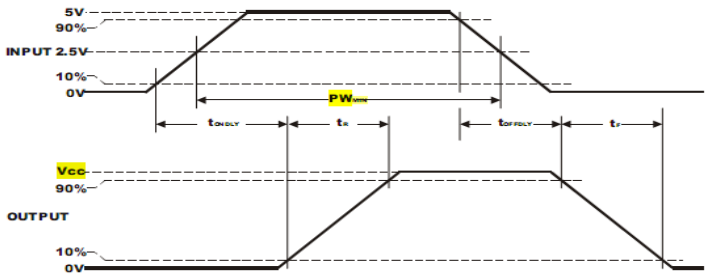


Figure 3.2: Pin configuration of IXDD415SI.

Inputs, INA and INB (see figure 3.2), should be driven by a Transistor-Transistor Logic (TTL) pulse which determines the pulse width of the output. The output pulse amplitude is controlled by the V_{CC} that limits driving each output channel independently. Separate input enables, ENA and ENB (see figure 3.2), and separate inputs, INA and INB, allow the user to drive each of the outputs for different pulse widths but with the same amplitude. The pulse width and V_{CC} should be controlled by a PC-controllable source to support the set up automation. To achieve this, TTL pulse is provided by the counter output of the DAQ. This will be discussed later in section 3.2.3. V_{CC} is controlled by one of the analog output channels of the DAQ Floating Source (FS) mode.



a) Characteristic test diagram



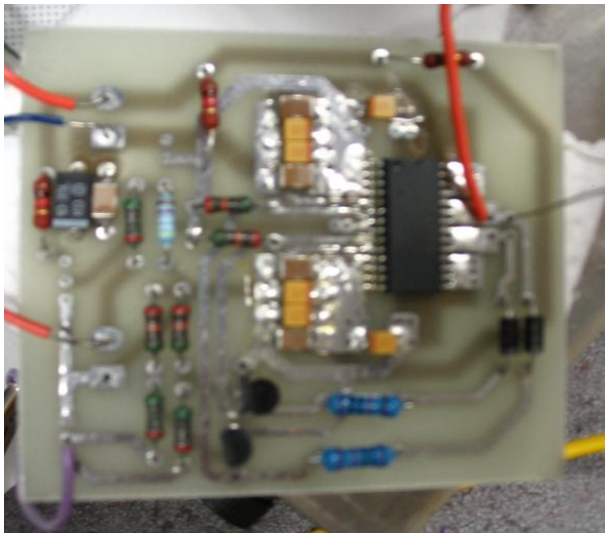
b) Timing diagram

Figure 3.3: Typical performance characteristic of IXDD415SI [30].

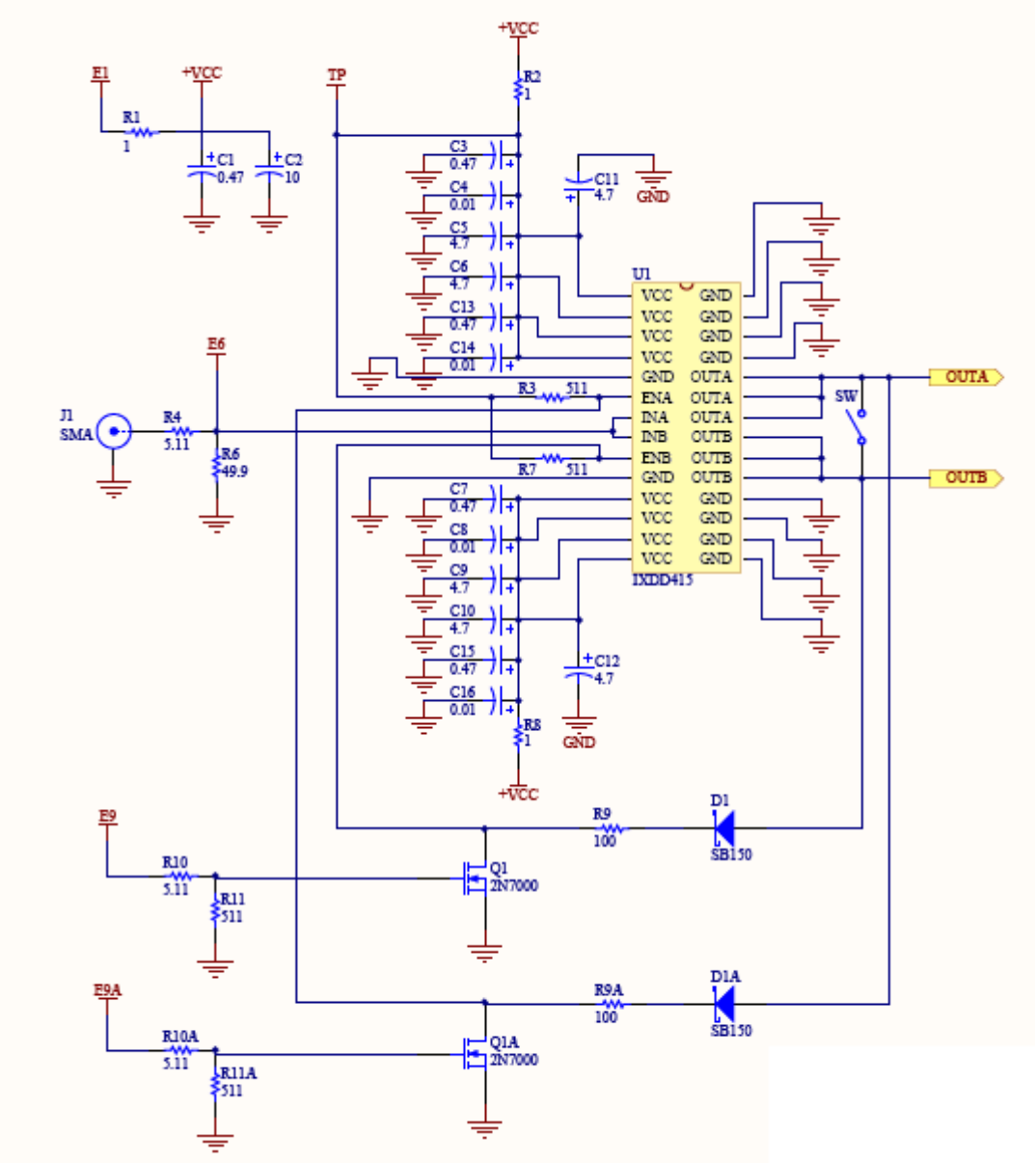
Due to very high switching speed while driving the gate, a considerable attention must be given to the circuit loop inductance, Vcc bypassing and grounding, Considering these parameters, Printed Circuit Board (PCB) is designed in such a way that the loop between the Vcc and Vcc ground is kept as minimum as possible to avoid the loop inductance.

- The power supply is bypassed to decrease the impedance between driver and power supply to turn on/off the control MOSFET properly.
- The grounding paths are as low as possible in resistance and inductance to turn off the load properly.

A photograph of the driver circuit and the schematic of the designed circuit are shown in figure 3.4.



a) Photography of PCB



b) Schematic

Figure 3.4: Gate driver circuit

3.2.2 Ground Isolation

The MOSFET current source is located in high side configuration. Therefore, it required to be driven by a high side gate driver to provide a floating voltage source as will be described in details in section 4.4. The IXDD415SI is a low side gate driver and all voltages are referenced to its GND. To employ this IC as a high side gate driver, its output should be floated. This means

that its GND requires being isolated from test gear's GND. To achieve this, the inputs should be driven by a floating source while the DAQ counter channel provides a ground-based output. Therefore, ground isolation is required. A 4N33optocoupler is employed that add a negligible delay to the system to provide GND isolation. The 4N33 optocoupler is a photo-darlington output with high speed switching and very high current transfer ratio as needed for the desired purpose [31].

3.2.3 Pulse Generation by DAQ

A TTL pulse is required to input the IXDD415SI. This pulse can be generated by Arbitrary Waveform Generator (AWG) or any other pulse generator. As the available AWG does not provide as low duty cycle as is necessary for the application, a DAQ counter is used. Difficulties regarding the counter-generated pulse are discussed in section 3.2.2. Although the DAQ analog output channels are capable of generating floating voltages, they can't provide microseconds duty cycles. Figure 3.5 demonstrates the developed LabVIEW program for pulse generation.

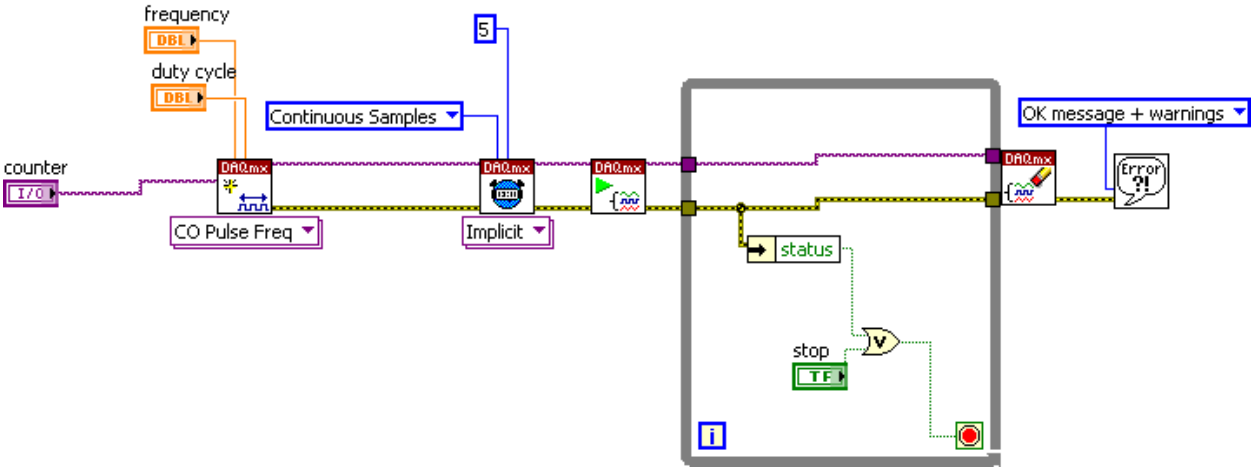


Figure 3.5: Developed program for pulse generation in LabVIEW environment.

3.3 Temperature Control Unit

The intrinsic behavior of semiconductors suddenly changes under high excitation sources due to self-heating. This indicates the importance of accurate temperature measurement and thermal modeling of semiconductors. Transient Thermal Impedance (TTI) is an indicator of self-

heating in semiconductors due to power dissipation. It can be found in the data sheet of the components based on the pulse width and duty cycle of the excitation input. It is used in measurement phase to calculate the junction temperature of the DUT. All temperature measurement should be performed with respect to a reference point. The device junction temperature should be calibrated to a constant value before any excitation is applied. Having a constant reference temperature is impractical due to existence of thermal impedance between junction and case and case and ambient. This introduces a measurement error which is further increased due to inaccuracy of temperature sensors. However, the cumulative error due to these factors is between 2%-3% and can be neglected [33].

One solution to provide constant reference temperature includes a copper-water cooled heatsink with two drilled holes to hold two thermocouples. One is used to measure the junction temperature and the other one is used to monitor heatsink temperature [33]. Another solution is to employ a closed loop temperature controller by application of a proportional integral-differential (PID) controller. In this work, the latter solution is utilized. A software-based PID controller and peltier module is used to provide both heating and cooling options.

Temperature control designed to monitor and maintain the junction temperature of the DUT at a desired constant value. It consists of the following parts:

- Peltier Module which is used as a heater/cooler;
- Heatsink where a DUT and a peltier module are mounted;
- Thermocouple which is used to measure the heatsink temperature;
- Transmitter which converts temperature to voltage;
- Data acquisition system as an interface between hardware and LabVIEW environment;
- Developed LabVIEW program which simulate a PID controller

The block diagram of temperature control system is shown in figure 3.6.

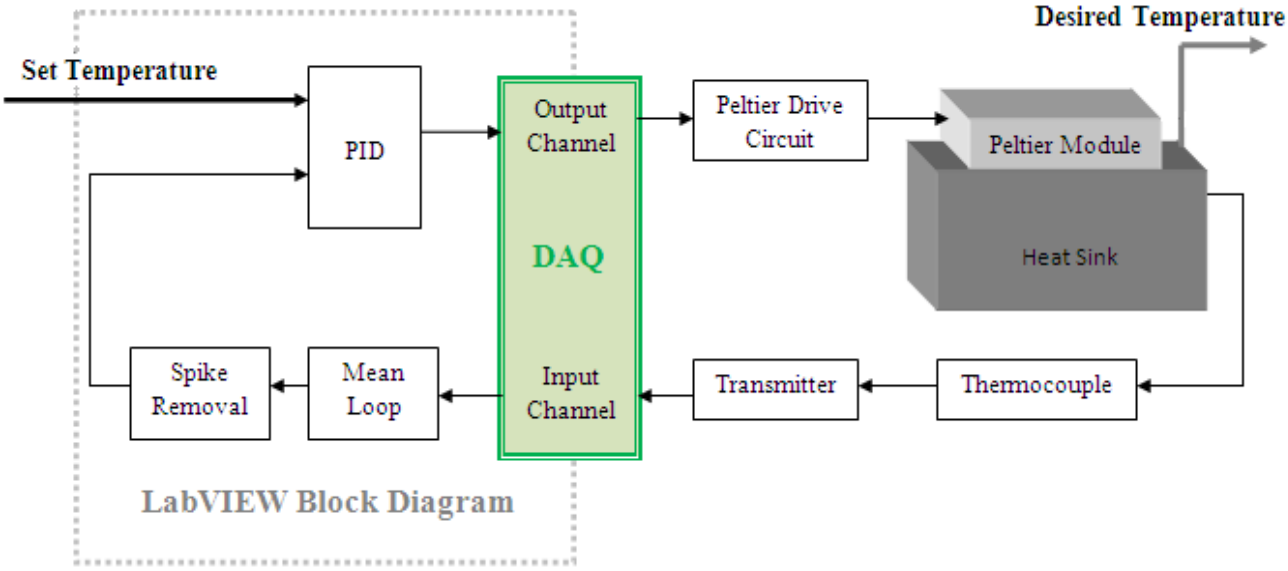


Figure 3.6: Block diagram of the developed temperature control system.

3.3.1 Peltier Module

3.3.1.1 Peltier Theory and Module Structure

Peltier module, also known as Thermoelectric (TE) module, is a small solid state device that can operate as a heat pump. The module function is based on the Peltier effect which is discovered by Jean Peltier early in 19th century [34]. He found that passing current through two dissimilar electrical conductors causes heat absorption or generation at the junction of the materials.

The development of this phenomenon requires semiconductors which are very good conductor of electricity but poor conductor of heat. To achieve this, semiconductors should be doped heavily either positive or negative. Bismuth and telluride are used for this purpose. Figure 3.7 shows a Peltier module as a combination of these P/N pairs (couples). They are serially connected to conduct electricity and sandwiched between two ceramic substrates.

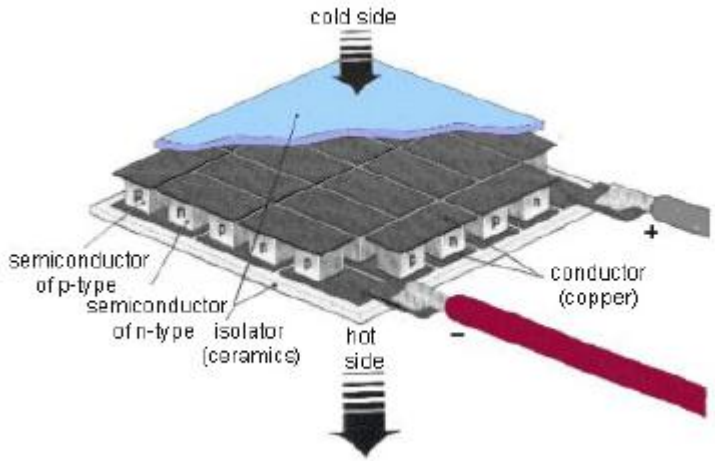


Figure 3.7: Peltier module.

As shown in figure 3.8, applying a DC voltage across a Peltier module causes a flow of carriers in couples where by they absorb energy from one substrate and release it at the opposite side. The surface that energy is absorbed from becomes cold and the other surface becomes hot. Reversing the polarity of the power supply results in the reversed hot and cold sides.

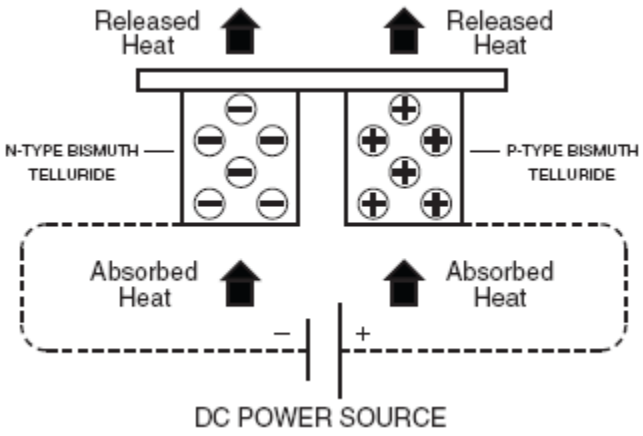


Figure 3.8: Exciting a Peltier module.

The heat transferred to the cold side should be removed by attaching an appropriate heatsink. Otherwise, the cold side can keep the temperature difference with hot side and do not stay cold for a long time and module goes down.

The amount of heat pumped through the TE module is directly proportional to the supplied power. This is true as long as the temperature difference between two sides do not exceed the

maximum rated. For each module, the maximum electric current (Imax) and voltage (Vmax) are defined in the datasheet. However, these values are not absolute maximum rated values. In fact, the maximum performance efficiency happens around the 80% of theses maximums. Performance can be temperature difference, heat pump at cold side or a combination of both. Figure 3.9 shows performance versus input power. Most modules operate near-linearly between 40% and 80% of input power max. This behaviour especially happens when they are controlled by a closed-loop temperature controller. Exceeding the maximum rated values causes more joule heating and less heat absorbing as well as possible reverse diffusion [35].

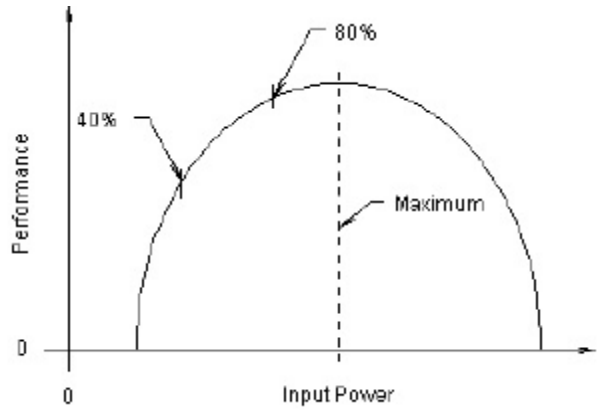


Figure 3.9: Performance curve of a Peltier module versus input power.

3.3.1.2 Temperature control of the Peltier module

To drive a Peltier module, a DC voltage supply with AC ripple not more than 10% is required. There are a number of control solutions to control the module temperature. They includes on-off control signal, pulse width modulation control by frequency above 1 kHz or 2 kHz and closed loop control .The best solution is to use a closed-loop control using temperature sensor feedback. This method can provide accuracy up to 0.1^0C. The closed-loop control method, briefly described in the sections 3.3.5 and 3.3.6 is used in this research work.

3.3.1.3 Thermal Grease

Heat must be transferred from the object (Aluminium block in this work, see section 3.3.3.6) being cooled (heated) to the Peltier module and from module to heatsink. Realistically, theses surfaces are not perfectly flat. The peaks and valleys on them cause flow of air which is a poor

heat conductor and decreases the operation efficiency as shown in figure 3.10 [36]. Thus, any surface as a part of a thermal interface should be flat to +/- 0.001 inches over the entire surface and smooth to a surface finish of 32 micro inches or better. If possible a polished surface finish of #6 to #8 is very helpful to decrease the size of the peaks and valleys.

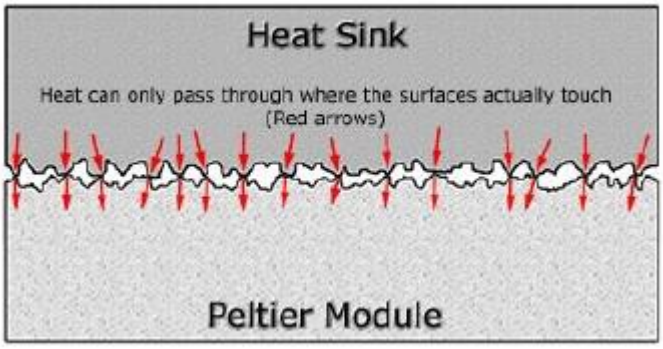


Figure 3.10: Peaks and valleys on the contact surfaces [36].

Thermal Interface Material (TIM) is used between the Peltier module surfaces and what is mated to them. The purpose is to fill microscopic surface imperfections with compressible material that has a much higher thermal conductivity than the air gaps as shown in figure 3.11 [36].

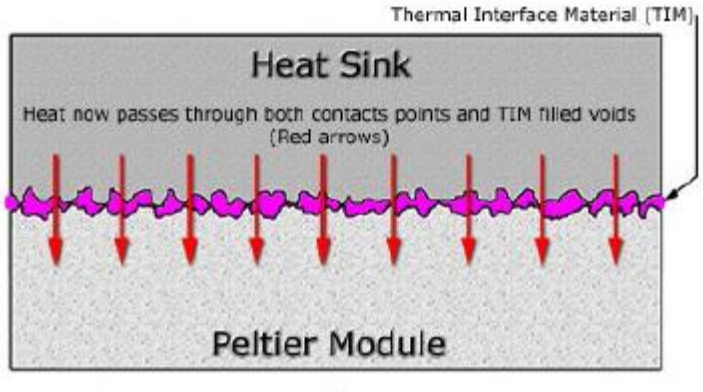


Figure 3.11: TIM application increases the surface contact and thermal conductivity.

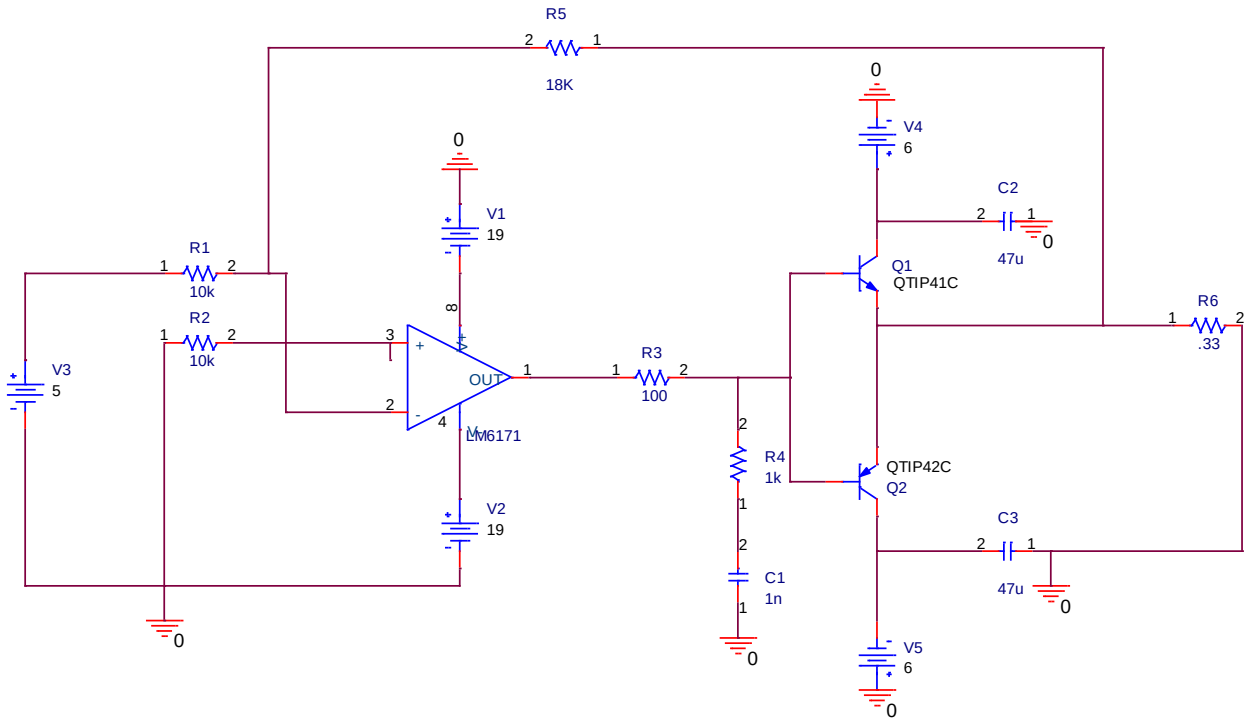
There are silicon-based greases, elastomeric pads, thermally conductive tapes, adhesives, and so on that can be used as TIM. In this work, silver-based grease having high conductivity in comparison with silicon-based greases is used.

3.3.1.4 Peltier Drive Circuit

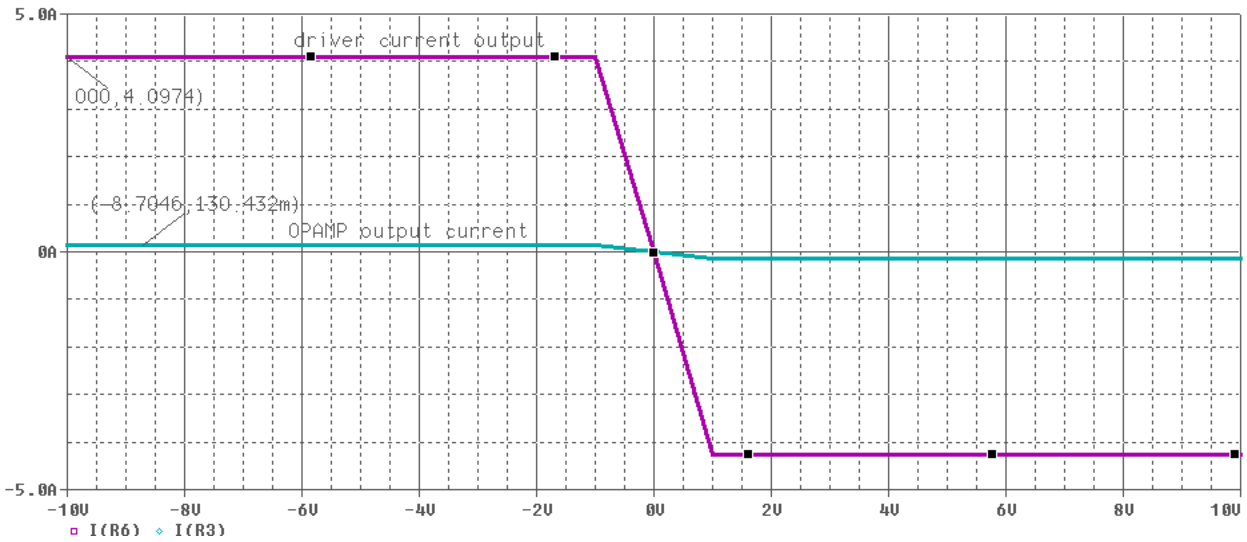
The Peltier drive circuit is used to supply the module with a constant current. This circuit consists of two stages including voltage amplifier and current amplifier to provide a constant current of ± 4 amperes. The voltage amplifier consists of a high output current Op-Amp (LM6171) inputted by output channel of a DAQ to automate the control set up by LabVIEW based temperature controller.

The current amplifier employs two power BJTs (TIP41A and TIP42A) in totem pole configuration. According to the Peltier specifications, the output current can be limited by adding a resistor. The amplifier gain is adjustable by feedback resistor.

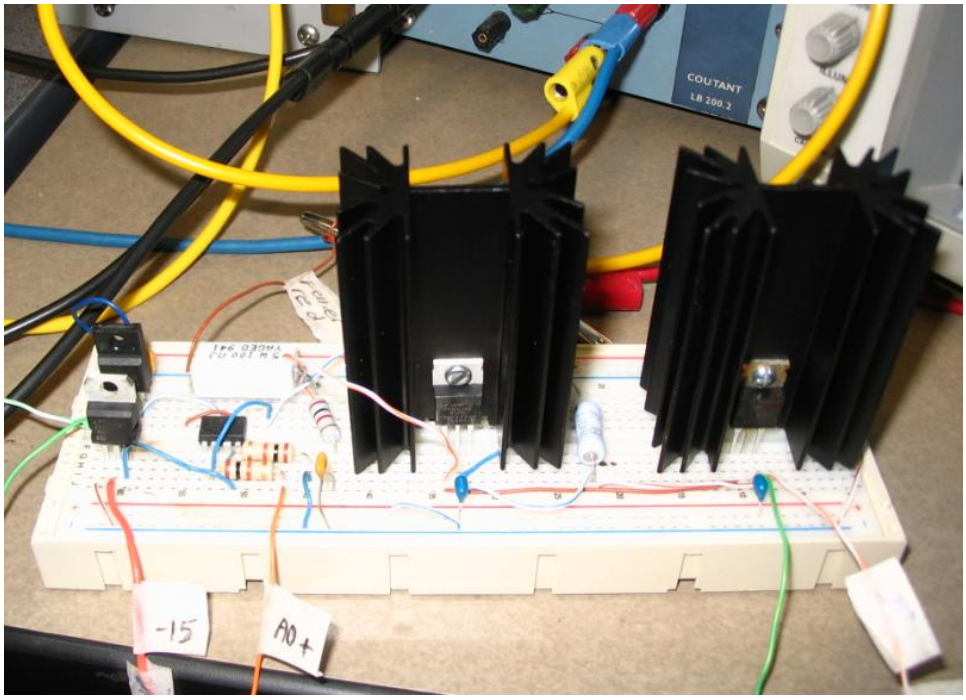
Figure 3.12a-b illustrates both schematic and output results of the drive circuit in PSpice, respectively. Figure 3.12c shows a photograph of the implemented board.



a) Schematic representation in PSpice



b) Output results in PSpice



c) Photograph of the Board

Figure 3.12: Peltier drive circuit.

3.3.1.5 Module Selection

The Peltier module CP60333 is selected for the proposed temperature control. It is rated for Imax=6A, Qmax=50.5Watt, Vmax=15.4V, ΔTmax=60^0C, and Tmax=66^oC. This module has the highest maximum power for the Imax that the chosen driver can provide.

Thermoelectric modules can be used as both heater and cooler. Peltier module is used to control the junction temperature of the DUT and mostly used as a heater. The module is powered with adverse polarity i.e. the positive side of the input power is applied to the negative side of the module. Therefore, the so-called hot plate starts to become cold and the so-called cold plate starts to warm up. A large cold sink on the cold side is employed to keep drawing in more heat from the air.

As shown in figure 3.13, two heat sinks, the Al block (HS1) and a fined heatsink (HS2) are used. HS1 is supposed to be heated up and heats the DUT which is mounted on one of the block sides. Two holes are made on both heat sinks as close as possible to the edge of the sides where two plates of the module are mounted.

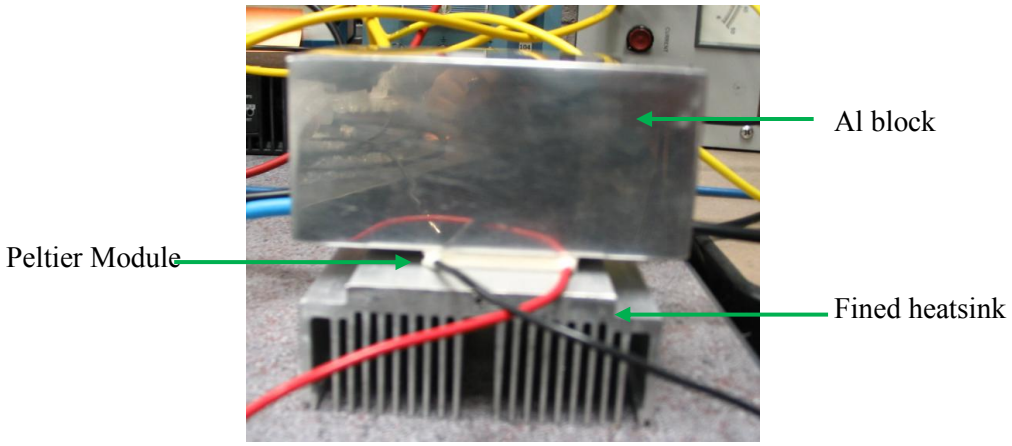


Figure 3.13: Photograph of a Peltier module and heatsinks.

3.3.2 Thermocouple and Temperature Transmitter

Three temperature sensors are used to measure the temperature. Two of them are placed through the holes inside of each heatsink (HS1 and HS2) close to the sides of the Peltier module. They are used to measure the temperature difference between two plates of the module to avoid

exceeding the maximum allowed temperature difference. Both of them are K-type thermocouples. A hand-held thermometer (model HH-23A from OMEGA Engineering) is used to monitor the temperature readings. The thermometer has the accuracy of 0.1% with reading rate of one per second. As the available thermometer is not pc-controllable, the temperature difference should be monitored by user to avoid any failure in the system.

The third temperature sensor, a J-type thermocouple, is a part of the PID controller set up. A 502A-J thermocouple transmitter connected to the thermocouple converts the temperature to the voltage signal. The voltage is then acquired by the DAQ board to automate the system. This sensor measures the heatsink temperature at the location where the DUT is mounted as shown in figure 3.14.

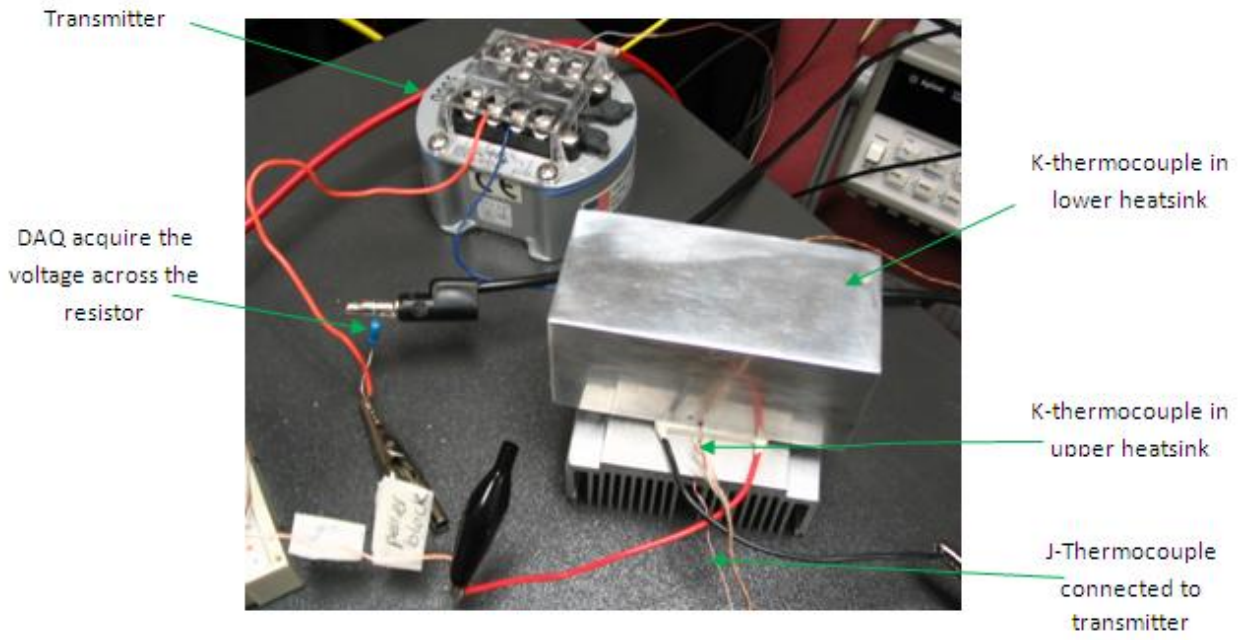


Figure 3.14: Temperature sensor and transmitter.

The 502A-J temperature controller is able to convert the input voltage range in micro order to 4-20 mA. This current causes a voltage drop across a 10 ohm resistor. The dropped voltage is measured by the analog input channel of the DAQ. The LabVIEW subroutine for virtual instruments (sub-VI), V2T converts the measured voltage to the corresponding temperature which later is fed to the developed PID-LabVIEW program.

The transmitter is calibrated for the range of -20 to 180^0C. This is the smallest range that satisfies the set up requirements. The calibration is performed with respect to the ambient temperature as a reference temperature. A DC voltage source, Yokogawa 7651, with accuracy of 10μv is used for the calibration. The voltage adjustment error and the temperature measurement error are negligible (2% and 0.14%, respectively).

3.3.3 PID Temperature Controller Design

A PID controller is designed using the LabVIEW development environment to control the heatsink and consequently junction temperature. The mathematical algorithms of a PID controller is described as:

$$V_{out}(t) = K_p e(t) + K_i \int e(t)dt + K_d \frac{de(t)}{dt} \quad 3.1$$

$$K_i = {K_p}/{T_i} \qquad K_d = {K_p}/{T_d} \quad 3.2$$

where e(t) is the input error. K_p, K_i, and K_d are coefficients of proportional, integral, and derivative gains, respectively. T_i and T_d are integral and derivative action time [37].

The integral LabVIEW sub-VI is employed to calculate the integral of e(t) based on the trapezoidal method as shown in figure 3.15:

$$\int_0^n e(t)dt = \sum_{k=0}^{n} \left(\frac{e(KT) + e[(k+1)T]}{2} \right) T \quad 3.3$$

A boolen parameter to verify whether the PID output lies in the desired limit is included in the PID LabIEW program. If it does, the result is added to the previous summation. Otherwise, zero is added and the previous summation is extracted to avoid PID saturations. As a result, the integral output remains constant until the PID output lies within the range.

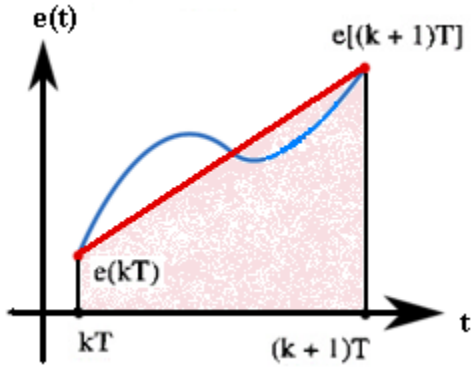


Figure 3.15: Trapozoidal method.

The derivative LabVIEW sub-VI is utilized to calculate the the derivative of e(t) based on the backward difference method. According to equation 3.4, the prvious processing value is sustracted from the current value and the result is divided by sample time.

$$\frac{de(t)}{dt} = \frac{e(KT) - e[(k-1)T]}{T} \qquad 3.4$$

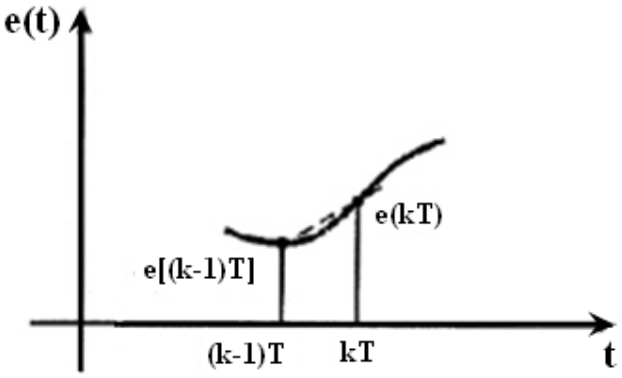


Figure 3.16: Backward difference method.

The tick count function is applied to compute the time interval between every two samples. The first sample is refernced to the start time value measured from the moment the PID code is called (elapsed time). As this value might be large for the first iteration, it is compared with an arbitrary value. As shown in figure 3.17, in every iteration, this time difference is stored in a

variable to be used in the next iterations. The developed PID labVIEW program is used in the main code described in the next section.

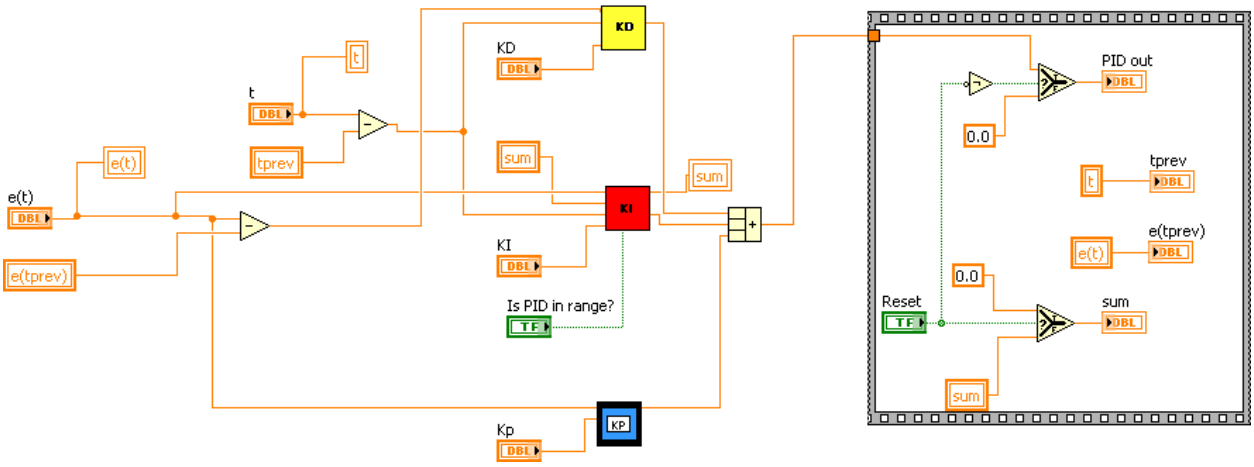
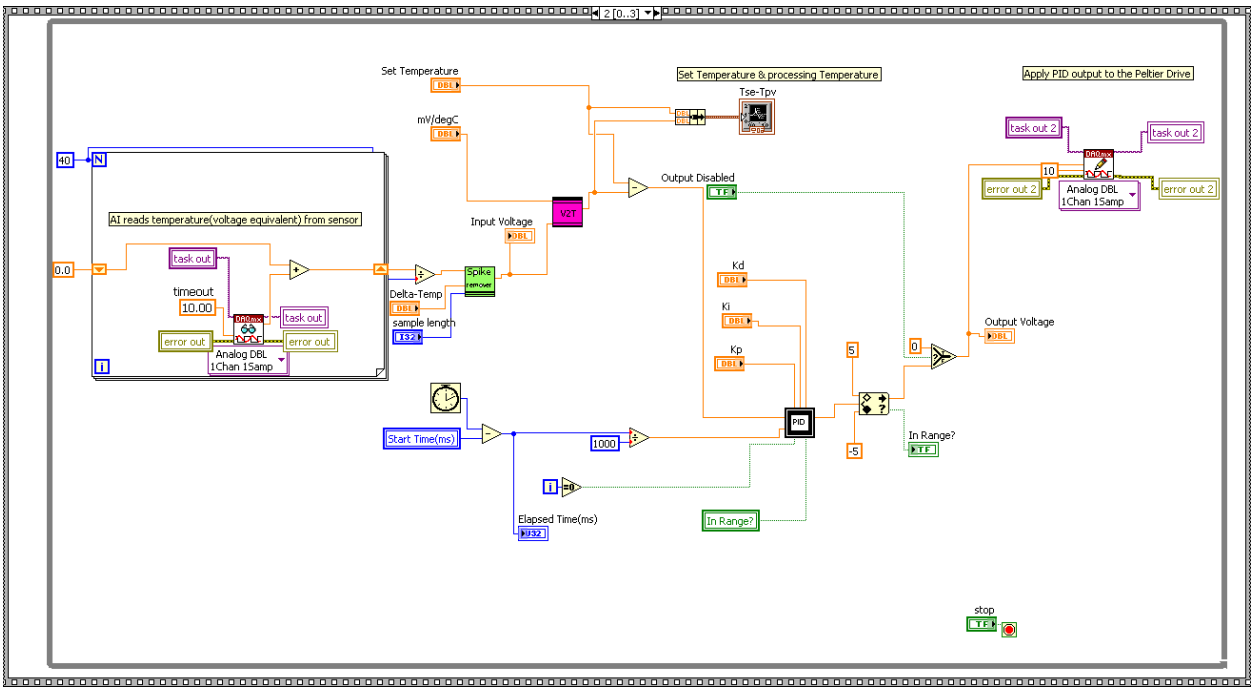


Figure 3.17: PID controller in LabVIEW.

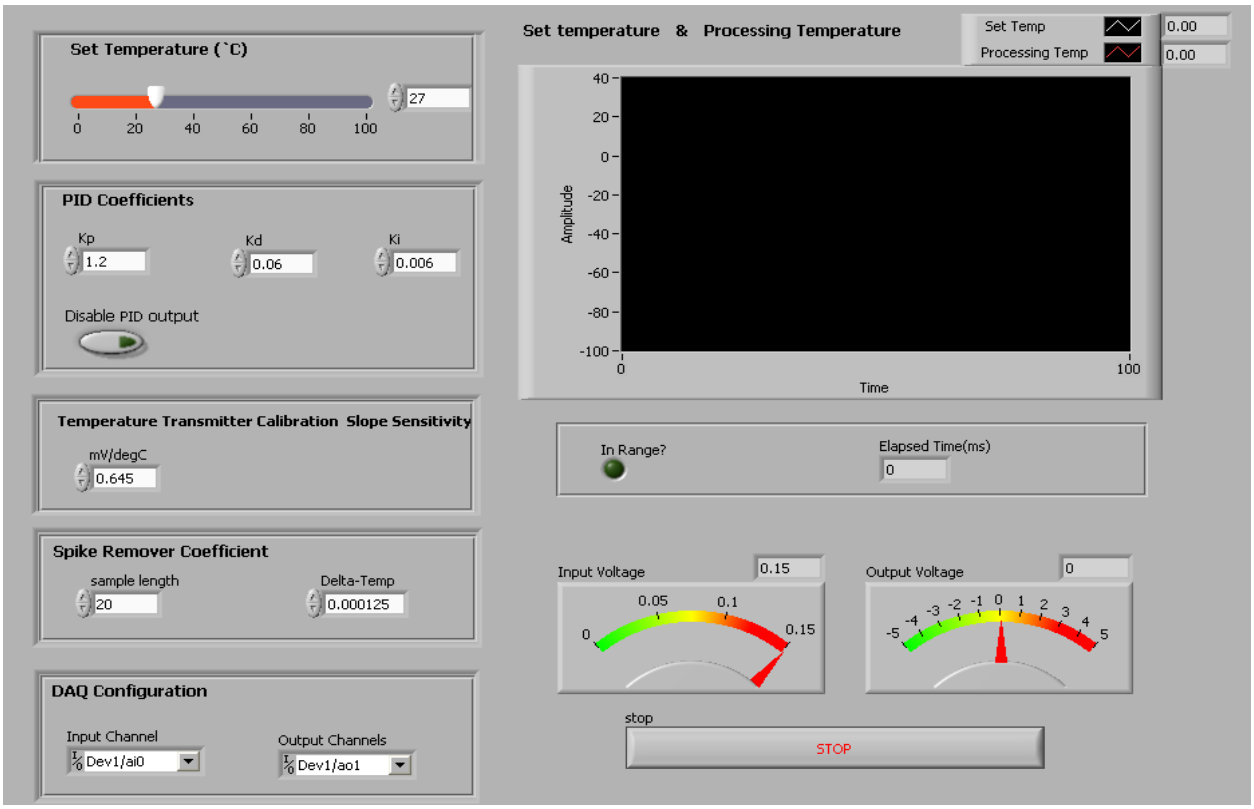
3.3.4 Temperature Controller Design in LabVIEW

A LabVIEW program was also developed for the temperature controller. This program consists of four sequence frames. In the fisrt frame, the analog input and output channels are initiated. The input channel is used to acquire voltage across the resistor in transmitter circuit. The output channel is used to control the input voltage of the Peltier drive circuit. In the second frame, tick count function is used to return the internal timer of the CPU. This is used to calculate the time increment (Δt) for the fisrt iteratoion calculations in the PID sub-VI. The third frame includes the main part of the temeperature controller design which is described in details in section 3.3.7. In the last frame, the volatge masurement and generation tasks are cleared to make the sources free.

The third frame of the developed LabVIEW program is shown in figure 3.18a-b. The block diagram of the developed program is shown in figure 3.18a. Several voltage samples from the transmitter are read and averaged to eleminate the effect of high frequency noises. The output is passed to the Spike remover sub-VI to eleminate the spikes and outliers related to the temperature transmitter. The procedure is as follows: The mean value of voltages is calculated



a) Block diagram



b) User interface

Figure 3.18: Main code for temperature controller in LabVIEW.

continuously. Any temperature deviation from the mean value by a specified value, is substituted by the mean value. The voltage output is then passed to the LabVIEW V2T subroutines (see section 3.3.4) and is converted to the corresponding temperature. This temperature (as a processing variable) is substracted from the set temperature. The result is the error function that is fed to the PID sub-VI. The output is verified to see whether it passes the specified limits as described in section 3.3.5 . The output is transfered to the analog output channel of the DAQ. The user interface for temperature controller is illustrated in figure 3.18b. The PID coefficients, set tempearture, DAQ channel selection and transmitter senistivity scale can be changed through the user interface.

3.3.5 How Temperature Control System Works

The temperature of the heatsink is measured by the thermocouple at the location where the DUT is mounted. A transmitter is used to convert the temperature to voltage signal. The voltag is acquired by input channle of the DAQ. The PID controller provides the appropriate voltage for Peltier drive circuit that drives Peltier module to the desired temperature. As a result, the temperature of the heatsink is increased/decreased and the junction temperature reaches to the desired value.

3.4 Other Parts

3.4.1 DAQ

The PID temperature controller is implemented on a PC in LabVIEW environment using NI PCI-6052E data aquisition system. This multifunction DAQ provides 16 analog input and 2 analog ouput channels with 16 bits resolution and sample/update rate of 333KS/s [25].One of the input channels is used for voltage measurement of temperature transmitter circuit. Two DAQs are needed as four output channels are required to feed enable pins of the IXDD415SI, the DUT's gate and Peltier drive circuit. One counter channel is employed to provide the digital pulse input for IXDD415SI.

3.4.2 DUT's Gate Driver

Although the DUT is placed in low-side configuration, it is necessary to drive the gate by a floating source to keep the gate-source volatge constant while the drop voltage across sensing resitor is high. For this purpose, a 7851-YOKOGAWA programmable DC source through a general purpose interface bus (GPIB) and LabVIEW Driver[39].

~~one of the analog output channels of the DAQ is employed in Floating Source (FS) mode.~~

3.4.3 Oscilloscope

A digital osciloscope is employed to measure the drain-source voltage (V_{DS}) across the DUT and V_R across the current sensing resistor during the measurement phase.

3.5 Summary

In this chapter, the trace circuit set up was described in detailes. The proposed set up includs five main parts: CPU/PC, voltage ramp control unit, temperature control unit, gate voltage control unit and oscilloscope. Developed stategies for the voltage ramp and temperature control units were discussed in detail. LabVIEW is used as a development platform to provide application interface, desgin controllers, develop the measurement strategies and monitor & control instrumenstation system. The limitations and difficaulties related to the selected components and corresponding errors were studied.

CHAPTER 4

Test Board

4.1 Introduction

The main parts of the test board are introduced in this chapter. The implementation of each part has also been described. Figure 4.1 depicts the block diagram of the test board.

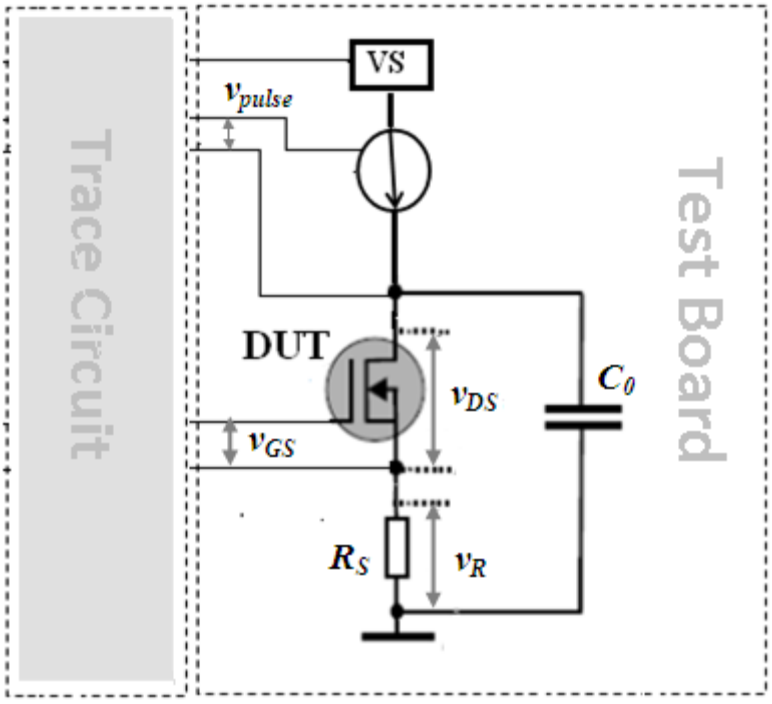


Figure 4.1: Test board block diagram.

The test board is composed of five main components as follows:

1. *PC-controllable high current power supply* to drive the current source and the DUT, rated for high currents depending on the DUT.

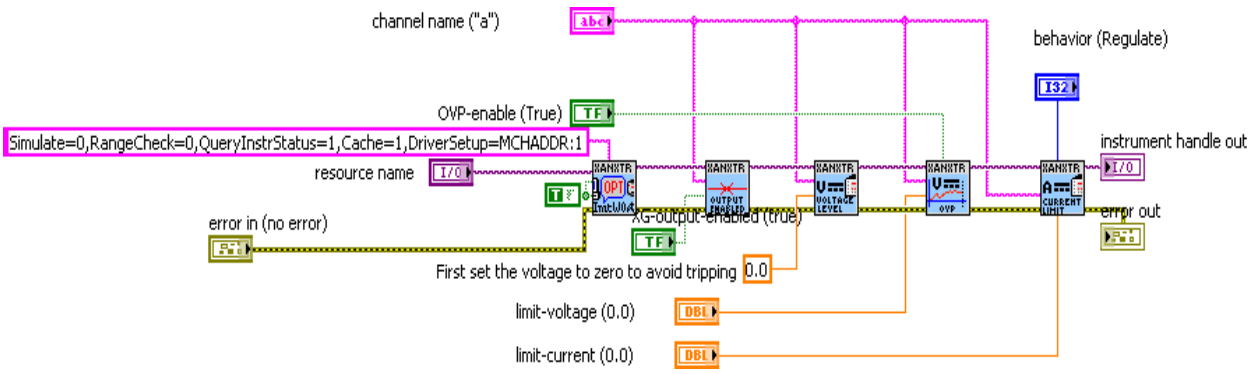
2. *DUT*
3. *Current source* to provide constant current to charge a capacitor.
4. *Current sensing resistor* to measure the current flows in the DUT.
5. *Capacitor* used as a ramp voltage source to drive the DUT.

4.2 PC-controllable High Current Power Supply

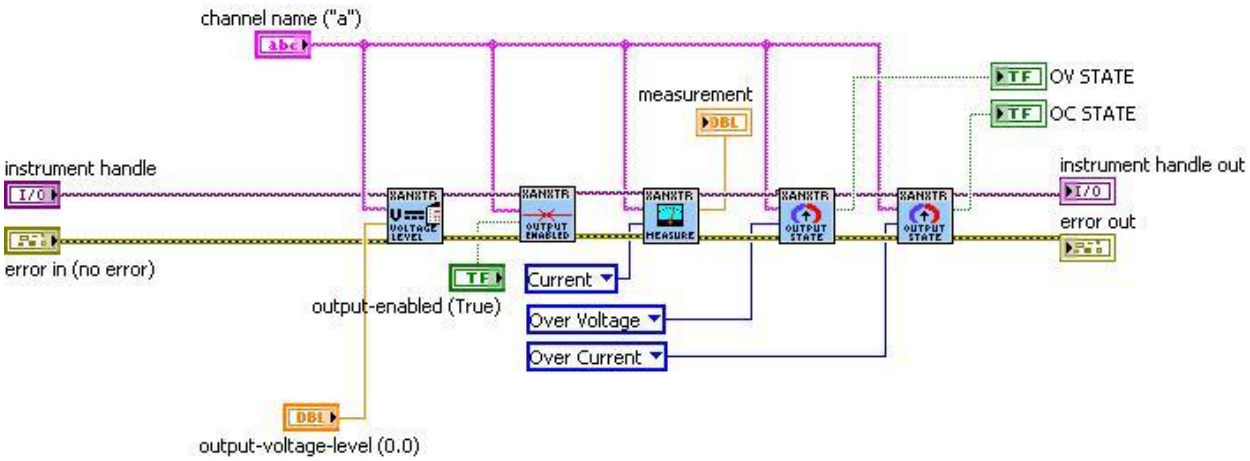
Power supply along with *voltage ramp control unit* (see section 3.2) adjusts the current of current source depending on the region that the DUT is working. Therefore, it should be remote-controllable.

A power supply of model XG-100 from Xantrex has been used. This PC-controllable high current power supply may provide a maximum voltage and current of 8V and 100A, respectively [38].

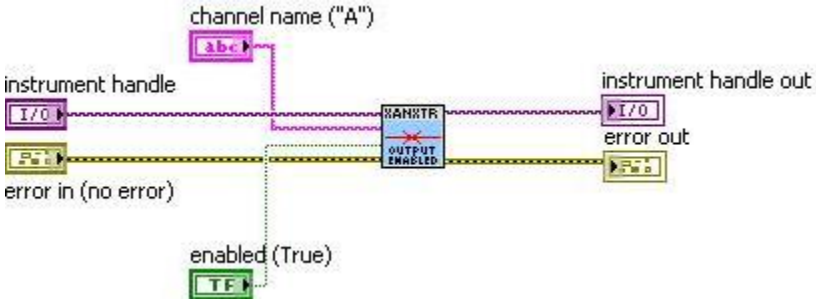
Several subroutines for virtual instruments (sub-VIs) are developed in LabVIEW development environment to drive the power supply during the measurement procedure. These sub-VIs initialize the instrument (figure 4.2a) for the appropriate ranges (figure 4.2b) at the beginning of the main program (section 5.7) and allow the user to enable and disable the output (figure 4.2c) during different steps of the measurement procedure. Figure 4.2a-c depicts the developed sub-VIs in LabVIEW environment.



a) Initialization



b) Adjust the output



c) Enable/disable the output

Figure 4.2: Developed LabVIEW program for XG-100.

4.3 DUT

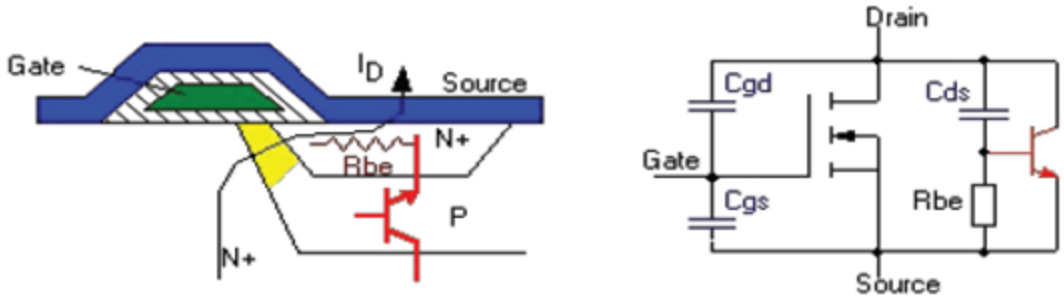
A power transistor has been used as switching element. For this reason, they are employed in saturation region, resulting in a low on-state voltage drop. It is important to highlight especially for power application, that MOSFETs have a resistive nature. The voltage drop across the drain source terminals of a MOSFET is a linear function of the current flowing in the semiconductor. This linear relationship is characterized by the $R_{DS(on)}$ of the MOSFET and known as the on-resistance. On-resistance is constant for a given gate-to-source voltage and temperature of the device. As opposed to the -2.2mV/°C temperature coefficient of a p-n junction, the MOSFETs exhibit a positive temperature coefficient of approximately 0.7%/°C to 1%/°C. This positive temperature coefficient of the MOSFET makes it an ideal candidate for

parallel operation in higher power applications where using a single device would not be practical or possible. Initial tolerance in $R_{DS}(on)$ values and different junction to ambient thermal resistances can cause significant error in current distribution up to 30% .

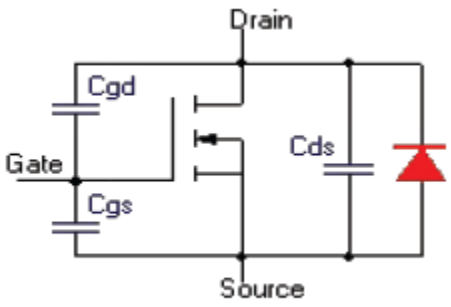
The switching speed of modern transistors is much higher than that of thyristors and they are extensively used in dc-dc and dc-ac convertors. However, their voltage and current ratings are lower than those of thyristors and transistors which are generally used in low-to-medium-power applications [40].

Among power transistors, high power MOSFET is of interest in this research work. A power MOSFET is a voltage-controlled device and requires only a small input current.

Without any gate signal, an enhancement power MOSFET may be considered as two diodes connected back to back or as an NPN-transistor. The gate structure has parasitic source and drain capacitances C_{GS} and C_{GD} respectively. The NPN- transistor has a reverse-bias junction from drain to the source and offers a capacitance, C_{DS}. The parasitic capacitances depend on their respective voltages. The equivalent circuit of a parasitic bipolar transistor in parallel with a MOSFET is shown in figure 4.3(a). The base-to-emitter region of an NPN-transistor is shorted at the chip by metalizing the source terminal and the resistance from the base to emitter due to bulk resistance of N and P-regions (R_{be}) is small.(see figure 4.3(a)). Hence, MOSFET may be considered as having an internal diode with the equivalent circuit as shown in figure 4.3(b) [41]. The parasitic diode does not have the structure of a fast diode and must be neglected and a separate fast diode used in a high speed switching circuit [40]



a) Parasitic bipolar



b) Internal diode

Figure 4.3: Parasitic model of enhancement power MOSFET.

CDS=Coss-Crss
CGS=Ciss-Crss

C_{GS} a[illegible]o the actual geometry of the device while the C_{DS} capacitor is the capacitanc[illegible]r diode of the parasitic bipolar transistor. These capacitors values are given i[illegible]ly by C_{iss}, C_{rss}, and C_{oss} and must be calculated as:

$$C_{GD} = C_{rss}$$

$$C_{GS} = C_{iss} + C_{rss}$$

$$C_{GS} = C_{iss} + C_{rss} \quad (4.1)$$

The switching speed is very high and the switching times in the range of nanoseconds. The turn-on time of an MOSFET depends on the charging time of the input or gate capacitances [42] The gate current to charge the gate capacitance should be controlled by a RC/R network in gate terminal [41,43] otherwise a high current may lead to increased electromagnetic interference (EMI) due to rapid turn-on and turn-off. Figure 4.4 shows a gate circuitry. One of the resistors is to control the turn-on time and the other to control the turn-off time. A diode is used to separate the two functions, but it can be omitted in some cases if the timing is less critical [44] In this work, two adjustable 1K resistors along with a Schottky barrier 1N5817 diode have been used[45].

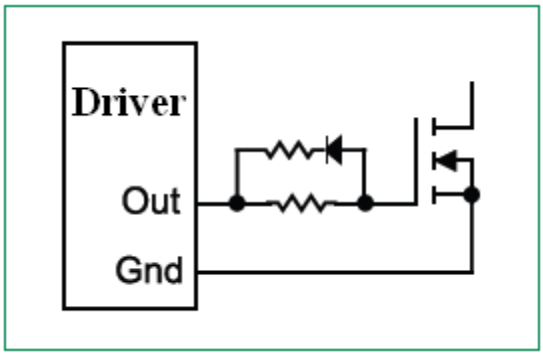


Figure 4.4: Gate circuitry.

4.4 DUT Selection

Fairchild FDD8780 [45] is a N-channel power MOSFET which is used as the DUT. It is rated for maximum drain-source voltage of 40V and drain current of 35A. The very low on-state resistance of 8.5mΩ provides less power loss during switching period. Figure 4.5 shows normalized on resistance versus junction temperature.

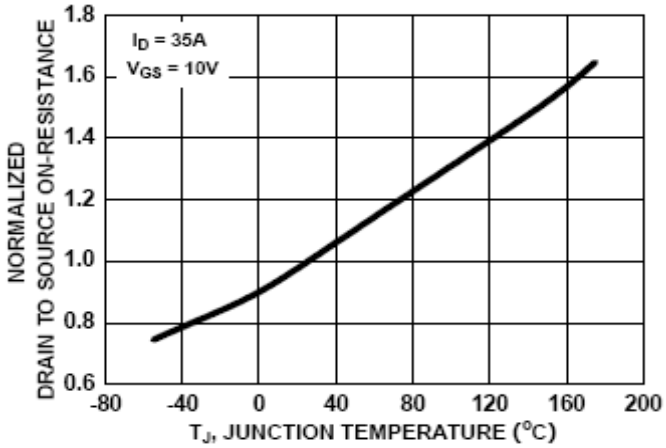


Figure 4.5: Normalized on resistance versus temperature

As it can be seen and described in 4.3, the on-resistance is strongly temperature dependent. Also the VGS and ID are constant but the normalized on-resistance has a significant change. Therefore, measurement of the on-resistance in ohmic region is challenging and should be performed before the temperature rise starts, i.e. in the lower currents (see section 5.6).

Drain current is the other temperature dependent parameter of a transistor that should be measured during the characterization. Figure 4.6 shows the drain current dependency on both

gate voltage and temperature. It can be seen that, with the same gate voltage, the drain current is different for various junction temperature. Thus, to fully characterize the device, the I-V curve should be measured in different junction temperatures. This option is provided in this research work, by a PID temperature controller that adjusts the junction temperature (see section 3.3) to the desired value.

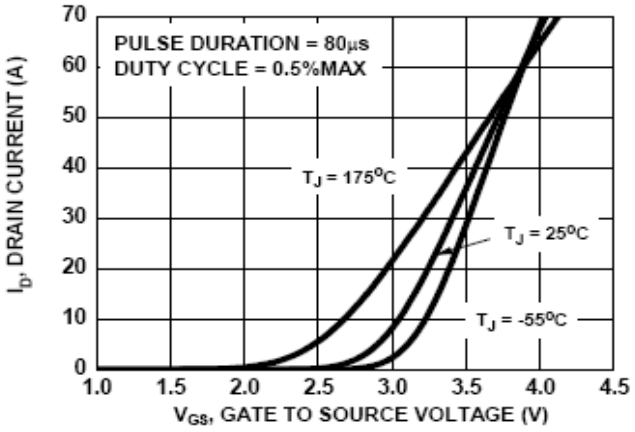


Figure 4.6: Transfer characteristic

The transient thermal impedance of the DUT from junction to mounting base as a function of pulse duration is shown in Figure 4.7. Figure clearly shows the effect of time interval that DUT is stimulated; as the applied pulse width gets higher, thermal response of the device gets higher as well, in other words the junction temperature rise gets higher. This demonstrates the importance of the selected duty cycle and pulse width to characterize the device.

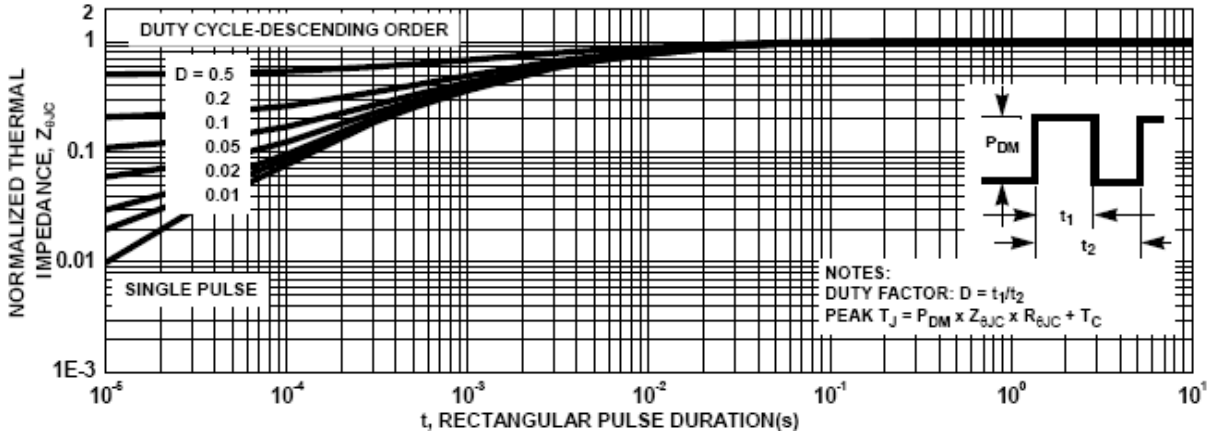


Figure4.7: Transient thermal response curve

Figure 4.8 shows the forward bias safe operating area (SOA). Based on the proposed measurement approach (see chapters 2 and 5) that uses pulse width of excitation in microseconds order, the DUT can be driven in very large area.

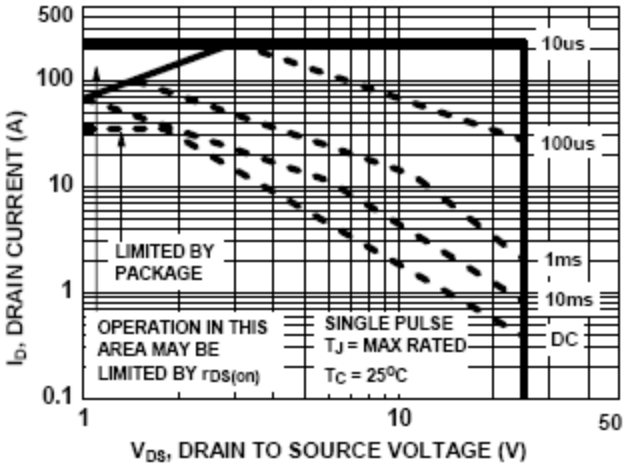


Figure 4.8: Forward bias safe operating area.

4.5 Current Source

The measurement technique requires providing a voltage ramp source to excite the DUT. The proposed methodology uses capacitor charging with constant current to provide this ramp source. The magnitude of this current should be adjustable in desired range. This allows the control of the charging slope.

In this research work, a voltage controlled open loop current source is used. It is implemented by utilizing a power MOSFET which is driven into saturation region, resulting in a low on-state voltage drop. For this purpose, a FDD8780 power MOSFET with an appropriate gate driver (see 3.2.1) is employed. Small size of on-state resistance along with low conduction losses of this transistor provides a suitable choice for the desired purpose [45].

4.6 Current Sensing Resistor

A current sensing resistor is used to monitor the current in a circuit and translate the amount of current in that circuit into a voltage that can be easily measured and monitored. It is designed for low resistance as well as minimizing the power consumption.

A sensing resistor of 0.1Ω is used in the proposed test board set up. It is appropriate for lower currents up to 10A but for higher currents, a smaller resistor should be employed.

4.7 Capacitor

A capacitor can be charged and discharged using a constant current *I*. The voltage drop across a capacitor can be written as equation 4.1.

$$V_c(t) = \frac{1}{C}\int_0^t i_c(t)dt + V_c(0) = \frac{1}{C}\int_0^t I\,dt + V_c(0)$$

4.2

Therefore, for a constant current $i_c(t)$ the capacitor charges linearly according to the equation 4.2.

$$V_c(t) = \frac{I}{C}.t + V_c(0)$$

4.3

Thus, the rate of charge depends on the current magnitude and the capacitance. The time that takes for the capacitor to charge to a certain voltage is given by:

$$t_{Charge} = \frac{C \times [V_{target} - V_c]}{I}$$

4.4

where V_{target} is the voltage to reach.

4.7.1 Capacitor Selection

A 100nF ceramic capacitor (SMD X7R) is chosen. The capacitor is connected across the DUT (see figure 4.1) to provide the drain-source voltage in almost linear fashion.

Based on the proposed methodology presented in chapter 2, the capacitor is charged with a constant current according to the equation 4.3. As a result, the slope of the charging voltage of the capacitor is proportional to *I* and *C* where *I* is the constant current of the current supplier discussed in section 4.7. The variation of the value of the capacitor versus temperature should be minimal, since that would affect the slope. Thus, a X7R ceramic capacitor is chosen. It has a

±15% change over -55^{0}C to +125^{0}C and standard tolerance of 10% [46]. Figure 4.9 shows a typical X7R temperature coefficient graph. It can be seen that the temperature coefficient at 25^{0}C is almost zero.

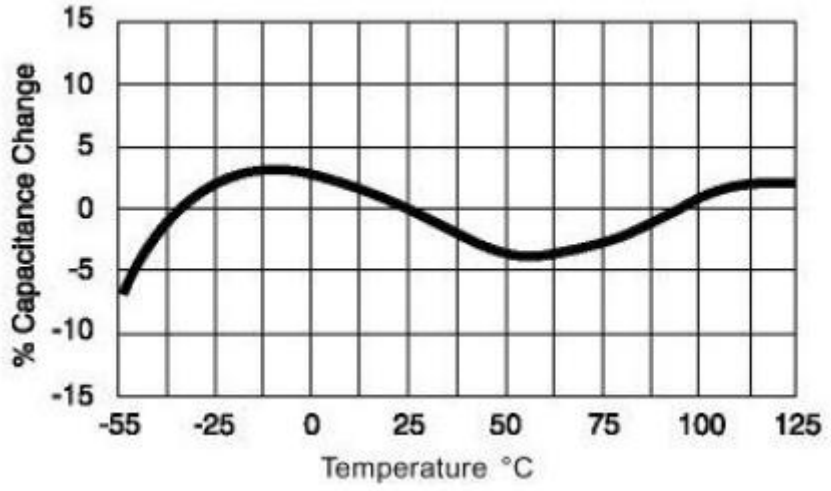


Figure 4.9: Typical temperature coefficient for X7R ceramic capacitors.

4.8 Summary

The test board set up was described in detailes in this chapter. The proposed set up includs five main parts: PC-controllable power supply, current source, DUT, sensing resistor and a capacitor.The set up implementation to provide a ramp voltage source by charging a capacitor is described. Several subroutines for virtual instruments were developed in LabVIEW environment to achieve a PC-controllable test mechanism along with a voltage ramp control unit. FDD8780 (a power MOSFET) is introduced as the target DUT, and some of its temperature-dependent specifications are studied to highlight the importance of excitation and measurement method to decrease the interference of temperature dependency of different parametrs in DUT characterization.

CHAPTER 5

Measurement Implementation and Validation

5.1 Introduction

The measurement technique described in chapter 2 is further analyzed and implemented in LabVIEW environment. This results in a development of a PC-based device characterization curve tracer within the desired accuracy range. The measured results for a DUT is presented and discussed.

5.2 Measurement Theory

According to the proposed measurement technique presented in section 2.4 and its operational set up (see figure 2.7), this measurement technique is looking for the maximum ramp slope and drain-source voltage to provide the desired measurement accuracy.

All experiments are inherently affected by errors. In general, most of these errors can be reduced to a level that is adequate given the objective of the analysis. In order to realize this, the experiments usually have to be designed very carefully. Inaccuracy of the instruments may also be added to the measurement uncertainty errors. This inaccuracy may be evaluated through the instruments datasheets as well as calibration procedure. Some of these errors such as the transmitter calibration errors (see section 3.3.2), resistor tolerance, nonlinearity of sensors, temperature dependency of resistors and capacitors, inaccurate synchronization between instruments, and non-ideal GND isolation were included in this research work. The scope of this thesis does not allow for an in-depth discussion, and the interested reader is encouraged to

consult other articles, such as [47]. Our comments focus mainly on sources of measurement errors due to parasitic impedances of the test board (including DUT). The errors are originated from two main sources. First, the errors are produced by the dynamics of different parts of the tracer circuit and the test board. These errors disturb the initial set points such as adjusted gate-source voltage and consequently measured values. This group can be studied under the category of *electrical parasitic errors*. Second group is *thermal parasitic errors* (thermal impedances) which not only causes self-heating but also disturbs the correct estimation of the junction temperature.

5.3 Electrical Parasitic Errors

According to section 4.3, the parasitic capacitances of a power MOSFET can be modeled as shown in figure 5.1.

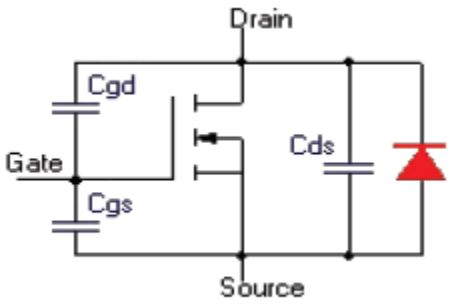


Figure 5.1: Parasitic model of an enhanced power MOSFET.

Other than parasitic capacitance, stray inductance in both power devices and PCB layout has a strong influence during switching transient. In addition, the Equivalent Series Inductance (ESL) of the components inside the measurement circuit can cause error measurement [48].

Therefore, the above mentioned electrical impedances in the test board were modeled as shown in figure 5.2. This model is used as the proposed dynamic circuit to study the effect of electrical parasitic impedances during measurement efforts. R_G is the poly-silicon gate resistance of the power MOSFET and L_{ESL} is the equivalent series inductance of the sensing resistor.

These parasitic impedances cause not only inaccuracy in applied gate-source voltage but also error in signal measurement including drain current and drain-source voltage. These disturbances can be described using the proposed dynamic circuit. They are as follows:

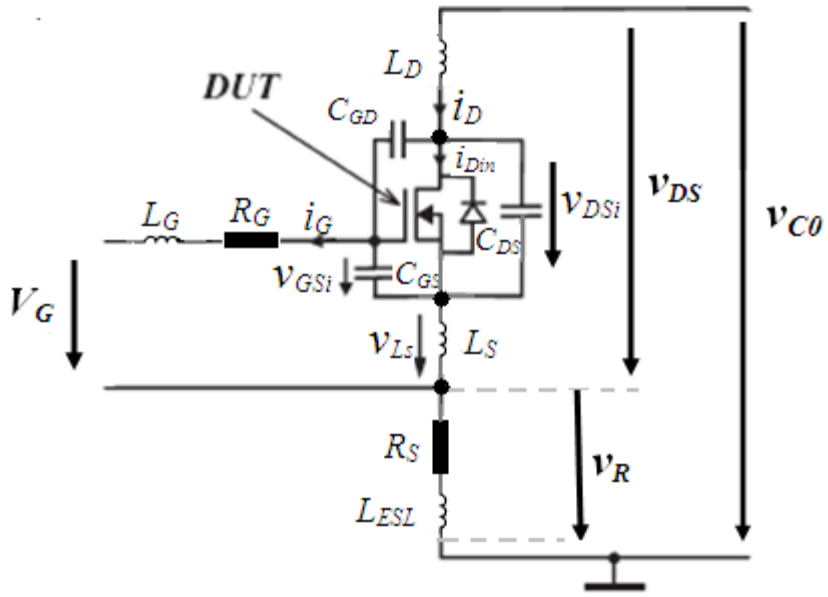


Figure 5.2: Proposed equivalent circuit to model the electrical parasitic impedances.

1. Inaccuracy in applied gate-source voltage;
2. Error in sensing the drain current;
3. Error in sensing the drain-source voltage.

5.3.1 Inaccuracy in Applied Gate-Source Voltage

While the drain-source voltage across the capacitor is increasing (decreasing), voltage across the C_{GS} may deviate from the set point gate-source voltage by gate voltage control. This may happen due to the following reasons:

1. The current flows through C_{GD} charges C_{GS} as well. This causes an increase in the voltage across C_{GS} from set-point V_G. This cause is predominant when the DUT is working in active region and the current change is almost negligible.
2. Variation in drain current causes an induced voltage in *Ls*. This voltage charges (discharges) C_{GS}. The result is an increase (decrease) from set-point V_G.As a result; it

is more noticeably effective when the DUT is acting in ohmic region. In ohmic region, the rate of current change is much higher than drain-source voltage variation.

Although both causes are effective in disturbance of the set-point V_G but the work region of the DUT play more effective role. Worst-case study may consider only one of the causes depending on the operating region. For this purpose, the maximum acceptable deviation from set-point that causes acceptable error will be discussed shortly.

In active region, the drain current is almost constant. Therefore, the induced voltage across inductors shown in figure 5.2 is negligible. As a result, the circuit can be simplified to a series RLC circuit as shown in figure 5.3.

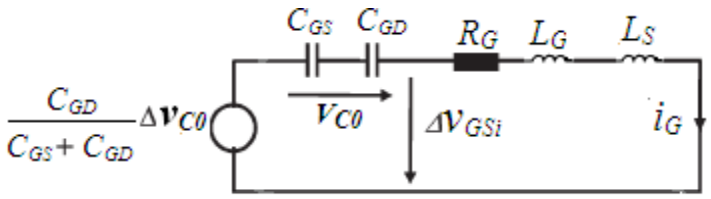


Figure 5.3: Simplified model of the circuit presented in Figure 5.2.

By solving the corresponding differential equation, the maximum gate voltage deviation can be expressed as [49]:

$$\Delta v_{GSi}(MAX+)|_{\zeta<1} = K_V R_G C_{GD} + K_V C_{GD} \frac{e^{-\zeta \omega_n t_p}}{\sqrt{1-\zeta^2}} .\left[L_G \omega_n \sin\left(\omega_n \sqrt{1-\zeta^2} t_p\right) - R_G \sin\left(\omega_n \sqrt{1-\zeta^2} t_p + \phi\right)\right] \quad 5.1$$

where

$$t_p = \frac{\pi}{\omega_n \sqrt{1-\zeta^2}} - \frac{1}{\omega_n \sqrt{1-\zeta^2}} .\tan^{-1}\left(\frac{L_G \omega_n^2 \sqrt{1-\zeta^2} - R_G \omega_n \sqrt{1-\zeta^2}\cos(\phi) + \zeta \omega_n R_G \sin(\phi)}{R_G \omega_n \sqrt{1-\zeta^2}\sin(\phi) - \zeta \omega_n^2 L_G + \zeta \omega_n R_G \cos(\phi)}\right) \quad 5.2$$

$$\omega_n = \frac{1}{\sqrt{L_G + C_{GS} + C_{GD}}} \quad 5.3$$

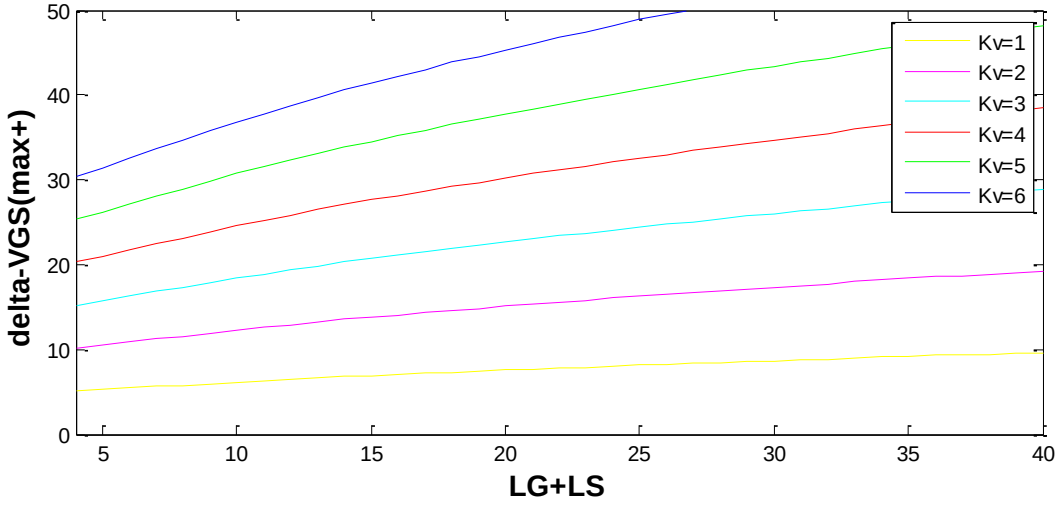
$$\zeta = \frac{R_G}{2}\sqrt{\frac{C_{GS} + C_{GD}}{L_G}} \quad 5.4$$

$$\phi = \tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right) \quad 5.5$$

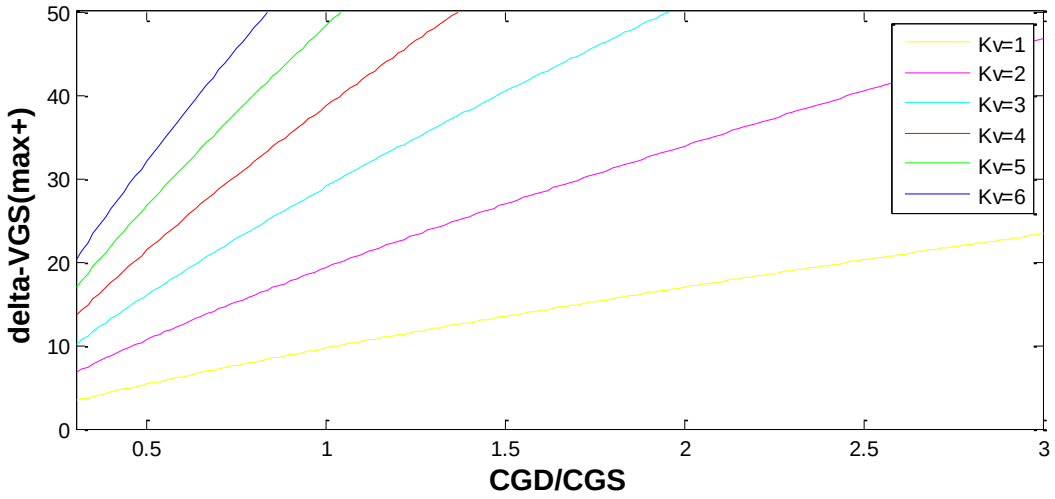
for $\zeta>1$, there is no overshoot and the equation is simplified to:

$$\Delta v_{GSi}(MAX+)|_{\zeta>1} = K_V R_G C_{GD} \quad 5.6$$

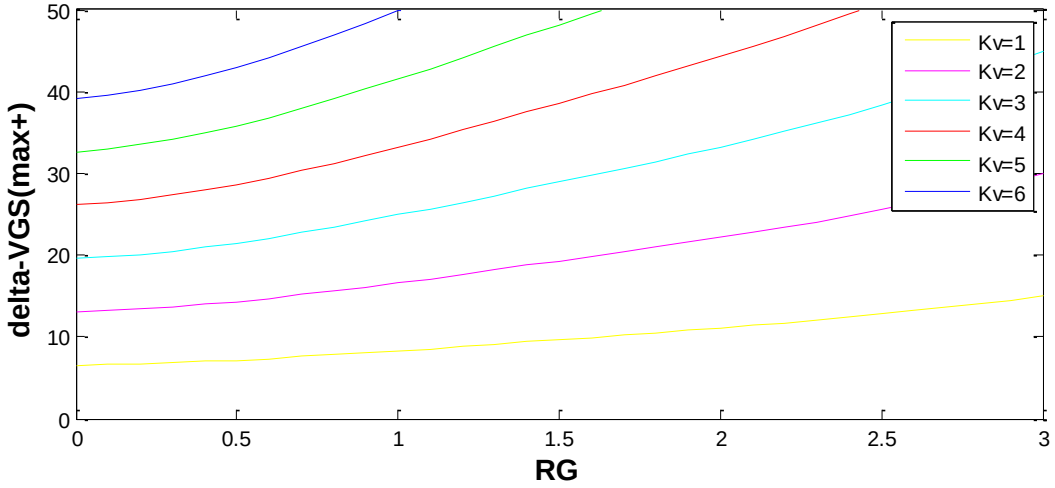
The dependency of $\Delta v_{GSi}(MAX+)$ on parasitic impedances for different values of voltage ramp slope (Kv) is shown in figure 5.4a-c. Also, the relation between voltage ramp slope and gate voltage deviation for different values of L_S+L_D and C_{GD} is depicted in figure 5.5a-b. It can be observed that the steeper the slope is, the higher the gate voltage deviation gets.



a) $\Delta v_{GSi}(MAX+)$ (mV) versus L_G+L_S (nH)

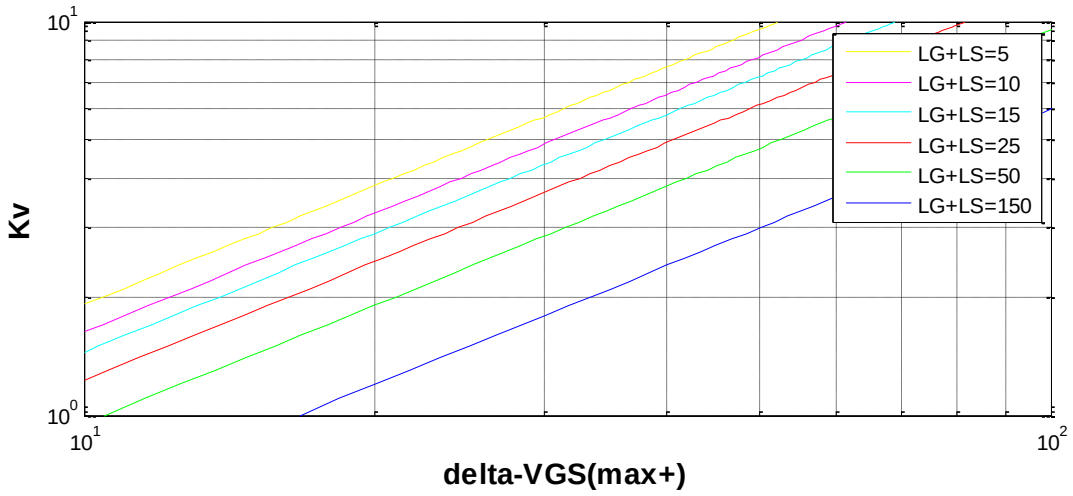


b) $\Delta v_{GSi}(MAX+)$ (mV) versus C_{GD}/C_{GS}(nF)

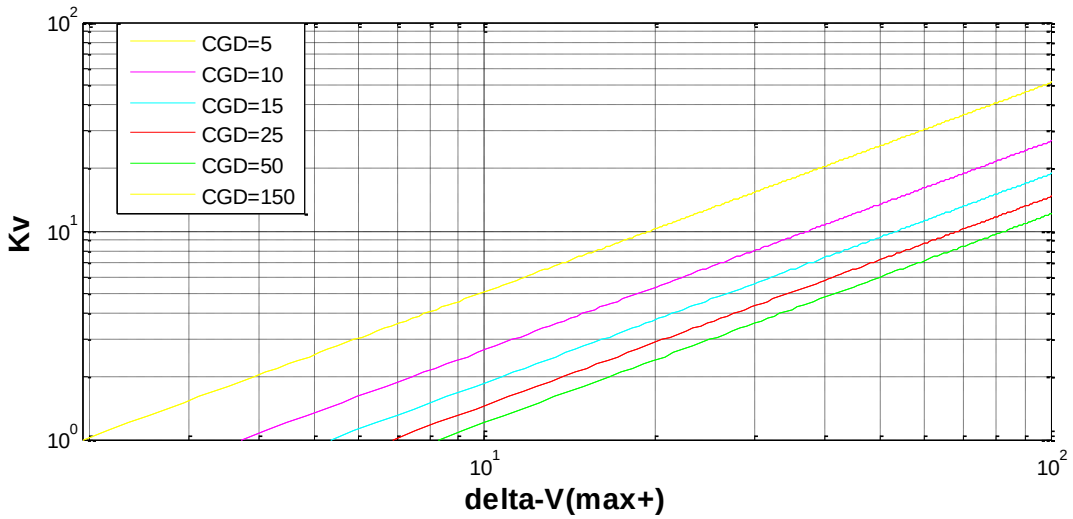


c) $\Delta v_{GSi}(MAX+)$(mV) versus RG(Ω)

Figure 5.4: Maximum gate voltage deviation dependency (mV) on parasitic impedances for different values of voltage ramp slope (V/μs).



a) For different values of L_G+L_S



b) For different values of C_{GS}

Figure 5.5: Voltage ramp slope (V/µs) versus $\Delta v_{GSi}(MAX+)$(mV)

In ohmic region, the rate of current variation is significant. Neglecting the capacitance current, the deviation of the gate-source voltage from the set-point V_G due to the induced voltage in L_{ESL} is calculable from:

$$\Delta v_{GSi}(MAX-) = v_{L_S} \cong L_S \frac{K_V}{R_{DSon}|_{v_{GSi}=V_G}}$$

5.7

5.3.2 Error in Sensing the Drain Current

Error in sensing the current occurs due to two reasons. First, the current (i_D) sensed by the sensing resistor is not the drain current (i_{Din}) that flows through MOSFET's channel (see figure 5.2). The output capacitance (C_{DS}+C_{GD}) current interacts the measured current. Computing these capacitances is not straight forward because they are strongly voltage-dependent. This causes a difficulty to compensate the mentioned error. However, practically, the impact of this error is negligible [50].

Second, the measured current is calculated by dividing the voltage drop (V_R) across the sensing resistor (*Rsense*). The calculated current is not accurate because V_R also includes the voltage drop across the L_{ESL}. It can be compensated by solving:

$$i_D(t) = \int_0^t v_R(\tau) h_{RL}(t-\tau)\, d\tau \tag{5.8}$$

$$h_{RL}(t) = \frac{1}{L_{ESL}} e^{-\frac{t}{\tau R_L}} \tag{5.9}$$

$$\tau_{RL} = \frac{L_{ESL}}{R_S} \tag{5.10}$$

5.3.3 Error in Sensing the Drain-Source Voltage

Drain current variation induces voltage drop across L_D and L_S whereby, an error measurement happens. Using the equation 5.11 the error make-up can be achieved.

$$v_{DSi} = v_{DS} - (L_D + L_S)\frac{di_D}{dt} \tag{5.11}$$

5.4 Thermal Parasitic Error

The temperature control unit is described in section 3.3. The temperature sensor is a J-type thermocouple which is placed in a hole inside the aluminum block. It is assumed that the block temperature is uniformly distributed. This assumption was verified experimentally to study the resultant error. For this purpose, the temperatures of the both sides that a DUT and a Peltier module attached are measured simultaneously by two similar k-type thermocouples. The temperature difference at any time is not going over 1^{o}C that has been compensated in LabVIEW code. Figure 5.6 shows the equivalent thermal circuit based on the aforementioned assumption.

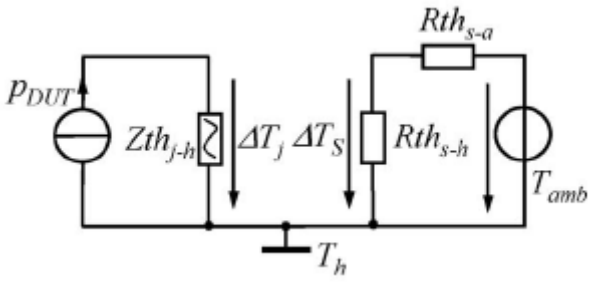


Figure 5.6: Equivalent thermal circuit.

There is a thermal resistance between the sensor and the heatsink (aluminum block), $R_{th\text{-}hs}$, as well as between the sensor and the ambient t, $R_{th\text{-}sa}$. These resistances cause a difference between the temperatures, measured by a sensor, and the real temperature of the aluminum block. In other words, the set-point temperature by the control loop differs from the real temperature of the aluminum block. Placing the sensor as close as possible to the DUT' base minimizes the ratio of $R_{th\text{-}hs}$ to $R_{th\text{-}sa}$ and consequently the earlier mentioned error.

As long as self-heating in a DUT is negligible, the temperature of the DUT junction and the block aluminum are equal so that temperature adjustment error is negligible. During the ramp excitation, the junction temperature rises due to the self-heating. It gets higher than block temperature due to the thermal impedance between junction and aluminum block ($Z_{th\text{-}jh}$). Equation 5.12 determines this temperature rise.

$$T_j(t) = T_0 + \int_0^t P(\tau) dZ_{th}(t-\tau) d\tau$$

5.12

where T_0 is the initial temperature which is also equal to aluminum block temperature in the steady state, dZ_{th} is the derivative of thermal response (see section 5.5) of the DUT with respect to time, P is the dissipated power in the DUT and is calculated based on the measured signals.

To calculate the thermal response of the DUT, cooling or heating curve techniques may be employed that have been described briefly in It is used to calculate the appropriate pulse width and power amplitude for the desired temperature rise in junction temperature.

5.5 Transient Thermal Impedance

Transient Thermal Impedance (TTI) is an indicator of self-heating in semiconductors due to power dissipation. It contains the full thermal description of the system. TTI can be determined by heating up the device and measuring the appropriate Temperature Sensitive Parameters (TSEP) such as threshold voltage, PN-junction forward voltage or leakage current. This implies the coexistence of heating and measuring signals that often interfere with each other. To avoid this, the heating and cooling curve techniques which are based on the switching electrical method [51] are used. There are two experimental techniques to measure TTI as well as a number of analytical and numerical methods based on the power system modeling.

Thermal impedance is defined as the temperature difference between the junction temperature and a reference point caused by constant power dissipation pulse in the device. Temperature measurement should be developed with respect to a reference point. Therefore, the device junction temperature should be calibrated to a constant value before the system is excited by any power pulse. There are two experimental techniques to measure TTI response of a semiconductor device: heating and cooling curves techniques. In both techniques, regardless of the TSEP used, the measurement system consists of a DUT, switching part to provide and control the power pulse signal, measurement devices such as digital multimeter (DMM) to measure the TSEP, arbitrary wave generator (AWG) to generate the control signal for switching device, oscilloscope to monitor the signals and PC as a system controller and analyzer. In addition, a temperature control part should be used to provide the reference temperature.

TTI response can be measured during device heating or cooling phase. Both methods are defined based on the simple concepts. However, the cooling curve technique is more practical to implement since the cooling response is much easier to measure than heating response.

In heating curve technique, the device is heated up by a single pulse of power with the short duration t and amplitude of p. The junction temperature is measured at the end of stimulation.

This procedure is repeated by increasing the pulse width until the steady-state condition is reached. Before applying each pulse, enough resting time is needed to allow the device to cool down to the reference temperature [52-53].

Similar to the heating curve technique, in cooling curve technique, a single pulse of power is applied to the DUT to reach the steady-state situation. At the end of the heat excitation, the measurement phase starts. For each measurement phase, an arbitrary number of temperature samples are measured as the device cools down. This technique is based on the assumption that the cooling response of the device is the conjugate of the heating response. To maintain the validity of this assumption, the measurement should be done under certain conditions: The thermal conductivity and thermal diffusivity of the device must be constant and the power density distribution and current density must not change as the device heats.

Figure 5.7 shows a transient response for a power MOSFET, FDD8780. This graph can be found in datasheet of all power transistors. It is also used for modeling the thermal behavior of a device. Two common models which are extracted from thermal transient response are shown in figure 5.8a-b. The chain model (see figure 5.8a) is a purely formal structure, i.e. the internal structure of the network neither is related to the real physical structure nor can be an indicator of the internal temperature distribution. The ladder model (see figure 5.8b) is called natural equivalent model as it is derived directly from transmission line theory. This model is the only topology that can indicate the internal temperature [54].

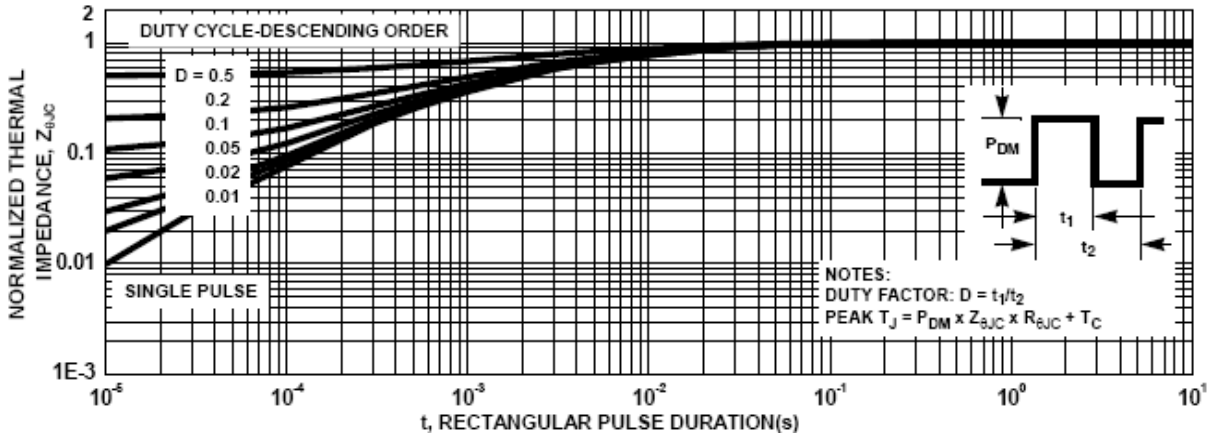
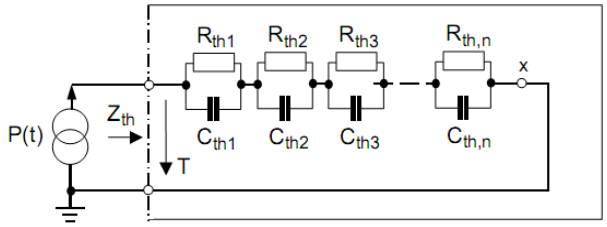
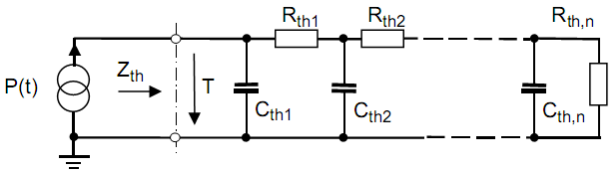


Figure 5.7: Transient thermal impedance from junction to mounting base as a function of pulse duration.



a) Chain (Foster) model



b) Ladder (Cauer) model

Figure 5.8: Thermal equivalent circuit.

5.6 Determination of Maximum Ramp Slope and Maximum Drain-Source Voltage

To stimulate the DUT with voltage ramps, the maximum slope should be determined. This slope controls the stated disturbances in desired limits to achieve the specified measurement

accuracy. Therefore, those disturbances which are not compensated should be limited. This includes disturbances in the applied gate voltage and drain current. Also, the maximum drain to source voltage that does not cause excessive self-heating in a DUT should be determined.

The effect of gate voltage deviation in measured parameters depends on the operating region of the DUT. Measurement of R_{DSon} in ohmic region and drain current in active region are affected by the gate voltage deviation.

In the ohmic region, the maximum absolute measurement error of on-state resistance is calculated from equation 5.13.

$$R_{DSon(error)} = \left(\frac{dy}{dx}|_{v_{GSi}=V_G}\right)\Delta v_{GSi(MAX-)} \quad (5.13)$$

Therefore, equation 5.14 determines the maximum allowable gate voltage deviation to have maximum 1% measurement error.

$$\Delta v_{GSi(MAX-)} < 0.01\frac{R_{DSon}|_{v_{GSi}=V_G}}{\frac{dR_{DSon}}{dv_{GSi}}|_{v_{GSi}=V_G}} \quad (5.14)$$

From equation 5.14, the maximum ramp slope in ohmic region is computed as equation 5.15.

$$K_{v(MAX-Ohm)} = \frac{0.01}{L_S}\cdot\frac{(R_{DSon}|_{v_{GSi}=V_G})^2}{\frac{dR_{DSon}}{dv_{GSi}}|_{v_{GSi}=V_G}} \quad (5.15)$$

The measurement should be performed at low values to avoid self-heating. In a similarly manner, in active region, the maximum measurement error for drain current is

$$I_{D(error)} = g_m|_{v_{GSi}=V_G}\Delta v_{GSi(MAX+)} \quad (5.16)$$

where g_m is the DUT's transconductance. Therefore, the maximum gate voltage deviation is computed from

$$\Delta v_{GSi(MAX+)} < 0.01 \frac{I_D|_{v_{GSi}=V_G}}{g_m|_{v_{GSi}=V_G}}$$

5.17

Employing the equation 5.6, the maximum slope is

$$K_{v(MAX+)}|_{\zeta>1} = \frac{0.01}{R_G C_{GD}} . \frac{I_D|_{v_{GSi}=V_G}}{g_m|_{v_{GSi}=V_G}}$$

5.18

Similarly, $K_{v(MAX+)}|_{\zeta<1}$ yields $K_{v(MAX+)}$ for $\zeta < 1$. I_D in 5.18 should be measured in the beginning of the active region, i.e. the smallest drain-source voltage.

To determine the maximum allowable drain-source voltage, the maximum allowable junction temperature rise should be calculated. Equation 5.19 determines the maximum junction temperature rise to guarantee a 1% error in ohmic region.

$$\Delta T_{j(MAX-Ohm)} = \frac{0.01}{\alpha}$$

5.19

where α is the temperature coefficient of R_{DSon} at 25^0C. In active region, this value is determined from equation 5.20.

$$\Delta T_{j(MAX-Act)} = 0.01 \frac{I_D|_{Tj=Tj_o}}{\frac{dI_D}{dT_j}|_{Tj=Tj_o}}$$

5.20

where T_{j0} is the set point temperature.

5.7 Measurement Set up

A typical measurement set up is shown in figure 5.9. Based on the measurement technique described in chapter 2 and section 2.4.2, a main LabVIEW VI program and several Sub-VIs were developed to automate the measurement system. The aim was to generate a family of IV curves for a high current power MOSFET within certain error. As stated earlier, the measurement technique is based on the stimulation of the DUT by voltage ramps (see chapter 2, section 2.4.2). Each curve is generated during one ramp with specific slope and amplitude. These adjustable slope and amplitude let the user to generate the output for the desired error. In this research work, 2% error due to parasitic impedances was of interest.

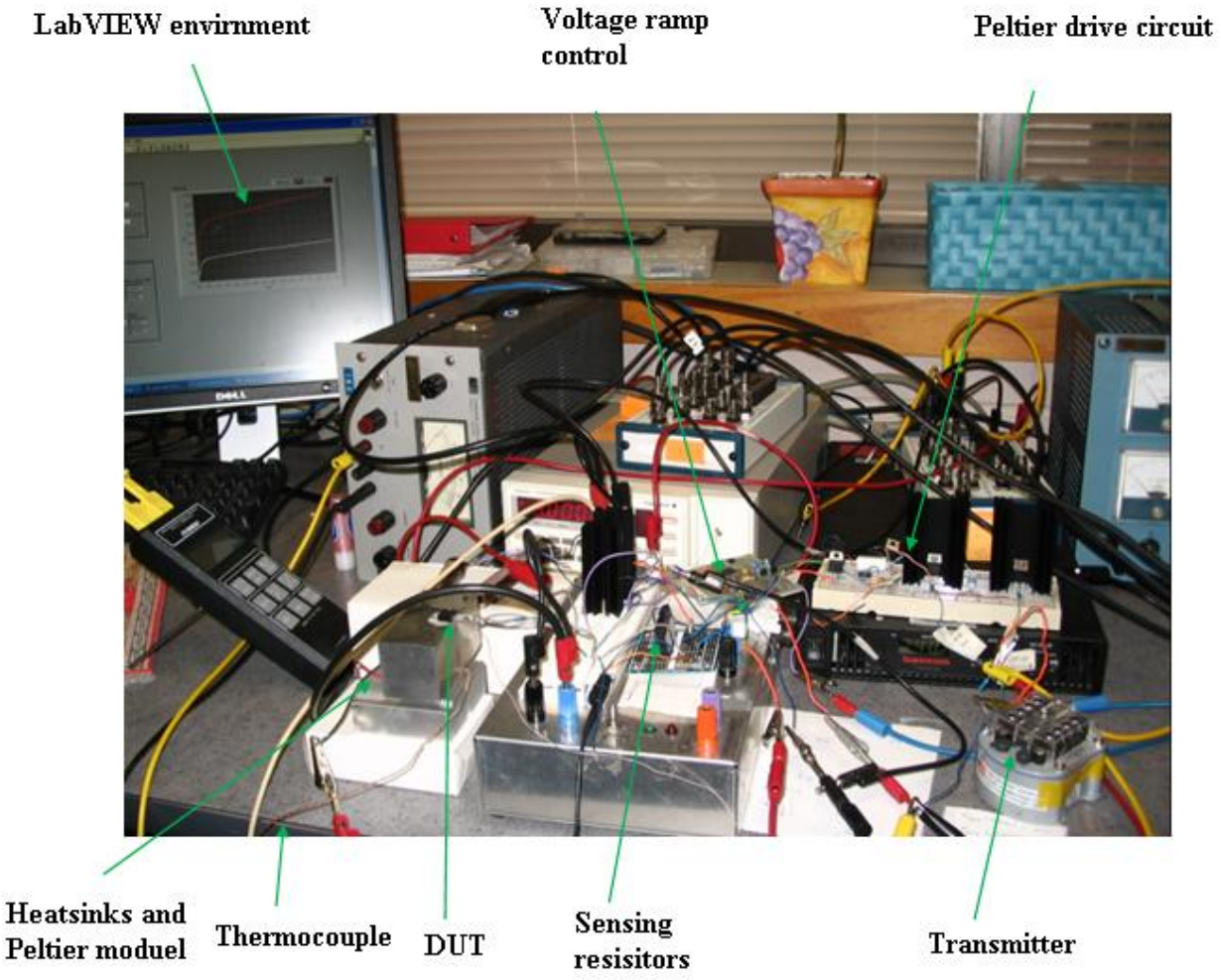


Figure 5.9: Photography of a typical measurement set-up.

Figure 5.10 illustrates the main flowchart of the developed LabVIEW code. To generate one IV curve for the assigned gate voltage and junction temperature, two phases are considered in measurement procedure: calibration and transient measurement. In calibration phase, a low voltage slope is applied to avoid disturbance of the parasitic impedances. After the calibration is completed the maximum slope and amplitude of voltage ramp for the desired measurement error is calculated and applied for the measurement phase. The measurement phase generates the I-V curve for the assigned gate voltage and junction temperature. These two phases are performed for both ohmic and active region. Figure 5.11 and figure 5.12 illustrate the detailed calibration procedure for both ohmic and active region, respectively. It is necessary to note that the sufficient time between each series of measurement should be considered to avoid the error by self-heating and let the DUT comes back to the steady-state i.e. the junction temperature should be cooled down to the initial temperature before the stimulation is applied. An interval time of some hundreds of milliseconds seems enough for this purpose.

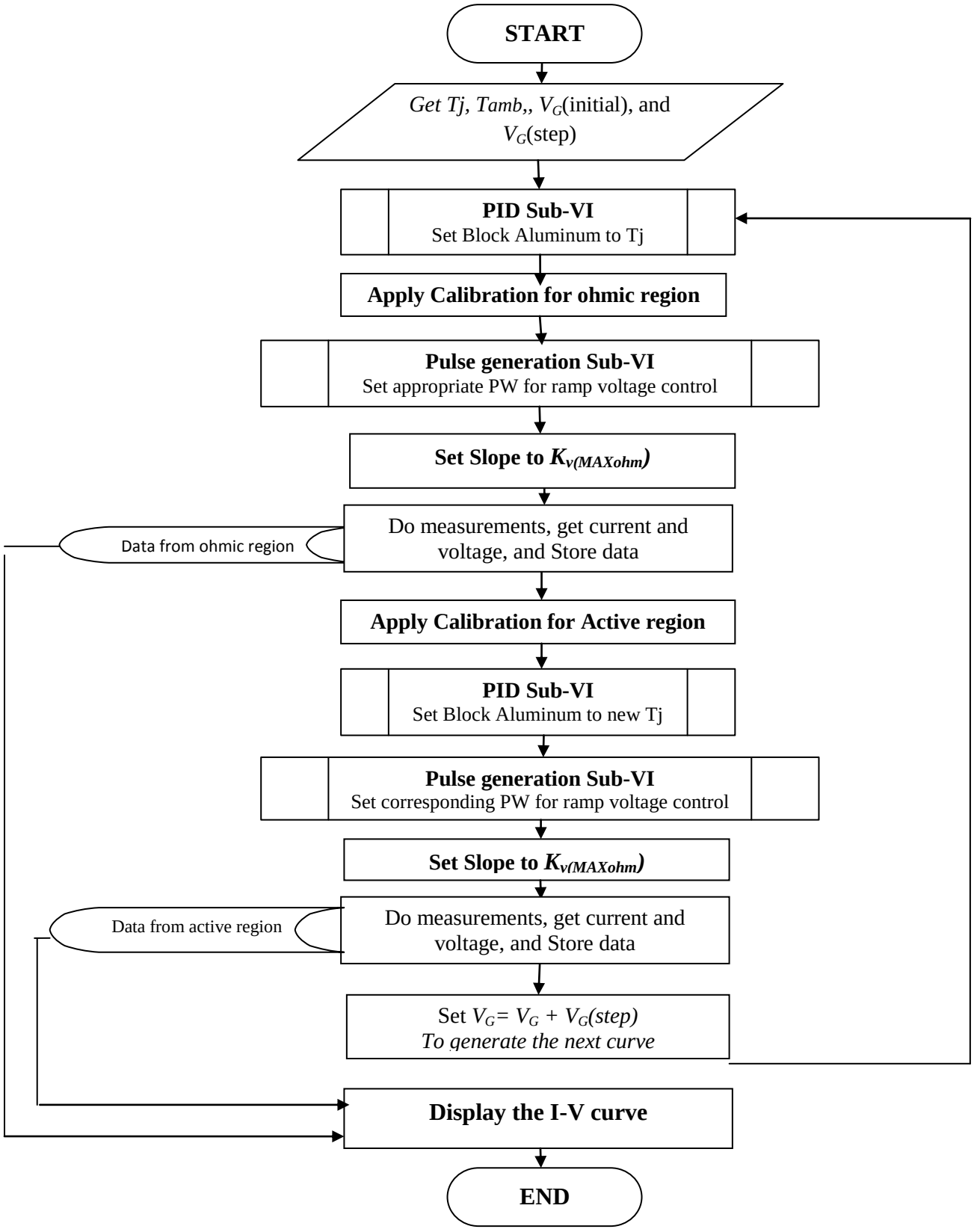


Figure 5.10: Flowchart of the main LabVIEW VI program

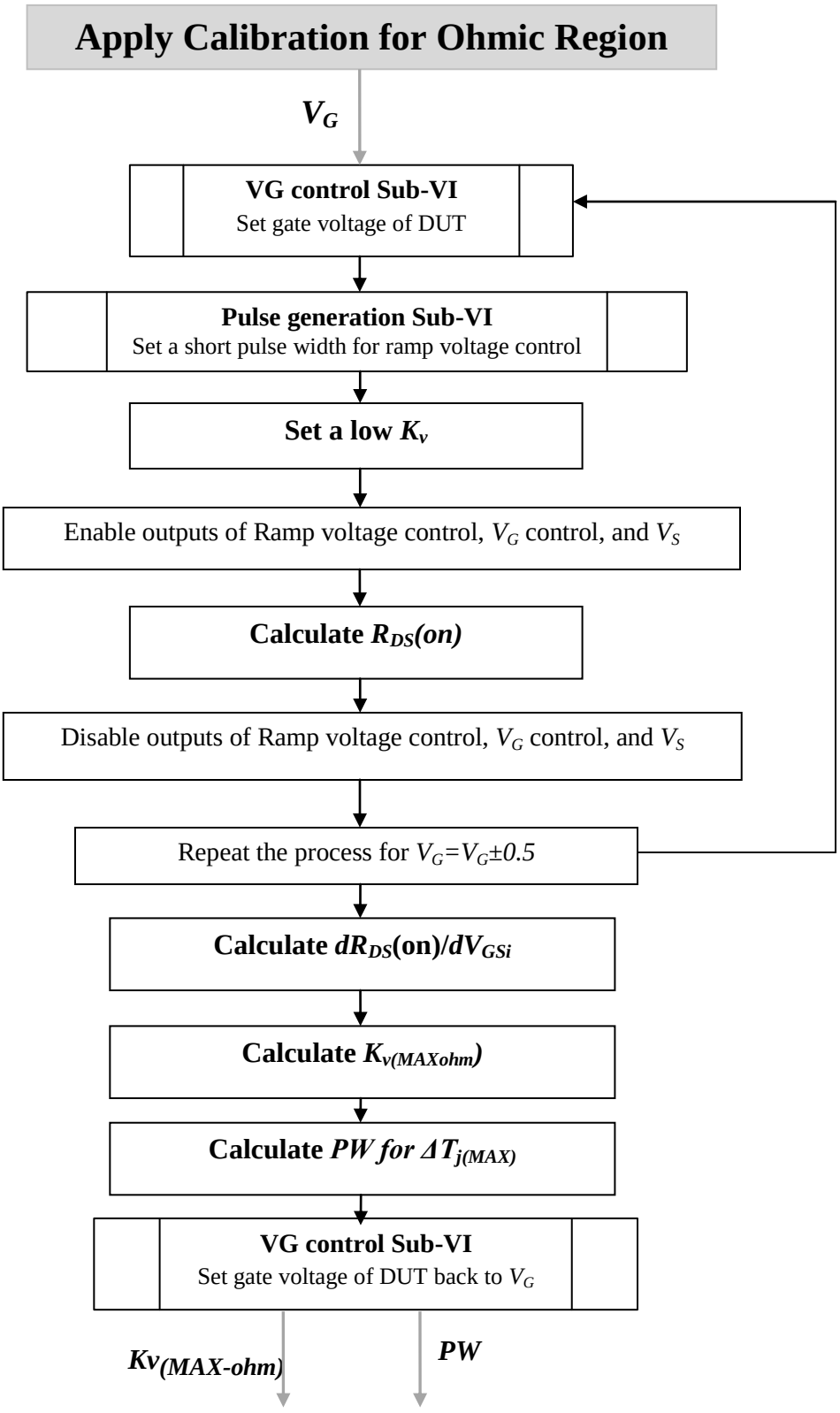


Figure 5.11: Calibration procedure for ohmic region

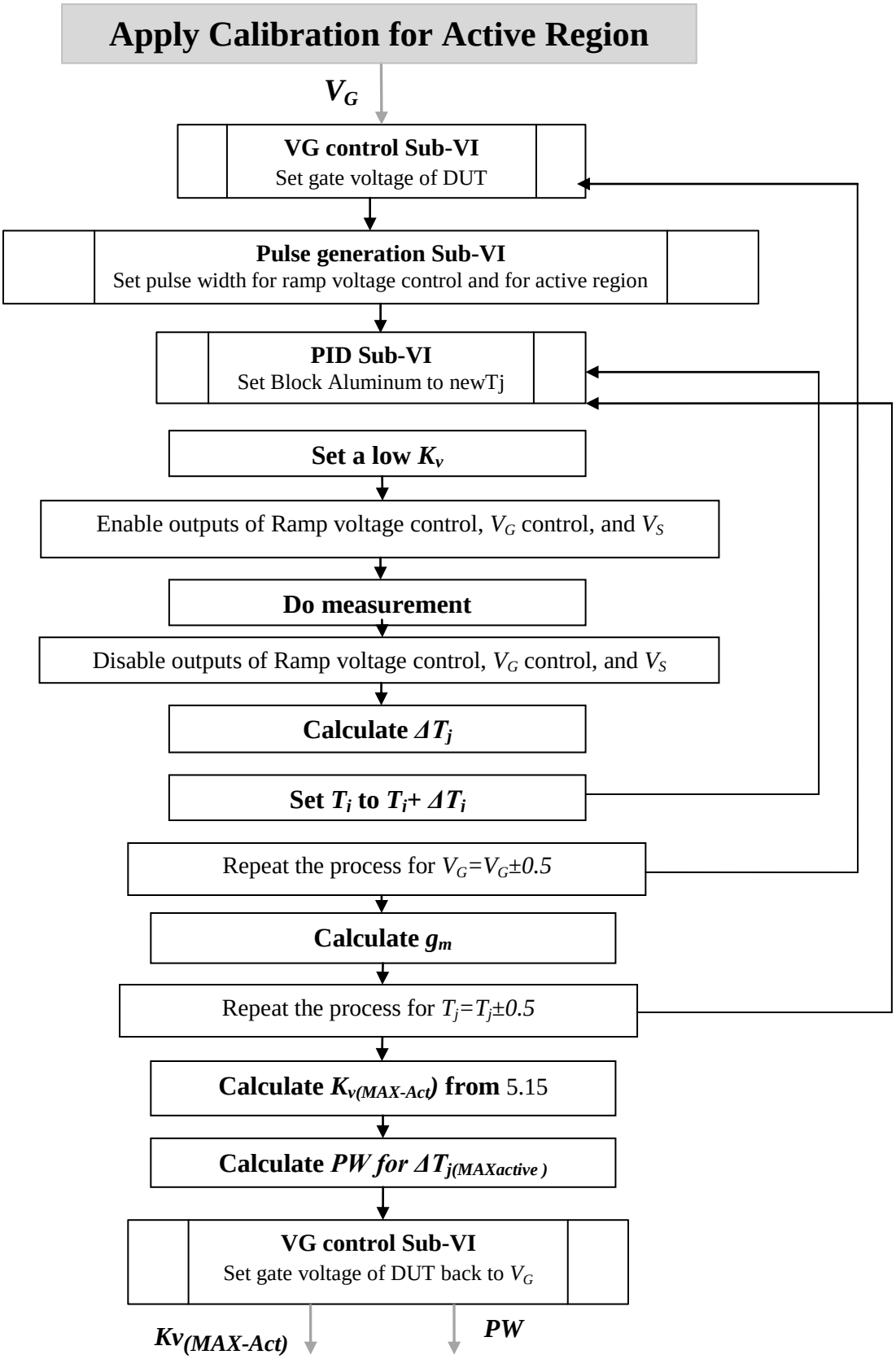


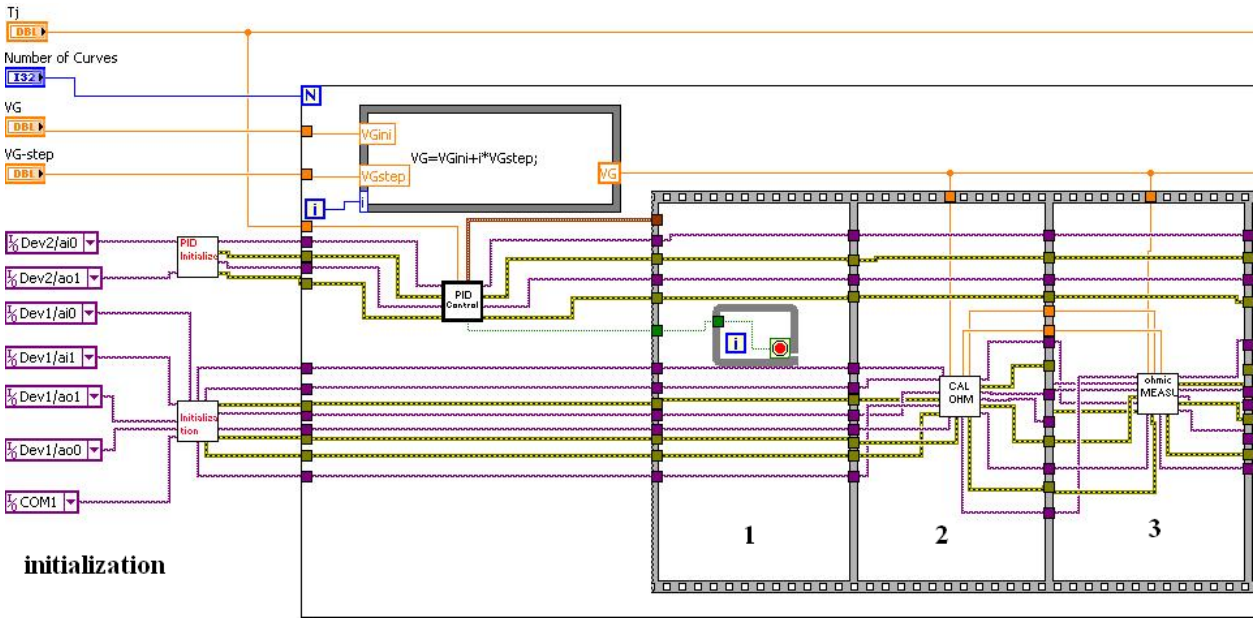
Figure 5.12: Calibration procedure for active region.

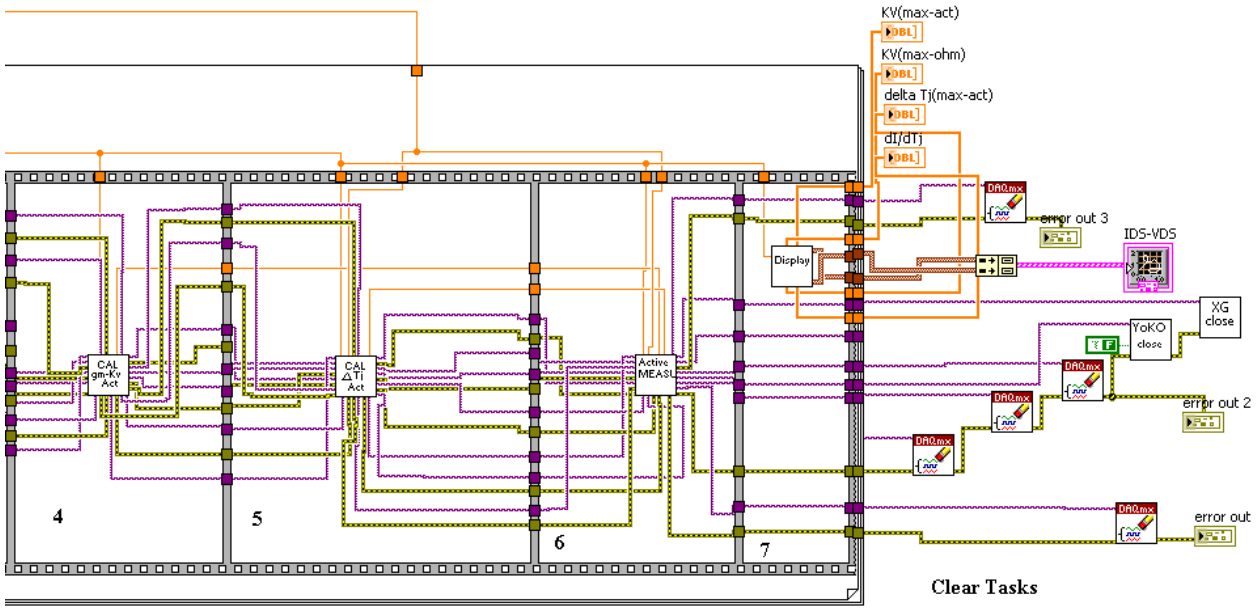
The developed LabVIEW program is shown in Figure 5.13. The main code starts with initialization for defining the analog input/output channels (DAQmx tasks) and instrument initialization.

The main body of the code consists of seven main steps that should be run in sequence. To do this a 7-frame flat sequence is used. These seven steps are as follows:

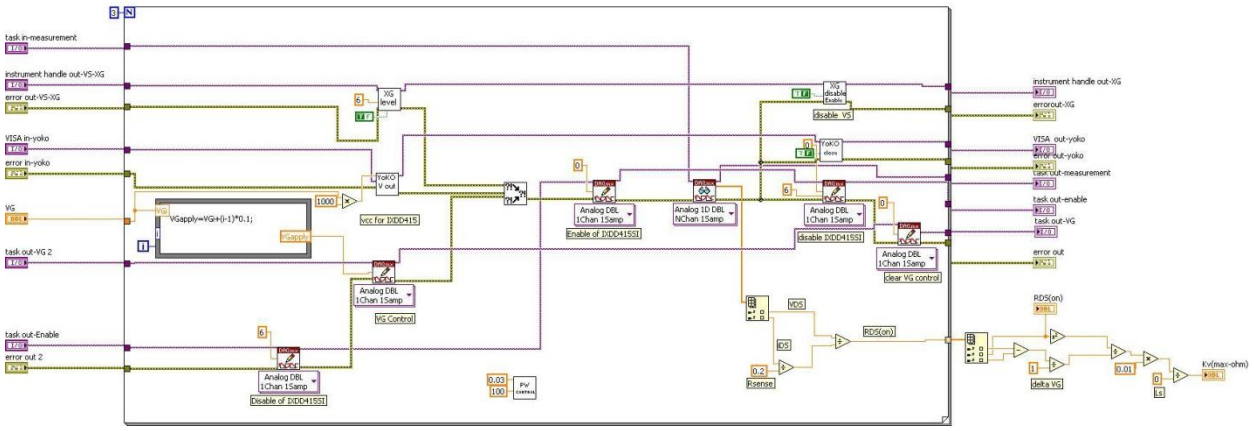
1. The temperature control starts to adjust the set up for input junction temperature. The code waits in first frame until the PID temperature controller is set for the desired junction temperature.
2. Ohmic Calibration sub-VI calculates the maximum allowed slope for ramp voltage source (Figure 5.13b).
3. Ohmic Measurement sub-VI measures the output I-V characteristic for ohmic region and records the resultant data in an excel file (Figure 5.13c).
4. Active calibration is performed in two separate steps. Active Calibration sub-VI-1 drives the DUT for the active region and measures the transconductance (g_m) and maximum allowed slope for ramp voltage source (Figure 5.13d).
5. Active Calibration sub-VI-2 calculates the maximum allowed temperature rise in DUT's junction (Figure 5.13e).
6. Active Measurement sub-VI measures the output I-V characteristic for active region and records the resultant data in an excel file (Figure 5.13f).
7. Display sub-VI plots the I-V curve for the DUT using the recorded data in steps 3 and 6.

To generate a family of I-V curves the above mentioned steps should be repeated using a predefined loop. The code ends with clearing the DAQmx tasks and turning off the devices.

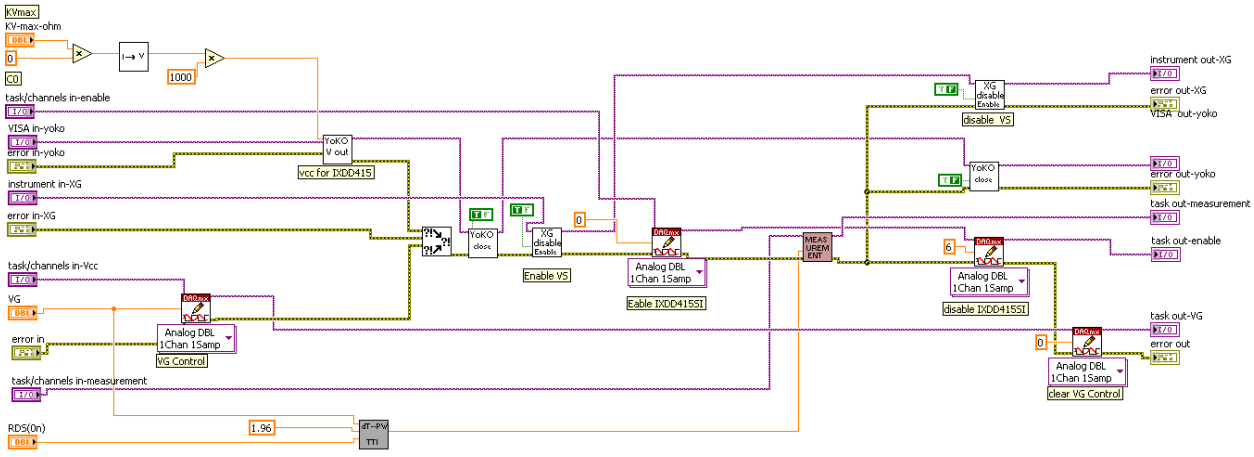




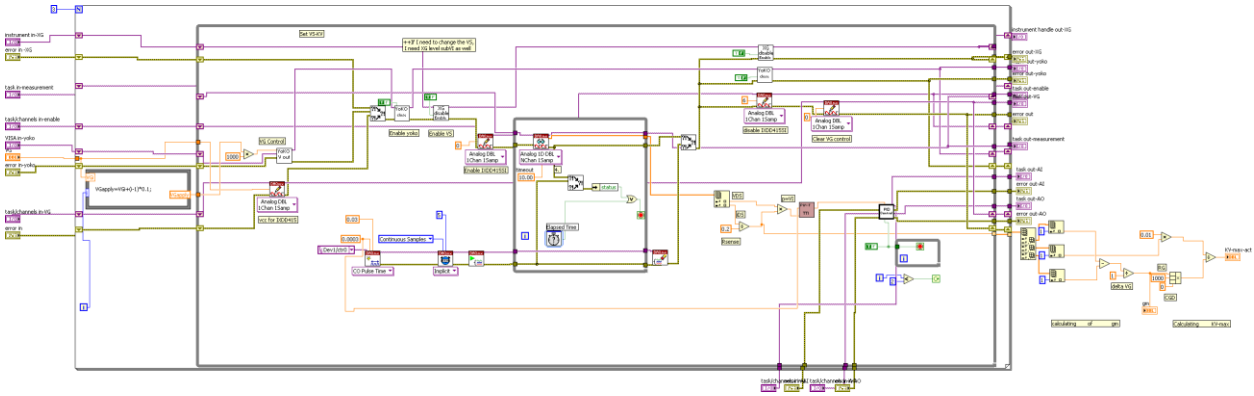
a) Main program



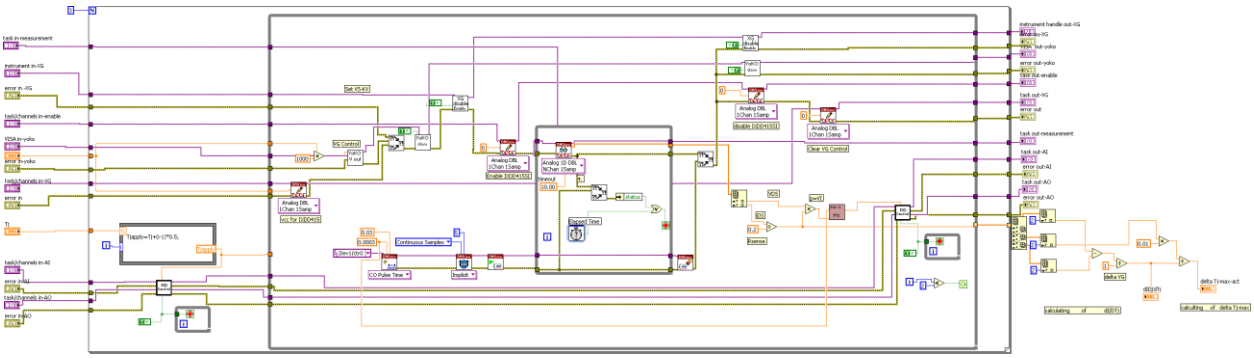
b) Ohmic Calibration



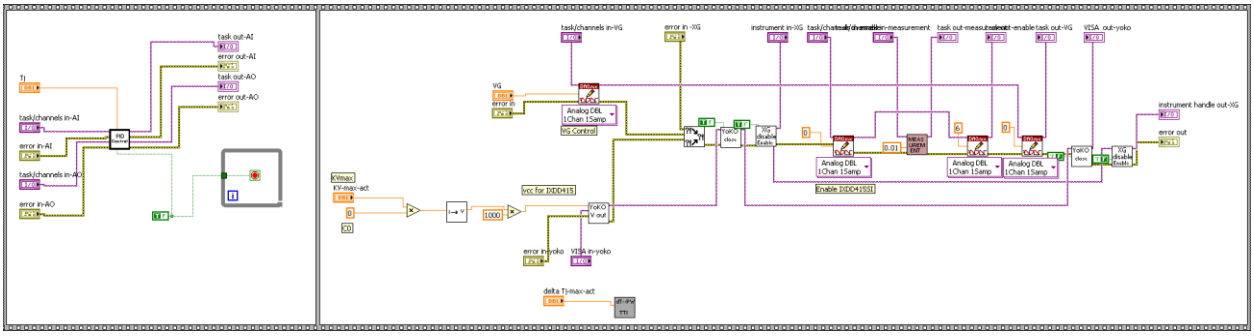
c) Ohmic Measurement



d) Active Calibration-1



e) Active Calibration-2



f) Active Measurement

Figure 5.13: Developed LabVIEW code to measure the output characteristic of a DUT.

The user Interface of the proposed code is depicted in figure 5.14. The user sets the initial gate voltage (V_G) for the first curve. The number of output curves and their corresponding gate voltages are determined by adjusting the *Number of Curves* and *VG-step* controls, respectively.

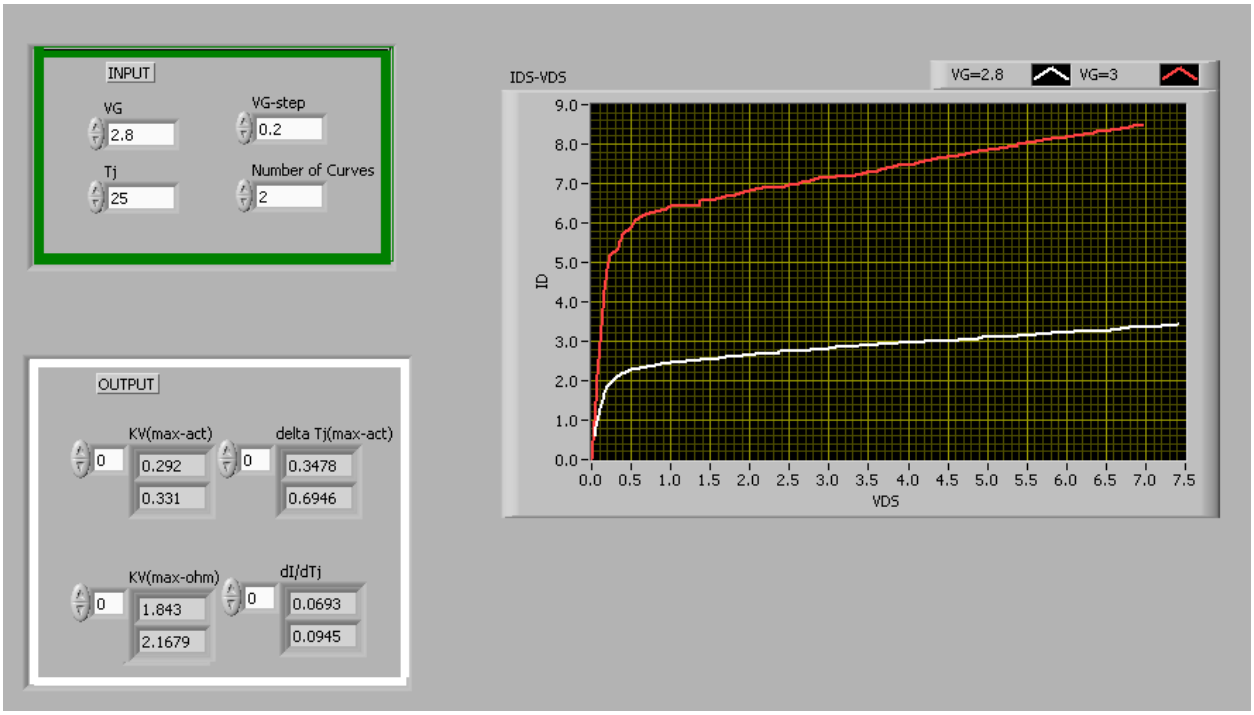


Figure 5.14: The user interface of developed LabVIEW code.

5.8 Measurement Results and Discussion

Figure 5.14 shows the measured I-V curves for the DUT (high current power MOSFET, Fairchild FD8780) for the gate voltage of 2.8V and 3V at junction temperature of 25^{o}C. Similar procedure may be repeated for different gate voltage and junction temperature. The maximum ramp voltage slope for both ohmic and active regions are measured based on the formulas stated in section 5.6 during the measurement process, as it can also be seen from the user interface window (figure 5.14). Therefore, the gate voltage deviation may be determined from the equations 5.1 and 5.7. In addition, the maximum junction temperature rise to have 1% measurement error is computed by measuring the temperature coefficient of the drain current. The resulting values for the maximum permissible ramp slope (K_V), maximum gate voltage deviation (ΔV_{GS}) and junction temperature deviation (ΔT_j) in both ohmic and active regions are listed in Table 5.1.

Table 5.1: Resultant parameters

	VG=2.8	VG=3
$K_V(MAX-Ohm)$ [mV/µs]	1.843	2.168
$\Delta v_{GSi}(MAX-Ohm)$ [mV]	0.121	0.158
$K_V(MAX-Act)$ [V/µS]	0.292	0.331
$\Delta v_{GSi}(MAX-Act)$ [mV]	1.024	1.160
$\Delta T_j(MAX-Act)$ [^{0}C]	0.348	0.695
dI_D/dT_j [A /^{0}C]	0.069	0.094

The DUT is tested in moderate inversion region with V_{GS} of 2.8V and 3V while the threshold voltage is approximately 1.8 [45]. Therefore, it is supposed to have positive

temperature coefficient for this region [54]. This fact is demonstrated by the measurement results.

From Table 5.1, it can be seen that, the maximum gate voltage deviation has almost the same order of magnitude for both ohmic region (0.121 mV) and active region (1.080 mV). Where as, the maximum ramp slope is far limited in ohmic region (1.843 mV/μs) compare to active region (292 mV/μs). Therefore, based on the equations 5.15 and 5.16, it can be concluded that L_S causes stronger disturbances in measurement than C_{GD} .

Comparison between the results of two different gate voltages in Table 5.1 reveals the importance of slow ramp excitation in lower gate voltages; as the gate voltages rises, the maximum permissible voltage slope increases. Moreover, the results indicate that gate voltage increase causes an increase in maximum allowed junction temperature

5.9 Validation

Figure 5.15 depicts the output characterization of the DUT (Fairchild FDD8780) at 25^0C junction temperature from its datasheet [45]. This characterization was obtained based on the pulsed I-V (PIV) characterization with pulse width of 80μs and duty cycle of 0.5%.

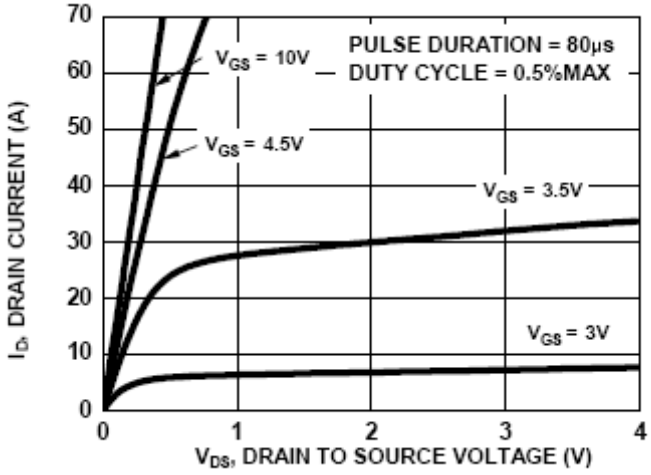


Figure 5.15: Output Characteristics of FDD8780.

The measurement results of the developed PC-based device characterization curve tracer were compared with the data sheet results for the DUT's I-V curve. The corresponding I-V curve at gate voltage of 3V is interpolated and curve fitted from sample points within LabVIEW. Figure 5.16 shows the comparison of this curve and the data sheet curve (from figure 5.14).

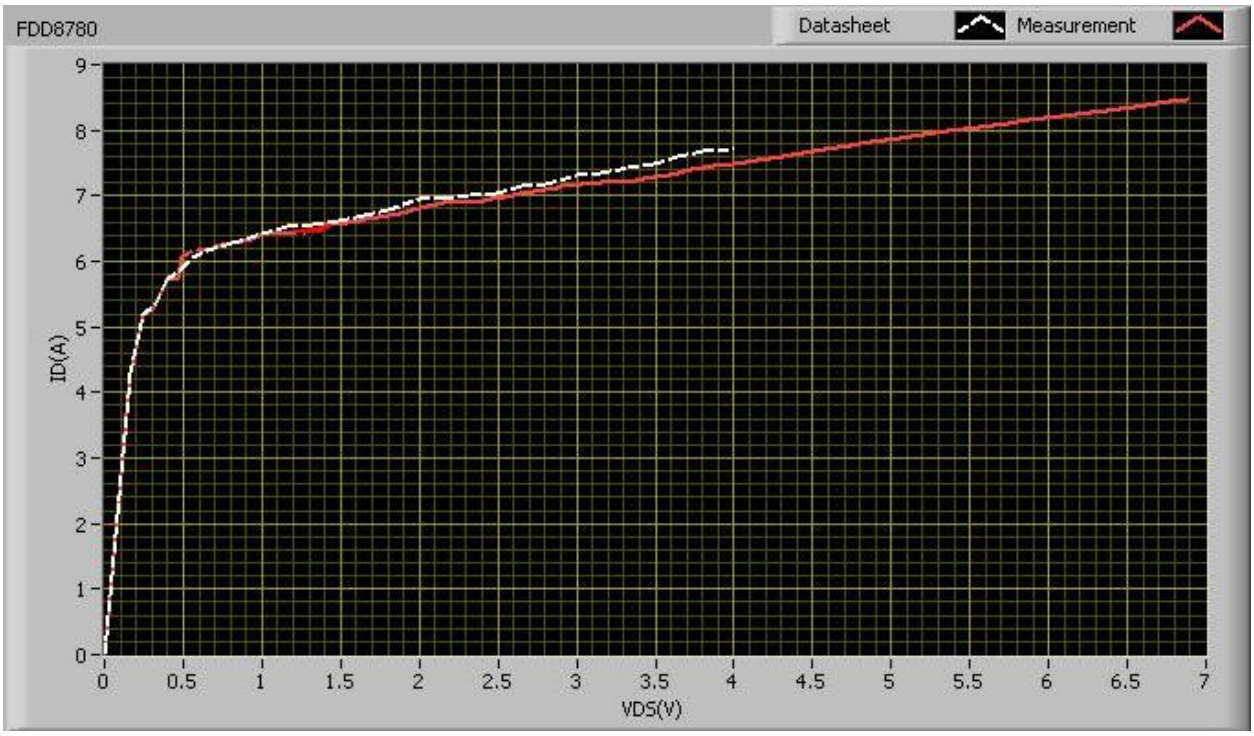


Figure 5.16: Comparison of measured and datasheet I-V curve at V_G=3.

Based on the measurement results in figure 5.16, the DUT is allowed to be excited with the maximum drain-source voltage of around 7V to guarantee the desired measurement accuracy and not exceeding the allowed maximum junction temperature rise listed in Table 5.1. It should be noted that the discrepancy between two curves starts from around 1.8 V which is the threshold voltage of the DUT. This can indicate the high temperature sensitivity of the device in threshold region which results in self heating. The result shows maximum discrepancy at V_{DS} of 4V which is about 4%.

It should be highly noted that the proposed device characterization curve tracer *guarantees* the maximum error of 2% (1% form parasitic impedances and 1% due to self heating) other than accuracy of measurement instruments.

5.10 Summary

In this chapter, the developed measurement techniques is described and implemented based on the proposed dynamic model of the test board. The measurement procedure is programmed in LabVIEW platform. In addition, by employing PC-controllable instruments, the measurement is automated by a LabVIEW program. This resulted in a development of PC-based device characterization curve tracer. This curve tracer is validated based on the datasheet results for a power MOSFET. It *guarantees* the maximum error of 2% (1% form parasitic impedances and 1% due to self heating). Finally, the effect of parameters such as maximum allowed ramp slope and junction temperature deviation in both ohmic and active regions are studied and discussed based on the measurement results.

CHAPTER 6

Conclusions and Future Work

In this thesis, a measurement technique for I-V characterization of power devices was proposed to further minimize power dissipation in a DUT during measurement. This technique was based on the stimulation of a DUT by voltage ramp that allows for fast transient measurement. This way of stimulation excites the parasitic impedances which cause systematic errors. These errors were mathematically formulated based on the proposed dynamic model of the DUT and test board. The operating condition for the measurement within a minimum accuracy was defined. As a result, the maximum allowed ramp voltage and maximum allowed temperature rise were determined mathematically.

A measurement set up for the PC-based curve traced which employs the proposed measurement technique for power device characterization is presented. The set up employs LabVIEW platform to automate the measurement process. A PID temperature controller to control and monitor the DUT's temperature was developed. Moreover, several subroutines were developed to control the instrument from the software platform, acquire the measurement signals, generate output signals and eventually perform the measurement. All of these subroutines were employed in a main LabVIEW program to execute the measurement procedure sequentially. A Fairchild power MOSFET was used as the DUT. Two I-V curves for gate voltages at 2.8V and 3V at 25^0C were generated. The measurement result was validated based on the datasheet I-V characteristic of the DUT. The comparison showed a maximum 4% discrepancy in the active region for a gate voltage of 3V. The I-V curve of the datasheet is obtained based on PIV characterization method. The proposed measurement technique is designed for the maximum 2% error from parasitic electrical and thermal disturbances plus instruments accuracy.

The *major improvement* of the proposed measurement technique over the reported works in the literature is that the *self-heating is effectively mitigated* and that *guarantees* the performance of measurement with the *desired accuracy*. Therefore, the technique is shown to provide a more accurate measurement of the device characteristic.

Hopefully, in future we would like to couple this work with the on going research on electrothermal analysis of integrated circuits. This will allow accurate assessment of performance of electronic products and systems to avoid high risk of overheating causing early device failure.

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