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High-Power Multimodular Matrix Converters and Modulation

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Abstract

High-power multimodular matrix converters (MMMCs) comprising multiple three-phase to single-phase matrix converter modules have emerged as a viable topology candidate for medium-voltage adjustable speed drives. As a combination of direct power conversion and cascaded multilevel structure, the MMMCs inherit features such as elimination of dc capacitors, four quadrant operation capability, employment of low-voltage devices only, and superior output waveform quality under a limited device switching frequency. Due to their particular topological structure, modulation scheme design for the MMMCs is not straightforward and complicated. The presented work is mainly focused on development of suitable modulation schemes for the MMMCs. Several viable schemes as well as their corresponding switching patterns are proposed and verified by both simulation and experimental results.

In order for the MMMCs to produce sinusoidal waveforms at both input and output ac terminals, a direct transfer matrix based modulation scheme is presented. It is revealed that a suitable modulation strategy for the MMMCs should aim at fabricating the total input

current on the primary side of the isolation transformer. For topologies with more than two modules in cascade on each output phase, switching period displacement is necessary among modules to generate multilevel output waveforms.

An indirect space vector based modulation scheme for the MMMCs is developed. With a few presumptions satisfied and viewed from a certain perspective, the MMMCs can still be modeled indirectly and be divided into fictitious rectifier and inverter stages. Therefore, space vector modulation methods can be independently applied to both stages for duty ratio calculation, before the results are converted and combined for determining per-phase output pulses. A new output switching pattern providing improved harmonic performance is also proposed.

A novel modulation scheme based on diode rectifier emulation and phase-shifted sinusoidal pulse-width modulation is proposed. The method sacrifices input power factor adjustment, but enables the use of an indirect module construction leading to significantly reduced device count and complexity. Strategy for reducing additional switchings caused by input voltage ripples is also implemented and explained.

In addition to simulation verifications, all the proposed schemes are further tested experimentally on a low-voltage prototype built in the lab. Details about the prototype implementation are introduced.

Acknowledgement

My foremost appreciation goes to my dissertation advisor, Professor Bin Wu, for his continuous and invaluable guidance, support, and patience throughout the course of this work. I was fortunate enough to have worked with him over the last several years.

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Table of Contents

List of Figures

List of Tables

Glossary of Acronyms

ANPC	Active Neutral Point Clamped
CHB	Cascaded H-Bridge
CSC	Current Source Converter
CSR	Current Source Rectifier
DFE	Diode Front End
EMI	Electromagnetic Interference
FPGA	Field Programmable Gate Array
FLC	Flying Capacitor
GTO	Gate Turn-Off Thyristor
HVDC	High-Voltage Direct Current
IM	Induction Machine
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
LS-SPWM	Level-Shifted Sinusoidal Pulse-Width Modulation
LCI	Load Commutated Inverter
LVDS	Low-Voltage Differential Signaling
MC	Matrix Converter
MV	Medium Voltage
MOV	Metal Oxide Varistor
MMC	Modular Multilevel Converter
MMMC	Multimodular Matrix Converter

NPC	Neutral Point Clamped
PS-SPWM	Phase-Shifted Sinusoidal Pulse-Width Modulation
PWM	Pulse-Width Modulation
RL	Resistor and Inductor
RB-IGBT	Reverse Blocking Insulated Gate Bipolar Transistor
SHE	Selective Harmonic Elimination
SCR	Silicon Controlled Rectifier
SPWM	Sinusoidal Pulse-Width Modulation
SVM	Space Vector Modulation
SGCT	Symmetric Gate-Commutated Thyristor
SM	Synchronous Machine
THD	Total Harmonic Distortion
TPWM	Trapezoidal Pulse-Width Modulation
VSC	Voltage Source Converter
VSI	Voltage Source Inverter

Chapter 1

Introduction

In the area of high-power converters for medium-voltage (MV) motor drives, research and development efforts have been made to either devise new converter configurations, or solve technical problems and optimize performance of existing topologies for specific applications. During the past decade, since there were few revolutionary high-power semiconductors rising, a large percentage of the relevant work was focused on existing topologies and their variants. At present, several major multilevel voltage-source inverters (VSIs) fed by diode or active front-ends are the primary converter choices for most commercial MV drives [1]. Competitive solutions such as the pulse-width modulated (PWM) current-source converter (CSC) are also finding widespread application in industry [2]. In addition to the conventional converters that are relatively mature, alternative topologies including several types of hybrid multilevel converters [3-5], active neutral point clamped (ANPC) converters [6, 7], modular multilevel converters (MMCs) [8, 9], and multilevel matrix converters [10-12] have also attracted increased research interests over the past years. Although the overall effectiveness and potential benefits of these emerging topologies still need further investigation and proof, a few of them have already made their way into practical products and entered the commercial market. Correspondingly, modulation and control strategies adapted to these new converters have been proposed and studied in a large number of recent publications, helping improve operating performance as well as exploring new possibilities.

Among all emerging high-power converter topologies, the multilevel matrix converters form a special category that incorporates the concepts of both multilevel structure and direct power conversion. As alternatives to dc-link based ac-dc-ac converters, direct ac-ac topologies such as the conventional matrix converter (MC) have been extensively studied for several decades [13-15]. However, mainly due to the lack of power semiconductor that can offer sufficiently high voltage and current handling capability, the conventional MCs are not suitable for high-power applications. The fact has led to the invention of multilevel MCs that can reach higher power and voltage levels with existing power semiconductors. This research line is evident in a series of recent publications where the ideas of several major multilevel converter topologies, for instance the neutral-point-clamped (NPC) converter [16], the flying capacitor converter (FLC) [17], and the cascaded H-bridge converter (CHB) [18], are borrowed and combined with the matrix converter concept, resulting in a number of corresponding multilevel MC topologies, namely, the neutral-point-clamped multilevel MCs [10, 19], the capacitor clamped multilevel MC [20], and the multiple cell based MCs [11, 21, 22].

To date, only one particular type of multilevel MC topology has been practically implemented as a commercial MV drive. Designated here as the multimodular matrix converter (MMMC), the topology is composed of a multiple number of three-phase to single-phase MC power modules, cascaded to allow the converter to operate at very high power and voltage levels. It is reported that the commercialized MV drive using this topology has reached 3 MVA / 3.3 kV with three MC modules in series per phase, and 6 MVA / 6.6 kV with six modules in series per phase [12]. Being a member of the MC family, the MMMC possesses features such as elimination of dc energy storage components, extended lifespan, inherent four-quadrant operation, and fast dynamic performance. Additionally, it also possess inherited characteristics from the cascaded multilevel structure,

such as modular design, flexible scalability, and high quality multi-step output voltage waveforms.

Modulation is essential to the proper operation of any type of power converters. For the MMMC, modulation scheme design is not straightforward at first glance due to its particular topological structure. As the converter is composed of three-phase to single-phase MC modules without a stiff dc voltage or current, well established modulation strategies for neither the conventional MCs nor the multilevel converters can be directly adopted. This necessitates the development of specifically tailored modulation schemes for the MMMC to produce sinusoidal input and output waveforms with variable amplitude and frequency.

In this dissertation, several new modulation schemes are proposed and investigated for the MMMC topologies. All the presented schemes are able to generate sinusoidal waveforms at both input and output ports of the converters, with the frequency, amplitude and angle of the output fundamental component arbitrarily adjustable. The input power factor can be adjusted by the first two schemes, while for the last method, it is left uncontrolled but close to unity under suitable component parameters and working conditions.

This chapter is dedicated to the background introduction of the study. First, the general technical requirements on high-power converters for MV drives are briefly summarized. Then, an overview of the state-of-the-art MV drive converter candidates, as well as their features and limitations is provided. After the introduction of the newly emerged multilevel MC topologies, the main objectives and outline of the dissertation are presented at the end of the chapter.

1.1 Technical Requirements for MV Drive Converters

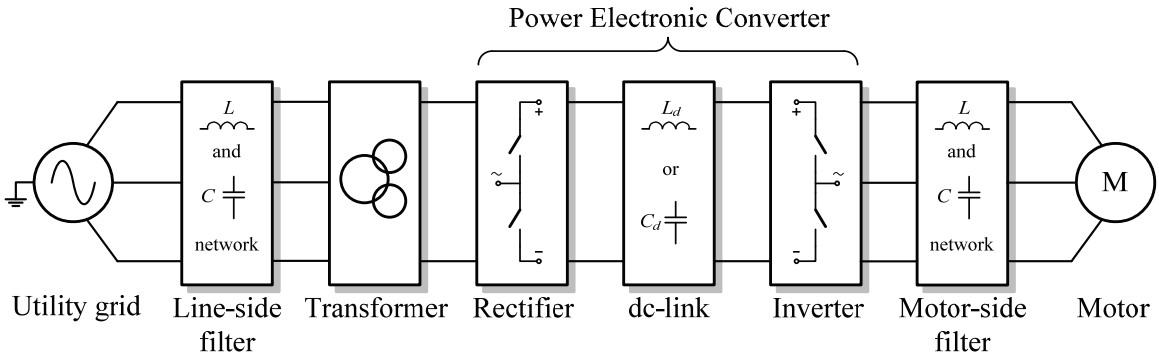


Fig. 1-1 General structure of a medium-voltage drive system.

The MV drive is basically an ac-to-ac power converter system which transforms the fixed amplitude and fixed frequency grid voltage into a desired form for varying the speed of the electric motor load. As demanded by motor control objectives such as speed and torque regulation, the output amplitude and frequency of the drive converter need to be freely adjustable. In Fig. 1-1, the general structure of a typical MV drive system is illustrated. The entire system is composed of the following stages: a line-side filter interfacing the grid, an input transformer providing isolation and adequate secondary voltage level, an ac-to-ac power converter which, in most cases, consisting of a rectifier and an inverter coupled through a dc-link, and an output filter located between the inverter and the machine. In a practical MV drive, some of the stages may be omitted depending on the particular converter configuration.

The majority of commercial MV drives are in the power range of 1 to 4 MW, and their voltage ratings are in the range of 3.3 kV to 6.6 kV [23]. As these apparatus present significant loads to the MV distribution grid, they are subject to strict line-side

requirements on the generation of harmonic contents and input power factor regulation. In the context of any electrical grid, harmonic distortions, if not properly contained, may cause many harmful effects such as malfunction and failure of equipments, tripping of important industrial processes, and excessive loss and heating in the transformers. Therefore, power electronics based apparatus like the MV drive should comply with established harmonic standards such as IEC 1000 and IEEE Standard 519-1992 [24]. As harmonic content generation in an MV drive is mainly due to the switching behavior of the rectifier stage, the choice of converter topology and its modulation scheme have a large impact on the line-side harmonic performance. Additionally, the input filter is necessary in most topologies to help with the harmonic reduction.

Besides harmonic distortion, input power factor regulation is another important line-side requirement. In most cases, a high input power factor within a small region close to unity is demanded by the utility grid.

On the motor side of the drive, the waveform quality is also of great importance. Harmonic contents generated by the inverter or LC resonance could result in additional power loss, heating, and torsional vibration in the electric machine, and therefore should be minimized. Minimization of the harmonic contents requires the inverter stage of the drive to produce high quality sinusoidal waveforms by means of well designed modulation strategies. Additional output filters are necessary in many situations to further smooth the waveforms and improve the machine current quality.

Other motor-side technical concerns include high dv/dt in the generated voltage waveforms, electromagnetic interference (EMI), and common-mode voltage stress on the machine load. Since most modern inverters are operated by PWM, the dv/dt and EMI associated with device switching transients can be very high considering the significant voltage ratings of the MV converter. If not properly mitigated, these detrimental effects

may cause premature failure of shaft bearing and motor winding insulation, as well as malfunction or failure of nearby electronic equipments [23]. Possible solutions to attenuate the harmful *dv*/*dt* and EMI include employment of *dv*/*dt* filters and use of multilevel converters to reduce PWM voltage waveform steps. In addition to *dv*/*dt* and EMI, the common-mode voltage stress – also a by-product of the switching behavior of the converter – is another serious concern in the MV drive system. If completely placed on the motor, the high stress caused by common-mode voltages could result in premature failure of the motor winding insulation as well [23]. To avoid this situation, most available MV drives employ an input isolation transformer to undertake the dominant part of the stress. In a few designs where the input transformer is eliminated, the major part of the common-mode voltage can be taken by a specially designed common-mode choke [25]. Furthermore, it is worth mentioning that, the choice of multilevel converter topologies and/or suitable modulation schemes may reduce or even eliminate the switching-generated common-mode voltages [26], thereby relieve the stress on isolation transformer and/or common-mode chokes.

1.2 Overview of Modern MV Drive Converter Topologies

This section gives an overview of the most relevant high-power converter topologies for MV drives. The focus is mainly placed on existing topologies that have found practical presence in industry, as well as several potential topology candidates which are recently proposed and studied in the literature. Although not considered as high-power converters, the conventional matrix converter and some of its multilevel derivatives are also briefly reviewed due to their high relevance to the subject matter.

As shown in Fig. 1-2, converter topologies for MV Drives can be generally classified into two major categories: the ac-dc-ac indirect converters, which contain dc-links

interconnecting the rectifier and inverter stages, and the ac-ac direct converters, which perform power conversion directly between their input and output ac terminals.

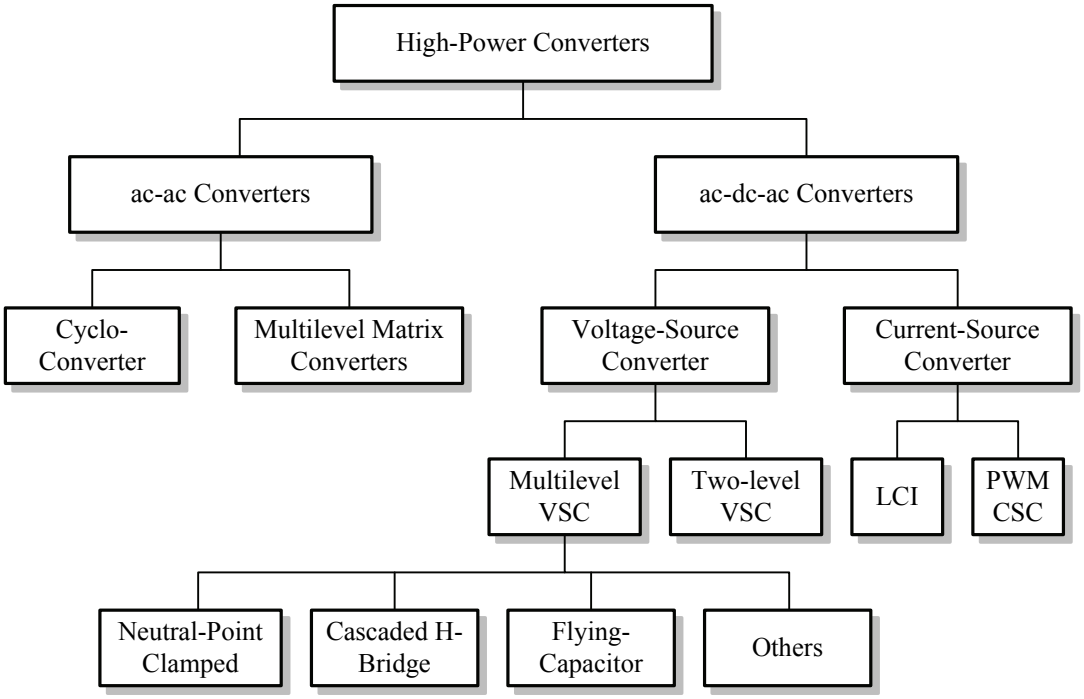


Fig. 1-2 Classification of high-power converters for MV drive.

1.2.1 ac-dc-ac Indirect Converters

The ac-dc-ac indirect converters invariably require dc energy storage components and can be further divided into current-source converters (CSCs) and voltage-source converters (VSCs). The CSCs have a current-stiff dc-link realized by dc inductors, whereas the VSCs feature voltage-stiff dc-links comprised of dc capacitors. Both CSC and VSC topologies have found wide commercial application in the MV drive industry; but they are associated with different characteristics and features.

1.2.1.1 Current-Source Converters

In the subcategory of CSCs, the load-commutated inverter (LCI) and the PWM CSC are the only two types currently being used in practical products. The LCI is built with silicon-controlled rectifier (SCR) devices, and is mainly suitable for very high power synchronous machine (SM) drives. In contrast, the more modern PWM CSC is made up of symmetric gate-commutated thyristors (SGCTs) with reverse voltage blocking capability. The PWM CSC can be used to drive both megawatt induction machines (IMs) and SMs.

LCI based CSC

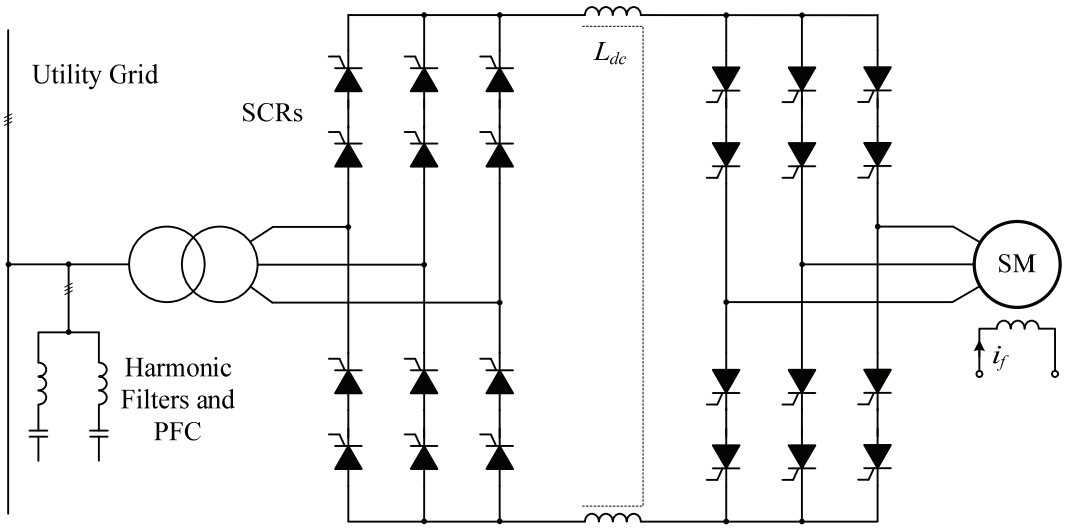


Fig. 1-3 LCI based MV drive for synchronous machine load.

The LCI based MV drive as shown in Fig. 1-3 is essentially a back-to-back thyristor converter constructed with SCR devices [27]. In the dc-link of the converter, a large inductor is employed to smooth the current. Aimed at very high power SM applications, the

power rating of an LCI drive is typically in the range of a few to tens of megawatts, and may even reach a hundred megawatts or beyond in some particular cases. Due to its simple structure and use of inexpensive and rugged SCR devices which are commutated at the fundamental frequency, the LCI drive features low converter cost, low power loss, high efficiency, high reliability, simple control, and allows regenerative operation. As the commutation of SCR devices require a load voltage of leading power factor (hence the name "load-commutated"), the LCI drive is most suited for large SMs that can work in the over-excited condition by adjusting the rotor field current. Along with all the benefits obtained, the LCI has limitations and drawbacks from using the phase-controlled SCRs as well, those include: limited control freedom and dynamic performance, high harmonic contents in both the line- and motor-side currents, and variable input power factor under different load conditions [2, 28]. In a practical LCI drive, input filter and power factor compensator are normally required.

PWM CSC

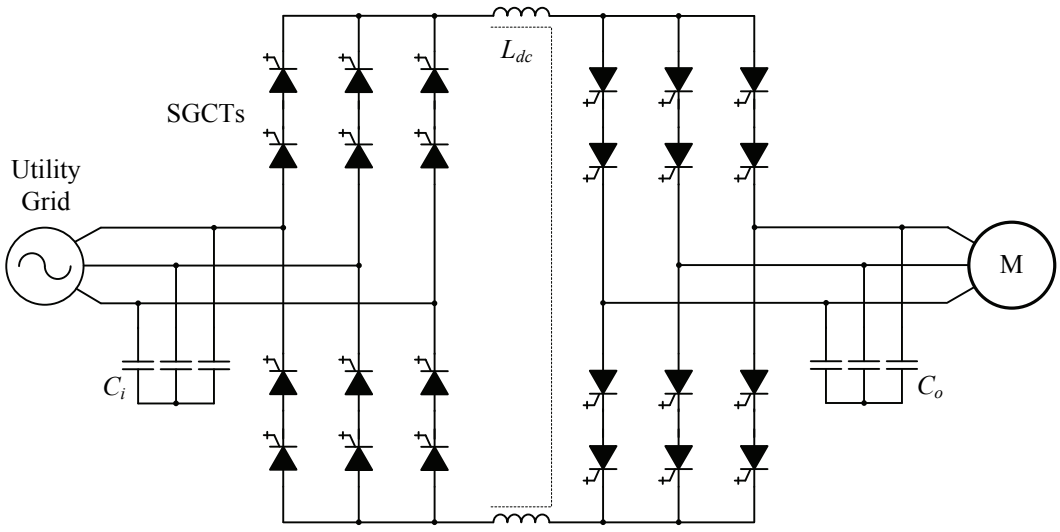


Fig. 1-4 Configuration of PWM CSC based MV drive system.

The state-of-the-art PWM CSC drive possesses a similar topology to that of the LCI, featuring two three-phase full-bridge converters connected in the classic back-to-back configuration through a dc-link inductor [29]. However, unlike the LCIs which are composed of SCRs and operated by phase control, the PWM CSC consists of fully controllable SGCT devices that can be arbitrarily turned off by the gate signals. These modern high-power devices allow the PWM CSC to be operated by various PWM schemes at a switching frequency of several hundred hertz, generating chopped current pulses at both ac terminals of the converter. Due to PWM operation, ac filter capacitors are required to assist device commutation and to attenuate the generated harmonic current contents. The PWM CSC drive is able to produce variable amplitude variable frequency sinusoidal waveforms with adjustable angle at both the line and motor side. Generally speaking, features of the PWM CSC include simple topology, motor friendly waveforms, and reliable fuse-less short-circuit protection. Moreover, the topological structure of the PWM CSC enables an integrated dc-link choke design using a common magnetic core to realize a practical transformerless MV drive. The integrated choke consists of a differential part as the normal dc-link inductor, and a common-mode choke to undertake the dominant part of the common-mode voltage stress. The otherwise required input isolation transformer can therefore be eliminated.

The PWM CSC can be switched by various modulation schemes, such as trapezoidal PWM (TPWM), selective harmonic elimination (SHE), and space vector modulation (SVM) [23]. The TPWM is a carrier-based modulation strategy where a trapezoidal modulating wave is compared with a specially tailored carrier wave to generate gate signals. Although the scheme satisfies the CSC switching constraints, the generated PWM waveforms contain relatively high low-order harmonic contents. The SHE is an offline calculated method that offers both low switching frequency and superior harmonic profile due to its purposeful

elimination of several low-order harmonics. However, when compared with the online switching schemes, the SHE's dynamic performance is inferior, owing mainly to its lack of modulation index adjustment capability. The SVM is a digital modulation method which performs real-time duty-cycle calculation and reference vector synthesis, and provides excellent dynamic performance for the converter control by offering the complete degrees of control freedoms (modulation index and delay angle). However, the harmonic performance of the conventional CSC SVM is not as good as that of the SHE. Also the SVM is associated with more switchings and power losses by introducing the short-through pulses. These two drawbacks, together with the fact that in a practical PWM CSC drive, the motor-side magnitude adjustment is normally done through controlling the dc-link current level by the rectifier, rather than to utilize the inverter-side modulation index, make SHE the main modulation scheme choice in a PWM CSC drive in the medium to nominal speed range. TPWM and SVM may also be chosen when the load machine works in the low speed region, where the SHE may not find a viable solution for the calculation of angles.

The main drawback of the PWM CSC drive lies in its slow dynamic performance, which is primarily because of the large choke employed in the dc-link, and the drive's control strategy of using the rectifier to regulate dc current level for load-side magnitude adjustment.

1.2.1.2 Voltage-Source Converters

Compared with CSCs, VSC topologies are much more popular in many applications including the MV drive. In the fast developing MV drive industry, both conventional two-level VSC and a number of multilevel VSC topologies are currently present in the market. The two-level VSC based MV drive needs to put devices in series to withstand the high voltage stress, and produces large voltage steps in the output waveform equaling that of the

entire dc-link voltage. The multilevel converters, on the other hand, are relieved from many problems of the two-level VSC and, in general, possess the following advantages:

1) Reduced voltage stress on individual power switches. This enables the use of power semiconductors with lower voltage rating and avoids the problems and challenges associated with series device connection;

2) Reduced *dv*/*dt* during device switchings. In contrast to the two-level VSC, each device in a multilevel VSC is normally switched between two adjacent voltage levels instead of the entire dc-link voltage. This also brings the benefit of lower common-mode voltage steps/amplitudes;

3) Better input/output waveform quality in terms of total harmonic distortion (THD) and harmonic profile due to the generated multi-step waveform shape that is closer to sinusoid. As a result, the requirement on input/output filters can be significantly lowered or even eliminated.

At present, several multilevel VSC topologies such as the NPC converter and the CHB converter are the primary converter choices for most commercial MV drives.

High-Power Two-level VSC

As the dominant topology in low-voltage motor drives, the two-level VSC has also been used to implement MV drives by a few manufacturers [23]. In a two-level VSC based MV drive, the power devices (insulated gate bipolar transistor, IGBT) need to block the entire dc-link voltage. Since there is no single device available to offer such a high voltage rating, the IGBTs in the converter legs have to be connected in series to share the voltage stress. The series-connection of devices is accompanied by static and dynamic voltage sharing issues which need to be addressed by active or passive means [30]. In addition, the voltage

step, dv/dt and common-mode voltage stress generated by the two-level VSC are very high, which require large-size differential and common-mode filters to suppress. Depending on specific application requirement, the dc-link of the two-level VSC drive can be fed by a diode front-end for non-regenerative operation, or an active front-end to realize a back-to-back configuration for regenerative breaking. In terms of modulation, the well-established carrier-based sinusoidal PWM (SPWM) and SVM schemes can both be used in the two-level VSC to implement advanced motor control strategies [31].

Neutral-Point-Clamped Converter

The three-level NPC converter as shown in Fig. 1-5 is presently one of the most widely used topologies in newly developed MV drives. Unlike the two-level VSC which only switches between the negative and positive rails of the dc-link, the NPC converter splits the dc-link equally with two cascaded capacitors, and thereby introduces a dc neutral point [16]. On each of the NPC's phase legs there are four power switches. In addition, two diodes are added to connect the dc neutral point to the junctions between the first and second, third and fourth switches, hence allowing the phase output terminal to be clamped to the dc neutral level. As a result, the phase output voltage of an NPC converter can have three levels (with respect to the dc neutral point): $+V_{dc}/2$, 0, and $-V_{dc}/2$. Compared with the two-level VSC, the device voltage stress in the NPC converter is halved for a given dc-link voltage. Besides, the output voltage quality of the NPC is better due to the multilevel waveform shape which reduces the requirement of the filter. Commercial NPC drives are implemented with high-voltage IGBTs or integrated gate commutated thyristors (IGCTs), which have replaced gate turn-off thyristors (GTOs) as the dominant high-power semiconductor devices. Currently, the NPC based MV drive covers a voltage rating up to 4.16 kV without putting devices in series or using step-up transformer, and is expected to

extend to higher voltage ranges with the advent of 10 kV IGCTs [32]. In a typical NPC drive, multi-pulse diode rectifier or active rectifier using the same NPC topology can be employed as the front-end converter, for unidirectional or bidirectional power flow applications, respectively.

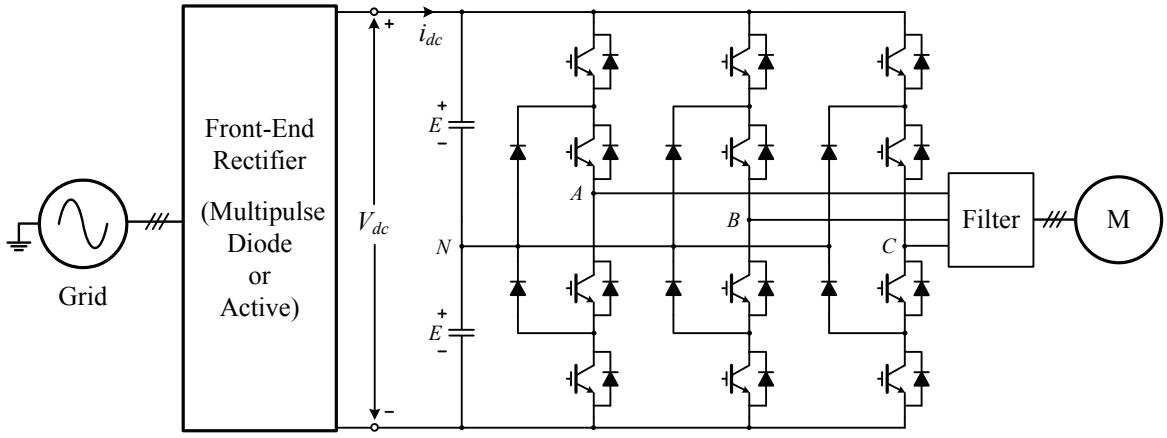


Fig. 1-5 NPC converter based MV drive.

The NPC converter can be modulated by various modulation schemes, such as the multi-carrier-based SPWM, three-level SVM, and SHE [33]. Both carrier-based PWM and SVM provide the complete control freedoms of modulation index and angle adjustment. Due to the multiplicative effect brought by the three-level structure, the equivalent converter switching frequency of the NPC is twice that of the device switching frequency, offering the converter a good dynamic performance for advanced motor control requirements.

One of the main technical issues associated to the NPC converter is the need to balance dc capacitor voltages during operation. The problem has been solved by many strategies proposed over the years for either diode-front-end-fed or active-front-end-fed configurations [34, 35]. Another drawback of the NPC lies in the uneven power loss and,

thereby, uneven heat dissipation on the outer and inner switches. Using active switches in place of the clamping diodes and forming a three-level active NPC topology may significantly improve the loss distribution, but at the expense of increased semiconductor cost [6].

Cascaded H-Bridge Converter

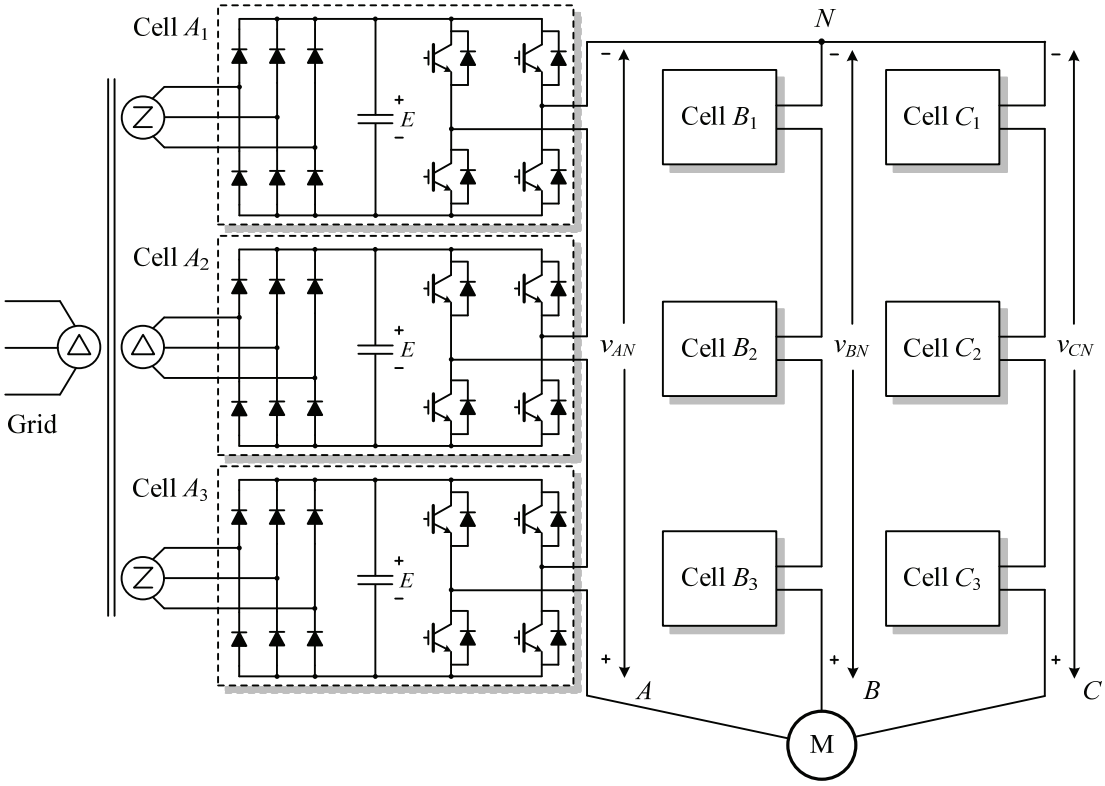


Fig. 1-6 A seven-level CHB converter based MV drive.

Besides NPC, the CHB converter (Fig. 1-6) is another very popular multilevel VSC topology that has been chosen by a large number of MV drive manufacturers. As the name indicates, the CHB is made up of series connected single-phase full-bridge converters (H-

bridges). The H-bridges are supplied by separate dc-link capacitors sourcing energy from three-phase diode-rectifiers, which are normally fed by the secondary windings of a phase-shifting input transformer interfacing the grid. Each H-bridge, together with the dc-link capacitor and the diode rectifier, forms a standard power cell and serves as the fundamental building block for the modular design of the entire converter. Regarding the power cells, although CHB converters with unequal dc-source modules were also revealed to have some advantages by scholarly research [5], the loss of modularity make them unfavorable choices for practical drive products. In a practical CHB drive with equal dc-source cells, as each power cell independently contributes three voltage levels (+*E*, 0, -*E*), the entire converter is able to produce high quality multilevel output voltages, and may reach very high voltage and power ratings using only low-voltage IGBTs. It was reported that the maximum ratings for the CHB converter in use is 13.8 kV / 31000 kVA [1]. On the input side of the converter, the harmonic contents caused by the diode rectifiers are mostly cancelled out in the phase-shifting transformer. Therefore, the total input current has low harmonic distortion and can meet the grid requirements.

The CHB converter can be modulated by several multicarrier-based SPWM schemes, such as the phase-shifted SPWM (PS-SPWM) which employs horizontally shifted triangle carriers for comparison with the sinusoidal modulating wave, and the level-shifted SPWM (LS-SPWM) schemes where the carriers are vertically distributed in the modulation plane. The CHB converter can also be operated by staircase modulation, SVM, and SHE schemes. In practice, the most used scheme is the PS-SPWM which provides decent harmonic performance, even device switchings, and balanced load sharing among the contributing cells. It is worth noting the equivalent switching frequency of the CHB can be several times that of the device switching frequency, making the topology an attractive candidate for high-speed applications.

A main drawback of the CHB converter is its need for a costly and bulky phase-shifting transformer with many secondary windings. Moreover, if regenerative operation is required for a CHB, the diode rectifiers in the power cells have to be replaced by active rectifiers [36], leading to significantly increased cost and complex control.

Flying Capacitor Converter

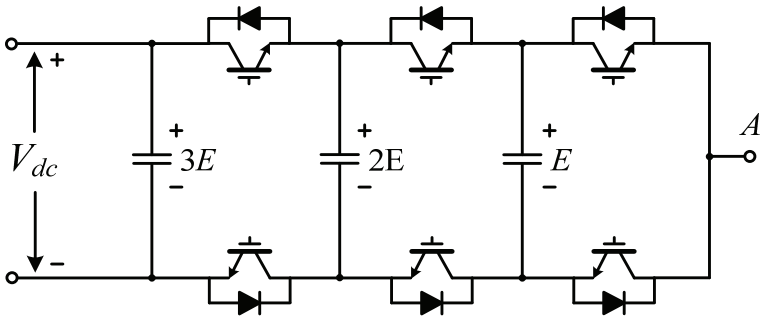


Fig. 1-7 Four-level flying capacitor converter (output phase A).

The flying capacitor (FLC) converter is among the classic multilevel converter topologies and has been well studied in the literature [17]. As shown in Fig. 1-7, The structure of the FLC is similar to that of the high-power two-level VSC, in which IGBT devices are connected in cascade in the phase legs to block the high dc-link voltage. However in an FLC, in addition to the switching devices, capacitors are added to the phase legs and connected between the switch pairs in the upper and lower half bridges, thereby clamping the device joints and introducing more output voltage levels. Although able to produce multilevel output waveforms, the FLC converter requires a large number of extra capacitors that need to be charged during startup and balanced during normal operation, which is main drawback of the topology. FLC converter based drive is offered by only one

manufacturer in the market and is much less popular than the NPC and CHB based products.

NPC/H-bridge Converter

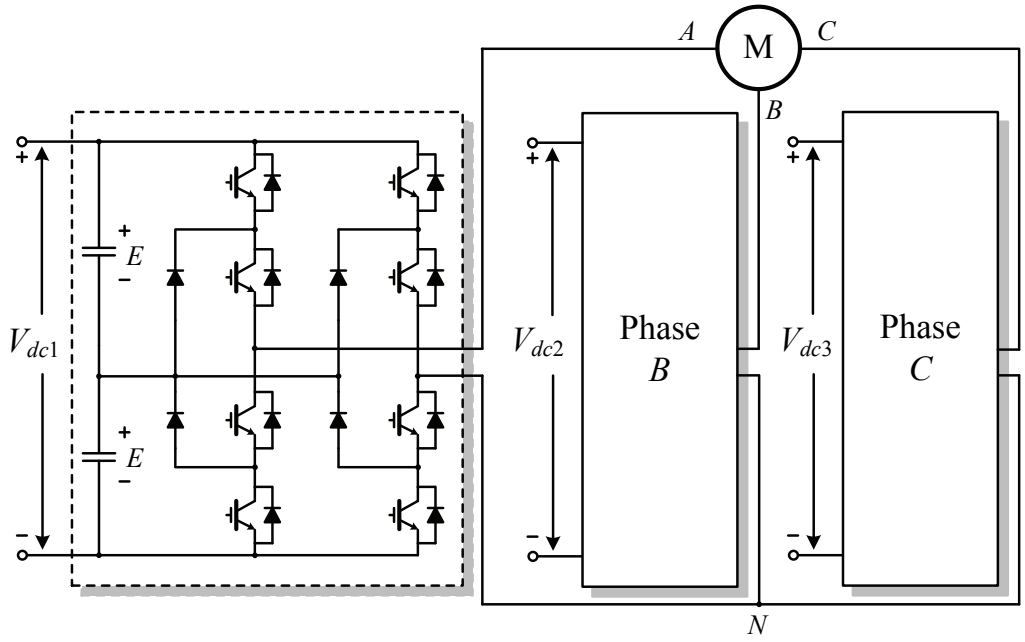


Fig. 1-8 NPC/H-bridge converter based MV drive.

The NPC/H-bridge converter in Fig. 1-8 employs two NPC legs to support each of its three output phases [37]. The two NPC legs are connected in the H-bridge configuration and able to generate five output voltage levels between their output terminal pair. Because each H-bridge provides one output terminal to be connected with those from the other phases, the three H-bridges in the converter cannot share a common dc-link as in the NPC converter. Instead, they need to be fed by isolated multi-pulse rectifier configurations from the input phase-shifting transformer. Having twice the device count in an NPC converter, the NPC/H-bridge converter provides more voltage levels and covers a higher

power/voltage range than the NPC does. Currently, two manufacturers offer NPC/H-bridge converter based MV drive products with the voltage rating up to 6.9 kV.

Five-level Active NPC Converter

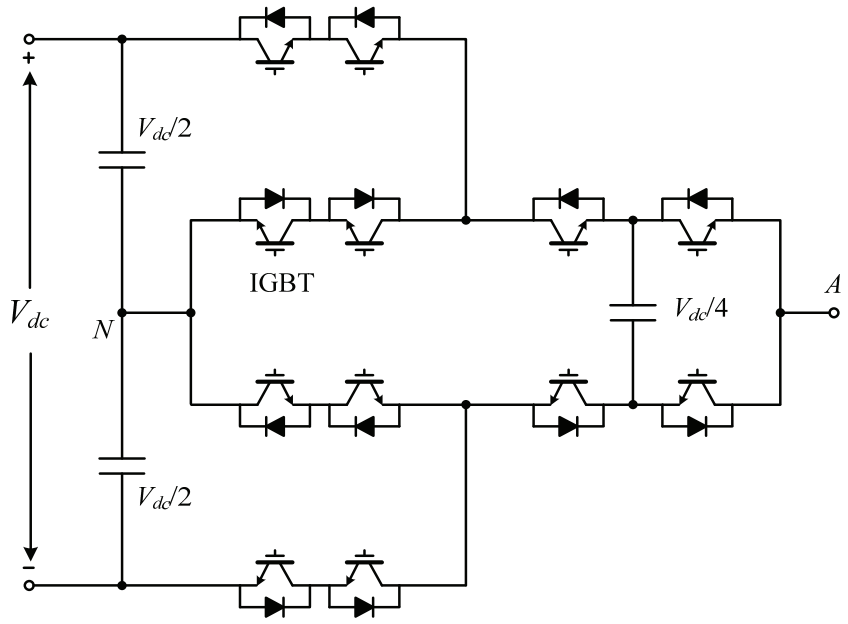


Fig. 1-9 Five-level active NPC converter (output phase *A*).

The three-level ANPC was further extended into a five-level converter topology in recent years [6, 7, 38]. The outcome is called a five-level ANPC but can be essentially considered as a hybrid combination of a three-level ANPC and a basic flying capacitor power cell. Fig. 1-9 shows the circuit diagram of the five-level ANPC for a single output phase. Through the use of redundant switching states, the voltage across the added flying capacitor is maintained at 1/4 of the dc-link voltage, such that the inverter phase output voltage can be chosen from the following five voltage levels (with respect to the dc neutral

point): $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$. Taking into account the voltage stress in the converter, series connection of devices is required in the ANPC part to enable use of unified devices with the same voltage rating. The back-to-back configuration of the five-level ANPC topology has been commercialized as an MV drive by one leading manufacturer, with the power rating up to 1 MVA / 6.9 kV and transformerless option available [7].

Modular Multilevel Converter

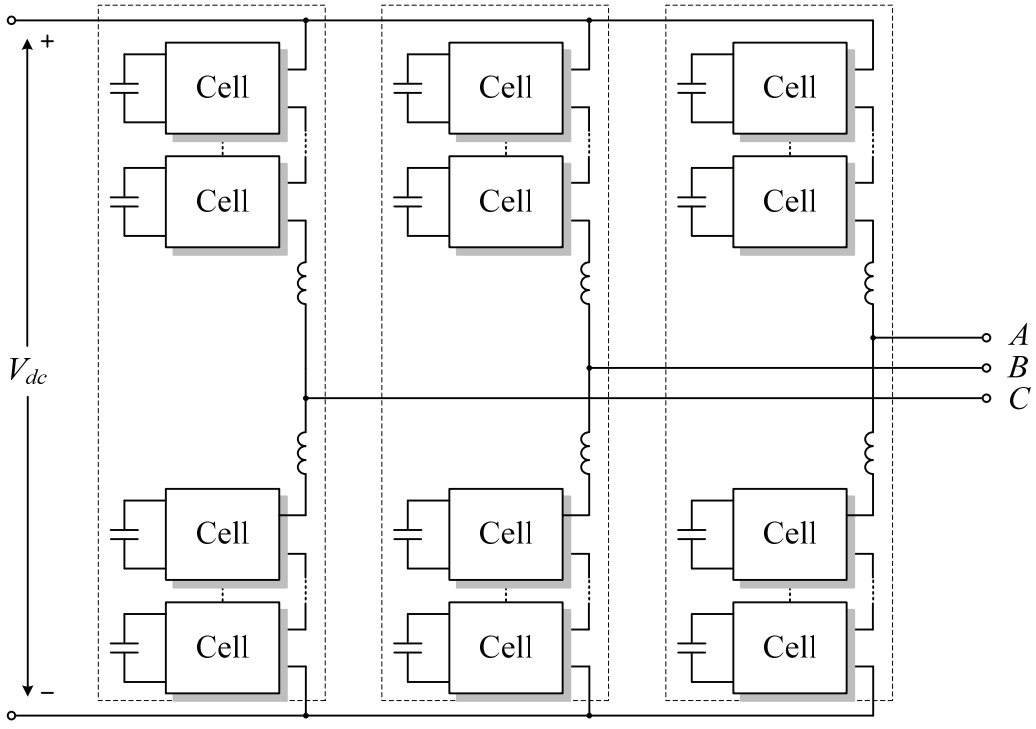


Fig. 1-10 Modular multilevel converter.

The modular multilevel converter (MMC) is a relatively new topology proposed for high-power applications [8, 9, 39]. During the past decade, it has attracted increasing

interest and has found industrial presence in a light-weight high-voltage direct current (HVDC) transmission system. The MMC is composed of stacks of series connected half-bridge choppers formed by two IGBTs and a capacitor. Each MMC phase leg consists of a positive stack and a negative stack as well as the necessary output inductors. Due to the cascaded structure, the MMC features very good modularity and scalability, and is therefore able to undertake very high voltages. Not like the CHB converter which is also based on series connection of power cells, the power modules in MMC do not need isolated dc sources. Therefore, the three inverter legs in the MMC can share a common dc-link fed by a common rectifier. The use of MMC for MV drive application was proposed in [40], where it was revealed the fluctuation of the chopper capacitor voltages are related to the motor current frequency. It was also concluded in [8] that the converter can be adapted for loads such as the fans, pumps, blowers and compressors, while not suitable for high-torque low-speed applications.

1.2.2 ac-ac Direct Converters

Unlike indirect converters that invariably synthesize output voltage or current from a dc-link stage supported by passive elements, the ac-ac converters perform single-stage power conversion directly from the ac inputs and are free of any dc-link components. To date, only a few ac-ac direct converters have found presence in the MV drive industry. These include the classic cycloconverters and one particular type of the newly developed multilevel MC topologies.

Cycloconverter

A cycloconverter is a direct frequency changer whereby fixed magnitude fixed frequency input ac power is converted to output ac power in a single stage [2]. With groups of thyristors employed and operated coordinately, both magnitude and frequency of the output can be varied. In order to avoid severe waveform distortion, the output frequency of a cycloconverter cannot exceed a fraction of the input frequency. The output voltage is constituted from selected portions of the input voltage pulses, and its magnitude can be adjusted by means of phase angle control. Motor drives using cycloconverters possess advantages such as simple structure, high reliability, low switching losses and very high efficiency due to the use of naturally commutated thyristor devices. Furthermore, these converters can be operated in all four quadrants and have inherent capability of bi-directional power flow. On the other hand, also owing to the use of phase controlled thyristors, the input power factor of cycloconverters is generally low, with significant harmonic currents being drawn from the grid by the converter. Cycloconverters are mainly used in low-speed high-power motor drives in industries of cement, mining, metals and the like. It should be mentioned that cycloconverter based drives are not as popular as inverter based drives in new designs due to technology advancement and performance improvement of the latter.

Matrix Converters

Although matrix converters (MCs) share the same basic functionality with cycloconverters: to perform single stage ac power conversion with variable magnitude and variable frequency, the MCs differ from the cycloconverters in many aspects. Equipped with four-quadrant bidirectional switches made up of force-commutated devices such as IGBT, a typical MC is able to generate output voltages with either higher or lower frequencies than that of the input. A conventional MC features inherent four quadrant

operation capability, sinusoidal input/output waveforms, and a controllable input power factor [14, 41]. If compared with dc-link based indirect converters, the MC possesses several advantages such as reduced size and higher power density, improved lifespan due to elimination of the bulky and often trouble-causing dc-link component, and faster dynamic performance owing to its single stage conversion. Nevertheless, for the same reason of the avoided dc-link component, MCs are also known for their relatively complex modulation and commutation techniques, limited voltage transfer ratio, and lack of ride-through capability.

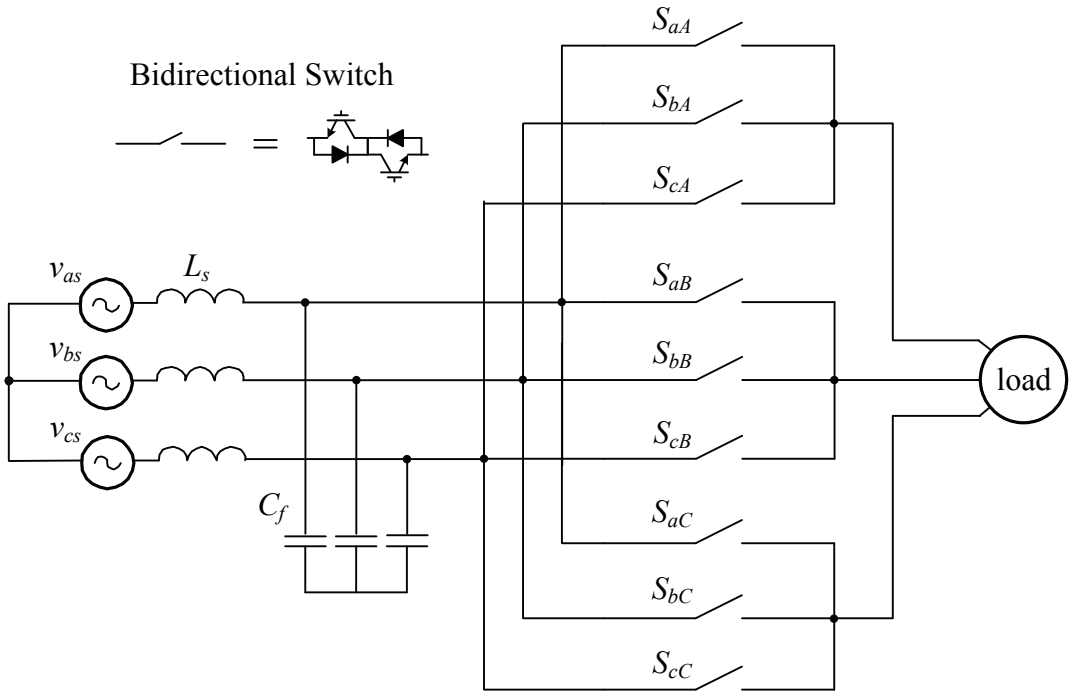


Fig. 1-11 Three-phase to three-phase conventional MC.

With maturation of suitable power devices and advancement of control, the MC has been considered an alternative topology for dc-link converters where power density and

regeneration capability are of great importance. Among all configurations, the three-input three-output MC (3 x 3 MC) as shown in Fig. 1-11 and its topological variants have attracted the most research interest. Although study on the conventional MC can be traced back to several decades ago [13], the topic only started to resurge lately and has regained much attention during the past years. Owing to the solving of several major technical challenges such as bidirectional switch commutation control, the MC has been pushed closer to practical application. It is worth mentioning that the first commercial MC based adjustable speed drive was already released [12]. So far, most of the research work about MC falls into the low-voltage category where the converter can be operated at a relatively high switching frequency, whereas the high power applications had never considered MC as a viable option due to concerns on efficiency and power device rating limitations.

Recently, there has been an increasing interest in introducing MCs into the high-power arena [20, 42-44]. Taking account of the limited voltage ratings of existing power semiconductors, the conventional 3 x 3 MC is still not a viable option for higher voltage applications. In view of this, researchers have directed attention to come up with new MC topologies which incorporate the concepts of multilevel converters. During the past decade, the ideas of several major multilevel VSC topologies have been utilized and combined with the conventional MC concept, resulting in the emergence of the neutral-point-clamped multilevel MCs, the capacitor clamped multilevel MC, and the multi-module based multilevel MCs. In addition to being members of the MC family, these new topologies also possess features similar to the multilevel VSCs. Correspondingly, their modulation and control aspects have been studied in a number of publications [10, 11, 19-21, 44, 45].

The neutral-point-clamped multilevel MCs are developed from the indirect construction of the conventional MCs. The indirect construction separates the whole converter into a rectifier stage and an inverter stage with no dc-link components. Instead of using a two-level VSC, a three-level NPC converter is employed in the inverter stage to provide more

output voltage levels. Recently, several topological variants of the NPC multilevel MC have been discussed in a few publications [10, 19, 43]. Compared with the conventional MC, the neutral-point-clamped MCs improve the output voltage quality at the cost of increased device count. However, the device voltage stress, especially for those in the rectifier stage, is not reduced. The topology is therefore still not suitable for higher voltage applications.

Another novel multilevel MC topology, the capacitor clamped multilevel MC, was proposed in 2005 [20]. This converter employs six flying capacitors to balance voltage distribution among series connected switch modules and to provide middle voltage levels. The voltage stress on the switches is halved comparing to that of a conventional MC. In the meantime, the harmonics in the output voltage and current waveforms are also significantly lowered. The main disadvantage of this topology lies in the large amount of clamping capacitors required, as well as the increased device count and complex converter structure.

At present, the only multilevel MC topology that has found commercial presence is the multimodular matrix converter (MMMC) [11, 12]. Formed by three-phase to single-phase MC (3 x 2 MC) modules, the MMMCs are very similar to the CHB converter in terms of topological structure, but are different from the latter in the construction of constituent power modules. In a CHB converter, each module contains a dc-link capacitor, and the output voltages are synthesized from the dc voltage; whereas in an MMMC, the output voltages of any single module are directly fabricated from the three-phase ac inputs. Due to the series connection of power modules, the MMMC can reach high voltage and power levels while using low-voltage IGBTs only. Meanwhile, they also need the input phase-shifting transformer to provide isolated ac sources, just like the CHB converter.

Proper operation of the MMMC topologies relies on suitable modulation schemes that can generate variable frequency sinusoidal waveforms at both ac terminals. To date, there is

no comprehensive study on the modulation scheme design for the MMMCs. It is therefore this work's primary aim to propose and develop appropriate modulation schemes for these particular converters.

1.3 Dissertation Objectives

Modulation scheme design for the MMMC topologies is not a straightforward task. Unlike the conventional MCs that feature a three-phase-in three-phase-out balanced structure, or the dc-link based indirect converters where the dc component decouples the rectifier and inverter stages, the MMMCs are composed of 3 x 2 MC modules in which the power flow is pulsating. Although synthesis of sinusoidal output voltage waveforms can be achieved without much difficulty, the simultaneous generation of sinusoidal line-side current waveforms requires coordination among different MC modules and needs careful design. Aiming at developing various possible modulation schemes for the MMMCs, the main objectives of this dissertation are listed as follows:

1) Establish the mathematical transfer function matrix of the MMMCs as a basis for modulation scheme design. Propose a direct transfer function based modulation scheme together with a suitable switching pattern to generate sinusoidal waveforms at both sides of the converters.

2) By applying the classic fictitious dc-link concept, create an equivalent indirect circuit model for the MMMCs to lay a foundation for the design of indirect space vector based modulation schemes. Based on the developed model, design indirect modulation schemes and novel switching patterns to improve waveform quality.

3) Develop a novel modulation scheme based on diode front-end emulation and phase-shifted SPWM. Different from the other proposed strategies, this new method

allows the use of an indirect module structure with significantly reduced device count and structure complexity, which come at the price of sacrificing the input power factor adjustment capability.

4) Provide simulation results to verify the proposed concepts, and build a low-voltage prototype of a nine-module system to further test the modulation schemes experimentally.

1.4 Dissertation Outline

This dissertation consists of six chapters which are organized as follows.

Chapter 1 provides the background and introduction of the study.

Chapter 2 describes the MMMC topologies, then proposes a direct transfer-function-based modulation scheme for generating sinusoidal waveforms at both sides of the converters. Starting with the most fundamental three-module version of the topology, it is revealed that, although the input currents of individual 3 x 2 MC modules contain significant harmonic distortion, the total line-side currents, being the sum of the secondary currents referred to the primary side of the transformer, can still be sinusoidal when a proper modulation method is applied.

Chapter 3 presents an indirect circuit modeling to design indirect space vector based modulation schemes for the MMMCs. Based on the fictitious dc-link concept, the indirect model separates the converter into a rectifier stage and an inverter stage. SVM methods for current-source rectifier and voltage-source inverters can then be independently applied to calculate the duty ratios needed for input current and output voltage synthesis. After the duty ratios are converted and combined, gate signals for the real switches are generated

according to two switching patterns. The second proposed switching pattern is proved to offer a superior harmonic profile in the generated waveforms.

Chapter 4 proposes a simple modulation method for the nine-module MMMC fed by an input phase-shifting transformer. Focusing only on fabricating multilevel output voltage waveforms, the method is essentially a combination of diode front-end emulation with phase-shifted SPWM. Although the method does not bother with input current synthesis, because power balance among modules on a same output phase is guaranteed, and owing to the harmonic elimination capability of the phase-shifting transformer, sinusoidal input current with good quality can still be achieved.

Chapter 5 introduces a low-voltage lab prototype constructed for experimental verification of the proposed modulation schemes. Details about the implementation of the power modules, voltage and current measurement, device commutation control as well as module synchronization, communication and protection are provided.

Chapter 6 summarizes the main contributions and conclusions of the presented work. Possible future research directions are also suggested.

Chapter 2

Direct Modulation Scheme for the MMMC Topologies

The multimodular matrix converters (MMMCs) are comprised of a multiple number of three-phase to single-phase (3 x 2) matrix converter (MC) modules. The MC modules are normally fed by a multi-winding input transformer, and can be cascaded on the load side to provide high voltage/power output without using power devices of increased voltage ratings. Similar to the cascaded H-bridge (CHB) converter, the MMMCs possess features such as modular design, high quality multi-stepped output voltage waveform, and allow the use of low-voltage power semiconductors under mass production. Moreover, the MMMCs eliminate the dc components necessary in the CHB, and they are inherently regenerative. Due to the unique topological structure, established modulation schemes for neither the CHB converter nor the conventional three-phase to three-phase (3 x 3) MCs can be directly applied to operate the MMMCs. In each 3 x 2 MC module, although generating any desired single-phase output voltage from the three-phase input voltages by means of pulse-width modulation (PWM) is not difficult to achieve, to synthesize three-phase input sinusoidal currents from the single-phase output current is basically an impossible job. The fact can also be appreciated from the power balance perspective, as the single-phase output power is always pulsating, while a balanced three-phase input provides a constant power flow.

The main objective of this chapter is to develop a direct modulation scheme for the MMMCs to synthesize sinusoidal voltage/current waveforms on both ac sides of the converters. Rather than trying to fabricate sinusoidal currents right at the input ports of the MC modules, the proposed strategy targets the total input currents on the primary side of the multi-winding transformer. It will be demonstrated that although the three-phase input currents of each MC module have distortions, the sum of the secondary-winding currents eventually becomes sinusoidal when referred to the primary side of the transformer. As for the output voltage, the generated frequency can be either higher or lower than that of the input, making the converters and the modulation scheme suitable for medium-voltage (MV) drive application where the output voltage and frequency need to be variable to control the machine load.

2.1 Topological Structure of the MMMCs

2.1.1 Three-Phase to Single-Phase (3 x 2) MC Module

The fundamental building block for the MMMC topologies is a three-phase-in single-phase-out MC module which consists of six bidirectional power switches. As shown in Fig. 1-1, each bidirectional switch can be practically formed by two insulated-gate bipolar transistor (IGBT)-diode pairs connected in anti-series, or by two reverse blocking IGBTs (RB-IGBT) connected in anti-parallel [46]. Since the bidirectional switches are four quadrant operable, they are able to block voltages of both polarities and allow currents in either direction. Under normal operating conditions, when the switches in the module are turned ON and OFF, the output terminals p and q can be arbitrarily connected to any one of the three input terminals a, b, and c to choose a proper voltage level. The input-side terminals of the MC module are fed by a three-phase power supply [v_{as}, v_{bs}, v_{cs}]. A three-

phase ac filter capacitor is needed at the input port of the module to assist switching commutation and suppress current harmonics. On the output side, the module should be connected to an inductive load, whose continuous current is utilized as a current source for fabrication of desired input currents.

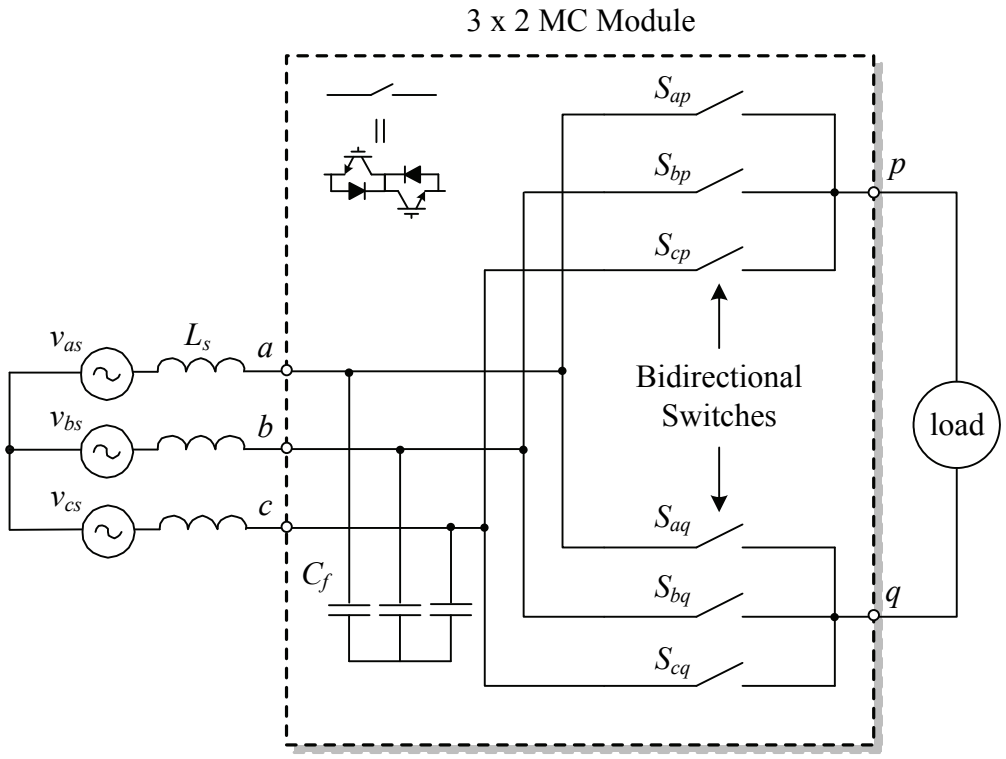


Fig. 2-1 Simplified diagram of a 3 x 2 MC module.

Similar to the conventional 3 x 3 MCs, the 3 x 2 MC module is subject to switching constraints. Any switching state that may cause short circuit of the filter capacitors or interrupt of the inductive load current is prohibited. Hence, at any instant of time, two and only two switches in the module, one from the upper group of [S_{ap}, S_{bp}, S_{cp}] and the other from the lower group of [S_{aq}, S_{bq}, S_{cq}] must be in the ON state. The switching constraint for the 3 x 2 MC module can be mathematically expressed as follows

$$\begin{cases} S_{ap}(t)+S_{bp}(t)+S_{cp}(t)=1 \\ S_{aq}(t)+S_{bq}(t)+S_{cq}(t)=1, \end{cases} \tag{2.1}$$

$$\text{where } S_{jk}(t)=\begin{cases} 1,\ S_{jk}\ is\ ON \\ 0,\ S_{jk}\ is\ OFF, \end{cases} \quad j\in\{a,b,c\},\ k\in\{p,q\}.$$

The switching constraint provides a basis for the modulation and switching state design for the MMMCs. In addition, due to the use of bidirectional switches, device commutation between different phases should comply with the constraint as well to avoid short circuit of the capacitors and open circuit of the inductive load during transients. Same as the direct type conventional 3 x 3 MC, the 3 x 2 MC modules can readily adopt the load current or input voltage based multi-step commutation strategies for device commutation control [47]. The principle and implementation details of the commutation are explained in Chapter 5.

2.1.2 Three-Module Multimodular Matrix Converter-I

Using three 3 x 2 MC modules, the simplest version of the MMMC topology (MMMC-I) can be built to supply an inductive load. Fig. 2-2 shows the simplified circuit diagram of MMMC-I, where a three-phase-four-winding transformer is employed to provide isolation and the required secondary-winding voltage level. The MC modules act as the interface between the input transformer and the load. On the input side, each module is fed by one of the secondary windings of the transformer, and ac filter capacitors are present to assist commutation as well as to filter the switching harmonics. On the output side, the q terminals from all the modules are connected together to form a reference neutral point,

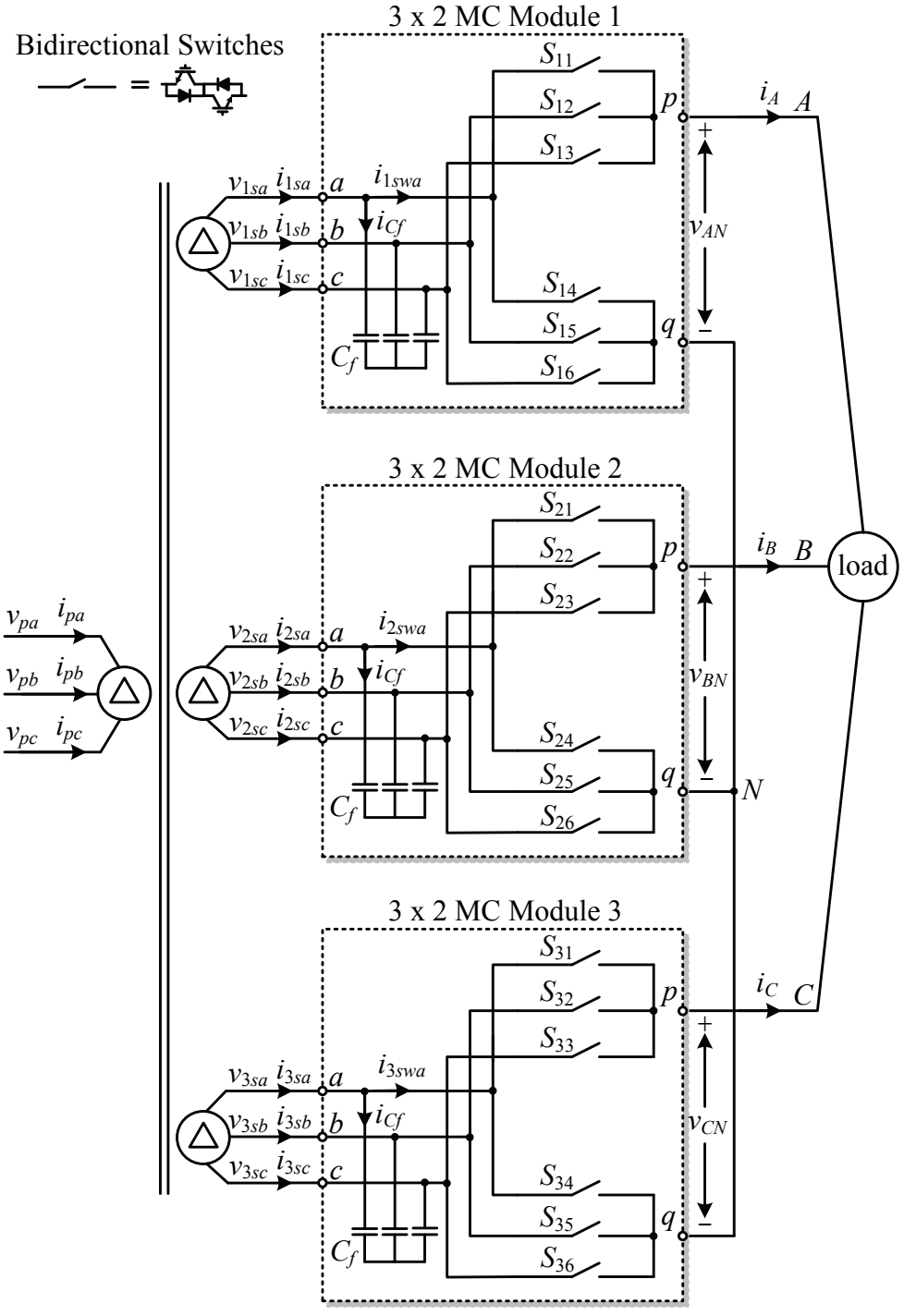


Fig. 2-2 Simplified circuit diagram of three-module MMMC-I.

while the p terminals are directly connected to the load phases. The load of the converter could be either a three-phase RL or an ac machine, the inductive nature of which is necessary for the proper operation of the MC modules.

2.1.3 Nine-Module Multimodular Matrix Converter-II

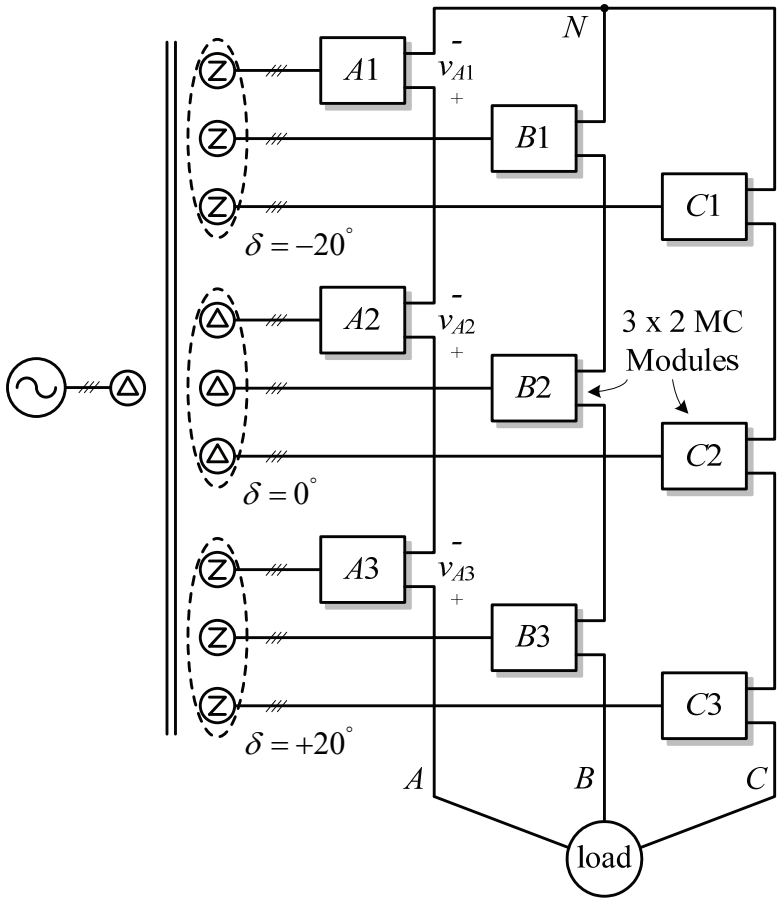


Fig. 2-3 Simplified circuit diagram of nine-module MMMC-II.

If a larger number of MC modules are employed, the fundamental three-module MMMC-I can be extended to multilevel configurations for higher power/voltage output

levels and better waveform quality. Fig. 2-3 illustrates the simplified circuit diagram of a nine-module version of the MMMC. Designated as MMMC-II, the converter is equipped with three MC modules on each of its output phases which are fed by a phase-shifting transformer having nine secondary windings. The secondary windings of the transformer are arranged into three groups with phase displacements of -20º, 0º and +20º, respectively. This configuration allows for cancellation of several unwanted low-order harmonic currents on the primary side [48]. The whole converter of MMMC-II can be essentially viewed as three sets of MMMC-Is connected in series. It is also very similar to the seven-level CHB converter in terms of structure, except that the H-bridge switching cells in the latter are replaced by the MC modules without dc capacitors.

In order to achieve even higher power and voltage output levels, the number of MC modules employed for series connection can be further increased. The commercial MV drive based on the MMMC topology, as an example, puts six MC modules in series per phase to reach a voltage level of 6.6 kV [12]. Nevertheless, this would require the input phase-shifting transformer to have a larger number of secondary windings and more sophisticated phase displacement arrangements, similar to the case of multilevel CHB converters.

2.2 Direct Modulation Scheme for the MMMCs

The challenge for the design of a modulation scheme suitable for the MMMCs lies in how to produce sinusoidal voltage/current waveforms on both sides of the converter. Just like in a conventional 3 x 3 MC, the inputs of the MC modules are regarded as voltage sources whereas the outputs are taken as current sources due to the inductive load. The task of a properly designed modulation scheme is to assemble sinusoidal output voltages from segments of the input voltages, and fabricate sinusoidal input currents with pieces from the

load currents, both at the same time. For the conventional 3 x 3 MC, a large number of modulation schemes have been well established in the literature [15, 49-56]. However, these methods cannot be directly applied to the MMMCs. As mentioned earlier, in each individual 3 x 2 MC module, although it is not difficult to generate any desired single-phase output voltage, to directly synthesize three-phase sinusoidal input currents from the single-phase output current would be almost impossible.

The succeeding sections present a direct-transfer-function-based modulation strategy for the MMMCs. The explanation is first carried out based on the three-module MMMC-I. Since the more complicated versions are essentially cascaded connection of multiple sets of MMMC-I, the basic modulation scheme can be easily modified to control them. Instead of trying to obtain sinusoidal currents at the input ports of the MC modules, the proposed scheme targets the total input currents on the primary side of the transformer. As a result of the modulation, although the input currents of each MC module are not sinusoids, the total input current at the primary side of the transformer is sinusoidal and well follows the angle reference. For the output voltage, the frequency and angle can be arbitrarily set, and the magnitude can be controlled through the modulation index adjustment.

2.2.1 Transfer Function Matrix Derivation

Referring to the circuit diagram of MMMC-I in Fig. 2-2, because all the three-phase windings of the input transformer have the same phase shifts, the relationship between the instantaneous output and input voltages of the converter can be established by means of a switching function matrix

$$v_L = \begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \begin{bmatrix} S_{11} - S_{14} & S_{12} - S_{15} & S_{13} - S_{16} \\ S_{21} - S_{24} & S_{22} - S_{25} & S_{23} - S_{26} \\ S_{31} - S_{34} & S_{32} - S_{35} & S_{33} - S_{36} \end{bmatrix} \begin{bmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{bmatrix} = H \begin{bmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{bmatrix} \tag{2.2}$$

in which the transformer-secondary-winding-fed input voltages of the MC modules (neglecting the voltage drops on line and leakage inductances) are given by

$$v_1 = \begin{bmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{bmatrix} = V_S \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t - 2\pi/3) \\ \cos(\omega_i t + 2\pi/3) \end{bmatrix} \tag{2.3}$$

where V_S and ω_i represent the magnitude and frequency of the secondary winding voltages, respectively. On the other hand, the fundamental components of the desired MC output voltages can be written as

$$\overline{v}_L = \begin{bmatrix} \overline{v}_{AN} \\ \overline{v}_{BN} \\ \overline{v}_{CN} \end{bmatrix} = V_L \begin{bmatrix} \cos(\omega_o t + \theta_o) \\ \cos(\omega_o t + \theta_o - 2\pi/3) \\ \cos(\omega_o t + \theta_o + 2\pi/3) \end{bmatrix} \tag{2.4}$$

in which V_L, ω_o, and θ_o denote the desired voltage magnitude, frequency, and phase angle of the output fundamental component, respectively. Suppose the converter is operated with

a switching frequency sufficiently higher than the input and output fundamental frequencies, the low-frequency form of (2.2) can be obtained by averaging it over the switching period

$$\overline{v}_L = \begin{bmatrix} \overline{v}_{AN} \\ \overline{v}_{BN} \\ \overline{v}_{CN} \end{bmatrix} = \begin{bmatrix} d_{11} - d_{14} & d_{12} - d_{15} & d_{13} - d_{16} \\ d_{21} - d_{24} & d_{22} - d_{25} & d_{23} - d_{26} \\ d_{31} - d_{34} & d_{32} - d_{35} & d_{33} - d_{36} \end{bmatrix} \begin{bmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{bmatrix} = \overline{H} \begin{bmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{bmatrix} \tag{2.5}$$

where d_{jk} represents the duty ratio of switch S_{jk}. As for the currents, the fundamental components of the load currents that are utilized for the input current synthesis can be expressed in terms of the output voltage and the load

$$i_L = \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \frac{\overline{v}_L}{Z} = \frac{\overline{v}_L}{|Z| \angle \theta_L} = \frac{V_L}{|Z|} \begin{bmatrix} \cos(\omega_o t + \theta_o - \theta_L) \\ \cos(\omega_o t + \theta_o - \theta_L - 2\pi/3) \\ \cos(\omega_o t + \theta_o - \theta_L + 2\pi/3) \end{bmatrix}. \tag{2.6}$$

In (2.6), Z and θ_L designate the load impedance and load power factor angle, respectively. Considering the transformer's turns ratio N_s / N_p and the influence of the filter capacitors, the total input current at the primary side of the transformer can be written as (taking phase *a* as an example)

$$
\begin{aligned}
i_a &= \frac{N_S}{N_P}(i_{1a} + i_{2a} + i_{3a}) \\
&= \frac{N_S}{N_P}\left(\begin{bmatrix} S_{11} - S_{14} & S_{21} - S_{24} & S_{31} - S_{34} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} + 3C_f dv_{1a} / dt \right).
\end{aligned} \tag{2.7}
$$

Hence, the low-frequency form of the three-phase input currents can be given in (2.8)

$$
\begin{aligned}
\overline{i}_i = \begin{bmatrix} \overline{i}_a \\ \overline{i}_b \\ \overline{i}_c \end{bmatrix} &= \frac{N_S}{N_P}\left(\begin{bmatrix} d_{11} - d_{14} & d_{21} - d_{24} & d_{31} - d_{34} \\ d_{12} - d_{15} & d_{22} - d_{25} & d_{32} - d_{35} \\ d_{13} - d_{16} & d_{23} - d_{26} & d_{33} - d_{36} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} + 3C_f \begin{bmatrix} dv_{1a} / dt \\ dv_{1b} / dt \\ dv_{1c} / dt \end{bmatrix} \right) \\
&= \frac{N_S}{N_P}\left(\overline{H}^T i_L + 3C_f dv_1 / dt \right).
\end{aligned} \tag{2.8}
$$

In order to obtain any desired output voltages with variable magnitude and variable frequency while achieving sinusoidal three-phase input currents, the solution to the transfer matrix, H, is derived in (2.9) based on the above equations. In the expression of H, θ_i is an arbitrary angle that can be utilized to control the input power factor, whereas m_a designates the modulation index for output magnitude adjustment. The low-frequency duty-ratio equivalent, $\overline{H}$, can be easily obtained by performing a regular sampling to H with the switching period, i.e. substituting nT_s into (2.9) for t.

$$H = m_a \begin{bmatrix} \cos(\omega_o t + \theta_o) \\ \cos(\omega_o t + \theta_o - 2\pi/3) \\ \cos(\omega_o t + \theta_o + 2\pi/3) \end{bmatrix} \begin{bmatrix} \cos(\omega_i t + \theta_i) & \cos(\omega_i t + \theta_i - 2\pi/3) & \cos(\omega_i t + \theta_i + 2\pi/3) \end{bmatrix}$$

$$= m_a \begin{bmatrix} \cos(\omega_o t + \theta_o) & \cos(\omega_o t + \theta_o) & \cos(\omega_o t + \theta_o) \\ \cos(\omega_i t + \theta_i) & \cos(\omega_i t + \theta_i - 2\pi/3) & \cos(\omega_i t + \theta_i + 2\pi/3) \\ \cos(\omega_o t + \theta_o - 2\pi/3) & \cos(\omega_o t + \theta_o - 2\pi/3) & \cos(\omega_o t + \theta_o - 2\pi/3) \\ \cos(\omega_i t + \theta_i) & \cos(\omega_i t + \theta_i - 2\pi/3) & \cos(\omega_i t + \theta_i + 2\pi/3) \\ \cos(\omega_o t + \theta_o + 2\pi/3) & \cos(\omega_o t + \theta_o + 2\pi/3) & \cos(\omega_o t + \theta_o + 2\pi/3) \\ \cos(\omega_i t + \theta_i) & \cos(\omega_i t + \theta_i - 2\pi/3) & \cos(\omega_i t + \theta_i + 2\pi/3) \end{bmatrix}.$$

(2.9)

The magnitudes of the input and output voltages can now be related as follows

$$V_L = \frac{3}{2} V_S \cdot m_a \cdot \cos(\theta_i). \tag{2.10}$$

If the input transformer is taken into account, the voltage transfer equation of the whole converter can be rewritten as

$$V_L = \frac{3}{2} \cdot \frac{N_S}{N_P} \cdot V_i \cdot m_a \cdot \cos(\theta_i) \tag{2.11}$$

where V_i designates the primary winding voltage magnitude. As a matter of fact, the limited voltage transfer ratio issue associated with conventional 3 x 3 MC [57] becomes a lesser concern in the MMMCs, as the transformer is able to provide an adequate secondary voltage level with a properly designed turns ratio.

2.2.2 Switching Pattern

After the duty ratios of the switches are determined by the transfer matrix, a certain switching pattern is needed for setting the commutation instants in the MC modules during a specific switching period. Here, a simple pattern with center-placed double-sided pulses is employed to investigate the performance of the modulation scheme. Without loss of generality, we take the first 3 x 2 MC module (the one supplying load phase *A*) in Fig. 2-2 as an example to explain the switching sequence. It is easy to identify that the duty ratios for the six switches in this module ($S_{11} \sim S_{16}$) are calculated from the first row of the transfer matrix, i.e. ($\bar{H}_{11} = d_{11} - d_{14}$, $\bar{H}_{12} = d_{12} - d_{15}$, $\bar{H}_{13} = d_{13} - d_{16}$), and their absolute values can be sorted and denoted as

$$\begin{cases} d_{\max} = \max(\left|\bar{H}_{11}\right|, \left|\bar{H}_{12}\right|, \left|\bar{H}_{13}\right|) \\ d_{\text{mid}} = \text{mid}(\left|\bar{H}_{11}\right|, \left|\bar{H}_{12}\right|, \left|\bar{H}_{13}\right|) \\ d_{\min} = \min(\left|\bar{H}_{11}\right|, \left|\bar{H}_{12}\right|, \left|\bar{H}_{13}\right|) \end{cases} . \tag{2.12}$$

For each pair of switches that are connected to the same input phase (S_{11} and S_{14}, S_{12} and S_{15}, S_{13} and S_{16}), which one to be controlled is decided by the polarity and value of the calculated duty ratio. Since the sum of $\bar{H}_{11}$, $\bar{H}_{12}$, and $\bar{H}_{13}$ is always zero, the one that has the maximum duty ratio is always of the opposite polarity to the rest two. Considering the case of $|\bar{H}_{11}| < |\bar{H}_{12}| < |\bar{H}_{13}|$ and $\bar{H}_{13} < 0$, the pattern is exemplified in Fig. 2-4. In this case, because $d_{\max} = |\bar{H}_{13}|$ and $\bar{H}_{13}$ is negative, S_{16} is kept ON throughout the entire switching period, whereas the three switches in the upper group (S_{11}, S_{12}, S_{13}) are successively turned ON and OFF in the specific order indicated by the pattern. Consequently, the output voltage of the module will be synthesized from two different input line-to-line voltages.

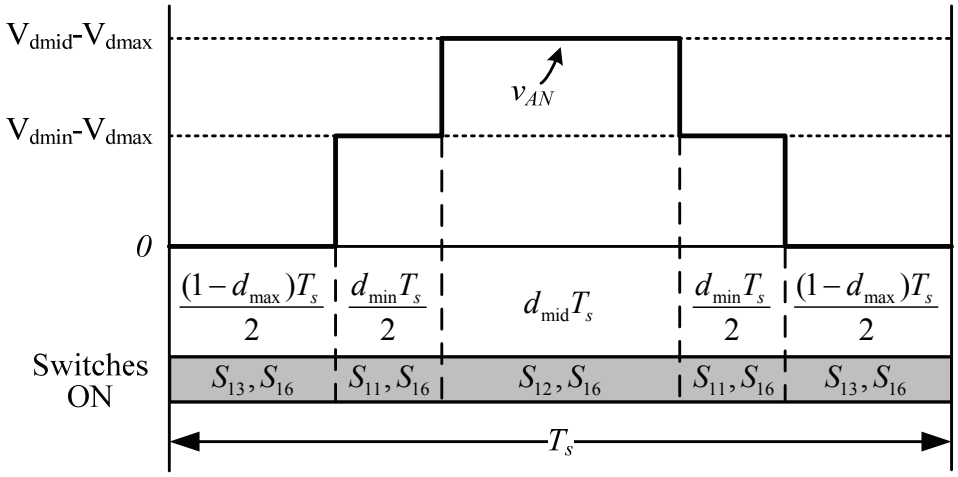


Fig. 2-4 Example of switching pattern in a complete switching period.

2.2.3 Switching Period Displacement for MMMC-II

Because the configuration of MMMCs with higher number of power modules can be essentially regarded as multiple sets of MMMC-Is in cascade, the direct modulation scheme

described in the last sections can be readily applied to control them. As for the nine-module MMMC-II, a total of three MMMC-I modulators are required. Each modulator is responsible for operating a group of three MC modules connected to the secondary windings that have the same phase shift.

In order to allow the input phase-shifting transformer to achieve maximum harmonic elimination performance, the input displacement modulation angles, θ_i , of the three modulators are required to have separate values to match their respective secondary winding phase shifts (-20º, 0º, +20º).

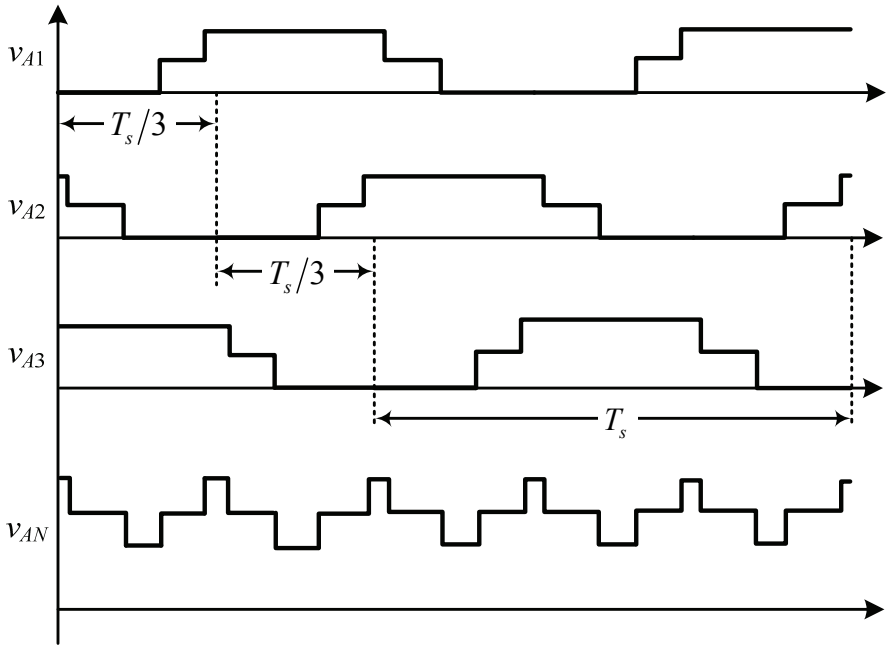


Fig. 2-5 Displaced switching periods and resultant phase voltage waveforms.

With reference to Fig. 2-3, on the output side of the converter, the total phase voltage impressed on the load is the sum of the individual output voltages from the three

contributing MC modules, e.g. $v_{AN} = v_{A1} + v_{A2} + v_{A3}$. Therefore, the output phase voltage references should be divided into three parts during any switching period. A simple and straightforward distribution would be to divide the references into three equal parts, such that a balanced load-power sharing among the transformer's secondary windings is achieved, allowing for a better harmonic elimination performance.

The last concern on the modulation of MMMC-II lies in how to set the switching instants within different MC modules. If the switching periods of the three modules in a same output phase are identically located on the time axis, switching transitions in different modules happen all at once, and the resultant output phase voltage would be the straight addition of the constituent pulses, leading to a voltage waveform with poor quality and high *dv*/*dt*. Alternatively, a displaced allocation of the switching periods can be employed among modules in the same output phase as a better solution. Exemplified in Fig. 2-5, the switching periods of module *A*1, *A*2 and *A*3 are displaced by one thirds of the complete period between one another. This approach is similar to the principle of phase-shifted modulation for the CHB converters, where the carriers are evenly distributed in the modulation plane to allow for phase shifts. The displaced switching periods effectively reduces the output voltage step and improves the waveform quality.

2.3 Simulation Results

Both MMMC-I and MMMC-II are modeled and simulated in MATLAB/Simulink to verify the validity of the topologies with the developed direct modulation scheme. The following part presents the simulation results of the models. The system parameters used for the simulations, such as the rated power and voltage, sampling and switching frequency as well as per-unit values of the passive components are listed in Table 2-1.

Table 2-1 System parameters for direct modulation scheme simulation

System Parameters	MMMC-I	MMMC-II
Rated Power	333 kVA	1 MVA
Grid Input Voltage (line-to-line, rms)	1387 V	4160 V
Input Frequency	60 Hz	60 Hz
Transformer Turns Ratio $N_P : N_S$	3 : 2	9 : 2
Sampling Frequency f_s	1.8 kHz	1.8 kHz
Device Switching Frequency f_{sw}	≈ 1.2 kHz	≈ 1.2 kHz
Total Line Inductance L_s (referred to the primary side)	0.08 pu	0.08 pu
Filter Capacitance C_f	0.2 pu	0.25 pu
Load Resistance R_L	0.9 pu	0.9 pu
Load Inductance L_L	0.25 pu	0.25 pu

2.3.1 Simulation Results for MMMC-I

Using the above-described modulation scheme, simulations for MMMC-I are carried out to supply a three-phase RL load. According to (2.11), the turns ratio of the input transformer is arranged to be 3 : 2 such that a unity total voltage gain can be obtained at the maximum modulation index. The sampling frequency for the modulation is 1.8 kHz. Based on the earlier-described switching pattern, each device in the converter is operated at around two third of the sampling frequency, i.e. 1.2 kHz.

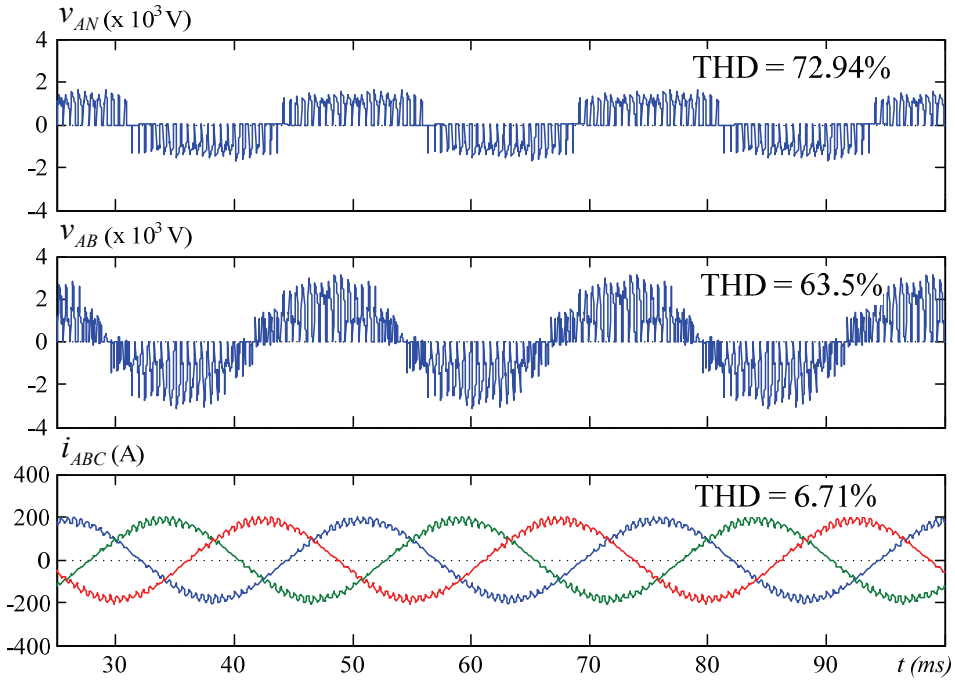


Fig. 2-6 Simulated output voltage and current waveforms of MMMC-I (f_o = 40 Hz, m_a = 0.9).

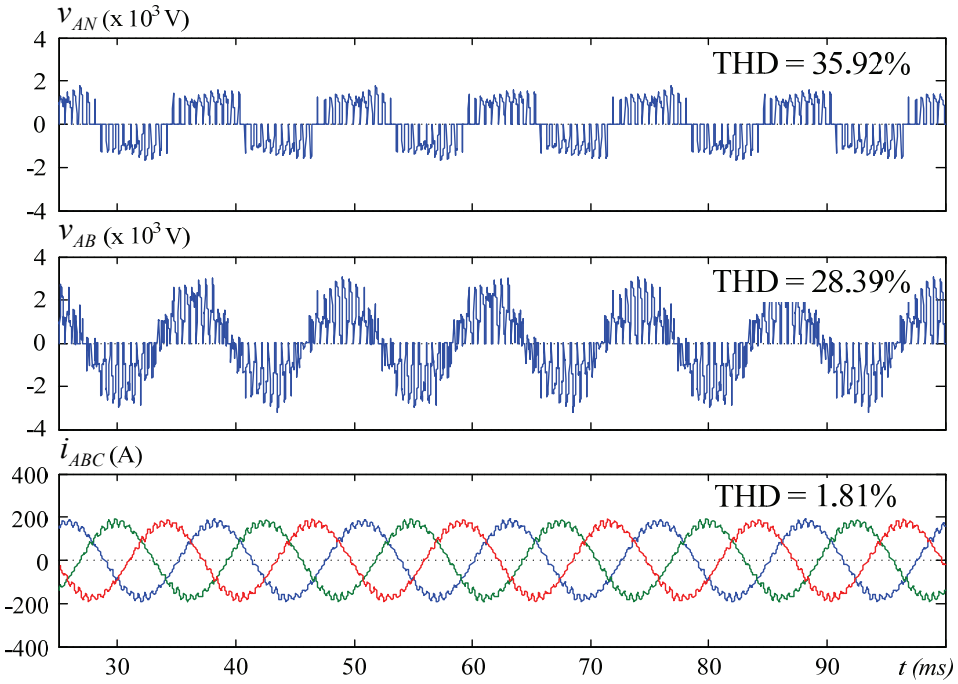


Fig. 2-7 Simulated output voltage and current waveforms of MMMC-I (f_o = 80 Hz, m_a = 0.9).

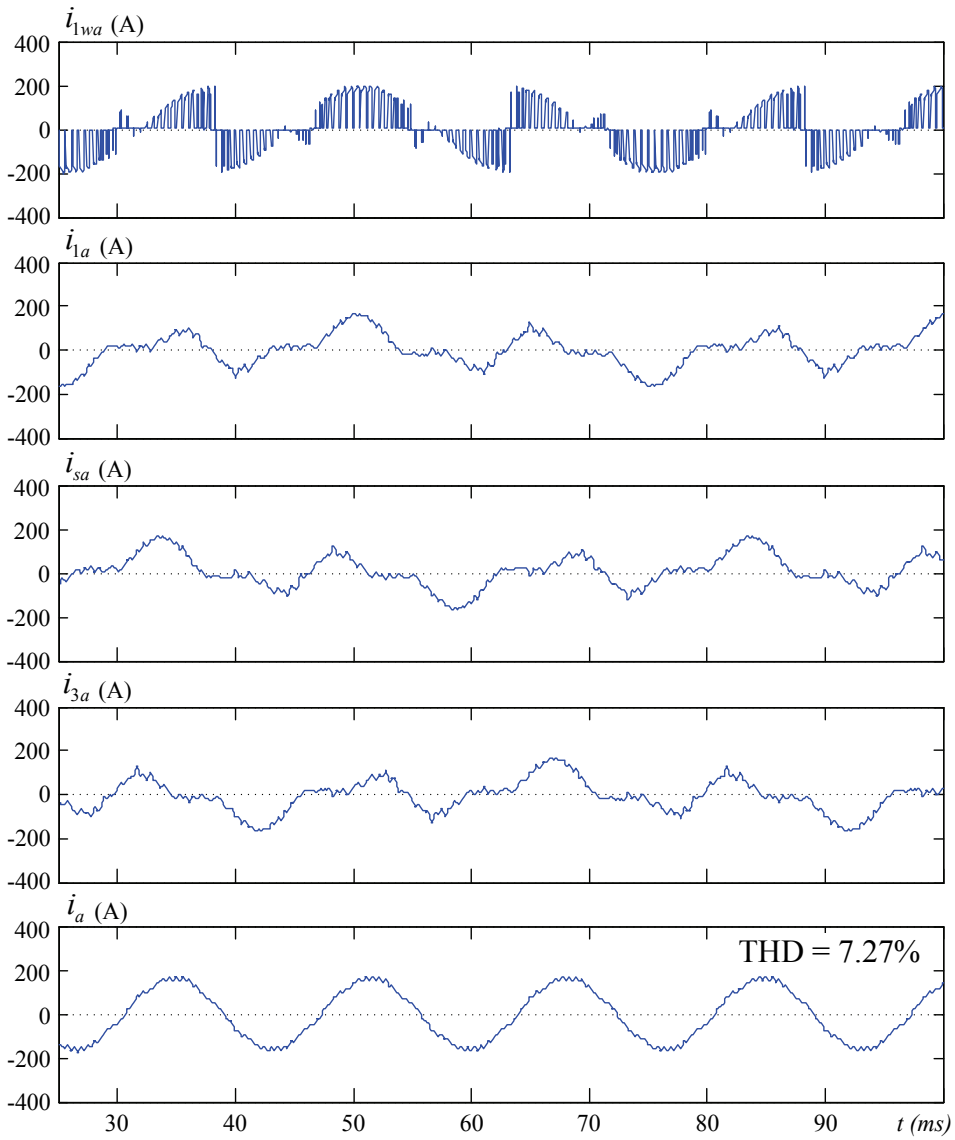


Fig. 2-8 Simulated input current waveforms of MMMC-I
(f_o = 40 Hz, m_a = 0.9).

In Fig. 2-6 and Fig. 2-7, typical waveforms of output voltage and current are illustrated for output fundamental frequencies of 40 Hz and 80 Hz, respectively. The figures show that the converter is able to yield output frequencies either lower or higher than that of the input. The output voltages are seen to be synthesized with chopped segments from the input voltages. Under a modulation index of 0.9, the line-to-line output voltage, v_{AB}, has an rms

value around 1200 V in both figures, almost equaling 0.9 times of the input voltage magnitude. The output currents are continuous sinusoidal waveforms and have a relatively low THD in both figures, which is due to the smoothing effect of the inductive load.

Fig. 2-8 shows the input current waveforms of MMMC-I when the output fundamental frequency is 40 Hz. The currents at the input port of the MC module are composed of chopped pulses from the load currents. Due to the presence of filtering capacitance and line inductance, the secondary winding currents i_{1a}, i_{2a}, and i_{3a} become continuous waveforms, despite the fact that they do not have a very sinusoidal shape. However when it comes to the primary winding, the three secondary currents, after being referred to the primary side, add up to the total input line current i_a, which can be seen from the figure as a sinusoid with a THD of 7.27%.

2.3.2 Simulation Results for MMMC-II

With switching periods for modules in series evenly displaced, Fig. 2-9 and Fig. 2-10 present a set of typical output voltage and current waveforms of MMMC-II at fundamental frequencies of 40 Hz and 80 Hz, respectively. As mentioned earlier, a total of three MMMC-I modulators are required for modulating the MMMC-II. Each modulator should have an input displacement angle θ_i that matches the phase shift of the supplying secondary winding of the transformer. Due to the cascaded structure and the displaced switching period arrangement, output phase-to-neutral (v_{AN}) and line-to-line (v_{AB}) voltages of MMMC-II possess multilevel waveform shapes and are associated with significantly reduced THD and dv/dt comparing to their counterparts of MMMC-I in Fig. 2-6 and Fig. 2-7. Accordingly, the quality of the load current waveforms is also improved.

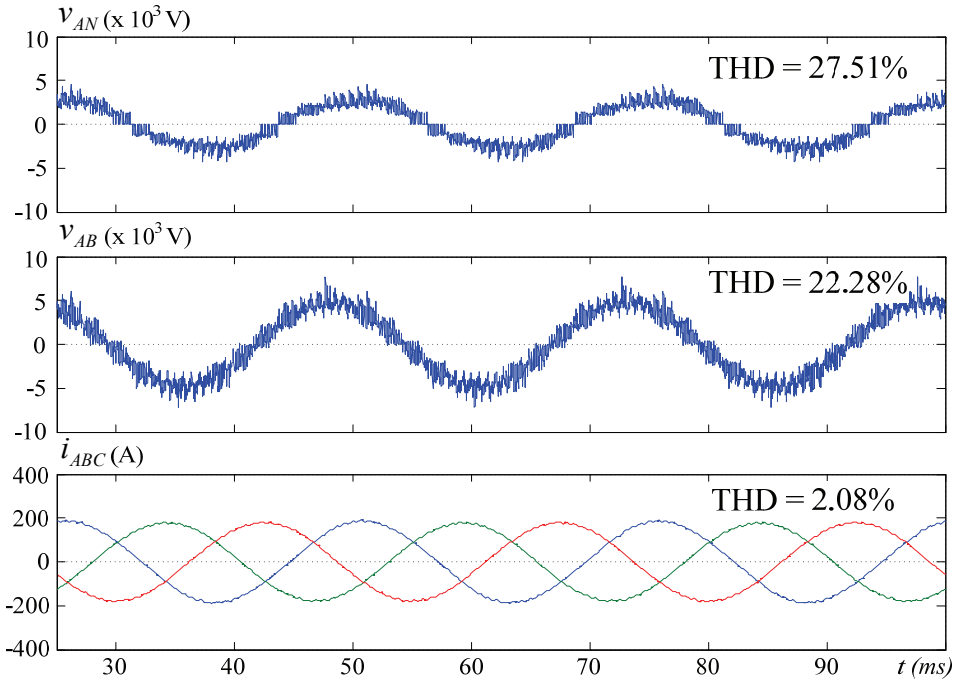


Fig. 2-9 Simulated output voltage and current waveforms of MMMC-II (f_o = 40 Hz, m_a = 0.9).

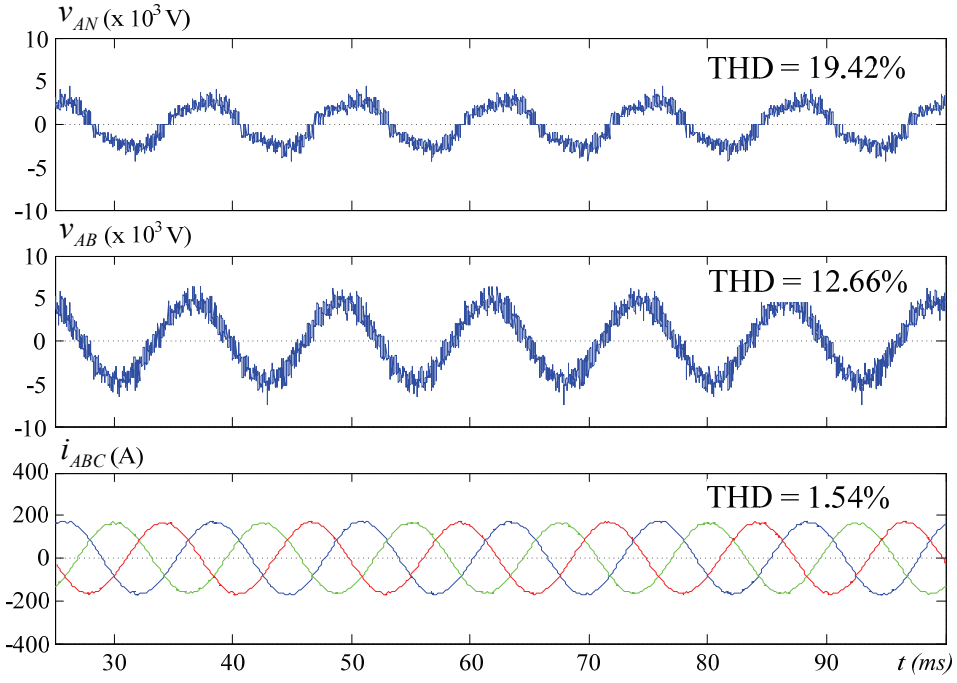


Fig. 2-10 Simulated output voltage and current waveforms of MMMC-II (f_o = 80 Hz, m_a = 0.9).

Fig. 2-11 illustrates the input current waveforms of MMMC-II. In this figure, the current waveforms at the input port of the MC module and in the secondary winding of the transformer have similar shapes to those in Fig. 2-8. On the primary side, the current components coming from the secondary windings that have the same phase shift, e.g. +20º, add up and form a sinusoidal waveform of i_{a_20}. It is then further combined with currents from the other secondary winding groups to build the total input current, i_a, whose THD is as low as 2.65% thanks to the harmonic elimination capability of the phase-shifting transformer.

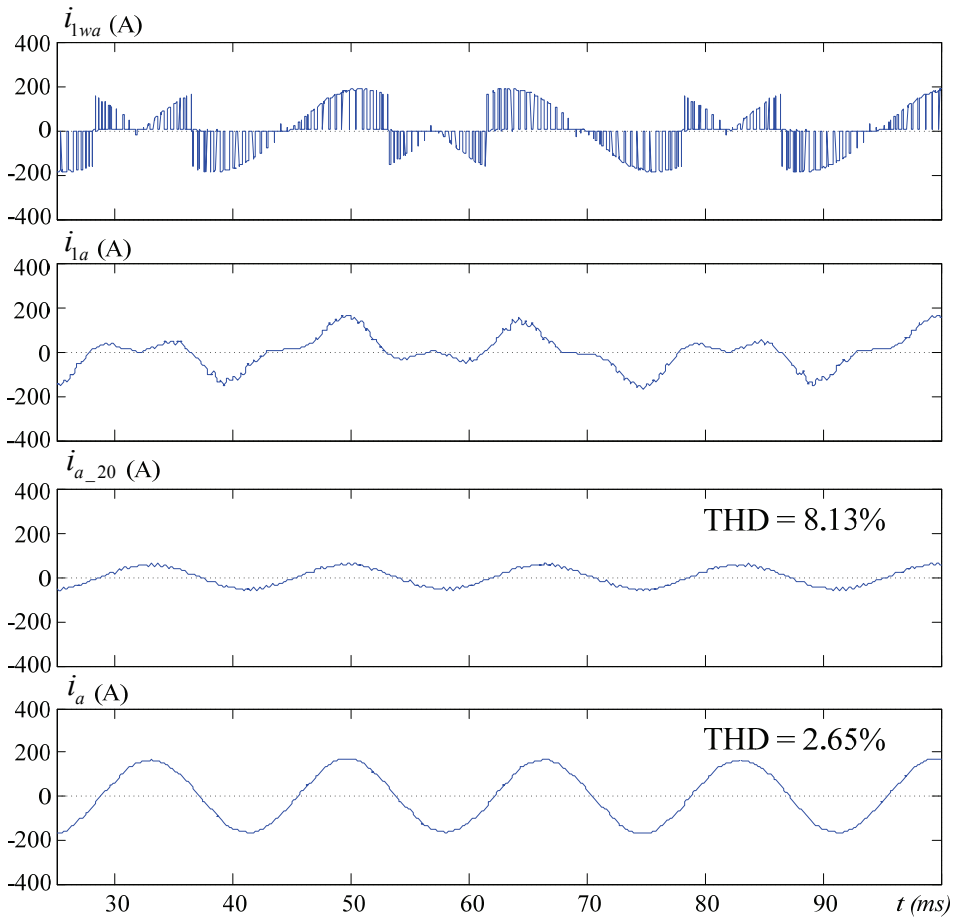


Fig. 2-11 Simulated input current waveforms of MMMC-II
(f_o = 40 Hz, m_a = 0.9).

Fig. 2-12 shows the adjustable input power factor of MMMC-II by varying the input displacement angle θ_i in the modulation program. The input power factor of the converter can be freely adjusted to be unity, leading, or lagging. It should be noted that being a part of the nature of a direct frequency converter, a phase shift in θ_i is a compromise on the voltage gain and will reduce the maximum obtainable output voltage magnitude. This can be clearly seen from the equation of (2.11).

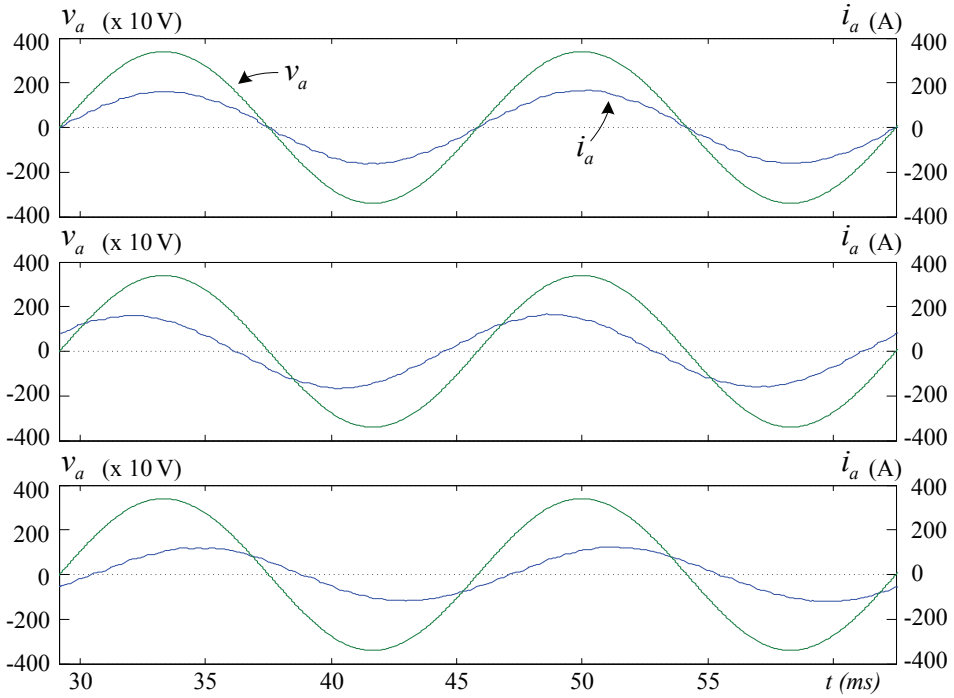


Fig. 2-12 Adjustable input power factor of MMMC-II
(f_o = 40 Hz, m_a = 0.9).

2.4 Experimental Verification

In addition to simulation results, a scaled-down low-voltage experimental prototype consisting of nine 3 x 2 MC modules has been built to verify the modulation concepts. Each

MC module is equipped with the necessary bidirectional switches, isolated gate drivers, as well as sensor circuits for voltage and current measurement. Field programmable gate arrays (FPGAs) are used to realize the modulation function, dispatch gating signals, and handle device commutations. Details about the experimental setup implementation are provided in Chapter 5.

Both MMMC-I and MMMC-II are tested on the platform supplied by 208 Vrms / 60 Hz grid voltage. Detailed experimental system parameters are listed in Table 2-2. The per-unit values of the passive components under a 5 kW rated power are similar to those provided for the simulations. The phase-shifting transformers used in the experiments have a fixed turns ratio of 2 : 1, therefore, a variac is inserted between the grid and the transformers to adjust the primary to secondary voltage gain.

Table 2-2 Experimental system parameters for direct modulation scheme

System Parameters	Value
Grid Input Voltage (line-to-line, rms)	208 V
Input Frequency	60 Hz
Equivalent Transformer Turns Ratio $N_P : N_S$	2 : 1 (MMMC-I) 9 : 2 (MMMC-II)
Sampling Frequency f_s	1.8 kHz
Device Switching Frequency f_{sw}	≈ 1.2 kHz
Equivalent Total Line Inductance L_s	≈ 2 mH (≈ 0.087 pu)
Filter Capacitance C_f	66 μF (0.21 pu)
Load Resistance R_L	7.9 Ω (0.91 pu)
Load Inductance L_L	5 mH (0.22 pu)

The experimental waveforms for MMMC-I and MMMC-II acquired from the lab prototype are shown in the following figures.

Fig. 2-13 and Fig. 2-14 provide MMMC-I output waveforms at 40 Hz and 80 Hz fundamental frequencies, respectively. The output voltages are fabricated by pieces from the input voltages and match well with their simulation counterparts. The output current is smoothed by the inductive load and appears to be continuous. In Fig. 2-15, the input voltage and current waveforms of phase *a* are presented. The converter is working at the unity power factor condition as the input voltage and current are in phase. The grid current has visible distortions due to reasons such as polluted grid voltage and LC resonance.

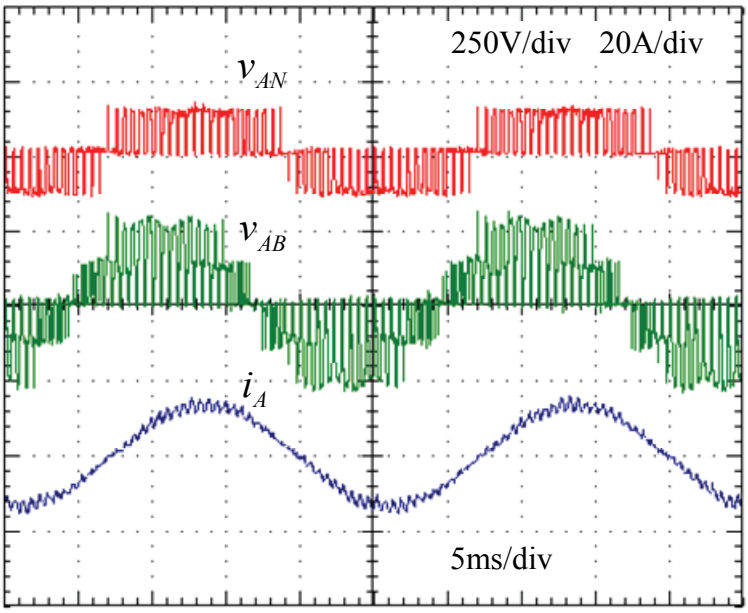


Fig. 2-13 Experimental output voltage and current waveforms of MMMC-I (f_o = 40 Hz, m_a = 0.9).

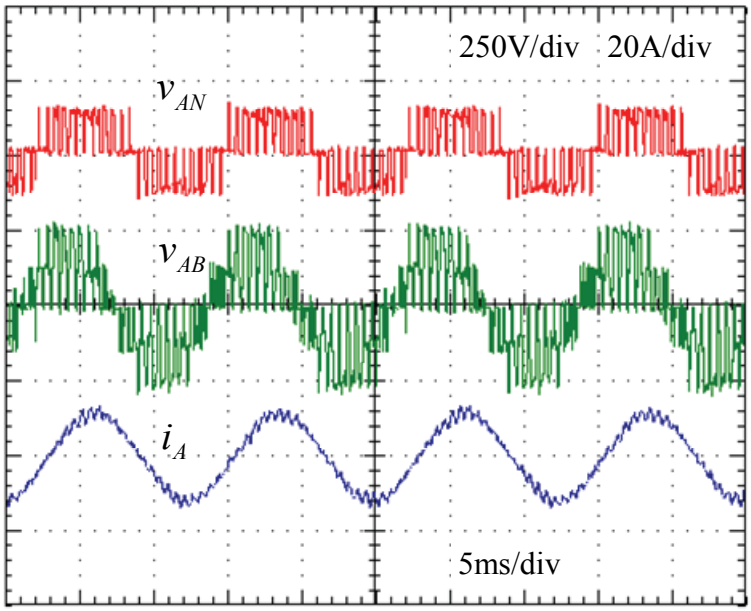


Fig. 2-14 Experimental output voltage and current waveforms of MMMC-I (f_o = 80 Hz, m_a = 0.9).

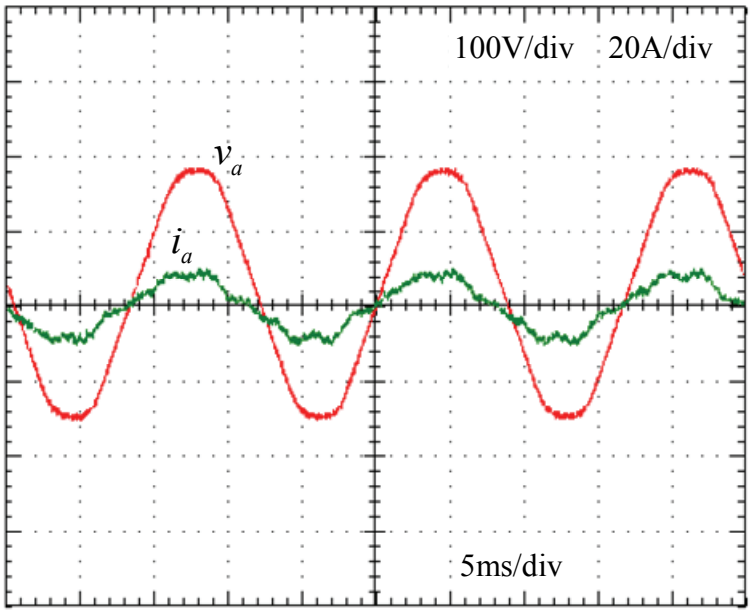


Fig. 2-15 Experimental grid voltage and current waveforms of MMMC-I (f_o = 40 Hz, m_a = 0.9).

Fig. 2-16 and Fig. 2-17 illustrate the experimental output waveforms of MMMC-II, with the fundamental frequency lower (40 Hz) and higher (80 Hz) than that of the input (60 Hz). Similar to simulation results, the experimental output voltage waveforms of MMMC-II have multilevel waveform shapes and are better in quality than those produced by MMMC-I. The output current waveforms are also improved as a consequence.

Fig. 2-18 shows the input-side waveforms of MMMC-II while the output frequency is 40 Hz. Compared to the relatively distorted input current of MMMC-I as shown in Fig. 2-15, the input current waveforms of MMMC-II appear as good sinusoids which can be adjusted by the input displacement angle to be leading, lagging, or in-phase with the grid voltage. The better current waveform of MMMC-II is due to the phase-shifting transformer's harmonic elimination capability which helps improve the input current quality.

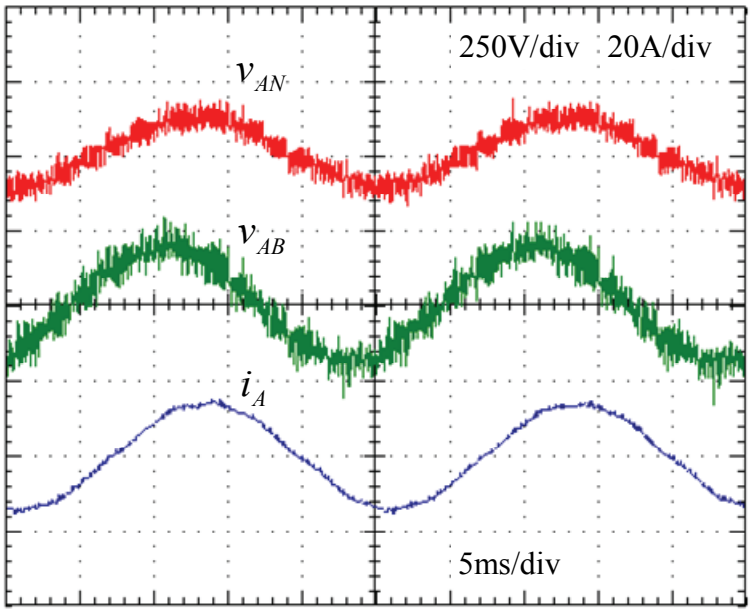


Fig. 2-16 Experimental output voltage and current waveforms of MMMC-II (f_o = 40 Hz, m_a = 0.9).

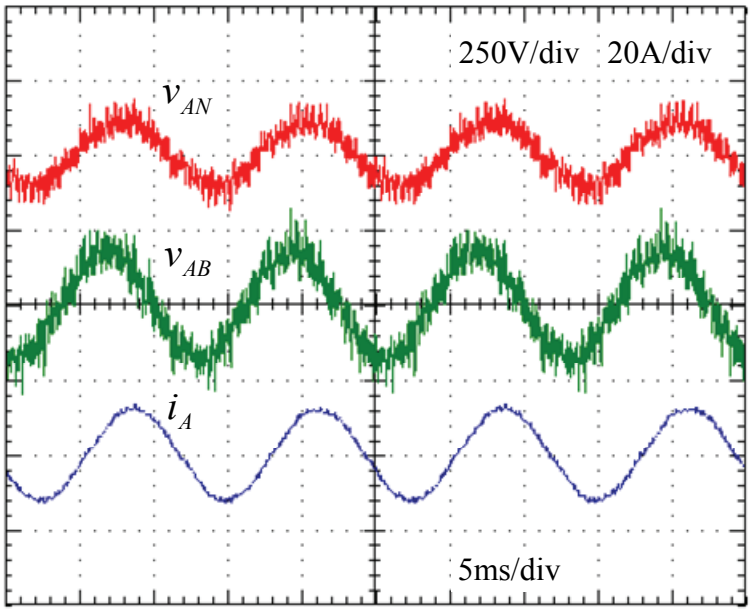


Fig. 2-17 Experimental output voltage and current waveforms of MMMC-II (f_o = 80 Hz, m_a = 0.9).

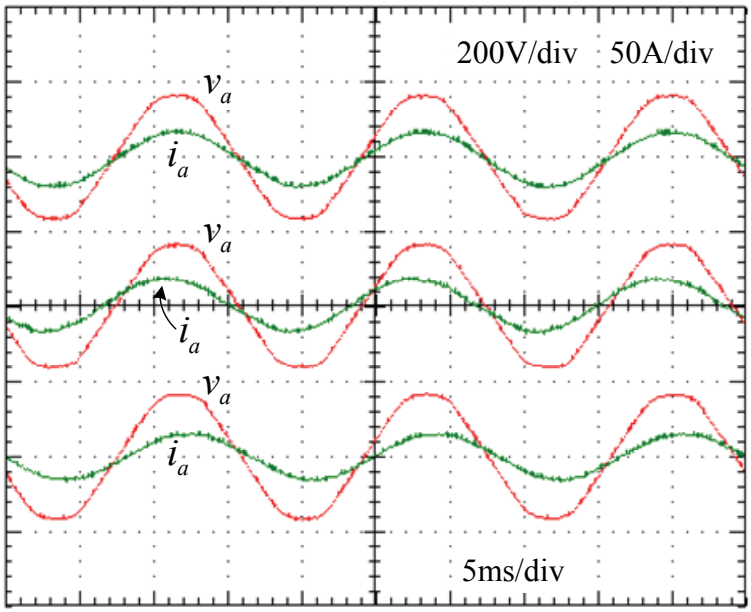


Fig. 2-18 Experimental grid voltage and current waveforms of MMMC-II (f_o = 40 Hz, m_a = 0.9).

2.5 Summary

In this chapter, studies on two MMMC topologies composed of multiple 3 x 2 MC modules are carried out. The MMMC topologies combine benefits of both multilevel and direct frequency conversion concepts. Similar to the multilevel voltage-source converters, the MMMCs allow the use of low-voltage power semiconductors in the power modules and are able to yield high-quality multi-stepped output waveforms. Moreover, they also possess features as MCs such as elimination of dc components, four-quadrant operation capability, fast dynamic response, sinusoidal input/output quantities, and adjustable input power factor. A direct modulation scheme based on input-output transfer matrix derivation is proposed to control the MMMCs for obtaining sinusoidal voltage/current waveforms on both sides of the converters. The output pulses are generated by the modulation program according to a center-placed double-sided switching pattern. In addition to simulated results, experimental verification has proved that, by targeting the primary side input current synthesis rather than the secondary side, the modulation scheme is able to generate sinusoidal output voltage and input current waveforms simultaneously, with the amplitude, frequency, and power factor all adjustable. For MMMC-II, owing to the cascaded structure and switching period displacements, multilevel output waveforms with superior quality can be readily achieved. It should be mentioned that the input phase-shifting transformer plays an important role in the MMMC-II system, helping improve the input current quality with its harmonic elimination capability.

Chapter 3

Indirect Space Vector Based Modulation Scheme for the MMMCs

In the previous chapter, a direct modulation scheme for the multimodular matrix converters (MMMCs) has been developed. By taking modules from all three phases as an integral for transfer matrix derivation and applying coordinated control, the direct modulation scheme is able to make the converters produce sinusoidal waveforms on both sides. Taking a different approach, this chapter is dedicated to the design of indirect space vector based modulation techniques for the MMMCs. It will be explained that although composed of 3 x 2 MC modules, the MMMCs can still adopt the classic rectifier – fictitious dc-link – inverter concept and be modeled indirectly if viewed from a certain perspective. Consequently, indirect space vector modulation (SVM) techniques can be developed based on the established circuit model. In the proposed methods, a current-source rectifier (CSR) SVM is employed to calculate duty ratios and determine switching states for the rectifier stage; while for the inverter stage, output voltage synthesis from either a two-level voltage-source inverter (VSI) SVM or a three-level VSI SVM is feasible. The duty ratios and switching states are then converted and combined to be mapped to the real switching devices. Finally, the gate signals are generated according to two output switching patterns, one being the same center-placed double-sided pattern as used for the direct modulation scheme, whereas the other has a different arrangement for negative half-cycle pulses. The second pattern produces voltage waveforms with significantly improved harmonic

performance. Its superiority over the conventional pattern will be explained and demonstrated with simulation and experimental examples.

3.1 Indirect Modeling for the MMMCs

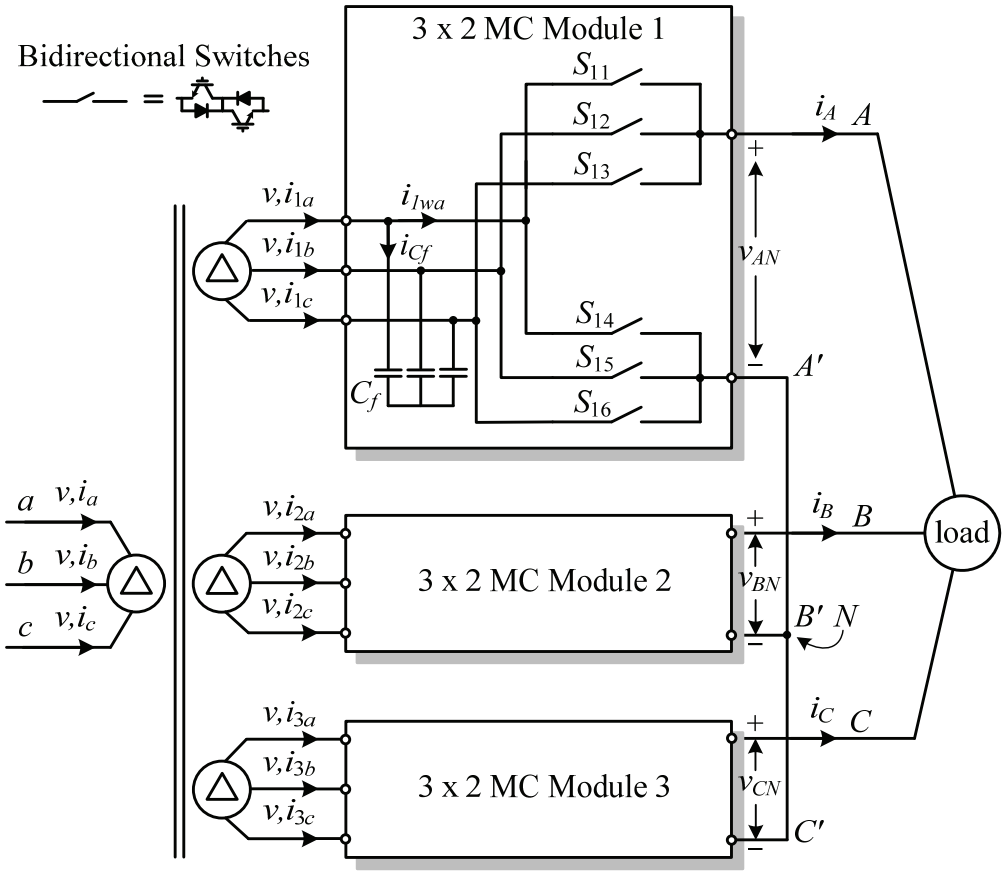


Fig. 3-1 Simplified diagram of three-module MMMC-I.

A simplified diagram of the three-module MMMC-I is redrawn in Fig. 3-1 for the explanation of the indirect circuit modeling. As mentioned earlier, the converter is composed of a four-winding input transformer, three 3 x 2 MC modules, and supplies a

three-phase inductive load. The switching states in the MC modules have to comply with a switching constraint. Taking the first module as an example, only two switches (one from S_{11}, S_{12} and S_{13} and the other from S_{14}, S_{15} and S_{16}) should be ON at any instant of time to avoid detrimental short circuit of the filter capacitors and current interrupt in the inductive load.

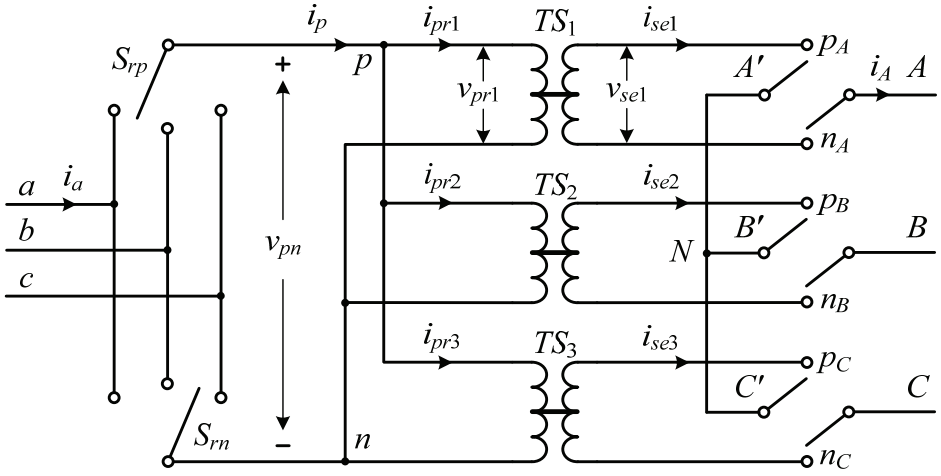


Fig. 3-2 Indirect model for MMMC-I using the fictitious dc concept.

For conventional 3 x 3 MCs, modulation schemes based on both direct and indirect models are well studied in the literature [15, 50, 53]. While the direct model takes the converter as a whole for the derivation of system transfer function matrix, the indirect model separates the MC into a rectifier stage and an inverter stage which are coupled to each other through an imaginary dc-link without real components. Accordingly, the transfer function for the entire system can be obtained as the product of the individual transfer functions of the rectifier and the inverter. As for the three-module MMMC-I, the same indirect modeling concept can be applied to all the power modules such that they can be regarded as a fictitious three-phase rectifier coupling with a fictitious single-phase inverter.

Then, if we consider the transformer as merely an isolation stage with a gain determined by its turns ratio, and assume the rectifier stages of all three modules are operated synchronously by the same gate signals (i.e. the same input line-to-line voltage is impressed onto the fictitious dc stages of these modules at any time), an equivalent indirect circuit model for MMMC-I can be derived in Fig. 3-2. The model is composed of a common rectifier part, a dc-link isolation stage represented by three "dc transformers [58]" (TS_1, TS_2, TS_3), and an inverter part consisting of two sets of three-phase output ports (A-B-C and A'-B'-C'). The rectifier stage of the model is identical to that of the conventional 3 x 3 MC's. As the switches are controlled by the modulation program to synthesize sinusoidal input currents, line-to-line voltages from the three-phase ac source are impressed on the dc-link. The dc-link voltage would then be transferred to the secondary side of the transformers and utilized by the inverter to fabricate output voltages. It should be noted that the three dc transformers have the same turns ratio (N_s / N_p), and their voltage/current characteristics are no different from those of an ideal ac transformer. Therefore, the load currents in their secondary windings are also transformed to the primary side, summed and then utilized by the rectifier modulation program as the dc current source for input current synthesis.

In the original MMMC-I as shown in Fig. 3-1, the voltage/current relationship between the input and output ports can be expressed as follows (taking input port a and output port AA' as an example and neglecting the current on the filter capacitor)

$$v_{AA'} = \frac{N_S}{N_P}[v_{ab}(S_{11} \cdot S_{15} - S_{14} \cdot S_{12}) + v_{bc}(S_{12} \cdot S_{16} - S_{15} \cdot S_{13}) + v_{ca}(S_{13} \cdot S_{14} - S_{16} \cdot S_{11})] \tag{3.1}$$

$$i_a = \frac{N_S}{N_P}[i_A(S_{11} - S_{14}) + i_B(S_{21} - S_{24}) + i_C(S_{31} - S_{34})] \tag{3.2}$$

where S_{jk} denotes the state of a bidirectional switch (0-OFF, 1-ON), subscript j indicates the module number, and k indicates the switch number; N_s / N_p represents the secondary-to-primary turns ratio of the input transformer. Taking account of the switching constraint mentioned earlier, $v_{AA'}$ consists only of scaled input line-to-line voltage pieces and zero.

In the indirect model of MMMC-I (redrawn in Fig. 3-3 with single-pole single-throw switches), the voltage/current relationship of the input/output ports can be derived as follows (again taking input port a and output port AA' as an example):

$$\begin{aligned} v_{AA'} = \frac{N_S}{N_P}(S_{Ap} - S_{A'p})[&v_{ab}(S_{ap}\cdot S_{bn} - S_{an}\cdot S_{bp}) \\ &+ v_{bc}(S_{bp}\cdot S_{cn} - S_{bn}\cdot S_{cp}) + v_{ca}(S_{cp}\cdot S_{an} - S_{cn}\cdot S_{ap})] \end{aligned} \tag{3.3}$$

$$\begin{aligned} i_a = \frac{N_S}{N_P}(S_{ap} - S_{an})[&i_A(S_{Ap} - S_{A'p}) + i_B(S_{Bp} - S_{B'p}) \\ &+ i_C(S_{Cp} - S_{C'p})]. \end{aligned} \tag{3.4}$$

Note that switching constraints exist for the symbolic switches in the indirect model as well. For the rectifier stage switches, the constraints are the same as those for a CSR; whereas for the inverter stage switches, the constraints are identical to those for a two-level VSI. The two equations of (3.3) and (3.4) serve as the mathematical base for the circuit model in Fig. 3-3; corresponding switching states can always be found making them equivalent to (3.1) and (3.2).

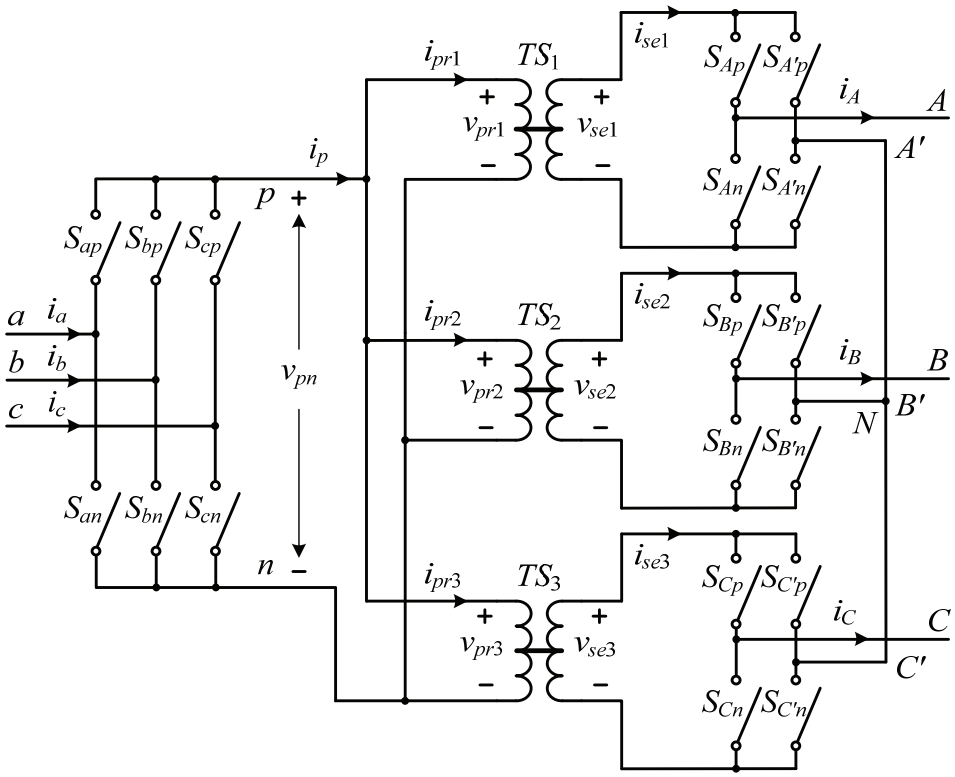


Fig. 3-3 Indirect model for MMMC-I with single-pole single-throw switches.

3.2 CSR SVM for Rectifier Stage Calculations

The indirect circuit model developed for MMMC-I in the last section facilitates the design of suitable indirect space vector modulation (SVM) schemes. Similar to what was used in the conventional 3 x 3 MC, the basic idea of an indirect modulation scheme is to separately apply SVM to the rectifier and inverter stages, before combining their switching states to produce the final gate signals. For the rectifier stage, a traditional SVM for operating current-source rectifiers (CSRs) can be readily employed. Its space vector diagram and synthesis of the current reference vector are shown in Fig. 3-4. With reference to the circuit model in Fig. 3-2, the stationary vectors ($\bar{I}_0 \sim \bar{I}_6$) in Fig. 3-4 correspond to the positions of the rectifier switches S_{rp} and S_{rn}. For instance, $\bar{I}_1(ab)$ indicates that S_{rp} is

connected to input phase a whereas S_{rn} is clamped to phase b, therefore, the primary side dc-link voltage v_{pn} is equal to v_{ab}. The CSR SVM assumes the total dc-link current, i_p, is constant and uses it as a current source for generation of the input currents. At any instant of time, the reference vector is synthesized by two adjacent active vectors and a zero vector. The duty ratios of the constituent vectors can be calculated by

$$\begin{cases} d_u = m_c \sin(\pi/3 - \theta_{sec}) \\ d_v = m_c \sin(\theta_{sec}) \\ d_o = 1 - d_u - d_v \end{cases} \tag{3.5}$$

where m_c represents the rectifier stage modulation index, which is normally set to unity because the input current magnitude actually depends on the load; while θ_{sec} denotes the sector angle of the reference vector $\vec{I}_{ref}$ (the angle between $\vec{I}_{ref}$ and its adjacent active vector on the clockwise side).

It can be noticed that, during any switching period, the two active vectors for synthesizing the reference current vector cause two different line-to-line voltages to be impressed onto the dc-link. In view of the fact that zero vectors have no contribution to the effective dc-link voltage, the local average of the dc-link voltage over a switching period can be expressed in terms of the averaged line-to-line voltages weighted with their respective duty ratios

$$\overline{v}_{pn} = \overline{v}_{ll1} d_u + \overline{v}_{ll2} d_v. \tag{3.6}$$

As an example, suppose $\vec{I}_{ref}$ dwells in Sector I, since the two adjacent active vectors in this case are $\vec{I}_1$ and $\vec{I}_2$, the effective part of the dc-link voltage at the primary side of the transformers would be a combination of segments from v_{ab} and v_{ac}.

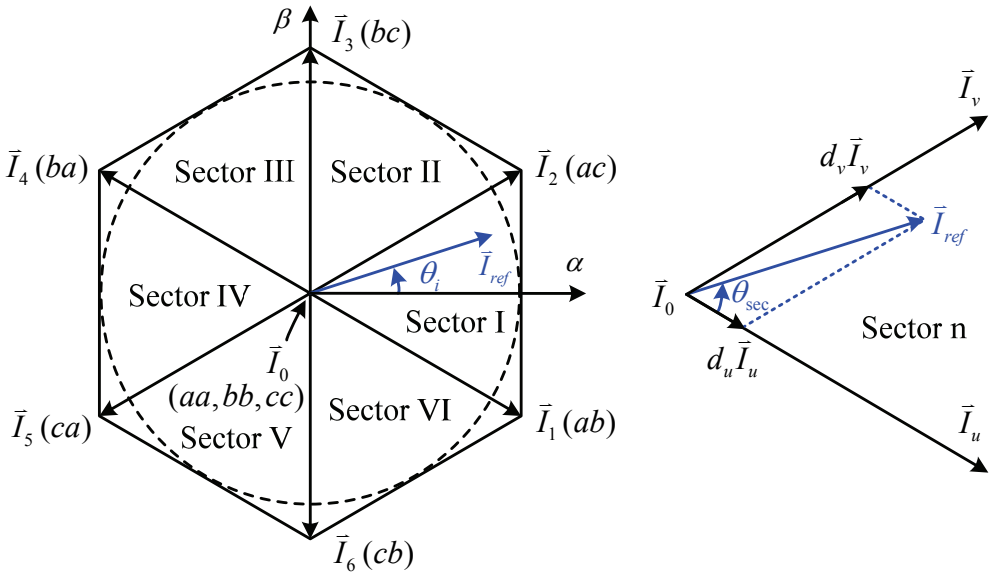


Fig. 3-4 CSR SVM for rectifier stage current synthesis.

3.3 Two-level VSI SVM for Inverter Stage Calculations

3.3.1 Duty Ratio Calculation

Provided the rectifier input voltages are three-phase balanced, the value of $\overline{v}_{pn}$ remains a constant throughout all the sectors [15]. In addition, because the three dc transformers (TS_1, TS_2, TS_3) have the same turns ratio and therefore identical voltage gain, the secondary voltages obtainable at ports (p_A-n_A), (p_B-n_B) and (p_C-n_C) are all equal. These prerequisites establish a basis for the inverter stage to adopt voltage-source inverter (VSI) SVM

techniques which requires an invariable dc source to generate sinusoidal output voltage waveforms. The two-level VSI SVM diagram for the inverter stage is shown in Fig. 3-5. As mentioned earlier, the inverter stage of the model can be regarded as two sets of three-phase outputs. Hence, the reference voltage vector, $\vec{V}_{ref}$, represents the desired three-phase voltages to be synthesized at ports (*A*-*B*-*C*), while $\vec{V}'_{ref}$ represents the voltages at the other three-phase output ports (*A*′-*B*′-*C*′). In the actual converter, since the latter ports are connected to form the reference neutral point *N*, the real output phase voltages v_{AN}, v_{BN}, and v_{CN} can be viewed as a vectorial combination of v_{ABC} and $v_{A'B'C'}$.

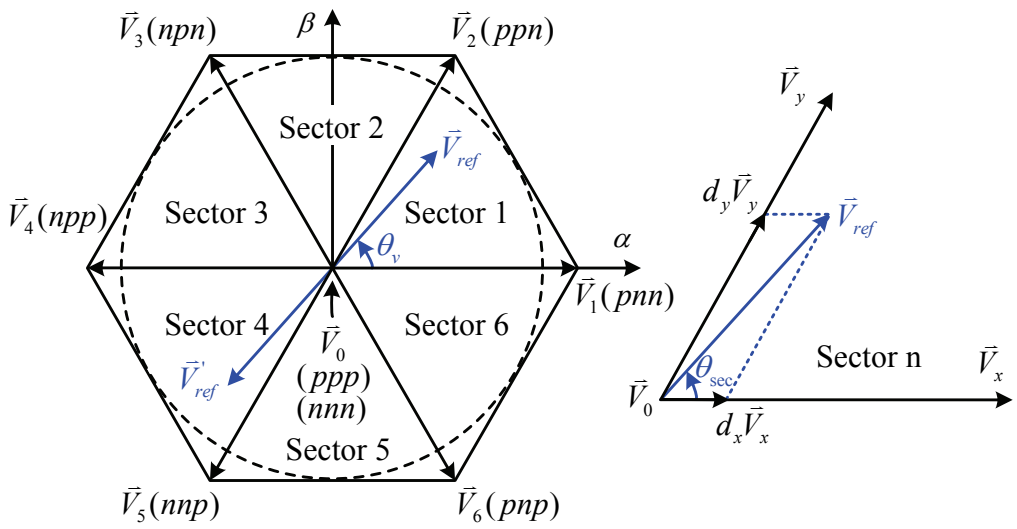


Fig. 3-5 Two-level VSI SVM for inverter stage voltage synthesis.

In Fig. 3-5, the VSI switching states are listed in the parentheses beside their respective stationary vectors ($\vec{V}_0 \sim \vec{V}_6$). Letter *p* or *n* in each switching state indicates whether the corresponding output phase should be clamped to the positive or the negative rail of the dc-

link, respectively. As shown in the figure, it is preferable to set $\vec{V}_{ref}^{'}$ in the opposite direction of $\vec{V}_{ref}$, for this disposition not only allows maximum voltage utilization, but also results in the minimum SVM computation burden. This is because the duty ratios of the active vectors adjacent to $\vec{V}_{ref}^{'}$ are always the same as those of $\vec{V}_{ref}$'s; moreover, the switching states pertaining to their active vectors are always complementary. For example, consider the situation that $\vec{V}_{ref}$ is in Sector 1, the two active vectors for its synthesis are $\vec{V}_1(pnn)$ and $\vec{V}_2(ppn)$ whose duty ratios are d_x and d_y, respectively; in this case, the corresponding active vectors for synthesizing $\vec{V}_{ref}^{'}$ in Sector 4 would be $\vec{V}_4(npp)$ and $\vec{V}_5(nnp)$. Obviously, switching states of these two vectors are the exact inverse to those of $\vec{V}_1$ and $\vec{V}_2$. Additionally, their respective duty ratios are also d_x and d_y. As a result, duty ratio calculation for all the vectors needs to be done only once using the following formulas

$$\begin{cases} d_x = m_v \sin(\pi/3 - \theta_{sec}) \\ d_y = m_v \sin(\theta_{sec}) \\ d_z = 1 - d_x - d_y \end{cases} \tag{3.7}$$

where m_v designates the inverter modulation index which can be used to adjust the output voltage magnitude, and θ_{sec} denotes the sector angle of $\vec{V}_{ref}$.

Assuming the inverter supplies a three-phase balanced inductive load (RL or ac machine), the sinusoidal output voltages generated by SVM result in continuous load currents that are also three-phase balanced. During every switching period, as the inverter dwells in the two switching states pertaining to the active vector pair for reference voltage

synthesis, the corresponding load currents are introduced into the dc-link. Taking again the example of when $\vec{V}_{ref}$ is in Sector 1 ($\vec{V}_{ref}^{'}$ in Sector 4), since the switching states for (*A*-*B*-*C*) and (*A′*-*B′*-*C′*) are (pnn, ppn) and (npp, nnp), the secondary winding currents of the dc transformers (i_{se1}, i_{se2}, i_{se3}) in a single switching period would be a combination of (i_A, -i_B, -i_C) and (i_A, i_B, -i_C). Accordingly, the local average of the total dc-link current at the primary side of the transformers can be expressed as a function of the averaged load currents weighted with their duty ratios

$$\begin{aligned} \overline{i}_p &= \overline{i}_{pr1} + \overline{i}_{pr2} + \overline{i}_{pr3} \\ &= N_s / N_p \cdot \left(\overline{i}_{se1} + \overline{i}_{se2} + \overline{i}_{se3} \right) \\ &= N_s / N_p \cdot (2\overline{i}_A d_x - 2\overline{i}_C d_y) \end{aligned} \tag{3.8}$$

in which N_s / N_p represents the turns ratio of the transformers.

Under balanced load currents condition, the value of $\overline{i}_p$ remains a constant regardless of the position of $\vec{V}_{ref}$. The dc-link current requirement of the rectification stage SVM is therefore satisfied.

3.3.2 Duty Ratio Conversion

In order to facilitate the design of optimized switching sequence, the duty ratios calculated by the two-level VSI SVM are then converted using a per phase approach. The conversion process is detailed in Table 2-1 for all six sectors. Delivered by the conversion are new duty ratios that represent the percentages of a switching period, during which the

Table 3-1 Duty ratio conversion for the inverter stage with the two-level SVM

Sector of $\vec{V}_{ref}$	***A-B-C***	***A′-B′-C′***	***AA′-BB′-CC′***	**Original duty ratio**	**Duty ratio conversion**
1	$\vec{V}_1(pnn)$	$\vec{V}_4(npp)$	*pn-np-np*	d_x	$d_{Ap} = d_x + d_y$; $d_{An} = 0$; $d_{Ao} = 1 - d_{Ap} - d_{An}$; if ($d_x > d_y$) then ($d_{Bp} = 0$; $d_{Bn} = d_x - d_y$) else ($d_{Bp} = d_y - d_x$; $d_{Bn} = 0$); $d_{Bo} = 1 - d_{Bp} - d_{Bn}$; $d_{Cp} = 0$; $d_{Cn} = d_x + d_y$; $d_{Co} = 1 - d_{Cp} - d_{Cn}$;
	$\vec{V}_2(ppn)$	$\vec{V}_5(nnp)$	*pn-pn-np*	d_y	
2	$\vec{V}_2(ppn)$	$\vec{V}_5(nnp)$	*pn-pn-np*	d_x	if ($d_x > d_y$) then ($d_{Ap} = d_x - d_y$; $d_{An} = 0$) else ($d_{Ap} = 0$; $d_{An} = d_y - d_x$); $d_{Ao} = 1 - d_{Ap} - d_{An}$; $d_{Bp} = d_x + d_y$; $d_{Bn} = 0$; $d_{Bo} = 1 - d_{Bp} - d_{Bn}$; $d_{Cp} = 0$; $d_{Cn} = d_x + d_y$; $d_{Co} = 1 - d_{Cp} - d_{Cn}$;
	$\vec{V}_3(npn)$	$\vec{V}_6(pnp)$	*np-pn-np*	d_y	
3	$\vec{V}_3(npn)$	$\vec{V}_6(pnp)$	*np-pn-np*	d_x	$d_{Ap} = 0$; $d_{An} = d_x + d_y$; $d_{Ao} = 1 - d_{Ap} - d_{An}$; $d_{Bp} = d_x + d_y$; $d_{Bn} = 0$; $d_{Bo} = 1 - d_{Bp} - d_{Bn}$; if ($d_x > d_y$) then ($d_{Cp} = 0$; $d_{Cn} = d_x - d_y$) else ($d_{Cp} = d_y - d_x$; $d_{Cn} = 0$); $d_{Co} = 1 - d_{Cp} - d_{Cn}$;
	$\vec{V}_4(npp)$	$\vec{V}_1(pnn)$	*np-pn-pn*	d_y	
4	$\vec{V}_4(npp)$	$\vec{V}_1(pnn)$	*np-pn-pn*	d_x	$d_{Ap} = 0$; $d_{An} = d_x + d_y$; $d_{Ao} = 1 - d_{Ap} - d_{An}$; if ($d_x > d_y$) then ($d_{Bp} = d_x - d_y$; $d_{Bn} = 0$) else ($d_{Bp} = 0$; $d_{Bn} = d_y - d_x$); $d_{Bo} = 1 - d_{Bp} - d_{Bn}$; $d_{Cp} = d_x + d_y$; $d_{Cn} = 0$; $d_{Co} = 1 - d_{Cp} - d_{Cn}$;
	$\vec{V}_5(nnp)$	$\vec{V}_2(ppn)$	*np-np-pn*	d_y	
5	$\vec{V}_5(nnp)$	$\vec{V}_2(ppn)$	*np-np-pn*	d_x	if ($d_x > d_y$) then ($d_{Ap} = 0$; $d_{An} = d_x - d_y$) else ($d_{Ap} = d_y - d_x$; $d_{An} = 0$); $d_{Ao} = 1 - d_{Ap} - d_{An}$; $d_{Bp} = 0$; $d_{Bn} = d_x + d_y$; $d_{Bo} = 1 - d_{Bp} - d_{Bn}$; $d_{Cp} = d_x + d_y$; $d_{Cn} = 0$; $d_{Co} = 1 - d_{Cp} - d_{Cn}$;
	$\vec{V}_6(pnp)$	$\vec{V}_3(npn)$	*pn-np-pn*	d_y	
6	$\vec{V}_6(pnp)$	$\vec{V}_3(npn)$	*pn-np-pn*	d_x	$d_{Ap} = d_x + d_y$; $d_{An} = 0$; $d_{Ao} = 1 - d_{Ap} - d_{An}$; $d_{Bp} = 0$; $d_{Bn} = d_x + d_y$; $d_{Bo} = 1 - d_{Bp} - d_{Bn}$; if ($d_x > d_y$) then ($d_{Cp} = d_x - d_y$; $d_{Cn} = 0$) else ($d_{Cp} = 0$; $d_{Cn} = d_x - d_y$); $d_{Co} = 1 - d_{Cp} - d_{Cn}$;
	$\vec{V}_1(pnn)$	$\vec{V}_4(npp)$	*pn-np-np*	d_y	

output phase voltages ($v_{AA'}$, $v_{BB'}$, $v_{CC'}$) are equal to the positive dc-link voltage, the negative dc-link voltage, or zero. As can be noticed, when $\vec{V}_{ref}$ is in Sector 1, the output state for AA' is pn under both active vector pairs ($\vec{V}_1(pnn) - \vec{V}_4(npp)$, $\vec{V}_2(ppn) - \vec{V}_5(nnp)$), thus, the resultant duty ratio d_{Ap} for AA' being pn is the sum of d_x and d_y, while d_{An} for AA' being np is 0, and d_{Ao} for AA' being pp or nn is $1-d_x-d_y$; As for phase B, due to the fact that d_x and d_y correspond to opposite output states for BB' (np and pn), a judgment on which one has more significance is required to determine the results; For phase C, the calculations are similar to those of phase A because the output state for CC' remains to be np under both active vector pairs.

3.4 Three-level VSI SVM for Inverter Stage Calculations

3.4.1 Duty Ratio Calculation

In the last section, the inverter stage of the MMMC-I indirect model is regarded as a pair of three-phase output sets, and accordingly, the desired output voltage for driving the load can be synthesized from the combination of two opposite voltage reference vectors rotating in the two-level space vector diagram. Nonetheless, if viewing from another standpoint, it is also possible to consider the inverter stage of the model as three output port pairs (AA', BB', CC'), and the voltage obtainable at each port pair can be freely selected from three possible values which correspond to different switching states. Taking AA' as an example, the voltage $v_{AA'}$ supplied by the first dc transformer may arbitrarily adopt a value of $+v_{se1}$, $-v_{se1}$, or 0. Furthermore, because the rectifier stage is commonly shared and the transformers are identical, the voltages at the secondary side of the transformers are all the same and equal to

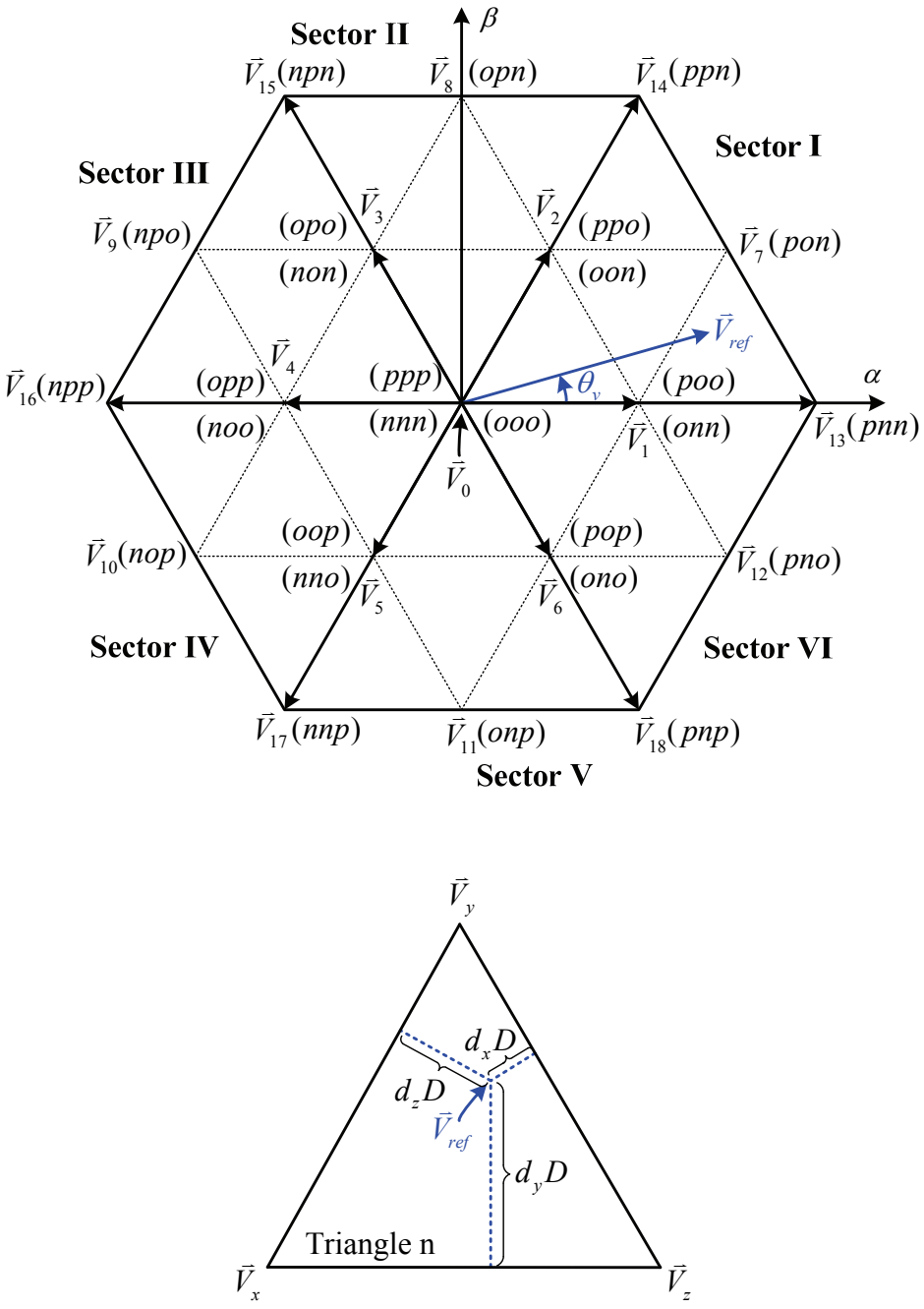


Fig. 3-6 Three-level VSI SVM for inverter stage voltage synthesis.

$$v_{se1} = v_{se2} = v_{se3} = N_s / N_p \cdot v_{pn} \tag{3.9}$$

where N_s / N_p represents the secondary-to-primary turns ratio of the transformers. If we take all three phases into account, a three-level VSI SVM diagram as shown in Fig. 3-6 can be employed for the derivation of inverter stage duty ratios and switching states, as a viable alternative to the two-level VSI SVM described in the last section.

For the three-level SVM, the reference vector is normally synthesized by the three nearest stationary vectors for better harmonic performance. The equations in [23] for neutral-point-clamped converter modulation can be used to calculate duty ratios of stationary vectors in all the sectors.

Table 3-2 Example of dc-link currents expressed in terms of the load currents

Triangle	**Inverter Vectors**	**Duty Ratio**	**dc-link Current i_p**
$\vec{V}_1 - \vec{V}_7 - \vec{V}_{13}$	$\vec{V}_1(poo, onn)$	$2 - 2m_v \sin(\frac{\pi}{3} + \theta_v)$	$N_s / N_p \cdot i_A$
	$\vec{V}_7(pon)$	$2m_v \sin\theta_v$	$N_s / N_p \cdot (i_A - i_C)$
	$\vec{V}_{13}(pnn)$	$2m_v \sin(\frac{\pi}{3} - \theta_v) - 1$	$N_s / N_p \cdot 2i_A$

In the indirect model of MMMC-I, the rectifier and inverter stages are coupled to each other through the ideal transformers, so the load currents introduced into the dc-link by the

inverter stage SVM are directly utilized by the rectifier stage modulation program for synthesis of input currents. It is always required that the local average of the dc-link current be a constant when the output voltage reference vector rotates in the space vector plane.

As shown in Fig. 3-6, assume at a certain time the output voltage reference vector ($\vec{V}_{ref}$) stays in the triangle surrounded by $\vec{V}_1$, $\vec{V}_7$ and $\vec{V}_{13}$, the dc-link currents corresponding to these three vectors are expressed in terms of the load currents in Table 3-2. During an entire switching period, as the inverter dwells at the three vectors to synthesize $\vec{V}_{ref}$, the average dc-link current can be derived as follows

$$\begin{aligned}\overline{i_p} &= [2-2m_v \sin(\frac{\pi}{3}+\theta_v)]\cdot(N_s/N_p\cdot\overline{i_A}) \\ &+[2m_v \sin\theta_v]\cdot[N_s/N_p\cdot(\overline{i_A}-\overline{i_C})] \\ &+[2m_v \sin(\frac{\pi}{3}-\theta_v)-1]\cdot(N_s/N_p\cdot 2\overline{i_A}).\end{aligned} \tag{3.10}$$

Assume the load is three-phase balanced, the load currents can be written as

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \frac{\hat{V}_L}{|Z|}\begin{bmatrix} \cos(\theta_v-\theta_L) \\ \cos(\theta_v-\theta_L-2\pi/3) \\ \cos(\theta_v-\theta_L+2\pi/3) \end{bmatrix} \tag{3.11}$$

in which $\hat{V}_L$, $|Z|$, and θ_L designate the magnitude of the output voltage, the impedance of the load, and the load power factor angle, respectively.

Substituting (3.11) into (3.10) and after a series of deductions, we have

$$\overline{i}_p = \frac{N_s}{N_p} \cdot \frac{\hat{V}_L}{|Z|} \cdot m_v \cdot \sqrt{3} \cos\theta_L \tag{3.12}$$

which is a constant value irrespective of any changing variables. The deductions can be applied to all the other triangles and the same result of (3.12) holds true. Therefore, the local average of the dc-link current is proved to be a constant throughout all the sectors and can be utilized by the rectifier SVM for the synthesis of input currents.

3.4.2 Duty Ratio Conversion

Similar to the two-level inverter stage modulation, to facilitate the design of optimized switching sequence, the duty ratios of the vectors calculated by the three-level VSI SVM are then converted using a per phase approach as well. The conversion procedure is exemplified in Table 3-3 for the triangle $\vec{V}_1 - \vec{V}_7 - \vec{V}_{13}$. Delivered by the conversion are new duty ratios that represent the percentages of a switching period during which the output phase voltages ($v_{AA'}$, $v_{BB'}$, $v_{CC'}$) are equal to the positive dc-link voltage, the negative dc-link voltage, or zero. The original vectors, their switching states, as well as the corresponding duty ratios are all listed in the table. For small vectors that have redundant switching states, the duty ratio is distributed evenly between the two states. For example, since the small vector $\vec{V}_1(poo, onn)$ has a duty ratio of d_1, both of its two switching states (*poo* and *onn*) would have a share of $d_1/2$. Hence, as $\vec{V}_{ref}$ is synthesized by $\vec{V}_1$, $\vec{V}_7$ and $\vec{V}_{13}$, the output state of AA' is *p* for $d_7(\vec{V}_7)$, $d_{13}(\vec{V}_{13})$, and a half of d_1 ($\vec{V}_1(poo)$); the resultant duty ratio d_{Ap} for

AA' being p is therefore $d_1/2 + d_7 + d_{13}$, whereas d_{An} for AA' being n is 0, and d_{Ao} for AA' being *zero* is 1 - d_{Ap} - d_{An}. Similar calculations can be applied to phases *B* and *C*.

Table 3-3 Example of duty ratio conversion for the inverter stage with the three-level SVM

Triangle	Inverter Vectors	Original Duty Ratio	Duty Ratio Conversion
$\vec{V}_1 - \vec{V}_7 - \vec{V}_{13}$	$\vec{V}_1(poo, onn)$	d_1	$d_{Ap} = d_1/2 + d_7 + d_{13}$; $d_{An} = 0$; $d_{Ao} = 1 - d_{Ap} - d_{An}$; $d_{Bp} = 0$; $d_{Bn} = d_1/2 + d_{13}$; $d_{Bo} = 1 - d_{Bp} - d_{Bn}$; $d_{Cp} = 0$; $d_{Cn} = d_1/2 + d_7 + d_{13}$; $d_{Co} = 1 - d_{Cp} - d_{Cn}$;
	$\vec{V}_7(pon)$	d_7	
	$\vec{V}_{13}(pnn)$	d_{13}	

3.5 Switching State Combination

After all the switching states and duty ratios for both stages of the indirect model are determined, the next step is to combine them and generate final gate signals for the actual devices. To make possible the combination it is required that the switching periods of both stages are equal and synchronized. Since the per phase forms of the output stage duty ratios have been derived in the last subsections, it is now convenient to explain the process using the example of the first MC module in Fig. 3-1. Assume the input current reference vector stays in Sector I in a certain switching period T_s, the rectifier stage is therefore supposed to dwell at $\vec{I}_1(ab)$ for a duty ratio of d_u and at $\vec{I}_2(ac)$ for a duty ratio of d_v. If in the meantime, the desired output voltage at port AA' is positive, duty ratio d_{Ap} which represents the percentage of AA' being *pn* has a positive finite value whereas d_{An} would be zero. Taking account of both stages then leads to the final distribution of the switching period: AA' should be connected to *(ab)* for an interval of $d_u d_{Ap} T_s$ and be connected to *(ac)* for another

interval of $d_v d_{Ap} T_s$; throughout the rest of the switching period, AA' will adopt the state *pp* and output a zero voltage, which implies both A and A' are connected to input phase a, a choice that results in the minimum number of switchings.

Table 3-4 Switching state combination for 3 x 2 MC Module 1

Rectifier State	Inverter State (AA')	Devices ON
ab	*pn*	S_{11}, S_{15}
	np	S_{12}, S_{14}
	pp / nn	S_{11}, S_{14} / S_{12}, S_{15}
ac	*pn*	S_{11}, S_{16}
	np	S_{13}, S_{14}
	pp / nn	S_{11}, S_{14} / S_{13}, S_{16}
bc	*pn*	S_{12}, S_{16}
	np	S_{13}, S_{15}
	pp / nn	S_{12}, S_{15} / S_{13}, S_{16}
ba	*pn*	S_{12}, S_{14}
	np	S_{11}, S_{15}
	pp / nn	S_{12}, S_{15} / S_{11}, S_{14}
ca	*pn*	S_{13}, S_{14}
	np	S_{11}, S_{16}
	pp / nn	S_{13}, S_{16} / S_{11}, S_{14}
cb	*pn*	S_{13}, S_{15}
	np	S_{12}, S_{16}
	pp / nn	S_{13}, S_{16} / S_{12}, S_{15}

Table 3-4 lists all the possible switching state combinations for MC module 1. The corresponding real devices that should be turned ON are also provided. From the table it can be seen that if the rectifier stage stays at *(ab)* while AA' is outputting a positive voltage,

the devices that should be ON are S_{11} and S_{15}. For modules 2 and 3, the combination process is similar.

It should be noted that the output state designations listed in the table are from the two-level SVM method. For the three-level SVM method, the output states of *p*, *o*, and *n* are equivalent to *pn*, *pp/nn*, and *np* from the two-level SVM method, respectively.

3.6 Switching Pattern Design

During a single switching period, the order in which the obtained intervals are put affects the switching frequency and harmonic performance. This necessitates the design of suitable switching patterns to make final the modulation program with optimized results. Fig. 3-7 and Fig. 3-8 illustrate two different switching patterns which are exemplified for output phases *A* and *B*. To distinctly show their difference, it is assumed the desired v_{CN} in this particular switching period is zero, while v_{AN} is positive, and v_{BN} is negative. Under this condition, the duty ratios and thus pulse widths for phases *A* and *B* are exactly the same. In the figure V_{LL1} and V_{LL2} denote the two magnitudes corresponding to the two input line-to-line voltages impressed on the dc-link. With the presumption that the switching frequency is sufficiently higher than the output fundamental frequency, they are considered as constants during the entire switching period. The duty ratios d_0, d_1, and d_2 represent the final values derived from the earlier described switching state combination process. In the case being shown, d_2 is greater than d_1.

The first switching pattern is actually the same as the one used for the direct modulation scheme in Chapter 2. And as can be noticed from the figures, both switching pattern I and II provide the same output in phase *A* whose voltage polarity is positive. The main distinction lies in phase *B* where the negative voltage output is differently arranged. In Fig.

3-7, the shape of v_{BN} appears to be a mirrored image to v_{AN} with respect to the horizontal axis, causing the line-to-line voltage v_{AB} to have the same double-sided center-placed pattern. However in Fig. 3-8, the pulses in phase *B* are equally split and placed at both sides of the switching period. With this arrangement, the effective part of v_{AB} is more evenly distributed and associated with lower voltage step jumps. It will be demonstrated that the second pattern brings better harmonic performance in the generated waveforms.

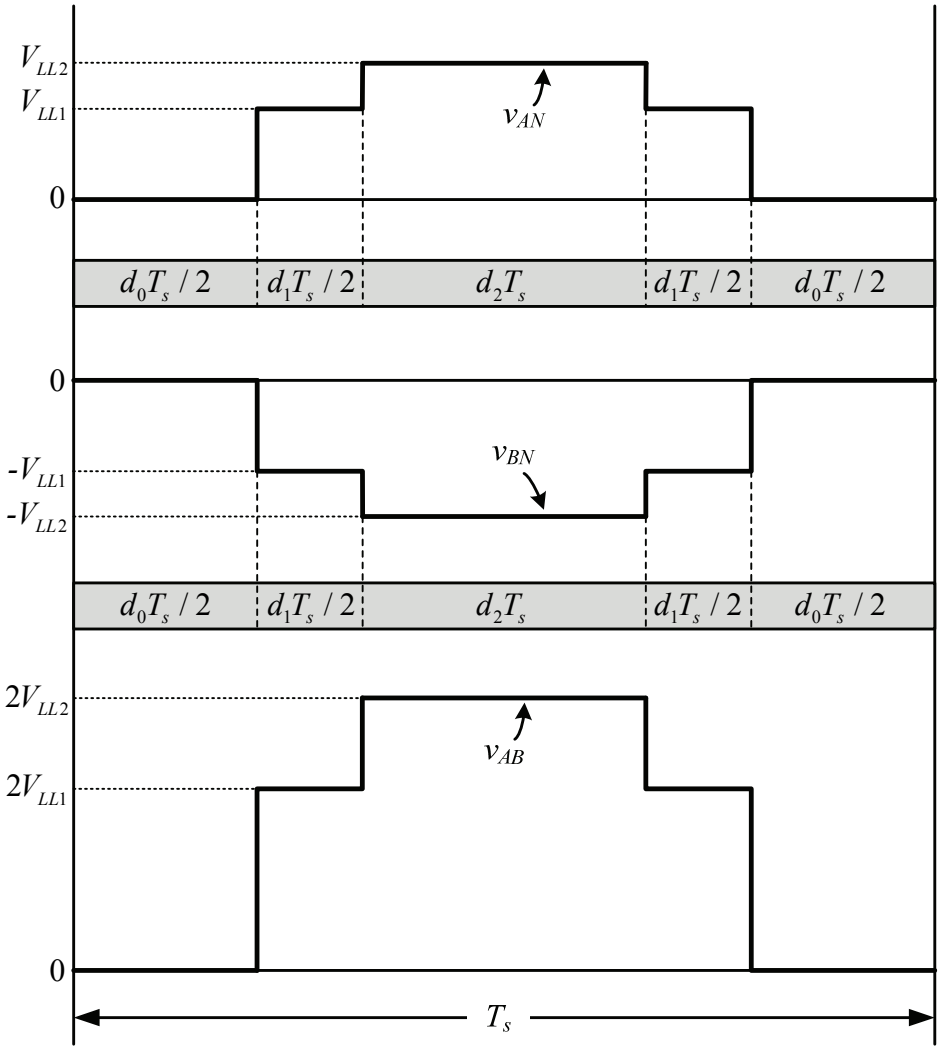


Fig. 3-7 Output switching pattern I

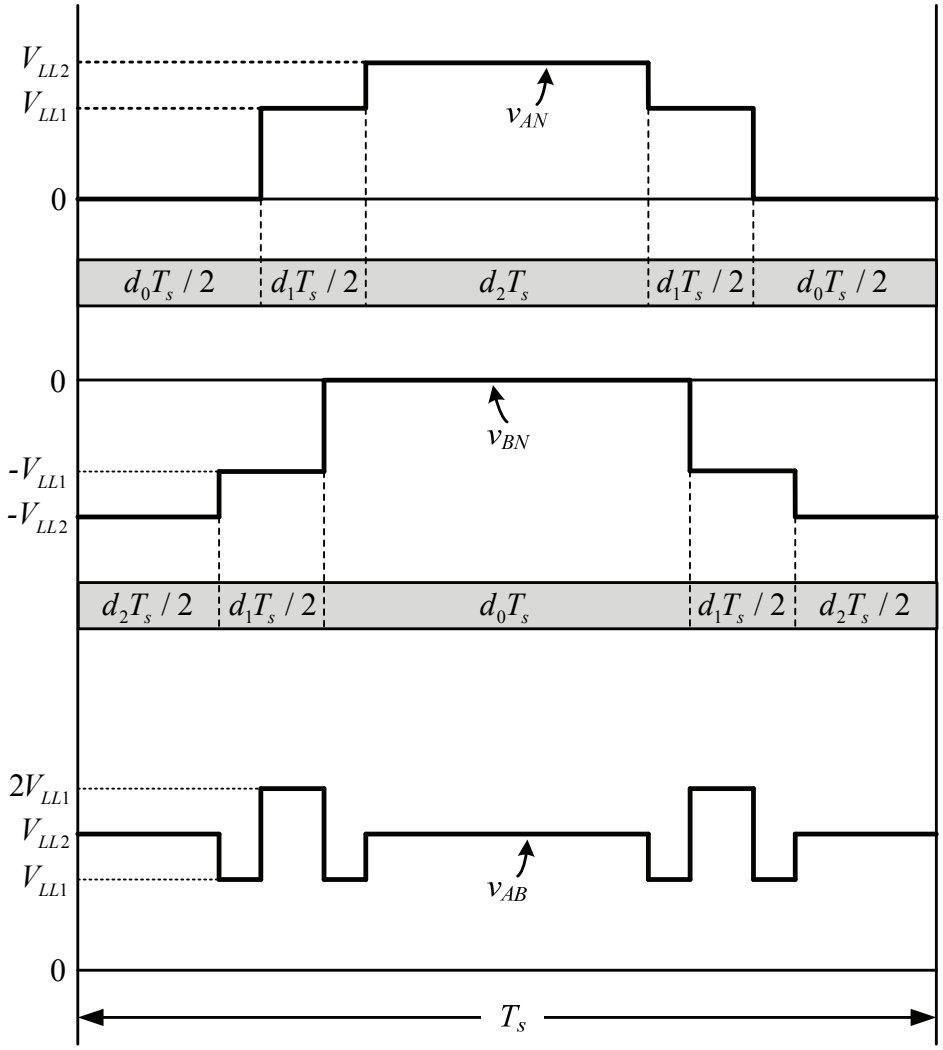


Fig. 3-8 Output switching pattern II.

3.7 Simulation Results

To verify the presented indirect modulation schemes, converter models and simulation programs are implemented and tested in MATLAB/Simulink. In the created models, the converters are used to supply a three-phase RL load. System parameters for the simulations are the same as those listed in Table 2-1. A functional diagram illustrating the software

implementation of the modulation scheme is given in Fig. 3-9. During the simulation, the modulation program accepts modulation index and angle settings and outputs the final gate signals. Under a sampling frequency of 1.8 kHz, the actual device switching frequency is around 1.2 kHz under both switching patterns.

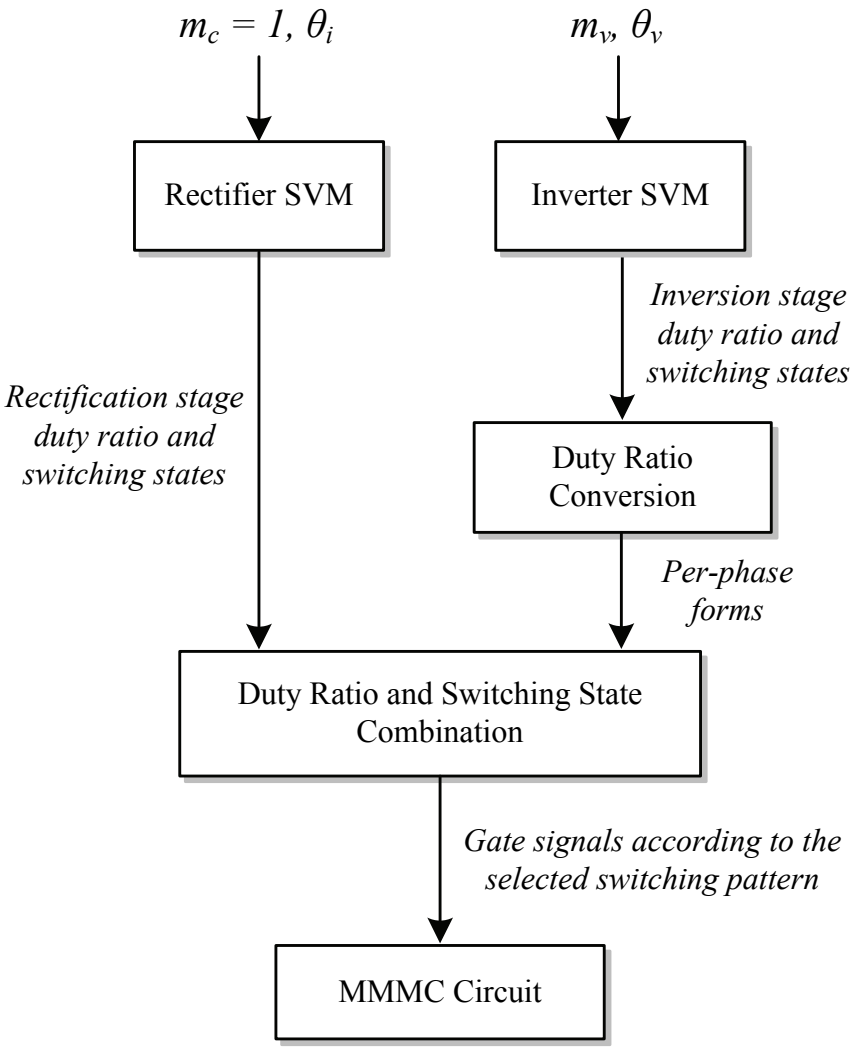


Fig. 3-9 Functional block diagram of the indirect modulation scheme implementation.

3.7.1 Simulation Results for MMMC-I

Using the proposed indirect modulation techniques, typical output voltage and current waveforms of MMMC-I obtained under the two switching patterns are shown in Fig. 3-10 and Fig. 3-11. For the inverter stage calculations, both the two-level and three-level SVM methods provide the same results, and the following waveforms are derived with the two-level method. In Fig. 3-10 and Fig. 3-11, the output fundamental frequency is 40 Hz while the total modulation index m_a is 0.9. Being the product of the individual modulation indices of the rectifier and inverter, m_a is essentially equal to m_v as a result of the rectifier's m_c set to unity.

The waveforms of the phase voltage v_{AN} are composed of chopped segments from the inputs. Its shapes in both figures are similar and the THDs are also on a same level. However, when it comes to v_{AB}, the quality improvement brought by Pattern II becomes distinct. Unlike the one obtained under Pattern I in Fig. 3-10 which has a THD of 56.60%, in Fig. 3-11, the center part pulses of the half cycles of v_{AB} does not return to zero, leading to a waveform closer to sinusoid with a much reduced THD of 36.19%. Accordingly, the load currents in Fig. 3-11 also have better waveform shapes with a THD as low as 2.48% compared to the 5.68% in Fig. 3-10.

Fig. 3-12 shows the output voltage and current waveforms of MMMC-I under Pattern II with the output frequency changed to 80 Hz. It verifies that by adjusting the reference vector's rotational speed, the modulation program is able to generate output frequencies either lower or higher than the input.

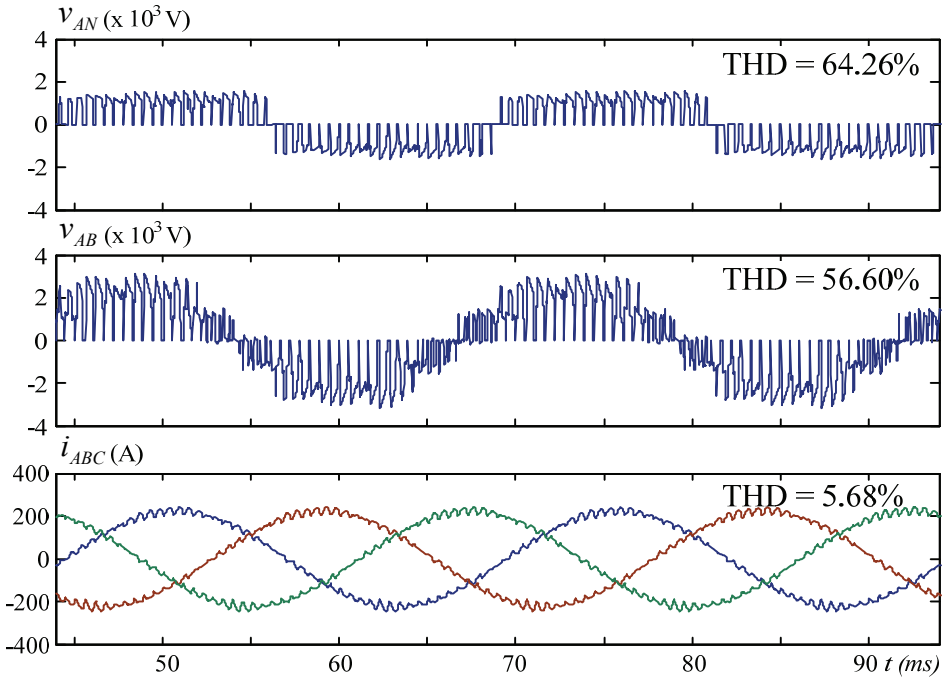


Fig. 3-10 Simulated output voltage and current waveforms of MMMC-I (Pattern I, f_o = 40 Hz, m_a = 0.9).

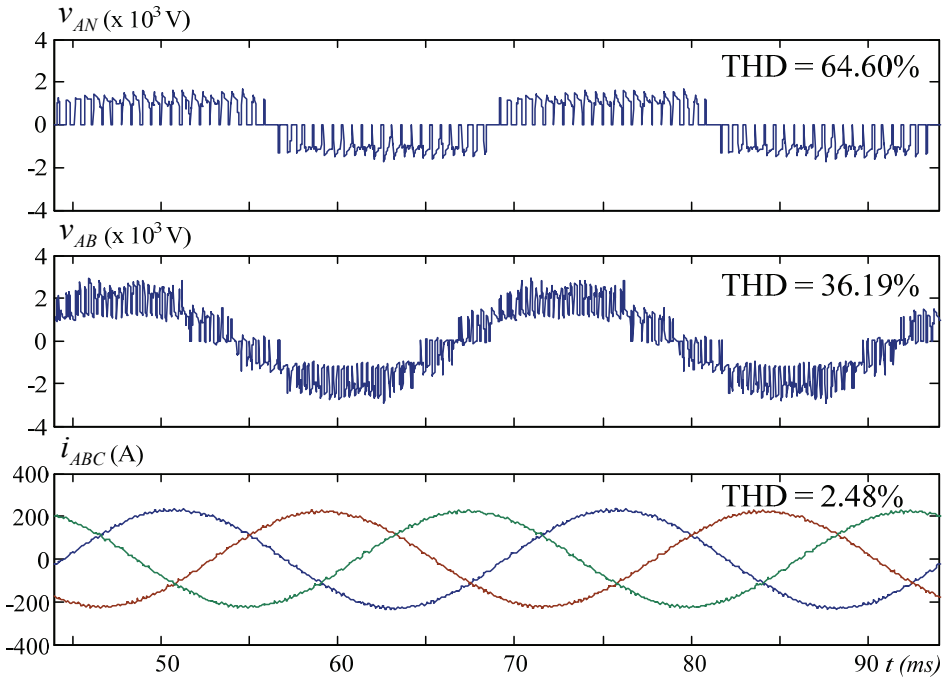


Fig. 3-11 Simulated output voltage and current waveforms of MMMC-I (Pattern II, f_o = 40 Hz, m_a = 0.9).

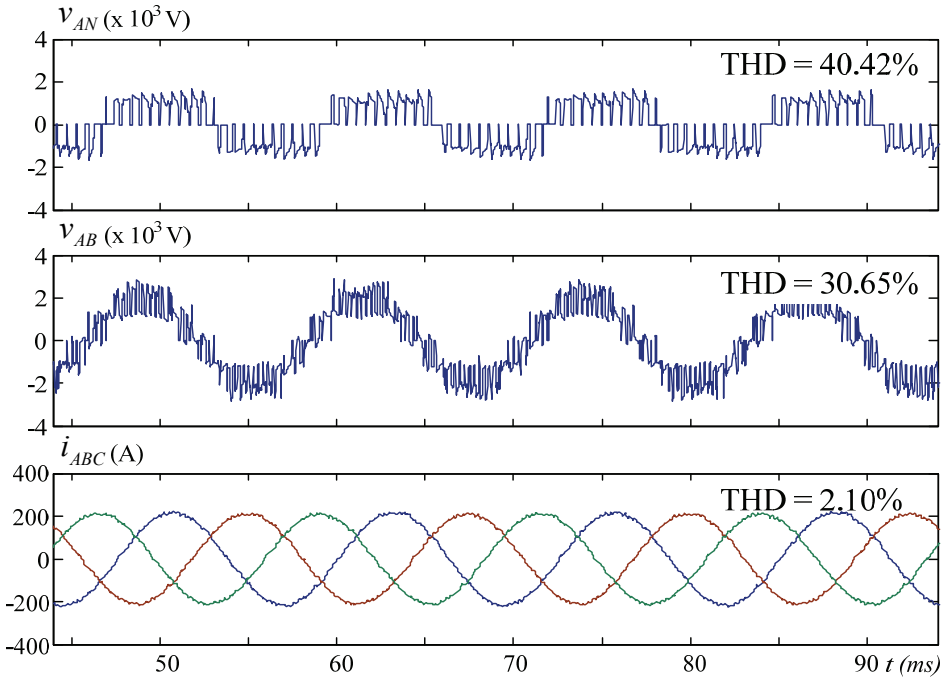


Fig. 3-12 Simulated output voltage and current waveforms of MMMC-I (Pattern II, f_o = 80 Hz, m_a = 0.9).

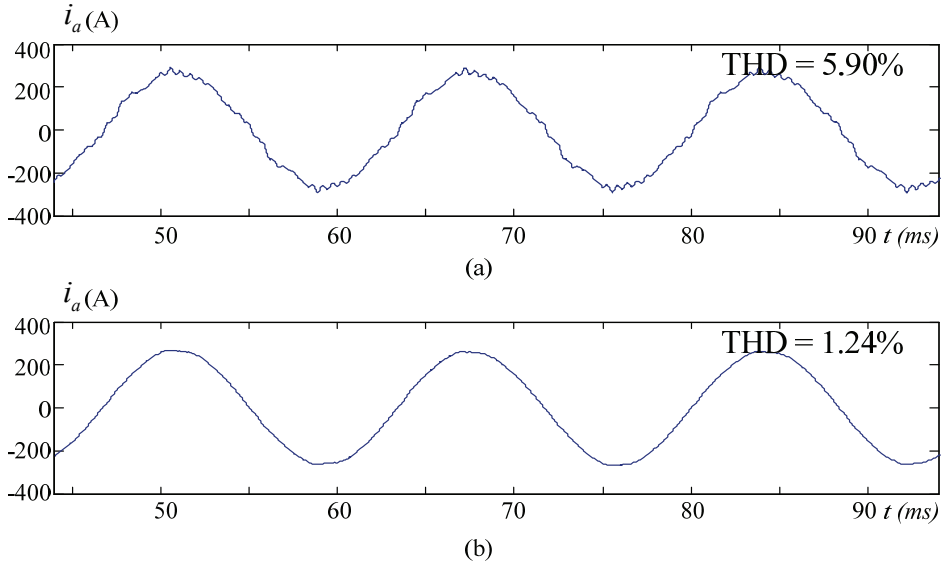


Fig. 3-13 Simulated input current waveforms of MMMC-I (a) Pattern I. (b) Pattern II. (f_o = 40 Hz, m_a = 0.9).

Fig. 3-13 illustrates the current waveform of input phase *a* under both switching patterns. Because the input currents are synthesized from load current pieces, a better waveform quality can be noticed under Pattern II in Fig. 3-13(b) with a lower THD.

3.7.2 Simulation Results for MMMC-II

Consisting of nine MC modules, the MMMC-II topology requires three MMMC-I modulators to operate. Each of them controls a group of three modules supplied by secondary windings that have the same phase shift. As described earlier in Chapter 2, in order to get multilevel waveforms at the outputs, switching periods of the three modulators are displaced from each other by one thirds of an entire cycle. Additionally, the initial angles of the input current reference vectors are adjusted to match their respective winding phase shifts (+20º, 0º, or -20º).

Fig. 3-14 and Fig. 3-15 present typical output voltage and current waveforms of MMMC-II under both switching patterns. In both figures the output fundamental frequency is 40 Hz and the modulation index is 0.9. Due to the higher number of waveform levels in the multi-stepped output voltage, all the results given here have significantly better waveform quality than their counterparts of MMMC-I in Fig. 3-10 and Fig. 3-11. Again, the output line-to-line voltage and load currents obtained under Pattern II possess better harmonic performance than those under Pattern I.

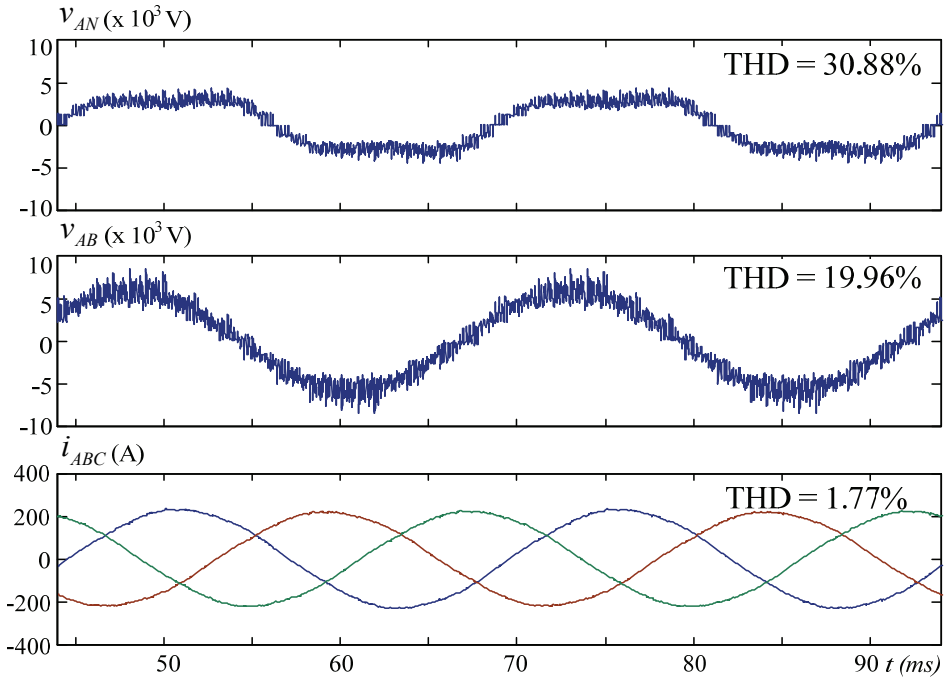


Fig. 3-14 Simulated output voltage and current waveforms of MMMC-II (Pattern I, f_o = 40 Hz, m_a = 0.9).

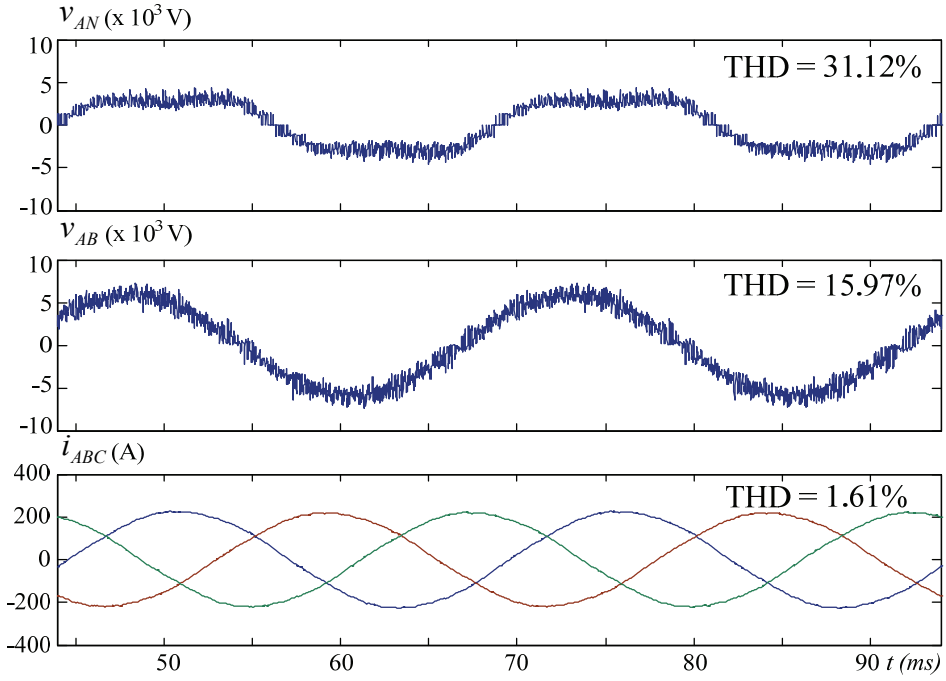


Fig. 3-15 Simulated output voltage and current waveforms of MMMC-II (Pattern II, f_o = 40 Hz, m_a = 0.9).

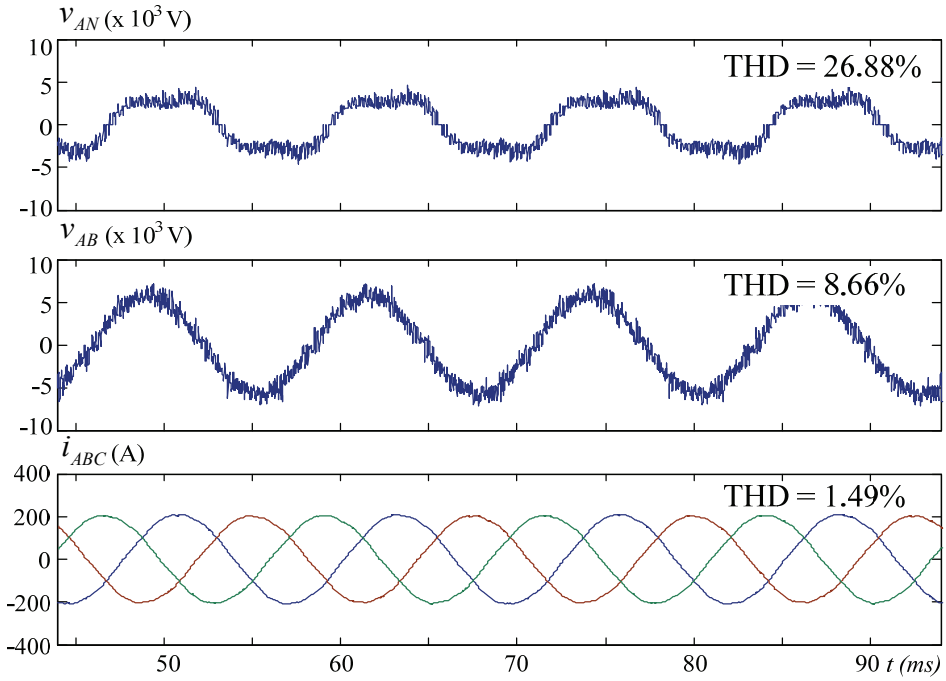


Fig. 3-16 Simulated output voltage and current waveforms of MMMC-II (Pattern II, f_o = 80 Hz, m_a = 0.9).

Fig. 3-16 shows the output waveforms of MMMC-II under Pattern II for a higher output fundamental frequency (80 Hz). Fig. 3-17 gives the input current waveforms of MMMC-II under both switching patterns. Thanks to the harmonic elimination capability of the 18-pulse transformer, the waveform quality of the input currents is further improved comparing to those shown in Fig. 3-13.

In Fig. 3-18, it shows that by controlling the angle of the input current reference vector, the input power factor of MMMC-II can be arbitrarily adjusted to be unity, leading, or lagging.

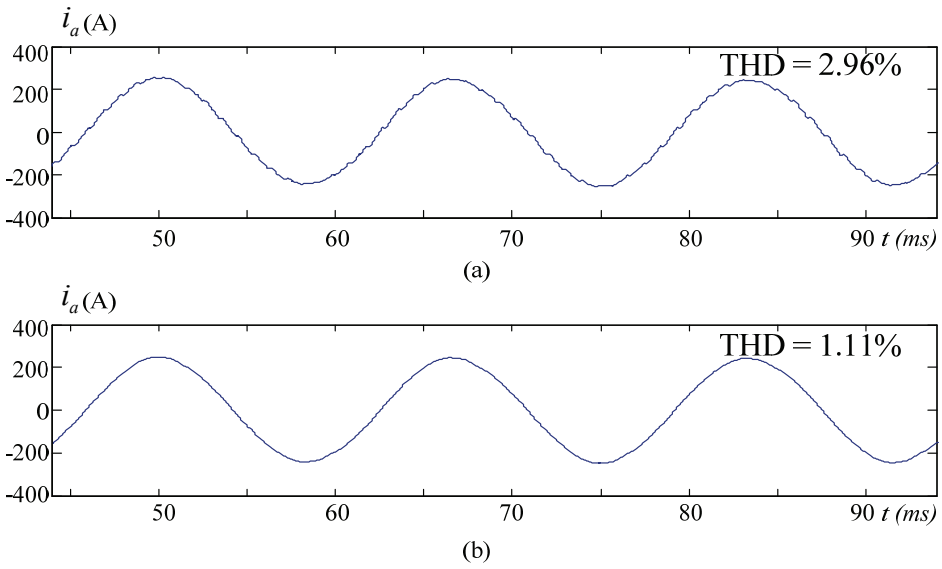


Fig. 3-17 Simulated input current waveforms of MMMC-II (a) Pattern I. (b) Pattern II. (f_o = 40 Hz, m_a = 0.9).

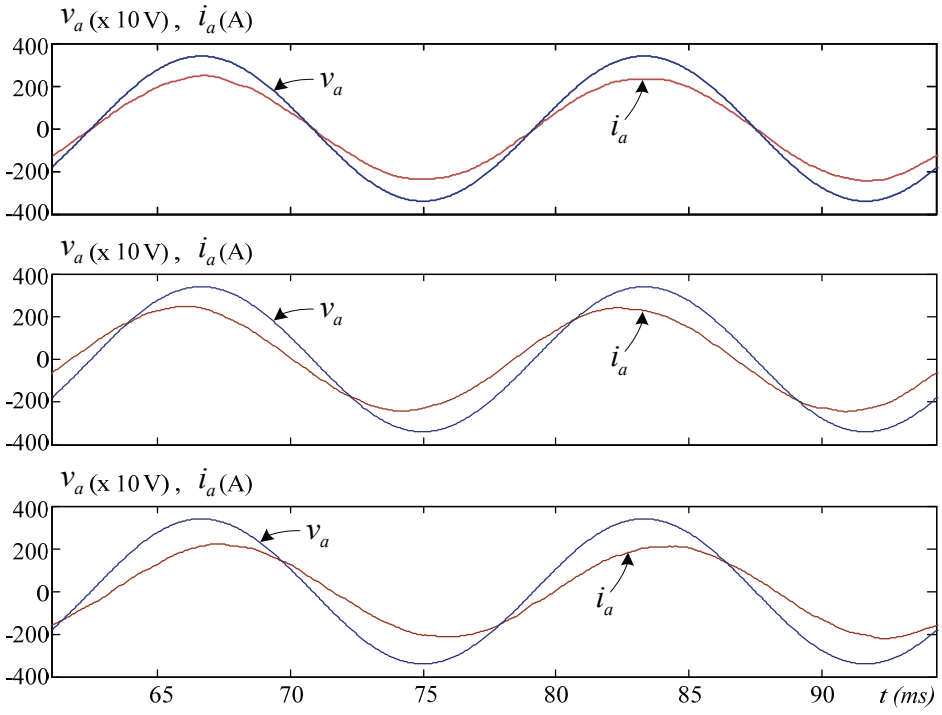


Fig. 3-18 Adjustable input power factor of MMMC-II (Pattern II, f_o = 40 Hz, m_a = 0.9).

3.8 Experimental Verification

The proposed indirect modulation techniques are further tested on the low-voltage prototype with the system parameters listed in Table 2-2. Same as the experiments for the direct modulation scheme presented in the last chapter, all the waveforms are obtained from the setup supplying an RL load, with a 5 kW rated power and fed by 208 Vrms line-to-line grid voltage. The following section provides the experimental waveforms obtained under the indirect modulation scheme under both switching pattern I and II.

In Fig. 3-19 and Fig. 3-20, output waveforms of MMMC-I under switching pattern I and II are presented for an output fundamental frequency of 40 Hz. Similar to the simulation results, although the phase-to-neutral voltage v_{AN} has close waveform shapes under both patterns, switching pattern II provides a waveform with significantly better quality when it comes to the line-to-line voltage v_{AB}. Correspondingly, the load current waveform in Fig. 3-20 under pattern II is also much smoother than that in Fig. 3-19.

Fig. 3-21 illustrates the output waveforms of MMMC-I under pattern II for a higher output fundamental frequency (80 Hz). By changing the rotational speed of the voltage reference vector in the VSI SVM, the output frequency can be adjusted at will by the modulation program.

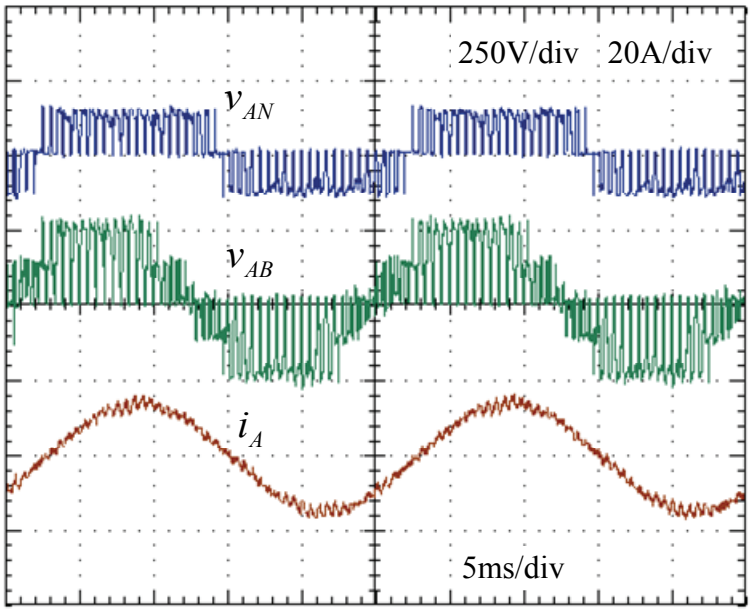


Fig. 3-19 Experimental output voltage and current waveforms of MMMC-I (Pattern I, f_o = 40 Hz, m_a = 0.9).

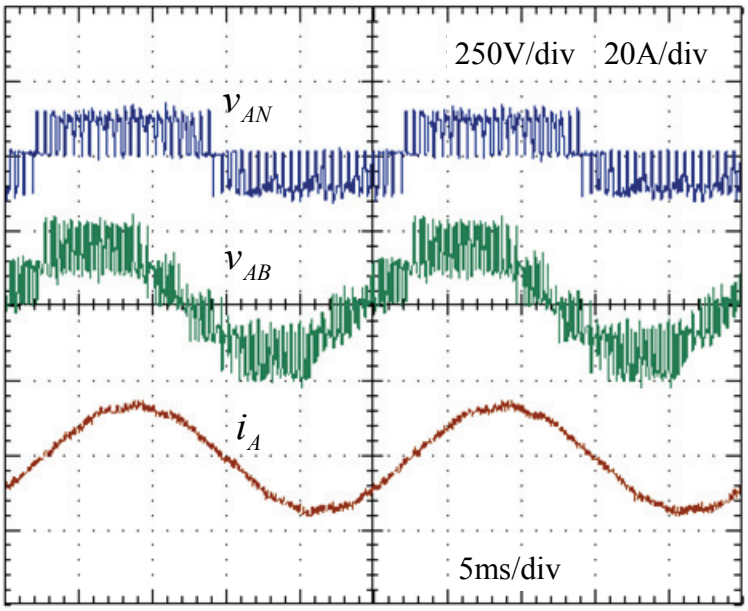


Fig. 3-20 Experimental output voltage and current waveforms of MMMC-I (Pattern II, f_o = 40 Hz, m_a = 0.9).

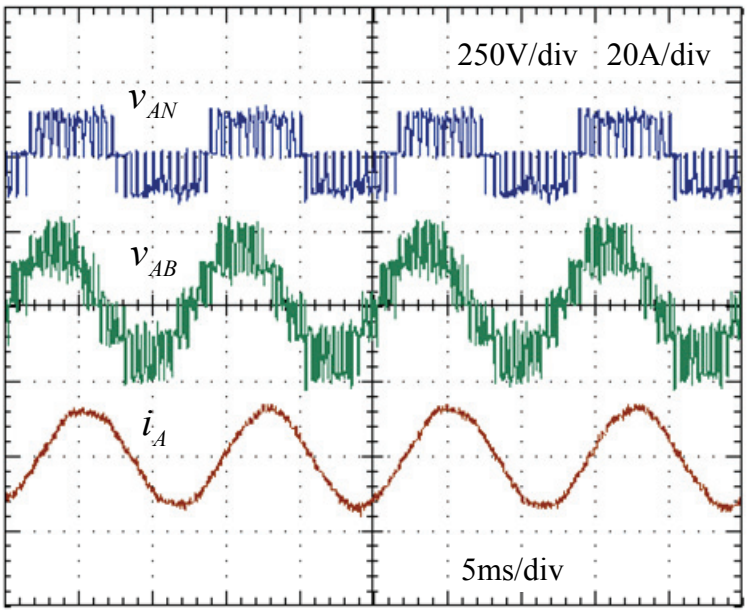


Fig. 3-21 Experimental output voltage and current waveforms of MMMC-I (Pattern II, f_o = 80 Hz, m_a = 0.9).

Fig. 3-22, Fig. 3-23 and Fig. 3-24 give the output side waveforms of MMMC-II, which are smoother and closer to sinusoids compared to those of MMMC-I due to their higher steps of multilevel waveform shapes. Same as the MMMC-I, by adjusting the rotational speed of the output voltage reference vector, output frequency either higher (80 Hz) or lower (40 Hz) than the input is achievable.

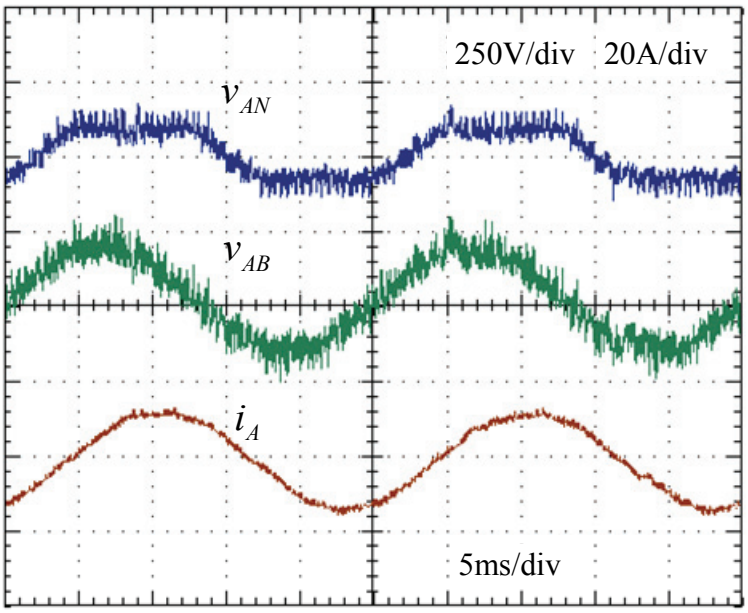


Fig. 3-22 Experimental output voltage and current waveforms of MMMC-II (Pattern I, f_o = 40 Hz, m_a = 0.9).

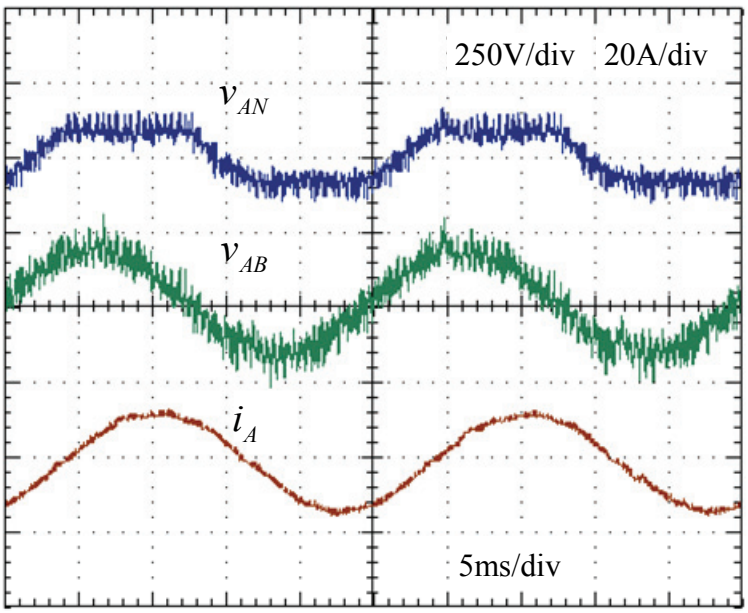


Fig. 3-23 Experimental output voltage and current waveforms of MMMC-II (Pattern II, f_o = 40 Hz, m_a = 0.9).

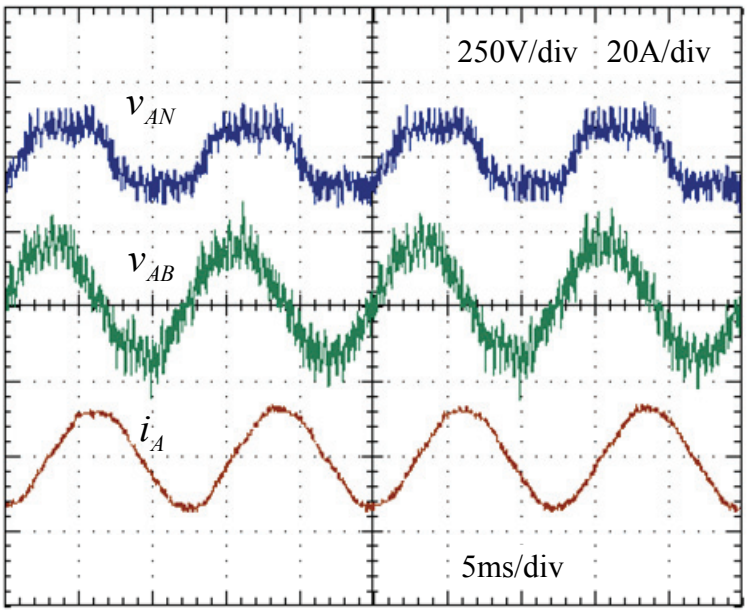


Fig. 3-24 Experimental output voltage and current waveforms of MMMC-II (Pattern II, f_o = 80 Hz, m_a = 0.9).

On the other side, input voltage and current waveforms of both converters are shown in Fig. 3-25 and Fig. 3-26 under unity power factor condition. Due to polluted grid and LC resonance, the input current waveforms for MMMC-I in Fig. 3-25 contain visible harmonic components. However, the same currents of MMMC-II appear with superior quality which is attributed to the harmonic elimination capability of the input phase-shifting transformers. Finally, the cases of leading, lagging, and unity input power factor of MMMC-II are given in Fig. 3-27, which are obtained by adjusting the initial angle of the input current reference vector in the modulation program.

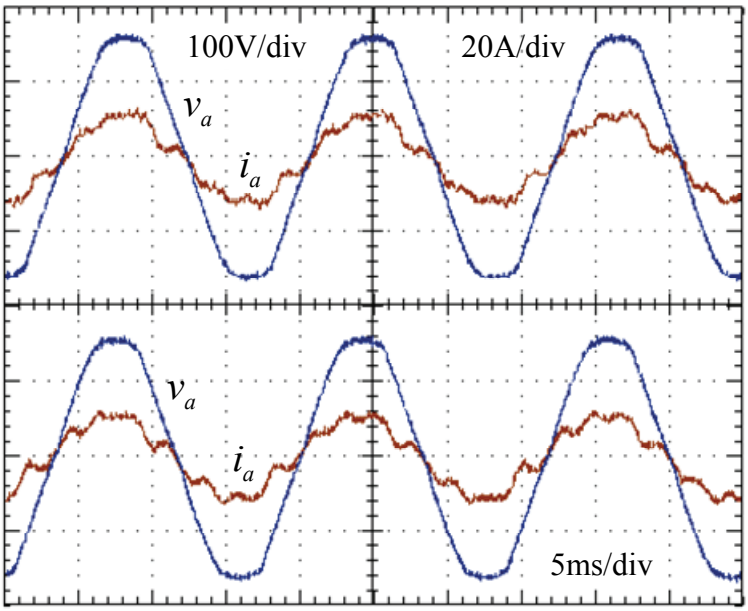


Fig. 3-25 Experimental input voltage and current waveforms of MMMC-I (Pattern I and II, f_o = 40 Hz, m_a = 0.9).

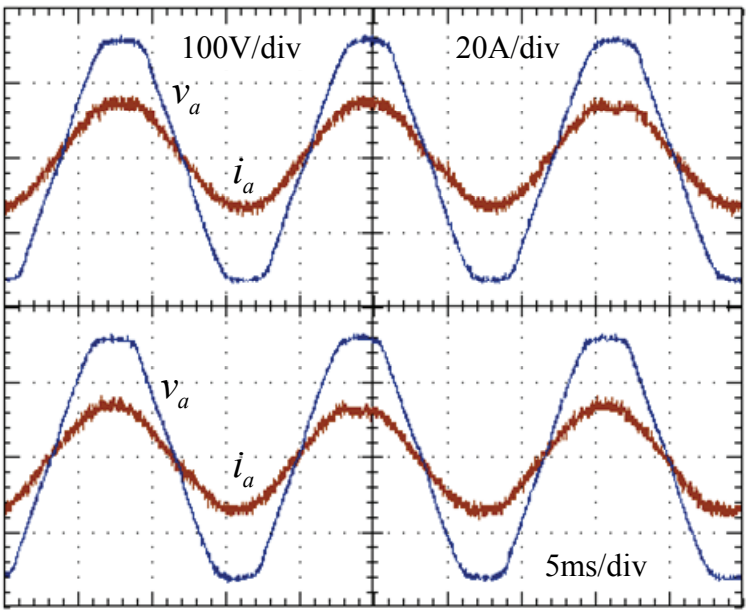


Fig. 3-26 Experimental input voltage and current waveforms of MMMC-II (Pattern I and II, f_o = 40 Hz, m_a = 0.9).

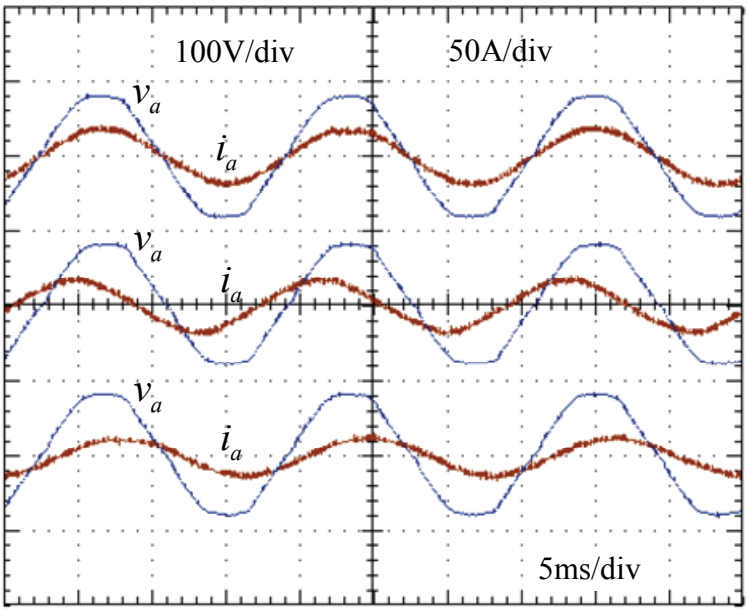


Fig. 3-27 Experimental input waveforms of MMMC-II showing adjustable power factor (Pattern II, f_o = 40 Hz, m_a = 0.9).

3.9 Summary

This chapter is focused on developing indirect space vector based modulation techniques for the MMMC topologies. It is revealed that as long as the input transformer is regarded no more than an isolation stage with a voltage gain, and the module outputs are seen as inverters that share a common input rectifier stage, the classic rectifier – fictitious dc – inverter concept from the conventional matrix converter can still be adopted for establishing an indirect circuit model of the MMMCs. Consequently, space vector modulation calculations can be separately applied to the rectifier and inverter stages of the model for duty ratio derivation. The derived switching states and duty ratios are then converted and combined to produce the final gate signals. For the inverter stage, both two-level and three-level SVM programs can be employed for the output voltage synthesis. This

chapter also proposes a novel switching pattern for the output pulse generation in the MMMCs, and demonstrates that the new pattern provides superior waveform quality over the conventional one. The modulation and switching concepts are verified by both simulation and experimental results.

Chapter 4

Modulation Using DFE Emulation and Phase-Shifted SPWM

As mentioned earlier, among all multilevel converter topologies, there exists a particular breed realized by connecting output terminals of modular converter cells in series. Typical members of this category include the cascaded H-bridge converter (CHB) [18, 59] and the modular multilevel converters (MMCs) [8, 40, 60]. With the cascaded structure, these converters can reach very high power/voltage levels while employing low-voltage devices only, and in general possess features like modular design, superior waveform quality under limited device switching frequency, and good fault-tolerant capability. Being a combination of cascaded structure and matrix converter (MC) modules, the multimodular matrix converters (MMMCs) also belong to the cascaded converter family. A typical MMMC fed by a phase-shifting-transformer is similar to the CHB converter in terms of topological structure, but is different from the latter in the construction of constituent power modules. In a CHB converter, each power module contains a dc capacitor, and the output voltage is synthesized from the voltage-stiff dc-link; however in an MMMC, the output voltage of any single module is directly fabricated from the module's ac input voltages.

The previous chapters introduced direct and indirect modulation schemes for the MMMCs. The presented schemes consider multiple MC modules as an integral and manage to synthesize output voltage and input current at the same time. They can generate

sinusoidal waveforms and are able to adjust the input power factor of the converter by varying the input current reference angle. In this chapter, a different modulation strategy for the phase-shifting-transformer-fed MMMC is proposed. Unlike the previous methods, the new scheme cannot adjust the input power factor. By taking advantage of the indirect construction of the MC modules, the new scheme makes the rectifier stage of each module emulate the voltage transfer characteristic of a diode front-end (DFE), while applying the well-known phase-shifted sinusoidal PWM (PS-SPWM) for inverter stage control. As a result, the input phase-shifting transformer is effectively made use of for output voltage and input current quality improvement. Compared with the previous methods, the new modulation scheme is simpler and more straightforward, easier to implement, and associated with lower switching losses. The possibility of its application to MMMCs built with physically constructed indirect 3 x 2 MC modules could lead to significant reduction of the converter's semiconductor cost, as well as elimination of the complexity involved in bidirectional switch device commutations which are essential in direct MC modules.

4.1 3 x 2 Converter Module Structures

Fig. 4-1 illustrates a cascaded converter structure consisting of nine power modules fed by an 18-pulse phase-shifting transformer. The overall topology structure is common for both the CHB converter and the MMMC topology, while the different 3 x 2 module structures for non-regenerative CHB, regenerative CHB, and MMMC are given in Fig. 4-2(a), (b) and (c), respectively. The non-regenerative CHB module is fed by a diode front-end whereas the regenerative CHB module contains an active rectifier. For the direct 3 x 2 MC module given in Fig. 4-2(c), a total of six bidirectional switches are needed, each of them realized by two insulated-gate bipolar transistor (IGBT)-diode pairs and connecting one of the module's output ports to one of the input ports. Because a single direct MC

module contains 12 IGBT devices, to build a nine-module MMMC with it requires 108 IGBTs in total. Moreover, as the IGBTs are grouped in pairs to form the four-quadrant bidirectional switches, complicated device commutation control as well as a large number of isolated gate drivers and power supplies is necessary, resulting in relatively high converter and accessory cost.

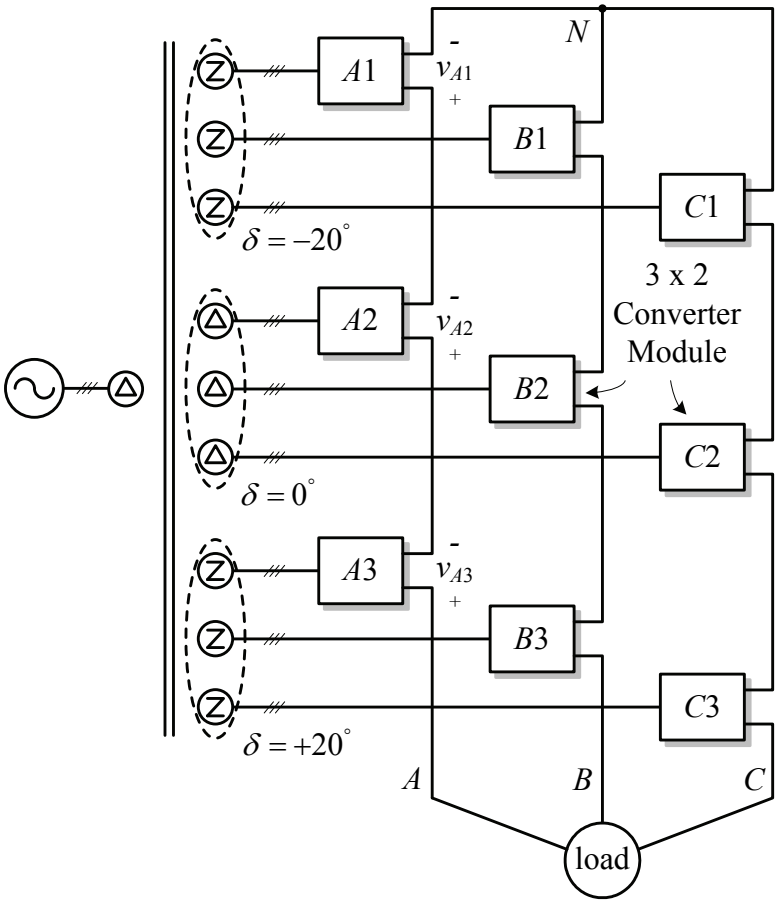
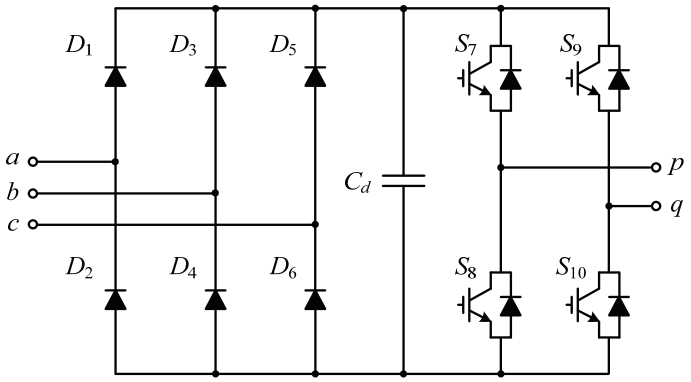
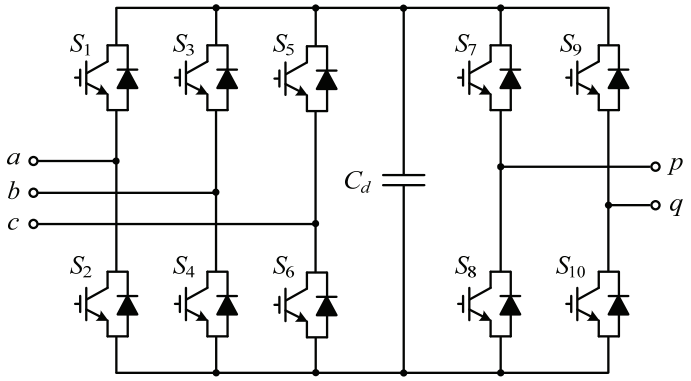


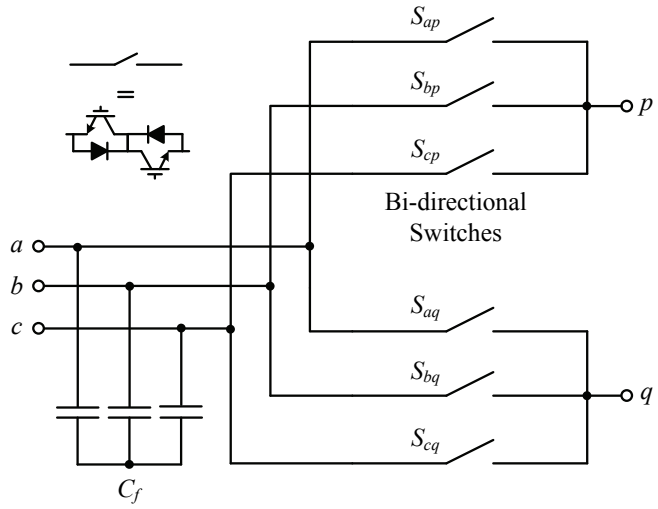
Fig. 4-1 Cascaded converter structure with nine power modules.



(a)



(b)



(c)

Fig. 4-2 Power module construction for (a) Non-regenerative CHB. (b) Regenerative CHB. (c) MMMC.

It is well known that a conventional three-phase to three-phase (3 x 3) MC can be constructed either directly or indirectly. While the direct construction is implemented with bidirectional switches making straight connections between input and output ports, the indirect construction separates the entire MC into a rectifier stage and an inverter stage, which are coupled to each other through an imaginary dc-link with no real energy storage components. Similarly, an alternative choice to realize a 3 x 2 MC module is to adopt the indirect construction consisting of a three-phase rectifier and a single-phase inverter. In a classic indirect MC construction, bidirectional switches are still needed in the rectifier or inverter stage to block possible reverse dc-link voltages [42], however, if a proper modulation scheme can guarantee the constant positive voltage polarity of the dc-link, the indirect module can be formed by unidirectional voltage-blocking switches only and could have a lower total device count. Fig. 4-3 illustrates an entire MMMC leg of output phase *A* using indirect 3 x 2 MC modules. The structure of the indirect MC modules is similar to a regenerative CHB cell, except that the MC modules do not have dc capacitors but are equipped with ac filter capacitors. It can be seen that with this specific module configuration, the total number of devices required by a nine-module MMMC is reduced to 90, and the number of necessary gate drivers/power supplies are significantly reduced too. Additionally, the complicated device commutation control for bidirectional switches is no longer necessary since only unidirectional switches are employed in the power modules.

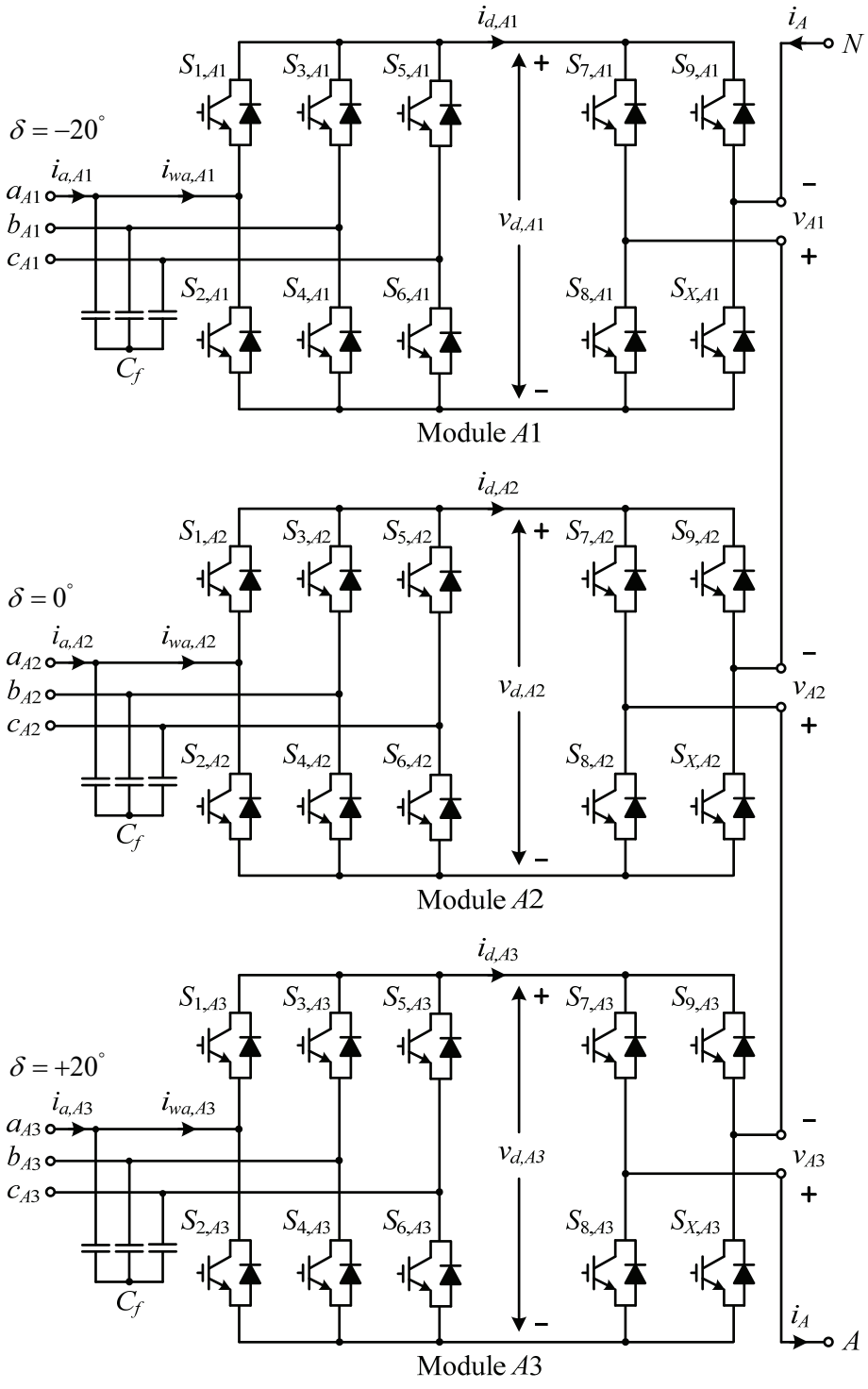


Fig. 4-3 MMMC leg of output phase *A* with indirect MC modules.

4.2 Modulation Scheme

4.2.1 Diode Front-End Emulation for the Rectifier Stage

The new modulation scheme functions by making the rectifier stage of the indirect MC modules emulate the voltage transfer characteristic of a diode rectifier, such that the maximum ac line-to-line input voltage is always passed to the dc-link for inverter use. However, because of the employment of active switches, bidirectional current flow and thereby regenerative operation is allowed in the rectifier, being its main difference from a real diode bridge. Fig. 4-4 shows the ideal rectifier stage voltage waveforms in an indirect MC module under this type of control. The dc-link voltage v_d in the figure appears to have the same shape as the output of a three-phase diode rectifier and contains six pulses per fundamental cycle of the input voltage. Consequently, the voltage polarity of the dc-link is always positive, and hence the use of conventional IGBTs without reverse voltage blocking capability as shown in Fig. 4-3 becomes viable.

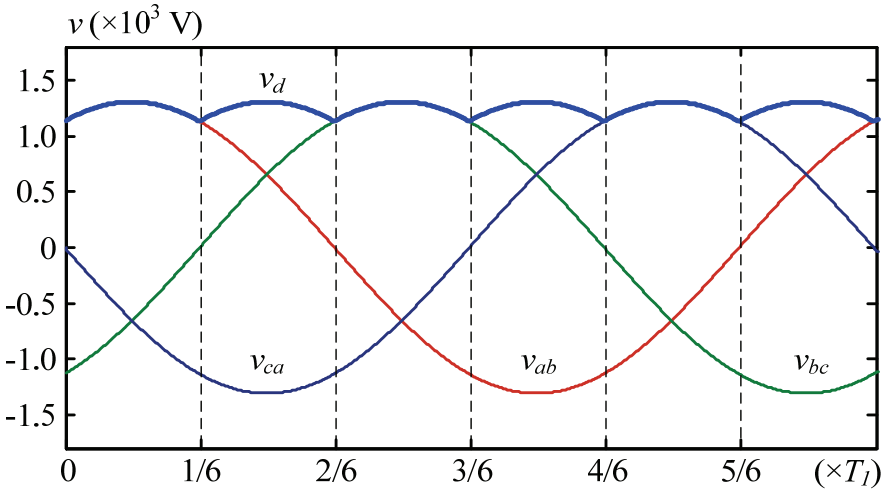


Fig. 4-4 Ideal rectifier side voltage waveforms in an indirect MC module.

4.2.2 Phase-Shifted SPWM for the Inverter Stage

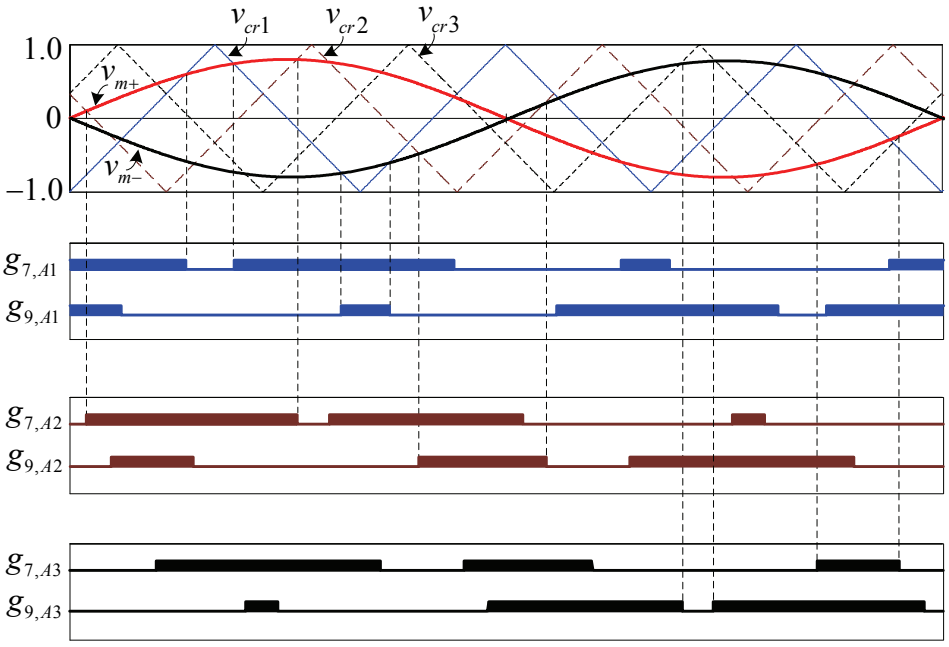


Fig. 4-5 Inverter stage gate signals generated by phase-shift modulation.

For the inverter stage, the widely used carrier-based phase-shifted SPWM for the CHB converters [23] can be readily employed. In Fig. 4-5, the PS-SPWM diagram and gate signal generation for the inverter stage devices of the three MC modules in Fig. 4-3 (output phase *A*) are illustrated. As the entire output phase leg consists of three modules, two sinusoidal modulating waves (v_{m+} and v_{m-}) as well as three triangular carrier waves (v_{cr1}, v_{cr2} and v_{cr3}) are needed. The triangular carriers are evenly distributed in the modulation plane and have equal phase displacements between one another. The resultant switching frequency of the inverter stage devices are determined by the frequency of the carriers. In the figure, only gate signals for the upper devices in each module are shown; the lower devices are switched complementarily with respect to the upper devices.

4.2.3 Mathematical Derivation of Input and Output Quantities

With the above described rectifier stage control, the dc-link voltage of each indirect MC module contains a dc component and ac harmonic components at orders of every multiple of 6. Taking into account the input voltage phase shifts introduced by the 18-pulse transformer, the dc-link voltages of the three modules in Fig. 4-3 can be expressed as the following by means of Fourier series expansion

$$\begin{aligned} v_{d,A1} &= V_{dc} + \sum_{k=1}^{\infty} V_{6k} \cos[6k(\omega_i t + \pi/9) + \varphi_{6k}] \\ v_{d,A2} &= V_{dc} + \sum_{k=1}^{\infty} V_{6k} \cos[6k\omega_i t + \varphi_{6k}] \\ v_{d,A3} &= V_{dc} + \sum_{k=1}^{\infty} V_{6k} \cos[6k(\omega_i t - \pi/9) + \varphi_{6k}] \end{aligned} \tag{4.1}$$

where V_{dc} is the dc component of the six-pulse rectified voltage waveforms (equaling to 1.35 times the transformer secondary line-to-line voltage); V_{6k} is the amplitude of the 6kth-order harmonic component; ω_i represents the input fundamental angular frequency; and φ_{6k} designates the initial angle of the 6kth-order harmonic component.

On the other hand, the inverter stage voltage relationship in a single module can be given as (taking Module $A1$ as an example)

$$v_{A1} = v_{d,A1} \cdot [S_{7,A1}(t) - S_{9,A1}(t)] \tag{4.2}$$

in which $S_{7,A1}$(t) and $S_{9,A1}$(t) are the switching functions controlled by gate signals $g_{7,A1}$ and $g_{9,A1}$. As the PS-SPWM is essentially bipolar sinusoidal pulse-width modulation with phase-shifted carriers, the switching functions are actually determined by the modulating waves of v_{m+} and v_{m-}

$$\begin{aligned} v_{m+} &= 0.5 m_a \cos(\omega_o t + \theta_o) \\ v_{m-} &= -0.5 m_a \cos(\omega_o t + \theta_o) \end{aligned} \tag{4.3}$$

where m_a and θ_o are the output modulation index and fundamental component angle which provide two degrees of freedom for load side control, and ω_o is the output fundamental angular frequency. Assuming the carrier frequency is sufficiently high, the low-frequency form of (4.2) when averaged over the carrier period can be written as follows

$$\overline{v}_{A1} = \overline{v}_{d,A1} m_a \cos(\omega_o t + \theta_o). \tag{4.4}$$

Hence, the total output phase-to-neutral voltage is

$$
\begin{aligned}
\overline{v}_{AN} &= \overline{v}_{A1} + \overline{v}_{A2} + \overline{v}_{A3} \\
&= m_a \cos(\omega_o t + \theta_o) \cdot (\overline{v}_{d,A1} + \overline{v}_{d,A2} + \overline{v}_{d,A3}) \\
&= m_a \cos(\omega_o t + \theta_o) \cdot \\
&\left\{ \begin{aligned}
&3V_{dc} + \sum_{k=1}^{\infty} V_{6k} \cos[6k(\omega_i t + \pi/9) + \varphi_{6k}] \\
&+ \sum_{k=1}^{\infty} V_{6k} \cos[6k\omega_i t + \varphi_{6k}] \\
&+ \sum_{k=1}^{\infty} V_{6k} \cos[6k(\omega_i t - \pi/9) + \varphi_{6k}]
\end{aligned} \right\}.
\end{aligned} \tag{4.5}
$$

It can be seen that, due to the phase shifts introduced by the 18-pulse transformer, all the 6*k*th harmonics except the multiples of 18th are cancelled out. As a result (4.5) can be rewritten as

$$
\begin{aligned}
\overline{v}_{AN} &= m_a \cos(\omega_o t + \theta_o) \cdot \\
&\left\{ 3V_{dc} + 3\sum_{k=1}^{\infty} V_{18k} \cos[18k\omega_i t + \varphi_{18k}] \right\}.
\end{aligned} \tag{4.6}
$$

Since the 18*k*th harmonic components have very little amplitudes, their effect on the inductive load is minimum. The total output-to-input voltage magnitude relationship can be then given as

$$
V_{AB} = 7.01 \cdot \frac{N_s}{N_p} \cdot m_a \cdot V_{ab} \tag{4.7}
$$

in which N_s / N_p stands for the secondary-to-primary turns ratio of the transformer, and m_a is in the range of 0 to 1.

For the current analysis, by neglecting the high order harmonics in the generated module output voltages, the converter output current can be derived for a given load impedance and expressed as follows (assuming the load is three-phase balanced)

$$i_A = I_L \cos(\omega_o t + \theta_o - \theta_L) \tag{4.8}$$

where I_L and θ_L are the load current magnitude and load power factor angle, respectively. Since the dc-link current in MC module $A1$ is

$$i_{d,A1} = i_A \cdot [S_{7,A1}(t) - S_{9,A1}(t)], \tag{4.9}$$

its low-frequency local average can be given as

$$\begin{aligned} \overline{i}_{d,A1} &= I_L \cos(\omega_o t + \theta_o - \theta_L) \cdot m_a \cos(\omega_o t + \theta_o) \\ &= \frac{I_L m_a}{2} [\cos(2\omega_o t + 2\theta_o) + \cos(\theta_L)]. \end{aligned} \tag{4.10}$$

Neglecting the line impedances, the phase a secondary winding current $i_{a,A1}$ at the input of module $A1$ is

$$
\begin{aligned}
i_{a,A1} &= \bar{i}_{d,A1} \cdot [S_{1,A1}(t) - S_{2,A1}(t)] + C_f dv_{a,A1} / dt \\
&= \frac{I_L m_a}{2} [\cos(2\omega_o t + 2\theta_o) + \cos(\theta_L)] \cdot \\
&\quad [S_{1,A1}(t) - S_{2,A1}(t)] + C_f dv_{a,A1} / dt
\end{aligned} \tag{4.11}
$$

where $S_{1,A1}$(t) and $S_{2,A1}$(t) are the switching functions for devices $S_{1,A1}$ and $S_{2,A1}$, respectively. In a similar way, the input currents of modules $B1$ and $C1$ can be derived and given in (4.12) and (4.13)

$$
\begin{aligned}
i_{a,B1} &= \bar{i}_{d,B1} \cdot [S_{1,B1}(t) - S_{2,B1}(t)] + C_f dv_{a,B1} / dt \\
&= \frac{I_L m_a}{2} [\cos(2\omega_o t + 2\theta_o - 4\pi/3) + \cos(\theta_L)] \cdot \\
&\quad [S_{1,B1}(t) - S_{2,B1}(t)] + C_f dv_{a,B1} / dt
\end{aligned} \tag{4.12}
$$

$$
\begin{aligned}
i_{a,C1} &= \bar{i}_{d,C1} \cdot [S_{1,C1}(t) - S_{2,C1}(t)] + C_f dv_{a,C1} / dt \\
&= \frac{I_L m_a}{2} [\cos(2\omega_o t + 2\theta_o + 4\pi/3) + \cos(\theta_L)] \cdot \\
&\quad [S_{1,C1}(t) - S_{2,C1}(t)] + C_f dv_{a,C1} / dt .
\end{aligned} \tag{4.13}
$$

Due to the fact that modules $A1$, $B1$ and $C1$ are supplied by a group of transformer secondary windings that have the same phase shift (-20º), the rectifier stage switching functions in these modules are all the same. Therefore, the $2\omega_o$ components in $i_{a,A1}$, $i_{a,B1}$, and $i_{a,C1}$ are cancelled out when the three currents are summed and referred to the primary side. As a result the remaining part of $i_{a,A1}$ can be expressed as

$$i'_{a,A1} = \frac{I_L m_a}{2}\cos(\theta_L)\cdot[S_{1,A1}(t) - S_{2,A1}(t)] + C_f dv_{a,A1}/dt. \tag{4.14}$$

As described earlier the rectifier stage of the MC modules is operated by diode front-end emulation, so the switching function in (4.14) can be expanded to the following Fourier series [58]

$$\begin{aligned} & S_{1,A1}(t) - S_{2,A1}(t) \\ &= \sum_{n=1,5,7,11\ldots}^{\infty} \frac{4}{n\pi}\sin(\frac{n\pi}{2})\sin(\frac{n\pi}{3})\sin(n\omega_i t) \\ &= \frac{2\sqrt{3}}{\pi}\left[\begin{array}{l}\sin(\omega_i t) - \dfrac{\sin(5\omega_i t)}{5} - \dfrac{\sin(7\omega_i t)}{7} \\ + \dfrac{\sin(11\omega_i t)}{11} + \dfrac{\sin(13\omega_i t)}{13} + \cdots\end{array}\right]. \end{aligned} \tag{4.15}$$

From (4.15) it can be identified that the secondary winding current $i_{a,A1}$ contains several low-order harmonics as a result of the rectifier stage switchings. However, because the average dc-link currents in modules $A1$, $A2$, and $A3$ are equal owing to the inverter stage PS-SPWM, and thanks to the 18-pulse rectifier configuration which is able to eliminate the 5th, 7th, 11th, and 13th harmonic components [23], the dominant harmonics are removed on the primary side of the transformer, leading to a sinusoidal current waveform of i_a.

4.2.4 Effect of the 18-Pulse Phase-shifting Transformer

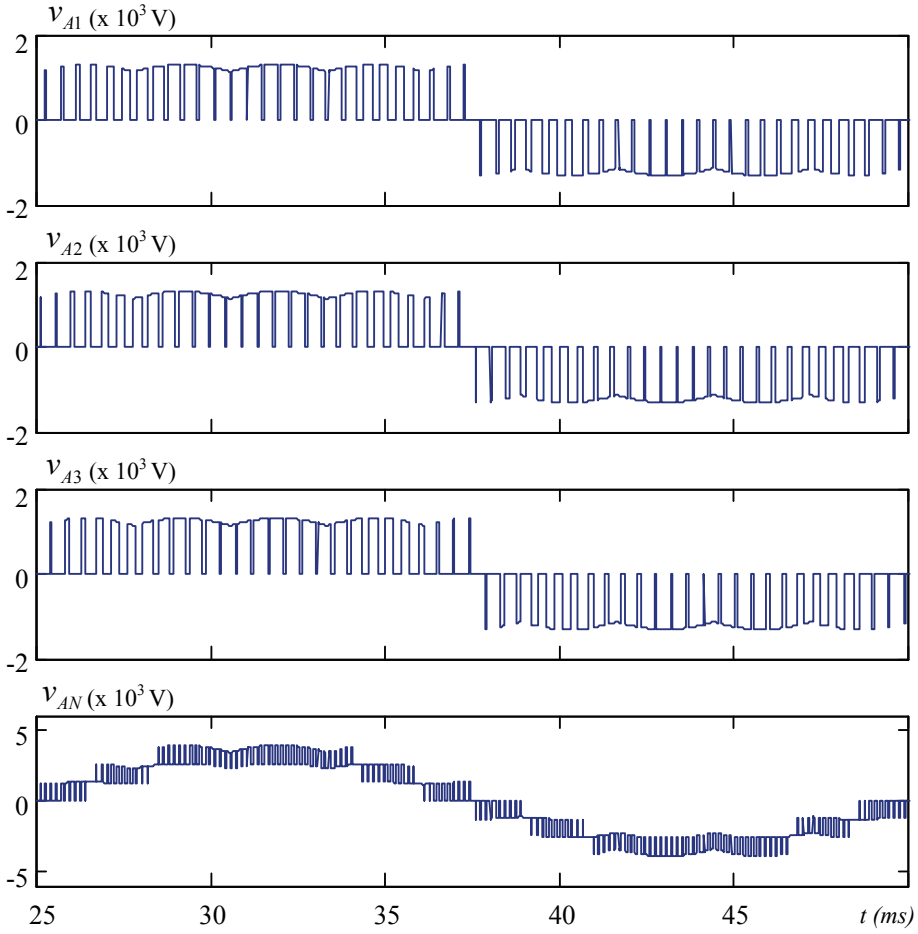


Fig. 4-6 Ideal phase *A* output voltages without phase shifts in the transformer secondary windings.

As is analyzed above, the 18-pulse phase-shifting transformer plays an important role to make effective the proposed modulation scheme. The transformer is essential for both input current and output voltage quality improvement. On the input side, because the rectifier stage of the MC modules is switched like a diode front-end, a significant amount of low order current harmonics exist in the transformer's secondary windings. But since the inverter stage employs the carrier-based PS-SPWM which guarantees balanced load sharing

among modules on a same output phase, the low-order current harmonics are cancelled out in the transformer, thereby resulting in sinusoidal current waveforms at the primary side.

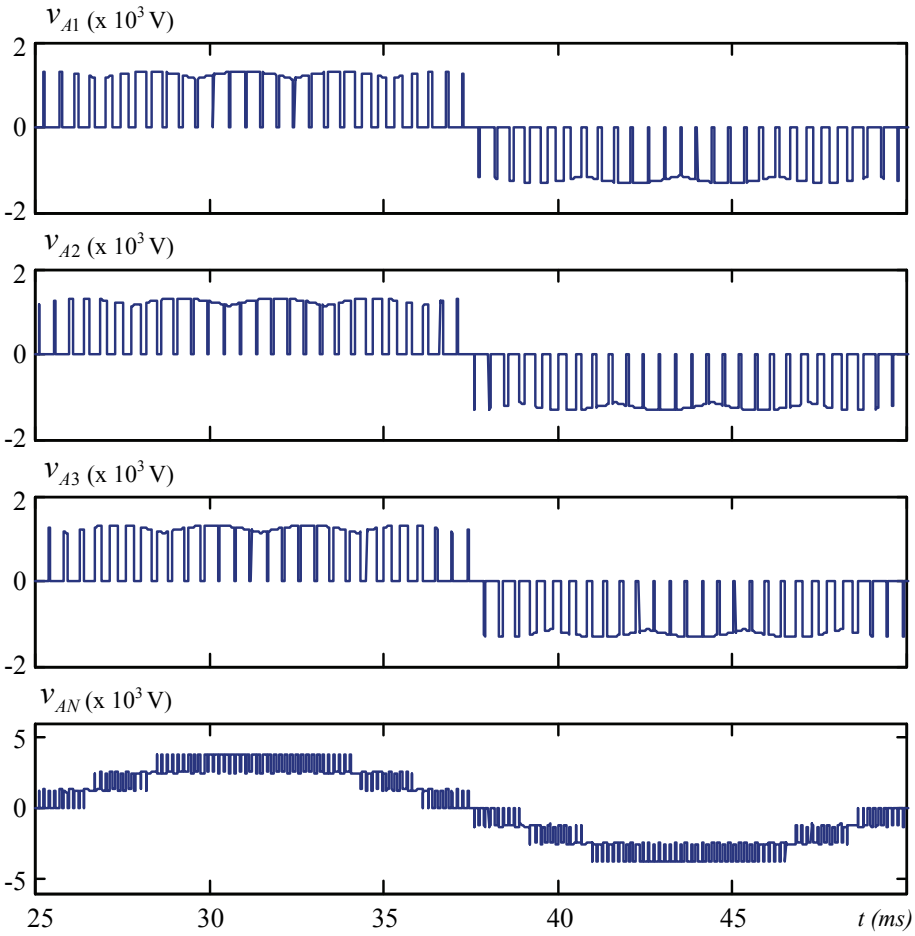


Fig. 4-7 Ideal phase *A* output voltages with phase shifts in the transformer secondary windings.

For the output voltage synthesis, the phase displacements in the transformer's secondary windings have a positive effect too. Fig. 4-6 shows the situation if the winding phase shifts do not exist, in which the output phase voltage v_{AN} is affected by the six-pulse voltage waveform in the dc-links of the MC modules and contains corresponding harmonic

distortions. With the 18-pulse effect introduced by the winding phase shifts, the waveform of v_{AN} is free of the low frequency distortions and has a much better shape in Fig. 4-7.

4.2.5 Gate Signal Mapping for Direct MC Module

The gate signals generated for the indirect 3 x 2 MC modules can also be used to control an MMMC constructed with direct 3 x 2 MC modules. Before the gate signals are applied to the switching devices, a logic mapping program is needed to convert them. Considering the direct MC module as shown in Fig. 4-2(c) and the indirect MC module $A1$ as shown in Fig. 4-3, the logic mapping of the signals can be expressed as

$$\begin{aligned}
g_{ap} &= g_{1,A1} \cdot g_{7,A1} + g_{2,A1} \cdot g_{8,A1} \\
g_{bp} &= g_{3,A1} \cdot g_{7,A1} + g_{4,A1} \cdot g_{8,A1} \\
g_{cp} &= g_{5,A1} \cdot g_{7,A1} + g_{6,A1} \cdot g_{8,A1} \\
g_{aq} &= g_{1,A1} \cdot g_{9,A1} + g_{2,A1} \cdot g_{\mathrm{X},A1} \\
g_{bq} &= g_{3,A1} \cdot g_{9,A1} + g_{4,A1} \cdot g_{\mathrm{X},A1} \\
g_{cq} &= g_{5,A1} \cdot g_{9,A1} + g_{6,A1} \cdot g_{\mathrm{X},A1} .
\end{aligned} \tag{4.16}$$

On the right side of the equations are the original gate signals generated for the indirect MC module, whereas on the left side are the corresponding gate signals for the direct MC module. Input/output equivalence between the two types of modules is hereby established.

4.2.6 Reduction of Additional Switchings Caused by Input Voltage Ripples

In Fig. 4-4, the ideal case source voltages at the input terminals of the MC modules consist of a balanced set of three-phase pure sinusoids. Since the amplitude relationship among the three waveforms changes six times per fundamental cycle, an entire input voltage period can be equally divided into six sectors, hence, the rectifier stage devices of the MC modules are switched exactly at the source voltage frequency. However, due to the existence of line and transformer impedances, the actual input terminal voltages (i.e. the voltages on the filter capacitors) may deviate from the source in practice. Among other factors, the inverter stage switching behavior adds higher frequency ripples to the capacitor voltages. These ripples may cause multiple instances of crossings between voltage waveforms, therefore leading to an increased number of amplitude relationship changes. Because the rectifier stage modulation is based on the input voltage amplitude judgment, the multi-crossings essentially result in additional switchings for the rectifier stage devices, specifically in the vicinity of sector transitions.

The phenomenon is exemplified in Fig. 4-8(a), where the input voltages $v_{a,A1}$, $v_{b,A1}$, and $v_{c,A1}$ of Module $A1$ in Fig. 4-3, as well as the gate signals $g_{1,A1}$ and $g_{3,A1}$ for rectifier stage devices $S_{1,A1}$ and $S_{3,A1}$ are shown for a certain period. The plot is derived under 60 Hz source voltage and 1080 Hz inverter stage switching frequency. In the center part of the figure, as $v_{a,A1}$ decreasing and $v_{b,A1}$ increasing, the two voltages come to their first intersection. Accordingly, device switchings take place in phases a and b and the dc-link voltage in the module transitions from $v_{ac,A1}$ to $v_{bc,A1}$, starting from where the inverter stage begins to take energy from phase b instead of a. In view of the fact that the filter capacitances are relatively small, the imposed load causes $v_{b,A1}$ to drop and crosses $v_{a,A1}$ again, leading to another round of device switchings in phases a and b, and forcing the dc-

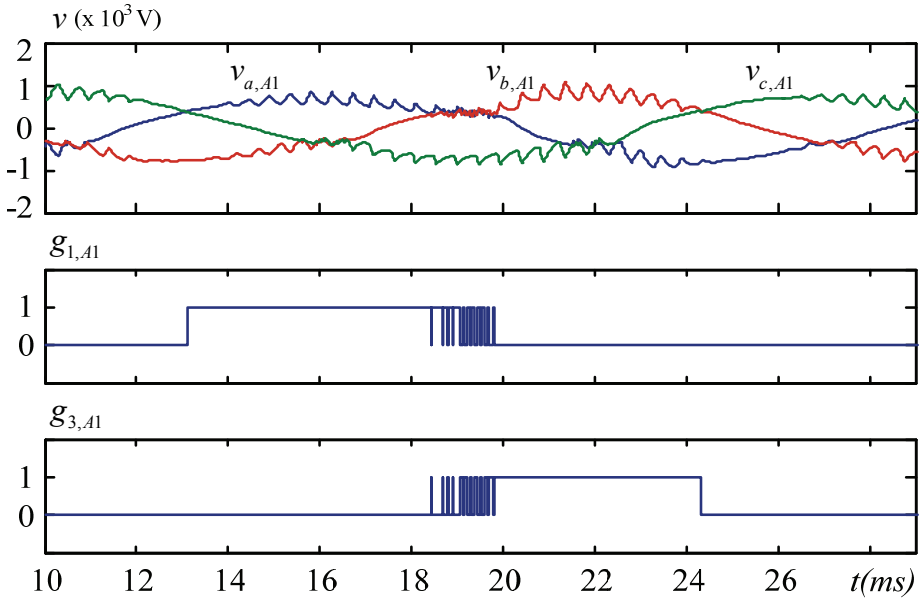
link voltage to transition back to $v_{ac,A1}$. Because the above-described process may repeat itself for a considerable number of times, a significant amount of additional switchings appear in the region as a result.

The extra device switchings are undesirable since they increase the rectifier stage switching frequency and introduce additional power losses. On the other hand, the extra switchings do have a positive effect on reducing the input voltage ripple magnitude during sector transitions and, therefore, help improve the output voltage/input current quality. To deal with the issue, the measured input voltages are passed through a second-order filter, the transfer function of which is given as,

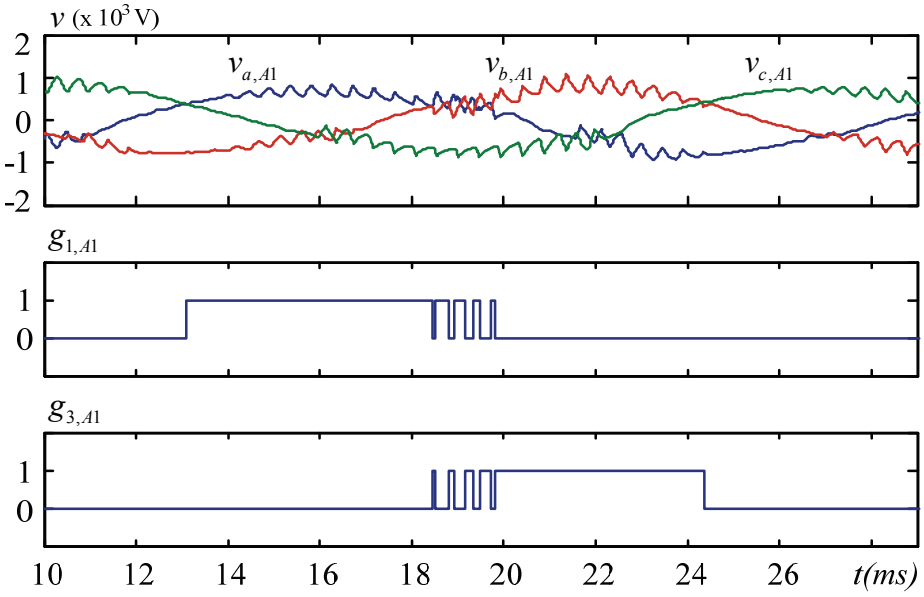
$$H_f(s) = \frac{K}{s^2/(2\pi f_c)^2 + s/(2\pi f_c Q) + 1} \tag{4.17}$$

where f_c is the cutoff frequency, Q is the quality factor and K denotes the filter gain. Assuming a unity Q, the phase angle delay introduced by the filter can be calculate by,

$$\theta(f) = -\arctan\frac{f/f_c}{1-(f/f_c)^2} \tag{4.18}$$



(a)



(b)

Fig. 4-8 Additional rectifier stage switchings caused by input voltage ripples. (a) Without filter. (b) With filter applied.

which needs to be compensated for the fundamental component. With the use of the filter, the amplitude judgment for the rectifier stage modulation is then performed on the filtered and compensated voltages. In order to achieve a balance between switching frequency and input/output waveform quality, a cutoff frequency of 2.5 KHz is selected for the filter. As shown in Fig. 7(b), after applying the filter, the number of additional switchings near the sector transition is substantially reduced.

4.3 Simulation Results

Table 4-1 System parameters of MMMC-II for simulation

System Parameter	Value
Rated Power	1 MVA
Grid Voltage (line-to-line, rms)	4160 V
Grid Voltage Frequency	60 Hz
Transformer Turns Ratio $N_P : N_S$	9 : 2
Inverter Stage Carrier Frequency f_s	1080 Hz
Total Line Inductance L_s (referred to the primary side)	0.08 pu
Filter Capacitance C_f	0.25 pu
Load Resistance R_L	0.9 pu
Load Inductance L_L	0.25 pu

To verify the proposed modulation scheme, a simulation model is built and tested in MATLAB/Simulink. In the simulation, the nine module MMMC-II circuit is supplied by

60 Hz grid voltage and is connected to a three-phase RL load. System parameters of the model are listed in Table 4-1.

Under 1080 Hz inverter stage switching frequency, the output voltage and current waveforms are shown in Fig. 4-9. The waveforms are obtained for an output frequency f_o of 40 Hz while the inverter stage modulation index m_a is set to 0.9. It can be seen that owing to the use of PS-SPWM, the output line-to-neutral and line-to-line voltages appear to be multi-stepped waveforms with decent quality. Because of the inductance in the load, the three-phase load currents are close to sinusoids with very low harmonic distortion.

Fig. 4-10 gives another set of output waveforms with the fundamental frequency changed to 80 Hz. With the use of PS-SPWM in the inverter stage, the output frequency, magnitude and angle can be arbitrarily adjusted by varying the reference waves for the PS-SPWM.

Fig. 4-11 illustrates the input side current waveforms of the converter. The first subplot exemplifies the input current waveform of a single MC module (phase $a1$ of Module $A1$) which contains chopped pieces from the load currents. Due to the filtering effect of the capacitors, the current in the corresponding secondary winding of the 18-pulse transformer, as shown in the second subplot, is much smoother but still contains significant harmonic components. However, because the inverter stage modulation imposes a balanced load sharing among modules in a same output phase, and with the rectifier stages of the modules emulating the voltage transfer characteristic of diode bridges, the harmonic elimination capability of the 18-pulse transformer is made good use of. Evident in the third subplot, the total input current on the primary side of the transformer is seen to be a sinusoid with low distortions. Additionally, although the proposed modulation does not control the input current angle, the line power factor is close to unity under medium to high load conditions.

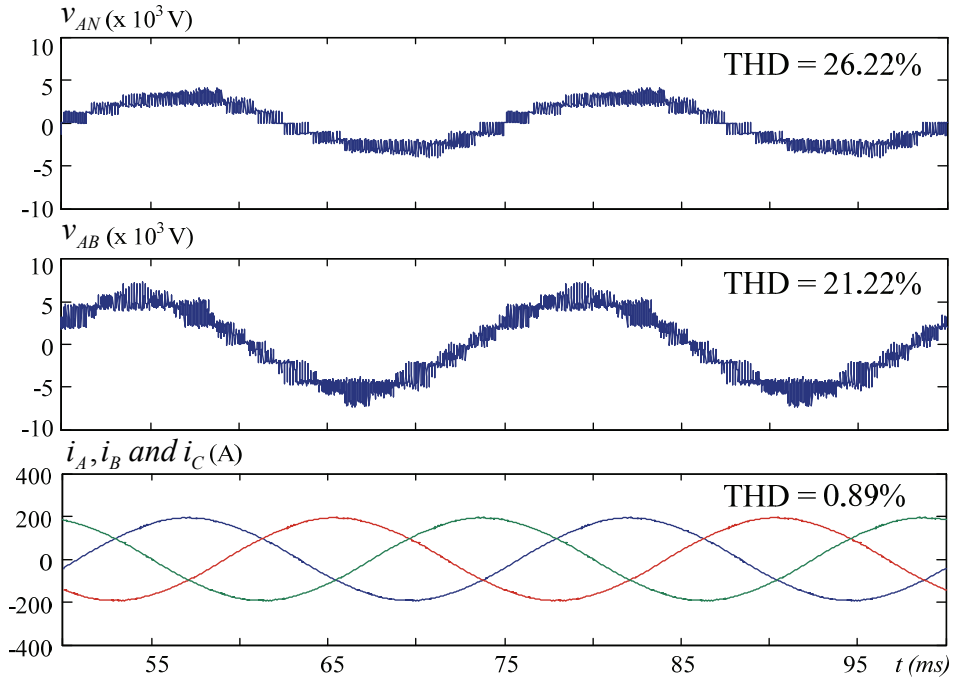


Fig. 4-9 Simulated output voltage and current waveforms of MMMC-II (f_o = 40 Hz, m_a = 0.9).

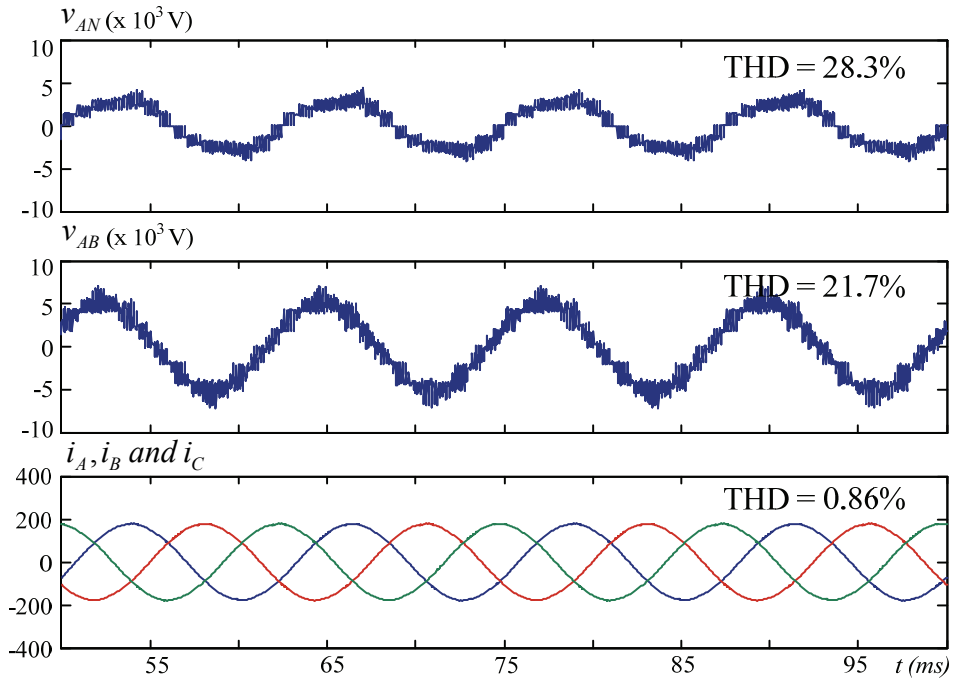


Fig. 4-10 Simulated output voltage and current waveforms of MMMC-II (f_o = 80 Hz, m_a = 0.9).

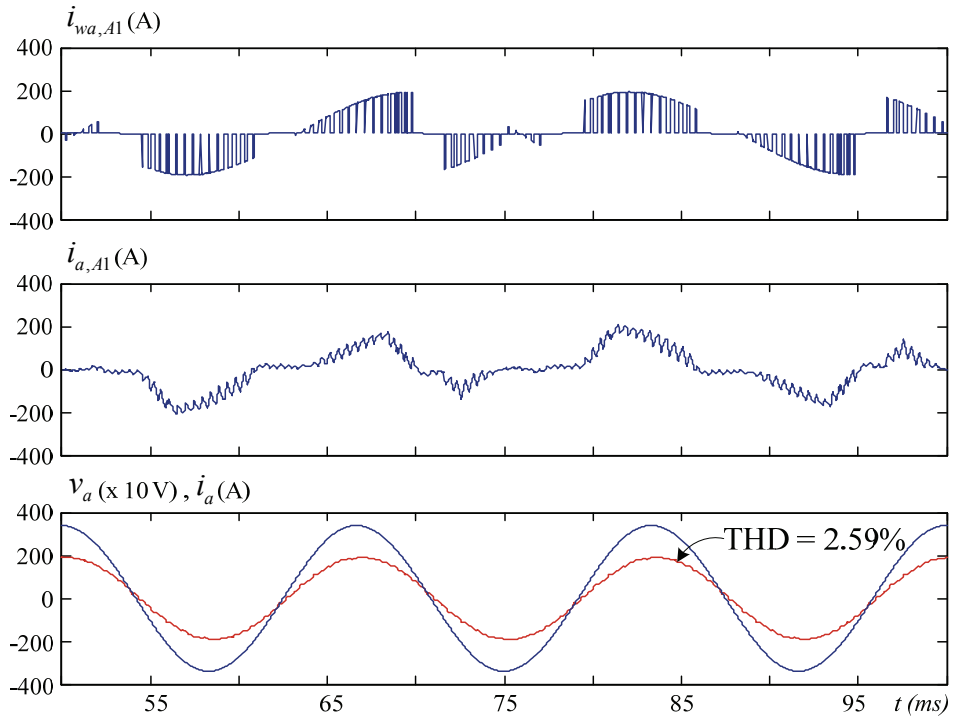


Fig. 4-11 Simulated input current waveforms of MMMC-II (f_o = 40 Hz, m_a = 0.9).

4.4 Experimental Verification

The proposed modulation scheme is also verified experimentally on the low-voltage prototype as described in Chapter 5. The prototype is composed of nine MC modules built with IGBT-diode pairs. Each module is equipped with sensor circuitry for input/output voltage/current measurement and field-programmable gate array (FPGA) devices for implementation of the modulation scheme, dispatching gate signals, interfacing the analog-to-digital converters, and handling other necessary tasks. Since the experimental MC modules are of the direct type, the gate signal mapping described in Section 4.2.5 is also realized in the FPGA. On the input side, the MC modules are fed by a group of three 18-

pulse phase-shifting transformers, which are put together to provide a total of nine secondary windings. As the transformers have a fixed turns ratio of 2 : 1, a variac is placed between the transformers and the 208 V / 60 Hz grid to provide the adequate voltage level. Same as the simulation, an RL is used as the load of the converter. Detailed experimental parameters are listed in Table 4-2.

Table 4-2 Experimental parameters of MMMC-II

System Parameters	Value
Rated Power	5 kVA
Grid Input Voltage (line-to-line, rms)	208 V
Input Frequency	60 Hz
Equivalent Transformer Turns Ratio $N_P : N_S$	9 : 2
Inverter Stage Carrier Frequency f_s	1080 Hz
Equivalent Total Line Inductance L_s	≈ 2 mH (≈ 0.087 pu)
Filter Capacitance C_f	66 μF (0.21 pu)
Load Resistance R_L	7.9 Ω (0.91 pu)
Load Inductance L_L	5 mH (0.22 pu)

Fig. 4-12 shows the experimental output voltage waveforms of v_{A1} and v_{AN} under no load condition. Although v_{A1} contains the six-pulse ripples introduced by the rectifier stage, v_{AN} is seen to be similar to Fig. 4-7 which is free of the low frequency ripples due to the 18-pulse transformer and has seven voltage levels.

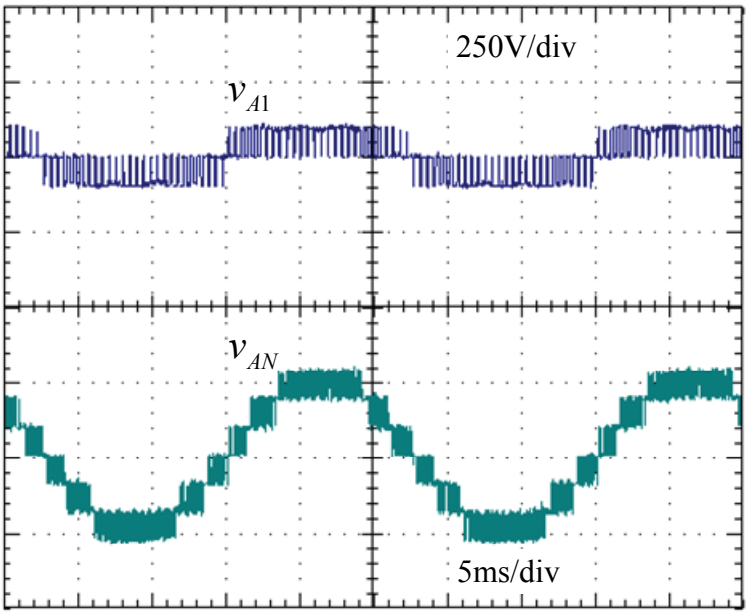


Fig. 4-12 Experimental output voltage waveforms of MMMC-II under no load condition.

Fig. 4-13 and Fig. 4-14 present the load side waveforms of the MMMC for output frequencies of 40 Hz and 80 Hz. Under both frequencies, the experimental waveforms of the line-to-neutral voltage v_{AN}, line-to-line voltage v_{AB} appear to have multilevel waveform shapes and resemble their simulation counterparts well. Due to the inductance in the load, the load current i_A possesses a smooth sinusoidal waveform.

The input side current waveforms are shown in Fig. 4-15, where the secondary winding current i_{a1} from module $A1$ can be noticed to contain significant harmonic distortions. However, the total input current i_a at the grid connection point has a good sinusoidal waveform, which proves the fact that although the input current is not controlled by the proposed modulation scheme, sinusoidal input currents can still be achieved by taking advantage of the harmonic elimination capability of the 18-pulse phase-shifting transformer.

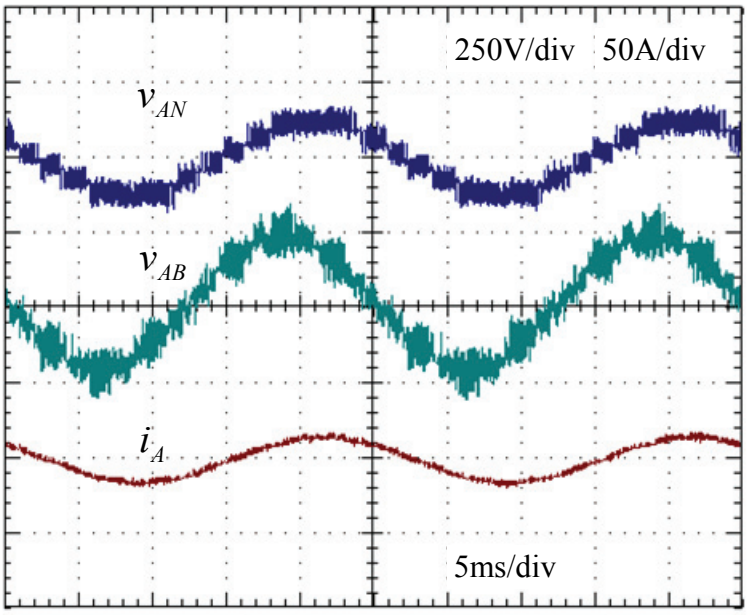


Fig. 4-13 Experimental output voltage and current waveforms of MMMC-II (f_o = 40 Hz, m_a = 0.9).

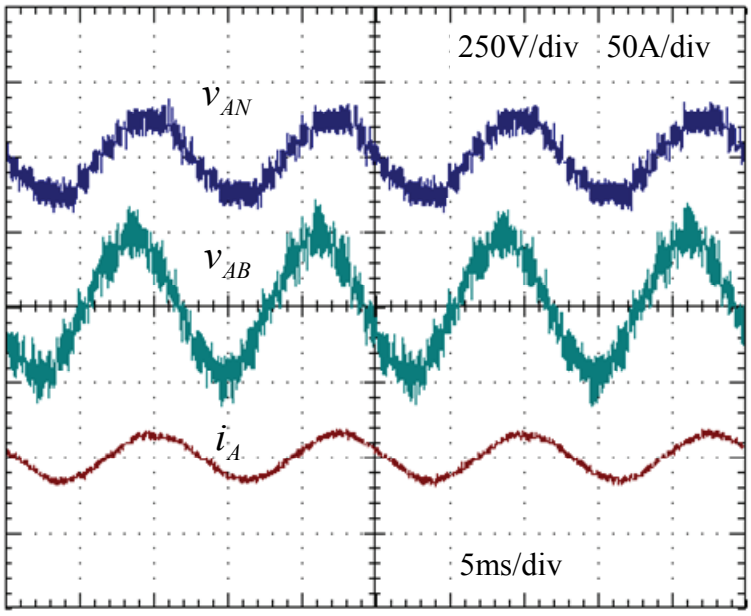


Fig. 4-14 Experimental output voltage and current waveforms of MMMC-II (f_o = 80 Hz, m_a = 0.9).

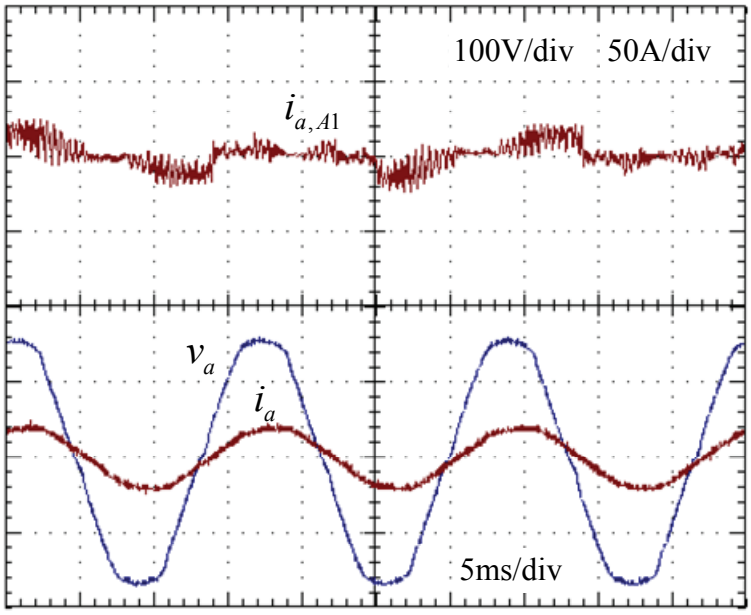


Fig. 4-15 Experimental input side waveforms
(f_o = 40 Hz, m_a = 0.9).

4.5 Summary

The MMMC topologies are a combination of cascaded converter structure and 3 x 2 matrix converter modules. This chapter presents a new and simple modulation scheme for the MMMC-II fed by a phase-shifting input transformer. The method is established by modeling the MC modules indirectly and using their rectifier stage to emulate the voltage transfer characteristic of a three-phase diode bridge, while applying the well-known phase-shifted modulation scheme to the inverter stage. On the output side, the magnitude and angle can be freely adjusted by the inverter stage modulation. On the input side, although the modulation does not involve input current synthesis, sinusoidal input current waveforms can still be obtained, which is owing to the harmonic elimination capability of the phase-shifting transformer.

Compared with the previously developed modulation schemes for the MMMC, the new modulation scheme is simpler, more straightforward, and associated with lower switching losses. Its features enable the use of an indirect module structure which does not need the complicated bidirectional switch realization and device commutation control in direct matrix converters, and significantly reduces the total number of switches required. The main limitation of the scheme lies in its lack of input power factor control capability.

Chapter 5

Experimental Platform Implementation

In order to provide experimental verification of the proposed modulation schemes, a low-voltage prototype of the multimodular matrix converters (MMMCs) has been implemented in the lab. All experimental results presented in the previous chapters are obtained from the prototype supplied by 208 V / 60 Hz grid voltage. For validation of modulation schemes on MMMC-II, a total of nine 3 x 2 matrix converter (MC) power modules has been constructed and assembled to collectively produce multilevel output waveforms. Fig. 5-1 shows the simplified schematic of the experimental setup, and a picture of the real platform is given in Fig. 5-2, which consists of three input phase-shifting transformers, a variac to offer the adequate input voltage level, nine MC power modules distributed in the three output phases, and an RL load. The phase-shifting transformers used in the experiment has only three secondary winding sets each, therefore, three such transformers are needed to provide nine secondary windings for the MMMC-II, while all the primary windings are connected in parallel for the line-side currents to add up. Since each transformer has a fixed primary to secondary turns ratio of 2 : 1, a variac is inserted between the transformers and the grid to adjust the input voltage magnitude. For experiments of the MMMC-I, only the three MC modules ($A2$, $B2$, and $C2$) fed by the zero degree secondary windings are used; the other modules are disconnected in this case.

This chapter provides detailed explanation of the major components constituting the low-voltage experimental platform for verifying the proposed modulation schemes for the MMMC topologies. The MC module construction, voltage and current sensor circuits, bidirectional device commutation, module coordination and communication will be described in the following sections, respectively.

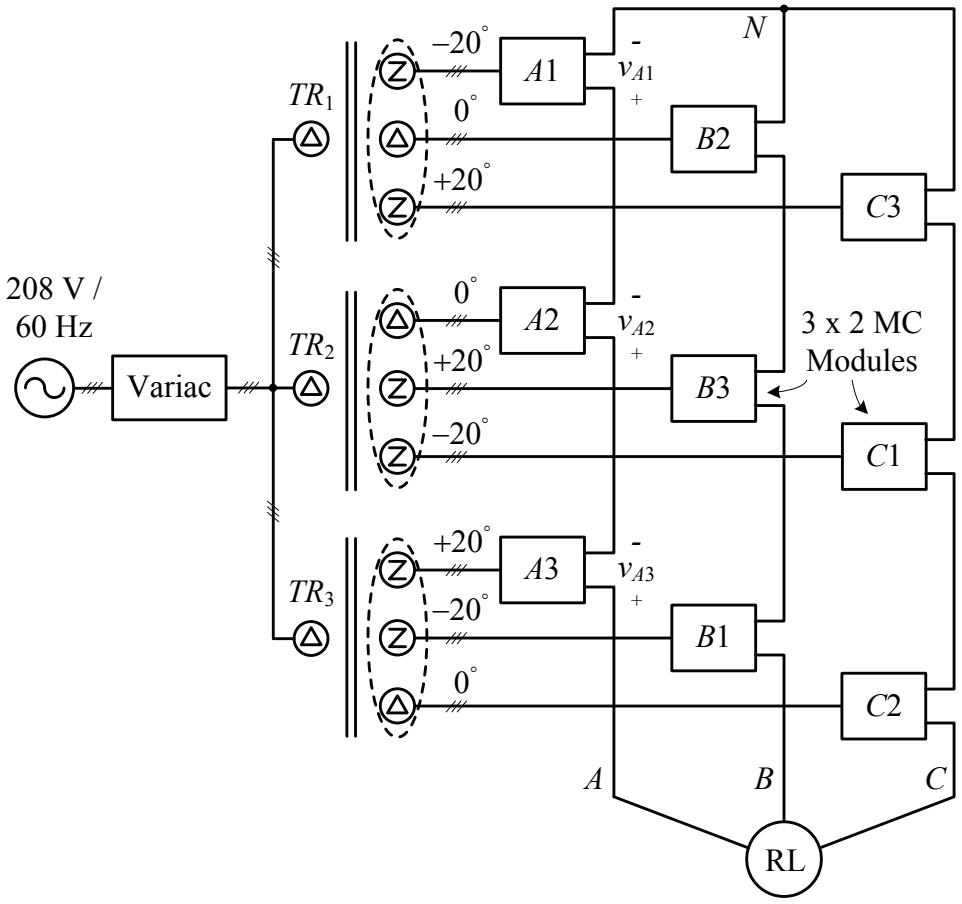


Fig. 5-1 Structural diagram of the low-voltage experimental setup.

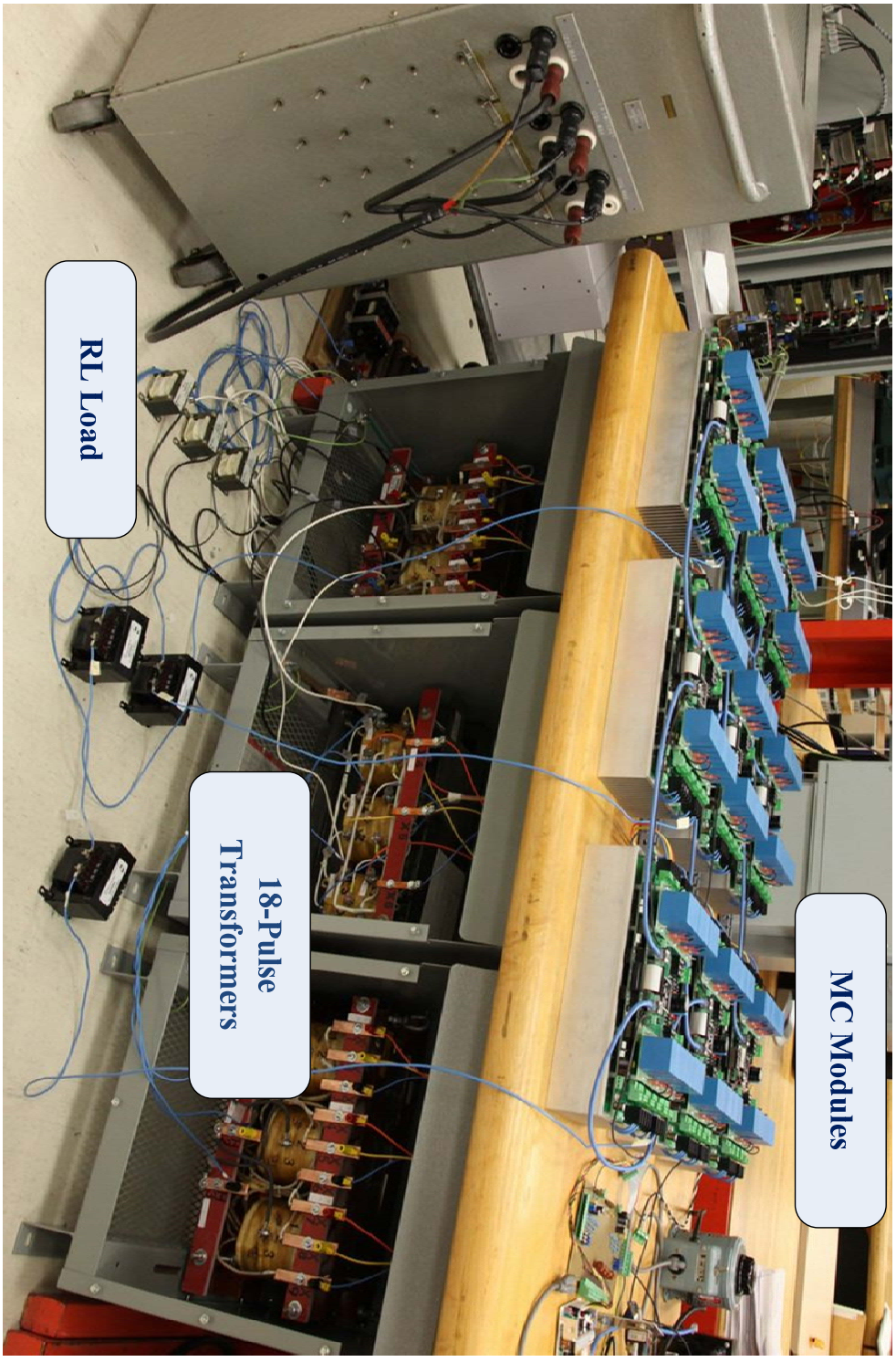


Fig. 5-2 Low-voltage experimental setup of the MMMC.

5.1 Construction of 3 x 2 MC Power Modules

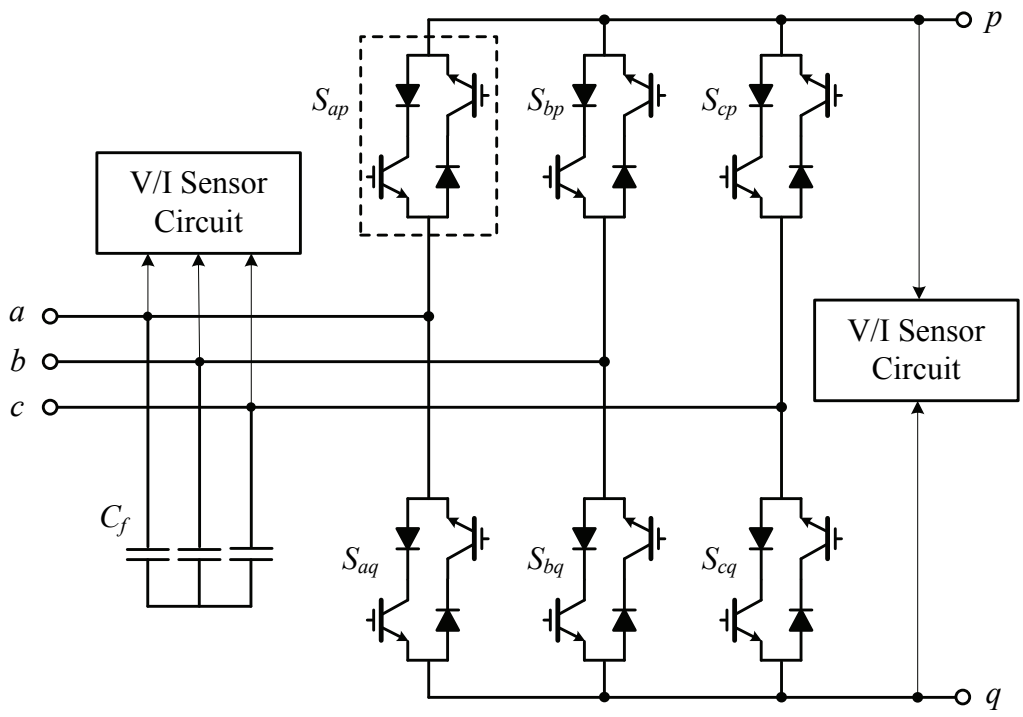


Fig. 5-3 Construction of the experimental 3 x 2 MC module.

Fig. 5-3 illustrates the experimental construction of the 3 x 2 MC modules. The bidirectional switches linking the input and output ports of the modules are realized by the anti-parallel connection of a pair of series-connected IGBT and diode (IRG7PH42U and DSEP60-12A). Fig. 4-1 shows the gate driving structure of a single bidirectional switch. Each IGBT device is equipped with an independent gate driver circuit supported by an isolated power supply sourcing energy from the main auxiliary power source. The gate driver circuit is built around an optocoupler IC (HCPL316J) which provides internal galvanic isolation between the power side and the signal side. The gate signals are delivered by a field programmable gate array (Altera Cyclone EP1C6) to the gate drivers, and in the meantime, diagnostic signals from the gate drive circuit are also fed back

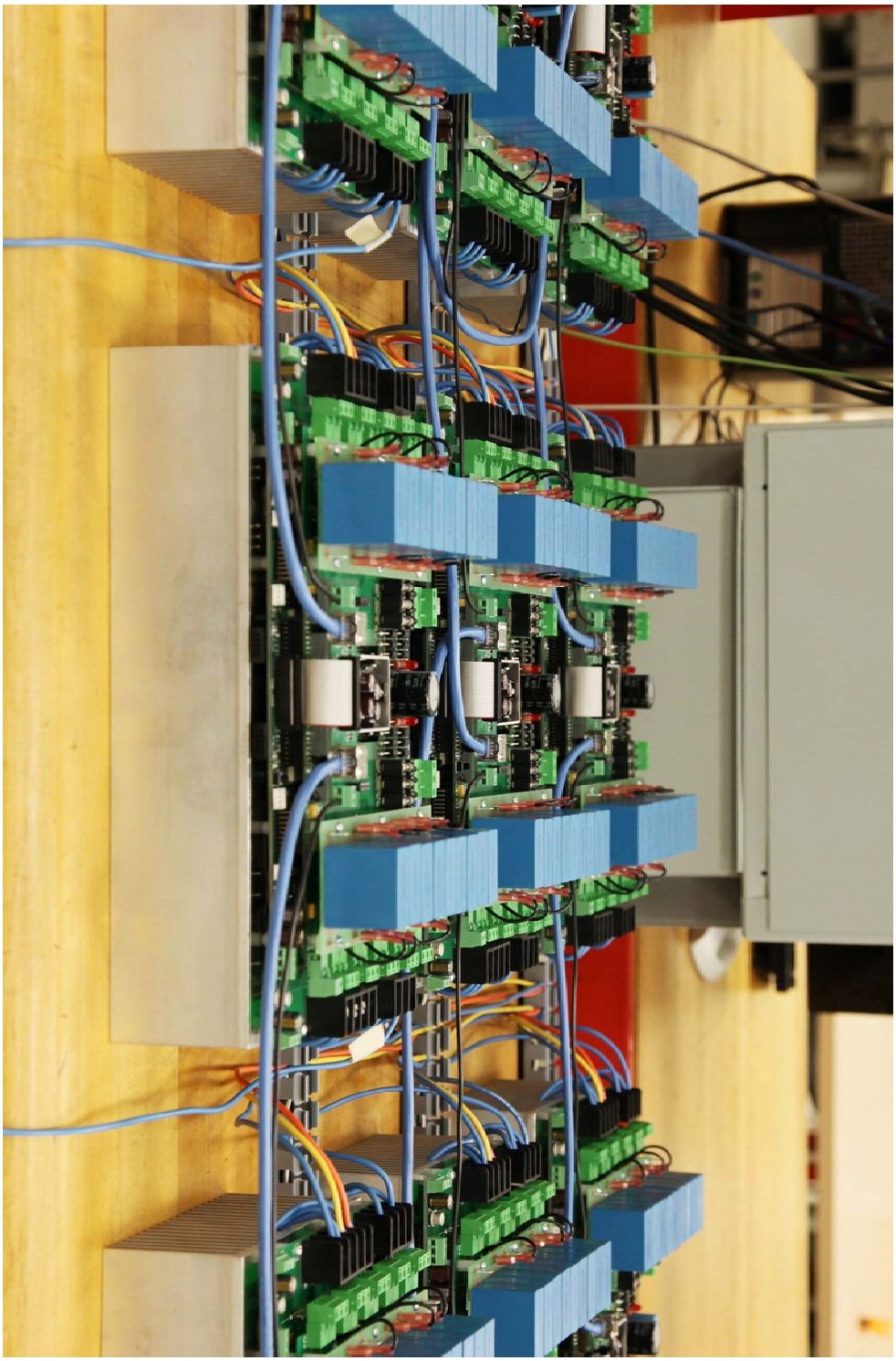


Fig. 5-4 Top-front view of the experimental MC modules.

to the FPGA for fault detection. By providing separate gate signals for the two IGBTs in a bidirectional switch, current flow in the switch can be controlled at will and, therefore, multistep device commutation between different phases can be achieved.

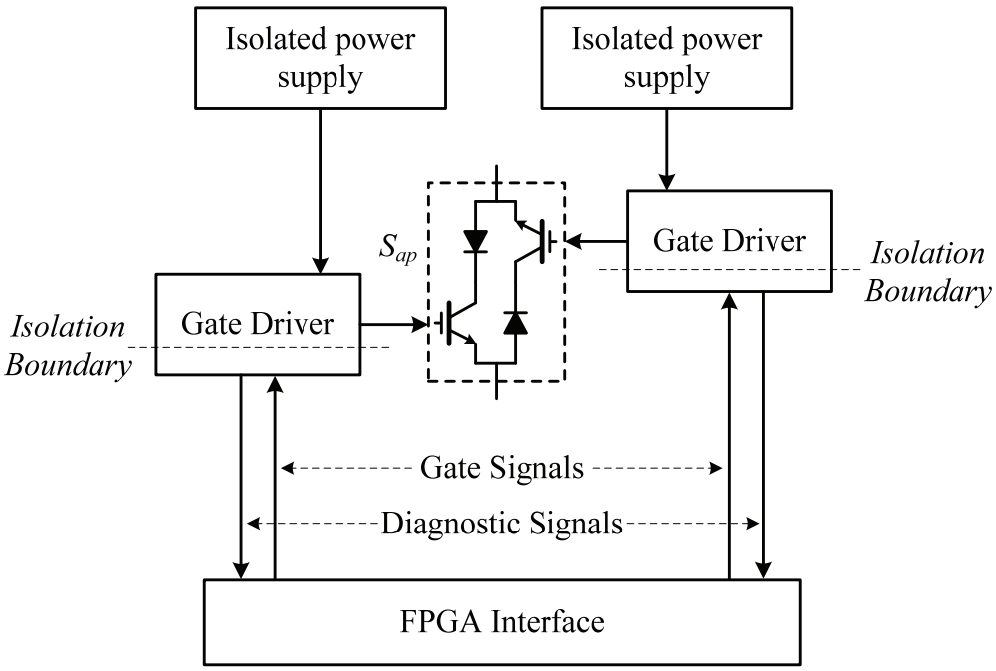


Fig. 5-5 Gate driving of the bidirectional switches.

At the input ports of each MC module, a set of three-phase film capacitors are mounted as the input filter. In addition, voltage and current sensing circuit are implemented to measure the polarity and magnitude of the input voltages and currents. The same circuit are installed at the single-phase output ports as well for measuring output voltages and currents, which are essential to the realization of device commutation algorithm.

5.2 Voltage and Current Measurement

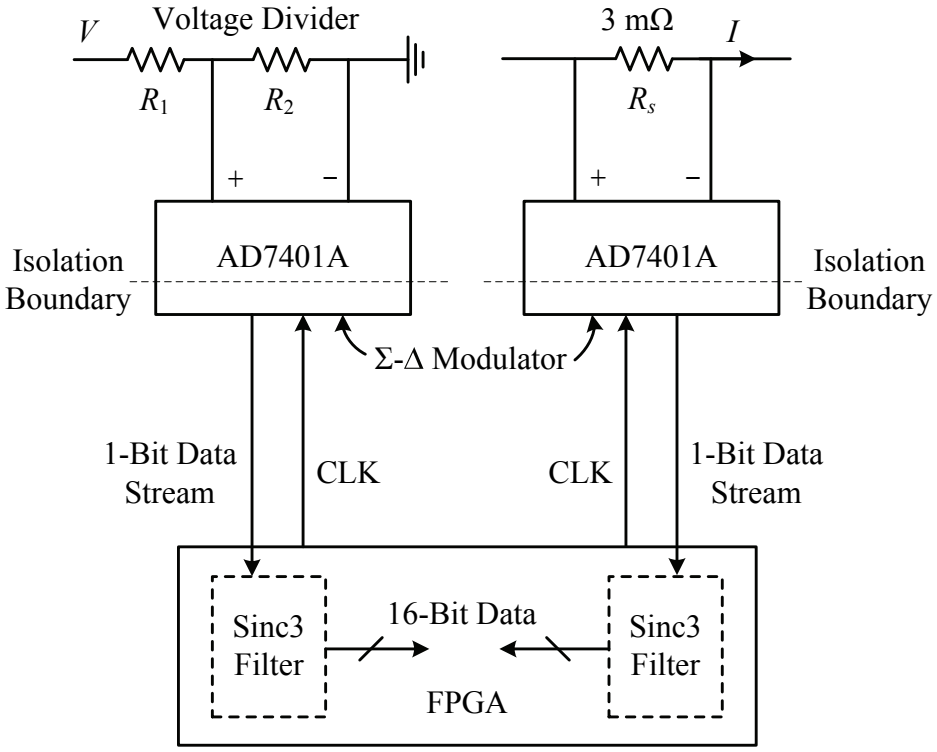


Fig. 5-6 Voltage and current measurement using isolated 1-Bit Σ-Δ Modulator.

The MMMC modulation schemes as well as the bidirectional switch commutation require voltage/current information from the sensing circuit. As mentioned earlier, the sensing circuit is implemented at both input and output ports of each 3 x 2 MC module. Core to the measurement circuit is an isolated Sigma-Delta modulator IC (AD7401A) which accepts a differential ±250 mV analog voltage input and converts it into a high-speed 1-bit data stream. As shown in Fig. 4-4, the input/output voltages of the MC module are scaled down using a voltage divider before being passed to AD7401A; whereas for current measurement, a 3 mΩ sensing resistor is employed to convert the measured current into the

acceptable voltage range. It is worth mentioning that the modulator IC possesses an on-chip internal isolation and therefore provides insulation for the digital circuit from the power circuit (5000 V minimum). The clock signal (up to 20 MHz) required by the operation of the modulator on the digital side is provided by the FPGA. The data bits are clocked out on the rising edges of the clock signal and transmitted to the FPGA, and passed through a low-pass Sinc3 digital filter. At the output of the filter the 16-bit digital data of the voltage or current is obtained which can be utilized by the other function modules.

5.3 Commutation Control of the Bidirectional Switches

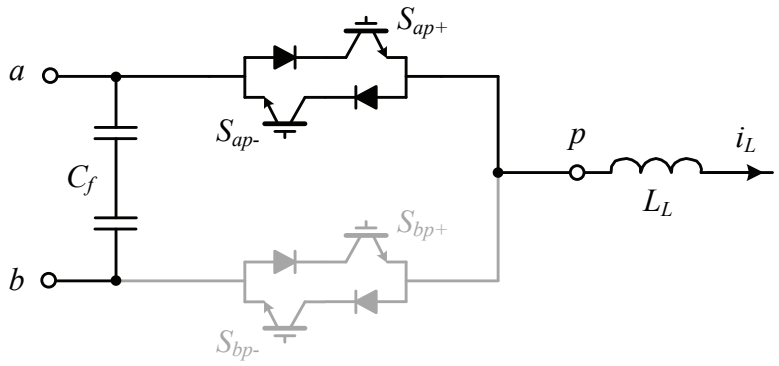


Fig. 5-7 Initial state of output port *p* connected to input phase *a*.

Due to the use of bidirectional switches involving devices connected in anti-parallel, the current commutation between different phases should be properly handled, such that during commutation transients, the switching constraint in the MC module is not violated. Unlike

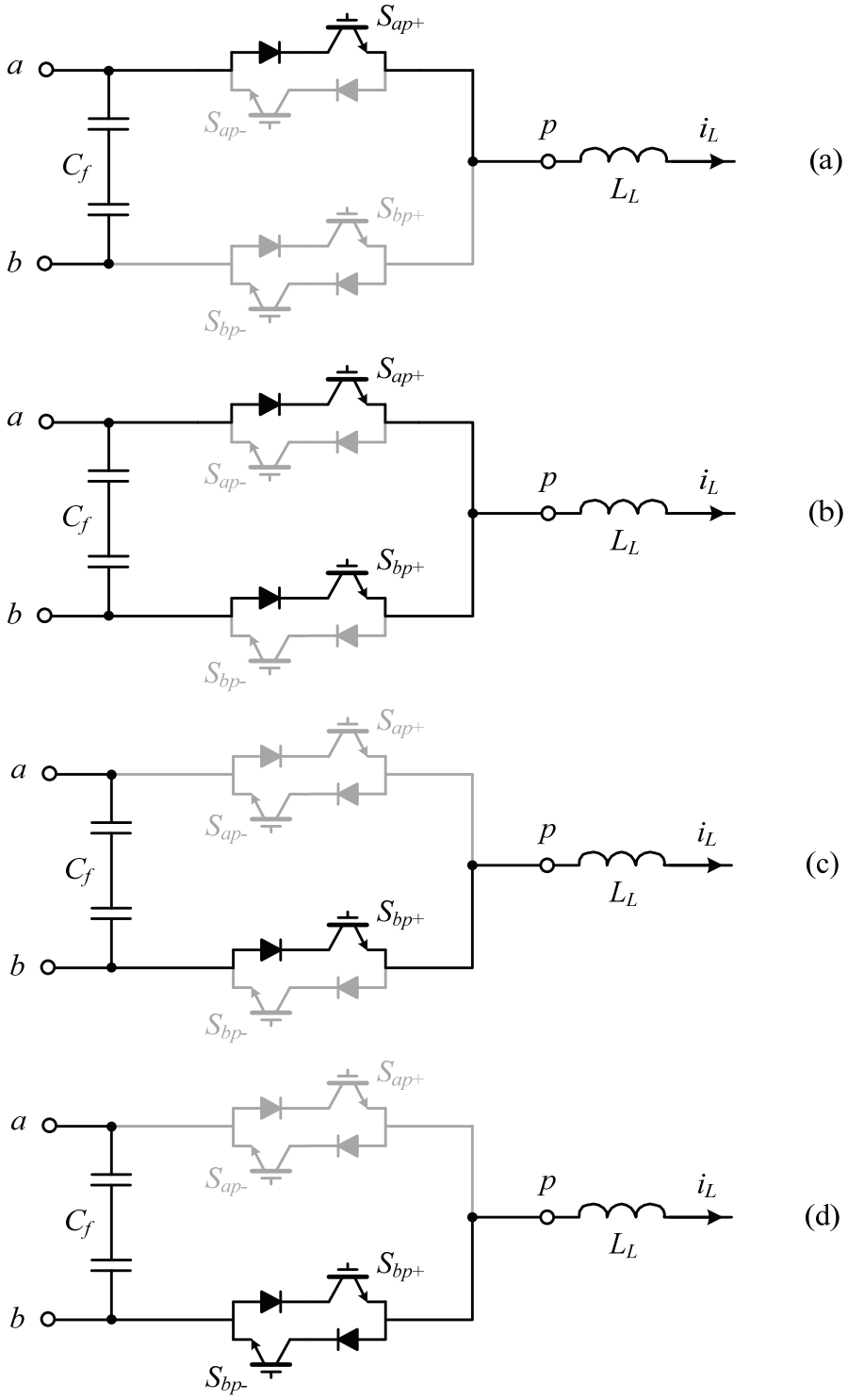


Fig. 5-8 Four-step device commutation based on load current direction. (a) Step 1. (b) Step 2. (c) Step 3. (d) Step 4.

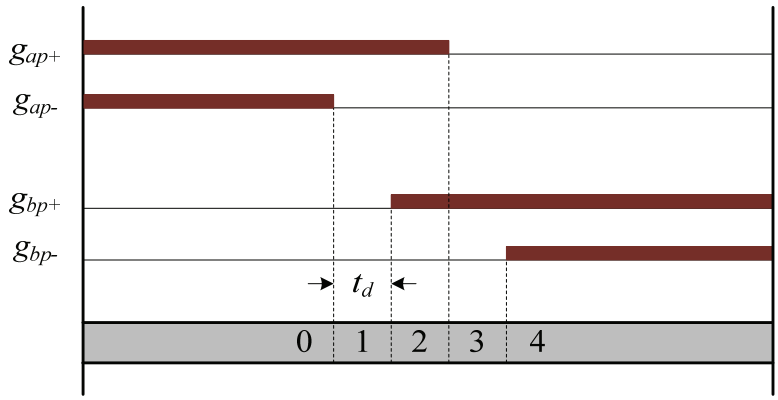


Fig. 5-9 Gate signals during the four-step device commutation.

voltage-source converters where dead-time can be inserted during commutation and current-source converters that can adopt gate signal overlaps, the MC modules have to employ a multistep commutation technique based on the load current and/or input voltage information to avoid detrimental short-circuit of the filter capacitors and open-circuit of the inductive load. For the experiments of the MMMCs, a four-step load current based commutation technique is implemented in the FPGA. The entire commutation process is illustrated from Fig. 4-5 to Fig. 5-9. Assuming the load current i_L at output port p is positive at the beginning, Fig. 4-5 shows the initial state of the circuit in which the load current is about to be commutated from input phase a to phase b. At this moment, both S_{ap+} and S_{ap-} are turned ON; but owing to the load current direction, S_{ap+} is the actual device that carries current. In Fig. 5-8 the four-step process is illustrated in detail. Before turning ON the incoming current carrying device in phase b (S_{bp+}), the device S_{ap-} not carrying current in the phase a bidirectional switch should be turned OFF first, as shown in Fig. 5-8 (a); otherwise, S_{ap-} and S_{bp+} would provide a short-circuit path for the input capacitors and cause harm. Subsequently, S_{bp+} is turned on to establish the current path for i_L in phase b; this is done prior to the turning OFF of S_{ap+} to provide a short overlap period and guarantee the continuity of the load current. The actual current is commutated from phase a to phase b

right after S_{bp+} is ON or S_{ap+} is OFF, depending on which input voltage is greater in magnitude. In the last step as shown in Fig. 5-8 (d), S_{bp-} is also turned ON to allow reverse load current flow, and the whole commutation process is finished.

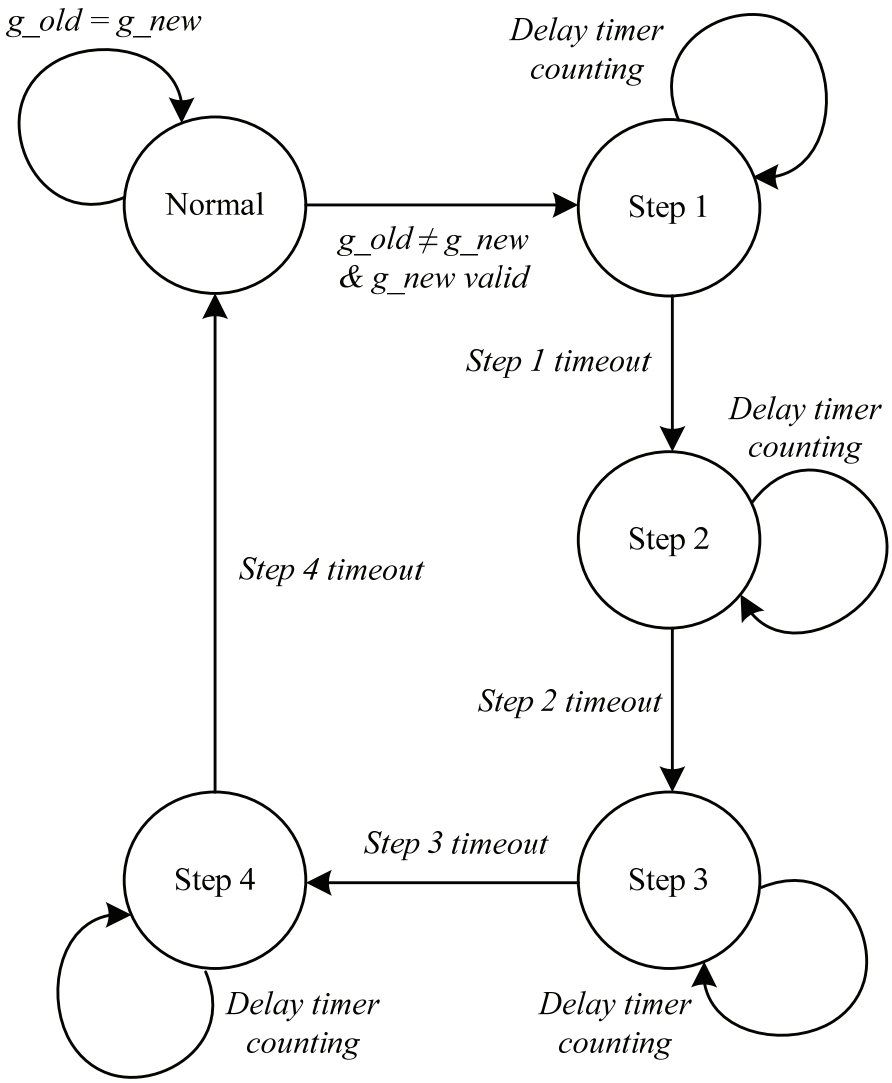


Fig. 5-10 FPGA finite state machine implementation of the four-step device commutation.

Fig. 5-9 shows the gate signals generated for the four devices involved during the commutation. It can be seen that each step lasts a period of t_d, which is settable in the FPGA to ensure complete turning ON and OFF of the IGBTs. The commutation program is implemented in the FPGA using a simple finite state machine as shown in Fig. 5-10. In the normal state, the commutation module accepts the original gate signals from the modulation program and compares it with the old one. If a change in the original gate signals is detected indicating that commutation is necessary, the commutation program will go through the four-step process and output corresponding final gate signals to control the IGBTs. During the entire process, the load current direction information is also fed into the commutation module for determining the right sequence.

5.4 Module Synchronization, Communication and Protection

In the experimental setup, each MC module is responsible for generating gate signals for its own on-board devices, therefore, it is required that all the modules are synchronized and coordinated for implementation of the proposed modulation schemes. With the equipped FPGAs, synchronization and serial data communication functions are implemented, and the signals are transmitted through a low-voltage differential signaling (LVDS) channel carried by category-5 network cables. It is worth mentioning that the FPGAs are operated at a basic clock frequency of 150 MHz, and the serial communication reaches a high baud rate of 37.5 MHz.

Moreover, protection measures are also implemented on each module to avoid harmful effects to the switching devices. Besides functions provided by the gate drivers, an overvoltage protection circuitry is placed at the output port of each module, which includes a metal oxide varistor (MOV) and a thyristor based crowbar controlled by a voltage comparator circuit monitoring the output voltage. In case an overvoltage happens, the

protection circuit functions immediately and provides a bypass current path, such that the devices voltage will not exceed the upper limit.

5.5 Summary

A low-voltage experimental platform has been built in the lab to verify the MMMC modulation schemes presented in the last chapters. The prototype is composed of nine 3 x 2 MC power modules, three 18-pulse phase-shifting transformers for feeding the modules, an input variac, and supplies a three-phase RL load.

The bidirectional switches in the MC modules are realized by anti-parallel connection of IGBT-diode pairs, with the IGBTs operated by separate gate drivers. The gate driving circuitry is built around an optocoupler driver IC with diagnostic and fault protection features. In each MC module, voltage and current measurement circuit are available at the input and output ports. The measurement circuit is implemented using an isolated Sigma-Delta modulator which converts the differential voltage input into a 1-bit high-speed data stream. The data stream is fed into the FPGA and passed through a digital filter for 16-bit data output. Also with the FPGA, the load current based four step method is implemented to control the commutation of the bidirectional switches. As a result, safe current commutation avoiding input voltage short-circuit and load current interrupt is successfully achieved. All the modules are equipped with synchronization, communication, and protection features, and are used to produce the final output waveforms collectively.

Chapter 6

Conclusions

Over the past decades, various high-power converter topologies were invented and extensively investigated for medium-voltage drive applications. However, of all the topologies that have been proposed in the literature, only a small portion have successfully entered and thrived on the commercial market. As one of the newly emerged MV converter candidates, the multimodular matrix converter (MMMC) is among the few that have found industrial presence so far. The MMMC topologies are composed of a multiple number of 3 x 2 matrix converter (MC) modules. And they are essentially a combination of structures of the conventional matrix and multilevel converters. Owing to the fact that modulation for the MMMCs cannot directly adopt existing schemes for either the conventional MC or the dc-link based multilevel converters, it is necessary to develop new schemes particularly suited for the MMMCs for generating sinusoidal input and output quantities with variable amplitude and frequency.

This dissertation is mainly focused on the development of modulation schemes for the MMMC topologies. Several different schemes, along with the relevant switching patterns, have been proposed and studied in the last chapters. All the results were supported by verifications from both simulation and experiment. The experimental validations are carried out on a low-voltage lab prototype fed by the grid voltage.

6.1 Main Contributions and Conclusions

The main contributions of the work are concluded as follows.

1) Developed a direct transfer matrix based modulation scheme for the MMMCs. The scheme is capable of producing sinusoidal waveforms at both input and output ports of the converters, with the frequency, amplitude and angle on both sides of the converters all adjustable.

It is identified that for synthesis of the input sinusoidal currents, different MC modules should be taken as an integral and coordinated in the modulation program. Consequently, although the secondary winding currents of the input isolation transformer still contain distortions, the total grid-side current as a sum of the input currents from different modules can possess a sinusoidal shape. For higher level MMMCs with more than two modules in series on each output phase, phase displacement among the module switching periods is necessary for the generation of multilevel waveforms with improved quality.

2) Established an indirect circuit model for the MMMCs consisting of virtual rectifier and inverter stages, based on which an indirect space vector based modulation scheme is developed. A new switching pattern producing superior waveform quality comparing to the conventional pattern is also proposed.

If viewed from a certain perspective, the MMMC topologies may still adopt the fictitious dc-link concept and be divided into virtual stages of a rectifier and an inverter. The rectifier stage is commonly shared assuming the input side of the modules is operated synchronously. For the output voltage synthesis, either a two-level or a three-level space vector diagram can be employed for duty ratio calculations. Finally, output pulses are generated according to two switching patterns. The proposed new pattern featuring split

negative half-cycle pulses is able to yield better harmonic performance than the conventional one.

3) Proposed a simple and straightforward modulation scheme for higher level MMMCs fed by a phase-shifting transformer. This method is a combination of diode front-end emulation and phase-shifted sinusoidal PWM. The fact that it can be applied to physically constructed indirect MC modules leads to reduced part count, gate supplies/drivers, and avoids the complexity involved in device commutations since only unidirectional switches are employed. At a much lower switching frequency, the new method is able to provide waveform quality on par with those from the previous strategies. The benefits associated with the new scheme are obtained at the expense of sacrificing input power factor adjustment capability.

The proposed scheme takes advantage of the indirect construction of the MC modules. By emulating the voltage transfer characteristics of the diode rectifier, the method ensures positive dc-link voltage polarity, and therefore allows the use of MC modules built with unidirectional devices only. This modulation relies on the phase-shifting transformer which plays an important role in output and input waveform quality improvement. Method for reducing additional switchings caused by input voltage ripples is also presented.

4) Constructed a complicated low-voltage prototype of the MMMC topology, on which the proposed modulation schemes are successfully verified. The prototype is composed of nine MC modules that are scaled-down versions of the simulated system. Each module is equipped with bidirectional switches, isolated gate drivers, voltage/current sensors, protection circuits, and FPGAs for implementing modulation program and handling necessary auxiliary tasks. Synchronization and communication functions are also realized among different modules.

6.2 Suggested Future Work

Based on the existing platform, possible future research can be carried out in the following directions.

1) Explore other possible modulation and control methods for the MMMCs and compare performances of different methods. New candidate methods such as model predictive control can be applied and investigated. In addition, comprehensive evaluation and quantitative comparison of existing schemes in terms of harmonic profile, switching frequency, semiconductor losses may further help to reveal the benefits and limitations associated with the respective methods, and identify the optimized scheme corresponding to particular working conditions.

2) Address issues related to unbalanced input voltage and/or fault conditions. If the input voltage or load is not three-phase balanced, special measure should be taken for the modulation schemes to perform properly. It would be then necessary to invent and investigate possible methods to compensate for the unbalances and maintain satisfactory performance of the modulation schemes.

3) Study methods to suppress resonances caused by filter capacitors and input inductances. Due to the existence of the filter capacitance in each MC module, resonances could be triggered on with the line and leakage inductances. The excited ripples can have negative effects on the modulation and degrade the waveform quality. To address this issue, suitable damping strategies may be employed to counteract the resonances and help improve the modulation performance.

Appendix I

Per-Unit System Calculation

In the per-unit representation of an electrical power conversion system, the base values are calculated according to the given rated power S_R, rms line-to-line voltage V_{LL}, and base frequency f_B. Assume we have a system with a rated power of 1 MW and line-to-line voltage of 4160 V/ 60 Hz, the values are calculated as follows

$$V_B = V_{LL} / \sqrt{3} = 4160 / \sqrt{3} = 2401.78\,\text{V} \tag{I.1}$$

$$I_B = S_R / \left(3V_B\right) = 1e6 / \left(3V_B\right) = 138.79\,\text{A} \tag{I.2}$$

$$Z_B = V_B / I_B = 17.31\,\Omega \tag{I.3}$$

$$\omega_B = 2\pi f_B = 2\pi \times 60 = 377\,\text{rad/s} \tag{I.4}$$

$$L_B = Z_B / \omega_B = 45.9\,\text{mH} \quad \text{and} \quad C_B = 1 / \left(\omega_B Z_B\right) = 153\,\mu\text{F} \tag{I.5}$$

Therefore, a 0.9 pu resistance in such a system would be

$$Z = 0.9 Z_B = 0.9 \times 17.31 = 15.58\,\Omega \tag{I.6}$$

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