HIGH EFFICIENCY HIGH POWER DENSITY ISOLATED MATRIX-TYPE RECTIFIER FOR TELECOM AND DATA CENTER APPLICATIONS

By

Jahangir Afsharian

B. Sc., Ryerson University, Toronto, Canada, 2005
M. A. Sc., Ryerson University, Toronto, Canada, 2009

A dissertation
presented to Ryerson University

in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy
in the program of
Electrical and Computer Engineering

Toronto, Ontario, Canada, 2019

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Jahangir Afsharian

Doctor of Philosophy
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Abstract

With the fast development of information technology (IT) industry, the demand and market volume for off-line power supplies keep increasing, especially those for telecommunication, computer servers and data centers. As the capital expenditure was measured by the square footage occupied rather than power consumption, the development of high power density converter system is of greater interesting. The rising energy prices have resulted in the cost of power and cooling exceeding the purchase cost in less than two years. Therefore, highly efficient power conversion is required for the power converter system. Generally, the power supply unit (PSU) for power distribution system (PDS) in data center and telecom are the standard two-stage approach which normally consists of power factor correction (PFC) circuit and isolated DC-DC converter. The two-stage power conversion has demonstrated excellent performance and high reliability, since the design can be optimized for each stage. However, limitations to prevent the existing two-stage PSU to fulfill future requirements for the PDS in data center and telecom applications are revealed, and a very promising and fundamentally different approach with the single-stage isolated converter is proposed in this dissertation.

The development of single-stage converters with the option of placing the energy storage outside of the PSU creates new degrees of freedom regarding e.g. simplified rectifier racks in telecom and data center. This provides tangible benefits in the form of space saving, better

airflow for power unit in rectifier racks and improved lifespan. The three-phase isolated buck matrix-type rectifier, capable of achieving high power density and high efficiency, is identified as an excellent candidate for the medium power level (5 kW~10 kW) single-stage power supply design. Nevertheless, the matrix-type rectifiers are known for their relatively complex modulation and commutation techniques, and lack of ride-through capability such as the stringent case of one phase loss operation.

This dissertation work provides comprehensive study on the commutation method and modulation scheme design for the isolated buck matrix-type rectifier. It aims to analyze the operation principle of the rectifier and propose viable modulation and commutation schemes for this rectifier under both three-phase and single-phase operation. The method is verified by the hardware experiments of the PSUs with high efficiency (> 98%) and high power density (> 70 W/in^3) for 54 V and 380 VDC applications. The prototypes demonstrated in the experiments show the effectiveness of the proposed modulation and commutation schemes for industry.

Dedicated to the memory of my father and my brother.

Acknowledgement

I would like to express my deep gratitude to my supervisor, Professor David Xu, for his support and help during my graduate studies at Ryerson University. His valuable advice and guidance has greatly enhanced my academic knowledge, scientific inspiration and practical skills.

I would also like to thank my previous supervisor Dr. Bin Wu who taught me how to conduct independent research, and for his attitude toward research and research methodologies, which can be applied to all aspects of life and will benefit me for the rest of my life.

My appreciation also goes to Dr. Dushan Boroyevich at CPES (Center for Power Electronics Systems) in Virginia Tech University, for his valuable discussion on my research topic.

I would also like to thank the committee member, respected professor Dr. Fred C. Lee, for his valuable questions, feedback, and time.

Thanks are extended to the rest of members of my thesis defense Dr. Vadim Geurkov, Dr. Amirnaser Yazdani and Dr. Bala Venkatesh.

I am grateful to fellow workers at Murata Power Solutions for their support and funding on building prototypes.

Finally, I wish to share my achievements with my family for their endless love and support.

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Acronyms

CRM	Critical-Conduction-Mode
DCM	Discontinuous-Conduction-Mode
EMI	Electromagnetic Interference
FB-PS	Full-Bridge Phase-Shifted
FPGA	Field Programmable Gate Array
GaN	Gallium-Nitride
IGBT	Insulated Gate Bipolar Transistor
PSU	Power Supply Unit
PDS	Power Distributed System
PDU	Power Distribution Unit
PWM	Pulse-Width Modulation
SiC	Silicon Carbide
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Chapter 1

Introduction

With the explosive development of information technology, the communication and computing systems, such as data centers, telecoms, and servers have become a large market for the power supply industry. In a typical data center, less than half of the energy consumed is delivered to the compute load, which includes microprocessors, memory and disk drives. The rest of the power is lost in power conversion, distribution, and cooling, resulting in high utility bills, a large environmental footprint and the inability to fill equipment racks [1]. Power savings in the power distribution system (PDS) result in further savings in the facility cooling system, because less heat is generated in the distribution and therefore less heat has to be cooled [1, 2]. Cooling is often the limiting factor in data center capacity (heat removal can be a bigger problem than getting power to the equipment) [3, 4]. Over the past decade energy efficiency and power density have become the top concerns for power conversions in data center and telecom. Rising energy intensity leads to a higher cost for delivering power. Meanwhile, the demand for compact power supply unit (PSU) grows significantly. It requires PSU with high efficiency, low profile and high power density. Generally, the power supplies for power distribution system in data center and telecom are the standard two-stage approach [5, 6, 7, 8]. It consists of a front-end power-factor-correction (PFC) rectifier with bulky dc-link capacitor followed by an isolated DC-DC converter as shown in Fig. 1-1. In general, the two-stage power conversion has demonstrated excellent performance and high reliability, since the design can be optimized for each stage. However, the cost for this type of approach is high due to relatively large number of components to accomplish the required functions of the front-end converters.

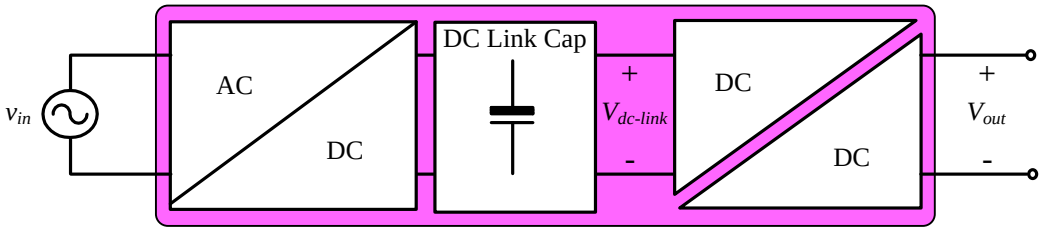
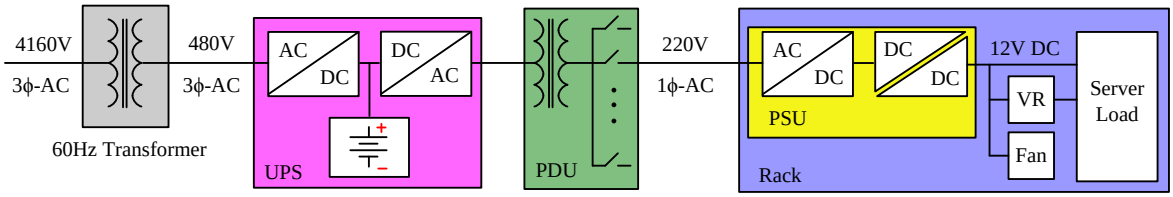


Fig. 1-1 Block diagram of the two-stage power supply (PSU).

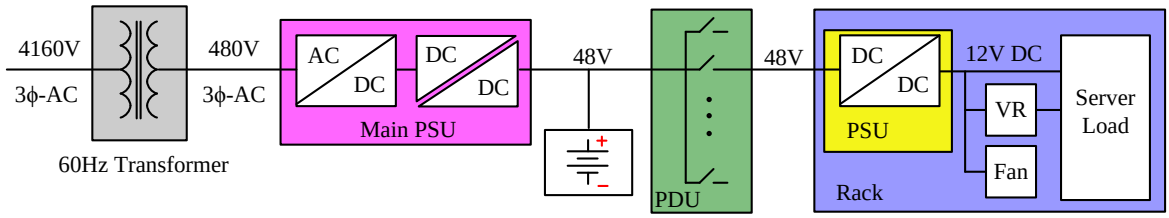
Before studying deeper into details of this growing application, the configuration and technical requirement of rectifier in DC PDS must be considered to fully understand the context of the dissertation and rationalize for using single-stage approach.

1.1 DC Power Distribution Systems (PDS)

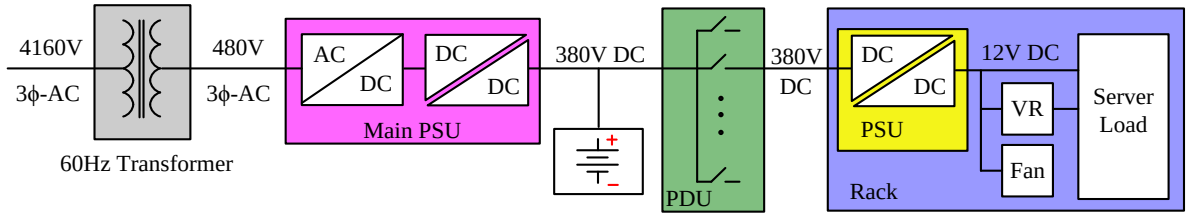
The basic structures of a conventional AC power distribution system (PDS) and a facility-level DC PDS are shown in Fig. 1-2. As can be noticed, the conventional AC PDS in Fig. 1-2 (a) includes multiple conversion stages, which lead to a strongly reduced overall efficiency. In the ac delivery system, the power immediately undergoes a double conversion in a centralized uninterruptable power supplies (UPS) which supplies power to many racks. Power is rectified to DC to feed an intermediate backup storage system, and then it is inverted back to AC and sent to the power distribution unit (PDU). At the PDU, voltage is stepped down to 208/120 V to feed each PSU in the server rack. The PSU in each server rectifies the 220 V AC to a DC voltage typically 380Vdc. The 380 V is then converted with an isolated DC-DC converter to 12 V. Some loads, such as hard drives, can take 12 V directly. Other loads, such as processors, need voltage regulators (VR) to step down the voltage. Depending on the efficiency of the different components, the overall efficiency of such an AC PDS is between 50% and 70% [1]. In a facility-level DC PDS, however, several conversion steps can be avoided to improve the efficiency. As shown in Fig. 1-2 (b) and (c), the DC-AC conversion in the UPS, the transformer in the PDU and the AC-DC conversion in the PSU are eliminated, resulting in a higher efficiency of the power distribution system [1].



(a) Conventional AC power distribution.



(b) 48V DC facility-level power distribution.



(c) 380V HVDC facility-level PDS.

Fig. 1-2 Block diagrams of power distribution systems for data center and telecom [1].

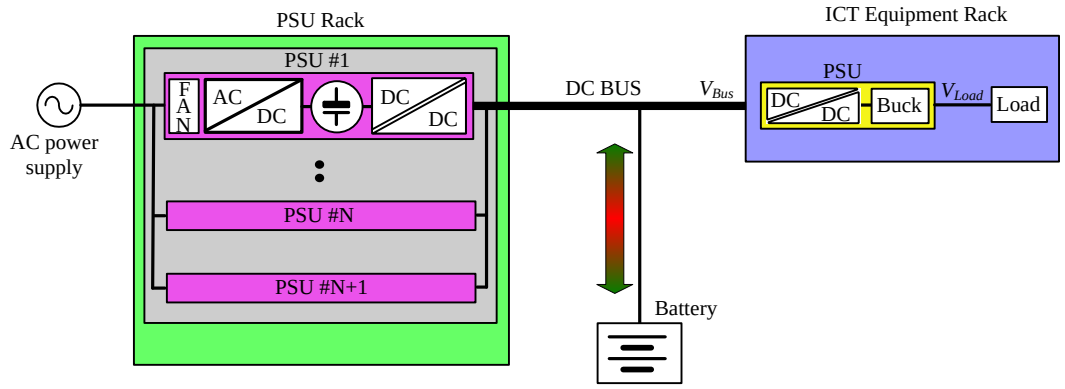
The 48 V and 380 V solutions architecture help reducing power loss from the data center facility, to the rack, and the server board level [9, 10, 11]. For example, compared with the current mainstream approach (12 V power distribution), 48 V architecture provides better power conversion efficiency at rack level, and works at lower current levels to deliver a sixteen times reduction in power distribution. Intel concluded that DC power distribution system (both 400 V and 48 V) was consistently more efficient than AC at all voltages.

1.2 Configuration PSU/Battery in Rack Level

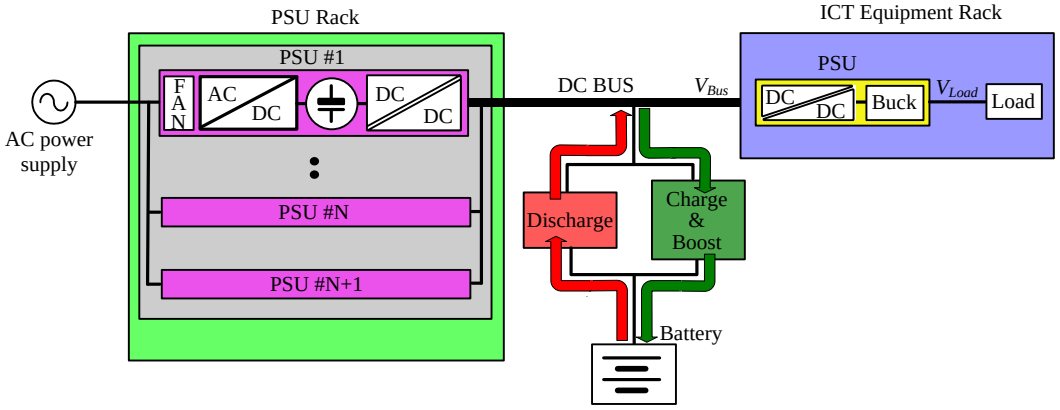
Given the trend towards high-density rack in the infrastructure, it is likely that the future may bring racks at a higher density than the existing equipment in the data center [3]. Data centers today use more kilowatts (kW) per rack or per square foot than ever before. As the rack power climbs, conversion efficiency becomes more important. A 1% efficiency improvement can result in saving hundreds of watts at rack level, and kilowatts in the data center [9]. The power is processed by redundant two-stage front-end converters represented by the power supplies (PUSs) #1 through #N+1 in Fig. 1-3. Each PSU consists of a PFC stage and a DC-DC converter used to regulate the DC bus. Conversion efficiency and total volume of the power distribution system (PDS) depend largely on PSU performance [13]. It is important to mention the main focus of the work in this dissertation is conducted on development of high efficiency and high power density PSU for this application.

There are various configurations of PSU connected to a backup battery as shown in Fig. 1-3. In common power architecture of a UPS system shown n Fig. 1-3 (a), a load is connected through a DC bus to both a main PSU and a backup battery [1]. The load is typically powered from the main PSU, for example through mains power. If the AC power supply is disrupted, for example, because of a power outage, the load is switched to the backup battery, which ensures continuous power supply. One drawback is that after a battery discharge, the DC bus voltage determined by the battery voltage is much lower than the battery floating voltage which results in a higher current at constant power ICT load. This higher current flowing through PDUs and power distribution lines impacts the design by increasing the cross-sectional area of distribution power lines and rated current of protection devices. In addition, the main PSU may require a wide operational range of DC bus voltage, e.g, in the order of tens of Volts. Such a wide operational voltage range may lower the power efficiency and increase cost and complexity of the supply and conversion operations in the system [14].

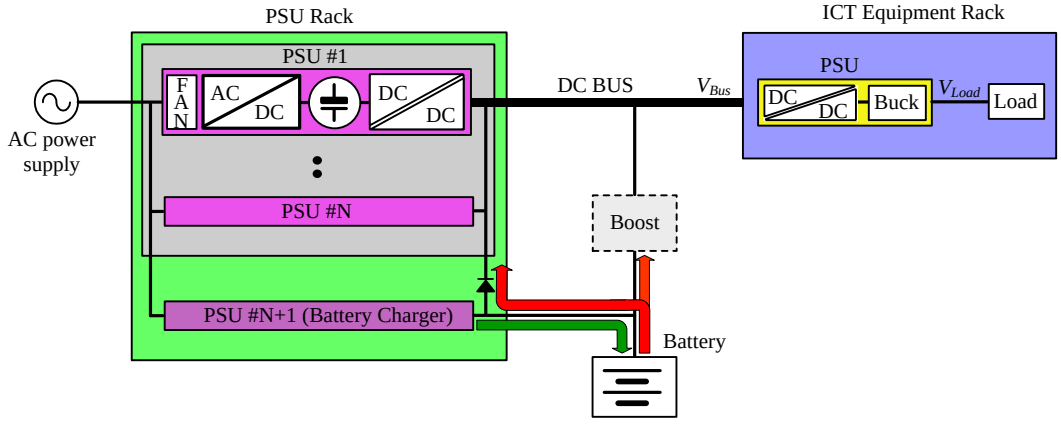
For the implementation of battery backup system architecture in Fig. 1-3 (b) [14], different charging and discharging paths may be used between the battery module and the DC bus such that the battery voltage is controlled to be higher than the DC bus voltage.



(a) 380V DC with direct battery connection.



(b) Battery backup with different charging and dischargin path in 48V DC Google system.



(c) Separated battery charger with boost option in 380 V DC NTT system.

Fig. 1-3 Various configuration of battery backup system in 48 V and 380 V power distribution system (note: PDU is not drawn and VR (Buck DC-DC converter) is redrawn as part of PSU for simplicity).

As a result, the DC bus voltage may operate at a narrower range than the battery voltage. This may improve overall efficiency and reduce cost of operation of the UPS system. The separation of charging and discharging path can also increase protection against system faults such as thermal runaways, short-circuits, and battery over and under voltage.

Fig. 1-3 (c) shows other configurations of the rectifier with a separate charger. Diode and battery rapidly provides the system with a nominal output voltage after the supplies are down. In addition to this, the PSUs separated by a diode from the battery do not need to have a battery charger function. Only the PSU directly connected to the battery needs to have a battery charger function. Redundancy of the charger is better for high reliability. If the range of the operation voltage defined by each PSU in ICT Equipment is narrow, the voltage DC bus must be compensated without interruption in the load. In this case, a system configuration with a boost is recommended [12].

1.3 Technical Requirements for PSU

The purpose of the front-end converter is to regulate the DC output voltage tightly, supply all the load connected to the distributed bus, guarantee current sharing, provide isolation and charge a bank of batteries to provide backup energy when the grid breaks down. The rectifier achieves N+1 parallel redundancy and increases reliability. In case of a failure in a rectifier unit in the cabinet, each PSU unit must be able to operate and maintain safe operation. These units are commonly modular and hot plug capable for simplifying maintenance and reducing repair time.

In addition to those basic PSU requirements, the front-end PSUs are required to operate with a wide input-voltage and/or output-voltage range. The front-end PSUs must meet the input stringent international requirements, such as the IEC 61000-3-2, to limit the harmonic currents drawn by the off-line equipment and provide unity power factor. As other requirements, PSU has to meet some abnormal input operation as shown in Fig. 1-4: voltage sag, surge, unbalanced input three-phase, and the most stringent one is one phase loss operation.

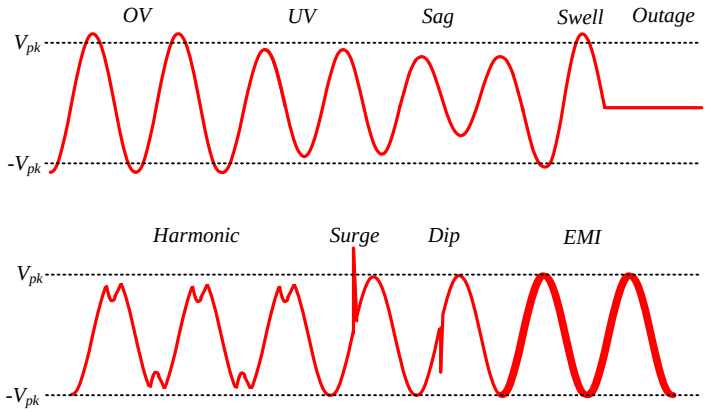


Fig. 1-4 Input power quality.

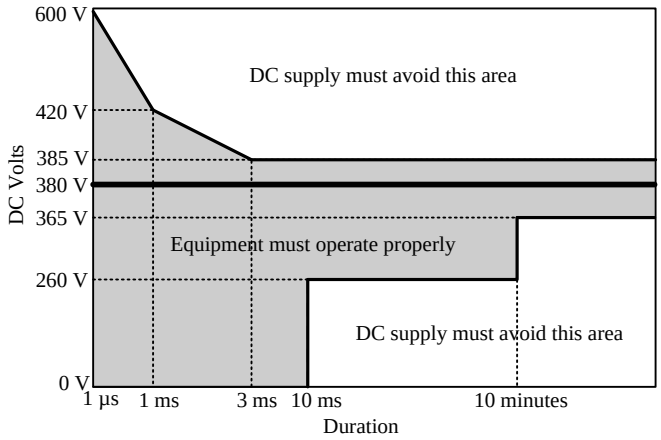


Fig. 1-5 Output voltage requirement.

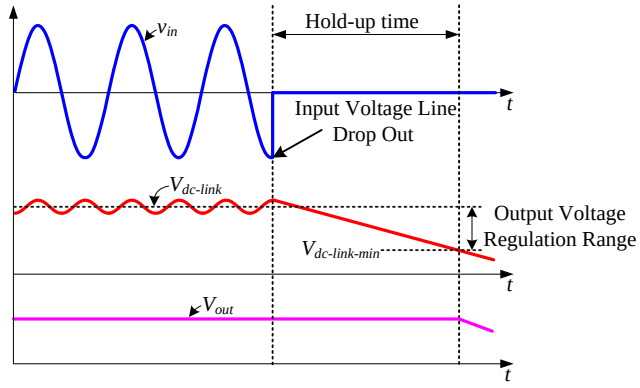


Fig. 1-6 Hold-up time voltage waveforms.

The new international standardization, ITU-T L.1200 specifies the direct current (DC) interface between the power feeding system and ICT equipment connected to it. It describes normal and abnormal voltage ranges, and immunity test levels for ICT equipment to maintain the stability of telecommunication and data communication services. The output voltage range of rectifiers should be adapted to interface based on ITU-T L.1200 as shown in Fig. 1-5.

Another obstacle for front-end PSU design is the hold-up time requirement. It requires the front-end system to provide full power output and regulate output voltage for a few mili-second, after the AC line is lost as shown in Fig. 1-6 (circuit block shown in Fig. 1-1). This hold-up time will ensure the digital system to have enough time to respond to power failure.

1.4 The Existing Commercialize Isolated Three-phase PSU and Proposed PSU

In following section, a review on the existing power supply technologies is provided, including the pros and cons of each technology. The existing three-phase isolated AC-DC converters for PDSs can be implemented either with three single-phase isolated AC-DC converters, or with a direct three-phase PFC rectifier front-end such as the Vienna rectifier or the six-switch PFC boost rectifier followed by an isolated DC-DC converter [15]. To be able to employ single-phase modules designed for 220/277 V_{rms} phase-to-neutral voltage in three-phase power systems with nominal phase-to-phase voltage of 380/480 V_{rms}, the three single-phase modules must be connected in star (Y) configuration. The delta (Δ) configuration cannot be used since it would require that single-phase modules be connected across two phases, i.e., to a voltage exceeding their rating.

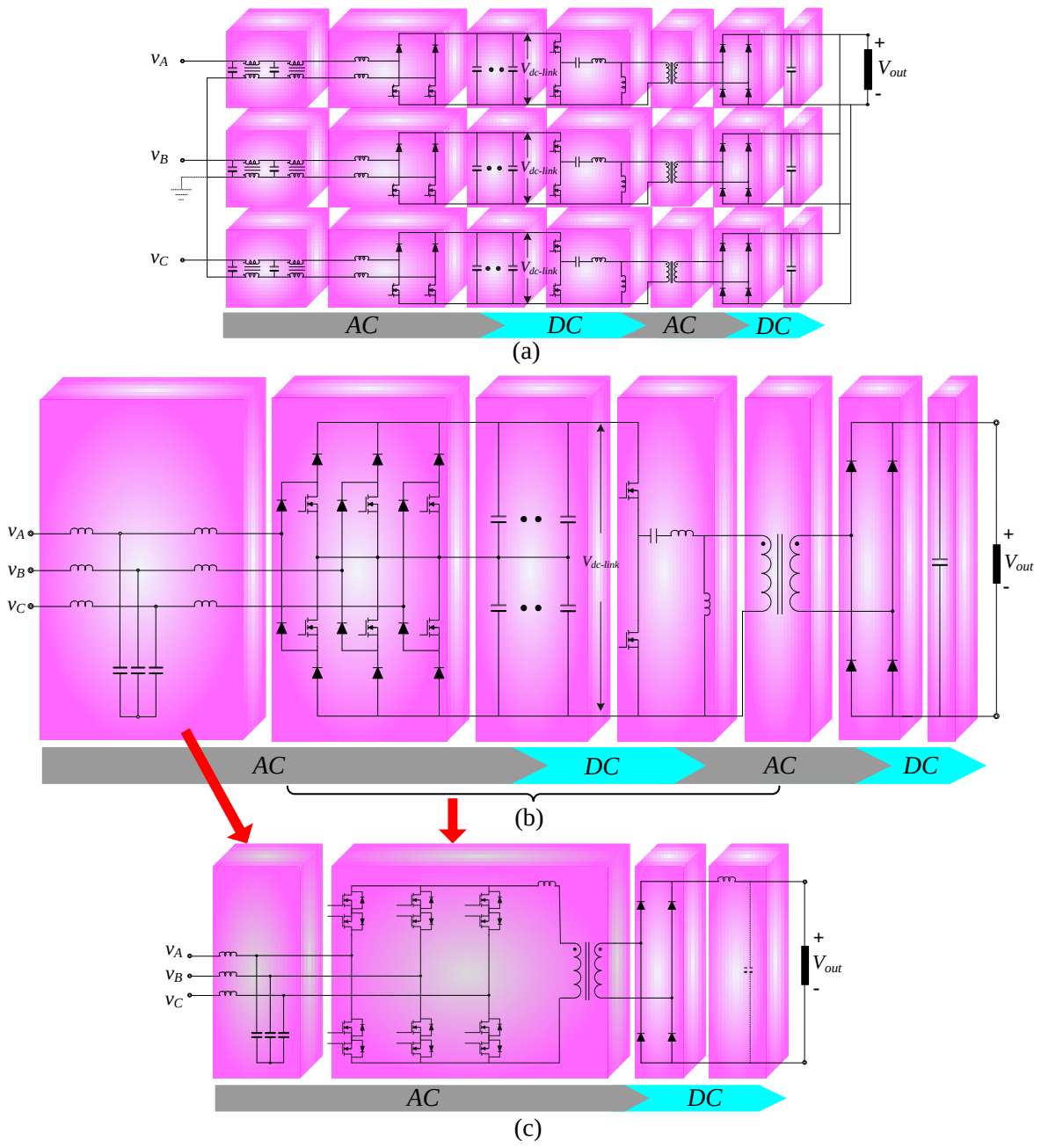


Fig. 1-7 Various configuration of PSUs with estimated power density in cubic block for data center and telecom applications: (a) single-phase module (bridgeless PFC + LLC) (b) direct three-phase (Vienna rectifier + LLC) (c) proposed single-stage PSU (isolated buck matrix-type rectifier).

1.4.1 Single-Phase Modules

Fig. 1-7 (a) shows three single-phase isolated AC-DC converters modules employed to implement an isolated three-phase, three-wire AC-DC converter. The single-phase isolated AC-DC module is a two-stage converter that consists of a PFC rectifier followed by an isolated DC-DC converter. The PFC rectifier can be a high frequency PWM rectifier of boost type to perform the PFC function to meet harmonic current standards [6]. The intermediate dc-link capacitor at the output of the PFC rectifier is to limit the bus voltage ripple due to the double grid frequency pulsating power and provide hold-up time. The DC-DC converter provides high frequency isolation, voltage scaling, and further output regulation [16]. LLC resonant topology [17] is commonly used for the second-stage isolated DC-DC converter. With advent of gallium-nitride (GaN) power semiconductor devices and SiC MOSFET, the efficiency and the power density of the two-stage converter can be significantly improved since the converter can operate at much higher switching frequency with minimum switching losses. Recently, the totem-pole bridge-less PFC rectifier with GaN implementation [18-19], has become a popular solution for application like front-end converter. The efficiency higher than 99% can be achieved with the CRM Totem-pole bridge-less PFC using GaN devices while the converter is switched at megahertz. A two-stage single-phase 3 kW module with 54 V output is demonstrated with 98% peak efficiency and close to 60 W/in^3 power density in today`s power supply market [20].

However, the two-stage single-phase module exhibits some drawbacks as highlighted in below. One of the drawbacks is that, regardless of hold-up time requirement, the two-stage power converters are enforced large intermediate dc-link capacitors to limit the bus voltage ripple and handle the pulsating power in single phase module. As shown in Fig. 1-7 (a) the intermediate dc-link capacitors usually occupy more than 20% of the volume of the PSU with today`s power density of 60 W/in$^3$. With increasing switching frequency in the range of MHz, the magnetics components get smaller in size and it is expected the power density of single-phase module PSU exceeds three times of today`s market in the future. This indicates that the space inside the PSU will be dominated by the bulky dc-link capacitors which cannot be avoided due to pulsating power operation. In addition, the pulsating capacitors make the PCB layout and packaging to be more difficult for high-power-density PSU since these capacitors must be placed

on the main PCB of PSU. Therefore, the thermal cooling is more challenge for major power components in the PSU such as switching power devices, heatsink and magnetic components as a result of the fan airflow blocked by these bulky capacitors.

In standard telecom power supplies, where the source neutral point is not provided, any unbalance in the three-phase source phase voltages and/or in the three single-phase modules shown in Fig. 1-7 (a) will create a potential difference between the Y point of the single-phase modules and the source neutral point, resulting in oscillations and significant variations of the input voltages of the single phase converters [15]. Therefore, a balancing control of the three single-phase modules is necessary for a stable and reliable steady-state operation, where the input voltage always stays within a specified range. The balancing control between the three single-phase modules can be achieved with additional passive components used to create a virtual (artificial) neutral point and by using balancing control methods [21-25], or without additional passive components by using only balancing control methods [26].

1.4.2 Direct Three-Phase

A significant breakthrough in simplifying the single-phase modules was achieved by three-phase PFC rectifiers as shown in Fig. 1-7 (b). Three-phase isolated AC-DC converters can be implemented with a direct three-phase PFC rectifier front end such as Vienna [27] or six-switch boost PFC rectifier [28] followed by an isolated DC-DC converter. With direct three-phase rectifier, the three-phase load balancing can be achieved automatically. The Vienna rectifier does not require a large bus capacitance because the three-phase input voltages eliminate the pulsating power in the dc-link. As a result, the amount of bus capacitance in the Vienna rectifier is reduced with respect to the single-phase PFC approach. Another advantage of this rectifier is that the voltage stress across the switches are subject to only half of the total bus voltage, thus allowing 500 V MOSFETs to be used in the VIENNA rectifier. Despite the power stage simplification achieved by the Vienna rectifier, the power density of direct three-phase rectifier is normally lower than the single-phase modules. Because the three-phase PFC converter in the first stage is usually hard switched and the converter cannot operate at very high switching frequency which

results in large size of input chokes. It is also noteworthy to mention the $/kW with direct three-phase solution is relatively higher than single-phase module PSUs.

1.4.3 Isolated DC/DC Converter in Second-Stage

The LLC resonant converters have been widely used as the isolated DC-DC converter in the second-stage in off-line power supplies of data centers due to its high efficiency and hold-up capability. Using LLC converters can minimize switching losses and reduce electromagnetic interference. Almost all the high-end offline power supplies employ LLC converters as the DC-DC converter. But there are few major challenges and limitation in using LLC converters. Generally, the detrimental effect of wide input and/or output voltage range on the conversion efficiency is more severe in resonant converters than in pulse-width-modulated (PWM) converters. LLC resonant converter regulates the output voltage by changing the switching frequency, i.e., by moving the operating point away from the resonant frequency as the input voltage and/or output voltage changes.

As a result, they suffer from progressively increased losses as the input- and/or output-voltage range is widened. This is the major reason LLC resonant converter, is not able to maintain high efficiency across the entire range when input voltage or output-voltage range is wide [29]. This significantly limits the power handling of LLC converter for constant power and constant current operations, since the output voltage relatively needs to be changed under these operations.

1.4.4 Proposed Single-Stage PSU for PDS in Telecom and Data center Applications

It is of paramount importance to minimize the cost of components, design complexity, to eliminate the bulky dc-link capacitors and at the same time realizing high efficiency and high power density PSU by choosing a reasonable converter topology.

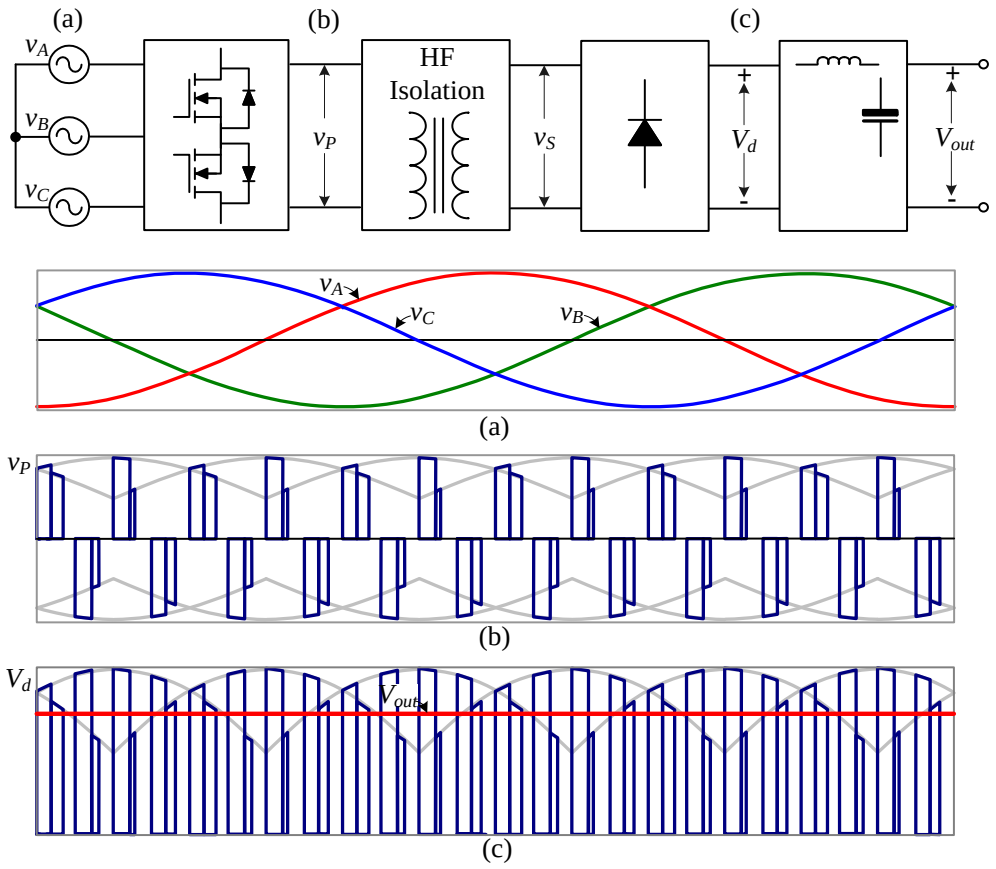


Fig. 1-8 Three-Phase high-frequency isolated matrix-type rectifier.

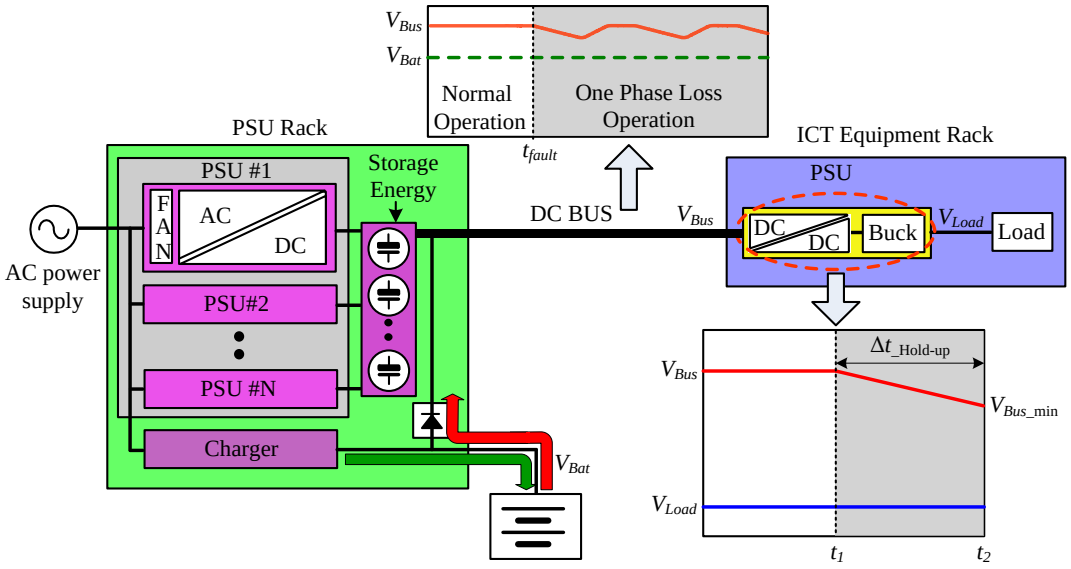


Fig. 1-9 An example of proposed PSU in configuration with separated battery charger and diode in 380V DC PDS.

Since conversion efficiency and total volume of the PDS in telecom and data center depend largely on the front-end PSU performance. Therefore, we are highly motived to study possibility of different topology which can be adopted for future PSU in telecom and data center applications. The advantage of performing PFC functionality and galvanic isolation in a single-stage conversion make the isolated single-stage topology to be considered as an attractive solution for the future front-end PSU in telecom and data center applications. Typically, the single-stage power conversion directly converts the mains-frequency AC voltage into a high-frequency AC voltage which is supplied to a high-frequency isolation transformer whose secondary voltage is then rectified to the desired DC output voltage as shown in Fig. 1-8 [30-31].

High conversion efficiency and compact construction stemming from the non-existence of an intermediated dc-link capacitors and the second stage DC-DC conversion can be achieved. Improved lifespan due to elimination of the bulky and often trouble-causing dc-link component is another benefit of using single-stage approached PSU. With single-stage approached PSU, the rack can be greatly simplified in PDS. The storage energy capacitors at the output of PSU can be placed outside of the PSUs as shown in the example of Fig. 1-9. This provides tangible benefits in the form of space saving, and better airflow for front-end PSUs which result in higher power density and smaller fans.

However, there have always been some concerns about employing single-stage PSU in telecom and data center applications such as continuous operation of single-stage PSU during faulty mode one phase loss and hold-up time requirement during input AC source drop out. Regarding the first concern, the single-stage PSU is able to deliver continuous power to the ICT load during one phase loss operation, but the DC bus (output of PSU) may contain output voltage ripple at double of the line frequency as shown in Fig. 1-9. The configuration of battery backup system in Fig. 1-9 is similar to the NTT solution described in Fig. 1-3 (c). In this example, the battery voltage set point is lower than DC bus voltage such that the battery will not be engaged in one phase loss operation. However, the downstream PSU in ICT equipment has to be able to operate at wide input range, which is normally true in real application, in order to take into account the DC bus voltage variation. Likewise, the hold-up time requirement can also be met thanks to the wide input range of the PSU in ICT equipment. By selecting reasonable small size

of storage energy at the output of PSU, the DC bus can ramp down with small slew rate and provide a few millisecond hold-up time within the range of input voltage of the first-stage (DC-DC converter) in ICT equipment when the power outage is occurred as shown in Fig. 1-9.

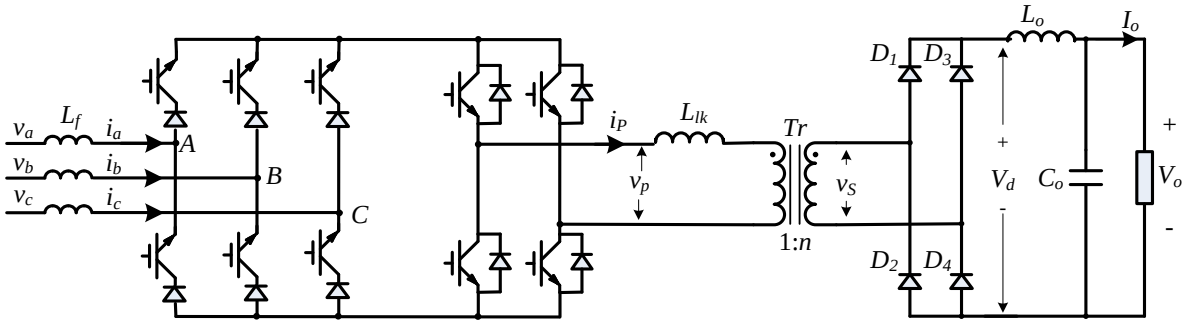
It is also important to note that, during one phase loss operation, the single-stage PSU for battery charger will exhibit different charging behavior. Prior to time t_{fault} (normal operation), the output voltage of the charger is tightly regulated and the battery is in floating state. After t_{fault} (during one phase loss), the charger output voltage may contain ripple which results in discontinuity of the float charging current of battery. However, this may not harm the battery since the battery consumes very small charging current during float state.

1.5 Topology Overview of Single-Stage Isolated Three-Phase Rectifiers

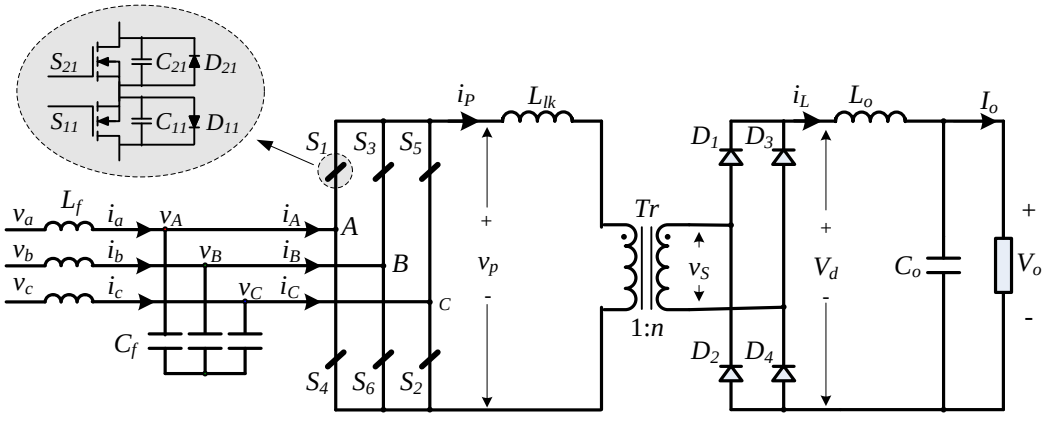
The power stage design clearly depends on the converter circuit topology. Therefore to achieve a high-efficiency and high-density design, it is a logical and necessary step to carry out the systematic design and evaluation for the topologies that meet the application requirements, and select among them the most suitable candidate. Several novel single-stage isolated three-phase rectifier topologies such as buck, boost, buck-boost, flyback/forward, and buck and boost matrix-type have been reported in [32-34]. In [35], an isolated single-stage (boost) topology is presented based on a two-switch three-phase rectifier. This topology is easy to control and it operates in discontinuous conduction mode (DCM). Thus it shows higher RMS current which can be useful for high frequency low-medium power application. An isolated single-stage Swiss-Forward (buck) topology is proposed in [36], showing lower number of high frequency transistors but higher voltage stress on semiconductors because of the forward structure. In addition, a single-stage three-phase AC-DC converter with high frequency isolation–could be also realized by the Cuk-based or SEPIC-based single-switch converters as proposed in [37-39] or single-switch three-phase flyback converters as proposed in [33]. These converters show a very simple structure of the power and control circuits which is paid for, however, by a high voltage and current stress on the devices and by a relatively high filtering effort for suppressing

electromagnetic interferences (discontinuous input current shape). The systems are economically applicable, therefore, only for output power levels below 3.5 kW and/or they are of minor importance for the realization of high power, high efficiency and high power density converter needed for PDS in telecom and data center applications.

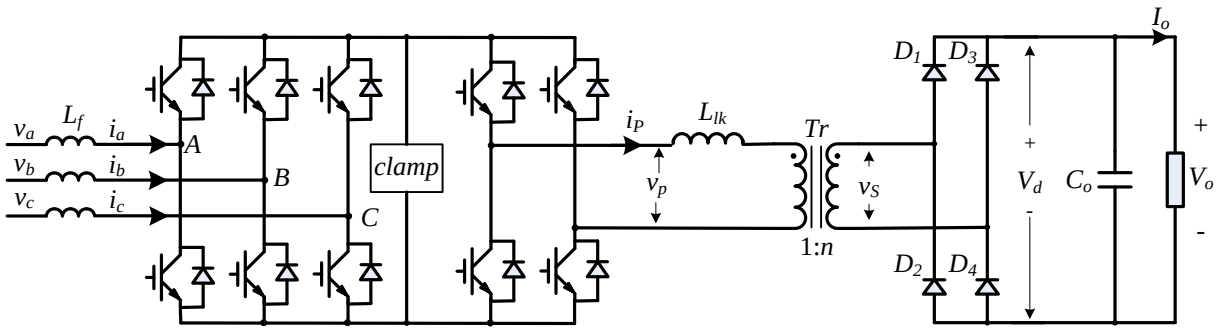
For higher power (≥ 3.5 kW), the single-stage isolated matrix-type rectifiers are the most favorable in terms of high power density and high efficiency [30, 32, 34] and [40-42]. These single-stage isolated matrix-type rectifiers can be classified into four major categories as shown in Fig. 1-10 (a) buck derived indirect matrix-type rectifier; (b) buck derived matrix-type (direct matrix) rectifier; (c) boost derived indirect matrix-type rectifier; (d) boost derived matrix-type (direct matrix) rectifier.



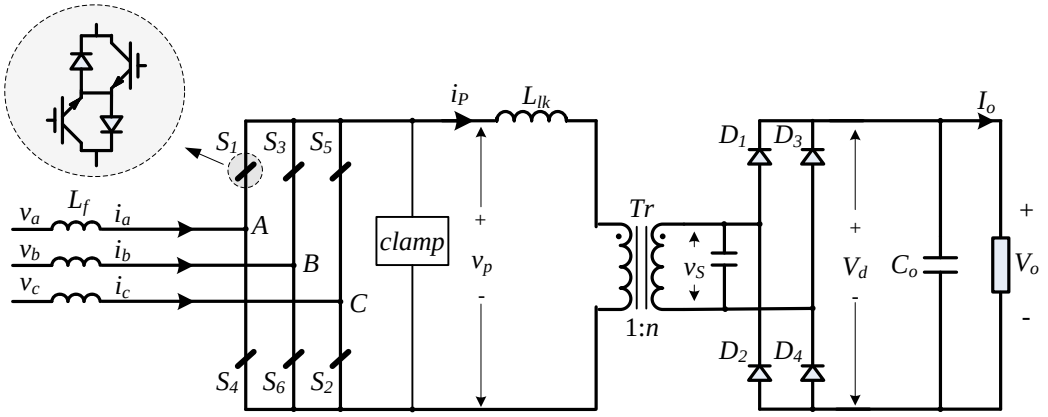
(a) Buck derived indirect matrix-type rectifier.



(b) Buck derived matrix-type (direct matrix) rectifier.



(c) Boost derived indirect matrix-type rectifier.



(d) Boost derived matrix-type (direct matrix) rectifier

Fig. 1-10 Basic structures of isolated matrix-type three-phase rectifiers.

1.5.1 Boost Derived Indirect and Direct Matrix-Type Rectifiers

The structures in Fig. 1-10 (c) and (d) are of boost derived indirect and direct matrix-type rectifiers. As shown in Fig. 1-10 (c), the boost derived indirect matrix-type rectifier is quite similar to the two stage PWM rectifier with a three-phase boost rectifier as an AC-DC stage and a full-bridge converter as a DC-DC stage. Due to the still missing intermediate energy storage, it is called indirect matrix-type PWM rectifier. The front end of boost derived matrix-type (direct matrix) rectifier in Fig. 1-10 (d) has a similar structure of a three-phase boost rectifier. However, all the six active switches are bidirectional for matrix-type and operating in DCM.

It is also observed that the boost derived indirect and direct matrix-type rectifiers are not strong candidate for PDS in telecom and data center applications, since the facility-level PDS is powered from the three-phase (400V/480V) ±10% with the mentioned output voltage of 380 V or 54 V the boost-type PFC rectifiers may not be suitable. The main reasons can be highlighted as follows:

- **High Voltage stress may require clamping**: the DC output voltage of boost-type PFC rectifiers has to be at least 15% above the peak value of the mains line-to-line voltage; thus, with a wide input voltage range up to (480 V_{rms}) ±10%, the output voltage is typically selected to be 850 V DC in ideal case. If the effect of the leakage inductance of the transformer is considered, the device voltage will be well above 1.2 kV. Therefore, the voltage clamping is required, which will increase the losses and complexity of the converter.
- **Low Power Density:** ZCS operation can be achieved with boost matrix-type rectifiers. ZCS is usually employed to alleviate the turn-OFF losses of devices that possess slow turn-OFF such as IGBT. However, Si IGBT devices cannot operate at high switching frequency due to the large turn-ON losses. As a result, the input boost inductors need to be to design with larger size.
- **High RMS current:** at the medium power levels considered in this study (5 kW), DCM converters are not appropriate because they have high RMS currents in the semiconductor devices, inductor and the transformer windings which result in high conduction losses.

Due to aforementioned drawbacks, boost derived indirect and direct matrix-type rectifiers will not be discussed further in this dissertation.

1.5.2 Buck Derived Indirect and Direct Matrix-Type Rectifiers

In the case of buck derived indirect matrix-type rectifier in Fig. 1-10 (a), the first-stage is buck type three-phase rectifier and the second-stage can be applied any high-frequency DC-DC converters. As proposed in [30, 32] a conventional buck-type PFC rectifier in combination with a phase-shift DC-DC converter or LLC resonant converter could be used. However, the

conventional buck-type PFC rectifier suffers from high conduction losses in the high frequency diodes which are needed in series to the switches [43, 44]. A novel three-phase isolated buck matrix-type rectifier with the structure as shown in Fig. 1-10 (b) is proposed in [45], which is capable of power factor correction (unity power factor), low harmonic current distortion, and at the same time realizing ZVS for primary power semiconductor devices. It is topologically equivalent to the converter described in [30, 31] with extra series inductor on the primary side of transformer to achieve soft-switching. It operates in CCM and realizes ZVS turn-on for the primary power devices in the same way as in the familiar phase-shift controlled ZVS full-bridge DC-DC [46, 47]. Under ZVS conditions and using fast turn-off devices such as MOSFETs, the rectifier can operate at high-switching frequency to achieve high-power density while maintaining high-efficiency. It should be noted that switching frequency is still limited by other factors such as secondary side ringing loss and duty cycle loss, since the operation of isolated buck matrix-type rectifier is similar to phase-shift full-bridge DC-DC converter.

The isolated buck matrix-type rectifier in Fig. 1-10 (b) can be a choice, when the input line voltage is high so its boost counterpart suffers from high device voltage ratings. The topology has relatively simple power train compared with the other topologies discussed above. Compared with the buck derived indirect matrix-type rectifier, the conduction losses can be significantly reduced since the diode voltage drop is eliminated. Therefore, among all the isolated matrix-type rectifiers discussed above, the isolated buck matrix-type (direct matrix) rectifier is the most promising topology to achieve high efficiency and high power density power supply design at the medium power level (5 kW~10 kW) for telecom and data center applications. The buck matrix-type rectifier is also favorable when variable output dc voltage is a must as it is the case for typical telecom and data center applications where the output is usually connected to a battery bank with large voltage fluctuations. Besides, better dynamic response and no starting problems are among the other advantages of the buck matrix-type rectifier. If compared with two-stage PSUs, the buck matrix-type rectifier possesses several advantages such as reduced size and higher power-density, improved lifespan due to elimination of the bulky and often trouble-causing dc-link component. In addition, compared with the two-stage converter with LLC as the second stage, the buck matrix-type rectifier provides a wide output-voltage control range (down

to zero volt) while maintaining PFC capability at the input. This can bring significant benefits to design the power supply with battery charging capability.

With all the advantages discussed above, together with the option of placing the energy storage outside the PSU, using buck matrix-type rectifier provides a potential breakthrough of the power supply design for data center and telecom applications. Nevertheless, for the same reason of the avoided dc-link component, the matrix-type rectifiers are also known for their relatively complex modulation and commutation techniques, and lack of ride-through capability such as stringent case of one phase loss. Therefore, one possible reason for their limited utilization in industries is the complex commutation and modulation schemes required simultaneously to perform PFC and isolated DC-DC conversion over the entire load and input voltage range. Especially under the faulty mode of one phase loss operation, PSU is required to deliver two-third of rated power and regulate the output voltage within the specification required for telecom and data center applications. To date, there is no comprehensive study on the commutation method and modulation scheme design for the isolated buck matrix-type rectifier. In addition, there is no reported study on the operation of the matrix-type rectifier under faulty mode of one phase loss. It is therefore this work's primary aim to propose and develop appropriate modulation and commutation schemes for this particular converter to be able to meet the stringent input and output requirements for telecom and data center applications.

1.6 Dissertation Objectives

The motivation of this work comes from the foregoing background. To achieve high power density, the converter must operate at a higher frequency, and to achieve high efficiency, the soft switching must be implemented to mitigate the switching loss. All these benefits can only be realized through the PWM modulation and commutation schemes. Therefore, the PWM modulation and commutation schemes play very important role to facilitate ZVS operation and reduce the switching events (turn-ON and turn-OFF actions) to further remove the associated loss while satisfying basic requirements of PSU such as the input currents THD, PFC, and output

voltage regulation. Aiming at developing various possible modulation schemes for the isolated matrix-type rectifier, the main objectives of this dissertation are listed as follows:

1. PWM Modulation and Commutation Schemes for Three-Phase Isolated Buck Matrix-Type Rectifier. Investigate several commonly practiced PWM schemes particularly for three-phase isolated buck matrix-type rectifier. Compare the performance of rectifier with different PMW schemes based on switching losses, duty-cycle loss, output inductor current ripple and input grid currents THD. Propose an optimal PWM candidate for MOSFET devices employed in the isolated buck matrix-type rectifier. The proposed PWM modulation strategy and commutation method is derived using the analysis synthesis method based on the ZVS FB-PS DC-DC topology. Provide simulation to verify the proposed concepts, and build prototype to further test the modulation schemes experimentally.

2. High Power Density with High Efficiency (> 98%). To achieve high power density, a higher switching frequency is desired, which greatly determines the size of passive components such as transformer and output inductor. However, the high switching frequency operation of a three-phase rectifier is thermally limited by the switching losses of the power devices. The duty-cycle loss is another major limitation of operation at a higher switching frequency and it generates circulating current on the primary side of transformer which results in large conduction loss and poor input current THD. To meet the overall efficiency for proposed targets 98% is a challenge. Minimizing switching losses by implementation of ZVS soft-switching is a major expectation for a three-phase soft-switching converter. In addition, the switching events (turn-ON and OFF actions) need to be reduced through proper PWM modulation schemes and commutation schemes which can be considered as one of the most important objectives of this dissertation.

3. PWM Modulation and Commutation Schemes for One Phase Loss Operation of Three-Phase Isolated Buck Matrix-Type Rectifier. Propose a novel PWM scheme based on the extension of the ZVS FB-PS DC-DC topology for one phase loss operation of three-phase isolated buck matrix-type rectifier. With the proposed PWM scheme, the maximum available voltage gain for one phase loss operation can be achieved, which permits the continuous operation of the converter to deliver two-third of the rated power and regulate the output voltage

with maximum output voltage drop less than 5% of nominal output voltage. In addition, propose a commutation method for a safe transition from one phase loss operation to normal operation and vice versa with minimum commutation steps (two-step) under ZVS condition. Evaluate and verify the performance of the converter with proposed PWM and commutation schemes during one phase loss operation through simulations and experiments.

4. Analysis of One Phase Loss Operation of Three-Phase Isolated Buck Matrix-Type Rectifier with Integrated Boost Output Stage. Analyze the one phase loss operation of the three-phase isolated buck matrix-type rectifier with proposed integrated boost output stage. The analysis of one phase loss with combination of buck and boost (buck+boost) operation shows that the converter is able to deliver two-third of rated power and regulate the output voltage with lower output voltage drop with significantly smaller output capacitor compared with conventional buck matrix-type rectifier. The performance of the converter in buck and buck+boost operation is evaluated and verified by simulations and experiments results.

5. Develop High Efficiency and High Power Density Prototypes for 54 V and 380 V Applications. Provide comprehensive loss breakdown and efficiency comparison on 5 kW isolated buck matrix-type rectifier prototypes with 380 V and 54 V output voltages respectively since 380 V and 54 V output voltages are the two popular solutions for PDS in data center and telecom applications. Compare efficiency and power density of 54 V and 380 V prototypes with the benchmark PSUs. Evaluate the semiconductor loss for Si IGBTs and SiC MOSFETs in the context of the isolated buck matrix-type PWM rectifier.

1.7 Dissertation Outline

This thesis consists of six chapters. The background information pertinent to comprehending the study in this dissertation is presented in this chapter, including the introduction of the PDS, the requirement for PSU and the review on the existing power supply techniques for PDS. The main objectives of the thesis are defined, with associated challenges and difficulties identified and discussed. According to study in this chapter, clear choices on the isolated matrix-type

topology, are stated. The employment of ZVS technique produces higher efficiency through the removal of switching losses, allowing all the benefits of higher switching frequency to be realized.

An overview of the most relevant soft switched single-stage isolated matrix-type converter topology for PDS is presented in Chapter 2. The main focus in Chapter 2 is placed on existing modulation and commutation schemes that have found practical presence in industry. Then, several various soft-switched modulation schemes are compared for high frequency isolated buck matrix-type rectifier considering the switching characteristics of different devices such as IGBTs and SiC MOSFETs. Finally, the most advantageous modulation scheme is identified for SiC MOSFET devices employed in high-frequency isolated buck matrix-type rectifier. In addition, Chapter 2 provides the principle operation and steady state analysis of isolated buck matrix-type rectifier with the proposed six-segment PWM scheme, followed by detailed comparison with eight-segment PWM scheme.

As discussed in Chapter 2, the proposed six-segment PWM has higher efficiency over eight-segment PWM. However, eight-segment PWM offers the benefit of smaller transformer size due to the doubled pulse frequency on the transformer resulting in lower core loss. Therefore, it is commendable to improve the eight-segment PWM which can be considered as an alternate PWM scheme for isolated buck matrix-type rectifier. Chapter 3 proposes an improved eight-segment PWM scheme with non-equally distributed zero-vector intervals to improve the large output inductor current fluctuation followed by detailed comparison with conventional eight-segment PWM scheme. In addition, a commutation method is proposed to achieve ZVS for all turn-ON actions of the bidirectional MOSFET devices in the rectifier. Duty-cycle loss, inductor current ripple, and THD in steady-state operation are all compared and verified by the simulation and experimental results for these two PWM schemes. Finally, the efficiency and the loss breakdown for 380 V and 54 V PSUs are analyzed and discussed.

Chapter 4 focuses mainly on developing a viable strategy to maintain proper operation of the converter during one phase loss condition as well as to provide smooth transitions between the faulty and normal modes. A desired modulation scheme to maximize the available rectifier output voltage for three phase matrix converter during one phase loss operation is proposed

based on the extension of ZVS FB-PS dc-dc converter. With the proposed commutation method, a safe transition from one phase loss operation to normal operation and vice versa can occur with minimum commutation steps (two-step) under the (ZVS) condition. The performance including output voltage regulation, input current THD and dynamic switching behavior of the proposed PWM scheme and commutation schemes during one phase loss operation is evaluated and verified by simulations and experiments on a 5 kW prototype.

Chapter 5 proposes three-phase isolated buck matrix-type rectifier with integrated boost output stage. The analysis of one phase loss with combination of buck and boost (buck + boost) operation is discussed in detail. The performance of the converter in buck and buck + boost operation is evaluated and verified by simulations and experiments on a 5 kW prototype.

Finally, Chapter 6 summarizes the main contributions and conclusions of the presented work. Possible future research directions are also suggested.

Chapter 2

Comparative Evaluation PWM and Commutation Schemes for ZVS Isolated Buck Matrix-Type Rectifier

After topology review and comparison in Chapter 1, a zero-voltage switched (ZVS) three-phase isolated buck PWM rectifier using MOSFET proposed in [45] as shown in Fig. 2-1 was selected as the most favorable topology for single-stage three-phase PSU design in data center and telecom applications. Low switching losses can be achieved due to the ZVS operation with MOSFETs such that the converter can operate at a higher switching frequency with high-efficiency. The operation principle of this rectifier is briefly described as below.

Within any 60^{o} interval between two successive zero crossings of input phase voltage as shown in Fig. 2-2, there are two line voltages that do not change sign. Since the switching frequency of the converter is much higher than the line frequency, the two line voltages can be treated as slowly varying dc voltages. Therefore, the three-phase converter in Fig. 2-1 can be redrawn as two ZVS full-bridge phase-shifted (ZVS FB-PS) converter sub-topologies "bridge *x*" and "bridge *y*" as shown in Fig. 2-3. The two bridges ("bridge *x*" and "bridge *y*") share one common phase leg where the phase voltage has the highest or lowest voltage potential. Then the steady state operation and ZVS analysis on the three-phase isolated buck matrix-type rectifier can be done in the same way as FB-PS converter [46].

Same as ZVS FB-PS converter, the isolated buck matrix-type rectifier also utilizes the transformer leakage inductance or together with an additional series inductance to achieve ZVS but at a price of reduction of effective duty-cycle. The duty cycle loss increases the conduction

losses and limits the switching frequency, which result in decreased conversion efficiency and power density of the converter.

Unlike the ZVS FB-PS converter where the input DC bus is constant, the DC bus for the two sub-topologies vary during every 60^o interval since the DC bus is one of the three line-to-line voltages. These variable operating conditions contribute to a large variation on output inductor current ripple. Then, a large output inductor may be required to limit the ripple current, which results in the reduction of power density of the converter. Because the switching sequence of the proposed PWM in [45] contains eight segments in each switching cycle, it is referred as "eight-segment PWM" in this dissertation.

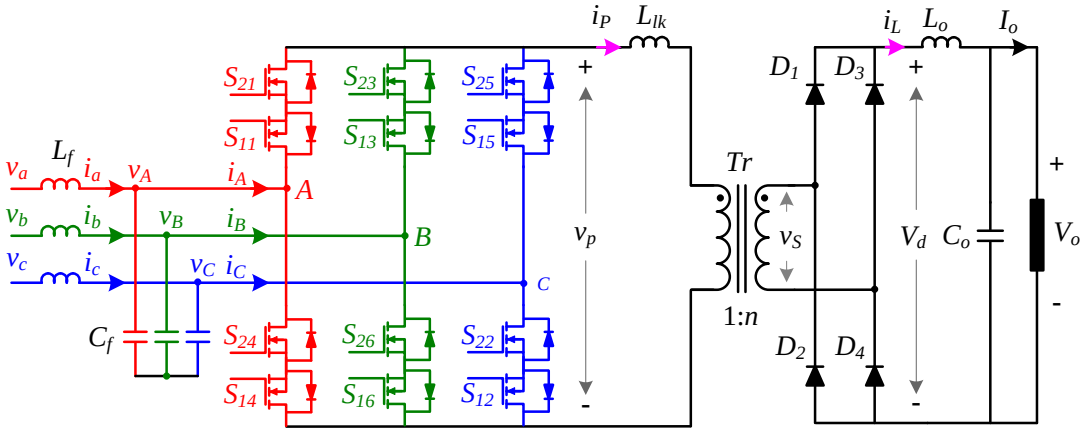


Fig. 2-1 ZVS three-phase isolated buck matrix-type rectifier.

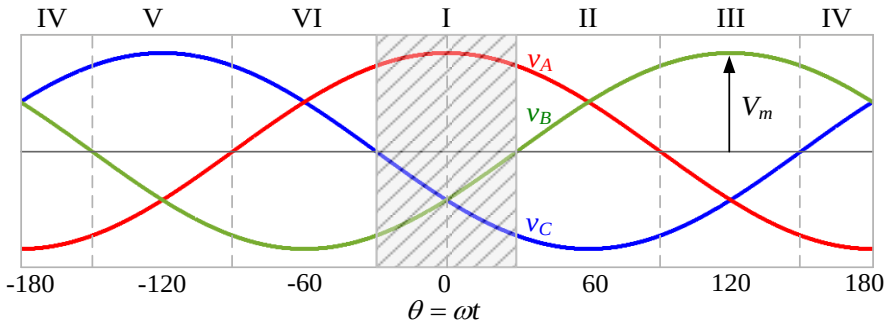


Fig. 2-2 Input phase voltages.

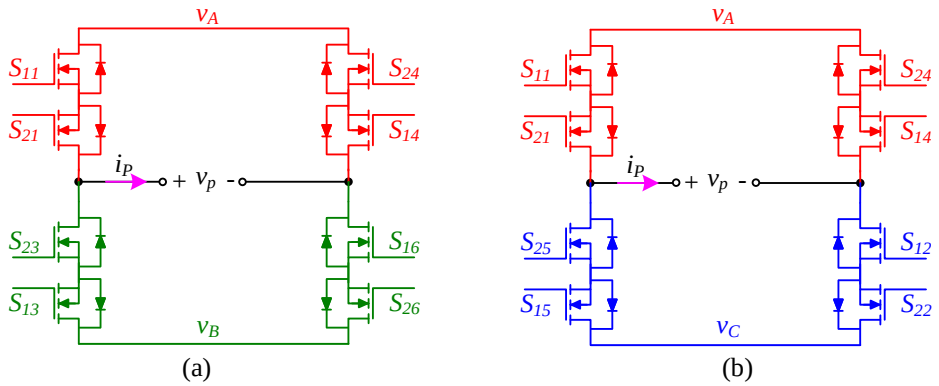


Fig. 2-3 Three-phase rectifier in Fig. 2-1 is redrawn as two ZVS FB-PS dc-dc converter within sector I operation with "leg *A*" as a common leg of (a) "bridge *x*" and (b) "bridge *y*".

Based on the same idea as [45], by rearranging the operating sequence of "bridge *x*" and "bridge y", different PWM schemes can be generated. A six-segment PWM scheme that combine operation of "bridge *x*" and "bridge *y*" to resemble the operation of one ZVS FB-PS converter is proposed. With the proposed six-segment PWM scheme, the aforementioned drawbacks of large duty cycle loss and large output inductor current ripple associated with eight-segment PWM can be significantly reduced. As other benefits of the proposed six-segment, it exhibits low turn-ON and turn-OFF switching losses compared with any other PWM schemes.

The rest of this chapter is organized as follows: the switching pattern and transition of several commonly practiced PWM schemes known as six-segment and eight-segment are reviewed and compared for three-phase isolated buck matrix-type rectifier, followed by the principle operation of the proposed six-segment PWM scheme. The steady-state analysis of duty-cycle loss, output inductor current ripple, and input current THD are described. Simulation and experimental results are presented to evaluate the robustness of proposed six-segment PWM scheme, followed by the conclusion.

2.1 Space Vector Modulation for Buck Matrix-Type Rectifier

In order to explain the operation of PWM schemes for three-phase isolated buck matrix-type rectifier, the space vector modulation for this topology is described in this section first. The

rectifier in Fig. 2-1 is equivalent to traditional current-source rectifier (CSR) [47], except that all the switches are bidirectional. A SVM technique can be used to achieve input unity power factor at the input and output voltage regulation simultaneously. The SVM technique applied to the CSR is based on the representation of the required instantaneous input current vector in the complex plane $\vec{I}(t) = I_m(t)e^{j\omega t}$. The input current space vector of the converter is defined as

$$\vec{I}(t) = \frac{2}{3}\left[i_a(t)e^{j0} + i_b(t)e^{j2\pi/3} + i_c(t)e^{j4\pi/3}\right]. \tag{2-1}$$

As shown in Fig. 2-4, the active switching states can be represented by active vectors $\vec{I}_1$ to $\vec{I}_6$ and zero switching states can be represented by zero space vectors $\vec{I}_7, \vec{I}_8$ and $\vec{I}_9$. For each active vector, there are two possible switching states depending on the direction of the current on the primary side of the transformer I_P as shown in Fig. 2-3. Based on different switching states, the six active vectors can be obtained by

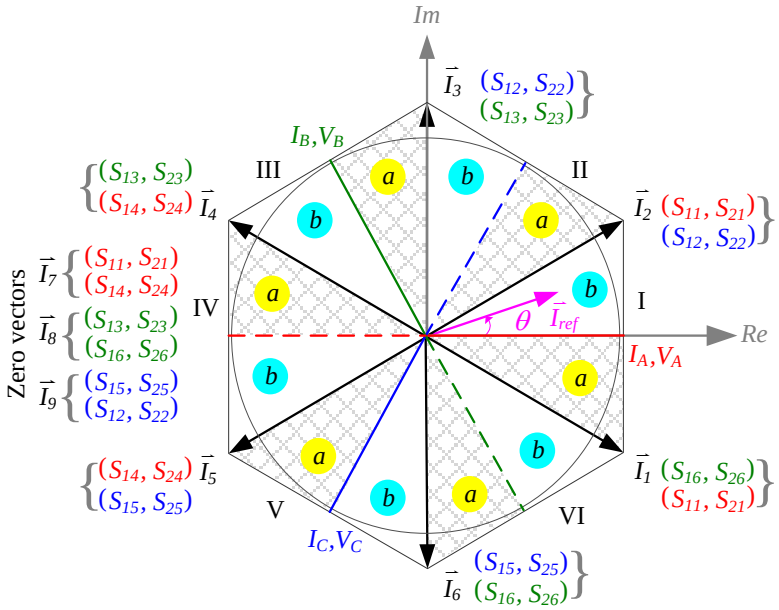
$$\vec{I}_n(t) = \frac{2}{\sqrt{3}} I_P(t)e^{j(n\pi/3-\pi/2)} \tag{2-2}$$

where $n = 1,2,...,6$ for sectors I, II,…,VI, respectively. The reference $\vec{I}_{ref}$ rotates in space at an angular velocity which is the same as the grid voltage vector in order to get a sinusoidal input current shape [48]. Unity power factor can be achieved by align $\vec{I}_{ref}$ with the grid voltage vector. The reference $\vec{I}_{ref}$ can be approximated by two adjacent active vectors $\vec{I}_x, \vec{I}_y$ and a zero vector $\vec{I}_0$. For example, with $\vec{I}_{ref}$ falling into sector I as shown in the Fig. 2-5, it can be synthesized by $\vec{I}_x = \vec{I}_1, \vec{I}_y = \vec{I}_2$ and $\vec{I}_0$. In this section, all the analysis is done in the sector I which comprises of $\vec{I}_1$ and $\vec{I}_2$.

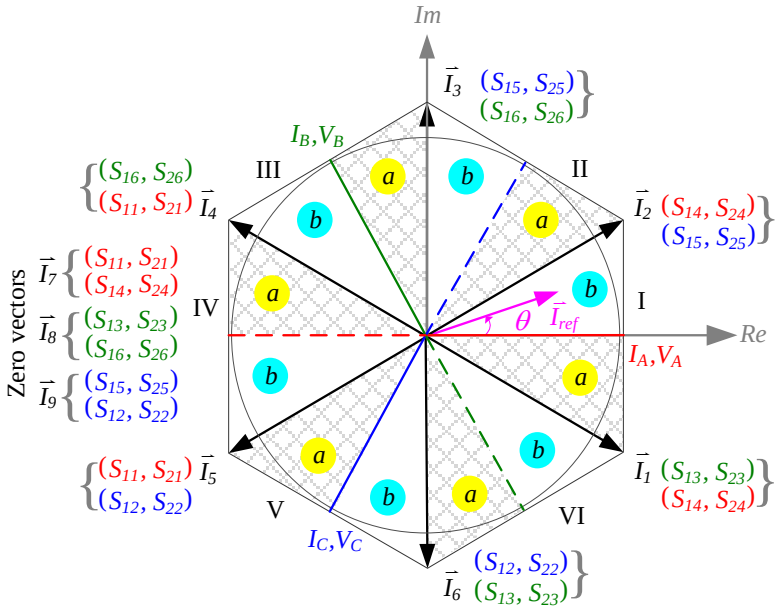
Assuming that output inductor current I_L is constant, the ampere-second balancing equation is thus given by

$$\vec{I}_{ref}T_s = \vec{I}_1T_1 + \vec{I}_2T_2 + \vec{I}_0T_0 \tag{2-3}$$

where T_1, T_2, and T_0 are the dwell times for the vectors $\vec{I}_1, \vec{I}_2$ and $\vec{I}_0$ respectively.



(a)



(b)

Fig. 2-4 Current Space vector representation. (a) $I_P = nI_L$, $V_P > 0$ and (b) $I_P = -nI_L$, $V_P < 0$.

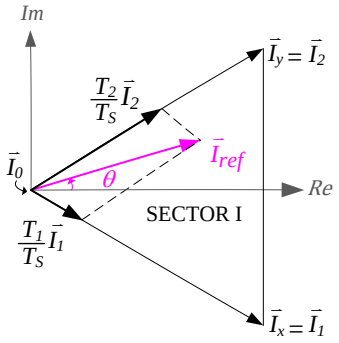


Fig. 2-5 Synthesis of $\vec{I}_{ref}$ by $\vec{I}_1, \vec{I}_2$ and, $\vec{I}_0$.

The dwell time for $\vec{I}_1, \vec{I}_2$ and $\vec{I}_0$ can be calculated as below:

$$\begin{cases} T_x = T_1 = m_a T_s \sin\left(\dfrac{\pi}{6} - \omega t\right) \\ T_y = T_1 = m_a T_s \sin\left(\dfrac{\pi}{6} + \omega t\right) \quad \text{for } -\dfrac{\pi}{6} \le \theta \le \dfrac{\pi}{6}, \\ T_0 = T_s - T_x - T_y \end{cases} \tag{2-4}$$

where m_a is the modulation index in the range of $0 \le m_a \le 1$, given by

$$m_a = \frac{1}{n}\frac{I_{ref}}{I_L} = \frac{I_m}{I_P} \tag{2-5}$$

in which I_m is the peak of the fundamental-frequency component in i_a.

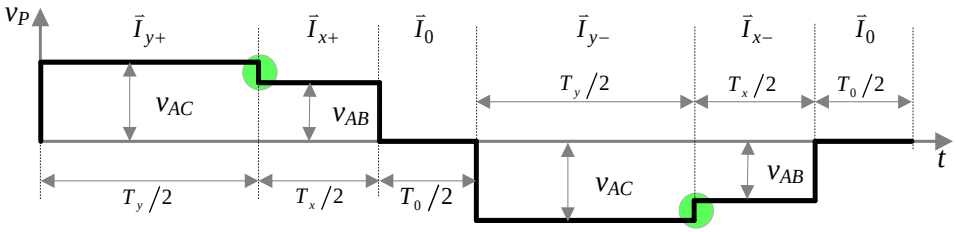
It is interesting to note that $\vec{I}_x$ is generated by "bridge *x*" while $\vec{I}_y$ is generated by "bridge *y*". Therefore the transformer primary voltage v_p is the bus voltage of "bridge *x*" (the line to line voltage associated with "bridge *x*") during the dwell time of $\vec{I}_x$ and is the bus voltage of "bridge *y*" (the line to line voltage associated with "bridge *y*") during the dwell time of $\vec{I}_y$. During the dwell time of zero vector $\vec{I}_0$, the transformer primary is bypassed through one of the phase leg and v_P is zero. In order to use transformer isolation, the primary voltage of the transformer v_P must be alternating positive and negative in high frequency to maintain the volt-sec balance. For

each active vector, there are two possible switching states depending on the direction of the current on the primary side of the transformer i_P as shown in Fig. 2-4. $\vec{I}_{x+}$ and $\vec{I}_{x-}$ represent the switching states of vector $\vec{I}_x$ when $i_P > 0$ and $i_P < 0$ respectively. In addition, $\vec{I}_{y+}$ and $\vec{I}_{y-}$ represent switching states of vector $\vec{I}_y$ when $i_P > 0$ and $i_P < 0$ respectively. By dividing $\vec{I}_x$ into $\vec{I}_{x+}$ and $\vec{I}_{x-}$ with equal dwell time and dividing $\vec{I}_y$ into $\vec{I}_{y+}$ and $\vec{I}_{y-}$ with equal dwell time, alternating voltage can be generated on the transformer primary side. It should be noted that the zero vector dwell time may also need to be divided in order to separate these active vectors. Depending on the arrangement of these active vectors and zero vectors, different switching pattern can be generated and can be identified by the transformer primary voltage waveform.

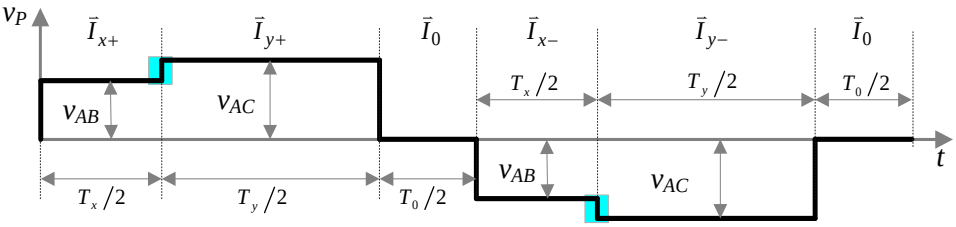
2.2 Several Practical PWM Schemes for Three-Phase Isolated Buck Matrix-Type Rectifier

For the analysis in this section, it is assumed the current reference vector $\vec{I}_{ref}$ in Fig. 2-5 is located in $0^\circ < \theta < 30^\circ$. During this interval the line-line voltage v_{AB} is lower than v_{AC} as shown in Fig. 2-2. The transformer primary voltage waveforms within a switching cycle with six-segment PWM schemes [30, 31, 49, 50] and eight-segment PWM scheme [32, 45], [51-53] are shown in Fig. 2-6. For the six-segment PWM scheme, the dwell time of each vector is divided by two ($T_x/2$, $T_y/2$, $T_0/2$) and the active vector $\vec{I}_x$ joints with active vector $\vec{I}_y$ ($\vec{I}_{x+}$ joints $\vec{I}_{y+}$ in positive half cycle and $\vec{I}_{x-}$ joints $\vec{I}_{y-}$ in negative half cycle). The switching patterns of the six-segment PWM are identified by the transition between the two attached active vectors. If the vector transition causes a step change in the transformer primary voltage from higher voltage magnitude to lower voltage magnitude the corresponding step change is defined as a high to low (HTL). Fig. 2-6 (a) shows the transformer primary voltage with HTL switching pattern within a switching cycle. It can be observed that there are two HTL step changes (regions in circle) in the positive half cycle and in the negative half cycle of the transformer primary voltage respectively.

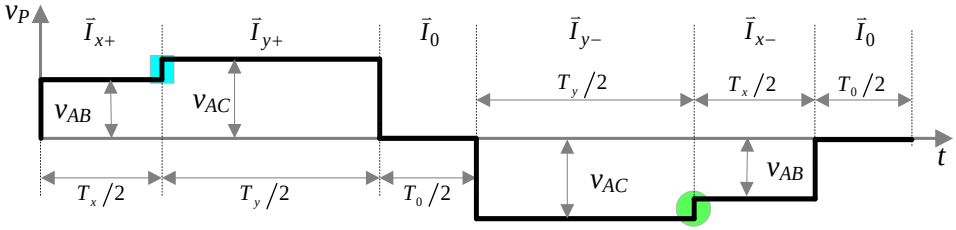
On the other hand, if the vector transition occurs from lower voltage magnitude to higher voltage magnitude, the corresponding step change is defined as a low to high (LTH). Fig. 2-6 (b) shows the transformer primary voltage with LTH pattern within a switching cycle. In addition, there is another type of six-segment switching pattern arrangement, which has different step change in each half-cycle, and it is defined as a hybrid pattern [31, 50, 51].



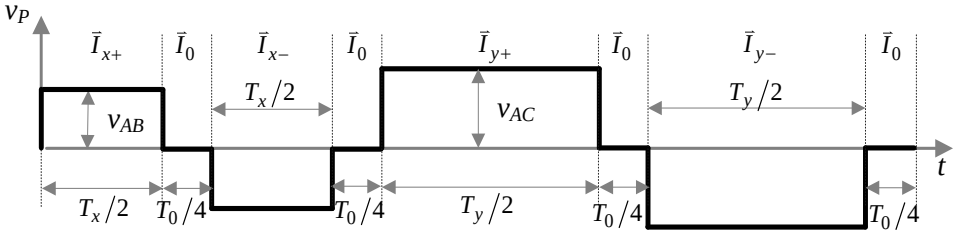
(a) Six-segment PWM with HTL pattern



(b) Six-segment PWM with LTH pattern



(c) Six-segment PWM with Hybrid pattern



(d) Eight-segment PWM pattern

Fig. 2-6 The transformer primary voltage within a switching cycle with different switching patterns when $\vec{I}_{ref}$ is located in $0^\circ < \theta < 30^\circ$.

Fig. 2-6 (c) shows Hybrid PWM pattern, with LTH step change in the positive half-cycle and HTL in the negative half-cycle. For the eight-segment PWM pattern, the dwell time of $\vec{I}_0$ is equally divided by four and inserted between active vectors as shown in Fig. 2-6 (d).

It is important to note that the turn-ON and turn-OFF switching losses corresponding to the transitions from zero vector to active vector and vice versa should not exhibit significant differences among different switching patterns in Fig. 2-6. However, the switching losses for two transitions HTL and LTH are different as discussed in detail in [54, 55]. The HTL transition exhibits low turn-on loss since the loss associated with this transition contains only energy of device capacitance $E_{oss}(V_{ds})$ which is fairly small due to low voltage transition. On the other hand, LTH has no turn-OFF switching loss but it suffers from large turn-ON switching losses. The turn-ON loss associated with the LTH includes E_{oss}, reverse recovery and triangular area due to overlapping voltage and current.

2.3 An Optimal PWM Scheme Candidate for MOSFET Devices

Fig 2-7 illustrates the transformer primary voltage waveforms with different PWM schemes within 60° interval of sector I. Depending on where the reference vector is located and how the vector sequences are arranged different switching patterns can be generated. As shown in Fig 2-7, as the reference vector moving within 60° interval of sector I, the magnitudes of two line-line voltages, v_{AB} and v_{AC} are varying. If the reference vector is located in $-30^\circ \le \theta < 0^\circ$, v_{AB} is greater than v_{AC} and if the reference vector is located in $0^\circ < \theta \le 30^\circ$, v_{AC} is greater than v_{AB}. Thus, for a given vector sequence, the switching pattern will be changed when the reference vector moves from the region of $\theta \in [-30^\circ, 0^\circ]$ to $\theta \in [0^\circ, 30^\circ]$. For example, "Type C" PWM in Fig. 2-7 (c) exhibits HTL switching pattern during interval of $-30^\circ \le \theta < 0^\circ$, and LTH switching pattern during interval of $0^\circ < \theta \le 30^\circ$ since similar vector sequence ($\vec{I}_{x+}, \vec{I}_{y+}, \vec{I}_0, \vec{I}_{x-}, \vec{I}_{y-}, \vec{I}_0$) is applied in both intervals.

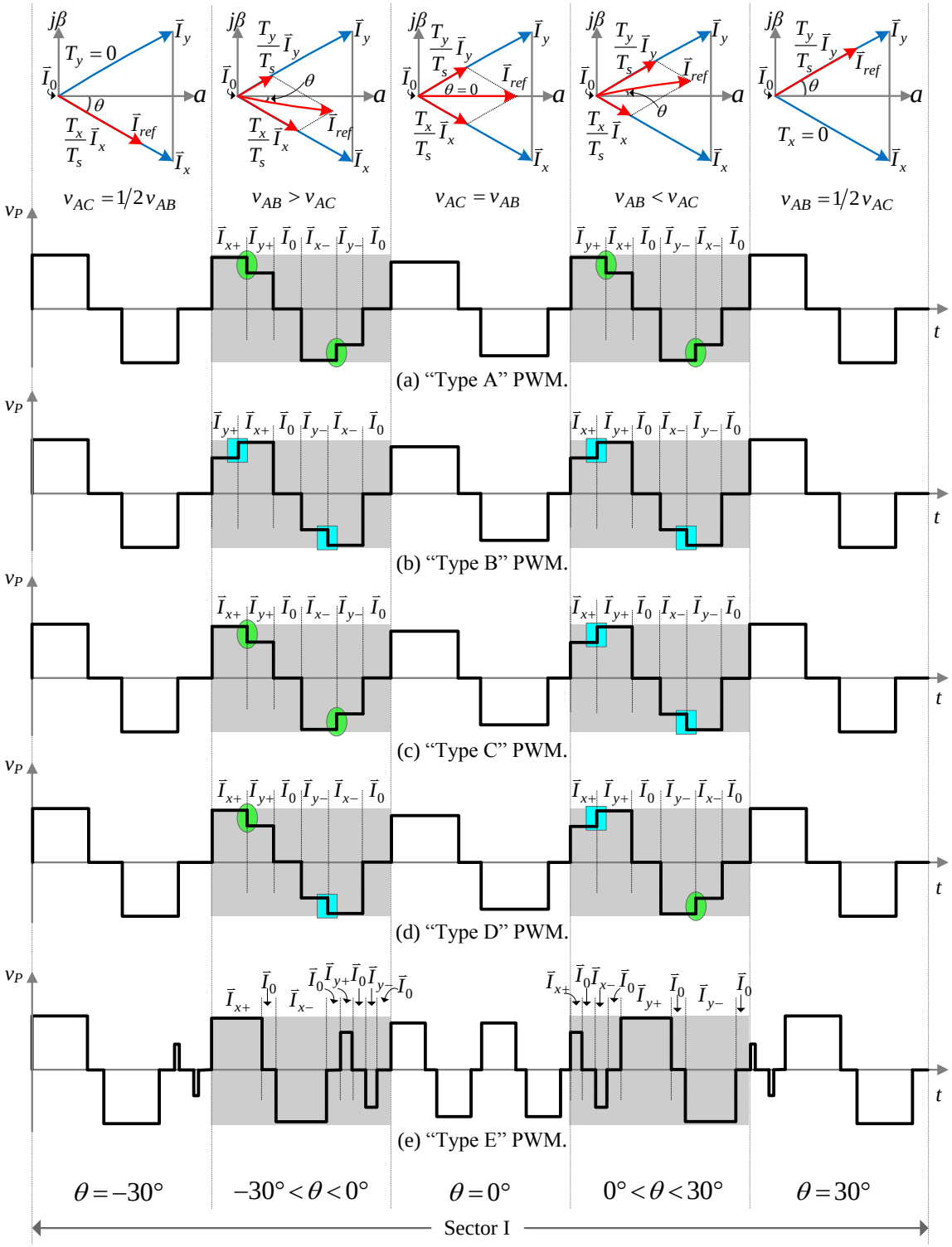


Fig. 2-7 Transformer primary voltage with different PWM schemes when $\bar{I}_{ref}$ is moving within sector I.

In order to maintain the same switching pattern during two intervals of $-30^{\circ} \le \theta < 0^{\circ}$ and $0^{\circ} < \theta \le 30^{\circ}$, the vector sequence of the two active vectors are swapped as shown in Fig. 2-7 (a) and (b). As shown in Fig. 2-7 (a), "Type A" PWM scheme always maintains HTL switching pattern with the vector sequence of $\vec{I}_{x+}, \vec{I}_{y+}, \vec{I}_0, \vec{I}_{x-}, \vec{I}_{y-}, \vec{I}_0$ during interval of $-30^{\circ} \le \theta < 0^{\circ}$ and $\vec{I}_{y+}, \vec{I}_{x+}, \vec{I}_0, \vec{I}_{y-}, \vec{I}_{x-}, \vec{I}_0$ during interval of $0^{\circ} < \theta \le 30^{\circ}$, whereas "Type B" PWM as shown in Fig. 2-7 (b) always maintains LTH switching pattern. "Type C" PWM pattern is the most popular PWM scheme [30, 31, 49] as a result of the simplicity of implementation since no sequence swapping is required during each sector. "Type D" PWM pattern is rarely used due to the drawback of asymmetrical voltage pulses across the transformer primary winding. As discussed earlier, the HTL transition exhibits lower turn-ON switching losses compared with the transition of LTH. Therefore, the proposed six-segment PWM scheme with HTL transition ("Type A") is one of the favorable PWM schemes for isolated buck matrix-type rectifier using MOSFETs as primary switches since it exhibits lowest turn-ON losses among all six-segment PWM schemes. It is also noteworthy to mention that "Type E" PWM scheme also allows the primary switches to turn on under ZVS condition except two switches as discussed in [45, 51]. However, later on in this chapter, the comparisons between the two PWM schemes "Type A" and "Type E" reveal that the "Type A" is the optimal PWM scheme for the MOSFET devices used in three-phase isolated buck matrix type rectifier due to its overall better performance.

2.4 Principle Operation of Rectifier with "Type A"PWM Scheme

As mentioned earlier in this chapter, the three-phase rectifier in Fig. 2-1 can be redrawn as two ZVS FB-PS DC-DC converters "bridge *x*" and "bridge *y*" as shown in Fig. 2-3. The circuit principal waveforms within 180° intervals with excessively increased switching period of PWM can be observed in Fig. 2-8. For example, in the sector I (a), the switches $S_{11,}\, S_{21}$ and $S_{16,}\, S_{26}$ of "bridge *x*" are turned on within time $T_x/2$ creating a positive voltage pulse $v_P = v_{AB}$ and a current pulse flowing from "phase *A*" into "phase *B*" with magnitude of I_P.

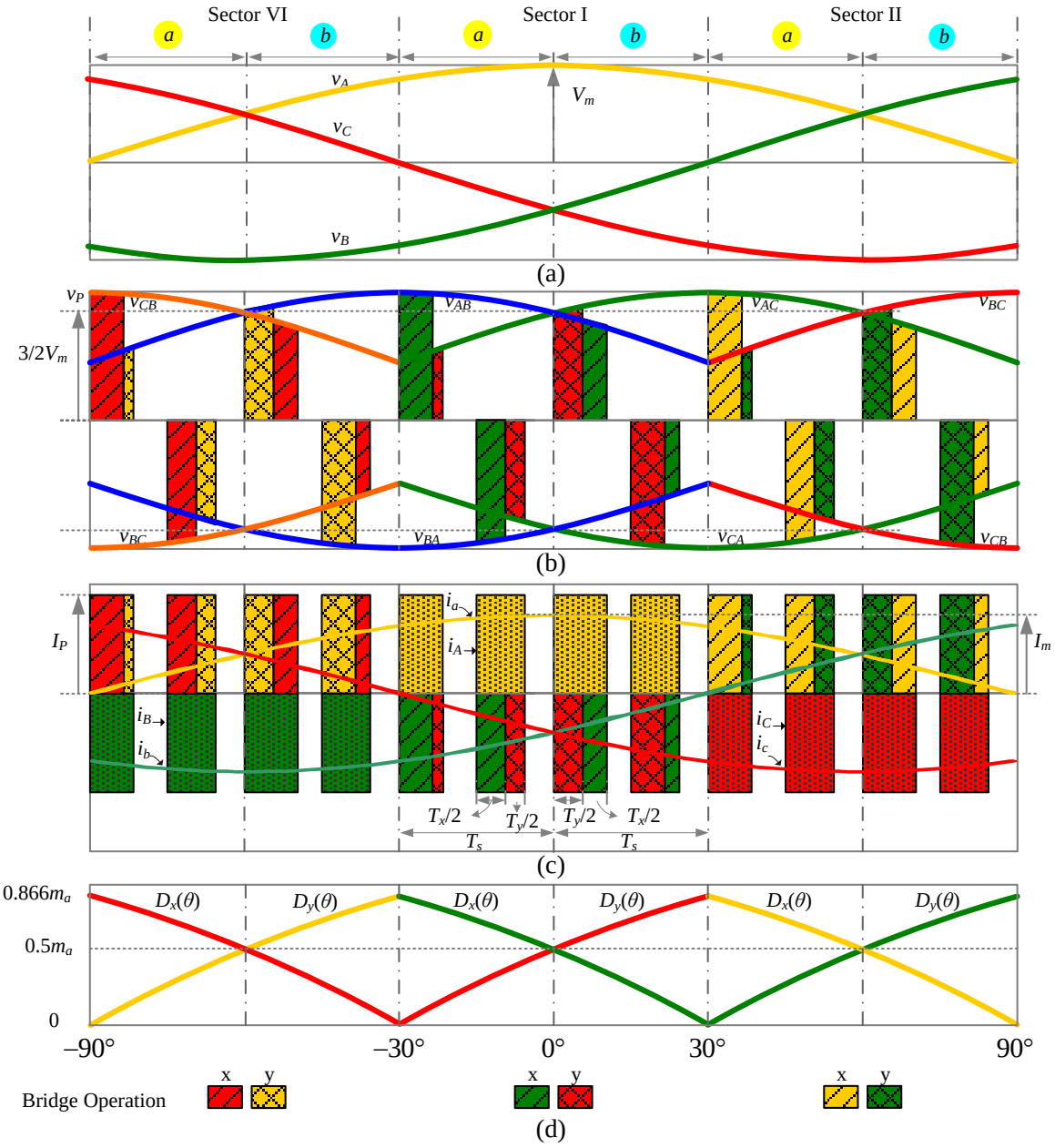


Fig. 2-8 Waveforms of "Type A" PWM with excessively increased switching period T_s: (a) phase voltages, (b) primary voltage, and (c) phase currents i_A, i_B and i_C (d) $D_x(\theta)$ duty-cycle of "bridge x" and $D_y(\theta)$ duty-cycle of "bridge y".

Then, S_{11}, S_{21} and S_{12}, S_{22} of "Bridge y" are turned on within time $T_y/2$ creating a positive voltage pulse $v_P = v_{AC}$ and a current pulse flowing from "phase A" into "phase C" with

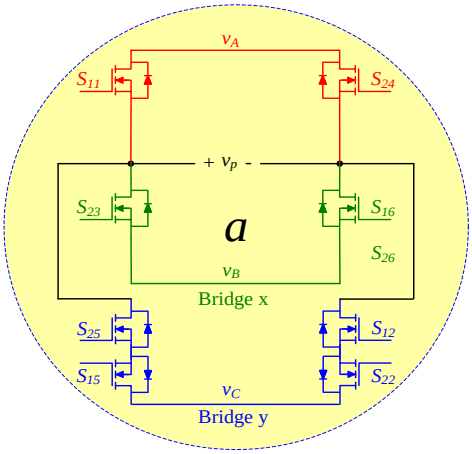
magnitude of I_P. In order to keep the transformer flux balanced, a negative voltage pulse of the same duration is next generated by turning on switches S_{14}, S_{24} and S_{13}, S_{23} of "bridge *x*" and S_{14}, S_{24} and S_{15}, S_{25} of "bridge *y*". It should be noted that the grid side currents shown in Fig. 2-8 (c) remain the same regardless the alternation of the transformer current. In order to realize "Type A" PWM, the sequence of the two attached active vectors needs to be swapped in the middle of each sector. As shown Fig. 2-8 (b) - (d), the pulse with larger voltage magnitude and duty-cycle always starts first. The phase currents are synthesized by the current pulses with a constant magnitude of I_P. The duty cycles $D_x(\theta) = T_x/T_s$ and $D_y(\theta) = T_y/T_s$ of the input current pulses shown in Fig. 2-8 (c) and (d) within the chosen 60° interval (sector I) are given by

$$\begin{bmatrix} T_x/T_s \\ T_y/T_s \\ (T_x+T_y)/T_s \end{bmatrix} = \begin{bmatrix} -i_b(\theta)/I_P \\ -i_c(\theta)/I_P \\ i_a(\theta)/I_P \end{bmatrix} = m_a \begin{bmatrix} -i_b(\theta)/I_m \\ -i_c(\theta)/I_m \\ i_a(\theta)/I_m \end{bmatrix}. \tag{2-6}$$

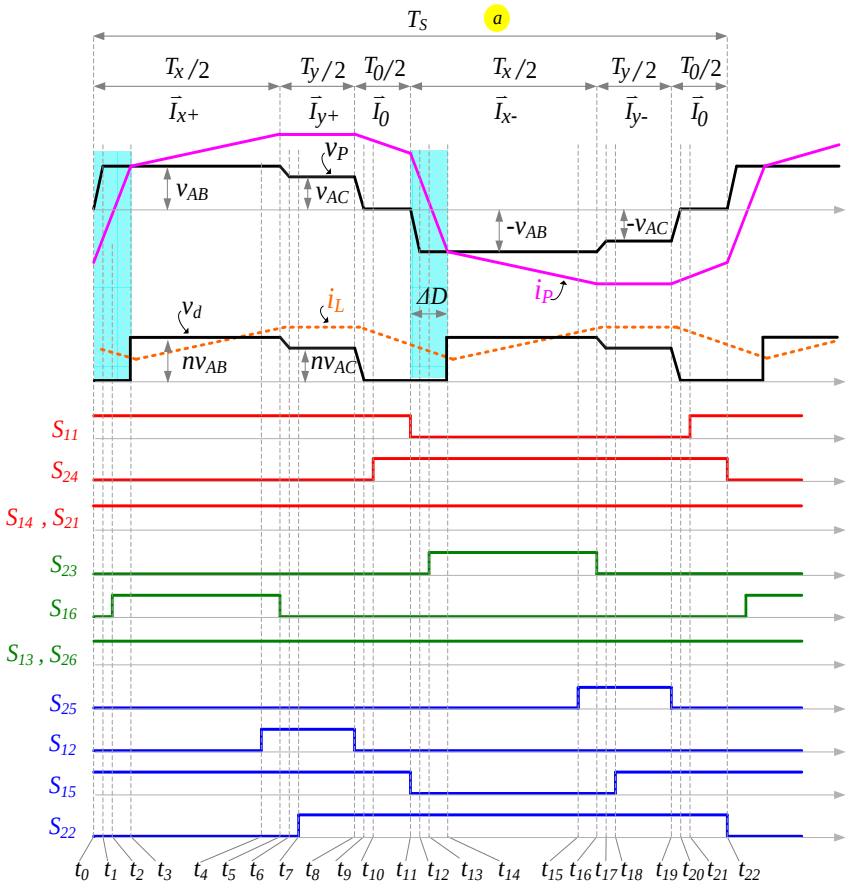
It can be observed that for a given m_a the duty-cycle of current pulse for each phase is proportional to its fundamental current. Then, m_a can be used to adjust the three-phase current magnitude without affecting their sinusoidal shape.

2.5 Analysis of ZVS Transition and Commutation Method for "Type A" PWM Scheme

The analysis performed in this section and next section is based on the assumption that the forward voltage drop across the diodes and the MOSFETs is zero, and that the rectifier diode capacitances are equal to zero. The complete operation of the three-phase converter during one switching period T_s is illustrated in Fig. 2-9 and Fig. 2-10. It shows the circuit waveforms of primary voltage v_P and current i_P, the rectified secondary voltage V_d and output inductor current i_L and the corresponding switch gate signals in sector I (a) and (b). In sector I (a) $\theta \in [-\pi/6, 0]$, v_{AB} is greater than v_{AC} and in sector I (b) $\theta \in [0, \pi/6]$, v_{AC} is greater than v_{AB}.

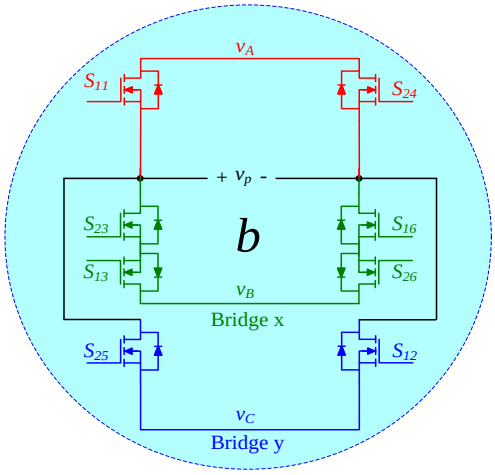


(a) subtopology circuit

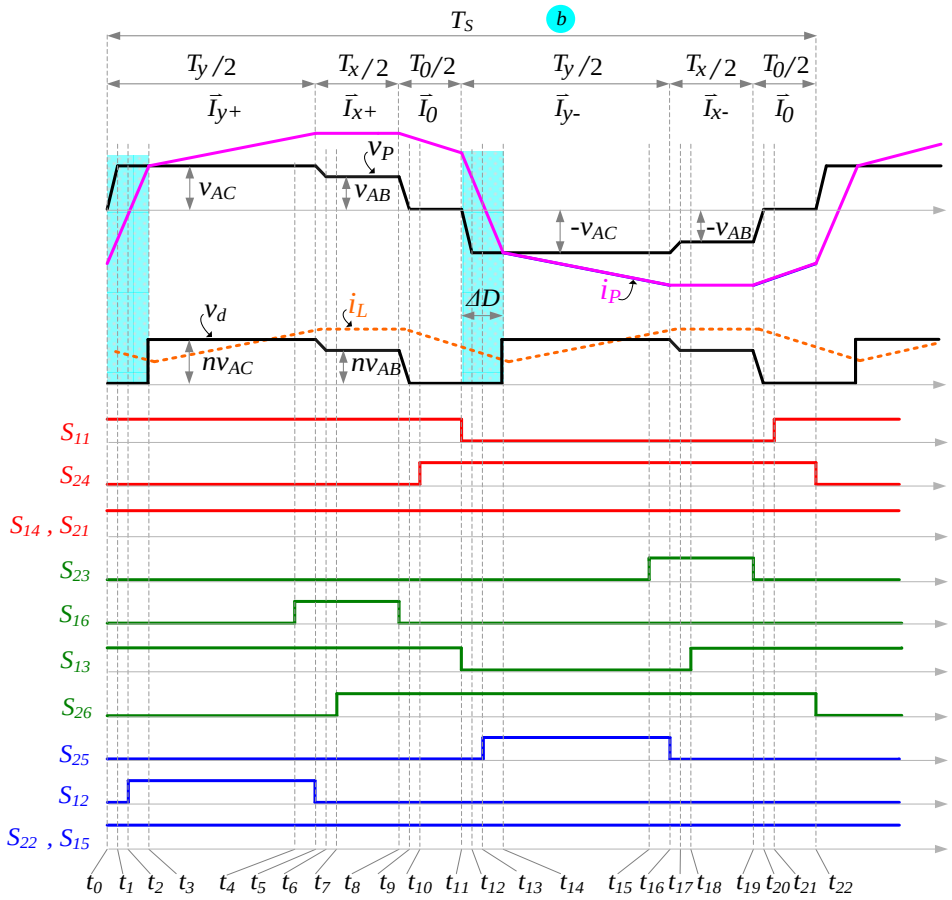


(b) proposed PWM waveforms

Fig. 2-9 Sector I (a) when $\theta \in [-\pi/6, 0]$ $v_{AB} > v_{AC}$:



(a) subtopology circuit



(b) proposed PWM waveforms

Fig. 2-10 Sector I (b) when $\theta \in [0, \pi/6]$ $v_{AC} > v_{AB}$:

The six switches ($S_{21,}$ $S_{14,}$ $S_{13,}$ $S_{26,}$ $S_{15,}$ S_{22}) discussed above function as synchronous rectification to bypass their body diodes since they are forward biased. The rest of the six switches ($S_{11,}$ $S_{24,}$ $S_{23,}$ $S_{16,}$ $S_{25,}$ S_{12}) operate in a similar manner of FB-PS converter to achieve ZVS. As shown in Fig. 2-9 and Fig. 2-10, at the leading edge transitions of v_P (t_0-t_2, and t_{11}-t_{13}), the energy stored in the leakage inductance is utilized to charge and discharge the parasitic capacitances of the switches. However, at the trailing edge transitions of v_P (t_8-t_{10}, and t_{19}-t_{21}), the combined energy stored in both the leakage inductance and the output inductor is utilized to charge and dischrge the parasitic capacitances of the switches. Two-step commutation can be applied for both leading and trailing edge transitions.

Table 2-1 Constraints of SR Operation.

sector		Complimentary Switches		
		SR		Active
I	a	S_{15}	$\rightarrow$	$\bar{S}_{23}$
		S_{22}	$\rightarrow$	$\bar{S}_{16}$
	b	S_{13}	$\rightarrow$	$\bar{S}_{25}$
		S_{26}	$\rightarrow$	$\bar{S}_{12}$
II	a	S_{16}	$\rightarrow$	$\bar{S}_{24}$
		S_{23}	$\rightarrow$	$\bar{S}_{11}$
	b	S_{14}	$\rightarrow$	$\bar{S}_{26}$
		S_{21}	$\rightarrow$	$\bar{S}_{13}$
III	a	S_{11}	$\rightarrow$	$\bar{S}_{25}$
		S_{24}	$\rightarrow$	$\bar{S}_{12}$
	b	S_{15}	$\rightarrow$	$\bar{S}_{21}$
		S_{22}	$\rightarrow$	$\bar{S}_{14}$
IV	a	S_{12}	$\rightarrow$	$\bar{S}_{26}$
		S_{25}	$\rightarrow$	$\bar{S}_{13}$
	b	S_{16}	$\rightarrow$	$\bar{S}_{22}$
		S_{23}	$\rightarrow$	$\bar{S}_{15}$
V	a	S_{13}	$\rightarrow$	$\bar{S}_{21}$
		S_{26}	$\rightarrow$	$\bar{S}_{14}$
	b	S_{11}	$\rightarrow$	$\bar{S}_{23}$
		S_{24}	$\rightarrow$	$\bar{S}_{16}$
VI	a	S_{14}	$\rightarrow$	$\bar{S}_{22}$
		S_{21}	$\rightarrow$	$\bar{S}_{15}$
	b	S_{12}	$\rightarrow$	$\bar{S}_{24}$
		S_{25}	$\rightarrow$	$\bar{S}_{11}$

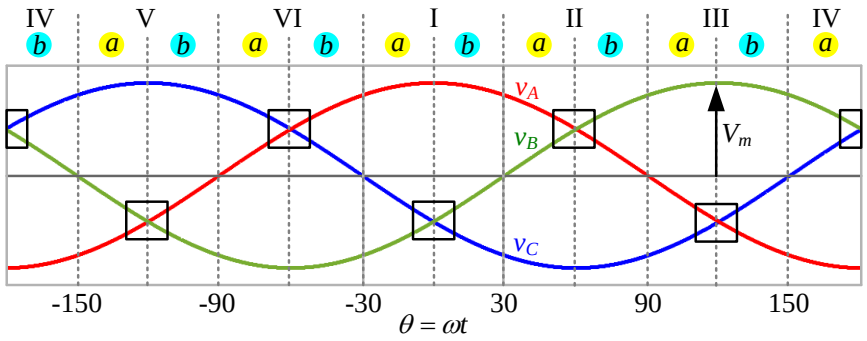


Fig. 2-11 Input phase voltages with sector division. In the vicinity of each bundary between part a and part b (inside the retangular box), two phase voltages are very close and contraints of the SR switches associated with both these two phases need to be applied.

It is important to note that the transitions between two active vectors (t_4-t_7, and t_{15}-t_{18}) require three commutation steps which consist of two-step commutation with ZVS and one additional commutation step with non-ZVS turn-ON. The two-step commutation for this transition with ZVS is realized in the same manner as trailing edge and since the transition voltage is low, ZVS can be easily achieved even at very light load. The turn-on loss associated with the non-ZVS switch is very small since it is turned on at zero current at low transition voltage.

It is important to mention that there are always two synchronous rectification switches in one of the phase legs where the phase voltage has the potential between the other two phases cannot be kept always on. They should be complimentary with other two active switches in another phase leg to avoid short circuit between these two phases. Different two switches will be selected to apply this constraint when the current reference vector moves from one sector to another sector and from part a to part b within each sector as summarzied in Table 2-1.

However, in the real three-phase system, the phase voltages might be distorted or unbalanced such that in the vicinity of the boundary between sector I (a) and I (b) (inside rectangular box in Fig. 2-11), the voltage difference between the two phase voltages may have reversed polarity compared with ideal cases. Therefore, in the vicinity of the boundary between “sector a” and “sector b”, switching constraints for both “sector a” and “sector b” need to be applied.

2.6 Steady-State Analysis of "Type A" and Performance Comparison with "Type E"

In this section, duty-cycle loss, output inductor current ripple and switching losses of the "Type A" and "Type E" PWM are compared. Also, the comparison indicates that the input current THDs of the converter are not significantly impacted by the two PWM patterns.

2.6.1 Analysis of Duty-Cycle Loss

The duty-cycle loss is one of the major limitations of operating at higher switching frequency and it generates circulating current on the primary of the transformer which results in conduction losses and poor input current THD. Selection of the transformer turns ratio, n, and the modulation index m_a is related to the loss of duty cycle, which depends on the choice of the switching frequency, leakage inductance, and the ZVS range. The duty-cycle loss ΔD_x happened at the transition from zero vectors to active vectors due to the finite transition time depending on the value of L_{lk} and the primary side voltage v_P as shown in Fig. 2-12 in the shaded area. During duty-cycle loss interval, the output inductor current is still freewheeling through the bridge rectifier and the transformer secondary voltage is clamped to zero. The primary current i_P swing from one direction to another direction and, as a result, the two input currents i_A and i_B (due to the bridge x duty-cycle loss in sector I (a)) contain two triangles A_1 and A_2 since the input phase current is synthesized by i_P. These two areas are canceled each other and result in zero net current during interval ΔD_x. Therefore, ΔD_x will not contribute to either the input phase-current or the output power, but generate losses due to the circulating current. The loss of duty-cycle will also affect the input current THD and output voltage ripple if the applied duty cycle is not compensated. As shown in Fig. 2-13, the duty-cycle applied to each phase follows the same shape as the phase current since the phase current is proportional to its duty-cycle. Due to the duty-cycle loss, however, the effective duty cycle (dashed-line) is lower than applied duty cycle (solid line). Then the curve of effective duty-cycle will contain step changes which occurred

every 60° interval as shown in Fig. 2-13. As discussed above, the phase current is determined by the effective duty-cycle so that the phase currents are also distorted causing higher THD. In addition, this will introduce low frequency harmonics into the output voltage as well. In order to eliminate these issues, the applied duty-cycle needs to be compensated such that the effective duty-cycle (which is also the secondary duty-cycle $D_{sx}(\theta) = T_{sx}/T_s$ and $D_{sy}(\theta) = T_{sy}/T_s$) satisfy the condition below:

$$\begin{aligned} D_{sx}(\theta) &= -m_a(I_b(\theta)/I_m) \\ D_{sy}(\theta) &= -m_a(I_c(\theta)/I_m) \end{aligned} \tag{2-7}$$

Then, the primary duty-cycle with duty-cycle compensation is defined as:

$$\begin{aligned} D_x(\theta) &= D_{sx}(\theta) + 2\Delta D_x(\theta) \\ D_y(\theta) &= D_{sy}(\theta) \end{aligned} \tag{2-8}$$

Since there is no duty-cycle loss for the transition from $\vec{I}_x$ to $\vec{I}_y$, the effective duty-cycle $D_{sy}(\theta)$ is equal to the applied duty-cycle $D_y(\theta)$. It should be noted that the duty-cycle loss will reduce the maximum available m_a, which is the effective duty-cycle at the peak of phase current.

The maximum loss of duty-cycle is obtained when the magnitude of $v_P(\theta)$ is minimum at $\theta = 0^\circ$ and $v_P(\theta) = 3/2V_m$. The maximum total loss of duty-cycle in term of the output load is given by equation (12):

$$\Delta D_{total\_\max} = \frac{4n^2 m_a L_{lk}}{R_o T_s} \tag{2-9}$$

where L_{lk} is the leakage inductance, n is the transformer turns ratio, and $R_o = V_o/I_o$ is the load resistance. After the duty-cycle compensation, given in (2-8), the maximum applied duty-cycle happened at $\theta = 0^\circ$ since both the effective duty-cycle and the loss of duty-cycle attain their maximum values at $\theta = 0^\circ$. Because the applied duty-cycle cannot exceed one, the maximum available effective duty-cycle is given by

$$D_{sx\_\max} = 1 - 2\Delta D_x(0). \tag{2-10}$$

Then, the effective m_a should be in the range of $[0, D_{sx\_\max}]$. Outwardly; large loss of duty-cycle reduces the range of the effective m_a and generates higher conduction loss. Compared with "Type A" PWM, the "Type E" has two additional duty-cycle losses, ΔD_y as shown in Fig. 2-14. The intervals of ΔD_y is longer than intervals of ΔD_x since ΔD_y is associated to the narrower pulse where the magnitude of $v_p(\theta)$ is lower. At the extreme case, when $\theta = \pm 30^\circ$, the interval of ΔD_y is twice of the interval of ΔD_x as shown in Fig. 2-14 (e) and (f) where the magnitude of $v_P(\theta)$ is only half of that during intervals of ΔD_x. In spite of the two missing pulses $\vec{I}_{y+}$ and $\vec{I}_{y-}$ on the secondary side at $\theta = \pm 30^\circ$, two pulses of $\vec{I}_{y+}$ and $\vec{I}_{y-}$ on the primary side always exist in order to compensate the duty-cycle loss as shown in the Fig. 2-14 (f). Therefore, these two pulses contribute no power to the output load, but create conduction and switching losses on the primary side of the transformer. The total duty-cycle losses for "Type A" and "Type E" PWM schemes are compared at different angle θ as provided in Table 2-2. In order to make an easier comparison, the total duty-cycle losses are normalized by using the total duty-cycle loss of "Type A" PWM at $\theta = 0^\circ$ as a base. It is interesting to note that the total duty-cycle loss of "Type E" PWM is two to three times higher than the "Type A" PWM if the same value of L_{lk} is used. In other words, if both designs have the same duty-cycle losses, the "Type A" PWM can achieve ZVS with wider load range.

Table 2-2 Comparison of Normalized Total Duty-Cycle Losses.

θ	ΔD_{total} of "Type A" PWM	ΔD_{total} of "Type E" PWM
$\theta = 0^\circ$	1	2
$-30^\circ < \theta < 0^\circ$ $0^\circ < \theta < 30^\circ$	$\sqrt{3}/2 < \Delta D_{total} < 1$	$2 < \Delta D_{total} < 3\sqrt{3}/2$
$\theta = \pm 30^\circ$	$\Delta D_{total} = \sqrt{3}/2$	$\Delta D_{total} = 3\sqrt{3}/2$

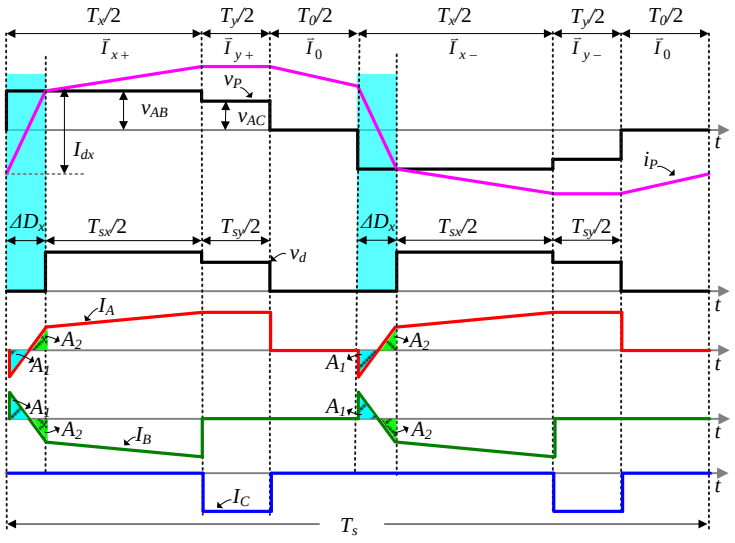


Fig. 2-12 Waveforms of the steady state operation in sector I (a).

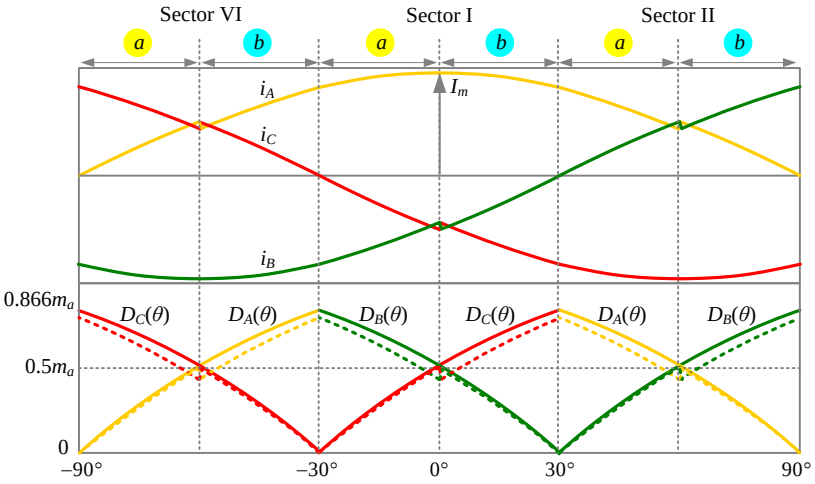


Fig. 2-13 Distorted input phase current waveforms without duty-cycle compensation (solid line: applied duty-cycle; dashed line: effective duty-cycle).

This significantly reduces the turn-on switching losses at lighter load. The reduction of duty-cycle loss also enables the operation of the converter at higher m_a and reduces the power loss caused by the circulating current in primary side switches.

2.6.2 Analysis of Output Inductor Current Ripple

For a given output voltage, the output inductor current ripple at steady-state is determined by the off-time of the output bridge rectifier voltage V_d. The off-time of V_d consists of the dwell time of zero vectors and the time intervals of duty-cycle loss. Fig. 2-14 shows the output inductor current ripple of "Type A" and "Type E" PWMs varying with phase angle θ due to the variable off-time of V_d. At θ = 0º, the total off-time of V_d is minimum and is given by $(1-m_a)T_s$.

Therefore, the current ripple for both "Type A" and "Type E" PWM schemes reaches the minimum value at θ = 0º. For "Type E" PWM, the off-time of V_d is divided into four intervals while for "Type A" PWM, the off-time of V_d is divided into two intervals as shown in Fig. 2-14 (a) and (b). Then the current ripple for both "Type A" and "Type E" PWMs is respectively given by

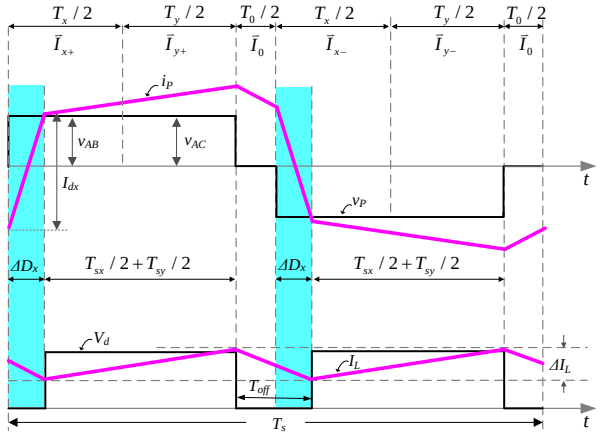
$$\Delta I_{min} = \frac{V_o(1-m_a)T_s}{2L_o} \tag{2-11}$$

$$\Delta I_{min} = \frac{V_o(1-m_a)T_s}{4L_o}. \tag{2-12}$$

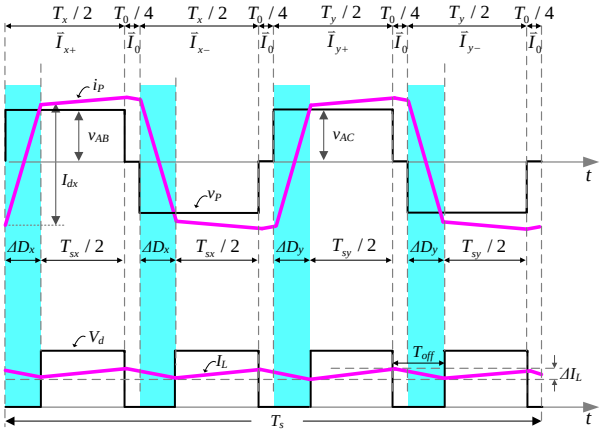
As shown in (2-11) and (2-12), the minimum current ripple of "Type E" PWM is only half of that of "Type A" PWM. At $\theta = \pm 30^{\circ}$, the total off-time of V_d is maximum and can be derived as $(1-\sqrt{3}/2\,m_a)T_s$. Therefore, the output current ripples of "Type A" and "Type E" PWMs reach the maximum values as shown in Fig. 2-14 (e) and (f). For "Type A" PWM, the off-time of V_d is still equally divided by two. The current ripple can be derived as

$$\Delta I_{\max} = \frac{V_o(1-\sqrt{3}/2\,m_a)T_s}{2L_o}. \tag{2-13}$$

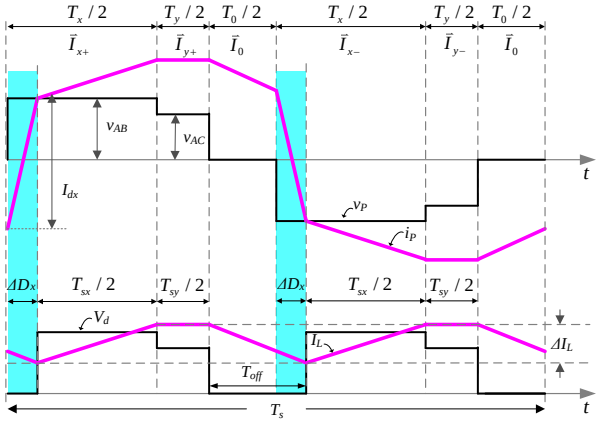
For the "Type E" PWM, three of the off-time intervals adjacent to the narrow pulses merge into one, resulting in larger current ripple.



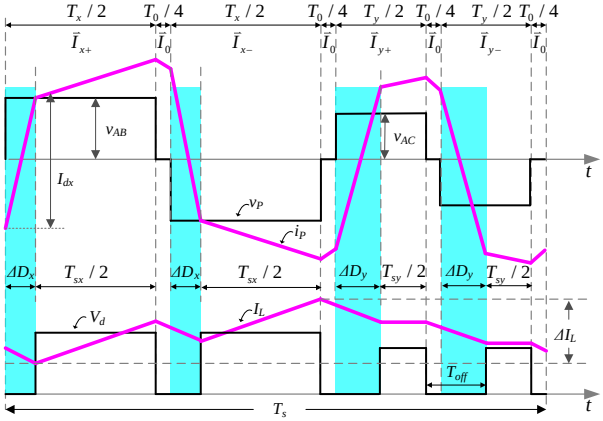
(a) "Type A" at $\theta = 0°$



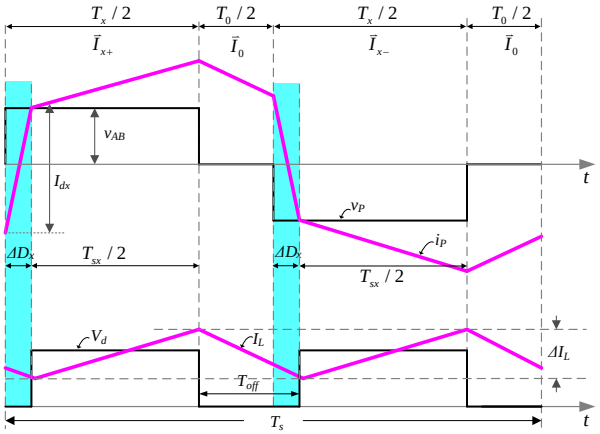
(b) "Type E" at $\theta = 0°$



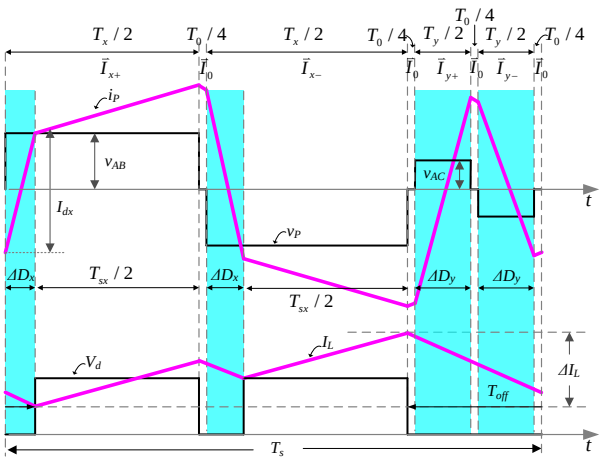
(c) "Type A" at $-30° < \theta < 0°$



(d) "Type E" at $-30° < \theta < 0°$



(e) "Type A" at $\theta = -30°$



(f) "Type E" at $\theta = -30°$

Fig. 2-14 Comparison waveforms of the duty-cycle loss and the output inductor current ripple for "Type A" and "Type E" PWM.

For example, at $\theta = -30^{\circ}$, the two pulses of $\vec{I}_{y+}$ and $\vec{I}_{y-}$ on the secondary side disappear so that three of the off-time intervals merge into one large interval as shown in Fig. 2-14 (f). Assuming that the difference between ΔD_x and ΔD_y is relatively small and can be ignored, the maximum current ripple of the "Type E" PWM can be derived as

$$\Delta I_{\max} = \frac{3V_o(1-\sqrt{3}/2\,m_a)T_s}{4L_o}. \tag{2-14}$$

In summary, the minimum current ripple in "Type A" PWM (at $\theta = 0^{\circ}$) is higher than "Type E" PWM by two times. This is one of the drawbacks of "Type A" PWM. However the maximum current ripple in the "Type A" PWM (at $\theta = \pm 30^{\circ}$) is smaller than that of "Type E" PWM. It is important to observe that, the frequency across the transformer with "Type E" is double of the "Type A" PWM, given that both PWM schemes have the same T_s. Then, the lower core loss and smaller core of the transformer can be expected with "Type E" PWM. However, "Type E" PWM will not offer a significant benefit in transformer design if the transformer is designed based on the maximum flux density which is normally the most important constraints for the transformer design. As shown from the primary side voltage of the transformer v_P in Fig. 2-14 (f), two pulses associated with v_{AB} attains its maximum magnitude and the other two pulses associated with v_{AC} reach to minimum. As a result, both PWM schemes attain the same maximum flux density on the primary side of the transformer at the vicinity of $\theta = \pm 30^{\circ}$, although the transformer with of "Type A" operates at half of the frequency of "Type E" PWM.

2.6.3 Analysis of Switching Loss

The analysis in this section is based on the switching operation in sector I (a) and this remains true for all the sectors due to the repetitive feature of the switching pattern. In addition, switching losses can be analyzed for turn-on and turn-off actions within a switching cycle. As shown in Fig. 2-10, there are eight turn-on switching actions (four per each half-cycle) and eight turn-off switching actions (four per each half-cycle). In the first half-cycle, S_{16}, S_{22}, and S_{24} are

turned on under ZVS while S_{12} is non-ZVS turn-ON. Before the MOSFET S_{12} is turned on the drain-source voltage V_{ds} is $(v_{AC} - 1/2\, v_{AB})$ and it varies from 0 to $3/4 V_m$ during one 30° interval and the current I_{ds} through this switch is zero. Since S_{12} is turned on at zero current to discharge the energy stored in output capacitance C_{oss} of MOSFETs S_{12} and S_{22}, the turn-on loss should be very small. Three turn-off actions in the first half-cycle contribute to the switching losses since S_{24}, S_{16}, and S_{12} are turned off at full current while S_{22} is turned off at zero current. Switching loss is also a function of the voltage transition across the switching device. Because the voltage transition between two joint active vectors is only the difference of the two line-line voltages, the turn-off loss of S_{16} corresponding to this transition is much smaller than that of the other two switches S_{24} and S_{12}. The number of switching actions and resulted switching losses in the second half-cycle are the same as the first half-cycle, but different switches are involved which will not be discussed here. In summary, six turn-off and two non-ZVS turn-on actions contribute to switching losses within one switching cycle of "Type A" PWM. For "Type E" PWM, there are ten turn-ON and turn-OFF actions within one switching cycle. As discussed in [45], two turn-ON and eight turn-OFF actions contribute to switching losses. It is also important to note that the losses associated to two non-ZVS turn-ON actions are very small for both PWM schemes due to low voltage transition prior to turn on [54].

Table 2-3 Switching Loss Comparison of "Type A" and "Type E" PWM Under ZVS Operation.

	"Type A"	"Type E"
Total number of turn-on or turn-off actions	8	10
Number of turn-on actions with ZVS	6	8
Number of turn-on actions with non-ZVS	2	2
Number of turn-off actions with high voltage transition of $(\sqrt{3}/2 V_m \sim \sqrt{3} V_m)$	4	8
Number of turn-off actions with low voltage transition of $(0 \sim \sqrt{3}/2 V_m)$	2	0
Total turn-on losses	ignorable	ignorable
Total turn-off losses (normalize based on 6-segment)	1	1.6

Compared with “Type A” PWM, “Type E” PWM has noticeable higher turn-off losses due to two reasons. First, more turn-OFF actions contributes to switching losses. Second, all the turn-off actions are switched at high voltage transition. The switching loss comparison between “Type A” and “Type E” is summarized in Table 2-3.

2.7 Experimental Verification

Table 2-4 Experimental Prototype parameters

L_f	90 μH	V_o	345 V
C_f	10 μF	n	2
f_{TR} of “Type A”	50 kHz	f_{TR} of “Type E”	100 kHz
f_{grid}	60 Hz	$L_{lk\_Six\_Seq}$ $L_{lk\_eight\_Seg}$	5.7 μH 3.2 μH
$V_{LL,rms}$	180 V	T_r	ZP47313TC
L_o	450 μH	S_{11} - S_{26}	IPW60R041P6
C_o	220 μF	D_1 - D_4	SCS215KG

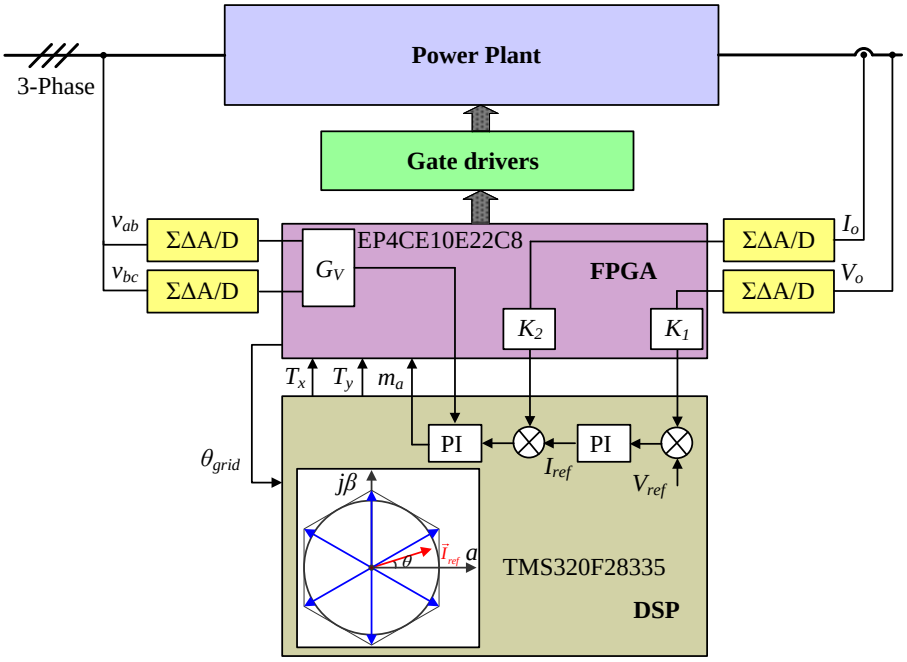
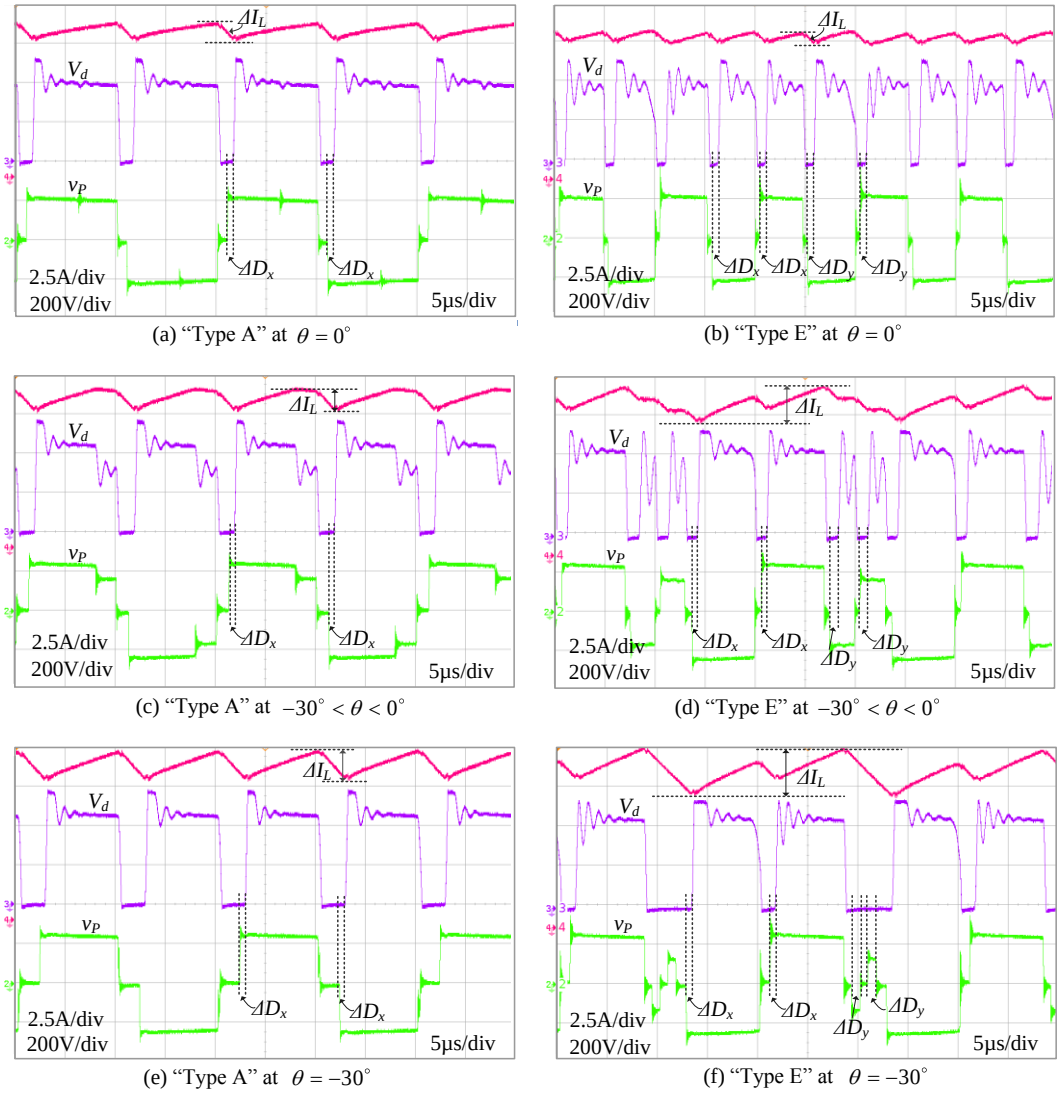


Fig. 2-15 Controller block diagram.

The purpose of the experimental results in this section is to validate the performance (duty-cycle loss, output inductor current ripple, dynamic switching behavior and input current THD) of the isolated buck matrix-type rectifier with "Type A" and "Type E" PWM schemes. The prototype is setup at 3.4 kW output power and 600 V Si-MOSFETs are employed for the primary bidirectional switches of the rectifier. A RCD snubber is added at the output of the bridge diode rectifier in Fig. 2-1 to reduce the high voltage spike. Detailed experimental system parameters are listed in Table 2-4. It is also important to note that the value of L_{lk} is calculated by (A-6) with considering 10% duty-cycle loss at full load current. The controller block diagram of the experimental prototype is shown in Fig. 2-15.

2.7.1 Experimental Waveforms for Duty-cycle Loss and Output Inductor Current Ripple

The duty-cycle loss can be identified as the intervals ΔD_x and ΔD_y as shown in the Fig. 2-16. In one cycle, the duty-cycle loss in "Type E" contains four intervals (two associated with wide pulses and two associated with narrow pulses) as shown in Fig. 2-16 (b), (d) and (f). The duty-cycle loss of proposed PWM only contains two intervals in one cycle as shown in Fig. 2-16 (a), (c) and (e). In "Type E" PWM, the two intervals associated with the two wide pulses have the same duration as that of "Type A" PWM, while the other two intervals associated with the two narrower pulses have longer duration because the voltage across the transformer is lower and i_p has longer ramping time. Therefore, the total duty loss in "Type E" is more than twice of the total duty-cycle loss of the proposed "Type A" PWM. Although the operating frequency of the "Type A" PWM is only half of "Type E" PWM, the maximum output current ripple in "Type A" is lower than the "Type E" PWM by more than 20% as shown in Fig. 2-16 (e) and (f). However, the minimum output current ripple in "Type A" is twice larger than "Type E" as shown in Fig. 2-16 (a) and (b).



(a) "Type A" at $\theta = 0^\circ$ (b) "Type E" at $\theta = 0^\circ$

(c) "Type A" at $-30^\circ < \theta < 0^\circ$ (d) "Type E" at $-30^\circ < \theta < 0^\circ$

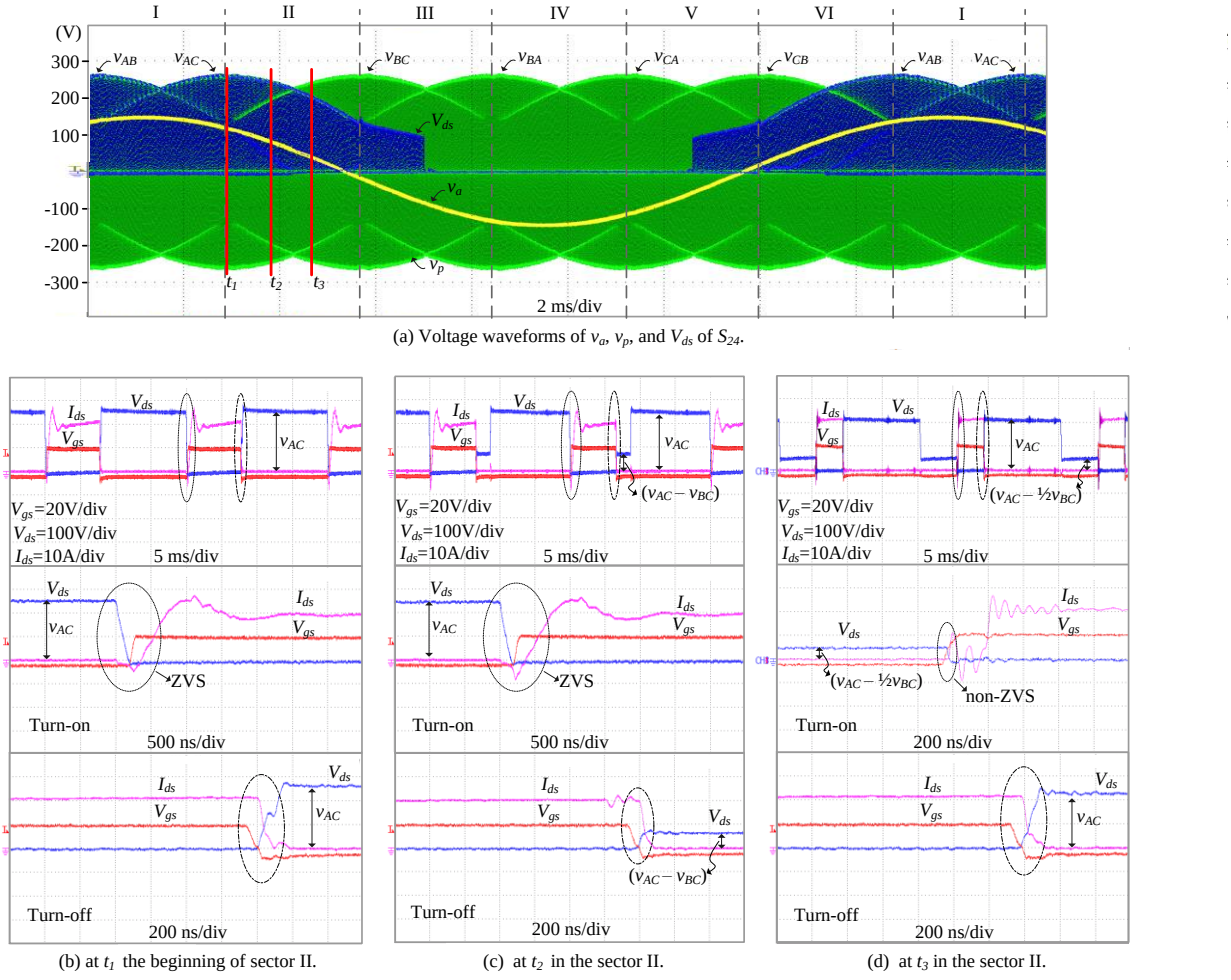
(e) "Type A" at $\theta = -30^\circ$ (f) "Type E" at $\theta = -30^\circ$

Fig. 2-16 Experimental waveforms of the transformer primary voltage v_P, rectifier voltage V_d and inductor current ripple ΔI_L.

2.7.2 Converter MOSFET Switching Dynamics Behavior with "Type A"PWM

It is crucial to observe the ZVS operation of the MOSFET switches in the converter with "Type A" implementation, since the ZVS operation is an indicator of switching loss reduction. To demonstrate the state of ZVS, switch S_{24} on the phase "leg A" is selected, thereby showing

the ZVS of all active switches. Fig. 2-17 (a) shows the voltage waveforms of "phase *A*" voltage v_a, the primary voltage of the transformer v_P and the drain-source voltage V_{ds} of MOSFET S_{24} in six sectors operation. The MOSFET turn-on and turn-off switching transitions are analyzed at three locations of t_1, t_2 and t_3 in sector II. At t_1 and t_2, S_{24} turn-on represents the ZVS turn-on action for the transition from zero vectors to active vectors, while S_{24} turn-off represents the turn-off action for the transition between the two joint active vectors. At t_3, S_{24} turn-on represents the non-ZVS turn-on action of the HTL transition, while S_{24} turn-off represents the turn-off action for the transition from active vectors to zero vectors.



(a) Voltage waveforms of v_a, v_p, and V_{ds} of S_{24}.

(b) at t_1 the beginning of sector II.

(c) at t_2 in the sector II.

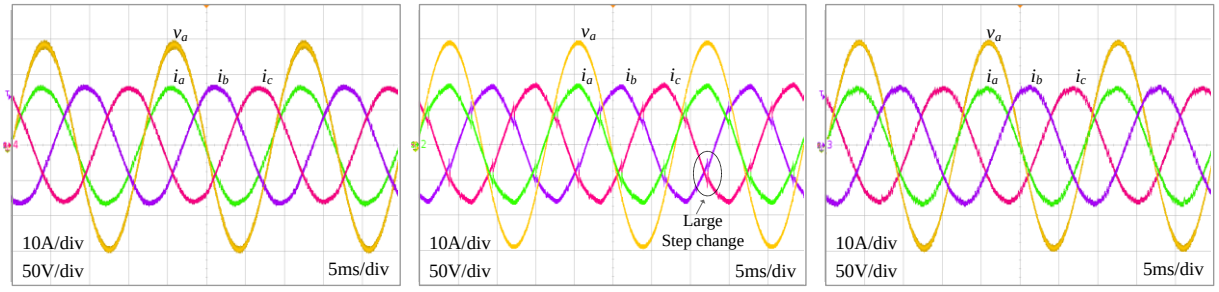
(d) at t_3 in the sector II.

Fig. 2-17 Experimental waveforms for rectifier MOSFETs switching behavior with "Type A" PWM implementation.

As shown in Fig. 2-17 (b) and (c), V_{ds} tends to zero before the gate to source voltage V_{gs} approaches high, which indicates that the body diode is on before the turn-on of the switch such that ZVS is realized. The non-ZVS transition is shown in Fig. 2-17 (d). Prior to turning on this switch, the drain-source voltage V_{ds} of the MOSFET is very small and the current i_{ds} through this switch is zero. Therefore, the resulted switching loss is very low. Due to the ZVS operation, the primary side voltage waveforms are free from high switching noise and no snubber is required. As shown in Fig. 2-17 (b) - (d) all the turn-off actions contribute to the switching losses since the MOSFET is turning off at full current. Because the voltage transition between two joint active vectors is only the difference of the two line-line voltages $(v_{AC} - v_{AB})$ in Fig. 2-17 (c), the turn-off loss at t_3 is much smaller than that at t_1 and t_2. However, the MOSFET turn-off action produces negligible losses since the overlapping of voltage and current is very small during turn-off transition.

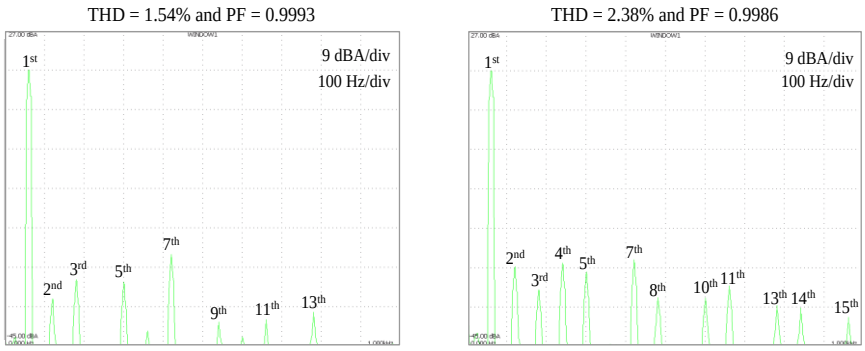
2.7.3 Verification of Input current THD

Fig. 2-18 shows the input phase voltage and currents waveforms with "Type A" and "Type E" PWM schemes implementation. As shown in Fig. 2-18 (b), in "Type A" PWM implementation without the duty-cycle compensation, there are step changes in the input phase currents that are caused by swapping the duty-cycle of "bridge *x*" and "bridge *y*" in the middle of each sector to achieve HTL switching pattern.



(a) "Type A" with duty-cycle compensation (b) "Type A" without duty-cycle compensation (c) "Type E" with duty-cycle compensation

Fig. 2-18 Waveforms of grid voltage v_a and currents i_a, i_b and i_c at the rated power.



(a) "Type A" PWM with compensation (b) "Type E" PWM with compensation

Fig. 2-19 Experimental spectrums of Input phase current.

The input current THD for "Type A" without duty-cycle compensation is 3.8%. Fig. 2-19 (a) and (b) show the experimental spectrums of the input currents obtained from the prototype with duty-cycle compensation for "Type A" and "Type E". The input current THD, calculated from the measurement, is 1.54% with "Type A" and 2.38% with "Type E" implementation.

2.8 Conclusions

The operation principle of the three-phase isolated buck matrix-type rectifier based on the traditional eight-segment PWM ("Type E") is described first. The relevance between SVM and the synthesis method with ZVS phase-shift full-bridge topology is also explained. Then several practical PWM schemes are analyzed and compared. It is shown that the proposed six-segment PWM scheme ("Type A") is the optimal PWM scheme for the MOSFET devices employed for bidirectional switches in the isolated buck matrix-type rectifier. The ZVS operation of the rectifier with "Type A" and "Type E" is analyzed at steady-state operation.

The performance of "Type A" PWM is compared with that of the traditional eight-segment PWM ("Type E") with theoretical analysis and experimental results. "Type A" PWM features lower switching losses, lower duty-cycle loss and lower maximum output inductor current ripple. The reduction of duty-cycle loss of the rectifier offers some other benefits such as improving the light load efficiency by using larger value of resonant inductor and reducing the conduction loss

caused by the circulating current. Very low input current THD can be achieved with duty-cycle compensation for both PWM schemes “Type A” and “Type E”. However, “Type E” offers the benefit of smaller transformer size due to the doubled pulse frequency on the transformer which results in lower core loss. Therefore, it is commendable to improve the eight-segment PWM which can be considered as an alternative PWM scheme for the isolated buck matrix-type rectifier.

Chapter 3

Improved “Type E” PWM and Efficiency and Power Density Evaluation for 380 V and 54 V Prototypes

In Chapter 2 several practical PWM schemes particularly for the isolated buck matrix-type rectifier are studied and “Type A” PWM scheme is identified as an optimal PWM scheme for the rectifier with MOSFETs implementation. Generally, the overall efficiency with “Type A” PWM is relatively higher than “Type E” especially at light load due to lower switching losses. However, “Type A” PWM suffers from larger core size compared with “Type E” PWM since with “Type E” PWM, the frequency on the transformer is nearly twice the frequency of “Type A” PWM when maintaining the same switching frequency. In order to take the advantage of “Type E” PWM, this PWM can be considered as an alternative PWM scheme in compact design. It is, therefore, important to improve the “Type E” PWM by overcoming its drawbacks. As discussed in Chapter 2, there are two major issues related to “Type E” PWM: first, “Type E” PWM contains two non-ZVS switches in each sector which contribute to turn-on losses and second, the rectifier operation with “Type E” PWM scheme suffers from large output inductor current ripple which results in having larger output inductor size and early loss of ZVS for the leading edge transition. In this chapter, an improved eight-segment PWM is introduced which mitigates these two issues related to traditional eight-segment PWM (“Type E”).

The next focus of this chapter is to provide comprehensive loss breakdown and efficiency comparison on 5 kW isolated buck matrix-type rectifier prototypes with 380 V and 54 V output voltages respectively since 380 V and 54 V output voltages are the two popular solutions for PDS in data center and telecom applications. The typical three-phase input voltage of the PDS in data center and telecom application is 400/480 Vrms. The peak reverse voltage applied to the

bidirectional switches of the rectifier is equal to the peak of the ac mains line-to-line voltage which results in 750 V maximum blocking voltage for a 480 Vrms mains with 10% overvoltage. Therefore, switches with a blocking voltage rating of 900 V or 1.2 kV are typically used.

Among the various switching devices to date, IGBTs has found commonplace usage within power converter systems operating at voltages in this range because of their relatively low on-state voltage compared to Si FET device. Moreover, IGBTs have been widely used for medium and higher power applications (> 5 kW) in industry to realize the bidirectional-switches of the matrix-type rectifier However, IGBT's drawback is its slower switching capability due to its bipolar output characteristic. To achieve the targeted efficiency (> 98%) SiC MOSFETs are selected due to their high blocking voltage rating and low conduction and switching losses compared to its Si counterparts. Although the loss reduction advantages in principle of SiC devices compared with Si devices are already well established [56, 57], but their benefit in the context of an isolated buck matrix-type rectifier is not so clear-cut. In order to compare the potential of advanced semiconductor technology against state-of-the-art low-cost technology in this application, the loss analysis of both Si IGBT and SiC MOSFETs is provided.

3.1 Improved "Type E" PWM

Similar to the six-segment PWM schemes in Chapter 2, the eight-segment PWM scheme also has different PWM patterns. Fig. 3-1 (a) and (b) show the eight-segment PWM scheme with two possible PWM patterns. The eight-segment PWM scheme ("Type E") in Fig. 3-1 (a) is preferable since the voltage-second is balanced in positive and negative half-cycle during entire six sectors operation. However, the PWM in Fig. 3-1 (b) is not desired because there are two large pulses with the same polarity appearing one after another at the boundary of sectors as shown in the circle. This creates large flux offset in the transformer core and may saturate the core.

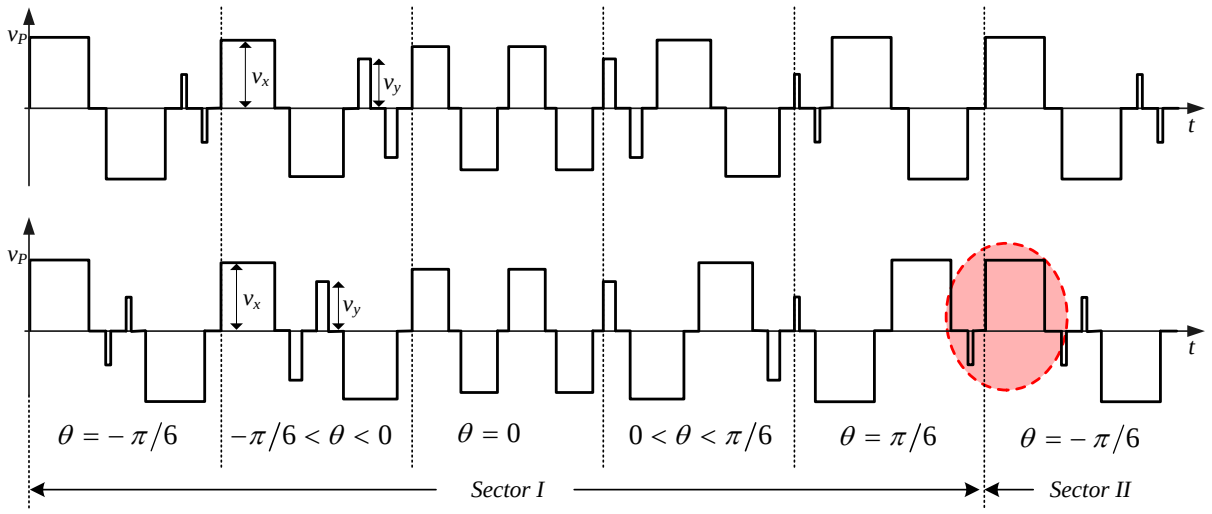


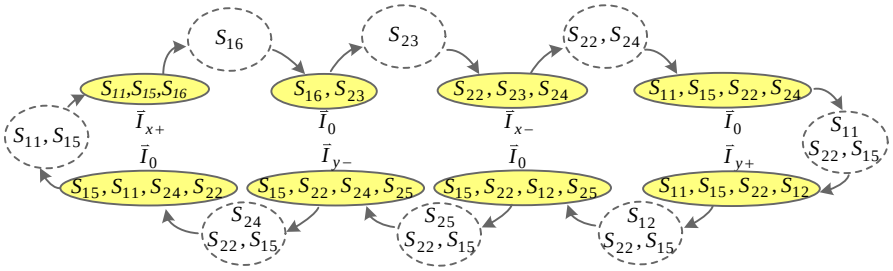
Fig. 3-1 Transformer primary voltage waveform with Eight-segment PWM scheme: (a) desireable PWM pattern (b) traditionl PWM pattern.

An improved "Type E" PWM scheme is introduced based on the same PWM pattern as "Type E", but the zero intervals are not distributed equally. By rearranging the zero vector intervals of "Type E', the output inductor current ripple can be significantly reduced. Therefore, the output inductor can be designed with smaller size. In addition, a two-step commutation method is applied in improved "Type E" to eliminate the loss of two non-ZVS turn-ON switches associated with "Type E" PWM.

3.1.1 Full ZVS Turn-ON for Devices with Proposed Commutation Scheme

The finite commutation state machines for improved "Type E" PWM scheme with the proposed commutation method are shown in Fig 3-2. The transition states (dashed-circle) are added between main states (in shaded color) to achieve ZVS and synchronous rectification operation. It is worth mentioning that the commutation scheme derived for improved "Type E" PWM scheme permits all the switches of the rectifier to turn ON under ZVS condition. This may be considered as an advantage over "Type A" PWM where two of the switches in each sector are non-ZVS although the associated turn-ON loss for these two switches is very small.

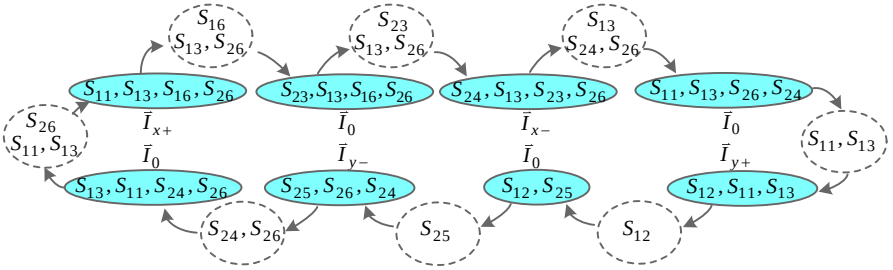
Sector I.(a)



3Φ Sync-Rect switches:

S_{21},S_{14},$\boxed{S_{13},S_{26}}$

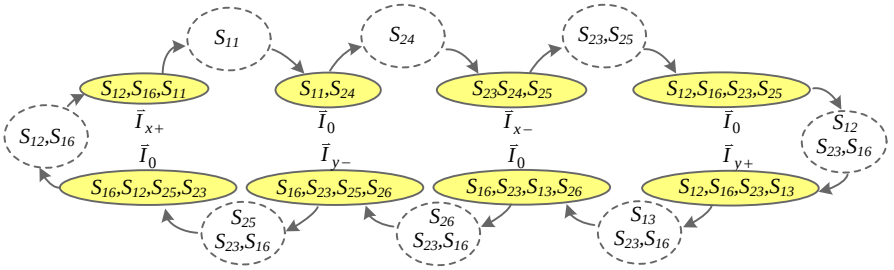
Sector I.(b)



3Φ Sync-Rect switches:

S_{21},S_{14},$\boxed{S_{15},S_{22}}$

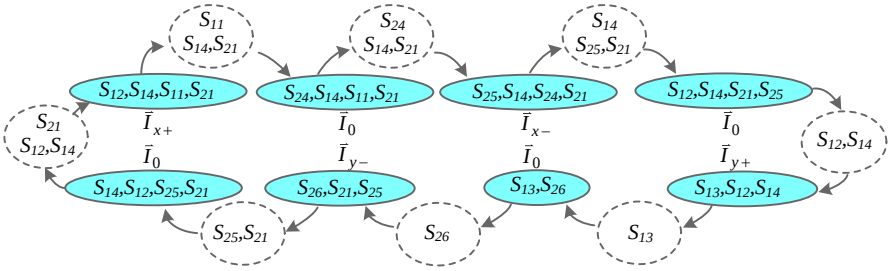
Sector II.(a)



3Φ Sync-Rect switches:

S_{22},S_{15},$\boxed{S_{14},S_{21}}$

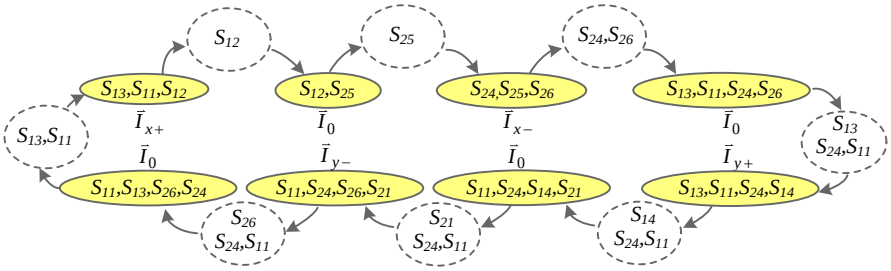
Sector II.(b)



3Φ Sync-Rect switches:

S_{22},S_{15},$\boxed{S_{16},S_{23}}$

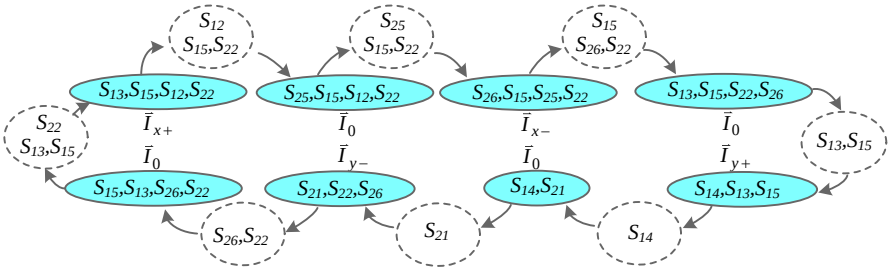
Sector III.(a)



3Φ Sync-Rect switches:

$S_{23},S_{16},\boxed{S_{15},S_{22}}$

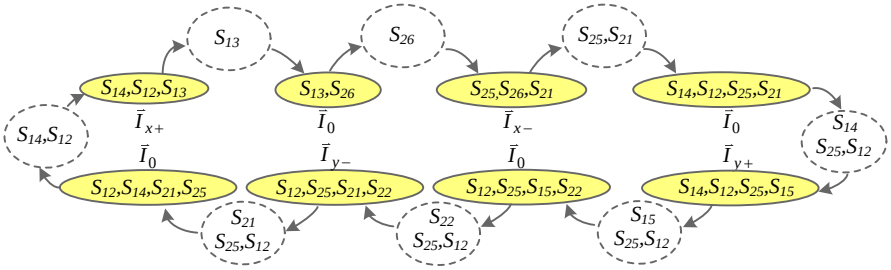
Sector III.(b)



3Φ Sync-Rect switches:

$S_{23},S_{16},\boxed{S_{11},S_{24}}$

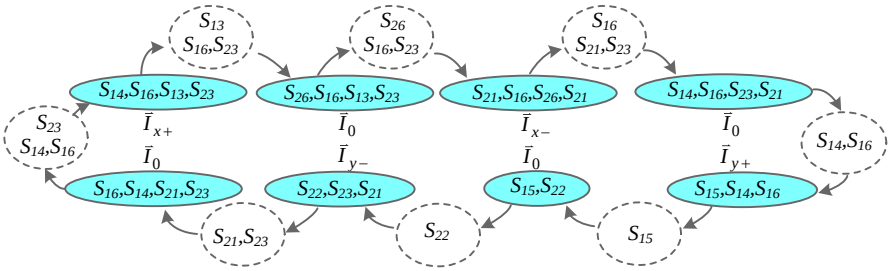
Sector IV.(a)



3Φ Sync-Rect switches:

$S_{24},S_{11},\boxed{S_{16},S_{23}}$

Sector IV.(b)



3Φ Sync-Rect switches:

$S_{24},S_{11},\boxed{S_{12},S_{25}}$

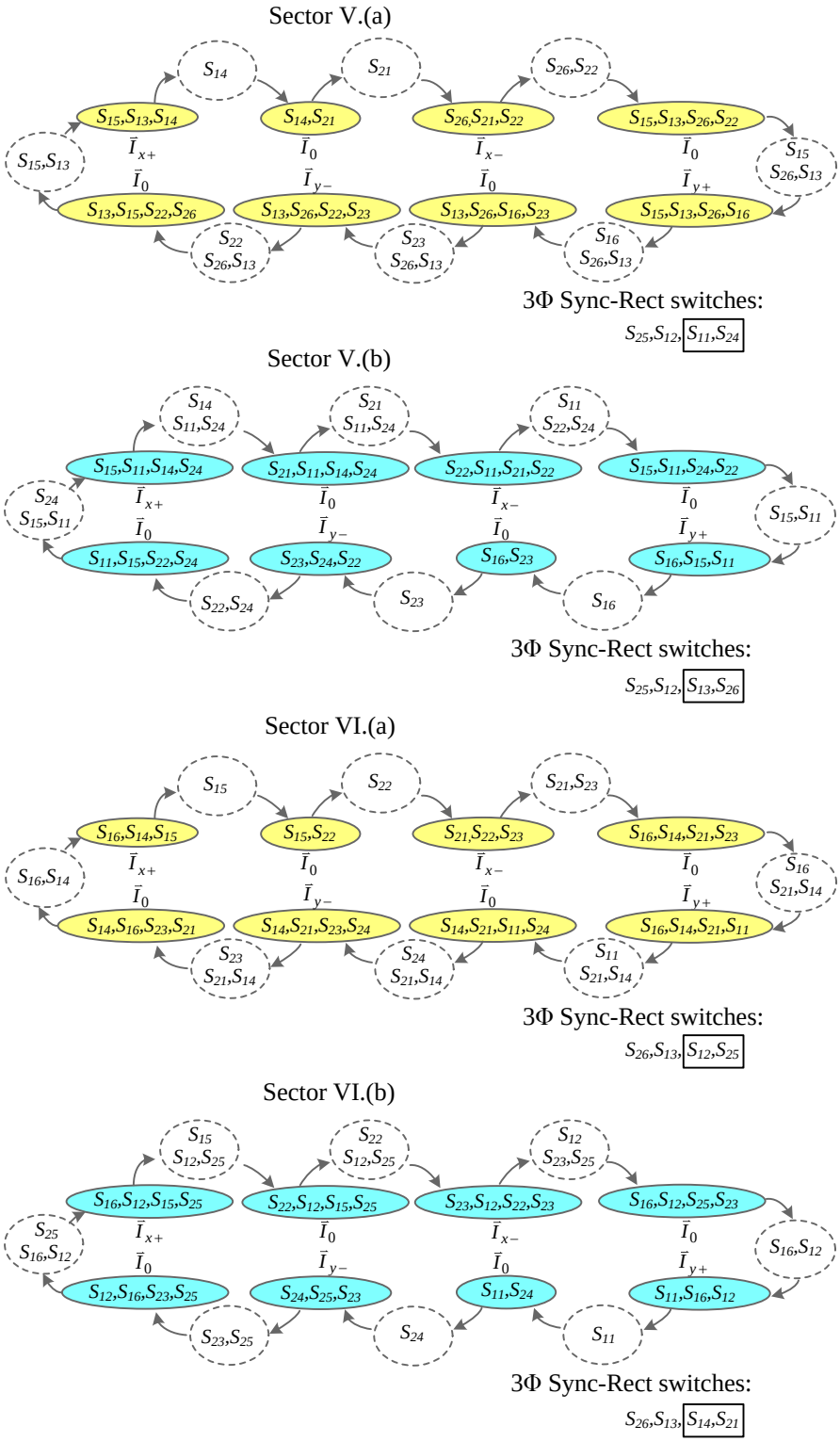


Fig. 3-2 Finite commutation state-machine in all sectors for improved "Type E" PWM (Not: all the primary MOSFET switches are turned ON under ZVS with the proposed commutation method).

3.1.2 Reduced Output Inductor Current Ripple with the Proposed Optimized Zero-Vector Dwell Times

As discussed in Chapter 2, in "Type E", the dwell time of $\vec{I}_0$ is equally divided by four and inserted between $\vec{I}_x$ and $\vec{I}_y$ as shown in Fig. 3-4 (b) and (d). With considering the duty-cycle losses, the dwell time can be calculated as

$$\begin{cases} T_x = [m_a \sin(\frac{\pi}{6} - \theta) + 2\Delta D_x]T_S \\ T_y = [m_a \sin(\frac{\pi}{6} + \theta) + 2\Delta D_y]T_S \\ T_0 = T_S - T_x - T_y \end{cases} \quad \text{for } -\frac{\pi}{6} \le \theta \le \frac{\pi}{6}. \tag{3-1}$$

Assuming the output inductor ripple current is relatively small compared with the load current I_o, duty-cycle losses ΔD_x and ΔD_y corresponding to vectors $\vec{I}_x$ and $\vec{I}_y$ respectively is the function of the voltage $v_P(\theta)$ across the leakage inductance L_{lk} during these intervals and the load current I_o as shown in (3-2) and (3-3).

$$\Delta D_x = \frac{2nI_oL_{lk}}{v_{P\_x}(\theta)T_s} \tag{3-2}$$

$$\Delta D_y = \frac{2nI_oL_{lk}}{v_{P\_y}(\theta)T_s} \ . \tag{3-3}$$

Here, $v_{P\_x}(\theta)$ and $v_{P\_y}(\theta)$ represent the magnitude of transformer pulses of "bridge *x*" and "bridge *y*" respectively ($v_{P\_x}(\theta) = v_{AB}$ and $v_{P\_y}(\theta) = v_{AC}$ in Fig. 3-4). For a given output voltage, the output inductor ripple at steady-state is determined by the total off-time of the transformer secondary side PWM voltage V_d and how the off-time is divided into four intervals in one switching cycle. Fig. 3-3 (b) shows the envelope of output inductor current ripple varying with phase angle θ with equally distributed zero-vector intervals ("Type E"). Zoom-in PWM waveforms are shown in Fig. 3-4 (b) and (d). At $\theta = 0^\circ$, total off-time of the secondary voltage

V_d is minimum and is given by $(1-m_a)T_s$. The resultant four pulses of V_d are identical and are evenly distributed in one switching cycle. Therefore, the output inductor current ripple is minimum and is given by (2-15). When phase angle θ is moving away from $\theta = 0$, the magnitude and width of one pair of pulses start increasing and that of another pair of pulses start decreasing. At the vicinity of $\theta = \pm\pi/6$, one of the two active vectors attains its maximum magnitude and the other vector reaches to minimum as shown in Fig. 3-4 (d). One of the pair of voltage pulses of V_d disappears due to the duty-cycle loss and three of the off-time intervals merge into one. As a result, voltage pulses of V_d are not evenly distributed within T_s, resulting in larger current ripple. The peak to peak ripple current is determined by T_{off}, the total value of the three merged off-time intervals, as shown in Fig. 3-4 (d). Assuming that the difference between ΔD_x and ΔD_y is relatively small and can be ignored, the maximum current ripple at $\theta = -\pi/6$ and $\theta = \pi/6$ can be calculated by (2-18). However, when loss of duty-cycle is large, the difference between ΔD_x and ΔD_y cannot be ignored, then (2-18) can be revised as:

$$\Delta I_{\max} = \frac{V_o(1-\frac{\sqrt{3}}{2}m_a) - (\frac{T_0}{4} + \Delta D_x)}{L_o}. \tag{3-4}$$

By properly dividing T_0 into four different intervals between these voltage pulses ($\bar{I}_x, \bar{I}_y$), the output inductor current ripple can be reduced. In order to minimize the output inductor current ripple, the zero vector interval between the pair of wider pulses (T_{01} at $\theta \in [-\pi/6, 0]$ and T_{03} at $\theta \in [0, \pi/6]$) should be long enough to let the output inductor current decay to the same value as that of the beginning of the pulse as shown in Fig. 3-4 (c). Based on the principle of the voltage-second balance, T_{01} and T_{03} with considering the loss of duty-cycle can be expressed as:

$$T_{01} = T_S \sin(\frac{\pi}{6} - \theta)(\frac{\sqrt{3}}{3}\sin(\theta + \frac{2\pi}{3}) - \frac{1}{2}m_a) - T_S\Delta D_x \ , \quad \theta \in [-\pi/6, 0] \tag{3-5}$$

$$T_{03} = T_S \sin(\frac{\pi}{6} + \theta)(\frac{\sqrt{3}}{3}\sin(\theta + \frac{\pi}{3}) - \frac{1}{2}m_a) - T_S\Delta D_y \ , \quad \theta \in [0, \pi/6] \ . \tag{3-6}$$

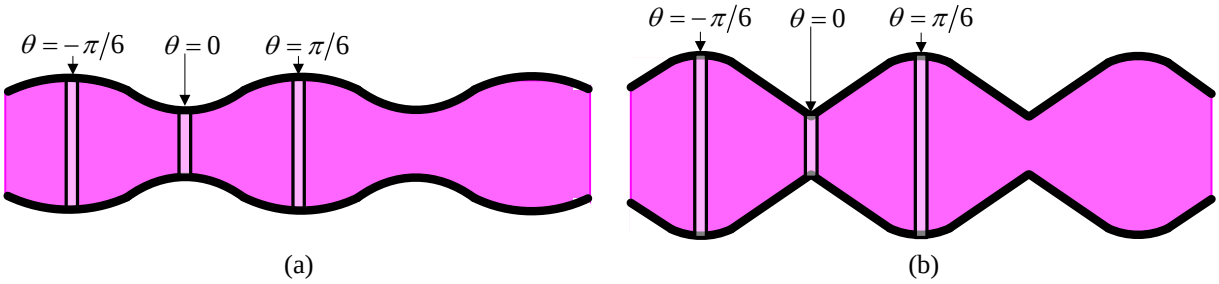
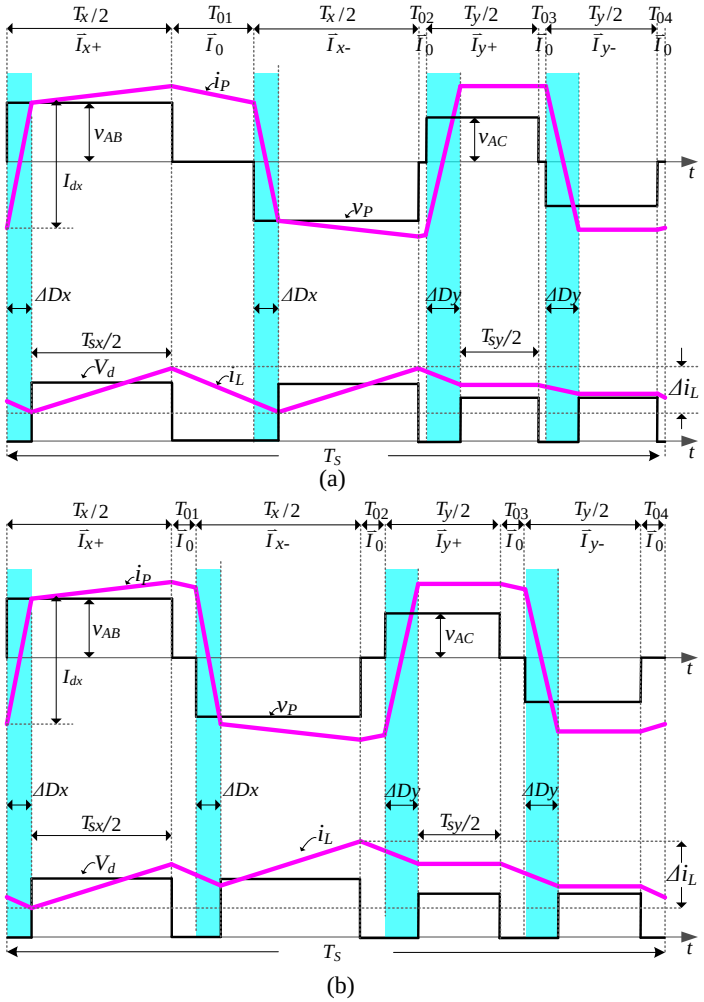


Fig. 3-3 Envelope of output inductor current ripple, i_L of the isolated buck matrix-type rectifier with: (a) improved "Type E" PWM and (b) "Type E" PWM.



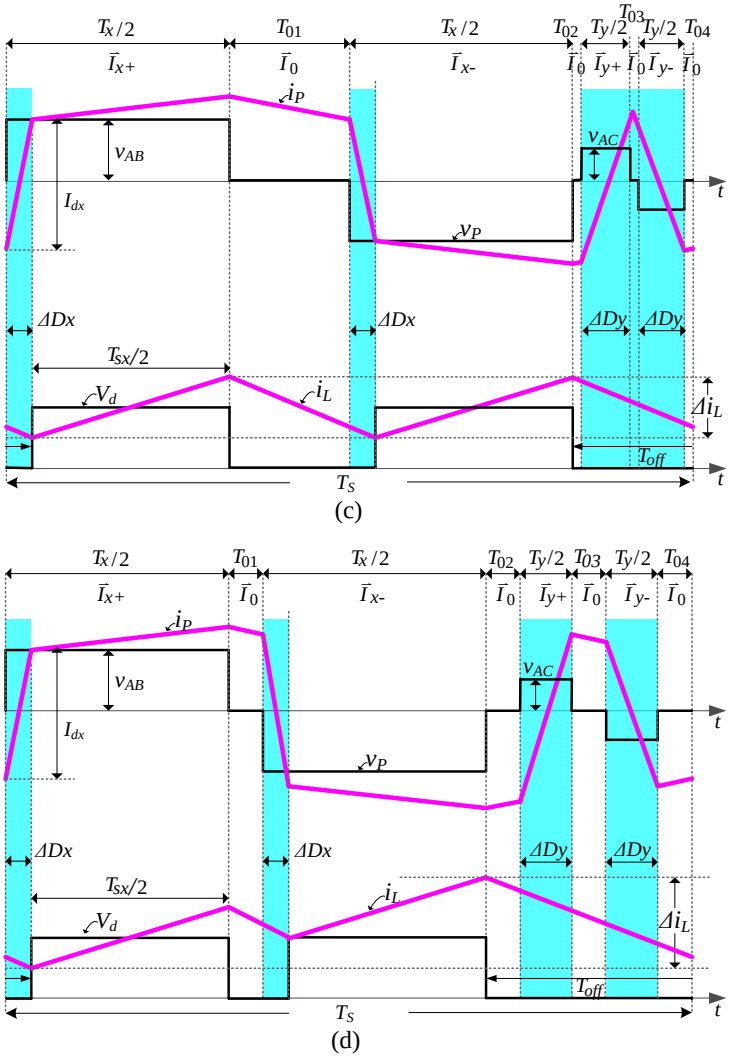


Fig. 3-4 Zoom-in waveforms of the primary side voltage v_P, primary side current i_P, output bridge diode rectifier V_d and ouptut inductor current i_L of the isolated buck matrix-type rectifier with (a) improved "Type E" PWM, (b) "Type E" PWM, (c) improved "Type E" PWM and (d) "Type E" PWM.

Then for easy implementation, the rest of three zero vector intervals can be derived by simply dividing the remaining total zero-vector dwell times into three equal intervals as shown in below:

$$T_{02} = T_{03} = T_{04} = \frac{1}{3}(T_0 - T_{01}), \quad \theta \in [-\pi/6, 0] \tag{3-7}$$

$$T_{01} = T_{02} = T_{04} = \frac{1}{3}(T_0 - T_{03}), \quad \theta \in [0, \pi/6]. \tag{3-8}$$

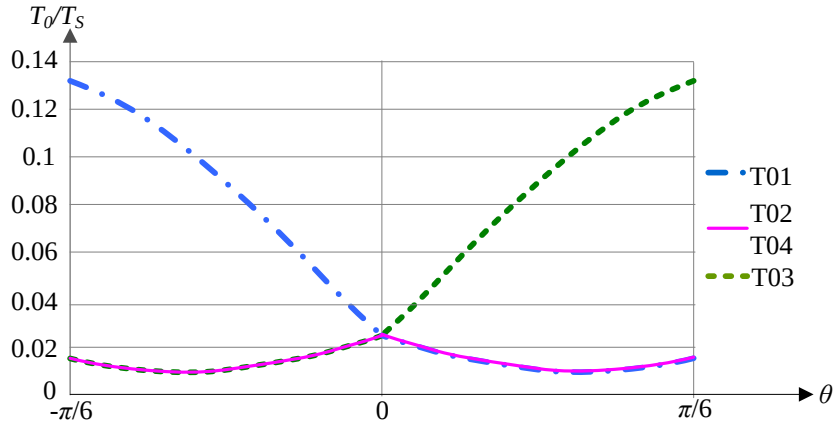


Fig. 3-5 Four zero-vector intervals of the improved "Type E" PWM (condition: m_a = 0.8 and $\Delta D_{total}(\theta) = \Delta D_{total}(0)$ = 0.1).

Fig. 3-5 shows the four zero-vector intervals (T_{01}, T_{02}, T_{03}, T_{04}) vary within each sector. Compared with "Type E" PWM, the peak of inductor current ripple at $\theta = \pm\pi/6$ with improved "Type E" PWM is reduced as shown in Fig. 3-4 (c) and Fig. 3-4 (d). It should be noted that the maximum achievable m_a may be reduced with proposed PWM scheme. When m_a is large, the calculated T_{01} or T_{03} may be larger than the total zero-vector dwell time T_0 and should be clamped to T_0, the rest of three zero-vector intervals will be zero. In this case, the resultant current ripple will be slightly compromised, but it is still smaller than the case with four equally distributed zero-vector intervals.

3.1.3 Simulation and Experimental Verification for Imporved "Type E"

The simulation model and the experimental prototype are the same as parameters given in Table 2-1 for "Type E" PWM. Fig. 3-6 shows the simulated and experimental waveforms for the improved "Type E" PWM. As shown in Fig. 3-6, the transformer primary voltage is clean and no large spike is noticeable due to the ZVS operation of the MOSFET switches. Compared with "Type E" in Fig 2-16, the peak of output inductor current ripple is around 20% lower at the $\theta = \pm\pi/6$. At $\theta = 0$, both PWMs exhibit equally low output inductor current ripple.

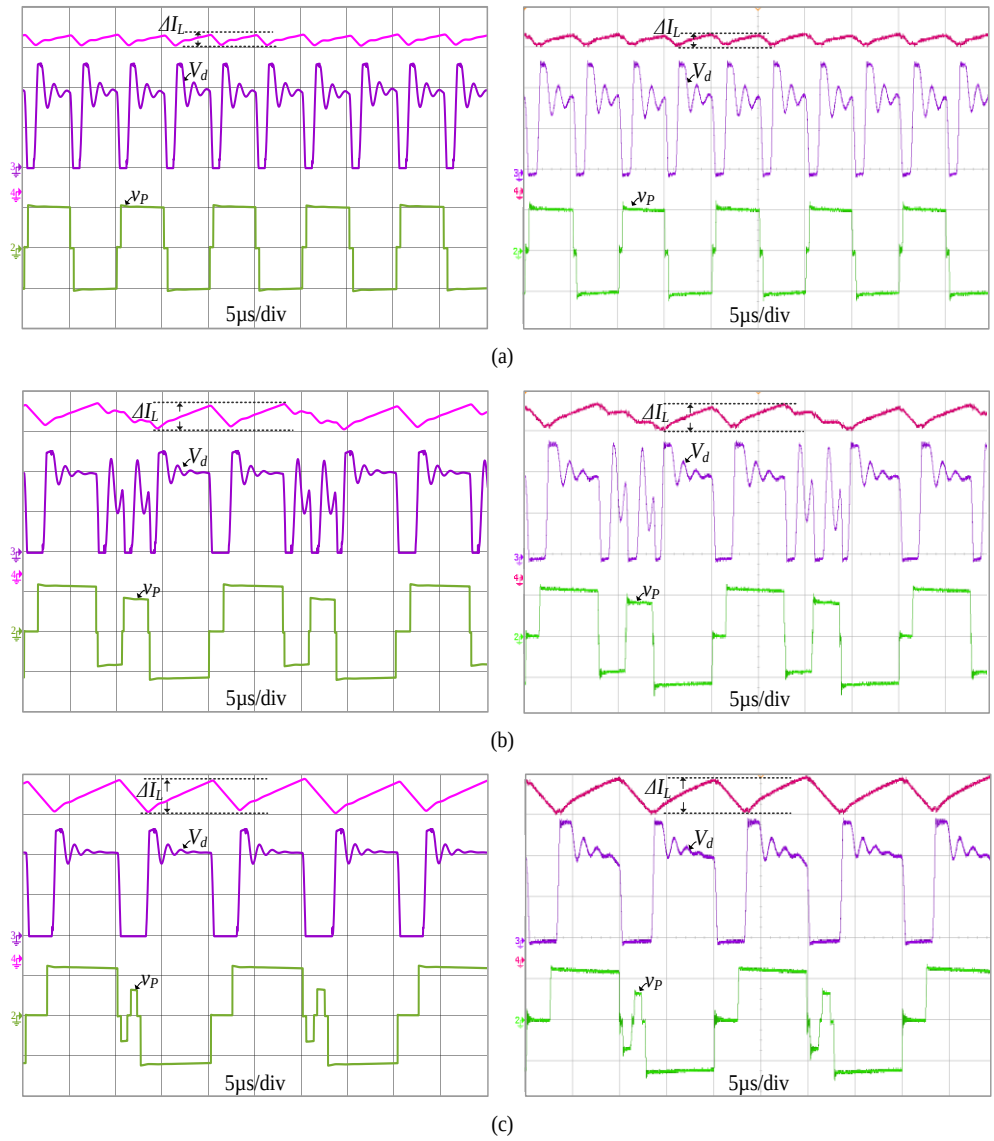


Fig. 3-6 Simulated waveforms (left) and experimental waveforms (right) of the transformer primary voltage v_P, rectifier voltage V_d and inductor current ripple ΔI_L with implementation of improved "Type E" PWM: (a) at $\theta = 0^\circ$, (b) $-\pi/6 < \theta < 0$ and (c) at $\theta = -\pi/6$. (Ch2 = 200 V/div, Ch3 = 200 V/div, Ch4 = 2.5 A/div).

The improved output inductor current ripple is also beneficial for current sensing which is used to implement average current mode control. The sampled current in the middle of pulses can accurately represent the average current for the current feedback loop. This results in better input currents THD.

3.2 Loss Breakdown and Efficiency Comparisons for 380 V and 54 V Prototypes

Evaluation of the semiconductor loss for Si IGBTs and SiC MOSFETs requires quantification of the conduction and switching characteristics for both switch families in the context of the isolated buck matrix-type PWM rectifier. For conduction losses, it is sufficient to use manufacture's datasheet. However, it is more difficult to determine the switching loss behavior of these devices from datasheets, particularly when they are operated well outside the test conditions that they are used to obtain the datasheet results. Since the mechanisms of commutation can affect the switching behavior, turn-ON and turn-OFF losses of each switching transition are analyzed for "Type A" and improved "Type E" respectively. In addition, the periodically varying operating conditions due to three-phase operation also add complexity to the switching loss calculation. The proper averaging techniques are used to get the equivalent switching losses.

3.2.1 Conduction Losses on Semiconductors

Assuming the inductor ripple current is small, the conduction loss can be calculated based on the average inductor current. Except the switching transition, the primary current path always contains four MOSFETs in series. Then the conduction losses can be calculated as

$$P_{C\_S} = 4(nI_o)^2 R_{DS\_on}. \tag{3-9}$$

R_{DS_on} is the on resistance of the primary MOSFETs at 100^{o}C and n is transformer turns ratio N_2/N_1. For 380 V prototypes, current path in secondary side diode bridge rectifier can be considered as two diodes in series, and then conduction loss of the semiconductors on secondary side can be calculated by

$$P_{C\_D} = 2[I_o{}^2 R_D + I_o V_D]. \tag{3-10}$$

In the 54 V prototype, two transformers are connected in series at the secondary side output as shown in Fig. 3-8. Therefore, the conducted current of the synchronous rectifier of each transformer is the same as the load current. The total conduction loss of the semiconductors on secondary side of two transformers can be calculated by

$$P_{C\_SR} = 2I_o{}^2 R_{DS\_on,SR} / N_{SR-tot} \tag{3-11}$$

where $N_{SR\text{-}tot}$ is the total number of parallel SR MOSFETs on one side of each transformer.

The total gate driver losses for SR MOSFETs can be calculated by

$$P_{C\_SR} = 4 f_{sw} V_{gs} Q_{g-SR} N_{SR-tot} . \tag{3-12}$$

where V_{gs} and $Q_{gs\text{-}SR}$ are the applied gate to source voltage and gate charges respectively.

3.2.2 Analsis of Switching Loss of the Bidirectional Devices in Isolated Buck Matrix-Type Rectifier with "Tpe A" and Imporoved "Type E"

In "Type A", there are six transitions in one switching cycle as shown in Fig. 3-7. As discussed and summarized in Chapter 2, all the switches of the isolated buck matrix-type rectifier are turned ON under ZVS condition for desired ZVS range (eg. 100% to 40% load) except two switches for transitions 2 and 5. All the turn-off switching events in Fig. 3-7 generate losses. The associated turn-ON and turn-OFF losses of each transition have been discussed in detail in Appendix A. The two non-ZVS transitions are related to the charging/discharging energy stored in output capacitance C_{oss} of MOSFETs and should be very small since the drain-to-source voltages prior to switching turn-ON are small. The turn-ON loss of two non-ZVS can be calculated by

$$P_{sw\_2non\_ZVS} = 2E_{on\_non\_ZVS\_avg} f_{sw} = 4E_{oss}(0.5V_m) f_{sw} . \tag{3-13}$$

As discussed in Appendix A, ZVS operation of the converter is similar to the operation of FB-PS. At light load when ZVS is lost, there are two leading edge turn-ON events contributing to the turn-ON switching losses for six-segment PWM and four leading edge turn-ON events

contributing the turn-ON switching losses for eight-segment PWM. The turn-ON loss is the function of residual voltage V_{res} and can be expressed as:

$$P_{sw\_on\_lead\_six\_seg} = 2E_{on\_lead}(V_{res})\, f_{sw} \tag{3-14}$$

$$P_{sw\_on\_lead\_eight\_seg} = 4E_{on\_lead}(V_{res})\, f_{sw}. \tag{3-15}$$

As discussed in [44], the equivalent total output capacitance for the leading edge operation is $5/2\,C_{oss}$ if all the other parasitic capacitances are neglected. The (3-14) and (3-15) can be revised as

$$P_{sw\_on\_lead\_six\_seg} = \frac{5}{2} C_{oss} {V_{res}}^2 f_{sw} = 5E_{oss}(V_{res})\, f_{sw} \tag{3-16}$$

$$P_{sw\_on\_lead\_eight\_seg} = 5C_{oss} {V_{res}}^2 f_{sw} = 10E_{oss}(V_{res})\, f_{sw}\ . \tag{3-17}$$

The ZVS for trailing edge switches can be achieved at lighter load because the energy stored in the output filter inductor is significantly larger than the energy stored in the leakage inductance. In addition, the transformer primary current during this transition is at peak. However, when the node capacitances are relatively very large and the primary current is very small such that ZVS is lost, the trailing edge switches also suffer from the turn-ON switching loss. To nullify the trailing edge turn-ON loss, adaptive delay is usually implemented such that the dead-time is increased at light load and reduced at heavy load. Small magnetizing current is also helpful to mitigate the trailing edge turn-ON switching loss.

In "Type A", each of the six transitions involves one turn-off event which contributes to the switching loss. Since the switching loss is a function of switching current and voltage, switching losses for these six turn-OFF events are different. As discussed in Appendix A, four of the turn-off switching events (1, 3, 4, 6) are switched at full voltage $v_{AB}(\theta)$ or $v_{AC}(\theta)$ which results in larger switching loss compared with the other two trun-off switching events (2, 5) with lower voltage (due to difference voltages between $v_{AB}(\theta)$ and $v_{AC}(\theta)$). In improved "Type E" as shown in Fig. 3-7 (b), there are eight transitions and each transition also involves one turn-OFF event which contributes to the switching loss.

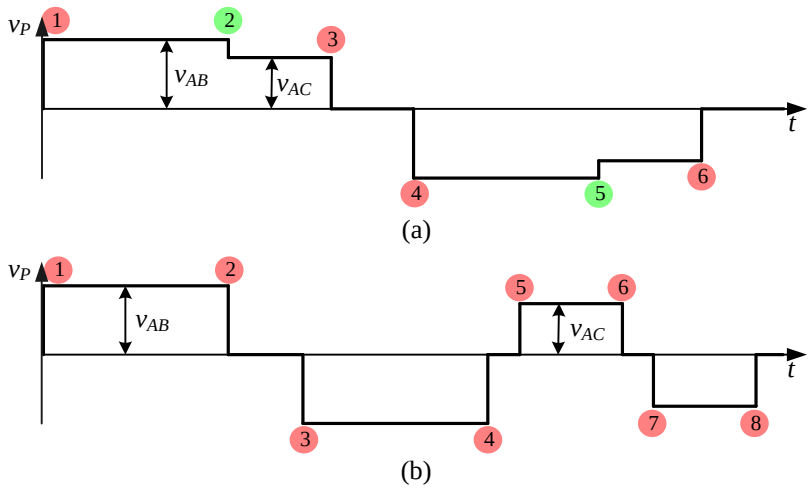


Fig. 3-7 Switching events for (a) "Type A" and (b) improved "Type E".

Four of the eight transitions are turned OFF at $v_{AB}(\theta)$ while the other four are turn OFF at $v_{AC}(\theta)$. Assuming the turn-OFF current is the same for all turn-OFF events by neglecting the effect of current ripple, the total turn-OFF loss for "Type A" and improved "Type E" can be calculated by

$$\begin{aligned} P_{SW\_off\_six\_seg} &= (2E_{off\_low\_six\_avg} + 2E_{off\_lead\_avg} + 2E_{off\_trail\_avg}) f_{sw} \\ &= 4E_{off\_lead\_avg} f_{sw} \approx 4(E_{off}(1.65V_m) - E_{oss}(1.65V_m)) f_{sw} \end{aligned} \tag{3-18}$$

$$\begin{aligned} P_{SW\_off\_eight\_seg} &= (4E_{off\_lead\_avg} + 4E_{off\_trail\_avg}) f_{sw} \\ &= 7E_{off\_lead\_avg} f_{sw} \approx 7(E_{off}(1.65V_m) - E_{oss}(1.65V_m)) f_{sw} \end{aligned} . \tag{3-19}$$

Table 3-1 Summary of the turn-ON and turn-OFF loss calculation for "Type A" and improved "Type E".

PWM Scheme	$P_{sw\_on\_Lead}$	$P_{sw\_non\_ZVS}$	P_{sw_off}
"Type A"	$5E_{oss}(V_{res}) f_{sw}$	$4E_{oss}(0.5V_m) f_{sw}$	$4E_{off\_lead\_avg} f_{sw}$ $= 4(E_{off}(1.65V_m) - E_{oss}(1.65V_m)) f_{sw}$
Improved "Type E"	$10E_{oss}(V_{res}) f_{sw}$	0	$7E_{off\_lead\_avg} f_{sw}$ $= 7(E_{off}(1.65V_m) - E_{oss}(1.65V_m)) f_{sw}$

Table 3-1 provides summary of the turn-ON and turn-OFF switching losses with “Type A” and improved “Type E” PWM implementations when the ZVS is lost for turn-ON switching actions. It is important to note the isolated buck matrix-type rectifier has turn-OFF switching loss for all load condition.

3.2.3 Analsis of Switching Loss on the Secondary Side of the Rectifier with “Type A” and Imporoved “Type E”

Similar to the operation of FB-PS, the secondary side bridge diode rectifier of the isolated buck matrix-type rectifier also suffers from large spike and high-frequency ringing loss due to the resonance between the leakage inductance of the transformer and the parasitic capacitance of the bridge diodes. The analysis of the ringing loss of the secondary side bridge diode of the isolated buck matrix-type rectifier is similar to that of a buck DC-DC converter where the ringing happens during the turn-OFF process of the freewheeling diode or SR MOSFET [58]. It is important to note that the reverse recovery charge of diode bridge rectifier also contributes to the ringing loss. Assuming the ringing is fully damped at the end of each pulse, the dissipated energy during the ringing period can be calculated in the same way as [58] and expressed as

$$E_{ring}(V_S) = V_S\left[Q_{rr\_rec} + \frac{1}{2}Q_{oss\_rec}(V_S)\right] \tag{3-20}$$

where Q_{rr_rec} is the reverse recovery charge, Q_{oss_rec} is the output capacitance charge of rectifier, and V_S is the transformer secondary-side voltage transition. In real designs, the parasitic capacitance of the PCB and transformer winding will also contribute to the output capacitance of the rectifier. For a 380V output design, a bridge diode rectifier with four SiC diodes is employed. Therefore, the portion of the ringing loss due to the reverse recovery can be neglected. Then the total charge of the rectifier is

$$Q_{oss\_rec\_380V} = 2Q_{oss\_diode}. \tag{3-21}$$

For the 54 V output design as shown in Fig. 3-8, two transformers are employed. The primary sides of the two transformers are connected in parallel while the secondary sides of the two transformers are connected in series at the output. Each transformer consists of four sets of primary windings connected in series with a total of 32 turns. The secondary side of each transformer contains two sets of center-tapped SR and their outputs are connected in parallel on the dc side. Each set of center-tapped SR includes six synchronous MOSFETs in parallel on each side to reduce the conduction loss. Each center-tapped winding has two turns on each side and is constructed with single turn stamped copper in an interleaved structure. The overall equivalent turns ratio n with considering both transformers is 4:32. The blocking voltage of each SR MOSFET is $V_S = nV_P$.

An adaptive turn-OFF delay time is applied to the SR MOSFET to minimize the body diode conduction time such that the portion of ringing loss due to the revers recovery can be neglected [59, 60]. The turn-ON and turn-OFF switching losses on synchronous MOSFETs are negligible since they are turned ON and turned OFF at zero voltage. Therefore, only the ringing loss due to the output capacitance of synchronous MOSFETs needs to be considered as the switching loss on the secondary side. The total charge of the rectifier is calculated by the following equation

$$Q_{oss\_rec\_54V} = 4Q_{oss\_rec\_set} = 4(6Q_{oss\_Syn}) = 24Q_{oss\_Syn}. \tag{3-22}$$

where $Q_{oss\_rec\_set}$ is the total charge of each set of rectifier, Q_{oss_Syn} is the charge of one synchronous MOSFET.

In six-segment PWM, there are two ringing transitions with full voltage (corresponding to leading edge transition 1 and 4) and two ringing transitions with low voltage (corresponding to transition 2 and 5) in each switching cycle. For leading edge transitions of 1 and 4, the transition voltage $v_{lead}(\theta)$ is equal to $nv_{AB}(\theta)$ during sector I(a) and $nv_{AC}(\theta)$ during sector I(b). It should be noted that there is no ringing happening at the trailing edge transitions 3 and 6. The ringing loss of the leading edge transition is

$$E_{ring\_lead}(\theta) = \frac{1}{2} v_{lead}(\theta) Q_{oss\_rec}(v_{lead}(\theta)) \approx \frac{1}{2} v_{lead}{}^2(\theta) C_{oss\_rec}. \tag{3-23}$$

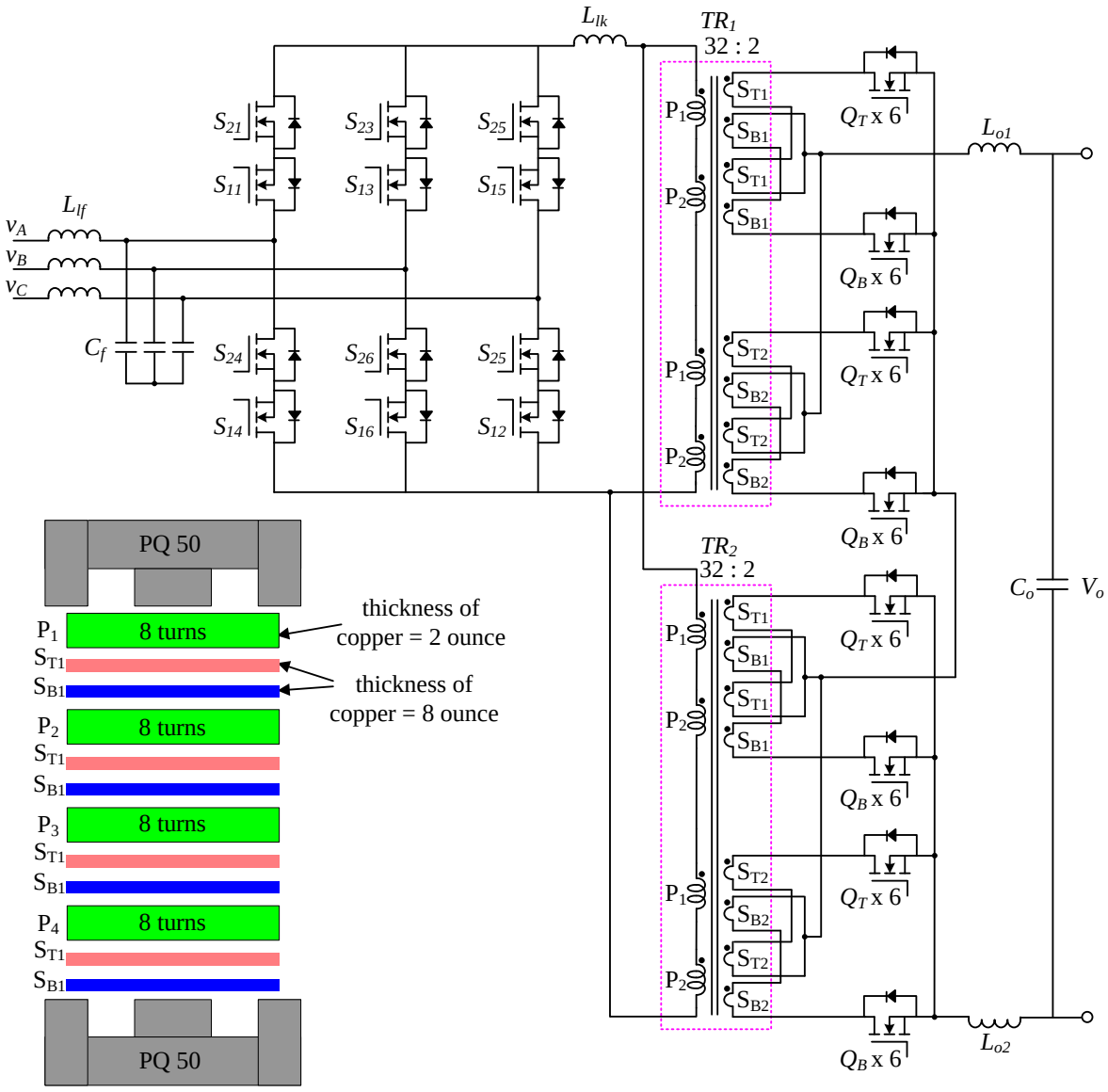


Fig. 3-8 Proposed transformer circuit diagram for 54 V PSU.

It should be noted that C_{oss_rec} should be charge equivalent total capacitance in order to calculate the losses accurately. Then the averaged ringing loss of the leading edge during one sector can be derived as

$$E_{ring\_lead\_avg} = \int_0^{\frac{\pi}{6}} \frac{1}{2} v_{lead}{}^2(\theta) C_{oss\_rec} d(\theta) = \frac{1}{2} C_{oss\_rec} \int_0^{\frac{\pi}{6}} (n v_{AB}(\theta))^2 d(\theta) . \quad (3\text{-}24)$$

For two transitions of 2 and 5, V_S is equal $nv_{CB}(\theta)$ during sector I (a). The ringing loss can be approximated as one fifth of that of leading edge since V_S is very small. The total ringing losses for six-segment PWM is

$$P_{SW\_rec\_six\_seg} = \left(2E_{ring\_lead\_avg} + 1/5E_{ring\_lead\_avg}\right) f_{sw}. \tag{3-25}$$

For eight-segment PWM, two ringing transitions are with $nv_{AB}(\theta)$ and the other two are with $nv_{AC}(\theta)$ during sector I. The total ringing losses for eight-segment PWM can be derived as

$$P_{SW\_rec\_eight\_seg} = C_{oss\_rec\_54}\left(\int_0^{\frac{\pi}{6}} (nv_{AC}(\theta))^2 d(\theta) + \int_0^{\frac{\pi}{6}} (nv_{AB}(\theta))^2 d(\theta)\right) f_{sw}. \tag{3-26}$$

It is important to note that for loss analyses and efficiency comparisons in the following sections, the secondary side devices are selected 3 to 4 times of their rated voltage. Since if not snubbed or clamped, the initial voltage spike across the rectifiers can be several times larger than the steady-state voltage, and therefore has to be removed or the devices with higher voltage rating should be selected.

3.2.4 Loss Breakdown and Efficiency Comparisons for "Type A" and Improved "Type E" on SiC-Based 380 V Prototype

Loss analysis is conducted on a 380 V prototype based on parameters given in Table 3-2. Losses of two PWM schemes are compared at different load conditions 1 kW, 2.5 kW and 5 kW. The load range to achieve ZVS is designed from 40% to 100% for both "Type A" and improved "Type E" PWM. As shown in Fig. 3-9 (a) and (b), the major losses are contributed by conduction loss on the primary bidirectional switches and secondary diode rectifier. The primary conduction loss for improved "Type E" is larger than "Type A", since the improved "Type E" has larger duty-cycle loss compared with "Type A", which results in higher turns ratio (N_2/N_1) and primary current. As shown in Fig. 3-9 (a) and (b) improved "Type E" has zero turn-ON loss and "Type A" PWM has small turn-ON loss due to two non-ZVS switches. As shown in Fig. 3-9 (c), both PWM schemes cannot achieve full ZVS for leading edge at 20% load which results in higher

turn-ON loss. This is more severe for improved “Type E” since more numbers of turn-ON events contributing to turn-ON switching losses. For all load conditions, improved “Type E” exhibits higher turn-OFF switching loss compared with “Type A” PWM.

It is important to note that “Type A” exhibits higher core loss but lower winding loss on transformer compared with improved “Type E” PWM scheme, which compromises to have similar total transformer loss. As shown in Fig. 3-10, the efficiency curve with “Type A” is higher than improved “Type E” for all load conditions, especially at light load. It should be noted that the measured efficiency is lower than the calculated results. The difference is more noticeable at light load efficiency. This is mainly due to the additional parasitic capacitances contributed by the PCB layout and transformer winding, which were not considered in the calculation for turn-ON and turn-OFF switching losses. Fig. 3-11 shows the measured efficiency comparison for proposed PSU (isolated buck matrix-type rectifier) with implementation of either “Type A” or improved “Type E” and the best existing 380 V PSU in today`s market. As shown in Fig. 3-11, the proposed PUS with implementation of either “Type A” or improved “Type E” exhibits significantly higher efficiency compared with benchmark.

Table 3-2 Experimental prototype parameters for 380 V output.

Prototype Parameter	**Value**
C_f	5 µF
L_f	90 µH
$v_{LL,rms}$	480 V
f_{Grid}	60 Hz
C_o	1.4 mF
L_o	315 µH
V_o	380 V
$L_{lk\_Six\_Seg}$ $L_{lk\_eight\_Seg}$	10 µH 20 µH
S_{11} - S_{26}	SCT3080KL (SiC MOSFET Prototype) IKW25N120T2 (Si IGBT Prototype)
D_1 - D_4	SCS215KG
$n_{Six\_Seg} = N_2/N_1$ $n_{eight\_Seg} = N_2/N_1$	30/33 26/27
TR (core and winding)	Ferrite core (ZT47313TC) Primary Litz wire (equivalent AWG 16) Secondary Litz wire (equivalent AWG 16)
$f_{TR\_Six\_Seg}$ $f_{TR\_eight\_Seg}$	50 kHz 100 kHz

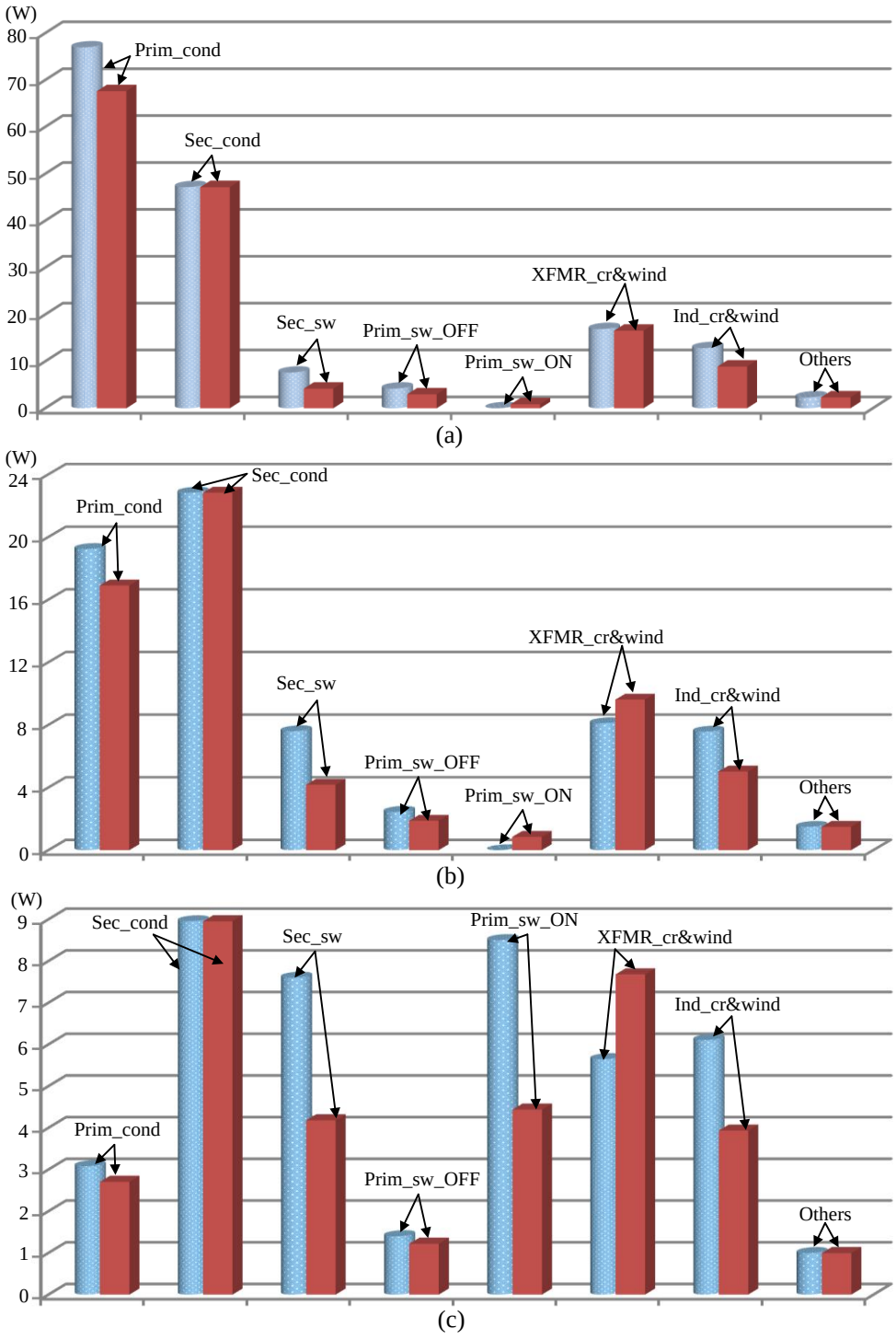


Fig. 3-9 Loss breakdown comparison of "improved Type E" (left bar) and "Type A" (right bar) PWM schemes conducted on SiC MOSFET-based prototype with V_o = 380 V and v_{LL} = 480 V: (a) Loss comparison at 5 kW (100% load) (b) Loss comparison at 2.5 kW (50% load) and (c) Loss comparison at 1 kW (20% load).

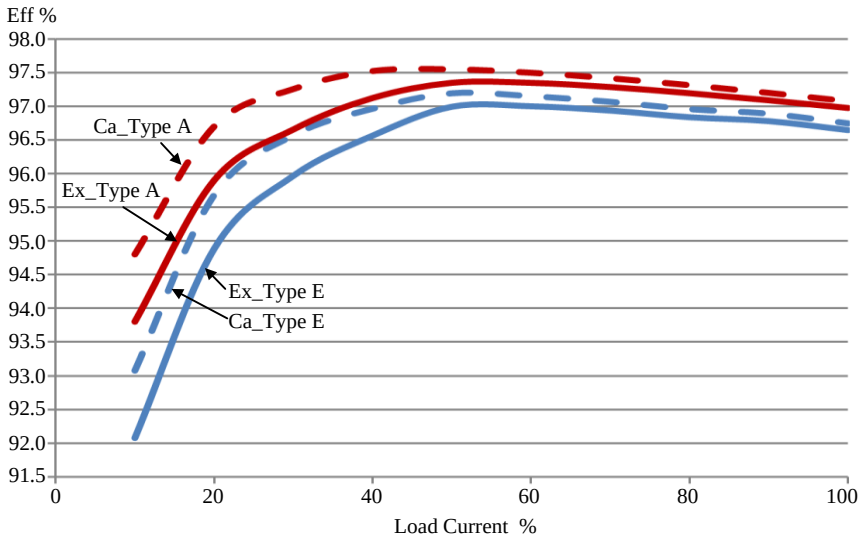


Fig. 3-10 Experimental (solid-line) and calculated (dash-line) efficiency comparison on "Type A" and improved "Type E" PWM schemes conducted on SiC MOSFET-based 380 V prototype.

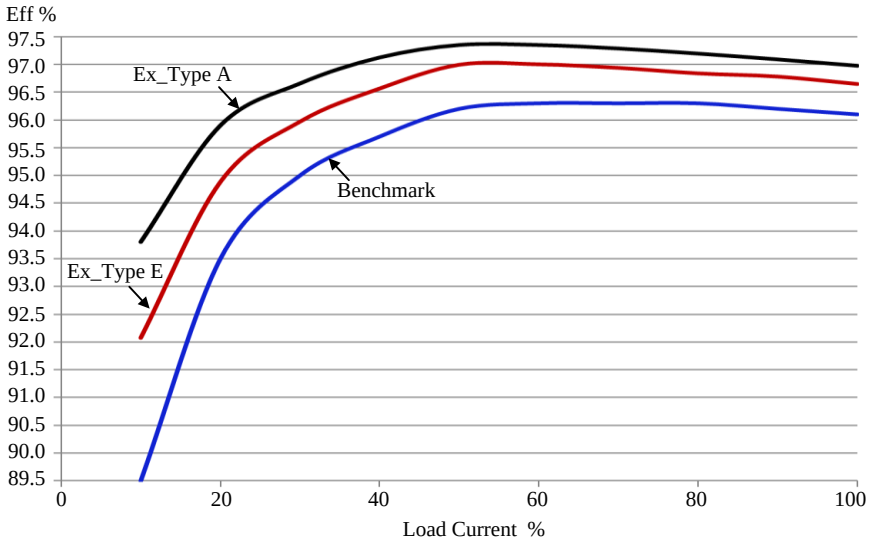
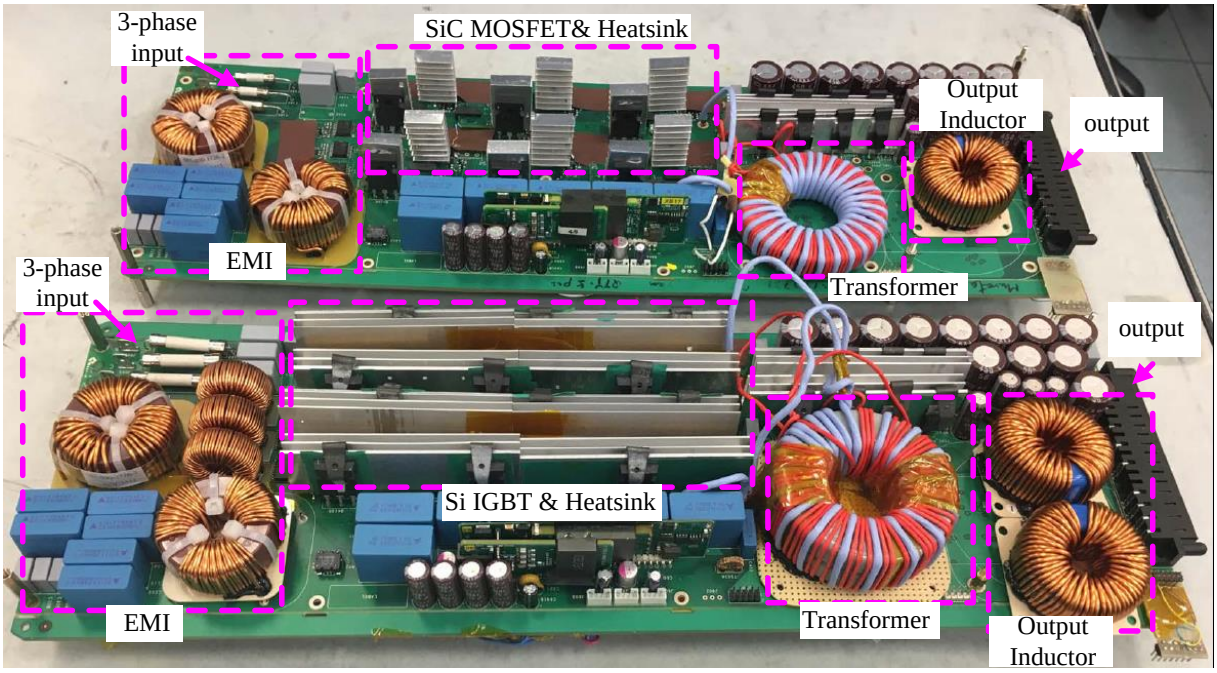


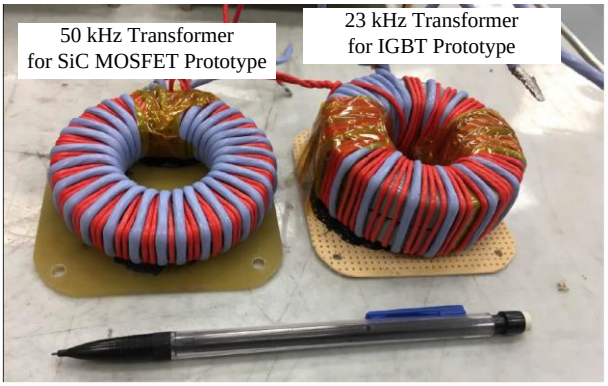
Fig. 3-11 Experimental efficiency comparison between proposed PSU with implementation of "Type A" and improved "Type E" PWM schemes and benchmark (Vienna rectifier + LLC).

3.2.5 Comparative Efficiency and Power Density Evaluation of Si IGBT-Based and SiC MOSFET-Based 380 V Prototypes

This section evaluates the efficiency and power density of SiC MOSFET-based prototype with respect to Si IGBT-based prototype. Fig. 3-12 (a) shows two 5 kW prototypes of three-phase isolated buck matrix-type rectifier with 380 V output.



(a)



(b)

Fig. 3-12 Power denisty comparison on Si IGBT-based and SiC MOSFET-based 380 V: (a) prototypes and (b) transformers.

The SiC MOSFET-based prototype operates at 50 kHz while the Si IGBT-based prototype operates at 23 kHz. An Si IGBT showing a good compromise between switching energies and forward voltage was selected as the more appropriate alternative for the comparison against the SiC MOSFET presented here. The toroidal core is opted to satisfy the transformer design requirement, because the toroidal core provides the most desirable voltage isolation level compared with other core shapes. Ferrite toroid also offers high magnetic efficiency as the cross-sectional area is uniform and does not need a bobbin, which also results in a compact design of the transformer. Fig. 3-11 (b) shows the picture of transformers for both prototypes. Due to the lower switching frequency, transformer of Si IGBT-based prototype is built with two core stacked together. Both prototypes operate under ZVS condition (no turn-ON loss) up to 40% load.

The loss breakdown and efficiency comparison for SiC MOSFET-based and Si IGBT-based prototype are provided in Fig. 3-13 and Fig. 3-14 respectively. The overall efficiency of the Si IGBT-based prototype is dramatically lower compared with the SiC MOSFET-based counterpart. The efficiency of the Si IGBT-based prototype drops significantly with the increased switching frequency as shown in Fig. 3-14. The main reason for the clear superiority of SiC MOSFETs in the application is their ohmic output characteristics and the absence of stored charge in the conducting device. The former allows considerably lower conduction losses in part-load operation than in-built forward voltage drop of bipolar IGBTs as shown in the loss breakdown of Fig. 3-13. The latter enables very low switching losses, whereas the tail current effect due to the internally stored charge causes large turn-OFF loss with Si IGBTs.

In the data center and telecom applications, there are quite high cost pressure and a very competitive market. Si IGBTs offer much lower unit price than SiC MOSFET. However, the higher semiconductor losses and thus lower permissible switching frequencies of Si IGBT-based prototype entail a larger and more expensive cooling system, PCB and passives, which largely compensate the cost advantage of Si IGBTs. This finally results in similar total cost of the two prototypes. The power density of Si IGBT prototype is 37.8 W/in^3. In SiC MOSFET-based prototype, the three-phase isolated buck matrix-type rectifier operates more than twice the switching frequency of Si IGBT-based prototype.

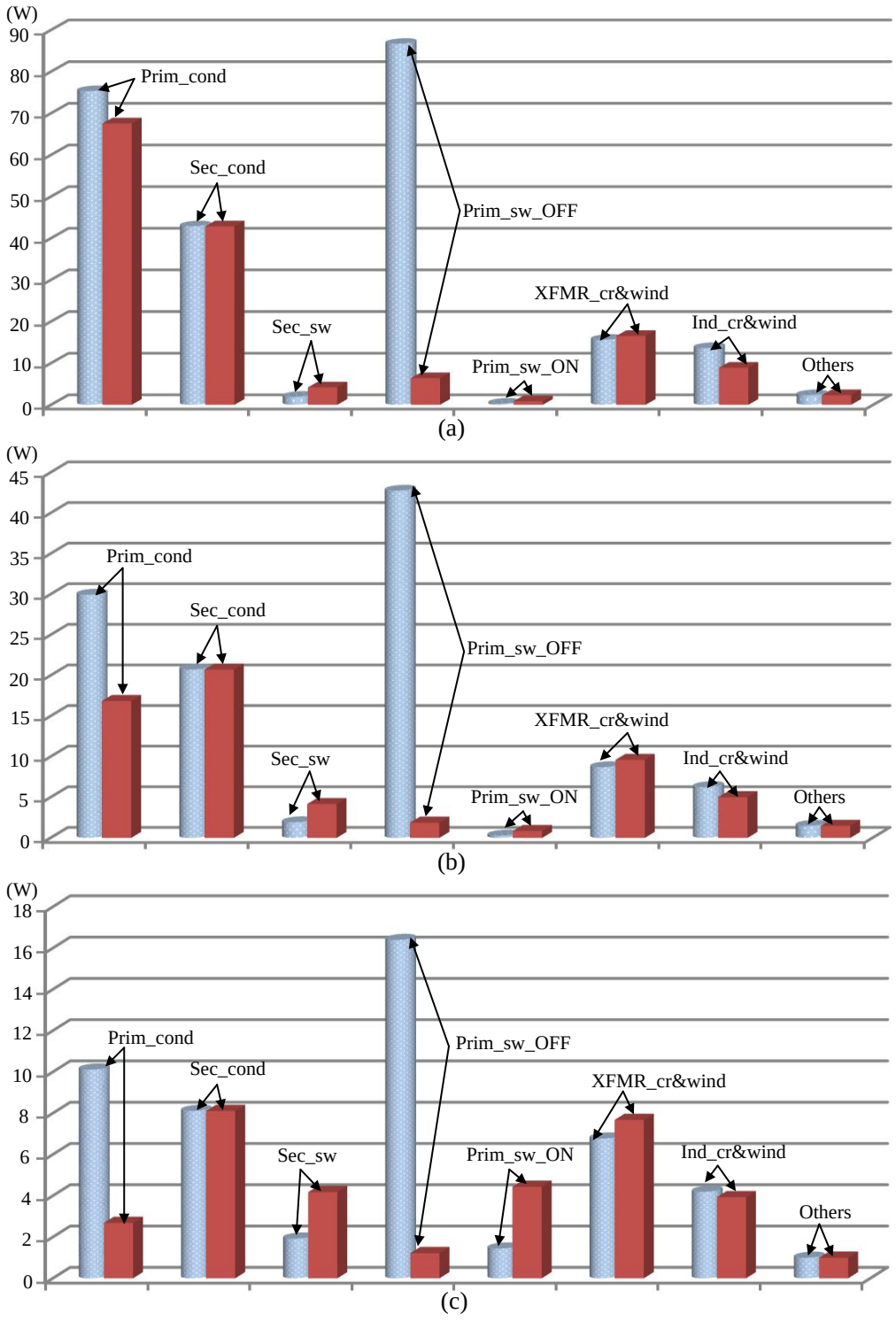


Fig. 3-13 Loss breakdown comparison on Si IGBT-base (left bar) and SiC MOSFET-based (right bar) 380 V prototypes: (a) Loss comparison at 5kW (100% load), (b) Loss comparison at 2.5kW (50% load) and (c) Loss comparison at 1 kW (20% load).

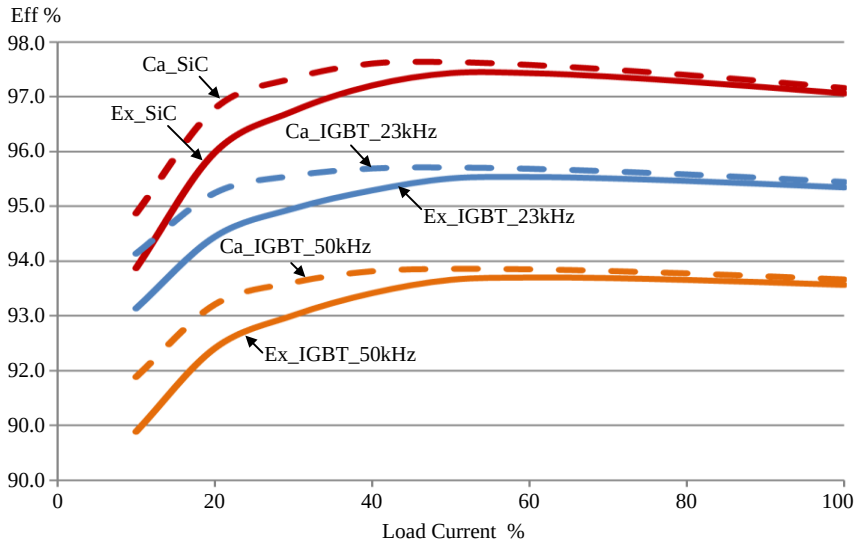


Fig. 3-14 Experimental (solid-line) and calculated (dash-line) efficiency comparison on SiC MOSFET-based and Si IGBT-based 380 Vprototype.

Hence, more than twice the power density of Si IGBT (> 76 W/in^3) can be expected. It is also worth mentioning that, the higher switching frequency also leads to a better performance such as THD and transient responses due to the higher achievable control bandwidth, etc. It is also important to note that by replacing the output bridge diode rectifier with 30 mΩ SiC MOSFET, the efficiency will gain 0.68% and by replacing the primary bidirectional SiC MOSFETs with lower R_{DS_on} (30 mΩ), the efficiency will gain additional 0.45% which results in an overall efficiency > 98.5%. In addition, by placing the output capacitors outside of the PSU, the overall power density is expected to exceed 100 W/in^3 which is much higher than benchmark 380 V PSU.

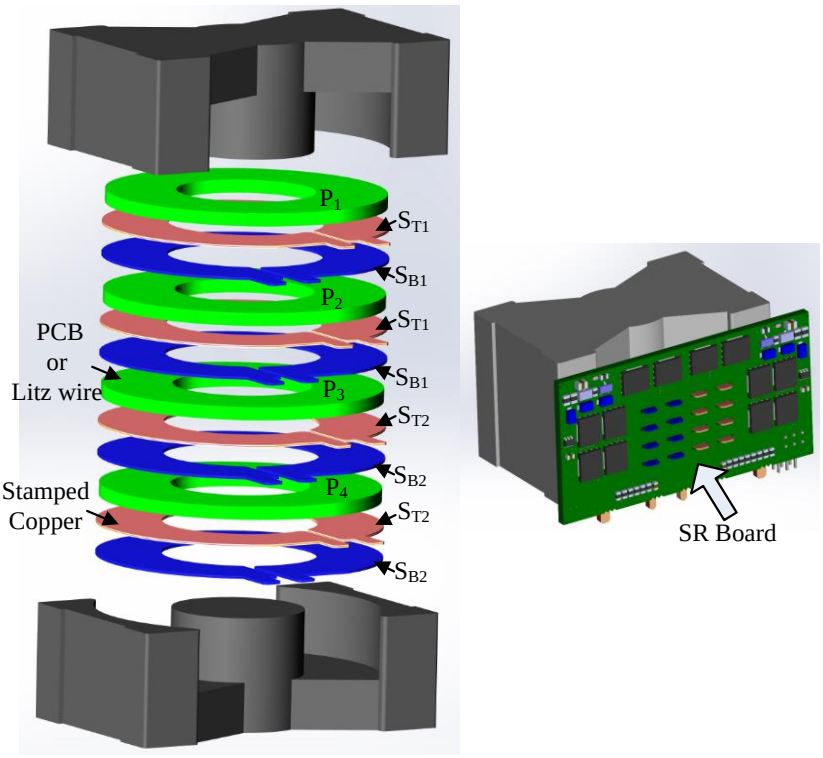
3.2.6 Analysis of Loss Breakdown and Efficiency for SiC MOSFET-Based 54 V Prototype

Loss analysis is conducted on SiC MOSFET-based 54 V prototype based on parameters given in Table 3-3. Transformer core loss and winding loss calculation is based on the transformer structure shown in Fig. 3-8.

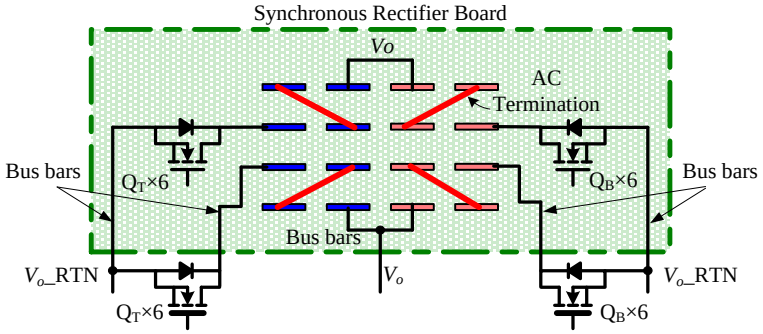
Table 3-3 Experimental prototype parameters for 54 V output.

Prototype Parameter	Value
C_f	5 μF
L_f	90 μH
$v_{LL,rms}$	480 V
f_{Grid}	60 Hz
C_o	1.5 mF
L_o	315 μH
V_o	54 V
$L_{lk\_Six\_Seq}$	10 μH
S_{11} - S_{26}	SCT3080KL (SiC1 Prototype) C2M0025120D (SiC2 Prototype)
SR MOSFET	BSC093N15NS5
$n = N_2/N_1$	2/32
2 x TR_{core}	Ferrite 3C96 (PQ50) Primary Litz Wire (Rubadue # TXXL230/44F3XX-2) Secondary Stamped Copper (8 Ounce)
f_{TR}	50 kHz
Microcontroller	TMS320F28075

It should be noted that design of high efficiency and high power density transformer for 54 V output is relatively more challenge compared with 380 V transformer due to the significantly higher current on the secondary side of the transformer. As discussed in Chapter 1, 1U (40 mm) height PSU is popular for data center and telecom applications. In order to design a transformer with 1U height limitation, the proposed transformer structure shown in Fig. 3-8 and Fig. 3-15 is adopted. Single-turn stamped copper windings are used on the secondary side of the transformer to carry high output current. Triple insulated Litz wire is used for primary windings to minimize the skin depth effect and meet the safety requirement for insulation. It should be noted that the primary windings can also be realized with PCB. The interleaved structure shown in Fig. 3-15 (a) can effectively reduce the magnetic-field-intensity such that the eddy current loss on the winding can be reduced. The center-tapped windings S_T and S_B are closely attached with thin captain tape in between for insulation to minimize the leakage inductance between them such that the voltage spike on the SR MOSFETs can be reduced. However, as shown from magnetomotive force (MMF) in Fig. 3-16 (a), there is a passive layer loss for winding S_T when S_B is active due to proximity effect since the AC magnetic field at S_T is not zero.



(a)



(b)

Fig. 3-15 High-density transformer structure for the 54 V application: (a) integrated with synchronous rectification (SR) board and (b) connection of secondary stamped copper windings to SR board.

Therefore, the thickness of the stamped copper needs to be properly selected as a compromise between AC losses and DC losses. Since the switching frequency is only 50 kHz, the thickness of 12 mil (8 ounce copper) can be a good choice. However, the associated loss of the passive layer can be easily eliminated by rearranging the interleaving structure of transformer winding similar as interleaved configuration reported in [61].

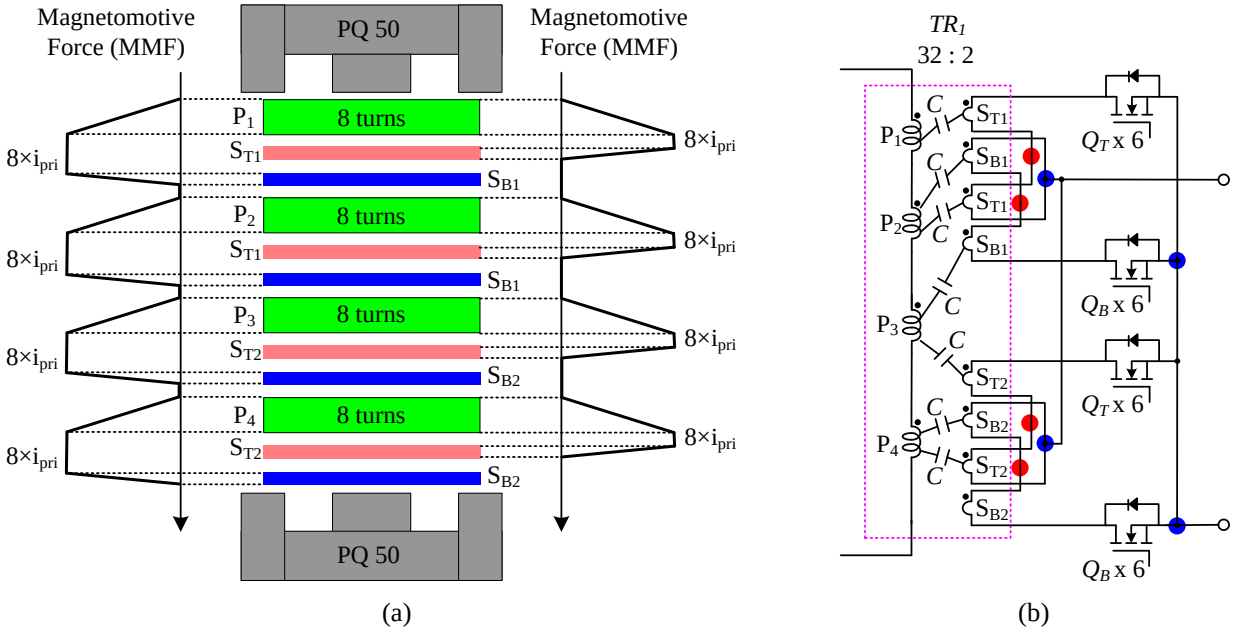


Fig. 3-16 Interleaved transformer structure (a) Magnetomotive Force (MMF) (b) with Inter-winding capacitance and terminations (red circle is ac termination, blue circle is dc termination).

It is worth mentioning that the increased inter-winding capacitance due to interleave will have an advert effect on the common mode noise rejection since the inter-winding capacitances provide the feedthrough path for the common mode noise from the primary side to secondary side of the transformer as shown in Fig. 3-16 (b). The stamped copper windings are terminated on a vertical synchronous rectification (SR) board to minimize the distance of current path between secondary windings and SR MOSFETs as shown in Fig. 3-15. Besides the winding losses, the termination loss is also an important factor impacting the efficiency, due to high currents passing through them. Especially the high frequency AC current (red arrow) tends to pass the surface of the terminals due to the proximity effect and skin effect such that high conduction losses and hot spots are generated. Therefore, it is important to minimize the AC current loop in order to reduce the termination losses. As shown in Fig. 3-8, the secondary side of the transformer contains two sets of center-tapped rectifiers. Each set of center-tapped rectifier uses six SR MOSFETs (Q_T×6) for top side and another six SR MOSFETs (Q_B×6) for bottom side.

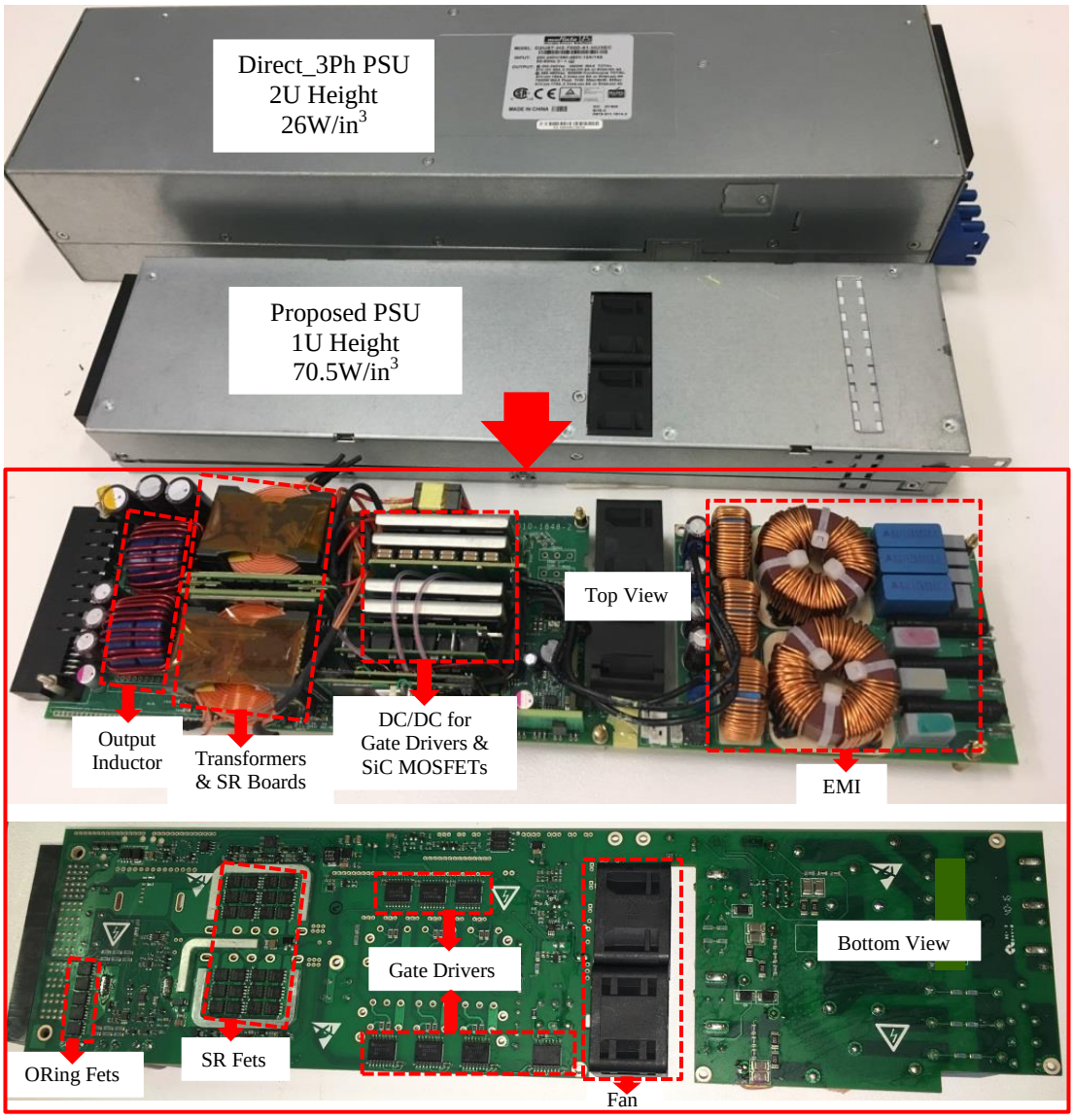


Fig. 3-17 Power density comparison of proposed PSU (isolated buck matrix-type rectifier) and direct three-phase PSU (Vienna rectifer + LLC) for 54 V output application.

The outputs of the two sets of rectifier are connected in parallel through copper bus bars. Using two sets of rectifier and paralleling them on the DC side can help reduce the termination loss compared with paralleling the winding directly on the AC terminals. It should be noted that half of the SR FETs is located on the synchronous rectification board as shown in Fig. 3-16 and the other half is located on the bottom of the main PCB due to the limited space as shown in bottom view of the PCB in Fig. 3-17.

It should be noted that it is difficult to calculate the AC termination and passive layer losses without simulation tool. Simulation using finite element analysis software such as ANSYS/Maxwell is required to accurately calculate the termination and passive layer losses.

Fig. 3-17 shows a 5 kW SiC MOSFET-based prototype of three-phase isolated buck matrix-type rectifier with 54 V output voltage. The 54 V prototype has an overall power density of 70.5 W/in^3 which is higher than any best existing PSU in the market. In today`s market, the direct three-phase (Vienna rectifier + LLC) PUS has 26 W/in^3 and single-phase (bridgeless PFC + three-phase interleaved LLC) PSU has 56 W/in^3. The proposed prototype is evaluated at 50 kHz for two different SiC MOSFET devices. SiC1 has $R_{DS\_on} = 110$ mΩ and SiC2 has $R_{DS\_on} = 35$ mΩ.

The total loss breakdown at 100%, 50% and 20% load current is shown in Fig. 3-18. At 100% and 50% load, the SiC1 has significantly larger conduction loss compared with SiC2 since the R_{DS_on} of SiC1 is three times larger than SiC2. However, SiC2 has larger turn-ON and turn-OFF switching losses compared with SiC1 since SiC2 has larger E_{oss} and $E_{off.}$ The turn-ON loss is very small at 100% and 50% load since the converter operates under ZVS condition and the small turn-ON loss is only contributed by two non-ZVS switches which is inherent in “Type A” PWM scheme.

As shown in Fig. 3-19, SiC2 exhibits higher efficiency compared with SiC1 for load current above 40% when the condition of ZVS is met. SiC1 and SiC2 have peak efficiencies of 97.9% and 98.3% respectively at 50% load. In addition, SiC2 maintains efficiency higher than 98% for all load above 40% due to significantly lower conduction loss compared with SiC1. It should be noted that the measured efficiency is noticeably lower than the calculated results at light load which is mainly due to the uncounted parasitic capacitances. Similarly at heavy load, this is mainly caused by the transformer AC termination and passive layer losses which were not considered in the transformer loss calculation.

Fig. 3-20 shows the efficiency comparison for 54 V application with proposed PSU and the benchmark. For all load conditions, the proposed PSU exhibits higher efficiency than the direct three-phase (Vienna rectifier + LLC) and single-phase (bridgeless PFC + three-phase interleaved LLC) PSUs.

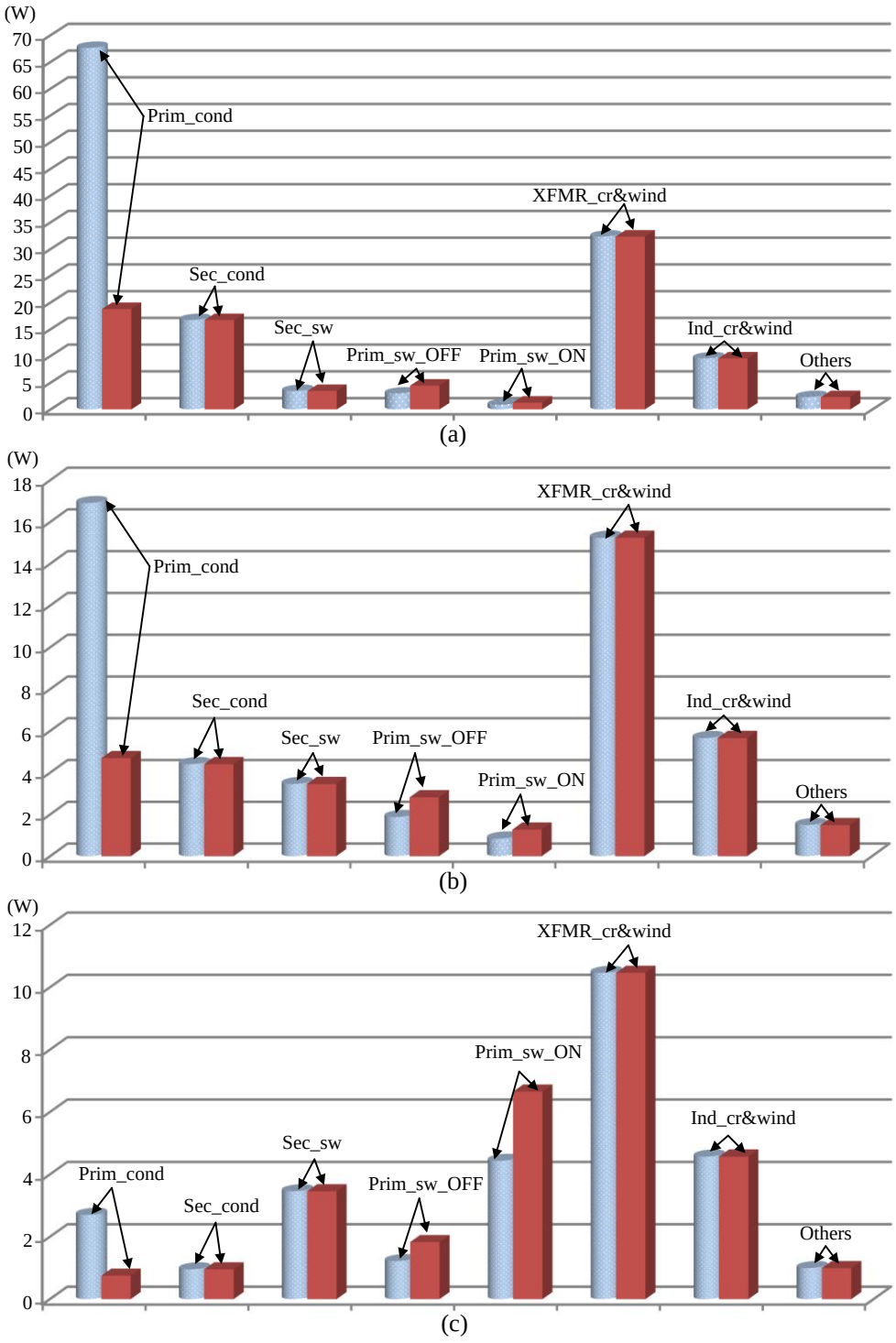


Fig. 3-18 Loss breakdown comparison on 110 mΩ (left bar SiC1) and 35 mΩ (right bar SiC2) SiC MOSFET-based prototype with V_o = 54 V and v_{LL} = 480 V: (a) Loss at 5 kW (100% load), (b) Loss at 2.5 kW (50% load) and (c) Loss at 1 kW (20% load).

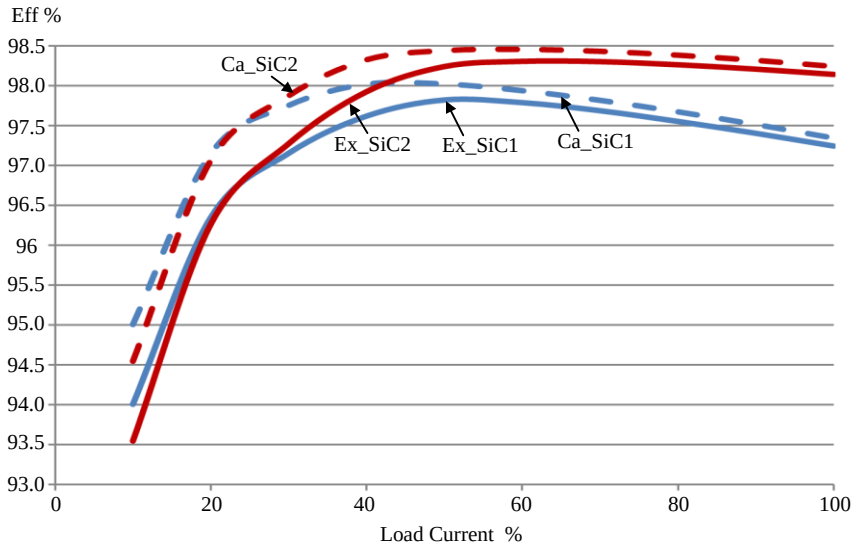


Fig. 3-19Experimental (solid-line) and calculated (dash-line) efficiency comparison on 110 mΩ and 35 mΩ SiC MOSFET-based 54 V prototype.

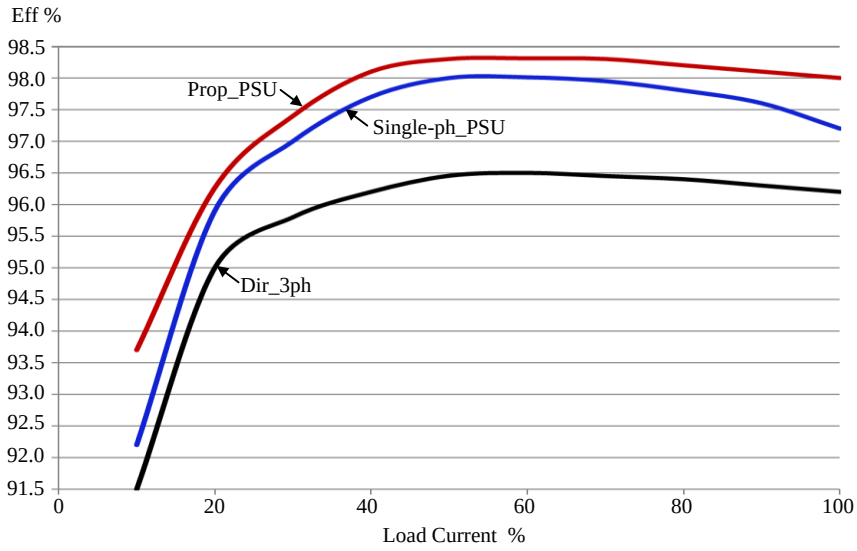


Fig. 3-20Experimental efficiency comparisons between proposed PSU (isolated buck matrix rectifier using 35 mΩ SiC MOSFET) and two types of the benchmark PSUs: single-phase PSU (bridgeless PFC + three-phase interleaved LLC resonant converter) and direct three-phase PSU (Vienna rectifier + LLC resonant converter).

3.3 Conclusions

An improved eight-segment PWM scheme (improved “Type E”) for the three-phase isolated buck matrix-type rectifier is proposed which overcomes a major drawback of a large output inductor current ripple with traditional eight-segment PWM scheme (“Type E”). With the reduction of output inductor current ripple, a smaller output inductor size can be realized. In addition, two-step commutation method with ZVS turn-ON is applied in improved “Type E” to eliminate the two non-ZVS switching actions associated with “Type E”. This improves the light load efficiency when the rectifier operates at very high frequency. The loss breakdown and efficiency curves are provided for 54 V and 380 V prototypes. First, two PWM schemes “Type A” and improved “Type E” are compared for loss breakdown and efficiency on SiC MOSFET-based 380 V prototype. The efficiency comparison reveals that “Type A” exhibits higher efficiency especially at light load with a nearly 2% efficiency boost. Then the efficiency curve and loss breakdown comparison are provided for both SiC MOSFET-based and Si IGBT-based 380 V prototypes. From the efficiency comparisons, SiC MOSFET-based prototype exhibits a significantly higher efficiency than Si IGBT-based prototype.

Chapter 4

One Phase Loss Operation of Isolated Buck Matrix-Type Rectifier

One phase loss can be defined as one phase opened or one phase shorted. For the case of one phase opened, one of the phase inputs of the converter is disconnected from the main due to the tripping of the fuse. For the case of one phase shorted, one of the phase inputs of the converter is connected to the neutral of the main as could be caused by an earth fault. The fuse of that faulty phase is tripped as well to isolate the fault from main. In both cases, the fault phase is not able to deliver the power and the output of the converter will lose regulation. The main focus of this chapter is on developing a viable strategy to maintain proper operation of the rectifier during one phase loss condition as well as to provide smooth transitions between the faulty and normal modes. Since it is a big challenge for the single-stage isolated buck matrix-type rectifier to maintain proper output voltage under this faulty mode and guarantee safe operation during the transitions, it is this studies' aim to provide an applied solution to these issues which have never been studied in the literature for this particular topology. A desired modulation scheme to maximize the available rectifier output voltage for phase loss operation is proposed which is based on the extension of ZVS FB-PS DC-DC converter. With the proposed PWM scheme, the maximum available voltage gain for one phase loss operation can be achieved. This permits the continuous operation of the rectifier to deliver two-third of rated power and to regulate the output voltage with maximum output voltage drop less than 5% of nominal output voltage.

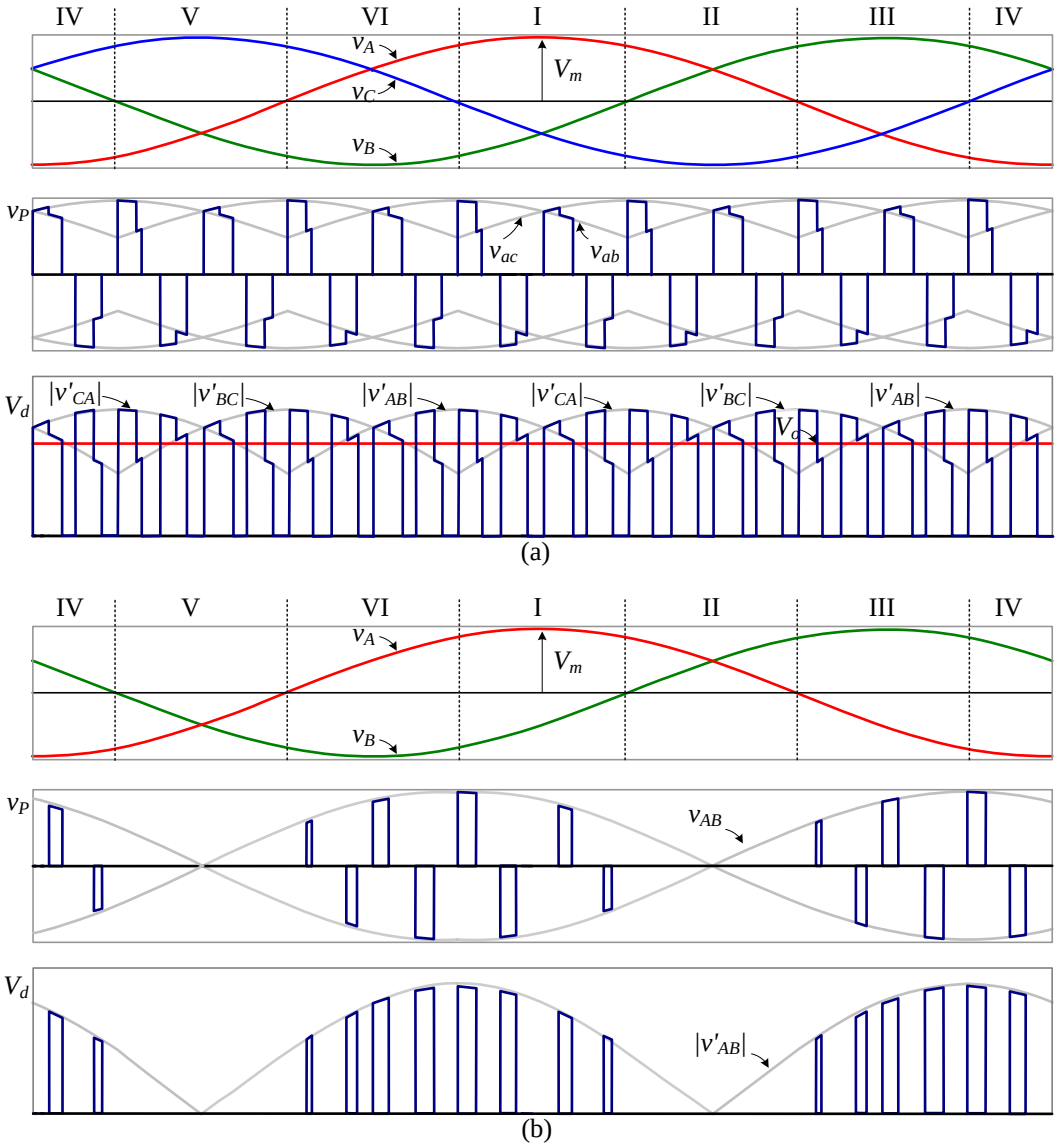


Fig. 4-1 Voltage waveforms correspond to circuit in Fig. 2-1: (a) three-phase operation (normal operation) and (b) when "phase *C*" is lost (one phase loss operation).

In addition, with the proposed commutation method, a safe transition from one phase loss operation to normal operation and vice versa can occur with minimum commutation steps (two-step) under zero voltage switching (ZVS) condition. The performance including output voltage regulation, input currents THD and dynamic switching behavior of the proposed PWM scheme and commutation schemes during one phase loss operation is evaluated and verified by simulations and experiments on 380 V prototype at 5 kW rated power.

4.1 Analysis of Rectifier during One Phase Loss Operation and Principle of Operation

The six-segment and eight-segment PWM schemes which are realized for three-phase isolated buck matrix-type rectifier operation cannot be directly applied for one phase loss operation since with them the output voltage drop and required output inductor current for sustaining two-third rated power is noticeably large. This will be mathematically analyzed in this section. The operation principle of the three-phase isolated buck matrix rectifier during normal operation when all the three phases are empowered in the converter is discussed in Chapter 2. As mentioned in there, the three-phase converter can be redrawn as "bridge *x*" and "bridge *y*" in each sector. Fig. 4-2 (a) shows the equivalent circuit of the converter in sector I which is identical to operation of FB-PS DC-DC converter.

The circuit principal waveforms within one complete gird side cycle with excessively increased switching period of PWM can be observed in Fig. 4-1 (a). Due to the alternative operation of "bridge *x*" and "bridge *y*", there are always two of the three line voltages involved to generate the pulses in each switching cycle. For example in sector one, "bridge *x*" generates the pulses with the magnitude of v_{AB} and "bridge *y*" generates the pulses with the magnitude of v_{AC}. Therefore, the output voltage is synthesized by two of the line to line voltage as shown in the secondary side rectifier output voltage V_d. Modulation index m_a is used to adjust the output voltage V_o. When one phase is lost (for example; "phase *C*" is lost for all the analysis in this dissertation), the switches related to this phase needs to stop gating since no power can be delivered from this bridge as shown in Fig. 4-2 (b). Besides, for the safe operation of the converter as this will be further discussed in this chapter. In this case, line to line voltage v_{BC} and v_{CA} will not exist and the only available input voltage is v_{AB}. As shown in Fig. 4-1 (b), only the pulses associated with v_{AB} exist. Seemingly, it is difficult to regulate the output voltage even with m_a equal to unity since the maximum available duty cycle of the pulses with v_{AB} is limited by the PWM scheme for the normal operation. This problem is mathematically described in the following section.

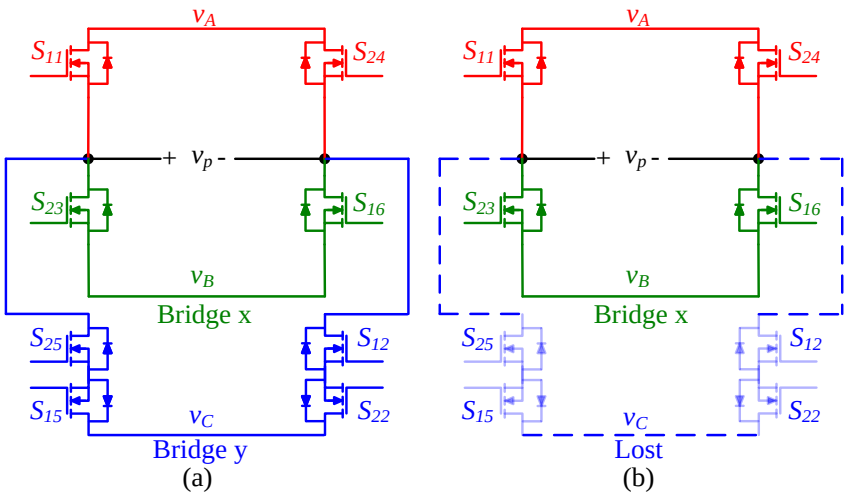


Fig. 4-2 Three-phase rectifier redrawn as: (a) two FB-PS DC-DC converters when the three phases are connected and (b) a single FB-PS converter during one phase loss ("phase *C*").

4.1.1 Analysis of One Phase Loss Operation with Three-Phase PWM Scheme

Due to the rectification on the secondary side, the magnitude of the pulses of V_d is the absolute value of v_{AB} and v_{AC} with respect to the secondary side of transformer. Since the rectifier behavior of our interest in this analysis is slow dynamic compared with switching behavior, the average model of V_d is used instead to simplify the analysis by neglecting the switching events of V_d. Therefore, the average voltage of V_d in each switching cycle can be expresses as

$$\bar{v}_d(\theta) = \left|v_{AB}'(\theta)\right| D_x(\theta) + \left|v_{AC}'(\theta)\right| D_y(\theta) \tag{3-4}$$

where $\left|v_{AB}'(\theta)\right|$ and $\left|v_{AC}'(\theta)\right|$ are the absolute value of v_{AB} and v_{AC} with respect to the transformer secondary side; $D_x(\theta)$ and $D_y(\theta)$ are the duty-cycle of $\left|v_{AB}'(\theta)\right|$ and $\left|v_{AC}'(\theta)\right|$ respectively. $\left|v_{AB}'(\theta)\right|$ and $\left|v_{AC}'(\theta)\right|$ can be expressed as

$$\begin{cases} \left|v_{AB}'(\theta)\right| = n\sqrt{3}V_m \left|\sin(\theta + \frac{2\pi}{3})\right| \\ \left|v_{AC}'(\theta)\right| = n\sqrt{3}V_m \left|\sin(\theta + \frac{\pi}{3})\right| \end{cases}. \tag{3-5}$$

With the conventional space vector modulation scheme presented in Chapter 2, $D_x(\theta)$ and $D_y(\theta)$ can be expressed as

$$\begin{cases} D_x(\theta) = m_a \sin(\frac{\pi}{6} - \theta) \\ D_y(\theta) = m_a \sin(\frac{\pi}{6} + \theta) \end{cases} \tag{3-6}$$

where m_a is the modulation index and in the range of $0 \le m_a \le 1$.

At steady-state, when converter is under regulation, $\bar{v}_d(\theta)$ is equal to output voltage V_o. During one phase loss operation ("phase *C*" lost), v_{AC} does not involve in the operation of the rectifier and V_d contains pulses associated with v_{AB} only. The equation (4-1) should be revised as

$$\bar{v}_d(\theta) = \left|v_{AB}'(\theta)\right| D_x(\theta) = \left|v_{AB}'(\theta)\right| m_a \sin(\frac{\pi}{6} - \theta). \tag{4-4}$$

Based on the conventional SVM, either $D_x(\theta)$ or $D_y(\theta)$ is selected for the duty-cycle of V_d as shown in Fig. 4-3 (d). In sector II and V, $D_x(\theta)$ and $D_y(\theta)$ are zero since "phase *C*" is lost and the line voltages with "phase *C*" cannot be used. With the conventional space vector modulation scheme $\bar{v}_d(\theta)$ reaches to maximum at m_a = 1. By substituting $\left|v_{AB}'(\theta)\right|$ with (4-2) and m_a with 1 into (4-4), after elementary trigonometric transformations, the maximum available $\bar{v}_d(\theta)$ is derived as

$$\bar{v}_{d\_\max}(\theta) = nV_m(\frac{3}{4} - \frac{\sqrt{3}}{2}\sin(2\theta)) \tag{4-5}$$

The resultant $\bar{v}_{d\_\max}(\theta)$ from (4-5) is shown in Fig. 4-3 (c). During the interval T_{on} when $\bar{v}_{d\_\max}(\theta)$ is higher than V_o, the rectifier regulates V_o back to the set point. During the interval T_{off} when $\bar{v}_{d\_\max}(\theta)$ is lower than V_o the rectifier output is reverse blocked and V_o drops since V_o is only sustained by the output capacitors. In sector II and V, $\bar{v}_{d\_\max}(\theta)$ is zero since the rectifier stops switching due to very low magnitude of $\left|v_{AB}'(\theta)\right|$. The voltage drop ΔV_o is the function of T_{off}, output capacitance C_o, and load current I_o, and can be derived as:

$$\Delta V_o = \frac{I_o T_{off}}{C_o}. \tag{4-6}$$

As shown in Fig. 4-3 (c), T_{off} is the distance between the two adjacent crossing points when $\bar{v}_{d\_\max}(\theta)$ is lower than V_o. Assuming that the ripple voltage ΔV_o is relatively small compared with V_o, the location of these two adjacent crossing points can be found by equaling $\bar{v}_{d\_\max}(\theta)$ with V_o. Since the output voltage can be expressed as $V_o = \frac{3}{2} n V_m m_a$ during normal operation, the angle θ at the crossing point can be estimated by

$$\theta = \frac{1}{2}\sin^{-1}\left(\frac{\sqrt{3}}{2} - \sqrt{3} m_a\right). \tag{4-7}$$

It should be noted that there are two solutions from (4-7), and the one within the range of $-\frac{\pi}{6} < \theta < \frac{\pi}{6}$ will be used for the calculation below. Then, the T_{off} can be expressed as

$$T_{off} = \frac{\pi - (\theta + \frac{2\pi}{3})}{\pi f_{grid}} = \frac{\frac{1}{2}\sin^{-1}(\sqrt{3} m_a - \frac{\sqrt{3}}{2}) + \frac{\pi}{3}}{\pi f_{grid}} \tag{4-8}$$

where f_{grid} is the grid frequency. Finally, the voltage drop ΔV_o can be derived by substituting T_{off} with (4-8) into (4-6):

$$\Delta V_o = \frac{I_o[\frac{1}{2}\sin^{-1}(\sqrt{3}m_a - \frac{\sqrt{3}}{2}) + \frac{\pi}{3}]}{C_o \pi f_{grid}} \quad . \tag{4-9}$$

Due to the limited duty-cycle of normal PWM scheme as shown in Fig. 4-3 (c), v_{AB} cannot be fully utilized to regulate the output voltage, causing large output voltage drop.

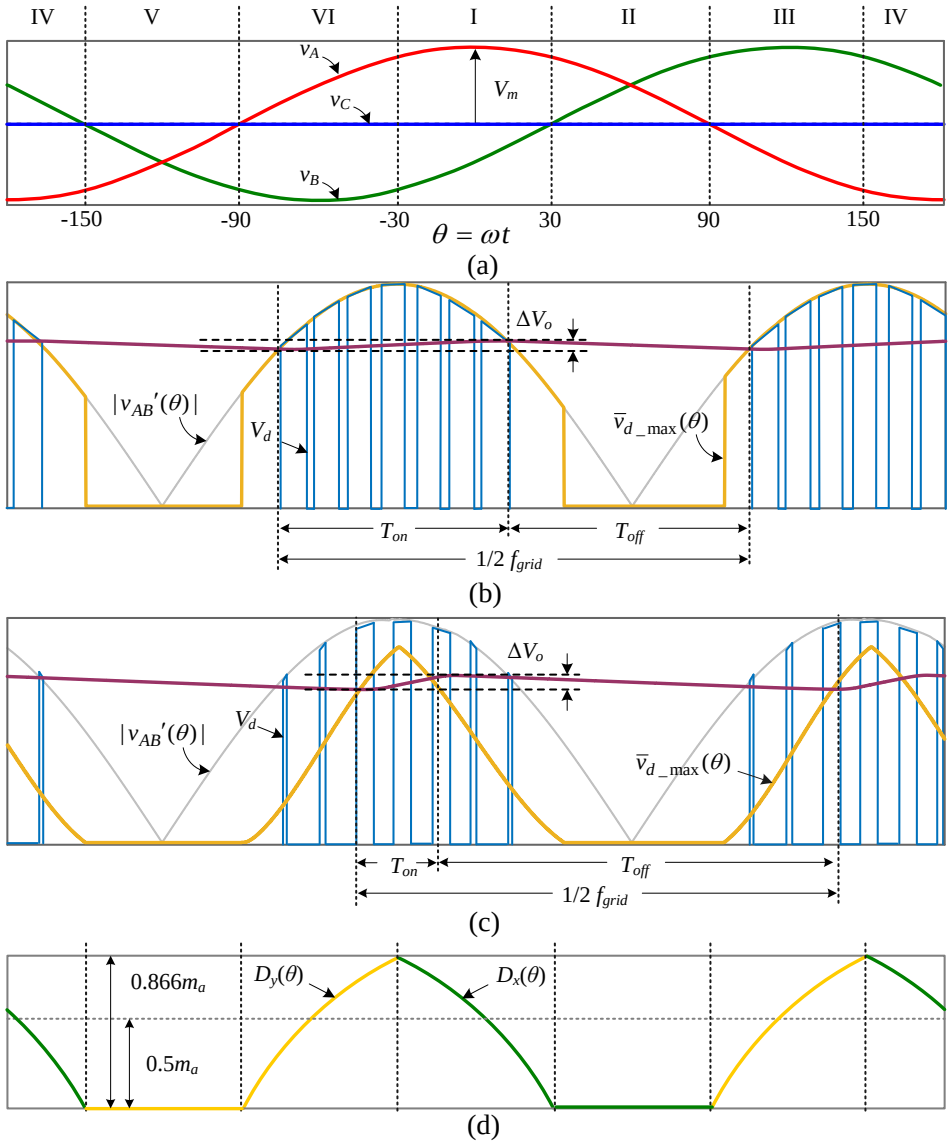


Fig. 4-3 One phase loss operation of three-phase buck matrix rectifer: (a) three-phase grid voltages with "phase *C*" is shorted, (b) with desired fault PWM for one phase loss operation converter, (c) with normal PWM applied to one phase loss operaion and (d) the duty-cyle corresponding to V_d in Fig. 2(c).

Therefore, applying a different PWM scheme from normal PWM scheme to regulate the output voltage of the rectifier during one phase loss is indispensable. Since the equivalent circuit with "Phase *C*" lost is exactly the same as a conventional FB-PS DC-DC converter. The same PWM scheme for FB-PS DC-DC converter can be directly applied in the rectifier during one phase loss operation as shown in Fig. 4-3 (b). The output voltage V_o is regulated by directly adjusting the duty-cycle of $V_{d.}$. Therefore, the average voltage of V_d can be expresses as

$$\bar{v}_d(\theta) = \left| v_{AB}'(\theta) \right| D(\theta) \tag{4-10}$$

where $D(\theta)$ is the duty-cycle of V_d in the range of $0 \le D(\theta) \le 1$. Then $\bar{v}_d(\theta)$ reaches to maximum at $D(\theta) = 1$. Neglecting the duty cycle loss, the maximum $\bar{v}_d(\theta)$ can be expressed as

$$\bar{v}_{d\_\max}(\theta) = \left| v_{AB}'(\theta) \right| \tag{4-11}$$

In this case, the maximum available voltage $\bar{v}_{d\_\max}(\theta)$ has the same magnitude as $\left| v_{AB}'(\theta) \right|$ which is much higher than that with normal PWM schemes as shown in Fig. 4-3 (c). The resultant voltage drop can be significantly reduced due to shorter interval of T_{off}. This will be further analyzed in the next section.

4.1.2 Principle Operation of Rectifier with Desireable PWM Scheme for One Phase Loss Operation

The circuit principal waveforms within one gird side cycle with desirable PWM when phase voltage v_c is shorted can be observed in Fig. 4-4, where v_P is the transformer primary voltage, V_d is the transformer secondary rectified voltage, I_L is the output inductor current and i_a, i_b , i_c are grid side currents. Since v_{AB}, the input voltage of "bridge *x*", is slow varying, the duty-cycle of the transformer voltage v_P or V_d needs to be adjusted accordingly in order to regulate the output voltage. When the magnitude of $\left| v_{AB}'(\theta) \right|$ is lower than V_o as shown in Fig. 4-4 (c), the duty-cycle of V_d reaches to maximum and V_o starts losing regulation. In this case, the rectifier should stop gating to reduce the switching losses and other associated losses. It is important to note that, a

large output ripple may be generated since the output voltage is only sustained by the output capacitors during the interval of T_{off}. Assuming the duty cycle loss of the buck converter is very small and can be neglected, in Fig. 4-4 T_{off} is the distance between the two adjacent crossing points when $|v'_{AB}|$ is lower than V_o. It is also assumed $T_1 = T_2$, since the ripple voltage ΔV_o is relatively small comparing with V_o. The location of these two adjacent crossing points can be found by equaling $|v'_{AB}|$ and V_o. Then, the T_{off} can be estimated by

$$T_{off} = \frac{\sin^{-1}(\frac{\sqrt{3}}{2} m_a)}{\pi f_{grid}} \tag{4-12}$$

where f_{grid} is the grid frequency.

By combining (4-6) and (4-12), the ripple voltage ΔV_o is described as

$$\Delta V_o = \frac{I_o \sin^{-1}(\frac{\sqrt{3}}{2} m_a)}{C_o \pi f_{grid}} \ . \tag{4-13}$$

When one phase is lost, the output power is reduced to two-third of rated power in order to limit the RMS value of phase currents $i_{a,b,c}$. One of the criteria of selecting capacitance of C_o is that the resultant maximum output voltage drop ΔV_o should be smaller than the difference between the set point of output voltage and the set point of the battery voltage to avoid the battery engagement during one phase loss operation. For example, if the rectifier output voltage set point is 380 V and the battery voltage set point is 360 V, the maximum of ΔV_o should be smaller than 20 V. A reasonable value of 2 mF for the output capacitance is selected as a compromise between the output voltage ripple and power density of the converter. Current stress is another important consideration when the rectifier operates during one phase loss. As shown in Fig. 4-4 (d), the output inductor current ramps up fast and reaches to the maximum value of I_{clamp} due to the fast response of the current control loop and large voltage error at the beginning of T_{on}. I_{clamp} is the upper clamping value for the current control loop.

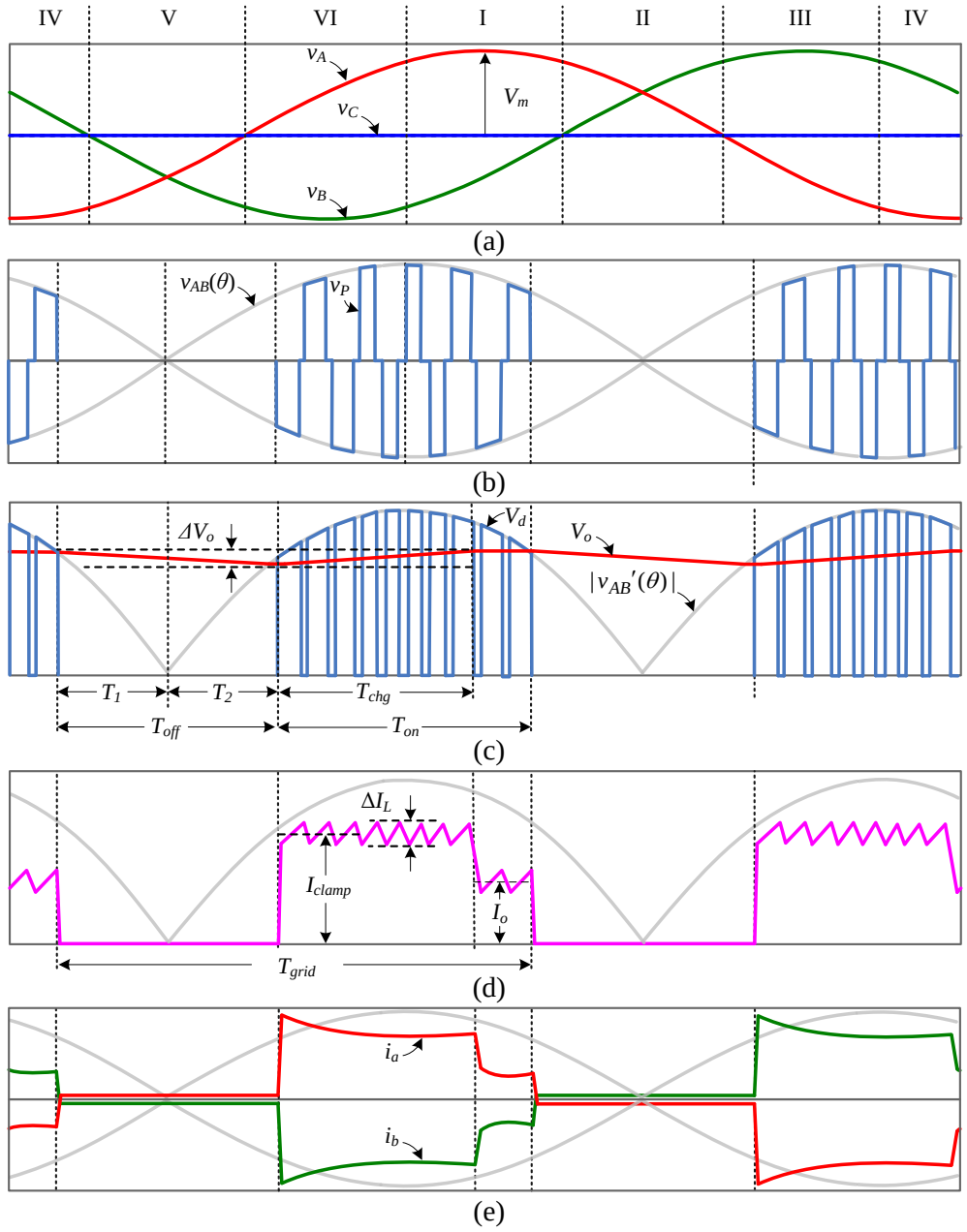


Fig. 4-4 Rectfier operation with "phase *C*" is shorted.

During the interval of T_{chg}, the output capacitor is charged by the current of (I_{clamp} - I_o), and the output voltage rises up until it reaches to the set point (380 V). During the interval when the output voltage is regulated at the set point, the inductor current equal to the load current and no charging and discharging currents go through the output capacitor (neglecting the inductor

current switching ripple). Since the output capacitor is discharged by I_o during T_{off} and based on the current-second balance of the output capacitor, the relationship between I_{clamp} and I_o can be derived as

$$(I_{clamp} - I_o)T_{chg} = I_o T_{off} \,. \tag{4-14}$$

Since the output capacitor voltage has to be charged to the set point within the time interval of T_{on} in order to maintain regulation, the charging time has to meet $T_{chg} \le T_{on}$. Then the minimum value of I_{clamp} is derived at $T_{chg} = T_{on}$ as shown in (4-15)

$$I_{clamp\_\min} = \frac{I_o(T_{off} + T_{on})}{T_{on}} = \frac{I_o T_{grid}}{T_{grid} - T_{off}} \tag{4-15}$$

where $T_{grid} = 1/2\, f_{grid}$ is the half-cycle of the grid duration.

Considering the maximum load current of one phase loss operation $I_o = 2/3 I_{rated}$ and substituting T_{off} with (4-12) and T_{grid} with $1/2\, f_{grid}$ into (4-15), $I_{clamp\_\min}$ can be described as

$$I_{clamp\_\min} = \frac{\frac{2}{3} I_{rated}}{1 - \frac{2}{\pi}\sin^{-1}(\frac{\sqrt{3}}{2} m_a)} \,. \tag{4-16}$$

Lowering I_{clamp} can reduce the current stress of the converter during one phase loss operation and the output inductor can be designed with smaller size and lower cost. However, I_{clamp} should be higher than $I_{clamp\_\min}$ in order to deliver $2/3 P_{o\_max}$ during one phase loss operation. Fig. 4-5 shows the curve of voltage drop ΔV_o vs C_o for one phase loss operation with three-phase (normal) PWM schemes studied in Chapter 2 and with proposed PWM for one phase loss operation at different m_a. It can be concluded that the required output capacitance with the proposed PWM can be much lower than that with normal PWM scheme to meet the same voltage drop. It also shows that higher m_a results in larger voltage drop. It should be noted that m_a here refers to the modulation index of normal operation prior to the fault.

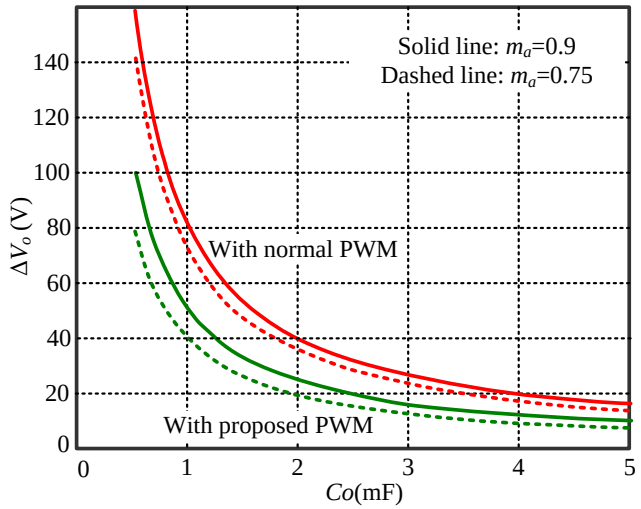


Fig. 4-5 The output voltage drop ΔV_o versus C_o in one phase loss operation at I_o = 2/3I_{rated} and f_{grid} = 50 Hz.

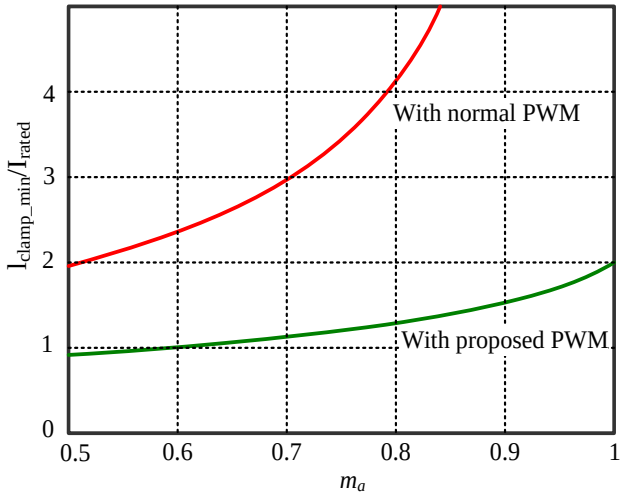


Fig. 4-6 The over current ratio I_{clamp_min}/I_{rated} versus m_a in one phase loss operation at I_o = 2/3I_{rated} and f_{grid} = 50 Hz. current stress can be remarkably smaller to regulate the output voltage during one phase loss operation.

The minimum required inductor current $I_{clamp\_min,3Ph\_PWM}$ to regulate the output voltage with normal (three-phase) PWM scheme is given by

$$I_{clamp\_min,3Ph\_PWM} = \frac{2I_{rated}}{1-\frac{3}{\pi}\sin^{-1}(\sqrt{3}m_a - \frac{\sqrt{3}}{2})}. \quad (4\text{-}17)$$

The minimum required inductor current to regulate the output voltage with normal PWM scheme and desired (FB-PS) PWM scheme for one phase loss operation are compared at

different m_a as shown in Fig. 4-6. With the desired PWM scheme for one phase loss operation, the current stress can be remarkably smaller to regulate the output voltage during one phase loss operation.

4.2 PWM Scheme for One Phase Loss Operation

Within every 180° interval the three-phase rectifier is operated as a ZVS FB-PS DC-DC converter as shown in Fig. 4-7. To achieve ZVS, the two legs of the bridge are operated with a phase shift. During every 180° interval, eight out of twelve switches are involved and the switches connected to the leg with phase loss are not involved. All the switches of the converter are turned ON under ZVS condition. Among these eight switches, four switches operate as active switches with hard-switching turn-OFF and the other four switches operate as synchronous rectification switches can be kept on all the time since their body diodes are forward biased. For example, during the 180° interval where the voltage potential v_A is higher than v_B ($v_A > v_B$), the switches S_{14}, S_{21}, S_{13} and S_{26} of bridge are synchronous rectification switches and can be kept on all the time. The rest four switches ($S_{11,}$ $S_{24,}$ $S_{23,}$ S_{16}) operate in a same manner of ZVS FB-PS converter. Similarly, during the other 180° interval where the voltage potential v_B is higher than v_A ($v_B > v_A$), the switches S_{23}, S_{16}, S_{11} and S_{24} are synchronous rectification switches and can be kept on all the time. The rest four switches ($S_{21,}$ $S_{14,}$ $S_{13,}$ S_{26}) operate in a same manner of ZVS FB-PS converter. The corresponding switch gate signals during one switching period T_s is shown in Fig. 4-8. It is important to be noted that there are two possible switching patterns in each 180° interval. For example, during the 180° interval with $v_A > v_B$, there are two type of switching patterns as shown in Fig. 4-8 (a) and (c) respectively. In each switching cycle, there are two bypassing intervals where switches of either phase "leg *A*" or phase "leg *B*" are used for bypassing (v_P = 0). As shown in Fig. 4-8 (a), switches ($S_{16,}$ S_{23}) of phase "leg *B*" are used for bypassing in the first bypassing interval and switches ($S_{11,}$ S_{24}) of phase "leg *A*" are used in the second bypassing interval.

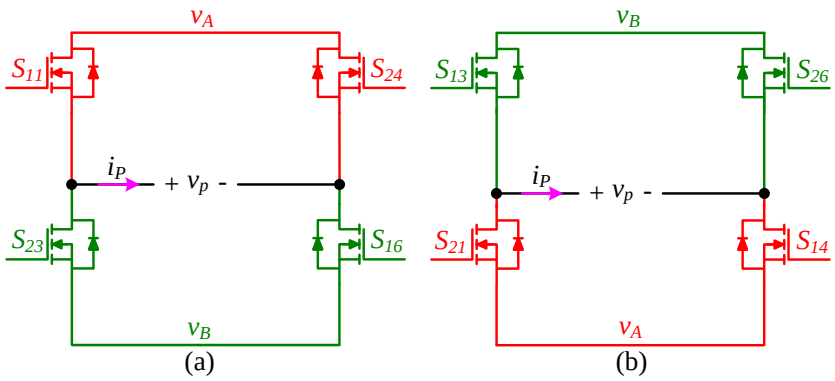


Fig. 4-7 Equivelant circuit for "Phase *C*" lost when (a) $v_A > v_B$ in sector VI and I (b) $v_A < v_B$ in sector III and IV.

While in switching pattern of Fig. 4-8 (c), switches ($S_{11,}$ S_{24}) of phase "leg *A*" are used for bypassing in the first bypassing interval and switches ($S_{16,}$ S_{23}) of phase "leg *B*" are used in the second bypassing interval. Identical voltage on the transformer primary side can be generated by these two switching patterns. However, the switching pattern needs to be properly selected in each sector to enable a smooth transition from one phase loss operation to normal operation (the lost phase recovered). In order to facilitate a smooth transition from one phase loss operation to normal operation, the switching state during the second bypassing interval at the end of each switching cycle must be the same as the bypassing switching state for normal operation. For normal operation, the switches of the phase leg whose voltage has the highest magnitude are used for the two bypassing (zero vector) intervals in each switching cycle.

Both normal operation and one phase loss operation must use the same phase leg for bypassing at the end of the switching cycle. For example, in sector I and sector IV, phase voltage v_A has the highest magnitude and the switches of phase "leg *A*" are used for bypassing at end of the switching cycle as shown in Fig. 4-8 (a) and Fig. 4-8 (d). Similarly, in sector III and VI, the switches of phase "leg *B*" are used for bypassing at the end of the switching cycle as shown in Fig. 4-8 (b) and (c). Detailed analysis of the transition from one phase lost operation to normal operation will be discussed in next section.

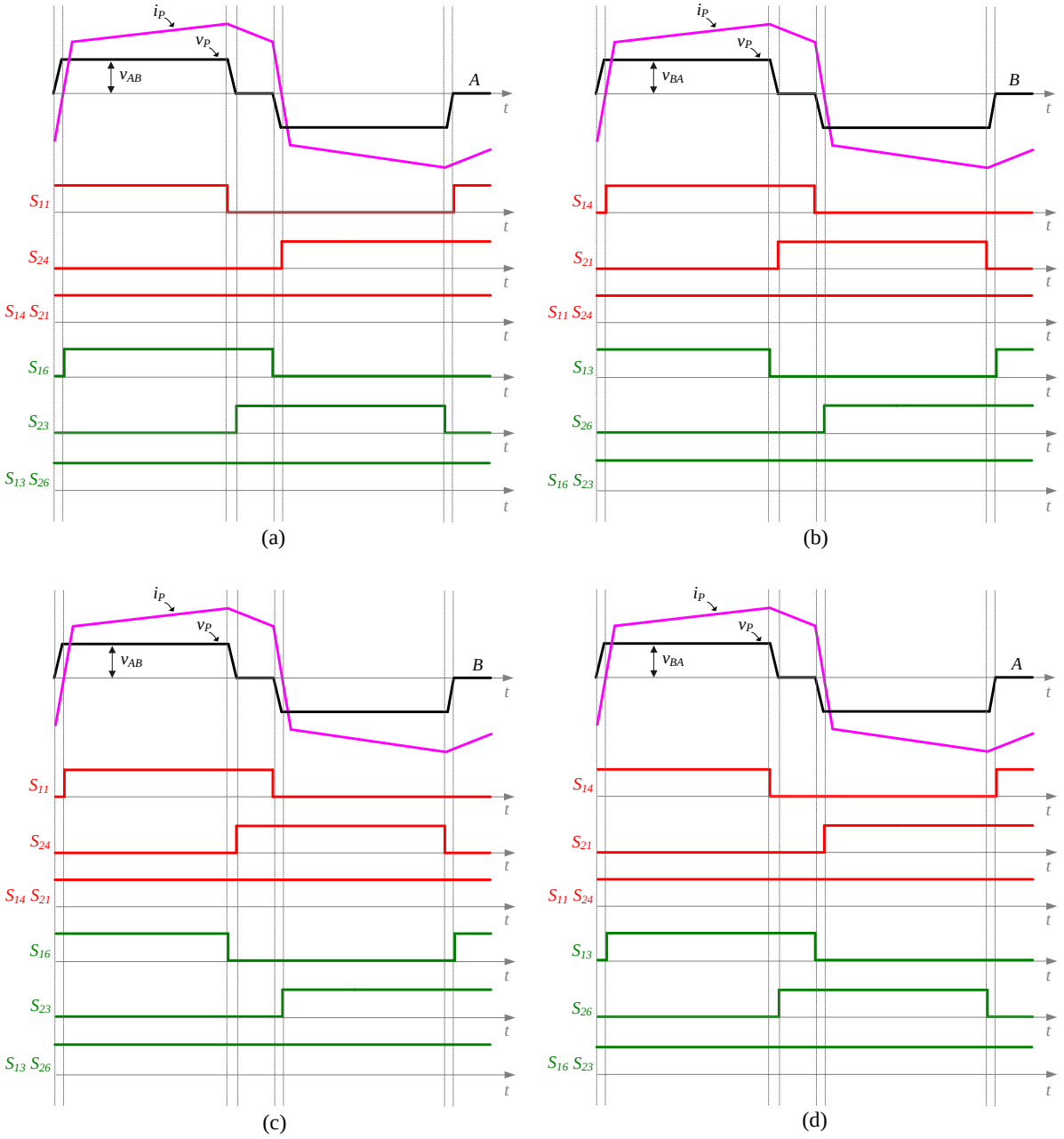


Fig. 4-8 Rectifier operation during one phase lost in interval of: (a) sector I with phase "leg *A*" for bypassing time at the end of the switching cycle, (b) sector III with phase "leg *B*" for bypassing time at the end of the switching cycle, (c) sector VI with phase "leg *B*" for bypassing time at the end of the switching cycle, (d) sector IV with phase "leg *A*" for bypassing time at the end of the switching cycle.

4.3 Analysis of Transition and Commutation Scheme for "Type A" and "Type E"

In this section, analysis of transition and commutation schemes from one phase loss operation to normal operation and vice versa is studied for two PWM schemes "Type A" and eight-segment PWM schemes which are implemented for normal operation. It is important to note that the analysis of transition and commutation scheme from one phase loss operation to normal operation and vice versa are the same among all the eight-segment PWM schemes ("Type E" and improved "Type E").

4.3.1 Analysis of Transition from One Phase Loss to Three-Phase Operation with "Type A" and Vice Versa

As discussed in Chapter 2, two-step commutation with ZVS can be achieved for the transition from zero state to active state and vice versa during normal operation. It is important to note that the corresponding modulation scheme is critical to facilitate this two-step commutation. Due to the inductive current on the transformer primary side, the continuity of the transformer primary current has to be ensured during the commutation. Therefore, the adjacent zero state and active state in the modulation scheme is arranged such that there is a common phase leg is involved in both active state and the zero state. The same criteria can be used to examine the transitions from normal operation to one phase lost operation or from one phase lost operation to normal operation. As shown in Fig. 4-9 (a), in sector I, smooth transition from normal operation to one phase loss operation (shaded area) can be achieved with two-step commutation since phase "leg *A*" is involved in both the zero state prior to the transition and the active state after the transition. Another case as shown in Fig. 4-9 (b), there is no common phase involved in the both states. As a result, the converter primary current cannot be switched from "leg *B*" to "leg *A*" and "leg *C*" directly using two-step commutation, therefore, more commutation steps are required. One of the solutions is to modify the switching sequence of the first cycle for normal operation, as shown in Fig. 4-9 (c), to have the active vector with phase "leg *B*" comes first.

Then smooth transition with two-step commutation can be achieved. However, the transition between the two active vectors in the first half cycle of the normal operation is hard switching and suffers from large diode reverse recovery of MOSFET since the switching pattern becomes low to high (LTH) as discussed in Chapter 2. This may not be a significant problem since this transition only happened once, but this solution will increase the complexity of switching scheme implementation. A better solution, as shown in Fig. 4-9 (d), is to select the switching pattern for one phase loss operation to have the same phase leg for zero state at the end of switching cycle as that for zero state in the normal operation. Then the criteria for two-step commutation are always satisfied.

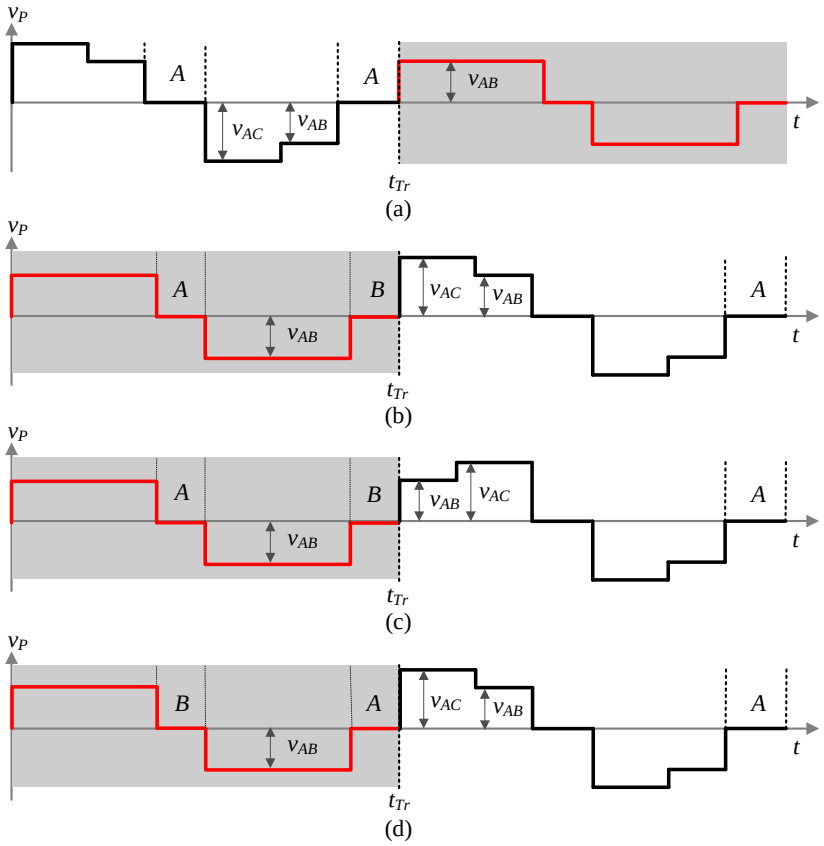


Fig. 4-9 Transformer primary side voltage transition in sector I (b) (shaded area represents one phase loss operation): (a) from normal operation to one phase loss operation, (b) from one phase loss operation to normal operation using phase "leg *B*" for bypassing prior to t_{Tr}, (c) from one phase loss operation to normal operation using phase "leg *B*" for bypassing prior to t_{Tr} and with modified switching sequenc for first cycle of normal operation (LTH), (d) from one phase loss to normal operation using phase "leg *A*" for bypassing prior to t_{Tr}.

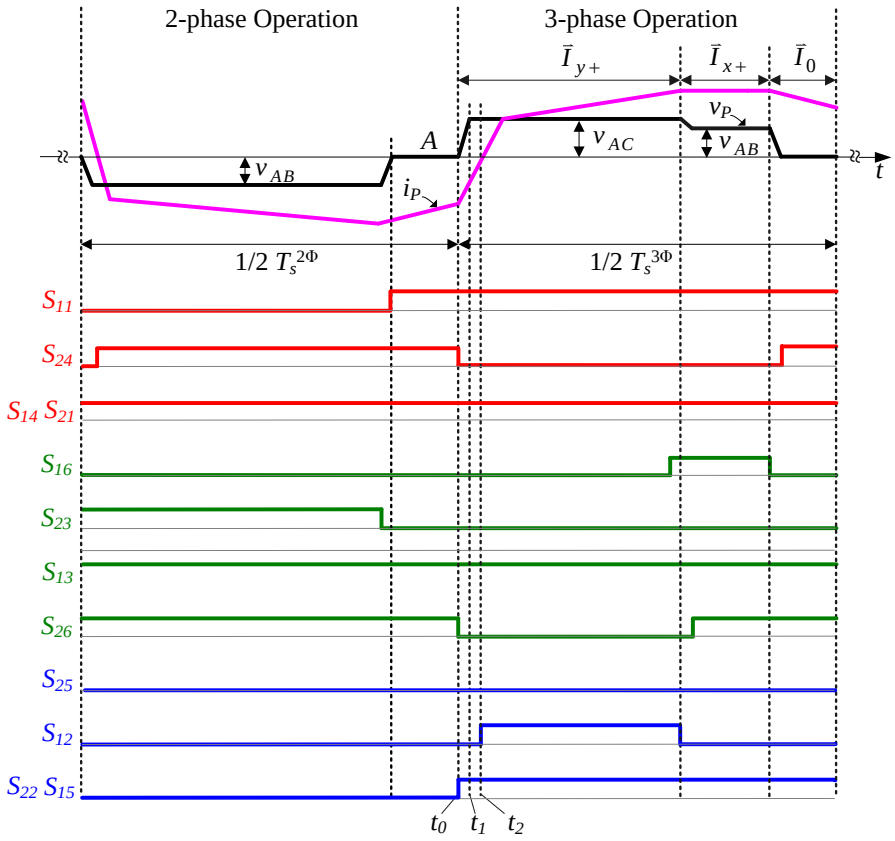


Fig. 4-10 The detail transition from one phase loss to normal operation: with the waveforms of transformer primary side voltage v_P and current i_P and corresponding switch gate signals ($T_s^{2\Phi}$ is period of 2-phase operation and $T_s^{3\Phi}$ period of 3-phase operation).

To further facilitate the explanation of transition from one phase loss to normal operation, the commutation steps are demonstrated in Fig. 4-10 and Fig. 4-11 using an example of the transition from zero state of one phase loss operation (2-phase operation when "phase *C*" is lost) to active vector $\vec{I}_{y+}$ of normal operation (3-phase operation when "phase *C*" is recovered) in sector I (b). Fig. 4-10 shows the PWM gate signals and Fig. 4-11 shows the equivalent circuit at different stages of the transition. At t_0^-, the switching state is the zero state for "phase *C*" loss operation where the phase "leg *A*" is used for by passing (all the switches of phase "leg *A*" are ON) and the current i_P is circulating through the primary side of transformer as shown in Fig. 4-11 (a). The voltage across transformer v_P is zero and voltage potential at the two terminals of the transformer v_1 and v_2 is equal to v_A.

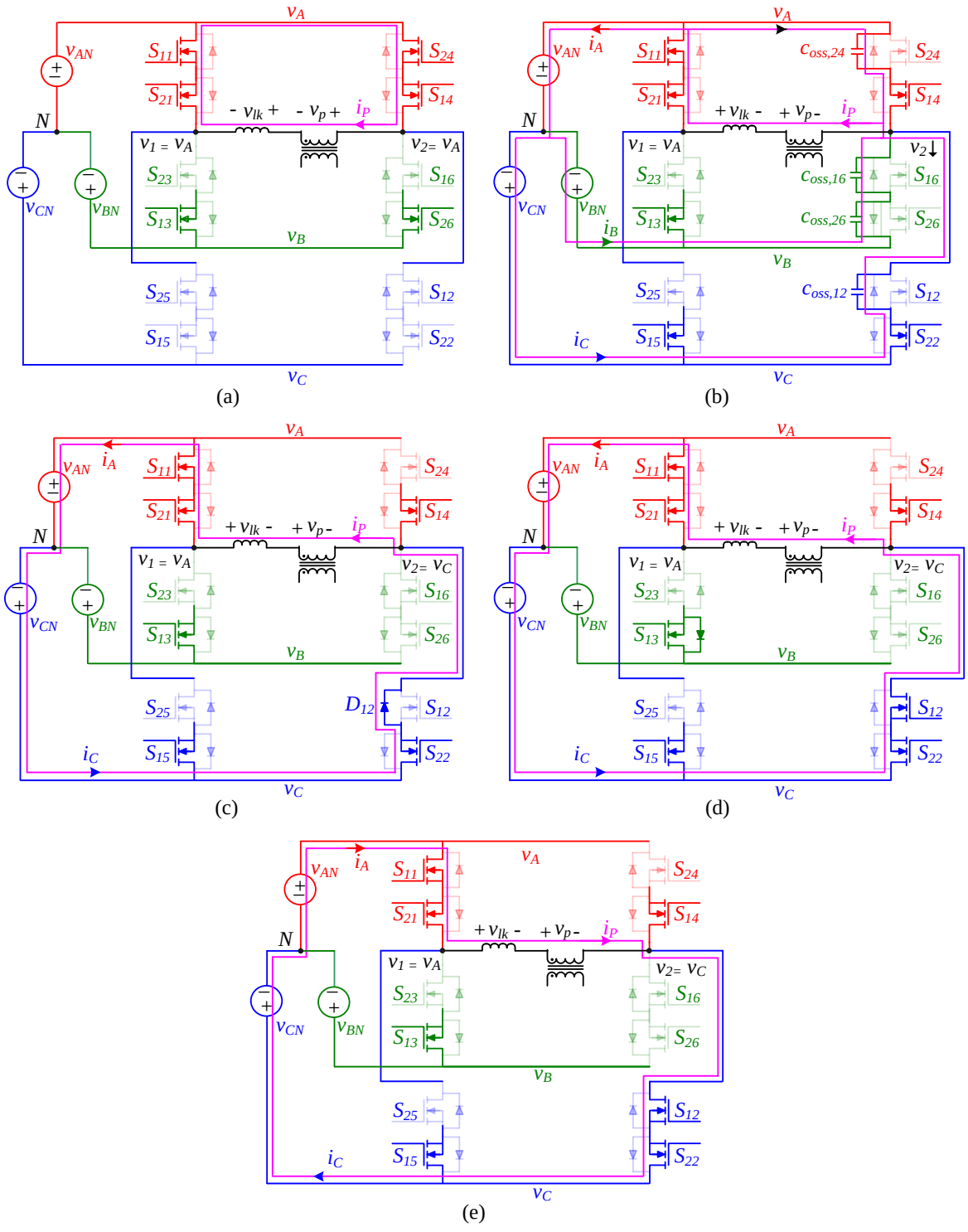


Fig. 4-11 Switching transitions during one phase loss operation to normal operation: (a) at t_0^-, (b) at t_0^+, (c) at t_1, (d) at t_2, (e) at t_2^+.

The first step of the two-step commutation is to turn ON switches S_{15}, S_{22} and turn OFF switches S_{24}, S_{26} at t_0^+. Then the circulating path for current i_P is broken and current i_P charges or discharges the output capacitance of S_{24}, S_{16}, S_{26} and S_{12} as shown in Fig. 4-11 (b). As a result, the voltage v_2 is going down until, at t_1, v_2 reaches to v_C and the body diode D_{12} of switch S_{12} conducts as shown in Fig. 4-11 (c).

During this commutation step, the switches S_{15}, S_{22} are turned ON at zero voltage switching (ZVS) condition for synchronous rectification since v_C has the lowest potential and their body diodes are forward biased. Switch S_{26} is turned OFF at zero current and the turn-OFF of S_{24} is hard switch. The second step of the two-step commutation happens at t_2, where S_{12} is turned on under ZVS condition before i_P change the direction as shown in Fig. 4-11 (d). When i_P ramps up to the same value as output inductor current with respect to the primary side, the transition from zero state of one phase loss operation ("phase *C*" loss) to active vector $\vec{I}_{y+}$ of normal operation is completed. Fig. 4-11 (e) shows the equivalent circuit of active vector $\vec{I}_{y+}$ of normal operation. This is a smooth transition with easy implementation since no extra step is needed compared with the commutation during normal operation or during one phase loss operation.

4.3.2 Analysis of Transition from One-Phase Loss to Three-Phase Operation with "Type E" and Vice Versa

In order to facilitate a smooth two-step transition from one phase loss operation to normal operation with "Type E" implementation, a common phase leg is selected which involved in the switching state prior to and after the transition. As shown in Fig. 4-12, the phase "leg *B*" is used for the bypassing interval at the end of each switching cycle when the "phase *C*" is lost or shorted, since the phase "leg *B*" is the common working leg in sector I, III, IV and VI.

Then the transition from the end of the switching cycle of the one phase loss operation to the beginning of the switching cycle of the normal operation is a smooth two-step transition. Fig. 4-13 shows the PWM gate signals and the transition from one phase loss to normal operation in sector III (a). The first step of the two-step commutation is to turn ON switches S_{15}, S_{22} and turn

OFF switches S_{24}, S_{26} at t_0^+. Then the circulating path for current i_P is broken and current i_P charges or discharges the output capacitance of S_{24}, S_{14}, S_{26} and S_{12}. As a result, the voltage across S_{12} starts going down until, at t_1, the body diode D_{12} of switch S_{12} conducts. During this commutation step, the switches S_{15}, S_{22} are turned ON at zero voltage switching (ZVS) condition for synchronous rectification since v_C has the lowest potential and their body diodes are forward biased. Switch S_{24} is turned OFF at zero current. During the second commutation step, S_{12} is turned ON under ZVS condition at t_2 before i_P changes the direction as shown in Fig. 4-13. When i_P ramps up to the same value as output inductor current with respect to the primary side, this transition completes. This is a smooth transition with easy implementation.

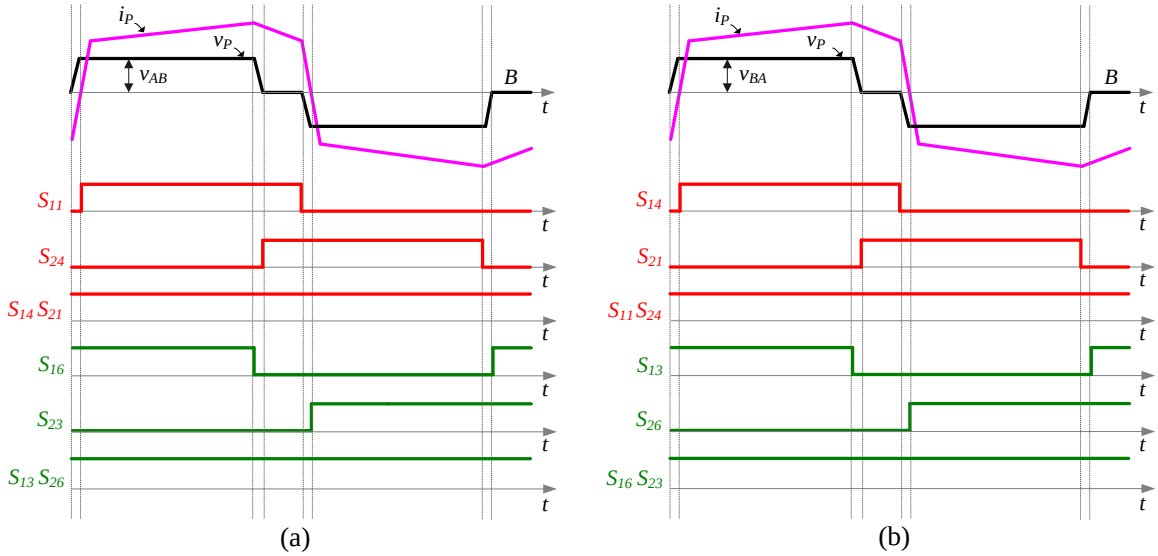


Fig. 4-12 One phase loss operation of rectifier during interval of: (a) sector I and sector VI ($v_A > v_B$) with "phase B" for bypassing time at the end of the switching cycle, (b) sector III and sector IV ($v_B > v_A$) with "phase B" for bypassing time at the end of the switching cycle.

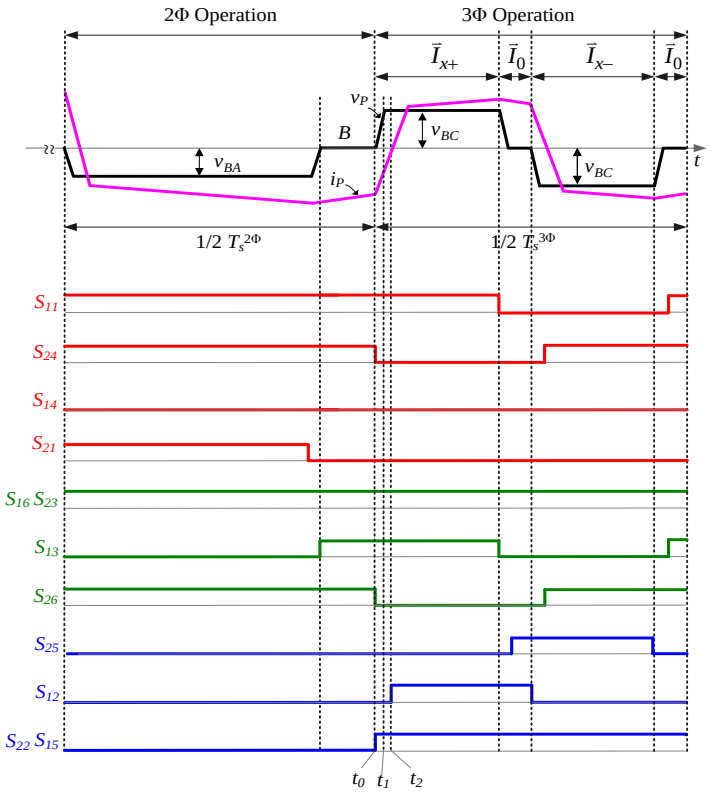
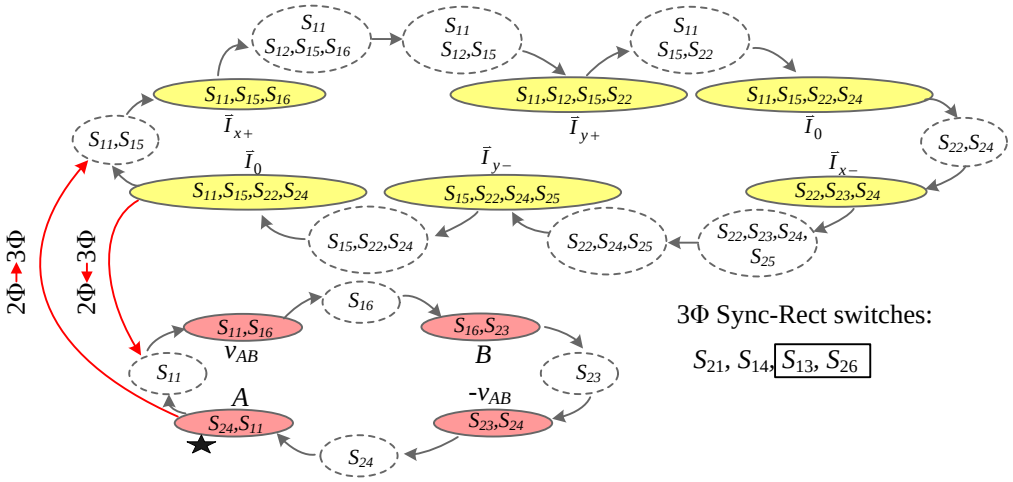


Fig. 4-13 Circuit waveforms: Primary voltage and current and corresponding switch gate signals for the transition from one phase loss to normal operation (with eight-segment PWM scheme) in sector III (a).

4.3.3 Commutation Scheme for One-Phase Loss to Three-Phase Operation with "Type A"

The commutation state machines with the proposed commutation method from one phase loss operation (2-phase operation) to normal operation (3-phase operation) and vice versa are shown in Fig. 4-14. It is important to note that Fig. 4-14 illustrates the commutation state machines in sector I, III, IV and VI except II and V since the "phase *C*" is lost (the converter switches stop gating in sector II and V). The transition states (in dash-line) are added between main states (in shaded color) to achieve zero voltage turn-ON and synchronous rectification operation. Two-step commutation is applied for the normal operation transitions from active vector to zero vector and from zero vector to active vector, while three-step commutation is required for transitions from active vector to another active vector.

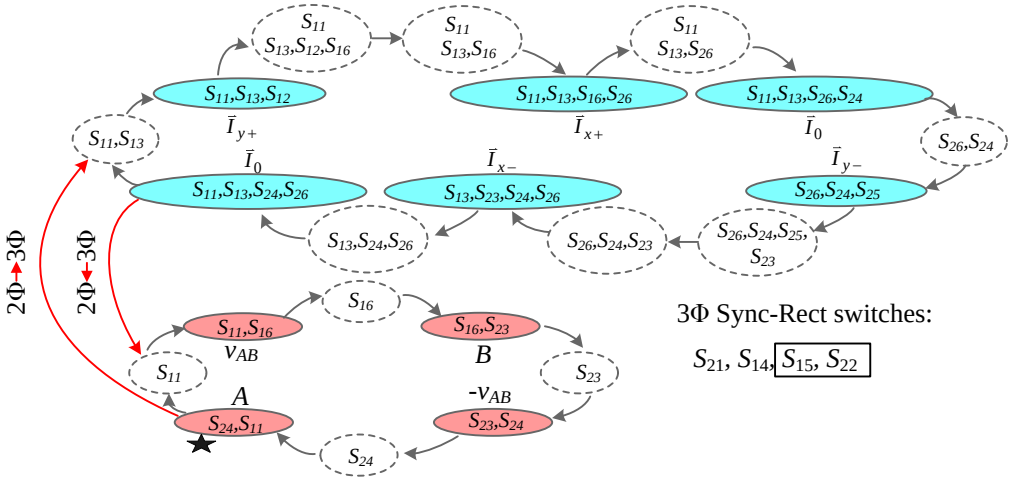
Sector I.(a)



3Φ Sync-Rect switches:

S_{21}, S_{14}, $\boxed{S_{13},\ S_{26}}$

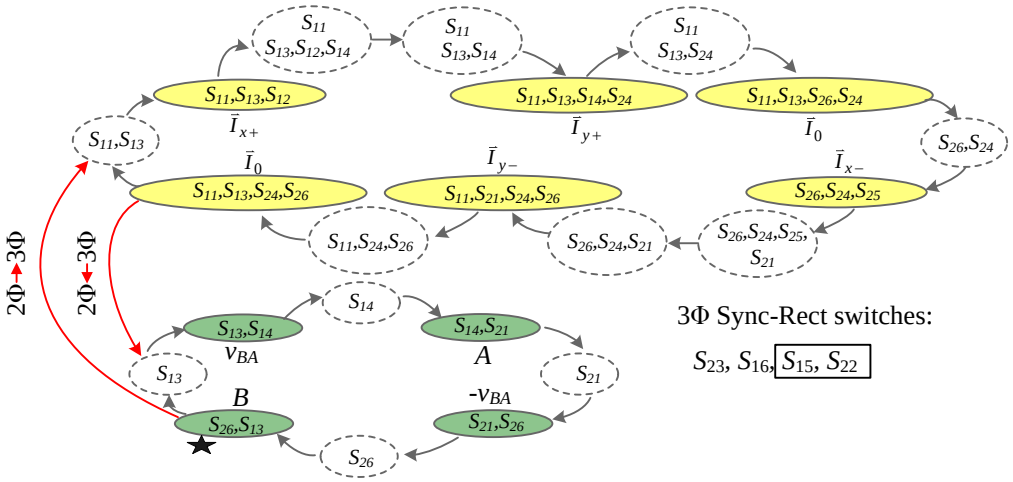
Sector I.(b)



3Φ Sync-Rect switches:

S_{21}, S_{14}, $\boxed{S_{15},\ S_{22}}$

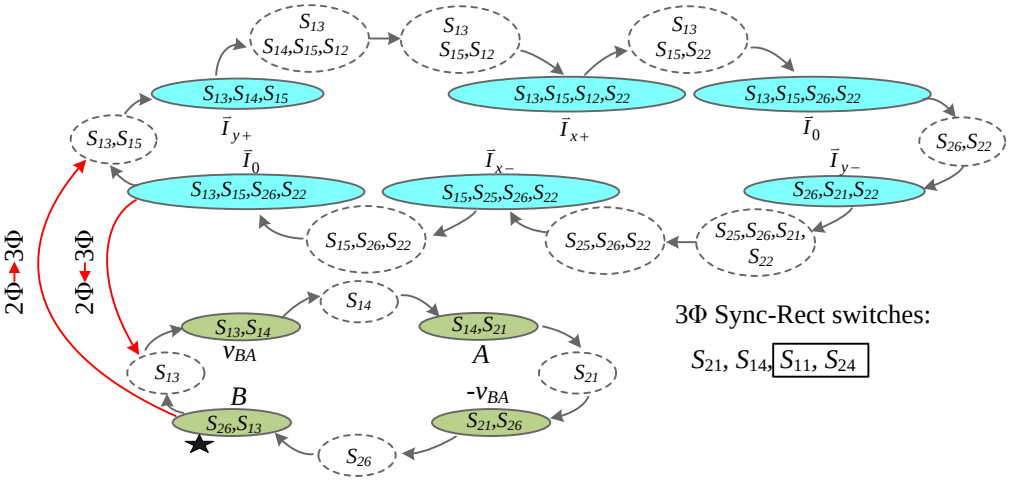
Sector III.(a)



3Φ Sync-Rect switches:

S_{23}, S_{16}, $\boxed{S_{15},\ S_{22}}$

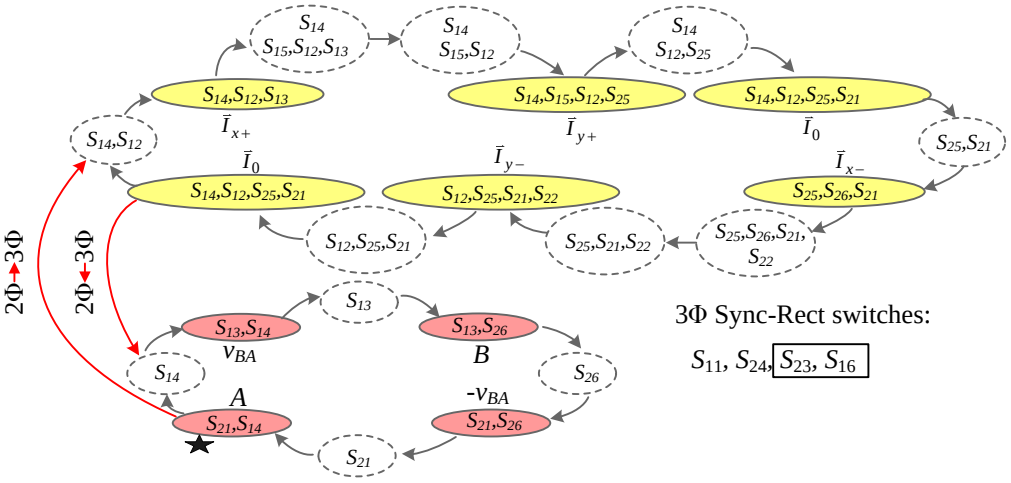
Sector III.(b)



3Φ Sync-Rect switches:

S_{21}, S_{14}, $\boxed{S_{11},\ S_{24}}$

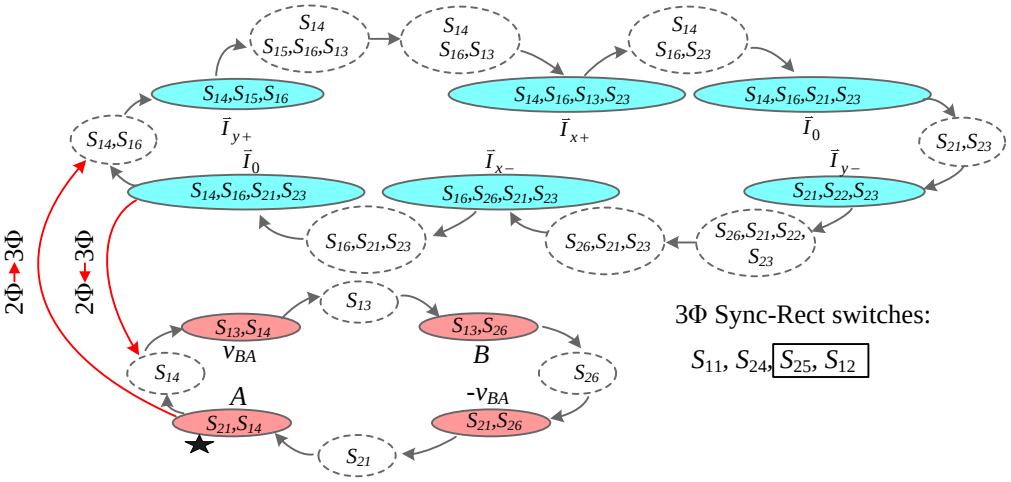
Sector IV.(a)



3Φ Sync-Rect switches:

S_{11}, S_{24}, $\boxed{S_{23},\ S_{16}}$

Sector IV.(b)



3Φ Sync-Rect switches:

S_{11}, S_{24}, $\boxed{S_{25},\ S_{12}}$

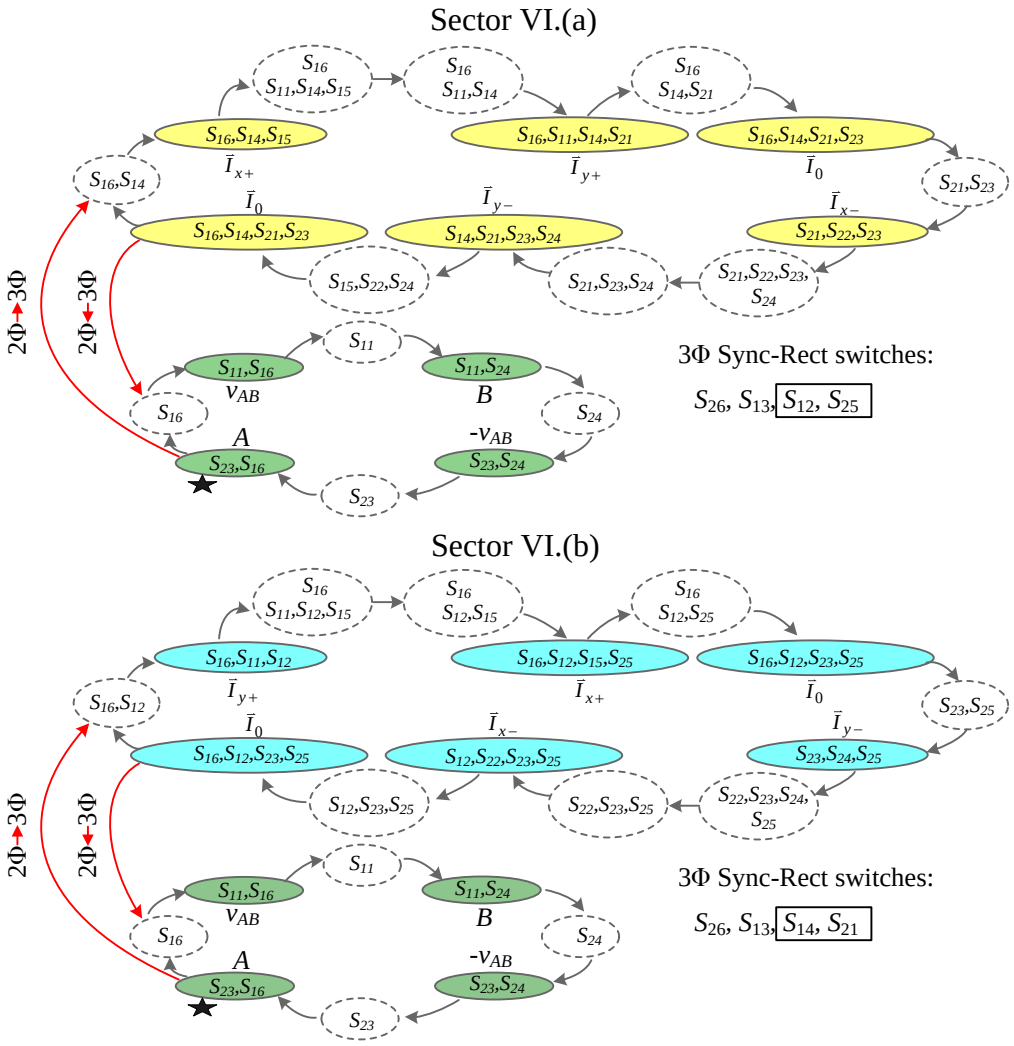
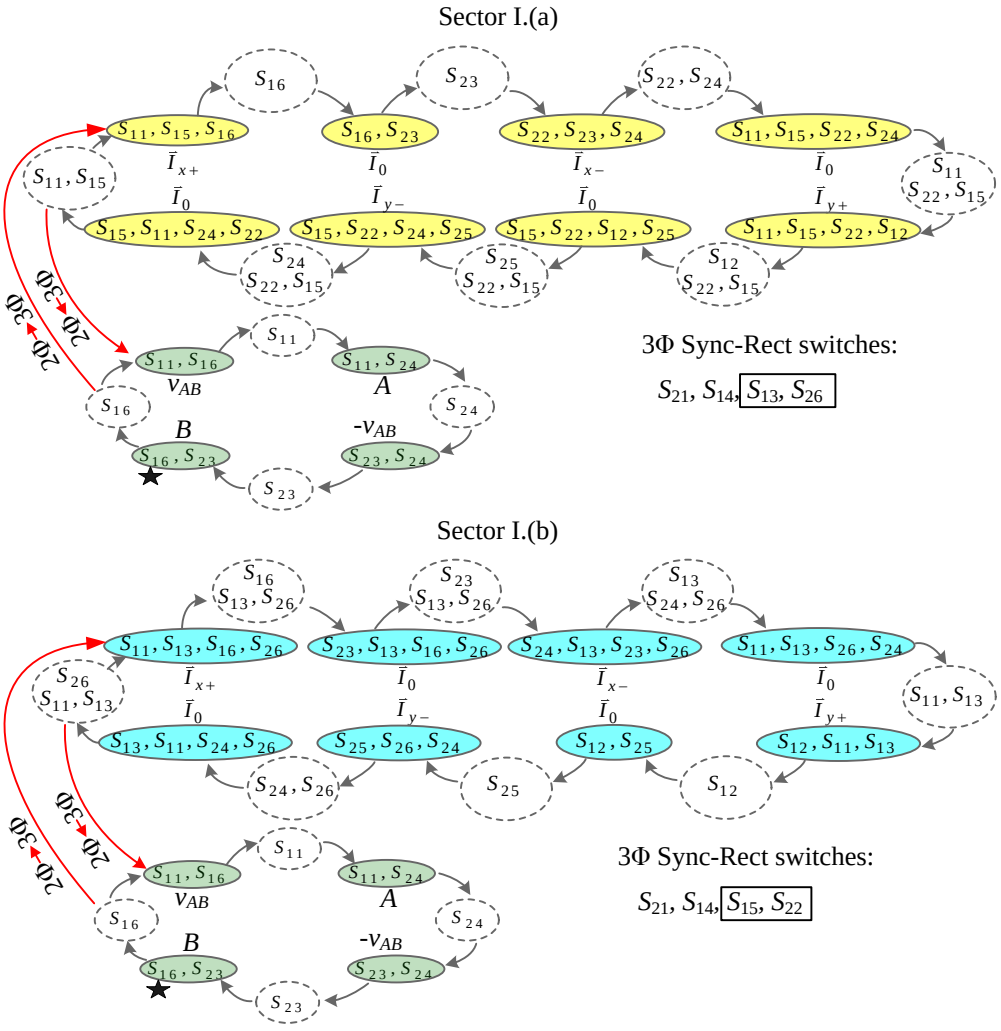


Fig. 4-14 Finite commutation state machine from normal operation (3Φ represents 3-phase operation) to one phase loss (2Φ represents 2-phase operations) and vice versa: two-step commutation realized for one phase loss operation, for the transition from one phase loss to normal operation and vice versa, for normal operation of zero vector to active vector and vice versa, three-step commutation realized for active vector to another active vector in normal operation. (star represents the end of switching cycle of one phase loss operation; Note: the switches in the rectangular boxes are the syncronous rectification switches for 3Φ operation and constraits should be applied on them in the the vicinity of the boundary between part a and part b per Table 2-1.)

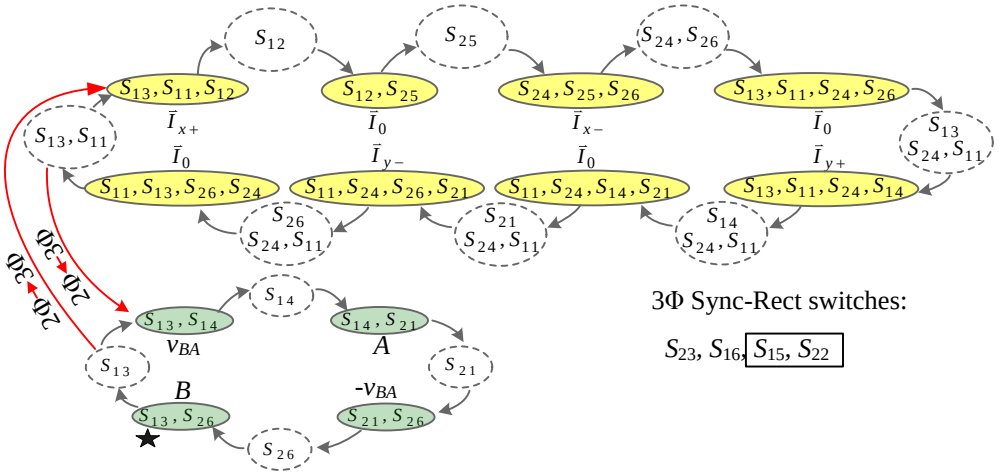
In different sectors, as shown in Fig. 4-14, different commutation state machines are applied to one phase loss operation according to the switching patterns described in Fig. 4-8. Therefore, two-step commutation is realized for transition from normal operation to one phase lost operation and vice versa.

4.3.4 Commutation Scheme for One-Phase Loss to Three-Phase Operation with Improved "Type E"

The finite commutation state machines between normal operation (with "Type E" PWM Scheme) and one phase loss operation with the proposed commutation method are shown in Fig. 4-15. The transition states (dash-circle) are added between main states (in shaded color) to achieve ZVS and synchronous rectification operation. By properly selecting the commutation state machine for one phase loss operation in different sector, two-step commutation with ZVS turn-ON is achieved for both transitions from normal operation to one phase loss operation and vice versa.



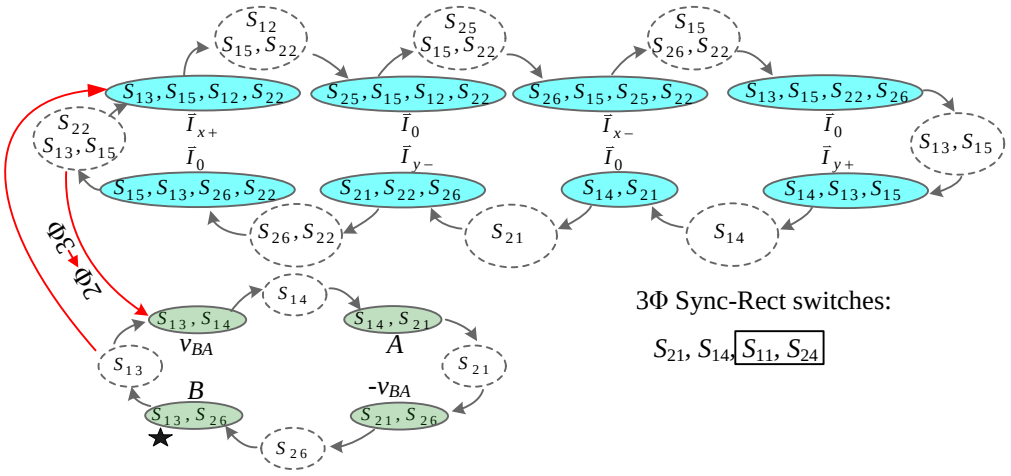
Sector III.(a)



3Φ Sync-Rect switches:

S_{23}, S_{16}, $\boxed{S_{15}, S_{22}}$

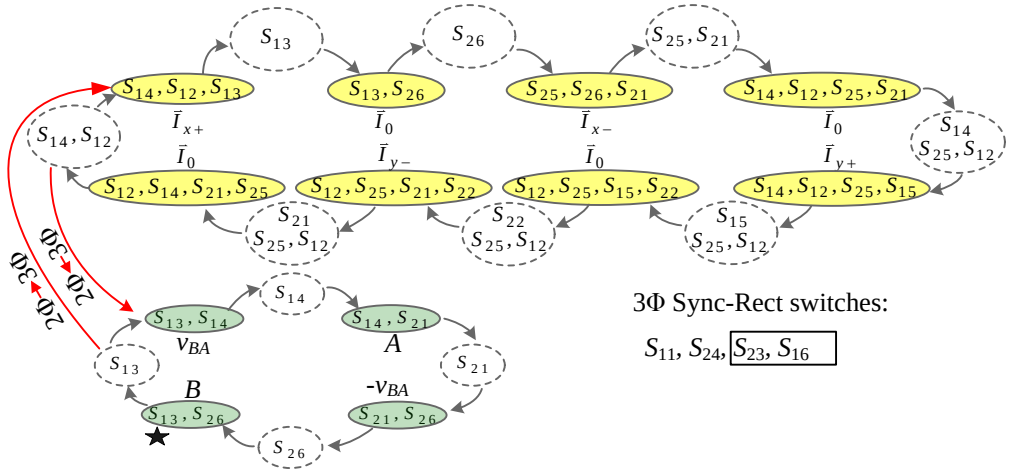
Sector III.(b)



3Φ Sync-Rect switches:

S_{21}, S_{14}, $\boxed{S_{11}, S_{24}}$

Sector IV.(a)



3Φ Sync-Rect switches:

S_{11}, S_{24}, $\boxed{S_{23}, S_{16}}$

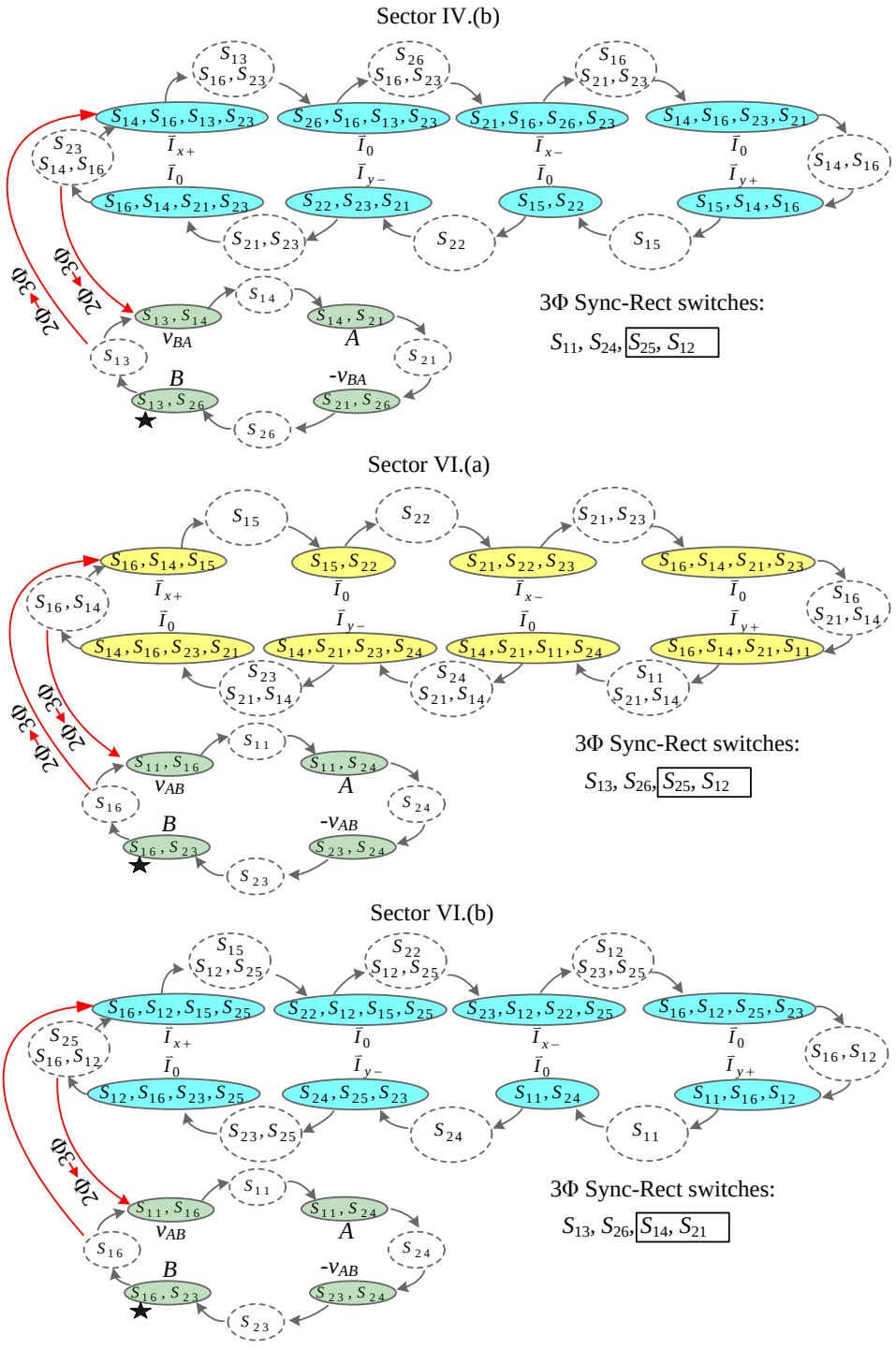


Fig. 4-15 Commutation state machine for normal operation (3Φ) and one phase loss (2Φ): two-step commutation realized for one phase loss operation, normal operation, transition from one phase loss to normal operation and from normal operation to one phase loss operation. (Note: star represents the end of switching cycle of one phase loss operation. Note: the switches in the rectangular boxes are the syncronous rectification switches for 3Φ operation and constraits should be applied on them in the the vicinity of the boundary between part a and part b per Table 2-1.)

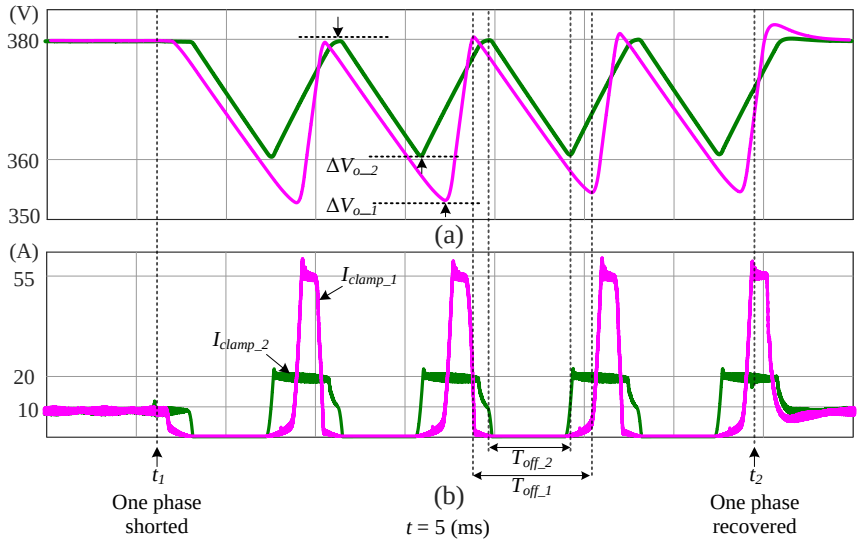


Fig. 4-16 Comparison of output voltage drop ΔV_o for case 1) at m_a = 0.8 and case 2) at m_a = 0.9 with f_{grid} = 60 Hz.

4.4 Simulation Results

To verify the analysis of one phase loss operation of the rectifier, a simulation model is built and tested at two-third of rated power. In the simulation, the output voltage drop of the rectifier and the required upper limit of the average output inductor current for one phase loss operation is studied for two cases: "case 1" applying three-phase (normal) PWM scheme such as "Type A" to one phase loss operation and "case 2" with desired PWM scheme proposed for one phase loss operation. The output storage energy C_o = 2 mF is selected based on the analysis provided earlier in this chapter. As discussed earlier (shown in Fig. 4-5 and Fig. 4-6), the worst case (maximum voltage drop ΔV_o and current clamp I_{clamp}) for ΔV_o and I_{clamp} happened at the highest m_a. Therefore, m_a = 0.9 is chosen for "case 2" in the simulation here. However, for "case 1", the converter cannot regulate the output voltage even with considerably large I_{clamp} when m_a is greater than 0.8. Therefore, m_a = 0.8 is chosen for "case 1" in the simulation. Fig. 4-17 shows the output voltage drops (ΔV_{o_1} and ΔV_{o_2}) and the output inductor current clamp value (I_{clamp1} and I_{clamp2}) for "case 1" and "case 2" at f_{grid} = 60 Hz.

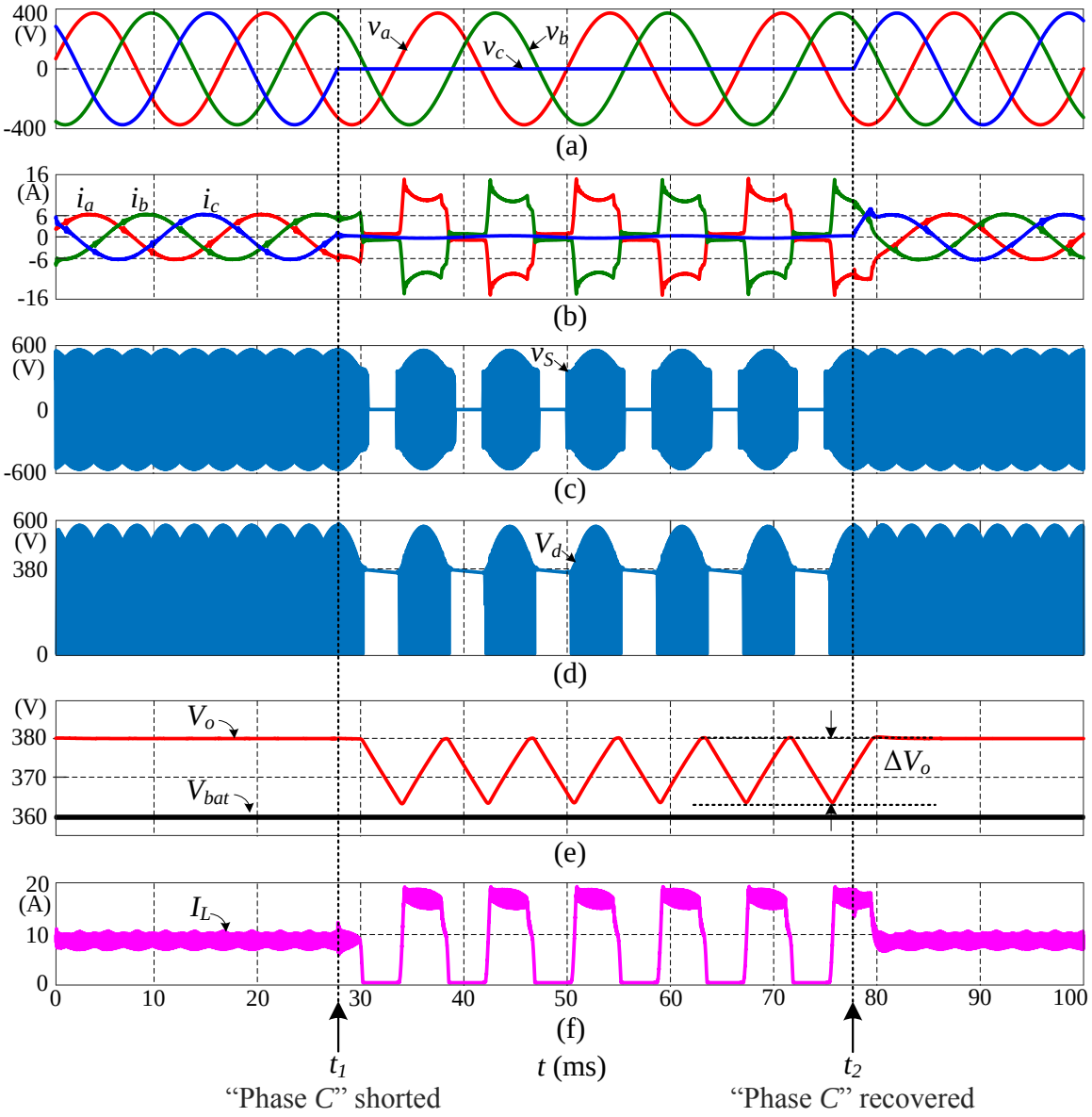


Fig. 4-17 Simulated waveforms for $2/3P_{O\_max}$, v_{LL} = 480V and m_a = 0.75 when "phase C" is shorted at t_1 and recovered at t_2: (a) input phase voltages, (b) input phase currents, (c) transformer secondary voltage, (d) output of bridge rectifier, (e) output voltage and battery voltage set point , (f) output inductor current.

The output inductor current clamp, I_{clamp_1} is significantly large with "case 1", which results in large current stress on the main components of converter and makes the converter operating in one phase loss condition not feasible. With the PWM scheme in "case 2" the output voltage drop is lower and the output inductor current is significantly smaller. The over current ratio (I_{clamp_2} /

I_{rated}) for case 2 is less than 1.5 which is normally acceptable in the real design. Fig. 4-17 shows the operation of one phase loss with proposed PWM for one phase loss at m_a = 0.75. The upper limit of the average output inductor current, I_{clamp} in one phase loss operation is set at 16 A (1.22 I_{rated}) which is higher than the minimum required inductor current at m_a = 0.75 as described in (4-16). The simulation result in here verifies the proposed PWM scheme derived for one phase loss operation and the analysis provided in the above. As shown in Fig. 4-17, the "phase *C*" is shorted at t_1 and recovered at t_2. The output voltage during one phase loss operation is above the battery set point to avoid the battery engagement during one phase lost.

4.4.1 Discussion of Output Voltage Regulation during One Phase Loss Operation with Different m_a

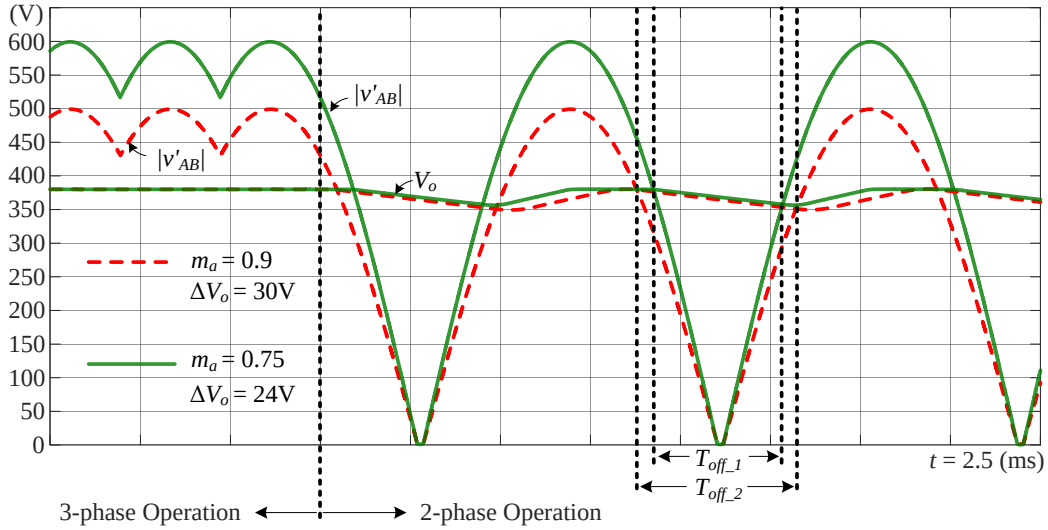


Fig. 4-18 Comparison of output voltage drop ΔV_o for m_a = 0.75 and m_a = 0.9 with f_{grid} = 60 Hz.

Simulation result with the proposed PWM in Fig. 4-18 shows the output voltage, V_o and the absolute value of v_{AB} with respect to the secondary side $|v'_{AB}|$ of the rectifier during normal operation and one phase loss operation with different m_a. The output voltage drop ΔV_o is larger when the rectifier operates at higher m_a, due to the longer off time during which the output voltage only sustains by the output capacitor. As shown in Fig. 4-18, T_{off_2} associated with the

case of m_a = 0.9 is longer than T_{off_1} associated with the case of m_a = 0.75 which results in relatively larger ΔV_o.

4.5 Experimental Verification

The experimental prototype with 380 V output is setup at 5 kW rated power in three-phase operation and in one phase loss operation the output power is reduced to 3.3 kW (two-third of rated output power). Detail experimental system parameters are the same as Table. 3-2 except the output capacitor C_o is increased to 2 mF.

4.5.1 Experimental Waveforms for One Phase Loss Operation with "Type A"

The experimental waveforms in Fig. 4-19 illustrate the operation when one phase is shorted and then recovered. As shown from transformer primary side voltage in Fig. 4-19 (c) and (e), a smooth transition occurs at t_2 and t_4 when "phase *C*" is shorted and then recovered. As shown in Fig. 4-20 (b), the upper limit of the average output inductor current, I_{clamp} in one phase loss operation (2-phase operation) is 16A which is consistent with the analysis in this chapter and the simulation results in Fig. 4-17 (f). The output voltage is regulated tightly at 380 V in normal operation and ΔV_o is less than 5% of nominal output voltage in one phase loss operation as shown in Fig. 4-19 (f) and (g) respectively. The large inrush current seen in grid currents in Fig. 4-20 (a) is due to the input EMI capacitors. Fig. 4-21 shows the experimental spectrums of the input phase currents for one phase loss operation at 3.3 kW output power. The total harmonic distortion of the input phase currents is around 1.6% for normal operation and 39.2% for one phase loss operation.

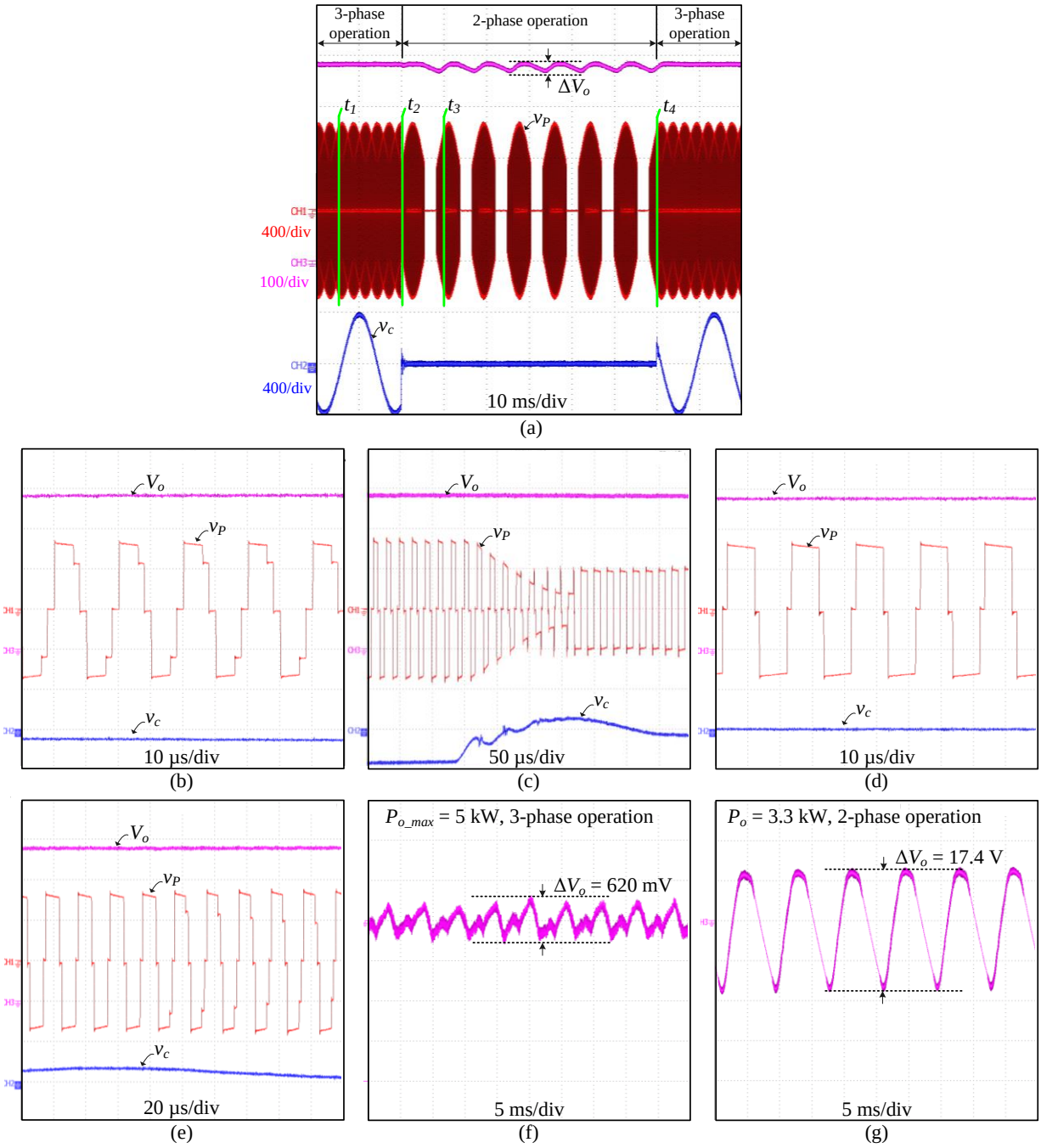


Fig. 4-19 Experimental waveforms for $2/3P_{o\_max}$ = 3.3 kW, v_{LL} = 480 V, f_{grid} = 60 Hz: (a) voltage waveforms of v_P, v_{LL}, V_o, (b) at t_1, normal operation (3-phase operation), (c) at t_2, instant "phase C" is shorted, (d) at t_3, one phase loss operation (2-phase operation), (e) at t_4, instant "phase C" recovered, (f) ac ripple of voltage V_o in normal operation at maximum output power P_{o_max} = 5 kW , (g) ac ripple of voltage V_o in one phase loss operation.

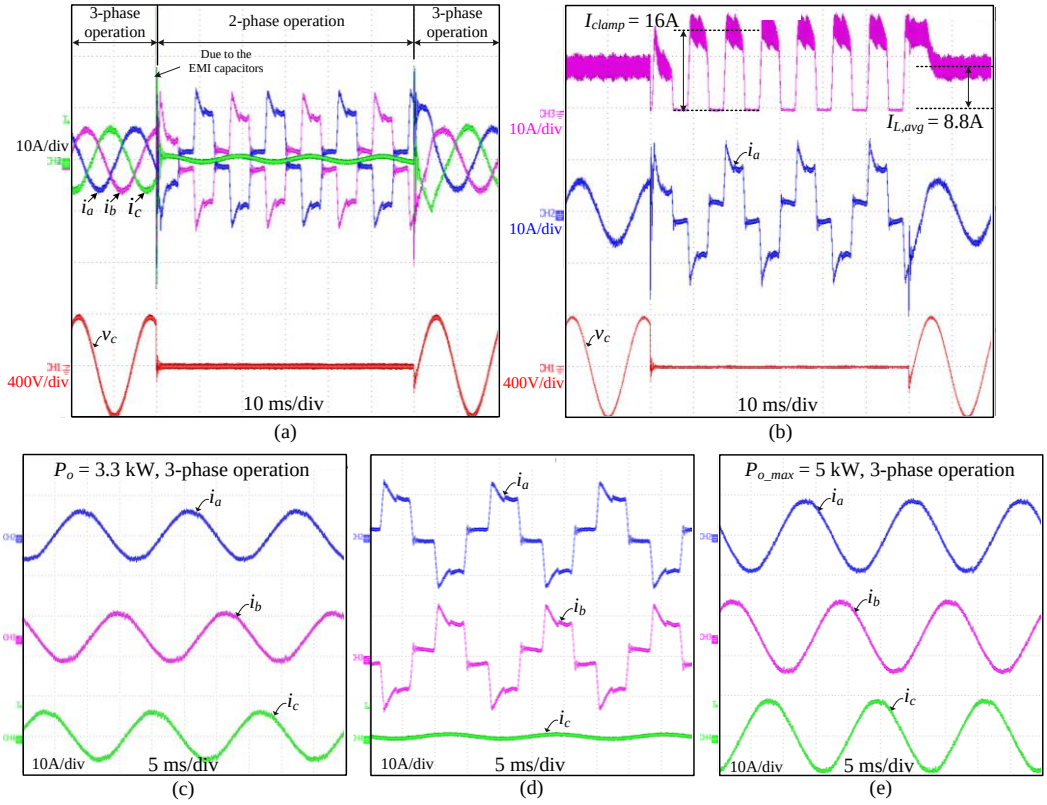


Fig. 4-20 Experimental waveforms for v_{LL} = 480 V, f_{grid} = 60 Hz, m_a = 0.75 at at $2/3P_{o\_max}$ = 3.3 kW: (a) input phase currents and voltage waveforms of i_a, i_b, i_c and v_c, (b) output inductor current I_L and input phase currents and voltage, (c) normal operation (3-phase operation) (d) one phase loss operation (2-phase operation), (e) normal operation at maximum output power P_{o_max} = 5 kW.

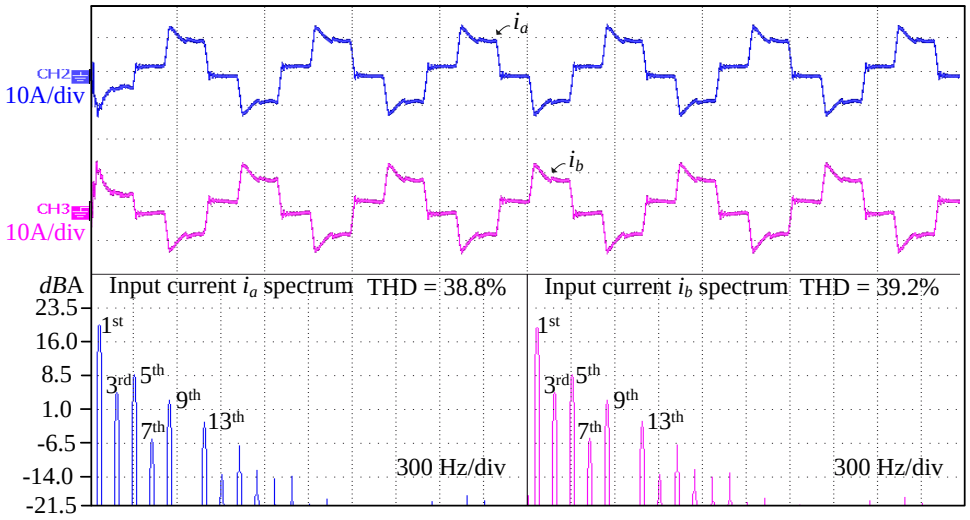


Fig. 4-21 Experimental spectrums of input phase currents of i_a and i_b at $2/3P_{o\_max}$ = 3.3 kW.

4.5.2 Converter MOSFET Switching Dynamics Behavior during One Phase Loss Operation

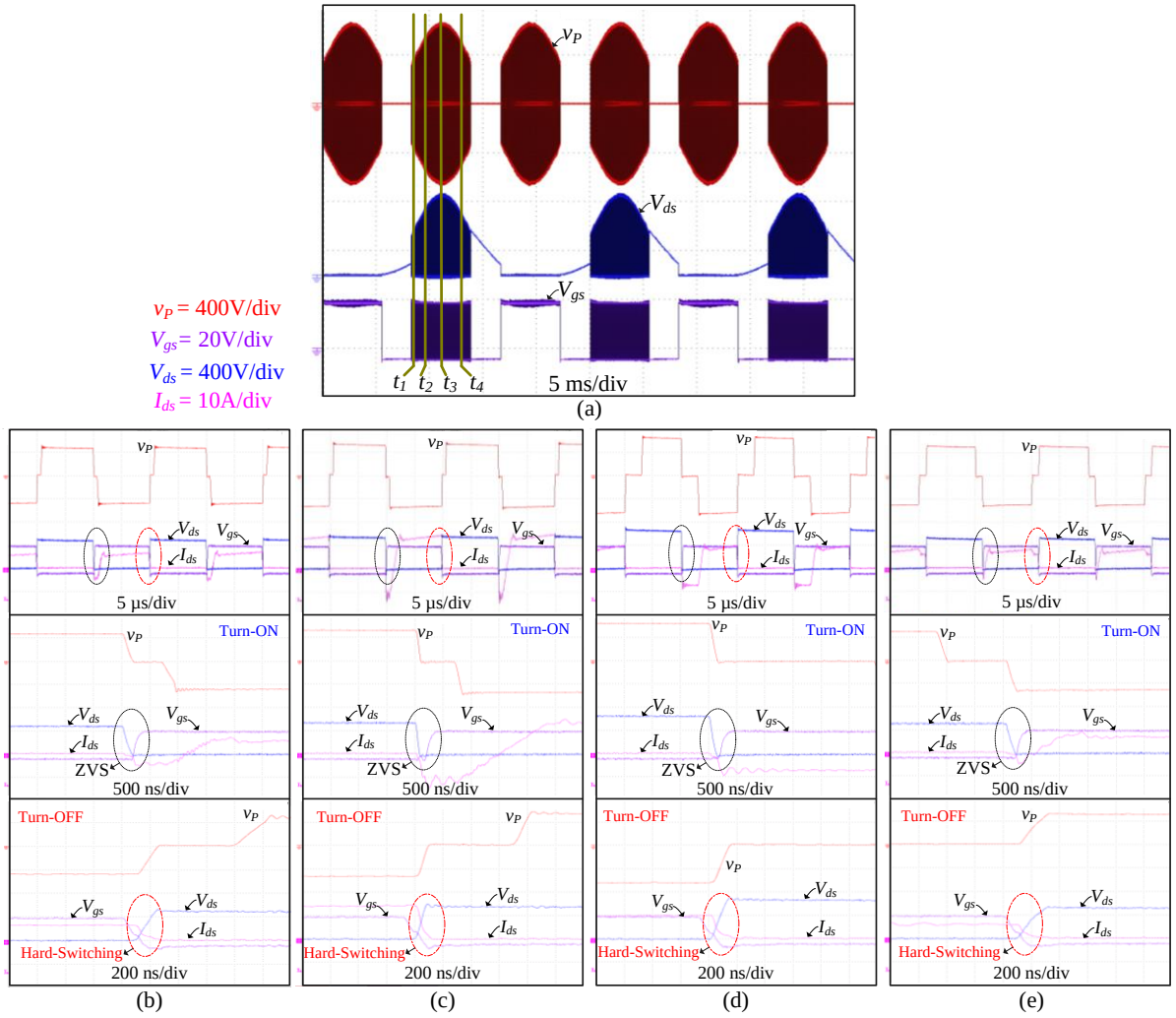


Fig. 4-22 Experimental waveforms for converter MOSFETs switching behavior (turn-ON and turn-OFF actions) during one phase loss operation: (a) voltage waveforms of v_P, V_{ds} and V_{gs}, (b) at t_1 (c) at t_2, (d) at t_3 and (e) at t_4.

The converter switching behavior (turn-ON and turn-OFF actions) during normal operation is analyzed and verified with experimental results in Chapter 2. Fig. 4-22 shows the converter turn-ON and turn-OFF switching actions during one phase loss operation. One of the MOSFETs that function as an active switch in the converter is selected for demonstrating the turn-ON and turn-

OFF switching transitions at four locations of t_1, t_2, t_3 and t_4 (to show the entire operation mode). As shown in Fig. 4-22 (b)-(e), drain-source voltage V_{ds} of the MOSFET tends to be zero before the gate-to-source voltage V_{gs} of the MOSFET approaches high, which indicates that the body diode is ON before the turn-ON of the switch such that ZVS is realized. As shown in Fig. 4-22, the transformer primary voltage v_P and the drain-source voltage V_{ds} of the MOSFET is clean and no large spike is noticeable since all the turn-ON actions are under ZVS condition. The turn-OFF actions of this MOSFET at t_1, t_2, t_3 and t_4 are all hard switching. However, these turn-OFF actions produce negligible losses since the overlapping of voltage and current is very small during the turn-OFF transition.

4.5.3 Experimental Verification for One Phase Loss Operation with Improved "Type E"

The experimental waveforms in Fig. 4-23 illustrate the operation of the rectifier when one phase is shorted and then recovered. As shown in Fig. 4-23, a smooth transition occurs at two intervals t_2 and t_4 when "phase *C*" is shorted and then recovered. The transformer primary voltage is clean and no large spike is noticeable due to ZVS operation of the MOSFET switches. It should be noted that during normal operation, the improved "Type E" is employed here due to its low output inductor current ripple and better input current THD. The output voltage is tightly regulated at 380 V in normal operation and the output voltage drop ΔV_o is less than 5% of nominal output voltage during one phase lost operation. The total harmonic distortion of the input phase currents is around 1.94% for normal operation and 38.6% for one phase loss operation.

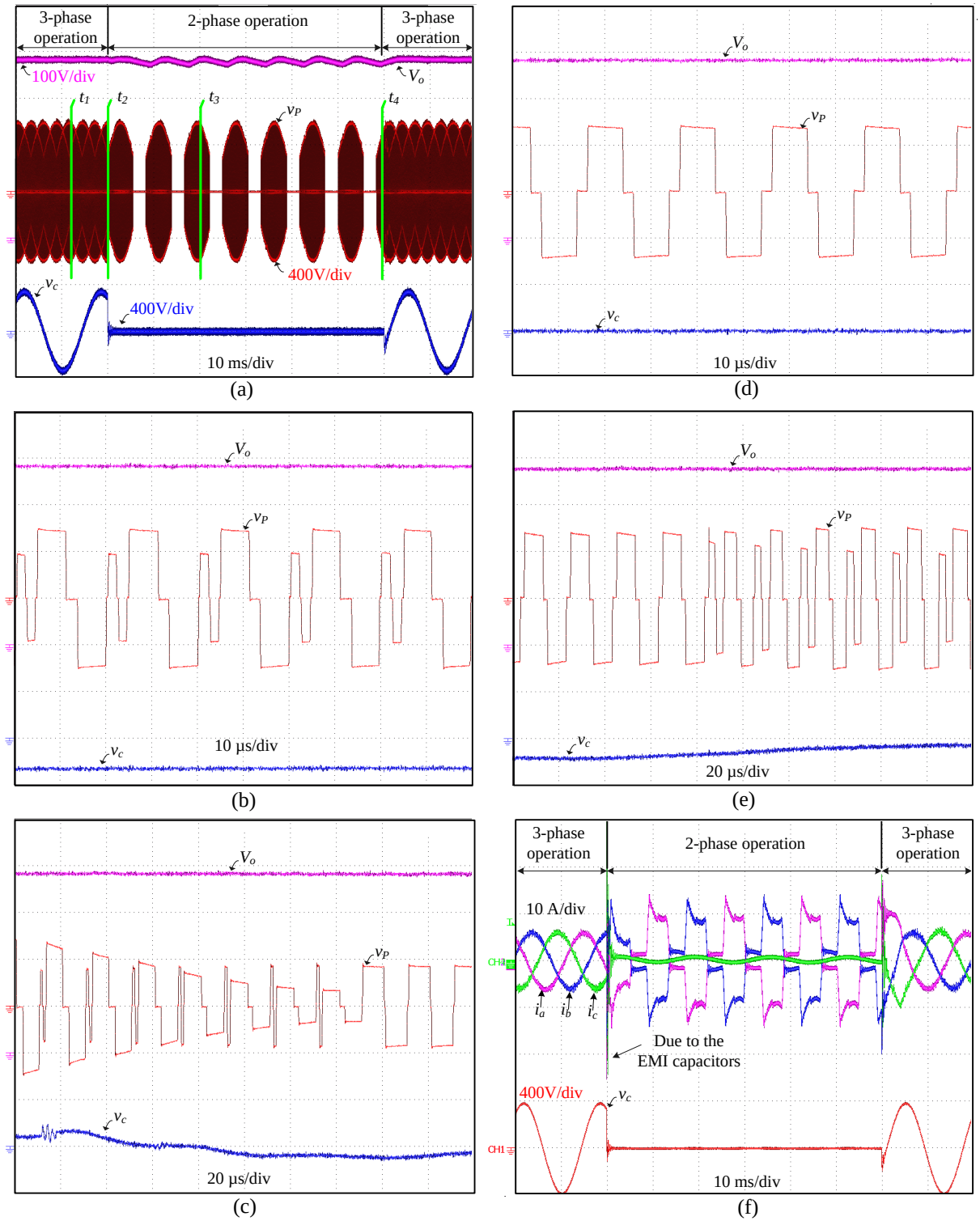


Fig. 4-23 Experimental waveforms at 2/3*Po_max*, v_{LL} = 480 V, f_{grid} = 60 Hz: (a) normal operation (3Φ) to one phase loss operation (2Φ), (b) at t_1, normal operation, (c) at t_2, instant "phase *C*" is shorted, (d) at t_3, one phase loss operation, (e) at t_4, instant "phase *C*" recovered, (f) input phase currents and voltage waveforms of i_a, i_b, i_c and v_c.

4.6 Conclusions

In this chapter, operation of the three-phase isolated Buck matrix-type rectifier under one phase loss condition is described and the limitation of the normal PWM scheme under one phase loss condition is mathematically analyzed. Then new PWM schemes and commutation methods are proposed for six-segment and eight-segment PWM respectively to improve the performance under one phase loss operation. It is shown that the maximum available average voltage envelop on the rectifier side can be achieved with the desired PWM scheme proposed for one phase loss operation so that significantly lower overall current stress on the converter and the output voltage drop can be achieved compared with the case when the normal PWM schemes are applied to one phase loss operation. With the proposed switching schemes and commutation methods, two-step commutation with ZVS turn-ON can be realized during one phase loss operation and during the transitions between normal operation and one phase loss operation. Operation and performance of the converter with the proposed PWMs and commutation methods are verified with simulation and experimental results.

The input current THD obtained during one phase loss operation is relatively high and may not be acceptable for the system that might even run for days. Therefore, how to improve the input current THD during one phase loss operation to resemble performance of single-phase two-stage converter is considered as the most important discussion of the next chapter.

Chapter 5

Isolated Buck Matrix-Type Rectifier with Integrated Boost Output Stage

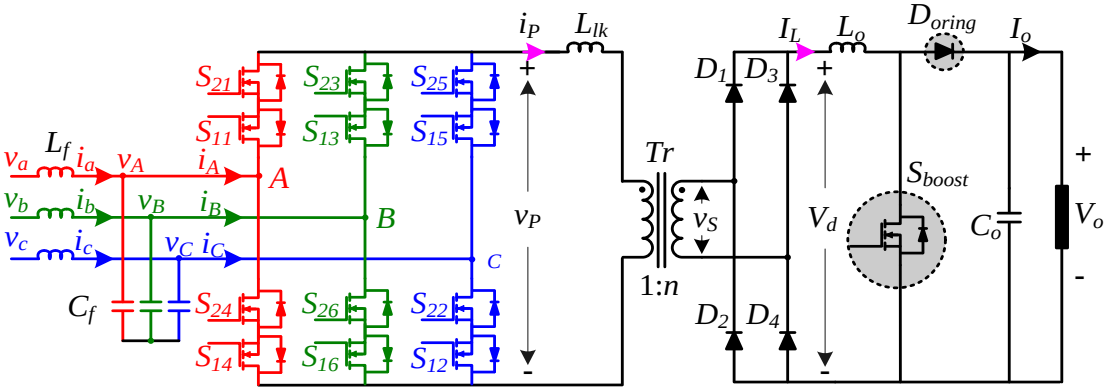


Fig. 5-1 Three-phase isolated buck matrix-type rectifier with a boost switch.

In the previous chapter, a PWM and commutation scheme are proposed for isolated buck matrix-type rectifier to maintain proper operation of the rectifier during one phase loss operation and to provide smooth transitions between the faulty and normal modes. Also, it is mentioned, large output voltage drop and high input current THD are of the major drawbacks of the isolated buck matrix-type rectifier when it operates in faulty mode of one phase loss. In order to overcome these drawbacks, integrating a boost output stage with the isolated buck matrix-type rectifier as shown in Fig. 5-1 is proposed in this chapter. Note, when ORing diode or ORing FETs are employed by integrated boost output stage, a small additional circuitry is required for pre-charging the output capacitor and assuring ORing functionality in the PSU. With integrated boost output stage, the output voltage drop and input current THD for one phase loss operation can be significantly improved compared with pure buck matrix-type rectifier (without boost stage). The rectifier exhibits similar performance for input currents THD and output voltage

regulation as single phase two-stage converter. The basic principle of operation and the modulation method which is used to control the three-phase isolated buck matrix-type rectifier with the proposed integrated boost output stage is described. The output voltage and input current THD performance of the converter during one phase loss operation is evaluated and verified by the simulations and experiments on a 5 kW prototype.

5.1 Analysis of Operation of the Rectifier during One Phase Loss (opened or shorted)

In case of one phase opened, the connection between the source and the converter of one of the phase is open and the leg of that phase is completely excluded from the operation of the converter since no power can be delivered from that phase. While in case of one phase shorted, the faulty phase at the rectifier side is shorted to the neutral. The line to line voltage between the faulty phase and the other phases become phase voltage. In this case the leg of the shorted phase can still be involved in operation if the converter has boost capability. Therefore, operation principle and control schemes for one phase opened and one phase shorted of the converter with integrated boost output stage will be discussed separately in the following sections. The main control objectives of the converter with boost stage are to regulate the output voltage and maintain good input current THD. However, during one phase loss operation, compromise has to be made between these two control objectives depending on the application. Therefore, different control schemes to achieve different control objectives for both one phase open and one phase shorted conditions will be discussed in the following sections.

5.1.1 Analysis Of Operation to Achieve Miminum Ouput Voltage Drop during One Phase Opened Fault

The equivalent circuit of the primary side during one phase opened operation is same as that described in the previous chapter, where the phase leg of the lost phase is excluded. The boost switch is activated when the input voltage is lower than the minimum value required to regulate the output voltage by the primary switches only. It should be noted that for simplicity the

analysis of converter in this chapter is based on the assumption that the duty cycle loss of the buck rectifier is very small and can be neglected unless it is specified. The circuit principal waveforms within one gird side cycle with excessively increased switching period of PWM when the boost switch is enabled during one phase loss operation can be observed in Fig. 5-2.

During interval (highlighted) where $|v'_{AB}|$ is lower than V_o, the converter operates in Buck+Boost mode in which the boost switch is enabled to regulate V_o and the primary of the matrix converter is operating at its maximum duty cycle. Therefore, the intervals of T_{off} are greatly reduced which results in smaller output voltage drop ΔV_o compared with the pure buck mode operation discussed in previous chapter. However, when $|v'_{AB}|$ is very low ($|v'_{AB}| < V_{lim}$), the output voltage V_o starts losing regulation since the output inductor current is clamped at the upper limit by the current controller. As shown in Fig. 5-2 (d), as $|v'_{AB}|$ goes down, the output inductor current rises until it reaches to the maximum value of I_{clamp} when $|v'_{AB}|$ reaches V_{lim}. If $|v'_{AB}|$ further goes down, very limited energy can be delivered to the secondary side due to the small value of $|v'_{AB}|$ and the substantially reduced effective duty cycle of V_d since the duty-cycle loss cannot be neglected when $|v'_{AB}|$ becomes very low. Therefore, the primary switches and the boost switch stop switching during T_{off} intervals to reduce the associated switching loss. The limit of maximum output inductor current I_{clamp} expressed in (5-1) can be applied to both buck and buck+boost mode control since the same inductor is involved in both operation mode

$$I_{clamp} = kI_{rated} \tag{5-1}$$

where k is the over current racial and I_{rated} is the inductor current in nominal condition.

Assuming the duty-cycle loss of the buck converter is very small, V_{lim} at $I_o = 2/3 I_{rated}$ (two-third of nominal power) can be derived as

$$V_{lim} = \frac{\frac{2}{3} I_{rated}}{I_{clamp}} V_o \ . \tag{5-2}$$

By substituting $V_o = \frac{3}{2} n V_m m_a$ and I_{clamp} with (5-1) into (5-2), it results in

$$V_{lim} = \frac{1}{k} n V_m m_a \,. \tag{5-3}$$

Since T_{off} is the interval when $|v'_{AB}| < V_{lim}$, T_{off} can be derived by combining (4-2) and (5-3)

$$T_{off} = \frac{\sin^{-1}(\frac{1}{\sqrt{3}k} m_a)}{\pi f_{grid}}. \tag{5-4}$$

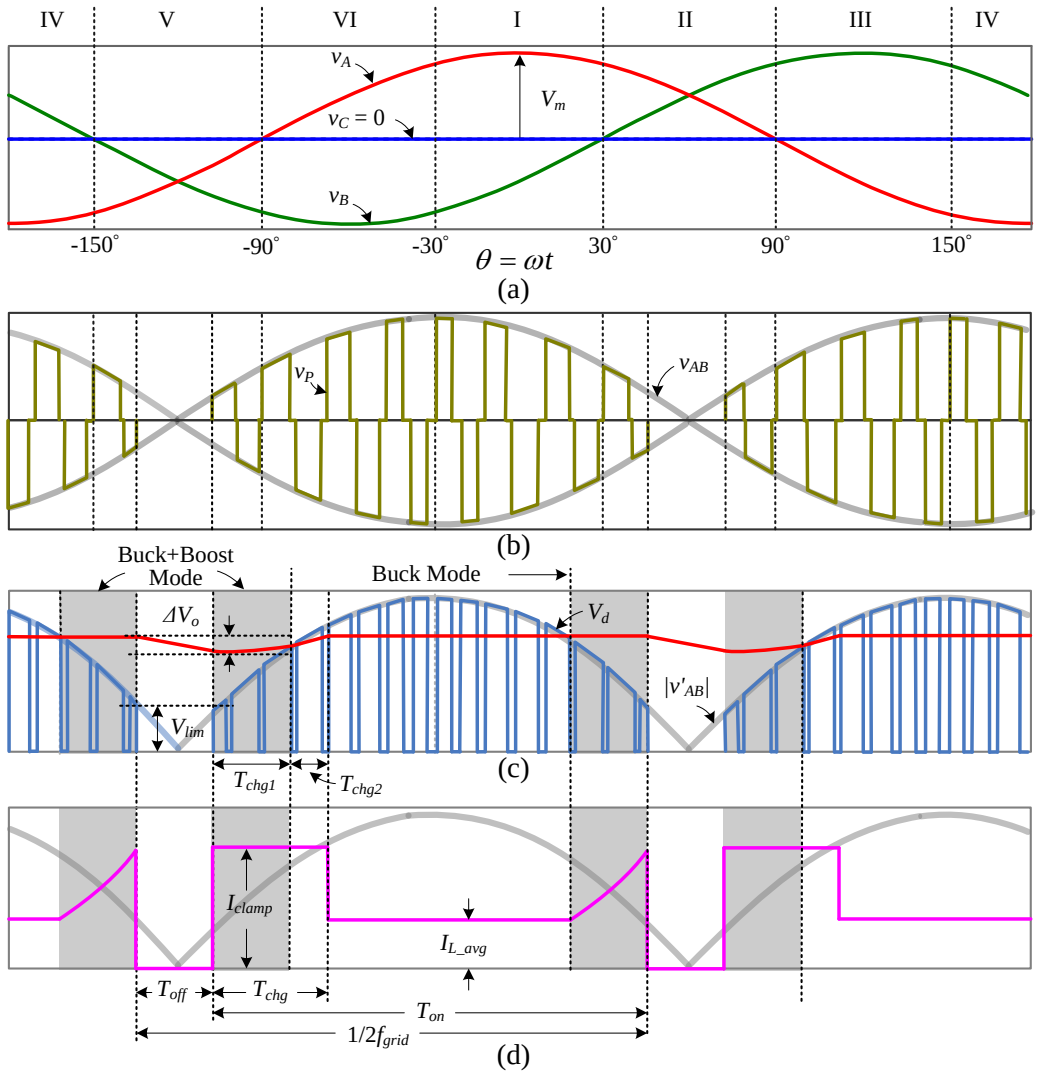


Fig. 5-2 Voltage Operation waveforms for three-phase buck matrix-type rectifier with integrated boost output stage to achieve minimum output voltage drop during one phase opened.

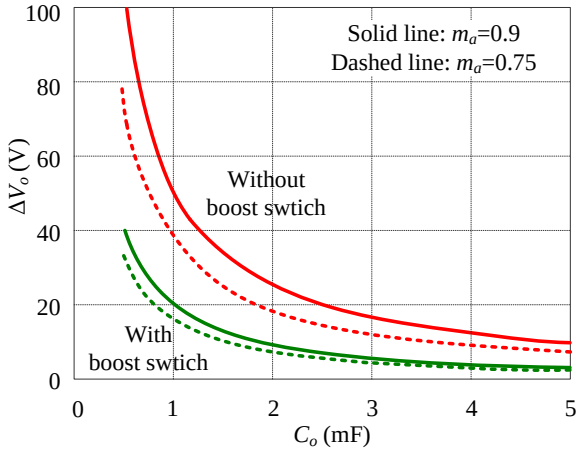


Fig. 5-3 The output voltage drop ΔVo versus Co in one phase loss operation with and without boost switch at Io = 2/3Irated, fgrid = 50 Hz, k = 1.4 with boost switch and k = 1.7 without boost switch.

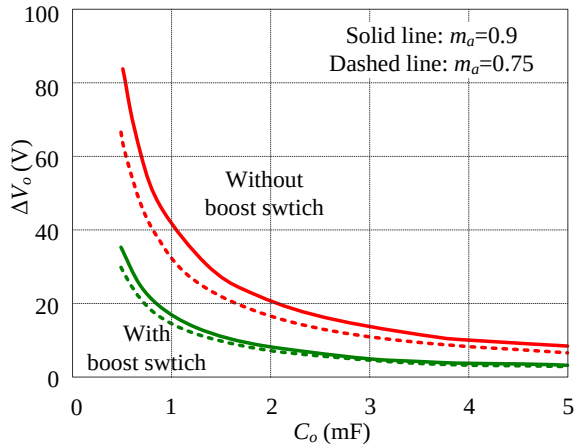


Fig. 5-4 The output voltage drop ΔV_o versus C_o in one phase loss operation with and without boost switch at I_o = 2/3I_{rated}, f_{grid} = 50 Hz, k = 1.4 with boost switch and k = 1.7 without boost switch (pure buck operation).

Neglecting the energy delivered from primary to secondary during T_{off}, the voltage drop ΔV_o with the boost stage activated can be derived by substituting T_{off} with (5-4) into (4-6)

$$\Delta V_o = \frac{I_o \sin^{-1}(\frac{1}{\sqrt{3}k} m_a)}{\pi f_{grid} C_o}. \qquad (5\text{-}5)$$

Fig. 5-3 and Fig. 5-4 show the comparison of the voltage drop ΔV_o versus C_o at 50 Hz and 60 Hz respectively with and without boost switch operation under faulty mode of one phase opened.

Both cases are plotted at the nominal condition v_{LL} = 480 V and v_{LL} = 400 V where m_a = 0.75 and m_a = 0.9 respectively. All the cases are at the same conditions of I_o = 2/3 I_{rated} (k = 1.4 with boost switch and k = 1.7 without boost switch operation).

A) Design Guidelines with Buck+Boost Mode Operation

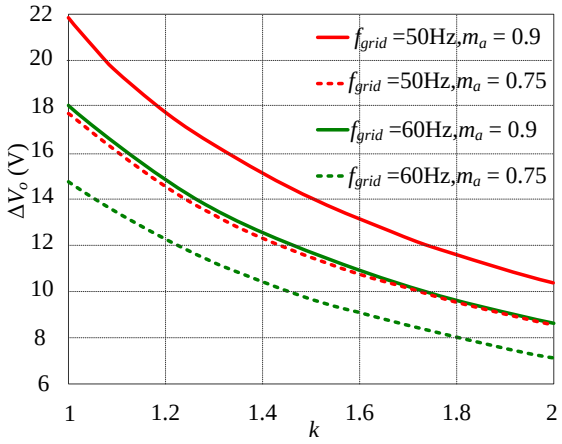


Fig. 5-5 The output voltage drop ΔVo versus the over current racial k in one phase loss operation with boost switch at ma = 0.75 and 0.9 respectively with C_o = 1.4 mF.

Compared with the pure buck operation (without boost switch), the voltage drop with the boost switch activated is significantly smaller. Alternatively, the output capacitance can be substantially reduced with boost mode operation if the voltage drop is kept the same as that of without boost operation. The m_a and grid frequency also play very important role in determining the voltage drop. Either higher m_a or lower grid frequency will result in higher voltage drop.

Since the boost capability is achieved by only adding a boost switch, the impact on the power density of the converter is very small. In addition, the boost switch is only operating during small interval (highlighted interval in Fig. 5-2 (c) and (d)) when $|v'_{AB}|$ is lower than V_o. Therefore, the high current through the boost switch won't cause a high thermal stress on the boost switch. From (5-5), we can conclude that higher over current racial k (higher I_{clamp}) will result in lower ΔV_o.

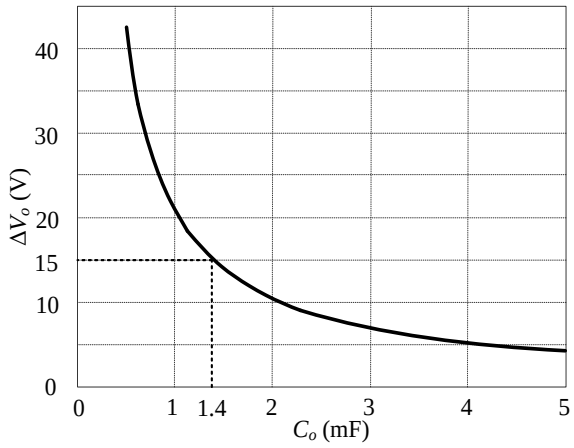


Fig. 5-6 The output voltage drop ΔV_o versus output capacitance C_o in one phase loss operation with boost switch at m_a = 0.9, f_{grid} = 50 Hz and $I_{clamp} = 1.4 I_{rated}$.

Fig. 5-5 shows curve of ΔV_o versus the over current racial k at different m_a and different grid frequencies. However, constrains need to be applied to k. The most important constraint for selecting I_{clamp} is the maximum allowable output inductor current. The maximum inductor current is designed based on the maximum required current in the normal three-phase operation. It is a popular case that the power supply should be able to deliver full power in the output voltage rang of (270 V~380 V) during three-phase operation. In this case, the maximum output inductor current should be at least $1.4I_{rated}$ plus some margin for transient. Then it's safe to set I_{clamp} = $1.4I_{rated}$. The next step is to decide the output capacitance to satisfy the required ripple voltage ΔV_o. Since the worst case for ΔV_o happens at the highest m_a and the lowest grid frequency, the case of m_a = 0.9 and f_{grid} = 50 Hz is selected to draw the curve of the voltage drop ΔV_o versus C_o at $I_{clamp} = 1.4 I_{rated}$ as shown in Fig. 5-6. Finally, capacitance of 1.4 mF is selected as a compromise between the output voltage drop and power density of the rectifier. With 1.4 mF output capacitance, the output voltage drop ΔV_o is less than 3% of nominal output voltage during one phase lost operation. In summary, the worst case to determine the maximum output voltage drop ΔV_o and the required current clamping during one phase loss is at maximum m_a and minimum grid frequency. Therefore, for the given ΔV_o and output power, the output capacitor and current clamping should be selected at maximum m_a and minimum grid frequency.

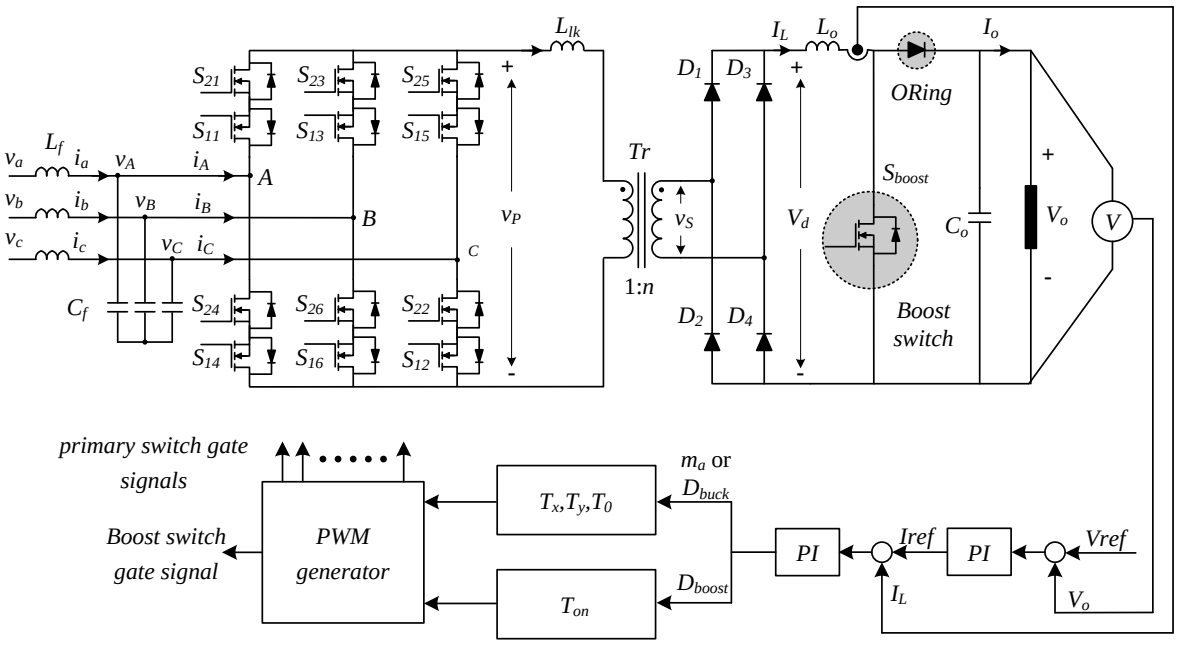


Fig. 5-7 The control block diagram of the converter for buck+boost and buck operation.

To prevent output inductor current oscillations at the boundary between the pure buck and the buck+boost operations, a common controller is employed as shown in Fig. 5-7. The output of the current controller is then utilized for the calculation of the relative on-times of the buck-type input part as well as for the boost output stage.

Since measurements in reality contain noise and/or delay times, the robustness of the control is significantly improved with a common controller. Control parameter design for the cascaded voltage loop and current loop with average current mode control is quite similar to conventional buck DC-DC converter and boost DC-DC converter.

Although the output voltage drop is significantly improved with the proposed control scheme, the high input currents THD obtained during one phase loss operation is the main drawback of this control scheme. It may not be acceptable for the system that might even run for days when one phase is lost. Therefore, another type of control scheme to minimize the input current THD and at the same time maintain low output voltage drop is also proposed and will be discussed in next section.

5.1.2 Analysis Of Operation to Achieve Miminum Input Current THD during One Phase Opened or Shorted

The equivalent circuit of the primary side during one phase loss operation is the same as that described in the previous chapter, where the phase leg of the lost phase is excluded for both one phase opened and shorted. Similar to buck + boost operation discussed in the previous section, the boost switch is activated when the input voltage is not high enough to regulate the output voltage. In order to achieve minimum input current THD, the input current is controlled to follow the same shape as the input voltage, which is similar to operation of the conventional single phase PFC. Therefore, this operation mode can also be called buck+boost with PFC. The primary switches of the isolated buck matrix-type rectifier need to be activated in the entire line cycle (six sectors) and there is no "off time" in sector II and V. The equivalent circuit can be simplified as a buck+boost converter as shown in Fig. 5-8. Similar to conventional single phase PFC, the inductor current is used for current mode control to shape the input grid currents. However the inductor current has to be properly shaped at both buck+boost operation and pure buck operation in order to have low distortion input grid current with unity power factor. Since the ideal input current is controlled to follow the same shape as the input voltage to mimic an ohmic load, the power drawn by the rectifier is given by the following equation:

$$p_{in}(\theta) = \frac{v_{in}^{\ 2}(\theta)}{R_{in}} = \frac{\hat{V}_{in}^{\ 2}\sin^2(\theta)}{R_{in}} = \frac{\hat{V}_{in}^{\ 2}(1-\cos(2\theta))}{2R_{in}} \tag{5-6}$$

where $v_{in}(\theta) = \left|v'_{AB}(\theta)\right| = n\sqrt{3}\hat{V}_m \sin(\theta + 2\pi/3)$ when "phase *C*" is considered as a phase loss.

For the following analysis, it is assumed that the input current is a pulsating sinusoid (the superimposed saw tooth current ripple is neglected), and is in phase with the input voltage $v_{in}(\theta)$. The output voltage V_o can be considered as a constant DC voltage because of the very high value output capacitor C_o. The output power is constant for the considered time interval. Fig. 5-8 shows the voltage, current and power curves of the rectifier in the time domain.

Because there is no intermediate energy storage inside the rectifier, the instantaneous power at the input and output of the rectifier has to be equal as stated by

$$p_{in}(\theta) = p_o(\theta) = i_{in}(\theta)v_{in}(\theta) = \hat{I}_{in}\hat{V}_{in}\sin^2\theta = \frac{1}{2}\hat{I}_{in}\hat{V}_{in}(1-\cos(2\theta))$$
$$= \underbrace{I_{in\_rms}V_{in\_rms}}_{\text{DC}} - \underbrace{I_{in\_rms}V_{in\_rms}\cos(2\theta)}_{\text{AC}} = \underset{\text{DC}}{P_o} - \underbrace{P_o\cos(2\theta)}_{\text{AC}} \quad (5\text{-}7)$$

Therefore, the input power consists of a DC and AC components where the DC component is equal to the output power $P_o = I_{load}V_o = \text{const}$ and AC component corresponds to AC power in (5-7). Since $p_o(\theta) = V_o \cdot i_o(\theta)$, the switching average output current $i_o(\theta)$ can be derived by

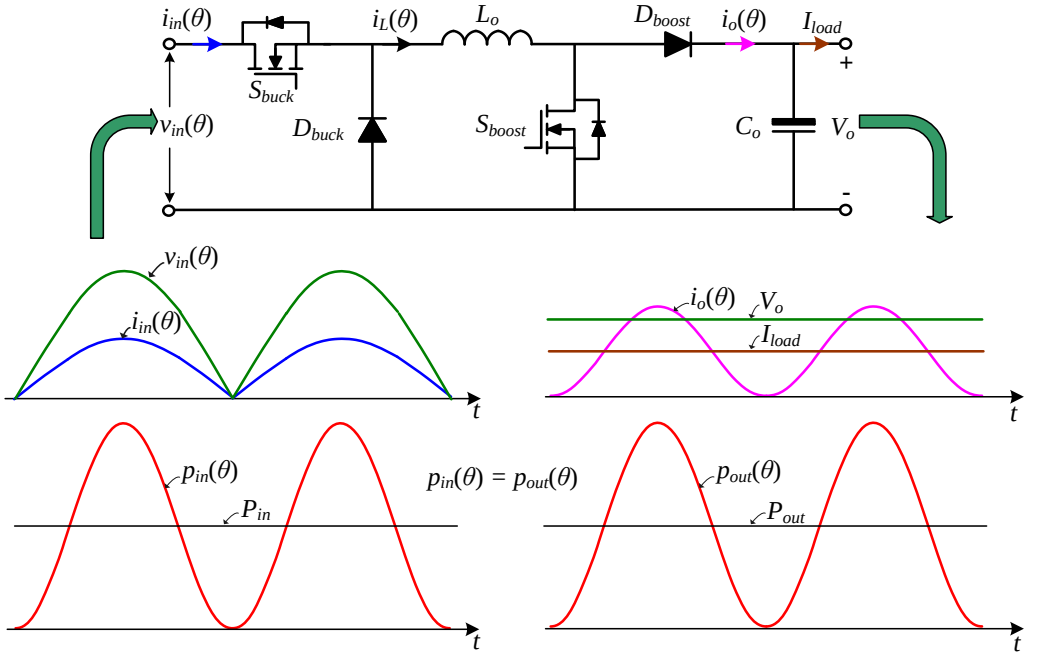
$$i_o(\theta) = \frac{p_o(\theta)}{V_o} = \underset{\text{DC}}{\frac{P_o}{V_o}} - \underbrace{\frac{P_o}{V_o}\cos(2\theta)}_{\text{AC}} = \underset{\text{DC}}{I_{load}} - \underbrace{I_{load}\cos(2\theta)}_{\text{AC}}. \quad (5\text{-}8)$$

It is important to note that during buck+boost operation the inductor is in series with input line terminal and during pure buck operation the inductor is in series with output terminal as shown in Fig. 5-8 (b) and (c) respectively. Therefore, it is essential the inductor current is shaped properly based on these two operations.

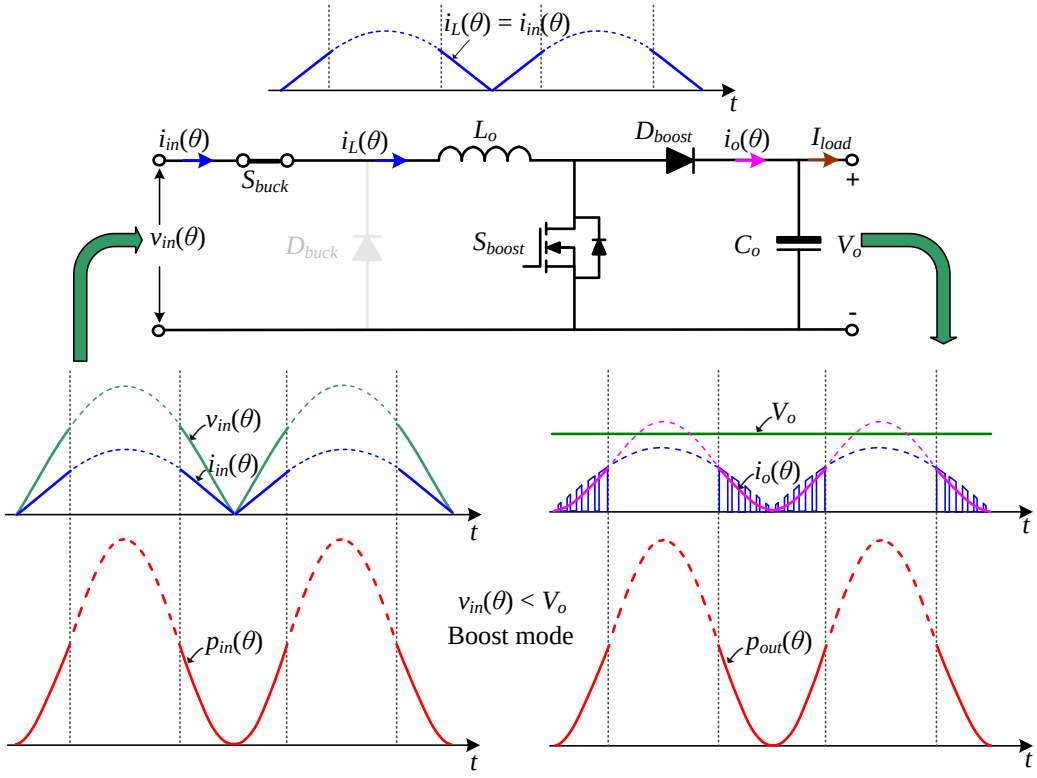
The circuit principal waveforms within one gird cycle with excessively increased switching period of PWM when the boost switch is enabled to function as a PFC during one phase loss operation can be observed in Fig. 5-9. During buck+boost operation (intervals of M1 and M3) in Fig. 5-9, buck switch S_{buck} operates at maximum duty cycle which can be considered as always closed and the boost switch S_{boost} is enabled to keep the input current the shape of the input voltage as shown in Fig. 5-8 (b). The switching average of the inductor current for this operation can be expressed as

$$i_L(\theta) = i_{in}(\theta) = \hat{I}_{in}\left|\sin(\theta)\right|. \quad (5\text{-}9)$$

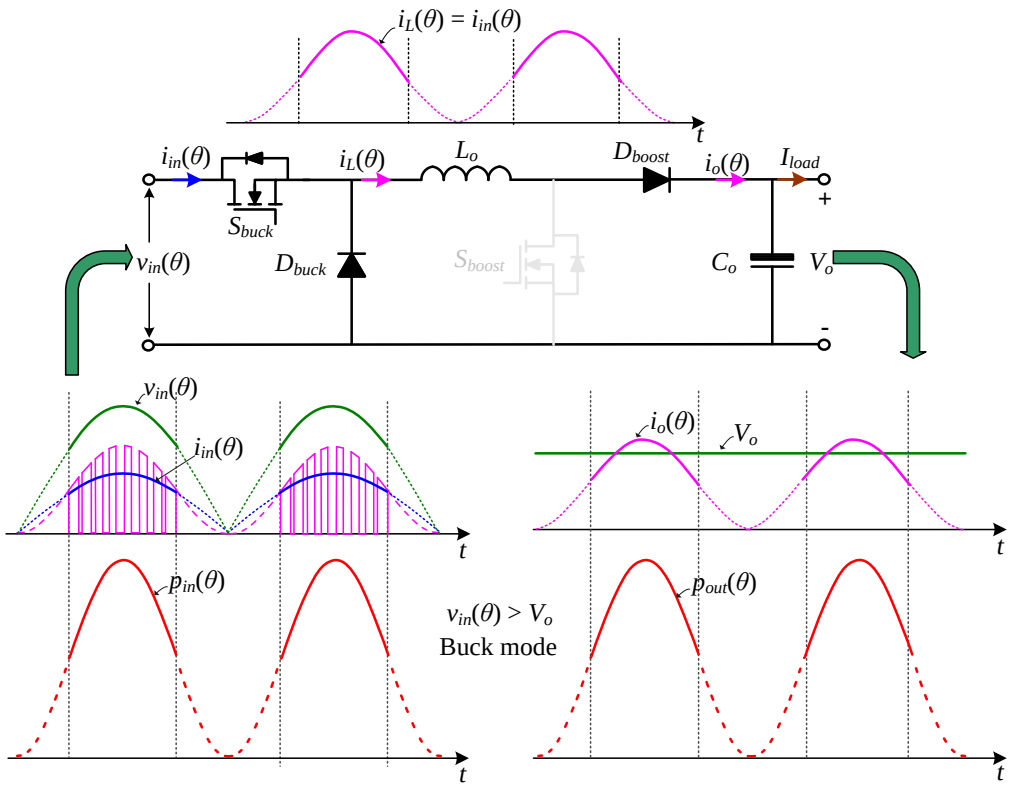
During pure buck operation (interval of M2) as shown in Fig. 5-9, the boost switch S_{boost} is disabled and the buck switch S_{buck} is switched to regulate the inductor current.


$i_{in}(\theta)$
$i_L(\theta)$
L_o
D_{boost}
$i_o(\theta)$
I_{load}
S_{buck}
$v_{in}(\theta)$
D_{buck}
S_{boost}
C_o
V_o
+
-
$v_{in}(\theta)$
$i_{in}(\theta)$
$i_o(\theta)$
V_o
I_{load}
t
$p_{in}(\theta)$
P_{in}
$p_{in}(\theta) = p_{out}(\theta)$
$p_{out}(\theta)$
P_{out}

(a)


$i_L(\theta) = i_{in}(\theta)$
t
$i_{in}(\theta)$
$i_L(\theta)$
L_o
D_{boost}
$i_o(\theta)$
I_{load}
S_{buck}
$v_{in}(\theta)$
D_{buck}
S_{boost}
C_o
V_o
+
-
$v_{in}(\theta)$
$i_{in}(\theta)$
V_o
$i_o(\theta)$
$p_{in}(\theta)$
$v_{in}(\theta) < V_o$
Boost mode
$p_{out}(\theta)$

(b)



(c)

Fig. 5-8 The simplyfied equivalent circuits of the converter during one phase loss operation (a) buck+boost operation (b) boost operation and (c) buck operation. (Note: v_{in} is the same as $|v'_{AB}|$)

The switching average of the inductor current for this operation can be expressed as

$$i_L(\theta) = i_o(\theta) = \hat{I}in(1-\mathrm{D})\sin^2(\theta) = 2I_{load}\sin^2(\theta) \tag{5-10}$$

or $i_L(\theta) = i_o(\theta) = I_{load} - I_{load}\cos(2\theta)$ as stated by (5-8).

It is important to note that the output voltage ripple was neglected for the discussion of current shaping above in order to simplify the analysis. Since the output voltage ripple is relatively small, it will not introduce large error. The output voltage has ripples due to the pulsation power with doubled line frequency delivered from the AC side to DC side. Similar to single phase PFC, the output voltage ripple can be calculated by

$$\Delta V_o = \frac{P_o}{2\pi f_{grid} C_o V_o}. \tag{5-11}$$

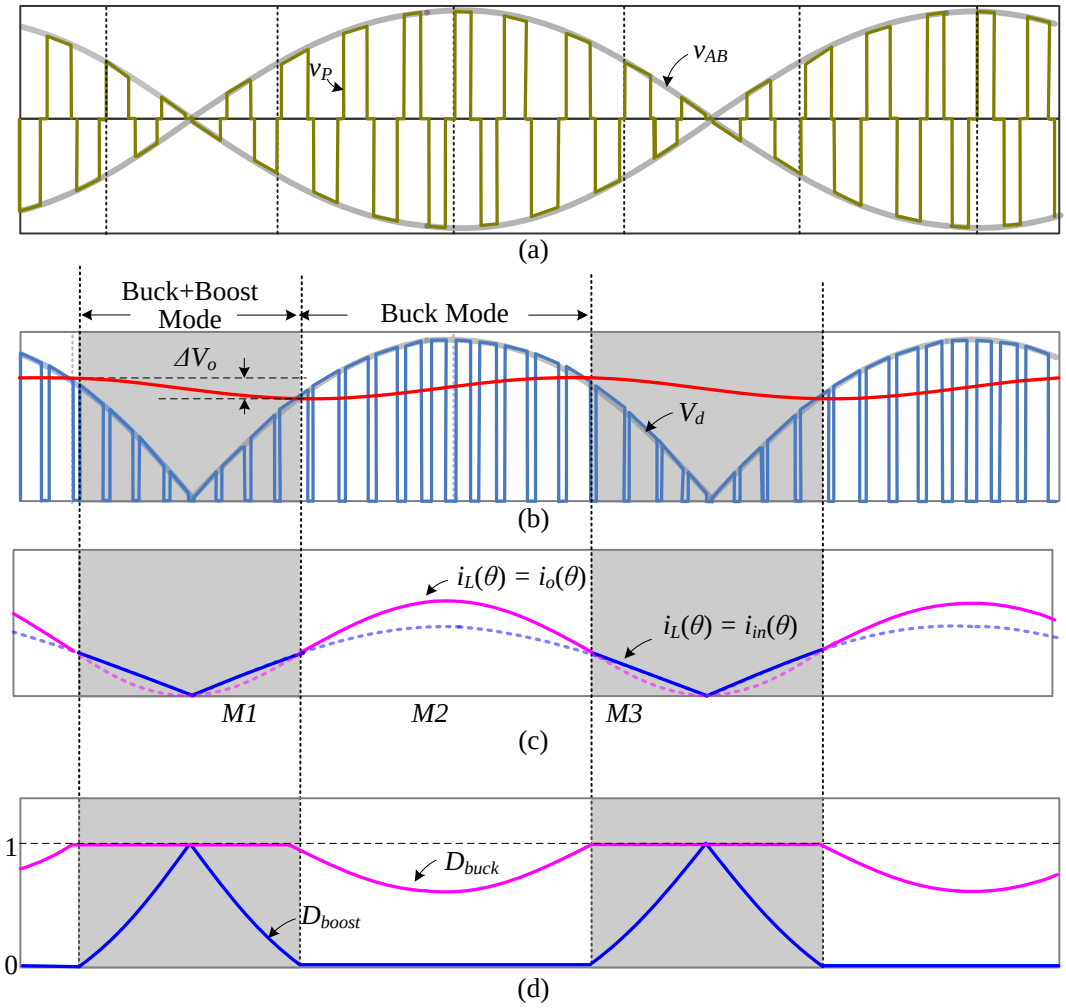


Fig. 5-9 Operation waveforms for Three-phase buck matrix rectifier with integrated boost output stage to achieve minimum input current THD during one phase opened.(d) output inductor current (e) duty cycle of Buck mode and buck+boost mode.

Fig. 5-10 shows the comparison of output voltage drop ΔV_o versus output storage capacitor for three different operations of the converter: pure buck, buck + boost and buck + boost with PFC. It is shown that the buck+boost operation has the minimum output voltage ripple compared with other two operations. The buck+boost with PFC operation has higher output voltage drop compared to buck+boost operation, however, it has lower output voltage drop compared with pure buck operation.

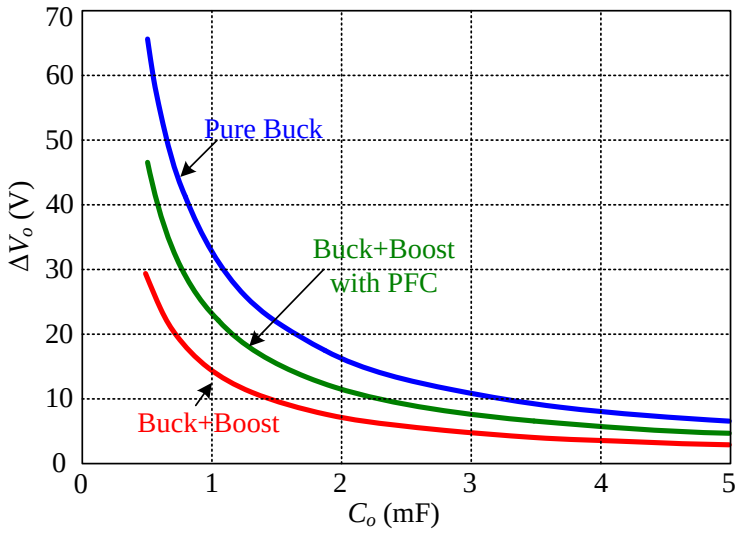


Fig. 5-10 Output voltage drop vs capacitor for different operations of rectifier during one phase loss operation.

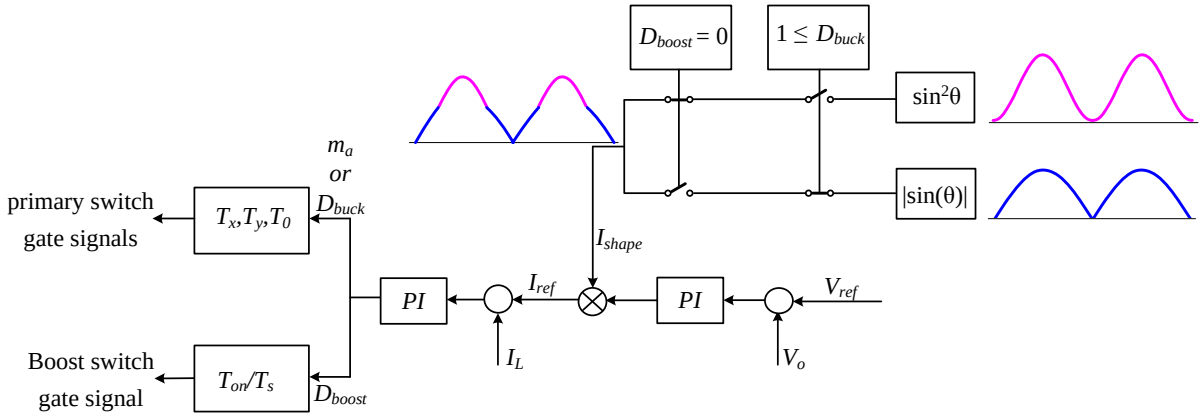


Fig. 5-11 Complete control structure enabling sinusoidal input currents under one phase loss operation.

A) Control Structure for Buck+Boost with PFC Operation during One Phase Loss

The basic control structure of the buck+boost with PFC is depicted in Fig. 5-11. A slow outer control loop regulates the output voltage to a constant reference voltage V_{ref} and sets the reference value for the fast inner inductor current loop. To realized unity PF and sinusoidal input current, the current reference I_{shape} must exhibit shape of $|\sin(\theta)|$ in buck+boost operation and shape of $\sin^2(\theta)$ in buck operation as stated by equations (5-9) and (5-10) respectively.

During three-phase operation I_{shape} is set to unity. The output of the current controller is the duty-cycle that is used for the calculation of the relative on-times of the transistors of the buck input part as well as the boost output part. It should be noted that, similar to operation of the single phase PFC, the voltage control loop bandwidth for one phase loss operation should be low (< 10 Hz) such that the current shape will not be affected by the voltage control loop. The controller design of the conventional single-phase PFC can be applied here.

5.1.3 Analysis of Operation to Achieve Tight Ouput Voltage Regulation during One Phase Shorted

When one phase is shorted to the neutral of the source, the shorted phase has the same potential as the neutral point. Therefore, the line-to-line voltage between the faulty phase and the other two phases reduced to the same value as the phase voltage. In order to achieve minimum output voltage drop, a modulation scheme is proposed to maximize the utilization of the input voltage during one phase shorted operation. In each sector, the highest line-to-line voltage is selected to synthesize the transformer primary voltage. The resultant transformer voltage v_p for phase *C* shorted operation is shown in Fig. 5-12. During sector I, III, IV and VI the transformer primary voltage is synthesized by v_{AB}, which is same as that of one phase opened operation.

While during sector II and V, the transformer primary voltage is synthesized by either v_{AC} or v_{BC} depending on which magnitude is higher. As shown in Fig. 5-12 (c), the minimum value of the envelope of rectifier output voltage $V_{d\_\min}$ (in the middle of sector II and V) is not zero with the proposed one phase shorted PWM scheme. The average of output voltage $\bar{v}_d(\theta)$ in each switching cycle during sector II and V is expressed by

$$\bar{v}_d(\theta) = \begin{cases} \left| v_{AC}'(\theta) \right| D_{\text{sec}}(\theta) \\ \left| v_{BC}'(\theta) \right| D_{\text{sec}}(\theta) \end{cases} . \qquad (5\text{-}12)$$

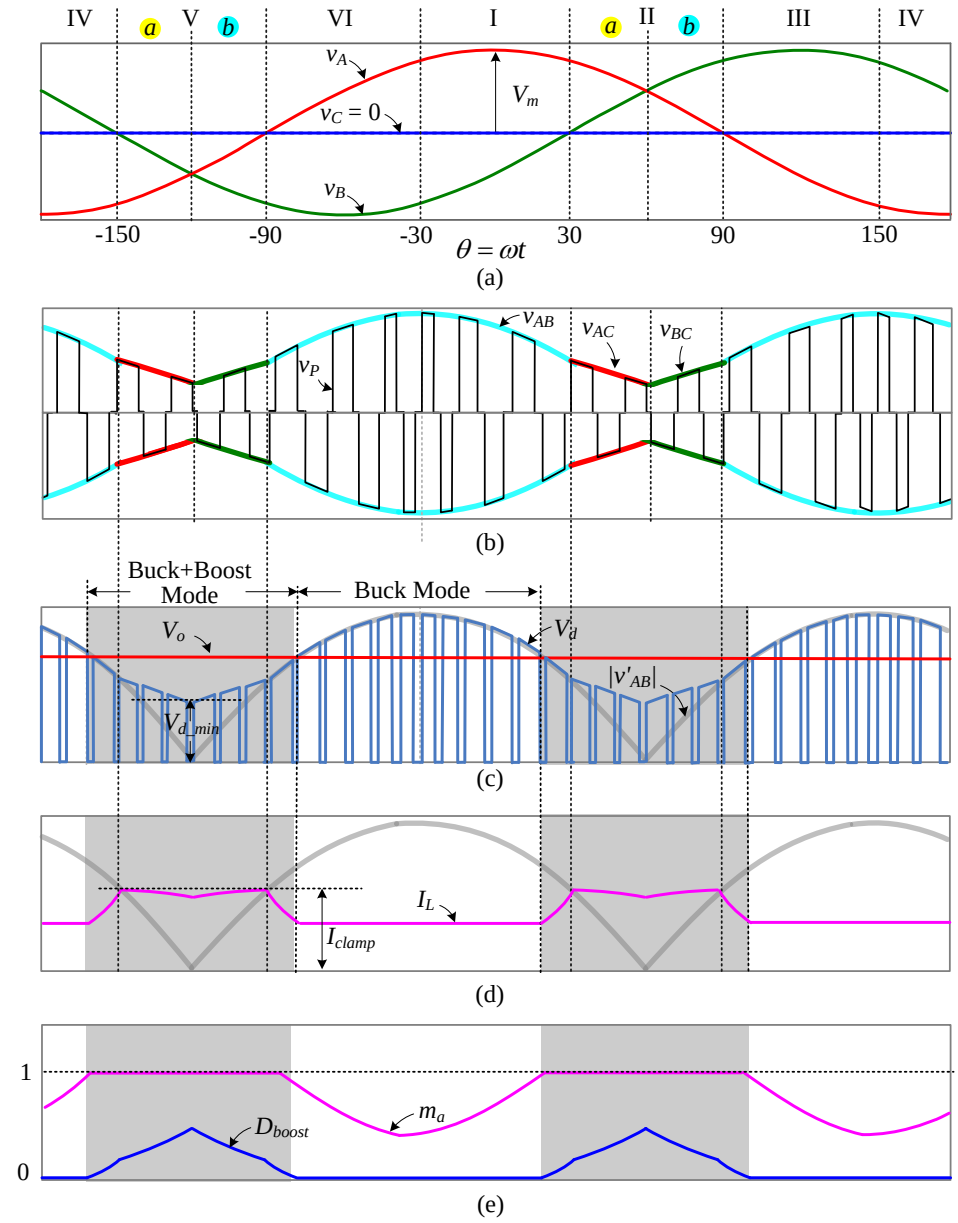


Fig. 5-12 Operation waveforms for Three-phase buck matrix rectifier with integrated boost output stage to achieve minimum output voltage drop during one phase shorted.

It should be noted that the duty-cycle loss cannot be neglected during sector II and V since V_d is relatively low and current is high. Due to the duty-cycle loss, $\overline{v}_d(\theta)$ can be significantly smaller than V_d. In the middle of sector II and V, $\overline{v}_d(\theta)$ is almost half of the $V_{d\_\min}$.

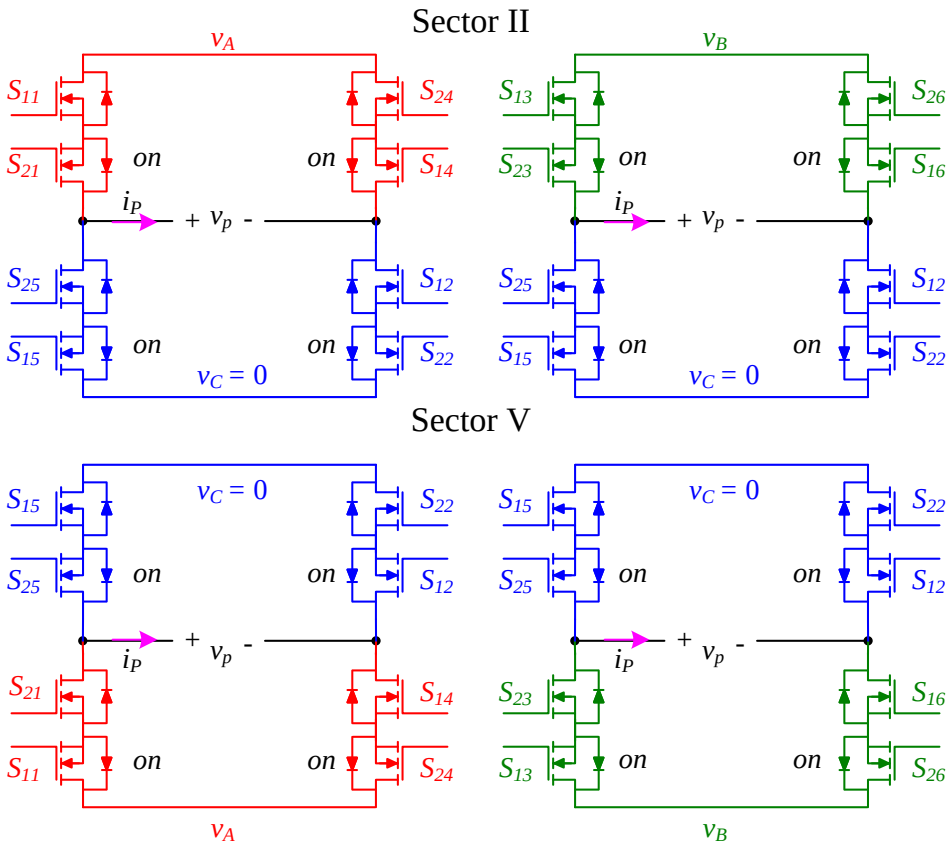


Fig. 5-13 The Equivalent circuit for one phase shorted operation during sector II and sector V.

The maximum required inductor current to regulate the output voltage at two-third of rated power can be calculated by

$$I_{L,\max} = \frac{2}{3}\frac{P_{o,rated}}{\overline{v}_d(\pi/6)}. \tag{5-13}$$

It is important to note that $I_{L,\max}$ may exceed the upper limit and will be limited at I_{clamp} by the controller. In this case a small voltage drop will be visible but it is much smaller than the case of one phase opened. In sector I, III, IV, VI, the equivalent circuits of converter primary side during one phase shorted is same as that for one phase opened operation. Therefor, associated PWM schem for one phase shorted operation is also same as that of one phase opened operation in these sectors. However, in sector II and V, the phase leg of the faulty phase is also involved in one phase shorted operation so that different equivalent circuits are derived as shown in Fig. 5-13

(assuming "phase *C*" is shorted $v_C = 0$) and the associated PWM schem is described in Fig. 5-14. ZVS operation principle of FB-PS can also be applied here so that ZVS can be achieved for one phase shorted operation in all the sectors. Fig. 5-13 and Fig. 5-14 show the equivalents circuit and PWM scheme respectively in one phase shorted operation. It is worth mentioning that the same control scheme as shown in Fig. 5-7 can be used for the case of one phase shorted.

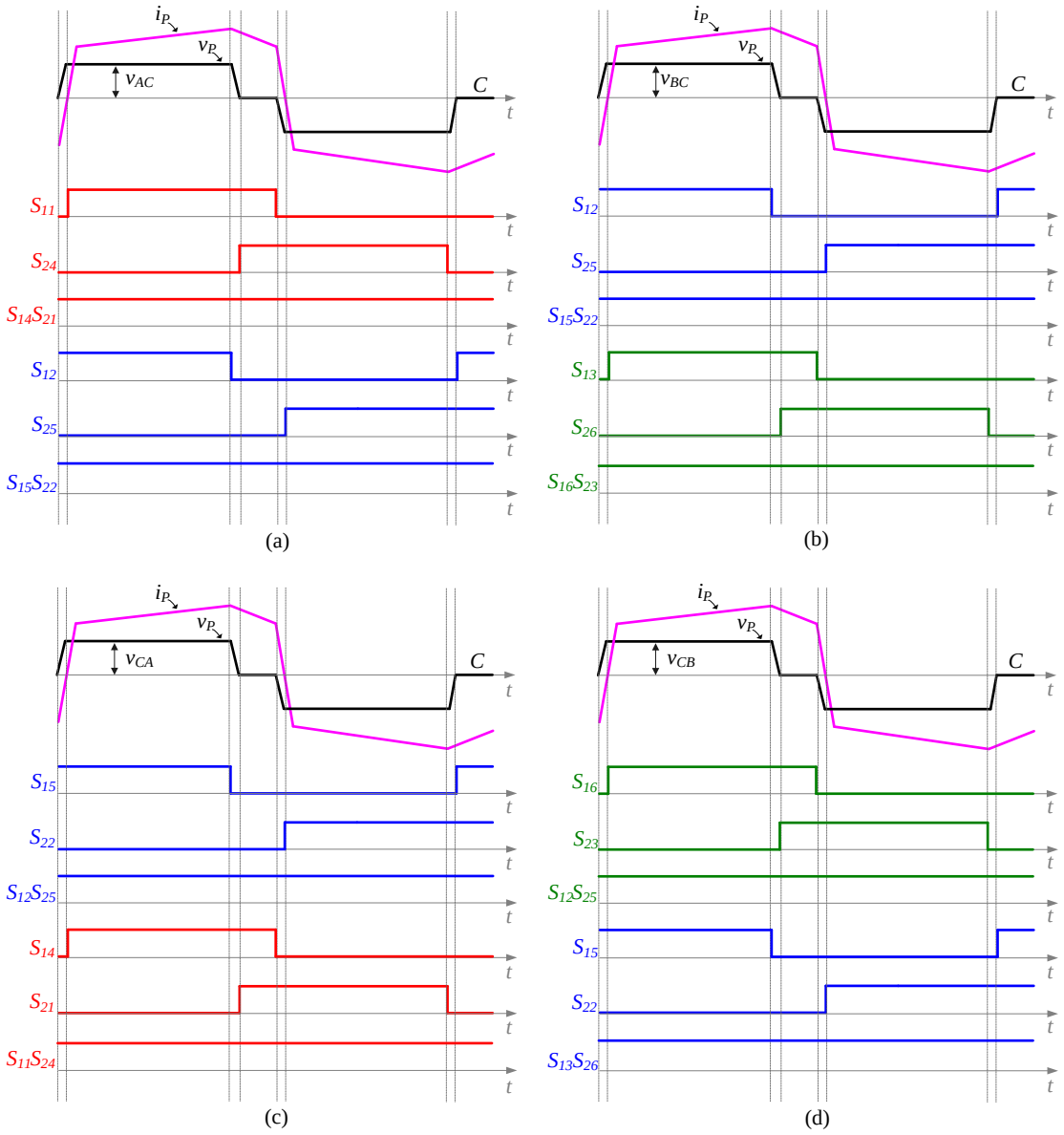


Fig. 5-14 PWM schem for one phase shorted operation during sector II and sector V.

5.2 Simulation Result and Discussion of Output Voltage Regulation

To verify the analysis of one phase loss operation of the converter, a simulation model is built and tested at two-third of rated power. In the simulation, the output voltage drop ΔV_o of the conventional buck converter (without boost switch) and of the converter with the proposed boost stage are compared. In addition, the key simulation waveforms for the converter with the boost stage activated is provided. The upper limit of the average output inductor current with buck+boost mode operation, I_{clamp}, is set at 18.5 A ($1.4I_{rated}$) and the output storage energy C_o = 1.4 mF is selected based on the analysis in section (5.3.1). It should be noted that the minimum required I_{clamp} for the operation without boost switch at m_a = 0.9 is 20.4 A based on (6) in section. II. Considering some margin to account for the duty cycle loss, I_{clamp} is set at 22 A ($1.7I_{rated}$). The minimum required I_{clamp} for the pure buck mode operation (without the boost switch) during one phase loss operation has been discussed in Chapter 4. However, the I_{clamp} given in Chapter 4 is chosen based on the nominal condition where m_a is equal to 0.75. If consider the worst case analysis at m_a = 1, then I_{clamp} = 26.3 A ($2I_{rated}$) should be selected.

5.2.1 Discussion of Output Voltage Regulation

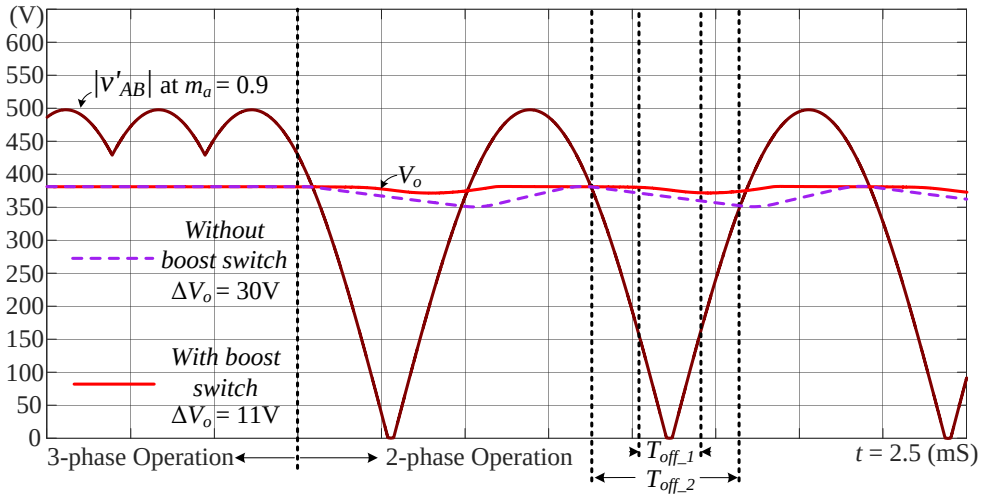


Fig. 5-15 Comparison of output voltage drop ΔV_o for conventional buck rectifier and buck rectifier with boost switch at m_a = 0.9 and f_{grid} = 60 Hz.

Fig. 5-15 shows the comparison of the output voltage drop at maximum m_a = 0.9 for pure buck (without boost switch) operation and buck rectifier with boost switch enabled to verify the analysis given in section. 5.1.1. As it is noticeable from two out voltage waveform, the output voltage drop ΔV_{o1} in boost operation is significantly smaller than the output voltage drop ΔV_{o2} in pure buck operation. This is due to the reduced off time intervals of T_{off_1} in boost operation compared with T_{off_2} of pure buck operation.

5.2.2 Key Simulation Waveforms of Buck Matrix Rectifier with Boost Switch Activated

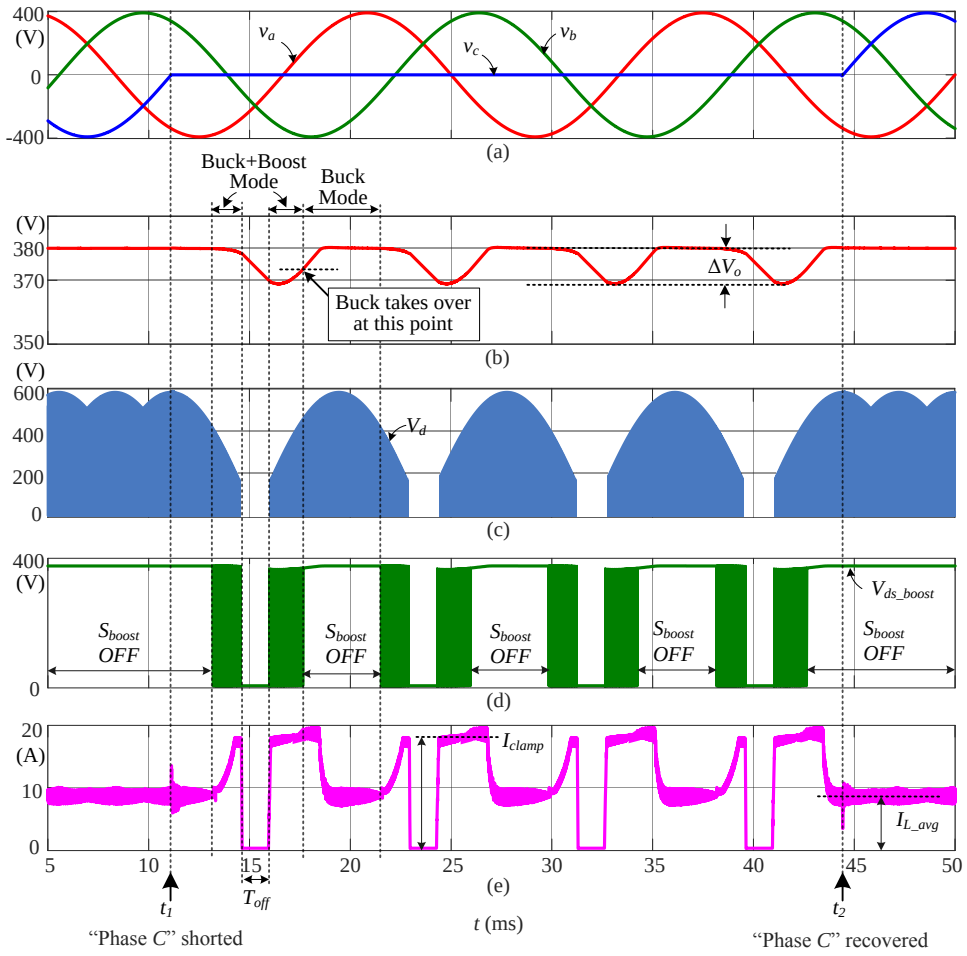


Fig. 5-16 Simulated waveforms for buck matrix rectifier with boost switch activated: v_{LL} = 480 V (at m_a = 0.75), f_{grid} = 60 Hz, k = 1.4 and 2/3Po_max when "phase C" is sorted and recovered.

The purpose of simulation result here is to verify the operation of the rectifier with integrated boost output stage. As shown in Fig. 5-15, at t_1, the "phase *C*" is shorted and at t_2 is recovered. Boost switch is enabled during one phase lost operation when V_d is lower than V_o. The maximum inductor current is clamped at 18.5 A by the controller during one phase lost operation. At steady state, I_{L_avg} is around 8.77 A to deliver two-third of rated power. The output voltage drop ΔV_o is around 11 V. Smooth transition between buck+boost mode operation and buck mode operation can be observed from the output inductor current, since both the primary switches of buck matrix rectifier and the boost switch are controlled by the same controller.

5.3 Experimental Verification

Experimental test is conducted on a 5 kW three-phase isolated buck matrix-type rectifier with integrated boost output stage, v_{LL} = 480 V, f_{grid} = 60 Hz, m_a = 0.75 and k = 1.4. Detail experimental system parameters are similar to Table. 3-2 with an additional S_{boost} (IPW60R041P6) and D_{oring} (2 x C3D16065A).

5.3.1 Experimental Verification to Achieve Minimum Output Voltage Drop in One Phase Opened Operation

As shown in Fig. 5-17 (a), the output voltage ripple ΔV_o is 11 V which is less than 3% of nominal output voltage. Waveform of V_{ds_boost} shows that the boost switch is enabled only during intervals of V_d lower than V_o. The zoom in waveforms in Fig. 5-17 (b) shows that the inductor current I_L is clamped at 18.5 A. The current shape is consistent with the analysis in Fig. 5-2 (d) and simulated waveform in Fig. 5-16 (e). However, the current stair case during buck+boost mode operation is caused by the quantization error of the ADC for voltage sensing in boost controller. Higher resolution of the ADC can help to mitigate this problem. During T_{off} interval, both the primary switches and the boost switch are stopped switching to reduce the losses since V_d is too low to regulate the output voltage. It should be noted that the PWM scheme of the isolated buck matrix-type rectifier during one phase loss operation is different from those PWM

schemes derived for normal (three-phase) operation and summarized in Chapter 2. A special care needs to be taken for the commutation scheme in order to achieve safe transition between the three-phase and one phase loss operation as discussed in Chapter 4. Input current i_a as shown in Fig. 5-17 (c) and (d) is highly distorted due to the large variation of output inductor current in order to regulate the output voltage during one phase loss operation. This is the main drawback of the proposed control scheme.

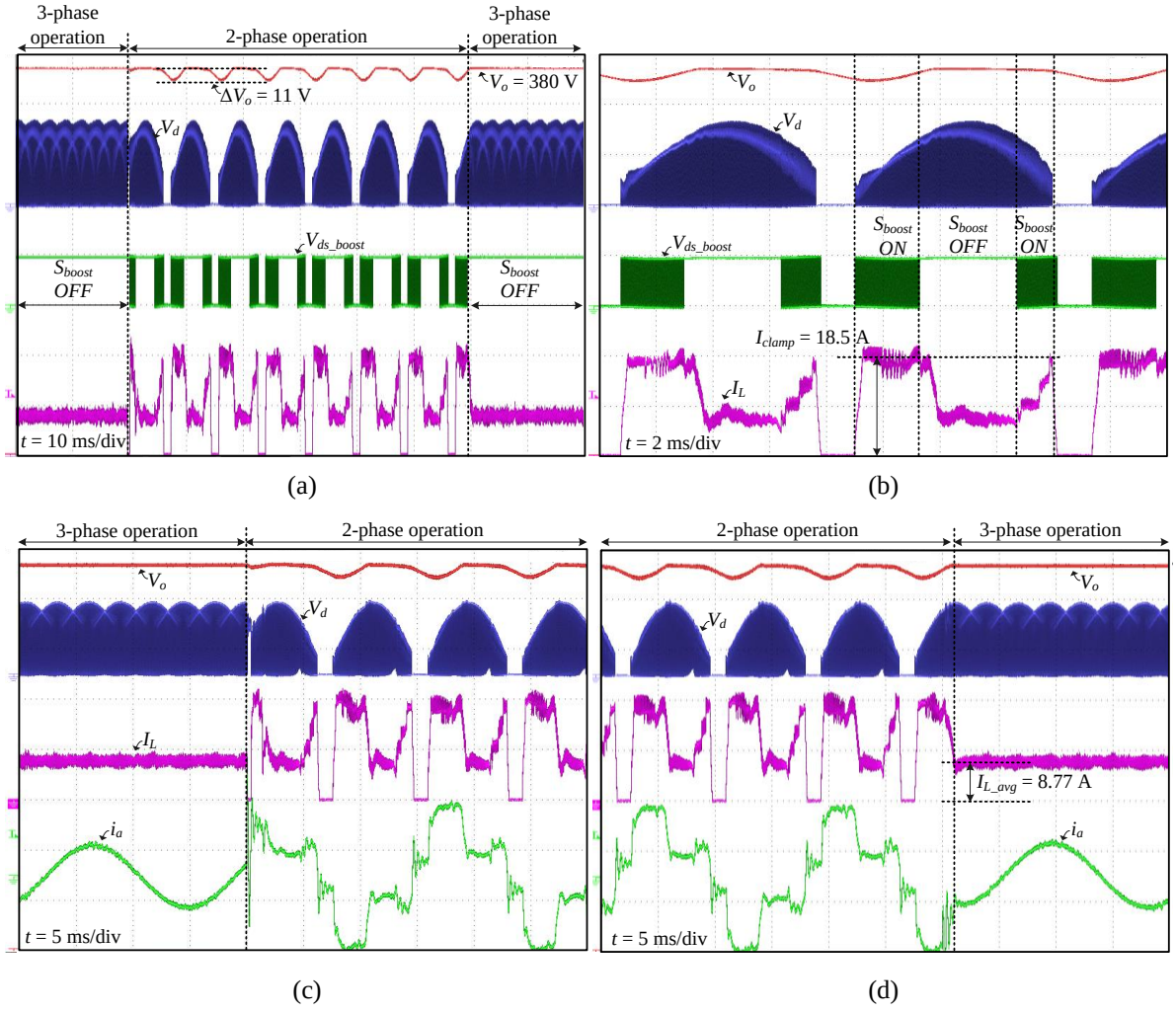


Fig. 5-17 Experimental waveforms of the converter with a boost switch for 2/3Po_max , v_{LL} = 480 V (at m_a = 0.75), f_{grid} = 60 Hz: (a) voltage waveforms of V_o (50 V/div), V_d (400 V/div), V_{ds_boost} (400 V/div), and I_L (10 A/div) (b) Zoom in waveformes of (a) during one phase opened (c) Waveforms from 3-phase operation to one phase opened operation , i_a (10 A/div) (d) Waveforms from one phase opened operation to 3-phase operation.

5.3.2 Experimental Verification to Achieve Minimum Input Current THD in One Phase Loss Operation

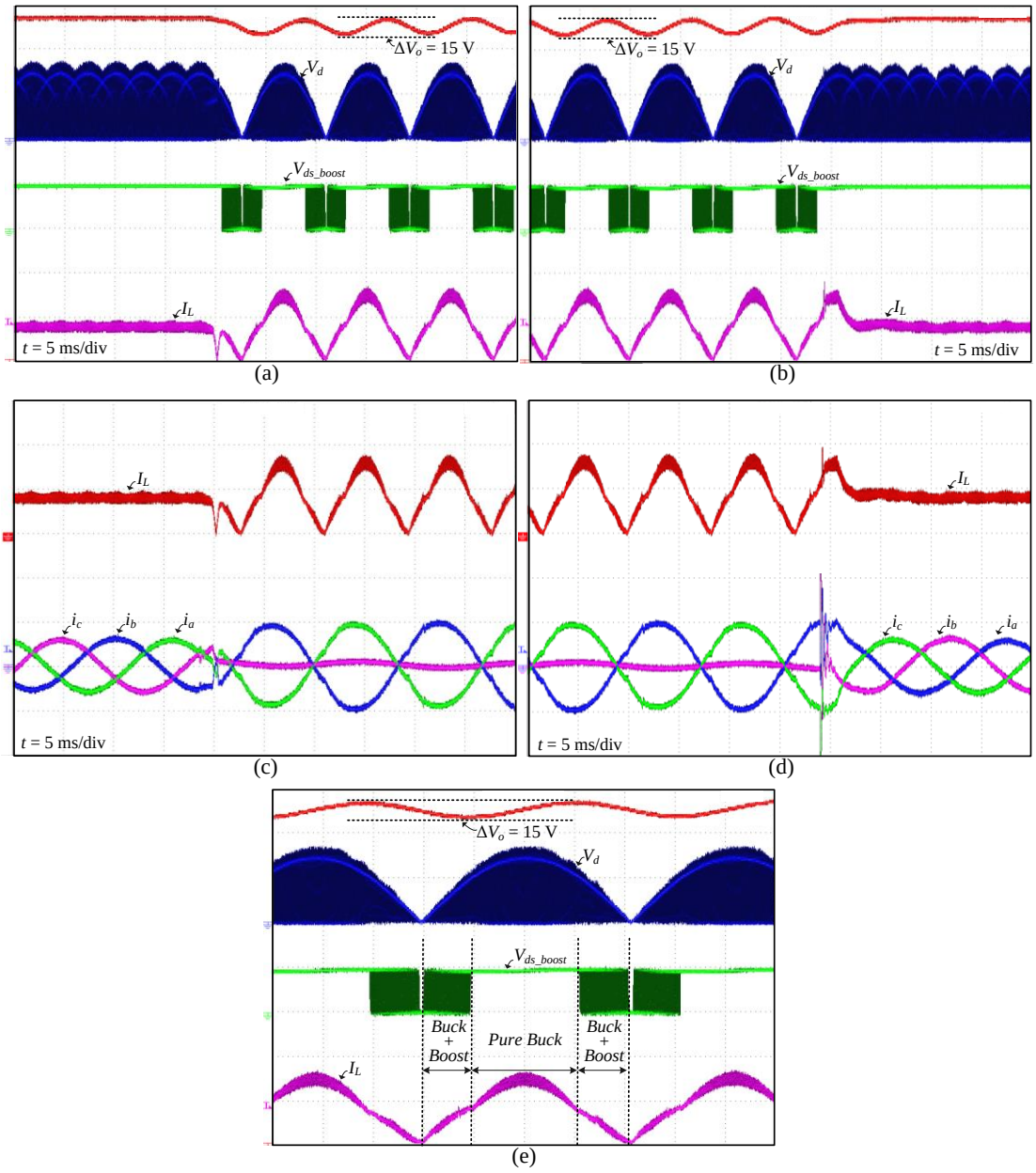


Fig. 5-18 Experimental waveforms of the converter with a boost switch for 2/3*Po_max* , v_{LL} = 480 V (at m_a = 0.75), f_{grid} = 60 Hz: (a) Waveforms of output voltage V_o, rectifier output voltage V_d, boost switch V_{ds} and inductor current I_L during transition from 3-phase operation to one phase loss opertion (b) Waveforms during transition from one phase loss operation to 3-phase operation. (c) current waveforms of i_a , i_b , i_c and I_L (10 A/div) from 3-phase operation to one phase loss opertion (d) current waveforms of i_a , i_b , i_c and I_L (10 A/div) from one phase loss opertion to 3-phase operation. Good input current THD can be maitained for both three phase operation and one phase loss operation (e) zoom-in waveforms shows smoth transition between pure buck mode and buck+boost mode.

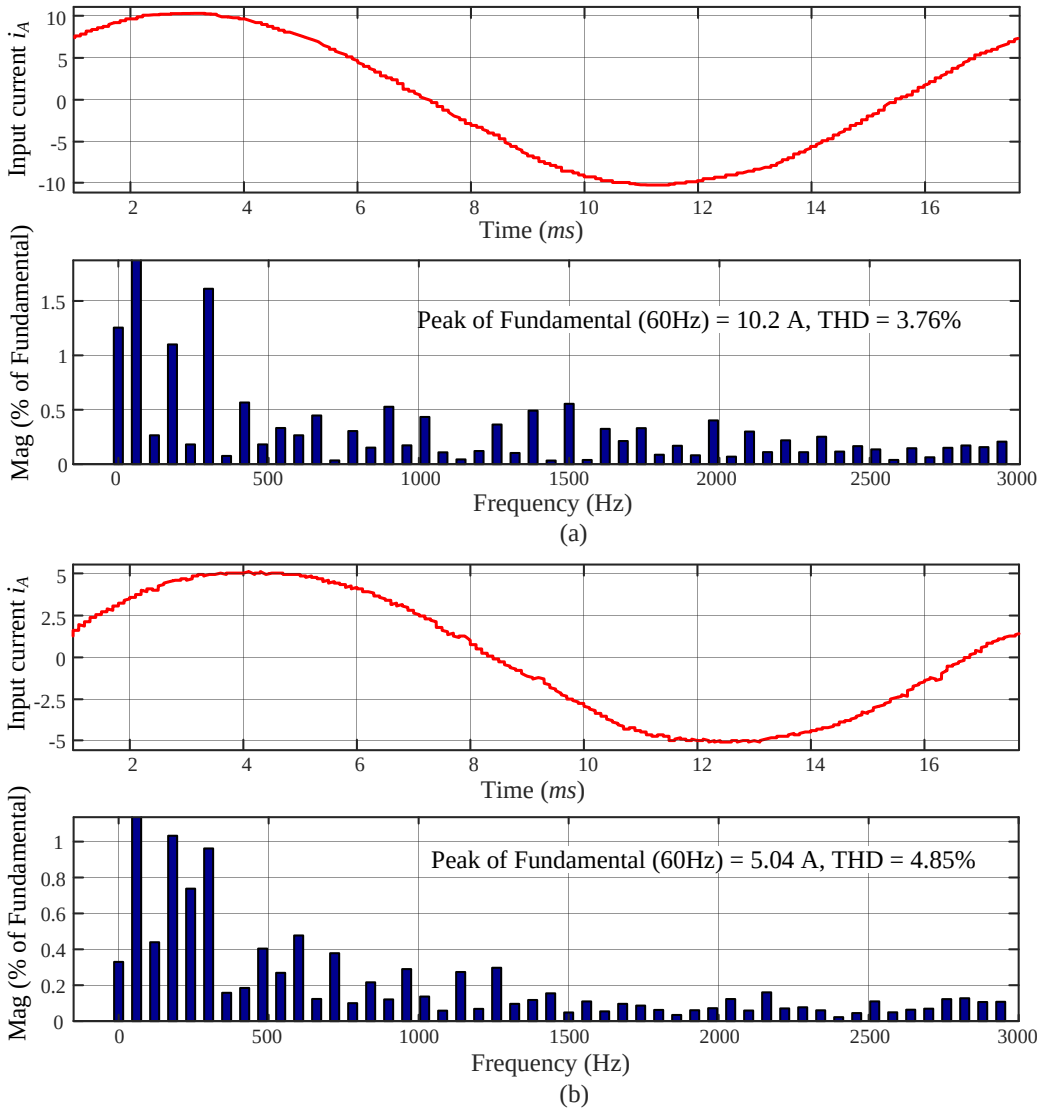


Fig. 5-19 Experimental spectrum analysis of input grid current wave during one phase loss operation shows low THD and its individual harmonics (a) at 100% load (3.3 kW) and (b) at 50% load (1.65 kW).

Fig. 5-18 shows the operation of rectifier during one phase loss with the boost switch is enabled during buck+boost operation and disabled during pure buck operation. Smooth transitions between buck mode and buck+boost mode operation and vice versa can be observed from inductor current. The output voltage ripple ΔV_o is 14.6 V which is less than 4% of nominal output voltage. Similar to single-phase PSU, the output voltage contains low frequency second order harmonics.

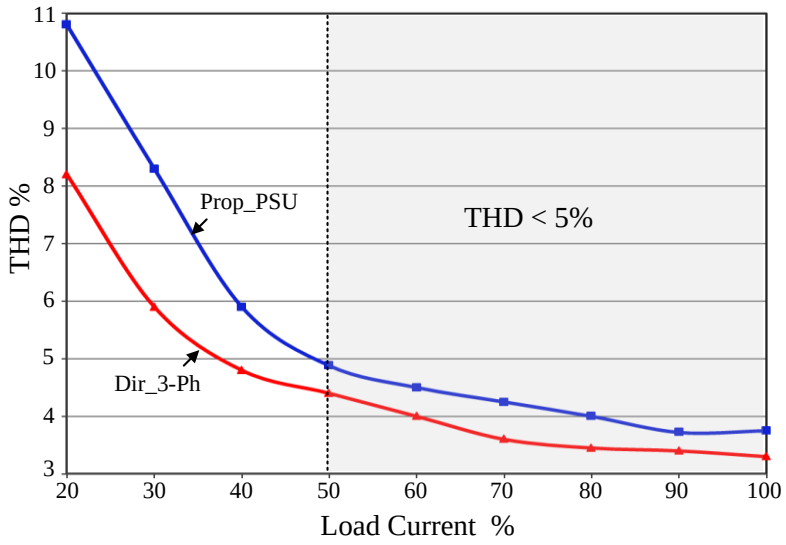
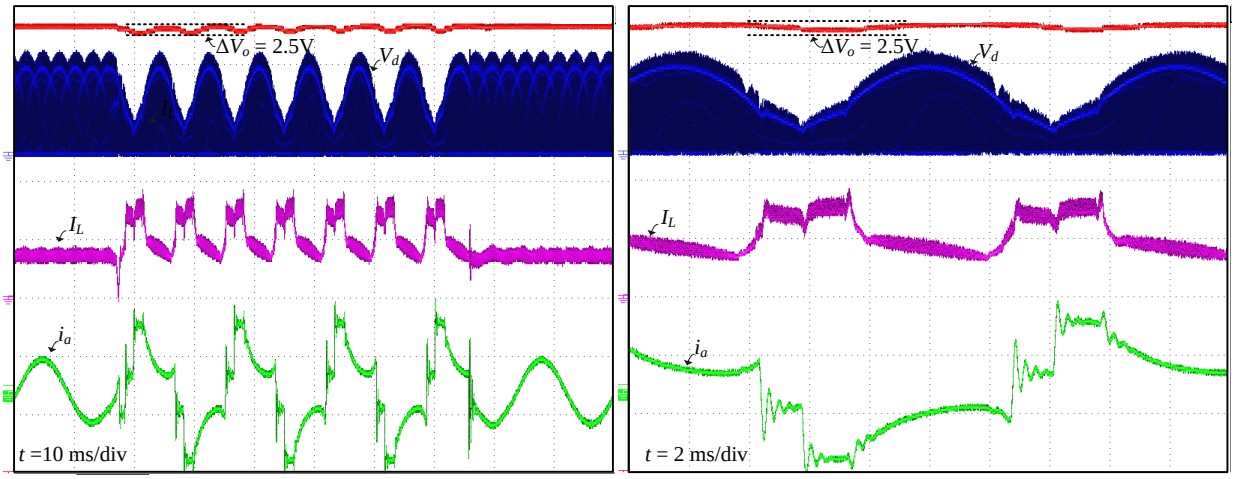


Fig. 5-20 Measured input grid current THD (%) vs load (%) during one phase loss operation for direct three-phase (Dir_3-Ph) and proposed PSU (Prop_PSU).

The input grid currents THD and its individual harmonics at different load currents during one phase loss operation are shown in Fig. 5-19. Very low THD for input grid currents is achieved due to the properly designed current shaping but a slightly higher output voltage drop compared with the buck+boost control. Low input current THD can be maintained for one phase loss operation with the proposed control scheme for buck+boost with PFC function as shown in Fig. 5-18 (c) and (d). This feature can bring significant benefit for the applications that PSU is required to operate at either three-phase or single phase input, e.g. the on board vehicle battery charger. Fig. 5-20 shows measured input grid current THD for direct three-phase (Vienna rectifier + LLC) and proposed PSU (isolated buck matrix-type rectifier) during one phase loss operation. As shown in Fig. 5-20, the input grid currents THD are less than 5% for all load currents above 50% which is below the specified standards in industries.

5.3.3 Experimental Verification to Achieve Tight Ouput Voltage Regulation during One Phase Shorted

As shown in Fig. 5-21, the output voltage drop ΔV_o is 2.5 V during one phase shorted which is within the specification for normal operation.



(a) (b)

Fig. 5-21 Input grid current wave and its indivitual harmonic in one phase loss operation: (a) at 100% load and (b) at 50% load.

The zoom in waveform in Fig. 5-21 (b) shows that the inductor current I_L is clamped at 18.5 A. With larger inductor current clamp (around I_{clamp} = 34 A), the output voltage can be tightly regulated. However, this is not practical way since very large inductor size is required. Grid side current i_a as shown in Fig. 5-20 is highly distorted due to the large variation of output inductor current in order to regulate the output voltage during one-phase shorted. This is the main drawback of the proposed control scheme. Similar control scheme as shown in Fig. 5-7 is applied for this operation.

5.4 Conclusions

In this chapter, the operation principle and performance of three-phase isolated buck matrix-type rectifier with an integrated boost output stage is studied. The boost switch is only enabled in one phase loss operation during the intervals in which the reflected input voltage to secondary side of transformer is lower than the output voltage and is kept OFF during the normal operation. Therefore, the associated loss and heatsink size of this switch is very small. The rectifier with integrated boost output stage exhibits smaller output voltage drop and input current THD during

one phase loss operation compared with pure buck operation. In addition, the value of output capacitance can be substantially reduced with buck+boost operation if the output voltage drop is kept the same as that of conventional buck matrix-type rectifier, rendering to high overall power density of the converter.

With integrated output boost stage, the converter has flexibility to work either with tight output voltage regulation or with very low input currents THD during one phase loss. To consider both tight output voltage regulation and low input current THD, larger value of output capacitance is required. To achieve low input grid current THD and high PF during one phase loss operation, the rectifier operates similar approach as single phase PFC. This feature enables the rectifier to be considered for both three-phase and single-phase applications

Chapter 6
Conclusions

This dissertation work provides comprehensive study on the commutation method and various PWM schemes which are implemented for the isolated buck matrix-type rectifier during three-phase operation and one phase loss operation. The main contribution and important results are summarized and highlighted in this chapter with future work that is also pointed out.

6.1 Main Contributions and Conclusions

The contributions of this dissertation thus lie in the design and implementation of a cost effective PSU with high efficiency and high power density for telecom and data center applications. Based on this and the previous discussion, the contributions are further addressed in what follows:

1) To achieve high power density, it is essential that the rectifier operates at a higher frequency to reduce the size of magnetics components and to achieve high efficiency, and it is essential to implement the soft-switching techniques to mitigate the switching loss. All these benefits are only realized through proposed PWM modulation and commutation schemes. Extend soft-switching techniques such as zero voltage switched phase-shift full-bridge (ZVS-FB-PS) to three-phase isolated buck matrix-type rectifier.

2) Several soft-switched PWM schemes known as six-segment and eight-segment in this dissertation are examined for isolated buck matrix-type rectifier. First, based on the switching characteristics of Si IGBT and MOSFET devices, a six-segment PWM scheme with minimum switching loss is identified among all the six-segment PWM schemes and then the performance of the proposed six-segment PWM scheme (“Type A”) is compared with traditional eight-segment PWM scheme “Type E”.

The comparison between “Type A” and “Type E” unveils “Type A” exhibits lower output inductor current ripple, duty-cycle loss and switching losses compared with “Type E”. However, “Type E” exhibits lower transformer core loss compared with “Type A” since it has a doubled frequency on the transformer when the switching frequency is kept the same for both PWM schemes. Therefore, an improved eight-segment PWM scheme (improved “Type E”) is proposed as an alternative PWM scheme to “Type A” which mitigates a major issue related to large output inductor current ripple with “Type E”

3) Commutation method for “Type A” and improved “Type E” under three-phase operation are proposed to maximize the efficiency with ZVS turn-ON and synchronous rectification operation. For converter with “Type A” implementation, two-step commutation is applied for the transitions from active vector to zero vector and vice versa under ZVS turn-ON, while three-step commutation is required for transitions from active vector to another active vector due to an additional non-ZVS turn-ON. However, the associated turn-ON loss for this transition is very small. The proposed commutation method for improved “Type E” permits all the bidirectional devices of the rectifier to be turned on under ZVS. Constraints of the gating of synchronous rectification are implemented in the proposed commutation scheme to ensure safe operation especially under non-ideal input conditions, e.g. distorted input voltage.

4) A zero voltage switched PWM scheme and commutation method are proposed to maintain proper operation of the rectifier during one phase loss operation. In addition, a safe transition from one phase loss operation to normal operation and vice versa can occur with minimum switching actions (two-step commutation). In order to achieve low input current THD and regulate the output voltage with a small value of output capacitance, the rectifier with integrated boost output stage is proposed. The boost switch is only enabled in one phase loss operation for short intervals of time and is kept OFF during the normal operation. The associated loss and heatsink size of this switch are very small. Therefore, the efficiency of rectifier during normal operation will not be affected and the overall power density of PSU still remains high. With the integrated boost output stage, the performance of the rectifier under one phase loss operation can be significantly improved with selective control objectives (either tight output voltage regulation or low input current THD and high PF) depending on the application. It is important to mention

that these features enable the rectifier to be considered for both three-phase and single-phase applications.

5) Operation and performance of the rectifier with the proposed PWM schemes and commutation methods are verified through simulated and experimental results on a 5 kW prototype. Also, one phase loss operation is evaluated and verified by the simulations and experiments on a 5 kW prototype where the power is reduced to two-thirds of the rated power.

6) Furthermore, the loss breakdown and efficiency comparisons are provided for three prototypes based on isolated buck matrix-type rectifier: SiC MOSFET-based 54 V, SiC MOSFET-based 380 V and Si IGBT-based 380 V. The 54 V prototype is demonstrated the peak efficiency of 98.3%, which is higher than the best commercial products, and the power density is 70.5 W/in^3, which is higher than the state-of-art direct three-phase (Vienna or six-switch boost as first-stage and LLC resonant converter as second-stage) rectifier design.

6.2 Suggested Future Works

1) Extend LLC resonant dc-dc converter concept to three-phase isolated matrix-type rectifier. This provides several advantages.

- Full ZVS turn-ON from no-load to full load for all the primary bidirectional switches.
- With the property of zero-voltage switching (ZVS) turn-ON for the primary switches and both ZVS turn-ON and zero-current switching (ZCS) turn-OFF for the secondary synchronous rectifiers (SRs).
- Higher efficiency and power density are expected with LLC resonant matrix-type rectifier compared with buck matrix-type rectifier since the converter is operated under ZVS for primary switches and ZCS for SRs at much higher switching frequency for all load conditions.
- The LLC resonant converter has boost capability; therefore, it does not require the output boost stage for faulty mode of one phase loss operation.

- The output inductor size can significantly be reduced since the LLC resonant converter doesn't require large output inductor.

2) Consider higher power density of the converter while high efficiency is still maintained. Push the switching frequency of isolated buck matrix-type rectifier to several hundred kHz (>300 kHz). This is possible by integrating the gate drivers and bidirectional MOSFET switches as a single module. With the single module, the stray inductance of devices and the parasitic node capacitances can be greatly reduced. Therefore, the turn-ON and turn-OFF switching losses are relatively decreased. Other way to increase the switching frequency of isolated buck matrix-type rectifier is using auxiliary switches to reduce the turn-OFF losses while the ZVS for turn-ON is still in effect. However, a special attention is required to that the auxiliary switches do not pose an additional switching loss. Especially, this approach is suitable for Si IGBT-based buck matrix-type rectifier where the converter suffers significantly from larger turn-OFF loss.

3) Consider bidirectional operation of the converter in DCM operation for low to medium power range while the soft-switching for switches of the rectifier is still in effect. Rectifier operates in DCM doesn't require output inductor which results in higher overall power density of the rectifier. In addition, there are not any large spikes on the secondary-side devices; therefore, lower-voltage devices with lower $R_{DS\text{-}on}$ can be selected.

Appendix A

Detailed ZVS Operation of "Type A" at Different Load Conditions

The switching loss is analyzed for sector I (a), which can also represent the loss in other sectors since there is no loss difference between sectors due to repetitive feature of PWM. As shown in Fig. 2-8, the three-phase converter can be redrawn as full-bridge DC-DC converter with "bridge x" and "bridge y" and the typical waveforms at different load conditions with the gating signals are shown in Fig. A-1. In one switching cycle, there are six transitions as shown in shaded area. As discussed in Chapter 2, ZVS operation of the rectifier is similar to the operation of FB-PS. Transition 1 and 4 are the leading edge transitions of v_p, where energy stored in L_{lk} is used to achieve ZVS. Two transitions 3 and 6 are the trailling edge of v_P, where the total energy stored in L_{lk} and L_o is used to achieve ZVS. Transition 2 and 5 are the transitions between two active vectors and ZVS is achieved in the similar way as the trailing edge transition. However, there is a non-ZVS turn-on during this transition which is independent with load condition.

a) Switching loss of transition 1

During transition 1, S_{22} and S_{24} are turned off at t_0 followed by S_{16} turn-on at t_1. S_{22} is turned off at zero voltage since it functions as synchronous rectification, therefore no losses created for this switch. S_{24} is turned off at full current and full voltage. The turn-off switching loss E_{off} is normally provided in datasheet. However, it cannot be directly used for loss calculation due to following reasons. E_{off} in datasheet is normally obtained by taking the integration of the product of the drain-to-source voltage V_{ds} and drain-to-source current I_{ds} of the switch in a double pulse test. It is important to note that the measured E_{off} overestimates the turn-off loss because it includes the energy stored in the output capacitance E_{oss} as discussed in [62]. Therefore, the charging energy E_{oss} has to be subtracted from the turn-OFF loss, if the turn-OFF loss is

calculated based on the E_{off} obtained from datasheet. In addition, the parasitic capacitances of the other device may help reduce the turn-off loss since the total equivalent capacitance across the switch is the sum of C_{oss} and the parasitic capacitances of the other device. Larger the total equivalent capacitance, lower the turn-off loss. However the effectiveness of this loss reduction is largely depending on the layout and device stray inductance. For simplicity, this factor is neglected in the loss calculation here. Finally the turn-off loss of S_{24}, which represents the turn-off loss of the leading edge transition, can be expressed as

$$E_{off\_lead} = E_{off}(V_{ds}) - E_{oss}(V_{ds}). \tag{A-1}$$

The drain-to-source voltage V_{ds} has the same magnitude as $v_{AB}(\theta)$ during sector I (a) and $v_{AC}(\theta)$ during sector I (b). Assuming a linear relationship between V_{ds} and E_{off_lead}, the averaged turn-off energy loss $E_{off\_lead\_avg}$ during sector I (a) or sector I (b) can be approximated as $E_{off\_lead}(V_{lead\_avg})$, where the V_{lead_avg} is the average voltage of V_{ds} for the leading edge during sector I (a) or sector I (b), and can be derived by

$$V_{lead\_avg} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} v_{AC}(\theta)d(\theta) = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} \sqrt{3}V_m \sin(\theta+\frac{\pi}{3})d(\theta) = \frac{3\sqrt{3}}{\pi}V_m \approx 1.65V_m. \tag{A-2}$$

Then the average of turn-off energy loss can be revised as

$$E_{off\_lead\_avg} = E_{off\_lead}(1.65V_m) = E_{off}(1.65V_m) - E_{oss}(1.65V_m). \tag{A-3}$$

However, when the converter operates at light load, the energy stored in L_{lk} is not sufficient to charge and discharge the output capacitances of MOSFET devices. Therefore, ZVS is partially lost. Then the residual voltage V_{res} has to be discharged by S_{16} which results in turn-on loss. The associated turn-on loss of S_{16} is the sum of discharging energy of C_{oss} of S_{16} and energy loss due to charging the parasitic capacitance C_{par} of other devices and it can be expressed as charging/discharging energy of the total equivalent capacitance $C_{eq.}$

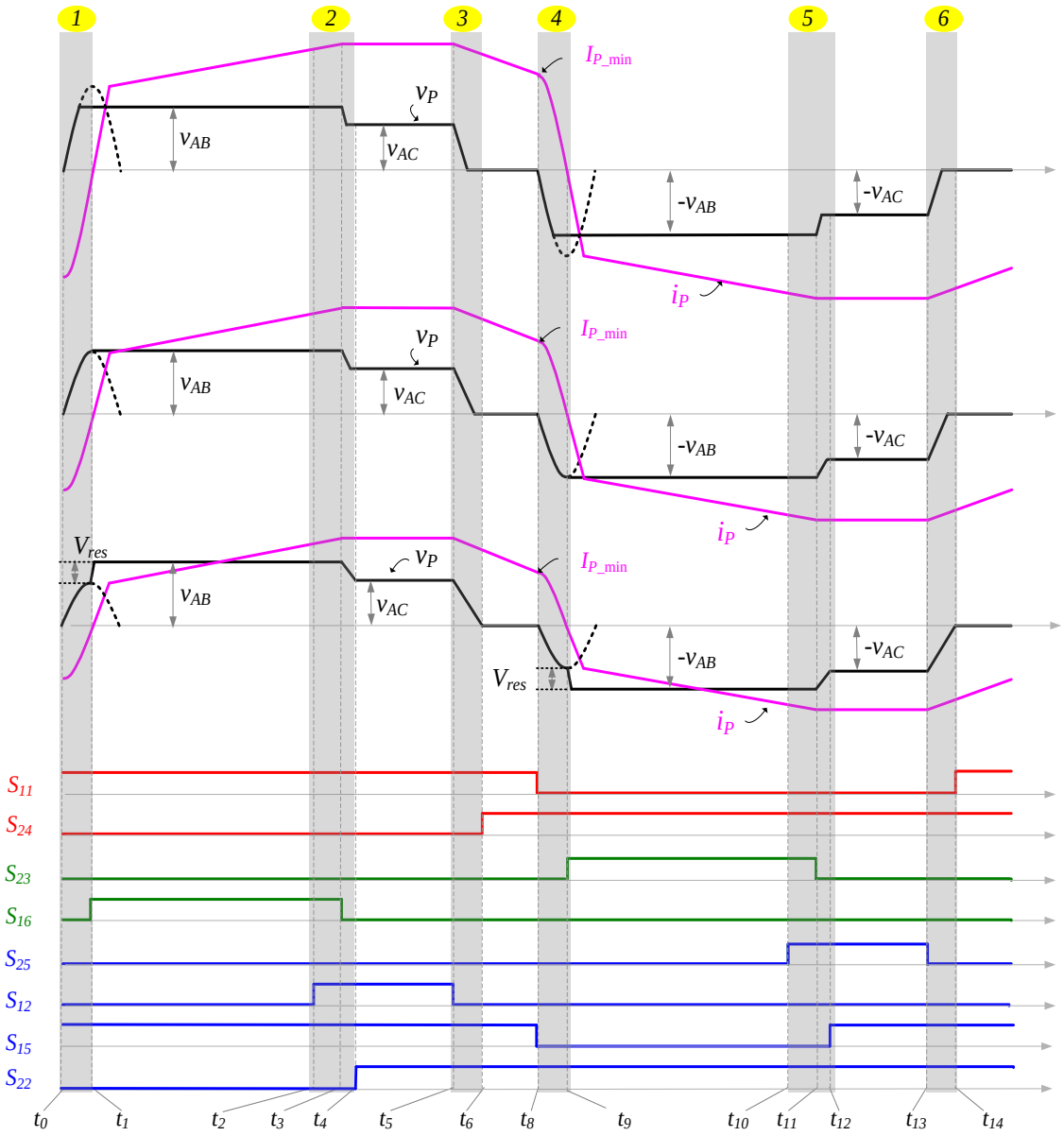


Fig. A-1 Typical waveforms and gate signals during sector I (a).

$$E_{on\_lead}(V_{res}) = \frac{1}{2}C_{oss}{V_{res}}^2 + \frac{1}{2}C_{par}{V_{res}}^2 + \frac{1}{2}C_{tr}{V_{res}}^2 = \frac{1}{2}C_{eq}{V_{res}}^2 \qquad \text{(A-4)}$$

It should be noted that (A-4) results in underestimated energy loss since the calculation is based on the energy-equivalent capacitance of C_{par}. For more accurate result, the capacitor

charge of C_{par} should be considered similar to [63]. However, this involves more complex calculations for three-phase isolated buck matrix-type rectifier due to the fact that C_{par} is not physically one capacitor and it comprises the capacitance of different branches having different voltages. For simplicity, the traditional method based on the energy-equivalent capacitance of all the capacitances is still used here, since they can be easily lumped into the total equivalent capacitance C_{eq}. The total equivalent capacitance C_{eq} for leading edge of the rectifier has been discussed in [54] and the resultant energy loss can be found from the E_{oss} versus the residual voltage V_{res} curve which is provided in the datasheet of device.The resonance between L_{lk} and C_{eq} provides a sinusoidal voltage across the capacitances that reaches a maximum at one fourth of the resonant period

$$\delta t_{\max} = \frac{T_{res}}{4} = \frac{\pi}{2}\sqrt{L_{lk}C_{eq}}\,, \tag{A-5}$$

where $C_{eq} = 5/2\,C_{oss} + C_{tr}$. Note, C_{tr} is the equivalent capacitance of transformer winding.

The dead-time between S_{16} and S_{24} is set at $\delta t_{\max}$ to ensure that all the energy stored in L_{lk} is available to charge/discharge the capacitances. The critical current requried in the primary side of the transformer to achieve ZVS for devices can be calculated from

$$\frac{1}{2}L_{lk}{I_{p\_crit}}^2 \geq \frac{1}{2}C_{eq}{V_{res}}^2 \tag{A-6}$$

For a given primary current I_p and if $I_p < I_{p\_crit}$, the turn on loss can also be calculated by

$$E_{on\_lead}(V_{res}) = \frac{1}{2}L_{lk}{I_{p\_crit}}^2 - \frac{1}{2}L_{lk}{I_p}^2. \tag{A-7}$$

b) Switching loss of transition 2

During transition 2, S_{12} is turned on at t_2 with non-ZVS. Since S_{12} is turn on at zero current, the associated turn-on loss is only due to discharging of the C_{oss} of S_{22} and S_{12} as shown in Fig. A-2. The resultant energy loss can be approximated by

$$E_{on\_non\_ZVS} = \frac{2C_{oss}V_{ds}^{\ 2}}{2} = 2E_{oss}(V_{ds}). \tag{A-8}$$

It should be noted that the voltage V_{ds} is independent with the load current but a function of θ and can be expressed as $(v_{AC}(\theta) - 1/2\, v_{AB}(\theta))$ during sector I (a) and $v_{AB}(\theta) - 1/2\, v_{AC}(\theta)$ during sector I (b). The average value of $E_{on\_non\_ZVS}$ can be approximated as

$$E_{on\_non\_ZVS\_avg} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} \frac{2C_{oss}(v_{AB}(\theta) - \frac{1}{2}v_{AC}(\theta))^2}{2} \approx 2E_{oss}(0.5V_m) \tag{A-9}$$

At t_3, S_{16} is turned off with full current. But the turn-off transition voltage is only the deference between $v_{AB}(\theta)$ and $v_{AC}(\theta)$ and the associated turn-off loss is also small. Since the turn-OFF transition voltage is $(v_{AB}(\theta) - v_{AC}(\theta))$ during sector I (a) and $(v_{AC}(\theta) - v_{AB}(\theta))$ during sector I (b), the average of the turn-off transition voltage can be derived as

$$V_{low\_avg} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} \sqrt{3}V_m(\sin(\theta + \frac{\pi}{3}) - \sin(\theta + \frac{2\pi}{3}))d\theta = \frac{6\sqrt{3}-9}{\pi}V_m \approx 0.443V_m \tag{A-10}$$

The resultant average loss of $E_{off\_low\_avg}$ during the entire sector can be approximated as

$$\begin{aligned} E_{off\_low\_avg} &= E_{off}(V_{low\_avg}) - E_{oss}(V_{low\_avg}) \\ &\approx E_{off}(0.443V_m) - E_{oss}(0.443V_m) = 0.268E_{off\_lead\_avg} \end{aligned} \tag{A-11}$$

At t_4, the synchronous rectification device S_{22} is turned on with ZVS.

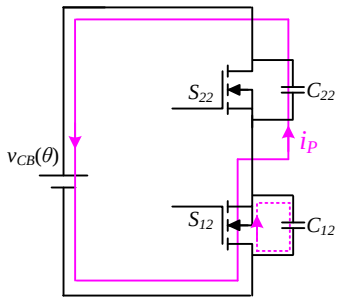


Fig. A-2 Equivalent circuit of non-ZVS turn-on. (note: $v_{CB}(\theta)$ is slow moving variable and can be assumed constant).

c) Switching loss of transition 3

During transition 3, S_{12} is turned off with full current and full voltage at t_5. The drain-to-source transition voltage V_{ds} has the same magnitude as $v_{AC}(\theta)$ during sector I (a) and $v_{AB}(\theta)$ during sector I (b). The average voltage of V_{ds} for trailing edge can be derived by

$$V_{trail\_avg} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} v_{AB}(\theta)d\theta = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} \sqrt{3}V_m \sin(\theta + \frac{2\pi}{3})d\theta = \frac{9-3\sqrt{3}}{\pi}V_m \approx 1.21V_m . \quad \text{(A-12)}$$

The associated average turn-off loss for this trailing edge transition can be expressed as

$$E_{off\_trail\_avg} \approx E_{off}(1.21V_m) - E_{oss}(1.21V_m) = 0.733E_{off\_lead\_avg} . \quad \text{(A-13)}$$

It should be noted that the turn-off current of the trailing edge transition is higher than that of leading edge transition since the primary current is at peak. At t_6, S_{24} is turned on with ZVS. It is important to note that adaptive dead time between t_5 and t_6 is applied to ensure ZVS operation of S_{24} at different load condition.

Switching losses for another half-cycle are the same as the first half-cycle. Similar loss analysis can be applied to eight-segment PWM scheme.

Appendix B

ZVS Range for Six-Segment and Eight-Segment PWM Schemes

As discussed above, the switches of rectifier can realize ZVS for trailing edge easily even at light load. However, the switches of rectifier lose ZVS during leading edge at lighter load.

The critical current I_{crit} required in the primary switch to achieve ZVS has been discussed in (A-6) of Appendix A. For a given load current I_o and with the consideration of the inductor ripple current, the available current through L_{lk} for the switching transition of the leading edge can be calculated by:

$$I_{P\_\min} = \frac{N_s}{N_p}\left[I_o + \frac{\Delta I_L}{2} - \frac{V_o}{L_f}(1-D)\frac{T_s}{2} \right]. \tag{B-1}$$

The load current range to achieve ZVS can be expressed as:

$$I_{P\_\min} > I_{crit} \tag{B-2}$$

or

$$I_o \geq \frac{N_p}{N_s} I_{crit} - \frac{\Delta I_L}{2} + \frac{V_o}{L_f}(1-D)\frac{T_s}{2}. \tag{B-3}$$

The selection of the series resonant inductance L_{lk} value can be done in two ways. One way is to choose L_{lk} to have a maximum 10% duty-cycle loss at full load current. Two equation (B-4) and (B-5) are used to calculate the maximum duty-cycle loss of rectifier with six-segment and eight-segment PWM schemes respectively at $\theta = 0$.

$$\Delta D_{total}(0) = \frac{8nI_oL_{lk}}{3V_mT_s} \tag{B-4}$$

$$\Delta D_{total}(0) = \frac{16nI_oL_{lk}}{3V_mT_s} \tag{B-5}$$

For a given m_a and with the consideration of duty-cycle loss, the total duty-cycle $D_{total}(\theta)$ attains its maximum at $\theta = 0$ for both PWM schemes in practical design. Therefore, the duty cycle loss at $\theta = 0$ is of the interest to determine the maximum available m_a which can be calculated by

$$m_a = D_{total}(0) - \Delta D_{total}(0). \tag{B-6}$$

For a maximum 10% duty loss at $\theta = 0$, the maximum available m_a will be 0.9 in order to satisfy the constraint $D_{total}(\theta) \le 1$.

Another way to select the resonant inductance value is based on ZVS range. With defined minimum load to achieve ZVS at $\theta = \pm\pi/6$, I_{crit} can be found from (B-3), and then L_{lk} can be calculated from (A-6).

When the rectifier is designed to provide a wide ZVS range, the loss of duty-cycle $\Delta D_{total}(0)$ is relatively large, which has to be compensated by increase in the transformer turns ratio, *n.* This increases the current in the primary, and leads to reduction in efficiency at higher load. On the other hand, if the ZVS range is narrow, and the ZVS property is lost with relatively high currents in the primary, the efficiency will suffer at light load. In this design the ZVS is retained from 40% to full load current with 10% duty-cycle loss for six-segment PWM scheme.

It should be noted that L_{lk} in eight-segment PWM should be less than half of the value of L_{lk} in six-segment PWM in order to maintain the same duty cycle loss at $\theta = 0$ as stated by (B-4) and (B-5).

Appendix C

Test-Setup for Experimental Verification

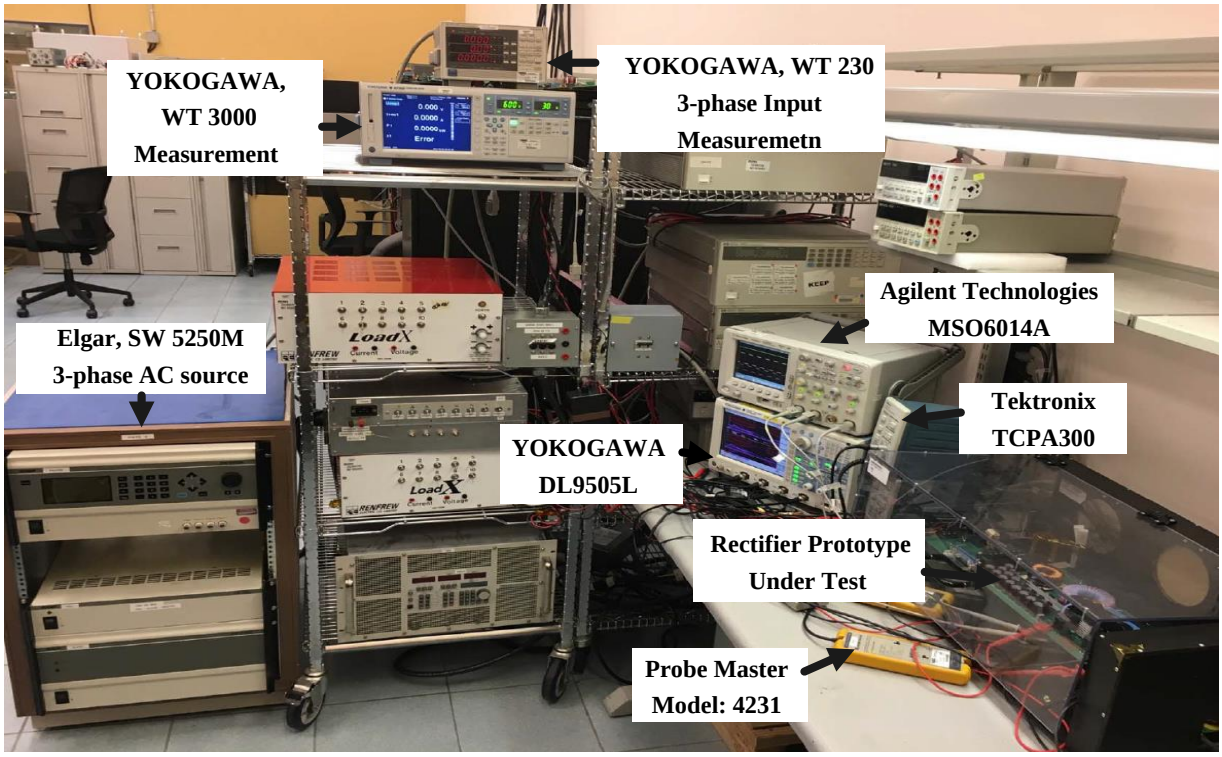


Fig. C-1 Experimental test setup with list of equipment.

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