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DIRECT VOLTAGE CONTROL FOR STAND-ALONE WIND ENERGY CONVERSION SYSTEMS WITH ENERGY STORAGE

by

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A thesis

presented to Ryerson University

in partial fulfillment of the

requirements for the degree of

Master of Applied Science

in the Program of

Electrical and Computer Engineering

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ABSTRACT

Direct Voltage Control for Stand-alone Wind Energy Conversion Systems with Energy Storage

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Electrical and Computer Engineering

Ryerson University

Toronto 2008

A control method for the stand-alone wind power generation system with induction generator and energy storage devices is proposed in this thesis. A fixed-speed self-excited induction generator is directly connected to the standalone power system, while battery powered energy storage devices are employed to balance the system power flow. A DC-AC power converter is connected between the energy storage device and the standalone power system, which maintains the voltage and frequency constant. Direct voltage control with current limits is developed for the converter with dynamic fast response. Mathematical models are developed to analysis the system performance as well as to design the lead-lag regulators in the control system. The proposed system is verified in the simulation and experiment.

ACKNOWLEDGMENTS

I wish to express my deep gratitude to my supervisor, Professor Dewei Xu for his support and the knowledge he shared during my graduate studies at Ryerson University.

I am grateful to Professor Bin Wu, Professor Richard Cheung, Dr. Yongqiang Lang, and all fellow students at LEDAR for their useful discussions on my research.

I also wish to share my achievements with my families and my wife Wei Li. I am very grateful for her understanding and support.

TABLE OF CONTENTS

CHA	PTER	1 INTRODUCTION	1
1.1	Win	d Energy Conversion System	1
1.2	Stan	nd-alone Wind Energy Conversion System	4
1.3	Mot	ivation and Objective	7
1.4	The	sis Outline	8
СНА	PTER	2 MODEL DEVELOPMENT FOR THE STANDALONE WECS	5 10
2.1	Intr	oduction	10
2.2	Win	d Turbine Characteristic	11
2.3	Indu	ıction Generator Model	12
2.4	Indu	ıctive Load and Self-Excitation Capacitor Model	15
2.5	Ene	rgy Storage System Model	15
2.6	Stan	dalone WECS Model	16
2.7	Sma	ll Signal Model	17
2.8	Con	clusions	20
СНА	PTER	3 CONTROL OF STANDALONE WECS	21
3.1	Intr	oduction	21
3.2	Dire	ct Voltage Control	22
	3.2.1	Voltage and Frequency Control	22
	3.2.2	Direct Voltage Controller Design	23
3.3	Con	clusions	28
СНА	PTER	4 SIMULATION AND EXPERIMENTAL RESULTS	29
4.1	Intro	oduction	29
4.2	Sim	ulation Model	30
4.3	Sim	ulation Results	32
	4.3.1	Non-ESS Stand Alone Wind Power Generation System	32
	4.3.2	Simulation Results with ESS	33
4.4	Exp	erimental Setup	37
4.5	Exn	erimental Results and Analysis	40

	4.5.1	Resistive Load Test	40
	4.5.2	Inductive Load Test	44
4.6	Con	clusions	48
СНА	PTER	5 CONCLUSIONS	49
5.1	Con	iclusions	49
5.2	Maj	or Contributions	50
5.3	Fur	ther Research Works	50
REF	EREN	CES	52
APP	ENDIC	CES	55
Ap	pendix	A Simulation Models	55
Ap	pendix	B System Parameters	56
Ap	pendix	C Code for Bode Plots	57
	_	D DSP Program Code	

LIST OF TABLES

Table 3-1: Parameters of the Lab Prototype System	. 25
Table 3-2: Parameters of lead-lag Controller	. 27
Table 4-1: System parameters of prototypes system	. 31
Table B-1 Parameters of DC Motor	. 56
Table B-2: System Parameters of Prototypes System	. 56

LIST OF FIGURES

Figure 1-1: Typical diagram of wind energy conversion systems	2
Figure 1-2: Constant-speed wind energy conversion systems	2
Figure 1-3: Typical configurations of variable speed wind energy conversion systems	3
Figure 1-4: Schematic of general wind-diesel system	5
Figure 1-5: Proposed wind energy conversion system	8
Figure 2-1: Proposed wind energy conversion system	10
Figure 2-2: Variables in three-phase (abc) stationary frame and two-phase (dq) synchronous frame	13
Figure 2-3: Induction generator equivalent circuits under synchronous reference frame	14
Figure 2-4: Energy storage system circuit	16
Figure 2-5: d-q Equivalent circuits in synchronous reference frame	17
Figure 2-6: Small signal model for d-q equivalent circuits in synchronous reference frame	20
Figure 3-1: Control block diagram of the whole system	21
Figure 3-2: Block diagram using transfer functions	22
Figure 3-3: System blocks model in S- domain	24
Figure 3-4: Bode plots of uncompensated loop	25
Figure 3-5: Bode plots of uncompensated loop with different loads	26
Figure 3-6: Bode plot of compensated loop gain	27
Figure 4-1: Block diagram of experimental set-up	29
Figure 4-2: System models of proposed WECS	
Figure 4-3: Direct voltage controller model	31
Figure 4-4: Wind power generation system without ESS	32
Figure 4-5: System voltage and frequency without ESS	32
Figure 4-6: Local bus voltage and frequency during load step change (with R Load) in Simulation	33
Figure 4-7: d-q axis inverter voltage during load step change (with R Load) in Simulation	34
Figure 4-8: d-q axis inverter current during load step change (with R Load) in Simulation	34
Figure 4-9: Current waveforms during load step change (with R load) in simulation	35
Figure 4-10: Voltage and frequency during load step change (with RL load) in simulation	36
Figure 4-11: Currents waveforms during load step change (with RL load) in simulation	36
Figure 4-12: d-q axis inverter voltages during load step change (with RL Load) in Simulation	37
Figure 4-13: d-q axis inverter currents during load step change (with RL Load) in Simulation	37
Figure 4-14: Experimental setup	38

Figure 4-15: DSP controller board	39
Figure 4-16: Steady-State waveforms with resistive load	41
Figure 4-17: Transient waveforms of local bus voltage and load current during load step change	42
Figure 4-18: Transient waveforms of generator and converter currents during load step change (with l	R
Load)	43
Figure 4-19: d-q axis Inverter side current during load step change (with R Load)	44
Figure 4-20: Steady-State voltage and current waveforms with RL load	45
Figure 4-21: Transient waveforms of local bus voltage and load current during load step change (with	ı RL
load)	46
Figure 4-22: Transient waveforms of currents of generator and inverter during load step change (with	RL
load)	46
Figure 4-23: d-q axis Inverter side current and voltage during step load change (with RL Load)	47
Figure 4-24: d-q axis Inverter current during step load change with compensation (with R-L Load)	47
Figure A-1: Simulink model of WECS	55
Figure A-2: Direct voltage controller model	55

LIST OF PRINCIPAL SYMBOLS

ρ	Air density (kg/m³)
A	Turbine swept area (m ²)
\mathcal{V}_{wind}	Wind velocity (m/s)
λ	Tip speed ratio of the blade tip speed to wind speed
β	Blade pitch angle (deg)
P_m	Mechanical output power of the turbine (W)
ω_e	Angular electrical speed
ω_r	Angular rotor speed
T_e	Electrical torque of the induction machine
$i_{ds}(t), i_{qs}(t)$	Stator side current of induction generator in d-q reference frame
$i_{dr}(t), i_{qr}(t)$	Rotor side current of induction generator in d-q reference frame
$v_{ds}(t), v_{qs}(t)$	Local bus terminal voltage in d-q reference frame
$v_{dr}(t), v_{qr}(t)$	Rotor side voltage of induction generator in d-q reference frame
$i_{Cd}(t), i_{Cq}(t)$	Self-excited capacitor current in d-q reference frame
$v_{ld}(t), v_{lq}(t)$	Load voltage in d-q reference frame
$i_{1d}(t), i_{1q}(t)$	Load current in d-q reference frame
v(t)	Converter output voltage
i(t)	Converter output current
E_s	Ideal voltage source representing the energy storage devices

L	Inductance of converter side filter	
C	C Capacitance of self-excited capaciton	
$f_{\it ref}$	f_{ref} Reference frequency for the local bus	
v_{ref}	Reference voltage for the local bus	
v	Converter-side feedback voltage	
T_s, f_s	Sampling period, sampling frequency	
G_{c0}	Gain of the lead-lag regulator	
T_i, T_z, T_p	Time constant of lead-lag regulator	
$K_{\scriptscriptstyle PWM}$	Gain of the PWM converter	
m_a	Modulation index of the converter	

Chapter 1 Introduction

Currently the world's energy consumption is greatly dependent on exhaustible fossil fuel, which is also main source contributing the green house gas and pollution to the environment. In this perspective, utilization of renewable energy, such as wind and solar energy, has gained considerable momentum since the oil crises of the 1970s. Wind power, as one of the alternative energy options, is gaining increasing significance throughout the world. Wind energy is non-depleting, site-dependent, non-polluting, becoming the most promising energy source for the future. Large and grid tired wind energy conversion system has been widely installed in many countries, in the effort to minimize the dependence on fossil based non-renewable fuels [1]. Wind energy has experienced accelerated expansion in recent years and its global production is predicted to grow from 60,000 MW in 2005 to 300,000 MW in 2015 [2].

1.1 Wind Energy Conversion System

A basic wind energy conversion system (WECS) consists of a wind turbine with tower, gearbox, generator, power converter and control system, as shown in Figure 1-1[3]. There are two types of wind turbines used in practice: vertical wind turbine and horizontal wind turbine according to the rotating of the blades. Most modern wind turbines are horizontal type with two or three blades due to higher efficiency and higher power capability.

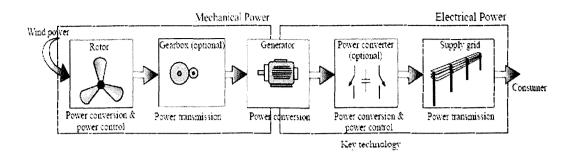


Figure 1-1: Typical diagram of wind energy conversion systems

WECS can also be classified into two types of the systems according to its operation: constant speed or variable speed operation systems. Fix speed WECS operate at a nearly fix speed while variable speed system adjusts its rotor speed according to different wind speed. Generally variable speed system extracts more wind energy (10-15%) than the fixed speed system.

A constant speed WECS usually contains a squirrel cage induction generator, as shown in Figure 1-2. Gearbox is necessary for the coupling of the low speed wind turbine and the high speed induction generator. SCR controlled starter between the generator and the grid aims at reducing the inrush current during connection to the grid. In normal operation, induction generator absorbs reactive power. Capacitor bank provides the required reactive power for generator. If enough capacitor is provided, the generator can be self-excited, which is useful when grid is not available. The speed of the generator varies little when the power changes. Thus the speed is almost constant. Constant speed WECS is usually easier to built up and cost less than the variable speed WECS. But because of the fixed speed, the overall energy conversion efficiency is not high.

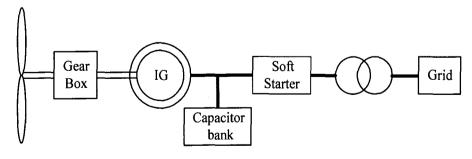
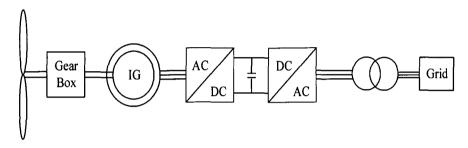
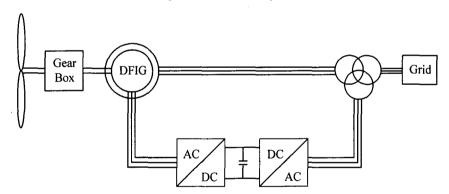


Figure 1-2: Constant-speed wind energy conversion systems

Variable speed configurations allow the rotor to rotate at required speed by introducing power electronic converters between the generator and the grid. Wind turbine system can operate at its optimum tip-speed ratio[4]. Thus more energy can be converted into electricity. Double-fed induction generators (DFIG), wound field synchronous generators and permanent magnet synchronous generators are three typical generators used in high power WECS. For medium and small power wind turbines, permanent magnet generators and squirrel cage induction generators are more often used because of their reliability and cost effectiveness. The typical configurations of variable speed WECS are shown in Figure 1-3[5].



(a) Inductor generator with full power converter



(b) Doubly-fed induction generator with fractional power converter

Figure 1-3: Typical configurations of variable speed wind energy conversion systems

Power converters are used to control the power flow between the wind turbine and grid when the variable frequency and variable voltage energy from generator is fed to the grid with fixed frequency and voltage. Most modern power converters are forced commutated PWM converters to provide a fixed voltage and frequency output with a high power capability. Both voltage source voltage controlled converters and voltage source current controlled converters have been

applied in wind energy applications. For certain high power wind turbines, effective power flow control can be achieved where real power and reactive power are independently controlled.

Most of the large wind energy conversion systems are grid connected. And many turbines are installed in a utility level wind farm with several hundred MW installed capacity. The prediction and power fluctuation are the main problem for the integration of wind farm to the grid. Many research efforts have been to solve these problems.

WECS sometimes can be used in the standalone power system in remote area where grid connection is not available. Hybrid system with battery, diesel generator and wind turbine/generator are connected together to provide a quality power to the load. The systems are often used in the small community; the capacity varies from several kilo-watts to hundreds of kilo-watt.

1.2 Stand-alone Wind Energy Conversion System

Many remote communities around the world cannot be physically or economically connected to an electric power grid. The electricity demand in these areas is conventionally supplied by small isolated diesel plants. These have the advantage of being able to deliver the required power whenever it is necessary. However, they also suffer from a number of drawbacks. Diesel generator engines are inherently noisy and expensive to run, especially for consumers in rural areas where fuel delivery costs may be high. In addition, small consumers always have a low load factor; this in turn reduces the overall efficiency and increases percentage maintenance costs. Considerable fuel savings can be achieved by integrating renewable sources such as wind and/or solar energy with existing diesel plants.

However, many off-grid places are in regions of high wind energy potential. Wind energy is one of the most important and promising forms of renewable energy sources. Its use is becoming more and more popular nowadays. This is because the price of fossil fuels is continuously increasing and the wind energy is a clean and inexhaustible energy source. But due to great varia-

tion in wind speed which occurs from season to season, it can not be used as an autonomous source of generation. Hence, it is necessary to explore possibilities of combining a wind generator with the diesel generator in order to reduce the running cost per kWh and to increase the reliability of the power supply[6].

A schematic diagram of a wind-diesel system is shown in Fig. 1-4. A classic wind-diesel power system consists of the following components: one or more wind turbines, one or more diesel generators, consumer load, an additional controllable dump load, energy storage system and control unit[7]. In order to save the fuels cost, it is desirable to shut off the diesel generator(s) whenever possible. Energy storage system is used to compensate the fluctuation in the system coming from the wind fluctuation and to provide the short period energy during the diesel generator on or off periods. For the excess power from wind turbines, dump load will be used to resolve this problem.

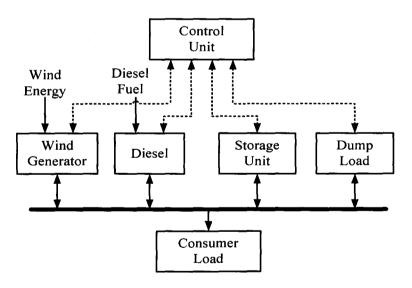


Figure 1-4: Schematic of general wind-diesel system

From the configuration of wind-diesel power system, it obviously shows that wind-diesel hybrid system has its own problems. Power fluctuation issue is one of the most important issues. It is well known that the mechanical shaft power obtained from a wind turbine may be approximated by [8]:

$$P_{m} = \frac{1}{2} \rho \pi R^{2} C_{p}(\lambda, \beta) V^{3}$$

$$\tag{1-1}$$

where ρ is the air density, $C_p(\lambda, \beta)$ is the power coefficient, R is the blade radius, β is the blade pitch angle, λ is the tip speed ratio and V is the effective wind speed respectively.

Equation (1-1) shows that small variations in the wind speed produce large changes in the captured power. These power fluctuations transferred to the output by the conversion system, including generator, power converter if existed, especially when the system is a fix speed system. For variable speed systems, part of the power fluctuation is absorbed as kinetic energy in the turbine. However, even for variable speed systems, power fluctuations can still be a serious problem if the generator is feeding a weak grid or a stand-alone load. For these applications, the wind turbine is augmented by an additional source, usually a diesel generator. In such hybrid systems, wind speed fluctuations not only produce fluctuations in the generator output voltage, but also an unacceptable number of start/stop cycles of the diesel generator if a temporary energy buffer is not available.

In [11-14], flywheel energy storage device is used as energy storage system to smooth the fluctuations in the wind-diesel system when the energy storage system is needed. Papers [11, 12] suggest that use vector control to control the induction machine to drive the flywheel system. [13] also shows a new sensorless field oriented control method to drive the induction machine. Almost all the control methods are based on the front-end converter. There are other papers [15-17] using battery bank or super-capacitor as the energy storage devices. The different kinds of energy storage device have its own advantages and disadvantages. Battery is a cost effective solution which is widely used in the energy storage system. But it has a high maintenance cost and low cycle life. Super-capacitor is a new energy storage device with much higher life but the capacity is low.

In [9, 10], sensorless control for double-fed induction generator in stand-alone system are presented. For the Doubly-fed induction generator, sensorless operation is desirable because the use of a position encoder has several drawbacks in term of robustness, cost, cabling and mainte-

nance. Most of the sensorless control methods are all based on the principle of rotor position observers using the rotor current error. For DFIG, itself can regulate the output voltage and the frequency regardless of the load and rotational speed. Batteries, as the energy storage devices, are integrated into the dc link of back-to-back converter for the DFIG, which enhance the system performance by expanding the operation range.

1.3 Motivation and Objective

Based on the configuration of the stand-alone system presented in the previous sections, the typical system consists of wind turbine, diesel engine, energy storage system and control part. In this project, the induction generator is used to be the wind turbine generator. For a small scale wind-diesel wind power system, squirrel cage induction generator is a better choice when cost and reliability are the first two considerations. As long as the energy storage devices are always need, a fixed-speed self-excited induction generator has its own advantages including cost, robustness and reliability can be used in the stand-alone system. The fluctuation in the power from the wind can be smoothed by the energy storage system with an appropriate controller.

As presented in the former section, many researches have been done on doubly-fed induction generator control. It usually uses a fractional size back-to-back converter to control the active power and reactive power to keep the constant voltage and frequency. And the controller usually contains two control loops to regulate the voltage and frequency. For a doubly-fed generator based system, the control of system voltage and frequency are very complicated since it is coupled by the control of induction generator's speed and torque.

Most of the control strategies for power balance controlling in the stand-alone system contain two cascaded loops: voltage loop and frequency loop, which based on the assumption that frequency loop is usually slower than the voltage loop. In these control systems, the dynamic response of grid voltage sometimes is not satisfied when the load is light.

In this thesis, the induction generator with self-excitation capacitor is directly connected to the standalone power system, as shown in Fig.1-5. The energy storage system (ESS) is employed to maintain the system frequency as well as voltage at collect bus. It supplies or absorbs the fractional power of the system, and keeps the system power flow balanced. When the wind energy is not enough for a long period, the back-up generators including diesel generator should be turned on to provide the rest of the energy. The renewable energy converters in the system are maintained at highest efficiency with the employed ESS, which reduces the energy consumption from diesel generators, reduces system operation cost as well as the greenhouse gas emission and pollution to the environment.

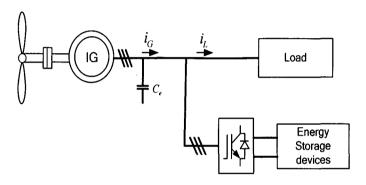


Figure 1-5: Proposed wind energy conversion system

Therefore, the main objectives of the thesis are:

- 1. Design a suitable controller for converter, which smooth the power fluctuation of wind energy conversion system.
- 2. Develop mathematical models for the system with induction generator and energy storage converter. This model will be used in the controller design.
- 3. Conduct variety of experiments to verify the performance of the developed control system.

1.4 Thesis Outline

This thesis is organized to provide the detailed information about the research work on standalone wind energy conversion system with induction generator and energy storage devices in five chapters. This chapter, chapter 1 presents the background of wind energy conversion systems, including the configurations, operation and grid connection. Standalone power system with integrated wind energy is introduced. Research motivation is discussed in this chapter.

Chapter 2 presents the development of mathematical model for each component in the standalone system with wind turbine and energy storage devices. The model is developed in the d-q reference frame. Finally the whole system model is developed.

Chapter 3 presents the direct voltage controller design for standalone WECS. Small signal model of wind energy power system is developed, followed by theoretical analysis of the control scheme with dump load and current protection. The diagram of controller scheme is discussed.

Chapter 4 shows all the simulation models for different components in Matlab/Simmulink. The simulation results are also given in this chapter. Experimental results are provided to compare with simulation.

Chapter 5 presents the conclusions of the thesis, major contributions and future work are discussed later.

All other relevant supporting materials are attached in appendices.

Chapter 2 Model Development for the Standalone WECS

2.1 Introduction

The diagram of the proposed wind energy conversion system is shown in Fig. 2-1. The electrical part consists of the induction generator with self-excitation capacitors, the energy storage devices with power converter, consumer load and dump load.

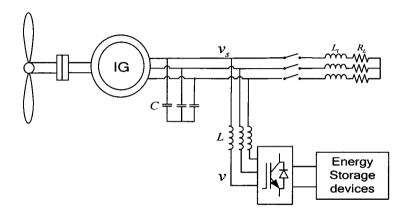


Figure 2-1: Proposed wind energy conversion system

In the system, self-excitation capacitors are needed to provide sufficient reactive power to the induction generator, which reduce the reactive power consumption from the power converter. It is assumed that the wind turbine is properly selected, which can provide most of the energy to the load. Thus the power converter and energy storage devices only provide fractional power to maintain the power balance between generator and load. In the system, the dump load will be connected to absorb these extra powers from induction generator. The dump load can be represented additional resistor. In the practical industry application, most of the energy storage devices usually can only store or supply limited power. So a back-up generator is essentially re-

quired if continuous power flow is required. In this thesis, energy storage devices are treated as an ideal voltage source. Different characteristics of the batteries are not the main research focus. Battery management is also not a consideration in this thesis.

Power fluctuation in the standalone system is one of the most common problems. Before deriving a solution for the controller, it is imperative to produce a comprehensive mathematical model of the whole electrical system that can be used in the controller design. The following sections provide different part mathematical models and the whole system model is presented in the last section.

2.2 Wind Turbine Characteristic

Generally, the wind turbine systems can be classified according to their aerodynamic configuration, transmission design and their operational speed range. Further classification can be performed based on the power output, the generator types, grid connection, etc.

The aerodynamic configuration divides the wind turbines in two main categories: the horizontal axis wind turbine (HAWT) and vertical axis wind turbine (VAWT). Due to reasons of mechanical resonance, efficiency and size more than 95 percent of the currently operating wind turbine designs are HAWT. The choice of this configuration has one major disadvantage that the main components of the energy conversion system such as generator, gearbox, pitch control mechanism, the power converter and the grid-interface device, have to be located in the nacelle of the turbine. This leads to the increased demands on the stability, strength and cost of the support structure.

Regardless of the aerodynamic configuration of the wind turbine, its absolute maximum power extraction efficiency is restricted by the Betz limit of 59.3 percent.

The mechanical power extracted from the wind is mainly governed by three quantities namely, the area swept by rotor blades, the upstream wind velocity and rotor co-efficient.

$$P_{m} = \frac{1}{2} \rho \pi R^{2} C_{p}(\lambda, \beta) V^{3}$$

$$\tag{2-1}$$

Cp, the power coefficient of rotor, itself is a function of tip speed ratio and pitch angle. A typical coefficient of the wind turbine is given at 0° pitch angle. The optimal Cp is only possible at certain speed ratio. Yet, it is not always possible to maintain zero blade pitch, because it would create unwanted output fluctuations as well as greatly increase the electrical and mechanical load on the whole system when the wind is too strong. In order to partially cure this problem, the pitch control mechanisms (or stall control) are installed to regulate the position of the blades and maintain the highest possible power the system can deliver.

2.3 Induction Generator Model

The use of reference frame theory can simplify the analysis of electric machines and also provides a powerful tool for the digital implementation of sophisticated control schemes. The synchronous reference frame is one of the most commonly used in the research and application. The transformation of the three-phase (abc-axis) variables of an induction motor to the equivalent two-phase (dq-axis) variables can be performed by[19].

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos(\theta - 2\pi/3) & \cos(\theta - 4\pi/3) \\ -\sin \theta & -\sin(\theta - 2\pi/3) & -\sin(\theta - 4\pi/3) \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}$$
(2-2)

where x represents either current, voltage, or flux linkage, and θ is the angular displacement between the a-axis and d-axis of the three-phase and two-phase reference frames as shown in Fig. 2-2. The three-phase variables, x_a , x_b and x_c , are in the stationary reference frame which does not rotate in space whereas the two-phase variables, x_d and x_q , are in the synchronous reference frame whose direct (d) and quadrature (q) axes rotate in space at the synchronous speed ω_e . Note that ω_e is the angular electrical speed of the rotating magnetic field of the motor, given by

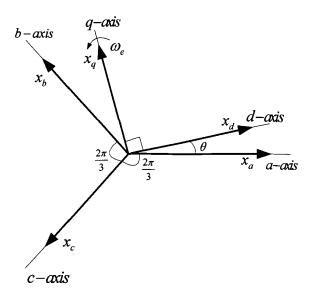


Figure 2-2: Variables in three-phase (abc) stationary frame and two-phase (dq) synchronous frame

$$\omega_e = 2\pi f_s \tag{2-3}$$

where f_s is the frequency of the stator variables. The angle θ can be found from

$$\theta(t) = \int_0^t \omega_e(t)dt + \theta_0 \tag{2-4}$$

In order to model the induction generator, the d-q equivalent circuit of induction machine is obtained. Refer all the variables of rotor side to stator side, following equations can be obtained by using Clark-Park transformation. The corresponding equivalent circuits are shown in Fig. 2-3.

$$v_{ds} = -R_s i_{ds} + \frac{d\psi_{ds}}{dt} - \omega_e \psi_{qs}$$
 (2-5)

$$v_{qs} = -R_s i_{qs} + \frac{d\psi_{qs}}{dt} + \omega_e \psi_{ds}$$
 (2-6)

Where:

$$\psi_{qs} = -L_{ls}i_{qs} - L_m(i_{qr} + i_{qs})$$

$$\psi_{ds} = -L_{ls}i_{ds} - L_m(i_{dr} + i_{ds})$$

Since the rotor rotates at speed ω_r , the d-q axes rotate at the speed $\omega_e - \omega_r$ referred to the rotor frame. Therefore, the equations are:

$$v_{dr} = 0 = -R_r i_{dr} + \frac{d\psi_{dr}}{dt} - (\omega_e - \omega_r)\psi_{qr}$$
(2-7)

$$v_{qr} = 0 = -R_r i_{qr} + \frac{d\psi_{qr}}{dt} + (\omega_e - \omega_r)\psi_{dr}$$
 (2-8)

Where:

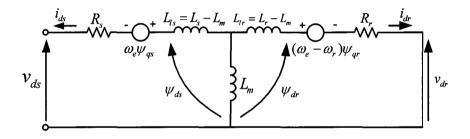
$$\psi_{dr} = -L_{lr}i_{dr} - L_m(i_{dr} + i_{ds})$$

$$\psi_{ar} = -L_{lr}i_{ar} - L_{m}(i_{ar} + i_{as})$$

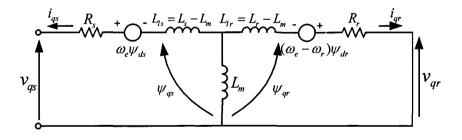
The rotor speed ω_r in equations (2-7) and (2-8) usually is treated as a constant during the electrical transient. The electrical torque of the induction machine is given by

$$T_e = \frac{3P}{2L_m} (i_{ds} i_{qr} - i_{qs} i_{dr})$$
 (2-9)

Where P is the number of the poles.



(a) d-axis equivalent circuit



(b) q-axis equivalent circuit

Figure 2-3: Induction generator equivalent circuits under synchronous reference frame

2.4 Inductive Load and Self-Excitation Capacitor Model

Capacitor is necessary in the standalone WECS. The capacitor can provide reactive power to the induction generator. The equations (2-12) and (2-13) represent the relation between capacitor currents and voltages in synchronous reference frame. For the load current and voltage, it has

$$i_s = i_C + i_I + i (2-10)$$

$$v_l = Ri_l + \omega L_l i_l \tag{2-11}$$

Through the Clark-Park transformation, the d-q synchronous reference frame equations can be obtained:

$$i_{ds} = i_{Cd} + i_{ld} + i_d + C\omega_e v_{qs}, \quad i_{qs} = i_{Cq} + i_{lq} + i_q - C\omega_e v_{ds}$$
 (2-12)

$$\frac{d}{dt}v_{ds} = (\frac{1}{C}i_{ds} - \frac{1}{C}i_{ld} - \frac{1}{C}i_{d}) + \omega_{e}v_{qs}, \quad \frac{d}{dt}v_{qs} = (\frac{1}{C}i_{qs} - \frac{1}{C}i_{lq} - \frac{1}{C}i_{q}) - \omega_{e}v_{ds}$$
 (2-13)

Equations (2-14) shows the load voltages and currents in reference frame, assume of inductive load.

$$v_{ld} = R_L i_{ld} + L_l \frac{d}{dt} i_{ld} - \omega_e i_{lq}, \quad v_{lq} = R_L i_{lq} + L_l \frac{d}{dt} i_{lq} + \omega_e i_{ld}$$
 (2-14)

2.5 Energy Storage System Model

The storage system consists of a bi-directional PWM voltage source based converter, grid connection inductors and batteries. In this thesis, the battery's characteristic is neglected and ideal voltage source *Es* is adopted. Since battery power management is another complex topic, the research here focuses on the converter control to maintain a smooth power flow to the load. The differential equations can be established for the energy storage system.

$$v(t) = dE_a \tag{2-15}$$

$$\frac{di(t)}{dt} = \frac{1}{I} [v(t) - Ri(t) - v_s(t)]$$
 (2-16)

In Eq. 2-15 and 2-16, d is the duty ratio, $v(t) = \begin{bmatrix} v_a(t) & v_b(t) & v_c(t) \end{bmatrix}^T$ is converter output phase voltage. $v_s(t) = \begin{bmatrix} v_{as}(t) & v_{bs}(t) & v_{cs}(t) \end{bmatrix}^T$ is terminal (or bus) voltage and $i(t) = \begin{bmatrix} i_a(t) & i_b(t) & i_c(t) \end{bmatrix}^T$ is converter side current.

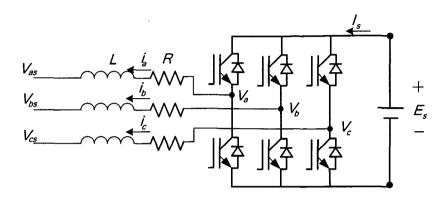


Figure 2-4: Energy storage system circuit

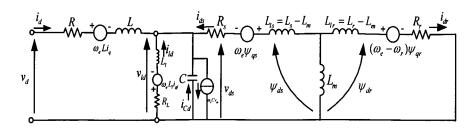
The above equations can be transferred to selected dq reference frame by applying parkclark transformation. Assume that the three-phase system is balanced three-phase three-wire system, in which zero components can be removed. The two differential equations can be written in Eq. (2-17) and (2-18), where ω is the rotating speed of reference frame.

$$\frac{di_d(t)}{dt} = \frac{1}{L} [v_d(t) - Ri_d(t) - v_{ds}(t)] + \omega_e i_q(t)$$
 (2-17)

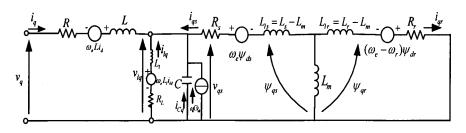
$$\frac{di_{q}(t)}{dt} = \frac{1}{L} [v_{q}(t) - Ri_{q}(t) - v_{qs}(t)] - \omega_{e}i_{d}(t)$$
 (2-18)

2.6 Standalone WECS Model

The completed dynamic model can be presented based on the previous analysis. According to the set of 10 differential equations corresponding to variables i_{ds} , i_{qs} , i_{dr} , i_{qr} , v_{ld} , v_{lq} , i_{ld} , i_{lq} , i_{d} , i_{q} , the d-q equivalent circuit at synchronously rotating frame can be obtained, as shown in figure 2-5.



(a) d-axis equivalent circuit



(b) q-axis equivalent circuit

Figure 2-5: d-q Equivalent circuits in synchronous reference frame

2.7 Small Signal Model

Eq. (2-5—2-18) present the whole system mathematical model. Base on that, the whole system small signal models can be obtained by introducing the small variation.

To construct a small-signal ac model at a quiescent operation point, assume that system currents and voltages are equal to some given steady state values I and V (quiescent operating point), plus superimposed small ac variations \hat{i} and \hat{v} . Hence, we have

$$v_d = V_d + \hat{v_d}$$
; $v_{ds} = V_{ds} + \hat{v_{ds}}$; $v_{ld} = V_{ld} + \hat{v_{ld}}$; $i_d = I_d + \hat{i_d}$; $i_{ds} = I_{ds} + \hat{i_{ds}}$; $i_{ld} = I_{ld} + \hat{i_{ld}}$ (2-19)

$$v_q = V_q + \hat{v_q}$$
; $v_{qs} = V_{qs} + \hat{v_{qs}}$; $v_{lq} = V_{lq} + \hat{v_{lq}}$; $i_q = I_q + \hat{i_q}$; $i_{qs} = I_{qs} + \hat{i_{qs}}$; $i_{lq} = I_{lq} + \hat{i_{lq}}$ (2-20)

$$\omega_e = \Omega_e + \hat{\omega_e}; \ \omega_r = \Omega_r + \hat{\omega_r}$$
 (2-21)

With the assumptions that the ac variations are small in magnitude compared to the steady values, then the equations can be simplified. This is done by substituting Eqs. (2-20) and (2-21) into Eqs. (2-5) and (2-6).

$$V_{ds} + v_{ds}^{\hat{}} = -R_s (I_{ds} + i_{ds}^{\hat{}}) + \frac{d(\psi_{ds} + \psi_{ds}^{\hat{}})}{dt} - (\Omega_e + \omega_e^{\hat{}})(\psi_{qs} + \psi_{qs}^{\hat{}})$$
 (2-23)

$$V_{qs} + \hat{v_{qs}} = -R_s (I_{qs} + \hat{i_{qs}}) + \frac{d(\psi_{qs} + \psi_{qs})}{dt} + (\Omega_e + \hat{\omega_e})(\psi_{ds} + \psi_{ds})$$
(2-24)

By cancelling the steady-state terms and neglecting high order ac terms in Eqs. (2-23) and (2-24), the first-order ac terms on both side of the equations are left. Hence,

$$\hat{v_{ds}} = -R_s \, \hat{i_{ds}} + \frac{d \, \hat{\psi_{ds}}}{dt} - \Omega_e \, \hat{\psi_{qs}} - \hat{\omega_e} \, \psi_{qs}$$
 (2-25)

$$\hat{v_{qs}} = -R_s \, \hat{i_{qs}} + \frac{d \, \psi_{qs}}{dt} + \Omega_e \, \hat{\psi_{ds}} + \hat{\omega_e} \, \psi_{ds} \tag{2-26}$$

Where:

$$\hat{\psi}_{as} = -L_{ls} \hat{i}_{as} - L_{m} (\hat{i}_{ar} + \hat{i}_{as})$$

$$\hat{\psi_{ds}} = -L_{ls} \hat{i_{ds}} - L_m (\hat{i_{dr}} + \hat{i_{ds}})$$

Similarly, eqs. (2-25) - (2-26) can be derived.

$$\hat{v_{dr}} = -R_r \hat{i_{dr}} + \frac{d\hat{\psi_{dr}}}{dt} - (\Omega_e - \Omega_r)\hat{\psi_{qr}} - (\hat{\omega_e} - \hat{\omega_r})\psi_{qr}$$
(2-27)

$$\hat{\mathbf{v}_{qr}} = -R_r \, \hat{i}_{qr} + \frac{d \, \hat{\psi}_{qr}}{dt} + (\Omega_e - \Omega_r) \, \hat{\psi}_{dr} + (\hat{\omega}_e - \hat{\omega}_r) \psi_{dr}$$
(2-28)

Where:

$$\hat{\psi_{dr}} = -L_{lr} \, \hat{i_{dr}} - L_m (\hat{i_{dr}} + \hat{i_{ds}})$$

$$\hat{\psi_{qr}} = -L_{lr} \hat{i_{qr}} - L_m (\hat{i_{qr}} + \hat{i_{qs}})$$

And similar procedures can be done on Eqs (2-130, (2-14), (2-16) to (2-18).

$$\frac{d}{dt}\hat{v}_{ds}^{\hat{}} = \frac{1}{C}\hat{i}_{ds}^{\hat{}} - \frac{1}{C}\hat{i}_{ld}^{\hat{}} - \frac{1}{C}\hat{i}_{d}^{\hat{}} + \Omega_{e}\hat{v}_{qs}^{\hat{}} + \hat{\omega}_{e}V_{qs}$$
 (2-29)

$$\frac{d}{dt}\hat{v_{qs}} = \frac{1}{C}\hat{i_{qs}} - \frac{1}{C}\hat{i_{lq}} - \frac{1}{C}\hat{i_{lq}} - \frac{1}{C}\hat{i_{q}} - \Omega_e \hat{v_{ds}} - \hat{\omega_e}V_{ds}$$
 (2-30)

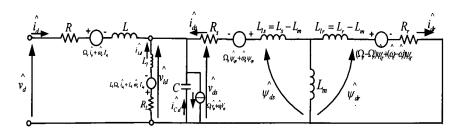
$$\hat{v}_{ld} = R \, \hat{i}_{ld} + L_l \, \frac{d}{dt} \, \hat{i}_{ld} - L_l \, \Omega_e \, \hat{i}_{lq} - L_l \, \hat{\omega}_e \, I_{lq}$$
 (2-31)

$$\hat{v}_{lq} = R \, \hat{i}_{lq} + L_l \, \frac{d}{dt} \, \hat{i}_{lq} + L_l \, \Omega_e \, \hat{i}_{ld} + L_l \, \hat{\omega}_e \, I_{ld}$$
 (2-32)

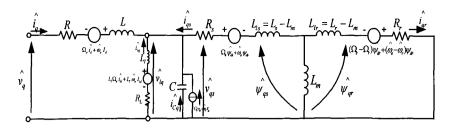
$$\frac{d\hat{i_d}}{dt} = \frac{1}{L} [\hat{v_d} - R\hat{i_d} - \hat{v_{ds}}] + \Omega_e \hat{i_q} + \hat{\omega_e} I_q$$
 (2-33)

$$\frac{d\hat{i_q}}{dt} = \frac{1}{L} [\hat{v_q} - R\hat{i_q} - \hat{v_{qs}}] - \Omega_e \hat{i_d} - \hat{\omega_e} I_d$$
 (2-34)

The small signal equivalent circuit for the whole system can be given based on Eqs. (2-25) – (2-34), as shown in Fig. 2-6.



(a) d-axis equivalent circuit



(b) q-axis equivalent circuit

Figure 2-6: Small signal model for d-q equivalent circuits in synchronous reference frame

2.8 Conclusions

In this chapter, the models of wind energy conversion system with induction generator and energy storage system are presented based on the model for each component. System model is developed to describe the dynamic behavior. Small signal model is derived based on the quiescent operating point and linearization. The model will be used for the controller design in Chapter 3.

Chapter 3 Control of Standalone WECS

3.1 Introduction

Based on the small signal model in the last chapter, the system transfer function can be obtained. Traditional control method can be used in the regulator design. Direct voltage control with current limit is developed for energy storage system to regulate the system voltage and frequency, and meanwhile, the real power and reactive power. In this research, compared with conventional power control with cascaded loops, the direct voltage control has faster dynamic performance with higher system bandwidth. The block diagram of the whole system is shown in Figure 3-1. And the controller design will be discussed in the followed sections.

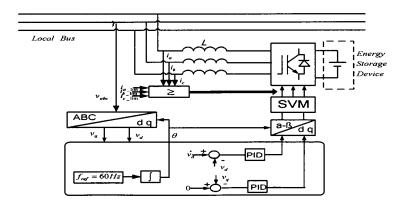


Figure 3-1: Control block diagram of the whole system

The stability analysis of the control system is based on the conventional method by using bode plots of the control loop in s-domain. Once the transfer function of the open loop is derived, the bode plots can be easily analyzed with the toolboxes in Matlab.

3.2 Direct Voltage Control

3.2.1 Voltage and Frequency Control

In Figure 3-1, the displacement angle for the synchronous reference frame is generated by a given frequency, which is the reference frequency in the standalone WECS. In a standalone system, no synchronization is needed since the induction generator is indirectly controlled by the power converter through adjusting the bus voltage. In the diagram, transformation block receives the synchronous angle and transform the three phase local bus voltage into d-q reference frame. Two lead-lag regulators are employed to directly regulate the d and q component voltages. The target of the control system is to force the bus voltage follow the reference voltage through a fixed frequency transformation. The frequency is indirectly controlled through the transformation block by the given frequency. Reference v_d^* and v_q^* are the desired bus voltage and the fixed frequency is the desired system operating frequency. If the system outputs follow the references, then active and reactive power balances are maintained.

The system can be decoupled on a d-q reference frame. The plant transfer functions can be derived from the small signal model in the Chapter2. Figure 3-2 shows the block diagram using transfer functions for d or q axis, while the cross-coupling terms in the system in the system are treated as the disturbances. In Figure 3-2, the PWM converter is treated as a power amplifier with the gain K_{PWM} and G(s) is the transfer function from $v_{d(g)}$ to $v_{d(g)s}$.

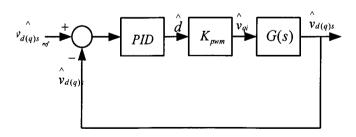


Figure 3-2: Block diagram using transfer functions

The controller for each axis uses a single loop to directly regulate the voltage. In this case, compared with conventional power control with cascaded loops, it has a much faster dynamic performance with even higher system bandwidth. Two lead-lag regulators are employed to regulated the d and q component voltages to obtain a higher phase margin and highest control bandwidth. The reference voltages can be arbitrary selected as long as the magnitude of the voltage is desired voltage. Usually the d-component reference voltage v_d^* is selected as the required local bus voltage, while the q-component reference voltage v_q^* is set to be zero. Space vector modulation (SVM) method is adapted to generate desired PWM gating signals.

It should be noted that the proposed system has no capability to protect the energy storage system (EES) from overload since the output current is not sensed in the control system. In order to protect the device from overload, several protection schemes have been developed. In this paper, dump load and current limit are employed together as the protection scheme. When the EES side current exceeds the maximum operating current of switching devices, the proper gating signal will be turned off to prevent the increase of current. The input power to EES is also detected, and the dump load is switched on when the input power exceeds the maximum power capability of the converter (or an energy storage device is applicable). The protection scheme with combination of fast act current limit and slow act dump load (due to power detection) functions well during overload. Other protections regarding over voltage, over temperature and devices short through are similar to regular converter system.

3.2.2 Direct Voltage Controller Design

Shown in Figure 3-3, the system transfer function G(s) can be obtained from the small signal model. The cross-coupling terms in the system are neglected since they are treated as the disturbances and compensated by either feed-forward or regulators.

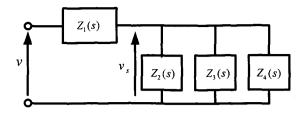


Figure 3-3: System blocks model in S-domain

The local bus voltage is the system output. The converter voltage, which controlled by the PWM signals is the system input. Then converter voltage to local bus voltage transfer function G(s) is shown in Eq. (3-1).

$$G(s) = \frac{v_s(s)}{v(s)} = \frac{Z_2(s)Z_3(s)Z_4(s)}{Z_2(s)Z_3(s)Z_4(s) + Z_1(s)[Z_3(s)Z_4(s) + Z_2(s)Z_3(s) + Z_2(s)Z_4(s)]}$$
(3-1)

Where $Z_1(s)$ is the transfer function of converter side filter. $Z_2(s)$ and $Z_3(s)$ are the transfer functions of load and self-excitation capacitors. In the analysis, resistive load is assumed since most of the consumer loads in the home are resistance loads, such as lighting, heating devices and so on.

$$Z_1(s) = sL (3-2)$$

$$Z_2(s) = R_L \tag{3-3}$$

$$Z_3(s) = \frac{1}{sC} \tag{3-4}$$

 $Z_4(s)$ represents the induction generator in S domain. The magnetization inductance is much bigger than the stator and rotor leakage inductances. So L_m can be neglected and the transfer function can be simplified in Eq.(3-5).

$$Z_4(s) = (R_s + R_r) + s(L_s + L_r)$$
(3-5)

Substitute the Eqs. (3-2) - (3-5) into Eq. (3-1), we have

$$G(s) = \frac{R_L[(R_s + R_r) + s(L_s + L_r)]}{(R_L + sL + s^2R_LLC_e)[(R_s + R_r) + s(L_s + L_r)] + sLR_L}$$
(3-6)

The bode plots of the uncompensated loop gain Tu(s) is shown in Figure 3-3, where

$$T_u(s) = K_{pwm}G(s) \tag{3-7}$$

The parameters are selected based on the 2kW lab prototype system which is shown in Table 3-1.

Table 3-1: Parameters of the Lab Prototype System

Load, R_L	22 Ω
Converter filter inductance, L	10mH/20A
Excitation Capacitance, C	141 μF
Stator Resistance, R_s	0.46Ω
Rotor Resistance, R,	0.7Ω
Stator Leakage Inductance, L_s	3.5mH
Rotor Leakage Inductance, L_r	3.5mH
Converter Gain, K_{PWM}	245

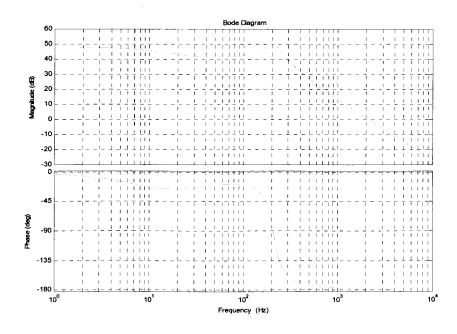


Figure 3-4: Bode plots of uncompensated loop

To analysis the load effect on the Bode plots, Fig. 3-5 shows the plots of the uncompensated loop under different loads. The load changes from 10 ohm to 100ohm in four steps. It can be seen that different loads only affect the overshoot value in magnitude plot and the slope of the curve at in phase plot (at resonant frequency). If the control bandwidth is selected to be much higher than the resonant frequency, the load variation has little effect to the dynamic response. In the prototype system, the bandwidth is selected at 1kHZ while the switching frequency of the converter is 10kHz.

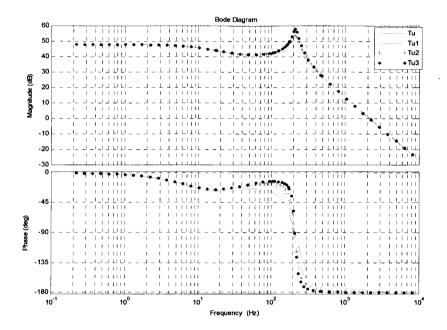


Figure 3-5: Bode plots of uncompensated loop with different loads

For the uncompensated loop, the cross-over frequency is around 2kHz, and the phase margin is no more than 5 degrees. For a stable system, the best phase margin should be around 52 degrees. In order to gain a higher bandwidth and enough phase margin, lead-lag regulators are used in equation 3-8. Thus the dynamic response of the control system will be faster than the cascaded system using PI regulators. In the prototype system the switching frequency is 10kHz. So the cross-over frequency of the compensated loop is selected to be around 1kHz (1/10th of the switching frequency). By proper selecting the regulator parameters, the compensated loop has

around 52 degrees phase margin at 1kHz. The bode plots of compensated loop gain T(s) (Eq.3-9) are shown in Figure 3-6.

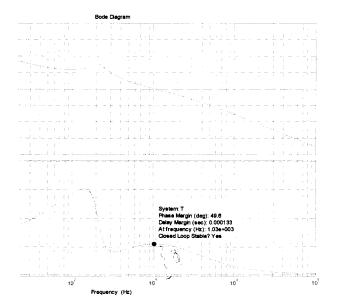
$$G_c(s) = G_{c0} \frac{1 + T_z s}{1 + T_p s} \frac{1 + T_i s}{T_i s}$$
(3-8)

$$T(s) = G_c(s)K_{pwm}G(s)$$
(3-9)

The parameters value of the lead-lag controller is shown in table 3-2, which are calculated through traditional method.

Table 3-2: Parameters of lead-lag Controller

T_z	T_p	T_i	
1	1	1	
$2\pi * 340$	$\frac{1}{2\pi * 2900}$	$2\pi * 100$	



5: Bode plot of compensated loop gain

3.3 Conclusions

In this chapter, a novel direct voltage control is proposed. Based on this analysis, the system local bus voltage and frequency can be regulated by the two control loops for d-q reference frame. But due to the non-sensed current, current protection scheme is employed in this control system. Based on the developed system transfer function, the direct voltage controller can be designed based on the traditional lead-lag regulator with increased the system phase margin and extended the system bandwidth. Thus reliability and dynamic performance are improved.

Chapter 4 Simulation and Experimental Results

4.1 Introduction

Both simulation models and experimental setup were built for the verification of the proposed wind energy conversion system with induction generator and energy storage. The whole system model was created using Simulink/Matlab. In the simulation, the system consists of the three major components: the wind power generation system with energy storage devices, the controller for power converter and the load. The wind turbine drives the induction generator to run at the based speed. In order to simulate the wind fluctuation, the wind speed is assumed to have the random changing around the base speed time by time. And the controller is used to regulate the local bus voltage and frequency constant. The details will be presented in the following sections.

As shown in Figure 4-1, the experimental set-up consists of a back to back converter, isolated transformer, a DC motor, an induction generator and a DSP-FPGA based digital controller. The proposed system is based on the 2kW LabVolt wound-rotor induction machine set.

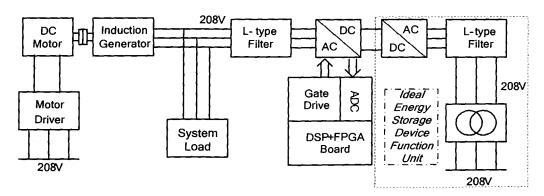


Figure 4-1: Block diagram of experimental set-up

The multipurpose back to back power converter was designed and built for several projects. In this project, one side of the converter works as a PWM rectifier, which maintains the DC link voltage constant. This part is functional as an ideal energy storage device. And the other side works as an inverter to maintain the local bus voltage and frequency constant with direct voltage control. The DC motor and induction generator are mechanically coupled together. The DC motor is operated as a prime mover to drive the induction generator in the super-synchronous speed mode. The Texas instruments TMS320F2812 DSP and Altera's Cyclone FPGA were employed as the core of the digital controller. Some experimental variables, such as dq components voltage and current, are captured form DSP internal memory since these variables are not directly available on the oscilloscopes.

4.2 Simulation Model

The whole system consists of the three major components: the wind power generator with energy storage, the controller for power converter and the load, as shown in Fig. 4-2.

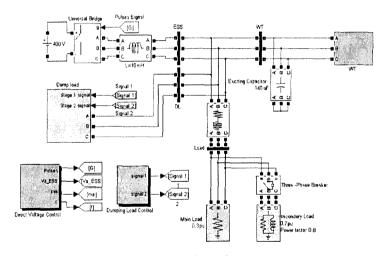


Figure 4-2: System models of proposed WECS

The system parameters of the prototypes system is shown in Table 4-1. Same parameters are used in the simulation.

Table 4-1: System parameters of prototypes system

System Ratings		Generator Parameters			
Power	2kW	Current	5.55A	Stator, Rotor Resistances	0.032pu
Voltage	208V	Frequency	60Hz	Stator, Rotor Leakage Induct- ances	0.061pu
Exitation	Capacitor	141 μ	F	Magnetization Inductance	0.875pu
Converter	Inductance	0.2рі]	Pole Pairs	2

Figure 4-3 shows the implementation of the controller outlined in Chaper3. The voltage references and frequency reference are given as constant values. The local bus voltages in pu system are sensed and feedback to the controller. The lead-lag regulators are used to regulate the bus voltage. The output of the regulator is used to generate the reference voltage for power converter, from where PWM gating signals are generated using SVM.

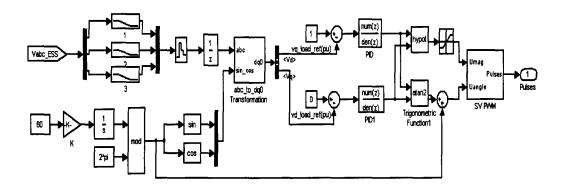


Figure 4-3: Direct voltage controller model

The energy storage devices (here is the ideal voltage source) are connected to the local bus through the inverter. Through the proposed controller, the local bus voltage and frequency should be kept constant in steady-state, and meanwhile, the system power flow should maintain balanced.

4.3 Simulation Results

4.3.1 Non-ESS Stand Alone Wind Power Generation System

When the WECS is connected to the load without the energy storage system, the local bus voltage and frequency will have a large fluctuation due to the wind speed fluctuation. The system configuration in simulation is shown in Figure 4-4. The wind turbine model use the standard block provided with the Simulink's Simpowersystem block set. The based wind speed is set to be 10m/s. A random source, whose range is from -1 to +1, is used to simulate the fluctuation in the wind. As shown in Fig. 4-5, the voltage and frequency have large fluctuations produced by wind generator without ESS. Both are not constant. So the power quality is not acceptable.

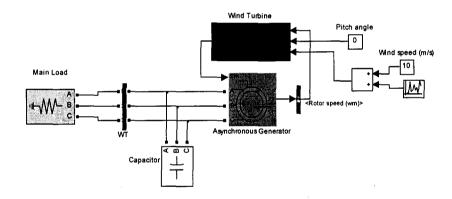


Figure 4-4: Wind power generation system without ESS

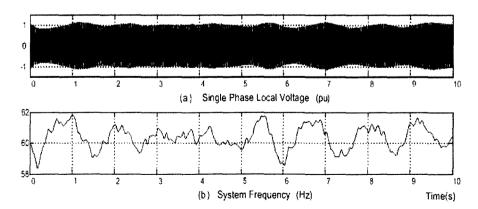


Figure 4-5: System voltage and frequency without ESS

4.3.2 Simulation Results with ESS

A. Resistive load Step Change

In order to test the controller performance both in steady state and transient response, a step load change was held at 1.0s in the simulation. The results are shown in Figure 4-6—4-13. With the EES, the voltage and frequency keep constant whenever before or after the load change. And meanwhile, the system power flow is maintained balanced.

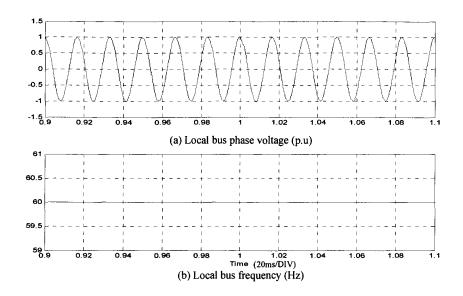


Figure 4-6: Local bus voltage and frequency during load step change (with R Load) in Simulation

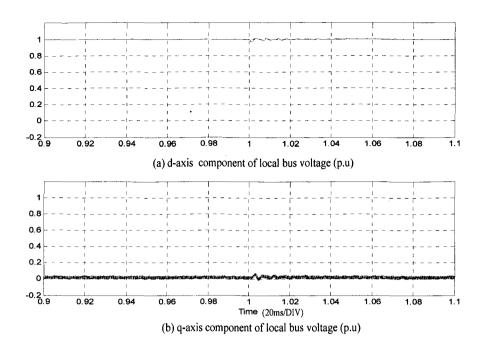


Figure 4-7: d-q axis inverter voltage during load step change (with R Load) in Simulation

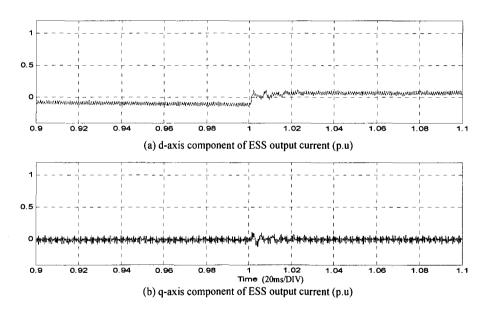


Figure 4-8: d-q axis inverter current during load step change (with R Load) in Simulation

In Fig.4-5, the voltage and frequency have large fluctuations by wind generator without ESS. When the EES is employed with proposed control system, the voltage and frequency are maintained constant as shown in Fig.4-6. Figure 4-7 and Figure 4-8 show the waveforms of d,q axis voltages and currents. During the load change, the voltages track the reference voltages in

very well with a small transient. It also can be observed from the waveforms that the frequency transient is less than ± 0.1 Hz and voltage dip is less than 1%. There is no steady-state error in the voltage and frequency due to the merits of synchronous frame and lead-lag regulators.

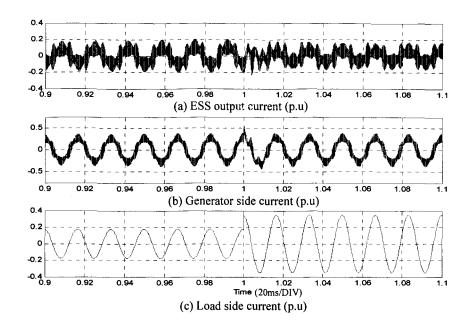


Figure 4-9: Current waveforms during load step change (with R load) in simulation

Fig.4-9 shows the current waveforms from the generator, ESS and load. The ESS absorbs the real power before 1.0s and provides real power after 1.0s. EES also compensates the fluctuation in the real power due to wind fluctuation at the same time. In the whole process, the power flow in the system maintained balance all the time.

B. Inductive Load Step Change

Fig.4-10 to Fig.4-13 show the simulation results with RL-load change at 1.0s. Fig.4-10 shows the local bus voltage and frequency. It has a similar response with the R load change. There's no significant change both in voltage and frequency. Fig. 4-11 shows the current waveforms with RL-load in simulation. The generator and EES together provide the real power. The reactive power is compensated from ESS. Fig. 4-12 and Fig.4-13 shows the d-q axis voltage and current simulation waveforms during load change. The d/q component voltages have very small dip. The d/q current components reflected the real power and reactive power from the EES respectively.

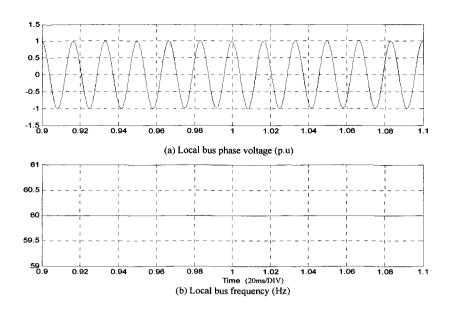


Figure 4-10: Voltage and frequency during load step change (with RL load) in simulation

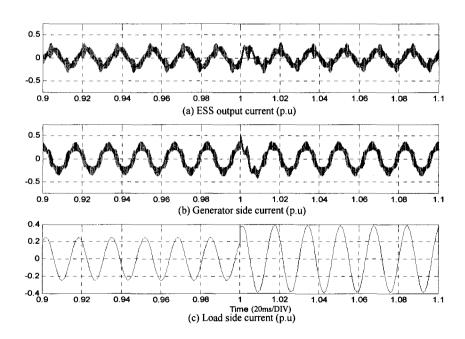


Figure 4-11: Currents waveforms during load step change (with RL load) in simulation

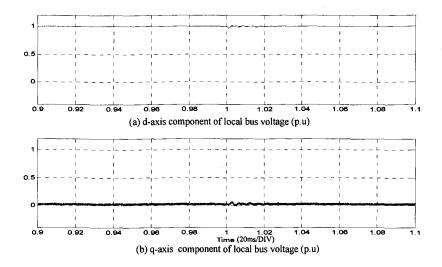


Figure 4-12: d-q axis inverter voltages during load step change (with RL Load) in Simulation

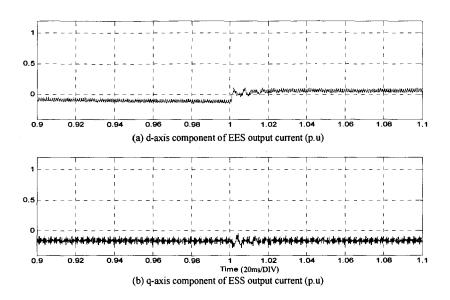


Figure 4-13: d-q axis inverter currents during load step change (with RL Load) in Simulation

Simulation results clearly show that the direct voltage control has good steady-state performance and fast transient response. The experimental results will be presented in the following section. Companied with the experimental results, the controller performance can be better tested.

4.4 Experimental Setup

The whole system experimental setup is shown in Fig.4-14, where part "A" is the DC motor, and part "B" is the induction generator. The DC motor and induction generator are mechanically coupled together. The DC motor is operated as a prime mover to drive the induction generator in the super-synchronous speed mode. Part "C" is the self-excition capacitor. The output of the induction generator is connected to the local bus, and only provides the real power to the load. The energy storage system is simulated by a back-to-back converter, which is part "D" in Figure 4-14. One side of the converter works as a PWM rectifier, which maintains the DC link voltage constant. This part is functional as an ideal energy storage device. The power fluctuation is buffed through the grid. And the other side works as an inverter to maintain the local bus voltage and frequency constant with direct voltage control, and meanwhile, keep the system power balanced. The DC link voltage is rated at 400V, and the Local bus voltage was rated at 208V/5.55A. Part "F" is the DSP-FPGA controller board. And part "E" is the filter inductor for PWM converter.

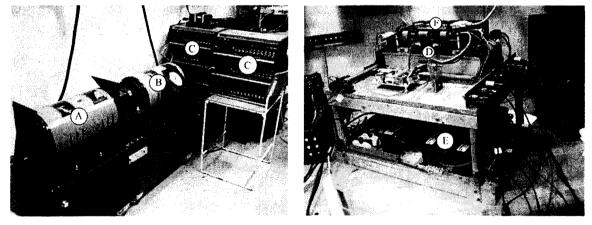


Figure 4-14: Experimental setup

(A: DC motor; B: Induction generator; C: Self-excited capacitor; D: Converter; E: Line indcutors; F: DSP-FPGA controller board)

The controller design developed in Chapter3 was implemented using the DSP-FPGA platform as shown in Fig.4-15. The controller hardware used in this experiment consisted of the analogue signal conditioning board, DSP ("A"), FPGA, interface circuit ("B")and a LED display ("C").

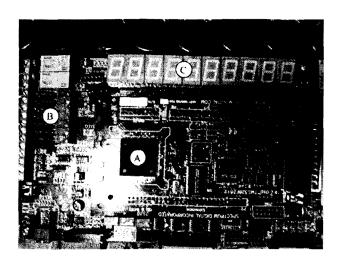


Figure 4-15: DSP controller board

(A: DSP chip; B: Interface circuit; C: LED display)

The controller algorithm from chapter3 was transferred into the DSP using C programming language. The complete code for the controller is given in Appendix D.

The system voltages and currents are sensed and fed to the conditioning circuit, which fed the signals to the A/D converter. The results of A/D converter are fetched by the DSP and used as the feedback signals. The final output signals of the DSP board are the switch signals for the PWM converter. The role of the FPGA in this experiment is to provide the phase information for the grid-side rectifier and to provide protection for the power converter in case of abnormal conditions. For this purposes the over-voltage, over-current and over-temperature protection circuits are interfaced directly with the FPGA to provide instantaneous protection of the power devices. In this system, the switching frequency is selected at 4.5 kHz. Higher switching frequency obviously would be better in the performance, but switching loss should be considered in the practical design.

The operational sequence of the controller is developed as following. First the gird side converter is energized. Once it is activated, the converter boosts the DC voltage to the required 400V. At this time the local bus side converter is turned on and works with constant V/f control strategy to drive the induction generator speeding up until it goes into steady state. The large starting current in the induction machine is avoided in the V/F control. And then, adjust the DC

motor input voltage to increase the input power until the rotating speed beyonds the synchronous speed. Now, the induction machine is operating in generator mode. The load then is connected to the local bus. And the controller starts to maintain the local bus voltage and frequency constant. The turn-off sequence for the converter is the opposite procedure of the start-up. In practical, the wind turbine speeds up the generator. The generator builds up the voltage with self-excitation capacitor. When the voltage reaches the desired level, the generator is brought to the local bus and ESS is started to maintain the local bus voltage and current. During the connection, synchronization is needed between ESS and generator. But in the experimental setup the synchronization is not necessary since the machine is started through the converter directly.

4.5 Experimental Results and Analysis

The performance of the direct voltage control was evaluated on the prototype system at several load conditions. The load step change is necessary. Through the load step change, the transient procedures are captured using the oscilloscopes through the voltage and current sensors. For different kind of loads, the local bus voltage and frequency are kept constant with direct voltage control. And the system power flow is maintained balanced with the ESS.

4.5.1 Resistive Load Test

Resistive load is connected on the local bus. When the generator starts up and goes into steady state, a three phase resistive load is connected to the system local bus. The resistor value is 120Ω . The steady state waveforms of the voltage and current at different sides are shown in Fig. 4-16.

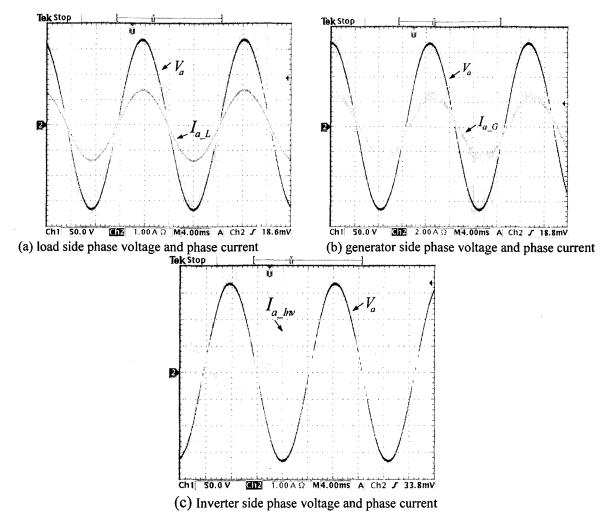


Figure 4-16: Steady-State waveforms with resistive load

Fig. 4-16(a) shows the waveforms of local bus voltage and the load current. As we can see, the local bus voltage is 120V in steady state. The load current is around 1A. Fig 4-16(b) and (c) shows the local bus voltage, generator side current and inverter side current. The generator provides the real power to load and EES. From Fig.4-16(b), the generator side current is around 1.7A. The load current is 1A. Fig.4-16(c) shows the additional 0.7A current entering the converter. From the current waveforms, it can be concluded that the system real power is balanced by ESS. Under same local bus voltage, the current reflects the system power flow.

When the wind power generation system runs in the steady state, another resistive load is switched on and off from the local bus. The transient waveforms of local bus voltage and currents were captured, as shown in Fig. 4-17.

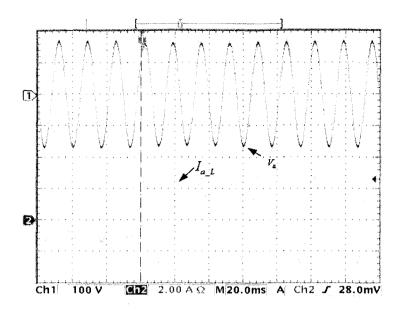
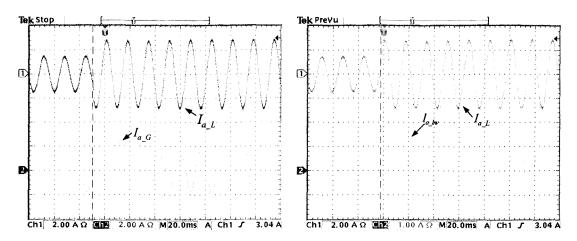


Figure 4-17: Transient waveforms of local bus voltage and load current during load step change

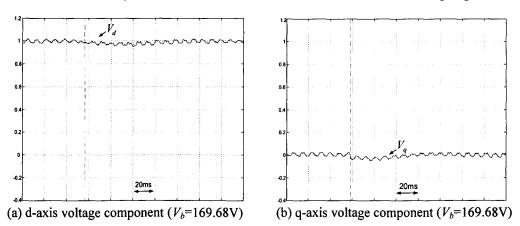
Fig. 4-17 shows the waveforms of local bus voltage and load current during the load change. After the additional resistor is switched on, the load current increases twice. From Fig.4-17, it can be seen that the local bus voltage has very small transient and thus a very small frequency change.

Fig 4-18 shows the waveforms of generator side current, inverter side current and load side current in the transient. It should be noted that the fluctuation in the generator current came from the oscillation of motor/generator set caused by load change. EES quickly compensates this oscillation and maintain the bus voltage/frequency constant. It also shows in Fig.4-18(b) that the ESS changes the power directional from absorbing excess real power to supplying the additional real power to the load.



(a) Load phase current and generator side phase current (b) Load phase current and inverter side phase current Figure 4-18: Transient waveforms of generator and converter currents during load step change (with R Load)

Voltage and current dq components waveforms of converter side are also captured from the DSP memory during the load change, as shown in Fig. 4-19. The reference voltage for v_d and v_q are 1.0 pu and 0 pu respectively. The voltage dq components trace the references very well. The current dq components are often referred to the real power and reactive power respectively. As it can be seen, i_d changes from negative to positive, indicating the power flow change for ESS. From the waveforms, it can be concluded that the control system has fast dynamic response during transient. And the steady-state error is almost zero because of the lead-lag regulators.



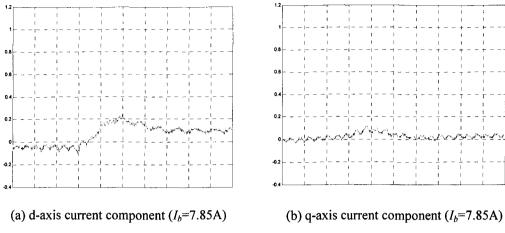
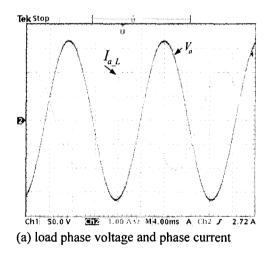
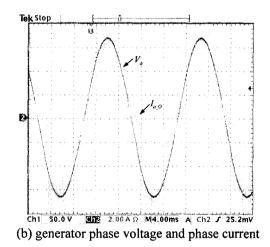


Figure 4-19: d-q axis Inverter side current during load step change (with R Load)

4.5.2 Inductive Load Test

The system performance is also verified by connecting the inductive load. A three-phase 120Ω resistor bank and a 0.31H inductor bank are connected to the bus in parallel. With RL load, the controller still maintains the local bus voltage and frequency constant by providing the reactive power to the load. The steady state waveforms are shown in Fig. 4-20.





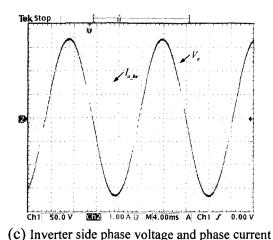


Figure 4-20: Steady-State voltage and current waveforms with RL load

Fig.4-20(a) shows the waveforms of local bus voltage and load current. Because of the RL load, the load current and voltage have about 45 degree phase displacement. Fig.4-20(b) and (c) show the waveforms of local bus voltage, generator side current and inverter side current. The generator only provides the real power to the load. So the current and voltage are almost in phase. The inverter absorbs the extra real in the system and provides the reactive power to the load. So the inverter side current lags the voltage at about 45 degree. From the Fig.4-20, it reflects the system power flow always maintains balance with the EES in the steady state.

Load step change is also carried in the RL load condition. When the whole system runs into steady state, an additional load (1200hm) is switched on and off. The transient waveforms are shown in Fig. 4-21 and Fig.4-22.

The local bus voltage and load current transient waveforms are given in Fig.4-21. It is similar to the waveforms with pure resistive load, and the local bus voltage has a very small transient. Fig. 4-22 shows the transient waveforms of the load current, generator side current and inverter side current.

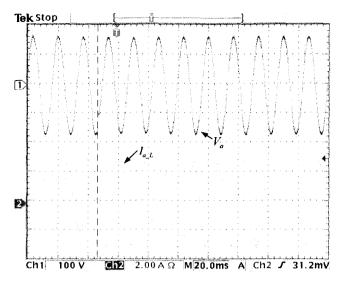
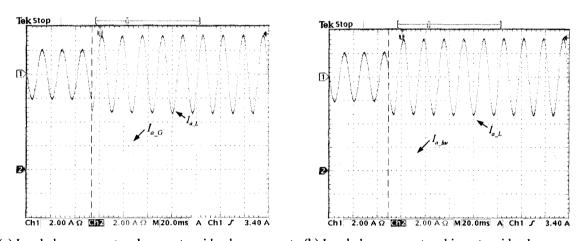


Figure 4-21: Transient waveforms of local bus voltage and load current during load step change (with RL load)



(a) Load phase current and generator side phase current
(b) Load phase current and inverter side phase current
Figure 4-22: Transient waveforms of currents of generator and inverter during load step change (with RL load)

Inverter side voltage and current dq components waveforms are also given in Fig. 4-23. The voltage dq components are very similar to the pure resistive load. During the load change, v_d has a very small dip and then went back to the reference value quickly. Current waveforms are also similar to the resistive load condition. Since the load change is only on resistance, i_d has the same waveform as resistive load and i_q maintains at -0.2 pu.

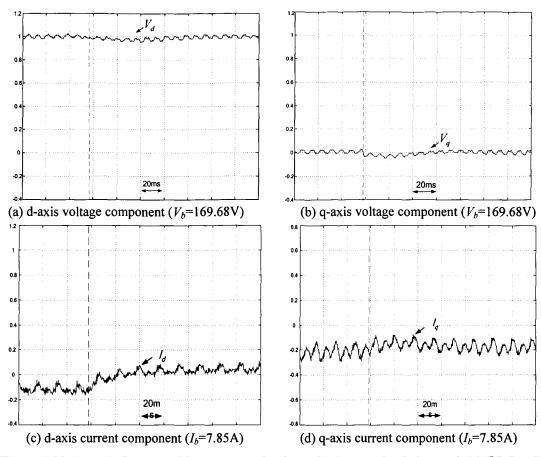


Figure 4-23: d-q axis Inverter side current and voltage during step load change (with RL Load)

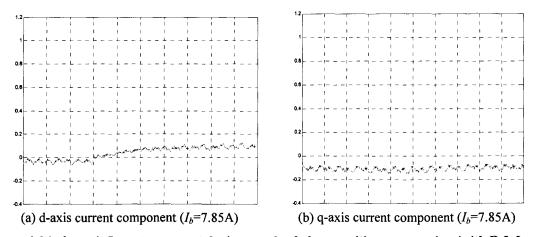


Figure 4-24: d-q axis Inverter current during step load change with compensation (with R-L Load)

It should be noted that current dq components waveforms contain an ac component at fundamental frequency both in R load and R-L load situations. It is verified that the inverter side current has a very small DC component. There are several reasons including non-symmetrical voltage output, sensor dc calibration and temperature drifting of the analog conditioning circuits. The last

two problems can be compensated through DSP using carefully calibrated circuit and dc bias compensation. But the unsymmetrical devices can not be avoided. The small DC voltage will cause large DC current in the system due to small resistance. This is the drawback of the proposed control system, which has no capability to direct regulate the current. So a simple DC compensation scheme is necessary in order to avoid the large DC current. The dq component current waveforms after compensation is are shown in Figure 4-24.

4.6 Conclusions

The model for standalone WECS with induction generator and energy storage system is constructed in the Simlink/Matlab software. The whole system with direct voltage control is verified in simulation and experiment. Different load conditions and load changes are carried in this project to verify the effectiveness of the controller. From the simulation and experimental results, it can be seen that the directly voltage control can achieve desired steady state performance with fast dynamic response.

Chapter 5 Conclusions

5.1 Conclusions

From the simulation and experimental results obtained in this thesis, several conclusions can be drawn regarding the design of the directly voltage controller for the standalone wind energy conversion system with induction generator and energy storage system.

The dynamic mathematical model for the whole system is developed. Small signal model is derived based on the dynamic model. The small signal model provides the basis for the controller design. A lead-lag regulator based controller is developed to regulated the local bus voltage constant in synchronous reference frame. The reference frequency and voltages are selected at the desired values. The transformer functions for d-q axis are developed. The regulator parameters is calculated through the traditional design using phase margin and system bandwidth. lead-lag regulators successfully improve system bandwidth while maintain high phase margin. Thus fast dynamic response and small overshoot/undershoot can be expected. The system stability is also improved.

The control scheme developed for the direct control of the system local bus voltage and frequency in the WECS has been tested using the simulation model and experimental setup. The control system successfully maintains the system voltage and frequency constant under different load condition and power fluctuation. The power flow in the system maintains balanced by the power converter and ESS. The transient waveforms shown in the experimental results, corresponding with the simulation results, verify the expected response from controller design.

Overall, this research work has shown that the energy storage system with direct voltage control can be effectively used in the stand-alone WECS. Though this kind of control scheme has

its own drawbacks such as no capability of current protection, simple scheme can be used to overcome the problems of overload protection as well as the dc current. In this thesis, the employment of squirrel cage induction generator gives benefit for reducing the manufacturing and maintainance cost. The system reliability can also be improved compared to DFIG or permanent magnetic machines. Only fractional capacity power converter is required in this configuration, which further reduce the system cost.

5.2 Major Contributions

One of the main contributions of this work is the design of the direct voltage control for the stand-alone WECS with induction generator and ESS. The control scheme shown in Figure 3-1 provides a novel control method compared with conventional cascaded control method. It directly regulated the local bus voltage and frequency, and maintained the power flow balance in the system. It has a faster dynamic performance and higher stability.

The configuration using induction generator is another contribution of this research work. Because its own advantages, such as reliable, low cost, low maintenance, this configuration has better cost per kW. The development of the small signal model is very useful for the controller design. The model accurately represents of the system behaviour around the quiescent operating point.

5.3 Further Research Works

In order to accommodate the system variations and improve the control system performance, the following research work should be done in the further.

1) Overload test should be done in the experimental conditions. The drawback of the direct voltage control is capability of current control. Current protection scheme should be improved if necessary.

- 2) Multiple generators operation should be investigated in the future research. Sometimes there are more than one wind turbine generators are connected to the local bus. The system model will become complicated and the control of ESS will be difficult.
- 3) The characteristics of the different energy storage devices should be considered. In this thesis, the energy storage device is assumed as an ideal source. In practice, the characteristic of the energy storage device needs to be considered and optimized power management should be implemented to increase the battery life.

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Appendices

Appendix A Simulation Models

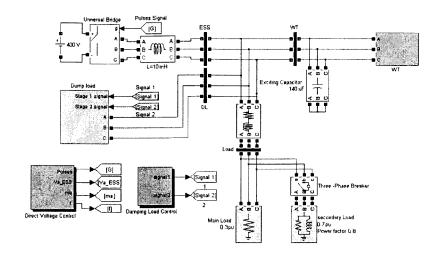


Figure A-1: Simulink model of WECS

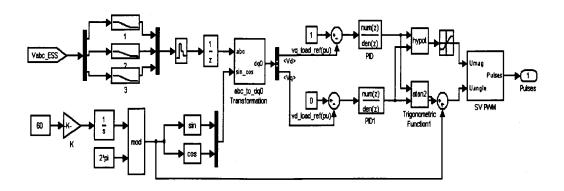


Figure A-2: Direct voltage controller model

Appendix B System Parameters

Table B-1 Parameters of DC Motor

Operating Condition	Motor	
Power	2 kW	
Armature Voltage	120 V	
Shunt Voltage	120V	
Armature Current	23 A	
Shunt Current	0.81A	
Speed	1800 rpm	
Armature Inductance	5mH	
Armature Resistance	2Ω	

Table B-2: System Parameters of Prototypes System

System Ratings		Generator Parameters			
Power	2kW	Current	5.55A	Stator, Rotor Resistances	0.032pu
Voltage	208V	Frequency	60Hz	Stator, Rotor Leakage Induct- ances	0.061pu
Excitation	n Capacitor	141 μ	F	Magnetization Inductance	0.875pu
Converter	Inductance	0.2рі	ı	Pole Pairs	2

Appendix C Code for Bode Plots

M-file for bode plots of compensated and uncompensated loops

```
clear all;
RL=22;Rs=0.46;Rr=0.70;Lls=0.0035;Llr=0.0035;Li=10e-3;
RL1=10;RL2=40;RL3=100;
C=1.41e-4;
Kpwm=245;
R1=Rs+Rr;L1=Lls+Llr;
s=tf('s');
G=(RL*(R1+s*L1)/(RL+R1+s*L1+s*C*(RL*(R1+s*L1))))/(s*Li+(RL*(R1+s*L1)/(RL+R1+s*L1+s*C*(RL*(R1+s*L1)))));
Tu=G*Kpwm;
Gc0=0.077;
Tz=1/2/pi/340; Tp=1/2/pi/2900; Ti=1/(2*pi*100); %Time constant of LEAD-LAG Gc=Gc0*(((1+Tz*s)/(1+Tp*s)))*(1+1/Ti/s); %LEAD-LAG controller
T=Gc0*Kpwm*Gc; %open loop gain with compensator bodeplot(Tu,T);
```

Appendix D DSP Program Code

DSP Program Code /*File Name: wecs.c "DSP281x Device.h" #include // DSP281x Headerfile Include File #include "DSP281x_Examples.h" // DSP281x Examples Include File #include "FPGA csr.h" "Display.h" #include #include <stdio.h> #include "IOmathLib.h" // Useful Definitions #define ADC usDELAY 8000 #define ADC usDELAY2 40 #define PI 3.1415926 #define sqrt3 1.732051 #define sqrt13 0.577350269 #define Sw_freq 8997.1//sampling frequency #define AVE SAMPLE 8 //AVE SAMPLE=2^AVE SHFT #define AVE SHFT #define AVE SAMPLE DC 16 //AVE_SAMPLE_DC=2^AVE_SHFT_DC #define AVE SHFT DC 4 #define w DC 1000.0//cut-off frequency(rad/s) of low-pass filter for DC voltage #define XL 0.016//0.016//Line to Converter inductance 0//current sensor position, #define sen posi 0:converter side, 1:grid side #define Kp Udc #define Ki Udc 40.0//for DC voltage control loop #define Kp I 0.04 #define Ki I 30.0//for current control loop #define Kp E 0.0796 #define Ki E 0.005//for loacal voltage control loop #define Kpp E 4.74

#define Kii E

#define Kdd E

3.735

0.0058

```
778700.0//gain for motor angle
#define K PLL
close loop
#pragma DATA SECTION(graph data, "graph data");
#pragma DATA SECTION(graph data1,"graph data1");
#pragma DATA_SECTION(graph_data2,"graph_data2");
#pragma DATA SECTION(graph data3,"graph data3");
#pragma DATA SECTION(graph data4,"graph data4");
#pragma DATA SECTION(graph data5,"graph data5");
#pragma DATA SECTION(graph data6,"graph data6");
//#pragma
DATA SECTION(wind profile,"wind profile");
**********
        VARIABLE DECLARATION
*/
/****************
/* ADC */
Uint16 Sample ch0[AVE SAMPLE],
Sample ch1[AVE SAMPLE],
   Sample ch2[AVE SAMPLE],
Sample_ch3[AVE SAMPLE],
   Sample ch4[AVE SAMPLE],
Sample ch5[AVE SAMPLE DC],
   Sample ch6[AVE SAMPLE DC],
Sample ch7[AVE SAMPLE],
   Sample ch8[AVE SAMPLE DC],
Sample_ch9[AVE_SAMPLE],
   Sample ch10[AVE SAMPLE],
Sample ch11[AVE SAMPLE],
   Sample ch12[AVE_SAMPLE],
Sample ch13[AVE SAMPLE],
   Sample ch14[AVE SAMPLE],
Sample ch15[AVE SAMPLE];
Uint16 ConversionCount=0;
Uint16 ConversionCount1=0;
int32 AD_BIAS0, AD_BIAS1, AD_BIAS2, AD_BIAS3,
  AD BIAS4, AD BIAS5, AD BIAS6, AD BIAS7,
  AD BIAS8, AD BIAS9, AD BIAS10, AD BIAS11,
  AD BIAS12, AD BIAS13, AD BIAS14,
AD BIAS15;
int32 Ia1, Ic1, Ia2, Ic2; //( iq18 format)
```

```
/* for testing*/
                                                      _iq18 V_d_L,V_q_L;
Uint32 watch =0;
Uint16 watch1 =0:
                                                      iq18 Ed err, Eq err, erro d, erro q,Ed_err0, Eq err0,
Uint 16 watch 2 = 0;
Uint16 watch3 = 0;
                                                               Ed err1, Eq err1, Eq D, Ed D, Eq D1,
 Uint16 Testswitch =0;
                                                      Ed_D1,
                                                               Ed_0, Eq_0, Ed_1, Eq_1;
                                                      _iq28 kp_E, ki_E, kpp E,kii_E,kdd E; // LEAD-LAG
/*PLL */
Uint 16 Theta con, Theta err; //phase and error info in
                                                      controller
counter format
Uint16 nmax,f;
Uint32 Theta pu; //line voltage angle in per unit value
                                                      /*Low-pass filter*/
iq28 Theta line; //line voltage angle in radian value
                                                      iq28 LPFa DC,LPFb DC;
(0-2pi)
ig28 Theta phase, angle offset; //phase voltage angle in
radian value
                                                      /* SVPWM*/
                                                      Uint16 Ts=16672;//PWM period in counter value
iq28 cos theta, sin theta;
                                                      Uint16 T1,T2,T0,Tc=0;
                                                      int16 section number;
/*=====VSR variables====== */
float Udc ref=400; // DC voltage reference
                                                      iq28 Theta, Theta 1, Theta sec;
iq18 Vab, Vbc, Vca,
                                                      iq18 Mmag, Mmag1;
   Ia, Ib, Ic,
   Vdc P,Vdc N;
                                                      /*Generator position and speed up*/
                                                      iq18 Speed n;
iq18 Va, Vb, Vc;
_iq18 V_alpha, V_beta;
                                                      ig28 Theta INV;
                                                      Uint16 Angle CNT, Angle CNT0, Speed CNT;
_iq18 V_d, V_q;
                                                      Uint16 Angle index=0;
                                                      Uint32 f counter;
/*Inner loop current control*/
iq18 I alpha, I beta;
                                                      Uint16 count_f, fL, F;
_iq18 I_d,I_d_ref, I_d_err,I_d_err1,
upperlimit Id, lowwerlimit Id;
                                                      /*Key input*/
                                                      int16 key value, key value1, key monitor,
iq18 I q, I q ref, I q err, I q err1;
                                                      key monitor1, key1;
_iq18 V_d_O, V_q O;
                                                      /* Display*/
ig18 I d in1, I d in2, I d out, I d out1, I d out2;
Uint16 display counter, display counter1;
iq28 kp I, ki I; //PI controller
                                                      /*Control flags*/
                                                      Uint16 MODE, //1:Rec 2:Inverter
/*Outer loop DC voltage control*/
                                                          CONTACTOR, /*For VSR:0-open, 1-close*/
ig18 Vdc ref, Vdc, Vdc0, Vdc L, Vdc L0,
                                                          CONTACTOR1, /*For VSI:0-open, 1-close*/
                                                                FAULT. /*0-no fault 1- fault detected*/
Vdc err.Vdc err1;
_iq28 kp_dc, ki_dc; //PI controller
                                                                PLL.
                                                                        /*0-PLL not locked 1-locked*/
                                                                Fault info A, /*Result of fault detection from
                                                      left (A) side*/
                                                          Fault info B, /*Result of fault detection from left (B)
/*=======*/
                                                      side*/
float Eq ref=0;
                                                                Initial over, //"0-not over, 1- over"/
iq18 Eab, Ebc, Eca, Ed ref, Eab0, Vab0,
   Iu, Iv, Iw:
                                                                SCREEN; /*0-system status screen0 1-status
iq18 Tu, Tw;
                                                      screen 1 */
                                                      Uint16 Res flag=0;
iq18 Ea, Eb, Ec;
                                                      Uint16 test number=0;
iq18 E alpha, E beta;
_iq18 Iuvw_alpha, Iuvw beta;
                                                      Uint16 test flag1=0;
iq18 E d, E q, Ed 0, Eq 0;
```

```
Uint16 Ready=0:
                                                        void Init variable(void);
                                                        void InitGpio(void);
Uint16 T CNT0=0:
                                                        void InitXintfClocks(void);
                                                        void InitPeripherals(void):
Uint16 T_CNT1=0;
Uint16 T CNT2=0;
                                                        void InitEVA(void);
                                                        void InitEVB(void);
/*Graph of waveform*/
                                                        void InitAdc(void):
int16 graph data[9000];//Vab
                                                        void init fpga(void);
int16 graph data1[9000];//I d ref
                                                        void Buffer rotating(int16 buffer[9000],Uint16
int16 graph data2[9000];//V d
                                                        shift times);
int16 graph data3[9000];//V q
int16 graph data4[9000];//I q
int16 graph data5[9000]://Vdc
int16 graph data6[9000];//Theta phase
                                                        /* NAME:
                                                                       main()
                                                        /* RETURNS: void
Uint16 index0=0:
Uint16 graph index=0;
Uint16 graph index1=0;
                                                        void main(void)
Uint16 graph index2=0;
Uint16 graph index flag=0;
                                                        // Step 1. Initialize System Control:
Uint16 data shift times=0;
                                                        // PLL(PLLCR=0xA), WatchDog(disable), enable
int16 data shift times1=0;
                                                        Peripheral Clocks
                                                          InitSysCtrl();
/*************
/*FUNCTION DECLARATION
                                                        // Step 2. Initialize the Xintf clocks
                                                          InitXintfClocks();
interrupt void adc isr(void);
                                                        // Step 3. Initalize GPIO:
interrupt void pdpinta isr(void);
                                                         InitGpio();
interrupt void t3cint_isr(void);
//interrupt void EVB CAPINT4 ISR(void);
                                                        // Step 4. Clear all interrupts and initialize PIE vector
//interrupt void EVB CAPINT5 ISR(void);
//interrupt void tlufint isr(void);
                                                          DINT: // Disable CPU interrupts
                                                         InitPieCtrl(); // Initialize the PIE control registers to
void Protection PLL (void);
                                                        their default state.
void get theta(void);
                                                                  // The default state is all PIE interrupts
void get frequency (void);
                                                        disabled and flags
void get adc V(void);
                                                                  // are cleared.
void abc dq transformation(void);
void speed up(void);
                                                         IER = 0x0000; // Disable CPU interrupts
void VSR Regulation(void);
                                                         IFR = 0x0000; // Clear all CPU interrupt flags
void VSI Regulation(void);
void SVPWM VSR(void);
                                                         InitPieVectTable(); // Initialize the PIE vector table
void SVPWM VSI(void);
void Enable Rec(void);
                                                       // Interrupts used are re-mapped to ISR functions
void Disable Rec(void);
                                                         EALLOW:
void Enable Inv(void);
                                                         PieVectTable.PDPINTA = &pdpinta isr;
void Disable Inv(void):
                                                         PieVectTable.ADCINT = &adc isr:
                                                         PieVectTable.T3CINT = &t3cint isr;
void Key input(void);
void Close Relay(void);
                                                         PieVectTable.CAPINT4=&EVB CAPINT4 ISR;
void Close Relay1(void);
                                                         PieVectTable.CAPINT5=&EVB CAPINT5 ISR;
void Open Relay(void);
                                                         //PieVectTable.T1UFINT = &tlufint isr;
void Open Relay1(void);
                                                         EDIS;
void AD bias16(void);
void Delay mili second (int delay);
                                                       // Step 5. Initialize all the Device Peripherals:
void get speed(void);
                                                         InitPeripherals();
```

```
{
// Step 6. User specific code, enable interrupts:
 PieCtrlRegs.PIEIER1.bit.INTx1 = 1; //Enable
PDPINTA
                                                   Sample ch0[ConversionCount]=((AdcRegs.ADCRESU
                                                   LT0>>4));
 PieCtrlRegs.PIEIER1.bit.INTx6 = 1; // Enable
ADCINT in the PIE: Group 1 interrupt 6
 PieCtrlRegs.PIEIER4.bit.INTx5 = 1; // Enable t3cint in
                                                   Sample ch1[ConversionCount]=((AdcRegs.ADCRESU
the PIE: Group 4 interrupt 5
                                                   LT1>>4));
 PieCtrlRegs.PIEIER5.bit.INTx5 = 1; // Enable
CAPINT4 in the PIE: Group 5 interrupt 5
                                                   Sample ch2[ConversionCount]=((AdcRegs.ADCRESU
 PieCtrlRegs.PIEIER5.bit.INTx6 = 1; // Enable
                                                   LT2>>4));
CAPINT5 in the PIE: Group 5 interrupt 6
 //PieCtrlRegs.PIEIER2.bit.INTx6 = 1; // Enable tlufint
                                                   Sample ch3[ConversionCount]=((AdcRegs.ADCRESU
in the PIE: Group 2 interrupt 6
                                                   LT3>>4));
 IER |= M_INT1; // Enable CPU INT1:
                                                   Sample ch4[ConversionCount]=((AdcRegs.ADCRESU
 IER |= M INT4; // Enable CPU INT4:
                                                   LT4>>4)):
 IER |= M INT5; // Enable CPU INT5:
                                                   Sample ch7[ConversionCount]=((AdcRegs.ADCRESU
 EINT; // Enable Global interrupt INTM
 ERTM; // Enable Global realtime interrupt DBGM
                                                   LT7>>4));
 Clear LED();
 AD bias16():
                                                   Sample ch9[ConversionCount]=((AdcRegs.ADCRESU
 Manu display();
                                                   LT9>>4));
 AdcRegs.ADCTRL2.bit.INT ENA SEQ1 = 1; //
                                                   Sample ch10[ConversionCount]=((AdcRegs.ADCRESU
enable SEQ1 interrupt (every EOS)
                                                   LT10>>4));
// Step 7. Infinite loop
 while(1)
                                                   Sample ch11[ConversionCount]=((AdcRegs.ADCRESU
                                                   LT11>>4));
   if (FAULT == 0)Key input ();
   display counter++;
                                                   Sample ch12[ConversionCount]=((AdcRegs.ADCRESU
        if(display counter==20000)
                                                   LT12>>4));
                                                       //
                                                   Sample ch13[ConversionCount]=((AdcRegs.ADCRESU
         display counter1++; display counter=0;
                                                   LT13>>4));
        if (display counter1==30)
                                                   Sample ch14[ConversionCount]=((AdcRegs.ADCRESU
   //Text LCD display();
                                                   LT14>>4));
   //key1=1://for test
                                                   Sample ch15[ConversionCount]=((AdcRegs.ADCRESU
   LED display();
   display counter1=0;
                                                   LT15>>4));
   display counter=0:
                                                       if (ConversionCount==AVE SAMPLE-1)
                                                   ConversionCount=0;
                                                       else ConversionCount++;
} /*End Main*/
/****************
                                                   Sample ch5[ConversionCount1]=((AdcRegs.ADCRESU
/* NAME: adc isr()
RETURNS: void
                                                   LT5>>4));//Udc+
DESCRIPTION: Interrupt for ADC results revieval
                                                   Sample ch6[ConversionCount1]=((AdcRegs.ADCRESU
/****************
                                                   LT6>>4));//Udc-
```

interrupt void adc isr(void)

```
Sample ch8[ConversionCount1]=((AdcRegs.ADCRESU
LT8>>4))://If
    if (ConversionCount1==AVE SAMPLE DC-1)
ConversionCount1=0;
    else ConversionCount1++:
 AdcRegs.ADCTRL2.bit.RST SEQ1 = 1;
                                         // Reset
SEO1
 AdcRegs.ADCST.bit.INT SEQ1 CLR = 1;
                                          // Clear
INT SEO1 bit
 PieCtrlRegs.PIEACK.all = PIEACK GROUP1; //
Acknowledge interrupt to PIE
} /*End of Adc isr*/
/* NAME:
             t3cint isr()
/* DESCRIPTION: Interrupt for computing
/****************
interrupt void t3cint isr(void)
 EINT:
 watch1= EvbRegs.T3CNT;
 get theta();
 get speed();
 get adc V();
 get frequency();
 abc dq transformation();
 switch (MODE)
 {
  case 1:
       upperlimit Id= IQ18(10);
  VSR Regulation();
  SVPWM VSR();
  break:
  case 2:
       speed up();
  upperlimit Id= IQ18(10);
  VSR Regulation();
  SVPWM VSR();
       VSI Regulation();
       SVPWM VSI();
  break;
 /*for waveforms display*/
```

```
graph data[graph index]= Iu>>12;
  graph data1[graph index]=Iw>>12:
  graph data2[graph index]= I E d>>12;
  graph data3[graph index]= I E q>>12;
  graph data4[graph index]=E d>>10;
  graph data5[graph index]=E q>>10;
  graph data6[graph index]=F;
  graph index++;
  if (graph index== 9000) graph index=0;
  if (graph index_flag==1) {graph index1++:}
  if (graph index1==6300) { graph index1--
;graph index--;}
  /*sampling data of speed*///9000points for 60s
  //if (graph index l == 60)
   //{graph data[graph index2]= torque G L>>8;
   //graph data5[graph index2]= veloc v>>11:
   // graph data4[graph index2]= torque shaft>>8;
   //graph index2++:graph index1=0;}
  //if (graph index2==9000)
{graph index1=0;graph index2=0;graph index flag=0;}
  watch2= EvbRegs.T3CNT;
  if (watch2>watch1) {watch3=watch2-watch1;}
  else {watch3=watch1-watch2;}
 EvbRegs.EVBIFRA.bit.T3CINT=1;// Clear INT
  PieCtrlRegs.PIEACK.all = PIEACK GROUP4;//
Acknowledge interrupt to PIE
} /*End of t3cint isr*/
/***********
/*NAME:
EVB_CAPINT4 ISR(),EVB CAPINT4 ISR()*/
interrupt void EVB CAPINT4 ISR(void) // CAP4
    CAP CNT0=EvbRegs.CAP4FBOT:
    Angle CNT0=EvaRegs.T2CNT;
    EvbRegs.EVBIFRC.all=BIT0;
    PieCtrlRegs.PIEACK.all=PIEACK GROUP5;
interrupt void EVB CAPINT5 ISR(void) // CAP5
    CAP CNT0=EvbRegs.CAP5FBOT;
    Angle CNT0=EvaRegs.T2CNT;
    EvbRegs.EVBIFRC.all=BIT1:
    PieCtrlRegs.PIEACK.all=PIEACK GROUP5;
  **************
  NAME:
             pdpinta isr()
```

}

```
/* DESCRIPTION: Protection interrupt generated from
                                                    PLL = 0;
                                                    //Protection PLL();
FPGA
/***********
                                                        else \{PLL = 1;\}
interrupt void pdpinta isr(void)
                                                   if (PLL==0) test number++;
  Open Relay();
  Disable_Rec();
  Disable Inv();
                                                              get adc V()
                                                 /* NAME:
       INTERRUPT = 0;
                                                 /* DESCRIPTION: Line voltage and current
                                                 conditioning with multi-sampling
       FAULT = 1;
  CONTACTOR = 0:
  Fault info A=*FAULT DETECT A;
  Fault info B=*FAULT DETECT B;
                                                 void get_adc_V(void)
  Display Fault ();
       PieCtrlRegs.PIEACK.all =
                                                        Uint16 i;
PIEACK GROUP1;// Acknowledge interrupt to PIE
                                                        Uint32 Sum ch0=0;
       /*No clear of the interrupt flag*/
                                                   Uint32 Sum ch1=0;
} /*End of Pdpinta isr*/
                                                   Uint32 Sum ch2=0;
                                                   Uint32 Sum ch3=0;
             Protection PLL()
                                                   Uint32 Sum ch4=0;
/* NAME:
/* DESCRIPTION: Protection action when PLL is lost
                                                   Uint32 Sum ch5=0;
                                                   Uint32 Sum ch6=0;
/*************
                                                   Uint32 Sum ch7=0;
                                                   Uint32 Sum ch8=0;
                                                   Uint32 Sum ch9=0;
void Protection PLL (void)
                                                   Uint32 Sum ch10=0;
                                                   Uint32 Sum ch11=0;
  Open Relay();
                                                   //Uint32 Sum ch12=0;
  Disable Rec();
                                                   //Uint32 Sum ch13=0;
  Disable Inv();
                                                   //Uint32 Sum ch14=0;
       INTERRUPT = 0;
                                                   //Uint32 Sum ch15=0;
       FAULT = 1:
  CONTACTOR = 0;
  Fault info A=*FAULT DETECT A;
                                                        for(i = 0; i < AVE SAMPLE; i++)
  Fault info B=*FAULT DETECT_B;
                                                      Sum ch0+=Sample ch0[i];
  Display Fault ():
} /*End of Protection PLL*/
                                                      Sum ch1+=Sample ch1[i];
                                                      Sum ch2+=Sample ch2[i];
Sum ch3+=Sample ch3[i];
                                                      Sum_ch4+=Sample ch4[i];
/* NAME:
             get theta()
/* DESCRIPTION: phase for abc-dq transformation
                                                      Sum ch7+=Sample ch7[i];
/***************
                                                      Sum_ch9+=Sample ch9[i];
                                                      Sum ch10+=Sample ch10[i];
                                                      Sum ch11+=Sample ch11[i];
void get theta(void)
                                                      //Sum ch12+=Sample_ch12[i];
                                                      //Sum ch13+=Sample ch13[i];
  Theta con = *PHASE A; /*phase info in counter
                                                      //Sum ch14+=Sample ch14[i];
format*/
                                                      //Sum ch15+=Sample ch15[i];
  Theta err = *PHASE\ LOCK\ A;\ /*DPLL\ phase
error in counter format*/
  nmax = *N_MAX_A + 1; /* */
                                                   for(i = 0; i < AVE SAMPLE DC; i++)
       /*PLL phase information*/
                                                     Sum ch5+=Sample ch5[i];
  if ((Theta err>15)&&(Theta err<480))
                                                     Sum ch6+=Sample ch6[i];
```

```
Vdc N = (Vdc N << (18-AVE SHFT DC)); //( iq18
    Sum ch8+=Sample ch8[i];
                                                    format)
                                                       Vdc N=Vdc N/2274;
                                                                                /*DSP ADC trim:
                                                    5V=1015 -5V=3130*/
                                                       Vdc N=-Vdc N*300;
                                                                             ///* sensor 30:1*/*/
 Ia2=Ia1:
                                                       Vdc0=Vdc:
   la1=la:
                                                       Vdc=Vdc P+Vdc N;
   Ic2=Ic1;
   Ic1=Ic:
                                                      /*Chanel 12*/
 /*Chanel 1*/
                                                       Iu=Sum ch7 - (AD BIAS7<<(AVE SHFT));</pre>
   Ia=Sum ch0 - (AD BIAS0 << (AVE SHFT));
   Ia=(Ia < < (18-AVE SHFT));
                                                       Iu=(Iu << (18-AVE SHFT));
                                                                                   //( iq18 format)
                               //( ig18 format)
                                                            //Iu=Iu-20972:
   Ia=Ia/2035; /*2023 for Iag,2035 for Ia*/
                                                       Iu=Iu/2510:
   Ia=-Ia*50: /*current sensor 5:1 */
                                                       Iu=-Iu*50; /*current sensor 5:1 */
  /*Chanel 2*/
   Ic=Sum ch1 - (AD BIAS1 << (AVE SHFT));
                                                      /*Chanel 13*/
        Ic=(Ic<<(18-AVE SHFT)); //( iq18 format)
                                                       Iw=Sum ch8 - (AD BIAS8<<(AVE SHFT DC));
                                                            Iw=(Iw<<(18-AVE SHFT DC)); //( iq18
        Ic=Ic/2050; /*2002 for Icg,2050 for Ic*/
        Ic=-Ic*50: /*current sensor 5:1 */
                                                    format)
                                                             Iw=Iw/1990:
                                                            Iw=-Iw*50; /*current sensor 5:1 */
       /*Chanel 3*/
   Vab=Sum ch2 - (AD BIAS2<<AVE SHFT);
   Vab=(Vab<<(18-AVE SHFT));
                                       //( ia18
                                                           /*Chanel 14*/
format)
                                                       Eab=Sum ch9 - (AD BIAS9<<AVE SHFT);
   Vab=Vab/2186; /*DSP ADC trim: 5V=3159 -
5V=1039*/
                                                       Eab=(Eab<<(18-AVE SHFT));
                                                                                           //( iq18
   Vab=Vab*450; /*Voltage sensor 45:1 */
                                                    format)
                                                       Eab=Eab/2208; /*DSP ADC trim: 5V=3159 -
                                                    5V=1039*/
       /*Chanel 4*/
   Vbc=Sum ch3 - (AD BIAS3<<AVE SHFT);
                                                       Eab=Eab*450; /*Voltage sensor 45:1 */
   Vbc=(Vbc<<(18-AVE SHFT)); // ( iq18 format)
   Vbc=Vbc/2065;/*DSP ADC trim: 5V=3156 -
                                                           /*Chanel 15*/
5V=1042*/
   Vbc=Vbc*450; /*Voltage sensor 45:1 */
                                                       Ebc=Sum ch10 - (AD BIAS10 << AVE SHFT);
                                                       Ebc=(Ebc<<(18-AVE SHFT)); // ( iq18 format)
                                                       Ebc=Ebc/2171;/*DSP ADC trim: 5V=3156 -
       /*Chanel 5*/
   Vca=Sum ch4 - (AD BIAS4<<AVE SHFT);
                                                    5V=1042*/
   Vca=(Vca<<(18-AVE SHFT));
                                      // ( iq18
                                                       Ebc=Ebc*450; /*Voltage sensor 45:1 */
format)
   Vca=Vca/2153; /*DSP ADC trim: 5V=3170 -
                                                           /*Chanel 9*/
5V=1026*/
   Vca=Vca*450; /*Voltage sensor 45:1*/
                                                       Eca=Sum ch11 - (AD BIAS11<<AVE SHFT);
                                                       Eca=(Eca<<(18-AVE SHFT));// ( iq18 format)
                                                       Eca=Eca/2171; /*DSP ADC trim: 5V=3170 -
       /*Chanel 6*/
                                                    5V=1026*/
   Vdc P = Sum ch5 -
(AD BIAS5<<(AVE SHFT DC));
                                                       Eca=Eca*450; /*Voltage sensor 45:1*/
   \overline{V}dc P = (Vdc P << (18-AVE SHFT DC)); //
       ( ig18 format)
   Vdc P=Vdc P/2204:
                           /*DSP ADC trim:
                                                     /*Low pass filtering for Vdc*/
5V=1041 -5V=3158*/
                                                       Vdc L0=Vdc L;
   Vdc P=-Vdc P*300;
                        ///* sensor 30:1*/*/
                                                       Vdc L= IQ18mpyIQX(LPFa DC,28,
                                                    (Vdc0+Vdc),18);
                                                       Vdc L= IQ18mpyIQX(LPFb DC,28,
       /*Chanel 7*/
                                                    Vdc L0,18)+Vdc L;
   Vdc N = Sum ch6 -
(AD BIAS6<<(AVE SHFT DC));
```

```
} /*End of Get adc V*/
                                                        if (count f==290) {count_f=0;F=fL*30;fL=0;}
                                                     }
/* NAME:
              get_speed()
/* RETURNS:
                           */
                void
/* DESCRIPTION: Generator speed w(rad/s)*/
                                                     /* NAME:
                                                                    abc_dq transformation() */
                                                     /* DESCRIPTION: abc to dq transformation */
void get_speed(void)
  Angle CNT0=Angle CNT;
                                                     void abc dq_transformation(void)
  Angle_index++;
  if (Angle index==90)
                                                       Theta pu = (long)Theta con << 16;
        {Angle CNT=EvaRegs.T2CNT;
                                                       Theta pu = Theta pu/nmax;
  if (Angle_CNT<Angle_CNT0)
                                                       Theta_pu = IQ28(1)- (Theta_pu<<12); /*PLL is in
Speed CNT=Angle CNT+14400-Angle CNT0;
                                                     counting down mode*/
  else Speed_CNT=Angle_CNT-Angle_CNT0;
                                                       Theta line = IQ28mpy( IQ28(2*PI), Theta pu);
           Angle index=0;
                                                     /*Va phase angle*/
       Speed_n=_IQ18mpyIQX( _IQ8(Speed_CNT), 8,
IQ28(6000.0/14400), 28);//motor speed in (rpm)
                                                       Theta phase = Theta line- IQ28(PI/2); /*angle for
                                                     DQ transformation */
                                                       Theta phase = Theta phase- angle offset;
}
                                                       if (Theta phase > IQ28(2*PI))
                                                       Theta phase = Theta phase - IQ28(2*PI);
                                                       if (Theta phase < 0)
/****************************/
                                                        Theta phase = Theta phase + IQ28(2*PI);
/* NAME:
              speed up() */
/* DESCRIPTION: U/f control to speed up: f:0--60Hz in
                                                       sin theta = IQ28sin(Theta_phase);
                                                       cos theta = IQ28cos(Theta phase);
20s */
                                                       /*Convert voltage from a-b-c to d-q*/
                                                       Va = (Vab - Vca)/3;
void speed_up(void)
                                                       Vb = (Vbc - Vab)/3;
 if (f<121)
                                                       Vc = (Vca - Vbc)/3;
  { f counter++;
        if (f_counter==3000)
                                                       V alpha = Va;
                                                       V beta = IQ18mpy(IQ18(sqrt13), (Vb - Vc));
        {f=f+1; f counter=0;}}
 else f=120;
                                                       V d = IQ18mpyIQX(cos theta, 28, V alpha, 18);
                                                       V d += IQ18mpyIQX(sin_theta, 28, V_beta, 18);
 Theta INV += IQ28mpyIQX( IQ18(f/2.0), 18,
IQ28(2*PI/9000.0), 28);
                                                       V_q = IQ18mpyIQX(-sin\_theta, 28, V_alpha, 18);
 if (Theta INV > IQ28(2*PI))
                                                       V q += IQ18mpyIQX(cos_theta, 28, V_beta, 18);
  Theta_INV = Theta_INV - _{IQ28(2*PI)};
  if (Theta INV < 0)
                                                             /*Convert current from a-b-c to d-q*/
  Theta_INV = Theta_INV + _{IQ28(2*PI)};
                                                        Ib = -Ia-Ic;
}
                                                        I alpha = Ia;
                                                        I_beta = IQ18mpy(IQ18(sqrt13), (Ib - Ic));
void get frequency(void)
                                                        I d = IQ18mpyIQX(cos theta, 28, I_alpha, 18);
  count f++;
  if ((Vab>0) && (Vab0<0)) {fL++;}
                                                        I_d += IQ18mpyIQX(sin\_theta, 28, I\_beta, 18);
                                                        I q = IQ18mpyIQX(-sin\_theta, 28, I\_alpha, 18);
  Vab0=Vab;
```

```
/* Outer loop voltage PI control*/
    I q += IO18mpyIOX(cos theta, 28, I beta, 18);
                                                          Vdc err = Vdc ref-Vdc L;
                                                                kp dc= IQ28(Kp Udc);
                                                                                           //kp = 0.5
                                                          ki dc= IQ28(Ki Udc/Sw freg);//ki/fs=45/9k=0.005
  /*Inverter voltage from a-b-c to d-q*/
                                                          if ((Vdc err< IQ18(1.2))&&(Vdc err> IQ18(-1.2)))
  Ea = (Eab - Eca)/3;
                                                        {kp dc= IQ28(Kp Udc/4);ki dc= IQ28(Ki Udc/Sw fr
        Ea = Ea/170;
                                                       eq/4);Res flag=1;}
  Eb = (Ebc - Eab)/3:
                                                                //if ((Vdc err< IO18(-
                                                       5))&&(Vdc err> IQ18(5)))
        Eb = Eb/170;
  Ec = (Eca - Ebc)/3:
                                                          //{kp dc=kp dc<<1;ki dc=ki dc<<1;Res flag=0;}
        Ec = Ec/170;
                                                          Vdc err1 += IQ18mpyIQX( ki dc, 28, Vdc err, 18);
  sin theta = IQ28sin(Theta INV);
                                                                if (Vdc err1>upperlimit Id)
  cos theta = IQ28cos(Theta INV);
                                                        Vdc err1=upperlimit Id;
                                                          if (Vdc err1< IQ18(-30)) Vdc err1= IQ18(-30);
                                                                I d ref= IO18mpvIOX(kp dc, 28, Vdc err,
  E alpha = Ea:
  E beta = IQ18mpy(IQ18(sqrt13), (Eb - Ec));
                                                        18)+Vdc err1;
                                                          if (test flag1==1) I d ref= IO18(13.7);
                                                          if (I d ref>upperlimit Id) I d ref=upperlimit Id;
  E d = IQ18mpyIQX(cos theta, 28, E alpha, 18);
  E d += IQ18mpyIQX(sin theta, 28, E beta, 18);
                                                          if (I d ref< IQ18(-30)) I d ref= IQ18(-30);
  E q = IQ18mpyIQX(-sin theta, 28, E alpha, 18);
  E q += IQ18mpyIQX(cos theta, 28, E beta, 18);
                                                                /* Inner loop current PI-Res control*/
                                                          I d in2 = I d in1:
                                                          I d in 1 = I d err;
                                                          I d out2 = I d out1;
 /*Inverter Current from a-b-c to d-q*/
                                                          I d out1 = I d out;
  Iu = Iu-Tu:
                                                          I d err = I d - I d ref:
        Iw = Iw + Tw;
                                                          //if (Res flag==1)
                                                          //{I_d_out=_IQ28mpyIQX(Res 6a,28, (I d err-
  Iv = -Iu-Iw;
                                                       I d in2),18);
   Iuvw alpha = Iu;
                                                          // I d out=I d out-I d out2-
   Iuvw beta = IQ18mpy( IQ18(sqrt13), (Iv - Iw));
                                                        IQ28mpyIQX(Res 6b,28, I d out1,18);}//resonant
                                                       regulator
   I E d
                = IO18mpvIOX(cos theta, 28,
Iuvw alpha, 18);
                                                          I d err1 += IQ18mpyIQX( ki I, 28, I d err, 18);
                                                          if (I d err1> IQ18(0.97)) I d err1= IQ18(0.97);
   I E d += IQ18mpyIQX(sin theta, 28, Iuvw beta,
                                                          if (I d err1 < IQ18(0.3)) I d err1 = IQ18(0.3);
18);
                                                                V_dO = IQ18mpyIQX(kp_I, 28, I_d_err,
   I E_q
                = IQ18mpyIQX(-sin theta, 28,
Iuvw alpha, 18);
                                                       18)+I d err1;
   I E q += IQ18mpyIQX(cos theta, 28, Iuvw beta,
                                                          if (V \ d \ O > IQ18(0.97)) \ V \ d \ O = IQ18(0.97);
                                                          if (V \ d \ O < IQ18(0.3)) \ V \ d \ O = IQ18(0.3);
18);
                                                          V_d O += IQ18mpyIQX(IQ28(XL), 28, Iq, 18);
   }
                                                          //if (Res flag==1) V d O +=I d out >> 10;//add
                                                       resonant regulator output
                                                          //if (display counter1<27)
/****************/
                                                          //V d O += V d H;//for active damping
                                                                if (V_d O > IQ18(0.97)) V d O = IQ18(0.97);
/* NAME:
               VSR_Regulation() & VSI Regulation()
                                                          if (V d O < IQ18(0.3)) V d O = IQ18(0.3);
/* DESCRIPTION: Converter side control
                                                          I_q in2 = I_q in1;
                                                          I_q_{in1} = I_q_{err};
void VSR Regulation(void)
                                                          I_q_out2 = I_q_out1;
                                                          I_q out 1 = I_q out;
                                                          I_q_err = I_q-I_q_ref;
```

```
Ed 0=Ed 0-_IQ18mpyIQX(kdd_E, 28, Ed 1, 18);
  //if (Res flag==1)
                                                        if (Ed_0 > IQ18(0.97)) Ed_0= IQ18(0.97);
  //\{I_q_out=_IQ28mpyIQX(Res_6a,28,(I_q_err-
                                                        if (Ed_0 < IQ18(0.01)) Ed 0 = IQ18(0.01);
I q in2), 18);
 // I q out=I q out-I q out2-
IQ28mpyIQX(Res 6b,28, I q out1,18);}//resonant
                                                                      Eq err = Eq ref-E q;
regulator
                                                                Eq_{err1} += IQ18mpyIQX(ki_E, 28, Eq_{err},
                                                      18);
                                                        if (Eq err1> IQ18(0.97)) Eq err1= IQ18(0.97);
  I q err1 += IQ18mpyIQX(ki I, 28, I q err, 18);
  if(I_q_err1>_IQ18(0.4)) I_q_err1=_IQ18(0.4);
                                                        if (Eq_err1 < IQ18(0.01)) Eq_err1=IQ18(0.01);
                                                                Eq D1=Eq D;
  if (I q err1 < IQ18(-0.4)) I q err1 = IQ18(-0.4);
        V \neq O = IQ18mpyIQX(kp I, 28, I \neq err,
                                                                Eq D = IQ18mpyIQX(kp E, 28, Eq_err,
18)+I q err1;
                                                      18)+Eq err1;
                                                              if (Eq D> IQ18(0.97)) Eq D= IQ18(0.97);
  V_qO += IQ18mpyIQX(IQ28(XL), 28, (-I_d), 18);
                                                        if (Eq D< IQ18(0.01)) Eq D= IQ18(0.01);
  //if (Res flag==1) V q O +=I q out >> 10;//add
resonant regulator output
  //if (display_counter1<27)
                                                          Eq 1=Eq 0;
                                                          Eq 0= IQ18mpyIQX(kpp_E, 28, Eq D, 18);
  //V \neq O += V \neq H;//for active damping
  if (V \neq O) = IQ18(0.4) V \neq O = IQ18(0.4);
                                                          Eq 0 = \text{Eq } 0 - \text{IQ18mpyIQX}(\text{kii E}, 28, \text{Eq D1}, 18);
  if (V_q_O < IQ18(-0.4)) V_q_O = IQ18(-0.4);
                                                          Eq 0=Eq 0- IQ18mpyIQX(kdd E, 28, Eq 1, 18);
                                                        if (Eq_0 > IQ18(0.97)) Eq_0 = IQ18(0.97);
                                                        if (Eq 0 < IQ18(0.01)) Eq_0 = IQ18(0.01);
        /* for test*/
 // V d O = IQ18(0.8);
                                                        ///* for test*/
        //V q O = IQ18(0);
                                                        //Ed 0 = IQ18(0.5);
  //if((E d < IQ18(80))&&(graph index flag==0))
                                                              //Eq 0 = IQ18(0);
//{graph index flag=1;data shift times=graph_index;}//
trigger for supply voltage sag
                                                               if (Ready==1)
} /*End of Regulation*/
                                                      ((I E d> IQ18(1.0))&&(graph index flag==0))
                                                      {graph index flag=1;data_shift_times=graph index;}}
void VSI Regulation(void)
        Ed_ref = IQ18(f/120.0);
  Ed err = Ed ref-E d;
        kp E = IQ28(Kp E); //kp = 0.07969
  ki E= IQ28(Ki E);//ki=0.005
                                                      /* NAME:
                                                                     SVPWM 7S()
                                                      kpp E = IQ28(Kpp E); //kpp = 4.74
                                                      void SVPWM VSR(void)
  kii E= IQ28(Kii E);//kii=3.735
        kdd E= IQ28(Kdd E); //kdd=0.0058
                                                         iq28 T1_sin,T2_sin;
                                                        Uint16 comp1,comp2,comp3,comp4;
        Ed err1 += IQ18mpyIQX( ki E, 28, Ed err,
                                                        Mmag= IQ18mag(V q O,V d O);//PU value
18);
                                                              if (Mmag> IQ18(0.98)) Mmag=_IQ18(0.98);
  if (Ed err1> IQ18(0.97)) Ed err1= IQ18(0.97);
                                                        Mmag= Mmag*(Ts>>2);//count value of every half
  if (Ed err1 < IQ18(0.01)) Ed err1 = IQ18(0.01);
                                                      PWM period
          Ed D1=Ed D;
          Ed D = IQ18mpyIQX(kp E, 28, Ed err,
18)+Ed_err1;
                                                        Theta= IQ28atan2(V q O,V_d_O);
        if (Ed D> IQ18(0.97)) Ed D= IQ18(0.97);
                                                        Theta+=Theta phase;//Phase for SVPWM
  if (Ed_D < IQ18(0.01)) Ed_D = IQ18(0.01);
                                                        if (Theta > IQ28(2*PI))
   Ed 1=Ed 0;
                                                        Theta = Theta - IQ28(2*PI);
   Ed 0= IQ18mpyIQX(kpp_E, 28, Ed_D, 18);
                                                        if (Theta < 0)
                                                        Theta = Theta + _{IQ28(2*PI)};
    Ed 0 = Ed \ 0 - IQ18mpyIQX(kii E, 28, Ed_D1, 18);
```

```
section number=Theta/ IQ28(PI/3);
 Theta sec= Theta-
                                                  void SVPWM VSI(void)
IQ28mpyI32( IQ28(PI/3),(long)(section number));
                                                   {
                                                     ig28 T1 sin, T2 sin;
       T1 sin= IQ28sin( IQ28(PI/3)-Theta sec);
                                                    Uint16 comp1,comp2,comp3,comp4;
  T2 sin= IQ28sin(Theta sec);
                                                    Mmag1=_IQ18mag(Eq 0,Ed 0)://PU value
       T1= IQ18mpyIQX(T1 sin, 28, Mmag,
                                                         if (Mmag1> IQ18(0.98)) Mmag1= IQ18(0.98);
18)>>16;// T1/2
                                                    Mmag1 = Mmag1*(Ts>>2)://count value of every half
  T2= IQ18mpyIQX(T2 sin, 28, Mmag, 18)>>16;//
                                                  PWM period
T2/2
  T0=Ts-T1-T2;/// T0/2
                                                    Theta1= IO28atan2(Eq 0,Ed 0);
 comp1=T0>>1;
                                                    Theta1+=Theta INV://Phase for SVPWM
       comp2=comp1+T1;
 comp4=comp1+T2;
       comp3=comp2+T2;
                                                    if (Theta1 > IQ28(2*PI))
                                                    Theta1 = Theta1 - IQ28(2*PI);
 switch (section number)
                                                    if (Theta1 < 0)
                                                    Theta1 = Theta1 + IQ28(2*PI);
   case 0:
                                                    section number=Theta1/ IQ28(PI/3);
    EvbRegs.CMPR4 = comp1;
    EvbRegs.CMPR5 = comp2;
                                                    Theta sec= Theta1-
                                                   IQ28mpyI32( IQ28(PI/3),(long)(section number));
    EvbRegs.CMPR6 = comp3;
        break;
                                                          T1 sin= IQ28sin( IQ28(PI/3)-Theta sec);
   case 1:
                                                    T2 sin= IQ28sin(Theta sec);
    EvbRegs.CMPR4 = comp4;
                                                          T1= IQ18mpyIQX(T1 sin, 28, Mmag1,
                                                   18)>>16;// T1/2
    EvbRegs.CMPR5 = comp1;
                                                    T2= IQ18mpyIQX(T2 sin, 28, Mmag1, 18)>>16;//
    EvbRegs.CMPR6 = comp3;
                                                  T2/2
        break:
                                                    T0=Ts-T1-T2;/// T0/2
   case 2:
                                                    comp1=T0>>1:
                                                          comp2=comp1+T1;
    EvbRegs.CMPR4 = comp3;
                                                    comp4=comp1+T2;
    EvbRegs.CMPR5 = comp1;
                                                          comp3=comp2+T2:
    EvbRegs.CMPR6 = comp2;
                                                    switch (section number)
        break:
   case 3:
                                                     {
                                                      case 0:
    EvbRegs.CMPR4 = comp3;
    EvbRegs.CMPR5 = comp4;
                                                       EvaRegs.CMPR3 = comp1-Tc;
                                                       EvaRegs.CMPR2 = comp2-Tc;
    EvbRegs.CMPR6 = comp1;
        break:
                                                       EvaRegs.CMPR1 = comp3-Tc;
                                                           break;
   case 4:
                                                     case 1:
    EvbRegs.CMPR4 = comp2;
                                                       EvaRegs.CMPR3 = comp4-Tc;
    EvbRegs.CMPR5 = comp3;
                                                       EvaRegs.CMPR2 = comp1-Tc;
    EvbRegs.CMPR6 = comp1;
                                                       EvaRegs.CMPR1 = comp3-Tc;
        break:
   case 5:
                                                           break;
                                                     case 2:
    EvbRegs.CMPR4 = comp1;
                                                       EvaRegs.CMPR3 = comp3-Tc;
    EvbRegs.CMPR5 = comp3;
    EvbRegs.CMPR6 = comp4;
                                                       EvaRegs.CMPR2 = comp1-Tc;
                                                       EvaRegs.CMPR1 = comp2-Tc;
        break;
                                                           break;
}
                                                      case 3:
```

```
EvaRegs.CMPR3 = comp3-Tc;
    EvaRegs.CMPR2 = comp4-Tc;
    EvaRegs.CMPR1 = comp1-Tc;
        break;
   case 4:
    EvaRegs.CMPR3 = comp2-Tc;
    EvaRegs.CMPR2 = comp3-Tc;
    EvaRegs.CMPR1 = comp1-Tc;
        break:
   case 5:
    EvaRegs.CMPR3 = comp1-Tc;
    EvaRegs.CMPR2 = comp3-Tc;
    EvaRegs.CMPR1 = comp4-Tc;
        break:
  }
/************
/* NAME:
Enable Rec(), Disable Rec(), Enable Inv(), Disable_Inv()
/* DESCRIPTION: Enable or disable PWM output*/
/************************/
void Enable Rec(void)
 EvbRegs.COMCONB.bit.FCOMPOE=1;
} /*End of Enable Rec*/
void Disable Rec(void)
 EvbRegs.COMCONB.bit.FCOMPOE=0;
void Enable Inv(void)
 EvaRegs.CMPR1 = 0x0000;
 EvaRegs.CMPR2 = 0x0000;
 EvaRegs.CMPR3 = 0x0000;
 EvaRegs.COMCONA.bit.FCOMPOE=1;
void Disable Inv(void)
{
 EvaRegs.COMCONA.bit.FCOMPOE=0;
/*******
/* NAME:
             Close Relay(), Open Relay*/
/* DESCRIPTION: Open and close relay for protection
/************************/
void Close_Relay(void)
Uint16 i;
```

```
GpioDataRegs.GPBCLEAR.bit.GPIOB12 = 1;//grid
side charging resistor by-pass relay open
 GpioDataRegs.GPACLEAR.bit.GPIOA7 = 1;//motor
side charging resistor by-pass relay open
 Delay mili second(400);
 GpioDataRegs.GPBDAT.bit.GPIOB7 = 1;//grid side
power relay close
       for (i=0; i<10; i++)
       Delay mili second(100);
       LED display();
 GpioDataRegs.GPBDAT.bit.GPIOB12 = 1;//grid side
charging resistor by-pass relay close
 GpioDataRegs.GPADAT.bit.GPIOA7 = 1://motor side
charging resistor by-pass relay close
 CONTACTOR = 1;
void Close Relay1(void)
 Uint16 j;
 GpioDataRegs.GPBDAT.bit.GPIOB11 = 1;//inverter
side power relay close
       for (j=0; j<10; j++)
       Delay mili second(100);
       LED display();
 CONTACTOR1 = 1;
void Open Relay(void)
 GpioDataRegs.GPBCLEAR.bit.GPIOB7 = 1;//grid side
power relay open
 CONTACTOR = 0;
void Open Relay1(void)
 GpioDataRegs.GPBDAT.bit.GPIOB11 = 0;//inverter
side power relay open
CONTACTOR1 = 0;
              Key input() */
/* NAME:
/* DESCRIPTION: LCD display and push button
command
void Key input(void)
```

// key_value = *KEY_IN;	break;
	case 2:
if(key_value)	//Iarm_ref= Iarm_ref+ _IQ18(0.5);
{	//if (Iarm_ref>_IQ18(20))
// key monitor++;	larm_ref= _IQ18(20);
// if(key monitor==300)	// Speed_w_ref=Speed_w_ref+_IQ18(5);
// {	//if (Speed_w_ref>_IQ18(180)) Speed_w_ref=
// key monitor1++;key_monitor=0;	_IQ18(180);
// }	break;
// if (key_monitor1==1000)	}
{	break;
// key monitor $1 = 0$;	or carry
. · · · · · · · · · · · · · · · · · · ·	case 6:
- " "	switch (MODE)
$// *KEY_IN = 0xf;$	Switch (WODE)
	case 0:
switch (key_value)	1
{	key1;
	if
case 1:	$(\text{key1} < 0 \text{key1} > 9) \{ \text{key1} = 9; \}$
if (CONTACTOR==0)	break;
{ SCREEN=1;Close_Relay	case 1:
();* $FAN_CONFIG = 0x1F$;}	key1;
CONTACTOR=1;	if
break;	$(\text{key1}<0 \text{key1}>9)\{\text{key1}=9;\}$
	break;
case 2:	case 2:
if(CONTACTOR1==0)	//Iarm_ref= Iarm_refIQ18(0.5);
{ SCREEN=2;Close_Relay1	//if (Iarm_ref<_IQ18(-5))
();*FAN_CONFIG = 0x1F;}	Iarm ref= IQ18(-5);
CONTACTOR1=1;	//Speed w ref=Speed_w_refIQ18(5);
break;	//if (Speed w ref< IQ18(0.1)) Speed_w_ref=
ordan,	_IQ18(0.1);
case 3:	break;
if (CONTACTOR==1)	}
{ MODE=1;	break;
Enable Rec();}	bicak,
	2002 7.
break;	case 7:
	if (CONTACTOR==1)
case 4:	P. H. P. O. MODE
//if (CONTACTOR==1)	Disable_Rec(); MODE =
//{ Enable_Rec();}	0;Open_Relay (); SCREEN=0;
	test_flag1=0;
if(CONTACTOR1==1)	Delay_mili_second(500);}
{	
MODE=2;	//if (data_shift_times>=2700)
break;	data_shift_times=data_shift_times-2700;
	//if (data_shift_times<2700)
case 5:	data_shift_times=data_shift_times+6300;
switch (MODE)	//
{	Buffer_rotating(graph_data,data_shift_times);
case 0:	// Buffer_rotating(graph_data1,data_shift_times);
keyl++; if	//Buffer_rotating(graph_data2,data_shift_times);
$(\text{key }1>9)\{\text{key }1=0;\}$	//Buffer_rotating(graph_data3,data_shift_times);
break;	//Buffer_rotating(graph_data4,data_shift_times);
case 1:	// Buffer_rotating(graph_data5,data_shift_times);
$key1++; if (key1>9){key1=0;}$	Manu_display();*FAN_CONFIG = 0x1D;

```
break;
                                                           bias data+=AdcRegs.ADCRESULT5>>4;
                                                                                  break;
      case 8:
      if (CONTACTOR1==1)
                                                                          case 6:
                       {Disable_Inv(); Open_Relay1
                                                           bias data+=AdcRegs.ADCRESULT6>>4;
();
                       if (CONTACTOR==1)
       MODE=1;
                                                                          case 7:
                       else MODE=0;
                       Delay mili second(500);}
                                                           bias data+=AdcRegs.ADCRESULT7>>4;
                                                                                  break;
                break;
                                                                          case 8:
                                                           bias data+=AdcRegs.ADCRESULT8>>4;
        }
       key value=0;//for control without keypad
                                                                          case 9:
} /*End of Key input*/
                                                           bias_data+=AdcRegs.ADCRESULT9>>4;
/*************************/
                                                                                  break;
                                                                          case 10:
/* NAME:
             AD bias()*/
/* DESCRIPTION: ADC dc bias caliberation */
                                                           bias data+=AdcRegs.ADCRESULT10>>4;
                                                                                  break;
                                                                          case 11:
int AD bias (unsigned int channel)
{
       int32 bias data=0;
                                                           bias data+=AdcRegs.ADCRESULT11>>4;
       Uint32 i;
                                                                                  break;
                                                                          case 12:
       bias data=0;
       for (i=0; i<65536; i++){
                                                           bias data+=AdcRegs.ADCRESULT12>>4;
                                                                                  break;
               while
                                                                          case 13:
(AdcRegs.ADCST.bit.INT SEQ1== 0){}
    AdcRegs.ADCST.bit.INT SEQ1 CLR = 1;
                                                           bias data+=AdcRegs.ADCRESULT13>>4;
Clear INT SEQ1 bit
                                                                                  break;
               switch (channel) {
                      case 0:
                                                                          case 14:
                                                           bias data+=AdcRegs.ADCRESULT14>>4;
       bias data+=AdcRegs.ADCRESULT0>>4;
                              break:
                                                                                  break;
                       case 1:
                                                                          case 15:
                                                                          default:
       bias data+=AdcRegs.ADCRESULT1>>4;
                                                           bias data+=AdcRegs.ADCRESULT15>>4;
                              break:
                                                                                  break;
                       case 2:
       bias data+=AdcRegs.ADCRESULT2>>4;
                                                           bias_data=bias_data>>16;
                              break:
                                                           return bias data;
                      case 3:
                                                   } /*End of AD bias*/
       bias data+=AdcRegs.ADCRESULT3>>4;
                              break;
                       case 4:
                                                                 AD bias16() */
                                                   /* NAME:
                                                   /* DESCRIPTION: LCD display and ADC dc bias
       bias data+=AdcRegs.ADCRESULT4>>4;
                                                   caliberation
                              break;
```

case 5:

```
/*****************************
                                                       Delay mili second(100);
                                                     } /*End of AD bias16*/
void AD bias16(void)
                                                     void Delay mili second (int delay)
{
       Text LCD clear display():
       Text LCD printxy(0,1," Test the AD Bias");
                                                             Uint16 i,i;
                                                             i=delay*30;//150M Hz DSP clock
       Text LCD printxy(0,2," Calculating CH 0");
                                                             for (j=0; j<1000; j++)
       AD BIAS0=AD bias(0);//2059
                                                              while (i)\{i--;\};
       Text LCD printxy(0,2," Calculating CH 1");
                                                        i=delay*30;
       AD BIAS1=AD bias(1);//2066
                                                             }
                                                     }
       Text LCD printxy(0,2," Calculating CH 2");
       AD BIAS2=AD bias(2);//2053
       Text LCD printxy(0,2," Calculating CH 3");
                                                     /* NAME:
                                                                   Init variable()
       AD BIAS3=AD bias(3);//2059
                                                     /* DESCRIPTION: Initialization of
                                                      system control variables
       Text LCD printxy(0,2," Calculating CH 4");
       AD BIAS4=AD bias(4);//2059
                                                      void Init variable(void)
       Text_LCD_printxy(0,2," Calculating CH 5");
                                                      /*ADC*/
       AD BIAS5=2046;//AD bias(5);
                                                      ConversionCount=0;
       Text_LCD_printxy(0,2," Calculating CH 6");
       AD BIAS6=2049;//AD bias(6);
                                                      /*PLL */
                                                      Theta con = 0;
       Text LCD_printxy(0,2," Calculating CH 7");
                                                      Theta err = 0;
       AD BIAS7=AD bias(7);//2047
                                                      nmax = 0:
                                                      Theta pu = 0; //phase in per unit value
                                                      Theta_line = 0; //phase in radian value (0-2pi)
       Text LCD printxy(0,2," Calculating CH 8");
                                                      angle offset = 0;
       AD BIAS8=AD bias(8);//2050
       Text LCD printxy(0,2," Calculating CH 9");
                                                      /*Speed up*/
                                                      Theta INV = 0;
       AD_BIAS9=AD_bias(9);//2055
                                                      f counter= 0;
       Text LCD printxy(0,2," Calculating CH 10");
                                                      f=0:
       AD BIAS10=AD bias(10);//2051
                                                      F=0:
                                                      fL=0;
       Text_LCD_printxy(0,2," Calculating CH 11");
                                                      count f=0;
       AD BIAS11=AD bias(11);//2047
                                                      /*Low pass filter*/
       /*Text LCD printxy(0,2," Calculating CH 12");
       AD BIAS12=AD bias(12);
                                                      LPFa DC= IO28(1-2.0/(2.0+w DC/Sw freq));
                                                      LPFb DC= IQ28(1)-(LPFa DC<<1);
       Text LCD printxy(0,2," Calculating CH 13");
       AD BIAS13=AD bias(13);
                                                      /*PI controller*/
       Text LCD printxy(0,2," Calculating CH 14");
                                                      kp dc = IQ28(Kp Udc);
                                                                                //kp=0.5
                                                      ki_dc=_IQ28(Ki_Udc/Sw freq);//ki/fs=45/9k=0.005
       AD BIAS14=AD bias(14);
                                                      kp_I = IQ28(Kp_I); //kp = 0.04
                                                      ki I= IQ28(Ki I/Sw freq);//ki/fs=30/9k=0.0033
       Text_LCD_printxy(0,2," Calculating CH 15");
       AD BIAS15=AD bias(15);*/
       Text LCD printxy(0,2," Calculation DONE "); | Vdc ref = IQ18( Udc ref);
```

```
Vdc err = 0;
 Vdc err1 = 0;
                                                   void InitGpio(void)
                                                     // sets GPIO Muxs as I/Os
I d ref= 0;
I d err = 0;
                                                     EALLOW;
I d err1=0;
                                                     GpioMuxRegs.GPAMUX.all= 0x077F; // Configure
                                                   MUXs as digital I/Os or
I q ref=0;// IQ18(-0.3);
                                                     GpioMuxRegs.GPBMUX.all= 0x077F; // peripheral
I_q_err = 0;
I_q err1 = 0;
                                                     GpioMuxRegs.GPDMUX.all=0x0000;
 V d O = IQ18(0.8);
                                                     GpioMuxRegs.GPEMUX.all=0x0000;
                                                     GpioMuxRegs.GPFMUX.all=0x0030;
 V q O=0;
                                                     GpioMuxRegs.GPGMUX.all=0x0030;
/*VSI LEAD-LAG controller*/
                                                     GpioMuxRegs.GPADIR.all=0xF8FF; //
Ed ref=0;
                                                     GpioMuxRegs.GPBDIR.all=0xF8FF; // GPIO DIR
                                                   select GPIOs as output or input
kp E = IQ28(Kp E);
ki E = IQ28(Ki E);
                                                     GpioMuxRegs.GPDDIR.all=0x0000;
                                                     GpioMuxRegs.GPEDIR.all=0x0000;
                                                     GpioMuxRegs.GPFDIR.all=0x3FDF;
kpp E = IQ28(Kpp E); //kpp = 4.74
                                                     GpioMuxRegs.GPGDIR.all= 0x0010;
kii E= IQ28(Kii E);//kii=3.735
kdd E=_IQ28(Kdd E); //kdd=0.0058
                                                     GpioMuxRegs.GPAQUAL.all=0x0000; // Set GPIO
                                                   input qualifier values
Ed err=0; Ed err0=0; Ed err1=0; Ed D=0; Ed 0=0;
                                                     GpioMuxRegs.GPBQUAL.all=0x0000;
Ed D1=0;Ed 1=0;
Eq err=0; Eq_err0=0; Eq_err1=0; Eq_D=0; Eq_0=0;
                                                     GpioMuxRegs.GPDQUAL.all=0x000F;
Eq D1=0;Eq 1=0;
                                                     GpioMuxRegs.GPEQUAL.all=0x000F;
Tu=26614; Tw=17614;
                                                     EDIS:
                                                   } /*End of Gpio select*/
/* Key input*/
key value = 0;
                                                   /* NAME: InitXintfClocks(),InitPeripherals()*/
key monitor = 0;
                                                   /* DESCRIPTION: System configuration
key monitor1 = 0;
key1=7;
                                                   /* NOTES:
                                                   /****************
/*system flags*/
                                                   void InitXintfClocks(void)
CONTACTOR1 = 0;
CONTACTOR = 0;
                                                    XintfRegs.XTIMING0.all=0x000358AC;
MODE = 0;
                                                    XintfRegs.XTIMING6.all=0x0003E746;//3D4A5;
FAULT = 0:
                                                    XintfRegs.XINTCNF2.all=0x00000007;
PLL = 0;
                                                   } /*End of InitXintfClocks*/
Initial over=0;
SCREEN = 0;
                                                   void InitPeripherals(void)
display counter=0;
display counter1=0;
                                                    //Text LCD initiate();
} /*End of Init variable*/
                                                    InitAdc();
                                                    InitEVA();
/*********************************/
                                                    InitEVB();
             Gpio select()
/* NAME:
                                                    init fpga();
/* DESCRIPTION: GPIO configuration
                                                    Init variable();
initialization
/************
```

```
void InitEVA(void)
                                                      EvbRegs.DBTCONB.all = 0x0FF4; // Enable deadband
                                                     3.4uS
                                                      //EvbRegs.COMCONB.all = 0x9000;//five segments
  // Configure EVA
  // EVA Clock is already enabled in InitSysCtrl():
                                                      EvbRegs.COMCONB.all = 0xA000://0xA000://seven
                                                     segments and update twice
 EvaRegs.EVAIMRA.bit.PDPINTA=1;//PDPINTA
                                                     /* Initalize the timers*/
protection enable
 // Enable compare for PWM1-PWM6
                                                     /* Initalize EVB Timer3*/
 EvaRegs.CMPR1 = 0x0000;
 EvaRegs.CMPR2 = 0x0000:
                                                       EvbRegs.T3PR =Ts;// Timer3 PWM period(for
                                                     computing fre of 8997Hz which is twice of rectifier
 EvaRegs.CMPR3 = 0x0000;
 // Compare action control. Action that takes place
                                                     switching frequency)
 EvaRegs.ACTRA.all = 0x0666;// active high
                                                       EvbRegs.T3CMPR = Ts >> 1;
                                                                                   // Timer3 compare
                                                       EvbRegs.T3CNT = 0x0000;
 EvaRegs.DBTCONA.all = 0x0FF4; // Enable deadband
                                                                                    // Timer3 counter
                                                       // TMODE = continuous up/down
3.4uS
 EvaRegs.COMCONA.all = 0xA000;//update twise
                                                       // Timer enable
                                                       EvbRegs.T3CON.all = 0x0802: // (updowncount mode)
/* Initialize OEP circuits*/
                                                     //input clock(HSPCLK)/1//timer compare enable
 EvaRegs.CAPCONA.all = 0x9004://disable capture
                                                       EvbRegs.EVBIMRA.bit.T3CINT=1: //Enable Timer3
                                                     compare interrupt
1.2:select timer2:detect rising edge for capture 3.
/* Initalize EVA Timer1*/
                                                      /* Initalize EVB Timer4*/
  EvaRegs.T1PR = Ts;// Timer1 period (for motor side
                                                       EvbRegs.T4CNT = 0x0000:
                                                       EvbRegs.T4PR =Ts>>4; // Setup period register (for
switching frequency)
  EvaRegs.T1CNT = 0x0000:
                              // Timer1 counter
                                                     sampling feq of 8997Hz*8)
                                                       EvbRegs.GPTCONB.bit.T4TOADC = 1;
 // Timer enable
                                                     EVASOC in EVB (underflow starts ADC)
 EvaRegs.T1CON.all = 0x0800; // (updowncount mode)
                                                       EvbRegs.T4CON.all = 0x0880;
//input clock(HSPCLK)/1
                                                                                      // (updowncount
 //EvaRegs.EVAIMRA.bit.T1UFINT=1; //Enable
                                                     mode) //input clock(HSPCLK)/1//start with T3
Timer1 underflow interrupt
                                                       EvbRegs.T3CON.bit.TENABLE=1;//Timer enable
/* Initalize EVA Timer2*/
  EvaRegs.T2CNT = 0x0000;
                                                       /* Initalize EVB Capture4&5*/
  EvaRegs.T2PR =14399; // period register (for 3600*4
                                                       EvbRegs.CAPCONB.all=0xA6F0;
                                                       EvbRegs.EVBIMRC.all=0x0003;
pules every cycle of speed sensor)
  EvaRegs.T2CON.all = 0x1870; //(directional-
                                                       EvbRegs.EVBIFRC.all=0x0007;
u/dpowncount mode)input clock from QEP
                                                     /***************************/
  EvaRegs.T1CON.bit.TENABLE=1;//Timer enable
                                                                                    */
                                                     /* NAME:
                                                                   InitAdc()
                                                     /* RETURNS:
                                                                     void
                                                     /* DESCRIPTION: ADC configuration, use Event
void InitEVB(void)
                                                     Manager A to start ADC
                                                                                    */
 // Configure EVA
                                                                                    */
                                                     /* NOTES:
 // EVA Clock is already enabled in InitSysCtrl();
 EvbRegs.EVBIMRA.bit.PDPINTB=1;//PDPINTA
protection enable
                                                     void InitAdc(void)
// Enable compare for PWM7-PWM12
                                                             /*Start ADC*/
                                                             AdcRegs.ADCTRL3.bit.ADCBGRFDN = 0x3;
 EvbRegs.CMPR4 = 0x0000;
 EvbRegs.CMPR5 = 0x0000;
                                                             // Power up bandgap/reference circuitry
 EvbRegs.CMPR6 = 0x0000;
                                                             Delay micro second (ADC usDELAY);
 // Compare action control. Action that takes place
                                                     // Delay before powering up rest of ADC
                                                             AdcRegs.ADCTRL3.bit.ADCPWDN = 1;
 // on a cmpare event
 EvbRegs.ACTRB.all = 0x0666;//active high
                                                             // Power up rest of ADC
                                                             Delay micro second (ADC usDELAY2);
```

```
/*Thermal Protection (disabled)*/
 /*Configure ADC*/
                                                           *FAULT THERMO_ENABLE = 0x0;
 AdcRegs.ADCTRL1.bit.ACQ_PS = 0x1;//S/H width in
ADC module periods = 2 \text{ ADC clocks}
                                                           *FAN PERIOD = 14999;
 AdcRegs.ADCTRL3.bit.ADCCLKPS = 0x5; //ADC
                                                           *FAN COUNT = 0x0;
module clock = HSPCLK/5 = 25MHz
                                                           *FAN COMPARE_A = 0x0;
 AdcRegs.ADCTRL1.bit.SEQ CASC = 1;
                                         // 1
                                                           *FAN COMPARE_B = 12180;
Cascaded mode
                                                           //*FAN_CONFIG = 0x1F;
 AdcRegs.ADCTRL1.bit.CONT RUN = 0; //not
Continous running
                                                           /*Fault signal distribution*/
// AdcRegs.ADCTRL1.bit.SEQ OVRD = 1;
                                                           *FAULT DISTRIBUTE = 0xffff;
Enable Sequencer override feature (bit 5)
                                                           /*Zero-crossing detection (Zero-crossing starts
 AdcRegs.ADCMAXCONV.all = 0x000B; // Setup 16
                                                   automatically)*/
conv's on SEQ1
                                                     *PHASE SHIFT A = 0x4DDc; // 0x4c2c ///*shift
 AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x1;
                                                   input to 90degree delay*/
 AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x2;
                                                                          // 0xb090 /*shift input to
 AdcRegs.ADCCHSELSEQ1.bit.CONV02 = 0x3;
                                                   180degree delay*/
 AdcRegs.ADCCHSELSEQ1.bit.CONV03 = 0x4;
                                                     //*PHASE SHIFT CONFIG A = 0x0118;///*
                                                   divider=24+1,DPLL freq=Fclock/(divider+1); input
 AdcRegs.ADCCHSELSEQ2.bit.CONV04 = 0x5;
 AdcRegs.ADCCHSELSEQ2.bit.CONV05 = 0x6;
                                                   Vbc*/
 AdcRegs.ADCCHSELSEQ2.bit.CONV06 = 0x7;
                                                     *PHASE SHIFT CONFIG A =
 AdcRegs.ADCCHSELSEQ2.bit.CONV07 = 0xC;
                                                   0x0118;//divider=24+1,DPLL
 AdcRegs.ADCCHSELSEQ3.bit.CONV08 = 0xD;
                                                   freq=Fclock/(divider+1); Vbc //0x0418 input Vvw
 AdcRegs.ADCCHSELSEQ3.bit.CONV09 = 0xE;
                                                           /*IO pin configuration*/
 AdcRegs.ADCCHSELSEQ3.bit.CONV10 = 0xF;
                                                           *GPIOA6 CONFIG = 0x0A; /*A side PLL
 AdcRegs.ADCCHSELSEQ3.bit.CONV11 = 0x9;
                                                   output*/
 AdcRegs.ADCCHSELSEQ4.bit.CONV12 = 0x8;
                                                           *GPIOB6 CONFIG = 0x0B; /*A side SYN
 AdcRegs.ADCCHSELSEQ4.bit.CONV13 = 0xE;
                                                   signal*/
 AdcRegs.ADCCHSELSEQ4.bit.CONV14 = 0xF;
 AdcRegs.ADCCHSELSEQ4.bit.CONV15 = 0x9;
                                                           /*XINT interrupt configuration*/
                                                           *XINT1 CONFIG = 0x0; /*Disable XINT1,
                                                   2*/
 //AdcRegs.ADCTRL2.bit.INT ENA SEQ1 = 1; //
                                                           *XINT2_CONFIG = 0x0;
enable SEQ1 interrupt (every EOS)
 AdcRegs.ADCTRL2.bit.EVB SOC SEQ = 1;
                                              //
                                                           /*Key input Text LCD displace interface*/
enable EVBSOC to start SEQ1
                                                           *KEY IN = 0xf;//clear all the registered key
} /*End of InitAdc*/
                                                   input
                                                           *SWITCH IN = 0x00;
                              */
/* NAME:
             init fpga()
                             */
                                                           /*FPGA LED*/
/* RETURNS:
               void
/* DESCRIPTION: Initialization of FPGA registers
                                                           *FPGA LED = 0x0;
                                                   } /*End of Init_fpga*/
*/
/* NOTES:
                                                   void Buffer rotating(int16 buffer[9000],Uint16
                                                   shift times)
void init fpga(void)
                                                    int16 a:
                                                    Uint16 i,i;
  /*Hardware Protection*/
        *FAULT CLEAR A = 0x0;
                                                    for (i=shift times;i>0;i--)
        *FAULT ENABLE A = 0x1ff;
                                                    {
        *FAULT CLEAR B = 0x0;
                                                     a=buffer[0];
                                                    for (j=0; j<9000; j++)
        *FAULT ENABLE B = 0x1ff;
                                                    {buffer[i]=buffer[i+1];}
```

buffer[8999]=a;	
} /*End of Buffer_rotating*/	//====================================
	//===================================