MODEL PREDICTIVE CONTROL OF HIGH POWER CURRENT-SOURCE CONVERTER FOR MEDIUM-VOLTAGE INDUCTION MOTOR DRIVE

By

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Model Predictive Control of High Power Current-Source Converter for Medium-Voltage Induction Motor Drive

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Doctor of Philosophy
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Ryerson University, Toronto, 2018

Abstract

As a crucial player in medium-voltage (MV) applications, high power current-source converters (CSCs) feature some distinct advantages in contrast to their voltage-source counterparts. However, the traditional control techniques, based on linear proportional-integral (PI) regulators and low band-width modulation, impose several technical issues during low switching frequency operation. In order to meet more and more stringent performance requirements on industrial drives, various high performance finite control-set model predictive control (FCS-MPC) schemes are proposed in this thesis to control CSCs employed in MV induction motor (IM) drives.

The continuous-time and discrete-time dynamic models of high power CSC-fed MV IM drive are deduced, which are used to predict the evolution of state variables in the system. Issues related to MPC approach, such as prediction horizon, weighting factor selection, control delay compensation, accurate extrapolation of references, and nature of variable switching frequency are addressed as well.

Model predictive power factor control (MPPFC) is proposed to accurately regulate the line power factor of CSR under various operating conditions. Meanwhile, an active damping function is incorporated into MPPFC to suppress the possible line-side *LC* resonance. Moreover, an online capacitance estimation method is designed in consideration on the perturbation of the filter parameters of CSR.

In order to keep fixed switching frequency of CSC and improve its dynamic responses, model predictive switching pattern control (MPSPC) and model predictive space vector pattern control (MPSVPC) are proposed, in which MPC technique is combined with selective harmonic elimination (SHE) modulation and space vector modulation (SVM), respectively. In steady state, the PWM waveform of CSC follows the pattern of traditional modulation schemes, whereas during transients CSC is governed by MPC approach for the purpose on dynamic performance improvement.

A common-mode voltage (CMV) reduced model predictive control (RCMV-MPC) is studied, with which the peak value of CMV in high power CSC-fed MV IM drive can be further reduced in comparison with the traditional RCMV modulation schemes. The dynamic responses of the motor drive system are further improved as well.

The simulation on a megawatt motor drive system and experimental results on a low power prototype, validate the effectiveness of the proposed various control schemes.

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Glossary of Acronyms and Symbols

Acronyms

MV	Medium-Voltage
LCI	Load Commutated Inverter
SCR	Silicon Controlled Rectifier
PWM	Pulse-Width Modulated
VSI	Voltage-Source Inverter
CSI	Current-Source Inverter
NPC	Neutral-Point Clamped
CHB	Cascaded H-Bridge
SVM	Space Vector Modulation
AFE	Active Front End
CMV	Common-Mode Voltage
THD	Total Harmonic Distortion
SGCT	Symmetry Gate Commutated Thyristor
CSR	Current-Source Rectifier
RMS	Root Mean Square
IM	Induction Motor
CSC	Current-Source Converter
TPWM	Trapezoidal PWM
SHE-PWM	Selective Harmonic Elimination PWM
SVM	Space Vector Modulation
LUT	Look-Up Table
HPF	High-Pass Filter
FOC	Field-Oriented Control
RCMV	Reduced CMV
AZS	Active-Zero-State
NTS	Nearest Three-State
MPC	Model Predictive Control
FCS-MPC	Finite Control-Set Model Predictive Control
DSP	Digital Signal Processor
MPPFC	Model Predictive Power Factor Control
MPSPC	Model Predictive Switching Pattern Control
MPSVPC	Model Predictive Space Vector Pattern Control
RCMV-MPC	Common-Mode Voltage Reduced Model Predictive Control
ZOH	Zero-Order Hold
PF	Power Factor
MAPF	Maximum Achievable Power Factor
LPF	Low-Pass Filter
BSF	Band-Stop Filter
PLL	Phase-Lock-Loop
TDD	Total Demand Distortion

MPFOC	Model Predictive Field-Oriented Control
MS-SVM	Multi-Sampling SVM
RL	Load resistor and inductor
LC	Inductor and capacitor

Symbols

Voltage Quantities

V	Magnitude of phase voltage or DC voltage (V)
v	Instantaneous value of alternating voltage (V)
$\vec{V}$	Stationary voltage space vector (V)
$\vec{v}$	Rotating voltage space vector (V)

Current Quantities

I	Magnitude of line current or DC current (A)
i	Instantaneous value of alternating currnet (A)
$\vec{I}$	Stationary current space vector (A)
$\vec{i}$	Rotating current space vector (A)

Power Quantities

P	Active power (W)
Q	Reactive power (VAr)
$Q_g^p(k+1)$	Predicted line reactive power at (k+1)th sampling instant (VAr)
P_g	Line active power (W)
P_{dc}	DC-side power (W)
Q_g^*	Line reactive power reference (VAr)
P_g^*	Line active power reference (W)

RLC Quantities

C	Capacitance (μF)
L	Inductance (mH)
R	Resistance (Ω)

Frequency and Phase Angle Quantities

θ	Angle of space vector (rad)
ϕ	Phase angle difference (rad)
β	Independent phase angles used to generate selective harmonic elimination PWM waveform (rad)
ω	Angular frequency (rad/s)
f	Frequency (Hz)

T	Control period or sampling interval (μs)

Induction Motor Quantities

$\vec{\lambda}_r$	Rotor flux vector (Wb)
λ_r	Magnitude of rotor flux vector (Wb)
R_s	Stator resistance (Ω)
R_r	Rotor resistance (Ω)
L_s	Stator inductance (mH)
L_r	Rotor inductance (mH)
L_m	Magnetizing inductance (mH)
ω_r	Electrical angular frequency of induction motor (rad/s)
P	Number of pole pairs
σ	Induction motor total leakage factor
k_r	Coupling factor
R_σ	Coefficient
τ_σ	Transient time constant (s)
τ_r	Rotor time constant (s)

Predictive Controller Quantities

x	State vector
u	Input vector
A	System matrix
B	Input matrix
Φ	Prediction matrix
Γ	Prediction matrix
I	Identity matrix
$\vec{x}$	Space vector of state variable
$\vec{u}$	Space vector of input
w_{cmv}	Weighting factor for common-mode voltage reduction term
w_{Cp}	Weighting factor for average switching frequency reduction term
C_p	Number of commutations between two switching states
S_x	State of *x*th switching device (x = 1, 2, 3, …, 6)
$J^{\max}$	Threshold value of cost function
g	Output value of cost function

Miscellaneous

m	Modualting index
K	Gain value used in active damping function
η	The efficiency of power converter

Superscripts

LP	Value after a low-pass filter
p	Predicted value
(*x*)	Prediction corresponding to *x*th current space vector of a CSC
(*y*)	Prediction corresponding to *y*th current space vector of a CSC
*	Reference value
lim	Limitation value
R	Rated value
op	Optimally selected
SHE	Following SHE modulation PWM pattern
init	Initial value
est	Primarily esitimated value
^	Estimated value

Subscripts

r	Recitifier side quantities
i	Inverter side quantities
C	Voltage or current of Capacitor
Lf	Votlage or current of Filter inductor
g	Voltage or current of utility power supply
s	Voltage or current of stator in an induction motor
dc	Voltage or current of DC side
cm	Common mode
z	Neutral point
(1)	Fundament frequency component
(*h*)	High-order harmonic components
n	*n*th current space vector of a CSC
α	α -axis component
β	β -axis component
d	*d*-axis component
q	*q*-axis component
damp	Quantities used for damping
sec	Quantities with respect to a sector in a space vector domain
mr	Mechanical rotor

1 Introduction

1.1 Overview and Prospect of Medium-Voltage Motor Drive

The medium-voltage (MV) drives cover power ratings from 0.4MW to 40MW at the MV levels of 2.3kV to 13.8kV. The power rating can be extended to 100MW, where synchronous motor drives with load commutated inverters (LCIs) are often used [1-4]. However, the majority of the installed MV drives are in the 1- to 4MW range with voltage ratings from 3.3kV to 6.6kV [5].

The high power MV drives have found widespread applications in industry. They are used for pipeline pumps in the petrochemical industry [6], fans in the cement industry [7], pumps in water pumping station [8], traction applications in the transportation industry [9], steel rolling mills in the metals industry [10], and other applications [11, 12].

Fig. 1.1 shows a general block diagram of high power MV drives. Depending on the system requirements and the type of the converters employed, the line- and motor-side filters are optional. A phase shifting transformer with multiple secondary windings is often used mainly for the reduction of line current distortion.

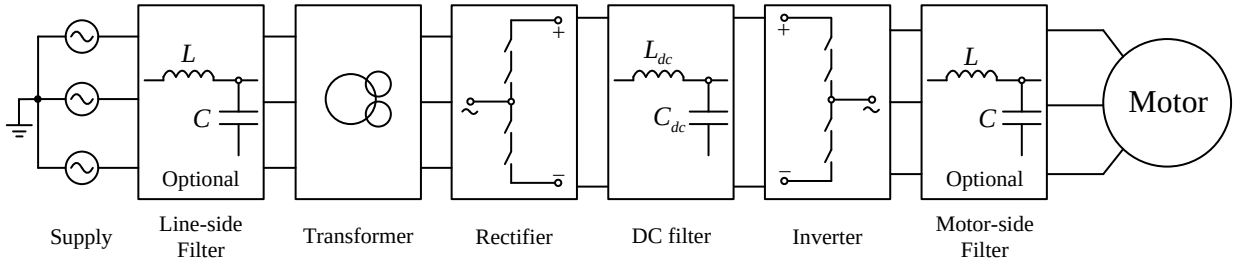


Fig. 1.1 General block diagram of high power MV drives.

In Fig. 1.1, the rectifier converts the utility power supply voltage to a (direct-current) DC voltage with a fixed or adjustable magnitude. The commonly used rectifier topologies include multiphase diode rectifiers, multipulse silicon controlled rectifiers (SCRs), or pulse-width modulated (PWM) rectifiers. The DC filter can simply be a capacitor that provides a stiff DC voltage in voltage source drives or an inductor that smoothes the DC current in current source drives.

The inverter can be generally classified into voltage-source inverter (VSI) and current-source inverter (CSI). The VSI converts the DC voltage to a three-phase AC voltage with adjustable magnitude and frequency whereas the CSI converts the DC current to an adjustable three-phase AC current. A variety of VSI topologies have been developed for MV drives, including two-level VSI, neutral-point clamped (NPC) inverter, and cascaded H-bridge (CHB) inverter.

1.2 Voltage-Source Inverter Topologies for Medium-Voltage Drives

The VSI-fed MV drives have found wide applications in industry. These drives come with a number of different configurations, each of which has some unique features.

1.2.1 Two-level Voltage-Source Inverter

It is well known that two-level VSI is a dominant converter topology for low-voltage (lower than 600V) drives. This technology has now been extended to MV drives, which are commercially available for the power rating up to a few megawatts [13]. Fig. 1.2 shows a typical two-level inverter topology for MV drives. There are three switching devices in series per inverter branch. The inverter can be controlled by either carrier-based modulation or space vector modulation (SVM) scheme. Two-level VSI has the features as follows.

1) Simple PWM scheme. The conventional carrier-based sinusoidal modulation or SVM scheme can be implemented for the inverter. Only six gate signals are required for the six groups of synchronous switches;

2) Ease of DC capacitor pre-charging. The DC capacitor in the two-level inverter needs only one pre-charging circuit;

3) Provision for four-quadrant operation and regenerative braking. An active front end (AFE) with the same configuration as the inverter can provide four-quadrant operation or regenerative braking.

However, there are some drawbacks associated with two-level VSI, including the followings.

1) High dv/dt in the inverter output voltage. The dv/dt is particularly high for two-level inverter employing series connected switches in a synchronous manner, which causes a

number of problems such as premature failure of motor winding insulation, early bearing failure and wave reflections;

2) Motor harmonic losses. Two-level VSI in MV drives usually operates at low switching frequencies, typically lower than 1kHz, resulting in a high harmonic distortion in stator voltages and currents;

3) Common-mode voltages (CMVs). The switching action of the rectification and inversion normally generates CMVs [14]. If not mitigated, these voltages would appear on the motor, causing premature failure of its winding insulation.

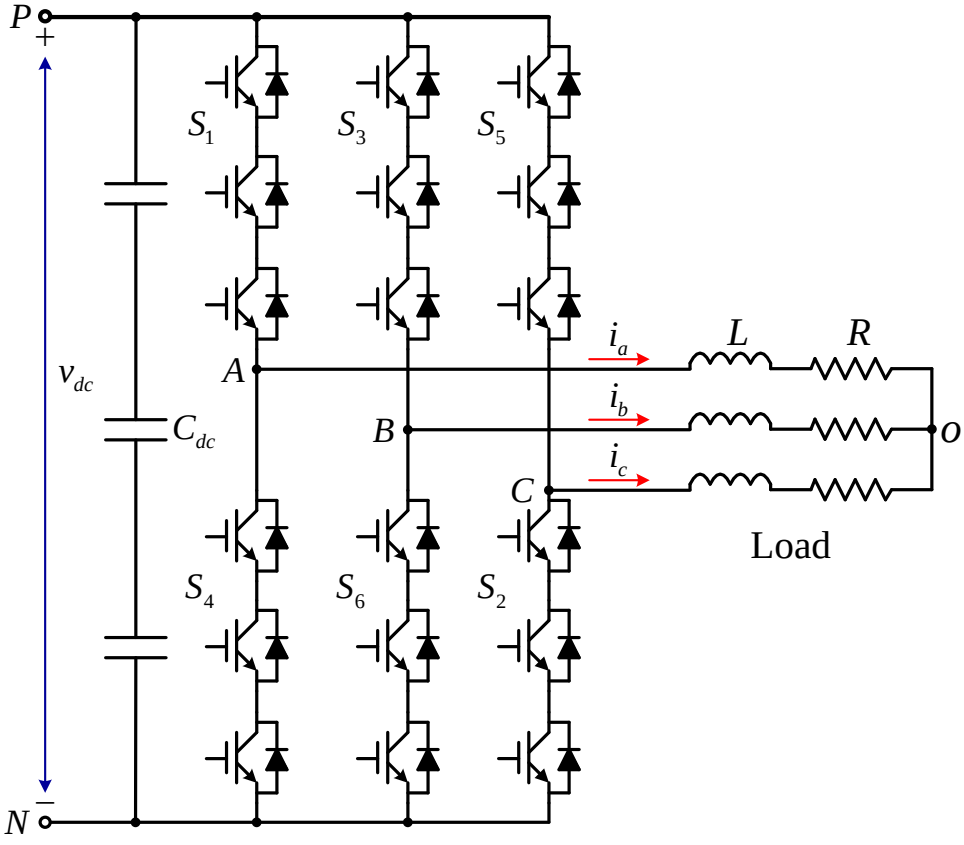


Fig. 1.2 Simplified two-level VSI for high-power applications.

1.2.2 Neutral-Point Clamped Voltage-Source Inverter

Three-level neutral-point clamped (NPC) inverter, has found wide applications in high power MV drives [15-17], as Fig. 1.3 shows. On the DC side of the inverter, the DC bus capacitor is split into two capacitors, providing a neutral point Z. The diodes connected to the neutral point,

D_{Z1} and D_{Z2}, are the clamping diodes. When switches S_2 and S_3 are turned on, the inverter output terminal A is connected to the neutral point through one of the clamping diodes. The main features of NPC inverter include reduced *dv*/*dt* and total harmonic distortion (THD) in its (alternating-current) AC output voltages in comparison with wo-level inverter discussed earlier. More importantly, the inverter can be used in MV drives to reach a certain voltage level without switching devices in series.

However, there are still some limitations with NPC inverters, including the followings.

1) Complexity of PWM schemes. Due to the increased number of switching devices, the complexity of PWM scheme is increased, especially in the corresponding SVM scheme;

2) Neutral-point voltage deviation. With a finite value for C_{dc1} and C_{dc2}, the capacitors can be charged or discharged by neutral current i_z, causing neutral point voltage deviation issue.

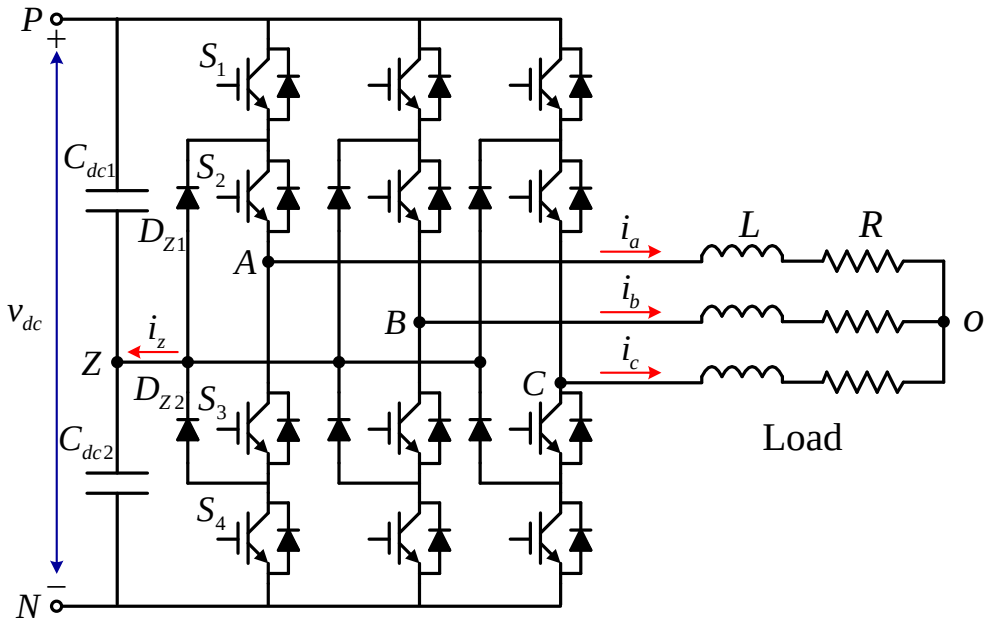


Fig. 1.3 Three-level NPC inverter.

1.2.3 Cascaded H-Bridge Multilevel Voltage-Source Inverter

Cascaded H-bridge (CHB) multilevel inverter is one of the popular converter topologies used in high power MV drives [18-20]. It is composed of a multiple units of single-phase H-bridge power cells. The H-bridge cells are normally connected in cascade on their AC side to achieve

MV operation and low harmonic distortion. In practice, the number of power cells in a CHB inverter is mainly determined by its operating voltage and manufacturing cost. A seven-level CHB multilevel inverter-fed MV drive is illustrated in Fig. 1.4. The phase-shifting transformer is an indispensable device for the CHB multilevel inverter, which provides isolated power supplies for the power cells and line current THD reduction. The CHB multilevel inverter has a number of features, as follows.

1) Modular structure. The CHB multilevel inverter is composed of multiple units of identical H-bridge power cells, which leads to a reduction in manufacturing cost;

2) Lower voltage THD and *dv*/*dt*. The inverter output voltage waveform is formed by several voltage levels with small voltage steps;

3) High-voltage operation without switching devices in series: The H-bridge power cells are connected in cascade to produce high AC voltages.

There are several drawbacks for CHB multilevel inverter, as follows.

1) High cost of phase-shifting transformer. The multi-winding transformer is the most expensive device in the CHB multilevel inverter-fed drive;

2) High component count. CHB multilevel inverter uses a large number of IGBT modules.

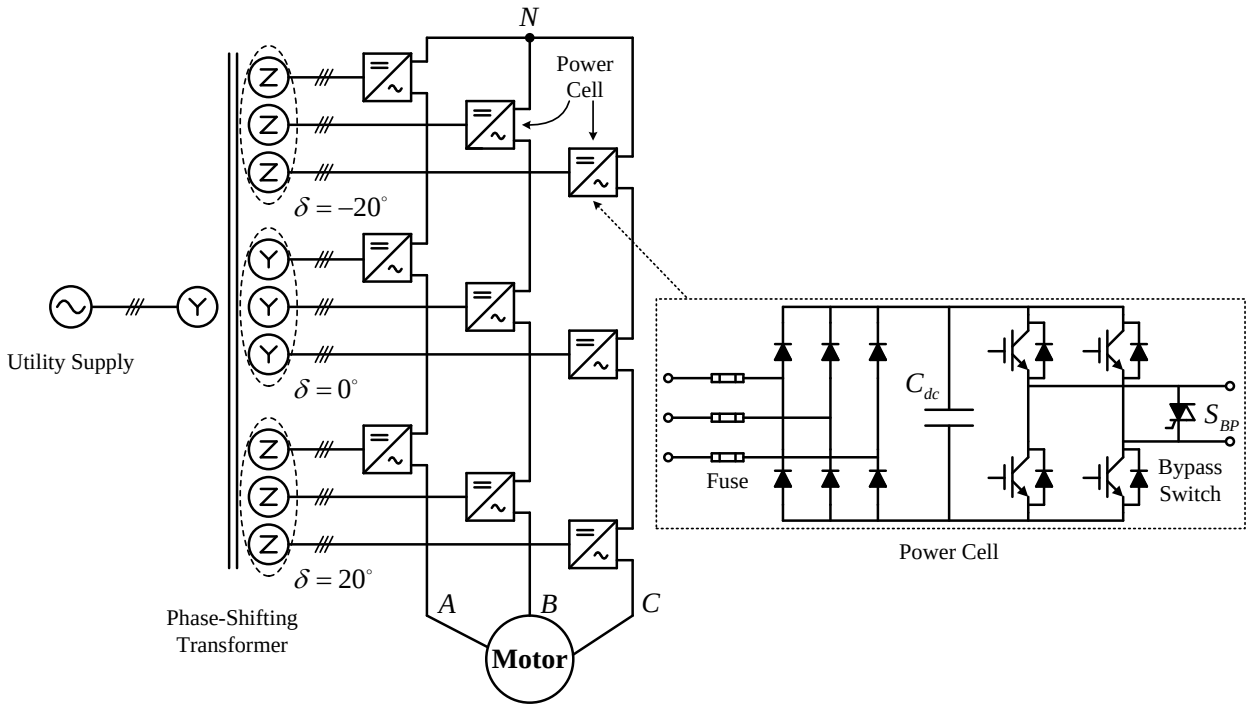


Fig. 1.4 Seven-level CHB multilevel inverter-fed drive with an 18-pulse diode rectifier.

1.3 High Power Current-Source Converter-Fed Medium-Voltage Motor Drive

The current-source inverter (CSI) technology is well-suited for MV drives. The CSI-fed drive generally features simple converter structure, motor-friendly waveforms, inherent four-quadrant operation capability and reliable fuseless short-circuit protection. Two types of CSIs are commonly used in the MV drives, namely load-commutated inverter (LCI) and PWM inverters. The power rating of the PWM CSI-fed drives is normally in the range of 1-10MW. For a higher power rating up to 100MW, the LCI is a preferred choice.

1.3.1 Load-Commutated Current-Source Inverter

One of the well-known CSI topologies is load-commutated inverter (LCI) [21]. Fig. 1.5 shows the typical LCI configuration for synchronous motor drives. The inverter employs thyristors as switching devices which can just be naturally commutated by the load voltage with a leading power factor. Therefore, the ideal load for LCI is synchronous motors operating at a

leading power factor. On the DC side of the inverter, a DC choke, L_{dc}, is required to provide a smooth DC current, I_{dc}.

The LCI-fed motor drive features low manufacturing cost and high efficiency due to the use of low-cost thyristor devices and lack of PWM operation. LCI is a popular solution for very large drives, where the initial investment and operating efficiency are of great importance.

The main drawback of LCI drive is its limited dynamic performance. In addition, the power losses in the motor are high due to the large amount of harmonics in stator currents [22].

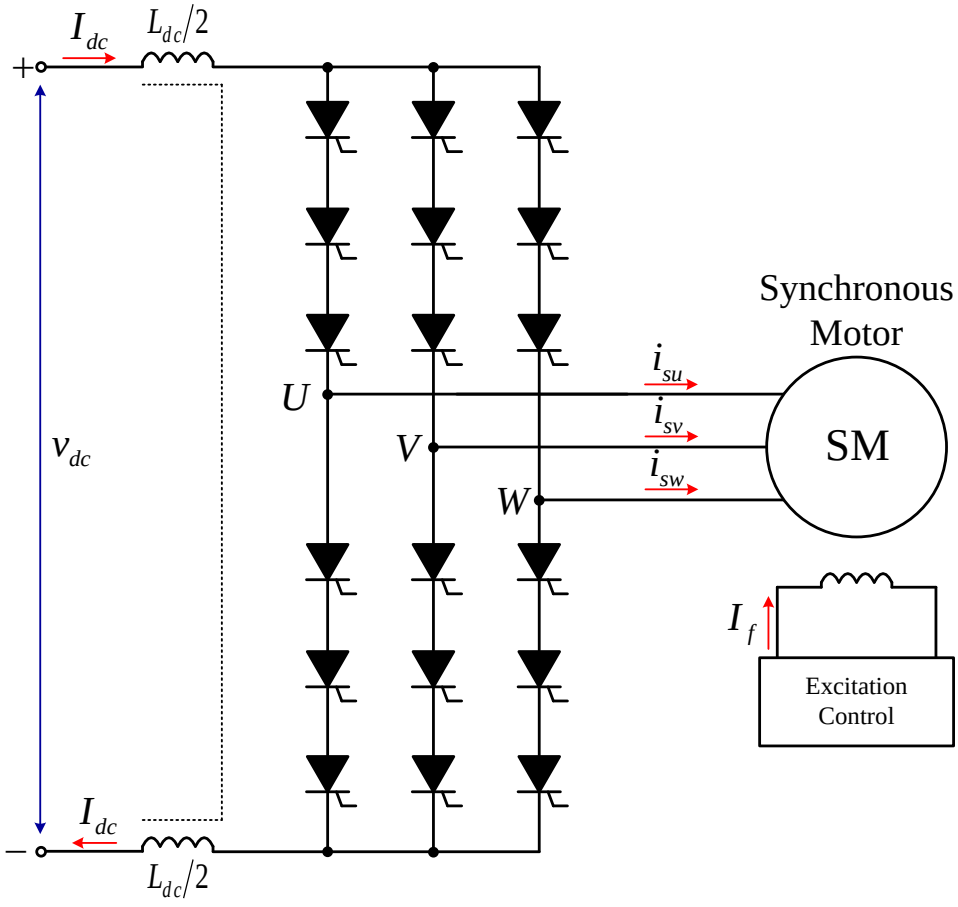


Fig. 1.5 LCI for synchronous motor drives.

1.3.2 Pulse-Width Modulated Current-Source Inverter

An idealized PWM CSI is shown in Fig. 1.6. The inverter is composed of six symmetry gate commutated thyristor (SGCT) devices, with reverse voltage blocking capability. The inverter

produces a defined PWM current, i_{wx} (x=a, b, c). The CSI normally requires a three-phase capacitor, C, at its output to assist the commutation of the switching devices. Besides, the capacitor also acts as a harmonic filter, improving the load current and voltage waveforms, of which value can be reduced accordingly with the increase of switching frequency.

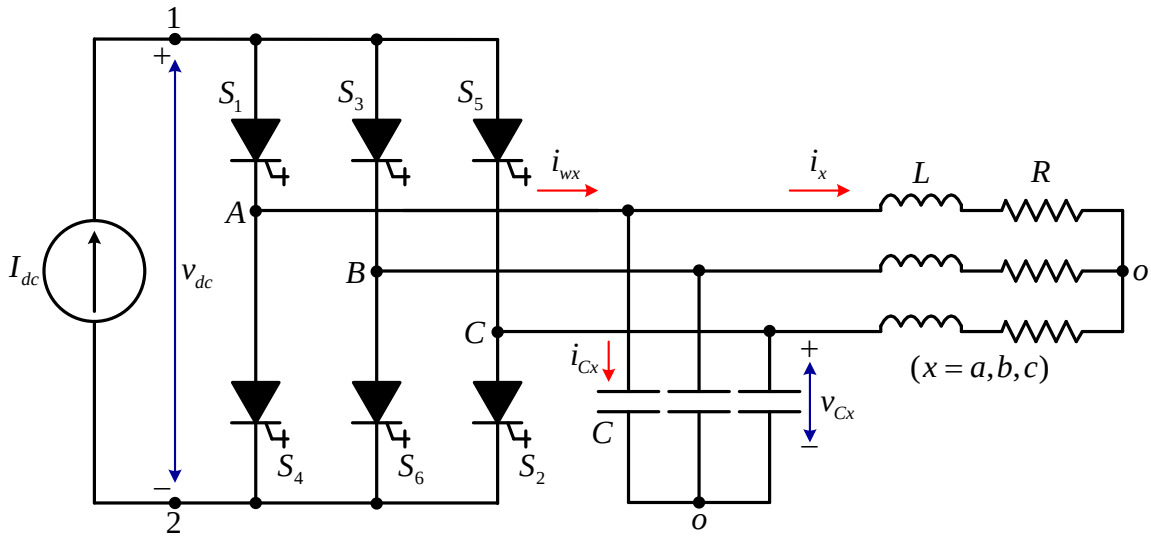


Fig. 1.6 Simplified SGCT based PWM CSI.

The DC current source can be generated by an SCR or PWM current-source rectifier (CSR) with a DC current feedback control. To make the DC current, I_{dc}, smooth and continuous, a DC choke, L_{dc}, is an indispensable device for the CSR.

The CSI-fed MV drive has the following features.

1) Simple converter topology with low component count. The converter topology is very simple. Both CSR and CSI use SGCT devices that do not require antiparallel freewheeling diodes, leading to a minimum component count;

2) Simple PWM schemes. Only six gate signals are required for the six groups of synchronous switches per converter;

3) Motor friendly waveforms. The motor voltage and current waveforms are close to sinusoidal and does not contain any voltage steps with high *dv*/*dt*;

4) Reliable fuseless short circuit protection. In case of short circuit at the inverter outputs, the rate of rise of the DC current is limited by the DC choke, providing sufficient time for the drive controller to react;

5) Long input and output cables. Due to near sinusoidal input and output waveforms, there are virtually no limit on the length of the cables connecting the transformer to the rectifier or connecting the inverter to the motor;

6) Four-quadrant operation and regenerative braking capability. The power flow in the CSI drive is bidirectional.

1.3.3 Configuration of High Power Current-Source Converter-Fed Medium-Voltage Motor Drive

1.3.3.1 CSI-Fed MV Motor Drive with Single-Bridge PWM CSR

Fig. 1.7 shows a typical CSI-fed drive using a single-bridge PWM CSR as the active front end. The rectifier and inverter have an identical topology using SGCTs. With the GCT voltage rating of 6000V and two GCTs connected in series in each of the converter branches, the drive is capable of operating at the utility power supply voltage of 4160V, which is line-to-line root mean square (rms) value.

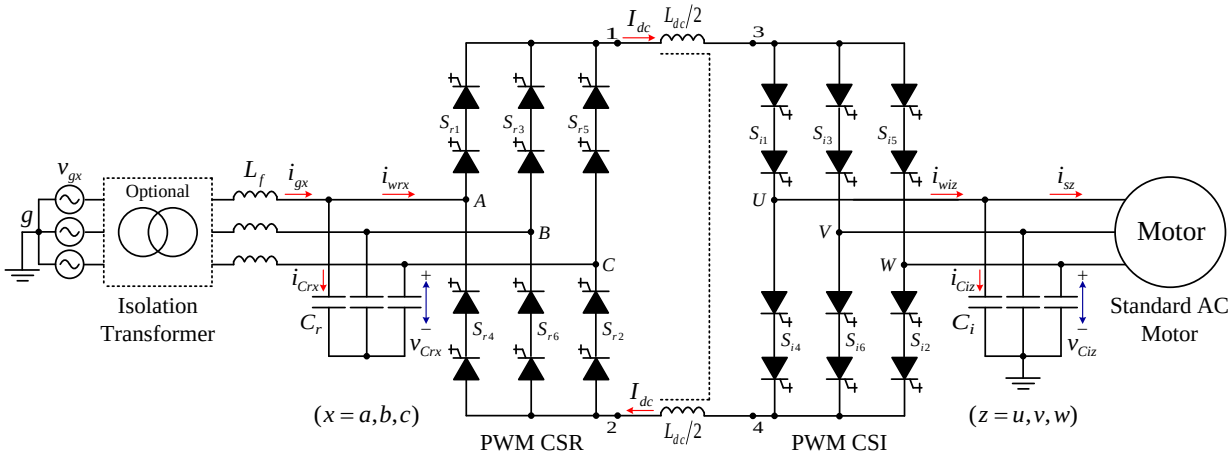


Fig. 1.7 A typical 4160V CSI-fed drive with a PWM rectifier and inverter.

The illustrated configuration consists of an MV induction motor (IM), three-phase filter capacitors, and a full rating back-to-back PWM current-source converter (CSC). The PWM CSR

is connected with the PWM CSI through a DC choke. The DC choke, L_{dc}, is required to smooth the DC current. The choke usually has a magnetic core with two coils, one connected in the positive DC bus and the other in the negative bus. Such an arrangement is preferred in practice for CMV reduction [23]. To limit DC link current ripples to an acceptable level (lower than 15%), the size of the DC choke is normally around 1pu.

The line side of the CSR can be equivalently represented by a line inductance, L_f, which denotes the total inductance between the utility power supply and the rectifier, including the equivalent inductance of the utility power supply, the leakage inductance of an isolation transformer if any, and the inductance of a line reactor for line current THD reduction. The line inductance, L_f, is normally in the range of 0.1 to 0.15pu. As shown in Fig. 1.7, a number of switching devices can be connected in series in each phase leg to meet the MV level requirements. The input and output three-phase AC capacitors, C_r and C_i, help the switching devices' commutations and filter out current harmonics. The capacitor size is mainly dependent on the rectifier and inverter's switching frequencies. The value of capacitor is normally in the range of 0.3 to 0.6pu for high power MV level applications with a switching frequency below 1kHz.

Since the rectification and inversion processes in the CSC-fed drive generate CMVs. If not mitigated, the CMVs would appear on the motor, causing premature failure of its winding insulation. The problem can be effectively solved by introducing an isolation transformer and grounding the neutral of the inverter filter capacitor as shown in Fig. 1.7. In doing so, the motor is not subject to any CMVs. Therefore, this kind of CSI-fed drive is suitable for retrofit application, where standard AC motors are usually used. However, isolation transformer increases the total cost of the whole system. On the other hand, some CMV reduction schemes can be applied to reduce the peak value of CMV through appropriate deployment of the switching states at both CSR and CSI sides, which reduces the dependency on isolation transformer.

1.3.3.2 CSI-Fed MV Motor Drive with a Dual-Bridge PWM CSR

Fig. 1.8 illustrates a 4160V CSI-fed drive with a dual-bridge PWM rectifier, in which a phase shifting transformer is utilized to cancel the 5th, 7th, 17th, and 19th harmonics. The rectifier uses selective harmonic elimination (SHE) modulation scheme to eliminate the 11^{th} and 13^{th} harmonics. The line current waveform is virtually sinusoidal [24, 25]. This drive is suitable for applications that require extremely low line current distortion. However, a bulky phase shifting transformer is indispensable in the system, which increases the footprint, and adds the initial cost.

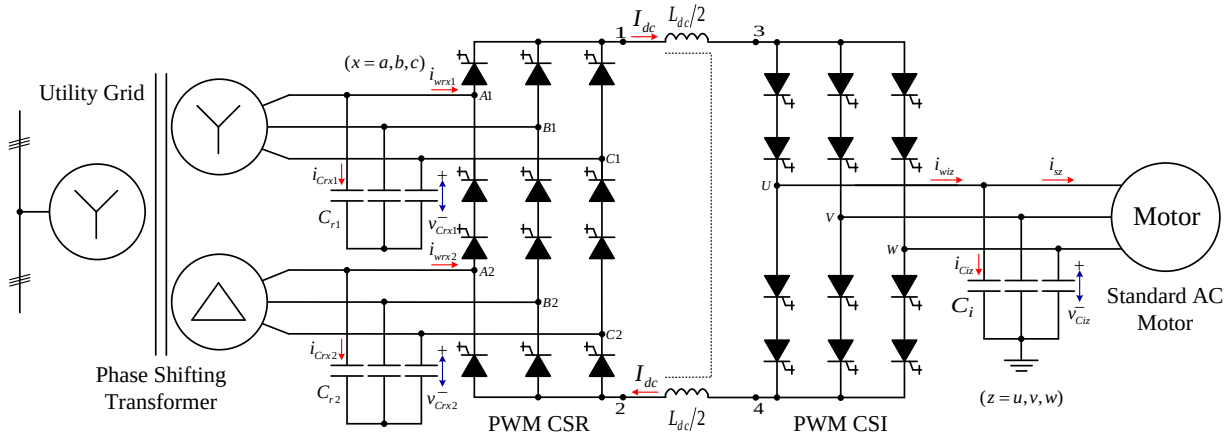


Fig. 1.8 4160V CSI-fed drive with dual-bridge PWM rectifier for sinusoidal inputs.

1.3.3.3 Transformerless CSI-Fed MV Motor Drive

Fig. 1.9 shows the configuration of a transformerless CSI-fed drive, where an integrated DC choke is used. The choke can provide two inductances, a differential inductance, L_{dc}, that is inherently required by the CSI-fed drive and a common-mode inductance, L_{cm}, that can block the CMV. The use of the integrated DC choke leads to the elimination of isolation transformer, resulting in a significant reduction in manufacturing and operating costs. To ensure that the motor is not subject to any CMVs, the neutral points of the line- and motor-side filter capacitors are connected together directly or through a small *RL* network. However, the use of the integrated DC choke increases the complexity of manufacturing.

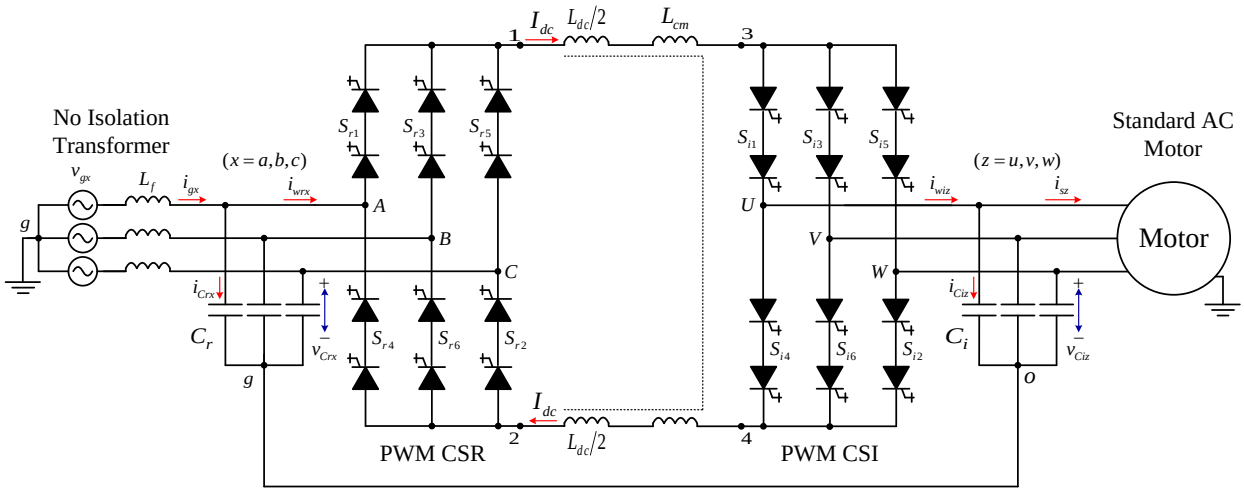


Fig. 1.9 A transformerless CSI-fed MV motor drive with an integrated DC choke.

1.3.4 Technical Challenges

The technical challenges for CSC-fed MV drives differ in many aspects from those for low-voltage AC drives. These challenges can be generally divided into three groups: the challenges related to CSR, the challenges associated with CSI, and the general drive system requirements.

1.3.4.1 CSR-Side Challenges

1) Line current distortion. Though there are large capacitors in CSR to reduce line current THD, line current drawn by CSR is normally distorted, and it also causes notches in voltage waveforms. The distorted current and voltage waveforms can cause numerous problems such as nuisance tripping of computer-controlled industrial processes, overheating of transformers, equipment failure, computer data loss, and malfunction of communications equipment. Nuisance tripping of industrial assembly lines often leads to expensive downtime and ruined product. Hence, the quality of line current needs to be improved;

2) *LC* resonance suppression. The large capacitors in CSR form *LC* resonant circuits with the filter reactors. The *LC* resonant modes may be excited by the harmonic voltages in utility power supply or harmonic currents produced by CSR. Since the utility power supply at MV level normally has very low line resistance, the lightly damped *LC*

resonances may cause severe oscillations or over-voltages that may destroy the switching devices and other components in CSR;

3) Line power factor. High line power factor is a general requirement for all electric equipment, which is especially important for high-power MV drives. However, due to the large capacitors in CSR, it is always an issue to maintain a maximum possible power factor for CSR at different operating points.

1.3.4.2 CSI-Side Challenges

1) Limited dynamic performance. This is mainly due to the use of a DC choke and a three-phase capacitor connected at the output of CSI. To smooth DC current, a DC choke is inevitable in CSI-fed drives. Since the magnitude of inverter output current is not directly regulated by modulation index instead of adjusting DC current through CSR, the DC choke will limit the changing rate of DC current. However, more advanced control schemes can be applied into CSR in order to improve the dynamic response of DC current regulation. On the other hand, the large capacitor (normally 0.3pu to 0.6pu) at the output of CSI also has significant influence on the transient process of CSI-fed drives. Since the stator currents are not directly controlled by the PWM currents of CSI, the transient process of capacitor currents will lead to large torque overshoot and stator current oscillation in CSI-fed drives. Unfortunately, traditional FOC for CSI-fed IM drive totally neglects the transient responses of the capacitor currents, which makes the regulation of the stator currents during transients more difficult;

2) Reduction of electromagnetic torque pulsations. Though the large capacitor at the outputs of CSI improves the waveforms of stator voltage and current, the reduction on torque pulsations is always a noteworthy issue. Torque pulsation may result in shaft failures, couplings and damage of other mechanical equipment, when the natural frequency of the mechanical system coincides with the frequency of the torque pulsations. Better control and modulation schemes, which achieve smaller distortion on stator current, can be developed and applied for CSI to realize smaller torque pulsations;

3) Potential *LC* resonances. Similar as CSR, the motor-side capacitors constitute resonant modes with the motor leakage inductors as well. Even though some damping effects can

be provided by motor winding resistance, the motor-side capacitors still need to be carefully sized, and modulation scheme with reduced low order harmonics is required to be considered at the design stage of CSI-fed drives.

1.3.4.3 General MV Motor Drive System Challenges

1) Common-mode voltage stress. The switching action of CSR and CSI normally generates CMVs. The CMVs are essentially zero-sequence voltages superimposed with switching noise. If not mitigated, they will appear on the neutral of the stator winding with respect to ground, which should be zero when the motor is powered by a three-phase balanced utility supply. Furthermore, the motor line-to-ground voltage, which should be equal to the motor line-to-neutral (phase) voltage, can be substantially increased due to the CMVs, leading to the premature failure of the motor winding insulation system. As a consequence, the motor life expectancy is short-ended;

2) Device switching frequency. The device switching loss accounts for a significant amount of the total power losses in MV drives. The switching loss minimization can lead to a reduction in the operating cost when the drive is commissioned. The physical size and manufacturing cost of the drive can also be reduced due to the reduced cooling requirements for the switching devices. In practice, the device switching frequency is normally around 500Hz for GCT devices. However, in order to fix switching frequency of SVM at a low value, a relatively long sampling period is normally used, which results in the inclusion of low-order harmonics in the PWM waveforms. In the case of SHE modulation, though low-order haromonics can be perfectly eliminated through pre-calculated switching angles, the flexibility of SHE modulation is very limited, since a new set of switching angles needs to be calculated correnponding to different output frequencies and modulation indexes.

1.4 Review on Traditional Modulation and Control Schemes of High Power Current-Source Converter for Medium-Voltage Motor Drive

The development of control techniques for power converters is an ongoing research topic [43-46]. A summary of the most established control techniques is summarized in Fig. 1.10. The classical control schemes include linear and hysteresis control, while the sliding-mode, intelligent and predictive control belong to the advanced control category.

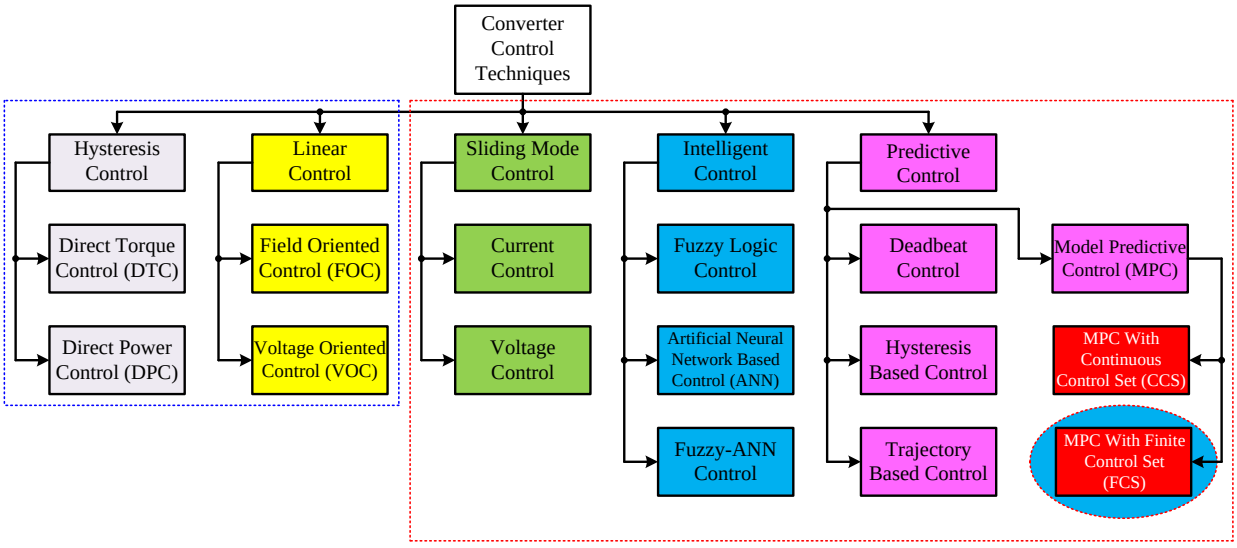


Fig. 1.10 Classification of control techniques used for power converters.

The classical control techniques are simple and widely accepted by various power converters. The classical control approach uses cascaded linear PI regulators PWM or SVM. The favorable approach to use classical control scheme with PWM or SVM is its fixed switching frequency. The lower switching frequency operation is an important requirement at MV level. This section mainly introduces the existing traditional control schemes for CSC-fed IM drive and the respective shortcomings of them. First, operating principle and modulation schemes of CSC are presented. Mathematical models of CSI-fed IM drive in stationary or *dq*-axis synchronous frames are analyzed. Then, the traditional control schemes of CSR and CSI-fed IM drive are classified and discussed. Finally, several methods tackling some special issues in CSI-fed IM drive are introduced.

1.4.1 Traditional Modulation Schemes

Various modulation techniques have been developed for PWM CSI, including trapezoidal PWM (TPWM), selective harmonic elimination PWM (SHE-PWM), and space vector modulation (SVM) [26-29]. In a back-to-back PWM CSC system, the CSR and CSI are similar in terms of modulation. Therefore, the above-mentioned modulation schemes can be applied to both of them. SHE-PWM scheme is considered the best in term of THD and therefore is usually used in CSRs with a fixed input frequency of 60Hz. However, in CSIs, due to variable frequency operation, various modulation schemes might be used for different operating frequencies.

The simplified diagram of a PWM CSI is shown in Fig. 1.6. The inverter is composed of six SGCT devices. The inverter produces a defined PWM output current i_w. At the DC side of the inverter is an ideal DC current source I_{dc}. The switching pattern design for the CSI should generally satisfy two conditions.

1) The DC current should be continuous;

2) The inverter PWM current should be defined by the switching patterns for a CSC.

The two conditions can be translated into a switching constraint, that is at any instant of time (excluding commutation intervals) there are only two switches conducting, one in the top half of the bridge and the other in the bottom half.

1.4.1.1 Trapezoidal PWM

The principle of trapezoidal PWM for PWM CSI is shown in Fig. 1.10, where the trapezoidal modulation wave is represented by v_m and the triangular carrier wave is represented by v_{cr}. Similar to the carrier-based PWM schemes for VSI-fed drive, the gate signal is generated by comparing v_m with v_{cr}. However, trapezoidal PWM does not generate any gate signals in the center $\pi/3$ interval of the positive half cycle and in the negative half cycle of the fundamental frequency. Such arrangements can satisfy switching constraints of CSC.

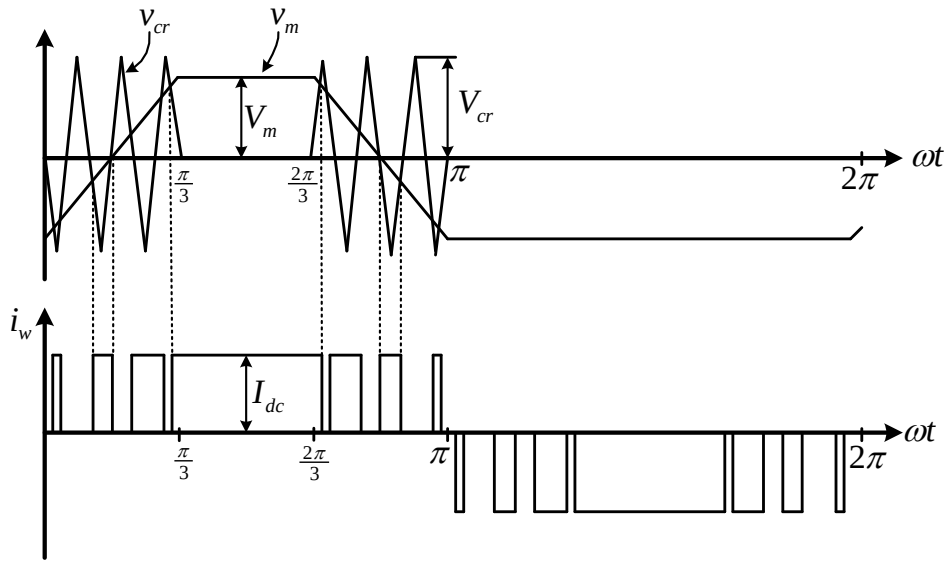


Fig. 1.11 Trapezoidal PWM.

1.4.1.2 Selective Harmonic Elimination PWM

SHE-PWM technique is an offline modulation scheme that can eliminate a number of unwanted low-order harmonics with a limited number of pulses. In this technique, the switching angles are precalculated and then imported into a digital controller for implementation. In order to achieve a better harmonic profile and to reduce the complexity in finding switching pattern solutions, the calculated pulses are normally arranged in such a way that the derived PWM waveform has a quarter-wave symmetrical shape. In high power applications, where SHE-PWM is usually preferable, low switching frequency is needed to reduce the switching losses. Therefore, five or seven switching angles per quarter of one cycle are preferred. In the case shown in Fig. 1.11, five pulses are employed per half cycle. This figure shows a typical SHE-PWM pattern that satisfies the switching constraint of CSC. There are five pulses per half cycle with five switching angles in the first quarter. However, only two out of the five angles, β_1 and β_2, are independent. Given these two angles, all other switching angles can be derived.

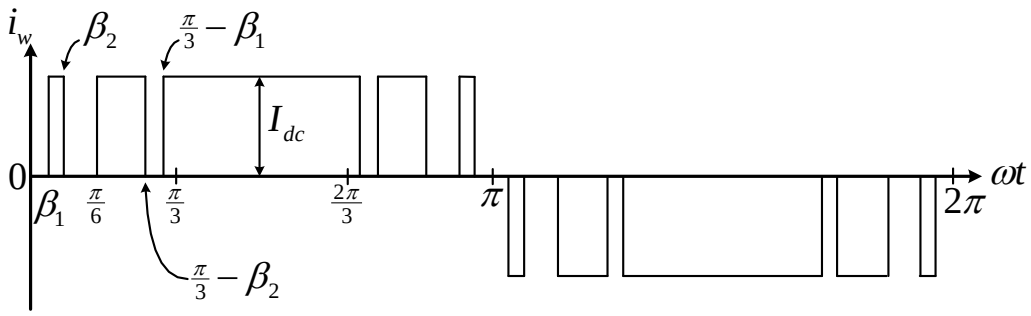


Fig. 1.12 Five-pulse SHE PWM pattern for CSC.

The main disadvantage of SHE-PWM is a lack of flexibility due the offline calculated set of angles only valid at a certain modulation index. In practice, SHE-PWM is normally used with a fixed modulation index. If variation of the modulation index is needed, the solutions for all the required modulation indices have to be calculated offline and stored in a look-up table (LUT) with their set of angles. This adds more complexity to the modulation scheme implementation and it is not practical in real applications. Moreover, the calculation of SHE-PWM angles with a large number of pulses per fundamental cycle sometimes involves transcendental equations that have no solutions, which prevents SHE-PWM from being applied to a full frequency range.

1.4.1.3 Space Vector Modulation

Similar to VSC, CSC can also be controlled by SVM scheme. A typical space vector diagram for a CSC is shown in Fig. 1.12 (a), where $\vec{I}_1$ to $\vec{I}_6$ are active-state vectors and $\vec{I}_0$ is the zero-state vector. The active-state vectors form a regular hexagon with six equal sectors, whereas the zero-state vector $\vec{I}_0$ lies at the center of the hexagon.

The desired three-phase output current of CSC can be expressed as a reference vector $\vec{I}_w^*$ rotating counter clockwise in the space-vector plane. For a given length and position, $\vec{I}_w^*$ can be synthesized by three nearby stationary vectors, based on which the switching states can be selected and gating signals for the switches can be generated. The inverter output frequency corresponds to the rotating speed of $\vec{I}_w^*$, and the magnitude of the output current can be adjusted by the length of $\vec{I}_w^*$. The ratio between the magnitudes of $\vec{I}_w^*$ and the DC link current I_{dc} is the modulation index *m* of the inverter. The angle θ_w^* is defined as the phase displacement between

the reference vector and α-axis of the space vector plane. As shown in Fig. 1.12 (b), the reference vector $\vec{I}_w^*$ can be synthesized by the adjacent vectors based on the ampere-second balance principle. With a sufficiently small sampling period T_s, the reference vector $\vec{I}_w^*$ can be considered constant during T_s. Under this assumption, the reference vector $\vec{I}_w^*$ can be synthesized by vectors $\vec{I}_1$, $\vec{I}_2$ and $\vec{I}_0$. The ampere-second balancing equation can be given by

$$\begin{cases} \vec{I}_w^* \cdot T_s = \vec{I}_1 \cdot T_1 + \vec{I}_2 \cdot T_2 + \vec{I}_0 \cdot T_0 \\ T_s = T_1 + T_2 + T_0 \end{cases} \tag{1.1}$$

The vector dwelling time can be derived by solving (1.1)

$$\begin{cases} T_1 = m \cdot \sin\left(\pi/6 - \theta_{\text{sec}}\right) \cdot T_s \\ T_2 = m \cdot \sin\left(\pi/6 + \theta_{\text{sec}}\right) \cdot T_s \\ T_0 = T_s - T_1 - T_2 \end{cases} \tag{1.2}$$

where θ_{sec} is the displacement angle of the reference vector within a certain sector. Therefore, its value is in the range of $-\pi/6 \le \theta_{\text{sec}} < \pi/6$. Once the vector dwelling time are calculated, the vector sequence in a sampling period needs to be determined for the generation of PWM pulses. Different sequence patterns can be generated, however, the selection of the sequences are associated with different switching frequencies and harmonic profiles. One of the most widely-used sequences is called a three-segment sequence. The switching pattern generated with this sequence has the advantage that the transition from one sector to another requires only one switching action. Hence, in each sampling period, three switch-on and three-switch-off actions happen, which is equivalent to three full device switching actions. Therefore, if the sampling frequency f_s is equal to $1/T_s$, the corresponding device switching frequency f_{sw} is half of f_s.

Though SVM, as an online modulation scheme, possesses a lot of merits, its performance in high power CSC is limited by a relatively long sampling period, due to the requirement on low switching frequency. Since it is inaccurate to consider that the location of $\vec{I}_w^*$ is fixed during the whole sampling period, the resulting output PWM waveform contains low-order harmonics,

such as 5^{th} and 7^{th} order harmonics, which heavily influences on the distortion of load current, and is not easy to be elimintated.

In order to cope with this issue, an improved SVM, called multi-sampling SVM (MS-SVM), is presented in [30]. In MS-SVM, the angle and the magnitude of $\vec{I}_w^*$ are updated several times during one sampling period, so the dwell time for each current vector can be adjusted more frequently. Finally, with MS-SVM, the low-order harmonic components in ouput PWM currents can be effectively mitigated. However, MS-SVM has two imperfections. First, MS-SVM involves more chanlleges on realization. When realizing SVM on a digital signal processor (DSP) based platform, only one interruption, normally PWM interruption, is enabled to execute the calculation of control scheme. For MS-SVM, since the calculation of control scheme needs to be executed several time to update $\vec{I}_w^*$ during one sampling period, more interruptions are required to be enabled, which on one hand requires DSP with higher performance, and on the other hand introduces the potential risk between several interruptions into realization. Moreover, though MS-SVM can fulfill satisfying steady state performance, its transient responses is still restricted by the synthesis process. Since the effect of $\vec{I}_w^*$ is applied through the synthesis process, which is conducted over the whole sampling period, even if $\vec{I}_w^*$ can be faster updated in MS-SVM, $\vec{I}_w^*$ cannot be directly taken into effect to manipulate the output PWM currents during transient conditions, and the dynamic performance of MS-SVM is still very limited.

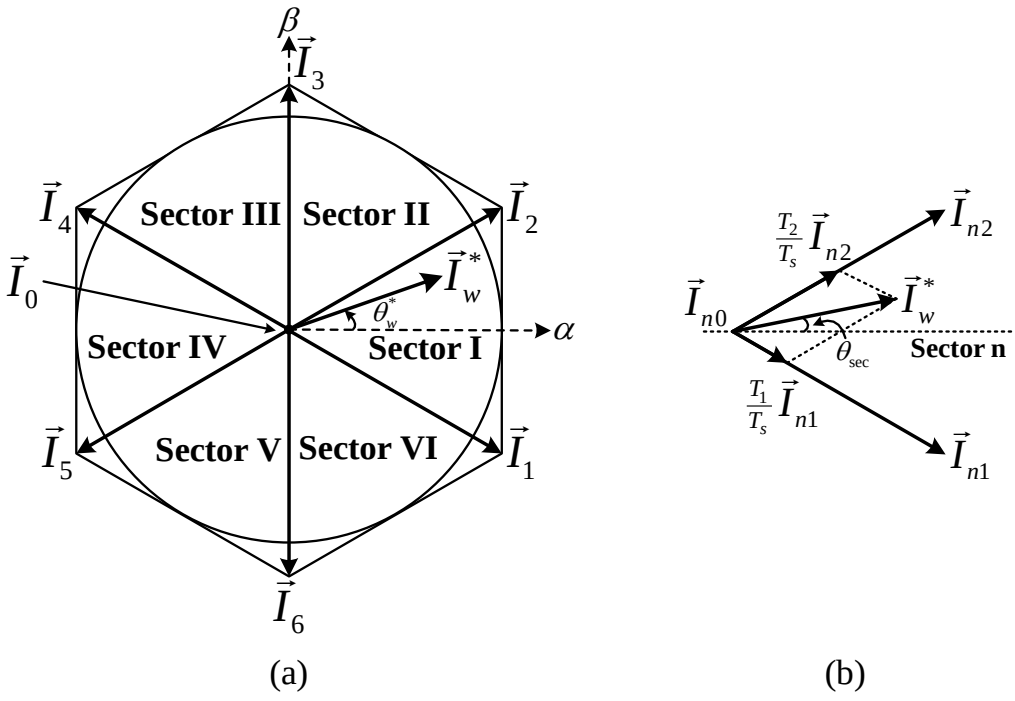


Fig. 1.13 SVM scheme: (a) space vector location and (b) vector synthesis.

1.4.2 Traditional Control Schemes of High Power Current-Source Rectifier

The simplified configuration of a CSR is shown in Fig. 1.13, where a CSR is connected to a DC load resistor R_{dc} through the DC link inductor.

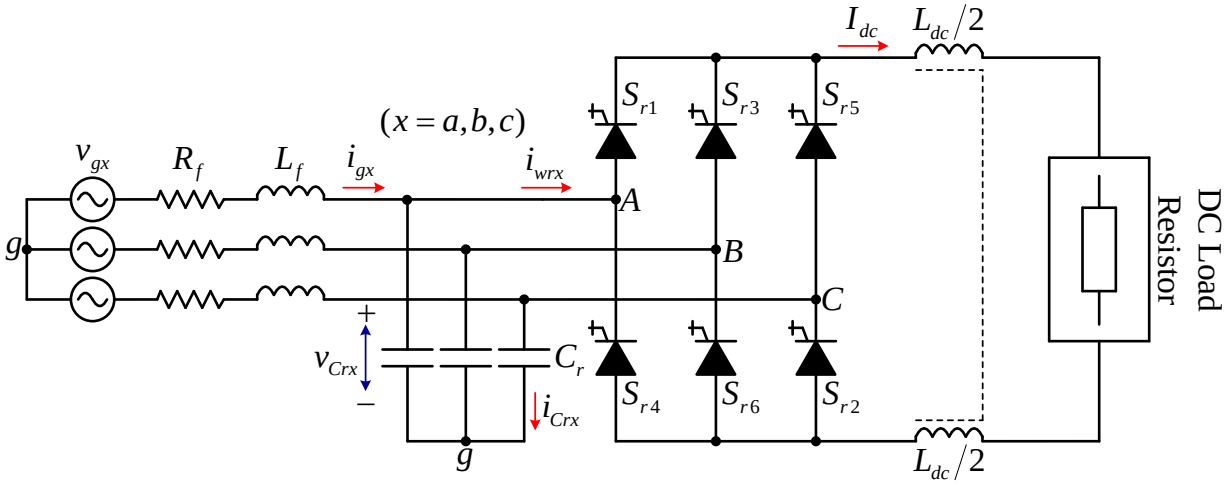
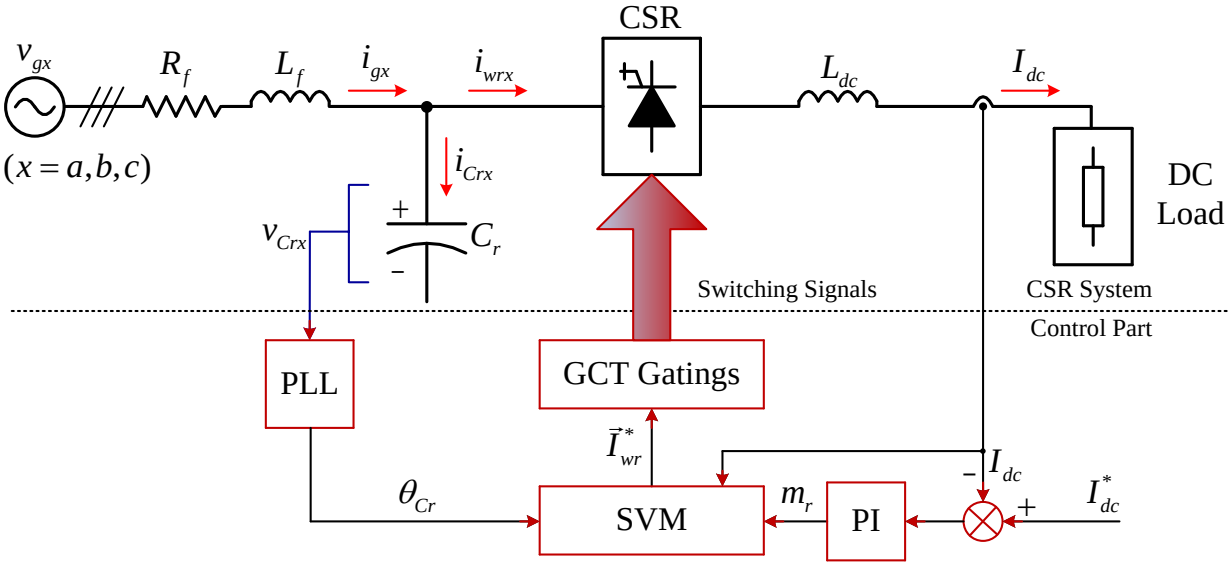


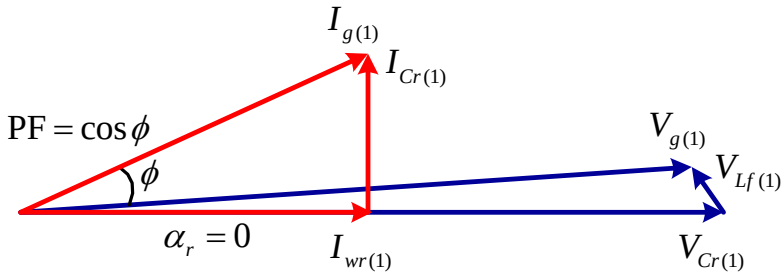
Fig. 1.14 Configuration of a CSR with a DC load resistor.

1.4.2.1 Modulation Index Control

Fig. 1.14 (a) shows the control block diagram of modulation index control for CSR [31, 32]. The output of the DC current controller is the modulation index m_r. Then, the modulation reference vector synchronized to the capacitor voltage angle θ_{Cr} is generated and sent to PWM modulation stage for generation of switching signals. Since a variable modulation index is needed in the scheme, SVM is normally used in the modulation stage. Fig. 1.14 (b) shows the phasor diagram of the rectifier with modulation index control, where all the voltage and current phasors, such as $I_{g(1)}$, $I_{wr(1)}$, and $V_{Cr(1)}$, only represent their fundamental-frequency components. The PWM current $I_{wr(1)}$ is in phase with the filter capacitor voltage $V_{Cr(1)}$ while the line current $I_{g(1)}$ leads the utility supply voltage $V_{g(1)}$ by the power factor angle ϕ due to the capacitor current $I_{Cr(1)}$. However, the leading line-side power factor is a disadvantage of modulation index control.



(a)



(b)

Fig. 1.15 Modulation index control: (a) block diagram and (b) phasor diagram.

1.4.2.2 Delay Angle Control

The control block diagram and phasor diagram of delay angle control is shown in Fig. 1.15 [33, 34]. In delay angle control, modulation index is fixed, normally chosen as near unity. Due to a constant modulation index, both SVM and SHE-PWM schemes can be used in it. The delay angle between filter capacitor voltage and PWM current is adjusted to realize the DC current control. As Fig. 1.15 (a) shows, a feed-forward of load DC voltage is added to improve the dynamic performance of delay angle control. In Fig. 1.15 (b), the delay angel control provides a lagging current and improves the line-side power factor, which can compensate part of or even total the leading current imposed by the filter capacitor. However, since the lagging current is variable according to different operating state of CSR, accurate power factor control of CSR cannot be guaranteed with delay angle control.

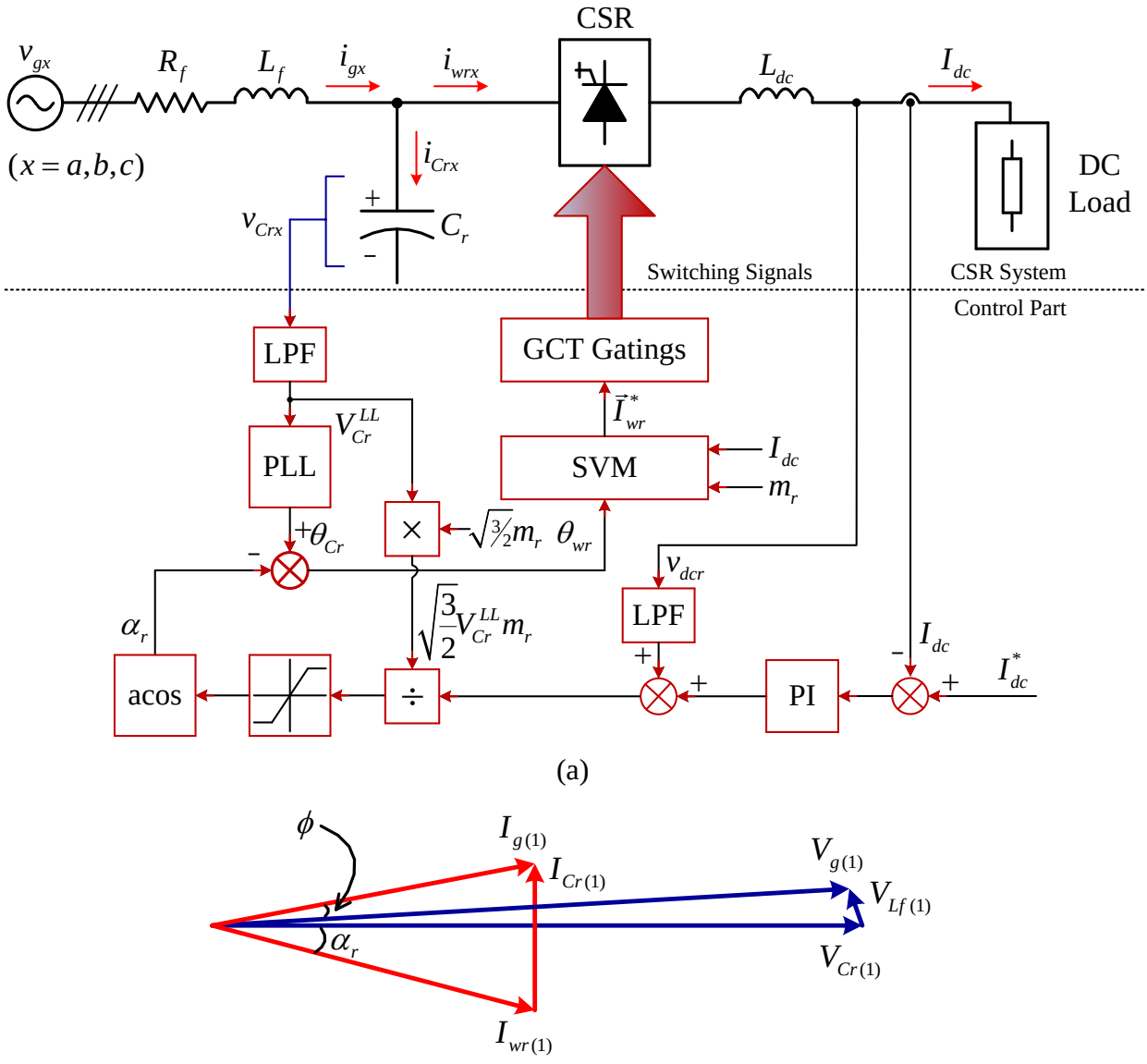


Fig. 1.16 Delay angle control: (a) block diagram and (b) phasor diagram.

1.4.2.3 Active Damping Method

In PWM CSR, the capacitor C_r forms an *LC* resonant circuit with the filter reactor L_f. The *LC* circuit in a high power CSR is lightly damped due to a very low equivalent line resistance R_f, normally from 0.005pu to 0.01pu, which is the total resistance of the distribution line, filter reactor and isolation transformer (if any). The *LC* resonant mode may be excited by the

harmonic voltages in the utility power supply and harmonic currents produced by the rectifier. The single-phase equivalent circuits of the two modes of resonance are shown in Fig. 1.16.

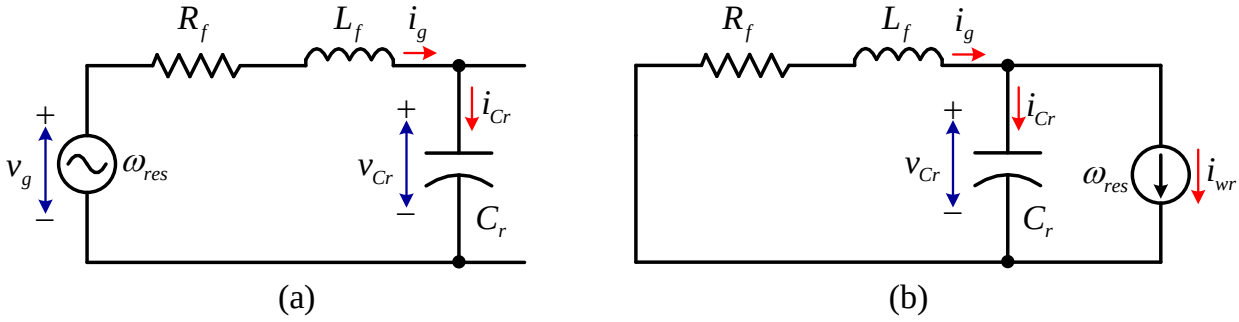


Fig. 1.17 Series and parallel resonant modes in a CSR: (a) series resonant mode (b) parallel resonant mode.

The transfer functions of these two resonant modes can be expressed as

$$G_s(s)=\frac{I_g(s)}{V_g(s)}=\frac{sC_r}{C_rL_fs^2+C_rR_fs+1} \tag{1.3}$$

$$G_p(s)=\frac{I_g(s)}{I_{wr}(s)}=\frac{1}{C_rL_fs^2+C_rR_fs+1} \tag{1.4}$$

Neglecting R_f, the resonant frequency of the series and parallel modes can be found as $1/\sqrt{C_rL_f}$. With the capacitor in the range of 0.3 and 0.6pu and the filter reactor between 0.1 and 0.15pu, the resonant frequency is in the range of 3.3 to 5.8pu. With the switching frequency around 500Hz, no matter TPWM or SVM schemes contain 5^{th} and 7^{th} order harmonics, which would be very close to the resonant frequency. Though SHE-PWM can eliminate all the low order harmonics, it cannot suppress series mode resonance as an off-line modulation scheme.

It is well known that an *LC* resonance can be suppressed by adding a physical damping resistor to the resonant circuit. For a CSR, a damping resistor R_{damp} can be connected in parallel with the capacitor. However, adding a resistor to the system results in additional power losses and thus is not practical, especially in MV drives. The capacitor voltage feedback or virtual resistor based active damping method is to use the CSR to emulate a damping resistance [31, 32, 35]. The damping current i_{damp} can be calculated as v_{Cr}/R_{damp} and generated by the CSR through

adjusting the modulating index dynamically. In fact, this method is essentially a capacitor voltage feedback process. The control block diagram is shown in Fig. 1.17.

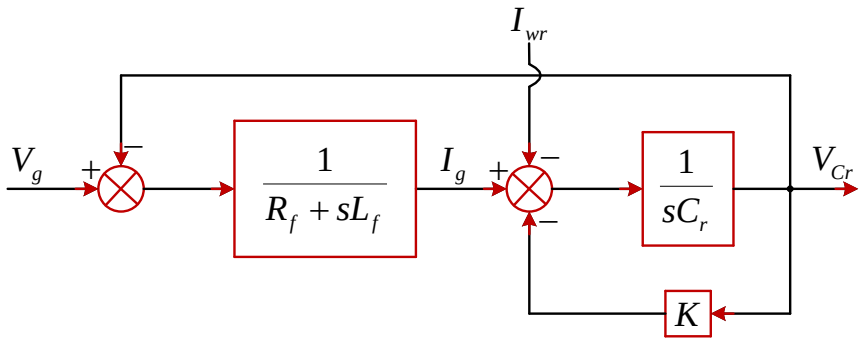


Fig. 1.18 Block diagram of capacitor voltage feedback based active damping method.

where the gain K is just equal to $1/R_{damp}$, which increases the damping ratio and suppresses both series and parallel mode resonances.

This active damping method is normally associated with the modulation index control of CSR. The block diagram is shown in Fig. 1.18, which is conducted in *dq*-axis synchronous frame, respect to capacitor voltage. The fundamental component of v_{Cr} becomes a DC component in the synchronous frame, which is eliminated with a high-pass filter (HPF) to avoid influence on the DC current control. The remaining signal represents the high frequency harmonic voltages $v_{Cr(h)}$ in the synchronous frame. The calculated damping current i_{damp} is normalized to the DC current and converted into the damping modulation index $m_r^{'}$. The damping modulation index $m_r^{'}$ is summed with the modulation index m_r for DC current control in the SVM scheme. Due to variable modulation index required, SVM with switching frequency of several hundred Hz is preferred for this method. However, the virtual resistor based active damping method still suffers from some problems, which can be classified as modulation index saturation, virtual damping resistance selection and degraded transient response [35].

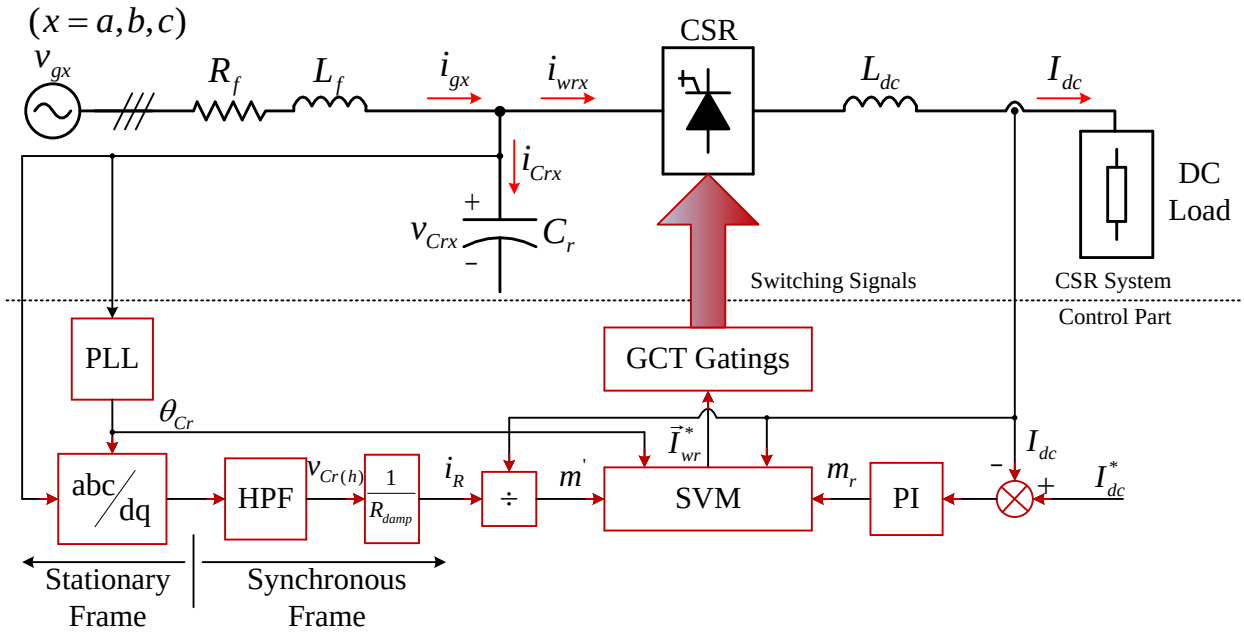


Fig. 1.19 Block diagram of modulation index control with active damping method.

1.4.3 Traditional Control Schemes of High Power Current-Source Inverter-Fed Induction Motor Drive

The field-oriented control (FOC) is mostly applied control scheme for high power CSI-fed MV IM drive [36, 37]. The field orientation usually denotes the rotor flux orientation, which is extensively used in AC motor drives. The rotor flux orientation is achieved by aligning the *d*-axis of the synchronous reference frame with the rotor flux vector $\vec{\lambda}_r$. In *dq*-axis synchronous frame, the stator current is resolved into two components along the *dq*-axes. The *d*-axis current, I_{sd}, is referred to as flux-producing current while the *q*-axis current, I_{sq}, is the torque-producing current. In the field-oriented control, I_{sd} is normally kept at its rated value while I_{sq} is controlled independently.

The FOC scheme for high power CSI-fed IM drive is implemented with three feedback control loops, one for the rotor mechanical angular speed ω_{mr}, one for the rotor flux magnitude λ_r, and another for the DC current I_{dc}. The *dq*-axis inverter PWM current references can be given by

$$\begin{cases} I_{wid}^{*} = I_{Cid} + I_{sd}^{*} \\ I_{wiq}^{*} = I_{Ciq} + I_{sq}^{*} \end{cases} \tag{1.5}$$

where I_{Cid} and I_{Ciq} are the *dq*-axis capacitor currents, which are given by

$$\begin{cases} I_{Cid} = C_i \dfrac{dV_{sd}}{dt} - \omega_e C_i V_{sq} \\ I_{Ciq} = C_i \dfrac{dV_{sq}}{dt} + \omega_e C_i V_{sd} \end{cases} \tag{1.6}$$

The first term on the right-hand side of the equation represents capacitor transient current, and the second term is the steady-state current. To reduce the sensitivity and noise caused by the derivative terms, the effect of the capacitor transient response on the drive dynamic performance may be neglected. (1.6) can be simplified as

$$\begin{cases} I_{wid}^{*} = -\omega_e C_i V_{sq} + I_{sd}^{*} \\ I_{wiq}^{*} = \omega_e C_i V_{sd} + I_{sq}^{*} \end{cases} \tag{1.7}$$

Since the magnitude of CSI-side PWM current reference vector, $\vec{I}_{wi}^{*}$, is proportional to the DC current, the DC current reference can be calculated as

$$I_{dc}^{*} = \frac{\sqrt{\left(I_{wid}^{*}\right)^2 + \left(I_{wiq}^{*}\right)^2}}{m_i} \tag{1.8}$$

The angle of CSI-side PWM current reference vector, θ_{wi}^{*}, is the sum of rotor flux angle, θ_{Fr}, and α_i, where θ_{Fr} can be obtained from the rotor flux estimator, and α_i can be determined by

$$\alpha_i = \tan^{-1}\left(I_{wiq}^{*} / I_{wid}^{*}\right) \tag{1.9}$$

Normally, SVM scheme is used under low output frequency condition. Whereas, SHE-PWM scheme is selected at high output frequency condition.

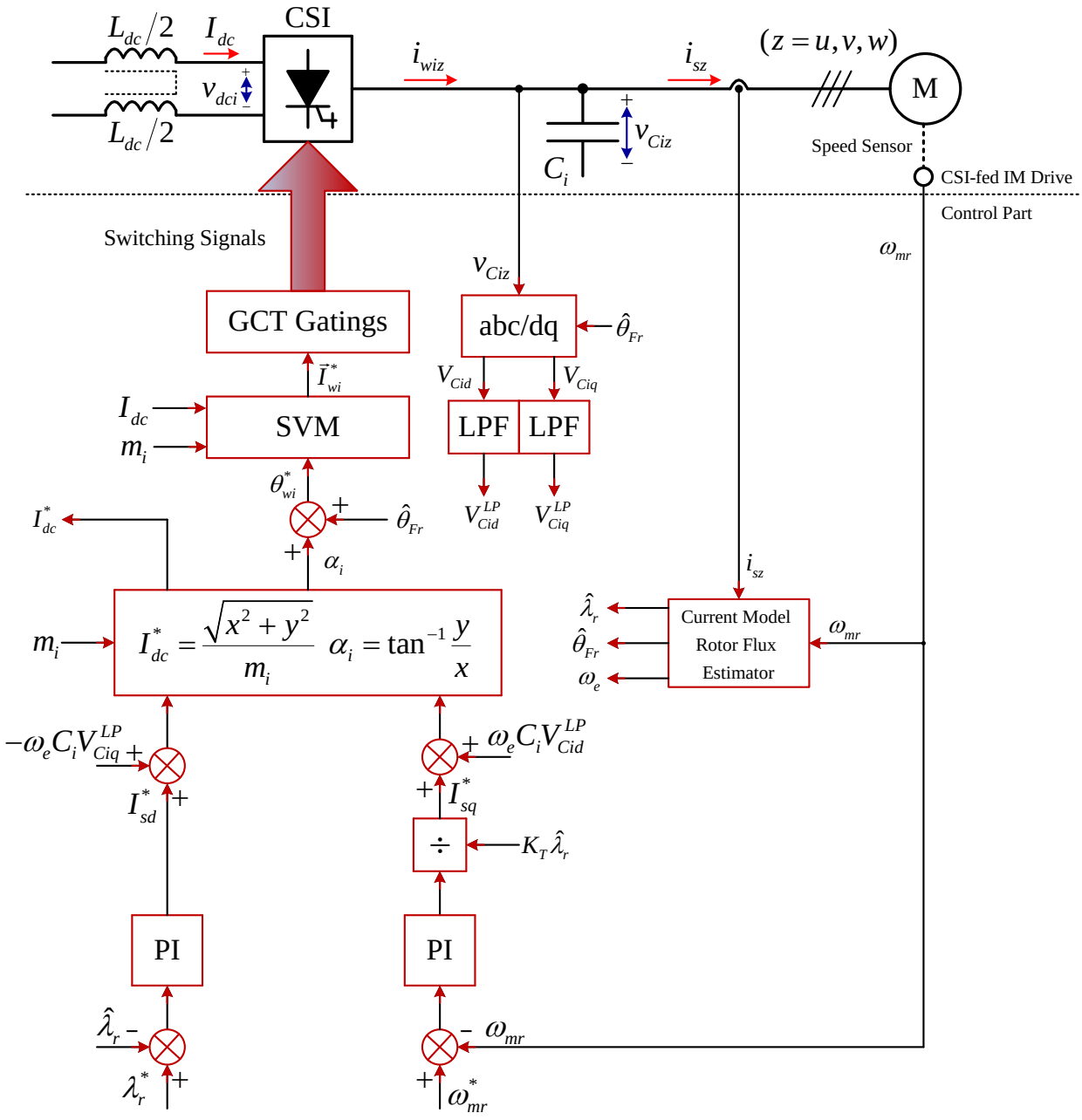


Fig. 1.20 Block diagram of FOC scheme for CSI-fed MV IM drive.

1.4.4 Traditional Common-Mode Voltage Reduction Method

To reduce the peak value of CMV, various reduced CMV (RCMV) PWM schemes have been proposed for CSC, which can mainly be categorized into three groups, nonzero-state SVM [38], zero-state selection SVM [39, 40], and coordinated SVM for both CSR and CSI [41].

1.4.4.1 Nonzero-state SVM

Two types of nonzero-state SVM schemes has been proposed for CSC, namely active-zero-state (AZS) modulation and nearest three-state (NTS) modulation. AZS modulation maintains the sector divisions and active space vectors as in traditional SVM, but replaces the zero vectors by two opposing active vector. Fig. 1.20 shows the principle of AZS modulation in Sector I with the leading adjacent space vector and its opposite one used to produce zero-state vector effect.

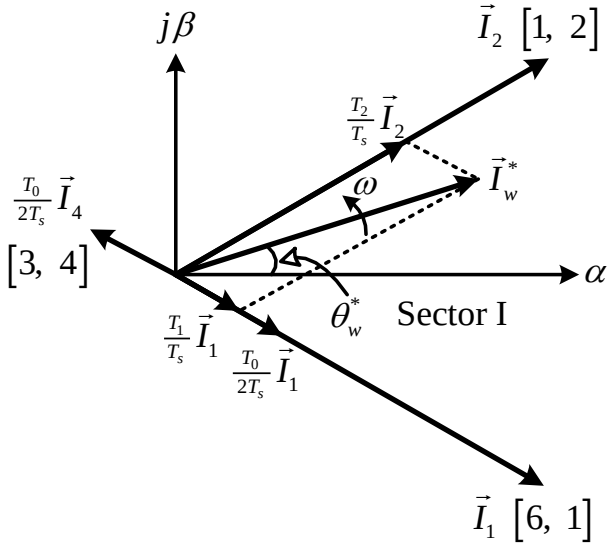


Fig. 1.21 Vector synthesis of the AZS modulation methods in Sector I.

NTS modulation method employs the nearest three active space vectors to synthesize the current reference. The principle of NTS modulation method is shown in Fig. 1.21.

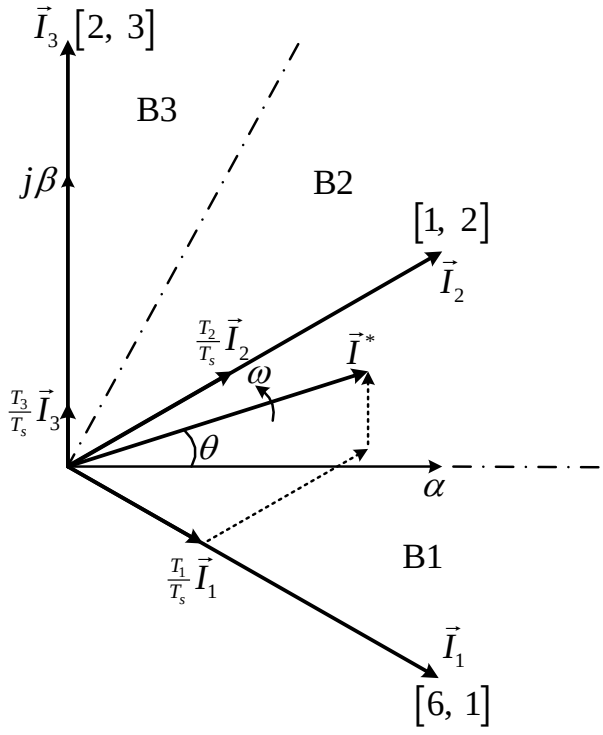


Fig. 1.22 Vector synthesis of the NTS modulation method in Sector B2.

Although those nonzero-state modulation methods can effectively reduce CMV, they are all subject to some problems, such as the shrink of modulation index range, increased switching frequencies, and output performance deterioration.

1.4.4.2 Zero-State Vector Selection SVM

Fig. 1.22 shows that at any given time there exists a zero-state vector, which generates the CMV peak value no larger than half of the capacitor phase voltage. The zero-state vector selection rule is that the zero-state vector producing the lowest CMV among the three zero-state vectors at any sampling period would be selected. Then, the CMVs produced by both active-state and zero-state vectors will be no larger than the half of the capacitor phase voltage. According to this rule, the selected zero-state vectors and the corresponding phase voltages in one fundamental period are also illustrated in Fig. 1.22.

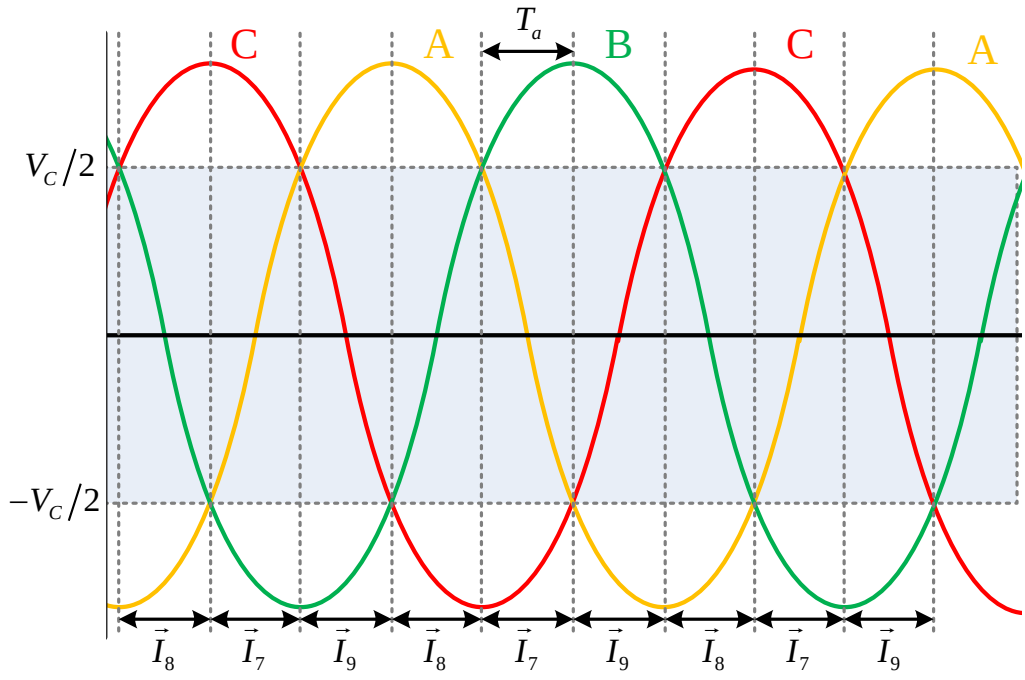


Fig. 1.23 Selected zero-state vectors in zero-state vector selection SVM in each instant of one fundamental period.

Since the zero-state vectors are still used in this method, the issues in nonzero-state vector modulation can be avoided. However, the zero-state vector selection will increase the switching frequency as well. To maintain the switching frequency same as that in traditional SVM, the SVM sequence needs to be rearranged according to the phase displacement angle between filter capacitor voltage and PWM current, which is determined by the operating state of CSC-fed drives. This process increases the complexity of modulation stage design.

1.4.4.3 Coordinated SVM

The coordinated SVM method associates the active-state and zero-state vectors of both CSR and CSI, instead of eliminating zero-state vectors or optimal selection of zero-state vector. Just three segment SVM scheme is used in this method. But during every sampling interval, the sequence of two active-state vectors and one zero-state vector will be rearranged according to the magnitude of corresponding CMVs. For instant, at both CSR and CSI sides, the sequences will be rearranged to make the CMVs from large to small order. Then, the largest CMV at CSR side will correspond to the largest one at CSI side and the smallest CMV at CSR side will

correspond to the smallest one at CSI side. Hence, the CMV of the whole system can be reduced. Fig. 1.23 shows the flowing chart of sequence determination with reference vector located in Sector I.

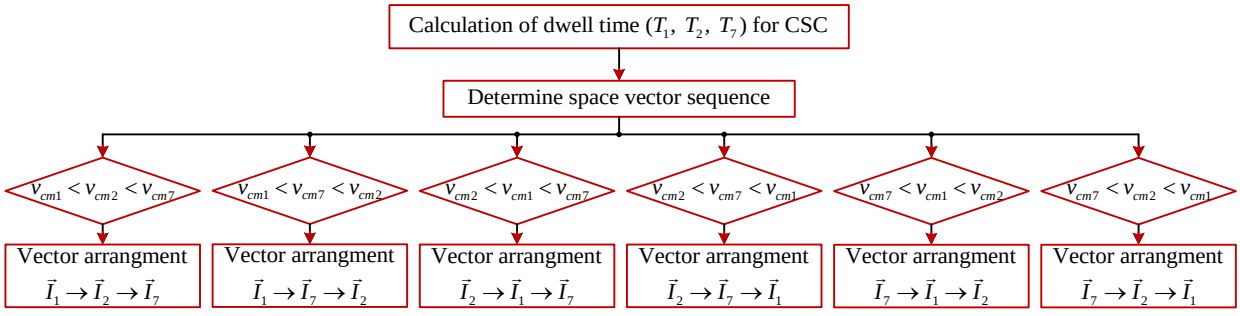


Fig. 1.24 Flowing chart diagram of optimized sequence arrangement.

Though this method can reduce the CMV in the whole system, the sequence change will increase the switching frequency as well. Moreover, the performance of this method is only ensured at high switching frequency condition, even larger than 10kHz. Therefore, this method is not suitable for CSC-fed MV drives.

1.4.5 Technical Challenges

Traditional control techniques impose several technical, operational and implementation challenges as follows.

1) Switched nolinear system. Power electronic systems represent switched nolinear system. For different on-off position combinations of active and passive switching devices, different system dynamics arise. At the same time, Nonlinearities arise, for instance, when motor variables such as electromagnetic torque or stator flux magnitude are directly controlled, in which both quantities are nonlinear functions of currents and flux linkages. For grid-connected converter, real and reactive power are nonlinear in terms of currents and voltages. Besides, current constraints lead to additional nonlinearities, which exasperate the difficulties of designing traditional linear controllers;

2) Multi-input-multi-output (MIMO) system. Power electronics systems are typical MIMO systems. The decomposition of MIMO system control into multiple single-input-single-output (SISO) loops and the use of cascaded control loops simplifies the control design.

This approach works well when the time constants of the cascaded control loops differ by at least one order of magnitude and while operating at steady-state operating conditions. During transients and faults, however, the different loops often start interacting with each other in an adverse manner, limiting the achievable performance in terms of controller bandwidth and robustness, and complicating the tuning of the control loops;

3) Low control frequency. For low switching frequencies, low control frequencies are normally used in high power MV drives. On one hand, transient response becomes sluggish because of the low-bandwidth modulation stage [44, 47]; On the other hand, control performance degrades, even becomes unstable because of longer control delay [45].

4) Difficulty of including nonlinear constraints. Including nonlinear constraints such as THD, common-mode voltage minimization, and switching frequency or loss reduction is not straight forward in the design of a traditional linear controller or a modulation stage.

1.5 Review on Conventional Model Predictive Control for Current-Source Converter

The family of predictive control techniques includes deadbeat predictive control, hysteresis based predictive control, trajectory based predictive control and model predictive control (MPC) [43]. Generally, MPC can be categorized into two groups: MPC with continuous control set and MPC with finite control set. In MPC with continuous control set, the control variable is a continuous voltage or current vector which can be synthesized by a modulation stage using SPWM or SVM [48]. Contrary to MPC with continuous control set, finite control-set model predictive control (FCS-MPC), as an approach to implement MPC for power converters and drives, is to take advantage of the inherent discrete nature of power converters, which has appeared as a simple and promising alternative to control power converters [49]. Since power converters have a finite number of switching states, FCS-MPC optimization problem can be simplified and reduced to the prediction of the system behavior only for those possible switching states. Then, each prediction is used to evaluate a cost function, and consequently, the switching state leading to the minimum cost is selected and generated.

FCS-MPC eliminates the need for linear regulators and modulators, which is a nonlinear control method, and provides better suited approach to control power converters while mitigating the aforementioned disadvantages associated with classical control techniques. With an appropriate definition of cost function, several constraints and technical requirements can be incorporated straight forward into the design and operation of controller. One of the best features of MPC is that several control objectives can be fulfilled at the same time as long as they are mathematical functions of the converter switching states. With an appropriate definition of cost function, better control flexibility can be achieved with the optimization of several control objectives for power converters.

The cost which is paid to use FCS-MPC is higher computational burden, but the modern digital signal processors (DSPs) can perform large amount of calculations at low cost. In fact, FCS-MPC has been extensively introduced into the control of power converters, especially VSCs. The two main applications are grid-connected rectifier or inverter [44, 50-54] and motor drives [55-58], respectively. Not only two-level VSCs, FCS-MPC schemes for three-phase four leg VSC [59-61] and different kinds of multilevel converters [62-71] have also been proposed. In the following chapters, FCS-MPC will be directly referred to as MPC for simplicity.

1.5.1 Principle of Operation

A simplified control block diagram of MPC applied to power converters and motor drives is presented in Fig. 1.25. The power converter can be of any topology and number of phases, while the generic load shown in the figure can represent an electrical machine, the utility power supply, or any other active or passive load. In this scheme, measured variables, $x(k)$, are used in the model to calculate predictions, $x^p(k+1)$, of the controlled variables for each of the *n* possible actuations, that is, switching states, voltage or current vectors. These predictions are evaluated using a cost function, which involves the reference values, $x^*(k)$, and restrictions. Finally, the optimal actuation is selected and applied to the converter. There are four key attributes of MPC, which can be summarized in the following.

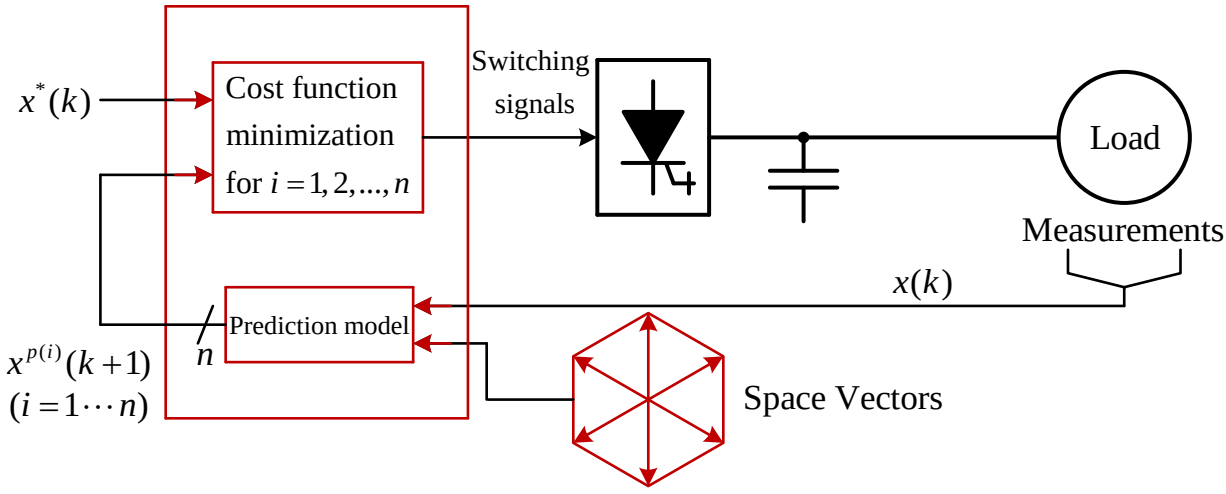


Fig. 1.25 Generalized control block diagram of MPC for power converters.

1.5.1.1 Dynamic Model

MPC incorporate a dynamic model of the system to be controlled. Let $\mathbf{x} \in \mathbb{R}^{n_x}$ denote the state vector of the system. Starting from the current state, the dynamic model enables MPC to predict the sequence of future system states and outputs for a given sequence of manipulated variables. The dynamic evolution of the system can be described in continuous-time domain by state-space representation

$$\begin{cases} \dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) \end{cases} \tag{1.10}$$

with the system matrix, $\mathbf{A}$, input matrix, $\mathbf{B}$, and output matrix, $\mathbf{C}$.

Most MPC schemes are formulated in discrete-time domain, using a constant sampling interval, T_s. The manipulated variable is restricted to changing its values only at the discrete sampling instants, that is the time instants, $t = kT_s$, where $k \in \mathbb{N}$ denotes the time steps. For the continuous-time state-space model (1.10), the discrete-time representation can easily be computed through different discretization methods. The discrete-time representation can be given as

$$\begin{cases} \mathbf{x}(k+1) = \mathbf{\Phi}\mathbf{x}(k) + \mathbf{\Gamma}\mathbf{u}(k) \\ \mathbf{y}(k) = \mathbf{C}\mathbf{x}(k) \end{cases} \tag{1.11}$$

The matrices, $\mathbf{\Phi}$ and $\mathbf{\Gamma}$, can be computed from their continous-time counterparts; The output matrix, $\mathbf{C}$, remains the same when deriving the discrete-time system representation.

1.5.1.2 Constraints

In power electronics systems, the switch position of the converter constitutes the manipulated variable, which is constrained to a finite set of integers. A single-bridge CSC, for instance, has nine swithing states. This characteristic can be captured by the input constraint

$$\mathbf{u}(k) \in \boldsymbol{\mu} \tag{1.12}$$

$\boldsymbol{\mu}$ denotes a set of constrained inputs for a CSC.

1.5.1.3 Minimization of Cost Function

The control objectives are translated into the cost function, which maps the sequences of future states, outputs, and manipulated variables into a scalar cost value. The cost function facilitates the assessment and comparison of the predicted impact the different sequences of manipulated variables have on the system. This enables MPC to choose the most suitable scenario, which is the one that minimizes the value of the cost function.

A general definition of the cost function is

$$J\left(\mathbf{x}(k), \mathbf{U}(k)\right) = \sum_{l=k}^{k+N_p-1} \Lambda\left(\mathbf{x}(l), \mathbf{u}(l)\right) \tag{1.13}$$

which is the sum of the state costs (or weighting functions) $\Lambda(\cdot,\cdot)$ over the finite horizon of the time step, N_p. The stage cost penalizes the predicted system behavior, such as the deviation of controlled variables from their references and the control effort, such as the switching frequency. The stage cost is required to be nonnegative. The cost function uses the current statevector, $\mathbf{x}(k)$, and the sequence of manipulated variables

$$\mathbf{U}(k) = \left[\mathbf{u}^T(k)\ \mathbf{u}^T(k+1)\ \ldots\ \mathbf{u}^T(k+N_p-1)\right]^T \tag{1.14}$$

The future states and controlled variables can be predicted over the prediction horizon and penalized accordingly.

Minimizing the cost function subject to both the evolution of the discrete-time dynamic system mode over the prediction horizon and the constraints gives rise to a constrained finite-time optimal control problem. The argument of the result is the optimal sequence of manipulated variables, $\mathbf{U}_{opt}(k)$, which can be given by

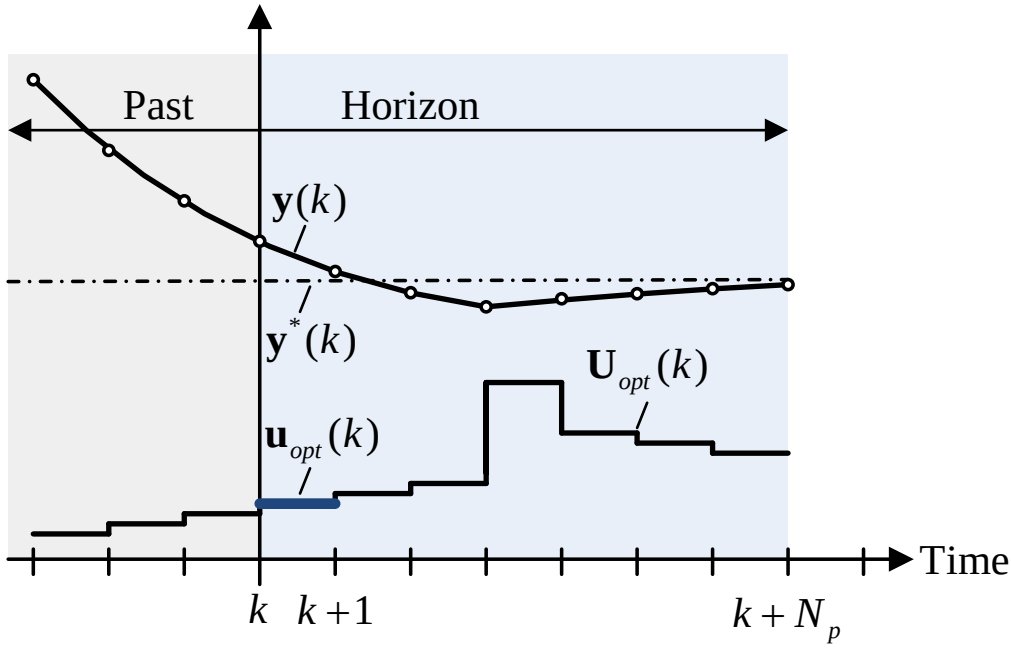
$$\begin{aligned} &\mathbf{U}_{opt}(k) = \arg \text{ minimize } J\left(\mathbf{x}(k), \mathbf{U}(k)\right) \\ &\text{subject to } \mathbf{x}(l+1) = \mathbf{A}\mathbf{x}(l) + \mathbf{B}\mathbf{u}(l) \\ &\qquad\qquad \mathbf{y}(l+1) = \mathbf{C}\mathbf{x}(l+1) \\ &\qquad\qquad \mathbf{u}(l) \in \boldsymbol{\mu} \quad \forall l = k, ..., k + N_p - 1 \end{aligned} \tag{1.15}$$

Traditionally, the optimization problem has exclusively been solved online, requiring the solution to be available in real time.

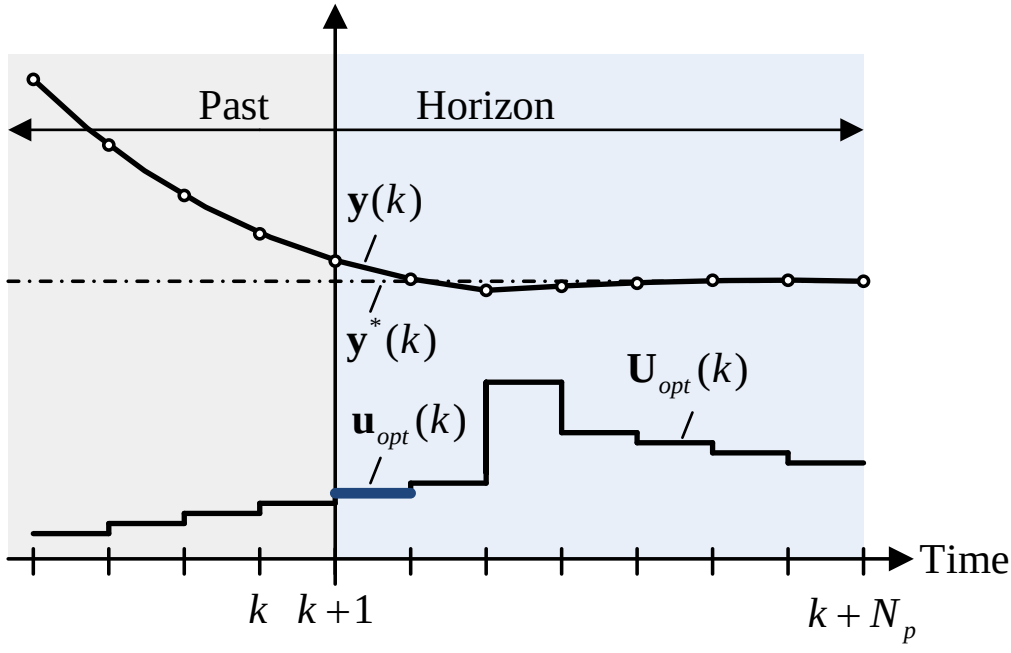
1.5.1.4 Receding Horizon Policy

The solution to the optimization problem (1.15) yields at time step k an open-loop optimal sequence of manipulated variables, $\mathbf{U}_{opt}(k)$, from time step k to $k + N_p - 1$. This policy is referred to as receding horizon control, which is illustrated in Fig. 1.26.

In summary, the principle of MPC is that at each sampling instant the manipulated variable is obtained by solving a constrained optimal control problem over a finite prediction horizon. A dynamic model of the system is used to predict future states and controlled variables, using the current state of the system as the initial state. The control objectives are captured by a cost function, which is mininmized subject to the evolution of the dynamic model and system constraints. The solution to the underlying optimization problem yields an optimal sequence of manipulated variables. A receding horizon policy is employed, that is, only the first element of this sequence is applied to the system, and the sequence of manipulated variables is recomputed at the next sampling instant over a shifted horizon. Hence, MPC combines constrained optimal control with the receding horizon policy that provides feedback and closes the control loop.



(a)



(b)

Fig. 1.26 Receding horizon policy exemplified for the prediction horizon $N_p = 7$.

1.5.2 Conventional Model Predictive Control for High Power Current-Source Converter

As mentioned above, MPC concept has been extensively introduced into the control of VSCs, no matter two-level or multilevel converters in grid-connected and motor drive applications. Up to now, there is not much literature on MPC for CSC. An MPC scheme for CSR, in which the DC current regulation and input power factor control are associated into one cost function, is presented in [72]. The model predictive output voltage control for CSI is proposed in [73], which follows the duality of output current control in VSCs. The model predictive current control for CSI with a simple three-phase *RL* load is proposed in [74]. However, the performance and characteristics of MPC for CSC have not been studied in detail yet. Besides, the performance of MPC for CSI-fed motor drives has not been covered yet.

1.5.2.1 Conventional MPC for CSR

In [72], an MPC scheme for CSR is presented. The prediction model of CSR is calculated based on Caley-Hamilton theorem [75]. The proposed scheme uses the prediction of the line current and the DC current with a prediction horizon of one sampling interval to calculate the best suited switching state for the rectifier that accomplishes the dual purposes of controlling the line power factor and the DC current without any modulation stage. The block diagram of the scheme is illustrated in Fig. 1.26.

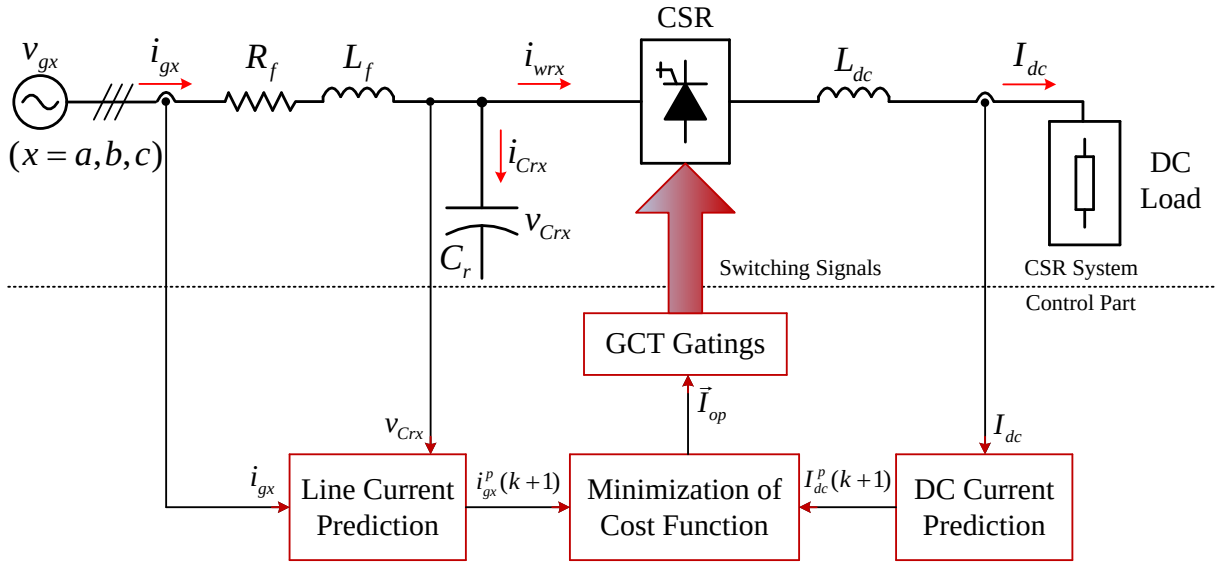


Fig. 1.27 Block diagram of MPC for CSR.

The cost function used here is given by

$$g(k) = \left|Q_g^p(k+1)\right| + W_{dc} \cdot \left|I_{dc}^* - I_{dc}^p(k+1)\right| \tag{1.16}$$

where $Q_g^p(k+1)$ is the predicted line reactive power at (k+1)th sampling instant, which can be calculated based on the predicted line current vector, $\vec{i}_g^{\,p}(k+1)$. I_{dc}^* and $I_{dc}^p(k+1)$ are the DC current reference and the predicted DC current, respectively.

Though this scheme can realize DC current regulation and reactive power control to an extent, it has two major shortcomings. The first is that the line power factor cannot be regulated accurately. Since the compromise between DC current regulation and reactive power control, it cannot ensure the maximum possible line power factor under various operating conditions of CSR. The second is that the *LC* resonance issue is not taken into consideration. In [72], a relatively large line resistor is physically connected to the line reactor in series, which provides some damping effect. However, in CSI-fed MV drives, the equivalent line resistance is just between 0.005pu and 0.01pu, which leads to a lightly damped *LC* circuit. Hence, an active damping method should be associated into MPC to mitigate the possible line-side resonance.

1.5.2.2 Conventional MPC for CSI

[73, 74] present MPC schemes for CSI with a simple *RL* load. Two control objectives have been studied, one is output voltage control and the other is load current control. Both of schemes can be illustrated with the block diagram in Fig. 1.27.

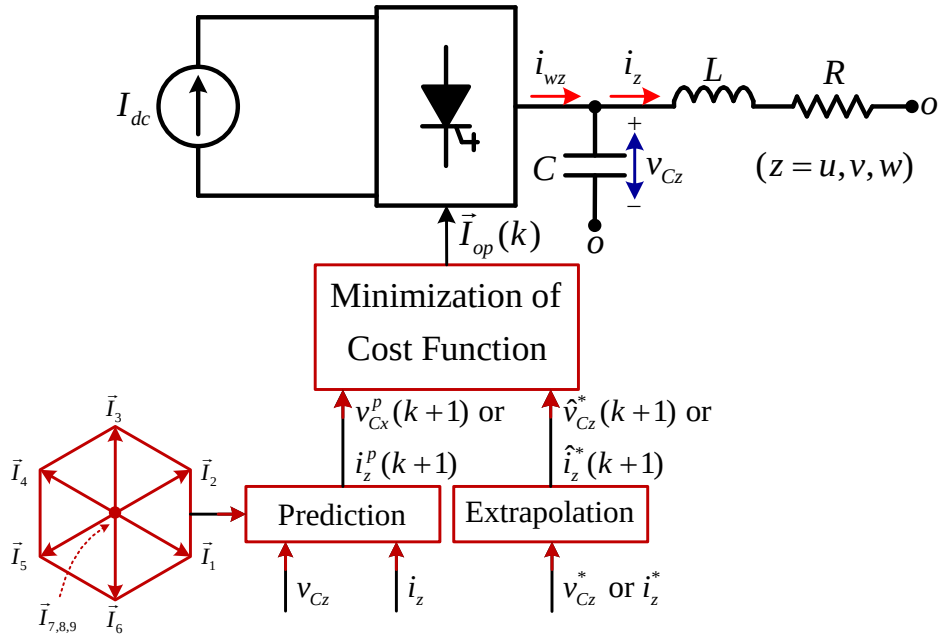


Fig. 1.28 Block diagram of MPC schemes for a CSI.

In Fig. 1.27, C is the filter capacitor at CSI side. R and L are the load resistor and inductor, respectively. Just using the Euler's forward method, the prediction model for output voltage and load current can be obtained based on the state-space model at CSI side. The fourth-order Lagrange method is used to estimate the future output voltage and load current reference at (k+1)th sampling instant, as

$$\hat{x}^*(k+1) = 4x^*(k) - 6x^*(k-1) + 4x^*(k-2) - x^*(k-3) \tag{1.17}$$

where x^* can represent either output voltage reference or load current reference. The cost function used for three-phase references tracking can be given by

$$g(k+1) = \left|\hat{x}_u^*(k+1) - x_u^p(k+1)\right| + \left|\hat{x}_v^*(k+1) - x_v^p(k+1)\right| + \left|\hat{x}_w^*(k+1) - \hat{x}_w^p(k+1)\right| \tag{1.18}$$

where $\hat{x}^{*}_{u,v,w}(k+1)$ denote either three-phase output voltage references or load current references at (k+1)th sampling instant; $x^{p}_{u,v,w}(k+1)$ represent either three-phase predicted output voltages or load currents at (k+1)th sampling instant.

Moreover, as one of nonlinear constraints, switching frequency reduction is also associated into the final cost function in [73, 74] with a term related to the number of commutations between two switching states introduced. So the final cost function can be obtained as

$$g^{'}(k) = g(k) + W_{sw} \cdot C_p(k, k-1) \tag{1.19}$$

where W_{sw} is the weighting factor to involve number of commutations into the cost function; C_p is the number of commutations between the possible switching state for kth sampling interval and the applied one at (k-1)th sampling instant.

Though model predictive output voltage and load current controls have been proposed for CSI, they are only conducted with a three-phase *RL* load, not specified for motor drives. Hence, the performance and the characteristics of MPC for CSI-fed motor drives are deserved to be investigated and analyzed. In [73, 74], only simulation results are provided, in which there is no calculation delay. However, in practical implementation, the calculation delay always exists. So how to compensate the influence of calculation delay on control performance needs to be investigated further. In addition, only switching frequency reduction has been introduced into the cost function as a nonlinear constraint. But there are more other control constraints for CSI-fed MV drives, such as CMV reduction and DC current minimization. Hence, how to solve these issues through MPC based approach is also a challenge to be coped with.

1.5.3 Technical Challenges

Despite the simple and attractive nature of MPC scheme, several technical challenges still exist in the state-of-the-art research, which includes, but not limited to, as follows.

1) Accurate modeling of power converters. The accurate continuous and discrete-time modeling of power converters is the foundation of achieving high performance control;

2) Appropriate selection of cost function and weighting factors. Different variables can be included in a single cost function. Since some variables have completely different values,

even different physical natures than others, mainly because they are expressed in different units, this can lead to coupling effects or changes in the relative importance of one variable over the other in the cost function. A simple way to address this issue is to include a coefficient or weight factor for each variable in the cost function. At the present state-of-the-art, the coefficients of the cost function are determined by empirical procedure. There is no analytical or numerical solution proposed yet to obtain an optimal solution for weighting factor. This challenge is an open research topic for future contributions to MPC scheme;

3) Control delay compensation. In the real-time implementation of MPC scheme, the large number of online calculations introduce a considerable time delay in the actuation. The computational delay deteriorates the performance of the system if it is not considered in the design stage of the controller;

4) Variable switching frequency nature. Since there is no linear modulation stage and switching state is selected according to minimization of a cost function in MPC scheme, switching frequency is normally variable with the operating state of power converter. The variable switching frequency increases the complexity of output filter design. Hence, to keep switching frequency constant or limit it in a defined range is always a challenge for MPC scheme;

5) Enhancement of robustness. Like in all control theories, measurement noise and parameter uncertainty (or variability under operation) can degrade the control system performance and even affect system stability. This is also true for MPC scheme. A theoretical approach or analysis in relation to the robustness of MPC scheme of power converters and drives is still a possible field of research and development.

1.6 Objectives of Dissertation

The target application for this proposal is high power CSI-fed MV drives. As summarized in Fig 1.28, the objectives for this proposal are twofold: the first one is to investigate the challenges in high power CSC-fed MV drives through MPC approach for better performance; and the second one is to investigate the challenges of MPC scheme itself.

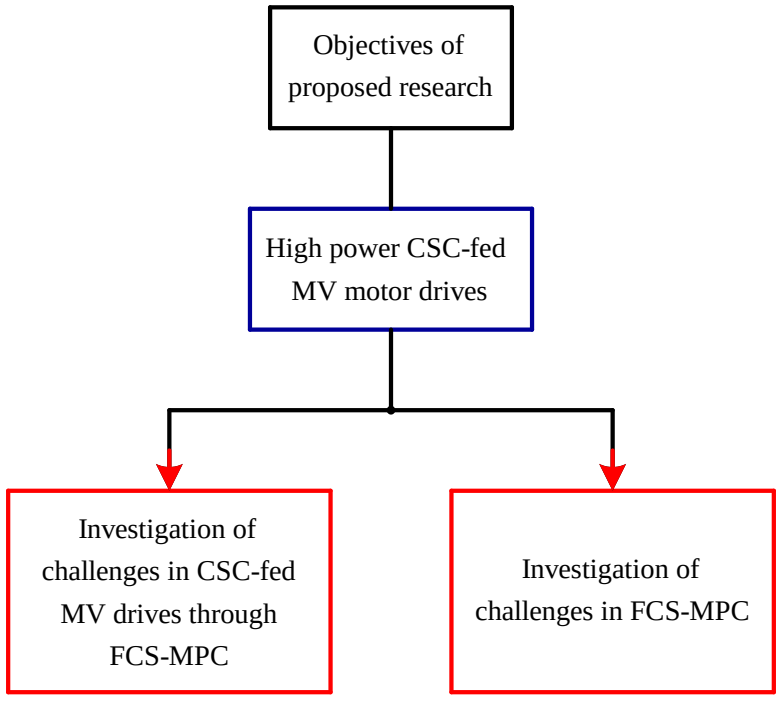


Fig 1.29. Objectives of proposed research.

1.6.1 Investigation of Challenges in High Power Current-Source Converter through Model Predictive Control

The first direction of the proposed research is to investigate the challenges in high power CSI-fed MV drives through MPC approach. The intention of this work is to introduce the advantages of MPC such as better dynamic performance, intuitive concept, and easy involvement of nonlinear constraints into control design of CSI-fed MV drives to obtain better output performance. Some sub-objectives can be summarized as follows.

1) Continuous- and discrete-time modeling of CSR and CSI-fed MV drives. The optimal control actions of MPC scheme are mainly based on the model of plant. A poor modeling of the plant will lead to an inferior control performance. The continuous-time models should be converted to discrete-time with a suitable method such that control delay and prediction horizon can be incorporated. Hence, accurate modeling of different control variables in terms of converter switching states is crucial;

2) Development of efficient MPC schemes for CSR. The CSRs in CSI-fed MV drives play a vital role in regulating DC currents and satisfying utility codes. This objective is specified to

design efficient MPC schemes such that the control requirements of CSRs such as DC current regulation, lower line-side current THD, maximum possible power factor, and mitigation of *LC* resonance can be fulfilled simultaneously;

3) Completion of motor-side MPC schemes for CSI-fed MV motor drives. The development of model predictive motor control methods for CSI-fed MV drives is set as an objective as well. This objective is specified to obtain better dynamic performance of CSI-fed MV drives with MPC schemes, especially better better stator current and electromagnetic torque responses during transients;

4) Investigation of MPC based CMV reduction method for CSI-fed MV drives. The reduction on CMV, as one of general requirements of CSI-fed MV drives, has been discussed in many academic works. But most of the existing methods realize the CMV reduction through the modification of SVM scheme and belong to linear control methods. Hence, this objective is defined to develop a MPC based CMV reduction method for CSI-fed MV drives to achieve better CMV mitigation performance;

5) Reduction on switching frequency. Switching frequency is always a big concern for high power MV motor drive. Conventional MPCs normally leads to a high switching frequency of power converter due to the use of high sampling frequency. Hence, in this study, some effort will also be paid on further reducing average switching frequency of MPC schemes, and makes the final switching frequency meet the requirement (normally lower than 1kHz) of high power MV motor drive.

1.6.2 Investigation of Challenges in Finite Control-Set Model Predictive Control

MPC scheme is anticipated to be one of next generation control tools, and thus considered as the secondary subject matter of this research.

6) Simiplification of calculation process. Both prediction process and minimization of cost function in MPC involve a bunch of calculation. Though some research results state that multi-step prediction process can improve output performance, and even reduce average switching frequency in comparison with conventional one-step prediction, multi-step prediction operation can result in exponential increase on calculation burden, which

complicates the realization of MPC. Hence, in this research, only one-tep prediction is used, but no matter output performance or switching frequency of MPC in this study will compete that of multi-step prediction;

7) Investigation on fixing switching frequency of CSC at a constant value in steady state. Conventional MPC usually results in variable switching frequency due to loss of modulation stage, which is not helpful for designing and sizing filters, especially at rectifier side. In this research, improvements on MPC will be conducted to fix the switching frequencies of CSC at a constant value in steady state operation, but still keep superior dynamic performance;

8) Weighting factor selection issue. So far, weighting factor selection is still an open topic in the filed of MPC research. In this research, depending on different proposed MPCs, the relationship between weighting factor value and output performance will be explicitly reveiled as a reference for weighting factor selection. Moreover, the final goal is to eliminate the existence of weighitng factor in MPC, and still achieve additional constraints, which are originally realized by weighting factor;

9) Improvement on robustness of MPC. Because of its dependence on model parameter, MPC can be easily influenced by the variation of parameters. In this research, inaccurate parameter or parameter variation issue need to be coped with in order to increase the robustness of proposed MPC.

1.7 Outline of Dissertation

The research presented in this dissertation is organized into seven chapters. The work carried-out in each chapter is summarized as follows.

Chapter 1: The overview of high power CSC-fed MV motor drive is presented. The reviews on traditional control schemes and conventional MPC for CSC in MV motor drives are introduced. The technical challenges existing in high power CSC-fed MV motor drive and conventional MPC for CSC are discussed. Aiming at the technical challenges, the objectives of the proposed research are elaborated;

Chapter 2: This chapter reviews commonly used discretization methods to obtain prediction model. The prediction models of CSI with three-phase *RL* load, CSR with DC resistor, and CSI-

fed IM drive are analyzed, respectively. Besides, generalized MPC approach for CSC is analyzed in this chapter;

Chapter 3: Model predictive power factor control (MPPFC) with active damping function for high power CSR is presented in this chapter. The proposed scheme achieves accurate line power factor regulation, ensures CSR working at maximum achievable line power factor under various operating conditions, even with parameter mismatch of input capacitor. Moreover, in order to suppress possible *LC* resonance at line side, an active damping method is incorporated into this scheme, which effectively damps the possible resonance;

Chapter 4: In this chapter, model predictive switching pattern control (MPSPC) for high power CSC is proposed. The proposed scheme combines SHE modulation and MPC together. In steady state operation, CSC follows the switching patterns based on SHE modulation, which keeps a fixed and relatively low switching frequency. On the other hand, during transient process, according to a criteria set in this scheme, the switching pattern of CSC can be governed through MPC approach to further improve its dynamic response, and after transients, the switching pattern will return to follow the waveform of SHE modulation;

Chapter 5: Model predictive space vector pattern control (MPSVPC) for high power CSC-fed MV IM drive is presented in this chapter. This scheme can be viewed as an extension of MPSPC, and associated with SVM, which is more suitable for variable frequency application. Both CSR and CSI generate PWM waveforms imposed by SVM in steady state, which maintains a fixed switching frequency at both sides. During transients, through a judging process based on a threshold value, both CSR and CSI can be regulated through MPC approach, which improves dynamic responses, such as torque overshoot, stator, and line current oscillation, in contrast to traditional SVM;

Chapter 6: In this chapter, common-mode voltage reduced model predictive control (RCMV-MPC) is presented for high power CSC-fed MV IM drive. In comparison with traditional CMV reduction method, this scheme further reduces CMV peak values at various operating conditions. Moreover, since the proposed scheme inherits the essence of MPC, it achieves better dynamic responses as well in contrast to its traditional counterparts;

Chapter 7: The conclusions of the proposed research are drawn in this chapter, in which the main contribution of this research are highlighted, and the future work along with the topic of the proposed research is presented.

2 Modeling and Generalized Predictive Control Approach of High Power Current-Source Converter for Medium-Voltage Induction Motor Drive

Prediction model is the foundation of conducting MPC to power converter. In this chapter, different discretization methods to derive discretized prediction model are presented, and compared with each other. Following the finally selected discretization method, the prediction models for high power current-source rectifier, high power current-source inverter with resistive-inductive load, and high power current-source converter-fed induction motor drive are derived based on their respective continuous dynamic models.

2.1 Derivation of Prediction Model

In order to derive prediction model, continuous dynamic model needs to be discretized first. There are mainly three kinds of discretization methods, namely first-order Euler method, Caley-Hamilton method, and Heun's method.

A continuous dynamic model in state-space form can be given by

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{2.1}$$

where $\mathbf{x}$ is the vector of state variables, $\mathbf{u}$ is the vector of inputs. An appropriate discretization method should be selected to discretize (2.1), and derive prediction model.

2.1.1 Caley-Hamilton Theorem

A discrete-time state-space equation can be derived when a zero-order hold (ZOH) input is applied to a continuous-time system, which is described in (2.1). Considering a sampling interval of T_s, the discrete-time state-space equation can be given by

$$\mathbf{x}^p(k+1) = \mathbf{\Phi}\mathbf{x}(k) + \mathbf{\Gamma}\mathbf{u}(k) \tag{2.2}$$

where $\mathbf{x}^p(k+1)$ is the predicted state variable vector at (k+1)th sampling instant, $\mathbf{x}(k)$ and $\mathbf{u}(k)$ are the state variable vector and the input vector at kth sampling instant, respectively; $\mathbf{\Phi}$ and $\mathbf{\Gamma}$ are the prediction matrices, which can be given by

$$\mathbf{\Phi} = e^{\mathbf{A}\cdot T_s} \text{ and } \mathbf{\Gamma} = \int_0^{T_s} e^{\mathbf{A}(T_s-\tau)}\mathbf{B}d\tau = \mathbf{A}^{-1}\left(\mathbf{\Phi}-\mathbf{I}\right)\mathbf{B} \tag{2.3}$$

in which $\mathbf{A}^{-1}$ denotes the inverse of $\mathbf{A}$, and $\mathbf{I}$ is an identity matrix. $\mathbf{\Phi}$ can be calculated with Caley-Hamilton theorem [76].

Though the method based on Caley-Hamilton theorem is very accurate, the involved calculation is too complicated. For instance, Caley-Hamilton theorem needs to be used to calculate the exponentiation of matrix, in $\mathbf{\Phi}$. Besides, the calculation of $\mathbf{\Gamma}$ involves with the inverse of $\mathbf{A}$. The elements in $_{\mathbf{A}}$ are sometimes variable based on different applications, such as motor drive application in which some elements contain electrical angular speed of motor. The real-time update of $\mathbf{\Phi}$ and $\mathbf{\Gamma}$ introduces too much burden, and occupies longer computational time.

2.1.2 Euler's Method

Euler's Method can be considered as the most direct and simple way to discretize derivative part in continuous dynamic equation [77]. Here forward Euler method is used to discretize (2.1), and the result can be given by

$$\frac{\mathbf{x}^p(k+1)-\mathbf{x}(k)}{T_s} = \mathbf{A}\mathbf{x}(k)+\mathbf{B}\mathbf{u}(k) \tag{2.4}$$

Based on (2.4) and according to state variable vector and input vector at kth sampling instant, state variable vector at (k+1)th sampling instant can be predicted by

$$\mathbf{x}^p(k+1) = \mathbf{\Phi}'\mathbf{x}(k)+\mathbf{\Gamma}'\mathbf{u}(k) \tag{2.5}$$

where

$$\mathbf{\Phi}' = \mathbf{I}+T_s\cdot\mathbf{A} \text{ and } \mathbf{\Gamma}' = T_s\cdot\mathbf{B} \tag{2.6}$$

in which $\mathbf{\Phi}'$ and $\mathbf{\Gamma}'$ are the prediction matrices based on Euler's method.

2.1.3 Heun's Method

There is another discretization method called Heun's method, which may refer to the modified Euler's method [77], which can be given by

$$\begin{cases} \mathbf{x}^c(k+1) = \mathbf{x}(k) + T_s\left(\mathbf{A}\mathbf{x}(k) + \mathbf{B}\mathbf{u}(k)\right) \\ \mathbf{x}^p(k+1) = \mathbf{x}^c(k+1) + \dfrac{T_s}{2}\mathbf{A}\left(\mathbf{x}^c(k+1) - \mathbf{x}(k)\right) \end{cases} \tag{2.7}$$

where $\mathbf{x}^c(k+1)$ is the predictor-corrector of state variable vector at (k+1)th sampling instant, and $\mathbf{x}^p(k+1)$ is still the predicted state variable vector at (k+1)th sampling instant.

(2.7) can be rearranged and written in the form as

$$\mathbf{x}^p(k+1) = \mathbf{\Phi}''\mathbf{x}(k) + \mathbf{\Gamma}''\mathbf{u}(k) \tag{2.8}$$

where

$$\mathbf{\Phi}'' = \mathbf{I} + T_s \cdot \mathbf{A} + \frac{T_s^2}{2} \cdot \mathbf{A}^2 \text{ and } \mathbf{\Gamma}'' = \left(T_s + \frac{T_s^2}{2} \cdot \mathbf{A}\right)\mathbf{B} \tag{2.9}$$

$\mathbf{A}$ and $\mathbf{B}$ can be substituted into (2.9), and prediction matrices can be obtained. Though the calculation burden of this method is heavier than that of Euler method, prediction model can still be real-time updated.

2.1.4 Correlation Between Discretization Methods

The prediction matrix, $\mathbf{\Phi}$, based on Caylem-Hamilton Theorem can be extended as Taylor series, and given by

$$\mathbf{\Phi} = \mathbf{I} + T_s \cdot \mathbf{A} + \frac{T_s^2}{2} \cdot \mathbf{A}^2 + \ldots + \frac{T_s^n}{n!} \cdot \mathbf{A}^n + \ldots \tag{2.10}$$

It can be found from (2.10) that $\mathbf{\Phi}'$ based on Forward Euler method just keeps the first and the second terms of $\mathbf{\Phi}$. On the other hand, $\mathbf{\Phi}''$ based on Heun's method keeps the first three terms of $\mathbf{\Phi}$. $\mathbf{\Phi}'$ and $\mathbf{\Phi}''$ can also be substituted into (2.3), then $\mathbf{\Gamma}'$ and $\mathbf{\Gamma}''$ can be obtained. From this point of view, it can be concluded that Euler method and Heun' method are both

approximations of Caley-Hamilton theorem based method, and Heun's method is more accurate than Euler's method.

2.2 Modeling of High Power Current-Source Converter for Medium-Voltage Induction Motor Drive

2.2.1 Modeling of High Power Current-Source Inverter with Resistive-Inductive load

A typical three-phase high power CSI with *RL* load is illustrated in Fig. 2.1. An ideal DC current source is connected to the DC side of the CSI for simplicity.

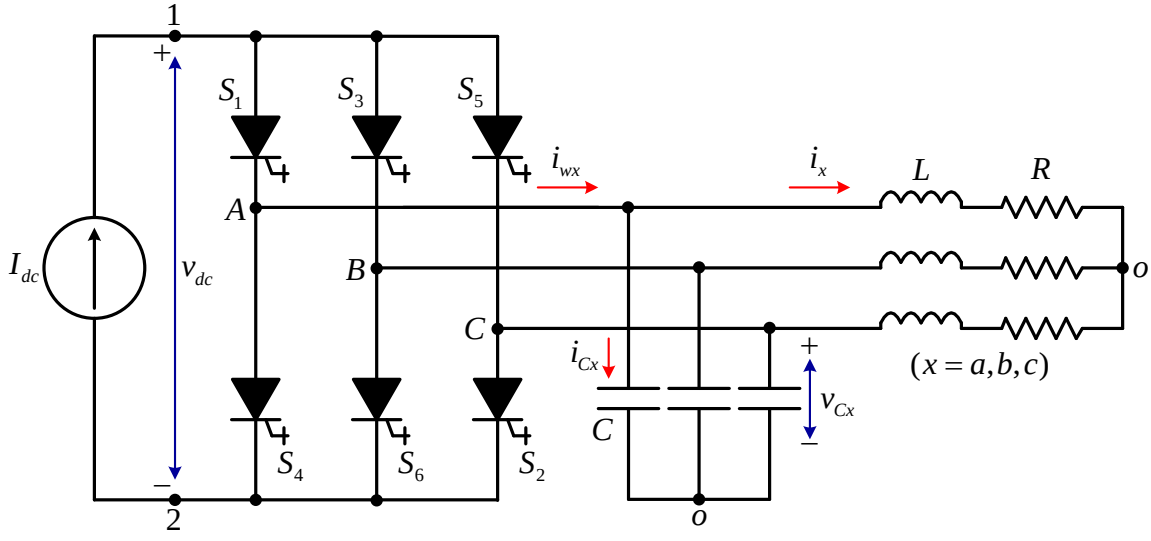


Fig. 2.1 Topology of high power CSI with *RL* load.

2.2.1.1 Continuous Dynamic Model

Hereafter, space vector representation is preferred to being used, of which the definition is

$$\vec{x} = x_\alpha + jx_\beta = \frac{2}{3}(x_a + e^{j\frac{2\pi}{3}}x_b + e^{j\frac{4\pi}{3}}x_c) \tag{2.11}$$

where $\vec{x}$ can represent the space vectors of capacitor voltage and load current; x_α and x_β are the components of $\vec{x}$ in $\alpha\beta$-axis stationary frame, while x_a, x_b, and x_c are the components in three-phase stationary frame.

The AC side of the CSI can be expressed at space vector format, and given by

$$\begin{cases} \vec{v}_C = L\dfrac{d\vec{i}}{dt} + R\vec{i} \\ \vec{i}_w = C\dfrac{d\vec{v}_C}{dt} + \vec{i} \end{cases} \tag{2.12}$$

where C is filter capacitance, L is reactor inductance, and R is load resistance; $\vec{v}_C$ is the capacitor voltage vector, $\vec{i}_w$ is the output PWM current vector, and $\vec{i}$ is the load current vector. The output PWM current vector is defined by nine switching states of the CSI, including six active-state vectors and one zero-state vector, which can be generated by three different switching states. The six active-state vectors can be given by

$$\vec{I}_n = \frac{2}{\sqrt{3}} I_{dc} e^{j\left((n-1)\frac{\pi}{3}-\frac{\pi}{6}\right)} \quad \text{for } n = 1, 2, ..., 6 \tag{2.13}$$

The space vectors of the CSI are illustrated in Fig. 2.2, in which zero-state vector corresponds to three switching states.

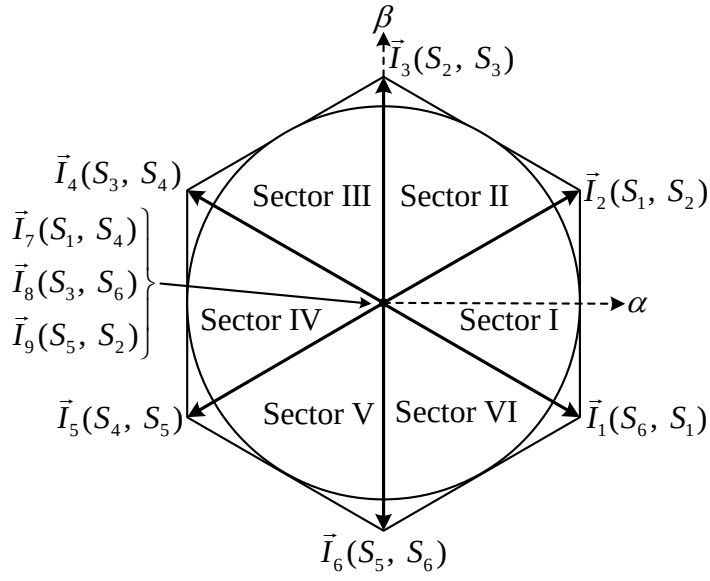


Fig. 2.2 Diagram of space vectors of a CSC.

(2.12) can be written in state-space form, and given by

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{2.14}$$

where $\mathbf{x}$ is the state variables, equal to $\begin{bmatrix} \vec{v}_C & \vec{i} \end{bmatrix}^T$, $\dot{\mathbf{x}}$ denotes the differentiation of $\mathbf{x}$, $\mathbf{u}$ is the input, equal to $\vec{i}_w$, $\mathbf{A}$ and $\mathbf{B}$ are given by

$$\mathbf{A} = \begin{bmatrix} 0 & -\frac{1}{C} \\ \frac{1}{L} & -\frac{R}{L} \end{bmatrix} \text{ and } \mathbf{B} = \begin{bmatrix} \frac{1}{C} \\ 0 \end{bmatrix} \tag{2.15}$$

2.2.1.2 Prediction Model

In Section 2.1, three kinds of discretization methods are introduced, in which Euler method and Heun's method impose lighter calculation burden, and can be easily real-time updated. With Euler method, (2.15) can be substituted into (2.6), and the prediction model can be given by

$$\mathbf{x}^p(k+1) = \mathbf{\Phi}'\mathbf{x}(k) + \mathbf{\Gamma}'\mathbf{u}(k) \tag{2.16}$$

where $\mathbf{x}^p(k+1)$ is equal to $\begin{bmatrix} \vec{v}_C^{\,p}(k+1) & \vec{i}^{\,p}(k+1) \end{bmatrix}^T$, $\mathbf{x}(k)$ and $\mathbf{u}(k)$ are the state variables and the input at kth sampling instant; the prediction matrices can be given by

$$\mathbf{\Phi}' = \begin{bmatrix} \phi_{11}' & \phi_{12}' \\ \phi_{21}' & \phi_{22}' \end{bmatrix} = \begin{bmatrix} 1 & -\frac{T_s}{C} \\ \frac{T_s}{L} & 1-\frac{T_s R}{L} \end{bmatrix} \text{ and } \mathbf{\Gamma}' = \begin{bmatrix} \varphi_{11}' \\ \varphi_{21}' \end{bmatrix} = \begin{bmatrix} \frac{T_s}{C} \\ 0 \end{bmatrix} \tag{2.17}$$

Based on $\mathbf{\Gamma}'$, it can be found that the impact of output current of CSI on load current is not reflected, since the element in the second row of $\mathbf{\Gamma}'$ is equal to 0. However, in most applications, load current references are calculated and tracked, which makes the Euler method based prediction model not suitable for prediction control of CSI.

On the other hand, with Heun's method, (2.15) can be substituted into (2.9), and the prediction model can be given by

$$\mathbf{x}^p(k+1) = \mathbf{\Phi}''\mathbf{x}(k) + \mathbf{\Gamma}''\mathbf{u}(k) \tag{2.18}$$

where the prediction matrices can be given by

$$\mathbf{\Phi}^{''} = \begin{bmatrix} \phi_{11}^{''} & \phi_{12}^{''} \\ \phi_{21}^{''} & \phi_{22}^{''} \end{bmatrix} = \begin{bmatrix} 1-\dfrac{T_s^2}{2CL} & \dfrac{T_s^2 R}{2CL}-\dfrac{T_s}{C} \\ \dfrac{T_s}{L}-\dfrac{T_s^2 R}{2L^2} & 1-\dfrac{T_s R}{L}-\dfrac{(L-CR)T_s^2}{2CL^2} \end{bmatrix} \text{ and } \mathbf{\Gamma}^{''} = \begin{bmatrix} \varphi_{11}^{''} \\ \varphi_{21}^{''} \end{bmatrix} = \begin{bmatrix} \dfrac{T_s}{C} \\ \dfrac{T_s^2}{2CL} \end{bmatrix} \quad (2.19)$$

Based on (2.18) and (2.19), the capacitor voltage vector and the load current vector at (k+1)th sampling instant can be given by

$$\begin{cases} \vec{v}_C^{\,p}(k+1) = \phi_{11}^{''} \cdot \vec{v}_C(k) + \phi_{12}^{''} \cdot \vec{i}\,(k) + \varphi_{11}^{''} \cdot \vec{i}_w(k) \\ \vec{i}^{\,p}(k+1) = \phi_{21}^{''} \cdot \vec{v}_C(k) + \phi_{22}^{''} \cdot \vec{i}\,(k) + \varphi_{21}^{''} \cdot \vec{i}_w(k) \end{cases} \quad (2.20)$$

where the impact of the output current vector of CSI on the load current vector is reflected, and can be used for optimal switching state selection in CSI.

Hereafter, Eeun's method is selected, and used to derive the prediction models of high power CSR and CSI-fed IM drive.

2.2.2 *Modeling of High Power Current-Source Rectifier*

A high power CSR with a resistive load connected at the DC side is shown in Fig. 2.3.

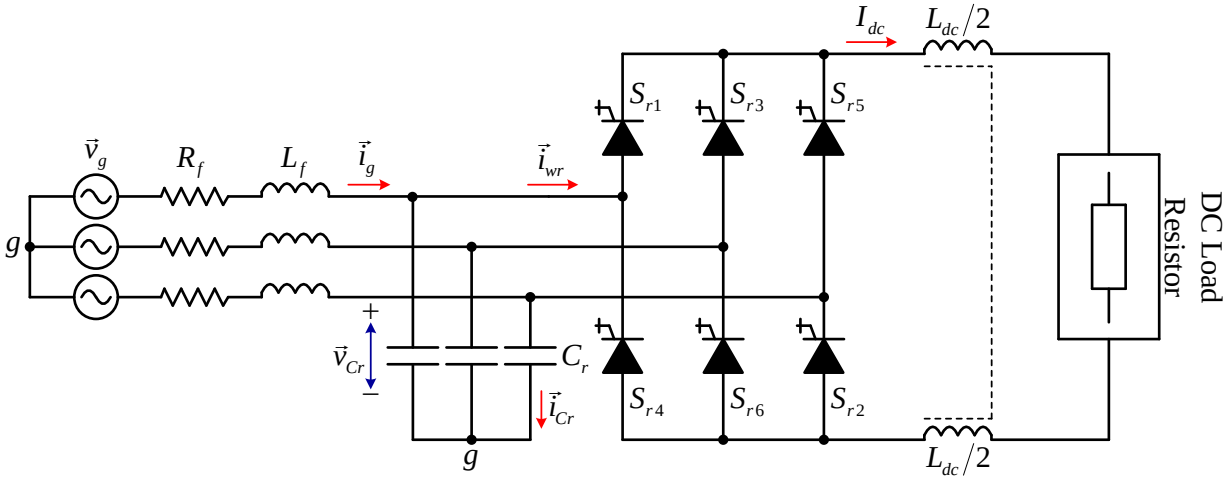


Fig. 2.3 Configuration of a CSR with a resistive load.

2.2.2.1 *Continuous Dynamic Model*

As shown in Fig. 2.3, the utility power supply is connected to the input of the CSR through a three-phase LC filter, of which each phase consists of a filter inductor, L_f, and a capacitor, C_r.

R_f denotes the equivalent line-side resistance. A resistive load is connected to the DC side of the CSR through a DC choke, L_{dc}. The line side of a CSR can be expressed at state-space format as

$$\dot{\mathbf{x}}_r = \mathbf{A}_r\mathbf{x}_r + \mathbf{B}_r\mathbf{u}_r \tag{2.21}$$

where $\mathbf{x}_r$ is the state variables, and equal to $\begin{bmatrix}\vec{v}_{Cr} & \vec{i}_g\end{bmatrix}^T$ (CSR-side capacitor voltage vector and line current vector); $\mathbf{u}_r$ is the inputs, and equal to $\begin{bmatrix}\vec{v}_g & \vec{i}_{wr}\end{bmatrix}^T$ (utility power supply voltage vector and input current vector); the matrices, $\mathbf{A}_r$ and $\mathbf{B}_r$, are given by

$$\mathbf{A}_r = \begin{bmatrix} 0 & \frac{1}{C_r} \\ -\frac{1}{L_f} & -\frac{R_f}{L_f} \end{bmatrix} \text{ and } \mathbf{B}_r = \begin{bmatrix} 0 & -\frac{1}{C_r} \\ \frac{1}{L_f} & 0 \end{bmatrix} \tag{2.22}$$

The value of $\vec{i}_{wr}$ is limited to six active-state vectors and one zero-state vector as well, as illustrated in Fig. 2.2.

2.2.2.2 Prediction Model

(2.22) can be substituted into (2.18), then, the prediction model for a high power CSR can be given by

$$\mathbf{x}_r^p(k+1) = \mathbf{\Phi}_r\mathbf{x}_r(k) + \mathbf{\Gamma}_r\mathbf{u}_r(k) \tag{2.23}$$

where

$$\mathbf{\Phi}_r = \begin{bmatrix} \phi_{r11} & \phi_{r12} \\ \phi_{r21} & \phi_{r22} \end{bmatrix} = \begin{bmatrix} 1-\frac{T_s^2}{2C_rL_f} & \frac{T_s}{C_r} \\ -\frac{T_s}{L_f} & 1-\frac{T_s^2}{2C_rL_f} \end{bmatrix} \text{ and } \mathbf{\Gamma}_r = \begin{bmatrix} \varphi_{r11} & \varphi_{r12} \\ \varphi_{r21} & \varphi_{r22} \end{bmatrix} = \begin{bmatrix} \frac{T_s^2}{2C_rL_f} & -\frac{T_s}{C_r} \\ \frac{T_s}{L_f} & \frac{T_s^2}{2C_rL_f} \end{bmatrix} \tag{2.24}$$

where $\mathbf{x}_r(k)$ are the state variables at *k*th sampling instant; $\mathbf{u}_r(k)$ are the inputs at *k*th sampling instant; $\mathbf{x}_r^p(k+1)$ are the predicted state variables at (*k*+1)th sampling instant, and equal to $\left[\vec{v}_{Cr}^{\,p}(k+1) \quad \vec{i}_g^{\,p}(k+1)\right]^T$. Based on (2.23), the prediction of the line current vector can be calculated, and used for optimal space vector or switching state selection.

2.2.3 Modeling of High Power Current-Source Inverter-Fed Medium Voltage Induction Motor Drive

The configuration of a high power CSC-fed MV IM drive is illustrated in Fig. 2.4, in which two DC chokes are connected at the DC side of the CSI, and the DC current is regulated by a CSR, which is connected to three-phase utility power supply.

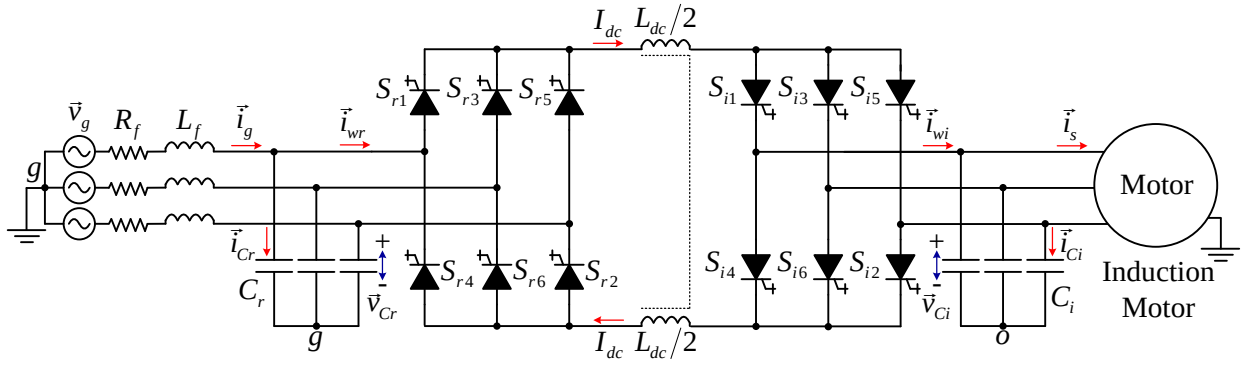


Fig. 2.4 Configuration of high power CSC-fed MV IM drive.

2.2.3.1 Continuous Dynamic Model

The continuous dynamic model of CSI-fed IM drive can be given in state-space form by

$$\dot{\mathbf{x}}_i = \mathbf{A}_i\mathbf{x}_i + \mathbf{B}_i\mathbf{u}_i \tag{2.25}$$

where $\mathbf{x}_i$ are the CSI-side state variables, and equal to $\left[\vec{v}_{Ci} \quad \vec{i}_s\right]^T$ (CSI-side capacitor voltage and stator current vectors); $\mathbf{u}_i$ are the CSI-side input variables, and equal to $\left[\vec{\lambda}_r \quad \vec{i}_{wi}\right]^T$ (rotor flux and output current vectors). The matrices, $\mathbf{A}_i$ and $\mathbf{B}_i$, are given by

$$\mathbf{A}_i = \begin{bmatrix} 0 & -\dfrac{1}{C_i} \\ \dfrac{1}{\tau_\sigma R_\sigma} & -\dfrac{1}{\tau_\sigma} \end{bmatrix} \text{ and } \mathbf{B_i} = \begin{bmatrix} 0 & \dfrac{1}{C_i} \\ \dfrac{k_r(1/\tau_r - j\omega_r)}{\tau_\sigma R_\sigma} & 0 \end{bmatrix} \tag{2.26}$$

in which

$$\sigma = 1 - \frac{L_m^2}{L_s L_r},\ R_\sigma = R_s + R_r k_r^2,\ k_r = \frac{L_m}{L_r},\ \tau_\sigma = \frac{\sigma L_s}{R_\sigma},\ \tau_r = \frac{L_r}{R_r} \tag{2.27}$$

where R_s and R_r are stator and rotor resistances; L_s, L_r, and L_m are stator, rotor, and mutual inductances; ω_r is electrical rotor angular speed, and equal to the number of pole pairs, P, times mechanical rotor angular speed, ω_{mr}. C_i is the capacitance of CSI-side capacitor, which is normally between 0.3pu to 0.6pu.

2.2.3.2 Discretized Prediction Model

Substituting (2.26) to into (2.9), the discretized prediction model of CSI-fed IM drive can be given by

$$\mathbf{x}_i(k+1) = \mathbf{\Phi}_i \mathbf{x}_i(k) + \mathbf{\Gamma}_i \mathbf{u}_i(k) \tag{2.28}$$

in which

$$\mathbf{\Phi}_i = \begin{bmatrix} \phi_{i11} & \phi_{i12} \\ \phi_{i21} & \phi_{i22} \end{bmatrix} = \begin{bmatrix} 1 - \dfrac{T_s^2}{2C_i r_\sigma t_\sigma} & \dfrac{T_s(T_s - 2\tau_\sigma)}{2C_i \tau_\sigma} \\ -\dfrac{T_s(T_s - 2\tau_\sigma)}{2r_\sigma \tau_\sigma^2} & 1 - \dfrac{T_s^2}{2C_i r_\sigma t_\sigma} - \dfrac{T_s}{\tau_\sigma} + \dfrac{T_s^2}{2\tau_\sigma^2} \end{bmatrix} \text{ and}$$

$$\mathbf{\Gamma}_i = \begin{bmatrix} \varphi_{i11} & \varphi_{i12} \\ \varphi_{i21} & \varphi_{i22} \end{bmatrix} = \begin{bmatrix} -\dfrac{T_s^2 k_r(1/\tau_r + j\omega_r)}{2C_i r_\sigma \tau_\sigma} & \dfrac{T_s}{C_i} \\ -\dfrac{T_s k_r (T_s - 2\tau_\sigma)(1 - j\tau_r \omega_r)}{2r_\sigma t_\sigma^2} & \dfrac{T_s^2}{2C_i r_\sigma \tau_\sigma} \end{bmatrix} \tag{2.29}$$

where $\mathbf{x}_i(k)$ are the state variables at *k*th sampling instant; $\mathbf{u}_i(k)$ are the inputs at *k*th sampling instant; $\mathbf{x}_i^p(k+1)$ are the predicted state variables at (*k*+1)th sampling instant, which are equal to

$\left[\vec{v}_{Ci}^{\,p}(k+1) \quad \vec{i}_s^{\,p}(k+1)\right]^T$. Based on (2.28), optimal switching state for CSI can be selected through the prediction process of stator current vector.

2.3 Generalized Predictive Control Approach of High Power Current-Source Converter

2.3.1 Selection of Prediction Horizon

In most existing literature and research, the prediction horizon is just chosen as 1, meaning one-step prediction. The operating principle for the prediction of variables using one-step prediction horizon is shown in Fig. 2.5, assuming that the converter possesses 3 kinds of switching states. The 3 possible switching states lead to 3 predictions for the variable to be controlled. Then, the switching state leading to minimum error between the corresponding prediction and reference is applied at *k*th instant.

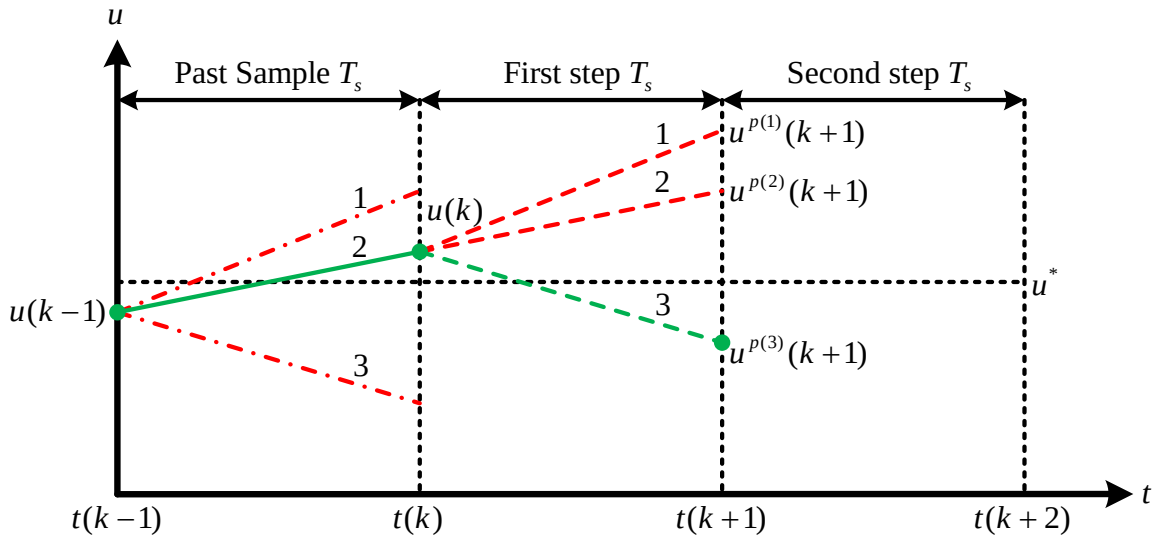


Fig. 2.5 FCS-MPC strategy using one-step prediction horizon.

In fact, a longer prediction horizon can also be used, meaning multi-step prediction. For every future instant, an optimal switching state will be selected. But just the switching state selected at *k*th instant will be applied finally. The operating principle for the prediction of variables using two-step prediction horizon is shown in Fig. 2.6, assuming that the converter possesses 3 kinds of switching states, either. The 3 possible switching states lead to 3

predictions at (k+1)th instant. But the number of predictions at (k+2)th instant becomes 9 (3^2). For a CSC , since there are 9 possible switching states, the number of predictions at (k+2)th instant will be equal to 81 (9^2). The multistep or long horizon prediction is just suitable for converters having less number of switching states and will involve large number of calculations. Besides, to realize real time control, a high sampling frequency is usually used for FCS-MPC strategy, normally larger than 10kHz. Under such a sampling frequency, the nowadays digital signal processors are just enough to achieve one-step prediction operation. Hence, that is the reason why one-step prediction is selected by most existing research. In this proposal, the prediction horizon is also selected as 1.

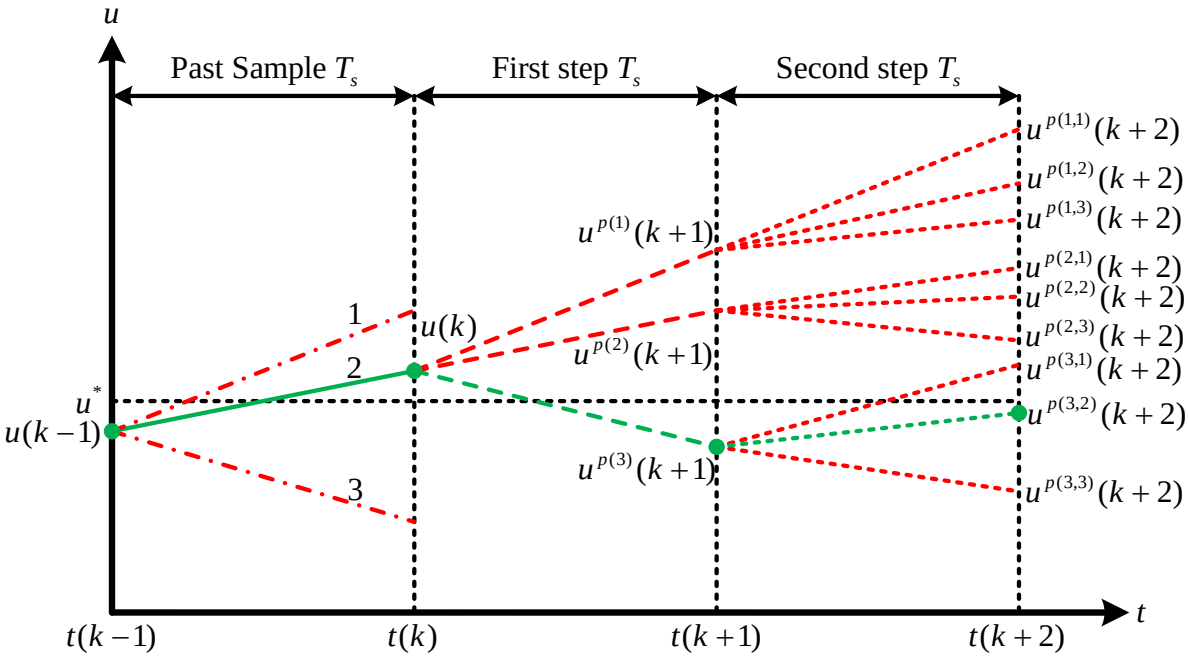


Fig. 2.6 FCS-MPC strategy using two-step prediction horizon.

2.3.2 Reference Extrapolation Methods

One of the important requirements in FCS-MPC strategy is reference tracking. In a CSC, the tracked reference would be output voltage or load current. When the sampling period T_s is sufficiently small ($<20\mu s$), no extrapolation is required. This implies that the sampling frequency is much higher than the fundamental frequency of the variables to be controlled. When the FCS-MPC strategy works with lower sampling frequencies, the references should be extrapolated to

(k+1)th instant to effectively minimize the tracking error. There are mainly two kinds of reference extrapolation methods, Lagrange method and vector angle method [45, 59-61].

2.3.2.1 Lagrange Method

A third-order Lagrange methods for one-step ahead extrapolation at (k+1)th instant is given as follows

$$u(k+1) = 3u(k) - 3u(k-1) + u(k-2) \tag{2.30}$$

where the variable u represents either voltage, current or power. To increase the performance of FCS-MPC strategy, a higher-order extrapolation methods can be employed. A fourth-order Lagrange method for (k+1)th extrapolation is given as follow

$$u(k+1) = 4u(k) - 6u(k-1) + 4u(k-2) - u(k-3) \tag{2.31}$$

2.3.2.2 Vector Angle Method

The other possible approach for the extrapolation is vector angle method. This method is very suitable for the reference vector expressed at space vector format. In this method, during each sampling interval, the change in vector angle of the three-phase variables is considered as the basis for extrapolation. A nth order vector angle extrapolation is given as

$$\vec{u}(k+n) = \vec{u}(k)e^{jn\omega T_s} \tag{2.32}$$

where ω is angular frequency of three-phase variables.

Since the better transient performance can be obtained with the vector angle method, this method will be used for reference extrapolation in the following research.

2.3.3 Cost Function Flexibility

One of the best features of FCS-MPC strategy is that several control objectives can be fulfilled at the same time as long as they are mathematical function of the converter switching states. As demonstrated in Fig. 2.7, with an appropriate definition of cost function, a better control flexibility can be obtained with the optimization of several control for CSC. The control objectives can be broadly classified as primary and secondary goals.

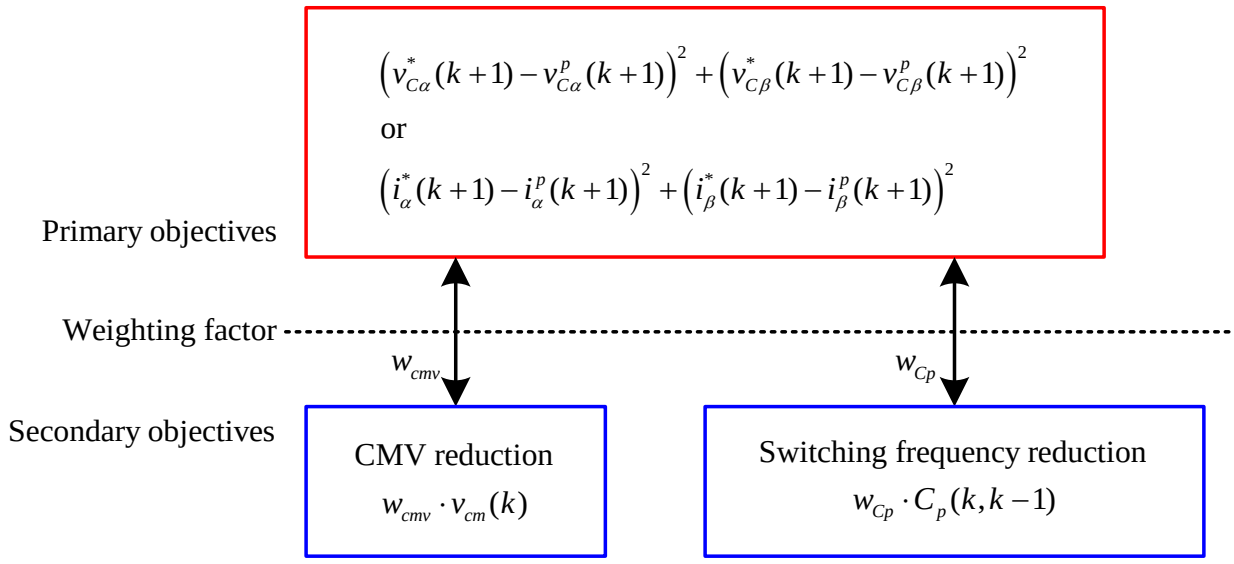


Fig. 2.7 Overview of cost function definition with primary and secondary objectives in CSC.

2.3.3.1 Primary Control Goal

For a CSC, there are mainly two kinds of primary control goals, output voltage reference tracking and load current tracking. Since the variables are expressed at space vector format in $\alpha\beta$-axis stationary frame, the cost function for output voltage reference tracking can be given as

$$g(k)=\left(v^*_{C\alpha}(k+1)-v^p_{C\alpha}(k+1)\right)^2+\left(v^*_{C\beta}(k+1)-v^p_{C\beta}(k+1)\right)^2 \tag{2.33}$$

The cost function for load current reference tracking can be given as

$$g(k)=\left(i^*_{\alpha}(k+1)-i^p_{\alpha}(k+1)\right)^2+\left(i^*_{\beta}(k+1)-i^p_{\beta}(k+1)\right)^2 \tag{2.34}$$

The cost functions used here are quadratic functions. Absolute minimization functions can also be used as cost function. But quadratic function can achieve over proportionate control action against the reference tracking [45]. So quadratic functions are chosen and utilized in the following research.

2.3.3.2 Secondary Control Goal

To improve the performance of converter or to meet particular technical requirements, some secondary objectives such as common-mode voltage reduction and average switching frequency reduction can be easily included in the cost function as demonstrated in Fig. 2.7.The relative

importance of one objective over the other can be set through the weighting factors. Since the primary objective is essential to ensure the proper operation of power converter, the weighting factor for primary objective part is normally selected as 1. The CMV reduction objective is expressed as another cost function as

$$g_{cmv}(k) = w_{cmv} \cdot v_{cm}(k) \tag{2.35}$$

where w_{cmv} is the weighting factor for CMV reduction. $v_{cm}(k)$ is the possible common mode voltage at *k*th instant, which is just related to filter capacitor voltage and possible switching state at *k*th instant.

The average switching frequency reduction can be achieved by penalizing the cost function as

$$g_{Cp}(k) = w_{Cp} \cdot C_p(k, k-1) \tag{2.36}$$

where w_{Cp} is the weighting factor for average switching frequency minimization. $C_p(k, k-1)$ denotes the total number of commutations between the switching state at (*k*-1)th instant and possible switching state at *k*th instant. In order to reduce the computational effort, the numbers of commutations have been calculated off-line and store in the digital signal processor, as listed in Table 2.1.

Table 2.1 NUMBER OF COMMUTATIONS FOR EACH SWITCHING STATE TRANSITION

C_p	$\vec{I}_1$	$\vec{I}_2$	$\vec{I}_3$	$\vec{I}_4$	$\vec{I}_5$	$\vec{I}_6$	$\vec{I}_7$	$\vec{I}_8$	$\vec{I}_9$
$\vec{I}_1$	0	2	4	4	4	2	2	2	4
$\vec{I}_2$	2	0	2	4	4	4	2	4	2
$\vec{I}_3$	4	2	0	2	4	4	4	2	2
$\vec{I}_4$	4	4	2	0	2	4	2	2	4
$\vec{I}_5$	4	4	4	2	0	2	2	4	2
$\vec{I}_6$	2	4	4	4	2	0	4	2	2
$\vec{I}_7$	2	2	4	2	2	4	0	4	4
$\vec{I}_8$	2	4	2	2	4	2	4	0	4
$\vec{I}_9$	4	2	2	4	2	2	4	4	0

2.3.3.3 Selection of Weighting Factor

Since the control variables possess different physical nature, they lead to coupling effects and thus the selection of suitable weighting factors becomes tedious. The analytical or numerical procedure for the weighting factor selection is still an open topic for research. In [78], some guidelines are presented for the selection of the weighting factor.

2.3.4 Delay Compensation

The FCS-MPC strategy uses optimization algorithm and thus incurs large number of online calculations. The computer simulations represent ideal case where the time taken to compute these online calculations is zero [45]. According to this approach, the switching state which minimizes the error at (k+1)th instant is selected and applied at kth instant, as Fig. 2.5 shows.

However, in the real-time implementation of FCS-MPC strategy, the large number of online calculations introduce considerable time delay in the actuation [45]. As Fig. 2.8 shows, the delay caused by calculation burden will degrade, or even deteriorate the reference tracking performance. Hence, it must be compensated for.

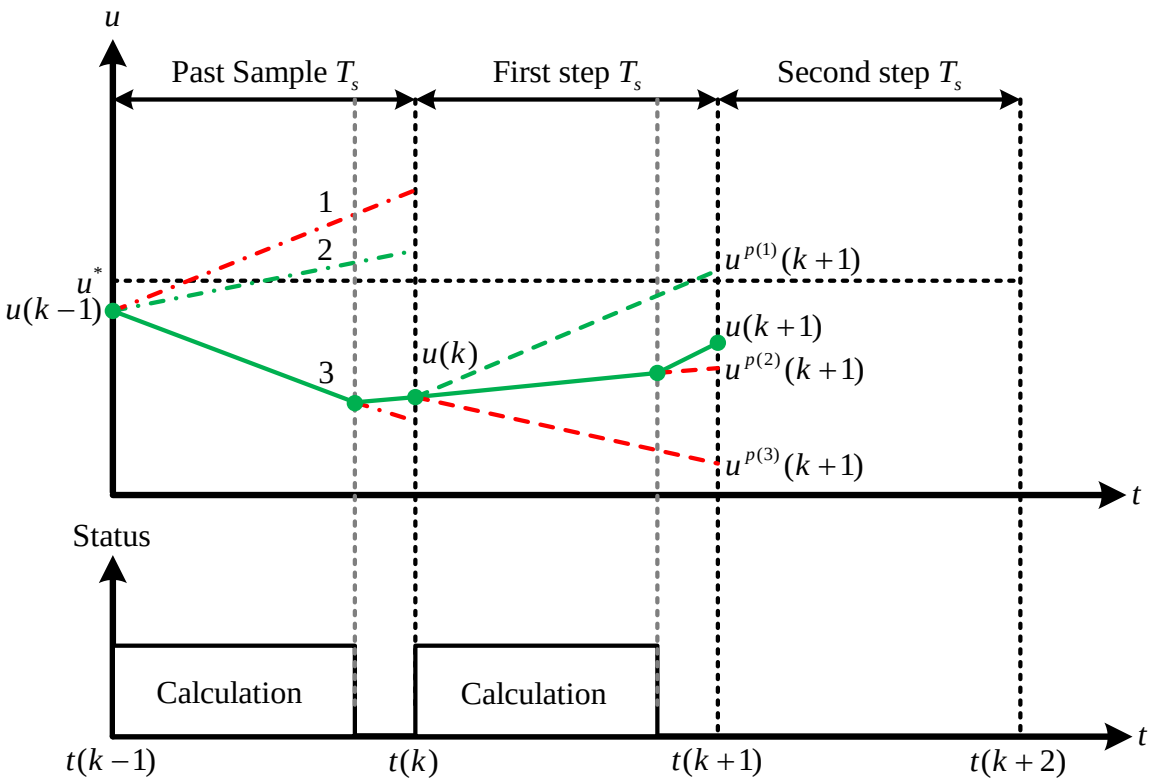


Fig. 2.8 One-step prediction with calculation delay and without compensation.

This calculation delay can be compensated by calculating the cost function for two sampling intervals ahead at (k+2)th instant, and this approach allows one sampling period for the control delay compensation and another sampling period for the optimization algorithm. The selected optimal switching state can be applied at (k+1)th sampling instant. The principle of the delay compensation method is illustrated in Fig. 2.9.

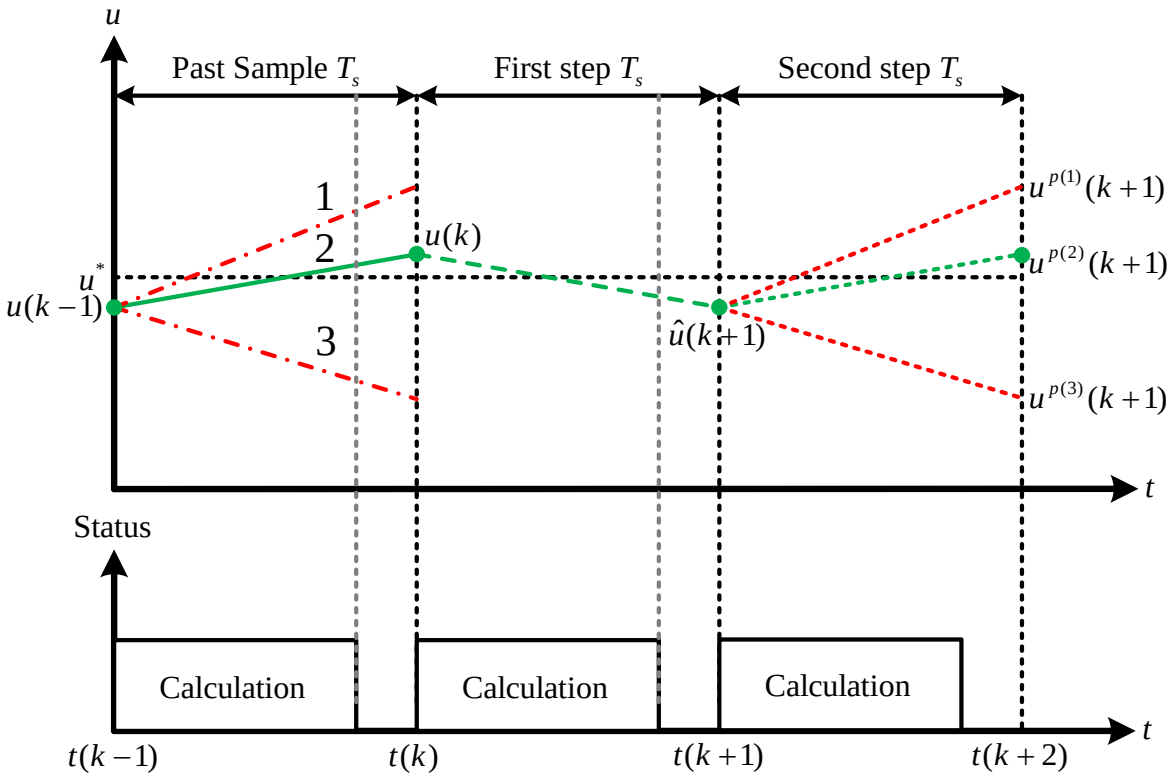


Fig. 2.9 Delay compensation method with modified one-step prediction.

According to this method, the optimal switching state from the previous iteration $x_{op}(k)$ is used to estimate the variables at (k+1)th instant ($\hat{u}(k+1)$), and all the possible switching states are used to predict the variables at (k+2)th instant. Then, the optimal switching state for (k+1)th instant $x_{op}(k+1)$ is selected and will be applied at (k+1)th instant.

2.4 Conclusions

In this chapter, three different discretization methods are introduced, and compared with each other, Finally, Heun's method is finally chosen to be applied to derive prediction models of three typical configurations of CSC, which are the foundation of various MPCs presented in the following chapters. Besides, some general concerns on MPC for high power CSC have also been discussed including prediction horizon selection, reference extrapolation, flexibility of cost function, and calculation delay compensation.

3 Model Predictive Power Factor Control With Active Damping Function for Current-Source Rectifier

In this chapter, model predictive power factor control (MPPFC) with active damping function is proposed for high power CSR, which tackles *LC* resonance and line power factor (PF) control issues in CSR. For reference, the configuration of a CSR has been depicted in Fig. 1.13. *LC* resonance is an inherent issue in CSR, especially the case with small line-side resistance. The demerits of the existing active damping methods for traditional linear controls and the challenges on importing active damping function into MPC can be referred to Section 1.4.5. In aspect of line PF regulation, the drawbacks of the traditional linear controls and MPC can be found in Section 1.4.5 as well. The innovation of MPPFC with active damping function can be classified as

- A line reactive power reference estimator with online capacitance correction, which is based on the line-side model of a CSR, is designed to modify the line reactive power reference based on operating states of a CSR for the purpose on maintaining unity PF or maximum achievable power factor (MAPF) at line side;
- To mitigate *LC* resonance during transients, the calculated damping current is intuitively superposed on the line current reference to achieve active damping effect. A novel damping current calculation method, which avoids the use of low-pass filter (LPF) or band-stop filter (BSF) is also proposed.

The merits offered by MPPFC with active damping function can be summarized as

- In comparison with the traditional linear line PF control, MPPFC avoids simultaneous adjustments on coupled variables, such as modulating index and delay angle for CSR. Besides, the DC current is not intentionally increased in MPPFC;
- Compared to the traditional linear controls with active damping function, MPPFC not only makes PF regulated, but also achieves better steady-state performance at line side. Moreover, there is no LPF and BSF used in MPPFC, which realizes better dynamic performance and simpler structure;

- In contrast to conventional MPC for CSR, MPPFC provides accurate line PF control, which also involves active damping function inside, and makes itself more suitable for high power MV CSR with lightly damped *LC* circuit.

3.1 Line Power Factor Control

3.1.1 Line Reactive Power Reference Estimator

A line reactive power reference estimator is proposed to keep unity PF or MAPF for CSR under various operating conditions. Normally, unity PF between power supply voltage and line current is anticipated. However, this requirement is invalid under mainly two conditions

1) when the DC current is too small, CSR cannot compensate all the leading capacitor current, and three-phase power supply needs to absorb extra capacitive reactive power;

2) the average DC-side voltage is so close to its rated value that the phase angle of the fundamental component in the input current of CSR does not have enough room to be regulated.

In *dq*-axis synchronous frame, with respect to the utility power supply voltage vector, $\vec{v}_g$, the space vector diagram for the line side of CSR is shown in Fig. 3.1, in which $\vec{v}_g$ and $\vec{i}_g$ can be given as

$$\begin{cases} \vec{v}_g = V_{gd} \\ \vec{i}_g = I_{gd} + jI_{gq} \end{cases} \tag{3.1}$$

where V_{gd} is the *d*-axis component of $\vec{v}_g$, which can be considered as a constant value, and equal to the magnitude of $\vec{v}_g$; I_{gd} and I_{gq} are the *d*- and *q*-axis components of $\vec{i}_g$, respectively.

Based on (3.1), the fundamental component in the voltage vector across the filter inductor can be given by

$$\vec{v}_{Lf(1)} = j\omega_g L_f \vec{i}_g \tag{3.2}$$

where ω_g is the line-side angular frequency, which is equal to 377rad/s, and corresponding to 60Hz.

Then, the fundamental components in the capacitor voltage vector and the capacitor current vector can be given by

$$\begin{cases} \vec{v}_{Cr(1)} = \vec{v}_g - \vec{v}_{Lf(1)} \\ \vec{i}_{Cr(1)} = j\omega_g C_r \vec{v}_{Cr(1)} \end{cases} \tag{3.3}$$

Finally, the fundamental component of the input current vector, $\vec{i}_{wr(1)}$, can be given by

$$\vec{i}_{wr(1)} = \vec{i}_g - \vec{i}_{Cr(1)} \tag{3.4}$$

Substituting (3.1) to (3.3) into (3.4), we have

$$\vec{i}_{wr(1)} = \left(1-\omega_g^2 C_r L_f\right) I_{gd} + j\left(\left(1-\omega_g^2 C_r L_f\right) I_{gq} - \omega_g C_r V_{gd}\right) \tag{3.5}$$

The modulus of both sides of (3.5) can be given by

$$\begin{aligned} \left|\vec{i}_{wr(1)}\right| &= \left|\left(1-\omega_g^2 C_r L_f\right) I_{gd} + j\left(\left(1-\omega_g^2 C_r L_f\right) I_{gq} - \omega_g C_r V_{gd}\right)\right| \\ &= m_r I_{dc} \end{aligned} \tag{3.6}$$

where m_r is the modulating index for CSR. When m_r is unity, the modulus of $\vec{i}_{wr(1)}$ is equal to I_{dc}, which indicates that the maximum compensation for the capacitor leading current can be achieved. With m_r equal to 1, I_{gq} can be calculated based on (3.6). After some arrangements, a quadratic equation can be established as (3.7) with the terms A and B expressed, respectively, by (3.8)

$$\mathrm{A}^2 \cdot I_{gq}^2 - 2\mathrm{AB} \cdot I_{gq} + \mathrm{B}^2 + \mathrm{A}^2 \cdot I_{gd}^2 - I_{dc}^2 = 0 \tag{3.7}$$

$$\mathrm{A} = 1-\omega_g^2 C_r L_f \text{ and } \mathrm{B} = \omega_g C_r V_{gd} \tag{3.8}$$

After substituting (3.8) into (3.7), the solutions to I_{gq} can be given by

$$I_{gq} = \frac{\mathrm{B} \pm \sqrt{-\mathrm{A}^2 \cdot I_{gd}^2 + I_{dc}^2}}{\mathrm{A}} \tag{3.9}$$

where I_{gd} can be further given by

$$I_{gd} = \frac{P_g}{1.5V_{gd}} = \frac{P_{dc}/\eta}{1.5V_{gd}} = \frac{I_{dc}^2 R_{dc}/\eta}{1.5V_{gd}} \tag{3.10}$$

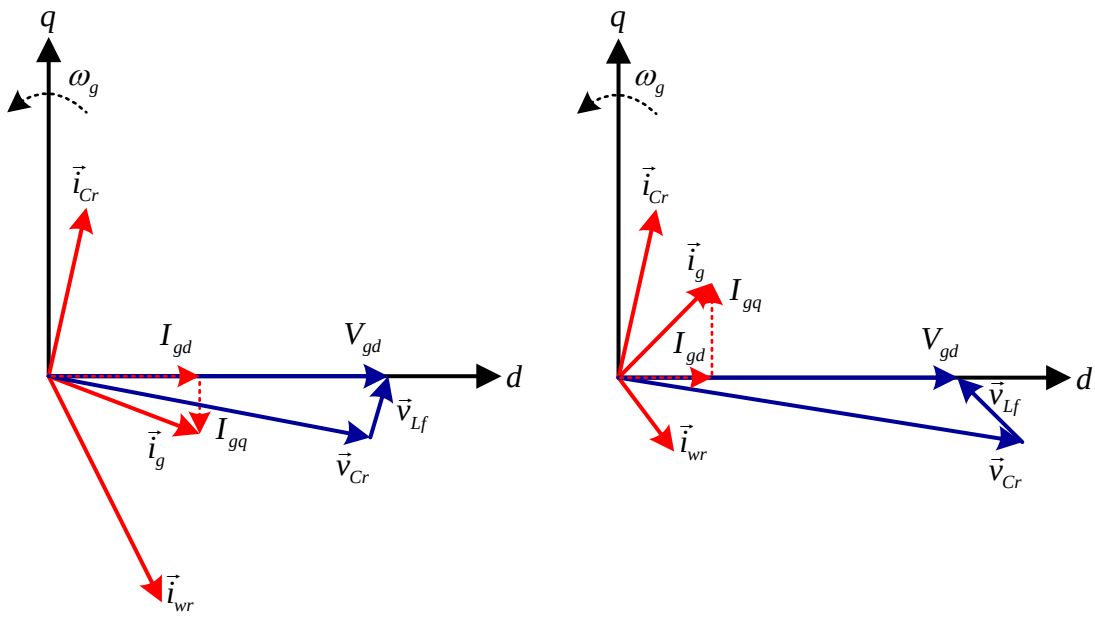
in which P_g is the line active power, η is the efficiency of CSR, and P_{dc} is the DC-side active power, equal to $I_{dc}^2 R_{dc}$. Based on (3.9) and (3.10), i_{gq} can be calculated with a specified DC current and DC load resistor. There are two values obtained from (3.9). The positive symbol before the square root term in I_{gq} represents no compensation for the capacitor leading current, and the negative symbol denotes the maximum compensation for the capacitor leading current. In order to achieve unity PF or MAPF, the second solution with negative symbol should be selected and given by

$$I_{gq} = \frac{\mathrm{B} - \sqrt{-\mathrm{A}^2 \cdot I_{gd}^2 + I_{dc}^2}}{\mathrm{A}} \tag{3.11}$$

If I_{gq} is smaller than 0, $\vec{i}_{wr}$ is enough to compensate all the capacitor leading current, even making the line PF lagging, as Fig. 3.1 (a) shows. Hence, Q_g^* can be set to 0. In Fig. 3.1 (b), if I_{gq} is larger than 0, $\vec{i}_{wr}$, even with the maximum compensation, is still not enough to compensate all the capacitor leading current. Then, Q_g^* should be calculated based on I_{gq}. Therefore, Q_g^* can be given by

$$Q_g^* = \begin{cases} 0 & , \quad I_{gq} \le 0 \\ -1.5V_{gd} I_{gq}, & I_{gq} > 0 \end{cases} \tag{3.12}$$

where V_{gd} is considered as a constant value.



(a) (b)

Fig. 3.1 Space vector diagram for line side of CSR: (a) line PF lagging and (b) line PF leading.

Based on (3.8) and (3.11), it can be found that I_{gq} heavily depends on the parameters of CSR, such as L_f and C_r, so inaccurate system parameters have impacts on Q_g^*. Based on Q_g^*, MAPF can be given by

$$\text{MAPF}=\frac{P_g}{\sqrt{P_g^2+(Q_g^*)^2}} \tag{3.13}$$

Fig. 3.2 (a) shows MAPF with different capacitors at various DC current conditions. The range, over which the line PF is equal to unity, shrinks with the increase of filter capacitance. For example, at 0.4pu DC current condition, MAPF with 0.4pu capacitor is 0.987, whereas, MAPF decreases to only 0.480 with 0.6pu capacitor. Similarly, at 0.3pu DC current condition, MAPF with 0.4pu capacitor is only 0.536, but that with 0.2pu capacitor can still be maintained at unity. MAPF with different filter inductances at various DC current conditions is shown in Fig. 3.2 (b). It can be found that with filter inductance varied from 0.05pu to 0.15pu there is no apparent influence on MAPF. Over the whole range of DC current, the three curves in Fig. 3.2 (b) closely align with each other. In contrast to filter inductor, the discrepancy between the real

capacitance and the value used in calculation has more significant impact on MAPF, especially at low DC current condition.

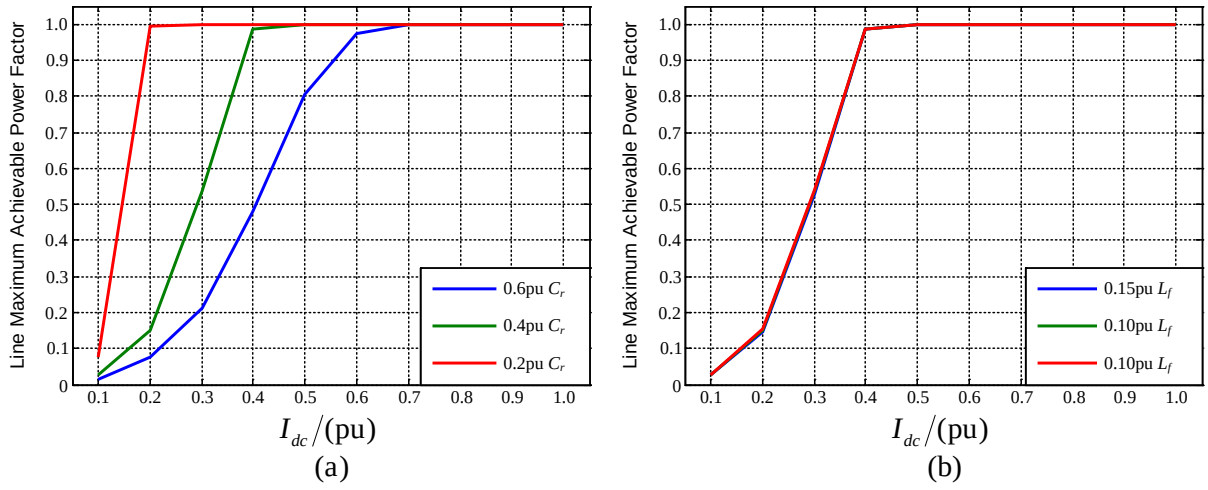


Fig. 3.2 Profile of MAPF versus DC current: (a) with different capacitors and (b) with different filter inductors.

In order to ensure the accuracy of the line reactive power reference estimator, an online capacitance estimation method is introduced into the line reactive power reference estimator to improve its performance under capacitance mismatch condition, in consideration of the impact of capacitance on MAPF. Based on (2.21), the derivative of the capacitor voltage vector can be given by

$$C_r \frac{d\vec{v}_{Cr}}{dt} = \vec{i}_g - \vec{i}_{wr} \tag{3.14}$$

(3.14) can be discretized with backward Euler method as

$$C_r \frac{\vec{v}_{Cr}(k) - \vec{v}_{Cr}(k-1)}{T_s} = \vec{i}_g(k-1) - \vec{i}_{wr}(k-1) \tag{3.15}$$

where $\vec{v}_{Cr}(k)$ and $\vec{v}_{Cr}(k-1)$ represent the capacitor voltage vectors at kth and (k-1)th sampling instants; $\vec{i}_g(k-1)$ and $\vec{i}_{wr}(k-1)$ represent the line current vector and the applied input current vector at (k-1)th sampling instant. Considering the α-axis components in (3.15), the estimated capacitance can be given by

$$\hat{C}_r = \frac{T_s\left(i_{g\alpha}(k-1) - i_{wr\alpha}(k-1)\right)}{v_{Cr\alpha}(k) - v_{Cr\alpha}(k-1)} \tag{3.16}$$

However, since (3.16) is derived from the discretization of a derivative operation, which is very sensitive to measurement noise, the estimated capacitance value fluctuates all the time, and cannot be directly used in the line reactive power reference estimator. Hence, a regulation method for stabilizing the estimated capacitance is proposed here, as Fig 3.3 shows, where C_r^{init} is the initial capacitance; C_r^{est} is the finally estimated capacitance. After passing through a low-pass filter (LPF), $\hat{C}_r$ is sent to a PI controller. C_r^{init} is used as a feedforward in this regulation method. There are two advantages offered by this method. First, there is no influence caused by the estimated capacitance regulation method on start-up process, due to the feedforward of C_r^{init}; Second, the PI controller also provides some filtering effect, which ensures C_r^{est} stabler.

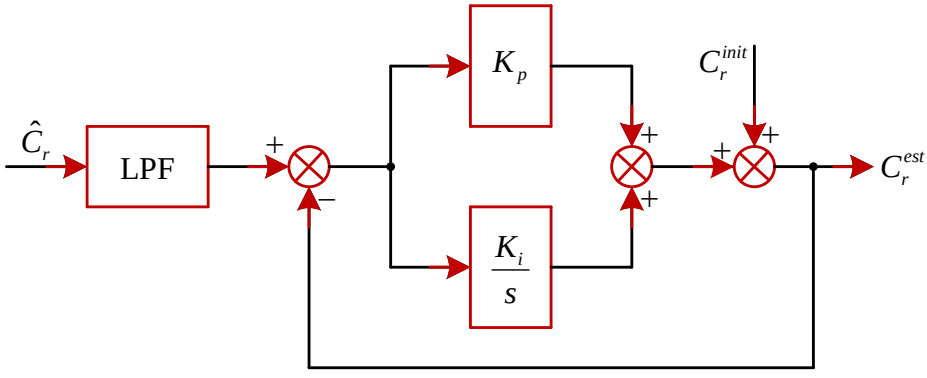


Fig 3.3. Diagram of regulation method for estimated capacitance.

3.1.2 Predictive Line Current Control

In MPPFC, the line active power reference, P_g^*, is obtained from a PI controller for DC current regulation. Then, substituting the *d*-axis line current reference, I_{gd}^*, and the DC current reference, I_{dc}^*, into (3.11) and (3.12), the *q*-axis line current reference, I_{gq}^*, and the line reactive power reference, Q_g^*, can be calculated. Since MPPFC is realized in $\alpha\beta$-axis stationary frame, the line current reference in $\alpha\beta$-axis can be expressed as

$$\begin{cases} i_{g\alpha}^{*} = \dfrac{2}{3}\dfrac{v_{g\alpha}}{v_{g\alpha}^2 + v_{g\beta}^2} P_g^{*} + \dfrac{2}{3}\dfrac{v_{g\beta}}{v_{g\alpha}^2 + v_{g\beta}^2} Q_g^{*} \\ i_{g\beta}^{*} = \dfrac{2}{3}\dfrac{v_{g\beta}}{v_{g\alpha}^2 + v_{g\beta}^2} P_g^{*} - \dfrac{2}{3}\dfrac{v_{g\alpha}}{v_{g\alpha}^2 + v_{g\beta}^2} Q_g^{*} \end{cases} \tag{3.17}$$

Based on (2.23), the line current vector at (k+1)th sampling instant, $\vec{i}_g(k+1)$, can be predicted. In MPPFC, the active and reactive power control is realized by tracking the line current references, which is achieved by a cost function as

$$g(k) = \left| \hat{\vec{i}}_g^{*}(k+1) - \vec{i}_g^{\,p}(k+1) \right|^2 \tag{3.18}$$

where $\hat{\vec{i}}_g^{*}(k+1)$ is the estimated line current reference vector at (k+1)th sampling instant, which can be calculated through vector extrapolation method, and given by

$$\hat{\vec{i}}_g^{*}(k+1) = \vec{i}_g^{*}(k) e^{j\omega_g T_s} \tag{3.19}$$

During each sampling interval, the optimal switching state leading to the minimum value of (3.18) is selected from the nine possible switching states, and applied during the entire sampling interval, in order to closely track the line current references.

3.1.3 Switching Frequency Reduction

A crucial issue in high power applications is the efficiency of power converters, to which switching losses are particularly relevant. With MPPFC, the average switching frequency, and consequently the switching losses, can be reduced by adding a switching commutation related term to the cost function (3.18). This new term penalizes those switching states producing larger number of switching commutations from one sampling interval to the next. The new cost function can be given by

$$g'(k) = g(k) + w_{sw} \sum_{x=1,2,\ldots,6} \left| S_x(k) - S_x(k-1) \right| \tag{3.20}$$

where $S_x(k-1)$ represents the optimally selected switching states of six switching devices in the CSR during (k-1)th sampling interval; $S_x(k)$ represents the predicted switching states for kth

sampling interval; w_{sw} is a weighting factor, which can be increased to give more priority to switching frequency reduction over line current regulation. In consideration of delay caused by calculation, with the two-step prediction method introduced in Section 1.5.2, (3.20) also needs to be shifted one-step ahead, and given by

$$g'(k+1) = \left|\hat{\vec{i}}_g^{*}(k+2) - \vec{i}_g^{\,p}(k+2)\right|^2 + w_{sw} \sum_{x=1,2,\ldots,6} \left|S_x(k+1) - S_x(k)\right| \tag{3.21}$$

where $\hat{\vec{i}}_g^{*}(k+2)$ and $\vec{i}_g^{\,p}(k+2)$ are the estimated line current reference vector and the predicted line current vector at (k+2)th instant; $S_x(k)$ represents the optimal switching state applied during kth sampling interval, and $S_x(k+1)$ represents the predicted switching state for (k+1)th sampling interval.

3.2 Active Damping Function Associated With MPPFC

Due to optimal switching state selection process, the input PWM current of MPPFC features spread harmonic distribution. Therefore, severe resonance is possibly excited in a lightly damped *LC* circuit. Hence, an active damping method, which is suitable for MPPFC, is crucial to guarantee its performance. However, unlike traditional linear control, there is no modulation stage and input PWM current reference used in MPPFC, which makes it challenging to involve active damping function into MPPFC. The other thing is that in conventional active damping methods, high frequency components in capacitor voltage are usually extracted to be used for damping current calculation. Since MPPFC is realized in $\alpha\beta$-axis stationary frame, band-stop filters (BSFs) are needed to filter out fundament components in capacitor voltages, which further complicate the control design. To overcome the two hurdles, a novel realization method is proposed to involve active damping function into MPPFC. Moreover, an intuitive approach to calculating damping current is also designed, which avoids the use of BSFs, and simplifies the control structure.

3.2.1 Damping Current Calculation

As Fig. 3.4 (a) shows, in conventional linear control, active damping uses CSR to emulate a damping resistor, R_{damp}, which is connected in parallel with capacitor. Then, damping current vector can be calculated by the division between harmonic components in capacitor voltage vector and R_{damp}. In the proposed damping current calculation method, capacitor voltage vector and filter inductor voltage vector can be given by

$$\begin{cases} \vec{v}_{Cr} = \vec{v}_{Cr(1)} + \vec{v}_{Cr(h)} \\ \vec{v}_{Lf} = \vec{v}_{Lf(1)} + \vec{v}_{Lf(h)} \end{cases} \tag{3.22}$$

where $\vec{v}_{Cr(1)}$ and $\vec{v}_{Cr(h)}$ represent the fundamental component and the harmonic component in $\vec{v}_{Cr}$; $\vec{v}_{Lf(1)}$ and $\vec{v}_{Lf(h)}$ represent the fundamental component and the harmonic component in $\vec{v}_{Lf}$. According to the line-side model of CSR, a voltage equation can be given by

$$\vec{v}_g = \vec{v}_{Lf} + \vec{v}_{Cr} \tag{3.23}$$

Substituting (3.22) into (3.23), after some arrangements, the voltage equation can be modified into

$$\vec{v}_g - \vec{v}_{Lf(1)} - \vec{v}_{Cr(1)} = \vec{v}_{Lf(h)} + \vec{v}_{Cr(h)} \tag{3.24}$$

Here it is assumed that power supply voltage vector, $\vec{v}_g$, only contains fundamental component. Hence, the left-hand side of (3.24) is equal to 0. Then, $\vec{v}_{Cr(h)}$ can be given by

$$\vec{v}_{Cr(h)} = -\vec{v}_{Lf(h)} = \vec{v}_{Cr} + \vec{v}_{Lf(1)} - \vec{v}_g \tag{3.25}$$

In MPPFC, $\vec{v}_{Cr}$ and $\vec{v}_g$ have been measured. Since the objective of the cost function in MPPFC is to track line current references, the fundamental component in filter inductor voltage, $\vec{v}_{Lf(1)}$, can be calculated by

$$\vec{v}_{Lf(1)} = j\omega_g L_f \vec{i}_g^{\,*} \tag{3.26}$$

Finally, based on $\vec{v}_{Cr(h)}$, damping current can be calculated as

$$\vec{i}_{damp} = \frac{\vec{v}_{Cr} + j\omega_g L_f \vec{i}_g^* - \vec{v}_g}{R_{damp}} \tag{3.27}$$

The equivalent circuit for the proposed damping current calculation is shown in Fig. 3.4 (b), the small-signal transfer function from input PWM current of CSR to line current can be given by

$$G(s) = \frac{I_g(s)}{I_{wr}(s)} = \frac{1}{s^2 C_r L_f + (L_f / R_{damp})s + 1} \tag{3.28}$$

It can be found from (3.28) that with the decrease of R_{damp} larger damping effect can be obtained, but higher damping current, which contains high frequency components, has more influence on the performance on tracking line current references. Here the value of R_{damp} is selected as 2pu, which makes a trade-off between damping effect and influence on tracking line current references.

3.2.2 Damping Current Associated into MPPFC

In MPPFC, the main challenge on involving damping current is that there are no modulating stage and reference vector used to generate input PWM current. Fortunately, according to Fig. 3.4 (b), the line current vector, $\vec{i}_g$, can be expressed by

$$\vec{i}_g = \vec{i}_{Cr} + \vec{i}_{wr} + \vec{i}_{damp} \tag{3.29}$$

which reveals that $\vec{i}_g$ also includes the emulated damping current vector. Hence, the damping effect can also be achieved by introducing the damping current vector into the line current reference vector. Considering calculation delay compensation, the estimated damping current at (k+1)th sampling instant can be given by

$$\hat{\vec{i}}_{damp}(k+1) = \frac{\hat{\vec{v}}_{Cr}(k+1) + j\omega_g L_f \hat{\vec{i}}_g^*(k+1) - \hat{\vec{v}}_g(k+1)}{R_{damp}} \tag{3.30}$$

where $\hat{\vec{v}}_{Cr}(k+1)$, $\hat{\vec{v}}_g(k+1)$ and $\hat{\vec{i}}_g^*(k+1)$ are the estimated capacitor voltage vector, power supply voltage vector, and line current reference vector at (k+1)th sampling instant, in which $\hat{\vec{v}}_g(k+1)$ can be calculated with space vector angle compensation, as

$$\hat{\vec{v}}_g(k+1) = \vec{v}_g(k)e^{j\omega_g T_s} \tag{3.31}$$

In order to associate damping current into MPPFC, the cost function needs to be further modified into

$$g(k+1) = \left|\hat{\vec{i}}_g^*(k+2) + \hat{\vec{i}}_{damp}(k+1) - \vec{i}_g^{\,p}(k+2)\right|^2 + w_{sw}\sum_{x=1,2,\ldots,6}\left|S_x(k+1) - S_x(k)\right| \tag{3.32}$$

where the damping current vector is introduced into the line current reference vector.

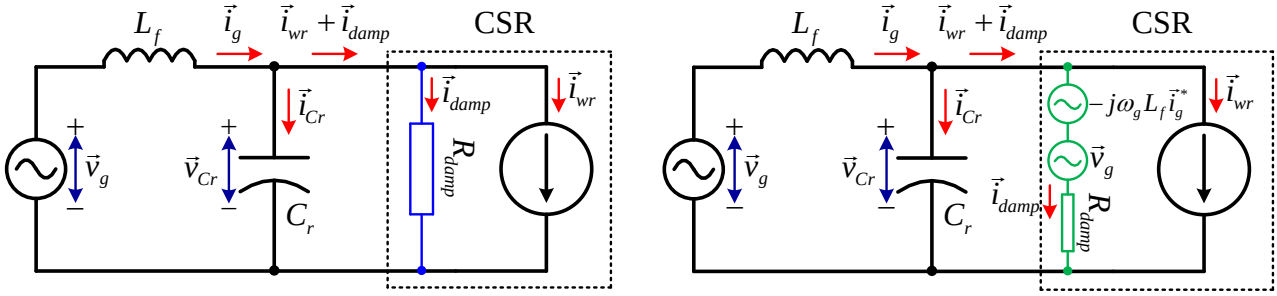


Fig. 3.4 Active damping methods for CSR: (a) traditional method and (b) proposed method.

Finally, the block diagram of MPPFC with active damping function and one-step delay compensation is shown in Fig. 3.5, which can be realized step-by-step as follows

1) At kth sampling interval, measure the power supply voltages, the line currents, the capacitor voltages, and the DC current first;

2) Estimate the capacitance using (3.16), and calculate the line reactive power reference using (3.11) and (3.12);

3) Update the prediction model, and estimate the line current and the capacitor voltage vector at (k+1)th sampling instant based on (2.23) and the optimal input PWM current vector selected during last sampling interval;

4) Calculate the line current reference vector using (3.17), and estimate the damping current vector at (k+1)th sampling instant using (3.30);

5) Predict the line current vector at (k+2)th instant using (2.23) based on all the possible input PWM current vectors for a CSR. The predicted line current vector is compared with the summation of the line current reference vector and the damping current vector using (3.32). The input PWM current vector minimizing (3.32) is applied to the CSR at the beginning of (k+1)th sampling interval.

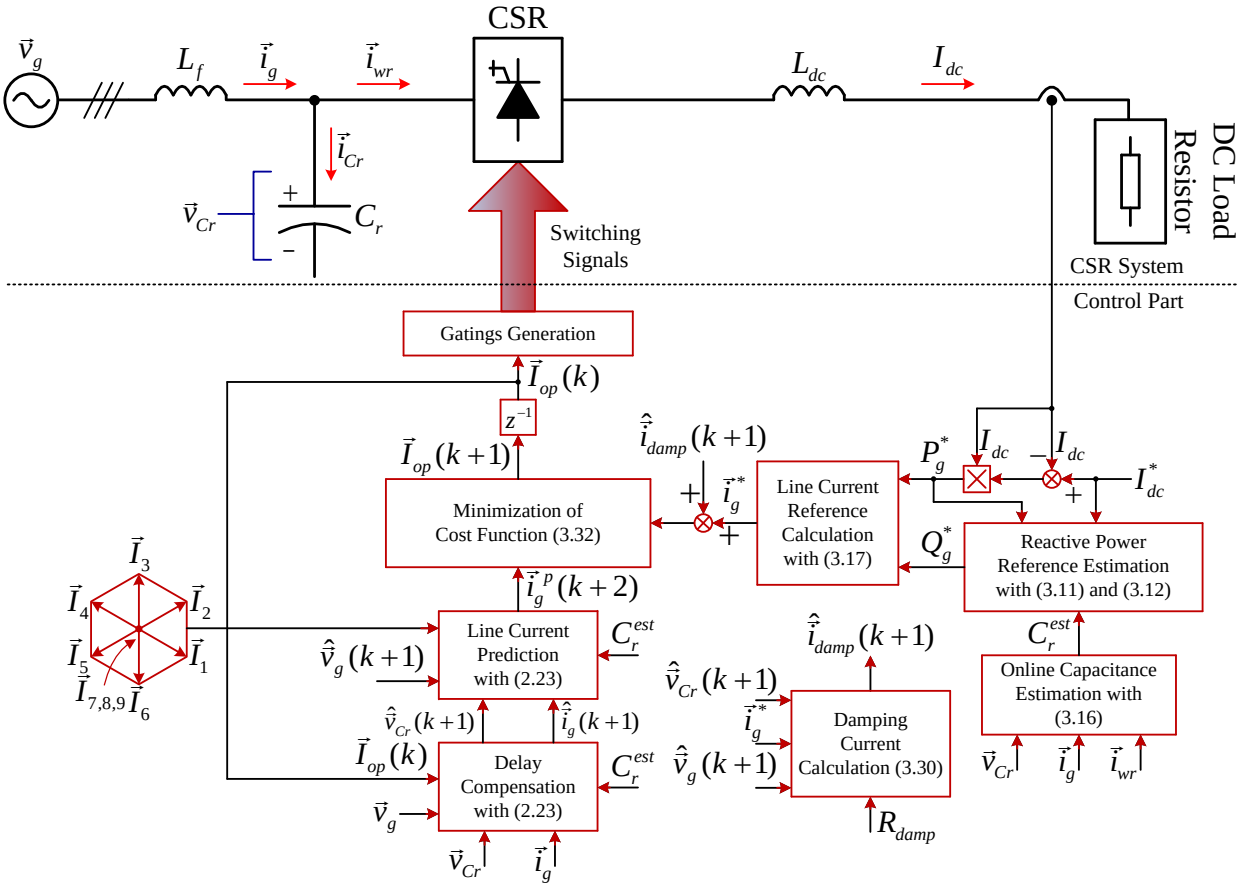


Fig. 3.5 Block diagram of MPPFC with active damping function.

3.3 Simulation Validation

To verify the performance of MPPFC, simulation on a high power CSR is conducted. The parameters used in the simulation are listed in Table 3.1. Besides, the simulated results of conventional MPC and modulating index control with active damping are also provided. SVM

with switching frequency of 1080Hz is used in modulating index control. The sampling intervals in both conventional MPC and MPPFC are 100μs . w_{sw} is selected as 0.4 in MPPFC. For simplicity, afterwards conventional MPC and modulating index control with active damping are called Scheme I and Scheme II, respectively. To evaluate switching losses by different control schemes, the average switching frequencies of conventional MPC and MPPFC are measured, and can be given by

$$\overline{f}_{sw} = \frac{\sum_{x=1,2,...,6} \overline{f}_{swx}}{6} \tag{3.33}$$

where $\overline{f}_{swx}$ is the average switching frequency of each power device in CSR, which is calculated by measuring the number of switching commutations for each power device over 30 consecutive fundamental cycles, which is equal to 0.5s with fundamental frequency of 60Hz.

Table 3.1 SIMULATION AND EXPERIMENTAL PARAMETERS

Variable	Description	Simulation	Experiment
V_{gLL}^{R}	Rated line-to-line voltage (L-L)	4160V	208V
P^{R}	Rated power	1MVA	5kVA
T_s	Sampling interval	100μs	100μs
L_f	Filter inductance	0.1pu	0.218pu
C_r	Capacitance	0.4pu	0.378pu
L_{dc}	DC link inductance	1pu	1.16pu
R_{dc}	DC resistor load	0.8pu	0.8pu

3.3.1 Steady State Performance

Fig. 3.6 shows the profile of the line PF versus the DC current. Only fundamental component in line current is used to calculate line PF. The line PF of MPPFC can closely align with MAPF (the purple dot line) over the whole DC current range, which demonstrates the effectiveness of the proposed line reactive power reference estimator. In comparison with MPPFC, Scheme I cannot ensure the line PF equal to MAPF value, since the line reactive power is not accurately regulated in its cost function. Scheme II produces the lowest line PF over the entire DC current range, since the capacitor current is totally not compensated in modulating index control.

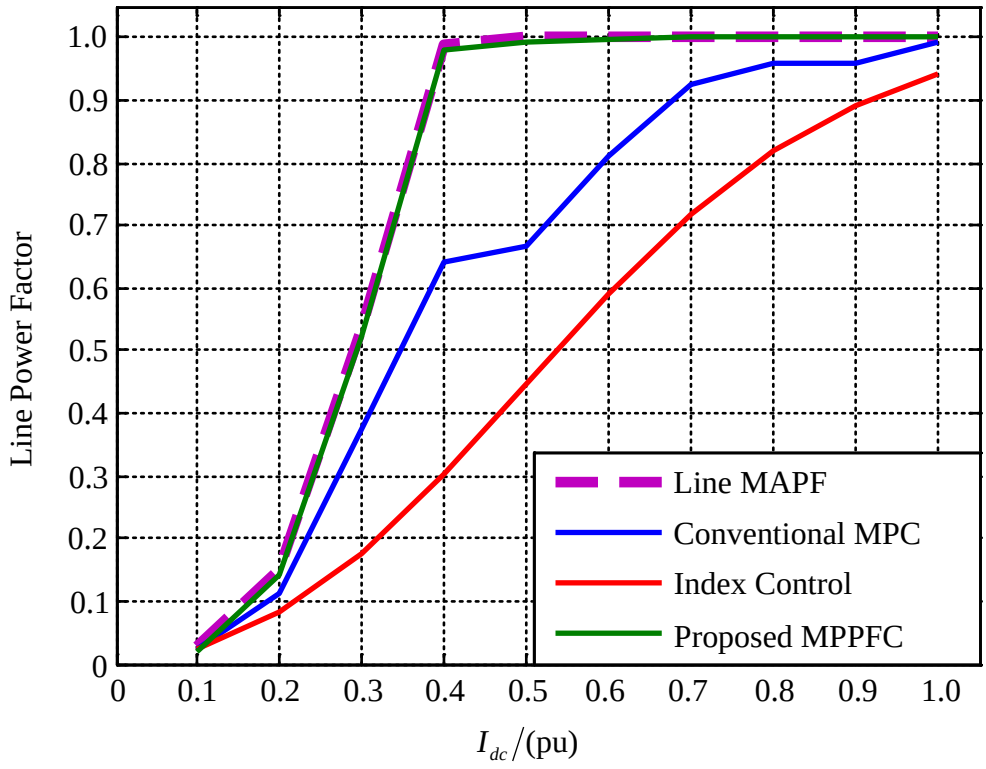


Fig. 3.6 Line power factor profile of three schemes.

Fig. 3.7 shows the THD profile of three schemes at various DC current conditions. Due to no active damping function involved and the distributed spectrum of the input PWM current, Scheme I produces very severe *LC* resonance with a lighted damped *LC* circuit, which results in deteriorating line current distortion and very high THD. In contrast to Scheme I, Scheme II and MPPFC generate much lower line current distortion. When compared to Method II at higher DC current conditions, MPPFC produces better performance on line current. On the other hand, the line current THD of Method II is smaller at lower DC current conditions, since the influence of input PWM current on the line current is weakened with lower modulating index. However, though Method II can guarantee very acceptable line current performance, it cannot achieve line PF regulation as that done with MPPFC.

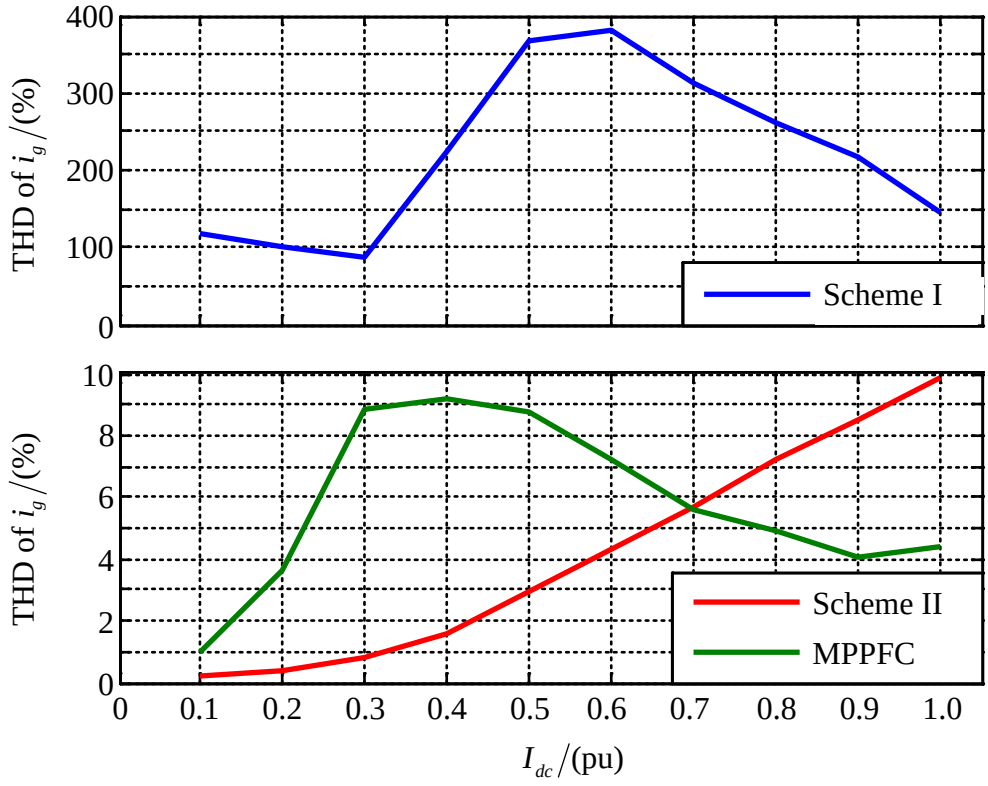


Fig. 3.7 Line current THD profile of three methods.

Fig. 3.8 shows the total demand distortion (TDD) profile of Scheme II and MPPFC at various DC current conditions. Since Scheme I leads to severe resonance and unacceptable distortion in the line current, hereby only the comparison between Scheme II and MPPFC is conducted. It can be found in Fig. 3.8 that with the DC current between 0.6 and 1.0pu, the TDD of MPPFC is smaller than that of Method II, and the maximum TDD appears when DC current is set to 1.0pu in both cases. Though the TDD of MPPFC becomes higher than that of Scheme II when the DC current is lower than 0.6pu, both of them have dropped into very insignificant range, specifically lower than 2%. On the other hand, the line-side performance of CSR should comply with the utility codes, especially IEEE standard 519-1992 [79]. Obviously, MPPFC can fulfill the requirement over the whole DC current range, whereas when the DC current is higher than 0.8pu, the TDD of Scheme II cannot meet the standard anymore, which implies that with MPPFC the volume of the *LC* filter in CSR has the potential to be further reduced, but in the case of Scheme II, the filter volume needs to be increased to meet the requirement over the whole operating range.

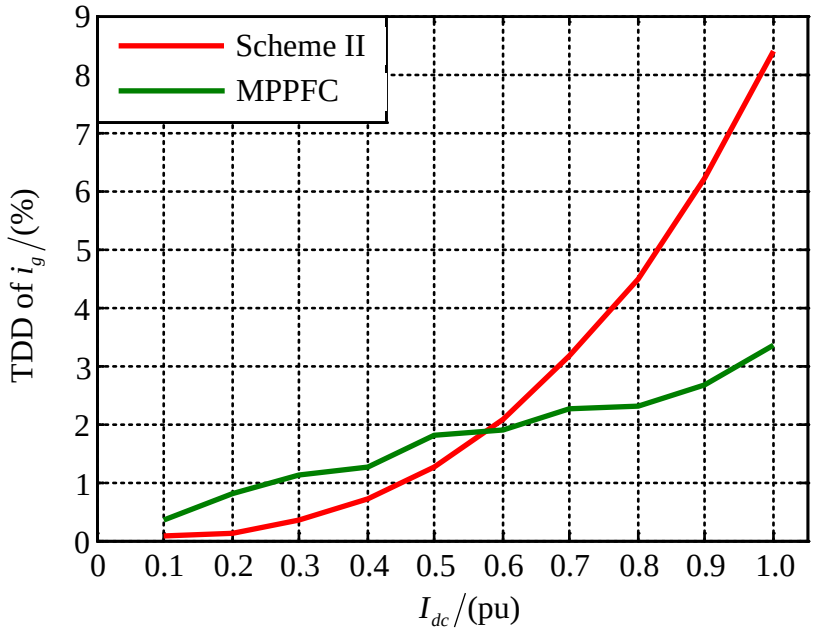


Fig. 3.8 Line current TDD profile.

In a high power MV CSR, the sizes of the filter inductor and the capacitor are normally around 0.1pu and 0.4 to 0.6pu, respectively. In terms of pu system, the size of the capacitor is apparently larger than that of the filter inductor. Hence, with the filter inductor fixed at 0.1pu, the maximum TDDs, appearing when the DC current is set to 1.0pu, are illustrated in Fig. 3.9 with respect to various capacitor sizes. Fig. 3.9 shows that only if the capacitor, C_r, is larger than 0.6pu, the maximum TDD of Scheme II can be kept not higher than 5%, whereas when C_r is not lower than 0.3pu, the maximum TDD of MPPFC can always meet the grid code requirements. From this point of view, with the same parameters except the capacitor and under the same operating condition, MPPFC can help reduce C_r by up to 50% in contrast to that of Scheme II.

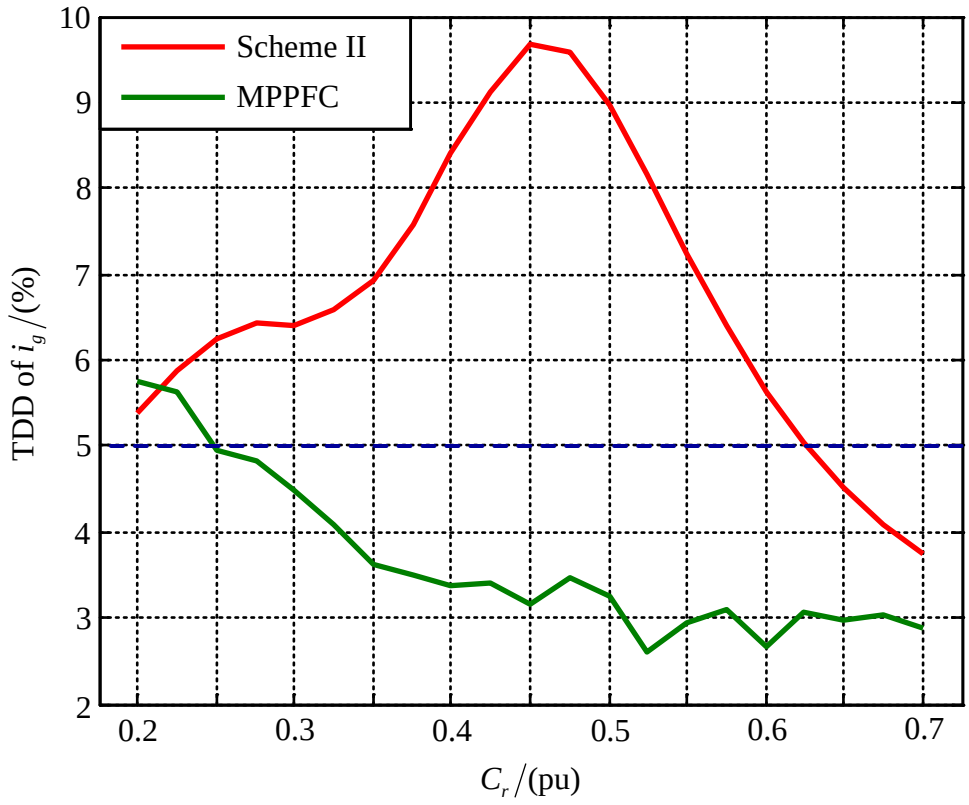


Fig. 3.9 Maximum TDD (I_{dc}=1.0pu) versus size of capacitor.

On the other hand, in order to justify the effect of reduced filter inductor on output performance, the maximum TDDs of MPPFC with different filter inductors, L_f, are shown in Fig. 3.10. It can be found that with L_f reduced to 0.08pu, the minimum requirement on C_r for MPPFC should be raised to 0.4pu. Based on the comparison between the two kinds of filter combinations, that are 0.1pu L_f with 0.3pu C_r and 0.08pu L_f with 0.4pu C_r, it can be found that 20% reduction on L_f would lead to 33.3% increase on C_r. Hence, it is suggested that MPPFC is mainly used for capacitor reduction purpose, which is more functional and effective.

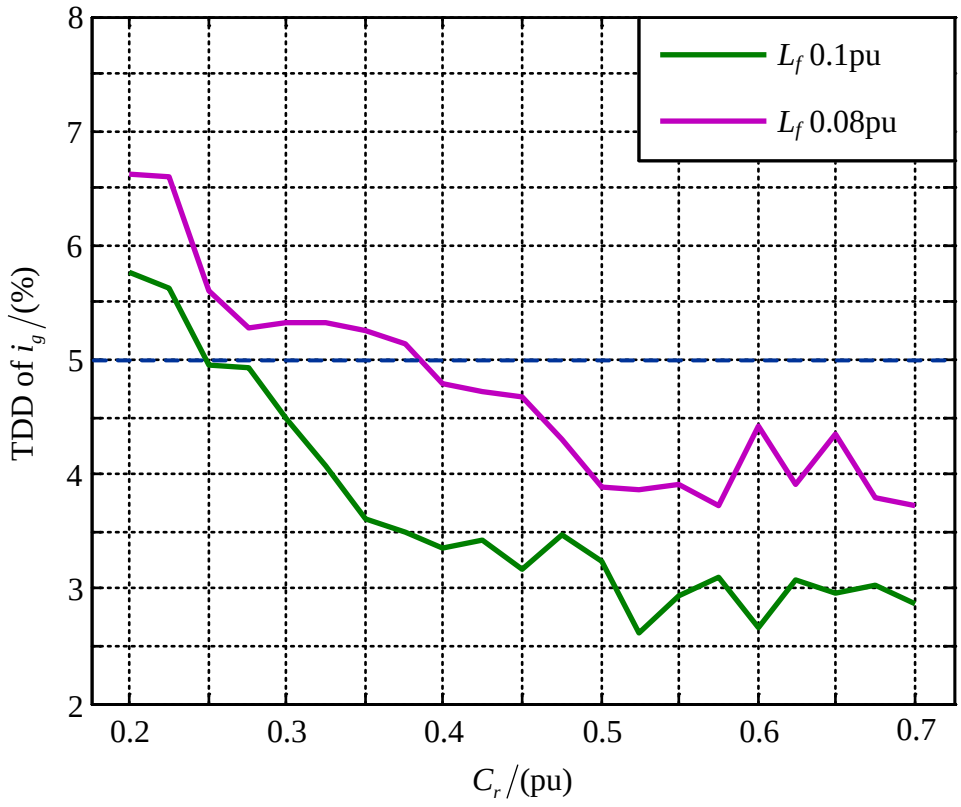


Fig. 3.10 Maximum TDD (I_{dc}=1.0pu) of MPPFC with different filter inductors.

Fig. 3.11 shows the switching frequency profiles of three schemes at various DC current conditions. The average switching frequencies of Scheme I and MPPFC are a little higher than that of Scheme II, which is equal to 1080Hz. Due to the effect of the switching commutations related term in (3.32), the average switching frequency of MPPFC has been very close to that of Scheme II over the whole DC current range. The average switching frequencies of Scheme I and MPPFC are very similar between each other, MPPFC offers significant advantages in terms of the performance on line PF regulation and line current distortion.

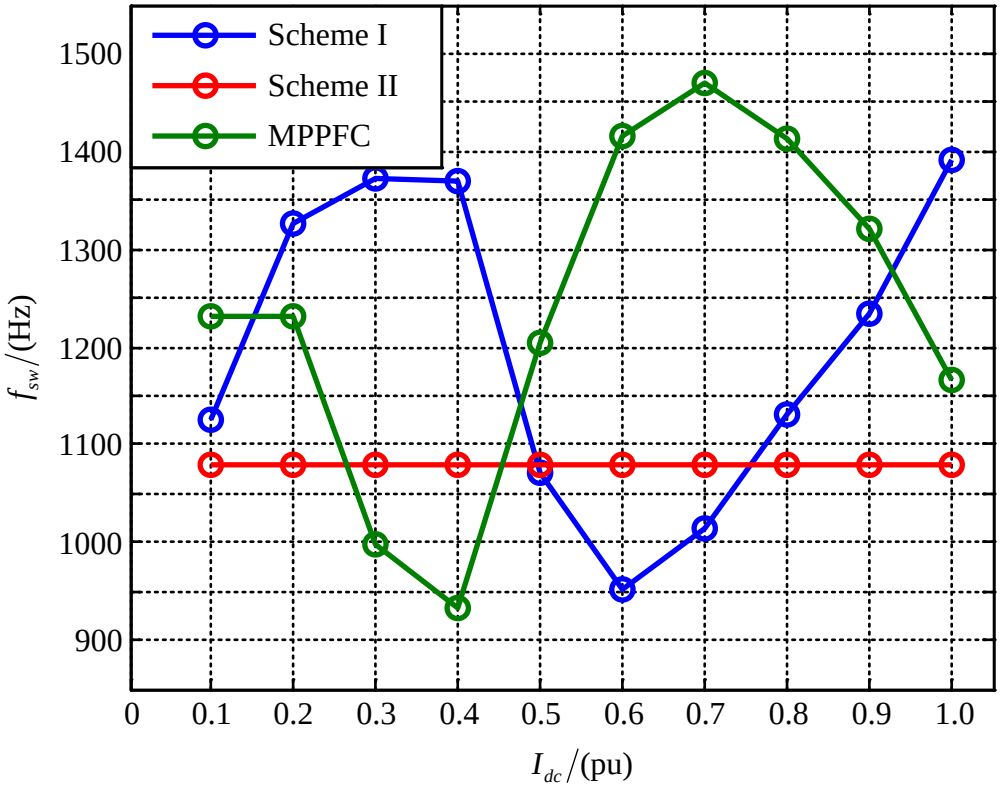
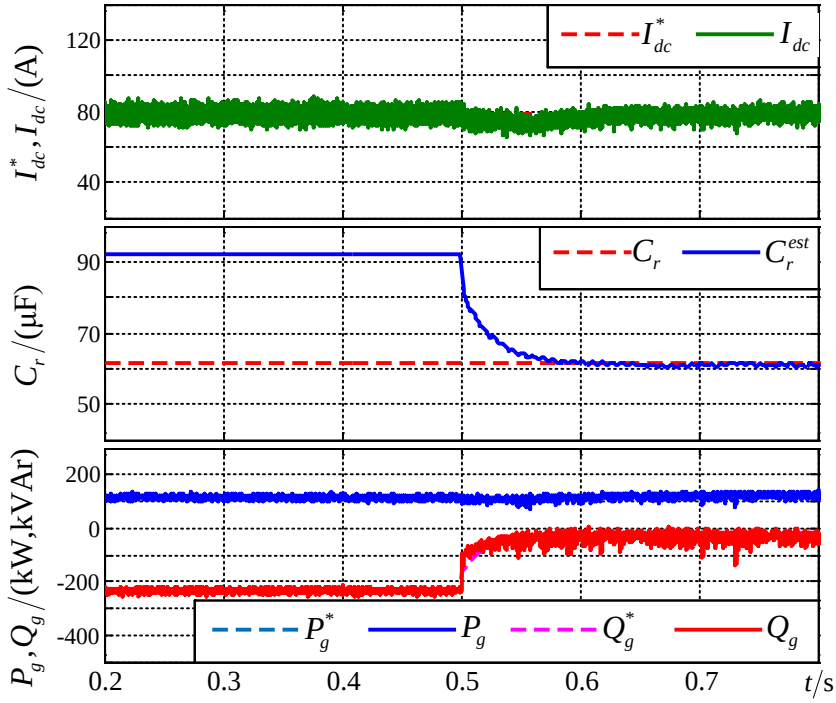


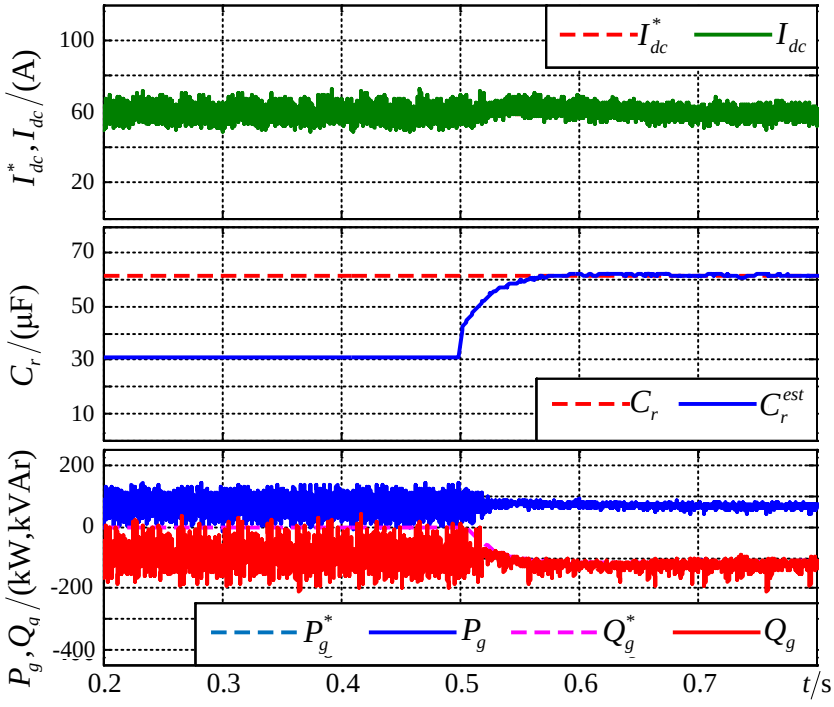
Fig. 3.11 Switching frequency profile of three schemes.

Fig. 3.12 verifies the effectiveness of the online capacitance correction of the line reactive power estimator. The real value of the capacitor is 0.4pu. From top to bottom, the DC current, the estimated capacitance, and the line active and reactive power are presented. In Fig. 3.12 (a), the initial capacitance used in the line reactive power estimator is 1.5 times its real value. The DC current reference is set at 0.4pu. The online capacitance estimation isn't activated until time *t* of 0.5s. Before 0.5s, due to the mismatched capacitance, the line reactive power reference is approximately -220kVAr, which makes the line PF only equal to 0.470. With the capacitance online estimation introduced, it can be observed that the estimated capacitance gradually approaches the real value. During this process, with the estimated capacitance modified, the line reactive power reference gradually becomes close to 0, which eventually makes the line PF around 0.98. In Fig. 3.12 (b), the initial capacitance is 0.5 times its real value, and the DC current reference is set to 0.3pu. The online capacitance estimation is also activated after 0.5s. Before 0.5s, with the mismatched capacitance, the line reactive power reference is 0. However, the unity line PF is totally unachievable at 0.3pu DC current condition. It can be found that the

line reactive power cannot follow its reference, and the line PF cannot be fixed at unity before 0.5s. Besides, the large ripples can be found in both line active and reactive powers and even the DC current. With the online capacitance estimation introduced at 0.5s, the estimated capacitance gradually increases to 0.4pu, and the line reactive power reference decreases to around -120kVAr. The line PF is finally kept at 0.48. With the accurate capacitance value, the ripples in both line active and reactive powers are significantly reduced, and the fluctuation in the DC current becomes smaller as well.



(a)

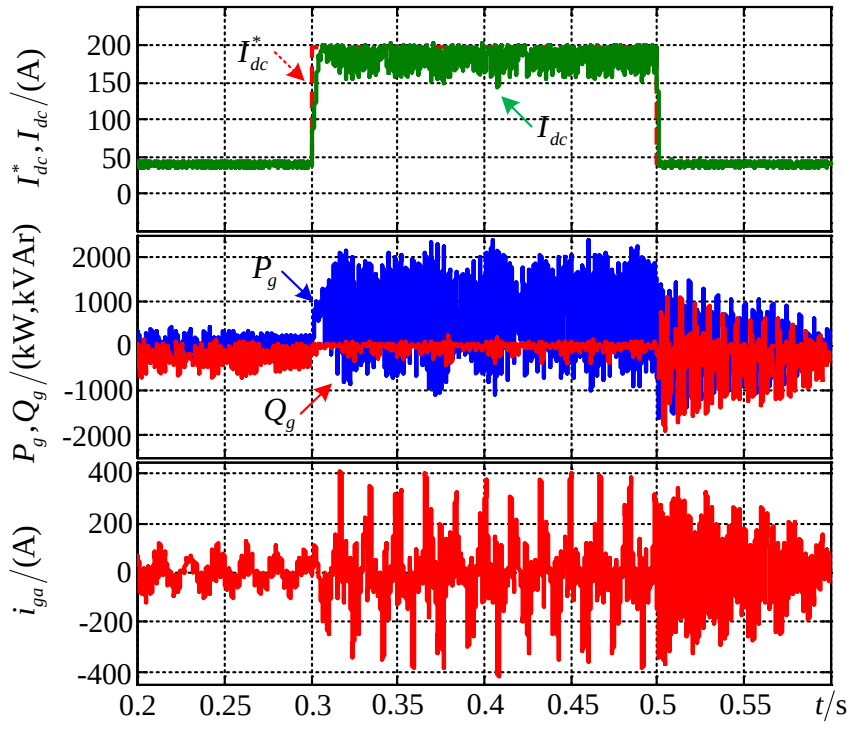


(b)

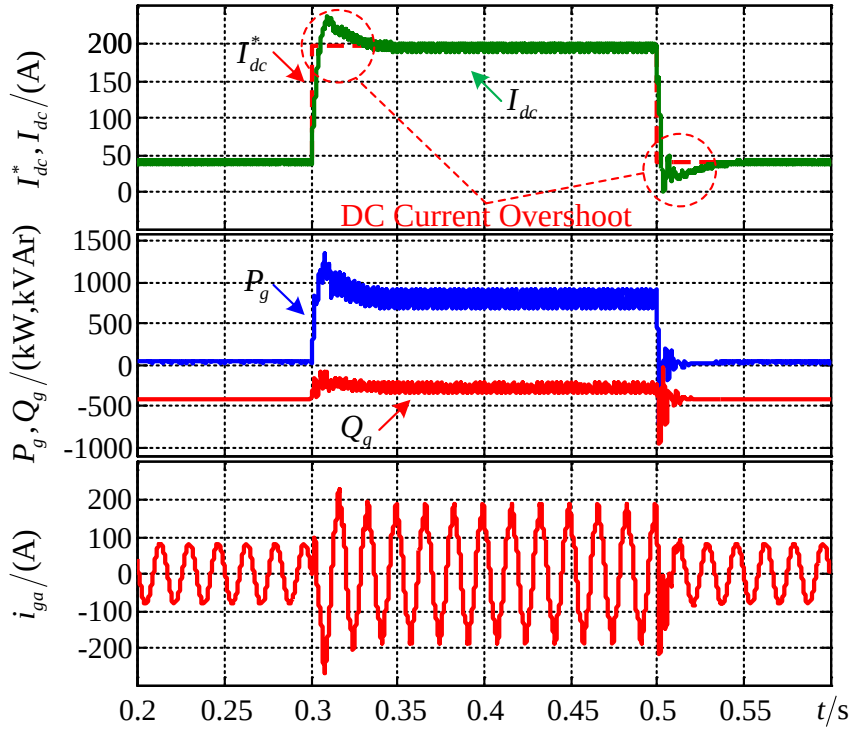
Fig. 3.12 Performance of online capacitance estimation: (a) 1.5 times mismatched capacitance at 0.4pu DC current, and (b) 0.5 times mismatched capacitance at 0.3pu DC current.

3.3.2 Dynamic Performance

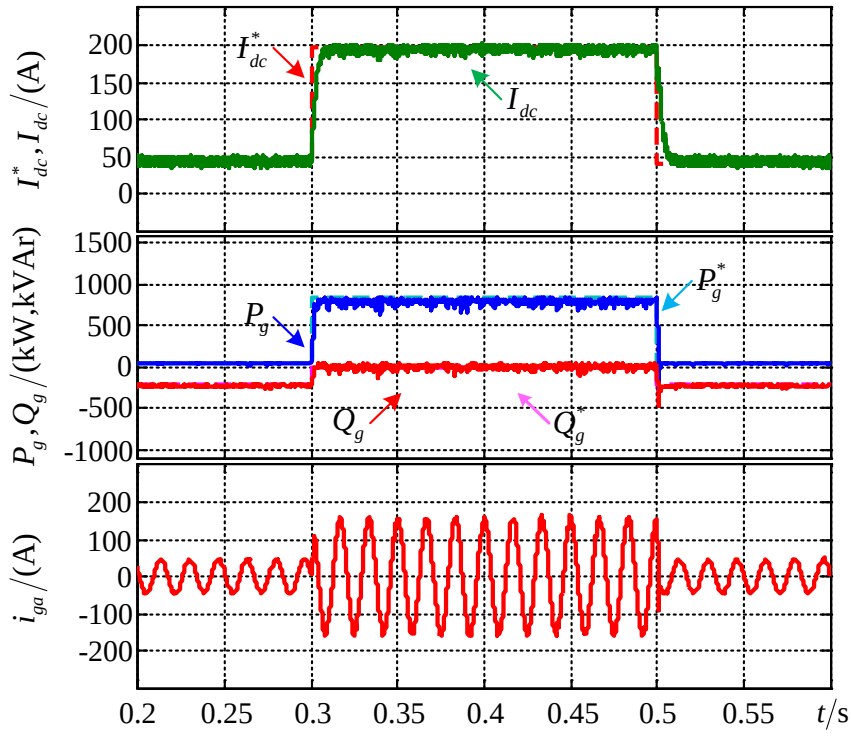
Fig. 3.13 shows the dynamic performance at the sudden change of the DC current. At time *t* of 0.4s, the DC current reference jumps from 0.2pu to 1pu, then it drops to 0.2pu again at 0.7s. Fig. 3.13 (a) shows the results of Scheme I. Since the DC current is directly regulated through its cost function, very fast DC current response is achieved. However, due to the severe line-side *LC* resonance, the ripples in the line active and reactive powers are too large to be accepted, which leads to the large fluctuation in the DC current in turn. As Fig. 3.13 (b) shows, the overshoot can be observed in the DC current of Scheme II. Due to the nonlinear nature of power converter, the overshoot during the DC current jumping is different from that when the DC current drops. Besides, although active damping function has been involved into Scheme II, significant power ripples, caused by *LC* resonance, and the limitation imposed by linear control and LPF used for calculating damping current, can still be observed, especially when the DC current drops. The results of MPPFC are shown in Fig. 3.13 (c), where the overshoot in the DC current is effectively mitigated, and the line active and reactive powers can closely track their respective references. Moreover, the presented results further verify the effectiveness of the line reactive power reference estimator. When the DC current is only 0.2pu, the leading current produced by the capacitor cannot be totally compensated. Therefore, the line reactive power reference at 0.2pu DC current is -120kVAr, indicating that the unity line PF is unachievable. When the DC current jumps to 1pu, the line reactive power reference quickly turns into 0, meaning that the line PF can be kept at unity.


I_{dc}^*
I_{dc}
I_{dc}^*, I_{dc}/(A)
200
150
100
50
0
P_g
Q_g
P_g, Q_g/(kW,kVAr)
2000
1000
0
-1000
-2000
i_{ga}/(A)
400
200
0
-200
-400
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
t/s

(a)


I_{dc}^*
I_{dc}
I_{dc}^*, I_{dc}/(A)
200
150
100
50
0
DC Current Overshoot
P_g
Q_g
P_g, Q_g/(kW,kVAr)
1500
1000
500
0
-500
-1000
i_{ga}/(A)
200
100
0
-100
-200
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
t/s

(b)



(c)

Fig. 3.13 Dynamic responses when DC current suddenly changes: (a) Scheme I, (b) Scheme II, and (c) MPPFC.

Fig. 3.14 verifies the performance of the active damping function involved into MPPFC during transients. At time *t* of 0.25s, the DC current drops from 1pu to 0.2pu. Without the active damping function, *LC* resonance is induced, and significant oscillation can be observed in the waveform of the phase A line current. With the active damping function introduced, *LC* resonance during transients is effectively mitigated. Moreover, the ideally sinusoidal line current references in MPPFC can compel the line currents to be close to sinusoidal waveform in steady states, the introduction of the active damping function further reduces the distortions of the line current and the capacitor voltage, which can also be validated from Fig. 3.14.

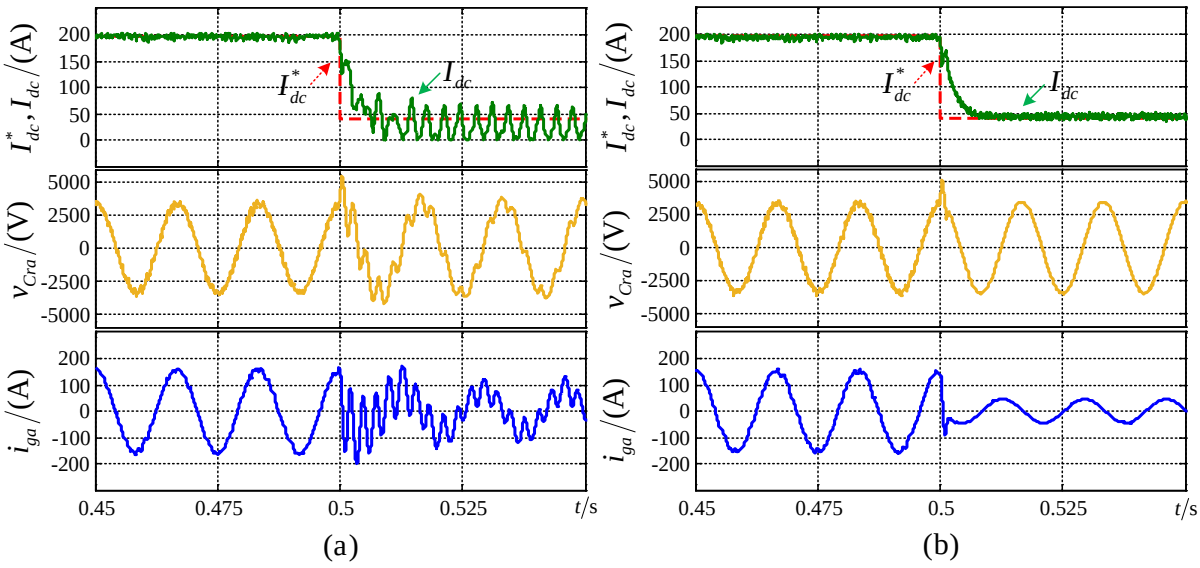


Fig. 3.14 Effectiveness of active damping function in MPPFC: (a) without active damping function and (b) with active damping function.

3.4 Experimental Validation

Experiments are conducted on a low power CSR prototype, where the power devices are IGBTs (IRG7PH42U-ND from International Rectifier) in series with diodes (DSEP60-12A-ND from IXYS) and the controller design is based on DSP (TMS320F28335) and FPGA (EP4CE10E22C8). The control algorithm part is realized in the DSP, and the FPGA takes responsibility of measurement and gating signal generation. Fig. 3.15 shows a photograph of the experimental setup. The parameters of the experimental setup have been listed in Table 3.1. For comparison, the experimental results of Scheme I and Scheme II are also provided. The switching frequency of Scheme II is still 1080Hz. The sampling intervals for Scheme I and MPPFC are still selected as 100μs. The average switching frequencies of Scheme I and MPPFC are still calculated based on (3.33).

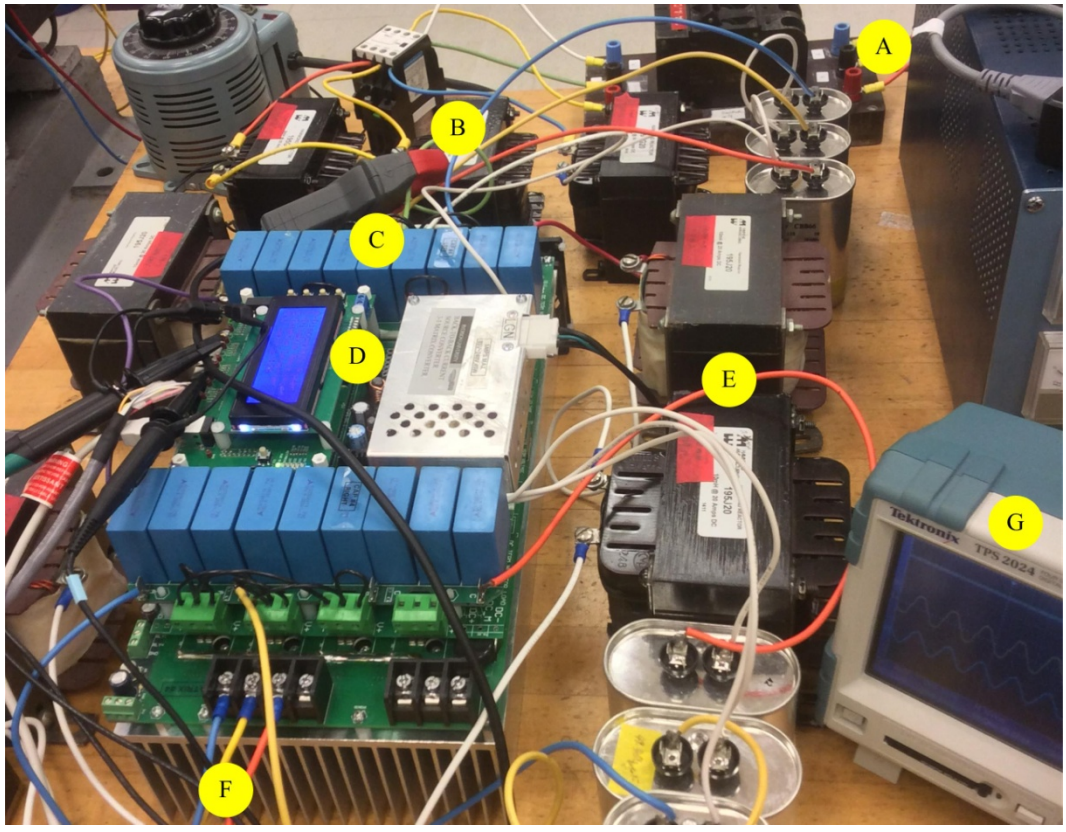
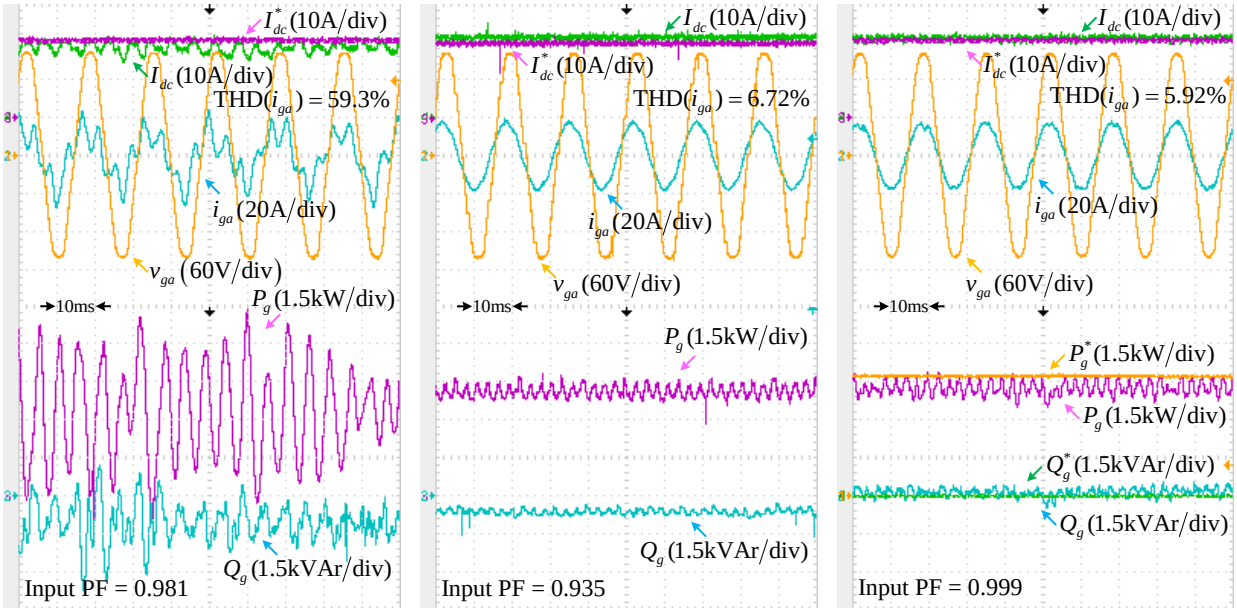


Fig. 3.15 Photograph of a low power CSR prototype: (A) three-phase power supply, (B) filter inductance, (C) capacitors, (D) CSR, (E) DC choke, (F) DC load resistor, and (G) oscilloscope.

3.4.1 Steady State Performance

Fig. 3.16 shows the steady state performance at 1pu DC current. The DC current and the phase A line current are directly measured with current probes. The DC current reference, the phase A power supply voltage, the line active and reactive powers are obtained through D/A interfaces in the prototype. In Fig. 3.16 (a), Scheme I leads to severe resonance in the phase A line current, due to the spread spectrum distribution of the input PWM currents. Large ripples can be found in the line active and reactive powers of Scheme I. The unity PF cannot be maintained with Scheme I, which is indicated by the negative average line reactive power. Fig. 3.16 (b) shows the results of Scheme II. The distortion in the phase A line current, of which the THD is 6.72%, is suppressed by the active damping function involved into Scheme II. However, since modulating index control is used to regulate the DC current in Scheme II, unity PF still cannot be achieved, which can be verified from its nonzero and negative line reactive power.

The results of MPPFC are shown in Fig. 3.16 (c). the line reactive power reference is zero, and unity PF is achieved by the line reactive power closely tracking its reference. With the predictive line current controller and the proposed active damping method, the waveform of the phase A line current is close to sinusoidal waveform with the smallest THD of 5.92%. Due to the smaller distortion in the line currents, the fluctuation in the DC current, and the ripples in the line active and reactive powers are also effectively constricted with MPPFC.



(a) (b) (c)

Fig. 3.16 Steady state performance at 1pu (19.6A) DC current: (a) Scheme I, (b) Scheme II, and (c) MPPFC.

Table 3.2 lists the quantitative comparison of three schemes at different DC currents, including THD and TDD of line current, measure line PF (only fundamental component of line current considered), MAPF, and measured average switching frequency. At all the listed operating conditions, the line PF of MPPFC is the highest among three schemes, and very close to MAPF, in which the discrepancy between MAPF and the line PF is mainly caused by the losses of the prototype. Relying on the reactive power term in the cost function, Scheme I can also improve the line PF. However, the line PF cannot be accurately regulated to align with MAPF values. Scheme II results in the lowest line PF, since it totally neglects line PF regulation. With the active damping function involved, both Scheme II and MPPFC can suppress possible *LC* resonance, and achieve relatively low THD of line current. Since there is no active damping

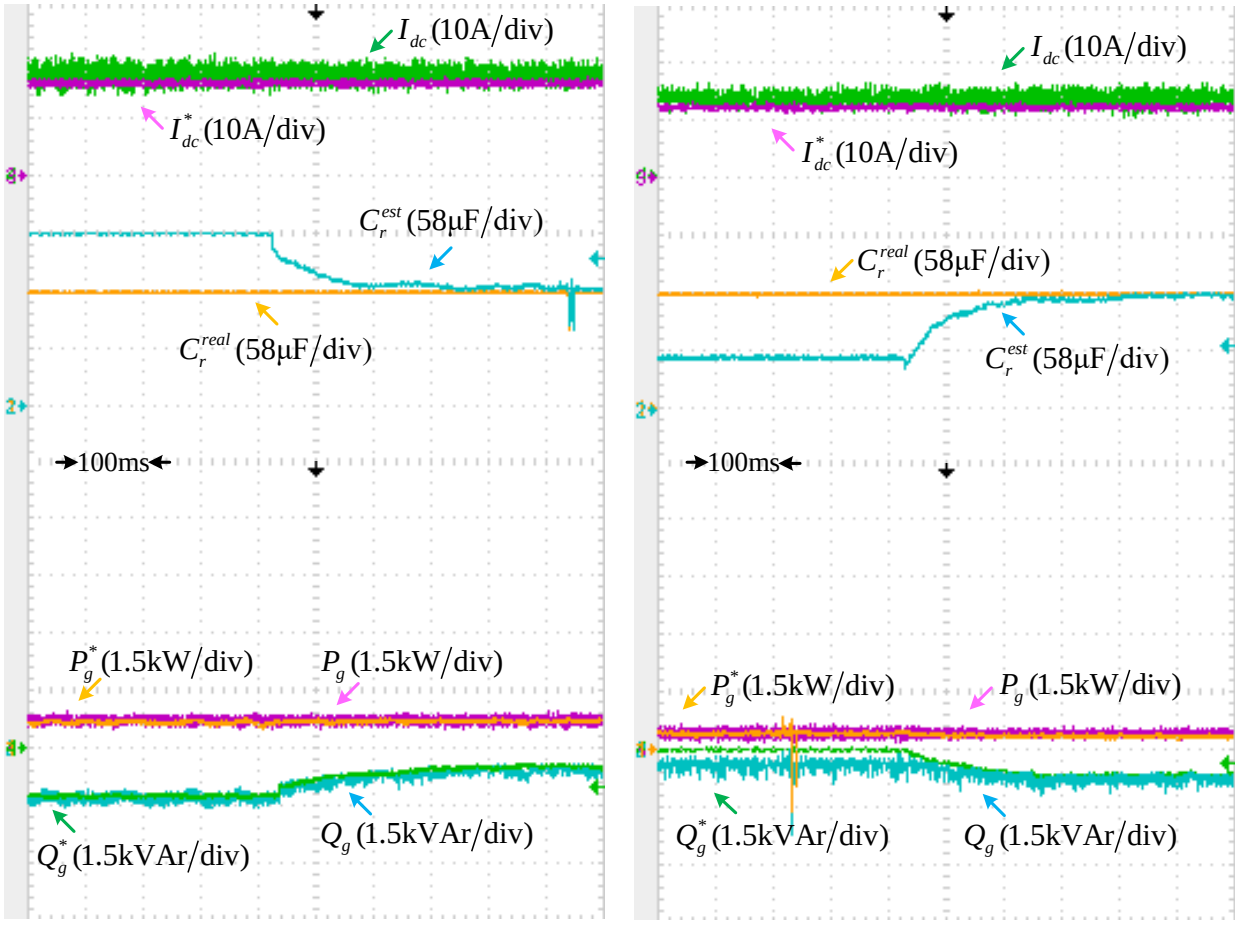
function in Scheme I, severe *LC* resonance appears in the line current of Scheme I at all operating conditions. Besides, in terms of TDD, MPPFC offers the lowest TDDs at all the operating conditions, and it also verifies that in contract to Scheme II, MPPFC possesses the potential to reduce the volumes of *LC* filter, especially the capacitor, and meets the grid code requirements at the same time, which also aligns with the results shown in Fig. 3.16. Moreover, the three schemes share very similar switching frequencies, which means that MPPFC can achieve line PF regulation and active damping function with not so high switching frequency.

Table 3.2 STEADY STATE PERFORMANCE OF THREE METHODS FOR COMPARISON

Conditions	Methods	THD of i_g (%)	TDD of i_g (%)	PF	MAPF	f_{sw} (Hz)
I_{dc} = 19.6A	Scheme I	59.3	42.3	0.981	1	1054
	Scheme II	6.72	6.06	0.935		1080
	MPPFC	5.92	5.22	0.999		1175
I_{dc} = 10A	Scheme I	193	72.7	0.681	1	1045
	Scheme II	9.96	4.48	0.474		1080
	MPPFC	13.6	3.20	0.998		1335
I_{dc} = 4A	Scheme I	30.4	8.43	0.119	0.175	1031
	Scheme II	11.96	4.90	0.071		1080
	MPPFC	11.2	2.64	0.172		1219

Fig. 3.17 verifies the effectiveness of the online capacitance estimation method. The real capacitance and the estimated value are measured from the D/A interfaces in the prototype. In Fig. 3.17 (a), the CSR operates at 0.4pu DC current, and the mismatched capacitance is 1.5 times its real value, that is 0.378pu (116μF). First, since the capacitance online estimation is not activated, the mismatched capacitance makes the line reactive power reference and the line PF equal to -1240VAr and 0.465, respectively. With the capacitance online estimation introduced, the estimated capacitance gradually approaches its real value. The line reactive power reference is modified to -458VAr, and the line PF increases to 0.831. In Fig. 3.17 (b), the CSR operates at 0.3pu DC current, and the mismatched capacitance is 0.5 times its real value. First, the capacitance online estimation is not activated, either. The mismatched capacitance makes the line reactive power reference equal to 0. However, it can be found that the line reactive power is not equal to 0, and unity PF is unachievable at 0.3pu DC current. With the online capacitance estimation introduced, the estimated capacitance increases, and finally aligns with its real value. The reactive power and the line PF are changed to -992VAr and 0.267, respectively. The

reactive power follows its reference, and the active power ripples become smaller after the introduction of the capacitance online estimation.



(a) (b)

Fig. 3.17 Online capacitance estimation: (a) 1.5 times mismatched capacitance at 0.4pu DC current and (b) 0.5 times mismatched capacitance at 0.3pu DC current.

3.4.2 Dynamic Performance

Fig. 3.18 shows the transient responses of three schemes. First, the DC current reference is 0.2pu (4A). Then, it steps to 1pu (19.6A). After 400ms, the DC current reference jumps back to 0.2pu. The dynamic response of Scheme I is shown in Fig. 3.18 (a). Since the DC current is directly regulated based on the DC-side prediction model of CSR, very fast DC current response can be obtained using Scheme I. Nevertheless, the ripples in the line active and reactive powers are inacceptable due to severe line current resonance, which is caused by the spread spectrum

distribution of the input PWM current by Scheme I. In Fig. 3.18 (b), the overshoots can be found in the DC current of Scheme II during transients, especially when the DC current drops. Due to the degraded active damping function during transients, significantly resonance can still be found in the line active and reactive powers during the sudden changes of the DC current. Fig. 3.18 (c) shows the results of MPPFC, in which the overshoot of the DC current is effectively mitigated. With the DC current changed from 0.2pu to 1pu, the line active and reactive powers are adjusted from 179W to 4665W and from -1005VAr to 0VAr, respectively, which validates the effectiveness of the reactive power reference estimator. The predictive line current controller realizes fast active and reactive power regulation, and better dynamic performance without resonance in the line active and reactive powers, which is achieved by the active damping function involved into MPPFC.

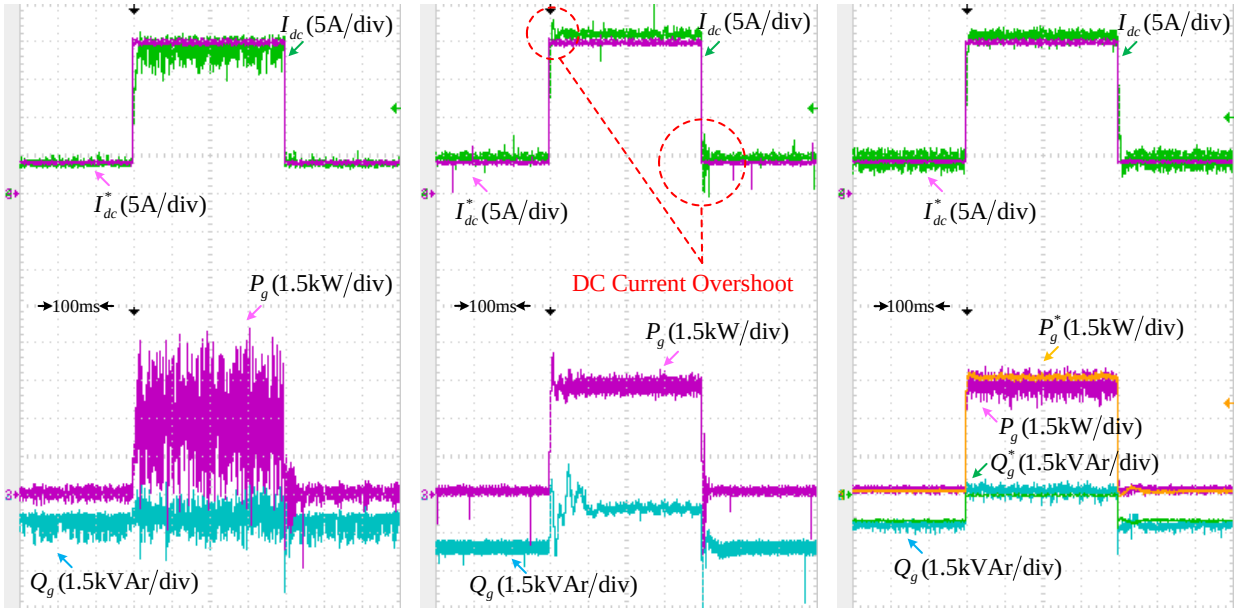
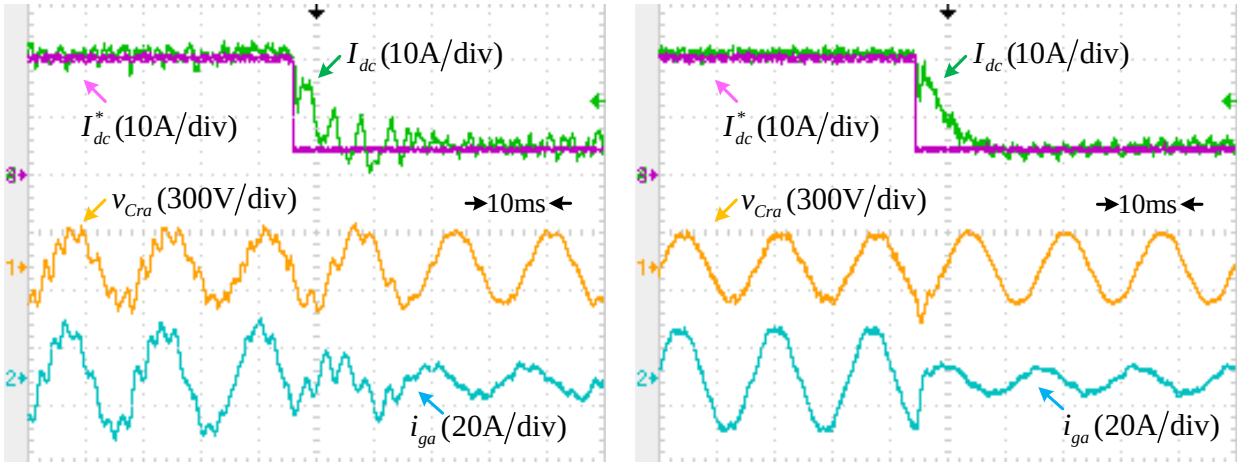


Fig. 3.18 Dynamic responses under sudden changes of DC current: (a) Scheme I, (b) Scheme II, and (c) MPPFC.

Fig. 3.19 verifies the effectiveness of the active damping function in MPPFC, when the DC current reference drops from 1pu to 0.2pu. Without the active damping function, significant resonance can be observed in the phase A capacitor voltage and the phase A line current during transients. The large fluctuation in the DC current also appears. In Fig. 3.19 (b), with the active damping function introduced, LC resonance is effectively mitigated, and the transitions of the

capacitor voltage and the line current become more flexible. Besides, the fluctuation in the DC current also decreases. Moreover, the distortion in the capacitor voltage and the line current becomes lower in comparison with that without the active damping function.



(a) (b)

Fig. 3.19 Effectiveness of active damping function in MPPFC during DC current drop: (a) without active damping function and (b) with active damping function.

3.5 Conclusions

MPPFC with active damping function has been presented in this chapter. The merits of the proposed scheme can be classified into three folds as

- First, in comparison with traditional linear control, MPPFC not only realizes input PF control, but also achieves better steady-state performance on meeting the grid code requirements, which implies that MPPFC has the potential to further reduce the volume of input *LC* filter;
- Second, in contrast to conventional MPC, MPPFC provides more accurate input PF control, and involves active damping function into it. Consequently, MPPFC suppresses the *LC* resonance, which is caused by harmonics in the input currents of CSR, and extends the application of MPC to high power CSR with lightly damped *LC* circuit;
- Last but not least, MPPFC offers better dynamic performance, especially smaller DC current overshoot and better active damping performance during transients when contrasted with the traditional linear counterpart.

4 Model Predictive Pulse Pattern Control With Low Switching Frequency for High Power Current-Source Converter

In Chapter 3, conventional model predictive control (MPC) approach has been imported into high power CSR to realize line power factor (PF) regulation with active damping function, and improved dynamic performance. However, based on the simulation and experimental results, the average switching frequencies of MPC are still relatively high, which are around 1kHz, even with switching frequency reduction term included in final cost functions, whereby some modifications on conventional MPC need to be applied in consideration of further reduction on switching frequency.

In this chapter, model predictive switching pattern control (MPSPC) with space vector based selective harmonic elimination (SHE) is proposed for single-bridge CSC, which achieves superb low-order harmonics elimination performance in steady state, and improved dynamic responses compared to that of traditional linear control with SHE modulation. The innovation of the proposed scheme can be classified as

- A representation of SHE-PWM pattern is designed, based on which MPSPC is realized;
- According to selected space vectors and calculated dwell time based on SHE-PWM pattern, load current at the end of each sampling interval can be predicted;
- The finally applied space vector will be optimally reselected if the error between load current reference vector and predicted load current vector is larger than a pre-defined threshold.

The advantages of MPSPC in comparison with traditional linear control and conventional MPCs with low switching frequency can be summarized as

- With a saw-tooth carrier based quasi-modulation process, there is no quantization error, as mentioned in [80], anymore, which totally maintains the performance on elimination of the selected low-order harmonics, and achieve better dynamic responses at the same time;

- There is no weighting factor selection issue which exists in [80, 81];
- MPSPC only uses a one-step prediction instead of multistep predictions in [81-83]. One-step prediction leads to a simpler structure, and reduces the complexity of the required calculation.

4.1 Selective Harmonic Elimination-Pulse Width Modulation for Current-Source Converter

Normally, there are two commonly used SHE-PWM patterns for a single-bridge CSC, namely six pulses per half cycle for output frequency around 60Hz, and eight pulses per half cycle for output frequency around 50Hz. With these two kinds of PWM patterns , the switching frequencies of switching devices in a CSC are just about 360Hz or 400Hz [5]. Fig. 4.1 shows typical SHE-PWM waveforms for a CSC. In Fig. 4.1 (a), there are six switching angles in the first $\pi/2$ period of the six-pulse waveform. Only three out of the six angles, β_1, β_2, and β_0, are independent, which can be used to eliminate two harmonics, and provide adjustable modulation index in the meanwhile. Similarly, the waveform with eight pulses per half cycle is depicted in Fig. 4.1 (b), in which there are only four independent angles, β_1, β_2, β_3, and β_0. With these four angles, three selected harmonics can be eliminated, and modulation index can be adjusted as well.

The PWM current waveform in Fig. 4.1 can be expressed in Fourier series as

$$i_w(\omega t) = \sum_{n=1}^{\infty} a_n \sin(n\omega t) \tag{4.1}$$

where

$$a_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} i_w(\omega t)\sin(n\omega t)d(n\omega t) \tag{4.2}$$

Here six-pulse waveform is used as an example. In order to eliminate two dominant low-order harmonics such as the 5th and 7th, and adjust modulation index, the following system of equations is defined as

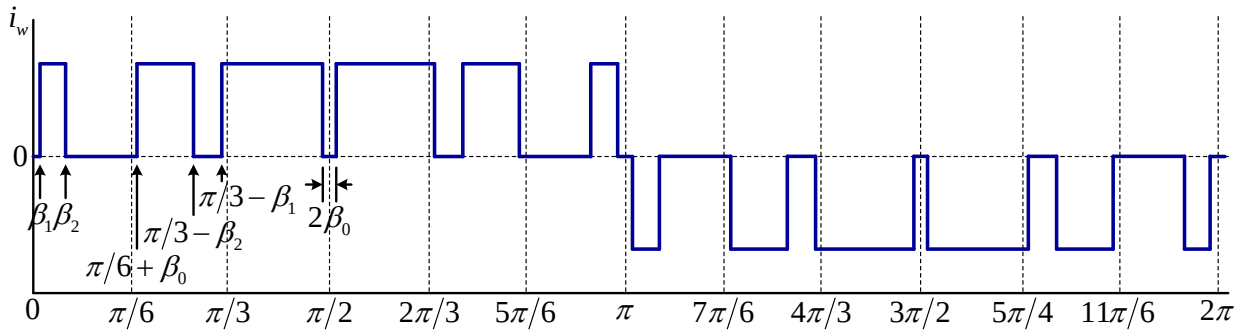
$$\begin{cases} F_1 = \cos(5\beta_1) - \cos(5\beta_2) + \cos\left(5(\pi/6+\beta_0)\right) - \cos\left(5(\pi/3-\beta_2)\right) \\ + \cos\left(5(\pi/3-\beta_1)\right) - \cos\left(5(\pi/2-\beta_0)\right) = 0 \\ F_2 = \cos(11\beta_1) - \cos(11\beta_2) + \cos\left(11(\pi/6+\beta_0)\right) - \cos\left(11(\pi/3-\beta_2)\right) \\ + \cos\left(11(\pi/3-\beta_1)\right) - \cos\left(11(\pi/2-\beta_0)\right) = 0 \\ F_3 = (4/\pi)[\cos\beta_1 - \cos\beta_2 + \cos(\pi/6+\beta_0) \\ - \cos(\pi/3-\beta_2) + \cos(\pi/3-\beta_1) - \cos(\pi/2-\beta_0)] - m_a = 0 \end{cases} \tag{4.3}$$

where m_a is the modulation index, which is given by

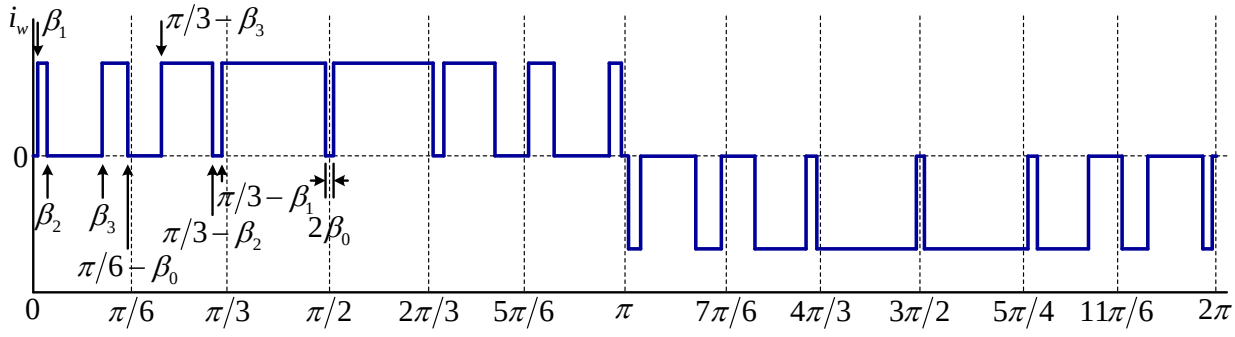
$$m_a = \frac{I_{w(1)}}{I_{dc}} \tag{4.4}$$

in which $I_{w(1)}$ is the magnitude of the fundamental-frequency component of PWM current, and I_{dc} is the value of DC current.

Similarly, for an eight-pulse waveform with four independent angles, four equations can also be established to eliminate three dominant harmonics, such as the 5th, 7th, and 11th, and adjust modulation index.



(a)



(b)

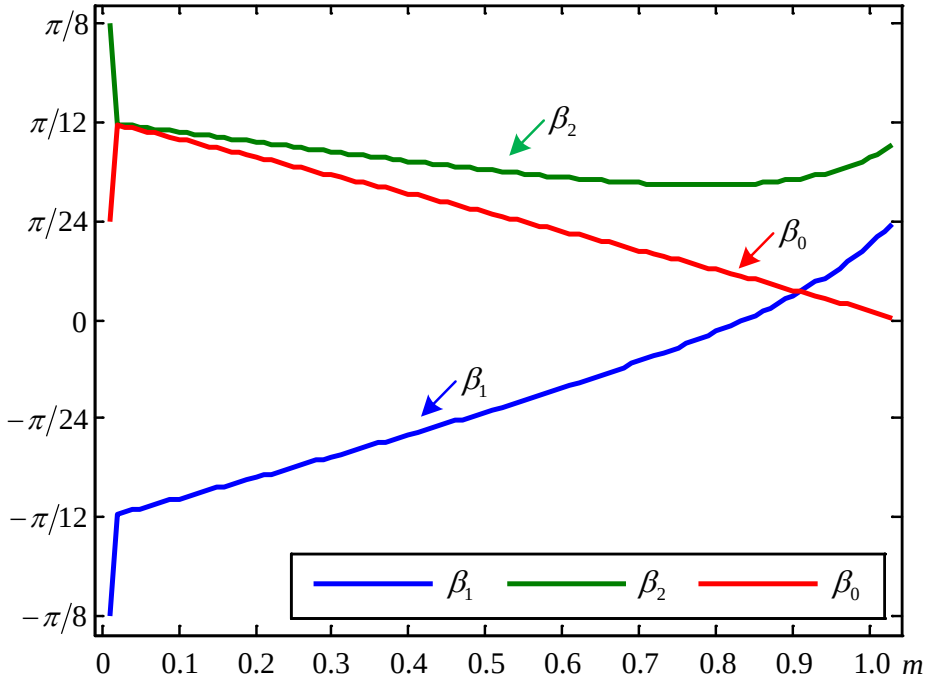
Fig. 4.1 SHE-PWM waveforms: (a) six pulses per half-cycle and (b) eight pulses per half-cycle.

The nonlinear and transcendental equations of (4.3) can be solved by a number of numerical methods [84], one of which is the Newton-Raphson iteration algorithm. At various modulation indexes, independent angles for six- and eight-pulse waveforms have been calculated and the solutions are shown in Fig. 4.2.

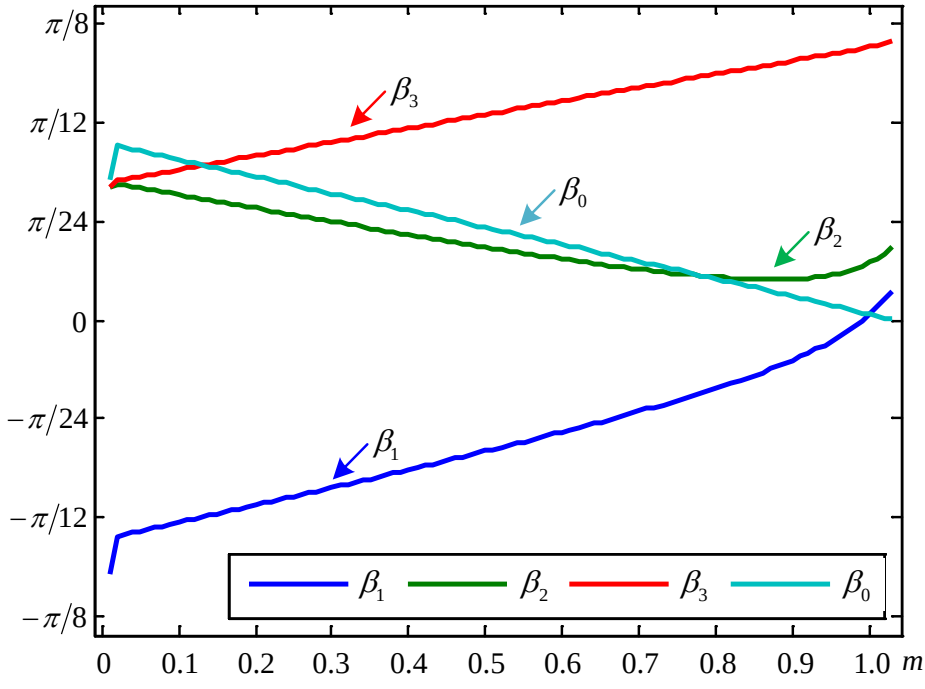
In Fig. 4.2, no matter for six-pulse or eight-pulse waveform, the maximum modulation index is around 1.02, at which β_0 becomes zero, the notch locating in the center of half-cycle PWM waveforms disappears. For a set of β_1, β_2, and β_0, the gate signals for the switching devices in a CSC can be arranged. As Fig. 4.2 (a) shows, for six-pulse waveform, when m_a is lower than 0.83, β_1 is smaller than 0, which means that there are two cases of gate signal arrangements for six-pulse waveform. In Fig. 4.3, g_1 and g_4 are the gate signals for S_1 and S_4 in a CSC. g_1 is composed of six pulses, of which one is the bypass pulse, defined between $3\pi/2-\beta_0$ and $3\pi/2+\beta_0$. If β_1 is larger than 0, there are only two bypass intervals, which are caused by

bypass pulses, as Fig. 4.3 (a) shows. If β_1 is smaller than 0, there are four bypass intervals per cycle. The bypass intervals, BP2 and BP4, are created by bypass pulses while the other two, BP1 and BP3, are due to the overlapping of the gate signals.

Similarly, as Fig. 4.3 (b) shows, for eight-pulse waveform, when m_a is lower than 0.98, β_1 is smaller than 0. When m_a is lower than 0.98, β_1 is smaller than 0. If m_a is between 0.89 and 0.98, $|\beta_1|$ is smaller than β_2. If m_a is between 0.26 and 0.89, $|\beta_1|$ is larger than β_2, but smaller than β_3. With m_a smaller than 0.26, $|\beta_1|$ is finally larger than β_3. These four situations lead to four cases of gate signal arrangements for eight-pulse waveform. As Fig. 4.4 shows, g_1 is composed of eight pulses. Similarly, there is one bypass pulse, defined between $3\pi/2-\beta_0$ and $3\pi/2+\beta_0$. If β_1 is larger than 0, there are only two bypass intervals, which are generated by bypass pulses, as Fig. 4.4 (a) shows. If β_1 is smaller than 0, and $|\beta_1|$ is larger than β_3, there are eight bypass intervals per cycle. The bypass intervals, BP3 and BP7, are created by bypass pulses while the other six are due to the overlapping of the gate signals, as Fig. 4.4 (d) shows.

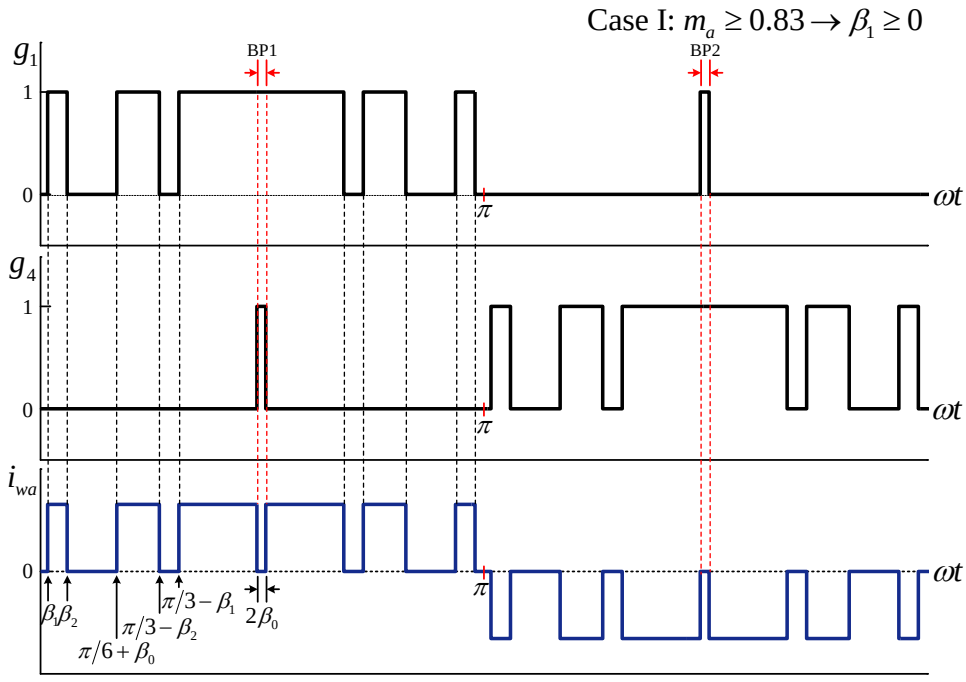


(a)

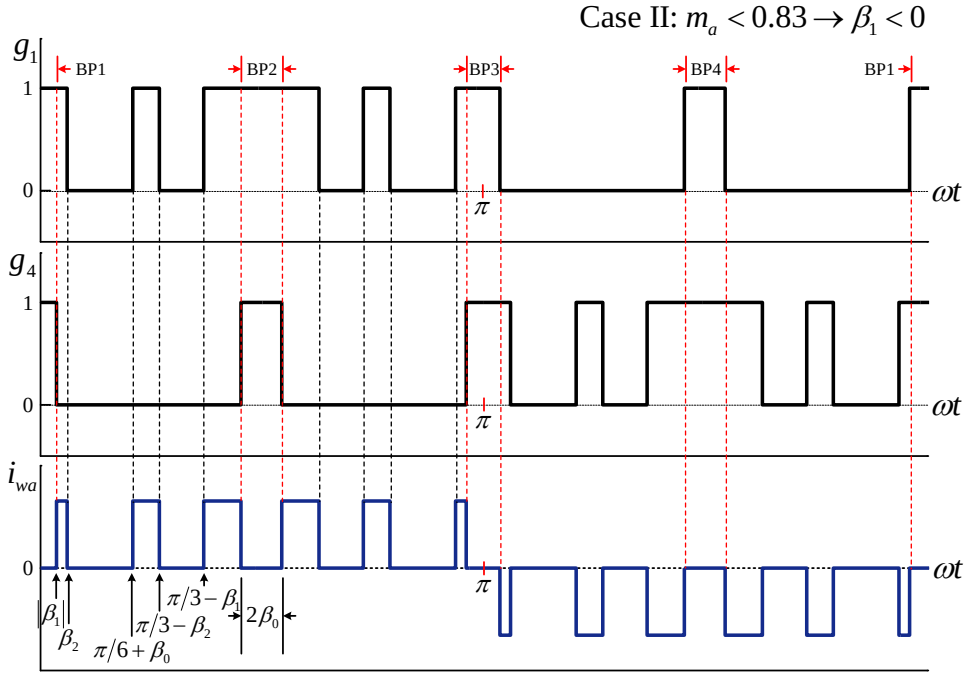


(b)

Fig. 4.2 Solutions to independent angles for SHE (a) six pulse per half cycle and (b) eight pulse per half cycle.



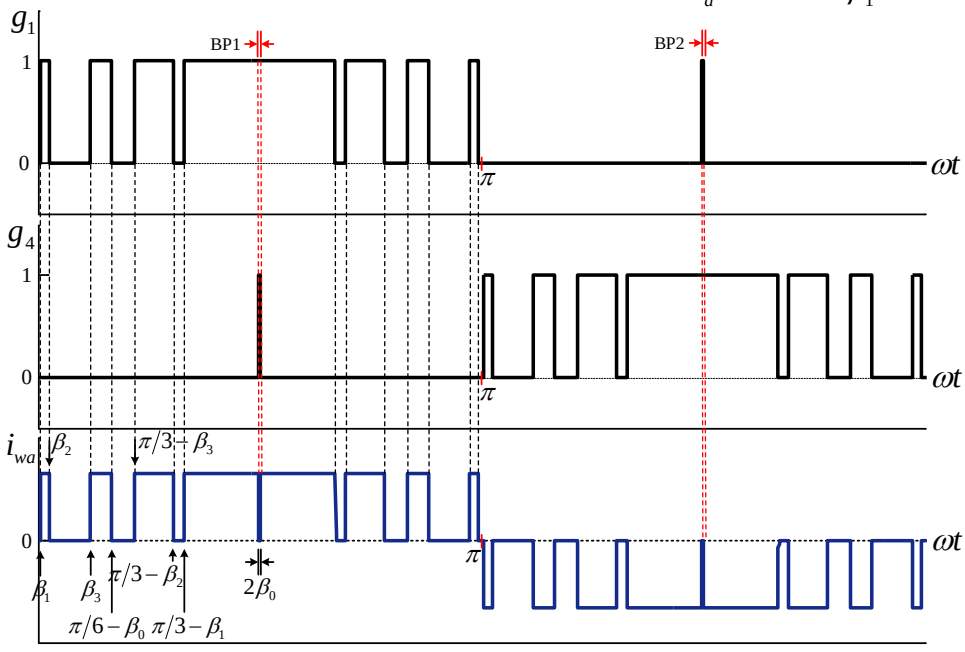
(a)



(b)

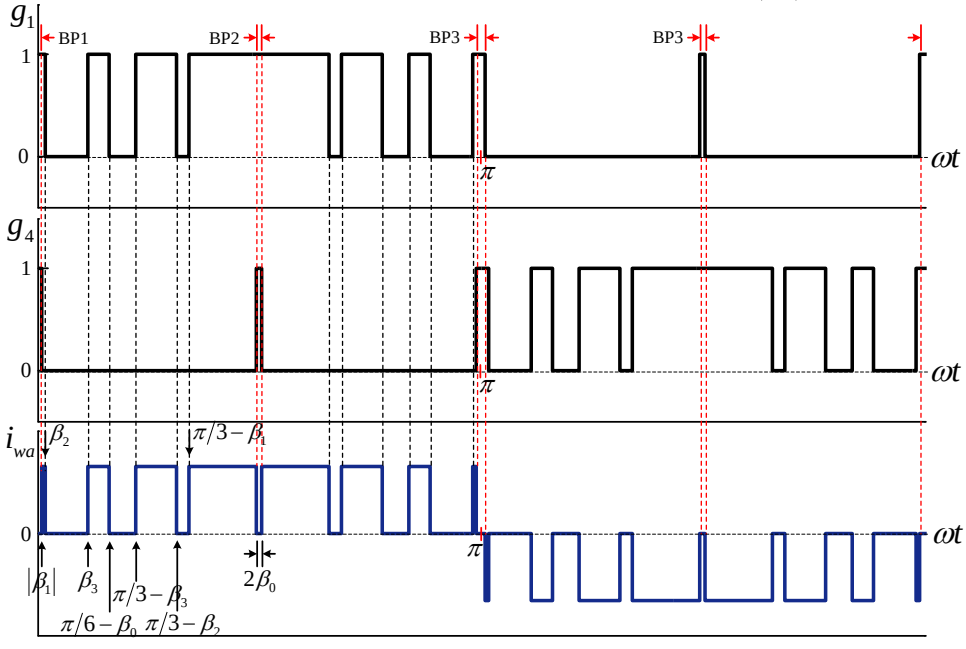
Fig. 4.3 Phase A gate signals for six-pulse waveform: (a) Case I and (b) Case II.

Case I: $m_a \geq 0.98 \rightarrow \beta_1 \geq 0$

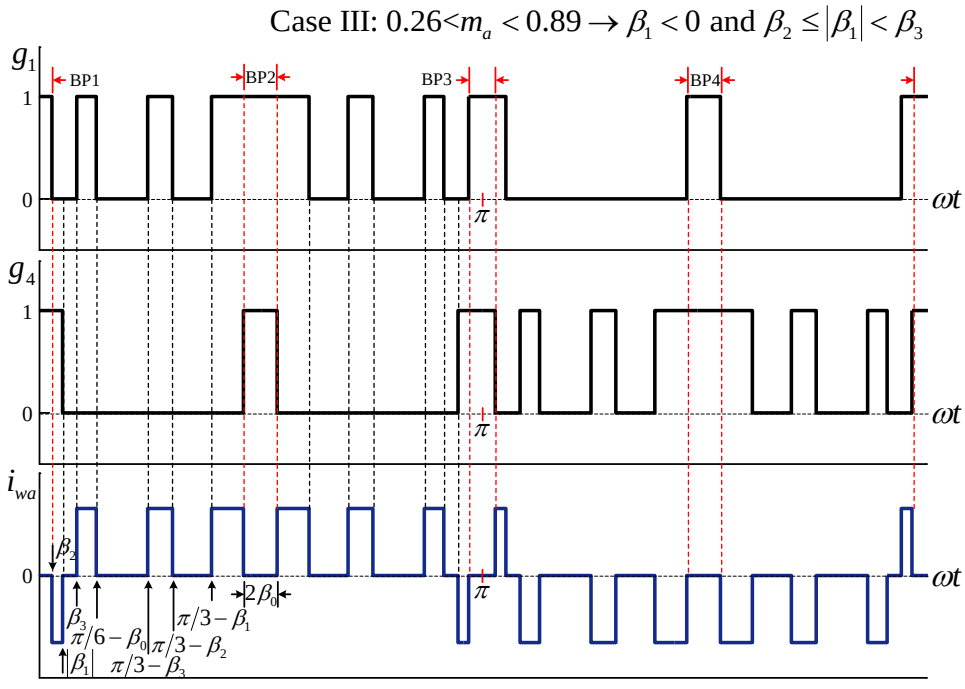


(a)

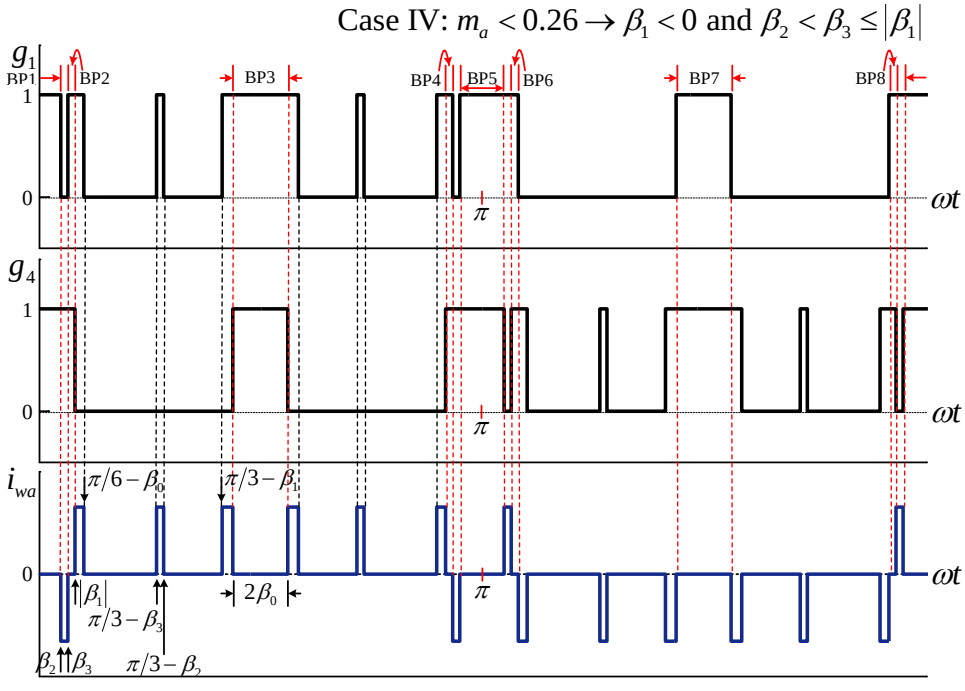
Case II: $0.89<m_a<0.98 \rightarrow \beta_1<0$ and $|\beta_1|<\beta_2<\beta_3$



(b)



(c)



(d)

Fig. 4.4 Phase A gating signals for eight-pulse waveform: (a) Case I, (b) Case II, (c) Case III, and (d) Case IV.

4.2 Space Vector Based Selective Harmonic Elimination

In traditional modulator, the switching angles for SHE are directly used to generate PWM waveform. However, a fixed sampling frequency, f_s, is normally used in MPC. The sampling process introduces a quantization error on the pre-calculated switching angles, as discussed in [80]. As a consequence, the elimination of undesired low-order harmonics may be compromised since the quantized angles may differ from the pre-calculated ones. In order to ensure an acceptable low-order harmonic elimination performance, a high sampling frequency needs to be used, which increases the requirement on calculating capability of hardware platform.

As the foundation of MPSPC, a space vector based SHE with a fixed sampling frequency, but without quantization error is proposed here. The space vector representation of SHE waveform will be introduced first, then the realization of space vector based SHE will be presented in details.

4.2.1.1 Space Vector Representation of SHE

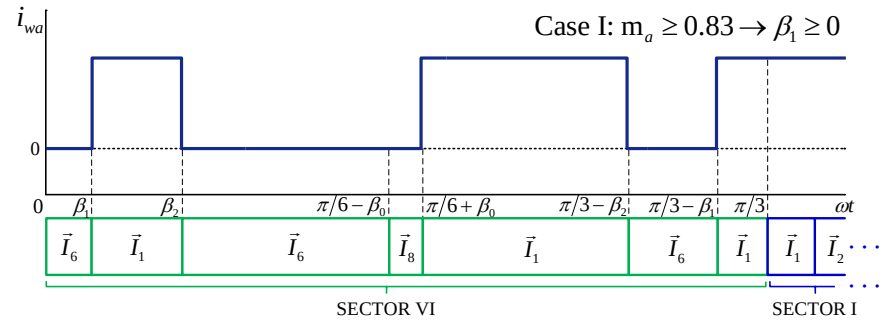
At any instant of time, SHE waveforms for a CSC satisfy the switching constraints, which means that one corresponding space vector is applied. The space vector diagram can be referred to Fig. 2.2. Hence, based on the switching signals for the six switching devices in a CSC, SHE waveforms can be represented in space vector form. Here the SHE waveforms during the time interval between 0 and $\pi/3$ are selected as an example. For six-pulse waveforms, shown in Fig. 4.3, since there are two cases of gate signal arrangements based on modulation index value, the space vector sequence during the selected interval also has two kinds of patterns, as Fig. 4.5 shows. Similarly, as Fig. 4.4 shows, since there are four gate signal arrangements for eight-pulse waveforms based on different modulation indexes, the four kinds of space vector sequences are shown in Fig. 4.6.

It can be found from Fig. 4.5 and Fig. 4.6 that with β_1 decreasing from positive value to negative value, more zero-state vectors appear in the space vector sequence due to the overlapping operation. Besides, the dwell time for each space vector can be calculated based on the difference between the start and the end terminals of one space vector, which changes with respect to different calculated optimal angles. Another thing is that during the selected duration,

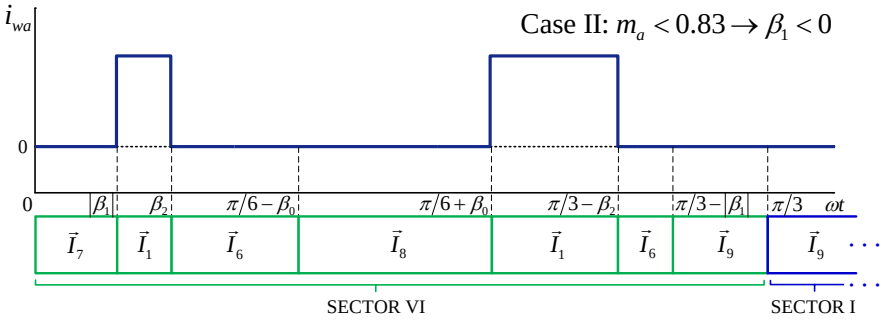
$\vec{I}_6$ and $\vec{I}_1$ mainly appear in the above sequences as active-state vectors, which indicates that the reference vector for generating SHE waveform locates in Sector VI of the space vector domain in Fig. 2.2. Since the sequences in Sector VI has been analyzed, the principle and regulation can be extended to other sectors. The dwell time for each space vector in the same case can also be used for other sectors. All the sequences in different sectors for six-pulse and eight-pulse waveforms have been listed in Table 4.1 and Table 4.2, respectively.

Table 4.1 SPACE VECTOR SEQUENCES FOR SIX-PULSE WAVEFORM

Sector No.	Case I	Case II
Sector I	$\vec{I}_1 \to \vec{I}_2 \to \vec{I}_1 \to \vec{I}_7 \to \vec{I}_2 \to \vec{I}_1 \to \vec{I}_2$	$\vec{I}_9 \to \vec{I}_2 \to \vec{I}_1 \to \vec{I}_7 \to \vec{I}_2 \to \vec{I}_1 \to \vec{I}_8$
Sector II	$\vec{I}_2 \to \vec{I}_3 \to \vec{I}_2 \to \vec{I}_9 \to \vec{I}_3 \to \vec{I}_2 \to \vec{I}_3$	$\vec{I}_8 \to \vec{I}_3 \to \vec{I}_2 \to \vec{I}_9 \to \vec{I}_3 \to \vec{I}_2 \to \vec{I}_7$
Sector III	$\vec{I}_3 \to \vec{I}_4 \to \vec{I}_3 \to \vec{I}_8 \to \vec{I}_4 \to \vec{I}_3 \to \vec{I}_4$	$\vec{I}_7 \to \vec{I}_4 \to \vec{I}_3 \to \vec{I}_8 \to \vec{I}_4 \to \vec{I}_3 \to \vec{I}_9$
Sector IV	$\vec{I}_4 \to \vec{I}_5 \to \vec{I}_4 \to \vec{I}_7 \to \vec{I}_5 \to \vec{I}_4 \to \vec{I}_5$	$\vec{I}_9 \to \vec{I}_5 \to \vec{I}_4 \to \vec{I}_7 \to \vec{I}_5 \to \vec{I}_4 \to \vec{I}_8$
Sector V	$\vec{I}_5 \to \vec{I}_6 \to \vec{I}_5 \to \vec{I}_9 \to \vec{I}_6 \to \vec{I}_5 \to \vec{I}_6$	$\vec{I}_8 \to \vec{I}_6 \to \vec{I}_5 \to \vec{I}_9 \to \vec{I}_6 \to \vec{I}_5 \to \vec{I}_7$
Sector VI	$\vec{I}_6 \to \vec{I}_1 \to \vec{I}_6 \to \vec{I}_8 \to \vec{I}_1 \to \vec{I}_6 \to \vec{I}_1$	$\vec{I}_7 \to \vec{I}_1 \to \vec{I}_6 \to \vec{I}_8 \to \vec{I}_1 \to \vec{I}_6 \to \vec{I}_9$

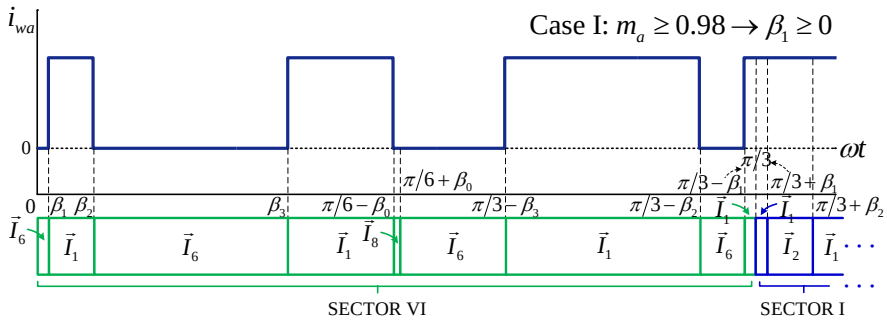


(a)

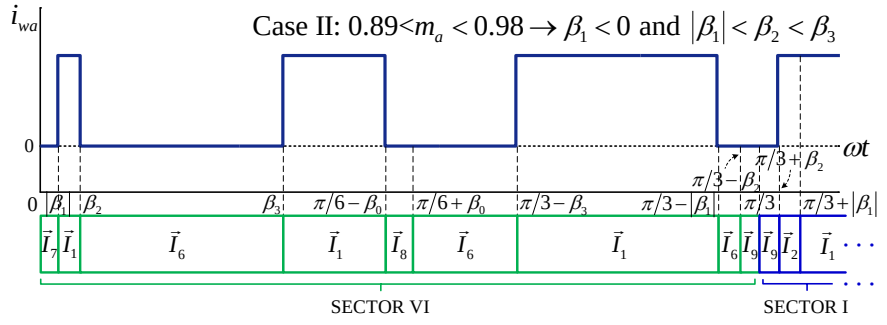


(b)

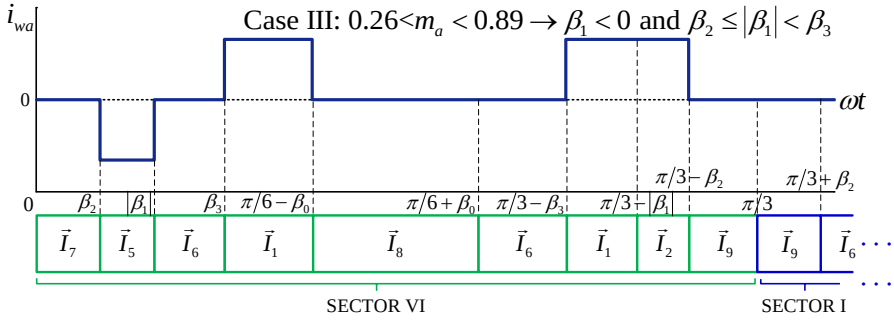
Fig. 4.5 Space vector sequence for six-pulse waveform: (a) case I and (b) case II.



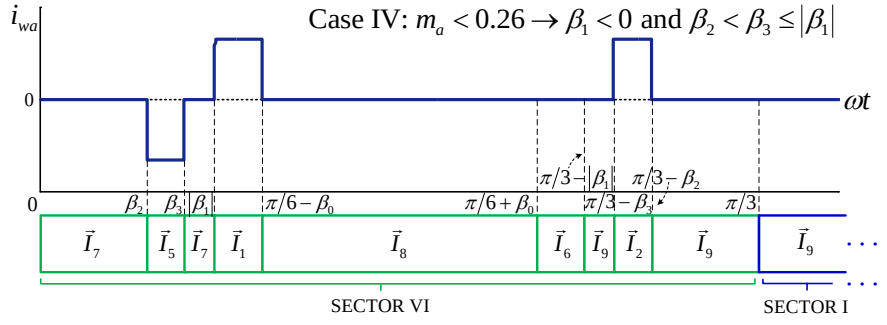
(a)



(b)



(c)



(d)

Fig. 4.6 Space vector sequence for eight-pulse waveform: (a) case I, (b) case II, (c) case III, and (d) case IV.

Table 4.2 SPACE VECTOR SEQUENCES FOR EIGHT-PULSE WAVEFORM

Sector No.	Case I	Case II	Case III	Case IV
	$\vec{I}_1 \rightarrow \vec{I}_2 \rightarrow \vec{I}_1$	$\vec{I}_9 \rightarrow \vec{I}_2 \rightarrow \vec{I}_1$	$\vec{I}_9 \rightarrow \vec{I}_6 \rightarrow \vec{I}_1$	$\vec{I}_9 \rightarrow \vec{I}_6 \rightarrow \vec{I}_9$
Sector I	$\rightarrow \vec{I}_2 \rightarrow \vec{I}_7 \rightarrow \vec{I}_1$	$\rightarrow \vec{I}_2 \rightarrow \vec{I}_7 \rightarrow \vec{I}_1$	$\rightarrow \vec{I}_2 \rightarrow \vec{I}_7 \rightarrow \vec{I}_1$	$\rightarrow \vec{I}_2 \rightarrow \vec{I}_7 \rightarrow \vec{I}_1$
	$\rightarrow \vec{I}_2 \rightarrow \vec{I}_1 \rightarrow \vec{I}_2$	$\rightarrow \vec{I}_2 \rightarrow \vec{I}_1 \rightarrow \vec{I}_8$	$\rightarrow \vec{I}_2 \rightarrow \vec{I}_3 \rightarrow \vec{I}_8$	$\rightarrow \vec{I}_8 \rightarrow \vec{I}_3 \rightarrow \vec{I}_8$
	$\vec{I}_2 \rightarrow \vec{I}_3 \rightarrow \vec{I}_2$	$\vec{I}_8 \rightarrow \vec{I}_3 \rightarrow \vec{I}_2$	$\vec{I}_8 \rightarrow \vec{I}_1 \rightarrow \vec{I}_2$	$\vec{I}_8 \rightarrow \vec{I}_1 \rightarrow \vec{I}_8$
Sector II	$\rightarrow \vec{I}_3 \rightarrow \vec{I}_9 \rightarrow \vec{I}_2$	$\rightarrow \vec{I}_3 \rightarrow \vec{I}_9 \rightarrow \vec{I}_2$	$\rightarrow \vec{I}_3 \rightarrow \vec{I}_9 \rightarrow \vec{I}_2$	$\rightarrow \vec{I}_3 \rightarrow \vec{I}_9 \rightarrow \vec{I}_2$
	$\rightarrow \vec{I}_3 \rightarrow \vec{I}_2 \rightarrow \vec{I}_3$	$\rightarrow \vec{I}_3 \rightarrow \vec{I}_2 \rightarrow \vec{I}_7$	$\rightarrow \vec{I}_3 \rightarrow \vec{I}_4 \rightarrow \vec{I}_7$	$\rightarrow \vec{I}_2 \rightarrow \vec{I}_4 \rightarrow \vec{I}_7$
	$\vec{I}_3 \rightarrow \vec{I}_4 \rightarrow \vec{I}_3$	$\vec{I}_3 \rightarrow \vec{I}_4 \rightarrow \vec{I}_3$	$\vec{I}_7 \rightarrow \vec{I}_2 \rightarrow \vec{I}_3$	$\vec{I}_7 \rightarrow \vec{I}_2 \rightarrow \vec{I}_7$
Sector III	$\rightarrow \vec{I}_4 \rightarrow \vec{I}_8 \rightarrow \vec{I}_3$	$\rightarrow \vec{I}_4 \rightarrow \vec{I}_8 \rightarrow \vec{I}_3$	$\rightarrow \vec{I}_4 \rightarrow \vec{I}_8 \rightarrow \vec{I}_3$	$\rightarrow \vec{I}_4 \rightarrow \vec{I}_8 \rightarrow \vec{I}_3$
	$\rightarrow \vec{I}_4 \rightarrow \vec{I}_3 \rightarrow \vec{I}_4$	$\rightarrow \vec{I}_4 \rightarrow \vec{I}_3 \rightarrow \vec{I}_4$	$\rightarrow \vec{I}_4 \rightarrow \vec{I}_5 \rightarrow \vec{I}_9$	$\rightarrow \vec{I}_9 \rightarrow \vec{I}_5 \rightarrow \vec{I}_9$
	$\vec{I}_4 \rightarrow \vec{I}_5 \rightarrow \vec{I}_4$	$\vec{I}_9 \rightarrow \vec{I}_5 \rightarrow \vec{I}_4$	$\vec{I}_9 \rightarrow \vec{I}_3 \rightarrow \vec{I}_4$	$\vec{I}_9 \rightarrow \vec{I}_3 \rightarrow \vec{I}_9$
Sector IV	$\rightarrow \vec{I}_5 \rightarrow \vec{I}_7 \rightarrow \vec{I}_4$	$\rightarrow \vec{I}_5 \rightarrow \vec{I}_7 \rightarrow \vec{I}_4$	$\rightarrow \vec{I}_5 \rightarrow \vec{I}_7 \rightarrow \vec{I}_4$	$\rightarrow \vec{I}_5 \rightarrow \vec{I}_7 \rightarrow \vec{I}_4$
	$\rightarrow \vec{I}_5 \rightarrow \vec{I}_4 \rightarrow \vec{I}_5$	$\rightarrow \vec{I}_5 \rightarrow \vec{I}_4 \rightarrow \vec{I}_8$	$\rightarrow \vec{I}_5 \rightarrow \vec{I}_6 \rightarrow \vec{I}_8$	$\rightarrow \vec{I}_8 \rightarrow \vec{I}_6 \rightarrow \vec{I}_8$
	$\vec{I}_5 \rightarrow \vec{I}_6 \rightarrow \vec{I}_5$	$\vec{I}_8 \rightarrow \vec{I}_6 \rightarrow \vec{I}_5$	$\vec{I}_8 \rightarrow \vec{I}_4 \rightarrow \vec{I}_5$	$\vec{I}_8 \rightarrow \vec{I}_4 \rightarrow \vec{I}_8$
Sector IV	$\rightarrow \vec{I}_6 \rightarrow \vec{I}_9 \rightarrow \vec{I}_5$	$\rightarrow \vec{I}_6 \rightarrow \vec{I}_9 \rightarrow \vec{I}_5$	$\rightarrow \vec{I}_6 \rightarrow \vec{I}_9 \rightarrow \vec{I}_5$	$\rightarrow \vec{I}_6 \rightarrow \vec{I}_9 \rightarrow \vec{I}_5$
	$\rightarrow \vec{I}_6 \rightarrow \vec{I}_5 \rightarrow \vec{I}_6$	$\rightarrow \vec{I}_6 \rightarrow \vec{I}_5 \rightarrow \vec{I}_7$	$\rightarrow \vec{I}_6 \rightarrow \vec{I}_1 \rightarrow \vec{I}_7$	$\rightarrow \vec{I}_7 \rightarrow \vec{I}_1 \rightarrow \vec{I}_7$
	$\vec{I}_6 \rightarrow \vec{I}_1 \rightarrow \vec{I}_6$	$\vec{I}_7 \rightarrow \vec{I}_1 \rightarrow \vec{I}_6$	$\vec{I}_7 \rightarrow \vec{I}_5 \rightarrow \vec{I}_6$	$\vec{I}_7 \rightarrow \vec{I}_5 \rightarrow \vec{I}_7$
Sector VI	$\rightarrow \vec{I}_1 \rightarrow \vec{I}_8 \rightarrow \vec{I}_6$	$\rightarrow \vec{I}_1 \rightarrow \vec{I}_8 \rightarrow \vec{I}_6$	$\rightarrow \vec{I}_1 \rightarrow \vec{I}_8 \rightarrow \vec{I}_6$	$\rightarrow \vec{I}_1 \rightarrow \vec{I}_8 \rightarrow \vec{I}_6$
	$\rightarrow \vec{I}_1 \rightarrow \vec{I}_6 \rightarrow \vec{I}_1$	$\rightarrow \vec{I}_1 \rightarrow \vec{I}_6 \rightarrow \vec{I}_9$	$\rightarrow \vec{I}_1 \rightarrow \vec{I}_2 \rightarrow \vec{I}_9$	$\rightarrow \vec{I}_9 \rightarrow \vec{I}_2 \rightarrow \vec{I}_9$

4.2.2 Realization of Space Vector Based SHE

In most applications, load currents are directly regulated by power converters. For a CSC, its output PWM current reference can be calculated based on the summation of load current reference and low frequency components in capacitor current. The reference vector for generating output PWM currents can be given by

$$\vec{i}_w^* = I_w^* e^{j\theta_w^*} \tag{4.5}$$

where I_w^* is the magnitude of the reference vector, and θ_w^* is the angle of the reference vector in space vector domain. Based on (4.4), the modulation index can be obtained. Based on the angle, θ_w^*, the sector number, in which the reference vector for output PWM current locates, can be

determined. Then, the angle of the reference vector, with respect to its corresponding sector, can be obtained. According to the modulation index, the optimal angles can be selected from the pre-calculated look-up table, then the space vector sequence, corresponding to the calculated modulation index and a specified sector, can be decided. Finally, based on the angle of the reference vector, with respect to the corresponding vector, the location of the start point of one sampling interval can be obtained in one sector sequence. Since a fixed sampling frequency is used here, the sampling interval is a constant value. Normally, for MPC, the sampling frequency is selected as high as 20kHz, even 50kHz in some cases. Here, taking into consideration of the calculation capability of most state-to-art DSPs, 10kHz sampling frequency is selected. With a constant sampling frequency and the information on the start point of one sampling interval, the location of the end point of the same sampling interval can also be calculated.

Here the space vector sequence in Case I of six-pulse waveforms is selected as an example. During the sampling interval, there are possibly three scenarios of space vector combinations, as Fig. 4.7 shows. In Fig. 4.7 (a), only one vector is applied during the whole sampling interval. As Fig. 4.7 (b) shows, if the sampling interval locates between two vectors, the applied vector needs to be changed once during the interval. There is another situation in which the applied vector, during one sampling interval, needs to be changed twice, as Fig. 4.7 (c) depicts. Since β_1 and β_0 can be very close to 0 at some specified modulation index, one sampling interval is possibly divided into three parts belonging to three space vectors. In fact, there are only two start point locations of sampling interval, which possibly leads to this situation. When the sampling interval locates around the half center of the PWM waveform, there may be three vectors contained inside the sampling interval, as the red rectangular shown in Fig. 4.7 (c). When the start point of the sampling interval locates near the end of the sector, the end point of the sampling interval may locate in the next sector. With a tiny value of β_1, the sampling interval also possibly contains three space vectors, as the red dotted rectangular shows in Fig. 4.7 (c). For eight-pulse SHE waveform, the three situations also exist, when the values of β_1 and β_0 are very small. Moreover, with higher sampling frequency or smaller sampling interval, the above discussion still holds true.

Based on a specified space vector sequence and the locations of the start point and end point of one sampling interval, the space vectors and their respective dwell time during one sampling interval can be determined. With a saw-tooth carrier, of which the frequency is equal to the sampling frequency, the selected space vectors can be modulated with their corresponding dwell time during one sampling interval, as Fig. 4.7 shows. Since in one sampling interval, space vector can maximum be changed twice, the quasi-modulation method can be easily realized on DSP or FPGA platform. Moreover, with space vector based SHE, there is no quantization error introduced by a fixed sampling frequency, since there is no compromise on practically applied switching angles in contrast to pre-calculated ones.

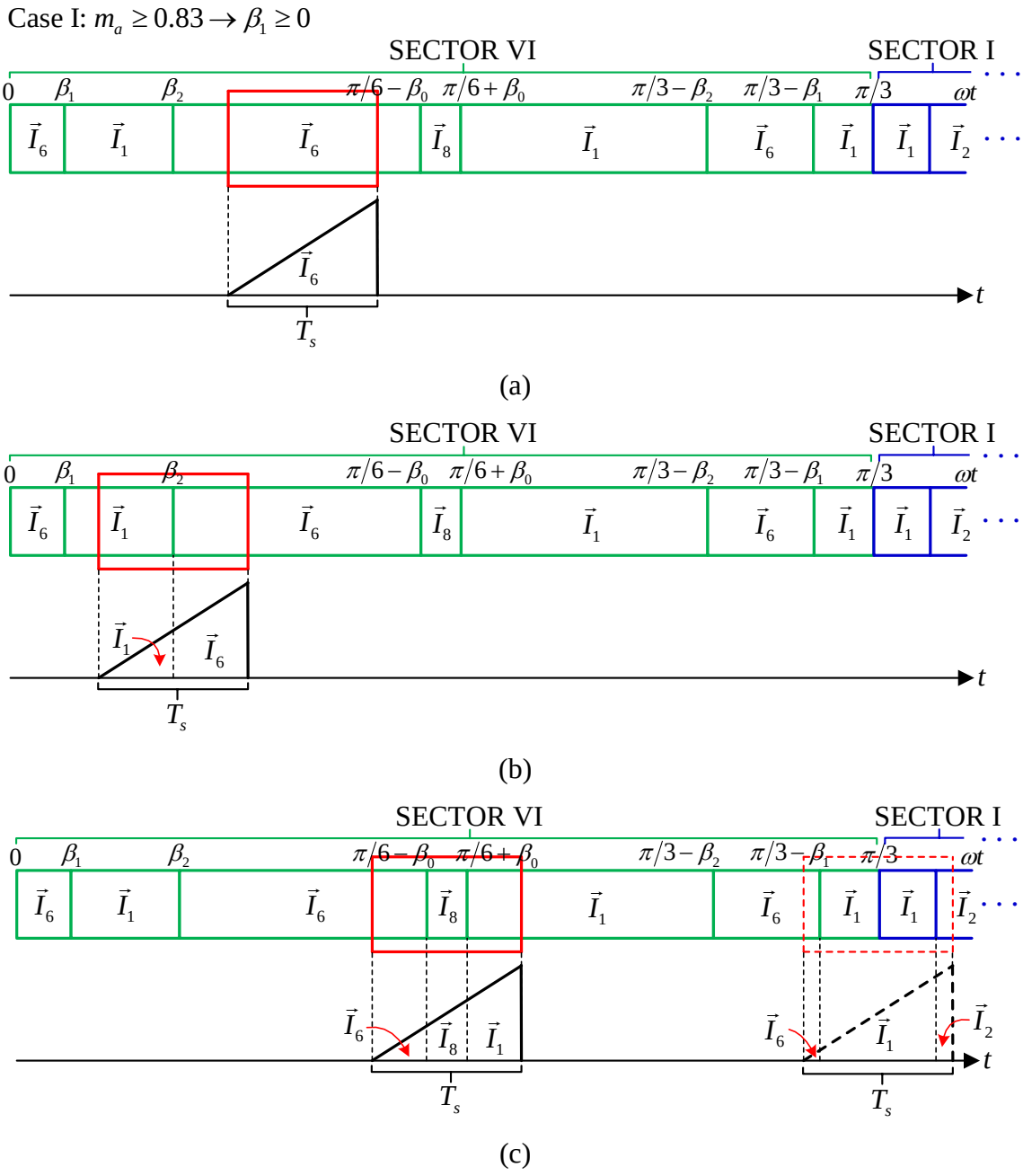


Fig. 4.7 Space vectors during one sampling interval: (a) one vector, (b) two vectors, and (c) three vectors.

4.3 Proposed Model Predictive Switching Pattern Control

With space vector based SHE, SHE waveform can be generated without quantization error, even with a fixed sampling frequency. However, SHE waveform generated by the method can

only ensure steady state performance. It is caused by two reasons, one is that when calculating the reference vector for generating output PWM currents for a CSC, capacitor current compensation only incorporates steady state capacitor currents with transient responses totally ignored, the other is that the essence of SHE modulation is an offline modulation method, which only guarantees steady state performance. In this section, MPSPC is proposed to improve the transient responses of space vector based SHE. In steady state, the output PWM waveforms of a CSC follow SHE-PWM pattern. During transients, the output PWM waveform will be naturally changed, and regulated by MPC approach in order to acquire better dynamic performance. Compared to the existing MPC schemes with low switching frequencies, there is no weighting factor selection issue, such as the one used to associate the predicted load currents and SHE-based output voltage states together in one cost function, as presented in [80]. Fig. 4.8 shows the control block diagram of MPSPC for a CSC with a three-phase *RL* load. In Fig. 4.8, $\vec{i}_w^{SHE}$ represents the selected space vectors based on SHE-PWM pattern during one sampling interval. The selected space vectors and their respective dwell time based on SHE-PWM pattern are sent into MPSPC stage, then the final output PWM current vector, $\vec{i}_w$, can be determined, and used to generate the gate signals for the switching devices in a CSC.

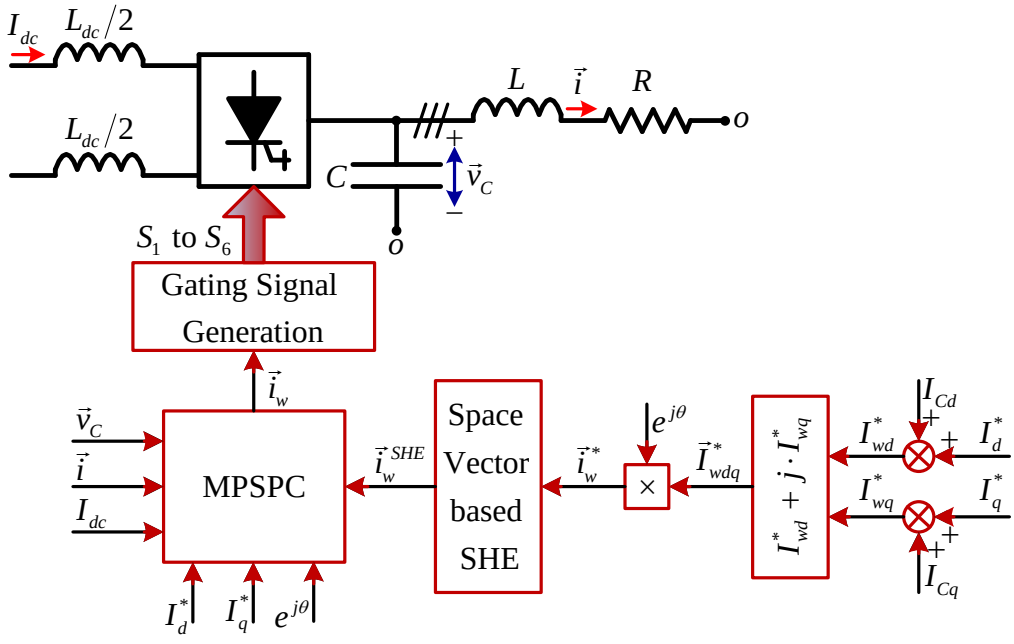


Fig. 4.8 Block diagram of MPSPC for a CSC.

4.3.1 Reference Calculation in Steady State

With load current references, the references for generating output PWM currents in *dq*-axis synchronous frame can be calculated as

$$\begin{cases} I_{wd}^{*} = I_{d}^{*} + I_{Cd}^{LP} \\ I_{wq}^{*} = I_{q}^{*} + I_{Cq}^{LP} \end{cases} \tag{4.6}$$

in which

$$\begin{cases} I_{Cd}^{LP} = -\omega C V_{Cq}^{LP} \\ I_{Cq}^{LP} = \omega C V_{Cd}^{LP} \end{cases} \tag{4.7}$$

where V_{Cd}^{LP}, V_{Cq}^{LP}, I_{Cd}^{LP}, and I_{Cq}^{LP} are the low frequency components of capacitor voltages and capacitor current in *dq*-axis synchronous frame. It can be found from (4.7) that the transient responses of capacitor currents are totally ignored. Finally, the reference vector for generating output PWM currents in $\alpha\beta$-axis stationary frame can be given by

$$\vec{i}_{w}^{*} = \left(I_{wd}^{*} + jI_{wq}^{*} \right) e^{j\theta} \tag{4.8}$$

where θ is the space angle of the synchronous frame, which has different definitions in different applications. In motor drives, θ is equal to the angle of estimated rotor flux vector. On the other hand, grid-connected rectifier or inverter applications, a phase-lock-loop (PLL) is used to acquire the angle of power supply voltage vector, which is the angle of the synchronous frame in these cases.

4.3.2 Principle of Model Predictive Switching Pattern Control

Here, for simplicity, a CSC, which is connected to a three-phase *RL* load, is selected as an example. Hence, with space vector based SHE, the load current vector at (*k*+1)th sampling instant can be predicted based on output PWM current vector following SHE-PWM pattern and corresponding dwell time based on (2.18). Here, the case in Fig. 4.7 (b) is used as an example, in which $\vec{I}_6$ and $\vec{I}_1$ are applied during one sampling interval. Here it is assumed that the dwell time

for $\vec{I}_6$ is equal to T_1, then the effect of the output PWM current vector, which is also the input in (2.18), during the sampling interval can be given by

$$T_s\mathbf{u} = T_1\vec{I}_6 + (T_s - T_1)\vec{I}_1 \tag{4.9}$$

Based on (2.18) and (4.9), the load current vector at the end of the sampling interval can be predicted. A cost function is established here to evaluate the performance on tracking load current reference vector with SHE-PWM pattern, and given by

$$J(k) = \frac{\left|\hat{\vec{i}}^*(k+1) - \vec{i}^{\,p}(k+1)\right|}{\left|\hat{\vec{i}}^*(k+1)\right|} \tag{4.10}$$

where $\left|\hat{\vec{i}}^*(k+1) - \vec{i}^{\,p}(k+1)\right|$ represents the Euclidean distance between the estimated load current reference vector and the predicted load current vector at (k+1)th instant, and $\hat{\vec{i}}^*(k+1)$ is equal to $\vec{i}^*(k)\cdot e^{j\omega T_s}$. $J(k)$ represents a ratio between the Euclidean distance and modulus of the load current reference vector, which can be directly used to evaluate the performance on tracking the load current reference vector.

Since SHE-PWM pattern cannot guarantee satisfactory performance during transients, a maximum limitation of the cost function, $J^{\max}$, can be defined, which is used as a criteria for determining the transition between SHE-PWM pattern and MPC based approach. When the value of $J(k)$ is smaller than $J^{\max}$, the performance on tracking load current reference with SHE-PWM pattern is acceptable, and the output PWM current of the CSC will follow SHE-PWM pattern, which means that $\vec{i}_w$ is equal to $\vec{i}_w^{SHE}$. If $J(k)$ is larger than $J^{\max}$, the output PWM current of the CSC during this sampling interval will be regulated through MPC approach. Here a dead-beat concept is introduced into MPSPC. Based on (2.20) and load current reference vector, the optimal output PWM current vector for the CSC, which eliminates the error between the load current vector and its reference vector in just one sampling interval, can be given by

$$\vec{i}_w^{\,op}(k) = \frac{\hat{\vec{i}}^*(k+1) - \phi_{21}\vec{v}_C(k) - \phi_{22}\vec{i}(k)}{\varphi_{21}} \tag{4.11}$$

where ϕ_{21}, ϕ_{22}, and φ_{21} denote the elements in the prediction matrices, $\mathbf{\Phi}$ and $\mathbf{\Gamma}$, which have been given in (2.19).

Taking delay compensation into consideration, the two-step prediction method, which is presented in Section 1.5.2, is also employed here, with which the load current reference vector should also be shifted one step forward. Finally, the cost function in (4.10) can be modified as

$$J(k+1)=\frac{\left|\hat{\vec{i}}^{*}(k+2)-\vec{i}^{\,p}(k+2)\right|}{\left|\hat{\vec{i}}^{*}(k+2)\right|} \tag{4.12}$$

where $\hat{\vec{i}}^{*}(k+2)$ is the load current reference vector at (k+2)th instant, and can be given by

$$\hat{\vec{i}}^{*}(k+2)=\vec{i}^{*}(k)\cdot e^{j\omega 2T_s} \tag{4.13}$$

in which ω is the angular output frequency of the CSC.

Hence, if $J(k+1)$ is larger than $J^{\max}$, the optimal output current vector for (k+1)th sampling interval, can be given by

$$\vec{i}_w^{\,op}(k+1)=\frac{\hat{\vec{i}}^{*}(k+2)-\phi_{21}\hat{\vec{v}}_C(k+1)-\phi_{22}\hat{\vec{i}}(k+1)}{\varphi_{21}} \tag{4.14}$$

where $\hat{\vec{v}}_C(k+1)$ and $\hat{\vec{i}}(k+1)$ are the estimated capacitor voltage vector and load current vector based on the space vector applied during kth sampling interval and the measured capacitor voltage vector and load current vector at kth sampling instant.

Here, unlike in traditional dead-beat controls, $\vec{i}_w^{\,op}(k+1)$ is not synthesized through SVM, since a high sampling frequency in MPSPC would lead to a large number of commutations during transients, which is not suitable for high power applications. To reduce the number of possible commutations, the space vector, which is the closet to $\vec{i}_w^{\,op}(k+1)$, would be selected and applied during the whole sampling interval, which is called low-complexity MPC in [50, 51], and preserves the advantage of conventional MPC with simpler realization. According to the six active-state space vectors, the space vector domain can be divided into six segments, and the

segment, where $\vec{i}_w^{op}(k+1)$ locates, just corresponds to the active-state space vector, that is the most adjacent to $\vec{i}_w^{op}(k+1)$, as Fig. 4.9 shows. For instance, both $\vec{i}_{w1}^{op}(k+1)$ and $\vec{i}_{w2}^{op}(k+1)$ locate in Segment II, which represent two possible situations appearing in one segment. For $\vec{i}_{w1}^{op}(k+1)$, since the length between $\vec{i}_{w1}^{op}(k+1)$ and $\vec{I}_2$ is shorter than the modulus of $\vec{i}_{w1}^{op}(k+1)$, $\vec{I}_2$ needs to be selected and applied during the sampling interval. In contrast, the length between $\vec{i}_{w2}^{op}(k+1)$ and $\vec{I}_2$ is longer than the modulus of $\vec{i}_{w2}^{op}(k+1)$, so zero-state vector should be chosen instead of $\vec{I}_2$. Due to the redundancy of zero-state vectors, the finally applied zero-state vector should be selected according to the last applied space vector, such as $\vec{I}_7$ corresponding to $\vec{I}_1$ or $\vec{I}_2$, $\vec{I}_8$ corresponding to $\vec{I}_3$ or $\vec{I}_4$, and $\vec{I}_9$ corresponding to $\vec{I}_5$ or $\vec{I}_6$.

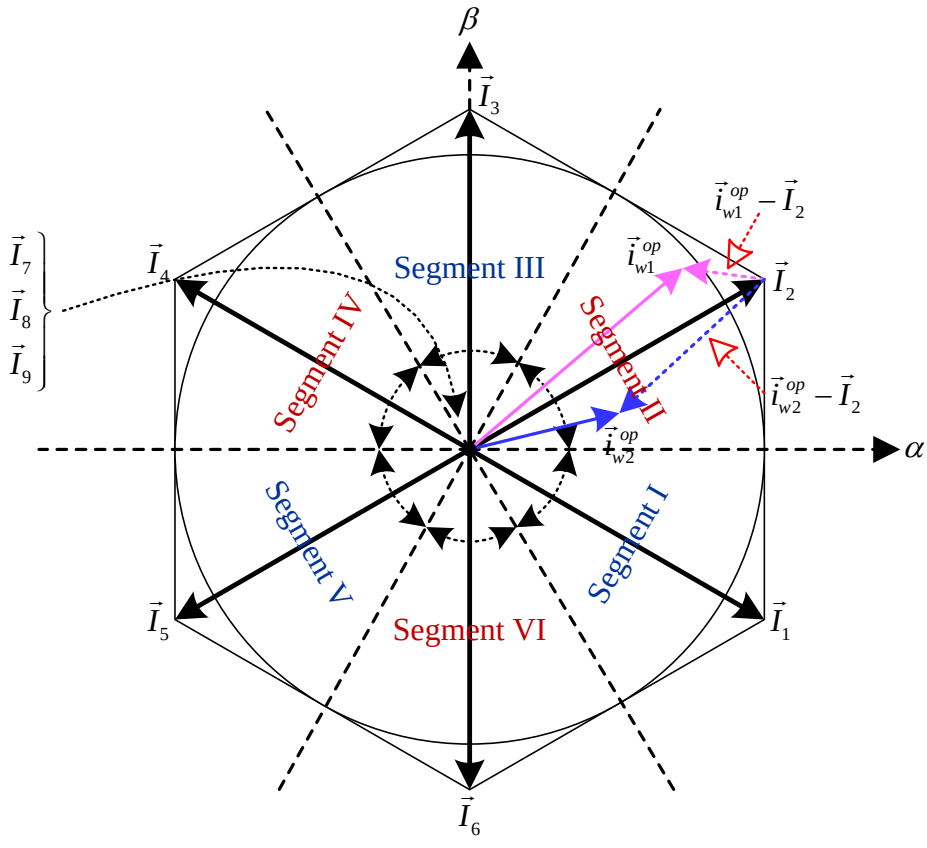


Fig. 4.9 Segment distribution on current vector domain.

The optimally selected space vector can be applied instead of original SHE-PWM pattern during the sampling interval to realize fast and improved transient responses. After transient

process, when $J(k+1)$ gradually decreases to the value smaller than $J^{\max}$, SHE-PWM will be retrieved and applied again. Fig. 4.10 shows the flowchart diagram of MPSPC. In comparison with the existing low switching frequency MPCs, there is no weighting factor tuning issue in the cost function. Though the maximum limitation, $J^{\max}$, is required to be selected, it has more significant physical meaning in contrast to a weighting factor associating two values with different units, since it directly represents the error between the predicted load current vector and its reference. Normally, $J^{\max}$ can be selected as around 15% to satisfy requirements in most application.

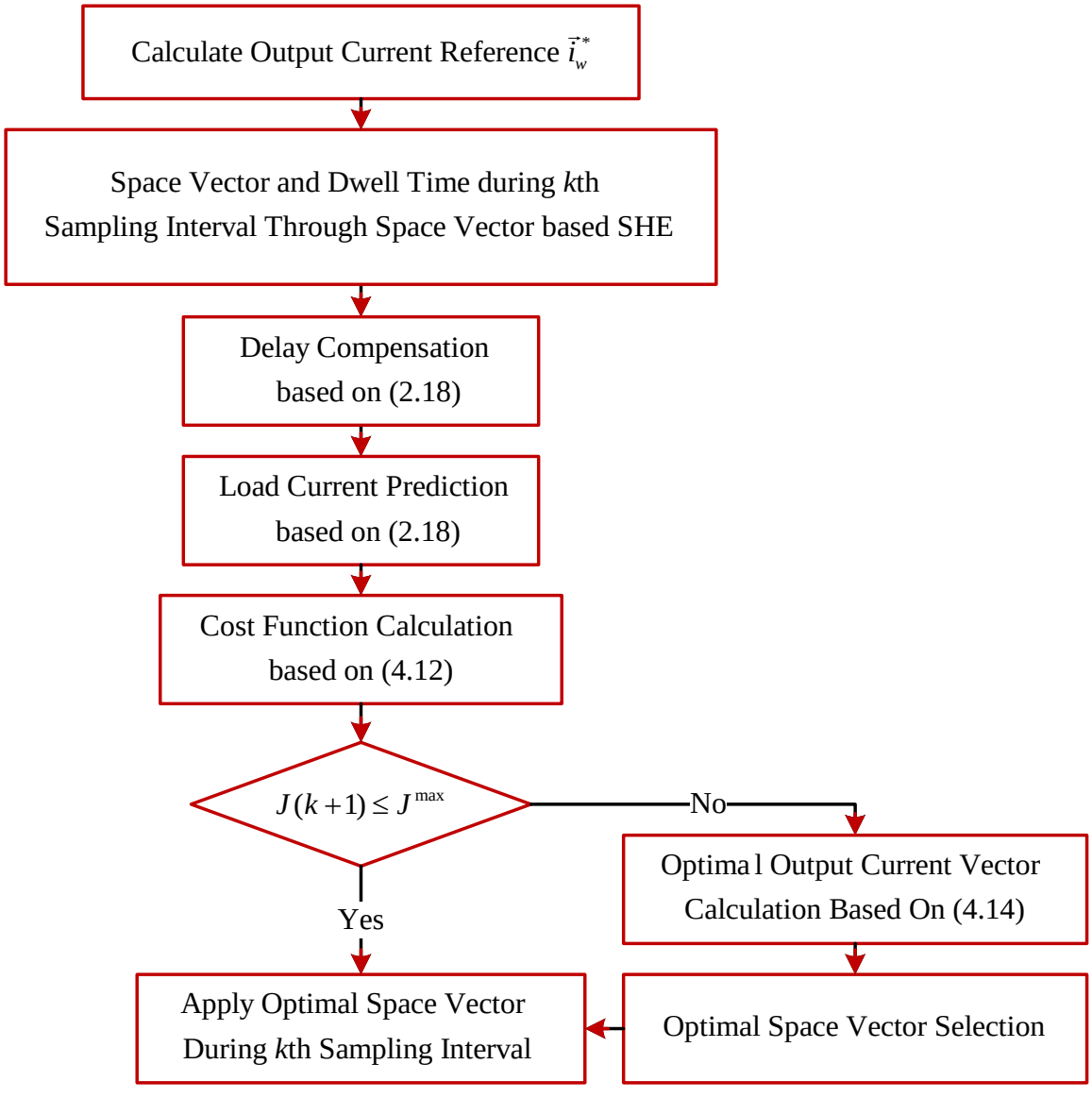


Fig. 4.10 Flowchart diagram of MPSPC.

4.4 Simulation Validation

The simulation results for a 1MW/4160V CSC are presented in this section. The parameters used in simulation are listed in Table 4.3. MPSPC with six-pulse and eight-pulse SHE-PWM pattern are both verified in simulation. The DC current is provided by an ideal DC current source, of which the value is kept at the rated DC current of 196A. The sampling frequency of 10kHz, meaning sampling interval of 100μs is used for MPSPC. The value of $J^{\max}$ is selected as 15%.

Table 4.3 PARAMETERS IN SIMULATION AND EXPERIMENTS

Item	Simulation	Experiment
Rated power	1MW	3kW
Rated voltage	4160V	208V
Capacitor	0.5pu	0.6304pu
Filter inductor	0.3pu	0.2614pu
Load resistor	0.3pu	0.3467pu

4.4.1 Steady State Performance

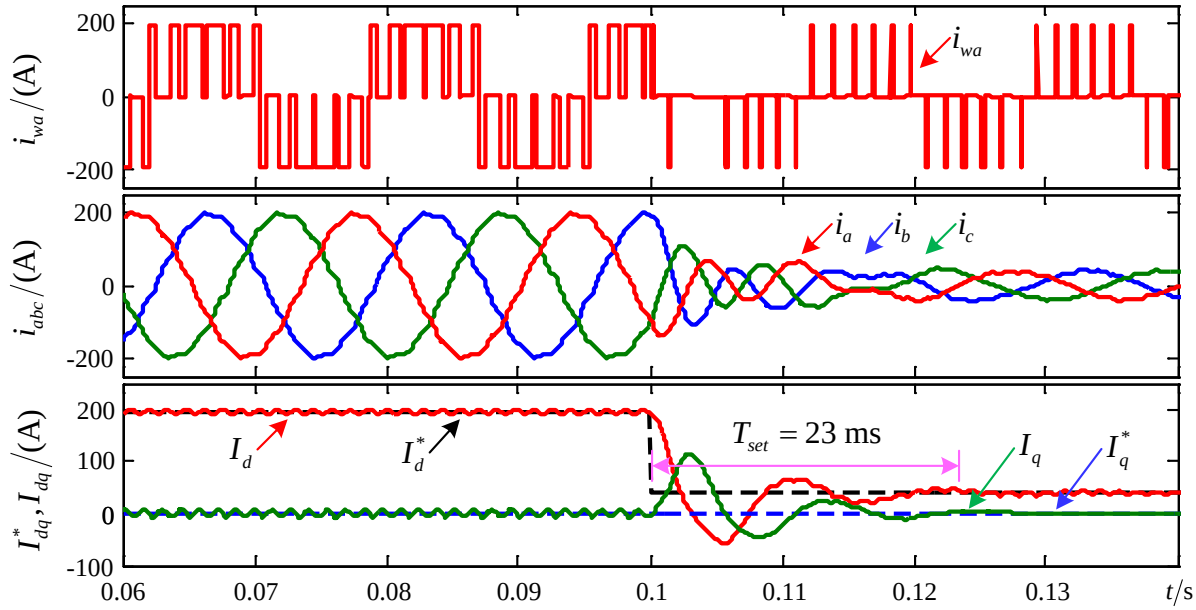
Table 4.4 lists the steady state performance of MPSPC at the operating condition of the *d*-axis load current reference equal to 196A, and the *q*-axis load current reference equal to 0A. For comparison, the results of conventional SHE-MPC with quantization error are also provided, in which the sampling frequency is still 10kHz. It can be found that with conventional SHE-MPC, the unwanted low-order harmonics, no matter 5^{th} and 7^{th} for six-pulse waveform or 5^{th}, 7^{th}, and 11^{th} for eight-pulse waveform, cannot be completely eliminated due to the effect of quantization errors. In contrast, MPSPC totally completes the objectives of low-order harmonic elimination. Though a constant sampling frequency is used in MPSPC, there is no compromise on finally applied switching angles, caused by quantization error, in comparison with pre-calculated optimal ones.

Table 4.4 SIMULATED STEADY STATE PERFORMANCE

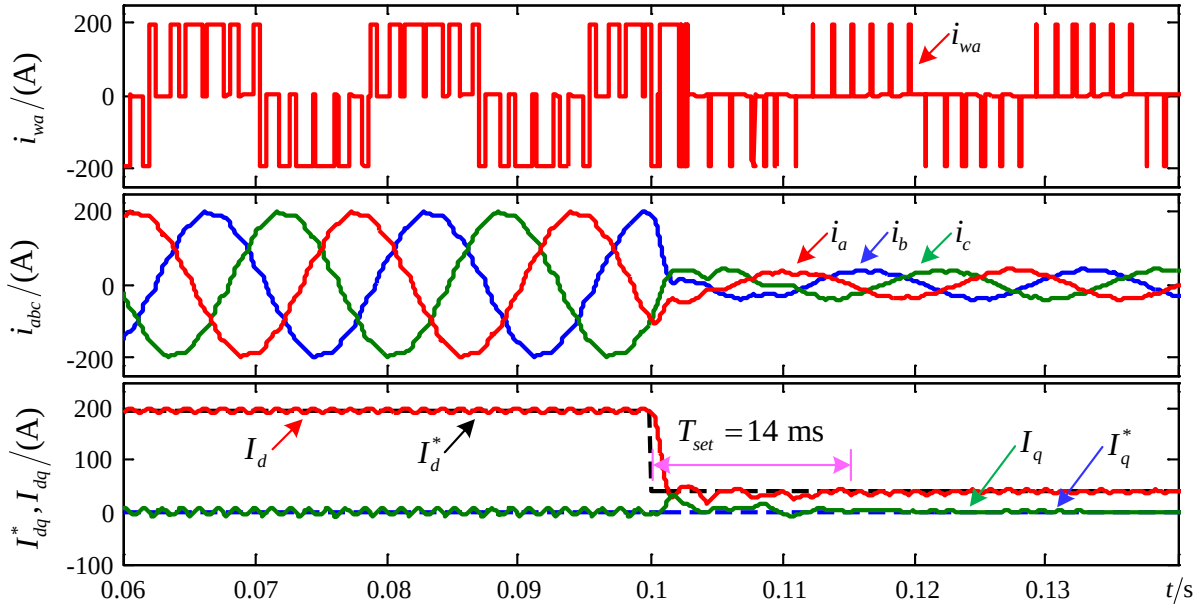
Control scheme	SHE	Harmonic order			
	PATTERN	5^{th} (%)	7^{th} (%)	11^{th} (%)	13^{th} (%)
Traditional SHE-MPC	Six-pulse	2.50	4.06	58.4	21.3
	Eight-pulse	1.66	1.98	3.06	36.3
MPSPC	Six-pulse	0.06	0.27	57.0	22.5
	Eight-pulse	0.28	0.06	0.16	36.8

4.4.2 Transient Responses

Compared to space vector based SHE without prediction process, MPSPC improves dynamic performance. For comparison, the transient responses with space vector based SHE are provided as well. In Fig. 4.11, the output frequency of the CSC is 60Hz, and six-pulse SHE waveform is used here. At time *t* of 0.1s, the *d*-axis load current reference drops from 196A to only 39.3A. The *q*-axis load current reference is kept at 0 during the whole process. During the transient process, the settling time, T_{set}, of the load current is measured with its response staying in a range of 5% of the rated value. It can be observed from Fig. 4.11 (a) that the transient responses of the load currents are very sluggish, and the settling time is equal to 23ms with space vector based SHE. Since the capacitor and the filter inductor in the CSC construct an *LC* resonance tank, obvious resonance can be observed in the load current, especially when transformed into *dq*-axis synchronous frame. On the other hand, during transients, with MPSPC, since the value of the cost function following SHE-PWM pattern can be easily higher than $J^{\max}$, the output PWM pattern of the CSC is naturally changed from SHE-PWM waveform to optimally selected space vectors by MPC approach, with which the load currents fast track their respective references, and the settling time is reduced to only 14ms. Moreover, *LC* resonance is suppressed, since the optimally selected space vector during the transients forces the load currents to follow their respective references. After the transients, it can be found that the output PWM pattern returns to SHE-PWM waveform due to the gradually reduced value of the cost function in the steady state. Hence, without weighting factor tuning issue, MPSPC can still keep SHE-PWM in steady state, and improves dynamic performance during transients.



(a)

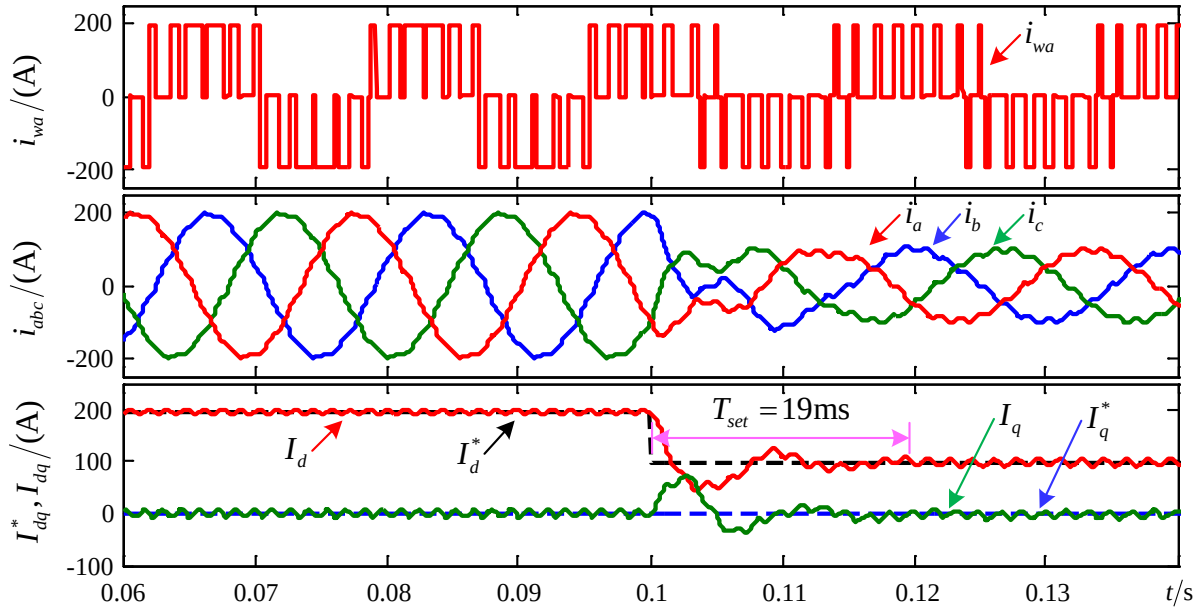


(b)

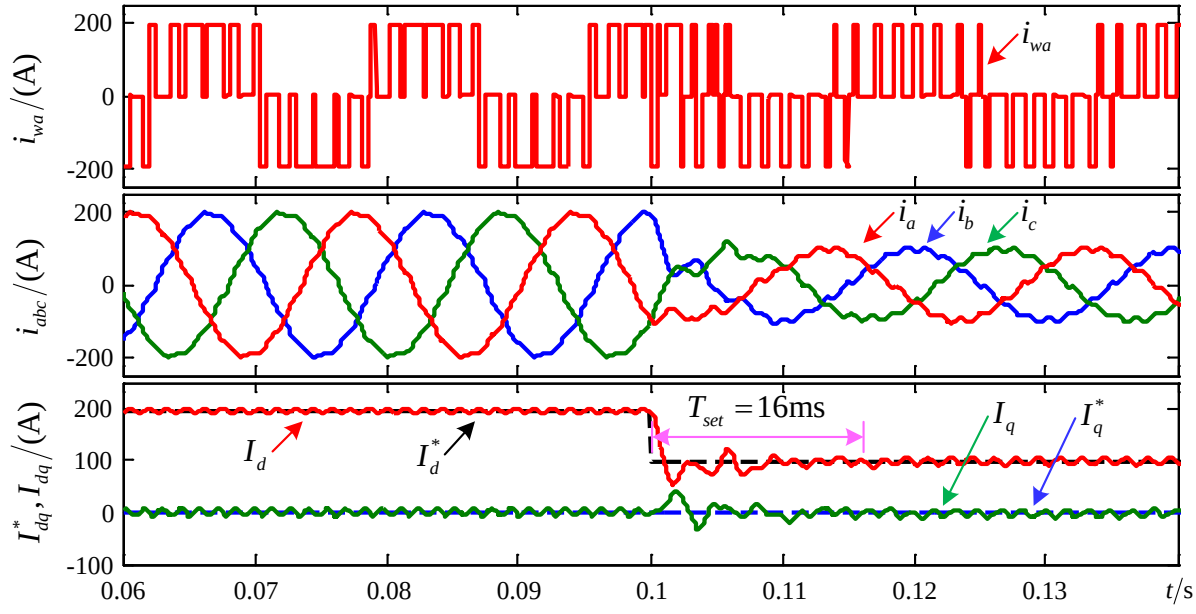
Fig. 4.11 Transient responses with six-pulse SHE waveform: (a) space vector based SHE and (b) MPSPC.

Fig. 4.12 shows the transient response during the change between six-pulse and eight-pulse SHE-PWM waveform. At time *t* of 0.1s, the output frequency of the CSC decreases from 60Hz to 50Hz, which makes the SHE-PWM pattern change from six pulse to eight pulse. At the same

time, the *d*-axis load current reference decreases from 196A to 98A, and the *q*-axis load current reference is kept at 0. With space vector based SHE, the transient responses are slow, and resonance appears in the load currents. With MPSPC, the dynamic performance of the load current is improved with the decrease of the settling time from 19ms to 16ms, and *LC* resonance is suppressed during the transients as well.



(a)



(b)

Fig. 4.12 Transient performance during the change of output frequency: (a) space vector based SHE and (b) MPSPC.

4.5 Experimental Validation

The experimental validation of MPSPC with six-pulse and eight-pulse SHE-PWM patterns is also conducted. The parameters used in experiments have already been listed in Table 4.3. The sampling frequency is still 10kHz, meaning the sampling interval of $100\mu s$, and $J^{\max}$ is still 15%. The DC current is kept at 11.8A, which is the rated value for a 3kW/208V CSC.

4.5.1 Steady-State Performance

The experimental results of conventional SHE-MPC and MPSPC are both presented at the operating condition of the *d*-axis load current reference equal to 11.8A and the *q*-axis load current reference equal to 0. Fig. 4.13 shows phase A load current, phase A output PWM current, and its spectrum diagram of conventional SHE-MPC and MPSPC. Due to quantization error, the output PWM current of conventional SHE-MPC contains obvious low-order harmonics. Moreover, as can be observed in Fig. 4.13 (b), the quantization effect makes some very small pulses missing from the eight-pulse waveform, which leads to only six or seven pulses per half cycle. On the other hand, MPSPC achieves better performance on low-order harmonic elimination than conventional SHE-MPC, no matter with six-pulse or eight-pulse SHE-PWM pattern. The details on the low-order harmonic contents are listed in Table 4.5. With MPSPC, the unwanted low-order harmonics can be mitigated to very small amounts. It can be found that the harmonic contents in Table 4.5 are higher than the results presented in Table 4.4. The reason is that the DC current used in experiments is not ideal, and contains some ripples, which leads to some compromises on low-order harmonic elimination.

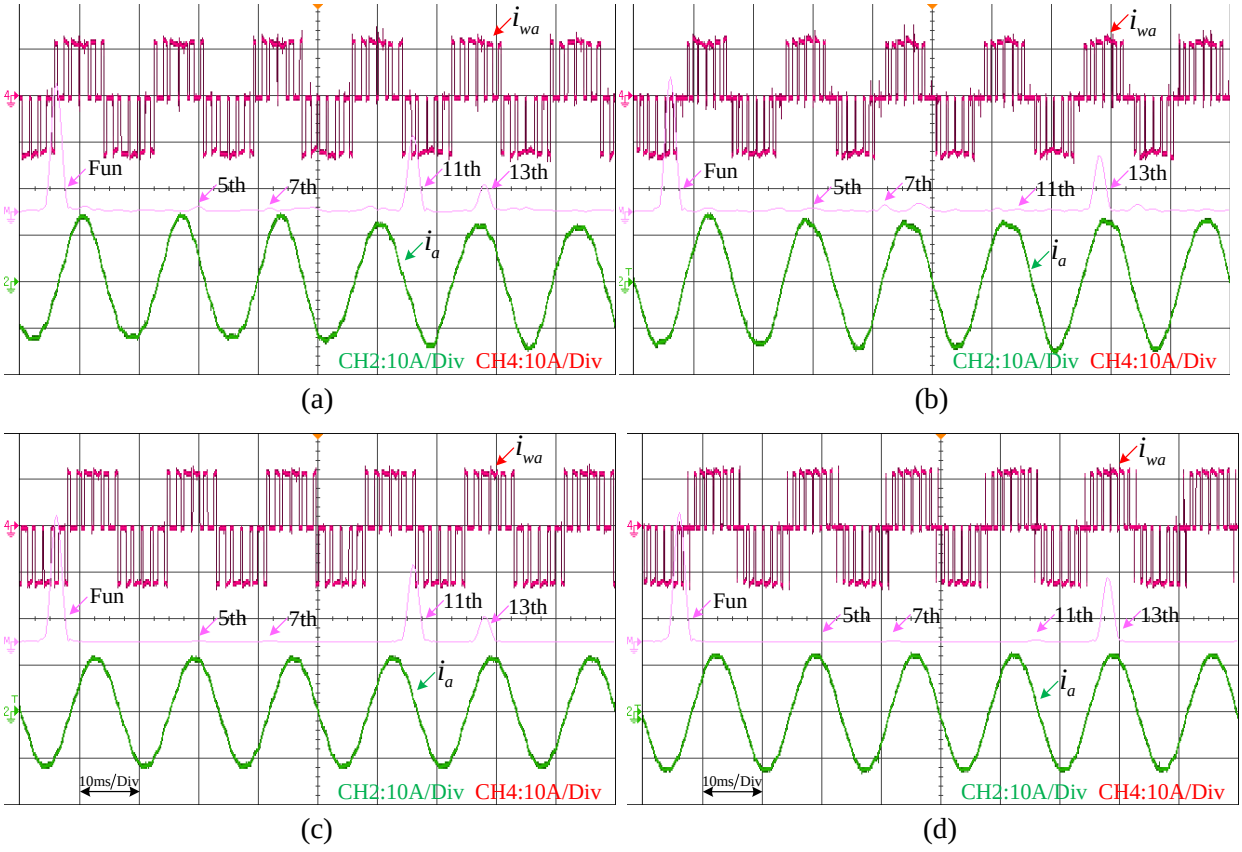


Fig. 4.13 Spectrum diagram of experimental output PWM currents: (a) six-pulse SHE-MPC, (b) eight-pulse SHE-MPC, (c) six-pulse MPSPC, and (d) eight-pulse MPSPC.

Table 4.5 EXPERIMENTAL STEADY STATE PERFORMANCE

Control scheme	SHE PATTERN	Harmonic order			
		5^{th} (%)	7^{th} (%)	11^{th} (%)	13^{th} (%)
Traditional SHE-MPC	Six-pulse	6.36	2.73	60.0	20.0
	Eight-pulse	2.63	5.26	2.61	42.1
MPSPC	Six-pulse	0.91	0.91	61.8	20.0
	Eight-pulse	0.45	0.91	1.81	50.9

4.5.2 Dynamic Performance

Fig. 4.14 shows the experimental transient responses with six-pulse SHE-PWM waveform. The output frequency is 60Hz, and the *d*-axis load current reference suddenly drops from 11.8A to 2.36A. From top to bottom, the phase A output PWM current, the phase A load current, the *dq*-axis load current components, and their respective references are shown. With space vector

based SHE, significant resonance can be observed in the waveforms of the *dq*-axis load currents, as Fig. 4.14 (a) shows. The settling time is equal to 21ms. Fig. 4.14 (b), with MPSPC, the *d*-axis load current changes from 11.8A to 2.36A faster, and resonance in the load currents is suppressed with the decrease of the settling time to 13ms. The transition from SHE-PWM pattern to MPC can be observed from the output PWM current waveform during the transient. After the transient, the output PWM current of the CSC is governed by SHE-PWM again.

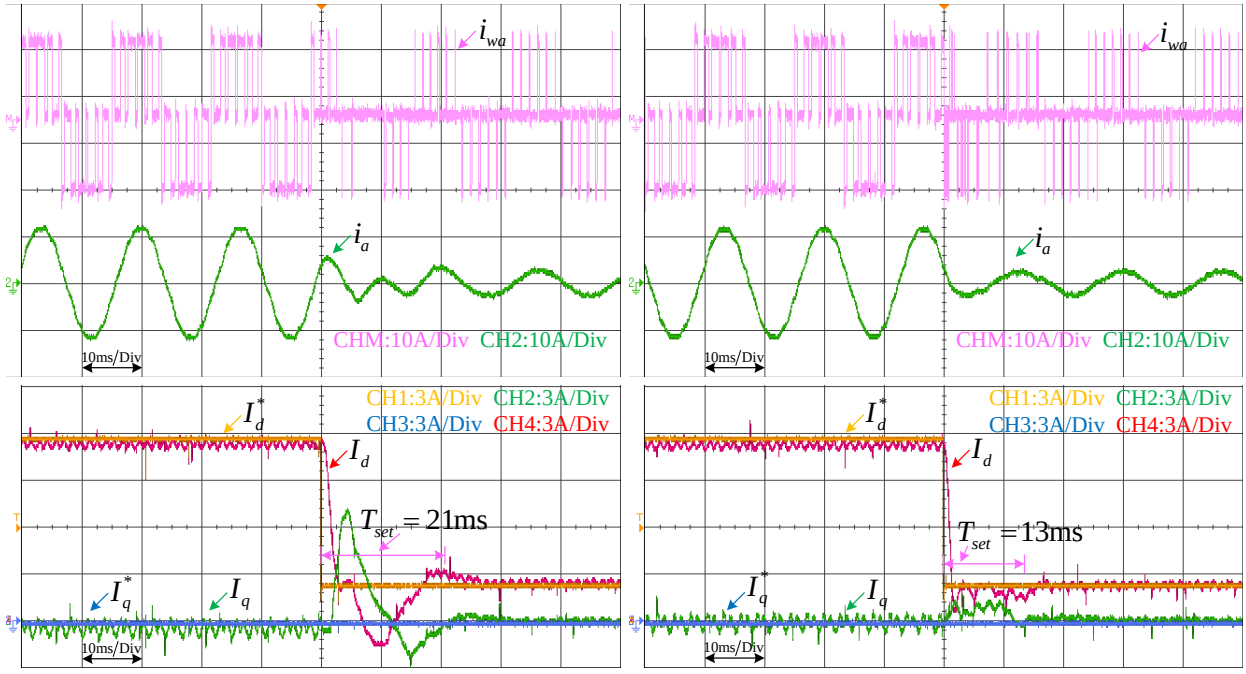
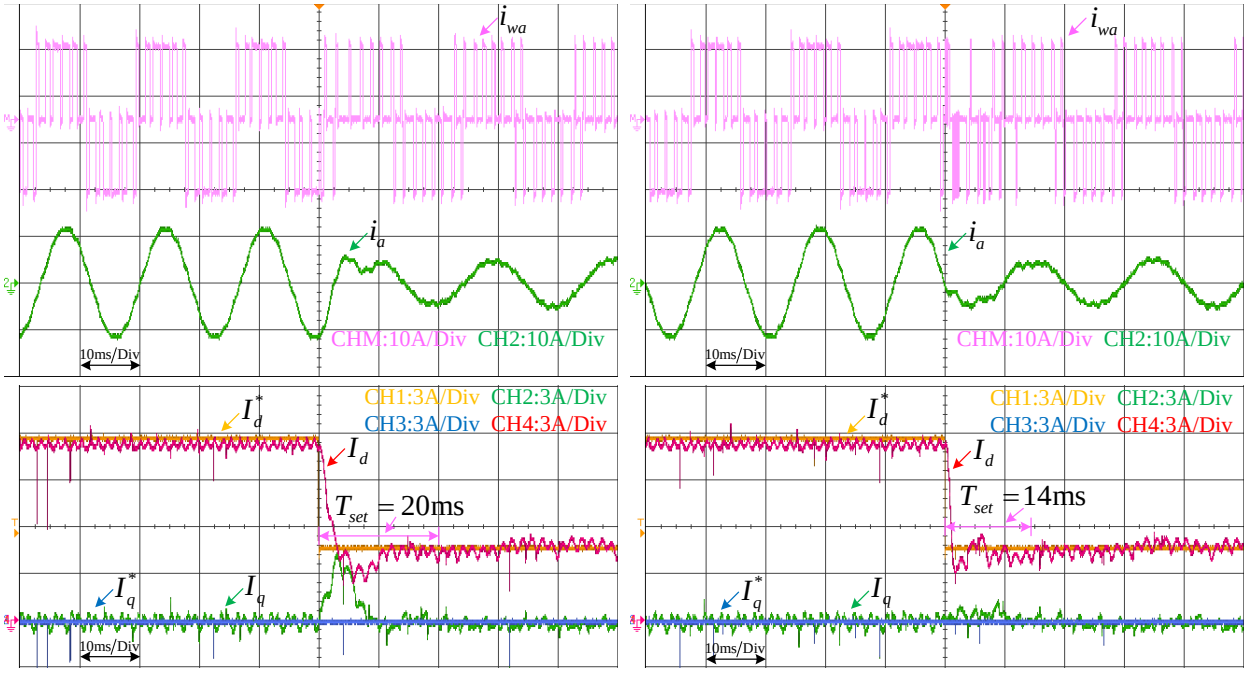


Fig. 4.14 Experimental transient responses with six-pulse SHE waveform: (a) space vector based SHE and (b) MPSPC.

Fig. 4.15 shows the experimental results the change from six-pulse to eight-pulse SHE-PWM. The output frequency is initially 60Hz, then changes to 50Hz with SHE-PWM pattern modified from six-pulse to eight-pulse. At the same time, the *d*-axis load current reference drops from 11.8A to 4.72A. Similarly, with the transition from SHE-PWM pattern to MPC with MPSPC, *LC* resonance is suppressed, the response of the load currents becomes faster, and the settling time decreases from 20ms to 14ms, in comparison with the results of space vector based SHE, which also verifies the improvement on dynamic performance with MPSPC.



(a) (b)

Fig. 4.15 Experimental transient performance during the change of output frequency: (a) space vector based SHE and (b) MPSPC.

4.6 Conclusions

In this chapter, MPSPC has been presented. In comparison with the state-of the-art schemes, MPSPC offers three major advantages

- As the foundation of MPSPC, space vector based SHE eliminates the quantization effect introduced by constant sampling frequency of MPC. Without quantization error, low-order harmonics elimination based on pre-calculated optimal switching angles can be thoroughly completed;
- Another benefit offered by MPSPC is that there is no weighting factor used in it. Though a maximum discrepancy limitation of regulating load currents needs to be selected to ensure transition between SHE-PWM pattern and optimal output current vector selected by MPC during transients, it owns more significant meaning in contrast to a weighting factor;
- MPSPC only uses one-step or horizon-one prediction, which leads to a simpler structure, and reduces complexity, in comparison with existing multi-step schemes.

5 Model Predictive Space Vector Pattern Control for High Power Current-Source Converter-Fed Medium-Voltage Induction Motor Drive

MPSPC has been presented in Chapter 4. However, the optimal switching angles to generate SHE-PWM pattern still need to be pre-calculated and stored, which makes MPSPC not suitable for motor drive application with variable output frequency, either. The concept of MPSPC can be further expanded, and involved with space vector modulation (SVM). In this section, based on the core methodology of MPSPC, model predictive space vector pattern control (MPSVPC) is proposed for high power CSC-fed MV IM drives. The innovation of this scheme is very similar to that of MPSPC, but MPSVPC is involved with SVM, which is an online modulation method.

The merits of MPSVPC can be classified as

- In contrast to traditional SVM, MPSVPC preserves a fixed and very low switching frequency in steady state, and improves dynamic performance during transient processes;
- In comparison with MPSPC, there is no requirement on calculation of optimal switching angles in MPSVPC;
- Last but not least, MPSVPC is still totally based on one-step prediction, and there is no weighting factor selection issue in it.

5.1 Model Predictive Space Vector Pattern Control

5.1.1 Limitation of Traditional Modulation and Linear Control

The configuration of a high power CSC-fed MV IM drive has been illustrated in Fig. 2.4. The control block diagram of the traditional linear controls for high power CSC-fed MV IM drive has been presented in Section 1.4, in which delay angle control is used for CSR, and FOC is applied into CSI. Though traditional linear controls are widely adopted in high power CSC-fed MV IM drive, they still have some drawbacks especially in terms of transient responses. The reasons resulting in their relatively poor dynamic performance are mainly three folds as

1) First, in order to minimize switching losses, the switching frequency of CSC is normally kept at several hundred hertz in high power MV applications, which leads to a relatively long control period and sluggish tuning of controllers;

2) Second, only steady state components in capacitor currents are compensated at CSI side, which makes dynamic performance of stator current not guaranteed;

3) Finally, three-phase capacitors construct *LC* resonance tanks with line inductor at CSR side and leakage inductor at CSI side, which further deteriorates transient responses due to possible *LC* resonance.

On the other hand, traditional SVM imposes some constraints on dynamic performance of CSC in high power MV IM drives as well. As an online modulation method, SVM can be flexibly used to generate output waveform with variable frequency. However, the output current reference vector is always synthesized over one relatively long control period, which weakens the speed and accuracy of responses during transient process.

5.1.2 Model Predictive Space Vector Pattern Control

Since the dynamic performance of traditional SVM is limited by its relatively long control period in order to keep low switching frequency, MPSVPC is proposed, which reserves fixed and low switching frequency as that of traditional SVM in steady state, and achieves improved dynamic performance. As Fig. 5.1 (a) shows, in traditional SVM, the dwell time for each current vector is only updated once during one control period of traditional SVM, $T_s^{'}$. In contrast, Fig. 5.1 (b) illustrates that with MS-SVM, the dwell time for each current vector is updated several times during every control period. Furthermore, Fig. 5.1 (c) shows that in MPSVPC every control period can be evenly divided into several small sampling intervals. The space vectors applied during every sampling interval can be determined based on space vector sequence, that is deduced through traditional SVM. According to space vectors and respective dwell time of each space vector during every sampling interval, the values of state variables at the end of sampling interval can be predicted based on prediction model and information on state variables at the beginning of sampling interval. The core part of MPSVPC is that based on pre-defined criteria, if the evolution of state variables based on space vector pattern set by traditional SVM

can fulfill this criteria, the applied space vector will just follow traditional space vector modulation pattern, which keeps a relatively low and fixed switching frequency. On the other hand, especially during transient process, due to the constraints imposed by the relatively long control period of traditional SVM, space vector pattern based on traditional SVM would fail to meet the criteria, so a reselected space vector would be applied during the sampling interval instead of the space vector pattern based on traditional SVM in order to improve dynamic performance.

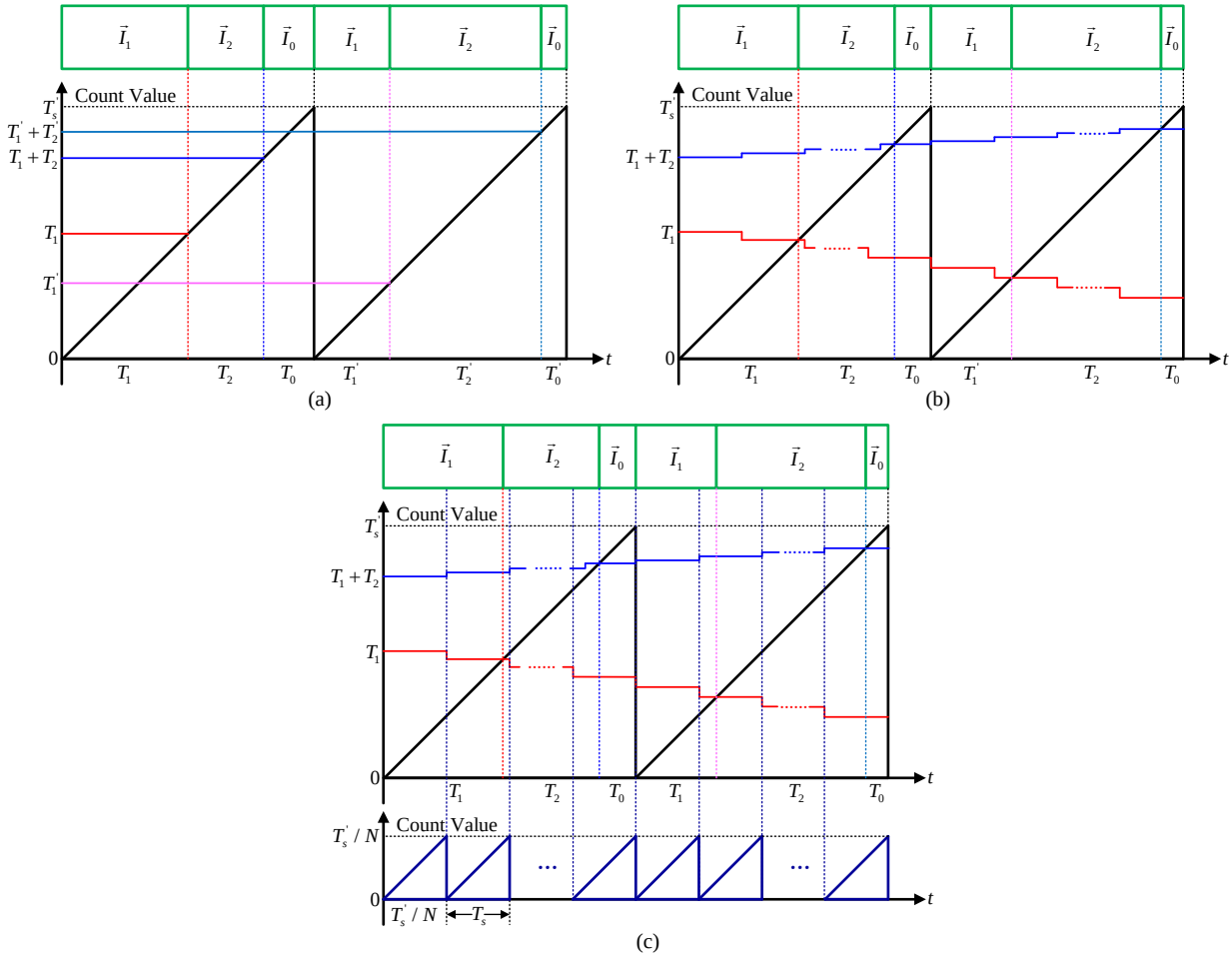


Fig. 5.1 Diagram of relation between sampling interval of MPSVPC and control period of traditional SVM: (a) traditional SVM, (b) MS-SVM, and (c) MPSVPC.

Following the mechanism of MPSVPC, there are three situations of the applied space vector during one sampling interval, as Fig. 5.2 shows. In Fig. 5.2 (a), the sampling interval locates inside the range of one space vector, which makes one space vector conducted during the whole

sampling interval. Fig. 5.2 (b) shows the second case in which one transition between two space vectors are applied during the sampling interval. The last case, as shown in Fig. 5.2 (c), possibly happens when the dwell time for the second space vector based on tradition SVM is very short, and the sampling interval includes the entire dwell time of the second space vector inside it, which leads to that there are three space vectors conducted during one sampling interval.

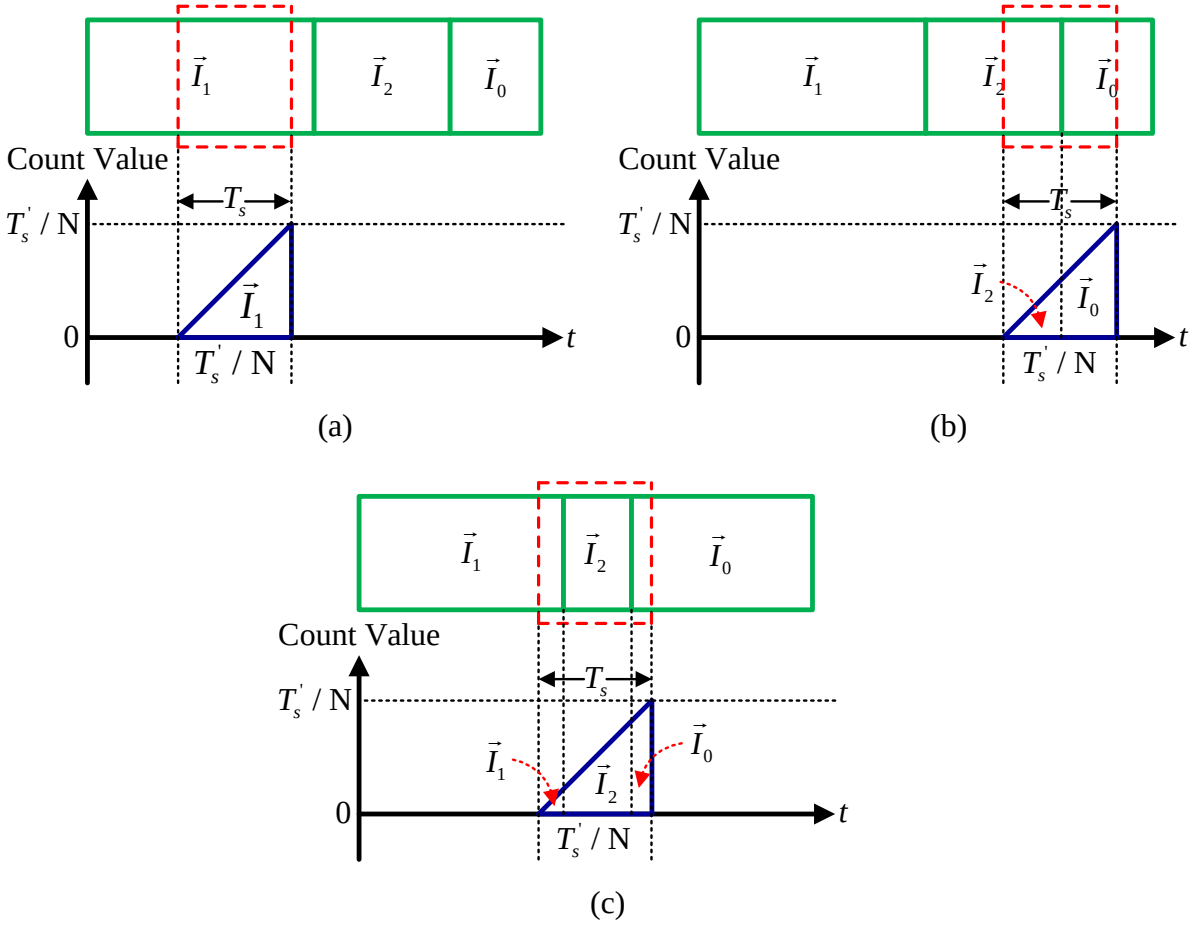


Fig. 5.2 Diagram of three situations of applied space vectors in one sampling interval with MPSVPC.

Based on the space vectors and the respective dwell time of them applied during one sampling interval, and the values of state variables at the beginning of the interval, the value of state variables at the end of the sampling interval can be predicted based on (2.21) and (2.28) for CSR and CSI in a high power CSC-fed MV IM drive.

A cost function can also be established here to assess the performance on tracking load current reference vector with traditional SVM pattern in one sampling interval, which is given by

$$J(k)=\frac{\left|\hat{\vec{i}}^{*}(k+1)-\vec{i}^{\,p}(k+1)\right|}{I^{R}} \tag{5.1}$$

where $\hat{\vec{i}}^{*}(k+1)$ denotes the estimated load current reference vector at (k+1)th sampling instant, which is given by $\vec{i}^{*}(k)\cdot e^{j\omega T_s}$; $\vec{i}^{\,p}(k+1)$ is the predicted load current vector at (k+1)th sampling instant; I^{R} is the magnitude of rated load current. The cost function represents a ratio between the predicted error on tracking load current reference vector with traditional SVM space vector pattern and rated load current magnitude, which is used to evaluate the performance on tracking reference.

Since space vector pattern based on traditional SVM cannot guarantee satisfactory performance during transients, a maximum value of (5.1), $J^{\max}$, is defined, and used as an evaluation index to determine transition between traditional SVM and MPC approach. If $J(k)$ is smaller than $J^{\max}$, the performance on tracking reference based on traditional SVM switching pattern is acceptable, and the output PWM current of CSC will follow traditional SVM space vector pattern. On the other hand, if $J(k)$ is larger than $J^{\max}$, the output PWM current of CSC during the sampling interval will be regulated by MPC approach, through which an optimal space vector is going to be selected, then conducted over the whole sampling interval. Similar as the selection process in MPSPC, based on load current reference vector and corresponding prediction model, an optimal output current vector, which eliminates the error between load current vector and its reference within only one sampling interval, can be given by

$$\vec{i}_{w}^{\,op}(k)=\frac{\hat{\vec{i}}^{*}(k+1)-\phi_{21}\cdot\vec{v}_{C}(k)-\phi_{22}\cdot\vec{i}(k)-\varphi_{21}\cdot\vec{u}_{1}(k)}{\varphi_{22}} \tag{5.2}$$

where ϕ_{21}, ϕ_{22}, φ_{21}, and φ_{22} are the elements in prediction matrices, $\mathbf{\Phi}$ and $\mathbf{\Gamma}$; $\vec{u}_{1}(k)$ represents the first input vector, which is determined according to different applications. At CSR

side, $\vec{u}_1(k)$ is equal to power supply voltage space vector, whereas it is equal to rotor flux vector at CSI side.

Taking delay compensation into consideration, based on the two-step prediction method, (5.1) should be shifted one step forward, and can be given by

$$J(k+1)=\frac{\left|\hat{\vec{i}}^{*}(k+2)-\vec{i}^{\,p}(k+2)\right|}{I^{R}} \tag{5.3}$$

where $\hat{\vec{i}}^{*}(k+2)$ is the estimated load current reference vector at (k+2)th sampling instant, which is equal to $\vec{i}^{*}(k)\cdot e^{j2\omega T_s}$, and $\vec{i}^{\,p}(k+2)$ is the predicted load current vector based on the space vectors applied during (k+1)th sampling interval based on traditional SVM space pattern, and the estimated load current vector at (k+1)th sampling instant.

If $J(k+1)$ is larger than $J^{\max}$, the optimal output current vector can be given by

$$\vec{i}_w^{\,op}(k+1)=\frac{\hat{\vec{i}}^{*}(k+2)-\phi_{21}\cdot\hat{\vec{v}}_C(k+1)-\phi_{22}\cdot\hat{\vec{i}}(k+1)-\varphi_{21}\cdot\vec{u}_1(k+1)}{\varphi_{22}} \tag{5.4}$$

where $\hat{\vec{v}}_C(k+1)$, $\hat{\vec{i}}(k+1)$, and $\vec{u}_1(k+1)$ are the estimated state variables and the first input at (k+1)th sampling instant.

Similarly as in MPSPC, in order to reduce the number of switching commutations, the space vector, which is the most adjacent to $\vec{i}_w^{\,op}(k+1)$, would be selected and applied during the whole sampling interval. The selection process has been discussed in Section 4.3.2. Fig. 5.3 shows the flowing chart of optimal space vector selection process in MPSVPC. Normally, $J^{\max}$ can be selected as 15% to satisfy requirements in most applications.

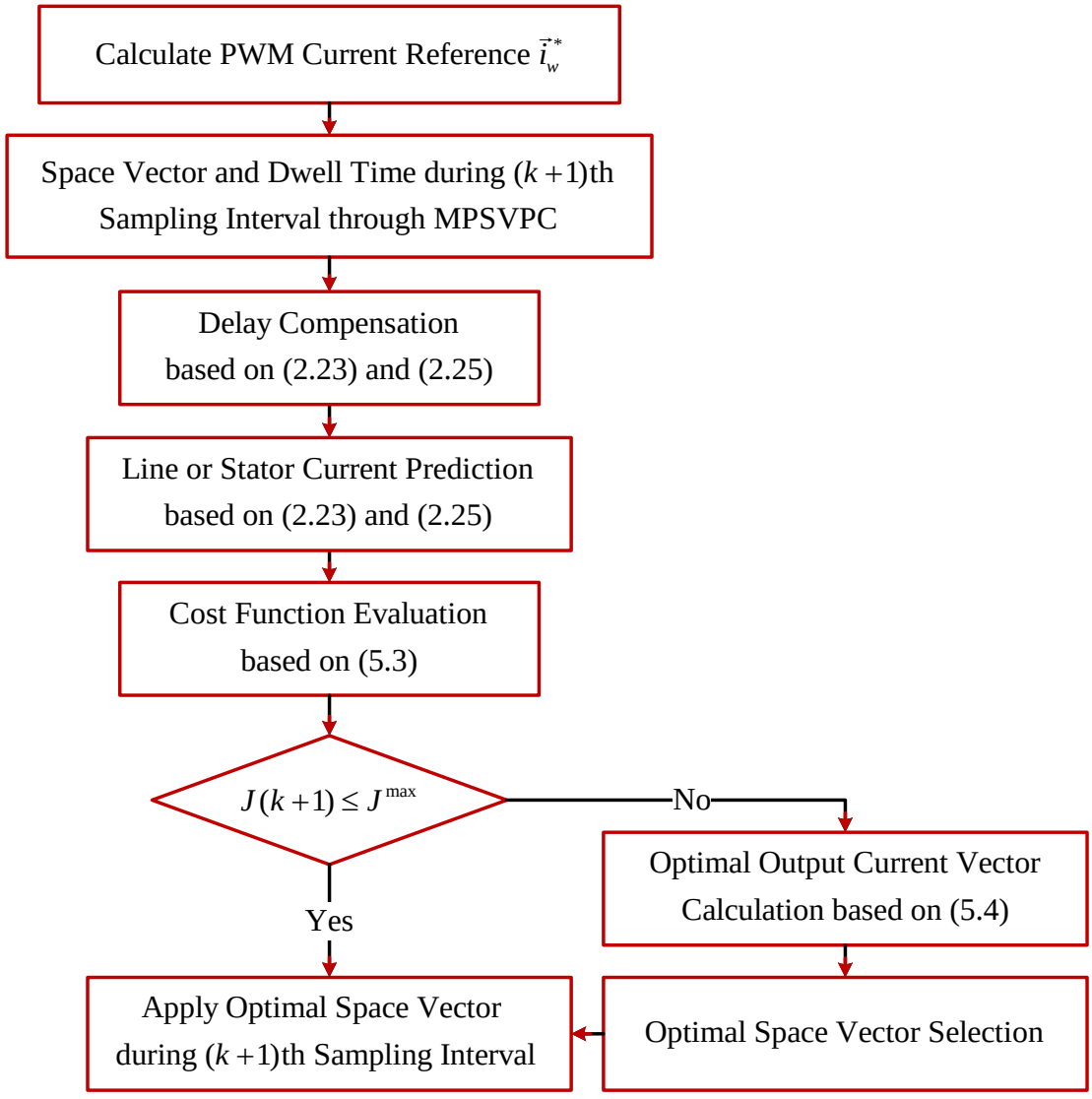


Fig. 5.3 Flowing chart diagram of optimal space vector selection process in MPSVPC.

5.1.3 Overall Control Structure

In contrast to the traditional control structure, discussed in Section 1.4, MPSVPC can be used to directly replace traditional SVM block. The calculated modulating index, input current reference angle, θ_{wr}, for CSR, and output current reference angle, θ_{wi}, for CSI, are still used to generate traditional SVM based space vector patterns, which are assessed with the pre-defined cost function (5.3). The main difference between the traditonal control scheme and MPSVPC focuses on that line current reference vector and stator current reference vector need to be calculated in MPSVPC. For CSR, since modulating index control is used to regulate DC current,

line current references in *dq*-axis synchronous frame with respect to CSR-side capacitor voltage can be given by

$$\begin{cases} I_{gd}^{*} = m_r I_{dc} + I_{Crd}^{LP} \\ I_{gq}^{*} = I_{Crq}^{LP} \end{cases} \tag{5.5}$$

where

$$\begin{cases} I_{Crd}^{LP} = -\omega_g C_r V_{Crq}^{LP} \\ I_{Crq}^{LP} = \omega_g C_r V_{Crd}^{LP} \end{cases} \tag{5.6}$$

in which ω_g is the angular frequency of power supply voltage; V_{Crd}^{LP} and V_{Crq}^{LP} are the filtered *dq*-axis components of CSR-side capacitor voltages. Finally, line current reference vector can be given by

$$\vec{i}_g^{*} = (I_{gd}^{*} + jI_{gq}^{*}) \cdot e^{j\theta_{Cr}} \tag{5.7}$$

where θ_{Cr} is the angle of CSR-side capacitor voltage vector, which is obtained from a PLL stage.

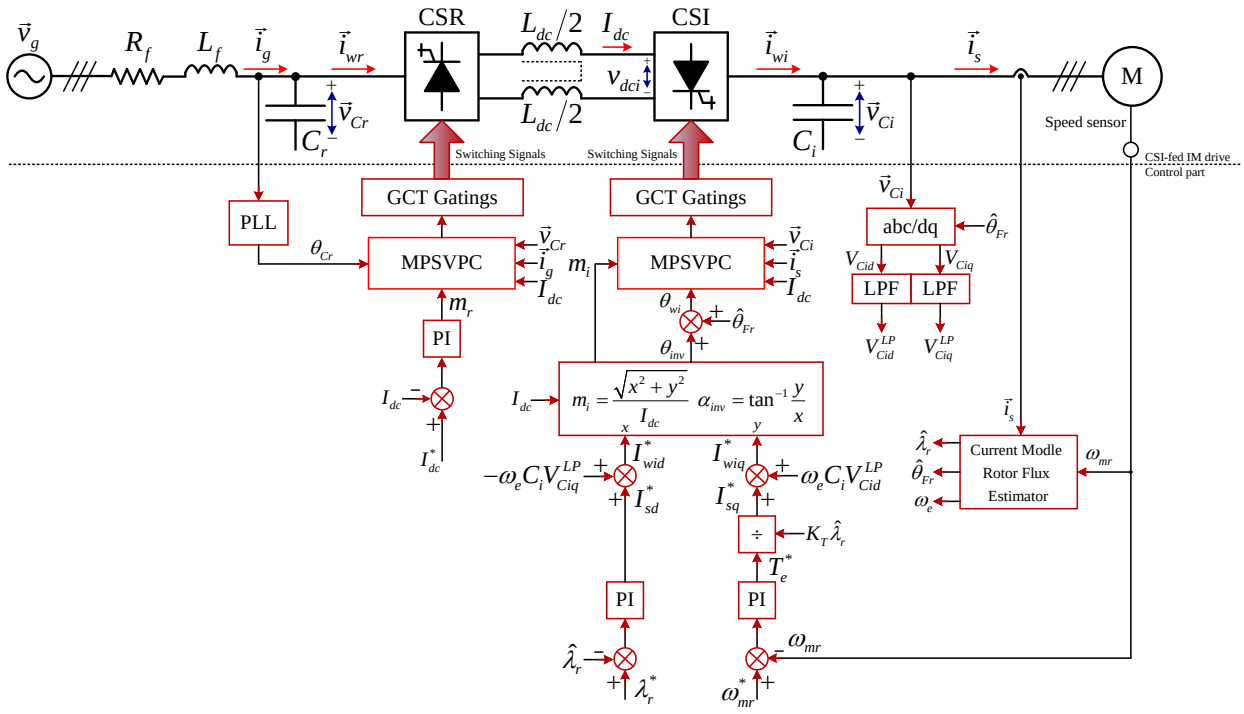
At CSI side, since the stator current references in *dq*-axis synchronous frame with respect to rotor flux vector have been calculated by outer control loops in traditional FOC, stator current reference vector in $\alpha\beta$ -axis stationary frame can be given by

$$\vec{i}_s^{*} = (I_{sd}^{*} + jI_{sq}^{*}) \cdot e^{j\theta_{Fr}} \tag{5.8}$$

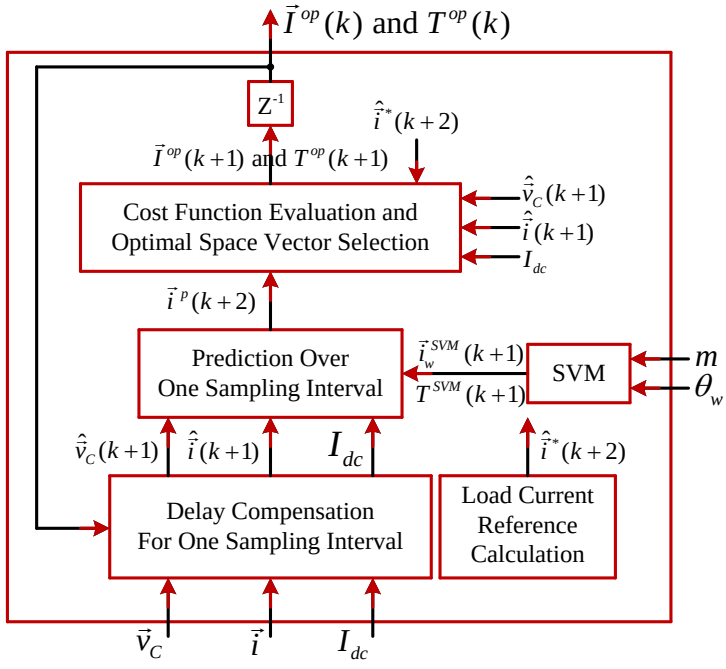
where θ_{Fr} is the angle of estimated rotor flux vector.

Fig. 5.4 shows the control block diagram of MPSVPC. The overall control structure is shown in Fig. 5.4 (a), it can be observed that except the PWM generation stage, the remaining part of MPSVPC is similar to that of traditional control scheme, which has been shown in Section 1.4. The similarity of outer control parts between MPSVPC and traditional control scheme makes the application of MPSVPC much easier. Fig. 5.4 (b) shows the details on the inner structure of MPSVPC block when used for high power CSC-fed MV IM drive, in which delay compensation process has been included. In Fig. 5.4 (b), based on state variables at *k*th sampling instant, optimal space vector determined during (*k*-1)th sampling interval, and prediction model, state

variables at (k+1)th sampling instant, namely $\hat{\vec{v}}_C(k+1)$ and $\hat{\vec{i}}(k+1)$, can be estimated. Based on the space vector pattern for (k+1)th sampling interval determined by traditional SVM, predicted load current vector at (k+2)th sampling instant can be calculated, then substituted into (5.3) to be compared with $\hat{\vec{i}}^*(k+2)$. When the result of (5.3) is lower than the criteria, space vector pattern defined by traditional SVM will be conserved, and applied as the optimal space vector pattern, otherwise, the optimal space vector will be reselected based on (5.4), and applied during (k+1)th sampling interval.



(a)



(b)

Fig. 5.4 Control block diagram of MPSVPC: (a) overall control structure and (b) inside details of MPSVPC block.

5.2 Simulation Validation

In order to assess the performance of MPSVPC, simulation is conducted on a high power CSC-fed MV IM drive (1MW/4160V/139A), of which the parameters are listed in Table 5.1. The control period for SVM is selected as $926\mu s$, which leads to control frequency of 1080Hz, and switching frequency of 540Hz. The sampling interval for MPSVPC, which is equal to $92.6\mu s$, is one tenth of the control period for traditional SVM. In order to keep a fair comparison, the output performance with multi-sampling SVM (MS-SVM) is also presented, of which the control period of SVM and the sampling interval are $926\mu s$ and $92.6\mu s$ as well, meaning the PWM current reference vector is updated ten times during one control period of SVM. In this study, total demand distortion (TDD) is used as index to evaluate steady state performance of line current, stator current, torque, and DC current.

Table 5.1 SIMULATION PARAMETERS OF HIGH POWER CSC-FED MV IM DRIVE

System Ratings		System Parameters	
Rated power	1MW	filter reactor L_f	0.15pu
		DC chock L_{dc}	1pu
Rated line-to-line voltage	4160V	Rectifier side capacitor C_r	0.4pu
		Inverter side capacitor C_i	0.4pu
Rated line current	139A	Control period for SVM	926μs
		Sampling interval for MPSVPC	92.6μs
Induction Motor Ratings		Induction Motor Parameters	
Rated output power	1260hp	Stator resistance R_s	0.21Ω
Rated line-to-line voltage	4160V	Rotor resistance R_r	0.146Ω
Rated stator current	150A	Stator leakage inductance L_{ls}	5.2mH
Rated speed	1189rpm	Rotor leakage inductance L_{lr}	5.2mH
Rated torque	7490Nm	Magnetizing inductance L_m	155mH
Rated rotor flux linkage	8.35Wb	Moment of inertia J	$22\text{kg}\cdot\text{m}^2$

5.2.1 Steady State Performance

The quantified steady state performance of MS-SVM and MPSVPC under various operating conditions is listed in Table 5.2. Over the speed range given in the table, the switching frequency of MPSVPC can be fixed at 540Hz in steady state, which is the same as that of MS-SVM. At the

same time, the steady state performance of MPSVPC, in terms of the TDDs of the line currents, the stator currents, the DC current, and the torque, is also similar as that of MS-SVM. Table 5.2 verifies that since there is no huge discrepancy between line or stator current reference and real line or stator current, MPSVPC just follows the space vector pattern generated by SVM.

Table 5.2 SIMULATED STEADY STATE PERFORMANCE

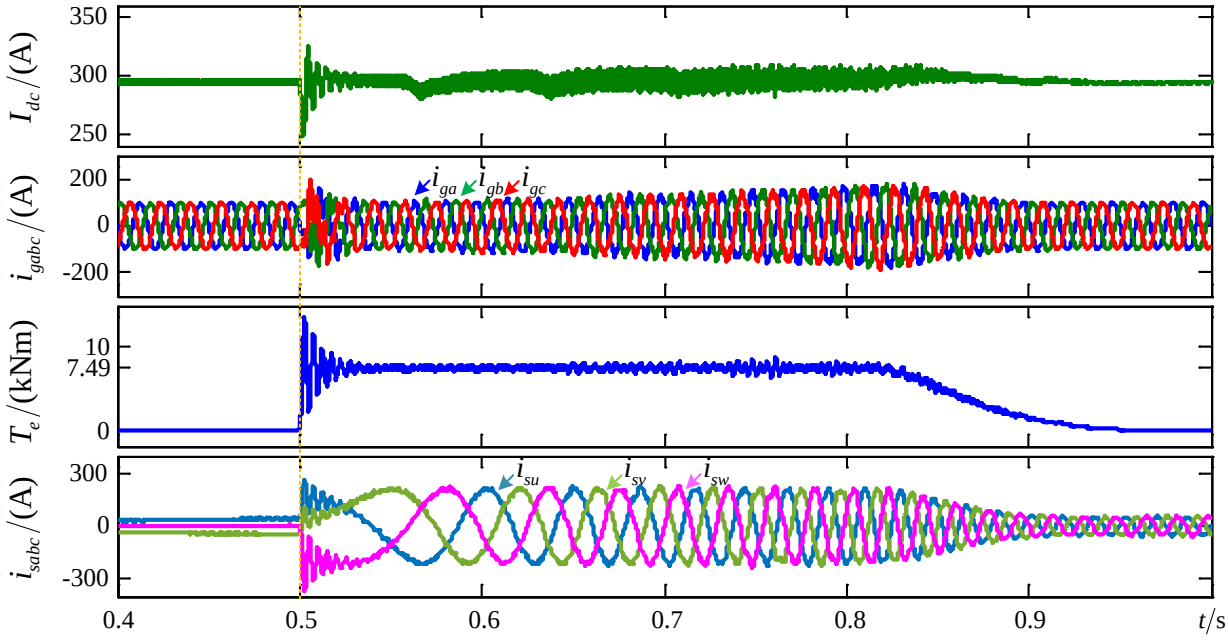
Rotor speed (rpm)	Load torque (pu)	Motor-side synchronous frequency (Hz)	Scheme	$\overline{f}_{sw}$ (Hz)		TDD (%)		TDD of DC current (%)	TDD of torque (%)
				CSR	CSI	CSR	CSI		
1189	0.8	60	MS-SVM	540	540	6.83	3.01	1.85	3.55
			MPSVPC	540	540	5.50	3.00	1.68	3.57
599	0.8	30.3	MS-SVM	540	540	6.02	6.92	3.65	7.69
			MPSVPC	540	540	5.54	7.14	3.65	7.53
180	0.8	9.44	MS-SVM	540	540	1.35	3.22	2.10	3.66
			MPSVPC	540	540	1.35	3.32	2.10	3.65

5.2.2 Dynamic Performance

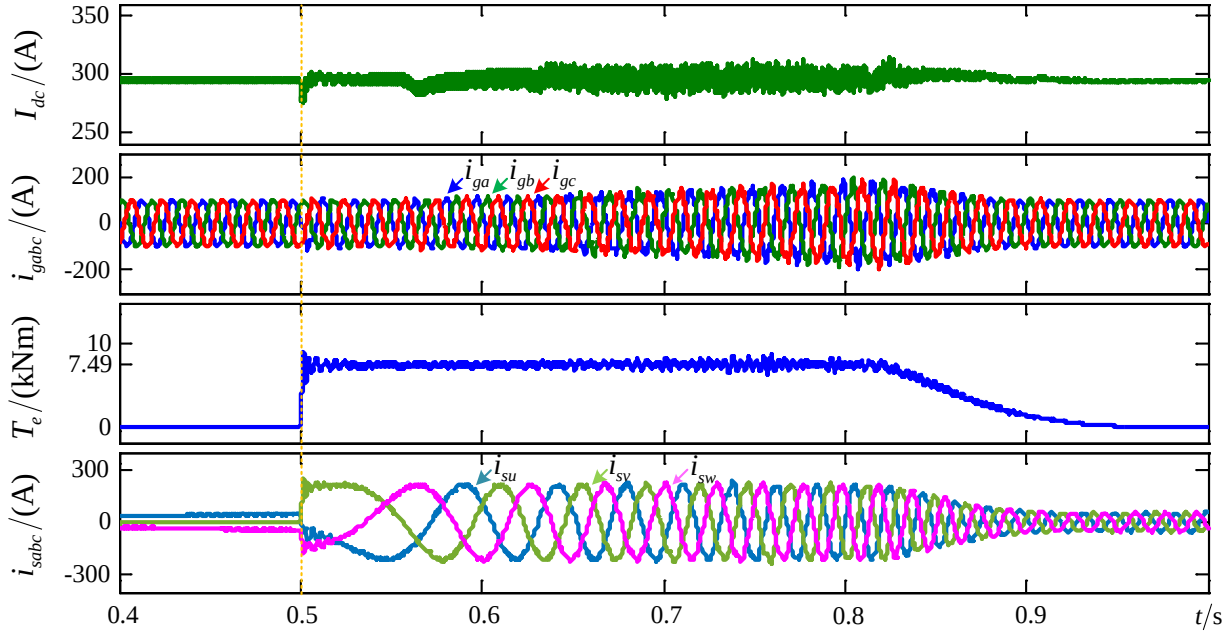
As mentioned above, due to the impact of *LC* resonance at both CSR and CSI sides, huge discrepancy between line or stator current reference and real line or stator current more probably appears during transient process, during which space vector pattern would be governed through MPC approach to improve dynamic performance. Two transient cases are investigated in this paper, namely start-up process and speed reverse process.

Fig. 5.5 illustrates the whole start-up process of two schemes. From top to bottom, the DC current, three-phase line currents, torque, and three-phase stator currents of two schemes are presented. As Fig. 5.5 shows, before time *t* of 0.5s, the IM is in stand-still status. At time *t* of 0.5s, the rotor speed reference jumps to its rated value, which is 1189rpm in this case. The output of the rotor speed controller is limited between positive and negative rated torque, that is 7490Nm. When the torque stepped from 0 to its rated value, resonance appears in both line and stator currents with MS-SVM, which also introduces large overshoot and oscillation into the DC current and the torque, as Fig. 5.5 (a) shows. By contrast, with MPSVPC, it can be observed that resonance in the line and stator currents is mitigated when the output torque is suddenly changed, therefore the overshoot and oscillation in the DC current and the torque are also reduced and

weakened. It can also be found that except a short period of time after the torque step change, there is no obvious difference between the output performance of MS-SVM and MPSVPC.



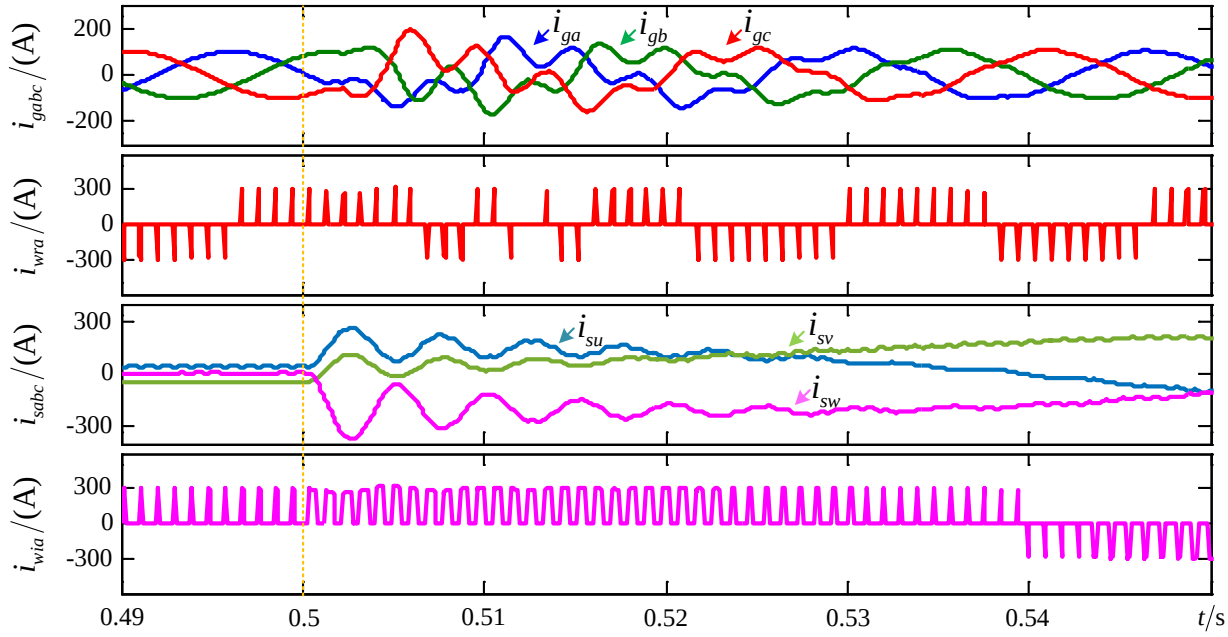
(a)



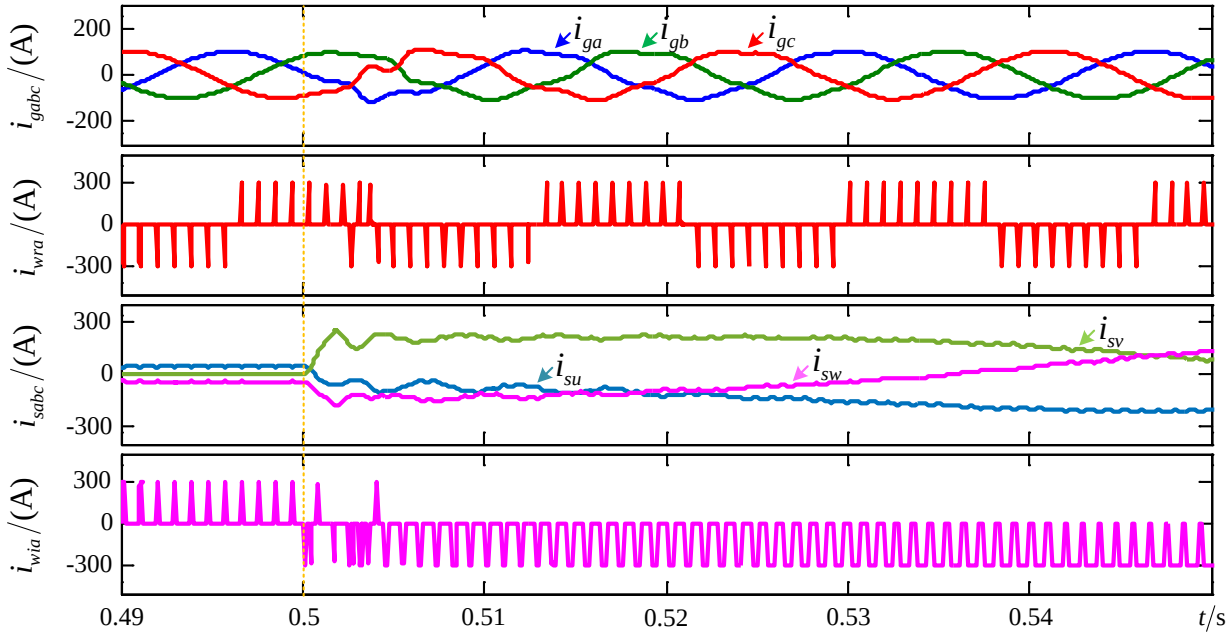
(b)

Fig. 5.5 Diagram of simulated whole start-up process: (a) MS-SVM and (b) MPSVPC.

Fig. 5.6 provides a much closer look at the transient process after the torque step happens. The three-phase line currents, phase A input current of the CSR, three-phase stator currents, and phase U output current of the CSI. As shown in Fig. 5.6 (a), after time *t* of 0.5s, severe resonance appears in both line currents and stator currents due to the sudden change of the torque. The resonance is gradually attenuated until time *t* of 0.53s. On the other hand, with MPSVPC, resonance in the line currents and stator currents is restrained from the starting point of the start-up process. The reason is that when the torque is suddenly changed from 0 to the rated value, due to the limitation on dynamic performance imposed by MS-SVM, the discrepancy between the estimated line or stator current references at future sampling points and the predicted line or stator currents based on space vector pattern of SVM, becomes larger. When the difference is higher than the pre-defined criteria value, input or output current at the CSR or CSI side will be governed through MPC approach, which can be verified from Fig. 5.6 according to that the phase A input current of the CSR and the phase U output current of the CSI with MPSVPC are different from those with MS-SVM after time *t* of 0.5s. With the resonance during the transient process attenuated, the difference between the estimated current references and the predicted currents becomes smaller. When the difference drops into the range set by the criteria, the input currents of the CSR and the output currents of the CSI return to follow the space vector pattern set by SVM again. As Fig. 5.6 (b) shows, after time *t* of 0.53, MPSVPC generates the same PWM current pattern as that with traditional MPC.



(a)

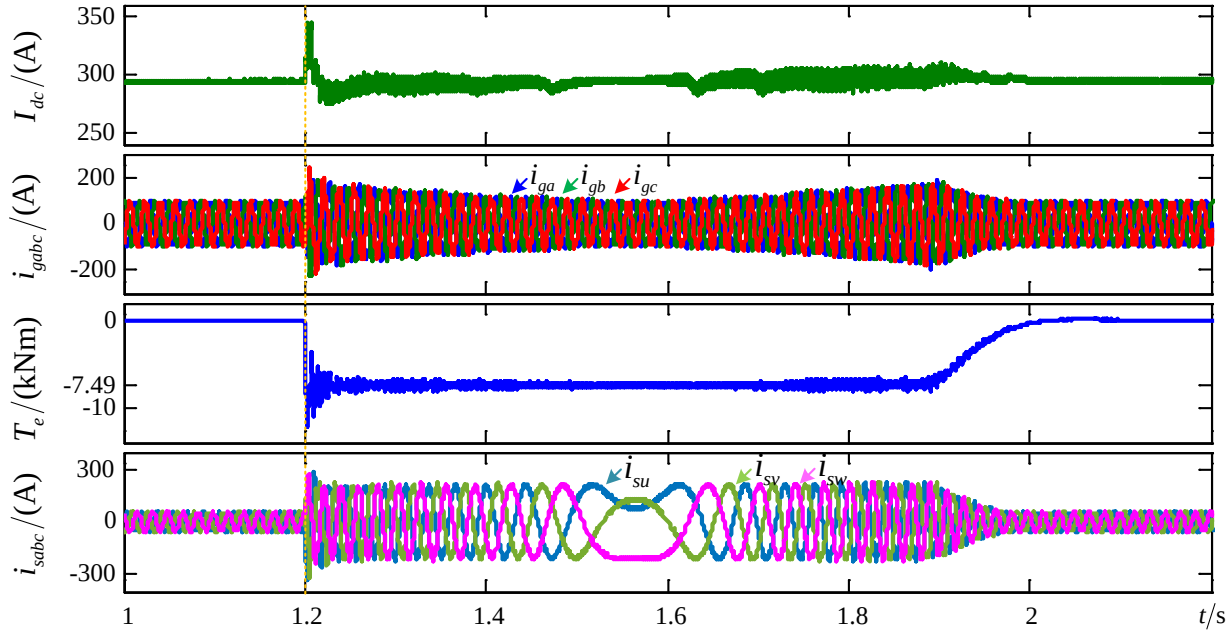


(b)

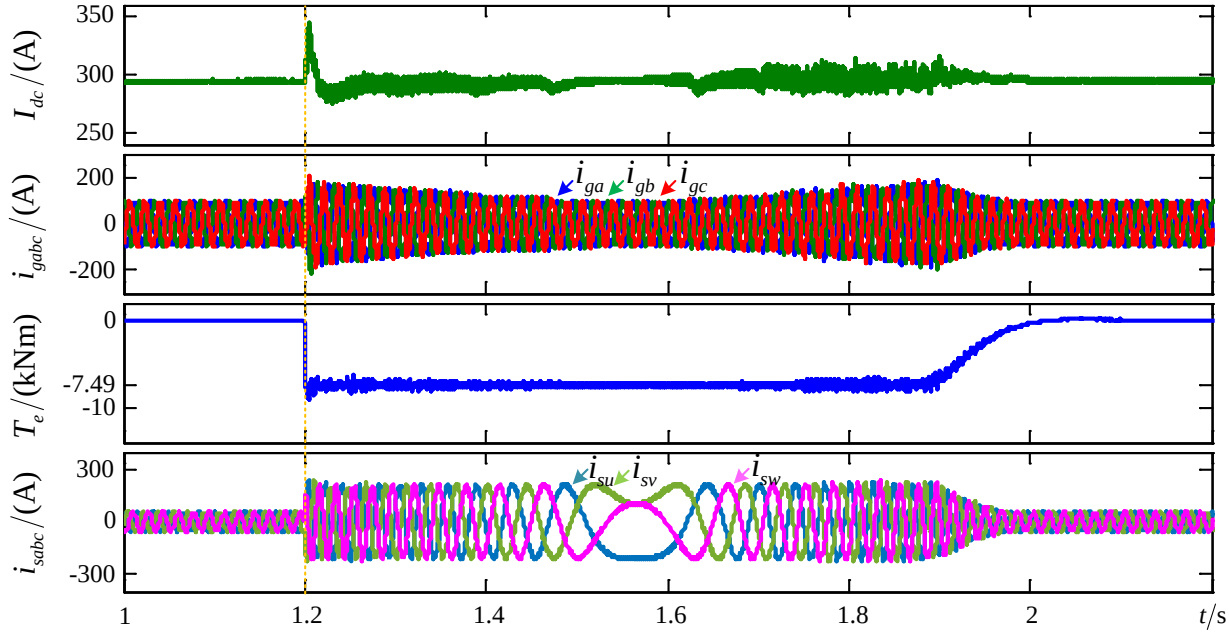
Fig. 5.6 Diagram of beginning part of simulated start-up process: (a) MS-SVM and (b) MPSVPC.

In order to further verify the effectiveness of MPSVPC, speed reverse process is also presented, as Fig. 5.7 shows. At time *t* of 1.2s, the rotor speed reference jumps from the positive

rated value to the negative rated value. Fig. 5.7 (a) shows the speed reverse process with MS-SVM, in which *LC* resonance appears in the line currents and the stator currents right after the speed reverse process begins, and results in the overshoots and oscillation in the DC current and the torque. On the other hand, with MPSVPC, when the torque steps to the negative rated value, the severity of the resonance in the line currents and stator currents is weakened, and the overshoot and oscillation in the torque is effectively mitigated. Though the overshoot in the DC current is close to that with traditional SVM, the variation of the DC current is smoother than that with traditional SVM.



(a)

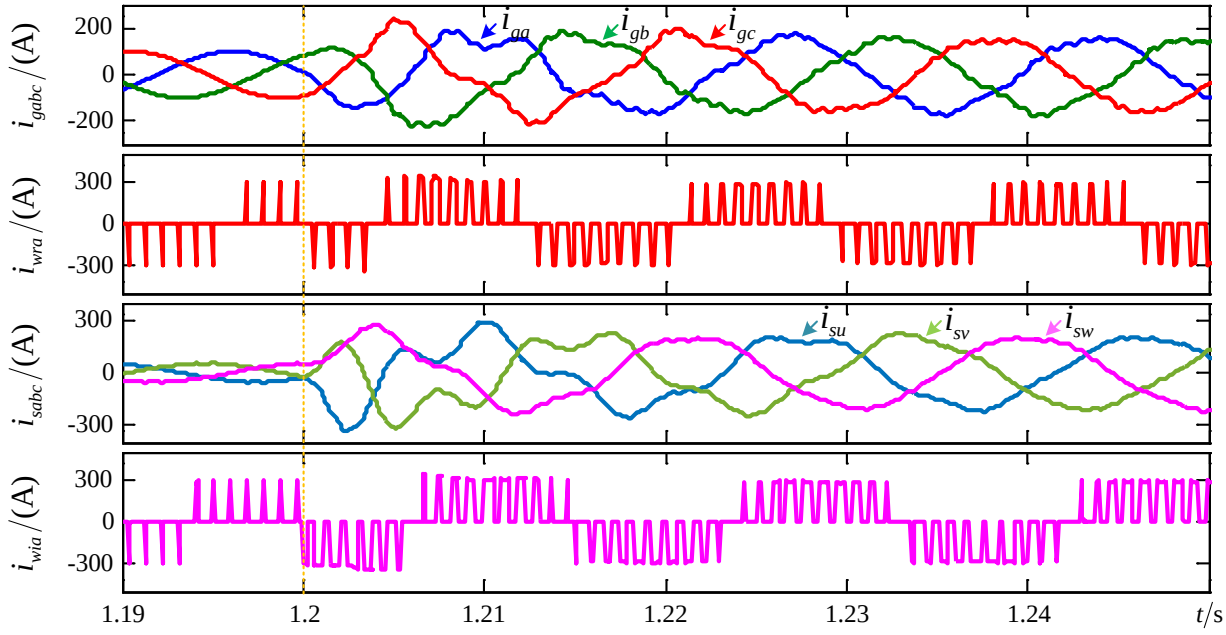


(b)

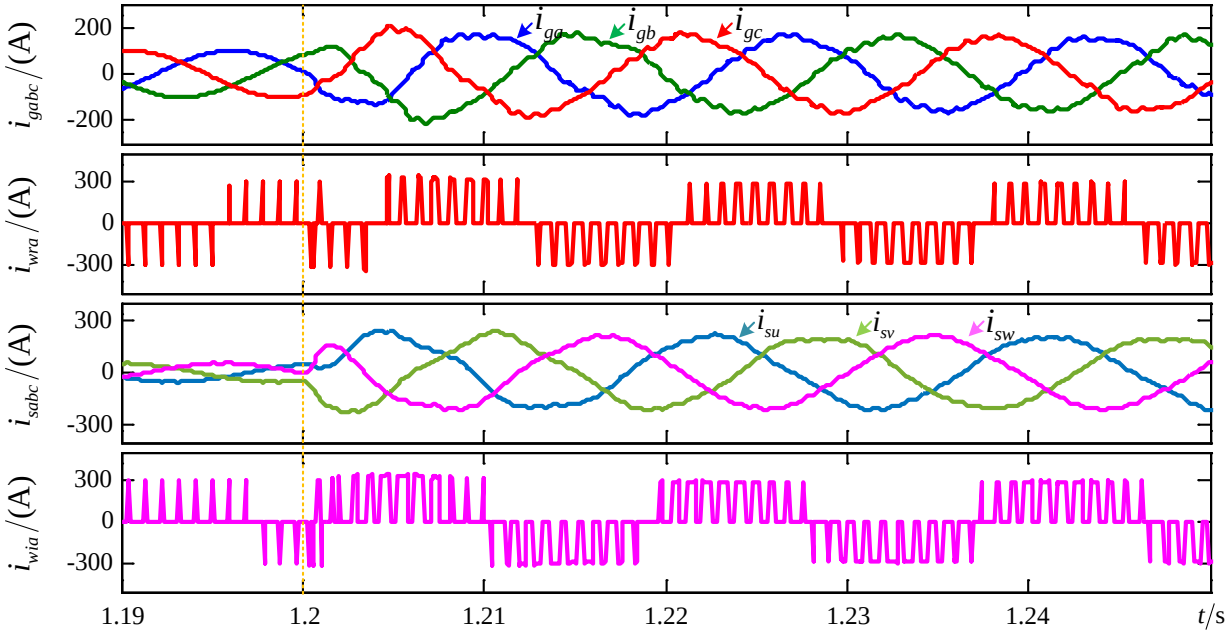
Fig. 5.7 Diagram of whole simulated speed reverse process: (a) MS-SVM and (b) MPSVPC.

Fig. 5.8 shows the details on the beginning of the speed reverse process. When MS-SVM is used, *LC* resonance is stimulated in the line currents and the stator currents after the torque is suddenly changed to the negative rated value. By contrast, since the input currents of the CSR

and the output currents of the CSI with MPSVPC are governed through MPC approach after the speed reverse process starts, the resonance in the line currents and stator currents is effectively suppressed, as Fig. 5.8 (b) depicts. With the resonance gradually mitigated, the CSR-side input currents and the CSI-side output currents return to follow the space vector pattern determined by SVM after time *t* of 1.22s, which fixes the switching frequencies at both CSR and CSI sides.



(a)



(b)

Fig. 5.8 Diagram of beginning part of simulated speed reverse process: (a) traditional SVM and (b) MPSVPC.

5.3 Experimental Validation

The experiments on a low power prototype (5kW/208V/13.9A) are conducted to further validate the effectiveness of MPSVPC as well. The parameters of the low power prototype are given in Table 5.3. The control period of SVM is still selected as 926μs. For contrast, the steady state and dynamic performance with traditional SVM are also presented. The sampling intervals of MS-SVM and MPSVPC are both 92.6μs as well.

Table 5.3 EXPERIMENTAL PARAMETERS OF LOW POWER PROTOTYPE

System Ratings		System Parameters	
Rated power	5kW	filter reactor L_f	0.22p.u.
		DC chock L_{dc}	1.16p.u.
Rated line-to-line voltage	208V	Rectifier side capacitor C_r	0.378p.u.
		Inverter side capacitor C_i	0.378p.u.
Rated line current	13.9A	Control period for SVM	926μs
		Sampling interval for MPSVPC	92.6μs
Induction Motor Ratings		Induction Motor Parameters	
Rated output power	5hp	Stator resistance R_s	0.395Ω
Rated line-to-line voltage	208V	Rotor resistance R_r	0.737Ω
Rated stator current	13.9A	Stator leakage inductance L_{ls}	1.95mH
Rated speed	1700rpm	Rotor leakage inductance L_{lr}	49.1mH
Rated torque	21Nm	Magnetizing inductance L_m	49.1mH
Rated rotor flux linkage	0.433Wb	Moment of inertia J	$0.103\text{kg}\cdot\text{m}^2$

5.3.1 Steady State Performance

Fig. 5.9 shows the experimental steady state performance at rated rotating speed and 0.8pu load torque condition. From top to bottom, the phase A line current, the phase A input PWM current of the CSR, the phase U stator current, and the phase U output PWM current of the CSI are presented. It can be found that the steady state performance with MPSVPC is close to that with MS-SVM no matter in terms of the TDDs of line current and stator current or average switching frequencies. The main difference between the steady state performance of MS-SVM and MPSVPC focuses on the input PWM current waveform and the average switching frequency of the CSR. It can be observed that one more switching action is added into the input PWM current waveform of the CSR with MPSVPC, which makes the average switching

frequency of the CSR be equal to 570Hz, not 540Hz as that with MS-SVM. The reason is that at rated rotating speed and 0.8pu load torque condition the difference between the estimated line current references and the predicted line currents following the space vector pattern set by MS-SVM is more easy to surpass the predefined maximum criteria value due to the higher magnitude of the line current.

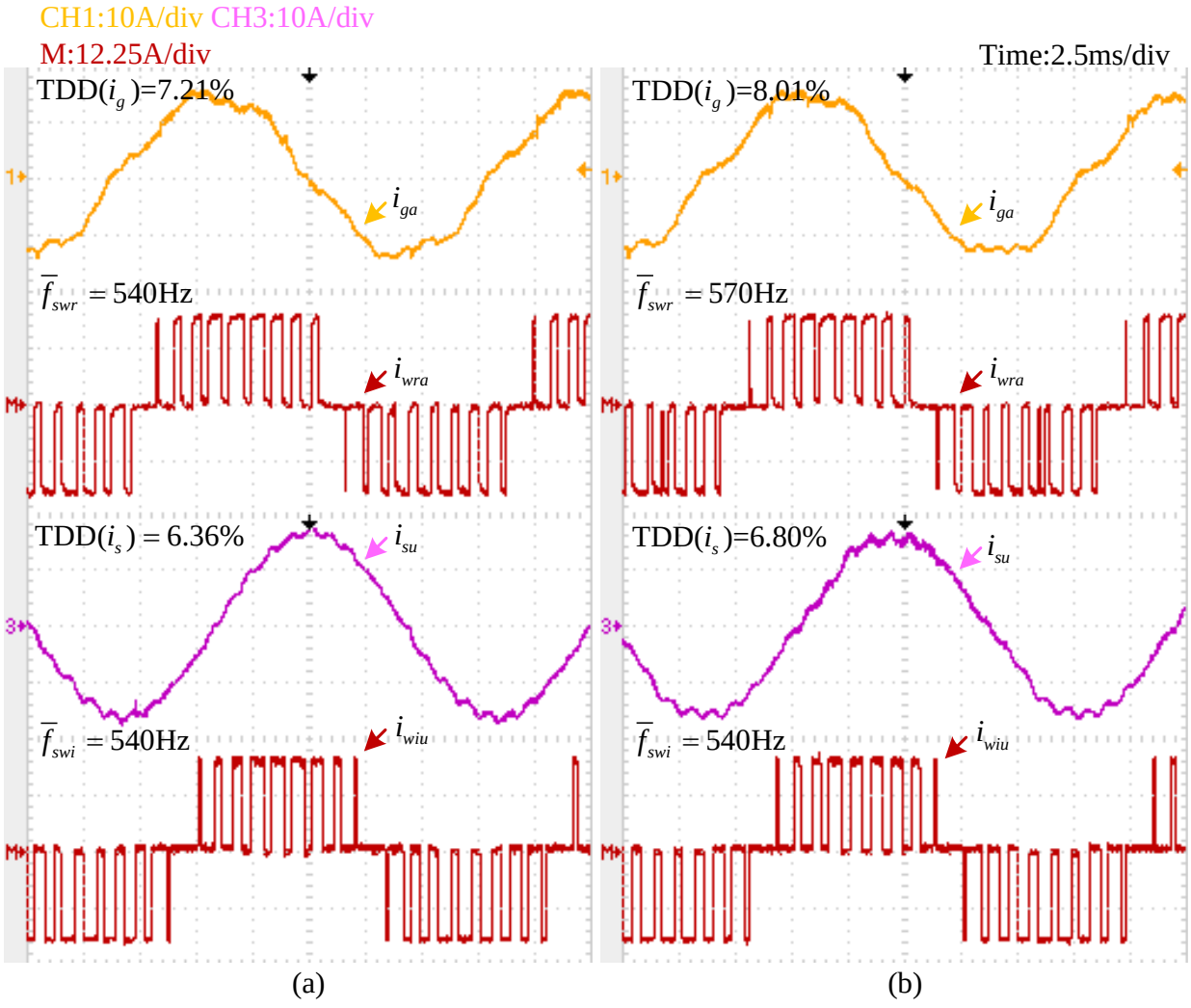


Fig. 5.9 Diagram of experimental steady state performance at rated rotating speed and 0.8pu load torque: (a) MS-SVM and (b) MPSVPC.

Table 5.4 illustrates a quantitative comparison of the experimental steady state performance between MS-SVM and MPSVPC at various operating conditions. Similar as the results shown in Table 5.4, the steady state output performance of MPSVPC is close to that of MS-SVM, which

is indicated by the TDD values of the line current, the stator current, the DC current, and the torque, and means that MPSVPC can generate a SVM-like PWM waveform with fixed switching frequency in steady state. However, in contrast to the values listed in Table 5.2, the TDD values in Table 5.4 are obviously higher, especially the TDDs of the line current and the DC current. The reason is that the utility power supply voltages in the experiments are not as ideally sinusoidal as that in simulation, and contain low-order harmonics, which further distort the line currents, and increase the fluctuation of the DC current through stimulating *LC* resonance at the CSR side.

Table 5.4 EXPERIMENTAL STEADY STATE PERFORMANCE

Rotor speed (rpm)	Load torque (pu)	Motor-side synchronous frequency (Hz)	Scheme	$\overline{f}_{sw}$ (Hz)		TDD (%)		TDD of DC current (%)	TDD of torque (%)
				CSR	CSI	CSR	CSI		
1700	0.8	60	MS-SVM	540	540	7.21	6.36	11.6	10.2
			MPSVPC	570	540	8.01	6.80	9.12	10.4
850	0.8	31.5	MS-SVM	540	540	4.13	5.96	6.41	9.22
			MPSVPC	540	540	4.26	6.38	5.34	9.71
180	0.8	9.5	MS-SVM	540	540	4.44	6.38	5.73	9.93
			MPSVPC	540	540	4.56	6.71	5.19	9.68

5.3.2 Dynamic Performance

In order to demonstrate the improvements on dynamic performance with MPSVPC, the start-up process and the speed reverse process are experimentally conducted. Fig. 5.10 shows the whole start-up process, in which the DC current, the phase A line current, the torque, and the phase U stator current are depicted from top to bottom. The output of the rotor speed controller is limited between positive and negative rated torque. It can be observed that with MS-SVM, significant overshoots appear in both DC current and torque at the beginning of the start-up process due to the degraded dynamic performance of traditional SVM and transient *LC* resonance. On the other hand, with MPSVPC, the overshoots in the DC current and the torque are effectively mitigated, and the fluctuation on the DC current is also reduced at the same time.

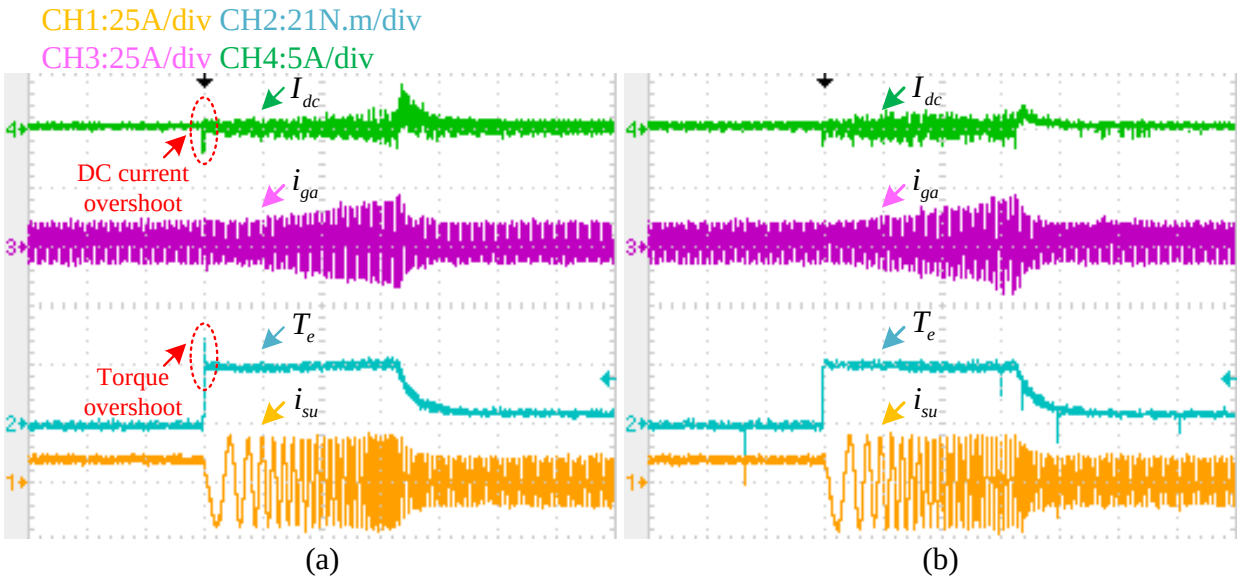
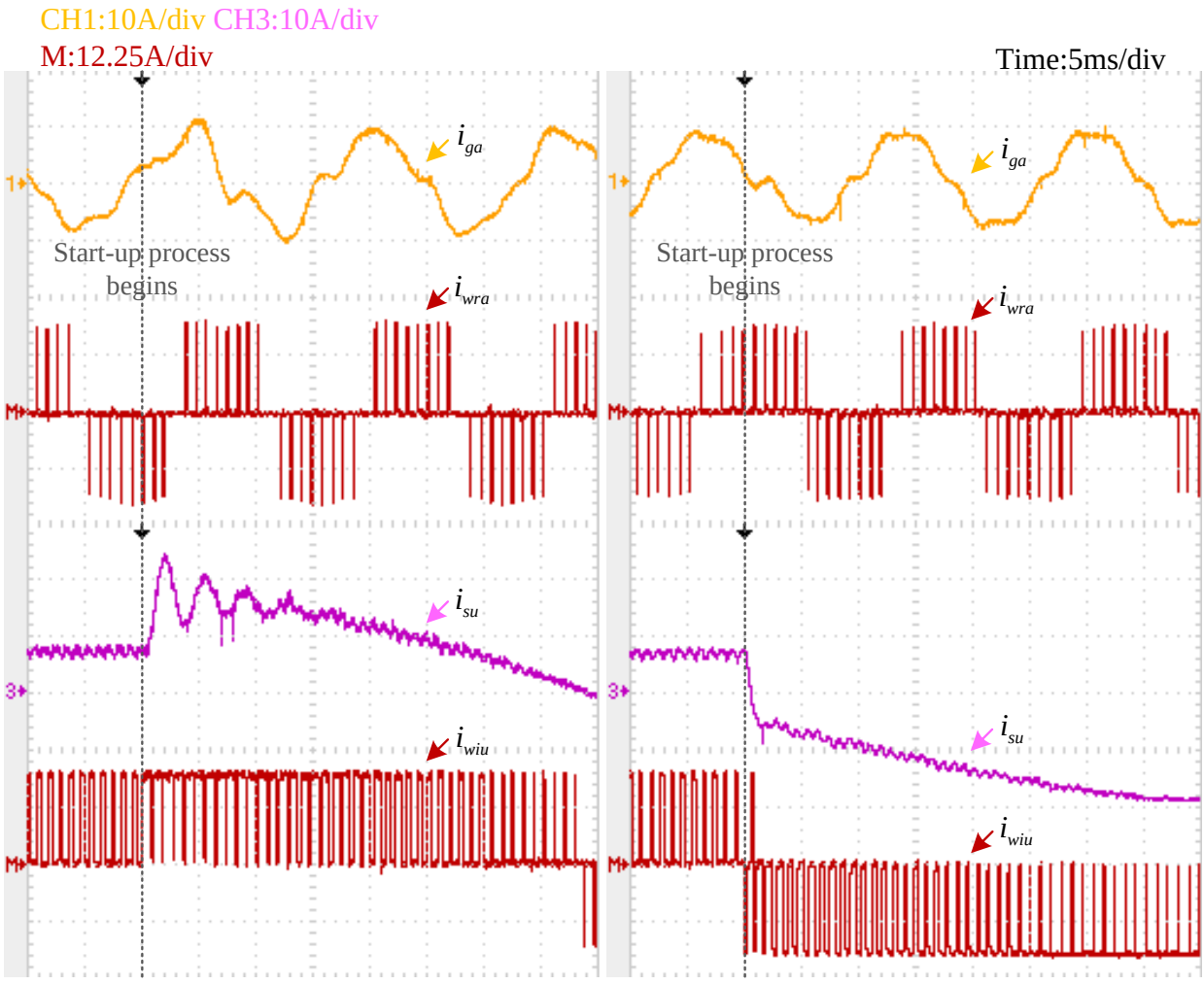


Fig. 5.10 Diagram of whole experimental start-up process: (a) MS-SVM and (b) MPSVPC.

Fig. 5.11 shows the very beginning part of the start-up process, where the phase A line current, the phase A input current of the CSR, the phase U stator current, and the phase U output current of the CSI are presented. In Fig. 5.11 (b), with MPSVPC, due to the difference between the estimated line current or stator current reference and the predicted line or stator current regulated by SVM higher than the maximum criteria, the switching patterns at both CSR and CSI sides are governed through MPC approach during a short period after the start of the start-up process, which can be verified by the rearranged PWM waveforms in contrast to that with MS-SVM, which are shown in Fig. 5.11 (a). Due to the PWM patterns regulated by MPC approach manipulating the line currents and the stator currents to follow their respective references more closely, better dynamic performance is achieved with MPSVPC, which can be validated by the mitigated resonance in the line current and the stator current after the start-up process begins. It can also be found that after a short period of time, the PWM waveforms with MPSVPC return to follow a SVM-defined pattern, which means that the calculated difference drops back into the ranges limited by the maximum criteria.



(a) (b)

Fig. 5.11 Diagram of beginning part of experimental start-up process: (a) MS-SVM and (b) MPSVPC.

Fig. 5.12 shows the whole experimental speed reverse process. In comparison with the results shown in Fig. 5.12 (a), MPSVPC can effectively mitigate the torque overshoot. Though the DC current overshoot is not obviously restrained by MPSVPC, the fluctuation on the DC current during the whole speed reverse process is reduced in contrast to that with MS-SVM.

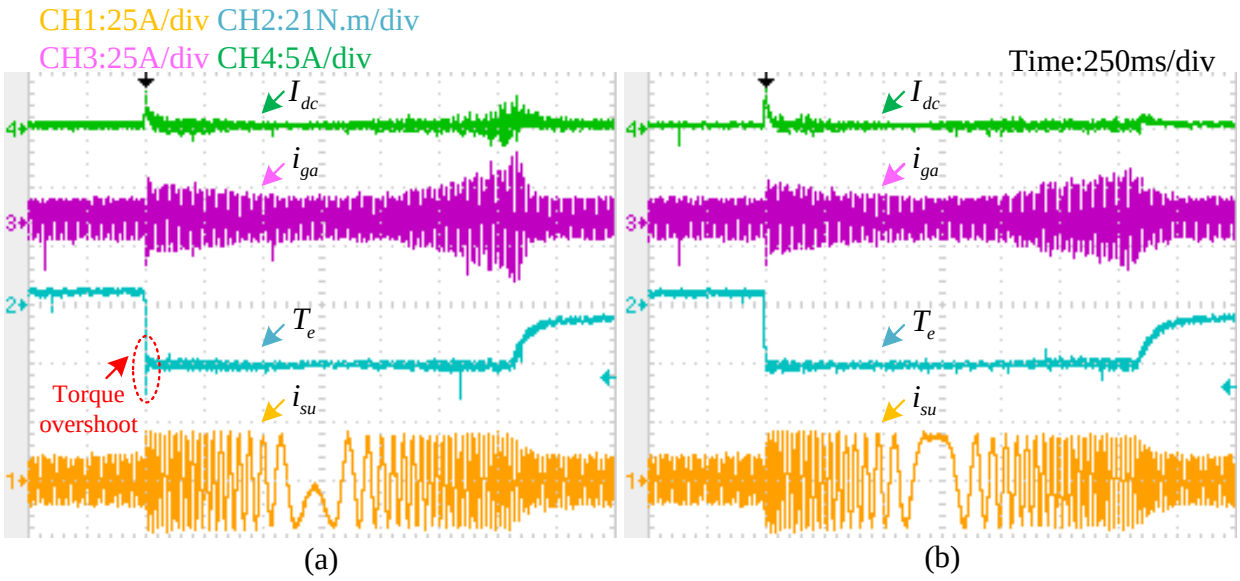


Fig. 5.12 Diagram of whole experimental speed reverse process: (a) MS-SVM and (b) MPSVPC.

Fig. 5.13 shows the beginning part of the experimental speed reverse process. As Fig. 5.13 (a) shows, after the beginning point of the speed reverse process, severe resonance appears in the line current and the stator current with MS-SVM. In Fig. 5.13 (b), with MPSVPC, during a short period after the beginning point of the speed reverse process, both line current and stator current are regulated by MPC approach, which can also be observed from the different PWM waveform patterns from that with traditional SVM, and the resonance in the line current and the stator current after the beginning of speed reverse process is effectively suppressed, which further verifies the effectiveness of MPSVPC on improving dynamic performance. After one fundamental period, which corresponds to 1/60s in this case, the PWM current waveforms return to follow the space vector pattern set by SVM again, which is just similar to the result shown in Fig. 5.8.

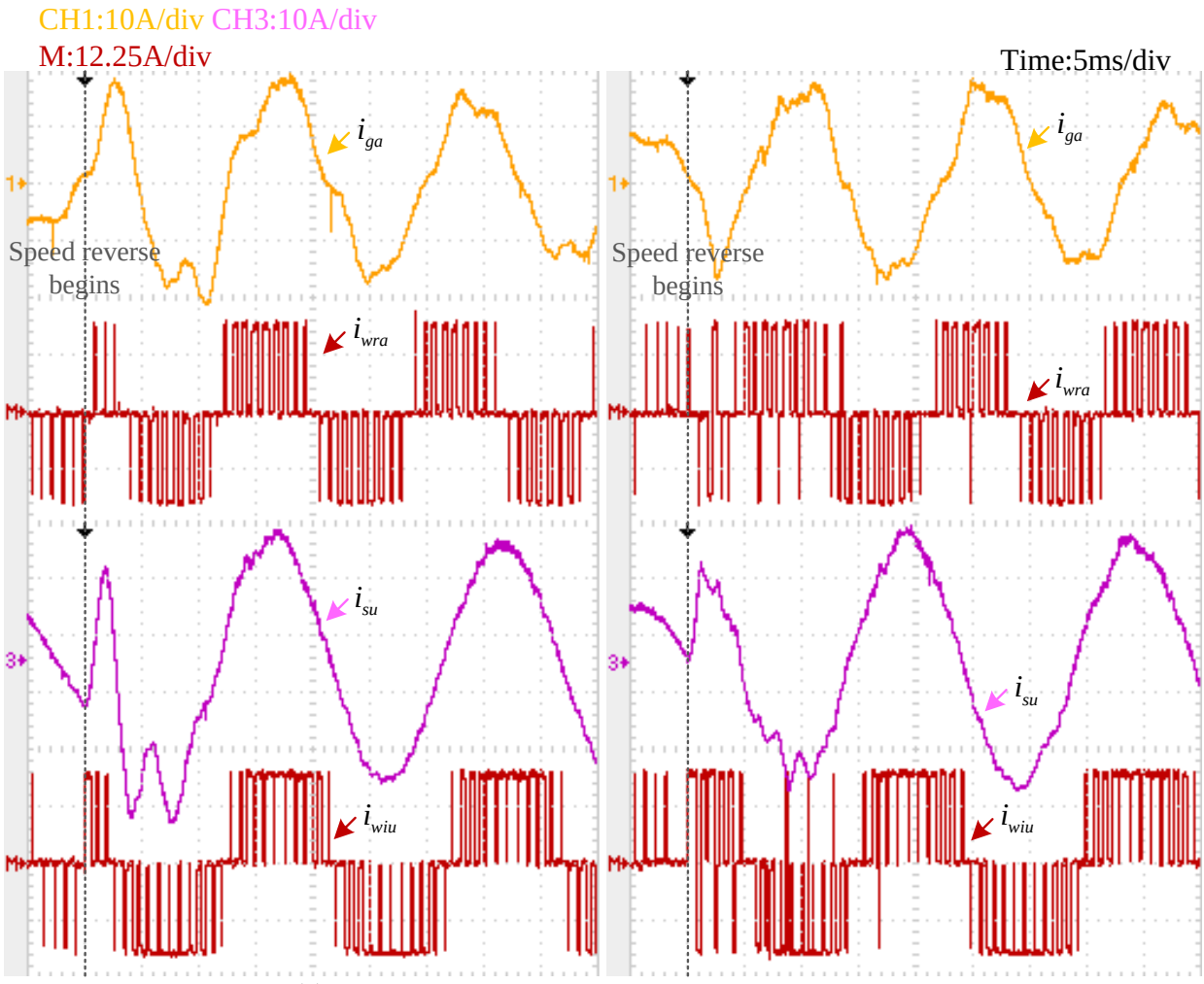


Fig. 5.13 Diagram of beginning part of experimental speed reverse process: (a) MS-SVM and (b) MPSVPC.

5.4 Conclusions

MPSVPC is presented in this chapter. In comparison with MS-SVM and the existing MPCs with relatively low switching frequency, the advantages of MPSVPC can be classified as follows

- In contrast to MS-SVM, MPSVPC can improve dynamic performance of high power CSC-fed MV IM drive, and keeps fixed switching at both CSR and CSI sides in steady state;

- In comparison with SHE-PWM or other SHE-PWM based schemes, there is no need to calculate optimal switching angles of SHE-PWM waveform in MPSVPC, which is totally an online method;
- Compared to the existing MPCs achieving low switching frequency, MPSVPC not only requires just one step prediction, but also does not include the weighting factor selection issue, which reaches a simpler structure and the reduction on computation effort.

6 Common-Mode Voltage Reduced Model Predictive Control for High Power Current-Source Converter-Fed Medium-Voltage Induction Motor Drive

In this Chapter, common-mode voltage reduced model predictive control (RCMV-MPC) is proposed for high power CSC-fed MV IM drives, which is illustrated in Fig. 6.1 again. The inherent feature of MPC, that is involving nonlinear constraints into control design, is used to realize CMV mitigation. The innovation in the proposed RCMV-MPC can be classified as

- Since the control objective of RCMV-MPC is the CMV reduction in a whole CSC-fed IM drive, optimal switching states for CSR and CSI are selected synchronously during every sampling interval, for which a unified cost function is established to track references for both CSR and CSI, simultaneously;
- During every sampling interval, only switching states fulfilling a pre-defined CMV limitation become candidates, from which optimal ones are finally selected to track references for both CSR and CSI. Moreover, a CMV related term is associated into the unified cost function to further reduce the CMV peak value in a CSC-fed IM drive.

In comparison with the existing RCMV-SVMs, which are introduced in Chapter 0, the merits provided by RCMV-MPC can be summarized as

- First, unlike traditional RCMV-SVMs, the limitation of CMV peak value is clearly defined in RCMV-MPC;
- Then, with RCMV-MPC, the CMV peak value can be further reduced in contrast to that by traditional RCMV-SVMs, but the average switching frequency of RCMV-MPC can still be kept around 1kHz;
- Last but not least, due to a relatively short sampling interval, the CMV mitigation effect during transients can also be guaranteed with RCMV-MPC.

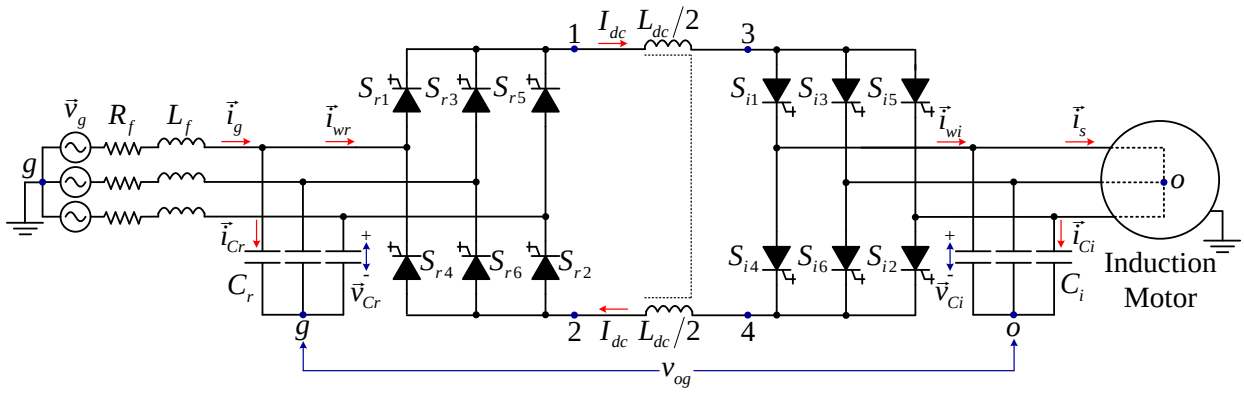


Fig. 6.1 Configuration of high power CSC-fed MV IM drive.

6.1 CMV in CSC-Fed IM Drives

6.1.1 CMV Definition in CSC-Fed IM Drives

As Fig. 6.1 shows, the CMV produced in a CSC-fed IM drive, consists of the CMV at the CSR side, v_{cmr}, and the CMV at the CSI side, v_{cmi}, which can be defined, respectively, by

$$v_{cmr} = \left(v_{1g} + v_{2g}\right)/2 \tag{6.1}$$

$$v_{cmi} = \left(v_{3o} + v_{4o}\right)/2 \tag{6.2}$$

where v_{1g} and v_{2g} are the voltages at point 1 and 2, with respect to the ground or the neutral of the rectifier-side three-phase capacitor; v_{3o} and v_{4o} are the voltages at point 3 and 4, with respect to the neutral of the IM stator windings or the neutral of the inverter-side capacitor.

If the differential inductance in the positive DC link is equal to that in the negative DC link, the CMV in a whole CSC-fed IM drive, v_{og}, can be expressed as [23]

$$v_{og} = v_{cmr} - v_{cmi} \tag{6.3}$$

It is important to note that the subtraction operation in (6.3) does not imply a reduction of the CMV in a whole CSC-fed IM drive. Since the CMV is bipolar, the maximum CMV in a whole CSC-fed IM drive is possibly higher than those at the CSR and the CSI sides. If PWM control is applied to CSC-fed IM drives, the CMV can be expressed as

$$v_{og} = v_{cmr} - v_{cmi} = \frac{\begin{bmatrix} S_{r1}+S_{r4} & S_{r3}+S_{r6} & S_{r2}+S_{r5} \end{bmatrix}}{2} \cdot \begin{bmatrix} v_{Cra} \\ v_{Crb} \\ v_{Crc} \end{bmatrix} - \frac{\begin{bmatrix} S_{i1}+S_{i4} & S_{i3}+S_{i6} & S_{i2}+S_{i5} \end{bmatrix}}{2} \cdot \begin{bmatrix} v_{Cia} \\ v_{Cib} \\ v_{Cic} \end{bmatrix} \tag{6.4}$$

where S_{r1} to S_{r6} are the switching functions of CSR; S_{i1} to S_{i6} are the switching functions of CSI; v_{Cra}, v_{Crb}, and v_{Crc} are the rectifier-side capacitor phase voltages; v_{Cia}, v_{Cib}, and v_{Cic} are the inverter-side capacitor phase voltages.

Fig. 6.2 shows the definitions of the space vectors in a CSC, and the instantaneous CMVs associated with the space vectors are also indicated in Fig. 6.2, where v_{Ca}, v_{Cb}, and v_{Cc} represent instantaneous capacitor phase voltages at CSR or CSI side. The maximum CMV peak value is produced by zero-state vectors, which can be as high as the peak values of capacitor phase voltages. According to the principle of zero-state vector selection based RCMV-SVM in [39], due to the redundancy of zero-state vectors, there is always one zero-state vector generating CMV no higher than half peak value of capacitor phase voltage at any instant. Hence, the zero-state vector with the lowest CMV absolute value can be selected to ensure that the CMV peak value is not higher than half peak value of capacitor phase voltage, either. Moreover, since zero-state vector is not avoided in zero-state vector selection based RCMV-SVM, there is no influence on the output performance of the modulation. Hence, it is possible that the CMV peak value in a whole CSC-fed IM drive is reduced to no larger than $0.5(V_{Cr}+V_{Ci})$, where V_{Cr} and V_{Ci} are the magnitudes of CSR and CSI-side capacitor phase voltages, without the tradeoff between output performance and CMV mitigation. $0.5(V_{Cr}+V_{Ci})$ will also be used as a CMV peak value limitation in RCMV-MPC.

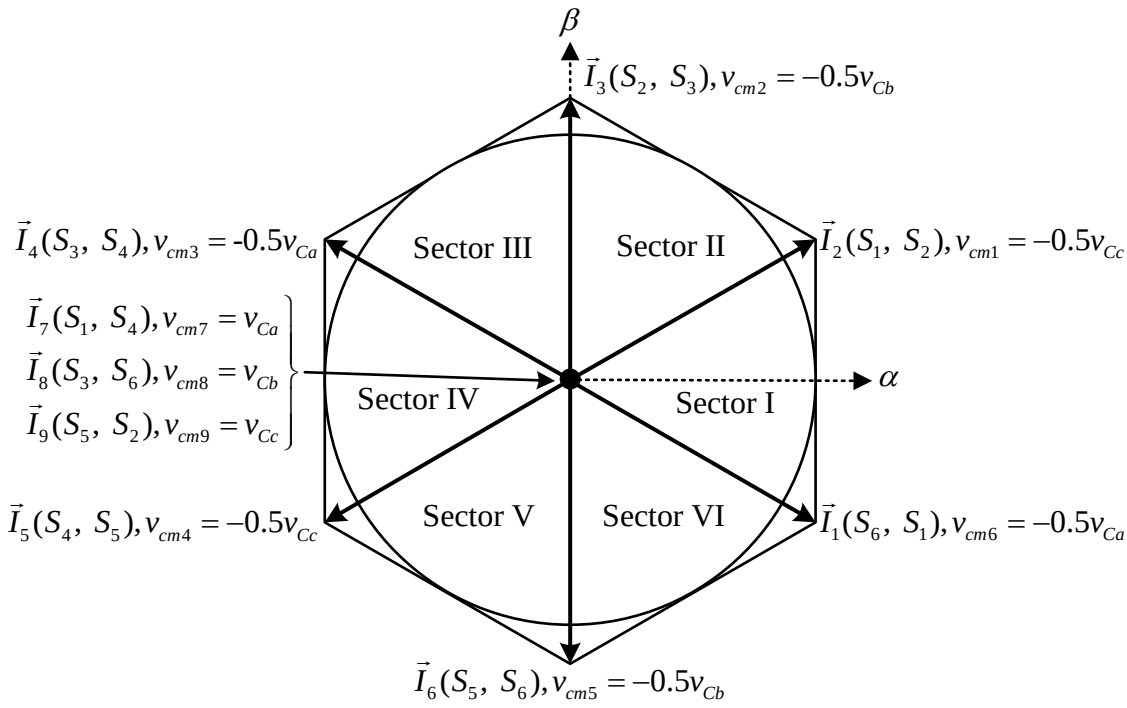


Fig. 6.2 Space vector definition and corresponding CMV of a CSC.

6.1.2 Principle of CMV Reduction in RCMV-MPC

(6.4) shows the relationship between instantaneous CMV in a CSC-fed IM drive and capacitor phase voltages. Hence, at every instant, CMV corresponding to every possible switching states' combination of CSR and CSI can be predicted. Due to a relatively short sampling interval, capacitor voltages can be considered constant during one sampling interval. For example, at *k*th sampling instant, CMVs at CSR and CSI sides can be given by

$$v_{cmr}(k) = \frac{\left[S_{r1}(k)+S_{r4}(k),\quad S_{r3}(k)+S_{r6}(k),\quad S_{r5}(k)+S_{r2}(k)\right]}{2}\begin{bmatrix} v_{Cra}(k) \\ v_{Crb}(k) \\ v_{Crc}(k) \end{bmatrix} \tag{6.5}$$

$$v_{cmi}(k) = \frac{\left[S_{i1}(k)+S_{i4}(k),\quad S_{i3}(k)+S_{i6}(k),\quad S_{i5}(k)+S_{i2}(k)\right]}{2}\begin{bmatrix} v_{Cia}(k) \\ v_{Cib}(k) \\ v_{Cic}(k) \end{bmatrix} \tag{6.6}$$

where $S_{r1}(k)$ to $S_{r6}(k)$ are the switching states of CSR at *k*th sampling instant; $S_{i1}(k)$ to $S_{i6}(k)$ are the switching states of CSI at *k*th sampling instant; $v_{Cra}(k)$, $v_{Crb}(k)$, and $v_{Crc}(k)$ are the

CSR-side capacitor phase voltages at *k*th sampling instant; $v_{Cia}(k)$, $v_{Cib}(k)$, and $v_{Cic}(k)$ are the CSI-side capacitor phase voltages at *k*th sampling instant. Then, the CMV of a whole CSC-fed IM drive can be estimated as

$$v_{og}(k) = v_{cmr}(k) - v_{cmi}(k) \tag{6.7}$$

Since the CMV in a CSC-fed IM drive can be estimated, the switching states of CSR and CSI can be optimally selected synchronously to reduce CMV peak value. Fig. 6.3 shows the principle of RCMV-MPC, in comparison with traditional zero-state vector selection based RCMV-SVM. As Fig. 6.3 (a) shows, zero-state vectors are independently selected in CSR and CSI, which only ensures that the CSR- and CSI-side CMVs are no larger than half peak values of respective capacitor phase voltages, and the absolute CMV value in a whole CSC-fed IM drive does not exceed $0.5(V_{Cr}+V_{Ci})$. However, due to the fixed sequence in SVM, it becomes hard to further mitigate the CMV peak value. Fig. 6.3 (b) shows the CMV mitigation process in RCMV-MPC. Since there is no restrictions introduced by modulating stage any more, the optimal space vectors need to be selected for CSR and CSI during every sampling interval. The primary control goal is still to track respective references for CSR and CSI. If the applied space vector for CSR and CSI can be selected synchronously, the CMV mitigation constraint can be considered during the selection of the optimal switching states for CSR and CSI, which provides the possibility of further mitigating the CMV peak value. In order to make sure that the CMV in a CSC-fed IM drive is restricted inside a predefined range, the CMV peak value limitation at *k*th sampling instant can be given by

$$V_{og}^{\lim}(k) = 0.5\left(V_{Cr}(k) + V_{Ci}(k)\right) \tag{6.8}$$

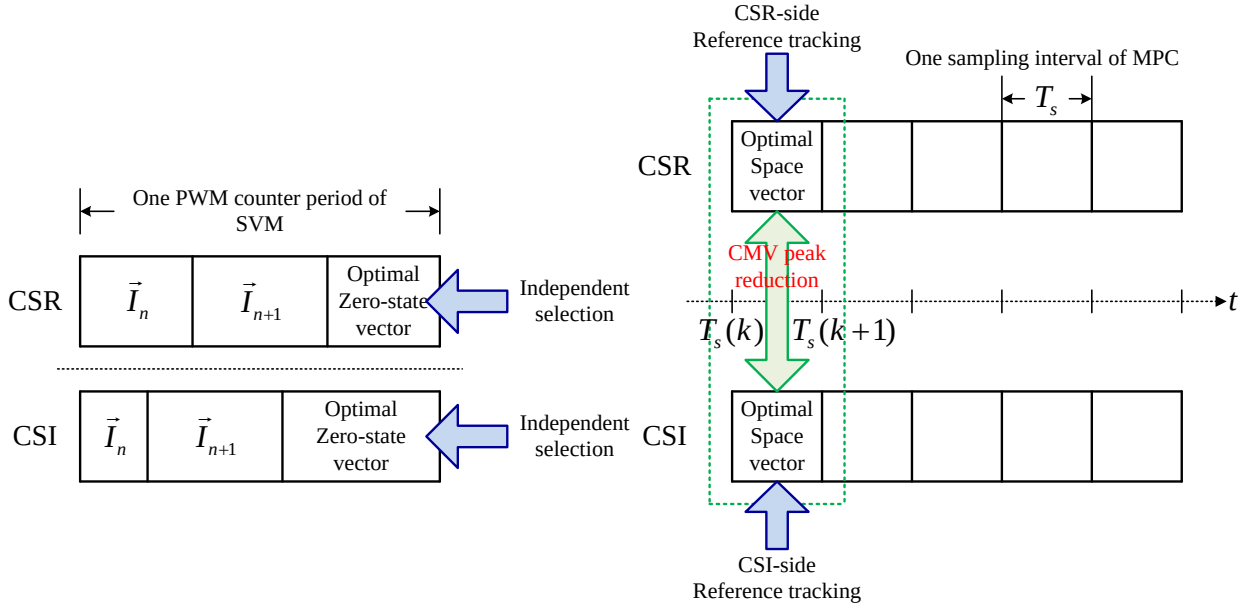
where $V_{Cr}(k)$ and $V_{Ci}(k)$ are the magnitudes of CSR- and CSI-side capacitor phase voltages at *kt*h sampling instant. Since the CMV of a CSC-fed IM drive can be estimated at every sampling instant, the switching states' combinations for CSR and CSI leading to CMV higher than (6.8) will be abandoned. The optimal switching states' combination for CSR and CSI will be only searched in the tentative ones generating CMV no larger than the limitation. Since (6.8) only eliminates the zero-state vectors generating CMV absolute value larger than half peak value of capacitor phase voltage, it only ensures the same CMV mitigation performance as traditional

RCMV-SVM. Therefore, a CMV related term will be imported into the cost function to further reduce the CMV peak value inside the CMV peak value limitation range. Hence, there are mainly three control objectives in RCMV-MPC, as

1) Tracking references at both CSR and CSI sides. This objective can be realized based on a unified cost function, in which the objectives of tracking references at both CSR and CSI sides are associated together, and the optimal switching states for CSR and CSI are selected synchronously;

2) CMV peak value limitation. This objective can be realized through inserting a CMV peak value limitation, defined in (6.8), into the selection process of the optimal switching states for CSR and CSI;

3) Further CMV peak value reduction. This objective is achieved by a CMV related term added into the cost function to further reduce the CMV inside the CMV peak value limitation range at various operating conditions.



(a) (b)

Fig. 6.3 Principle of CMV peak value reduction: (a) zero-state vector selection based RCMV-SVM and (b) RCMV-MPC.

6.2 RCMV-MPC For High Power CSC-Fed MV IM Drive

6.2.1 MPC for CSR

The proposed MPC for CSR is based on the traditional modulating index control [31]. Fig. 6.4 shows the phasor diagram of the traditional modulating index control, in which all the voltage and current phasors, such as $I_{g(1)}$, $I_{wr(1)}$, $V_{Cr(1)}$, and $V_{Lf(1)}$ represent the magnitudes of fundamental-frequency components. $I_{wr(1)}$ aligns with $V_{Cr(1)}$, and $I_{g(1)}$ is just equal to the summation of $I_{wr(1)}$ and $I_{Cr(1)}$. The reactive power generated by the three-phase capacitor can be given by

$$Q_{Cr} = -3\omega_g C_r \left(\frac{V_{Cr(1)}}{\sqrt{2}}\right)^2 \tag{6.9}$$

The reactive power generated by voltage across filter reactor and line current can be given by

$$Q_{Lf} = 3\omega_g L_f \left(\frac{I_{g(1)}}{\sqrt{2}}\right)^2 \tag{6.10}$$

Based on (6.9) and (6.10), the reactive power generated by utility power supply voltage and line current can be given by

$$Q_g = Q_{Cr} + Q_{Lf} \tag{6.11}$$

The primary control objective of CSR is DC current regulation, since the DC current is usually variable according to the operating state of the IM in order to reduce conducting losses in a high power CSC-fed MV IM drive. The DC current regulation is realized through tracking the line current references, which are calculated based on the active and reactive power references. The active power reference can be obtained by a PI controller for DC current control. On the other hand, the reactive power reference can be given by

$$Q_g^* = Q_g \tag{6.12}$$

where the line reactive power reference, Q_g^*, is just set to be equal to the calculated reactive power generated by power supply voltage and line current with the phase angle of $I_{wr(1)}$ aligning with that of $V_{Cr(1)}$.

The line current references in $\alpha\beta$-axis stationary frame can be given by

$$\begin{cases} \mathrm{Re}(\vec{i}_g^{\,*}) = \dfrac{2}{3}\dfrac{\mathrm{Re}(\vec{v}_g)}{\mathrm{Re}(\vec{v}_g)^2 + \mathrm{Im}(\vec{v}_g)^2} P_g^* + \dfrac{2}{3}\dfrac{\mathrm{Im}(\vec{v}_g)}{\mathrm{Re}(\vec{v}_g)^2 + \mathrm{Im}(\vec{v}_g)^2} Q_g^* \\ \mathrm{Im}(\vec{i}_g^{\,*}) = \dfrac{2}{3}\dfrac{\mathrm{Im}(\vec{v}_g)}{\mathrm{Re}(\vec{v}_g)^2 + \mathrm{Im}(\vec{v}_g)^2} P_g^* - \dfrac{2}{3}\dfrac{\mathrm{Re}(\vec{v}_g)}{\mathrm{Re}(\vec{v}_g)^2 + \mathrm{Im}(\vec{v}_g)^2} Q_g^* \end{cases} \tag{6.13}$$

where P_g^* is the active power reference; $\vec{i}_g^{\,*}$ is the line current reference vector; $\mathrm{Re}(\cdot)$ and $\mathrm{Im}(\cdot)$ denote the α-axis and β-axis components of a space vector.

The predicted line current vectors at (k+1)th sampling instant, corresponding to nine possible switching states of a CSR, are compared with line current reference vector in a cost function. The cost function to track line current reference vector at CSR side can be given by

$$g_r^{(x)}(k) = \left| \hat{\vec{i}}_g^{\,*}(k+1) - \vec{i}_g^{\,p(x)}(k+1) \right|^2 \qquad (x = 1, 2, ..., 9) \tag{6.14}$$

where operator $|\cdot|$ denotes the modulus of a space vector. (6.14) represents the square of the Euclidean distance between the line current reference vector and the predicted line current vector. $\vec{i}_g^{\,p(x)}(k+1)$ and $g_r^{(x)}(k)$ are the predicted line current vector and the cost function value corresponding to the xth switching state of a CSR.

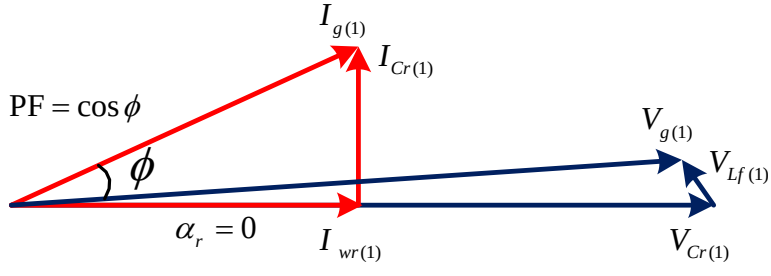


Fig. 6.4 Phasor diagram of traditional modulation index control.

6.2.2 MPFOC for CSI-Fed IM Drive

At the CSI side, model predictive field-oriented control (MPFOC) is introduced into the CSI to conduct IM control. Just similar as traditional FOC, there are two PI controllers to regulate the rotor speed and the rotor flux magnitude. The rotor flux magnitude reference is normally set to its rated value. In high power CSC-fed MV IM drives, the DC current reference is usually calculated at the CSI side based on the operating status of IM, then transmitted to the CSR for DC current regulation. At the CSI side, the produced stator current references in *dq*-axis synchronous frame, with respect to the rotor flux vector, can be transformed into $\alpha\beta$ -axis stationary frame, as

$$\vec{i}_s^{\,*} = \left(I_{sd}^* + jI_{sq}^*\right)e^{j\hat{\theta}_{Fr}} \tag{6.15}$$

where $\vec{i}_s^{\,*}$ is the stator current reference vector; I_{sd}^* and I_{sq}^* are the stator current references in *dq*-axis synchronous frame. As one of the inputs in the prediction model for CSI-fed IM drive, the rotor flux vector is estimated through a current-model flux estimator, which has good performance under low output frequency condition [85]. The estimated rotor flux vector can be given by

$$\hat{\vec{\lambda}}_r = \hat{\lambda}_r e^{j\hat{\theta}_{Fr}} \tag{6.16}$$

where $\hat{\lambda}_r$ is the estimated rotor flux magnitude, and $\hat{\theta}_{Fr}$ is the estimated rotor flux angle.

The predicted stator current vectors at (*k*+1)th instant, corresponding to nine possible switching states of a CSI, are compared with the stator current reference vector in a cost function. The cost function to track the stator current reference can be given by

$$g_i^{(y)}(k) = \left|\hat{\vec{i}}_s^{\,*}(k+1) - \vec{i}_s^{\,p(y)}(k+1)\right|^2 \qquad \left(y = 1,2,...,9\right) \tag{6.17}$$

where $\hat{\vec{i}}_s^{\,*}(k+1)$ is the estimated state current reference vector at (*k*+1)th sampling instant, equal to $\vec{i}_s^{\,*}(k)e^{j\omega_e T_s}$, in which ω_e is the angular frequency of the estimated rotor flux vector; $\vec{i}_s^{\,p(y)}(k+1)$ and $g_i^{(y)}(k)$ are the predicted stator current vector, and the cost function value

corresponding to the *y*th switching state of a CSI. (6.17) represents the square of the Euclidean distance between the stator current reference vector and the predicted stator current vector.

6.2.3 Unified Cost Function for CMV Reduction

As mentioned in Section 6.1.2, the CMV peak value reduction in RCMV-MPC is realized by two steps. The first step is to ensure the generated CMV peak value of a CSC-fed IM drive no higher than the defined CMV limitation in (6.8). The second step is to further mitigate the CMV peak value inside the CMV peak value limitations through synchronous selection of switching states for CSR and CSI, which means that the line current references and the stator current references need to be tracked instantaneously. For this reason, a unified cost function is designed here, and given by

$$g_1^{(x,y)}(k) = \frac{g_r^{(x)}(k)}{\left|\hat{\vec{i}}_g^{*}(k+1)\right|^2} + \frac{g_i^{(y)}(k)}{\left|\hat{\vec{i}}_s^{*}(k+1)\right|^2} \tag{6.18}$$

where $g_1^{(x,y)}(k)$ is the value of the cost function, which is determined by the *x*th switching state of the CSR and the *y*th space vector of the CSI. From a physical meaning point of view, $g_r^{(x)}(k)\Big/\left|\hat{\vec{i}}_g^{*}(k+1)\right|^2$ represents the square of the ratio of the difference of the Euclidean distance between the line current reference vector and the predicted line current vector corresponding to the *x*th space vector of the CSR over the length of the line current reference vector. Similarly, $g_i^{(y)}(k)\Big/\left|\hat{\vec{i}}_s^{*}(k+1)\right|^2$ denotes the square of the ratio of the difference of the Euclidean distance between the stator current reference vector and the predicted stator current vector corresponding to the *y*th space vector over the length of the stator current reference vector. Hence, the summation of these two terms can be considered as an overall ratio of error, which can be used to evaluate the performance on tracking references in a whole CSC-fed IM drive.

In order to further mitigate the CMV peak value, a CMV related term is incorporated into the unified cost function, which can be given by

$$g_2^{(x,y)}(k) = w_{cmv} \cdot \left(v_{og}^{p(x,y)}(k) / V_{og}^{\lim}(k)\right)^2 \tag{6.19}$$

where w_{cmv} is the weighting factor for the CMV related term, and $v_{og}^{p(x,y)}(k)$ is the predicted CMV in the CSC-fed IM drive corresponding to the *x*th space vector of the CSR and the *y*th space vector of the CSI, which can be calculated based on (6.5) to (6.7). The CMV related term represents the square of the ratio of the predicted CMV over the CMV peak value limitation, which can be considered as the maximum possible CMV value. The term in ratio form is chosen here since it is easier to be combined with the terms for tracking references in (6.18), which simplifies the selection of the weighting factor. So the finally unified cost function can be given by

$$g^{(x,y)}(k) = g_1^{(x,y)}(k) + g_2^{(x,y)}(k) \tag{6.20}$$

where tracking references and CMV peak value reduction are fulfilled by the unified cost function. Since both CSR and CSI have nine switching states, there are totally 81 switching states' combinations for CSR and CSI, which are needed to be evaluated based on (6.20) during every sampling interval.

The two-step prediction method is also used here to compensate the delay caused by calculation burden. With delay compensation method introduced in Section 2.3.4, $\hat{\vec{i}}_g(k+1)$, $\hat{\vec{v}}_{Cr}(k+1)$, $\hat{\vec{i}}_s(k+1)$, and $\hat{\vec{v}}_{Ci}(k+1)$ need to be estimated according to the optimal switching states' combination for *k*th sampling interval, and the state variables at *k*th instant. Then, $\vec{i}_g^{\,p}(k+2)$ and $\vec{i}_s^{\,p}(k+2)$ need to be predicted in order to optimally select the switching states' combination for (*k*+1)th sampling interval. The predicted CMV should also be calculated based on the estimated capacitor voltages at (*k*+1)th instant. Finally, the cost function used to evaluate the predicted values at (*k*+2)th instant should be given by

$$\begin{aligned} g^{(x,y)}(k+1) &= g_1^{(x,y)}(k+1) + g_2^{(x,y)}(k+1) \\ &= \underbrace{g_r^{(x)}(k+1)\Big/\left|\hat{\vec{i}}_g^{*}(k+2)\right|^2 + g_i^{(y)}(k+1)\Big/\left|\hat{\vec{i}}_s^{*}(k+2)\right|^2}_{\text{Reference tracks}} + \underbrace{w_{cmv}\cdot\left(v_{og}^{p(x,y)}(k+1)/V_{og}^{\lim}(k+1)\right)^2}_{\text{CMV further mitigation}} \\ &= \underbrace{\frac{\left|\hat{\vec{i}}_g^{*}(k+2)-\vec{i}_g^{\,p(x)}(k+2)\right|^2}{\left|\hat{\vec{i}}_g^{*}(k+2)\right|^2} + \frac{\left|\hat{\vec{i}}_s^{*}(k+2)-\vec{i}_s^{\,p(y)}(k+2)\right|^2}{\left|\hat{\vec{i}}_s^{*}(k+2)\right|^2}}_{\text{Reference tracks}} + \underbrace{w_{cmv}\cdot\left(v_{og}^{p(x,y)}(k+1)/V_{og}^{\lim}(k+1)\right)^2}_{\text{CMV further mitigation}} \end{aligned}$$

(6.21)

6.2.4 Overall Control Structure of RCMV-MPC

Fig. 6.5 shows the control block diagram of RCMV-MPC, in which delay compensation has been considered. Fig. 6.6 shows the flowchart diagram of the selection process of optimal switching states' combination for both CSR and CSI. An additional judgment in the red block is inserted into the flowchart to restrict the CMV peak value of the whole CSC-fed IM drive no higher than the CMV peak value limitation, $V_{og}^{\lim}(k+1)$, which abandons the zero-state vectors introducing too high CMV peak value, and has no influence on tracking references. Hence, the optimal switching states' combination leading to the minimum value of

(6.21) will be only selected from the tentative combinations, which satisfy the CMV peak value limitation. In Fig. 6.6, two loops are nested together, one for selecting the optimal switching state for the CSR, and the other for selecting the optimal switching state for the CSI. Since both CSR and CSI have nine switching states, the loop needs to be totally repeated 81 times during every sampling interval, which results in very huge computation burden. For more efficient computation, the CSR-side CMV, $v_{cmr}^{p(x)}(k+1)$, the predicted line current vector, $\vec{i}_g^{\,p(x)}(k+2)$, the cost function to track line current references, $g_r^{(x)}(k+1)$, corresponding to *x*th space vector of the CSR (*x*=1, 2, …, 9), are calculated before entering the loop. Similarly, the CSI-side CMV, $v_{cmi}^{p(y)}(k+1)$, the predicted stator current vector, $\vec{i}_s^{\,p(y)}(k+2)$, and the cost function to track stator current reference, $g_i^{(y)}(k+1)$, corresponding to *y*th space vector of the CSI (*y*=1, 2, …, 9) are also calculated. All the calculations are completed in the 'Preliminary Calculation' part in Fig. 6.6. Then, just some add operations and comparison operations need to be conducted in the 81 times loops. If the algorithm is not arranged in this manner, computation burden will dramatically increase. For instance, when *x* is equal to 1, all the CSI-side prediction values need to be calculated once, then, when *x* increases to 2, all the calculations at the CSI side need to be repeated, which introduces more computation burden.

Fig. 6.5 Block diagram of RCMV-MPC for CSC-fed IM drives.

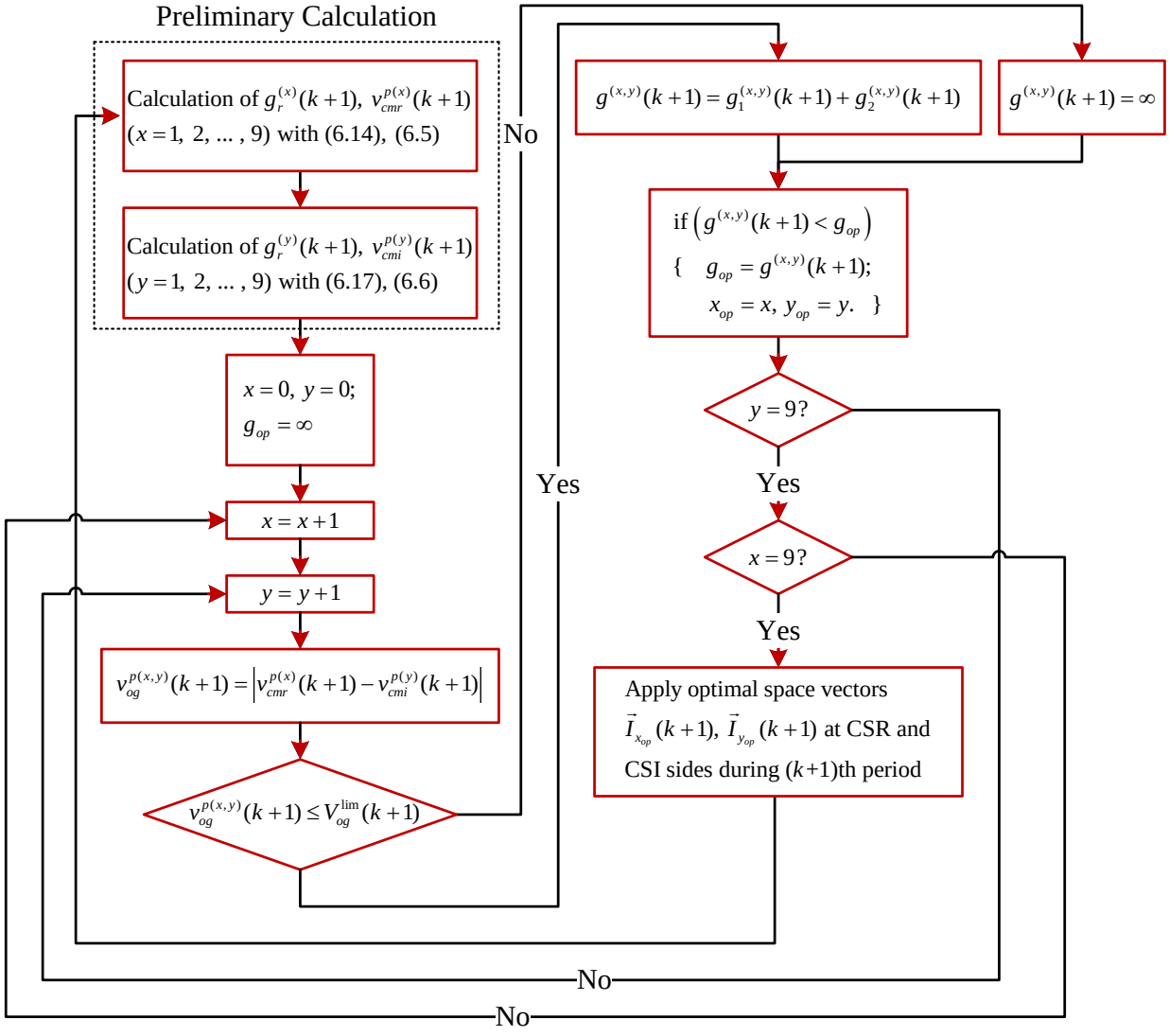


Fig. 6.6 Flowchart diagram of optimal switching states' combination selection.

6.3 Simulation Validation

In order to validate RCMV-MPC, simulation on a high power CSC-fed MV IM drive is conducted. The parameters used in the simulation are listed in Table 6.1. The simulation results of the CSC-fed IM drive with traditional control schemes are also provided, in which classic FOC and modulating index control are used in CSI and CSR, respectively. The modulating index for CSI is selected as 0.8. The conventional three-segment SVM is used in both CSR and CSI with switching frequency of 1080Hz, which indicates that the PWM counter period, which is used to generate gating signals, is 1/2160s. Besides, the simulation results of zero-state vector

selection based RCMV-SVM, presented in [39] are also provided, in which three-segment sequence is still used, and zero-state vector selection processes are separately conducted at CSR and CSI sides. In order to keep a fair competition, the same PI parameters are used in classic FOC and MPFOC. The PI parameters for traditional modulating index control and the proposed MPC for CSR have also been well tuned. Here, for simplicity, conventional SVM and zero-state vector selection based RCMV-SVM are called Method I and Method II, respectively. The average switching frequencies of CSR and CSI are updated based on (3.33) every 30 consecutive fundamental periods, meaning 0.5s in this case.

Table 6.1 SYSTEM PARAMETERS IN SIMULATION

System Ratings		System Parameters	
Rated power	1MW	filter reactor L_f	0.15pu
Rated line-to-line voltage	4160V	DC chock L_{dc}	1pu
Rated line current	139A	Rectifier side capacitor C_r	0.4pu
		Inverter side capacitor C_i	0.4pu
Induction Motor Ratings		Induction Motor Parameters	
Rated output power	1260hp	Stator resistance R_s	0.2Ω
Rated line-to-line voltage	4160V	Rotor resistance R_r	0.146Ω
Rated stator current	150A	Stator leakage inductance L_{ls}	5.2mH
Rated speed	1189rpm	Rotor leakage inductance L_{lr}	5.2mH
Rated torque	7490Nm	Magnetizing inductance L_m	155mH
Rated rotor flux linkage	8.35Wb	Moment of inertia J	$22\text{kg}\cdot\text{m}^2$

6.3.1 Sampling Frequency Selection

Sampling frequency is always a crucial parameter in control realization, which directly affects output performance. For MPCs, high sampling frequencies, normally higher than 10kHz, are required to ensure the accuracy of prediction process. In this work, the sampling frequency for RCMV-MPC is selected as 10kHz, meaning the sampling interval equal to $100\mu\text{s}$. In order to keep a fair comparison between conventional methods and RCMV-MPC, a multi-sampling SVM (MS-SVM), presented in [30], is used in both Method I and Method II. With MS-SVM, the PWM counter period is still kept constant at 1/2160s, but there are multiple sampling points in one counter period. Here the sampling frequency of 8640Hz is selected for both Method I and

Method II, which means that there are four sampling points every PWM counter period. The main advantage of MS-SVM is the reduction of low-order harmonics in PWM currents through optimizing dwell time for active and zero-state vectors in one counter period. On the other hand, MS-SVM does not affect the CMV values. Table 6.2 presents the output performance of Method I and Method II along with different sampling frequencies. At the same operating condition of 6000Nm and rated speed, it can be found that the THDs of line current and stator current decrease with the increase of sampling frequency. Nevertheless, the CMV peak values are unchanged along with the increase of sampling frequency, which indicates that higher sampling frequencies in Method I and Method II cannot reduce the CMV stress.

Table 6.2 OUTPUT PERFORMANCE ALONG WITH SAMPLING FREQUENCY

Sampling Frequency (Hz)	Method I			Method II		
	THD of i_g (%)	THD of i_s (%)	CMV Peak (V)	THD of i_g (%)	THD of i_s (%)	CMV Peak (V)
2160	9.68	2.14	6920	9.85	2.12	3975
4320	6.29	1.34	6750	6.38	1.39	3950
6480	4.24	0.81	7200	4.29	0.86	4000
8640	3.78	0.71	7200	3.79	0.69	4000

6.3.2 Weighting Factor Selection

In (6.21), tracking reference and CMV further reduction are associated together with the weighting factor, w_{cmv}, which has direct impact on output performance. Fig. 6.7 shows a profile of the CMV peak value and the THDs of the line current and the stator current with respect to the weighting factor in RCMV-MPC at rated speed and 6000Nm condition. It can be observed that with the increase of the weighting factor, the distortion in the line current and the stator current becomes higher, and the CMV peak value becomes smaller. However, with the further increase of the weighting factor, the effect on the CMV peak value reduction becomes not that significant, and the distortion in the line current and the stator current continuously becomes heavier. In fact, there is an approximate optimal trade-off point between CMV peak value reduction and output performance, which is just around 0.004 of the weighting factor, as Fig. 6.7 shows. Therefore, the weighting factor value in simulation and experimental parts are kept at 0.004.

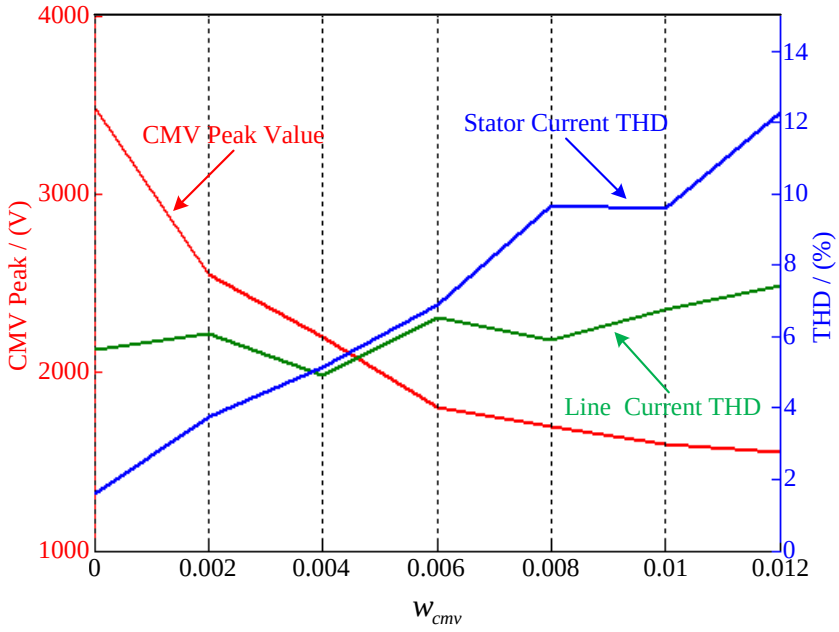


Fig. 6.7 Profile of CMV peak value and THD versus w_{cmv} at rated speed and 6000Nm condition.

6.3.3 Steady State Performance

Table 6.3 presents the quantitative steady state performance of three methods at various operating conditions. 'NA' represents that there is no CMV peak limitation used. The largest CMV peak value appears with Method I, which is caused by the CSR-side and the CSI-side zero-state vectors with higher CMV values. Due to the use of conventional SVM, the switching frequencies at both CSR and CSI sides are kept at 1080Hz. With Method II, the CMV peak value is reduced to just around the summation of the half peak values of the CSR-side and CSI-side capacitor phase voltages, which is also equal to the CMV limitation used in RCMV-MPC. Since optimal selection of zero-state vectors at both CSR and CSI sides will not have influence on output performance, it can be found that the THDs of the line current and the stator current are very close to those of Method I. Due to zero-state vector selection process, the switching frequencies of Method II become larger and variable with the operating conditions. The minimum CMV peak value is generated by RCMV-MPC all the time, with which the CMV peak value is approximately further reduced to only about 60% of that by Method II due to the penalty effect of the CMV related term, $g_2^{(x,y)}(k+1)$, in (6.21). The switching frequencies of RCMV-MPC are also variable. At different operating conditions, the CSI-side average

switching frequencies are around 1200Hz, which are even lower than that of Method II. On the other hand, the CSR-side switching frequencies, which become larger with the decrease of the rotating speed of the IM, are generally higher than that at the CSI side. In comparison with RCMV-MPC, Method I and Method II with very close switching frequencies and sampling frequencies can provide lower current distortion, especially on stator current, but the THD of stator current is not a crucial issue in motor drives. In terms of CMV, RCMV-MPC achieves the lowest CMV peak values all the time. Moreover, both Method II and RCMV-MPC are the methods aiming at CMV peak value reduction, and share very close switching frequencies no matter at CSR or CSI side. Though Method II realizes lower THDs of the line current and the stator current, RCMV-MPC achieves further CMV peak value reduction with respect to the results of Method II.

Table 6.3 SIMULATION RESULTS OF THREE METHODS FOR COMPARISON

Rotor speed (rpm)	Load torque (Nm)	Motor-side synchronous frequency (Hz)	Scheme	$\overline{f}_{sw}$ (Hz)		THD (%)		CMV limit (V)	CMV peak (V)
				CSR	CSI	CSR	CSI		
1189	6000	59.9	Method I	1080	1080	3.78	0.71	NA	7200
			Method II	1530	1532	3.79	0.69	NA	4000
			RCMV-MPC	1527	1179	4.91	4.59	3670	2000
1189	1000	59.6	Method I	1080	1080	2.61	0.83	NA	7100
			Method II	1530	1502	2.36	0.83	NA	3900
			RCMV-MPC	1517	1365	3.93	6.40	3485	1650
800	6000	40.5	Method I	1080	1080	3.14	2.72	NA	6200
			Method II	1481	1502	3.19	2.62	NA	3300
			RCMV-MPC	1969	1210	4.88	5.72	2945	1750
800	1000	40.1	Method I	1080	1080	3.04	3.36	NA	6100
			Method II	1440	1500	2.57	3.95	NA	3200
			RCMV-MPC	1757	1304	2.77	3.74	2916	1500
200	6000	10.5	Method I	1080	1080	2.33	2.70	NA	4760
			Method II	1260	1457	3.16	2.60	NA	2800
			RCMV-MPC	2235	1209	6.07	4.51	2140	1650
200	1000	10.1	Method I	1080	1080	1.73	2.12	NA	4450
			Method II	1170	1301	1.88	2.11	NA	2750
			RCMV-MPC	1949	1271	3.89	3.78	2087	1400

Fig. 6.8 and Fig. 6.9 show the waveforms of two typical cases in Table 6.3, representing a high power MV CSC-fed IM drive with a fan-type load. Fig. 6.8 illustrates that the IM operates at the rated speed and 6000Nm condition. From top to bottom, the phase A line current, the

phase U stator current, and the CMV of the motor drive system are depicted. With RCMV-MPC, the CMV peak value, which is further reduced compared to that with Method II, is strictly limited inside the CMV limitations. Besides, the performance on tracking the references at both CSR and CSI sides can be guaranteed with RCMV-MPC. Fig. 6.9 shows the waveforms at 200rpm speed and 1000Nm condition, since the load decreases with the drop of the speed for a fan-type load. The CMV peak value of RCMV-MPC is reduced to only 52% of that with Method II. Since the DC current reference becomes small at low speed and light load condition, the larger switching frequency at the CSR side with RCMV-MPC will not lead to too much increase on switching losses. Since the CSR-side control schemes in the conventional methods and RCMV-MPC are both modulating index regulation, the line current magnitudes of three methods are kept the same even at low speed and light load condition, which ensures a fair comparison, as Fig. 6.9 shows.

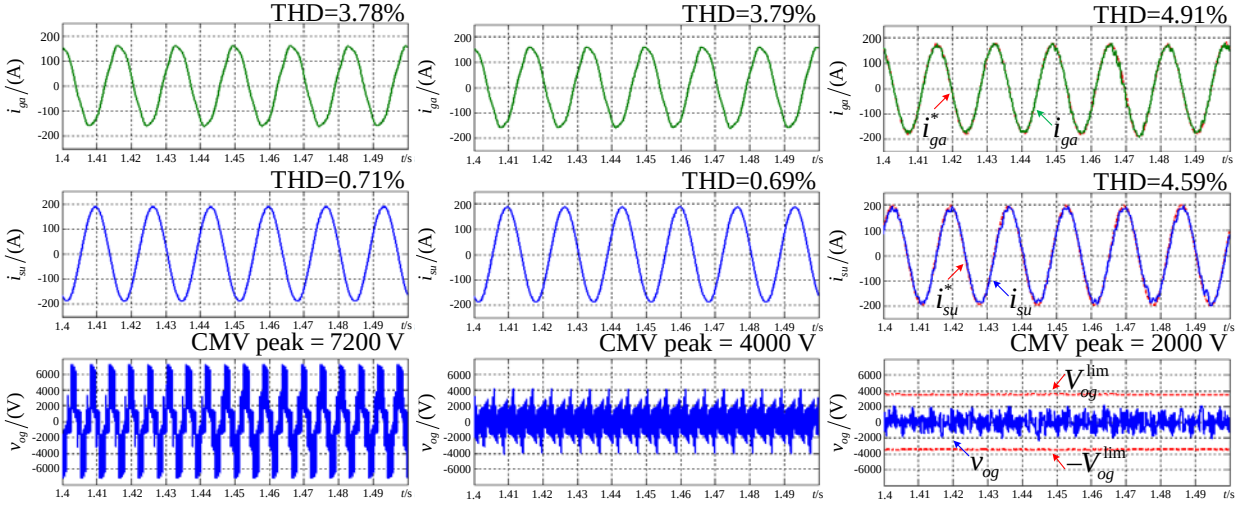


Fig. 6.8 Simulated results at rated speed and 6000Nm condition: (a) Method I, (b) Method II, and (c) RCMV-MPC.

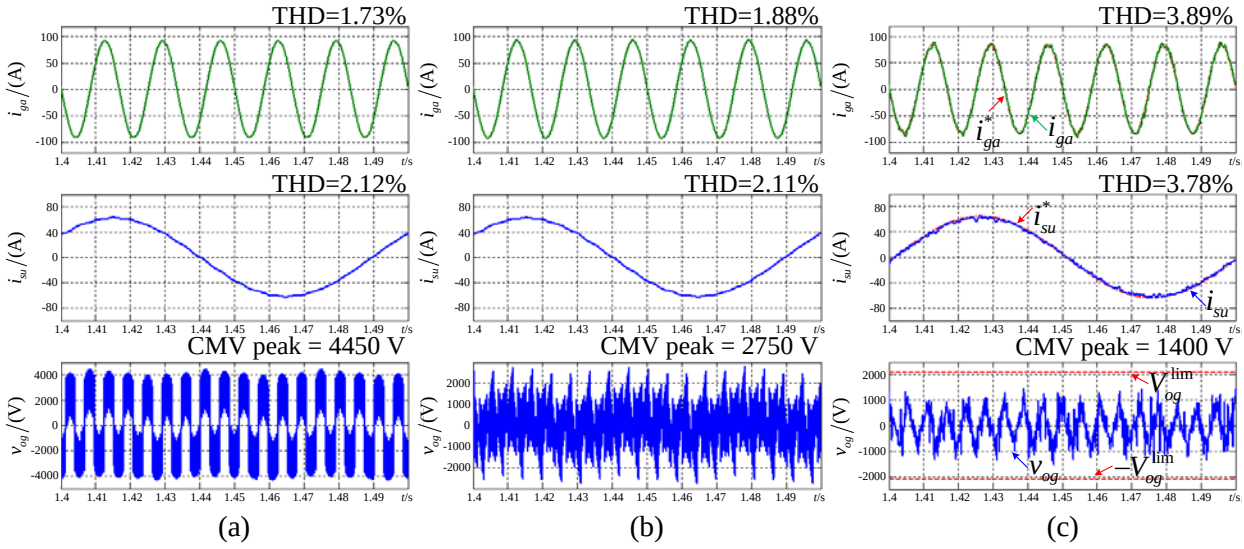


Fig. 6.9 Simulated results at 200rpm and 1000Nm condition: (a) Method I, (b) Method II, and (c) RCMV-MPC.

Fig. 6.10 shows a zoomed CMV diagram of Method II and RCMV-MPC at rated speed and 6000Nm condition to demonstrate the mechanism of CMV peak value further reduction in RCMV-MPC. The CMVs at the CSR and CSI side, and that of the whole system are illustrated from top to bottom. No matter with Method II or RCMV-MPC, the CMVs at the CSR and CSI sides can both be limited no larger than the half peak values of the respective capacitor phase voltages. As Fig. 6.10 shows, due to the further arrangement of the applied space vectors at both CSR and CSI sides, some peaks with Method II can be eliminated, which achieves the further reduction of the CMV peak values.

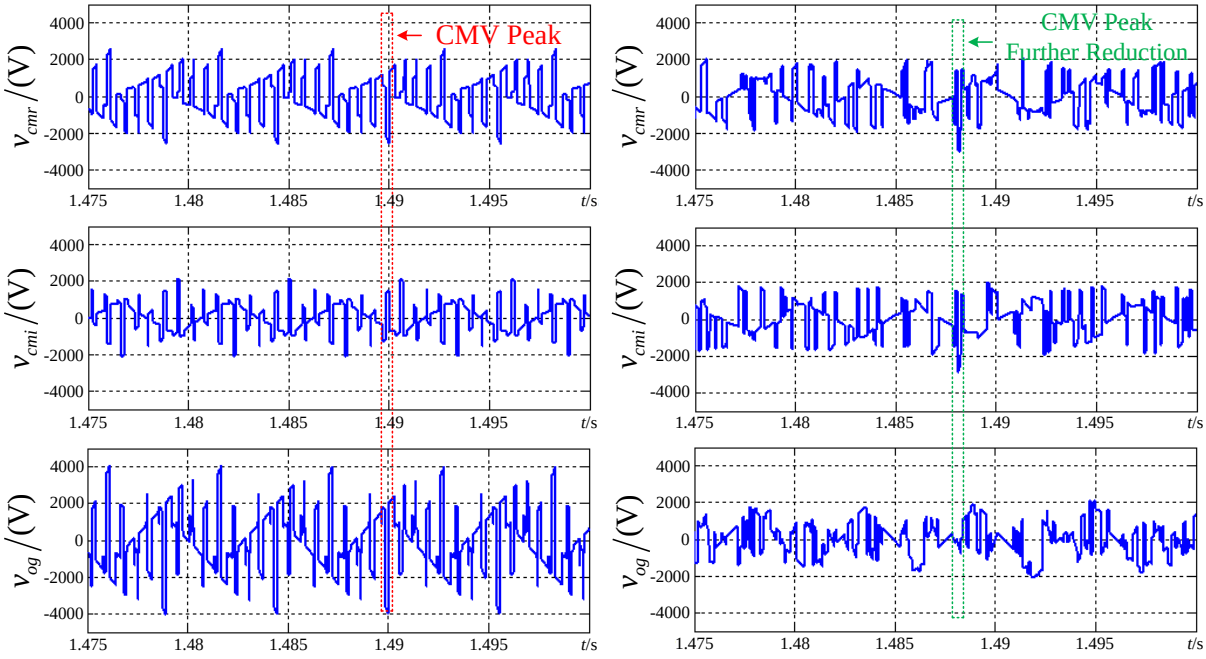
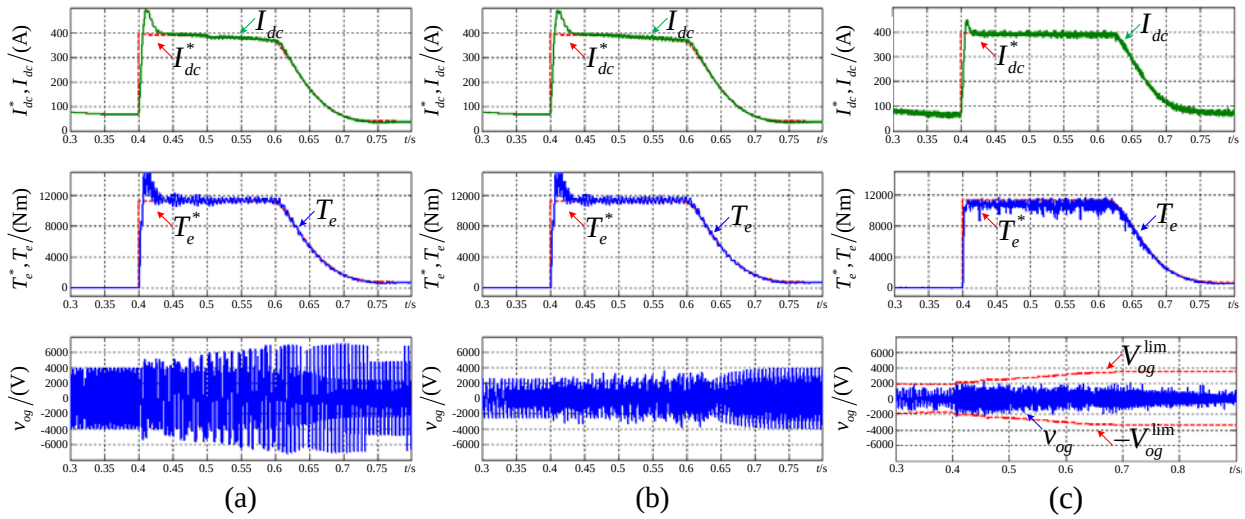


Fig. 6.10 Zoomed CMV results at rated speed and 6000Nm condition: (a) Method II and (b) RCMV-MPC.

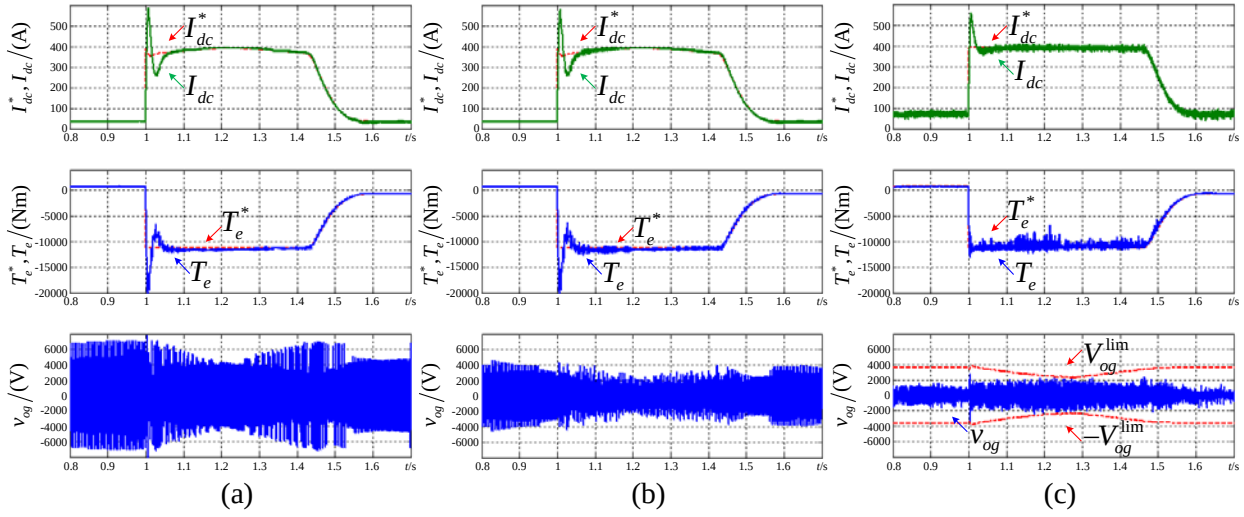
6.3.4 Transient Performance

The start-up performance at no-load condition with Method I, Method II, and RCMV-MPC is illustrated in Fig. 6.11. From top to bottom, the DC current, the torque, and the CMV, are depicted. In RCMV-MPC, the CMV peak value limitations, are also shown. At time *t* of 0.4s, the speed reference jumps from 0 to 1189rpm. The output limitation of the speed controller is 1.5 times the rated torque. Since the dynamic responses of the CSR-side and CSI-side capacitors are not taken into consideration in Method I and Method II, which are based on traditional linear control schemes, large overshoots can be observed in the torque and the DC current during the start-up process. Due to the advantages offered by MPC approach based scheme, better dynamic performance is obtained by RCMV-MPC, with which the torque and DC current overshoots are effectively mitigated. Moreover, during the whole start-up process, the CMV with RCMV-MPC can be limited not surpassing the CMV peak value limitations. In contrast to Method II, further CMV peak value reduction can also be achieved during the start-up process with RCMV-MPC.



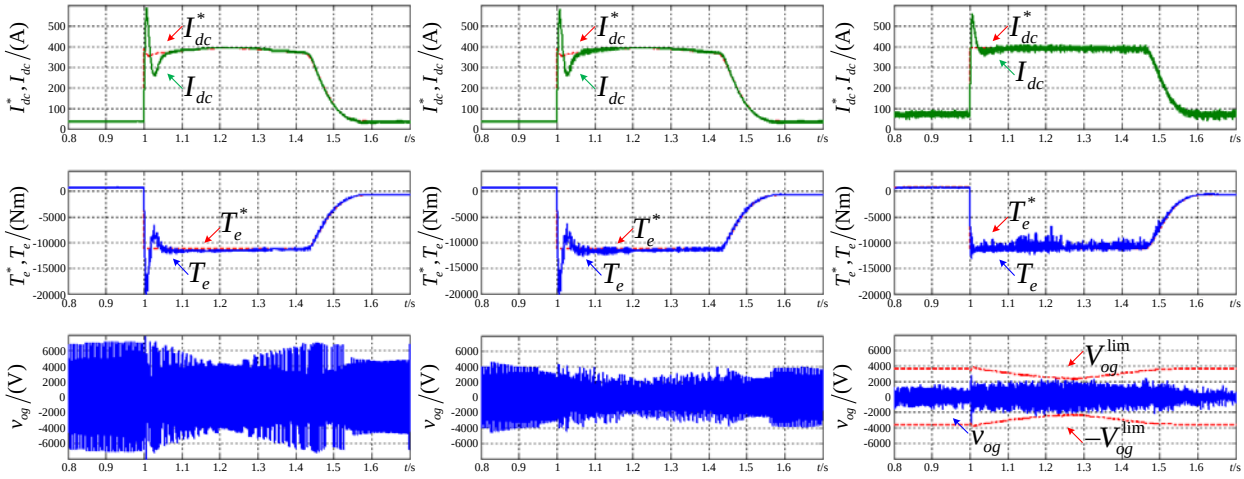
(a) (b) (c)

Fig. 6.11 Simulation results during start-up process at no-load condition: (a) Method I, (b) Method II, and (c) RCMV-MPC.



(a) (b) (c)

Fig. 6.12 shows the simulation results during speed-reverse process at no-load condition. When the IM operates at rated speed, the speed reference changes from the positive to the negative rated value at time *t* of 1s. Similar as the results during start-up process, RCMV-MPC achieves the smallest CMV peak value, which is strictly restricted between the CMV peak value limitations during the process. Moreover, in comparison with two conventional counterparts, RCMV-MPC obtains better dynamic performance indicated by the smaller DC current overshoot and the mitigation on the torque overshoot.



(a) (b) (c)

Fig. 6.12 Simulation results during speed-reverse process at no-load condition: (a) Method I, (b) Method II, and (c) RCMV-MPC.

6.4 Experimental Verification

In order to further verify the effectiveness of RCMV-MPC, some experiments are conducted on a low power CSC-fed IM drive prototype. Fig. 6.13 shows the photograph of the low power prototype, of which the ratings and parameters are listed in Table 6.4. The prototype mainly consists of a back-to-back CSC, an IM, and a DC generator, which is used to provide load torque. The details on the low power prototype can be referred to Section 3.4. The experimental results of Method I and Method II are also provided for comparison. In order to keep a fair comparison, the PWM counter period of 1/1800s and MS-SVM with sampling frequency of 7200Hz are used in both Method I and Method II, which leads to a switching frequency of 900Hz in Method I. The sampling interval and weighting factor before CMV reduction term are still 100μs and 0.004, respectively. The average switching frequency is calculated based on (3.33) as well.

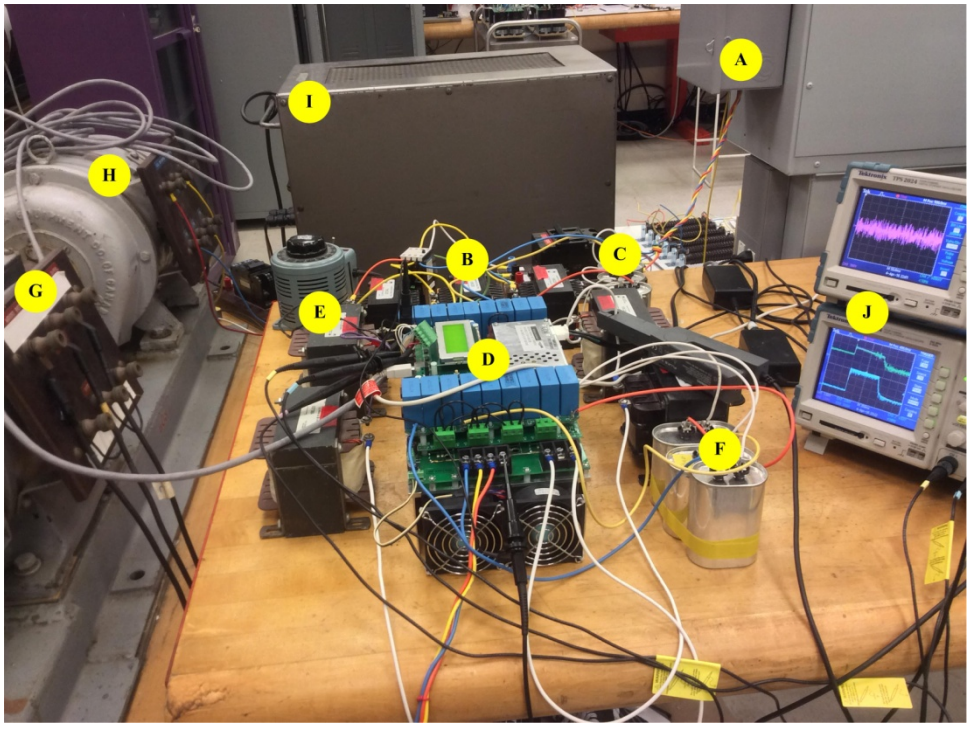


Fig. 6.13 Photograph of a low power CSC-fed IM drive prototype: (A) three-phase power supply, (B) filter inductor, (C) CSR-side capacitor, (D) CSR and CSI, (E) DC-choke, (F) CSI-side capacitor, (G) induction motor, (H) DC motor, (I) DC load, and (J) oscilloscopes.

Table 6.4 SYSTEM PARAMETERS IN EXPERIMENTS

System Ratings		System Parameters	
Rated power	5kW	Filter reactor L_f	0.218pu
Rated line-to-line voltage	208V	DC chock L_{dc}	1.16pu
Rated line current	13.9A	Rectifier side capacitor C_r	0.378pu
		Inverter side capacitor C_i	0.378pu
Induction Motor Ratings		Induction Motor Parameters	
Rated output power	5hp	Stator resistance R_s	0.395Ω
Rated line-to-line voltage	208V	Rotor resistance R_r	0.737Ω
Rated stator current	14.3A	Stator leakage inductance L_{ls}	1.95mH
Rated speed	1700rpm	Rotor leakage inductance L_{lr}	1.95mH
Rated torque	21Nm	Magnetizing inductance L_m	47.1mH
Rated rotor flux linkage	0.433Wb	Moment of inertia J	$0.08\text{kg}\cdot\text{m}^2$

6.4.1 Steady State Performance

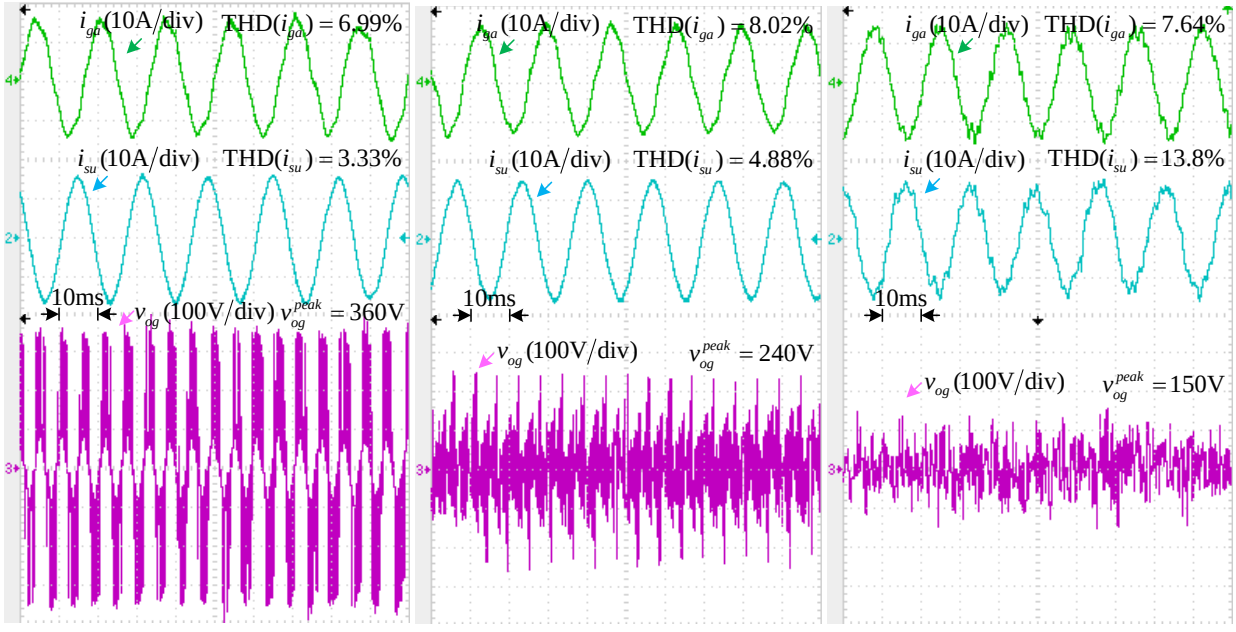
Table 6.5 EXPERIMENTAL RESULTS OF THREE METHODS FOR COMPARISON

Rotor speed (rpm)	Load torque (Nm)	Motor-side synchronous frequency (Hz)	Scheme	$\overline{f}_{sw}$ (Hz)		THD (%)		CMV limit (V)	CMV peak (V)
				CSR	CSI	CSR	CSI		
1700	16.8	60	Method I	900	900	6.99	3.30	NA	360
			Method II	1020	1019	8.02	4.88	NA	240
			RCMV-MPC	950	930	7.64	13.8	190	150
1700	2.1	58	Method I	900	900	8.97	4.12	NA	350
			Method II	1007	1016	8.98	4.79	NA	210
			RCMV-MPC	960	950	7.79	12.9	190	140
850	16.8	32	Method I	900	900	5.69	3.12	NA	280
			Method II	993	992	5.87	3.34	NA	200
			RCMV-MPC	1005	980	7.12	9.82	173	140
850	2.1	29	Method I	900	900	8.72	4.01	NA	260
			Method II	940	928	8.75	4.38	NA	185
			RCMV-MPC	1010	1005	8.44	9.49	165	130
180	16.8	10	Method I	900	900	9.25	4.39	NA	240
			Method II	931	967	10.3	5.11	NA	170
			RCMV-MPC	1020	992	7.59	8.10	148	130
180	2.1	7	Method I	900	900	9.98	4.96	NA	230
			Method II	930	921	10.1	5.13	NA	160
			RCMV-MPC	1020	1020	7.04	7.15	135	120

Table 6.5 lists the experimental results of three methods at various steady-state operating conditions. The minimum CMV peak value, which is highlighted in Table 6.5, can be obtained with RCMV-MPC at all the listed operating conditions. The CMV peak values of RCMV-MPC are limited not surpassing the CMV peak limitations, and around 70% of that with Method II, which verifies the CMV further reduction achieved by RCMV-MPC. Besides, according to the THDs of the line current and the stator current, the balance between the control objectives on tracking the references at both CSR and CSI sides can be realized based on (6.21). The average switching frequencies of Method II and RCMV-MPC are both variable, and the switching frequencies of Method II are even higher than that of RCMV-MPC in some cases. Similar as the simulation results of RCMV-MPC, the average switching frequencies of CSR are higher than that of CSI, and increase with the decrease of the rotor speed. Though Method I and Method II can realize lower current distortion, RCMV-MPC achieves CMV peak value further reduction, even in contrast to Method II. It can be observed that the line current THDs of Method I and Method II with MS-SVM are not as satisfactory as those in Table 6.3. The consequence is caused by low-order harmonics contained in the real power supply voltage. Since MS-SVM can

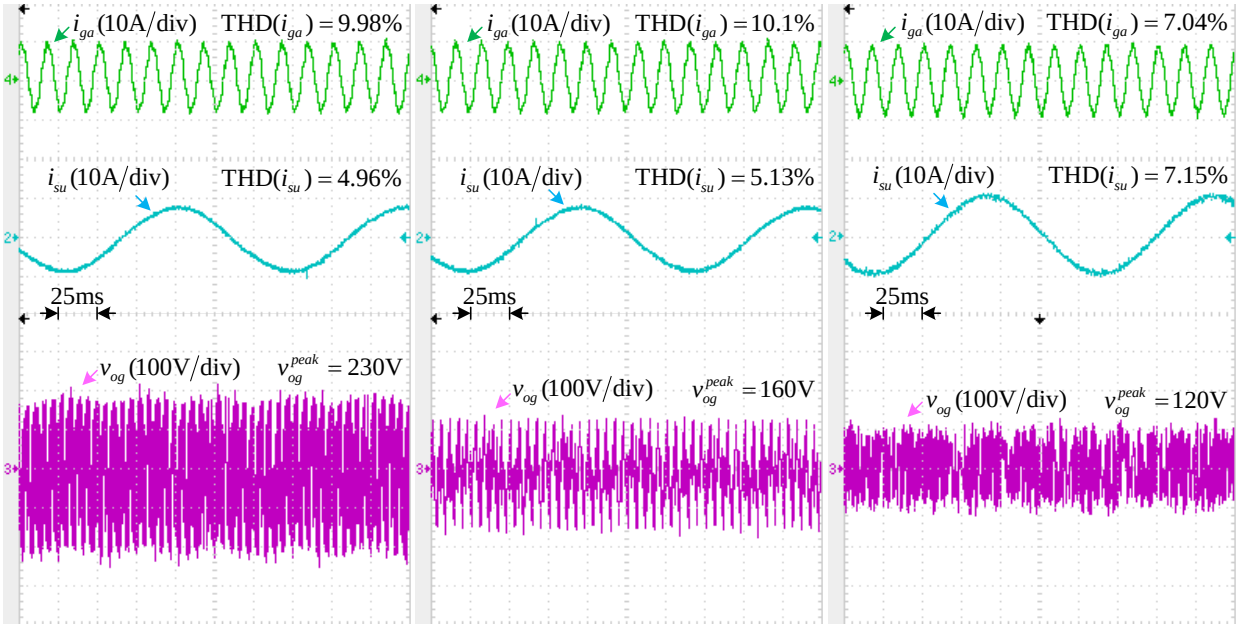
just eliminate low-order harmonics in PWM currents, the effect of the distortion in the power supply voltage on the line current cannot be mitigated.

Fig. 6.14 and Fig. 6.15 show the steady state responses at two typical operating conditions in Table 6.5 with a fan-type load. From top to bottom, the phase A line current, the phase U stator current, and the CMV of the whole system are presented. In Fig. 6.14, at 1700rpm and 16.8Nm condition, the CMV peak value of Method I is as high as 360V. Method II reduces the CMV peak value to 240V. The CMV peak value of RCMV-MPC is further reduced to only 150V, smaller than 70% of that with Method II. Fig. 6.15 shows the performance at 180rpm and 2.1Nm condition. The CMV peak values of Method I and Method II are 230Vand 160V, respectively. With RCMV-MPC, the CMV peak value is further reduced to only 120V.



(a) (b) (c)

Fig. 6.14 Experimental results at 1700rpm and 16.8Nm condition: (a) Method I, (b) Method II, and (c) RCMV-MPC.



(a) (b) (c)

Fig. 6.15 Experimental results at 180rpm and 2.1Nm condition: (a) Method I, (b) Method II, and (c) RCMV-MPC.

Table 6.6 shows the execution time of three methods in every sampling interval. It can be found that RCMV-MPC requires the longest execution time. Fortunately, due to superb calculation capability of nowadays DSPs and the reduced calculation burden by preliminary calculation stage in Fig. 6.6, RCMV-MPC can still be realized inside a small sampling interval, such as 100μs in this case.

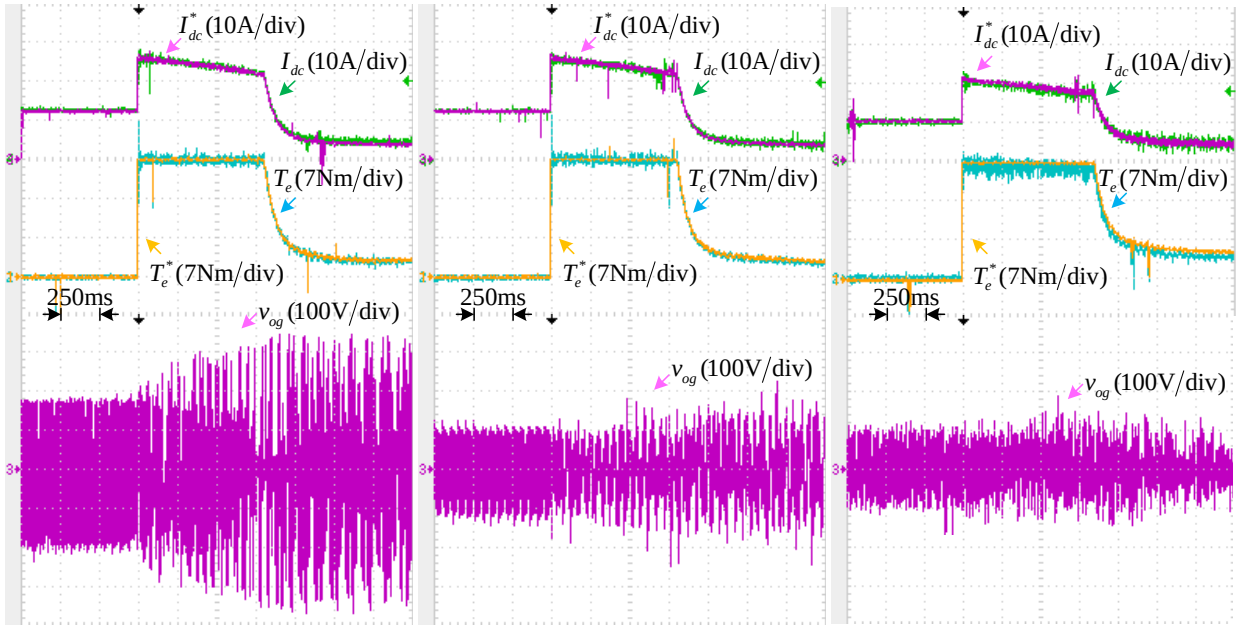
Table 6.6 EXECUTION TIME OF THREE METHODS

Method	Execution time
Method I	40μs
Method II	46μs
RCMV-MPC	75μs

6.4.2 Transient Performance

Fig. 6.16 shows the start-up performance of three methods at no-load condition. The DC current, the torque, and the CMV are presented. The DC current reference, the torque and its reference are measured through the D/A interfaces in the prototype. The DC current is directly

measured through a current probe. The speed reference steps to the rated speed of 1700rpm. The output limitations of the speed controller is the rated torque of 21Nm. The CMV peak value of RCMV-MPC during start-up process can still be regulated and further reduced. Moreover, in comparison with Method I and Method II, the torque overshoot is significantly mitigated with RCMV-MPC.



(a) (b) (c)

Fig. 6.16 Experimental results during start-up process at no-load condition: (a) Method I, (b) Method II, and (c) RCMV-MPC.

Fig. 6.17 shows the experimental results of three methods during speed-reverse process, in which the speed reference changes from the positive to the negative rated value at no-load condition. The CMV generated by RCMV-MPC is strictly restricted, and also the smallest among three methods during the whole process. Moreover, in contrast to Method I and Method II, RCMV-MPC presents better torque dynamic response with the reduction of the torque overshoot, which further verifies the effectiveness of RCMV-MPC as well.

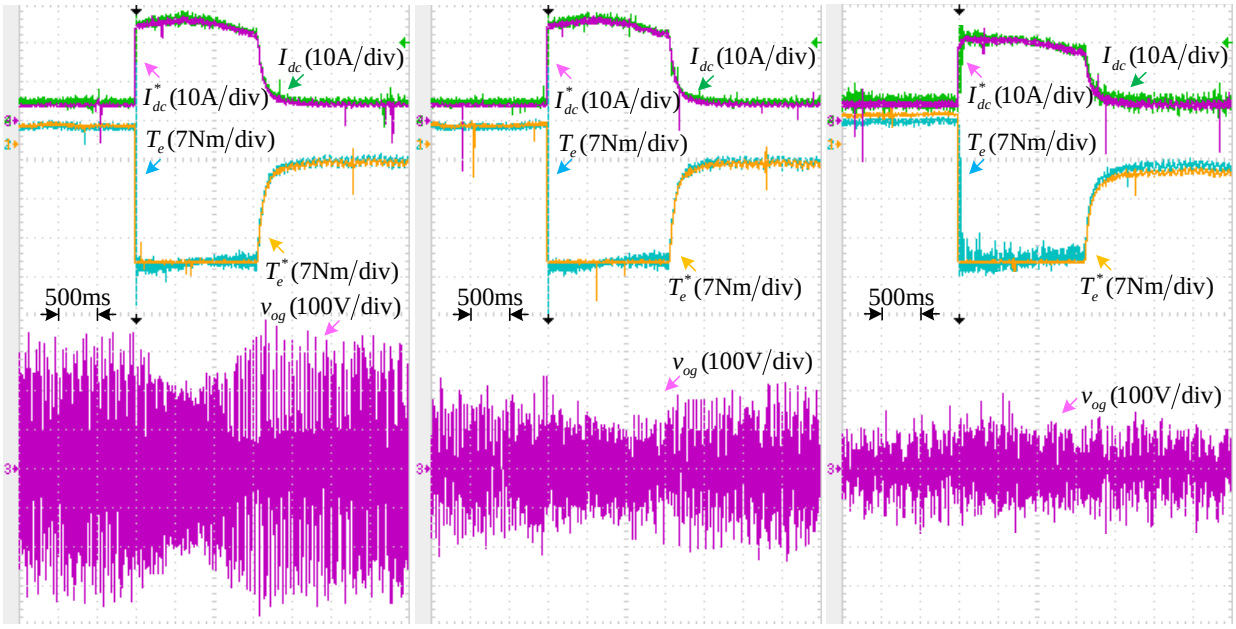


Fig. 6.17 Experimental results during speed reverse at no-load condition: (a) Method I, (b) Method II, and (c) RCMV-MPC.

6.5 Conclusion

In this chapter, RCMV-MPC for high power CSC-fed MV IM drive has been presented. Both simulation and experimental results are provided to validate the effectiveness of the two schemes, based on which some conclusions can be drawn as

- In terms of performance on CMV peak value reduction, RCMV-MPC can reduce the CMV peak value to only around 40% of that by conventional SVM. Moreover, compared to zero-state vector selection based RCMV-SVM, nearly 40% reduction on CMV peak value can be achieved in different operating states of IM. Relying on the unified cost function, satisfactory performance on tracking references at both CSR and CSI sides can be achieved by RCMV-MPC;
- Last but not least, thank to relatively high sampling frequency used in MPC, no matter MPPFC or RCMV-MPC can realize better dynamic performance in contrast to their traditional linear control counterparts. Especially for RCMV-MPC, constraint and

reduction on CMV peak value can still be kept during transient processes, which is not guaranteed by conventional methods.

7 Conclusions and Future Work

High power current-source converters (CSCs) have been more and more applied into medium-voltage (MV) motor drives, due to their specific features in contrast to their voltage-source counterparts. However, with more stringent requirements on control performance imposed on industrial drives, traditional control schemes cannot meet these stricter requirements. In this research, various model predictive control (MPC) schemes have been developed and validated aiming high power CSC-fed MV induction motor (IM) drives.

The outcomes of the research work presented in this dissertation has brought several major innovations in the development of advanced control schemes for high power CSC-fed MV drives, which promotes MPC schemes as a simple, efficient, and versatile control technique for high power CSC-fed MV IM drives, normally operating at a very low (<1kHz) switching frequency to minimize converter power losses. Various control objectives such as line current control, DC current regulation, manipulation of switching commutations, and CMV peak reduction are incorporated straight forward in the design and operation of MPC schemes. The modeling and analysis presented in this dissertation can also be used in other power converters and energy conversion applications.

7.1 Conclusions

The major contributions and conclusions of this research are summarized as follows.

1) A review on high power CSC-fed MV motor drive, its traditional control schemes, and conventional MPC schemes is presented

A review on the traditional control schemes and the conventional MPC schemes for high power CSC-fed MV motor drive is presented. Various control techniques for both CSR and CSI-fed motor drive, their features and drawbacks are analyzed and summarized;

2) An appropriate discretiaztion method is selected for the second-order system in CSC

In this research, various discretization methods are discussed and compared with each other, in which Henu's method is finally selected to discretize the continuous-time dynamic models of high power CSC-fed MV IM drive. The discrete-time models are suitable for second-order

systems as in CSR and CSI, and calculation friendly, which can be easily realtime updated, and used to predict various variables including line/stator currents, DC current, switching commutations, and CMVs, and to incorporate control delay compensation;

3) Model predictive power factor control (MPPFC) is proposed to control high power CSR

With MPPFC, the line power factor of high power CSR can be accurately regulated to reach maximum achievable value under various operating conditions. In comparison with conventional MPC and traditional modulation index control, the line power factor increases from 0.681 and 0.474 to 0.998 under half rated DC current condition. Moreover, aiming at the possible line-side *LC* resonance, an active-damping method is incorporated into MPPFC, which further improves the active-dampling performance during transients;

In consideration of the perturbation of the filter parameters in CSR, an online capacitance estimation method is proposed and incorporated into MPPFC. With the capacitance estimation method, the discrepancy between the real capacitance and the value used in control can be gradually mitigated, which enhances the robustness of MPPFC;

4) Model predictive switching pattern control (MPSPC) is proposed to achieve low switching frequency operation and improved dynamic performance for high power CSC

MPSPC combines selective harmonic elimination (SHE) modulation with MPC approach. The final control objective is that in steady state, the output currents of CSC can follow the switching patterns of SHE modulation, which fixes the switching frequency at a very low value, and achieves low-order harmonic elimination, on the other hand, CSC is governed through MPC approach in order to achieve better dynamic responses during transients;

In addition, the weighting factors in conventional MPC are normally selected through an experiential process. This process is avoided in MPSPC, which simplifies the complexity of control design;

5) Model predictive space vector pattern control (MPSVPC) is proposed for high power CSC-fed MV IM drive

MPSVPC can be viewed as an extension of MPSPC. Space vector modulation (SVM) takes the place of SHE modulation in MPSVPC, which makes it more suitable for variable-frequency application. In this research, MPSVPC is applied into high power CSC-fed MV IM drive, which achieves a fixed switching frequency with PWM waveform following space vector pattern of SVM, and improves dynamic response in contrast to traditional SVM scheme. The weighting factor selection issue is eliminated in MPSVPC as well as MPSPC;

6) Common-mode voltage reduced model predictive control (RCMV-MPC) scheme is proposed for high power CSC-fed MV IM drive

CMV would lead to the premature failure of motor winding insulation system, and shorten the life expectancy of motor, so the magnitude of CMV needs to be mitigated. The proposed RCMV-MPC scheme uses the prediction model of the CMV in high power CSC-fed MV IM drive to reduce the peak value of CMV. RCMV-MPC reduces the CMV peak value to only around 40% of that by conventional SVM. Moreover, compared to zero-state vector selection based RCMV-SVM, nearly 40% reduction on CMV peak value can be achieved in different operating states of IM with RCMV-MPC;

7) Simulation and experimental studies are conducted to validate the performance of the proposed schemes

All the simulations are carried out using MATLAB/Simulink software aiming a megawatt MV IM drive system. On the other hand, all the theory, control system design, and simulation have been validated through the tests on a low power CSC-fed IM drive.

7.2 Future Work

The following future research works are suggested as an extension to the knowledge presented in this dissertation.

1) Comparison of MPC schemes between VSC and CSC

The thorough comparison can be carried out between MPC schemes for VSC and CSC. Some features based on output performance and individual special issues can be unveiled to distinguish the application of MPC on these two kinds of converters;

2) Operation of the proposed scheme under unbalanced utility supply fault condition

Investigation of the proposed scheme for CSR under unbalanced utility supply fault condition and development of new control schemes denote a very good research direction to meet the emerging grid code requirements;

3) Application of MPC approach to multilevel current-source converter (MCSC)

In order to increase the power rating of motor drive system, several CSCs are possibly connected in parallel, and operated as a MCSC. Hence, appropriate MPC scheme for MCSC is also deserved to be studied in terms of the increment on difficulty of designing modulation scheme for MCSC.

Appendix A

Per-Unit Values for CSC System

A.1 Base values for AC-side quantities

The base values for a CSC system AC-side quantities are given in Table A.1.

Table A.1 BASE VALUES FOR CSC-SIDE QUANTITIES

Quantity	Symbol and Expression	Description
Apparent power	$S_B = \frac{3}{2} V_B I_B$	The rated power of induction motor or power converter
Active power	P_B	The rated induction motor mechanical output power or rated converter output power
Voltage	V_B	Amplitude of nominal line-to-neutral voltage
Current	$I_B = \frac{2S_B}{3V_B}$	Amplitude of nominal line current
Impedance	$Z_B = \frac{V_B}{I_B}$	
Frequency	$\omega_B = \omega_0$	Utility power supply nominal frequency
Inductance	$L_B = \frac{Z_B}{\omega_B}$	
Capacitance	$C_B = \frac{1}{\omega_B Z_B}$	
Flux-linkage	$\Phi_B = \frac{V_B}{\omega_B}$	
Torque	$T_B = \frac{P_B}{\omega_B}$	

A.2 Base values for DC-side quantities

The DC-side base values are determined based on those of the AC side. The base power is the same for both DC and AC sides. The DC-side base current is defined to be equal to the AC-side base current. The base values for DC-side quantities are summarized in Table A.2.

Table A.2 BASE VALUES FOR CSC DC-SIDE QUANTITIES

Quantity	Symbol and expression	Description
Power	$P_{B\_dc} = V_{B\_dc} I_{B\_dc} = P_B$	Same as AC-side base power
Current	$I_{B\_dc} = I_B$	
Voltage	$V_{B\_dc} = \frac{3}{2} V_B$	
Impedance	$Z_{B\_dc} = \frac{3}{2} Z_B$	
Inductance	$L_{B\_dc} = \frac{3}{2} L_B$	
Capacitance	$C_{B\_dc} = \frac{2}{3} C_B$	

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