

DESIGN TECHNIQUES FOR PASSIVE WIRELESS MICROSYSTEMS

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ABSTRACT

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The unique advantage of harvesting power wirelessly has evolved passive wireless microsystems to a fast-growing high-impact technology. In this dissertation, several new design techniques are proposed for the increasingly stringent requirements of passive wireless microsystems. The absence of on-board batteries imposes ultralow power consumption of passive wireless microsystems. Recent research reveals that multi-voltage systems-on-a-chip dramatically reduce power consumption such that power-efficient on-chip voltage level shifters are critically needed. This dissertation proposes a novel set of voltage level shifters built upon diode-based clamper-rectifier configurations. The voltage level shifters are passively powered by incoming signals with no static current consumption and are able to shift the incoming signals bidirectionally to suit the different voltage domains. The shifting steps could be continuous and are not bounded by the discrete transistor thresholds and power rails. A second bottleneck of passive wireless microsystems is the wireless power-harvesting efficiency that limits the wireless communication distance and the on-chip circuitry complexity and functionality. This dissertation proposes a transformer-based impedance matching network that greatly improves the power transfer efficiency from the receiving antenna to the on-chip circuit loads. The transformer is also capable of automatically calibrating its input impedance to match to the antenna impedance by a novel low-power varactor current tuning technique. In passive wireless microsystems, data modulation scheme largely determines the power transmission efficiency and data communication speed. Exploiting the constant carrier envelop of FSK modulation, this dissertation proposes a dual-tank architecture for FSK receivers in passive wireless microsystems. The dual receiving tanks significantly im-

proves the power conversion efficiency of on-chip AC-to-DC voltage multipliers by providing high-quality-factor resonating tank voltages at each of the alternating FSK carriers. High data transmission rate is also achieved by exploring the dual tanks in an all-digital and a voltage-level shifting FSK demodulators.

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Abbreviations

<i>AC</i>	Alternating Current
<i>ADC</i>	Analog-to-Digital Converter
<i>ADS</i>	Advanced Design Systems
<i>AM</i>	Amplitude Modulation
<i>ASK</i>	Amplitude-Shift Keying
<i>BSIM</i>	Berkeley Short-channel IGFET Model
<i>CAD</i>	Computer-Aided Design
<i>CMOS</i>	Complementary Metal-Oxide Semiconductor
<i>dBm</i>	Decibel with respect to 1 Milliwatt
<i>DC</i>	Direct Current
<i>EEPROM</i>	Electrically Erasable Programmable Read-Only Memory
<i>EM</i>	Electromagnetic
<i>EPC</i>	Electronic Product Code
<i>FF</i>	Fast(NMOS)-Fast(PMOS)
<i>FM</i>	Frequency Modulation
<i>FS</i>	Fast(NMOS)-Slow(PMOS)
<i>FSK</i>	Frequency-Shift Keying
<i>GHz</i>	Giga Hertz

<i>IBM</i>	International Business Machines
<i>IGFET</i>	Insulated-Gate Field-Effect Transistor
<i>ISM</i>	Industrial Scientific Medical
<i>ISO</i>	International Organization for Standardization
<i>LC</i>	Inductor-Capacitor
<i>LO</i>	Local Oscillator
<i>Mbps</i>	Mega Bit Per Second
<i>MHz</i>	Mega Hertz
<i>MIM</i>	Metal-Insulator-Metal
<i>MOSFET</i>	MetalOxideSemiconductor Field-Effect Transistor
<i>NMOS</i>	N-type Metal-Oxide-Semiconductor
<i>NRZ</i>	Non-Return-to-Zero
<i>PLL</i>	Phase-Locked Loop
<i>PMOS</i>	P-type Metal-Oxide-Semiconductor
<i>POR</i>	Power-ON Reset
<i>PSK</i>	Phase-Shift Keying
<i>PVT</i>	Process Voltage Temperature
<i>reltol</i>	relative tolerance
<i>RF</i>	Radio Frequency
<i>RFID</i>	Radio Frequency Identification
<i>RLC</i>	Resistor-Inductor-Capacitor
<i>SF</i>	Slow(NMOS)-Fast(PMOS)
<i>SS</i>	Slow(NMOS)-Slow(PMOS)

<i>THD</i>	Total Harmonic Distortion
<i>TT</i>	Typical(NMOS)-Typical(PMOS)
<i>UHF</i>	Ultra High Frequency
<i>VCO</i>	Voltage-Controlled Oscillator

Chapter 1

Introduction

RF powered microsystems, also known as passive transponders, are critically needed in many applications such as automated payment systems, irretrievable pressure sensors in cement structures, and remote tracking devices. They have also found emerging applications in implantable electronics [1, 2, 3, 4, 5, 6], retinal prosthetic device [7], neuromuscular stimulation [8], wireless environmental monitoring [9], RFID [10], and medical endoscopy [11, 12], to name a few. Its most recent evolution involves passive transponders harvesting RF energy from ambient or dedicated sources such as mobile telephones, handheld radios, mobile base stations, and television/radio broadcast stations [13, 14]. The great advantage of a passive transponder is not having a power supply on-board. This enables it to operate indefinitely without requiring a battery exchange or recharge. Moreover, not having a power source attached to them, the transponders can be manufactured in very small sizes, free of connectors, cables and battery access panels, making them attractive for producing consumer electronics such as e-book readers and headsets, and ASIC sensors for implantable discrete wireless nodes and RFID tracking tags.

In this chapter, we first introduce some of the basic background information of wireless passive microsystems in Section 1.1. We then discuss some of the current design issues in passive microsystems in Section 1.2 for our motivations and objectives. Section 1.3 presents the contributions of this dissertation. The organization of the dissertation is briefly described in Section 1.5. The chapter is summarized in Section 1.5.

1.1 Background

RF powered microsystems originate from the idea of wireless power transmission (WPT) which was proposed by Tesla early in 1899 [1]. In 1964, Brown et al. successfully demonstrated a working concept of a microwave-powered helicopter [2]. Recent research discovered that low-power wireless passive transponders can be powered by ambient RF energy such as mobile base stations, mobile phones, WiFi, Bluetooth and ZigBee [15, 16]. Wireless passive microsystems mainly operate by means of coupling through electric or magnetic fields. Inductive coupling of the magnetic field has been widely employed over short ranges with high efficiency using resonance magnetic coupling [2]. The second type, so-called rectenna, most often combines a rectifier and an antenna, coupling the power via electric field. The mix of magnetic and electric field couplings to form RF wave propagation for wireless passive microsystem enables a smaller scale integration of functionalities over longer operating distances. An RF powered transponder is a small wireless system that communicates with a nearby station called the reader. An illustration of the basic structure of an RF power microsystem comprising of a reader and a transponder is shown in Fig.1.1. The reader provides the transponder with power and initial information through a wireless channel. The reader-transponder communication protocol always starts with a relatively long power-up period during which the storage capacitor of the transponder is charged to an operational level [1]. At this point, the reader may send a data request which will be acknowledged by the transponder should the requested data be available. The transponder data are usually sensor readings or identification codes. These data are processed by the reader to gain the knowledge of the transponder's environment or identify subjects carrying the device.

1.1.1 Architecture

The architecture of an RF powered transponder has two majors layers: (1) an RF front and (2) baseband data units. The baseband circuits provide processing, generation and/or storage of baseband data or any combination of the three. These units may include EEPROMs for the storage of long ID codes, ADCs for quantizing sensor readings or even microprocessors that provide basic data/signal processing at the transponder. Fig.1.2 is the

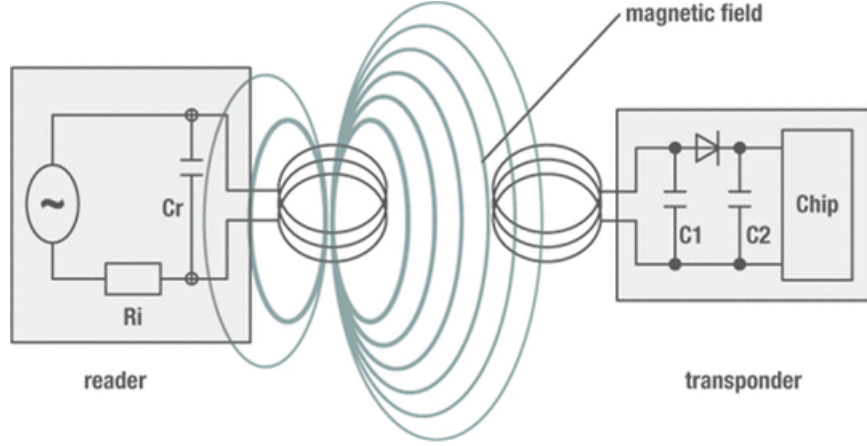


Figure 1.1: Basic structure of RF power microsystem.

block diagram of a generic transponder architecture. All these blocks will have very stringent power constraints in an RF powered microsystem. Design for lower power consumption remains the top challenge. The study of baseband circuits, however, is beyond the scope of this dissertation and will not be discussed here.

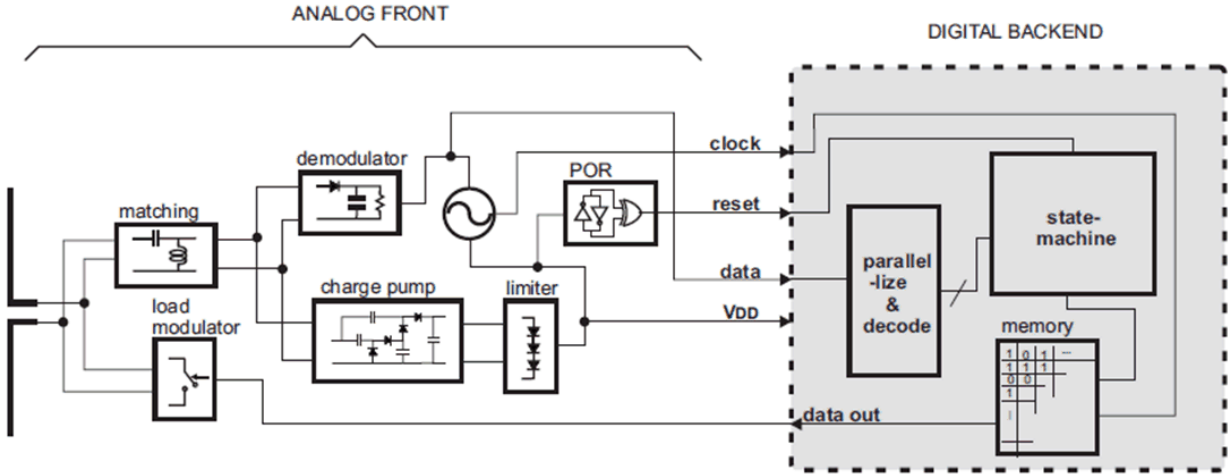


Figure 1.2: Architecture of a typical passive transponder device.

The RF front is responsible for the supply of power to the chip, and the wireless data interface with the reader. Major RF front components are an antenna, a matching network, a RF-to-DC converter, a modulator and a demodulator. The matching network and RF-DC

conversion block are some times together referred to as the RF power harvester. Each block will be briefly described here, and a more detailed presentation will be given in the following chapters.

1.1.2 Antenna

The antenna supplies the chip with power by gathering the electromagnetic wave emitted by the reader. It also receives the envelope of data modulated by the reader on the same carrier that provides the power. The shape and dimensions of the antenna are determined by the carrier wavelength, channel bandwidth and polarization of the EM field. For example, lower frequency (near-field) transponders often use magnetic coils whereas dipole, folded-dipole and meander-line antennas are popular configurations in UHF and microwave transponders. A small loop antenna is also popular geometry especially when the dimension of the antenna is required to be significantly smaller than the wavelength. Another advantage of the small loop antenna is its large inductive reactance which could be used to create a passive voltage gain in the received signal for better power harvest. Fig.1.3 shows different antennas used in passive transponders.

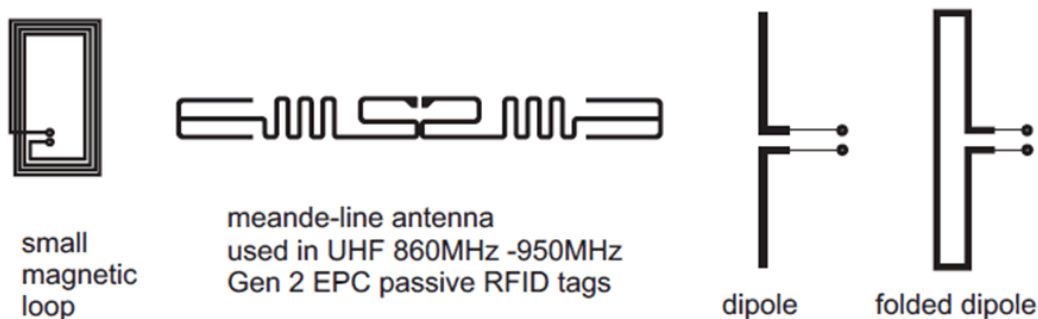


Figure 1.3: Popular antenna geometries for RFIDs and passive transponders.

1.1.3 Matching Network

Regardless of the configuration, the impedance of the antenna has to be matched to input impedance of the chip to ensure the maximum transfer of power. This is accomplished by using a power matching block, which is a network of inductors and capacitors. Since these elements have purely imaginary impedances, ideally the power matching network does not dissipate power. However, due to the conductive loss of the inductor traces, the efficiency of the matching network becomes a challenging issue especially in on-chip matching where, in addition to the conductive loss, a significant portion of the available power is consumed in the substrate. The loss of energy in the substrate is mainly due to the Eddy currents caused by the coupling of electric and magnetic fields into the substrate. Another power-matching issue is the variation of the chip impedance under different loading conditions and the proximity of the reader. Power matching will be further discussed in Chapter 3. Fig.1.4 shows topologies of some popular matching networks. Fig.1.4 (a), (b) and (c) are widely used in transponders [10, 17, 18] while Fig.1.4 (d) is proposed in this dissertation for on-chip RF power matching in transponders.

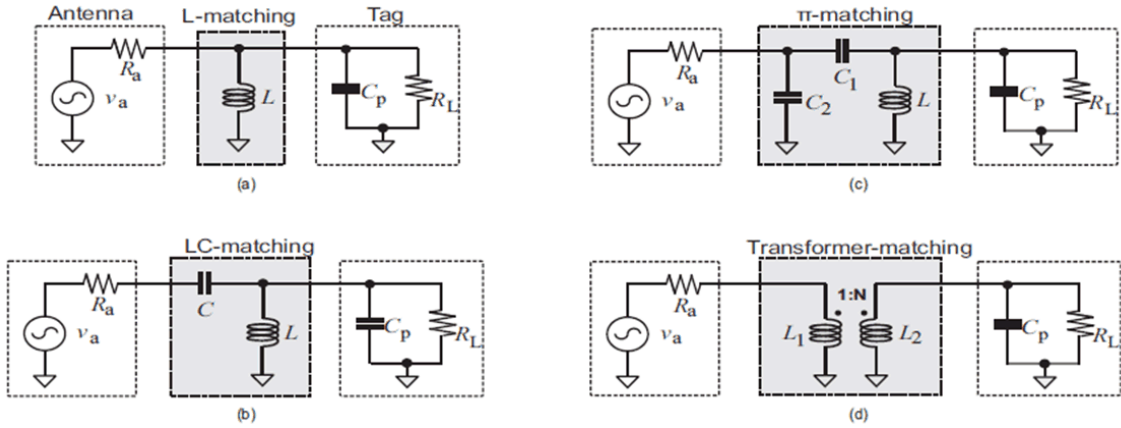


Figure 1.4: (a), (b) and (c): Matching network topologies for RF power harvesting. (d) Transformer power matching circuit proposed in this dissertation.

1.1.4 Rectification

RF-to-DC conversion is implemented using rectifiers or voltage multipliers. At higher frequencies, however, due to a smaller antenna aperture, the signal at the transponder is weak. Most transponders operating at these frequencies use special rectifying charge-pump circuits to boost the voltage of the signal. Such architectures are called voltage multipliers. The DC output of a voltage multiplier is normally higher than the peak of the AC voltage applied. The main challenge in the design of voltage multipliers is the conversion efficiency which is typically less than 30% in most reported designs. In fact, efficiencies higher than 15% can only be achieved by the use of non-standard features such as Shockley diodes or silicon-on-insulator technologies [19, 10, 20]. Fig.1.5 shows two of the charge-pump topologies that are widely used in passive transponders [20, 21].

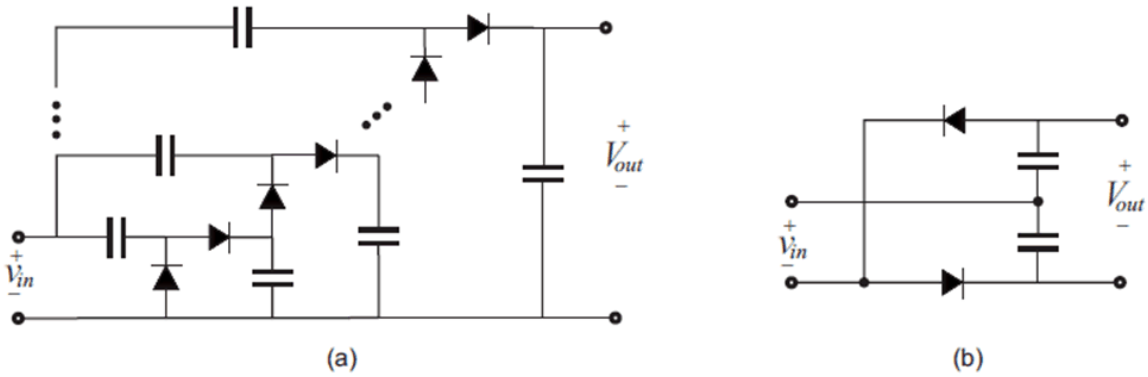


Figure 1.5: Dickson charge-pump and Nakamotos dual half-wave rectifier widely used for RF signal rectification and voltage boost in transponders.

1.1.5 Modulation Backscatter/Load Modulation

In passive wireless microsystems, the absence of a power source makes the transmission of signals from the transponder challenging. Most designs do not allocate any DC power for RF transmission. Instead, they utilize a phenomenon called backscattering or backscatter modulation. Backscatter in antennas is similar to the reflection phenomenon in radars. Here, a portion of the received signal is reflected from the antenna back to the reader. The

amount of the power reflected and the delay of the reflected wave are determined by the input impedance seen between the two terminals of the receiver antenna. Therefore, by modulating the termination impedance (or load) of the antenna, the reflected wave is modulated. Load modulation eases the power constraint of the design. In fact, by using this method along with other low-power design techniques, some of the recent UHF and microwave transponders have been able to lower the overall power consumption to a few microwatte, whereby increasing the operational range to over 12 meters while keeping the readers transmission powers within ISM bands regulations [20, 10]. Fig.1.6 shows the principle of backscattering in passive transponders.

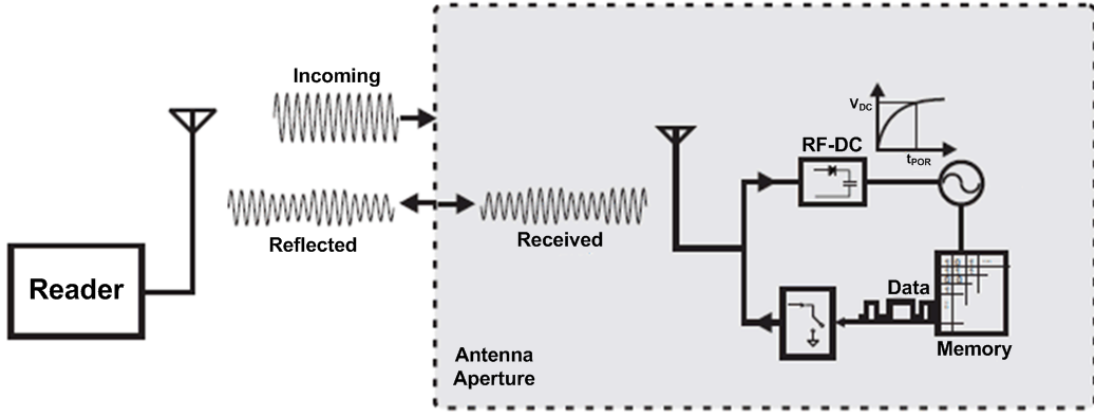


Figure 1.6: Different matching network topologies for RF power harvesting. Transformer power matching circuit is proposed in this dissertation.

1.1.6 Demodulation

As shown in Fig.1.2, the demodulator is located in parallel with the RF-DC conversion block, and draws a small fraction of the total RF current flowing into the chip. Due to power limitations, demodulation is usually done incoherently using an envelope detector followed by gain and signal quantizing circuits. Since the received signal must be large enough to power the device, envelope detection is well feasible in most cases.

1.1.7 Industry Standard

Table 1.1: RFID Standards

Band	Regulation	Range	Data Speed	Standards
120-150 KHz	Unregulated (LF Band)	10 cm	Low	ISO 11784 ISO/IEC 18000-2A ISO/IEC 18000-2B
13.56 MHz	ISM Band (HF Band)	1 m	Low to Moderate	ISO/IEC 14443 ISO/IEC 15693 ISO/IEC 18000-3
433 MHz	ISM Band for Short Range Devices (UHF Band)	1-100 m	Moderate	ISO 18000-7 ISO 18000-7 ISO 18000-7
865-868 MHz (Europe) 902-928 MHz (North America)	ISM Band (UHF Band)	1-2 m	Moderate to High	ISO 18000-6A ISO 18000-6A ISO 18000-6B ISO 18000-6C Class 0 Class 1 Class 1 Gen 2
2.45-5.80 GHz (Microwave)	ISM band (SHF Band)	1-2 m	High	ISO 18000-4 ISO/IEC 24730-2

The fast evolution of wireless passive microsystems prompts national and international committees to set standards for its vastly diverse applications. Due to the continuously emerging technologies for new passive devices and systems, only a portion of the applications have been standardized in industries, especially for RFID applications. A number of organizations have set standards for RFID, including the International Organization for Standardization (ISO) and EPCglobal, etc. One of the early popular ISO RFID standards, known as ISO 15693, addresses contactless integrated circuit devices, which are used in security access and payment systems. ISO later developed a new series of standards, known as ISO 18000 family, to address how tags and readers communicate in a number of item identification applications. For example, ISO 18000 part 3, identifies 13.56 MHz as the

frequency for tag-reader communication in its industrial and medical applications. Table 1.1 briefly summarizes some of the most popular RFID standards with its frequency bands, where the ISM bands are internationally reserved for industrial, scientific and medical purposes other than communications. The particular frequencies of the circuits proposed in this dissertation are ISM-HF band at 13.56 MHz and SHF-microwave band at 2.45 GHz.

1.2 Motivation and Objectives

Despite the numerous advantages of wirelessly powered passive microsystems, challenges in such systems must be overcome for the advantages to be feasible. These include the challenges of an efficient RF-power-receiving small antenna mentioned in Section 1.1.2, efficient matching networks for variations of input power and output loading impedances mentioned in Section 1.1.3, superior RF-to-DC power conversion efficiency mentioned in Section 1.1.4, novel low-power modulation/demodulation circuitries mentioned in Section 1.1.5 and 1.1.6, and optimization of wireless passive microsystem architectures.

1.2.1 Voltage Level Shifters

Due to the very limited power received in passive microsystems, each block in the architecture of a passive microsystem in Fig.1.2 has to be optimized for full functional operation with low-power consumption. In this dissertation, a family of low-power passive voltage level shifters will be proposed in Chapter 2. By properly configuring the proposed voltage level shifters, the demodulator block in Fig.1.2 can be implemented for low-power ASK and FSK wireless demodulation schemes. The proposed voltage level shifter can also be applied in the matching network block in Fig.1.2 for auto-calibration of the matching network to achieve the maximum power harvest. We will see such an auto-calibration peak amplitude detection technique by voltage level shifting in Chapter 3. Furthermore, to lower power consumption in passive wireless microsystems, devices in non-critical portion of these systems often operate in a sub-threshold mode with a reduced supply voltage while other blocks such as electronically erasable programmable read-only memories operate in a super-threshold mode with a higher supply voltage [22, 23, 10]. Voltage level shifters that provide

proper voltage signals to bridge sub-threshold and super-threshold blocks are needed [24, 25]. Voltage level shifters are commonly implemented in the following topologies: (1) Half-Latch Topology: a half-latch topology is to take the advantage of its simple configuration subsequently a small propagation delay. These voltage level shifters, however, suffer from a long propagation delay, large pull-down NMOS transistors, and an excessive short-circuit current. The low current driving ability of half-latch voltage level shifters can be mitigated by replacing the pull-up PMOS latch with a current mirror, however, at the cost of excessive static power consumption [26]. (2) Bootstrapping Technique: Bootstrapping technique reduces the power consumption of half-latch voltage level shifters by driving pull-up PMOS and pull-down NMOS with separate low-swing signals [27]. Among the bootstrapping techniques, the voltage level shifter proposed by Kwon and Min improves speed and lowers power consumption by employing an auxiliary level shifter [28]. (3) Subthreshold-Superthreshold Conversion: Ltkemeier and Rckert proposed a Wilson current mirror based voltage level shifter for subthreshold-to-superthreshold signaling [29]. The energy-efficient subthreshold voltage level shifter proposed by Wooters et al. used low- V_{TH} transistors to interface with the low- V_{DD} circuitry feeding the voltage level shifters so as to boost the current-driving ability [30]. (4) Gate Coupling Technique: Baek *et al.* proposed a power efficient up-converter by coupling the gate of protection transistors to the input capacitively [31]. (5) Multi- V_{TH} Transistor Topology: The voltage level shifter by Hasanbegovic and Aunet utilizes multi- V_{TH} transistors with low- V_{TH} transistors placed in locations where speed is critical and high- V_{TH} transistors placed in locations where leakage current is essential [32].

The preceding voltage level shifters only provide digital signaling and cannot provide continuous voltage level shifting. Although source followers, common-source, common-gate configurations or circuits alike are handy choices for shifting the median value of analog signals, their usefulness in low-power applications is largely hindered by the following factors: (1) the excessive static power consumption, (2) the minimum amount of the voltage shift that these voltage shifters can provide is typically lower-bounded by the gate-source voltage of MOSFETs in saturation, and (3) the maximum amount of the voltage shift that these voltage shifters can provide is upper and lower bounded by the voltages of the power rails, further limiting their applications in systems such as passive wireless microsystems where the

output of the power harvesters of these systems is typically much higher than the amplitude of the received radio-frequency signals.

In this dissertation, we will propose a different kind of voltage level shifters built upon the rectifying characteristics of diode-based voltage multipliers. We will demonstrate that these voltage level shifters are capable of removing the drawbacks of the aforementioned voltage level shifters.

1.2.2 Impedance Matching

Passive microsystems are not equipped with internal batteries. Their operating power has to be harvested wirelessly. Illustrated in Fig.1.2, the power harvesting module includes an antenna, a matching network and a charge-pump voltage multiplier. The matching network needs to be optimized for the maximum power transfer from the antenna to the voltage multiplier. The voltage multiplier ideally requires the input voltage magnitude as large as possible for efficient AC-DC conversion. The efficiency of power harvest determines the maximum distance over which reliable links between base stations and microsystems can be established, the complexity subsequently the functionalities of microsystems, and the minimum amount of time required to harvest a sufficient amount of power. The efficiency of radio-frequency power harvest is mainly determined by three key factors listed as follows: (1) Efficiency of Antenna: The higher efficiency of the antenna induces a larger voltage in the antenna. The voltage generated by an antenna is determined by the type and dimensions of the antenna, both of which are usually set by applications. (2) Efficiency of Voltage Multiplier: An effective approach to improve the efficiency of voltage multipliers is to maximize the input voltage fed into the voltage multipliers from the antenna [33]. The loss of the power conversion efficiency of voltage multipliers is due to the voltage drop of the rectifying devices [18, 21, 19]. It can be improved by increasing the amplitude of the input voltage or using low-threshold rectifying devices, such as Shockley diode and zero- V_T MOSFETs [20]. (3) Accuracy of Impedance Matching Network: The voltage at the input of voltage multipliers can be boosted using a resonant tank inserted between the antenna and the voltage multiplier that resonates at the carrier frequency [10, 34, 17, 35, 36]. To maximize the input voltage, in [33], an inductive matching technique is proposed to shunt

the input of a voltage multiplier with a parallel inductor for a resonant LC tank utilizing the equivalent input capacitance of the voltage multiplier. A further boost of the input voltage across the voltage multiplier is obtained by applying a LC matching network at the input of the voltage multiplier [17, 35, 36]. The effectiveness of resonating LC tanks is severely affected by the low quality factor of on-chip spiral inductors. Also, if a varactor is employed to provide frequency tuning, the resistive loss of the varactor will also have a detrimental effect on the quality factor of the tank. The performance of the LC matching network, in particular, the voltage gain, can be largely improved by replacing the spiral inductor with a step-up spiral transformer [37]. (4) Optimum Loading of Impedance Matching Network: Instead of finding the optimum matching network, [38] analyzed the optimum load that yields the maximum possible power efficiency under arbitrary input impedance conditions. For the step-up spiral transformer introduced in [37], the large turn ratio and the wide spiral of the primary winding yield a large quality factor and a large voltage gain. Since the load of the voltage multiplier varies with applications, the input impedance of the transformer matching network with a voltage multiplier load at its secondary winding will also vary, giving rise to an impedance mismatch between the antenna and the transformer subsequently the loss of energy transferred from the antenna to the transformer. In addition, process-spread also gives rise to errors in the inductances, parasitic capacitances and resistances of the transformer, resulting in process-spread induced drift of the input impedance and resonant frequency of the transformer matching network. The former affects the amount of power transmitted from the antenna to the transformer while the latter impacts the output voltage of the transformer especially when the quality factor of the transformer is high. It is highly desirable that the parameters of the transformer matching network can be tuned such that it will not only provide a matching impedance to the antenna to maximize energy transfer from the antenna to the transformer, but also resonate at the desired frequency, i.e., the carrier frequency, to maximize the voltage of the secondary winding of the transformer.

This dissertation proposes a transformer impedance matching and frequency tuning technique for high-efficiency power harvest of passive wireless microsystems. The proposed method utilizes a step-up transformer inserted between the antenna and voltage multiplier

to perform both impedance transformation for power matching and voltage amplification for improving the efficiency of the voltage multipliers.

1.2.3 FSK Demodulator

There are different modulation techniques for wireless passive microsystems, among which ASK has been the most popular one due to its simple implementation subsequently low power consumption. FSK modulation has been recently used in passive wireless microsystems for its constant-envelope modulation scheme. When FSK is used to encode the data transmitted from a base station to a passive wireless microsystem, the drawback of fluctuating power transmission encountered in ASK is eliminated. Since baseband data are represented by the frequency rather than the amplitude of the carrier, the effects of noise and disturbances on data transmission are also reduced. Another unique characteristic of FSK is its ability to transmit data at a high data rate owing to the fact that the demodulation of a FSK-modulated signal does not need to extract the envelope of the carrier using a low-pass filter with a large time constant. This is particularly important for biomedical implants as not only is the data rate of these microsystems such as cochlear implants and visual prosthesis implants high, the carrier frequency of these implants is typically 13.56 MHz due to the high degree of the absorption of electromagnetic waves by human bodies at high frequencies.

In FSK-based passive wireless microsystems, the quality factor of the coupling transformer between passive wireless microsystems and their base station is typically maximized in order to boost the amplitude of the received RF signal so as to maximize the power efficiency of downstream voltage multipliers [39]. Maximizing the quality factor of the coupling transformer, however, lowers the power efficiency when FSK is used as FSK modulates baseband data using two carriers whose frequency is largely distinct. To ensure that the amplitude of the received signal at both carrier frequencies is the same, the two carrier frequencies must be equally spaced from the resonance frequency of the coupling transformer resulting in a reduced power efficiency. To improve power efficiency, several techniques have been proposed: (1) Ghovanloo and Najafi proposed a wideband inductive link composed of a serial combination of a parallel and a series LC tanks on the transmitter side and a LC tank

on the receiver side [40]. The two LC tanks on the transmitter side are tuned to resonate at FSK carrier frequencies in order to maximize the voltage of the transmitted signal. Since the coupling transformer only resonates at a single frequency, the power efficiency of this FSK demodulator is still low. (2) Jung et al. proposed a simple FSK demodulator using elements to delay and sample the received FSK signal [41]. As compared with Ghovanloo-Najafi FSK demodulator, Jung FSK demodulator recovers the baseband data by sampling the incoming data at a specific time instant rather than measuring the period of the two sinusoids of the carrier. The elimination of the high-frequency oscillator used in Ghovanloo-Najafi FSK demodulator effectively lowers power consumption. The price paid, however, is the reduced degree of reliability. (3) The FSK demodulator proposed in [42] consists of a multiplexer, a shift register, a phase-frequency detector, and a charge-pump. (4) A stagger-tuning technique proposed in [43] improves power efficiency of FSK demodulators by separately tuning the transmitter and receiver tanks.

A common deficiency of the preceding FSK demodulators is their low power efficiency due to the low amplitude of the received FSK-modulated signal. This dissertation proposes a new dual-tank FSK demodulator using dual receiving LC tanks to boost the amplitude of the received signal at two FSK carrier frequencies, subsequently the power conversion efficiency of the following voltage multipliers. In addition, a full-wave voltage quadruple voltage multiplier is proposed to produce a dual-polarity supply voltage used by the FSK demodulator.

1.3 Contributions

This section summarizes the original contributions of this dissertation.

1.3.1 Passive Voltage Level Shifters

This dissertation proposes a family of low-power passive voltage level shifters. We show that the median value of an analog signal can be shifted in either positive or negative directions. The amount of voltage shift can be either a multiple or a fraction of the amplitude of the input signal with no restriction on the amplitude of the input signal. The proposed

voltage level shifters are powered by the input signal and are truly passive, making them particularly attractive for applications such as passive wireless microsystems where power consumption is of a critical concern. The simple configuration of the voltage level shifters also makes them well suited for high-frequency applications. The novelties of the proposed passive voltage level shifters include: (1) A current compensation technique for voltage clampers, (2) cascaded passive voltage level shifter architecture, (3) superimposed passive voltage level shifter architecture, and (4) low-leakage voltage rectification technique. An in-depth mathematical treatment and extensive simulation results of the proposed voltage level shifters are given. The layout and on-chip wafer measurement results of fabricated passive voltage level shifters are provided.

1.3.2 High-Gain On-Chip Transformer Impedance Matching

We propose a transformer impedance matching and frequency tuning technique to tune both the input impedance and resonant frequency of the transformer matching network so as to minimize the energy loss due to impedance mismatch and the efficiency loss of voltage multipliers due to voltage reduction. The novelties of the proposed transformer impedance matching and tuning techniques include: (1) a step-up transformer impedance matching technique for voltage gain boosting, (2) a varactor frequency tuning technique for reducing the efficiency loss of voltage multipliers, (3) an ultra-low power current tuning technique to overcome the drawbacks of widely used voltage tuning techniques for varactors, and (4) an ultra-low power self-tuning technique to find the optimum tuning state by automatic peak detection using the proposed voltage level shifter. The detailed mathematical analysis and circuit simulation results of the proposed transformer impedance matching network with automatic calibration are given. The layout and on-chip wafer measurement results of the transformer impedance matching network are provided.

1.3.3 Power-Efficient Dual-Tank FSK Demodulator

New dual-tank FSK demodulators using dual receiving LC tanks to boost the amplitude of the received signal at two FSK carrier frequencies subsequently the power efficiency are provided. The novelties of the proposed dual-tank FSK demodulator include: (1) a new

parallel resonant-tanks' architecture to boost the amplitude of the received signal at two FSK carrier frequencies subsequently the power efficiency, (2) a new full-wave quadruple voltage multiplier architecture to produce a dual-polarity supply voltage used by the FSK demodulator, and (3) a shunt switching technique to accelerate the energy depletion of the receiving LC tank when the other receiving tank starts to resonate so as to improve the data rate. Extensive simulation results of the dual-tank architecture in practical inductive ambients are given. Its applications in an all-digital FSK demodulator and a voltage-shifting FSK demodulator are explored in detail.

1.4 Dissertation Organization

The remainder of this dissertation is organized as the followings:

- Chapter 2 presents a family of ultra-low-power high-speed passive voltage level shifters for analog signaling.
- Chapter 3 presents a high-gain high-power-efficiency self-tunable transformer impedance matching technique for wireless power harvest.
- Chapter 4 presents a power-efficient dual-tank FSK demodulator for low-power high-speed passive FSK communication.

1.5 Chapter Summary

In this chapter we presented an overview of passive wireless microsystems. A brief introduction to the architecture of passive transponders and the wireless protocols for communication between transponders and readers was presented. The fundamental building blocks of the front end of passive transponders were examined in terms of their functionality, implementation, and design challenges. The design challenges and motivations of voltage level shifting for analog signals, antenna impedance matching for maximum power harvest, and FSK communication employing high quality-factor inductive tanks were addressed. New design techniques proposed in this study were briefly presented.

Chapter 2

Passive Voltage Level Shifters

Subthreshold operation is an emerging design technique to achieve low power consumption of passive wireless microsystems [22, 23]. This advantage arises from multi-voltage system design techniques where the critical parts of the passive microsystem operate in conventional super-threshold mode with a higher supply voltage, while the vast majority of the non-critical parts of the passive microsystem operates in subthreshold mode with a reduced supply voltage [24, 44]. The resulting multi-voltage subthreshold systems-on-a-chip (SoCs) lead to significant power reduction in passive wireless microsystems [32]. Resource-efficient on-chip voltage level shifters that bridge the different voltage islands within an SOC are therefore critically needed to interface subthreshold circuit modules with super-threshold modules. To compare performances of voltage level shifters, common benchmarks are its operating frequency, voltage shifting high/low levels, propagation delay and the power consumption.

In Section 1.2.1, the existing popular voltage level shifting topologies were briefly discussed. The common drawbacks of existing topologies include large static current consumption and discrete shifting levels bounded by transistor threshold levels and power supply rails. This chapter proposes a family of low-power passive voltage level shifters, whose contributions to a general passive wireless microsystem are shown in Fig. 2.1. We show the median value of an analog signal can be shifted in either positive or negative directions. The amount of voltage shift can be either a multiple or a fraction of the amplitude of the input signal with no restriction on the amplitude of the input signal. The proposed voltage level shifters are powered by the input signal and are truly passive, making them particularly

attractive for applications such as passive wireless microsystems where power consumption is of a critical concern. The simple configuration of the voltage level shifters also makes them well suited for high-frequency applications.

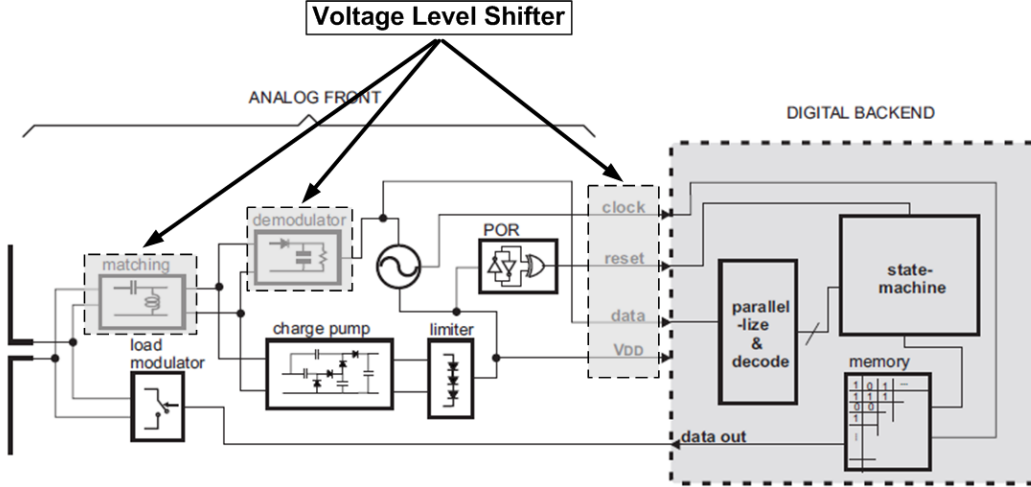


Figure 2.1: Contributions of the proposed voltage level shifters to a general passive wireless microsystem.

The remainder of the chapter is organized as following: Section 2.1 presents the operation of basic voltage level shifters. Section 2.2 proposes voltage level shifters with current compensation. Section 2.3 presents cascaded voltage level shifters and superimposed voltage level shifters that provide tunable voltage shift. In Section 2.4, a technique that minimizes the leakage of MOSFET diodes subsequently the power consumption of the proposed voltage level shifters is presented. Section 2.5 examines the key factors that affect the design of the proposed voltage level shifters and applies the voltage level shifter in high-speed ASK demodulation. The layouts and measurement results of the proposed voltage level shifters are presented in Section 2.6. Finally, the chapter is concluded in Section 2.7.

2.1 Basic Voltage Level Shifters

Consider the circuit in Fig.2.2. Let $v_{in}(t)$ be a sinusoid and assume diode is ideal. In the negative half cycle of v_{in} , C1 is charged by v_{in} . v_{clamp} is kept at 0 V by D1. When v_{in}

passes its minimum at $t = t_1$, $v_{clamp} = v_{in} + v_{c1} > 0$, D1 turns off. Since $v_{clamp} = v_{c1} + v_{in}$, with $v_{c1}(t_1^-) = V_m$, v_{clamp} rises to V_m and remains at V_m until the end of the negative half cycle ($t = t_2$). During $t_1 < t \leq t_2$, D1 is off and v_{clamp} climbs to V_m . In the following positive half cycle of v_{in} , i.e. $t_2 < t \leq t_4$, since D1 is off, v_{clamp} will follow v_{in} with a voltage offset V_m . It is evident that v_{clamp} is the up-shifted version of v_{in} . The voltage clamper thus behaves as a voltage level shifter that shifts the median value of the input signal by V_m .

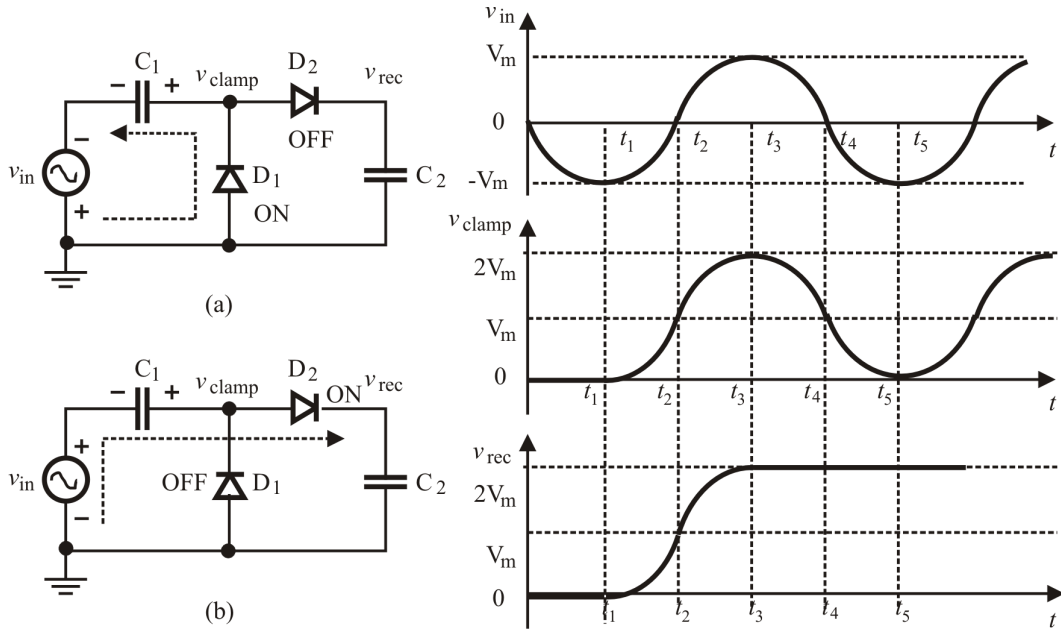


Figure 2.2: Positive voltage double with ideal diodes. The voltage of the clamping node v_{clamp} is a up-shifted version of the input.

When diodes are realized using MOSFETs, a voltage loss v_{gs} exists where v_{gs} is the gate-source voltage of MOSFETs. The voltage swing of the clamping node in this case becomes $-V_{TH} \leq v_{clamp} \leq 2V_m - V_{TH}$, and the voltage of the rectifying node is given by $v_{rec} = 2(V_m - V_{TH})$, where V_{TH} is the threshold voltage of MOSFETs. Note that when $v_{gs} < V_{TH}$, the transistors are in weak inversion and conduct a small current. The effective value of V_{TH} at which the current of the transistors is typically much smaller than the nominal value of V_{TH} required to operate the devices in strong inversion. A negative voltage level shifter can also be constructed conveniently by changing the direction of the diodes.

2.2 Voltage Level Shifters with Current Compensation

A close examination of the preceding voltage level shifter reveals that the median value of the voltage at the clamping nodes gradually drops with time, as illustrated in Fig.2.3. Let the input be a square wave. In the positive half cycle, the diode is ON and $v_{clamp} = v_{gs}$. v_c rises and v_{clamp} drops because $v_{clamp} = v_{in} + v_c$. Since the MOSFET is in strong inversion, v_c rises and v_{clamp} drops rapidly. When $v_{clamp} < V_{TH}$, the transistor enters sub-threshold, I_{ds} is small. If T is small, $v_{clamp} \approx V_{TH}$ at $t = T/2$ due to a small I_{ds} . $v_c \approx V_m - V_{TH}$ follows. When v_{in} switches its polarity at $t = T/2$, $v_{clamp}(T/2) = -(V_m + v_c) \approx -2V_m + V_{TH}$. The diode is OFF during $T/2 < t \leq T$. At $t = T$, $v_{clamp}(T) = v_{clamp}(T/2)$. During $T < t < 3T/2$, the diode is in sub-threshold and the charge of the capacitor is gradually depleted, resulting in slowly decreasing v_{clamp} .

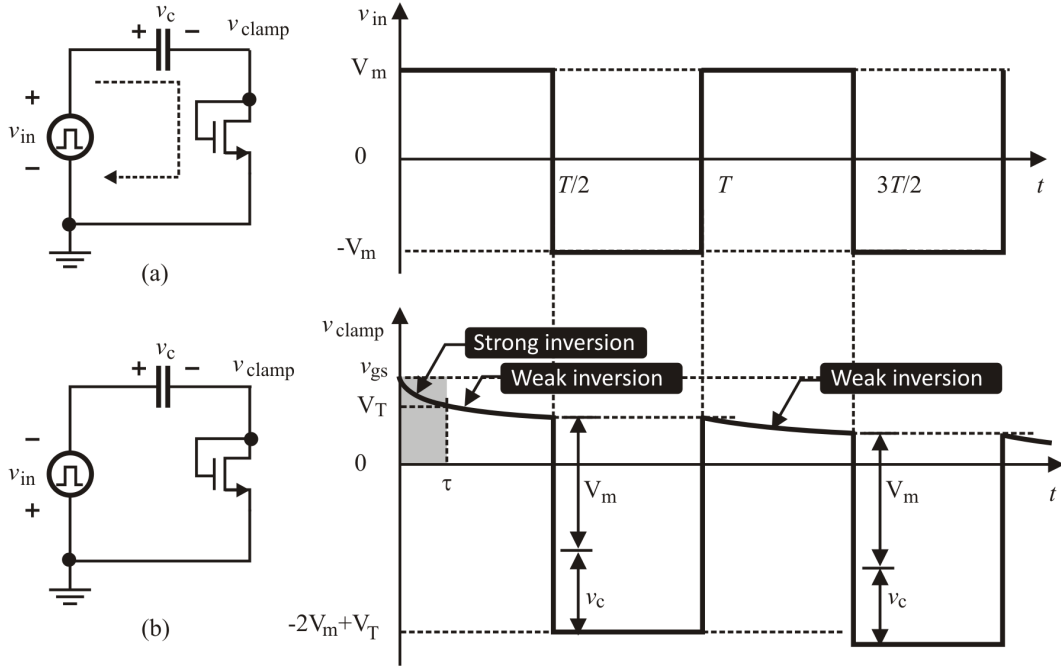


Figure 2.3: Single-stage negative voltage level shifter.

To stabilize the voltage, a current-compensating diode M1 is added in parallel with the capacitor, as shown in Fig.2.4. When $v_{in} = V_m$, M1 turns on. M2 is off as $v_c = v_{gs2} = 0$. v_{clamp} drops when the capacitor is charged. Along with the increase of the voltage across

the capacitor, M2 leaves off-state and enters subthreshold. When v_c reaches V_{TH} , M2 will enter strong inversion. M2 will supply a current to M1. When the current of M1 is identical to that of M2, the depletion of the charge of the capacitor by M2 will end and the voltage of the clamping node will remain unchanged. We say that the voltage level shifter is in an equilibrium state.

It is highly desirable that both M2 and M1 operate in sub-threshold in the equilibrium state to minimize the static power consumption. This can be ensured if $V_m < V_{TH}$. If V_m is larger than V_{TH} , sub-threshold can also be established by cascading more diodes. This is because the input voltage v_{in} is shared by the clamping diode and compensation diode. If the number of the clamping diodes is M and the number of the compensation diodes is N , then $v_{in} = (M + N)v_{gs}$ holds (assuming that all MOS diodes are identical). Clearly if $v_{gs} < V_{TH}$, MOS diodes will be in sub-threshold. In what follows, we derive the analytical expression of $v_{clamp,max}$, which occurs when both M2 and M1 operate in subthreshold and their currents are identical. The channel current of MOSFETs in weak inversion is given by [45]

$$I_{ds} = I_t \left(\frac{W}{L} \right) e^{\frac{V_{gs}-V_T}{nV_{TH}}} \left(1 - e^{-\frac{V_{ds}}{V_T}} \right), \quad (2.1)$$

where I_t is a process and temperature dependent current, W and L are the width and length of the channel, respectively, $V_T = kT/q$ is the thermal voltage, T is the temperature in degrees Kelvin, q is the charge of electron, k is Boltzmann constant, and $n = 1 + C_{js}/C_{ox}$ with C_{js} the capacitance between gate voltage induced depletion region and the substrate and C_{ox} the gate-oxide capacitance. Since I_{ds} is independent of V_{ds} when $V_{ds} = 3V_{TH}$, we neglect the effect of V_{ds} on I_{ds} . When $I_{ds1} = I_{ds2}$

$$\left(\frac{W}{L} \right)_2 e^{\frac{v_{clamp,max}-V_T}{nV_{TH}}} = \left(\frac{W}{L} \right)_1 e^{\frac{V_m-v_{clamp,max}-V_T}{nV_{TH}}}. \quad (2.2)$$

It follows that

$$v_{clamp,max} = \frac{1}{2} \left(V_m + nV_{TH} \ln \left[\frac{(W/L)_1}{(W/L)_2} \right] \right). \quad (2.3)$$

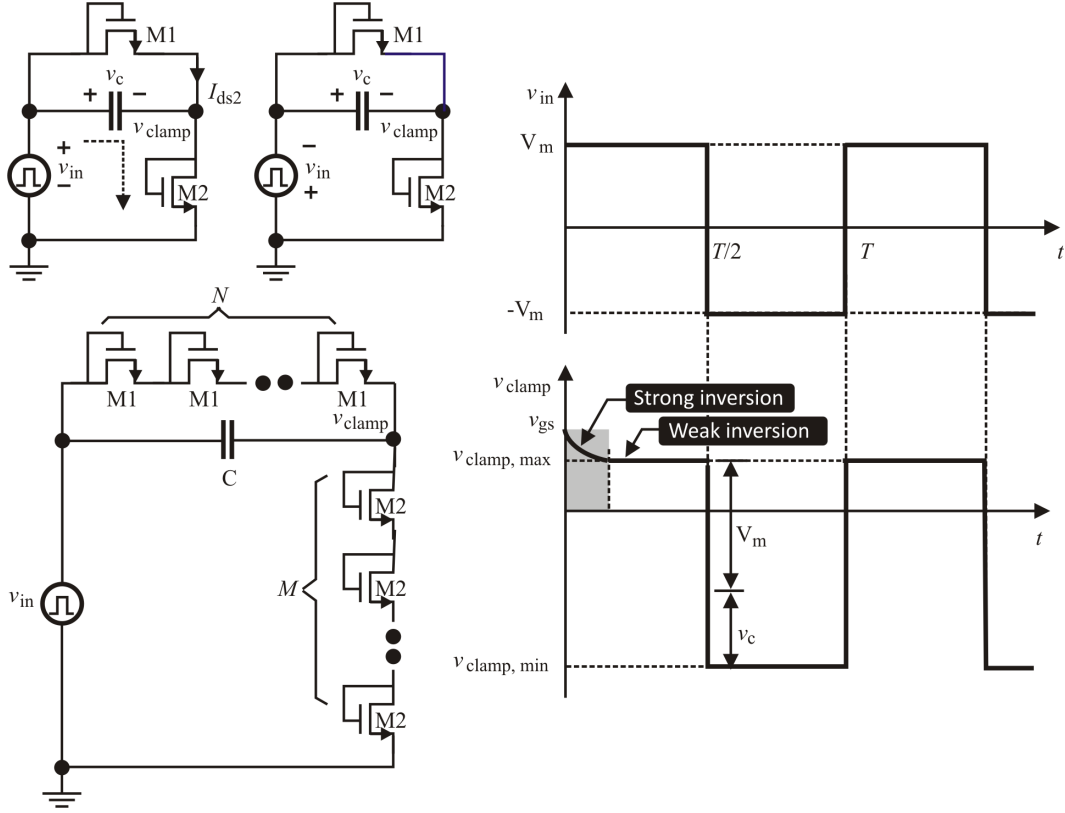


Figure 2.4: Negative voltage level shifter with current compensation.

If the number of current-compensating diodes of identical dimension $(W/L)_1$ is N and that of clamping diodes of identical dimension $(W/L)_2$ is M , we have

$$\begin{aligned} & \left(\frac{W}{L} \right)_2 e^{\frac{\frac{1}{M} v_{clamp,max} - V_T}{nV_{TH}}} \\ &= \left(\frac{W}{L} \right)_1 e^{\frac{\frac{1}{N} (V_m - v_{clamp,max}) - V_T}{nV_{TH}}}, \end{aligned} \quad (2.4)$$

from which we obtain

$$\begin{aligned}
v_{clamp,max} &= \left(\frac{M}{M+N} \right) V_m \\
&+ \left(\frac{MN}{M+N} \right) nV_{TH} \ln \left[\frac{(W/L)_1}{(W/L)_2} \right].
\end{aligned} \tag{2.5}$$

The minimum value of v_{clamp} occurs when v_{in} changes its polarity from positive to negative. Since $v_c(T^-/2) = V_m - v_{clamp,max}$ and remains unchanged during the transition, we have $v_{clamp,min} = -V_m - v_c(T^+/2) = -2V_m + v_{clamp,max}$.

To validate these theoretical results, a single-stage negative voltage-level shifter with one current-compensating diode and one clamping diode as in Fig.2.4 is simulated in IBM 130 nm 1.2 V CMOS technology with BSIM4 device models. The diodes are implemented in 3.3 V PFETs with the same aspect ratio of $W/L=0.5 \mu\text{m} / 0.4 \mu\text{m}$ and the capacitor is 1 pF. The input to the negative voltage-level shifter is a 10 MHz square wave with 0~1.2 V voltage swing. Fig.2.5 plots the voltage of the voltage level shifter with and without compensation. It is observed that the output voltage gradually levels off when the shunt current compensation is absent, and stabilized when the shunt current compensation exists. The minimum and maximum voltages of the clamping node are -582 mV to 620 mV, which agree well with theoretical values. The average compensation current is approximately 469.6 nA, the average clamping current is approximately 469.8 nA, and the average power drawn from the input source is 565.5 nW. Note that since only one current compensating diode and one clamping diode are used, both MOSFETs are in the strong inversion rather than the weak inversion, resulting in a large static current in the equilibrium state.

The same voltage-level shifting topology in Fig.2.4 applies to sinusoidal inputs as well. Shown in Fig.2.6 is a negative voltage level shifter with a single clamping diode and a single compensation diode, i.e. $M = N = 1$. The input signal is a 2.4 GHz $V_m = 400$ mV sinusoid. The diodes are implemented in low-threshold devices in IBM 130 nm CMRF8SF CMOS technology with aspect ratio $W/L=1.6 \mu\text{m} / 0.12 \mu\text{m}$. It is seen that the median value of the input signal is shifted down by approximately 185 mV. The predicted value is 200 mV. The discrepancy is due to the non-negligible reverse leakage current of the clamping diode as compared with its sub-threshold current. Further simulation shows that simulation

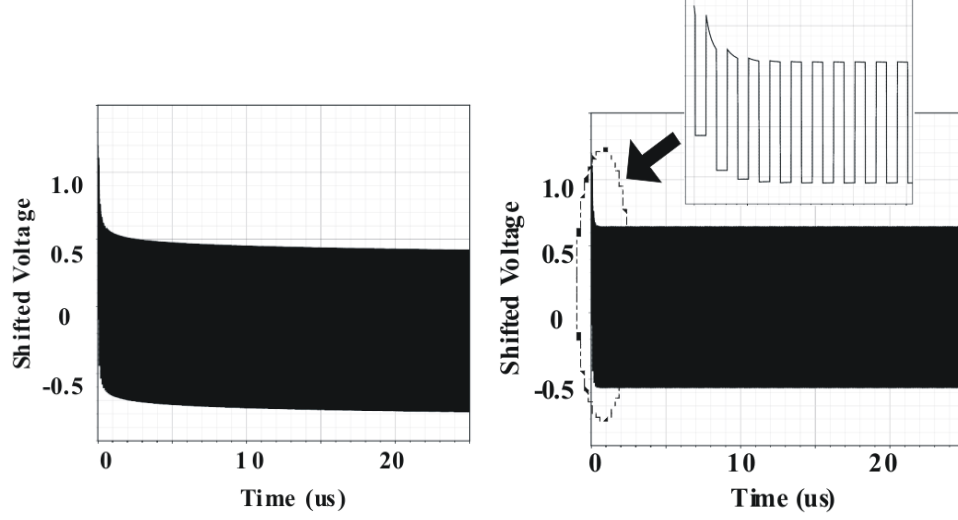


Figure 2.5: Simulated voltage of the clamping node of a single-stage negative voltage level shifter without current compensation (Left) and with current compensation (Right).

results will converge to the predicated value if the input voltage is increased. The clamping current and the compensation current are found to be 1.6 nA and 3.3 nA, respectively. The compensation current is smaller as compared with the clamping current due to the reversed-biased leakage current of the clamping diode. The power drawn from the input source is approximately 33.5 nW.

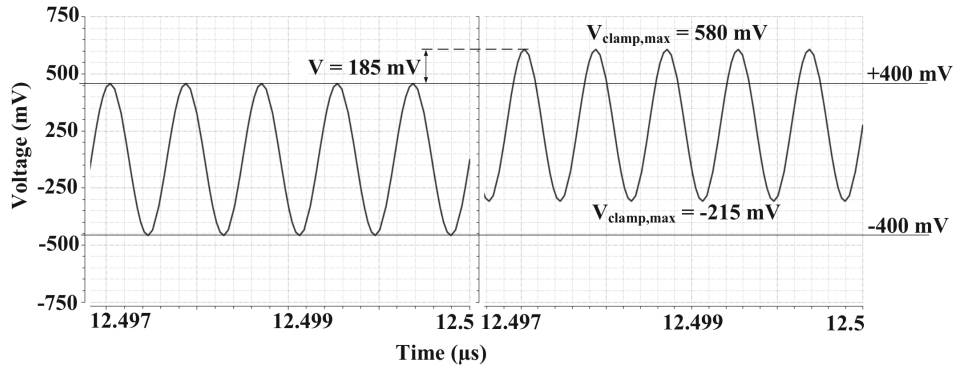


Figure 2.6: Simulated voltage of the clamping node of a single-stage negative voltage level shifter. Input is a 2.4 GHz 400 mV sinusoid. Left : Before voltage level shift. Right : After voltage level shift.

2.3 Voltage Level Shifters with Variable Voltage Shift

2.3.1 Cascaded Voltage Level Shifters

The minimum voltage shift that the preceding multi-stage voltage level shifters can provide is V_m . The voltage level shifter shown in Fig.2.7 provides a mechanism that allows the minimum voltage shift to be smaller than V_m . We notice that when $v_{in} = V_m$, most of the current of M1a flows to M1b. This is because there is only one transistor (M1b) from clamping node 1 to the ground while there are at least two transistors from M2a to the ground. The voltage of clamping node 1 is maximized when $v_{in} = V_m$ and the current of M1a and that of M1b are equal, and can be determined by noting $I_{ds,1a} \approx I_{ds,1b}$.

$$v_{1,max} = \frac{1}{2} \left(V_m + nV_{TH} \ln \left[\frac{(W/L)_{1a}}{(W/L)_{1b}} \right] \right). \quad (2.6)$$

The minimum voltage of clamping node 1 occurs when $v_{in} = -V_m$. Since $v_{c1}(T^-/2) = V_m - v_{1,max}$, and remains unchanged during the transition, we have

$$\begin{aligned} v_{1,min} &= -V_m - v_{c1}(T^+/2) \\ &= -2V_m + \frac{V_m}{2} + \frac{1}{2}nV_{TH} \ln \left[\frac{(W/L)_{1a}}{(W/L)_{1b}} \right]. \end{aligned} \quad (2.7)$$

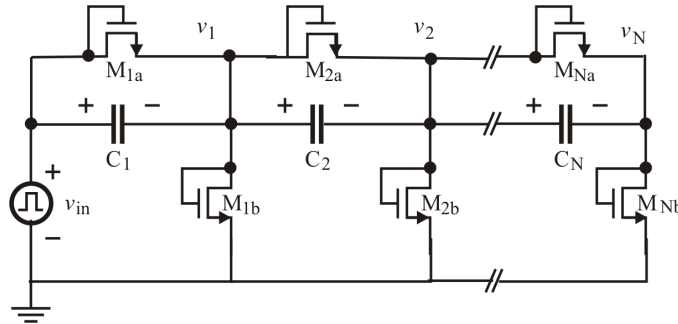


Figure 2.7: Cascaded negative voltage level shifters.

In a similar way, the voltage of clamping node 2 reaches its maximum when $v_{in} = V_m$ and the current of M2a and that of M2b are the same

$$\left(\frac{W}{L}\right)_{2a} e^{\frac{V_{2,max}-V_{1,max}-V_T}{nV_{TH}}} = \left(\frac{W}{L}\right)_{2b} e^{\frac{V_{2,max}-V_T}{nV_{TH}}}. \quad (2.8)$$

Solving (2.8) yields

$$v_{2,max} = \frac{1}{2} \left(v_{1,max} + nV_{TH} \ln \left[\frac{(W/L)_{2a}}{(W/L)_{2b}} \right] \right). \quad (2.9)$$

Substituting (2.6) into (2.9) yields

$$\begin{aligned} v_{2,max} &= \frac{V_m}{2^2} + \left(\frac{1}{2^2} \ln \left[\frac{(W/L)_{1a}}{(W/L)_{1b}} \right] \right. \\ &\quad \left. + \frac{1}{2} \ln \left[\frac{(W/L)_{2a}}{(W/L)_{2b}} \right] \right) nV_{TH}. \end{aligned} \quad (2.10)$$

Since

$$\begin{aligned} v_{c2} \left(\frac{T}{2^-} \right) &= v_{1,max} - v_{2,max} \\ &= \frac{1}{2} v_{1,max} - \frac{1}{2} nV_{TH} \ln \left[\frac{(W/L)_{2a}}{(W/L)_{2b}} \right]. \end{aligned} \quad (2.11)$$

and remains unchanged during the transition, we have $v_{2,min} = -V_m - v_{c1}(T^+/2) - v_{c2}(T^+/2)$.

Thus

$$\begin{aligned}
v_{2,min} &= -2V_m + \frac{V_m}{2^2} \\
&+ \left(\frac{1}{2^2} \ln \left[\frac{(W/L)_{1a}}{(W/L)_{1b}} \right] + \frac{1}{2} \ln \left[\frac{(W/L)_{2a}}{(W/L)_{2b}} \right] \right) nV_{TH}.
\end{aligned} \tag{2.12}$$

Following the similar approach, one can show that the voltage of clamping node N of the cascaded positive voltage level shifter shown in Fig.2.8 is given by

$$\begin{aligned}
v_{N,max} &= \frac{V_m}{2^N} + \left(\frac{1}{2^N} \ln \left[\frac{(W/L)_{1a}}{(W/L)_{1b}} \right] \right. \\
&+ \frac{1}{2^{N-1}} \ln \left[\frac{(W/L)_{2a}}{(W/L)_{2b}} \right] + \dots \\
&+ \left. \frac{1}{2} \ln \left[\frac{(W/L)_{Na}}{(W/L)_{Nb}} \right] \right) nV_{TH},
\end{aligned} \tag{2.13}$$

$$\begin{aligned}
v_{N,min} &= -2V_m + \frac{V_m}{2^N} + \left(\frac{1}{2^N} \ln \left[\frac{(W/L)_{1a}}{(W/L)_{1b}} \right] \right. \\
&+ \frac{1}{2^{N-1}} \ln \left[\frac{(W/L)_{2a}}{(W/L)_{2b}} \right] + \dots \\
&+ \left. \frac{1}{2} \ln \left[\frac{(W/L)_{Na}}{(W/L)_{Nb}} \right] \right) nV_{TH}.
\end{aligned} \tag{2.14}$$

The voltage swing of the cascaded positive voltage level shifter shown in Fig.2.8 can also be determined: $v_{1,max} = 2V_m + v_{1,min}$, $v_{k,max} = 2V_m + v_{k,min}$, and

$$\begin{aligned}
v_{1,min} &= - \left(\frac{M_1}{M_1 + N_1} \right) V_m \\
&+ \left(\frac{M_1 N_1}{M_1 + N_1} \right) nV_{TH} \ln \left[\frac{(W/L)_{1a}}{(W/L)_{1b}} \right],
\end{aligned} \tag{2.15}$$

$$\begin{aligned}
v_{k,min} &= \left(\frac{M_k}{M_k + N_k} \right) V_{k-1,min} \\
&+ \left(\frac{M_k N_k}{M_k + N_k} \right) n V_{TH} \ln \left[\frac{(W/L)_{ka}}{(W/L)_{kb}} \right].
\end{aligned} \tag{2.16}$$

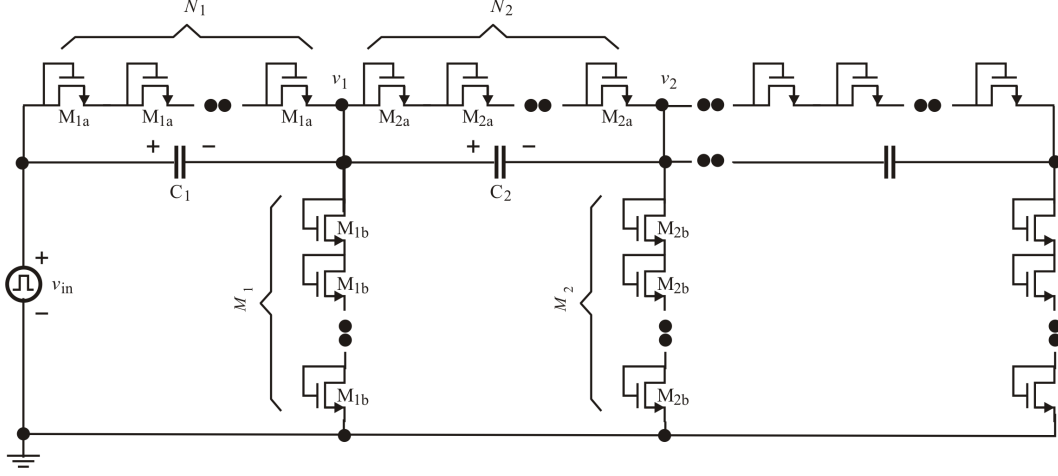


Figure 2.8: Cascaded negative voltage level shifters with multiple diodes.

To validate these theoretical results, two 3-stage cascaded negative voltage level shifters are designed.

1. Cascaded negative voltage level shifter 1: $M_1 = 2$, $M_2 = M_3 = 1$, $N_1 = N_2 = N_3 = 1$.
2. Cascaded negative voltage level shifter 2: $M_1 = M_2 = M_3 = 1$, $N_1 = N_2 = N_3 = 1$.

All transistors have the same dimension $W/L = 0.5 \mu\text{m} / 0.4 \mu\text{m}$. The values of the capacitors are: $C_1 = 10 \text{ pF}$, $C_2 = 5 \text{ pF}$, $C_3 = 1 \text{ pF}$. The input is a 10 MHz square wave with voltage swing -1.2 V to 1.2 V and rise/fall time of 1 ns. The voltages of the three clamping nodes are plotted in Fig.2.9. Both the minimum and maximum voltages of the clamping nodes 1, 2, and 3 decrease gradually. This agrees with the analytical results derived earlier. Also observed is that the voltage swing of the clamping nodes 1, 2, and 3 is the same as that of

the input. This is also in line with the analytical results. Table 1 compares the simulation and analytical results. A good agreement is observed.

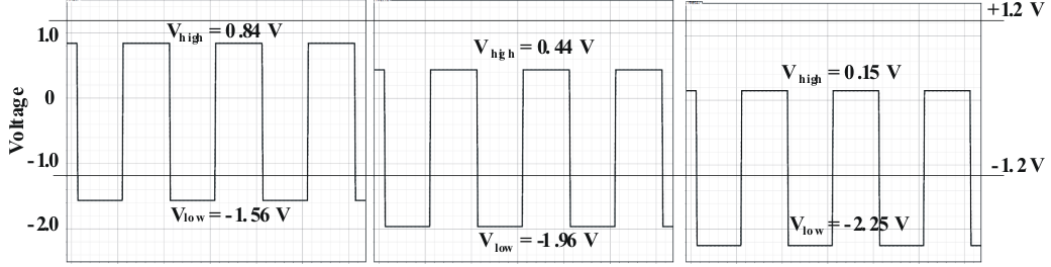


Figure 2.9: Simulated voltage of clamping nodes of 3-stage cascaded negative voltage level shifter ($M_1 = 2$, $M_2 = M_3 = 1$, $N_1 = N_2 = N_3 = 1$).

Table 2.1: Comparison of the analytical results and simulation results of the voltage of clamping nodes of 3-stage cascaded negative voltage level shifters. Parameters of cascaded negative voltage level shifter 1 : $M_1 = 2$, $M_2 = M_3 = 1$, $N_1 = N_2 = N_3 = 1$. Parameters of cascaded negative voltage level shifter 2 : $M_1 = M_2 = M_3 = 1$, $N_1 = N_2 = N_3 = 1$.

Voltage	Analytical results of voltage shifter 1 (V)	Simulation results of voltage shifter 1 (V)	Analytical results of voltage shifter 2 (V)	Simulation results of voltage shifter 2 (V)
$v_{1,max}$	0.8	0.84	0.6	0.64
$v_{1,min}$	-1.6	-1.56	-1.8	-1.76
$v_{2,max}$	0.4	0.44	0.3	0.34
$v_{2,min}$	-2.0	-1.96	-2.1	-2.06
$v_{3,max}$	0.2	0.15	0.15	0.16
$v_{3,min}$	-2.2	-2.25	-2.25	-2.23

To further validate the analytical results derived for cascaded voltage level shifters, two additional 3-stage cascaded positive voltage level shifters are designed.

1. Cascaded positive voltage level shifter 1: $M_1 = 2$, $M_2 = M_3 = 1$, $N_1 = N_2 = N_3 = 1$.
2. Cascaded positive voltage level shifter 2: $M_1 = M_2 = M_3 = 1$, $N_1 = N_2 = N_3 = 1$.

The same parameters as those of the preceding cascaded negative voltage level shifter are used. The voltages of the clamping nodes are plotted in Fig.2.10. Table 2 compares the simulation results and the analytical results. Again, a good agreement is observed.

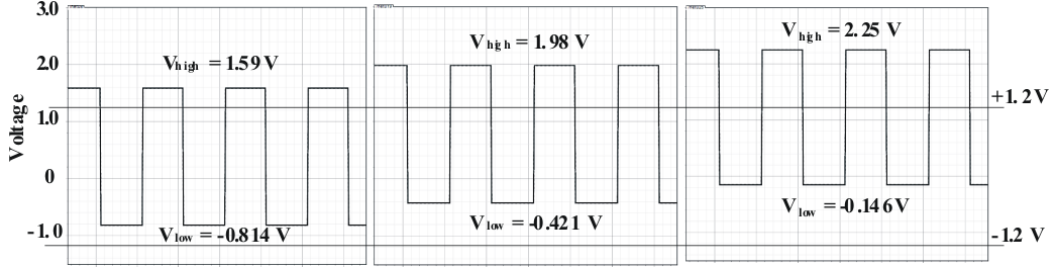


Figure 2.10: Simulated voltage of clamping nodes of 3-stage cascaded positive voltage level shifter ($M_1 = 2$, $M_2 = M_3 = 1$, $N_1 = N_2 = N_3 = 1$).

Table 2.2: Comparison of the analytical and simulation results of the voltage of clamping nodes of 3-stage cascaded positive voltage level shifters. Cascaded positive voltage level shifter 1 : $M_1 = 2$, $M_2 = M_3 = 1$, $N_1 = N_2 = N_3 = 1$. Cascaded positive voltage level shifter 2 : $M_1 = M_2 = M_3 = 1$, $N_1 = N_2 = N_3 = 1$.

Voltage	Analytical results of voltage shifter 1 (V)	Simulation results of voltage shifter 1 (V)	Analytical results of voltage shifter 2 (V)	Simulation results of voltage shifter 2 (V)
$v_{1,min}$	-0.8	-0.81	-0.6	-0.63
$v_{1,max}$	1.6	1.59	1.8	1.77
$v_{2,min}$	-0.4	-0.42	-0.3	-0.32
$v_{2,max}$	2.0	1.98	2.1	2.07
$v_{3,min}$	-0.2	-0.21	-0.15	-0.15
$v_{3,max}$	2.2	2.18	2.25	2.25

2.3.2 Superimposed Voltage Level Shifters

The maximum voltage shift of preceding cascaded voltage shifters is only V_m . To increase voltage shift, a superimposed voltage level shifter shown in Fig.2.11 is proposed.

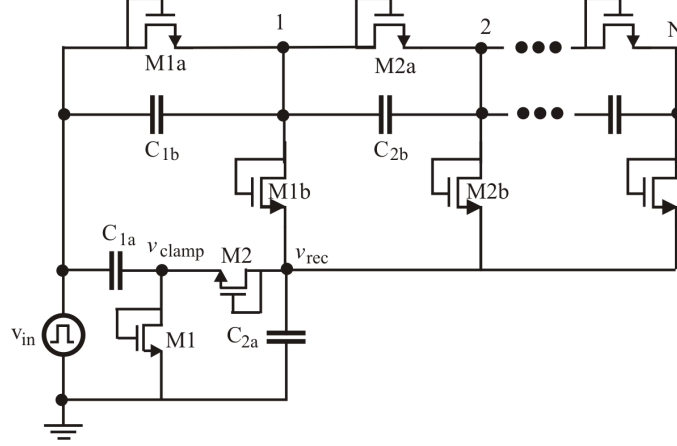


Figure 2.11: Superimposed negative voltage level shifters. The voltage multiplication stage is a voltage doubler. The number of current compensating diodes and that of the clamping diodes per stage of the cascaded voltage level shifting level shifter are one.

Superimposed negative voltage level shifter can be analyzed by representing the voltage multiplication stage with ideal voltage source v_{rec} , as shown in Fig.2.12. Equating the current of the current-compensating branch and that of the clamping branch in stage 1 yields

$$\begin{aligned}
 & I_t \left(\frac{W}{L} \right)_{1a} e^{\frac{\frac{1}{N_1}(V_m - v_{1,max}) - V_T}{nV_{TH}}} \\
 &= I_t \left(\frac{W}{L} \right)_{1b} e^{\frac{\frac{1}{M_1}(V_{1,max} - v_{rec}) - V_T}{nV_{TH}}}
 \end{aligned} \tag{2.17}$$

from which we obtain

$$\begin{aligned}
 v_{1,max} &= \left(\frac{M_1}{M_1 + N_1} \right) V_m + \left(\frac{N_1}{M_1 + N_1} \right) v_{rec} \\
 &+ \left(\frac{M_1 N_1}{M_1 + N_1} \right) nV_{TH} \ln \left[\frac{(W/L)_{1a}}{(W/L)_{1b}} \right].
 \end{aligned} \tag{2.18}$$

The minimum value of v_1 , denoted by $v_{1,min}$, occurs when v_{in} changes its polarity from positive to negative. Since $v_{c1b}(T^-/2) = V_m - v_{1,max}$ and $v_{c1b}(T^-/2) = v_{c1b}(T^+/2)$, we have $v_{1,min} = -V_m - v_{c1b}(T^+/2) = -2V_m + v_{1,max}$. The voltage swing of the remaining nodes of the cascaded stages can be obtained in an iterative way, specifically $v_{k,min} = -2V_m + v_{k,max}$

$$\begin{aligned}
v_{k,max} &= \left(\frac{M_k}{M_k + N_k} \right) v_{k-1,max} + \left(\frac{N_k}{M_k + N_k} \right) v_{rec} \\
&+ \left(\frac{M_k N_k}{M_k + N_k} \right) n V_{TH} \ln \left[\frac{(W/L)_{ka}}{(W/L)_{kb}} \right].
\end{aligned} \tag{2.19}$$

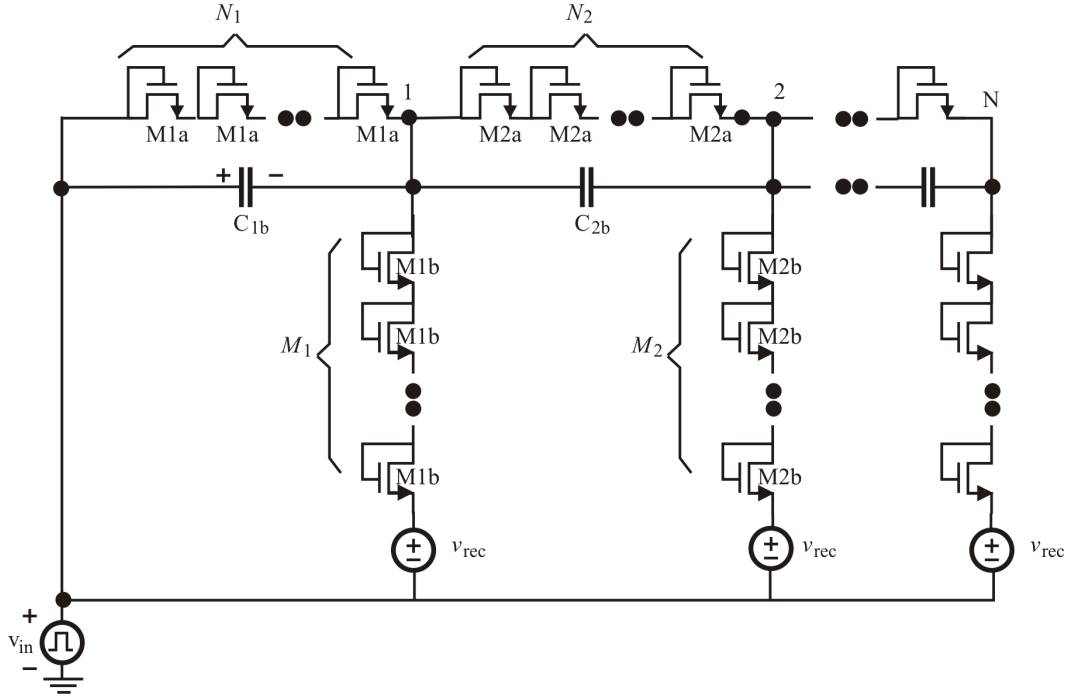


Figure 2.12: Superimposed negative voltage level shifter with an arbitrary number of current compensating diodes and clamping diodes.

To validate these results, a superimposed negative voltage level shifter and a superimposed positive voltage level shifter are designed. All transistors have the same dimension $W/L=0.5 \mu\text{m} / 0.4 \mu\text{m}$. The input is a 10 MHz square wave with voltage swing -1.2 V to 1.2 V. The details of these superimposed voltage level shifters are given below:

1. The superimposed positive voltage level shifter:

- Basic voltage level shifter positive voltage doubler with two identical capacitors of 1 pF.

- 3-stage cascaded positive voltage level shifter: $M_1 = 2$, $M_2 = M_3 = 1$, $N_1 = 3$, $N_2 = N_3 = 1$. $C_{1b} = 1$ pF, $C_{2b} = 0.5$ pF, $C_{3b} = 0.2$ pF.

2. The superimposed negative voltage level shifter:

- Basic voltage level shifter negative voltage doubler with two identical capacitors of 1 pF.
- 3-stage cascaded negative voltage level shifter: $M_1 = 2$, $M_2 = M_3 = 1$, $N_1 = 3$, $N_2 = N_3 = 1$. $C_{1b} = 1$ pF, $C_{2b} = 0.5$ pF, $C_{3b} = 0.2$ pF.

The voltages of the clamping nodes are plotted in Figs.2.13 and Fig.2.14. Table 2.3 compares the analytical and simulation results of the two voltage level shifters. It is observed that the voltage shift of both voltage level shifters exceeds $V_m=1.2$ V. Also observed is that the voltage swing of the clamping nodes is the same as that of the input. The small differences between the analytical and simulation results are due to the fact $V_{TH}=0.5$ V was used in calculation while the effective value of V_{TH} of MOSFETs is typically much smaller. To validate this, the voltages of the clamping nodes of the superimposed positive voltage level shifter are also calculated using the derived analytical expressions and $V_{TH}=0.35$ V. An excellent agreement was observed.

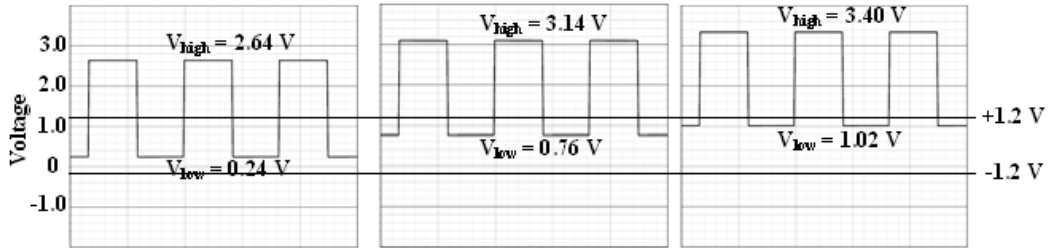


Figure 2.13: Simulated voltage of clamping nodes of 3-stage cascaded positive voltage level shifter ($M_1 = 2$, $M_2 = M_3 = 1$, $N_1 = 3$, $N_2 = N_3 = 1$).

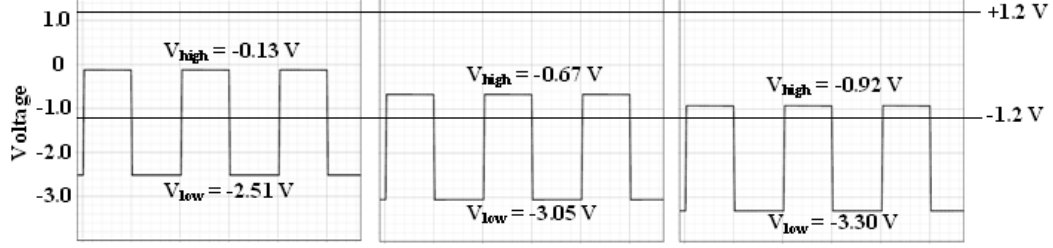


Figure 2.14: Simulated voltage of clamping nodes of 3-stage cascaded negative voltage level shifter ($M_1 = 2$, $M_2 = M_3 = 1$, $N_1 = 3$, $N_2 = N_3 = 1$).

Table 2.3: Comparison of the analytical and simulation results of the voltage of clamping nodes of superimposed voltage level shifters with $V_{TH} = 0.5$ V used in calculation.

Voltage	Analytical results of superimposed voltage shifter (V)	Simulation results of superimposed voltage shifter (V)	Analytical results of superimposed voltage shifter (V)	Simulation results of superimposed voltage shifter (V)
$v_{1,min}$	0.15	0.24	-2.55	-2.51
$v_{1,max}$	2.55	2.64	-0.15	-0.13
$v_{2,min}$	0.60	0.76	-3.07	-3.05
$v_{2,max}$	3.07	3.14	-0.60	-0.67
$v_{3,min}$	0.83	1.02	-3.23	-3.30
$v_{3,max}$	3.23	3.40	-0.83	-0.92

2.4 Low-Leakage Voltage Level Shifters

The bulk of NMOS diodes (p-substrate) needs to be connected to the most negative voltage while that of PMOS diodes (n-well) needs to be connected to the most positive voltage in order to minimize the leakage of drain-bulk junction. The drain-bulk junctions of the voltage level shifters studied earlier could be forward-biased, giving rise to a large leakage current. This is illustrated using the negative voltage level shifter shown in Fig.2.15(a). It was shown earlier that the voltage swing of the clamping node of the negative voltage level shifter is bounded by $-2V_m + V_{TH} < v_{clamp} < V_{TH}$. The voltage of the rectifying node of the negative voltage level shifter is given by $v_{rec} = 2V_{TH} - 2V_m$, and is the lowest dc voltage of the system. If $V_m > V_{TH}$, then $v_{rec} < 0$. Thus, to prevent the forward conduction of the pn-junctions, the substrate of the NMOS diodes should be tied to the lowest dc voltage of the

system, i.e., $v_{sub} = v_{rec} = 2V_{TH} - 2V_m$. The lowest voltage drop across the drain-substrate junction of M1 occurs when v_{clamp} is at its minimum $v_{db1} = v_{sub} - v_{clamp,min} = V_{TH}$. Similarly, for the positive voltage level shifter shown in Fig.2.15(b), the n-well of the NMOS diode are bulk-connected to the highest dc voltage of the system, i.e., $v_{nw} = v_{rec} = 2V_m - 2V_{TH}$. Since $-V_{TH} < v_{clamp} < 2V_m - V_{TH}$, we have $v_{db1} = V_{TH}$. It is evident that in both cases, the drain-bulk voltage is sufficiently large to give rise to non-negligible junction leakage currents, resulting in a large static power consumption especially when M1 and M2 operate in the sub-threshold mode where the channel currents are small.

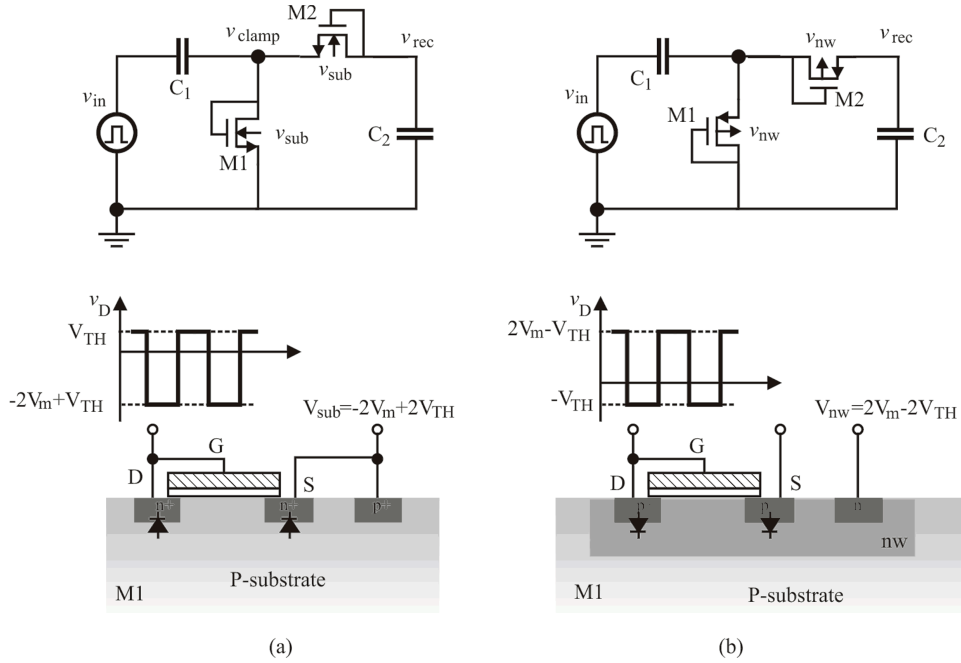


Figure 2.15: (a) Negative voltage level shifter. (b) Positive voltage level shifter.

The leakage current through the drain-bulk junction can be reduced effectively if NMOS diodes are only used in positive voltage level shifters and PMOS diodes are only used in negative voltage shifters. To demonstrate this, consider the complementary voltage level shifter shown in Fig.2.16. It consists of a positive voltage level shifter and a negative voltage level shifter. The substrate is tied to the rectifying node of the negative voltage level shifter (the lowest voltage of the system) : $v_{sub} = v_{rec,b} = 2V_{TH} - 2V_m$. The n-well

is tied to the rectifying node of the positive voltage level shifter (the highest voltage of the system) : $v_{nw} = v_{rec,a} = 2V_m - 2V_{TH}$. Because $-V_{TH} < v_{clamp,a} < 2V_m - V_{TH}$ and $-2V_m + V_{TH} < v_{clamp,b} < V_{TH}$, we have the voltage across the drain-substrate junction of M1a and M1b : $v_{db,a} = v_{sub} - v_{a,min} = 3V_{TH} - 2V_m$ and $v_{db,b} = v_{sub} - v_{b,max} = 3V_{TH} - 2V_m$. Since $V_{TH} \ll V_m$, the drain-bulk junctions will not forward conduct. The leakage current is therefore minimized.

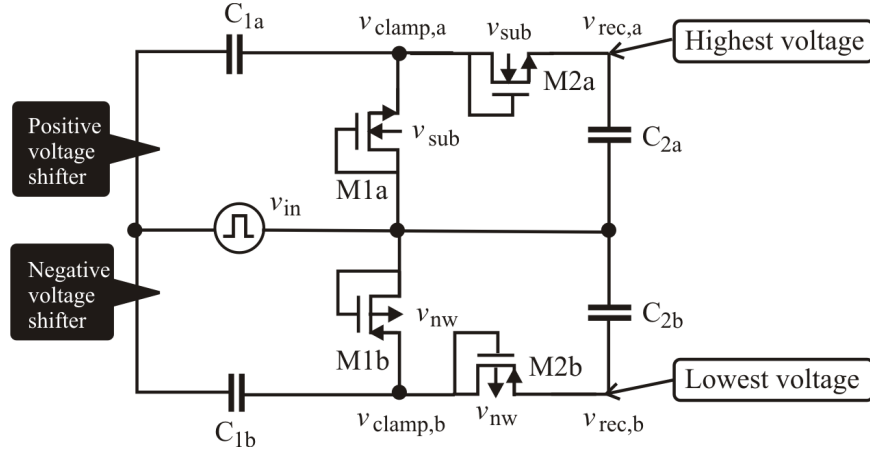


Figure 2.16: Low-leakage voltage level shifter.

To validate this, the voltage level shifter of Fig.2.15 and the low-power voltage shifter of Fig.2.16 are analyzed. Circuit parameters of the two voltage level shifters are: $C_{1a} = C_{2a} = C_{1b} = C_{2b} = 1$ pF. The dimensions of NMOS transistors are $W/L = 0.5 \mu\text{m} / 0.4 \mu\text{m}$ and those of PMOS are $W/L = 0.5 \mu\text{m} / 0.4 \mu\text{m}$. The power consumption of the two voltage level shifters is compared and the results are tabulated in Table 2.4. The leakage current of the low-leakage voltage level shifter is two orders of magnitude lower as compared with that of the basic voltage level shifter.

Table 2.4: Performance comparison of the voltage level shifter (Fig.2.15) and the low-power voltage level shifter (Fig.2.16). i_{leak1} and i_{leak2} are the drain-bulk currents of M1b and M2b, respectively.

Parameters	Basic voltage level shifter (Fig.2.15)	Low-leakage voltage level shifter (Fig2.16)
v_{reca}	1.492 V	+1.497 V
v_{recb}	-1.797 V	-1.577 V
i_{leak1}	23.6 μA	0.118 μA
i_{leak2}	22.1 μA	0.164 μA

2.5 Robustness

2.5.1 Process and Temperature Effect

Fig.2.17 shows the output voltage of the voltage shifter of Fig.2.3 at four process corners over temperature range $-20^{\circ}C \sim 100^{\circ}C$. It is seen that the normalized voltage variation due to process spread at $25^{\circ}C$ is approximately 1.5% and the normalized voltage variation due to temperature variation (TT) is 0.7%.

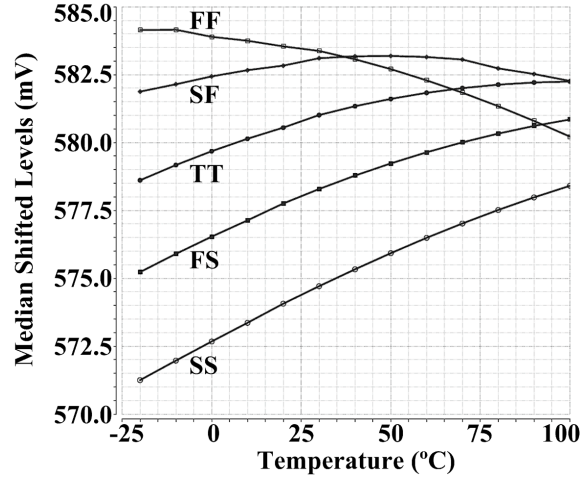


Figure 2.17: Effect of process spread and temperature variation on output voltage of Fig.2.3. Legends : FF (fast NMOS/fast PMOS), SF (slow NMOS/fast PMOS), TT (typical NMOS/PMOS), FS (fast NMOS/slow PMOS), and SS (slow NMOS/slow PMOS).

2.5.2 Amplitude of Input

The amplitude of the input signal does not need to be greater than the nominal threshold value of MOSFETs for the proposed voltage level shifters to function properly. When the amplitude of the input is less than the nominal threshold voltage of MOSFETs required for the devices in strong inversion, the devices will operate in sub-threshold. Although in principle the amplitude of the input to the voltage level shifters can be arbitrarily small, the voltage shifters will cease to function properly if the amplitude of the input is overly small. This is because when the amplitude of the input is overly small, the current conducted by the MOS diodes will also be small. As a result, not only the charging and discharging processes of the capacitors will be overly long, the leakage current of the reversed biased pn-junctions of MOS diodes will become comparable to the charging/discharging current, preventing the capacitors to be charged or discharged. Fig.2.18 shows such an effect. The curves represent the normalized voltage shift of the single-stage positive voltage level shifter with input amplitudes swept from 100 mV to 1 V and frequency swept from 10 MHz to 10 GHz. The following observations are made : (i) Lowering the amplitude of the input will reduce the amount of the voltage shift that the voltage level shifter can provide at high frequencies. This is due to the small currents that clamping and compensating diodes in sub-threshold can provide. (ii) Increasing the frequency of the input will reduce the amount of the voltage shift that the voltage level shifter can provide. This is especially true when the amplitude of the input is small. (iii) When the input is at 1 GHz, if the amplitude of the input is 100 mV, no voltage shift can be provided. This is because all diodes in this case are in sub-threshold and cannot cope with the change of the input at 1 GHz. Increasing the amplitude of the input gradually increase the amount of voltage shift. (iv) If the amplitude of the input is greater than 700 mV, the voltage level shifter can cope with inputs beyond 10 GHz. The preceding observation clearly reveals the trade-off between speed, voltage shift, and power consumption. For applications such as passive wireless microsystems, since the frequency of the input is typically low, both ultra-low power consumption and a sufficient voltage shift can be obtained simultaneously.

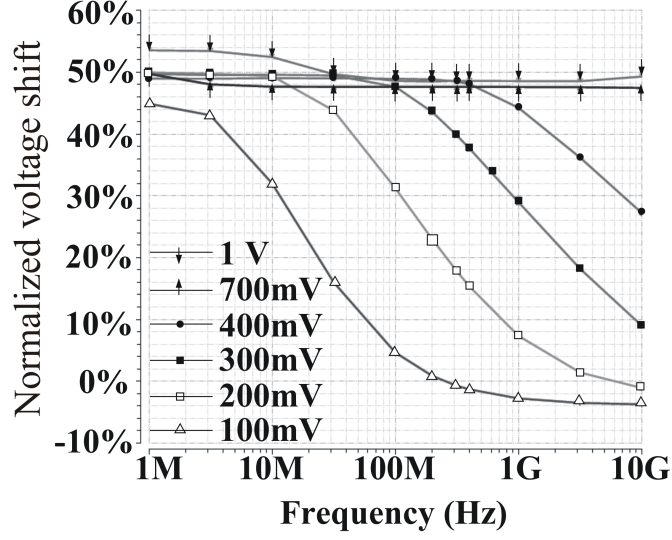


Figure 2.18: Effect of the amplitude and frequency of the input of single-stage positive level shifter with regular MOS diodes. Circuit parameters : Clamping diode : $W/L=1.6 \mu\text{m} / 0.12 \mu\text{m}$; Compensating diode : $W/L=0.32 \mu\text{m} / 0.12 \mu\text{m}$. The clamping diode is made larger than the compensation diode to counteract the reversed leakage current and parasitics at high frequencies.

2.5.3 Voltage Level Shifters with Native MOS Diodes

The reduction of the speed of voltage level shifters due to the small amplitude of the input can be mitigated if native MOSFETs, i.e., MOSFETs with a zero threshold voltage, are used. The zero threshold voltage of native MOS diodes allows them to conduct a large current even though the amplitude of the input is small. The result is demonstrated in Fig.2.19 for the same single-stage positive voltage level shifter implemented in native MOSFETs. It is observed that : (i) At the same amplitude of the input, the voltage level shifter with native MOS diodes provides a larger voltage shift (approximately 50% for regular MOS diodes and 65% for native MOS diodes). (ii) At 100 mV input amplitude, the voltage level shifter with regular MOS diodes cease to function properly when the frequency of the input exceeds 100 MHz. The voltage level shifter with native MOS diodes, however, will continue to function properly even when the frequency of the input exceeds 10 GHz. The amount of voltage shift, however, is reduced from 65% at 1 MHz to approximately 41% at 10 GHz. A similar pattern is observed for other values of the amplitude of the input. (iii) The frequency at which the amount of voltage shift that the voltage level shifter can provide drops due to the increase of

the frequency of the input is smaller when native MOS diodes are used. The reason for this is the large channel ON-resistance of native MOS diodes as compared with that of regular MOS diodes.

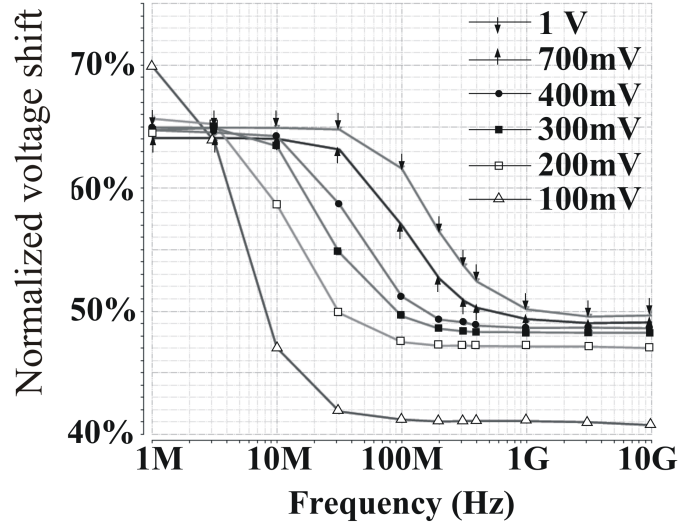


Figure 2.19: Effect of the amplitude and frequency of the input of single-stage positive level shifter with native MOS diodes. Circuit parameters : Clamping diode : $W/L=15 \mu\text{m} / 3 \mu\text{m}$; Compensating diode : $W/L=3 \mu\text{m} / 3 \mu\text{m}$.

2.5.4 Voltage Level Shifters with Bulk-Driven MOS Diodes

The reduction of the speed of voltage level shifters due to the small amplitude of the input can also be improved if bulk-driven MOSFETs are used for diodes. Bulk-driven is a mature technique frequently employed to adjust the threshold voltage of MOSFETs so as to achieve a specific design objective. Applying a positive voltage to the substrate lowers the threshold voltage of nMOS thereby offset the speed reduction caused by the small input. As compared with native MOS diodes, bulk-driven MOS diodes provide designers with a much needed extra design freedom.

2.5.5 Speed

The proposed voltage level shifters require an initial settling phase in which the clamping capacitors are charged. When the initial charging process is completed, the clamping current and compensating current are equal and we say that the voltage level shifters are in an equilibrium state. The operation of the voltage level shifters from now on is merely the charging and discharging of the capacitors by MOS diodes with nearly very small time constants when there is a change at the input of the voltage level shifters. This is the reason that the proposed voltage level shifters can operate at high frequencies. Please note that these few cycles are only needed at the very beginning of the voltage level shifters and are not needed once the equilibrium state is established. Fig.2.20 plots the response of the single-stage positive voltage-level shifter with a 2.4 GHz 1 V sinusoidal input during the initial charge-up process. It is observed that the voltage level shifter does require a few cycles (< 50 cycles) initially to establish the equilibrium state.

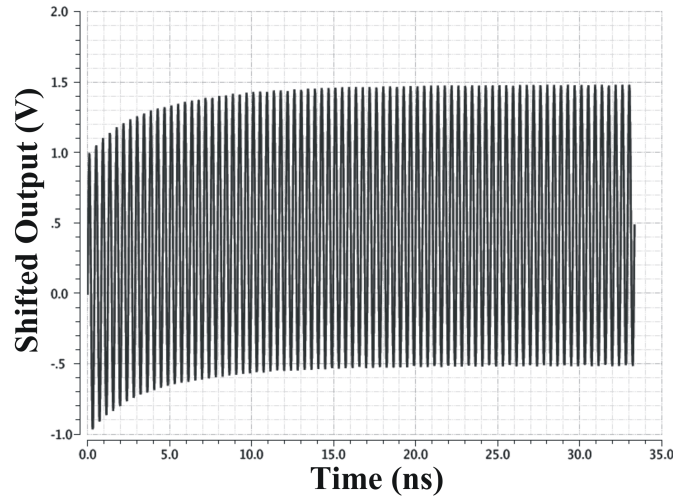


Figure 2.20: Propagation delay of voltage level shifter in initial charge-up state.

Fig.2.21 plots the response of the single-stage positive voltage-level shifter to a sudden change at the input after the voltage level shifter is in the equilibrium state. It is seen that once the equilibrium is established, the output of the voltage level shifter responds to the change of the input instantaneously.

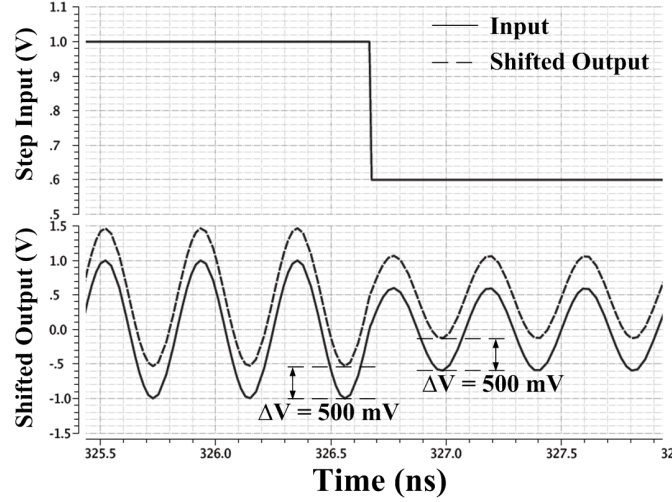


Figure 2.21: Propagation delay of voltage level shifter in equilibrium state.

2.5.6 Disturbances at Input

Assume a positive transient disturbance of amplitude ΔV_m and duration $\Delta t = t_2 - t_1$ is encountered at t_1 . At $t = t_1^-$ is present at the input, as shown in Fig.2.22, $v_{in}(t_1^+) = V_m$ and $v_c(t_1^-) = V_m - v_{clamp}(t_1^-)$. At $t = t_1^+$, $v_{in}(t_1^+) = V_m + \Delta V_m$. Since $v_c(t_1^+) = v_c(t_1^-)$, $v_{clamp}(t_1^+) = V_m + \Delta V_m$. During $t_1 < t < t_2$, since v_{clamp} is large, M2 will leave sub-threshold and enter strong inversion. As a result, v_c will be charged by a large current and rise rapidly. v_{clamp} , on the other hand, will drop at the same rate by the same amount as those of v_c . If the increment of v_c due to the disturbance is ΔV_c , i.e., $v_c(t_2) = v_c(t_1) + \Delta V_c$ where $\Delta V_c > 0$, since $v_{in}(t_2^+) = V_m$, $v_{clamp}(t_2^+) = v_{in}(t_2^+) + v_c(t_2^+) = -[V_m + v_c(t_1) + \Delta V_c]$, the output voltage will experience a dip. If we assume $v_{clamp}(t_1) = v_{clamp}(t_2)$ without the disturbance, then $\Delta v_{clamp}(t_2) = \Delta V_c$. During $t_2 < t < T/2$, the extra charge of C will be discharged through the path provided by M1. Since M1 is in sub-threshold, the discharge of C is rather slow. As a result, at $t = T/2$, $v_{clamp}(T/2)$ will be smaller as compared with that without the disturbance. Extensive simulation reveals that voltage shift error is proportional to the duration of the disturbance. The longer the duration, the larger the voltage shift error. It is also observed that the voltage shift is independent of the amplitude of the disturbance. The larger the amplitude of the disturbance, the faster the discharge of the charge of C when the disturbance vanishes. As a result, the final voltage at $t = T/2$ remains unchanged as most

of the charge of C has already been discharged when $t = T/2$. If the transient disturbance is negative, it will have no impact on the voltage shift. We conclude from the preceding analysis that transient disturbances have little impact on voltage shift.

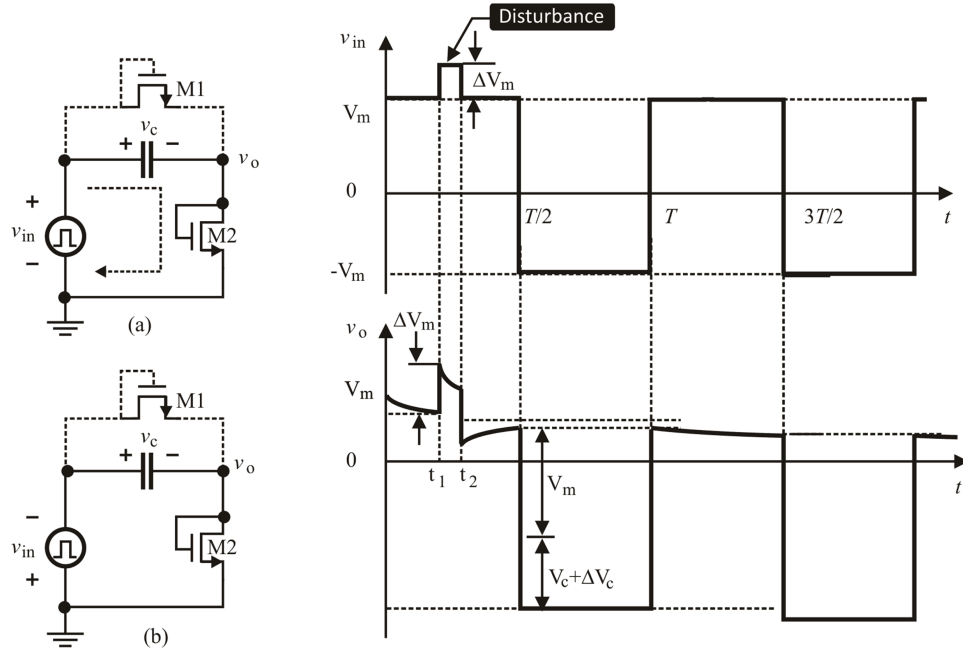


Figure 2.22: Response of single-stage negative voltage shifter whose input has transient disturbances.

2.5.7 Distortion

The waveform of the output of the proposed voltage level shifters is identical to its input signals with the median shifted either positively or negatively. To verify this, the total harmonic distortion (THD) of the output of the voltage level shifters to a sinusoidal input is analyzed using Spectre. Fig.2.23 plots the dependence of the THD of the output of the single-stage positive voltage level shifter to the amplitude of a 2.4 GHz sinusoidal input. It is seen although the THD levels up with the increase of the amplitude of the input, it is below 0.04%, revealing that the proposed voltage level shifters are well suited for analog signaling.

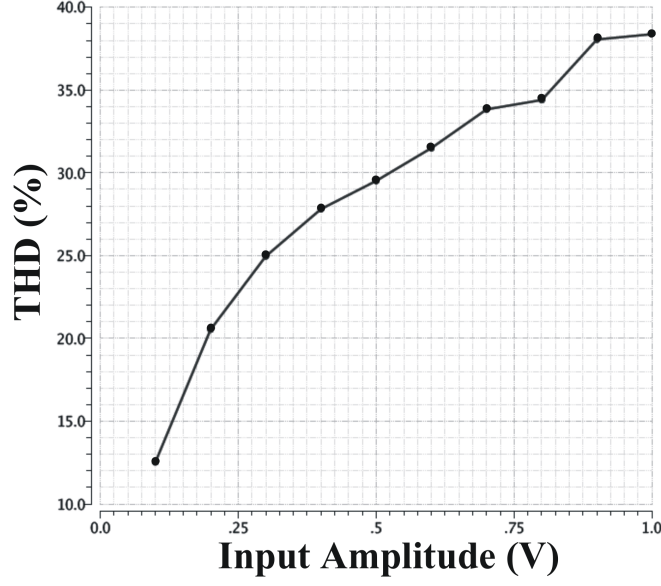


Figure 2.23: Total harmonic distortion of the output of single-stage positive voltage level shifter to a 2.4 GHz sinusoidal input.

2.5.8 Loading Effect

Because the proposed voltage level shifters are designed to operate in sub-threshold to minimize power consumption, the current drawn by the voltage level shifters from the input is therefore minimal. An alternative way to look at this is that the input impedance of the voltage level shifter is very large due to the sub-threshold operation of MOS diodes (large channel resistance in weak inversion). As a result, the resistive loading effect of the voltage level shifter on the input source is minimal.

The capacitive loading effect of the voltage level shifters can be analyzed using the negative voltage level shifter shown in Fig.2.24. To simplify analysis, we only consider the gate-source capacitance of MOSFETs. Thus, for capacitance analysis, M1 is replaced with C_{gs1} and M2 is replaced with C_{gs2} . It can be shown that

$$\begin{aligned}
 C_{in} &= \frac{(C_{gs1} + NC)C_{gs2}}{MC_{gs1} + NC_{gs2} + MNC} \\
 &\approx \frac{(C_{gs1} + NC)C_{gs2}}{MNC} \approx \frac{C_{gs2}}{M}.
 \end{aligned} \tag{2.20}$$

Note that we have assumed $MNC \gg MC_{gs1}, NC_{gs2}$ and $C \gg C_{gs1}, C_{gs2}$ in simplification of (2.20). Eq. (2.20) reveals that the input capacitance of the voltage level shifter seen by the source is small, especially when M is large.

The preceding findings are critical as they confirm that the proposed voltage level shifters will have a large input resistance and a small input capacitance. As a result, they will have the minimum impact on the input source.

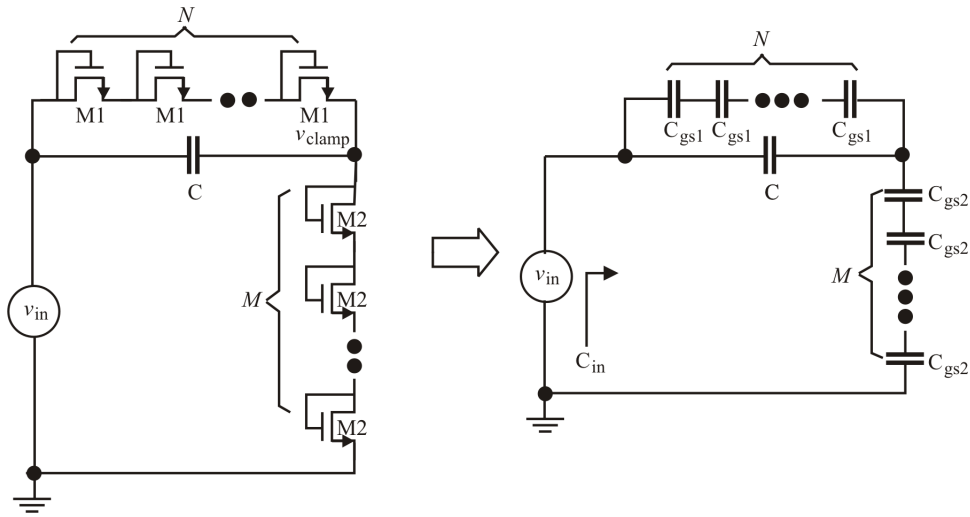


Figure 2.24: Capacitive loading effect of negative voltage level shifter.

2.5.9 Driving Capability

The effect of a capacitive load on the performance of the proposed voltage level shifters can be studied using Fig.2.25. When the clamping diode M2 is ON, the output voltage is the same as the voltage drop of the clamping diode and is defined as $v_{clamp,max}$ given earlier. When the clamping diode M2 is OFF, C_L and C_1 are in series such that $v_{clamp,min}$ becomes $C_1/(C_1 + C_L)v_{clamp,min}$. A similar approach can be used for cascaded and superimposed voltage level shifters.

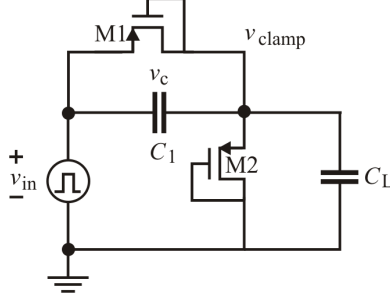


Figure 2.25: Load capacity of voltage level shifters.

2.5.10 Sizing Capacitors

Since in the steady state, the voltage of the clamping capacitors is determined by the current balance of the clamping and compensating diodes and will remain unchanged, the size of the clamping capacitors will therefore not affect the amount of voltage shift. It will, however, dictate the duration of the initial charge-up of the capacitors. To minimize the initial settling time, smaller clamping capacitors are desirable. Larger clamping capacitors, however, are preferred from a driving capability point of view. To compromise, we size the clamping capacitors using $C_1 \geq C_2 \geq \dots \geq C_N$. This is because clamping currents in later stages taper off. To minimize resultant speed penalty, the capacitance value is gradually reduced.

2.5.11 Power Consumption

The proposed voltage level shifters are powered by the input signal and are therefore truly passive. In the initial power-up, the clamping capacitors will be charged by the input signal and the voltage level shifters will draw a large current from the input source during the initial charge-up. To minimize the power consumption associated with the initial charge-up, smaller clamping capacitors are desirable. After the initial settling, the voltage level shifters enter the steady state (the equilibrium state). The only current drawn from the input signal source by the voltage level shifters in this case is the compensation current. Since MOS diodes operate in sub-threshold, the compensation current is very small. As a result, the voltage level shifters consume little static and dynamic powers. The power consumption of the proposed voltage level shifters is compared with other existing topologies in Table 2.6. Other common benchmark metrics of voltage level shifters are also compared.

2.5.12 ASK Demodulator

We use a low-power ASK demodulators to demonstrate the potential application of the proposed voltage shifters in passive wireless microsystems. ASK modulated data can be demodulated using a variety of approaches with envelope-based ASK demodulation the most popular due to their simplicity subsequently low power consumption. Envelope-based ASK demodulation, however, suffers from a low data rate [39]. The data rate of ASK demodulators can be improved by directly comparing the carrier with a reference at the cost of circuit complexity subsequently high power consumption. In this design the proposed voltage level shifter is used to shift the incoming ASK carrier. The shifted carrier is then compared to the threshold voltage of a static CMOS inverter to recover the baseband data, as shown in Fig.2.26.

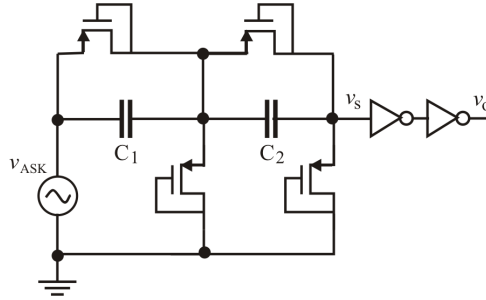


Figure 2.26: ASK demodulator utilizing a 2-stage cascaded negative voltage level shifter. Circuit parameters : $C_1=500$ fF, $C_2 = 500$ fF, and $W/L = 1.6 \mu\text{m} / 0.12 \mu\text{m}$.

The modulated data is 1.2 Gbps NRZ on a 2.4 GHz carrier with a 60% modulation index. The voltage of the ASK signal is ± 1 V. The voltage level shifter is a 2-stage cascaded negative voltage level shifter. The ASK demodulator is designed in an IBM 120 nm 1.2 V CMOS technology. The simulation results of the ASK demodulator are shown in Fig.2.27. The voltage shifter consumes only $1.7 \mu\text{W}$. The inverter pairs consume $20 \mu\text{W}$ due to high switching frequency. Table 2.5 compares the power consumption of reported ASK demodulators including the proposed ASK demodulator. Also important is that the power consumption of the proposed ASK demodulator is only $21.7 \mu\text{W}$ even though the data rate is 1.2 Gbps. Since most of the power is consumed by the two inverters whose dynamic

Table 2.5: Performance comparison of ASK demodulators for passive wireless microsystems.

Ref.	Tech.	Data rate	Power
[46](2004)	0.35 μm	10 Kbps	10 mW
[3](2006)	0.6 μm	18 Kbps	70 μW (CDR included)
[11] (2007)	0.25 μm	1 Mbps	– (over 23 transistors)
[47](2008)	0.35 μm	250 Kbps	1 mW
[48](2008)	180 nm	1 Mbps	336 μW
This work	130 nm	1.2 Gbps	21.7 μW

power consumption is directly proportional to the frequency of the input signal, the power consumption of the ASK demodulator will be approximately 21.7 nW if the data rate drops to 1.2 Mbps.

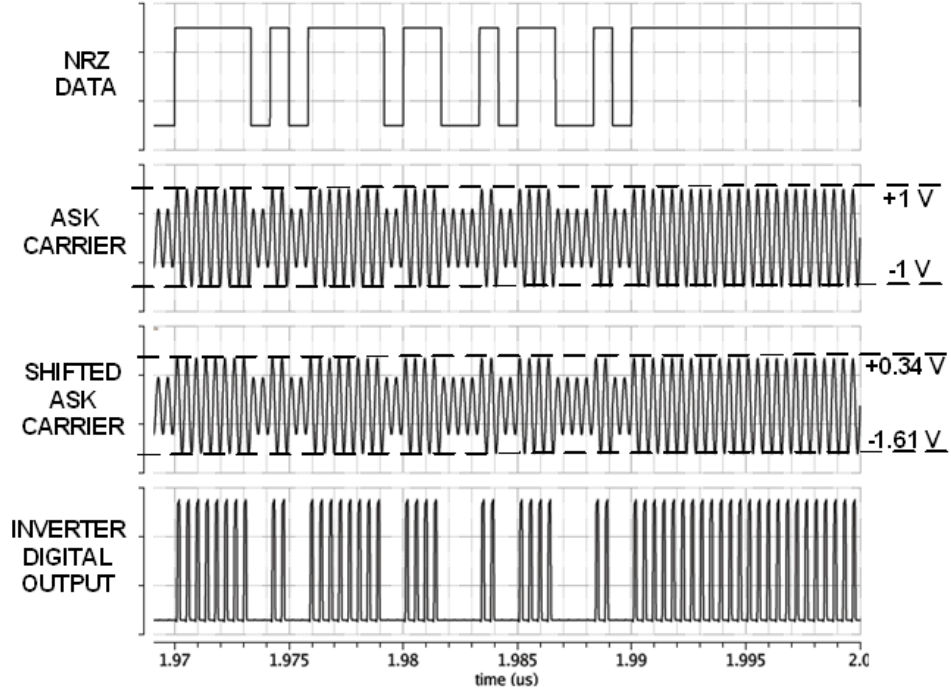


Figure 2.27: Response of ASK demodulator utilizing a 2-stage cascaded negative voltage level shifter. Top plot : Baseband data. Second plot : ASK carrier. Third plot : Output voltage of voltage level shifter v_s . Bottom plot : Output of ASK demodulator v_{clamp} .

2.6 Measurement Results

The proposed voltage level shifters have been implemented in 1.2 V IBM 0.13 μm CMRF8SF technology. Fig.2.28 is the layout of a single-stage positive voltage level shifter with $M_1 = N_1 = 1$. Fig.2.29 shows the layout of a 2-stage cascaded negative voltage level shifter with $M_1 = N_1 = 1$ and $M_2 = N_2 = 1$. Both designs employ a 50Ω passive resistor at its input for impedance matching. MiM capacitors have been chosen for clamping capacitors in both designs due to its relatively constant capacitance, needless substrate biasing and small parasitic capacitances to the substrate. For the positive voltage level shifter in Fig.2.28, NFETs were used as clamping and compensation diodes for low-leakage design discussed in Section 2.4. Similarly, for the negative voltage level shifter in Fig.2.29, PFETs were used instead for their low-leakage effects.

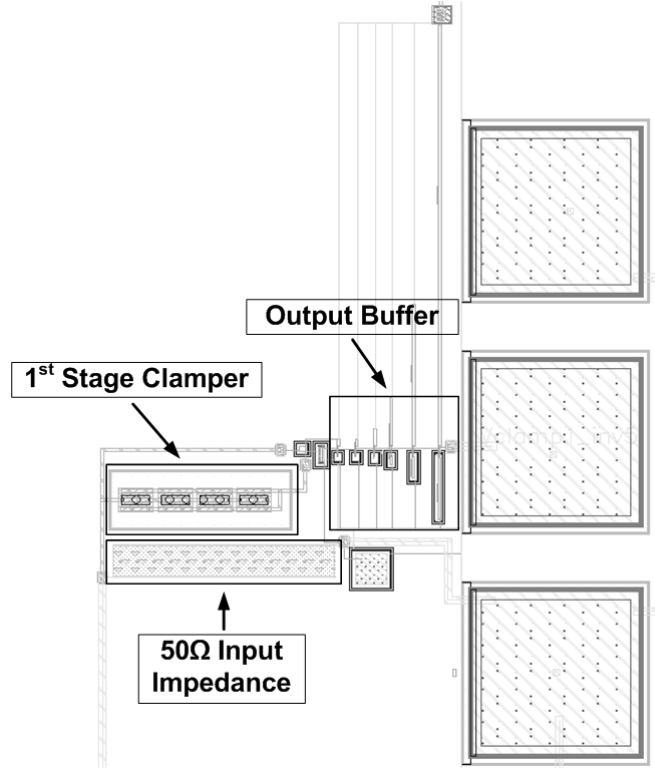


Figure 2.28: Single stage positive voltage level shifter with $M_1 = N_1 = 1$, $W_{1a}/L_{1a} = 30 \mu\text{m} / 0.56 \mu\text{m}$, $W_{1b}/L_{1b} = 6 \mu\text{m} / 0.56 \mu\text{m}$ and $C_{clamp} = 1 \text{ pF}$.

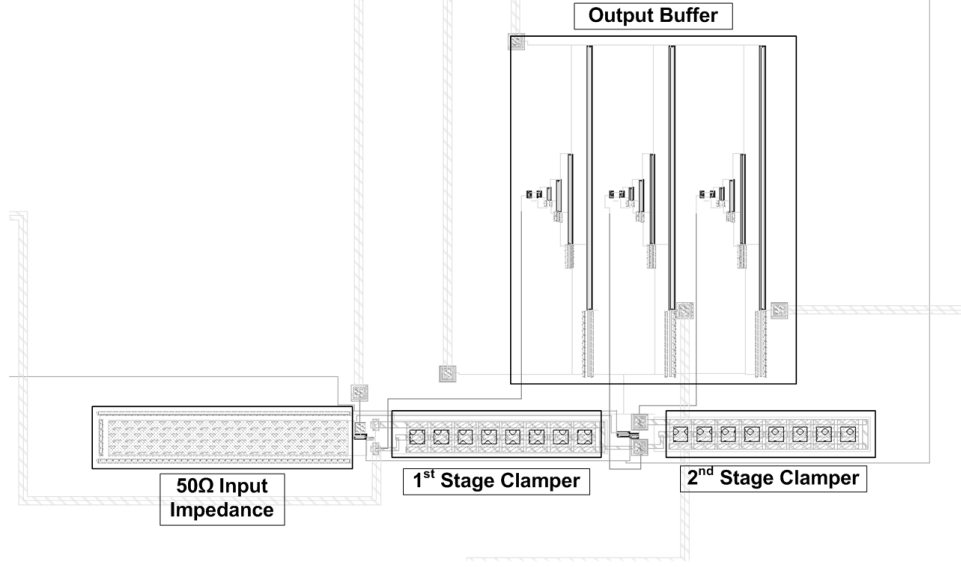


Figure 2.29: 2-stage cascaded negative voltage level shifter with $M_1 = N_1 = 1$, $M_2 = N_2 = 1$, $W_{1a}/L_{1a} = W_{1b}/L_{1b} = 3.2 \mu\text{m} / 0.12 \mu\text{m}$, $W_{2a}/L_{2a} = W_{2b}/L_{2b} = 1.6 \mu\text{m} / 0.12 \mu\text{m}$, and $C_{clamp1} = C_{clamp2} = 1.23 \text{ pF}$.

To observe the proper voltage shifting levels of incoming analog/RF signals at the output, output buffers must not introduce additional voltage level shifts, which implies that most common-drain-based or common-sourced-based buffers could not be applied in our design due to its biasing distortion. To drive a 50Ω oscilloscope load, an inverter-based buffer chain was used such that the voltage shifting levels can be measured indirectly as demonstrated in Fig.2.30 where A is the incident sinusoidal wave amplitude and ΔV_{shift} is the shifted voltage level. By shifting the input sinusoid positively or negatively, the resulted output will be asymmetric with respect to the ground level and the inverter-based output buffer will generate an asymmetric square wave with unequal duty periods for the high and low digital levels. The voltage shifting level is given by:

$$\Delta V_{shift} = A \cdot \sin\left(\frac{\pi}{2} - \theta\right) = A \cdot \cos(\theta) = A \cdot \cos\left(\pi \cdot \frac{\tau}{T}\right), \quad (2.21)$$

where θ is the above-ground passing angle of the shifted waveform. θ can be measured by the ratio of the duty periods as $\frac{\theta}{\pi} = \frac{2\theta}{2\pi} = \frac{\tau}{T}$ where τ and T are the duty intervals of the high and low levels of the buffer square-wave output signal respectively.

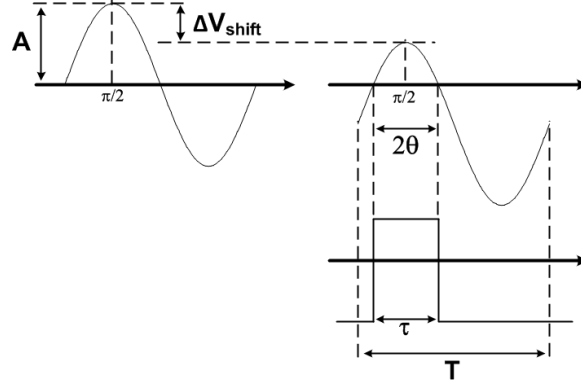


Figure 2.30: Calculation of voltage level shifts.

Fig.2.31 shows the die micrograph of the fabricated chip of the cascaded negative voltage level shifter of Fig.2.29 with probes in place for on-wafer measurement. On-wafer probing of the chip was conducted using a Microtech RF- 1 probe station to minimize the effect of the parasitics of packages. The pads were arranged as per the configuration of the probes that we have. A Microtech DCQ-06 dc probe with six ceramic bladed needles configured as SGSSGS (S=signal and G=ground) were used to supply required dc biasing voltages. Three single-ended Microtech ACP-40-D-GSG-150 RF probes were used for input analog/RF signal and output level-shifted voltages of the 1st and 2nd stages. The input signal was arranged to the left side of the pads and the output signals were arranged to the bottom and right sides of the pads. Flexible RF cables were used to connect the probes and test equipments. The loss of cable including connectors and adapters was negligible at low frequencies. The ground of all G (ground) pads are connected together on chip to avoid on-chip ground loops. The analog/RF input signal was generated using a Rohde & Schwarz signal generator. The waveform of the output was captured using an Agilent MOS-X 3024A oscilloscope. The dc biasing voltages were provided by BK precision 9124 programmable dc power supplies.

Both voltage level shifters were designed at 2.4 GHz. Due to some unknown reasons during measurement, the output buffer self-rings through substrate coupling such that only lower-end frequencies of the input signal at the 1st shifting stage could be observed. Shown in Fig.2.32 are measurement results of the input and output signals of the cascaded negative

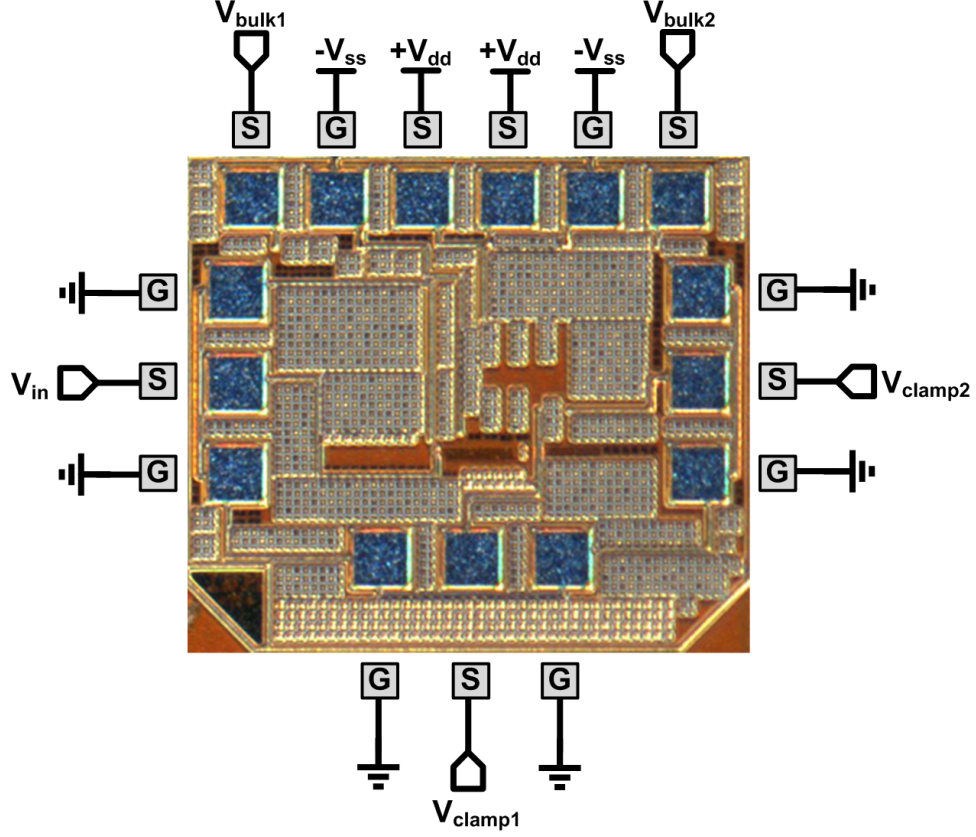


Figure 2.31: Micrograph of the cascaded negative voltage level shifter of Fig.2.29.

voltage level shifter of Fig.2.29. The input is a 10 KHz 400 mV amplitude sinusoidal and the output is a square-wave with uneven high/low duty intervals. The die was fabricated with 1.2 V regular- V_t devices such that the power supplies and substrate biasing from the 6-needle DC probe were: $V_{dd} = V_{bulk1} = V_{bulk2} = 0.6$ V and $V_{ss} = -0.6$ V, for V_{bulk1} and V_{bulk2} to be the n-well tie-up voltages for the PFET clamping and compensation diodes respectively. Measurement results are read from the oscilloscope that $\tau = 33.8 \mu s$ and $T = 100 \mu s$. By (2.21), the negative voltage shifting level at the 1st stage can be calculated to be: $400\text{mV} \cdot \cos\left(\pi \cdot \frac{33.8\mu s}{100\mu s}\right) = 400\text{mV} \cdot 48.72\% = 194.9 \text{ mV}$, which is close to the theoretically predicted voltage shifting level of $400\text{mV} \cdot 50\% = 200 \text{ mV}$.

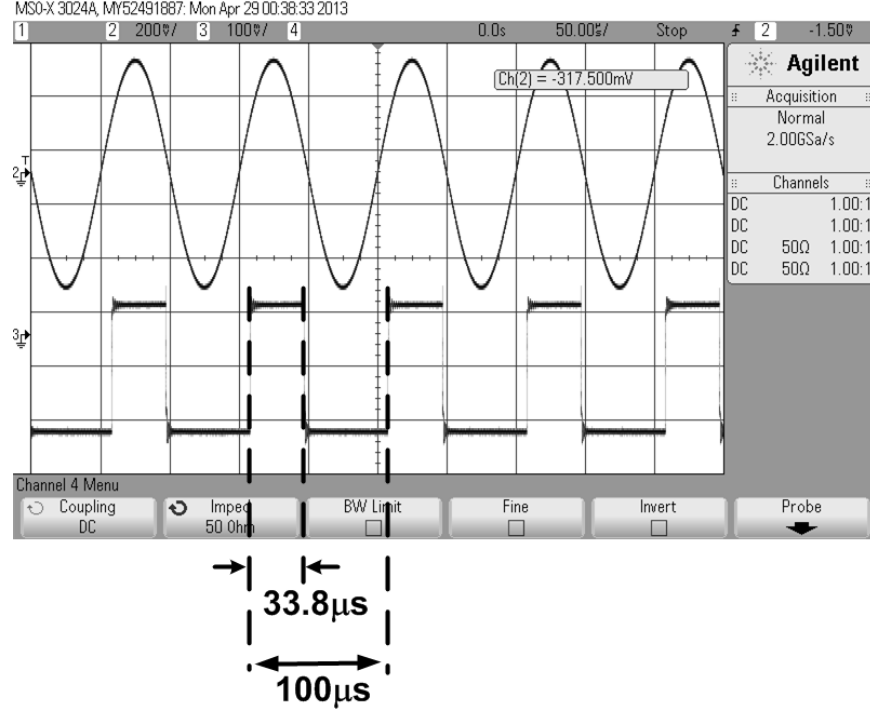


Figure 2.32: Measurement results on the 1st stage of the cascaded voltage level shifter in Fig.2.29

Table 2.6: Comparison of Voltage Level Shifters

Ref.	Tech.	Freq.	V_H	V_L	Delay	Power
[26]	0.25 μm SOI	200 KHz	0.35 V	1.2 V	125 ns	42.8 $\mu\text{W}/\text{MHz}$
[27]	1.5 μm CMOS	5 MHz	5 V	12 V	20 ns	0.3 mW/MHz
[29]	90 nm CMOS	1 MHz	200 mV	1 V	18.4 ns	9.3 nW/MHz
[30]	130 nm CMOS	1 MHz	280 mV	1.2 V	57.9 ns	10 $\mu\text{W}/\text{MHz}$
[31]	90 nm MTCMOS	1 MHz	180 mV	1.0 V	32 ns	2.5 nW/MHz
This Work	130 nm CMOS	2.4 GHz	340 mV	1.0 V	<10 ps	0.7 nW/MHz

2.7 Chapter Summary

A family of passive voltage level shifters for ultra-low power analog signaling were presented. The proposed voltage level shifters shift the median value of an analog signal in either positive or negative directions. The amount of voltage shift can be either a multiple or a fraction of the amplitude of the input signal with no restriction on the amplitude of the input signal. The proposed voltage level shifters are powered by the input signal and

are therefore truly passive, making them particularly attractive for applications such as implantable devices where power consumption is of a critical concern. The simple configuration of the proposed voltage level shifters also makes them well suited for high-frequency applications. A detailed mathematical treatment of the proposed voltage level shifters that provides the insight of the operational detail of the voltage level shifters was presented. Theoretical results were compared with simulation results. A good agreement was observed. Although the proposed voltage level shifters possess the mentioned advantages, its inputs are largely limited to AC signals which are required to reversely charge the diode-based clampers. To reduce loading effects in heavy loading applications, the required larger clamping capacitors could cause a concern in on-chip real estates.

Chapter 3

Remote Calibration for Maximum Power Harvest

Power harvest by passive wireless microsystems such as implantable devices [6, 35] becomes increasingly critical due to the need for on-chip power-demanding analog-to-digital conversion and digital signal processing. The efficiency that passive wireless microsystems harvest their operational power from radio-frequency waves is largely dominated by the conversion efficiency of voltage multipliers [21]. The power conversion efficiency of voltage multipliers can be increased by boosting the amplitude of the input voltage [33] or employing zero- V_T MOS transistors [20]. The former is achieved using a passive resonating LC tank [17]. Performance can be further improved if the inductor is replaced with a step-up transformer [37]. The input impedance and resonant frequency of the matching transformer, however, are severely affected by the variation of the load of the voltage multiplier, typically dictated by applications [38], and process spread. Impedance mismatch affects the amount of power transferred from the antenna to the transformer while frequency error affects the output voltage of the transformer and subsequently the power conversion efficiency of the voltage multiplier, especially when the quality factor of the transformer is large. Calibration of the input impedance and resonant frequency of the matching transformer is critical to the efficient power harvest of passive wireless microsystems. Common benchmark metrics for impedance matching networks in passive wireless microsystems are its voltage gain, input insertion loss (S_{11}), maximum deliverable power to a given load, and the power transfer efficiency from the antenna to the load of the impedance matching network.

This chapter presents a calibration technique to tune the input impedance and resonant frequency of the matching step-up transformer to achieve the maximum power transmission from the antenna to the transformer and the maximum power conversion efficiency of the voltage multiplier. Contributions of the calibration technique in a general passive wireless microsystem are shown in Fig. 3.1. The calibration technique tunes the transformer matching network by shunting a tunable varactor across the secondary terminal of the transformer. Simulation results show that by tuning the varactor, the input impedance of the transformer can be matched to the antenna radiation resistance exactly so as to eliminate matching errors due to process spread and loading variation. In Section 3.1, we derive the input impedance and voltage gain of the tuned transformer matching network. Section 3.2 presents the spice model of the designed on-chip transformer and investigates its performances in different error conditions. Section 3.3 introduces a low-power varactor current tuning technique. Section 3.4 presents a method that detects the optimum tuning state by introducing an ultra-low-power voltage level shifter. Post-layout simulation results and on-chip measurement results are reported in Section 3.5. Section 3.6 concludes the chapter.

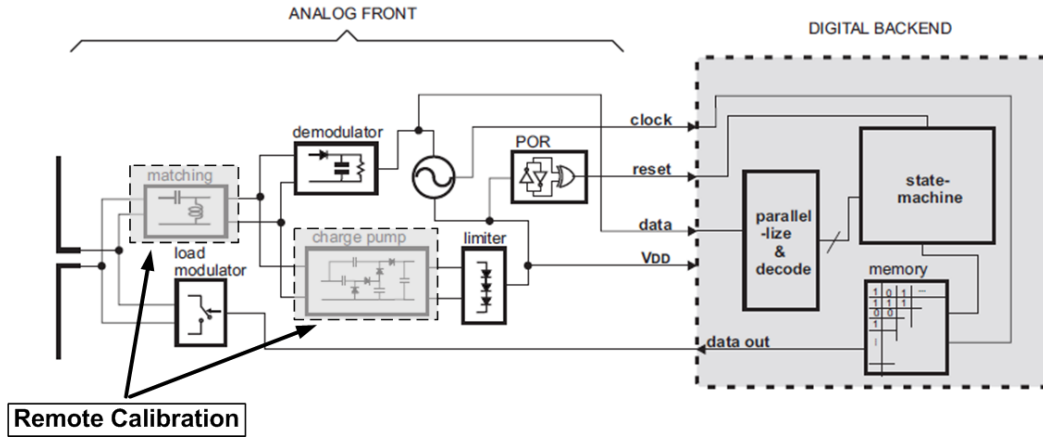


Figure 3.1: Contributions of the proposed remote calibration technique in a general passive wireless microsystem.

3.1 Transformer Impedance Tuning

3.1.1 Impedance Tuning

The proposed tunable transformer impedance matching network is shown in Fig.3.2 with a variable capacitor C_{tune} inserted between the secondary winding of the transformer and the voltage multiplier. The voltage multiplier is realized using MOSFET voltage rectifier and is usually modeled by C_m in parallel with R_m . The transformer is characterized by resistors R_{s1} and R_{s2} representing the series resistance of the primary and secondary windings, respectively, capacitors C_{p1} and C_{p2} representing the spiral-substrate shunt capacitance of the primary and secondary windings, respectively, C_{12} representing the capacitance between the primary and secondary windings, L_1 and L_2 representing the self inductance of the primary and secondary windings, respectively, and M representing the mutual inductance between the primary and secondary windings.

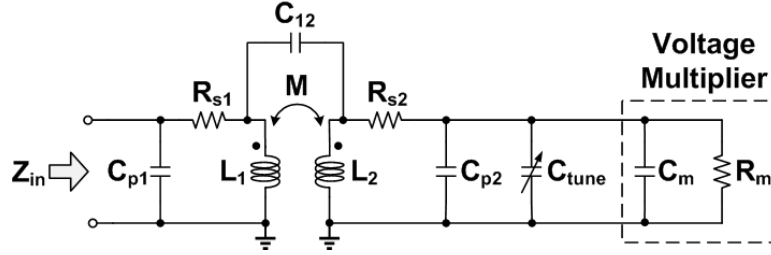


Figure 3.2: Proposed tunable step-up transformer impedance matching network.

To simplify analysis, R_{s1} and R_{s2} are replaced with shunt resistances R_{p1} and R_{p2} , and mutual capacitance C_{12} is replaced with two shunt capacitors C'_{12} and C''_{12} using Miller's theorem, as shown in Fig.3.3. C_{p1} and C'_{12} can be absorbed in L_1 since the capacitive reactance can be nulled by the inductive reactance of the primary winding. For the sake of convenience, we will still use L_1 to represent the overall effect of the inductance of the primary winding with C_{p1} and C'_{12} absorbed. To further simplify analysis, we neglect R_{p1} by assuming that the resistive loss of the primary winding is small. Such an assumption is justified as the number of the turns of the primary winding is much lower as compared with

that of the secondary winding and the width of the spiral of the primary winding is much larger as compared with that of the secondary winding [37]. The total capacitance seen by the secondary winding is given by

$$C_L = C_{12}'' + C_{p2} + C_{tune} + C_m \quad (3.1)$$

and the total shunt resistance seen by the secondary winding is given by $R_L = R_{p2} // R_m$.

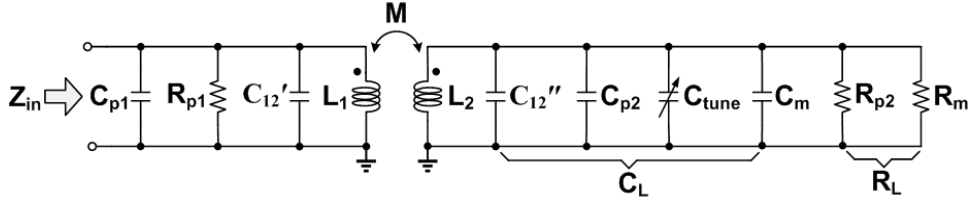


Figure 3.3: Tunable transformer impedance matching network.

Fig.3.4 shows the simplified schematic of the transformer impedance matching and gain boosting network. In the simplified model, the tuning of C_{tune} is equivalent to varying load capacitor C_L .

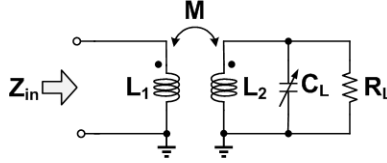


Figure 3.4: Simplified tunable transformer impedance matching network.

The input impedance of the simplified transformer matching network shown in Fig.3.4 is given by

$$Z_{in} = j\omega L_1 + \frac{\omega^2 M^2}{j\omega L_2 + Z_L}, \quad (3.2)$$

where

$$Z_L = \frac{R_L}{j\omega R_L C_L + 1}. \quad (3.3)$$

Since C_{tune} is a part of C_L , Z_{in} is a function of the tuning capacitor C_{tune} as well. By adjusting C_{tune} , the transformer input impedance can be found to be located on a track of a circle in a complex plane. Write the input impedance Z_{in} in the form $Z_{in} = \Re[Z_{in}] + j\Im[Z_{in}]$ and assume that the circle is centered at rectangular coordinates (p, q) with radius r . The input impedance matching circle can be represented by its norm (distance) from the center as:

$$||(\Re[Z_{in}] + j\Im[Z_{in}]) - (x + jy)|| = r. \quad (3.4)$$

It follows from (3.4) that

$$\Re[Z_{in}]^2 + \Im[Z_{in}]^2 - 2\Re[Z_{in}]x - 2\Im[Z_{in}]y + x^2 + y^2 - r^2 = 0. \quad (3.5)$$

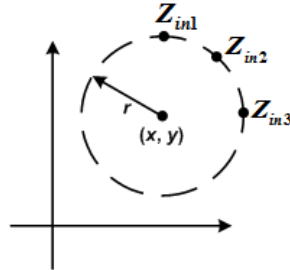


Figure 3.5: Impedance matching circle determined by tuning capacitors.

A circle can be determined by any of its three points on the track. Arbitrarily tuning C_{tune} into three different locations, C_{tune1} , C_{tune2} and C_{tune3} , we obtain a set of three different input impedances on the circle as shown in Fig.3.5 for $Z_{in1} = Z_{in}(C_{tune1})$, $Z_{in2} = Z_{in}(C_{tune2})$ and $Z_{in3} = Z_{in}(C_{tune3})$ using the Z_L and Z_{in} equations given in (3.3) and (3.2) respectively. By expanding (3.4) into its polynomial and substituting Z_{in1} , Z_{in2} and Z_{in3} into (3.5), a linear group can be established as,

$$\left\{ \begin{array}{l} \Re[Z_{in1}]^2 + \Im[Z_{in1}]^2 \\ \quad -2\Re[Z_{in1}]x - 2\Im[Z_{in1}]y + x^2 + y^2 - r^2 = 0, \\ \Re[Z_{in2}]^2 + \Im[Z_{in2}]^2 \\ \quad -2\Re[Z_{in2}]x - 2\Im[Z_{in2}]y + x^2 + y^2 - r^2 = 0, \\ \Re[Z_{in3}]^2 + \Im[Z_{in3}]^2 \\ \quad -2\Re[Z_{in3}]x - 2\Im[Z_{in3}]y + x^2 + y^2 - r^2 = 0, \end{array} \right. \quad (3.6)$$

And the location of the circle can be solved from (3.6) to be:

$$\left\{ \begin{array}{l} x = \frac{M^2 R_L}{2L_2^2}, \\ y = \frac{L_1 L_2 \omega - \omega M^2}{L_2}, \\ r = \frac{M^2 R_L}{2L_2^2}. \end{array} \right. \quad (3.7)$$

It is seen from (3.7) that the location (x, y) and radius r of the input impedance matching circle are determined by the properties of the transformer (L_1 , L_2 and M) and that of the voltage multiplier (R_L), and are not tuned by the tuning capacitor C_{tune} . The variation of C_{tune} only causes the input impedance Z_{in} to move around the circle to find the optimum position for impedance matching. The real-part of the input impedance $\Re[Z_{in}]$ can thus be tuned to match the antenna radiation resistor R_{ant} . The imaginary part $\Im[Z_{in}]$ can be tuned to resonate with an additional serial matching capacitor to achieve a high voltage gain

as that in conventional LC matching networks. The tuning of the input impedance matching network also facilitates the compensation of the variation of the resonance frequency of the LC network formed by the transformer and C_L , so as to offset the effects of the errors of self-inductances L_1 and L_2 arising from process spread.

3.1.2 Equivalent Model of Transformer Impedance Matching Network

The input impedance track of the transformer matching network around a circle when tuned by C_{tune} can be understood by its real part $\Re[Z_{in}]$ and imaginary part $\Im[Z_{in}]$. For the part of the track in the 1st quadrant, $\Re[Z_{in}] > 0$ is interpreted as a variable resistor with resistance $R_{eq} = \Re[Z_{in}]$ and $\Im[Z_{in}] > 0$ is interpreted as a variable inductor with inductance $L_{eq} = \Im[Z_{in}]/\omega$, as shown in Fig.3.6.

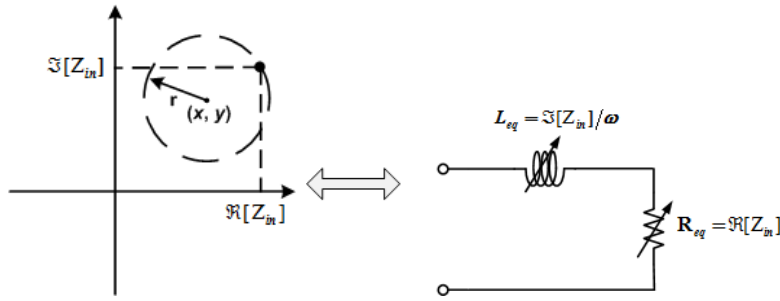


Figure 3.6: $L - R$ equivalent circuit of transformer impedance matching network.

The transformer matching network, together with the antenna represented by V_{ant} and R_{ant} , are shown in Fig.3.6. In order to provide a purely resistive matching resistance to the antenna, capacitor C_{match} is inserted. C_{match} will resonate with L_{eq} at the desired frequency, i.e., 2.4 GHz in our design. Since both L_{eq} and R_{eq} are the functions of C_{tune} , R_{eq} should be tuned to R_{ant} for the maximum power transfer at 2.4 GHz while L_{eq} will be resonated out with C_{match} at 2.4 GHz.

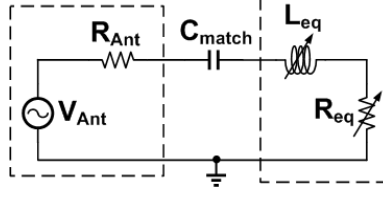


Figure 3.7: Variable $L - R$ model for impedance matching.

3.1.3 Quality Factor and Voltage Gain

The proposed tuned transformer impedance matching network achieves maximum power transfer and maximum voltage transfer simultaneously. The maximum power transfer is realized by tuning the input impedance of the transformer network at the antenna radiation resistance. And the maximum voltage transfer is by resonating both the primary and secondary windings at the operating frequency. The maximum voltage gain greatly improves the power conversion efficiency of the voltage multiplier due to the large input amplitude across the rectifying diodes. And the voltage gain A_v can be denoted as the product of the tuned transformer quality factor Q and its turn ratio n as:

$$A_v = Q \cdot n = Q \cdot \sqrt{\frac{L_2}{L_1}}, \quad (3.8)$$

where the tuned transformer quality factor is obtained by substituting (3.2) into (3.8),

$$\begin{aligned} Q &= \frac{\Im m[Z_{in}]}{\Re e[Z_{in}]} \\ &= \frac{L_1(C_L^2 L_2^2 R_L^2 \omega^4 - 2C_L L_2 R_L^2 \omega^2 + L_2^2 \omega^2 + R_L^2)}{(M^2 R_L \omega)} \\ &\quad - \frac{\omega(L_2 C_L^2 R_L^2 \omega^2 - C_L R_L^2 + L_2)}{R_L}. \end{aligned} \quad (3.9)$$

The quality factor of the tuned transformer is equivalent to the quality factor of the transformer equivalent model in Fig.3.6, where L_{eq} resonates with a serial matching capacitor C_{match} to achieve a resonant voltage peak. And the peak results in a maximum voltage across

the primary winding of the transformer, which in turn produces a maximum voltage on the secondary winding due to the transformer turn ratio n .

3.2 Transformer Matching Model

To verify the preceding theoretical findings, a spiral transformer is designed in IBM 0.13 μm CMRF8SF process. The spirals are shown in Fig.3.8 with the primary and secondary windings implemented with the second last (E1) and last (MA) top thick metal layers respectively. The top thick metal layer has the lowest resistive loss and capacitive loss. An extra shielding layer (BFMOAT) was inserted to isolate the transformer to the substrate to reduce the eddy current-induced loss. The primary winding is in a diameter of 150 μm and a number of turns $n_1 = 4$; the secondary winding is in a diameter of 300 μm and a number of turns $n_2 = 13$. The spice model of the transformer is extracted using ADS Momentum with circuit parameters given in Table 3.1.

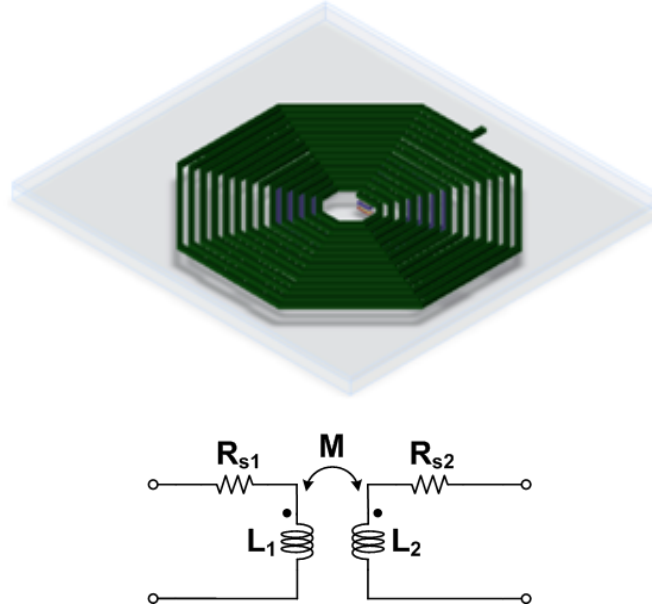


Figure 3.8: Top: Layout of step-up transformer. Bottom: equivalent circuit.

Table 3.1: Parameters of hexagon step-up transformer.

Windings	Parameters	Value
Primary (E1 metal layer)	Number of turns	4
	Diameter	150 μm
	Spiral width & spacing	5 μm & 5 μm
	Self-inductance	$L_1 = 3.016 \text{ nH}$
	Spiral series resistance	$R_{s1}=1.14 \Omega$
Secondary (MA metal layer)	Number of turns	13
	Diameter	300 μm
	Spiral width & spacing	5 μm & 5 μm
	Self-inductance	$L_2 = 44.84 \text{ nH}$
	Spiral series resistance	$R_{s2}=18.07 \Omega$.
	Mutual inductance	$M=7.983 \text{ nH}$

The proposed tuned transformer impedance matching network is loaded with a voltage multiplier that converts harvested AC power to a DC voltage. Depending on input signal amplitude and output DC current, the voltage multiplier can be modeled by the equivalent circuit shown in Fig.3.9 [33]. Assuming the input signal amplitude is 500 mV and an average output DC current of 100 μA , its input impedance can be estimated by the periodic steady state analysis for a single stage half-wave voltage doubler with zero-Vt NFET of $W/L=6 \mu\text{m}/0.42 \mu\text{m}$. By varying the voltage multiplier loading R_{dc} from 1 K Ω to 1 M Ω , the equivalent input resistance R_{eq} and capacitance C_{eq} are shown in Fig.3.9 as well.

Assuming the voltage doubler is loaded with $R_{dc} = 10 \text{ K}\Omega$, its input equivalent impedance can be found from Fig.3.9 with $R_{eq} \approx 3 \text{ K}\Omega$ and $C_{eq} \approx 12 \text{ fF}$. Since C_{eq} and C_{tune} are merged into C_L , and R_{eq} into R_L as in Fig.3.3, the transformer input impedance is simulated in Fig.3.10 for the impedance circle as predicted by (3.7). By setting $C_{match} = 1.12 \text{ pF}$ and tuning $C_L \approx 68 \text{ fF}$, Z_{in} passes 50 Ω in the real axis, which matches the antenna radiation resistance and produces a dip in S_{11} at 2.4 GHz in Fig.3.11. The transformer resonant gain on the secondary winding $G_{tran} = V_{out}/V_a$ and the powers on the primary and secondary terminals are also shown. The power on the secondary terminal P_{out} is slightly less than the incident power on the primary terminal P_{in} due to the parasitic losses of on-chip coils, but the loss will be compensated by a much higher power conversion efficiency in the following voltage multiplier due to the larger transformer gain.

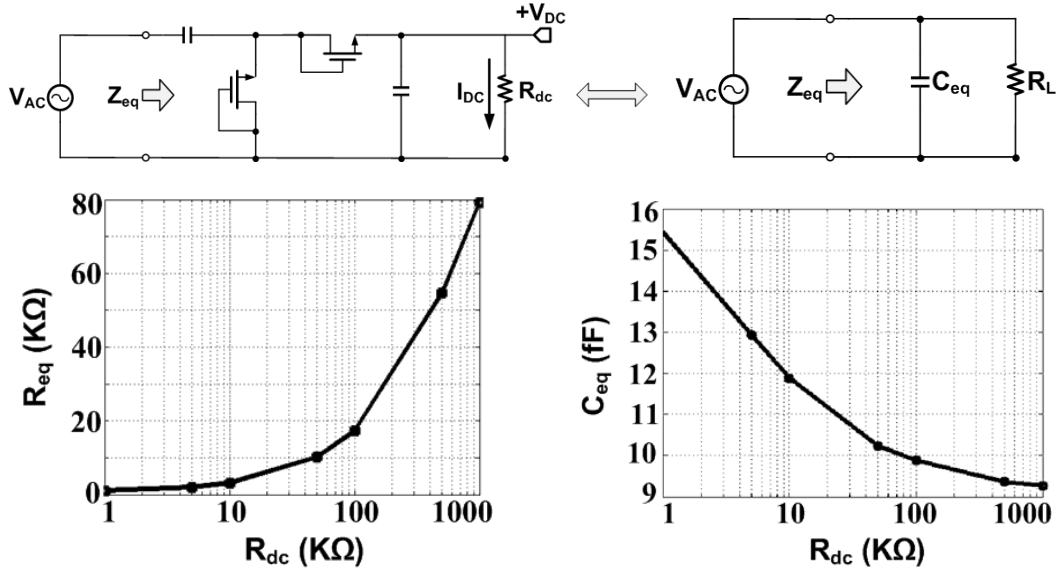


Figure 3.9: Top Left: Single-stage half-wave voltage doubler. Top Right: Equivalent circuit. Bottom Left: Simulated input resistance. Bottom Right: Simulated input capacitance.

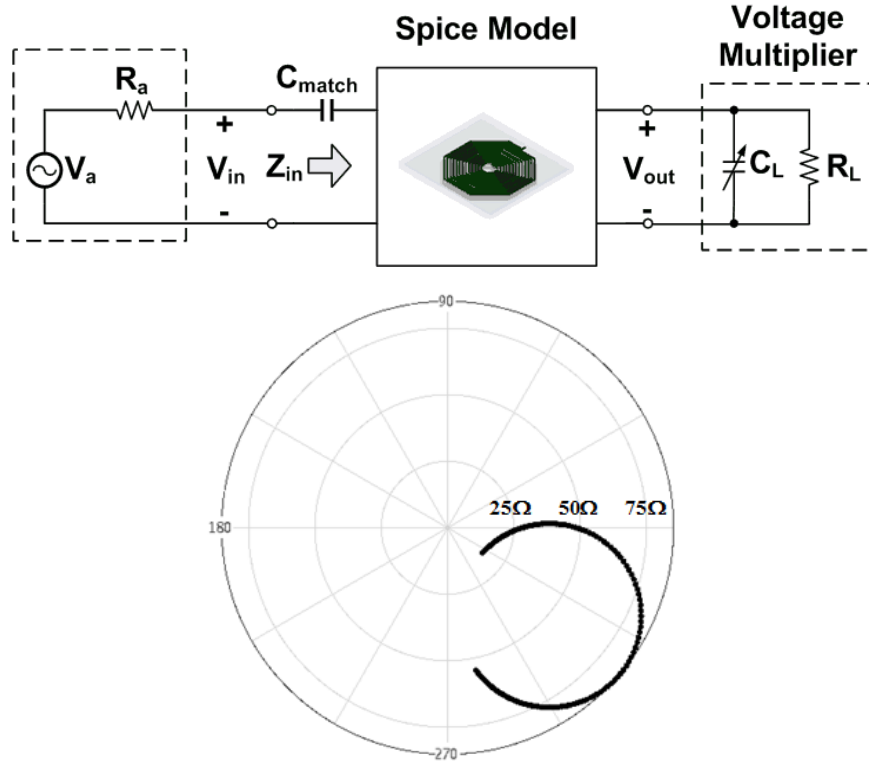


Figure 3.10: Top: Series capacitor-transformer network. Bottom: Input impedance. C_L is varied from 10 pF to 200 pF.

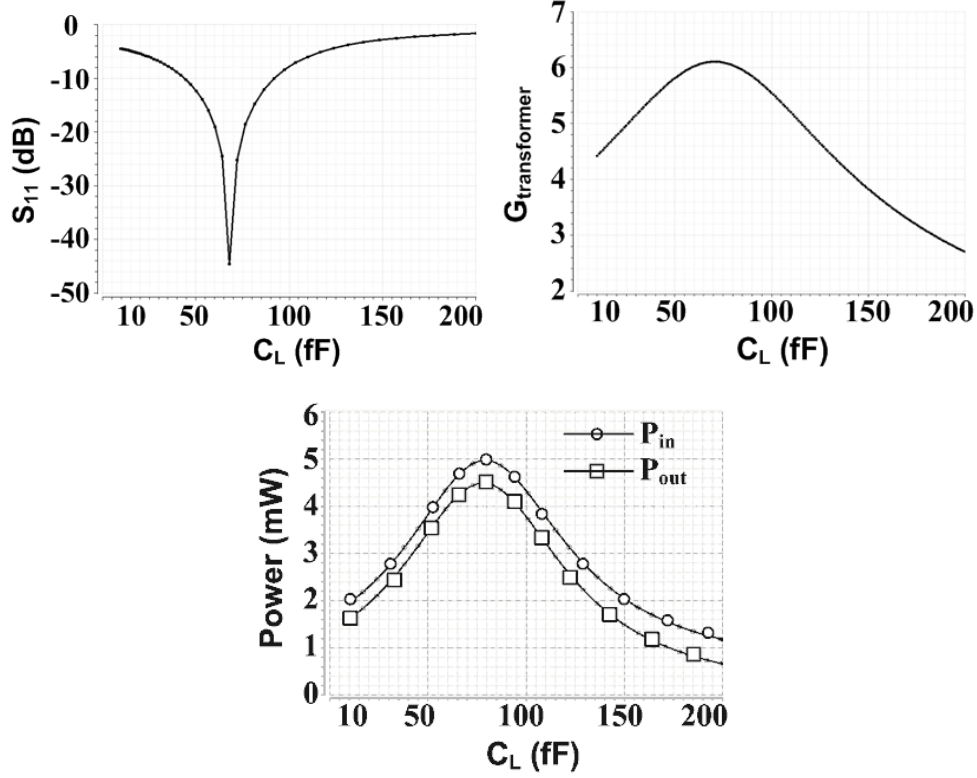


Figure 3.11: Top Left: S_{11} at the input port of capacitor-transformer network. Top Right: Voltage gain. Bottom: Power transfer.

3.2.1 Impedance and Frequency Tuning

Because the load of the voltage multiplier varies with applications, C_m and R_m used to model the voltage multiplier will vary as well. This will affect the input impedance, the resonance frequency, and the quality factor of the transformer matching network. Like other integrated devices, spiral transformers are also subjected to the effect of process spread, giving rise to errors in both self and mutual inductances subsequently the input impedance and resonance frequency of the transformer matching network. The error in resonance frequency will critically affect the voltage gain provided by the transformer matching network, specially when the quality factor of the transformer is high. Note that a large quality factor is highly desirable in boosting the voltage of the received signal. The uncertainty in both the load and the parameters of the transformer matching network demand that the transformer impedance matching network be tunable so as to achieve perfect impedance matching between the antenna and the transformer for the maximum power transfer from the antenna

to the transformer and resonance at the desired frequency for the maximum voltage gain subsequently the maximum power efficiency of voltage multipliers.

Since C_{match} is inserted between the antenna and the transformer impedance matching network, as shown in Fig.3.10, it is desirable that C_{match} can also be tuned along with the adjustment of C_L . Tuning C_{match} , however, turns out to be difficult due to the large series parasitic resistance of varactors. The resistive loss of the varactors that implements C_{tune} will severely reduce the quality factor of the transformer network subsequently lower its voltage gain. To avoid this difficulty, a fixed MIM capacitor is connected in series with the tuning varactor used in our design. To verify the tuning capability of the transformer impedance matching network for different loading conditions, s_{11} and the voltage gain are plotted in Fig.3.12 with R_L varied from 1 K Ω to 100 K Ω . Due to the matching capacitor C_{match} optimized at $R_L = 3$ K Ω , s_{11} worsens when R_L deviates from its optimum value 3 K Ω , as shown in Fig.3.11. The increasing return loss can be partially compensated by a larger voltage transfer gain, as shown in Fig.3.12.

To verify the tuning capability of the transformer-impedance matching network, a test bench shown in Fig.3.13 is used. The process spread-induced errors of the self-inductance of the transformer are represented by L_{err1} and L_{err2} for the primary and secondary windings, respectively. Similarly, the process spread-induced errors of the series resistance of the transformer are represented R_{err1} and R_{err2} for the primary and secondary windings, respectively. An approximation of $R_{eer} = L_{eer} \times 10^9$ (1 nH error in inductance will result in approximately 1 Ω error in series resistance) is used in our simulation. A 10% error for the primary and secondary inductances in the designed transformer in Fig.3.8 is represented by inductance errors $L_{eer1} = \pm 0.3$ nH and $L_{eer2} = \pm 4.5$ nH.

s_{11} and voltage gain are shown in Fig.3.14 for the primary winding and Fig.3.15 for the secondary winding. Because the secondary winding has a larger self-inductance, a 10% error causes the tuning curve to shift significantly. This will require the tuning capacitor C_{tune} to have a larger tuning range. For a +10% error in the secondary winding, $L_{eer2} = +4.5$ nH, the tuning capacitor is at $C_L = 25$ fF, and for a -10% error of $L_{eer2} = -4.5$ nH, the tuning capacitor is at $C_L = 115$ fF, both of which are largely away from the original designed tuning value at $C_L = 68$ fF.

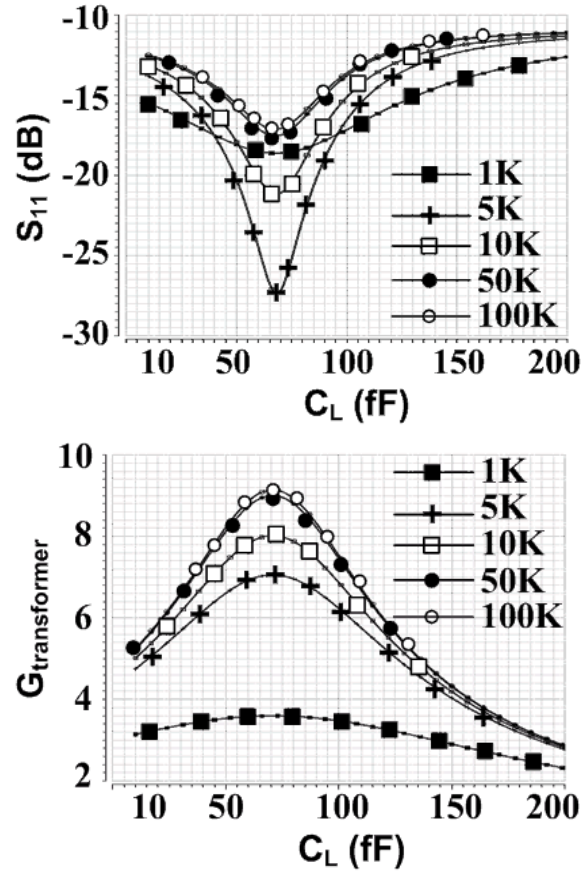


Figure 3.12: Loading effect. Top : s_{11} . Bottom : Voltage gain.

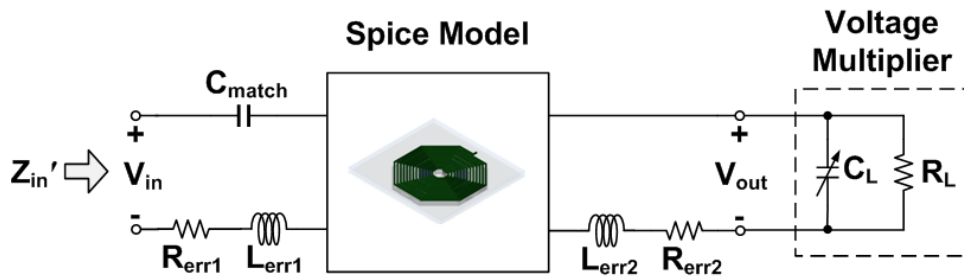


Figure 3.13: Test bench.

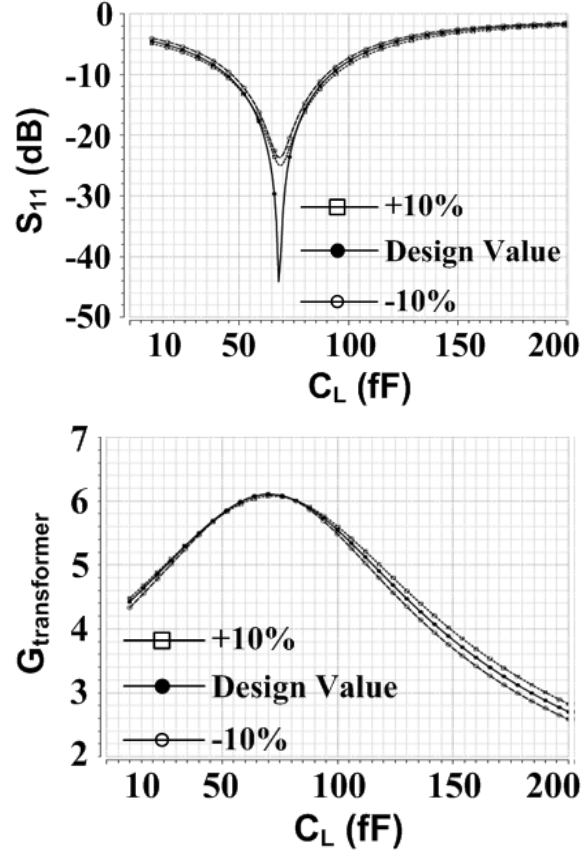


Figure 3.14: Effect of primary winding error. Top : s_{11} . Bottom: Voltage gain.

The drift of the resonance frequency of transformer matching network due to process spread can be compensated by tuning C_{tune} , as shown in Fig.3.16. For a +10% frequency error, C_L is tuned to 42 fF. For a -10% frequency error, C_L is tuned to 112 fF. The results are similar to the loss caused by inductance variation shown in Fig.3.15 since a frequency error can be treated equivalently to an inductance error.

3.3 Current Tuning

The tuning capacitor C_{tune} is implemented by a MOS varactor. To tune a MOS varactor, a variable DC voltage is typically needed as shown in Fig.3.17. But a variable DC voltage source is difficult to obtain in passive microsystems, so in this work we propose a current tuning technique as shown in Fig.3.18 for the minimum power consumption and circuit simplicity, where a pair of charge pumps are employed to adjust the voltage of the

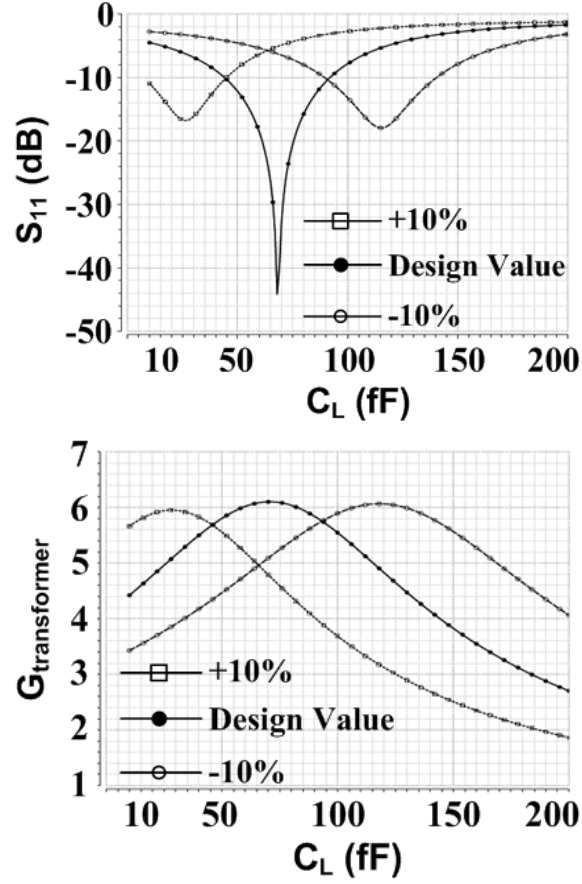


Figure 3.15: Effect of secondary winding error. Top : s_{11} . Bottom: Voltage gain.

tuning node V_{tune} . The injection pump injects a current to the tuning node to build up the tuning voltage for the varactor whereas the reset pump discharges the node thereby lowering the tuning voltage. The charging current needs to be sufficiently small to provide a fine tuning voltage. It is obtained by cascading pMOS switches in series such that the transistors operate in subthreshold region. The current of the reset pump, however, needs to be large in order to rapidly discharge the node subsequently lower the tuning voltage. A pair of ring oscillators are employed in Fig.3.18 as well to provide necessary clock signals for current injection and reset. When an optimum tuning voltage is reached, an ENABLE signal turns off the ring oscillators.

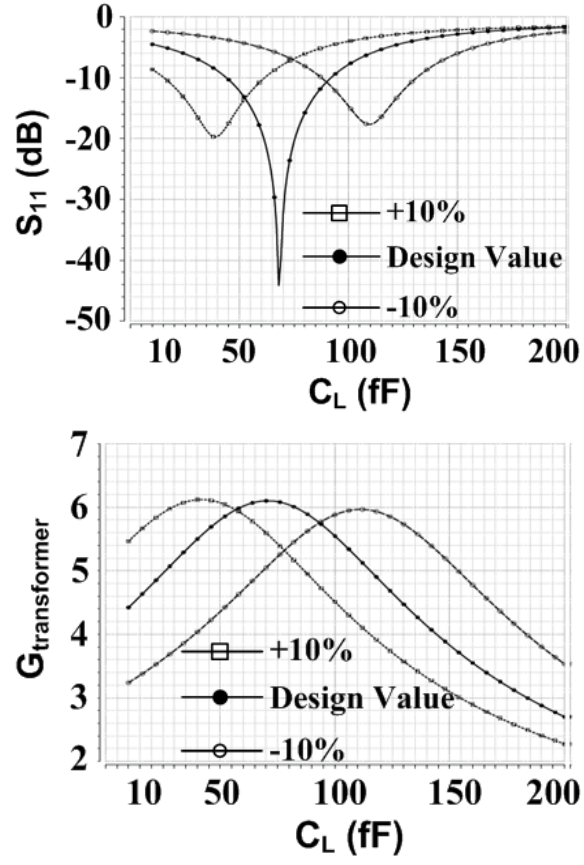


Figure 3.16: s_{11} and G_t due to frequency error.

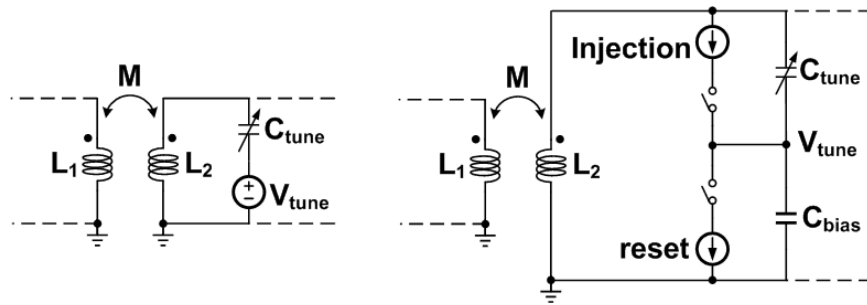


Figure 3.17: Voltage-mode varactor tuning.

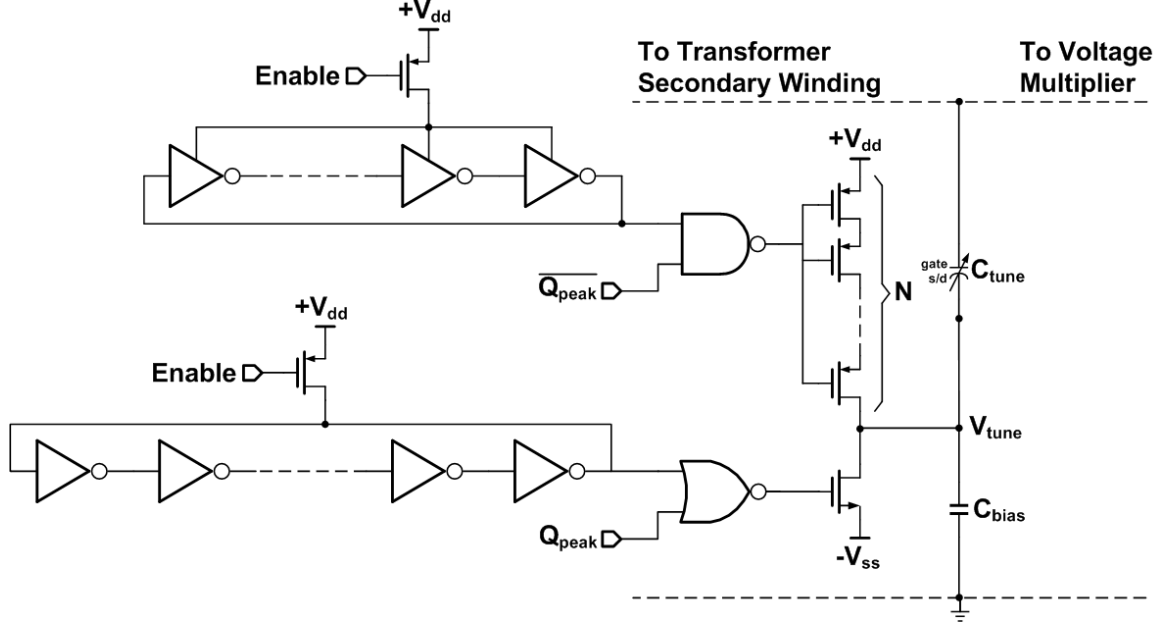


Figure 3.18: Current-mode varactor tuning. The injection pump is composed of eight series-connected PMOS transistors of dimensions $W/L = 0.5 \mu\text{m} / 0.4 \mu\text{m}$. The reset pump is a NMOS transistor of dimension $W/L = 5 \mu\text{m} / 0.4 \mu\text{m}$. The capacitance of the varactor of dimension $W/L = 6 \mu\text{m} / 2 \mu\text{m}$ can be varied from 26.4 fF at -0.5 V to 70.7 fF at 3.3 V. The biasing capacitor is 6 pF.

3.4 Peak Detection and Self Tuning

To detect whether the peak amplitude of the output voltage of the transformer reaches its maximum or not, in each C_{tune} tuning step, the input voltage of the voltage multiplier is shifted down by $V_m - V_T$ by the passive negative voltage level shifter formed by C_{clamp} and the MOS diode, as shown in Fig.3.19 [49]. Let the total load capacitance of the MOS diode be C_p . When the input voltage rises, I_{clamp} will flow through the diode, and C_{clamp} and C_p will be charged with total charge $Q_1 = I_1 \cdot T_{clamp}$ where T_{clamp} is the time in which the diode forward conducts. When the input voltage drops, the diode will switch off and the charge stored in C_p will be released through C_{clamp} by I_2 with total charge $Q_2 = C_s V_m$ and $C_s = C_p || C_{clamp}$. In the equilibrium, the charge stored in C_{clamp} by I_{clamp} is equal to the the charge released by I_2 . Since C_{clamp} is charged, the negatively shifted output forces the MOSFET into sub-threshold with current $I_{clamp} \approx I_t \exp[(V_{eq} - V_T)/(nV_t)]$ where V_{eq} is defined in Fig.3.19 and all other variables have their usual meaning. Setting $Q_1 = Q_2$ yields

$$V_{eq} = V_T + nV_t \ln \left(\frac{C_s}{T_{clamp} I_t} V_m \right). \quad (3.10)$$

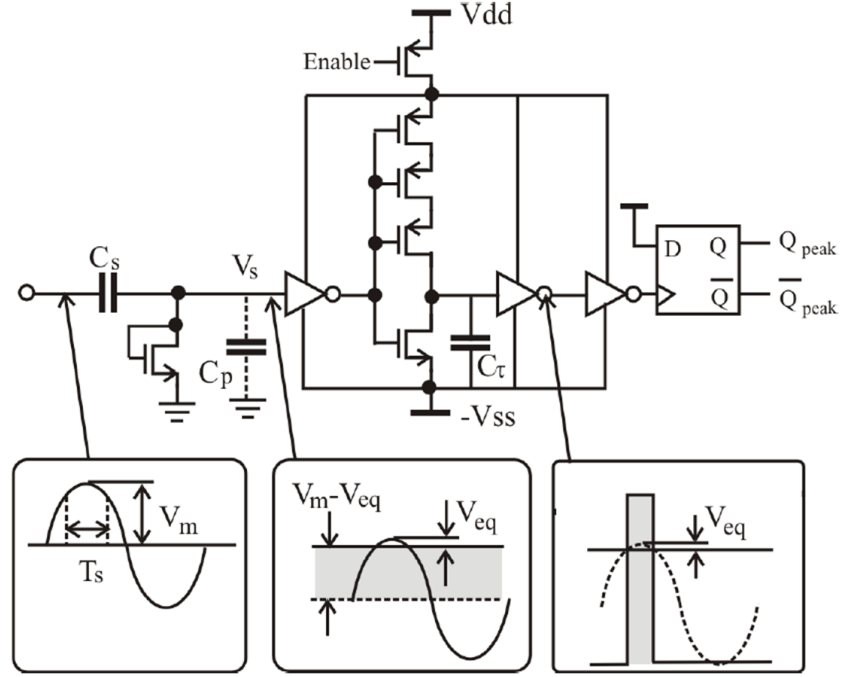


Figure 3.19: Peak detection by negative signal level shift.

To accurately estimate the peak position, V_{eq} needs to be small. A small V_{eq} can be obtained using a zero- V_T MOS transistor. For typical MOS transistors, the logarithmic term in (3.10) is negative, further lowering V_{eq} . V_{eq} can be detected by a series of inverter amplifiers and converted to a digital pulse, as shown in Fig.3.19. The delay block is a simple RC network where R_τ is implemented by a cascade of pMOS transistors in sub-threshold. The rising edge triggers a D-flip-flop, disabling the charge pumps and inverters to minimize power consumption. Note that the threshold voltage of zero- V_T MOS diodes is sensitive to process spread and leakage current. Since the voltage level shifter shifts down the input voltage by $V_m - V_T$, the portion that is above zero voltage is $0 \leq V_T$. If V_T is large, the inverting amplifier will be triggered when $V_{shifted}$ exceeds zero at which the shifted voltage might not be at its peak, giving rise to an error in detection of the location of the peak. Also

note that if the trigger point of the inverting amplifier is higher than V_{eq} due to the process variation, the negative level shifter may not work properly. Since the triggering voltage of the inverting amplifier can be adjusted by varying V_{dd} and V_{ss} , a proper triggering voltage of the inverting amplifier can therefore be set either manually or automatically using a triggering voltage set-up circuitry.

3.5 Measurement Results

The proposed transformer matching network was designed in IBM CMRF8SF 130 nm 1.2 V CMOS technology. Post-layout simulation results are given in Fig.3.21. It is seen varying V_{tune} allows V_{DC} to reach its maximum. A matching impedance is obtained once the input of the transformer is half of the RF input. With a 2.4 GHz 500 mV_{pp} sinusoid input, the voltage of the secondary winding of the transformer is 4 V_{pp}, providing a voltage gain of 8. Since $V_T \approx 0.4$ V, without the transformer, the input voltage would be simply too low to turn on the transistors of the voltage multiplier, resulting in 0% power efficiency of the voltage multiplier. With the transformer, the overdrive voltage is now 1.6 V, resulting in power efficiency 80%. The benefit of employing the step-up transformer overwhelms its loss. The simulated charge pump current is 10 μ A and the negative voltage level shifter consumes 50 nA. The charge pump current can be reduced to save power, however, at the cost of tuning time. The low power consumption of the voltage level shifter is due to the fact that the MOS diode only conducts for a very short period of time when the input voltage exceeds V_T and switches off when C_{clamp} is charged sufficiently.

Fig.3.22 shows the die micrograph of the chip with probes for on-wafer measurement. On-wafer probing was conducted using a Microtech RF-1 probe station with a Farady cage to minimize the effect of the parasitics of packages and external electromagnetic interferences. C_{match} is placed next to the RF input pad. The spiral transformer, charge pumps and tuning varactor are also placed in the immediate proximity. A Microtech DCQ-06 dc probe with six ceramic bladed needles configured as SGSSGS (S=signal and G=ground) were used to supply dc voltages and to probe the output of the voltage multiplier. Two single-ended Microtech ACP-40-D-GSG-150 RF probes and one differential Microtech ACP-40-D-

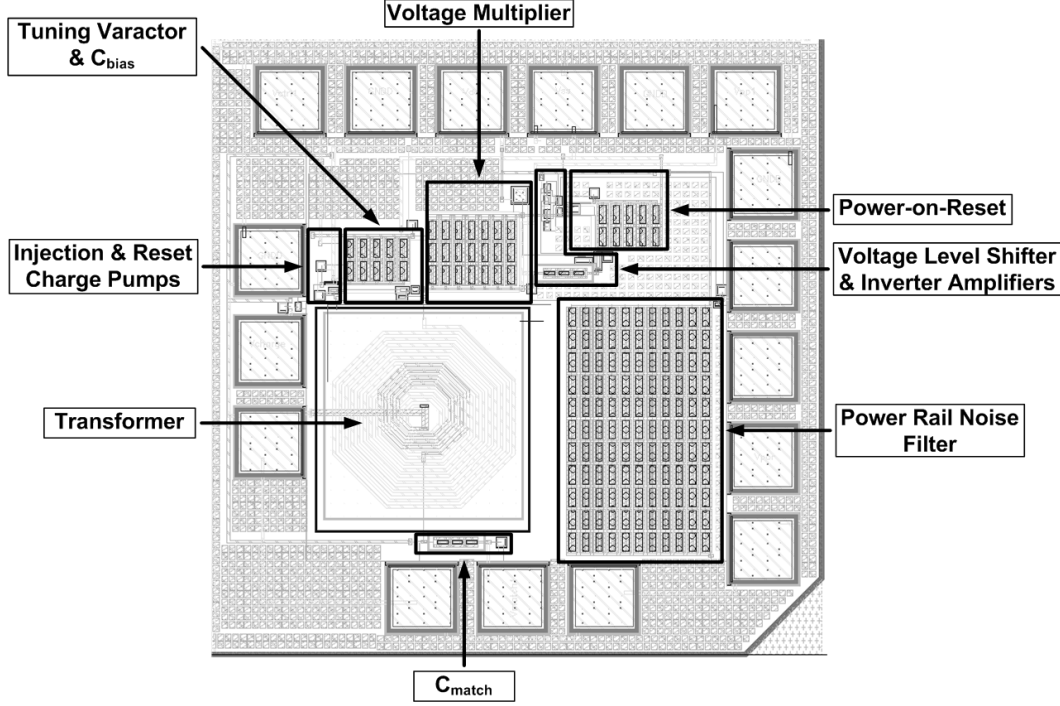


Figure 3.20: Layout of transformer matching network.

GSGSG-150 RF probe were used for clocks and inputs. The loss of cable including connectors was approximately 3 dB at 2.4 GHz and negligible at lower frequencies. The RF input signal was from a Rohde & Schwarz RF signal generator. Clocks were from an Agilent B1130A pattern generator. The waveform of the output was captured using an Agilent MOS-X 3024A oscilloscope. Figs.3.23 and 3.24 show the waveform of V_{tune} and V_{DC} captured from the oscilloscope. It is seen that the peak of V_{DC} can be located by varying V_{tune} . The maximum DC output voltages of the calibrated transformer impedance matching network when loaded with an on-chip voltage multiplier are measured and listed in Table 3.5. Measurement results are shown respectively for an external 10 K Ω and an external 1 M Ω loads at different input frequencies. For an input frequency of 2.4 GHz and an external load of 10 K Ω , the measured maximum DC output voltage is 1.3 V which is equivalent to an output power of $\frac{1.3^2}{10K\Omega} = 169\mu W$. The emulated incident RF signal from the 50- Ω signal generator is of 500 mV_{pp} amplitude such that the incident RF power can be approximated as $\frac{1}{2} \cdot \frac{500mV/2}{50\Omega} = 625\mu W$. Thus, the power efficiency of the proposed transformer impedance matching network can be

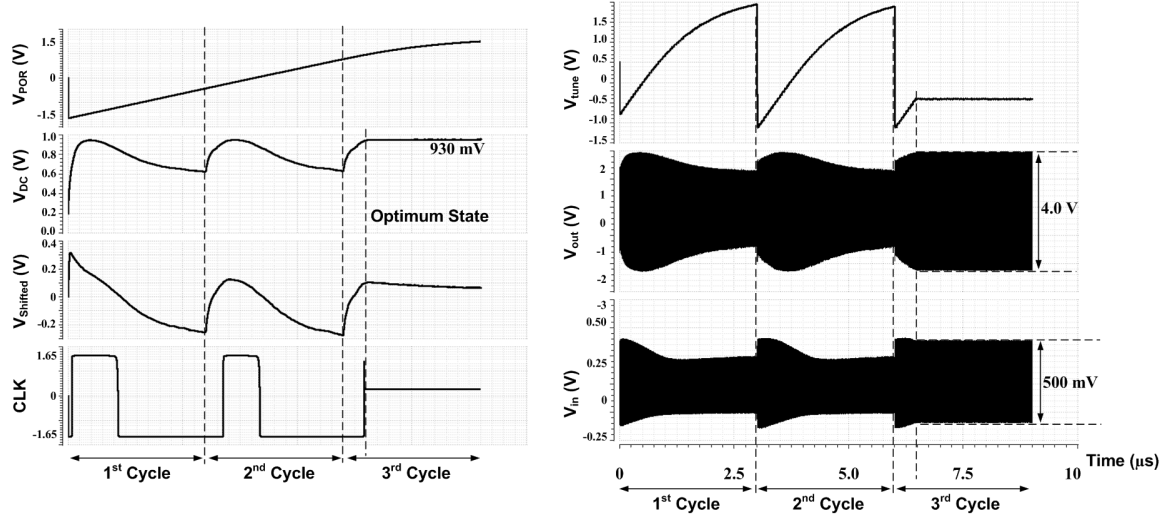


Figure 3.21: Post-layout simulation results. Input : 2.4 GHz 500 mV_{pp} sinusoid input. Injection clock period : 1 MHz. Reset clock period : 1 KHz. POR clock period : 100 Hz. C_{clamp} =5 pF. zero- V_T MOSFET : W/L = 6 μ m / 0.56 μ m. V_{dd} =1.65 V and V_{ss} =-1.65 V. V_{DC} : Output voltage of voltage multiplier. $V_{shifted}$: Output voltage of voltage level shifter. V_{in} : Input voltage of transformer. V_{out} : Output voltage of transformer.

calculated to be $\frac{170\mu W}{625\mu W} = 27.2\%$. Performances of existing impedance matching networks and this work are summarized and compared in Table 3.3.

Table 3.2: Measured maximum output voltage of transformer network.

Freq.	Max. voltage (10 K Ω load)	Max. voltage (1 M Ω load)
2.25 GHz	0.85 V	2.3 V
2.30 GHz	0.96 V	2.6 V
2.35 GHz	1.15 V	2.5 V
2.40 GHz	1.30 V	2.6 V
2.45 GHz	1.20 V	2.6 V
2.50 GHz	1.15 V	2.6 V
2.55 GHz	1.05 V	2.5 V

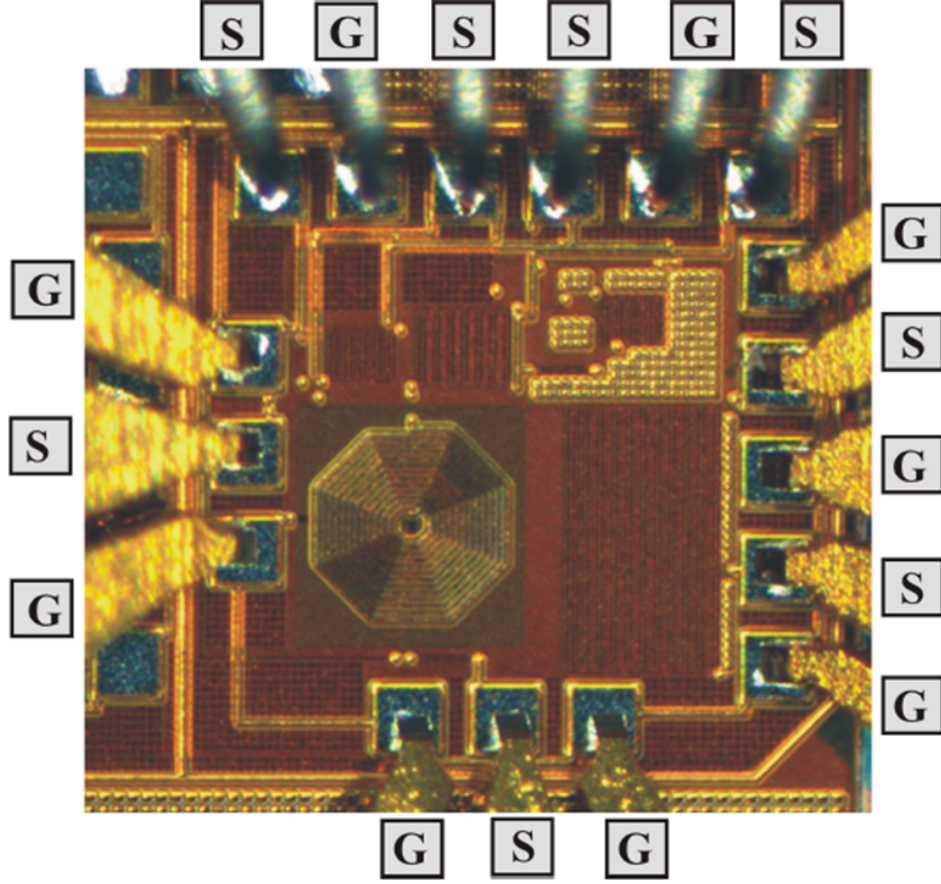


Figure 3.22: Die micrograph of transformer matching network with probes in place for on-wafer measurement.

3.6 Chapter Summary

A calibration technique to maximize RF power harvest with step-up transformers was presented. It was shown that both the input impedance and resonant frequency of the transformer matching network are sensitive to process spread and load variation, and both can be tuned by varying the varactor at the secondary winding of the transformer. A low-power current-tuning technique to tune the varactor and a passive voltage shifter method to find the optimal capacitance of the varactor were proposed. The performance of the proposed design was validated using simulation and on-wafer measurement. Although the proposed calibration technique enables the transformer impedance matching network for larger gain and higher power efficiency, the cost is the real-estate of on-chip transformers. Most current semiconductor foundries do not offer standard inductors including transformers

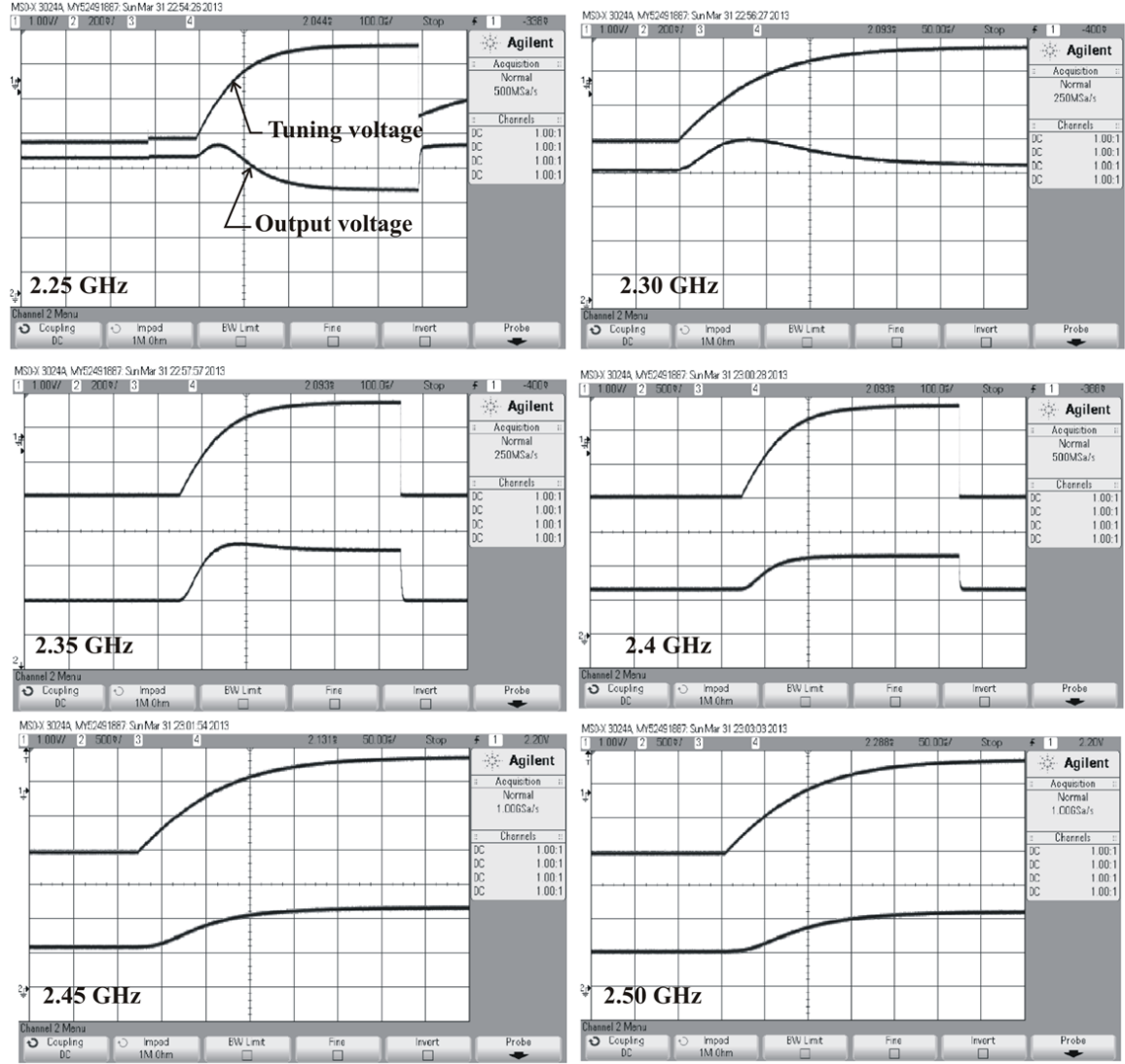


Figure 3.23: Screen capture of tuning voltage V_{tune} and output voltage of voltage multiplier with 10 K Ω load. The maximum voltage gain is 7.35. Due to the limited tuning range of the implemented varactor, the peak of V_{DC} does not change when frequency exceeds 2.4 GHz.

in their process design kits (PDK) such that the calibrated transformer impedance matching network will have to be customized in each individual design.

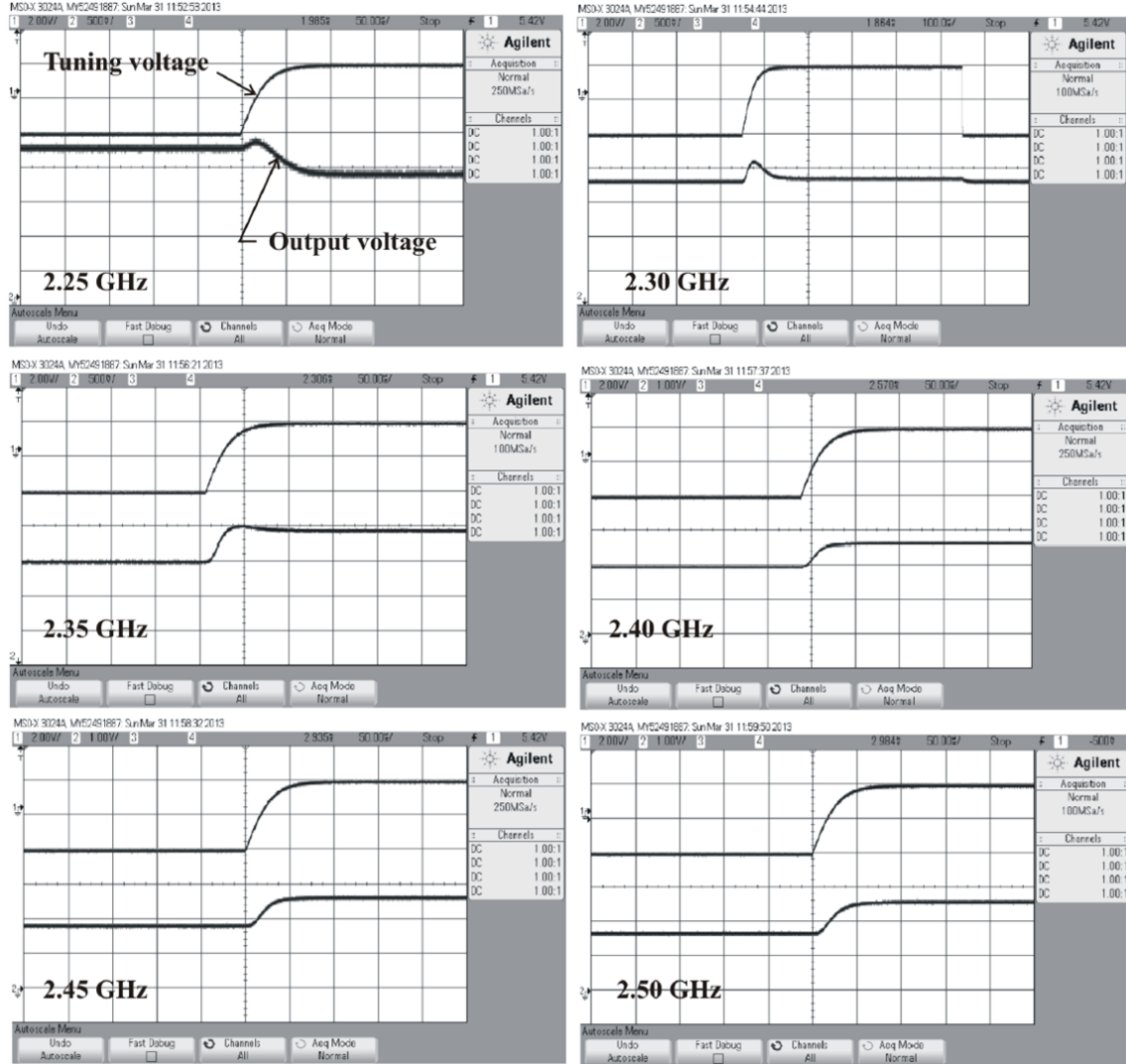


Figure 3.24: Screen capture of tuning voltage V_{tune} and output voltage of voltage multiplier with 1 M Ω load. The maximum voltage gain is 14.7. Due to the limited tuning range of the implemented varactor, the peak of V_{DC} does not change when frequency exceeds 2.4 GHz.

Table 3.3: Comparison of Impedance Matching Networks

Ref.	Tech.	Freq.	S_{11}	Voltage Gain	Power	Efficiency
[10]	0.5 μm SOI	2.45 GHz	-1.54 dB	0.918	1 μW (3.4 K Ω Load)	37%
[17]	0.18 μm CMOS	920 MHz	-12 dB	8 (max.)	2 μW (500 K Ω Load)	5.14%
[38]	130 nm CMOS	180 MHz	n/a	n/a	5.29 μW (1.4 K Ω Load)	0.389%
This Work	130 nm CMOS	2.4 GHz	< -20dB	> 10	170 μW (10 K Ω Load)	27.2%

Chapter 4

Dual-Tank FSK Demodulator

Frequency shift keying (FSK) has recently been applied to wireless passive microsystems such as RFID tags and biomedical implants to replace amplitude shift keying (ASK) for high-speed data transmission [2]. ASK modulators, though they possess the intrinsic advantage of simple configuration consequently low power consumption, suffer from high-order filters with large time constants and sharp cut-off frequencies [40]. Also the fluctuating carrier envelops gives rise to fluctuating rectified power transmission [39]. For high-speed, steady power and data transmission, several FSK demodulation schemes were proposed [40, 41, 42]. One of the most popular designs was introduced in [40], where both an analog FSK demodulator and a digital FSK demodulator were proposed to identify a transmitting bit by measuring the period of each received carrier cycle. In [41], a simple FSK demodulator was implemented using delay circuitries to sample the received FSK signal. The simple delay circuitry results in low-power consumption, but is prone to bit errors due to timing skews. The FSK demodulator proposed in [42] was composed of a multiplexer, a shift register, a phase-frequency detector, and a charge-pump. The complex circuitries achieve faster transmission speed, but results in larger power consumption. Generally, FSK receivers in passive wireless microsystems consist of two major functional blocks: a voltage multiplier for converting received RF energy into DC powers and an FSK demodulator for bit detection. Common benchmark metrics for an FSK receiver are therefore the maximum deliverable power and power conversion efficiency of the voltage multiplier, and data demodulation speed and power consumption of the FSK demodulator.

A common drawback of existing FSK demodulators is the low power efficiency. In order to boost the amplitude of the received RF signal so as to maximize the power efficiency of the passive wireless microsystems, the coupling antenna must have a high quality factor [39]. This, however, gives rise to a low power efficiency when FSK is used. This is because FSK modulates the baseband data using two carriers of greatly distinct frequencies. As a result, both carrier frequencies are not at the resonance frequency of the coupling antenna. A stagger-tuning technique proposed in [43] improves power efficiency by separately tuning the transmitter and receiver tanks at each one of the FSK frequencies. A further improvement of FSK power conversion efficiency was proposed in [40] where a wideband inductive link composed of a serial combination of a parallel and a series LC tanks was employed on the transmitter side to generate dual frequency-response peaks on the receiver side to maximize the amplitude of the received voltage. But the coupling transformer at the receiver side still only resonates at a single frequency, and the resulting power efficiency is rather low.

This chapter proposes a new architecture for low-power FSK demodulation by using dual LC tanks to boost the amplitude of the received signal at two FSK carrier frequencies subsequently the power efficiency. The new architecture is described in Section 4.1. Its contributions to a passive wireless microsystem are depicted in Fig. 4.1. In Section 4.2, a full-wave voltage quadruple voltage multiplier is proposed to produce a dual-polarity supply voltage used by the FSK demodulator. Section 4.3 proposes a digital FSK demodulation scheme which recovers baseband data by evaluating the voltage of the LC tanks at the receiver. A pair of shunting switches is employed to accelerate the energy depletion of the receiving LC tank when the other receiving tank starts to resonate so as to improve the data rate. Simulation and numerical results are presented in Section 4.4. Another FSK demodulator design employing both the dual-tank architecture and the voltage level shifting technique is introduced in Section 4.5. Finally, this chapter is summarized in Section 4.6.

4.1 Architecture of Dual-Tank FSK Demodulator

The configuration of the proposed dual-tank FSK demodulator is shown in Fig.4.2. It consists of a dual-tank analog front-end, a full-wave voltage quadrupler, and a FSK digital

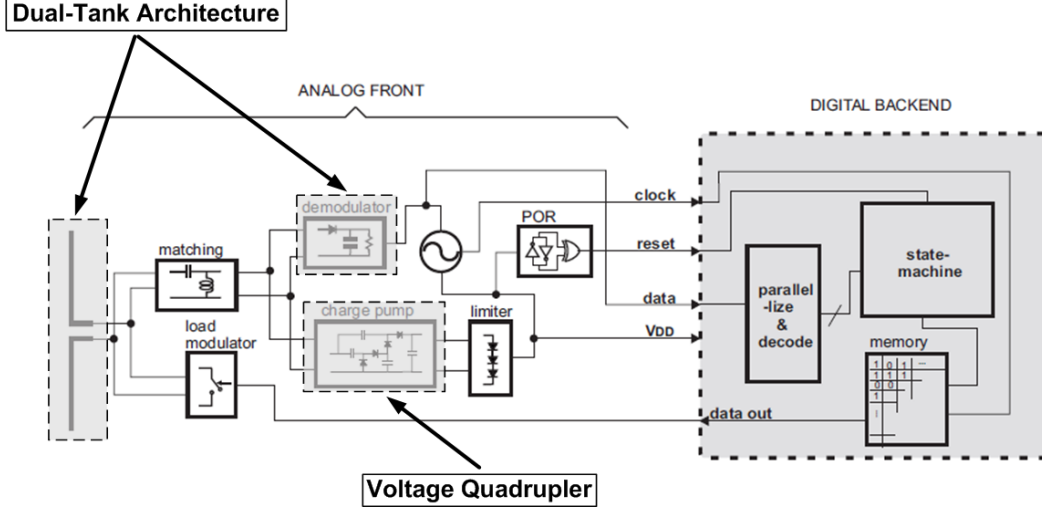


Figure 4.1: Contributions of the proposed dual-tank FSK architecture to a general passive wireless microsystem.

demodulator. The two receiving LC tanks are tuned to the two FSK carrier frequencies so that the voltages across each of the receiving LC tanks are maximized at the carrier frequencies. The full-wave voltage quadrupler rectifies the received FSK-modulated sinusoidal signal and converts it to two dual-polarity voltages V_{dd_high} and V_{dd_low} to be used by the FSK digital demodulator. The FSK digital demodulator performs FSK demodulation and recovers the baseband data.

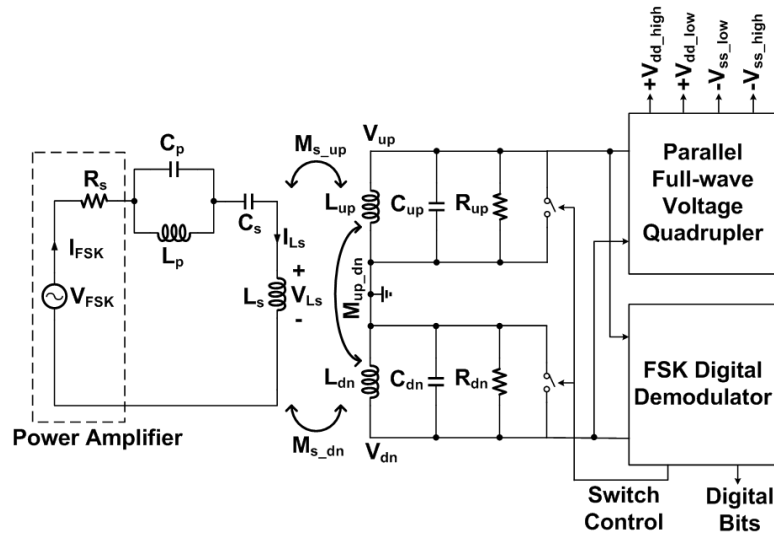


Figure 4.2: Proposed dual-tank FSK demodulator.

To assess the effectiveness of the proposed FSK demodulator, we follow Ghovanloo-Najafi's approach and model the FSK transmitter with a voltage source V_{FSK} of internal resistance R_s , a parallel LC tank $L_P \sim C_P$, and a series LC tank $L_S \sim C_S$. Each LC tank resonates at one of the carrier frequencies [40]. M_{s_up} and M_{s_dn} are the coupling coefficients of the coupling transformer. M_{up_dn} is the coupling coefficient between the two receiving tanks. M_{up_dn} causes the shift of the resonance frequencies of the tanks and should be minimized. M_{up_dn} can be largely eliminated by stacking the two planar spiral inductors with an offset [50]. Fig.4.3 plots the normalized frequency response of the proposed dual-tank front-end. It is seen that the current I_{L_s} and power P_{L_s} of the series inductor at the transmitter peak at the carrier frequencies. Also observed is that the voltage of the receiving tanks also peaks at the carrier frequencies.

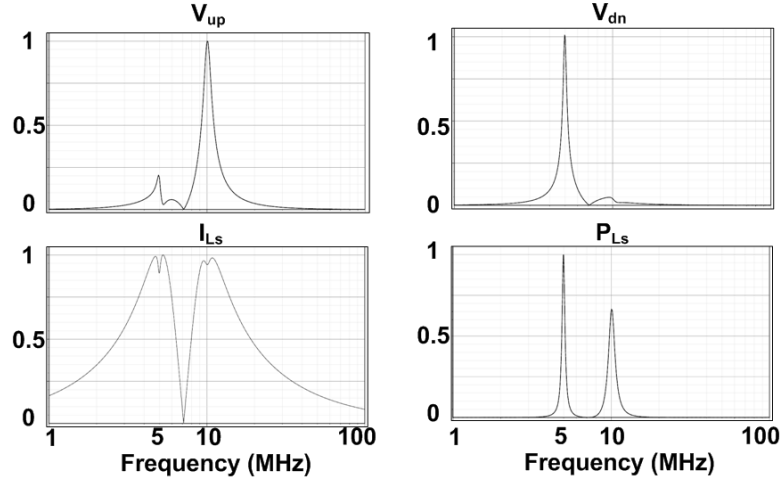


Figure 4.3: Normalized frequency and power responses of dual-tank analog front-end. I_{L_s} and P_{L_s} are the current and power of the transmitter series inductor L_s . FSK carrier frequencies: $f_{low} = 5$ MHz and $f_{high} = 10$ MHz.

4.2 RF-to-DC Power Conversion and Voltage Multiplication

Passive wireless microsystems use voltage multipliers to perform RF-to-DC conversion. A conventional half-wave voltage doubler is shown in Fig.4.4 where the voltage clamper and half-wave voltage rectifier are implemented with a pair of diodes and capacitors respectively. In standard CMOS processes, diode-connected NFETs are commonly used for positive voltage conversion. For negative voltage conversion, diode-connected NFETs, however, might cause a large substrate leakage current because V_{clamp} is largely shifted to the negative region, resulting in a forward-biased substrate. To reduce the substrate leakage, silicon-on-insulator (SOI) devices were used [10, 33]. In this chapter, we propose a simple and yet effective alternative by applying diode-connected PFETs to choke the substrate leakage current, as shown in Fig.4.5. Because the substrate of PFETs is connected to $+V_{dd}$, a negative V_{clamp} will strengthen the reverse biasing of the substrate PN-junctions, subsequently reduce the substrate leakage current significantly and improve power efficiency.

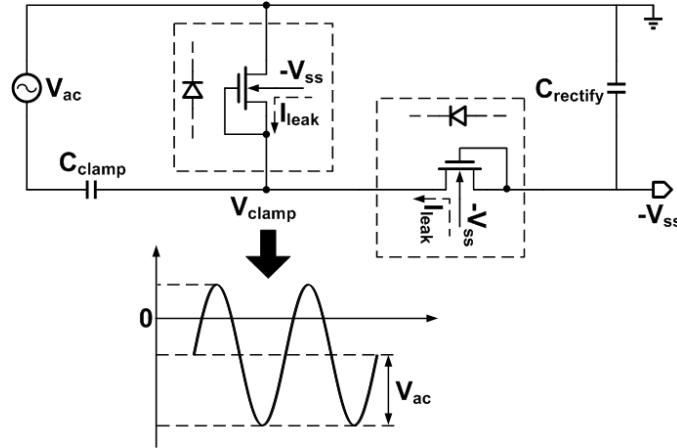


Figure 4.4: Conventional NFET half-wave voltage doubler.

Fig.4.6 shows the proposed full-wave voltage quadrupler. The positive and negative DC voltage rectification is realized by stacking an NFET positive-voltage half-wave voltage doubler and a PFET negative-voltage half-wave voltage doubler. The capacitors are shared

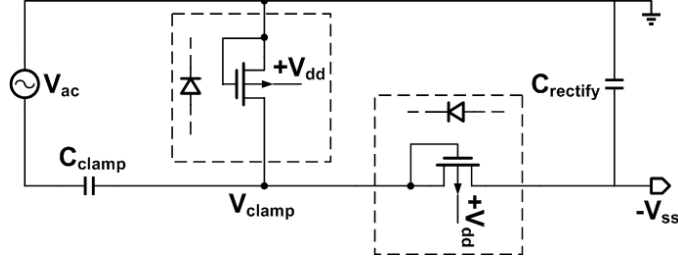


Figure 4.5: Proposed PFET half-wave voltage doubler.

and connected in series to form a voltage divider that generates $+V_{dd_high}$ and $-V_{ss_high}$, $+V_{dd_low}$ and $-V_{ss_low}$ for the digital FSK demodulator. A key advantage of dual-tank architecture is that there is always a tank resonating at one of the carrier frequencies, RF/DC power conversion is therefore continuous. This differs fundamentally from ASK-based power harvesters whose power fluctuates with the amplitude of the data. More importantly, since both receiving tanks are tuned to the carrier frequencies, the drawback of the low power efficiency of FSK demodulators with a single coupling transformer is also removed.

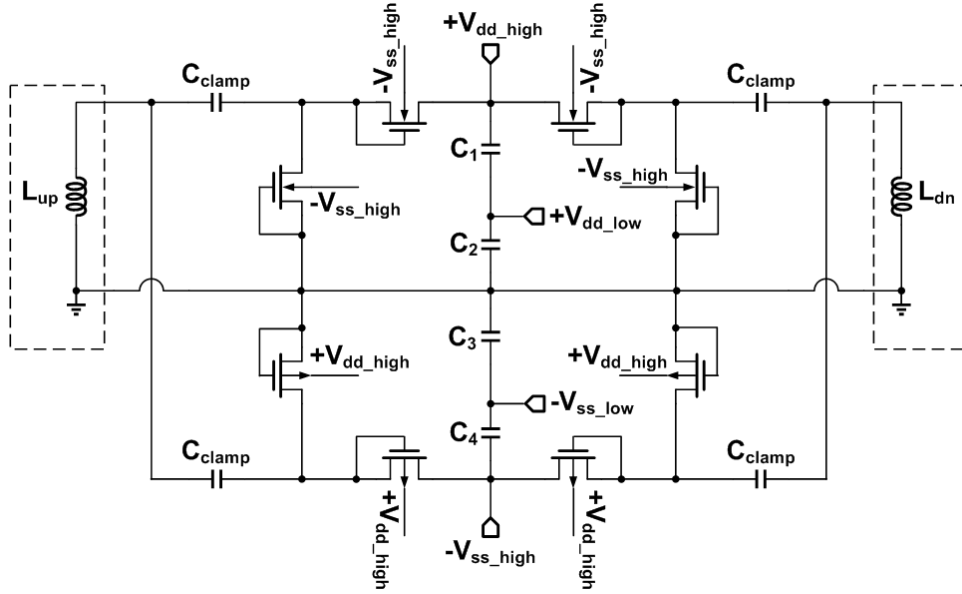


Figure 4.6: Proposed full-wave voltage quadrupler.

4.3 Digital FSK Demodulation

Fig.4.7 shows the configuration of the proposed dual-tank FSK demodulator. Since a one-to-one mapping between the voltage of the receiving LC tanks and the transmitted data exists, at a given time, the voltage of one of the receiving LC tanks peaks while that of the other dips. This suggests that data can be recovered by comparing the tank voltage of the receiving tanks with a preset threshold. In this work, the threshold voltage of a static CMOS inverter is used as the threshold. Digital control pulses, Q_{up} and Q_{dn} , are generated at the output of the D-Flipflop (DFF) following the static CMOS inverter and used to control the shunting switches of the receiving tanks. Shunting the resonating LC tank when the other tank is about to resonate will rapidly deplete the charge of the tank, speeding up the discharge process of the tank subsequently increasing the data rate. The pulse width of Q_{up} and Q_{dn} is set by a dual-time-constant delay cell shown in Fig.4.8. The delay cell with its charge and discharge time constants given by $t_c = R_{pmos}C_{delay}$ and $t_{dc} = (R + R_{nmos})C_{delay}$ where R_{pmos} and R_{nmos} are the on-resistance of NMOS and PMOS, respectively. The charging and discharging processes are shown in Fig.4.8 with t_{dc} and t_c the charge time and discharge time of the capacitor, respectively. The discharge process determines the width of Q_{up} and Q_{dn} when the capacitor discharges its voltage from the initial $+V_{dd}$ to the threshold voltage of the next CMOS inverter, $V_{th_Inverter}$. A resistor R is inserted to slow down the discharging process such that Q_{up} and Q_{dn} are long enough to drain the tank. The charging process is made faster in order to restore the capacitor to its initial voltage, $+V_{dd}$. At the end of Q_{up} and Q_{dn} pulses the channel detecting the bit will be disabled while the other channel is enabled by resetting the DFFs and the channel selection gates located before and after the dual-time-constant delay cell. In order to avoid time competition between resetting the DFFs and enabling channels through *Enable_Up* and *Enable_Dn*, a delay cell is inserted in each of the channels to displace the resetting signals and the channel enabling signals for a small time such that only one channel is active at a time.

The input voltage of the FSK demodulator could be larger than the voltage of the substrate of digital switches with a single $+V_{dd_low}$ power supply and result in a large leakage current. To prevent this from occurring, a CMOS complementary switch implemented in 3.3 V devices is employed, as shown in Fig.4.9.

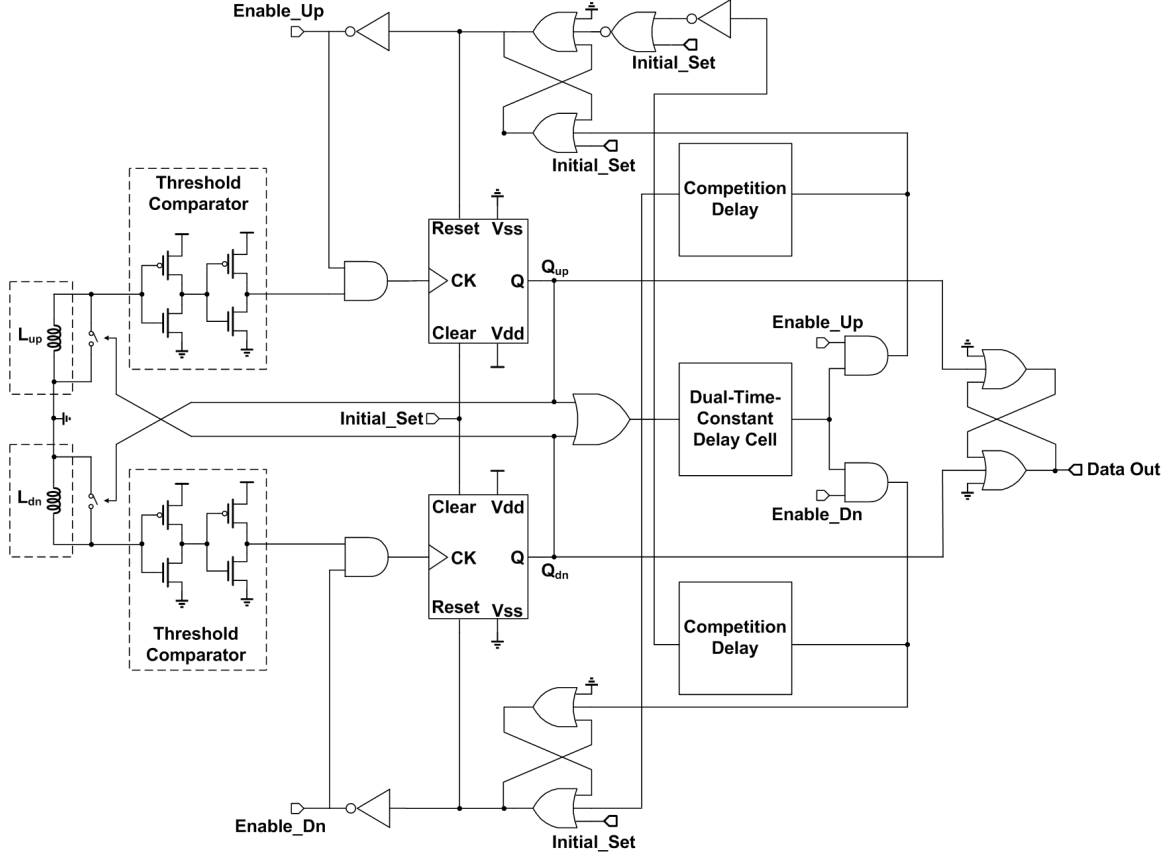


Figure 4.7: FSK demodulator designed for the proposed dual-tank architecture.

The substrate of the switch is connected to higher voltages $+V_{dd_high}$ and $-V_{ss_high}$ to minimize substrate leakage. In addition, the PFET resides in an n-well and the NFET is placed in a p-well such that the substrate of the switches is isolated from that of the digital FSK demodulation circuitry. Because the complimentary switch requires large dual-polarity voltages, the single-ended output of the FSK demodulator $0 \sim +V_{dd_low}$ needs to be converted to $-V_{ss_high} \sim +V_{dd_high}$. In order to convert $0 \sim +V_{dd_low}$ to $-V_{ss_high} \sim +V_{dd_high}$, a simple low-power voltage level shifter and a dual-supply step-up inverter amplifier show in Fig.4.10 are proposed in this work.

When $V_{in} = +V_{dd_low}$, the diode-connected PFETs are forward-biased and the capacitor is charged by the forward-biasing current such that $V_{out} = N \cdot V_{diode}$ where V_{diode} is the voltage drop of each of the PFETs. Though negatively shifted, V_{out} is still positive and forces the PFETs into subthreshold. V_{out} continues to drop because of the small subthreshold leak-

still forward-biased because of the voltage stored on the capacitor. The small compensation current discharges the capacitor slightly and produces a small upward slope at the bottom of V_{out} , which boosts V_{out} in the next cycle when the leakage current restores. The leakage current and the compensation current are only a few nAs. The overall power consumption is therefore negligible.

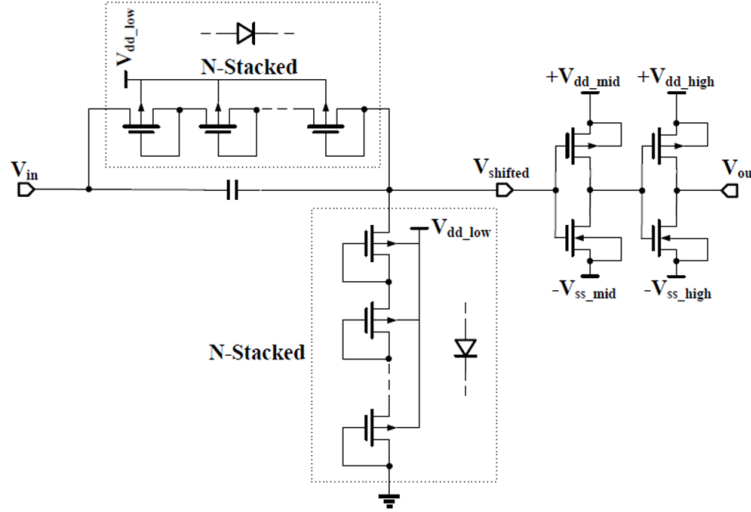


Figure 4.10: Low-power voltage shifter and dual-supply step-up inverter amplifier.

To interface the small output swing of the voltage level shifter with large analog I/Os, a dual-supply step-up inverter amplifier is used at the output of the voltage level shifter. The amplifier is composed of a pair of cascaded CMOS inverters with step-up supply voltages such that the input to the previous inverter stage is boosted at the output to exceed the current-transition region of the next inverter stage. With this arrangement, there is no static current in both inverters and their power consumption is minimized. The intermediate supply voltages can be conveniently obtained by capacitor-voltage dividers in power harvesting circuitry.

4.4 Numerical Results

A test circuit designed in IBM 130 nm CMOS technology, as shown in Fig.4.11, is used to verify the effectiveness of the proposed design. The simulated output voltages of $+V_{dd}$ and $-V_{ss}$, and the average substrate leakage currents for clamping and rectifying diodes of I_{leak1} and I_{leak2} in the steady state are tabulated in Table 4.1. The leakage current reduction is evident. The substrate leakage current is shown in the figure. Its periodicity due to switching is evident.

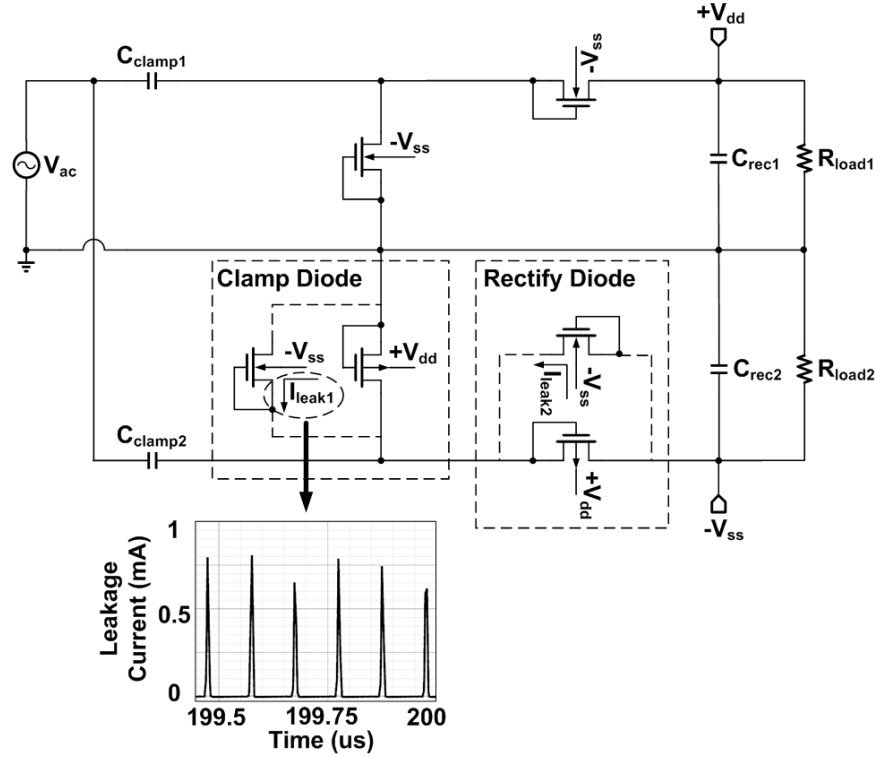


Figure 4.11: Half-wave voltage doubler implemented in PFETs and NFETs. Circuit parameters: $V_{ac}=4$ V, $C_{clamp1} = C_{clamp2} = 10$ nF, $C_{rec1} = C_{rec2} = 10$ nF and $R_{load1} = R_{load2} = 10$ K Ω , $(W/L)_{NFET} = 20:1$ and $(W/L)_{PFET} = 50:1$.

To compare the power efficiency of the proposed parallel full-wave voltage quadrupler with that of single-tank full-wave voltage quadrupler, two test circuits shown in Fig.4.12 are analyzed. The power efficiency is defined as

Table 4.1: Comparison of Half-Wave Voltage Doublers.

	NFET Diodes	PFET Diodes
$+V_{dd}$	+1.50 V	+1.50 V
$-V_{ss}$	-1.80 V	-1.47 V
Average leakage current of I_{leak1}	44 μ A	25 nA
Average leakage current of I_{leak2}	37 μ A	30 nA

$$\begin{aligned}
\eta &= \frac{\text{DC Output Power}}{\text{Average FSK Source Power}} = \frac{P_{+V_{dd}} + P_{-V_{ss}}}{P_{FSK}} \\
&= \frac{V_{dd}^2/R_L + V_{ss}^2/R_L}{\frac{1}{t_2-t_1} \int_{t_1}^{t_2} v_{FSK}(t) \cdot i_{FSK}(t) dt} \quad (4.1)
\end{aligned}$$

where $P_{+V_{dd}}$ and $P_{-V_{ss}}$ are the DC powers delivered to the load R_L . The power efficiency of both circuits is compared in Table 4.2. To achieve comparable DC output power, the single-tank configuration needs to have a larger V_{FSK} as compared with that of the dual-tank counterpart. As a result, the power efficiency of the single-tank receiver is lower as compared with that of the dual-tank receiver.

Fig.4.13 shows the waveforms of the dual-tank FSK demodulator. The time intervals for fast tank energy depletion are marked by the arrows. For a data transmission rate of 2 Mb/s, the FSK demodulator consumes 39 μ W with the lower power supplies, $+V_{dd,low}$ and $-V_{ss,low}$, providing an average power of around 28 μ W (72%) and the higher power supplies, $+V_{dd,high}$ and $-V_{ss,high}$, providing an average power of around 11 μ W(28%).

4.5 FSK Demodulation by Voltage Level Shift

It is not unusual that passive microsystems equip with dual-polarity power supplies for common configurations of full-wave voltage multipliers. In such systems, the dual-tank architecture proposed in Fig.4.2 needs to be modified appropriately since the inverter comparison threshold drops to ground level and the resonating and non-resonating tanks could both trigger the inverter outputs at the same time. Another scenario is when the transmitting FSK signal is strong, extra circuitries to prevent both tank oscillating voltages from

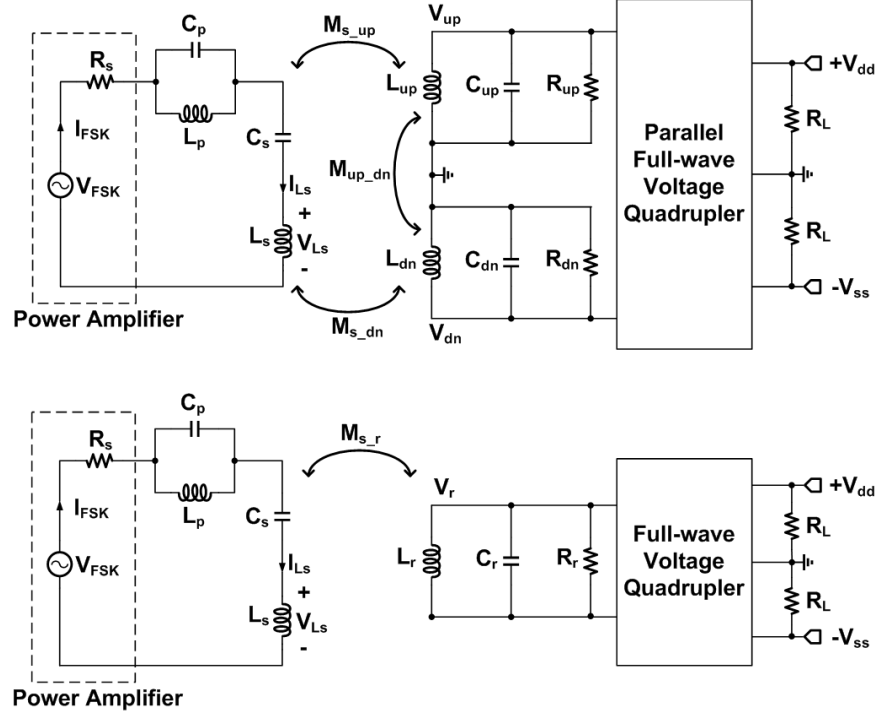


Figure 4.12: Top - Dual-tank full-wave voltage quadrupler. Bottom - Single-tank full-wave voltage quadrupler. Circuit parameters: $f_{low}=5$ MHz, $f_{high}=10$ MHz, $M_{s_up}=0.1$, $M_{s_dn}=0.1$, $M_{up_dn}=0.1$, $L_P=500$ nH, $C_P=1$ nF, $L_s=1$ μ H, $C_s=500$ pF, $L_{up}=2.5$ μ H, $C_{up}=101$ pF, $R_{up}=1.5$ K Ω , $L_{dn}=2.5$ μ H, $C_{dn}=404$ pF, $R_{dn}=2$ K Ω , $M_{s_r}=0.1$, $L_r=2.5$ μ H, $C_r=404$ pF, $R_r=2$ K Ω , and $R_L=10$ K Ω .

exceeding the inverter thresholds simultaneously are needed. A simple remedy to the above problems is to apply a voltage level shifter proposed in Chapter 2 to shift the tank oscillating voltages away from the comparison threshold. The voltage level shifter remembers the maximum amplitude of the input signal's envelop and shifts both tank voltages away for a distance proportional to their peak amplitudes. The shifted tank voltages only have a portion of the signal above or below the ground level and only a branch of the inverters can be triggered at a time.

The modified dual-tank architecture with passive voltage level shifters is shown in Fig.4.14. The upper 10 MHz tank employs a positive voltage level shifter and the lower 5 MHz tank employs a negative voltage level shifter. The 10 MHz resonating voltage is shifted upward and the 5 MHz resonating voltage is shifted downward such that their respective

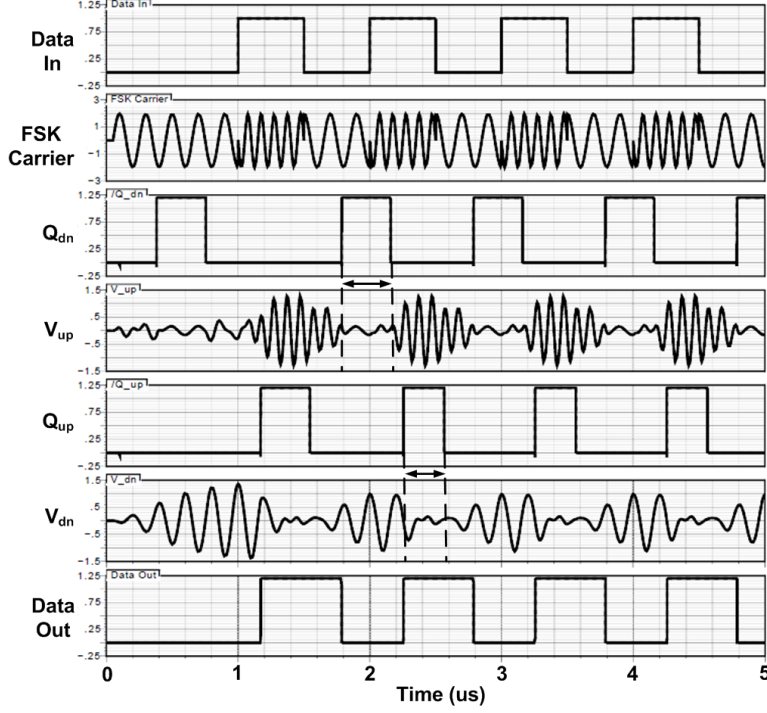


Figure 4.13: Simulated waveforms of dual-tank FSK demodulator.

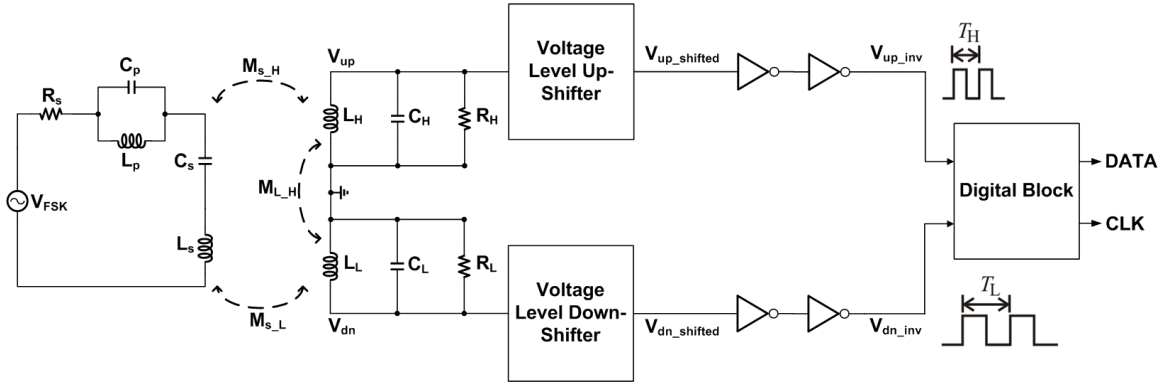


Figure 4.14: Dual-tank FSK demodulation utilizing voltage level shifters.

bottom and top portions are not overlapped together. The transmitting bit can subsequently be detected by the inverter series.

A testbench of Fig.4.14 is simulated in IBM 130-nm CMRF8SF technology with the identical environmental setups in Fig.4.12. Both the up-shifting and down-shifting voltage level shifters are composed of 3-stage cascaded voltage level shifters proposed in Section 2.3.1

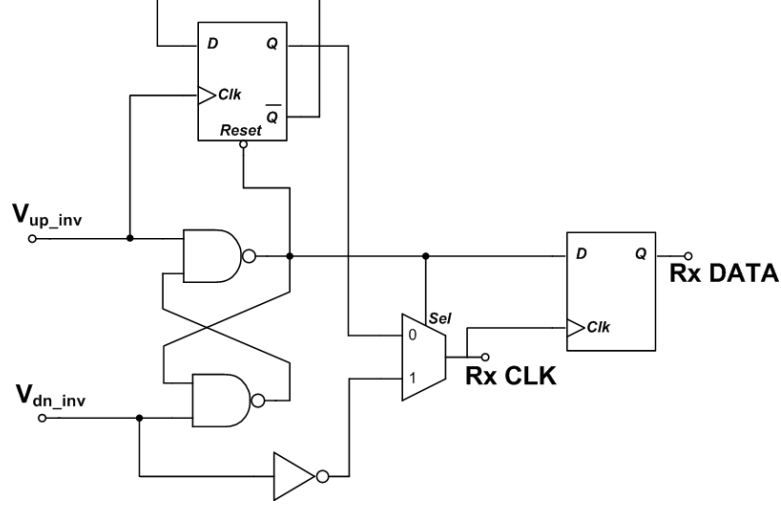


Figure 4.15: Logic circuit implementation of the digital block in Fig.4.14.

with the number of clamping and compensation diodes as $N_1 = M_1 = 3$ and $N_2 = M_2 = N_3 = M_3 = 1$. The clamping capacitors are chosen to be $C_1 = C_2 = C_3 = 500$ fF and the clamping and compensation MOSFET diodes are with uniform sizes of $W/L = 0.5 \mu\text{m} / 0.4 \mu\text{m}$. The 1st stage provides a shifting level of 50% of the tank's peak envelop; the 2nd stage provides an additional 25% shifting level; and the 3rd stage contributes the last 12.5% shifting level. So the shifted tank voltages just remain around 12.5% of its top or bottom portions exceeding the ground level. The input data is a 5 Mbps NRZ bit stream. FSK carrier frequencies are $f_H=10$ MHz and $f_L=5$ MHz. The digital block is implemented in Fig.4.15 where the RS latch is alternatively set and reset by the detected 10 MHz and 5 MHz FSK pulse streams from the upper and lower branches of inverters. The top D-flip-flop divides the upper 10 MHz digital pulses by 2 to be a 5 MHz digital signal. A recovered clock can be extracted from the upper and lower 5 MHz signals by a 2-to-1 multiplexer. And the final receiving bits are demodulated by using the extracted clock to sample the RS latch output.

The simulation results of the FSK demodulator are given in Fig.4.16. It is seen that the demodulated data are slightly skewed from the original data due to the dual tank hysteresis. This hysteresis can be remedied by extracting the correct timing of the digital clocks for synchronization. The power consumption of the voltage level shifters is 151 nW

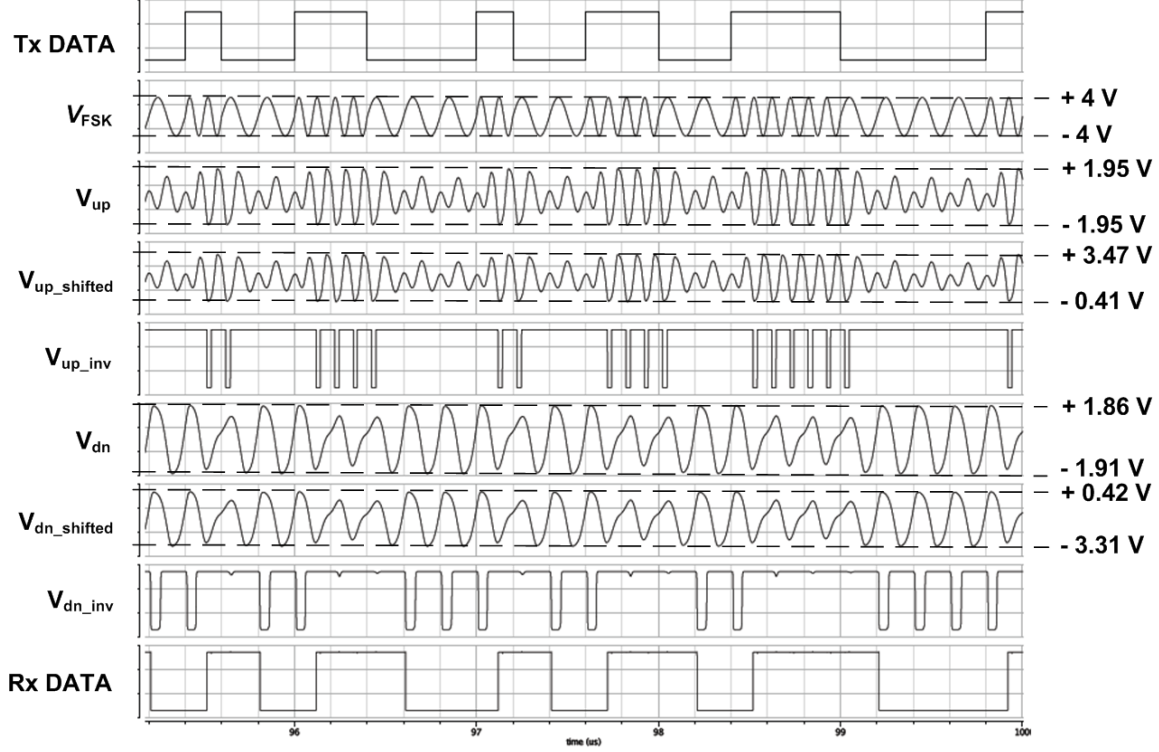


Figure 4.16: Response of FSK demodulation utilizing voltage level shifters.

Table 4.2: Comparison of Power Efficiency.

	Singe-Tank Receiver [6]	Dual-Tank Receiver (This Work)
T_x Resonant Freq.	f_L and f_H Dual Peaks	f_L and f_H Dual Peaks
R_x Resonant Freq.	Single Peak $\sqrt{f_L \cdot f_H}$	f_L and f_H Dual Peaks
T_x Power (P_{FSK})	2.056 W	75.66 mW
T_x Voltage (V_{FSK})	30 V _{pp}	6 V _{pp}
R_x Positive Power ($P_{+V_{dd}}$)	0.231 mW	0.213 mW
R_x Negative Power ($P_{-V_{ss}}$)	0.250 mW	0.292 mW
Power Efficiency	0.0234 %	0.667 %

each. With digital circuitries for bit detection, data recovery and clock synchronization, the total power consumption is 23 μ W. Carrier frequencies, data rates and power consumptions of the all-digital FSK demodulator proposed in Section 4.3 and this voltage shifting FSK demodulator are compared with other existing architectures in Table 4.3.

Table 4.3: Comparison of Performances of Published FSK Demodulators for Passive Microsystems and This Work

Ref.	Tech.	Carrier	Data Rate	Power
Ghovanloo & Najafi [40]	1.5 μm	5/10 MHz	2.5 Mbps	0.38 mW
Weng <i>et al.</i> [51]	0.18 μm	5/10 MHz	5.0 Mbps	0.22 mW
Hwang & Lin [42]	0.35 μm	6.78/13.56 MHz	1.0 Mbps	0.96 mW
All Digital FSK Demodulator (This Work)	0.13 μm	5/10 MHz	3.0 Mbps	0.039 mW
Voltage Shifting FSK Demodulator (This Work)	0.13 μm	5/10 MHz	5.0 Mbps	0.023 mW

4.6 Chapter Summary

In this chapter, a dual-tank architecture for low-power FSK demodulation was proposed. An all-digital FSK demodulator and a voltage-shifting FSK demodulator that utilize the proposed dual-tank architecture were also proposed. The FSK demodulators recover baseband data by evaluating the voltages of the dual receiving tanks and a fast depletion of the receiving tanks subsequently a high data rate is accomplished by employing two shunting switches. A full-wave voltage quadrupler for efficient RF-to-DC power conversion was also introduced. A dual-supply inverter amplifier was presented to provide appropriate control voltages for the shunting switches in order to minimize their substrate leakage currents. Simulation results demonstrated that the power efficiency of the proposed dual-tank voltage multiplier is approximately 30 times that of its single-tank counterpart. The proposed all-digital and voltage-shifting FSK demodulators can respectively achieve a data rate of 3 Mbps and 5 Mbps with 5 MHz/10 MHz carriers while consuming only a few tens of μW . Despite the significant performance improvements applying the dual-tank architecture in FSK receivers, the cost is an extra receiving inductor which results in larger real-estate in passive wireless microsystems.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

Passive voltage level shifters were presented and their applications in passive wireless microsystems were explored. The proposed voltage shifters shift the median value of an analogue signal by a multiple or a fraction of the amplitude of the signal in either positive or negative directions. The proposed voltage shifters are powered by the input signal, making them particularly attractive for applications where power is critical. The simple configuration of the voltage shifters also makes them well suited for high-frequency applications. Extensive simulation has confirmed that the performance of the voltage shifters is insensitive to process spread and temperature variation. The voltage shifters with native MOS diodes function properly even when the input drops to 100 mV. The voltage level shifters were designed in IBM 130 nm CMRF8SF CMOS technology. Layout diagrams and a wafer micrograph were provided. Measurement results of the voltage shifting levels agree well with theoretical values[32, 49, 52, 53].

A calibration technique to maximize the power harvest of passive wireless microsystems with step-up transformers was proposed. We showed that both the impedance and resonant frequency of the transformer matching network are sensitive to process spread and load variation such that calibration is much needed. The calibration is feasible by tuning a shunt varactor at the secondary winding of the transformer to maximize power transfer from the antenna to the transformer and power efficiency of the voltage multiplier. A low power current-mode tuning technique and a maximum peak amplitude detection technique

to allocate the optimal tuning capacitance at which the maximum power harvest exists were introduced. The proposed transformer matching network was designed in IBM CMRF8SF 130 nm 1.2 V CMOS technology and its performance was validated using both simulation and on-wafer measurement results [54, 55, 56].

A dual-tank architecture for FSK demodulation of passive wireless microsystems was proposed. The dual tanks alternate to receive wireless power continuously. The dual-tank architecture was utilized in a full-wave voltage quadrupler, an all-digital FSK demodulator and a voltage-shifting FSK demodulator. The full-wave voltage quadrupler significantly improves the power conversion efficiency. The all-digital and voltage-shifting FSK demodulators achieve high data transmission rates with the minimum power consumption. The proposed dual-tank designs were simulated in IBM 130 nm 1.2 V CMOS technology and analyzed with BSIMv4.4 device models. Simulation results showed that the full-wave voltage quadrupler attained a much higher power conversion efficiency than that of a single-tank FSK counterpart. The all-digital and voltage-shifting FSK demodulators achieved high-speed data rates with an efficient data-rate-to-carrier-frequency ratio while consuming powers less than a few tens of μW [57].

5.2 Future Work

Many possible extensions and applications could be further explored for the proposed new design techniques in passive wireless microsystems.

The proposed voltage level shifters are constructed on clamper-rectifier architectures, which are completely distinct from the traditional latched-based voltage level shifters. Due to its novelty, many possible modifications and applications could be explored in the future. Although the proposed voltage level shifters are powered by input signals, their shifting ability is limited to AC input signals. AC input signals are required for the charging and discharging processes of the clampers and rectifiers. If the input signal could be of a single polarity such as being DC biased, the improvement could be significant and more of its applications could be found. Another possible exploration is to apply the proposed voltage level shifters to pre-emphasis modules in high-speed digital communications. Since digital

pre-emphasis in wireline communications, in principle, is to superimpose the transmitting digital bits with their own delayed and weighted copies. If a deft mechanism could be developed such that the weighting functions could be arithmetically summed by the proposed voltage level shifters, a new type of high-speed, power-efficient pre-emphasis circuits could be of significant industrial applications. During the on-wafer measurements of the proposed voltage level shifter, the fabricated chip only operated in lower frequencies due to some faulty digital buffer layouts which caused the buffers to ring in higher frequencies. It is probably that the buffer transistors are over-sized, which caused substrate coupling or power-rail latch-ups. It is worth that future students investigate such layout faults to provide better understanding of occasions to apply the proposed voltage level shifters.

With regard to the calibration technique for transformer impedance matching networks, the on-wafer measurements were carried with external power sources. The external sources proved to be essential in the initial validation of the concepts for the simplicity of the layout and the reliability of testing environments. A future improvement could be the fabrication of on-chip voltage multipliers to supply the calibration circuitries with internal power sources. Such improvement could directly put forth the proposed calibration technique to commercial applications.

The proposed dual-tank FSK demodulator were originally intended for biomedical implants such that its operating frequencies are limited to tens of MHz. The lower carrier frequencies are required for the easy penetration of human skin and muscles, but impose difficulty on submicron fabrication due to the oversize inductors in the millimeter range. In the dissertation, only simulation results were provided. An possible extension of the dual-tank architecture is for RFIDs in UHF bands of 433MHz and 900MHz. The two UHF frequencies are on ISM regulated bands and the dual tanks could be efficiently activated due to the distantly spaced frequencies. For the higher resonant frequencies, inductors could be designed and fabricated on-chip, which could therefore lead to dual-tank FSK RFID systems.

Finally, during the study of my Ph.D., a few other techniques have been developed for mobile wireless communications. They include a PLL-based high-precision dual-mode cascaded-loop frequency synthesizer [58] and a low-power subthreshold Gilbert mixer [59]. Their applications to the passive wireless microsystems could be explored in the future.

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