A NEW PHASE-LOCKED LOOP WITH ACTIVE INDUCTOR RING OSCILLATOR

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Abstract

Many of today's applications require that a phase-locked loop (PLL) operate at high speeds, while maintaining reasonable phase noise and jitter performance. Voltage-controlled oscillators (VCO) are important building blocks in PLLs. More importantly, the VCO is the major contributor of phase noise in a PLL. The noisy environment, mainly due to the switching noise generated by the digital portion of these systems, imposes stringent constraints on the design of VCOs, especially phase noise or timing jitter. The switching noise originated in the digital portion of the systems are coupled to the supply and ground rails of the VCO of PLLs. Another important block of a PLL is the charge-pump, a block that is responsible for generating the control voltage to be applied to the VCO. The stability or fluctuation of the control voltage, can severely affect the phase noise performance of the VCO.

The research in this thesis, centered on (i) the design considerations of CMOS charge-pumps, (ii) the timing jitter of the delay-cells of low-voltage CMOS ring-VCOs, and (iii) the design of a high-speed ring oscillator.

A PLL was designed using a new active inductor 6.3-GHz ring oscillator, with a tuning range of $\pm 15\%$ was designed in 0.18μm CMOS technology. The ring oscillator employed active inductor loads that resulted in an improvement of about 42% in oscillation frequency when compared to the conventional resistor loaded ring oscillator.

Acknowledgment

I would like to thank first and foremost, my advisor Dr. Fei Yuan, for his support, guidance, and constant stream of fresh ideas through out my research made this work possible. I profoundly appreciate his enthusiasm and close interaction that inspires my exploration of integrated circuits. Moreover, I feel privileged to have had the freedom he has given me while conducting my research.

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Special thanks go to Oksana Evseeva for her gracious support and countless sacrifices that have allowed me to complete this work.

Dedication

I dedicate this work to my parents Khodre and Fairouz El-Hage for the support and endless encouragement they have given me.

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Chapter 1

Introduction

1.1 Motivation

Phase locked loops (PLLs) are used in almost every communication system. Some of their uses include recovering clock and data signals, performing frequency-phase modulation and demodulation and recovering the carrier from satellite transmission signals and frequency synthesis.

The demand for high speed, wide bandwidth communication systems has led to advancements in both wireless and fiber-optic systems. To ensure economic viability, the entire semiconductor industry has been pushing for the implementation of a low-cost, low power, high-speed fully integrated receiver-on-chip.

To achieve the goal of a fully integrated receiver on-chip, where analog and digital blocks co-exist on the same substrate, the PLL has to operate at high speeds, while maintaining reasonable phase noise and jitter performance. Voltage-controlled oscillators (VCOs) are important building blocks of PLLs. More importantly, the VCO is the major contributor of phase noise of PLLs. Another important block of a PLL is the charge-pump, a block that is responsible for generating the control voltage to be applied to the VCO. The stability or fluctuation of the control voltage, can severely affect the phase noise performance of the VCO. In addition, the noisy environment, mainly due to the switching noise generated by

the digital portion of these systems, imposes stringent constraints on the design of VCOs, especially on phase noise or timing jitter. The switching noise originated in the digital portion of the systems is coupled to the supply and ground rails of the VCO of PLLs.

The research of this thesis, is centered on (i) the design considerations of CMOS charge-pumps, (ii) the timing jitter of the delay-cells of low-voltage CMOS ring-VCOs, and (iii) the design of a high-speed ring oscillator.

I chose phase locked loop because it is an excellent research topic, as it covers many disciplines of electrical engineering such as communication theory, control theory, signal analysis, noise characterization, microelectronic transistor design, digital circuit design and non-linear circuit analysis.

1.2 Contribution

The contributions made in this thesis are three-fold:

1. A comprehensive review of the architectures of CMOS charge pumps and an in-depth comparison of their characteristics such as speed, minimum supply voltage, mismatch-induced errors, charge injection and clock feed-through induced errors, and noise rejection is presented.

2. A comparative study of the architecture and timing jitter of the delay-cells of low-voltage CMOS ring-VCOs. Design considerations, such as noise, single-ended versus differential configurations, linearity and symmetry of load, and the output voltage swing of delay cells were examined in detail. The worst-case sensitivity of the delay time of the delay cells and that of the oscillation frequency of corresponding ring-VCO were analyzed and simulation results are presented.

3. A new delay cell utilizing inductive loads to enhance the oscillation frequency of a four-

stage ring oscillator was proposed. Both theoretical analysis and simulation results are presented. The new delay cell improves the oscillation frequency by 42%.

1.3 Thesis Organization

This thesis is organized as follows:

- Chapter 2 introduces the PLL system theory, challenges and trade-offs that lie in the design of PLLs.
- Chapter 3 presents the performance metrics of phase-frequency detectors and examines their different architectures.
- Chapter 4 examines both the architectures and design considerations of CMOS charge pumps for phase-locked loops.
- Chapter 5 presents a comparative study of the architecture and timing jitter of the delay-cells of low-voltage CMOS ring-VCOs. Design considerations, such as noise, single-ended versus differential configuration, linearity and symmetry of load, and the output voltage swing of delay cells are examined in detail. The worst-case sensitivity of the delay time of the delay cells and that of the oscillation frequency of corresponding ring-VCO are presented.
- Chapter 6 details the design of a new delay cell used in a 4-stage ring oscillator. A comprehensive analytical analysis of the oscillating speed of ring VCOs is provided. Simulation results are presented to verify the speed improvement.
- Chapter 7 details the design of a charge-pump PLL that employs the proposed delay cell. System level design, transistor level design and simulation results are presented.
- Chapter 8 concludes the thesis and presents several research areas to be explored in the future.

Chapter 2

Phase-Locked Loops

This chapter introduces the PLL system theory, challenges and trade-offs that lie in designing a PLL. In Section 2.1, the PLL is introduced and its function and operating regions are defined. The PLL's loop dynamics are formulated in Section 2.2. Critical parameters of PLLs are defined in Section 2.3. Section 2.4 presents the loop dynamics and stability analysis of a charge-pump PLL.

2.1 Basic Topology and Function

A phase-locked loop is a feedback control circuit that synchronizes the frequency of the oscillator's output with that of a reference signal. A simple PLL utilizes three basic blocks: a phase detector (PD), a loop filter (LPF), and a voltage controlled oscillator (VCO), as shown in Figure 2.1 [3].

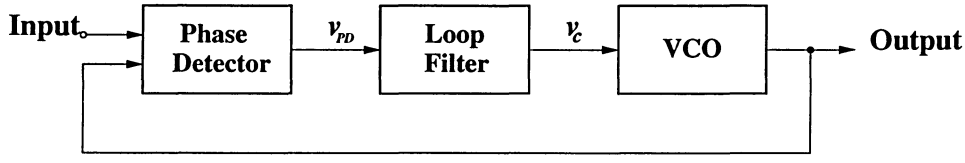

Figure 2.1: Basic phase-locked loop.

A phase detector compares the phase difference between the input reference signal and the oscillator output. The PD generates an output voltage v_{PD} proportional to the phase

difference between the two signals. A loop filter is a low-pass filter that filters out the high frequency components of v_{PD} to produce v_c, which is the control voltage of the VCO. The control voltage v_c determines the frequency of the output voltage of the VCO.

2.1.1 Phase Detectors

An ideal phase detector produces an output signal whose DC value is linearly proportional to the phase difference of the two input signals[2]:

$$\overline{v_{PD}} = K_{PD}\Delta\phi, \tag{2.1}$$

where K_{PD} is the gain of the phase detector, and $\Delta\phi$ is the phase difference between the two input signals, as shown in Figure 2.2.

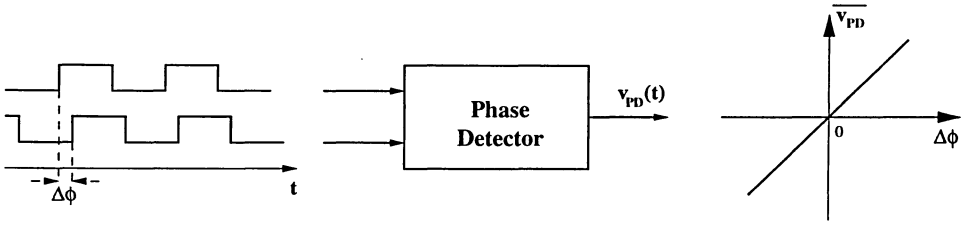

Figure 2.2: Characteristic of an ideal phase detector.

The phase detector input-output characteristic should ideally be linear, non-periodic, and monotonic for a wide range of phase difference values. In reality, the gain or slope K_{PD} of the characteristic is not constant and may depend on either the amplitude or duty-cycle of the input signals. Chapter 3 will further evaluate the design considerations of PDs, the different architectures, their advantages and limitations.

2.1.2 Voltage Controlled Oscillators

An ideal voltage controlled oscillator produces an output signal whose frequency ω_{out} is a function of the control voltage v_c[1]:

$$\omega_{out} = \omega_{FR} + K_{VCO}v_c, \tag{2.2}$$

where ω_{FR} is the free-running frequency of the VCO and K_{VCO} is the gain of the VCO. The relations between time, phase, and frequency provide us with an expression of the output voltage of the VCO:

$$y(t) = A\cos(\omega_{FR}t + K_{VCO}\int_{-\infty}^{t} v_c dt). \tag{2.3}$$

The VCO is considered a linear time-invariant system whose output of concern is the output excess phase. Equation (2.3) provides us the input (v_c) - output (ϕ_{out}) relationship as:

$$\phi_{out}(t) = K_{VCO}\int v_c dt, \tag{2.4}$$

from which we obtain the input-output transfer function:

$$\frac{\Phi_{out}(s)}{V_c(s)} = \frac{K_{VCO}}{s}. \tag{2.5}$$

It is important to know that v_c in itself does not determine the phase at the output, but the frequency. A change in v_c will lead to either an increase or decrease in the output frequency ω_{out} and consequently the output will either accumulate or dissipate phase faster thereby reducing phase-error. In essence, the initial conditions of the VCO and the system response determine the phase.

2.1.3 PLL Operating Regions

In this section we define the lock conditions, locked states, and the regions of operation of PLLs. Note that the behavior of PLLs in an unlocked state is not important. What is important is whether the PLL enters lock and how it acquires lock.

For PLLs to achieve *lock*, both frequency acquisition and phase acquisition must be attained. Frequency acquisition is defined as having equal input and output frequencies [1]. This condition is extremely important for applications such as frequency synthesis that is intolerant to frequency inaccuracies. Phase acquisition is defined as having the phase error settle to a constant value, not necessarily zero, with respect to time. In the case where frequency

acquisition is met, but phase acquisition is not, the loop must continue the transient, temporarily loosing frequency acquisition until both lock conditions are met.

In the locked state, all signals within the phase-locked loop will be in a steady state [1]. The phase detector will generate an output whose average DC value is proportional to the phase difference, and the VCO will oscillate at a frequency equal to the input frequency with a phase difference $\Delta\phi$.

The PLL's operation can be dissected to four different regions. In the case when the output signal is not *locked* in frequency and phase with the input signal, the PLL is said to be in a dynamic state. Alternatively, the PLL is said to be in a static state when the output signal is locked with only the frequency of the input reference signal. The four regions of operation are shown in Figure 2.3 [3] as *hold range, pull-in range, pull-out range*, and *lock range.*

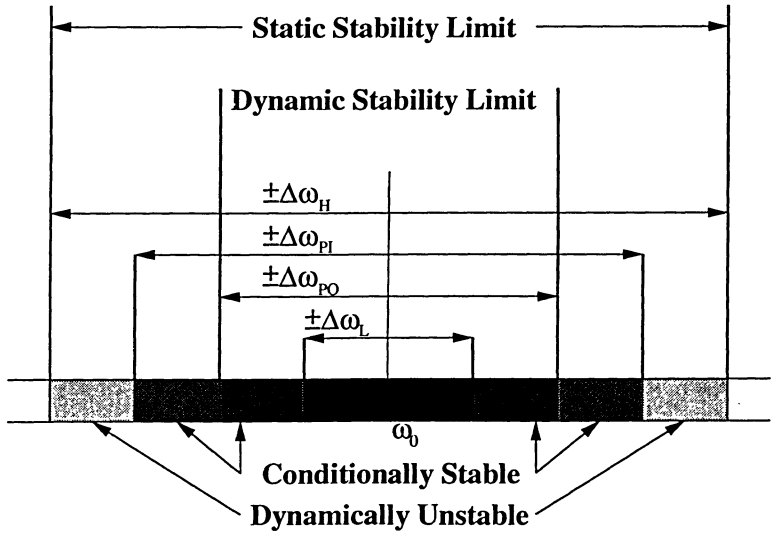

Figure 2.3: PLL Regions of Operations.

Hold range: The hold range $\Delta\omega_H$ is the frequency range over which the PLL can maintain phase tracking without falling out of lock.

Pull-in range: The pull-in range $\Delta\omega_{PI}$, also known as capture/acquisition range[1], describes the frequency range of the input signal over which the PLL can acquire lock. The process of acquiring lock within the pull-in range maybe a slow process. However, if the input reference frequency is within the narrower lock range, then the process of acquiring lock will be faster.

Lock range: The lock range $\Delta\omega_L$, also known as the tracking range[2], is the input frequency range over which the PLL can acquire lock without cycle slips. i.e. within a single beat.

Pull-out range: The pull-out range $\Delta\omega_{PO}$ determines the dynamic limit for stable operation. In other words, it determines the maximum value of the frequency step that can be applied at the input without causing the PLL to unlock. Assuming the PLL is in lock, if a frequency step that exceeds the pull-out range is applied to the input, the PLL will not be able to track and will fall out of lock.

2.2 Loop Dynamics

While the transient response of a phase-locked loop is a nonlinear process that is difficult to formulate, a linear approximation is useful in understanding the PLL's behavior and design tradeoffs. In this section, the transfer function of the PLL is derived and its static and dynamic behaviors are analyzed [2].
Using the linear model, the open loop transfer function of the PLL is given by:

$$H_o(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = K_{PD}G_{LPF}(s)\frac{K_{VCO}}{s}, \tag{2.6}$$

where G_{LPF} is the transfer function of the loop filter. Assuming the loop filter in use is a simple RC low pass filter, the transfer function will have the following form:

[1] We will avoid using the deceptive term *capture range*, since it is used as an alternative for lock range in some texts and pull-in range in others.

[2] When frequency detection is a property of the phase detector, tracking range becomes equal to acquisition range (Chapter 3).

$$G_{LPF}(s) = \frac{1}{1 + \frac{s}{\omega_{LPF}}} = \frac{1}{1 + sR_1C}. \tag{2.7}$$

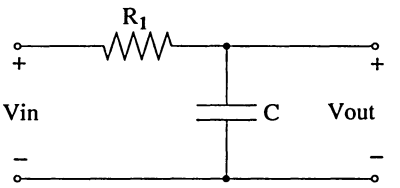

Figure 2.4: Simple low pass filter.

Thus the closed loop transfer function is simplified to

$$H_c(s) = \frac{H_o(s)}{1 + H_o(s)} = \frac{K_{PD}G_{LPF}(s)K_{VCO}}{s + K_{PD}G_{LPF}(s)K_{VCO}} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}. \tag{2.8}$$

The derived closed loop transfer function indicates that the PLL is a second order system with the loop gain $K = K_{PD}K_{VCO}$ and two poles, one contributed from the LPF and the other from the VCO. From control theory, we recognize the form of the close loop transfer function as:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{2.9}$$

where ω_n is the natural frequency, and ζ is the damping factor.

By comparing (2.8) and (2.9), we obtain

$$\omega_n = \sqrt{\omega_{LPF}K}, \tag{2.10}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K}}. \tag{2.11}$$

For a flat frequency response, the optimum value for damping factor ζ is equal to $\frac{\sqrt{2}}{2}$. This value dictates a relationship between the LPF's cut-off frequency ω_{LPF} and the loop gain K: $K = \frac{\omega_{LPF}}{2}$. This relationship puts a constraint on choosing K and ω_{LPF} independently in the design of a PLL.

2.3 Critical Parameters

In this section, we define the performance criteria of PLLs. They are static phase-error, tracking range, acquisition range, and acquisition time [1, 3, 5].

2.3.1 Static Phase Error

Even-though the PLL operates on excess phase ϕ_{out}, its phase error[3] final settling ($t \to \infty \equiv s \to 0$) value and its response to frequency variations is of interest . The phase error transfer function is obtained from:

$$H_e(s) = \frac{\Phi_e(s)}{\Phi_{in}(s)} = 1 - H(s) = \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{2.12}$$

With the current configuration where, a single pole loop filter is used, Equations (2.9) and (2.12) indicate that a *static* phase shift at the input is transferred to the output unchanged (as s $\to$ 0, H(s) $\to$ 1 and $H_e(s) \to 0$). On the other hand, a rapid variation of the phase of the input (*dynamic* phase shift) will lead to a small variation in the phase of the output.

Given that a phase shift is due to a change in frequency, it is worthwhile to analytically see the effect of an input step frequency $\Delta\omega u(t)$ to the output phase error, where $u(t)$ is the unit step function. The phase error is calculated as follows[4]:

$$\Phi_e(s) = H_e(s)\Phi_{in}(s) \tag{2.13}$$

$$= \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}\frac{\Delta\omega}{s^2}, \tag{2.14}$$

and its final settling value is:

$$\lim_{t\to\infty} \Phi_e = \lim_{s\to 0} s\Phi_e(s), \tag{2.15}$$

[3]In case where the PLL is designed to lock onto a non-zero phase difference ($\Delta\phi = constant \neq 0$), then $\phi_e \neq \Delta\phi$.

[4]The Laplace transform of the frequency step equals $\Delta\omega/s$, therefore the input phase would be its derivative $\Delta\omega/s^2$.

$$= \Delta\omega\frac{2\zeta}{\omega_n}, \tag{2.16}$$

$$= \frac{\Delta\omega}{K}. \tag{2.17}$$

The above calculations conclude that static frequency variations at the input will manifest themselves as static phase shifts attenuated by a factor K at the output. It is obvious that in order to minimize the phase error, a high loop gain K is needed. However, Equation (2.11) indicates that a tradeoff has to be made between ζ that determines the settling behavior (see Section 2.3.4), ω_{LPF} that determines the cutoff frequency of the loop filter, and K that determines the phase error, and width of the acquisition range (see Section 2.3.3).

To allow for a larger gain independent of ω_{LPF} and without sacrificing the settling time, a zero (resistor R_2) added to the LPF would modify the loop filter transfer function to

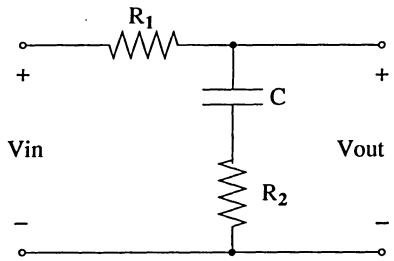

Figure 2.5: Loop filter with an added zero.

$$G_{LPF}(s) = \frac{sR_2Cs + 1}{s(R_1 + R_2)C + 1}. \tag{2.18}$$

A similar calculation to those presented before will yield a closed loop transfer function

$$H(s) = \frac{K\omega_{LPF}(\frac{s}{\omega_z} + 1)}{s^2 + \omega_{LPF}(\frac{K}{\omega_z} + 1)s + K\omega_{LPF}}, \tag{2.19}$$

where,

$$\omega_z = \frac{1}{R_2C}, \tag{2.20}$$

$$\omega_{LPF} = \frac{1}{(R_1 + R_2)C}, \tag{2.21}$$

and the damping factor ζ

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K}}(\frac{K}{\omega_z} + 1), \qquad \omega_z > \omega_{LPF}. \tag{2.22}$$

Using the same optimal ζ value introduced before, the reader can similarly calculate the gain K as $32\omega_{LPF}$, a much larger gain compared to $K = \frac{\omega_{LPF}}{2}$. However, a disadvantage of adding a zero to the loop filter is the decrease in the attenuation of high frequency signals. A possible solution would be to add another pole far from the zero in the form of a capacitor at the output. The downside of the additional pole is the degradation of the settling time, due to the change in the optimum damping factor.

2.3.2 Tracking Range

As explained earlier, the tracking range is defined as the input frequency range over which the PLL can acquire lock without cycle slips(*static tracking*) i.e. within a single beat [3].

Assuming that the loop filter's components are linear, for the PLL to track, the three characteristic curves (i) ϕ_e vs. ω_{in}, (ii) $\overline{v_{PD}}$ vs. ϕ_e, and (iii) ω_{out} vs. v_c must vary monotonically. In other words, the edge of the tracking range is determined by the slope/gain of each of the characteristic curves. The point at which any of the slopes approach zero or change sign defines the edge of the tracking range. While, the tracking range depends greatly on the type of phase detector used (see Chapter 3), for simplicity, we will assume that the phase detector is a simple analog multiplier. The gain K_{PD} of an analog multiplier, changes sign for input phase differences $\Delta\phi$ greater than $\frac{\pi}{2}$. Voltage controlled oscillators, on the other hand, have a limited frequency range, beyond which the gain K_{VCO} drops sharply. To lock within a single beat, the VCO output frequency can not vary by more than:

$$\Delta\omega_L = K_{PD}K_{VCO}\sin(\frac{\pi}{2}). \tag{2.23}$$

Because the tracking range refers to the deviation from the center free running frequency, the tracking range is half of the lock range.

2.3.3 Acquisition Range

In the case where a PLL acquires lock within a number of cycle slips or beats, the PLL is said to be in the *dynamic tracking* mode or within the acquisition range. In this section, we will determine the maximum input frequency range over which the PLL can acquire lock. We will present the process of acquiring lock in both frequency and time domains [1].

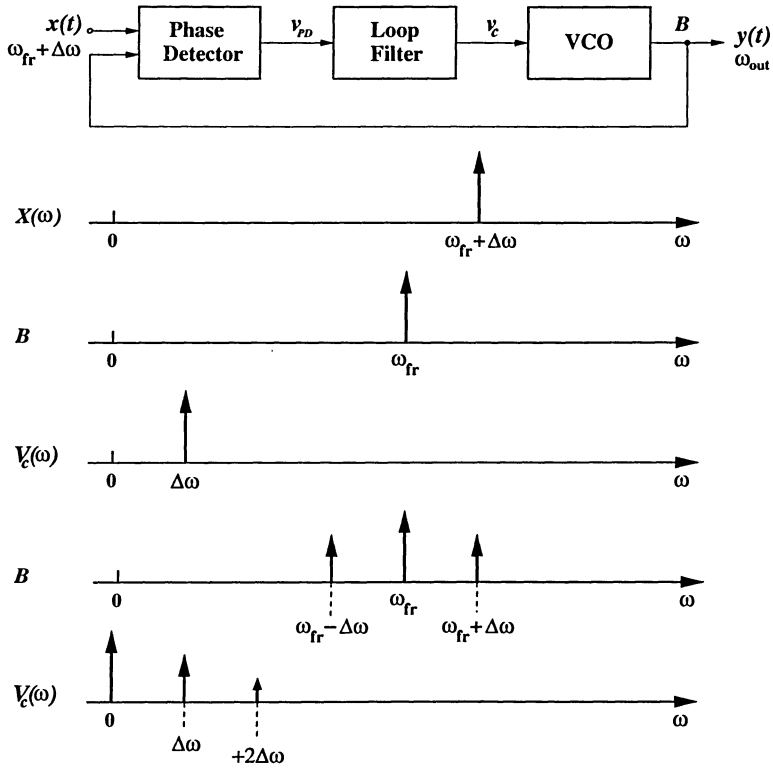

Figure 2.6: Acquisition of lock in frequency domain.

Frequency domain: Assuming that the phase detector is a simple analog multiplier, we will plot the frequency spectra (Figure 2.6) of the signals around the loop to illustrate the process of acquiring lock. With the assumption that the initial conditions of the loop filter are zero, the VCO output frequency should be $\omega_{out} = \omega_{fr}$. A frequency step $\Delta\omega$ is applied at the input to give $\omega_{in} = \omega_{fr} + \Delta\omega$. It can be shown analytically that the VCO output voltage will be [1]:

$$y(t) \approx A\cos\omega_{fr}t - \frac{K_{VCO}}{\Delta\omega}A_m \sin\omega_{fr}t \sin(\Delta\omega t), \tag{2.24}$$

where A is the amplitude of the output voltage, and A_m is the amplitude of the modulated control voltage. The spectra of the modulated signal has sidebands at $\omega_{fr} \pm \Delta\omega$, the phase detector multiplies the sidebands with the input frequency, resulting in a DC component at the control voltage. This DC component will grow over a number of cycles adjusting the VCO frequency until lock. From our analysis, we observe that the acquisition range is a function of: (1) the attenuation of the loop filter components at $\Delta\omega$ and (2) the feedback strength of the DC component. In other words, the acquisition range is a function of the loop gain at $\Delta\omega$. Simple type-I [5] PLLs mentioned so far, experience a fading loop gain at larger frequency differences.

Time domain: Assuming the same initial conditions mentioned above, in this section we illustrate the process of lock in the time domain. During the first cycle, where the feedback in the loop has not yet affected the response, the output of the combined analog phase detector and loop filter v_c is a sinusoid with a frequency equal to $\Delta\omega = \omega_{in} - \omega_{out} = \omega_{in} - \omega_{fr}$. Moreover, the frequency of the VCO increases and decreases with v_c. The implication is that $\Delta\omega_{max}$ refers to positive peak of the sinusoid and $\Delta\omega_{min}$ refers to the negative peak.

Without the feedback signal, the sinusoidal signal is periodic and symmetric with an average DC value of zero. To acquire lock, the DC value of v_c must move the frequency of the VCO in the direction of the reference input frequency. Fortunately, the feedback signal once introduced, has a time-varying frequency due to frequency modulation at the VCO. If the output frequency is modulated in the positive direction, the frequency difference decreases and the sinusoid will have longer positive cycles as shown in Figure 2.7. Consequently v_c will have a larger positive DC component that will allow the PLL to lock.

[5] Type-I refers to the order of the PLL, more specifically the number of poles in the loop filter, in this case being one

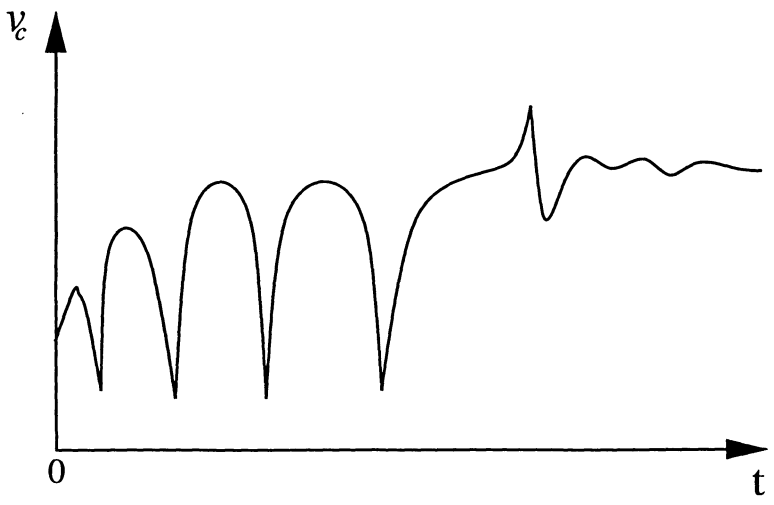

Figure 2.7: Acquisition of lock in time domain.

We can conclude that the proximity of ω_{in} to ω_{out} will determine whether the loop will acquire lock within one beat or several beats. The number of *cycle slips* needed for lock is a function of the initial conditions of the loop filter and VCO [3]. The analytical estimation of the acquisition range is [3]:

$$\Delta\omega_{acq} = K_{PD}K_{VCO} \mid G_{LPF}(j\Delta\omega) \mid . \tag{2.25}$$

2.3.4 Acquisition Time

The terms acquisition time and settling time are often mistakenly interchanged. The difference stems from the operating region of PLLs. While in the lock-tracking range, the time needed for a PLL to lock within a defined phase-error is referred to as the lock-in or settling time. For a second order PLL ($\zeta < 1$), the step response is given by [1]:

$$y(t) = \left[1 + \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin(\omega_n\sqrt{1-\zeta^2} - \psi\right] u(t), \tag{2.26}$$

where $\psi = \sin^{-1}\sqrt{1-\zeta^2}$. The settling time can be derived form (2.26):

$$t_{settle} = \frac{1}{\zeta\omega_n} = \frac{2}{\omega_{LPF}}. \tag{2.27}$$

Clearly, there is a trade-off to be made between stability and ripple noise on the control voltage v_c. To minimize the ripple in the control voltage, the cut-off frequency of the loop filter has to be decreased. The drawback of decreasing ω_{LPF} is stability degradation in the form of a prolonged settling time.

Acquisition time on the other hand, refers to the acquisition operating range of the PLL, and so defines the time needed for the PLL to acquire lock given a certain frequency difference. The acquisition time for a linear type-I PLL is given by [3]:

$$t_{acq} = \frac{\pi^2}{16}\frac{\Delta\omega_0^2}{\zeta\omega_n^3}. \tag{2.28}$$

2.3.5 Aided Acquisition

For a PLL employing a simple one-pole loop filter, designed for an optimum damping factor of $\zeta = \frac{\sqrt{2}}{2}$, Equation 2.25 will conclude an acquisition range of $\Delta\omega_{acq} = 0.5\omega_{LPF}$, a rather small range. Due to jitter and sideband suppression requirements, minimize the ripple on the control voltage v_c, increasing ω_{LPF} is not feasible. Moreover, the loop gain fades as the input output frequency deviation increases. For the reasons mentioned, PLLs often employ a frequency detector to aid in the acquisition of frequency. The frequency detector will produce a DC voltage proportional to the *frequency difference* $\omega_{in} - \omega_{out}$. The concept is simple, for large frequency differences, the VCO will be driven by the DC of the frequency detector, and for small frequency differences, the VCO will be driven by the DC of the phase detector. With the addition of frequency acquisition, the loop gain is now constant and independent of the value of $\omega_{in} - \omega_{out}$, this can substantially increase the acquisition range to a limit set by the tuning range of the VCO (see Chapter 3).

2.3.6 Phase Noise and Jitter

One of the more important design considerations of phase locked loops is phase noise or jitter. An ideal periodic signal has a frequency spectra with an impulse at the fundamental frequency, in addition to energy impulses at DC and the harmonic frequencies of the fundamental frequency. Timing jitter is the resultant of varying zero crossings in the time domain (see Figure 2.8(L)). In the frequency domain, these variations result in energy skirts (see Figure 2.8(R)) known as phase noise [1, 3, 12].

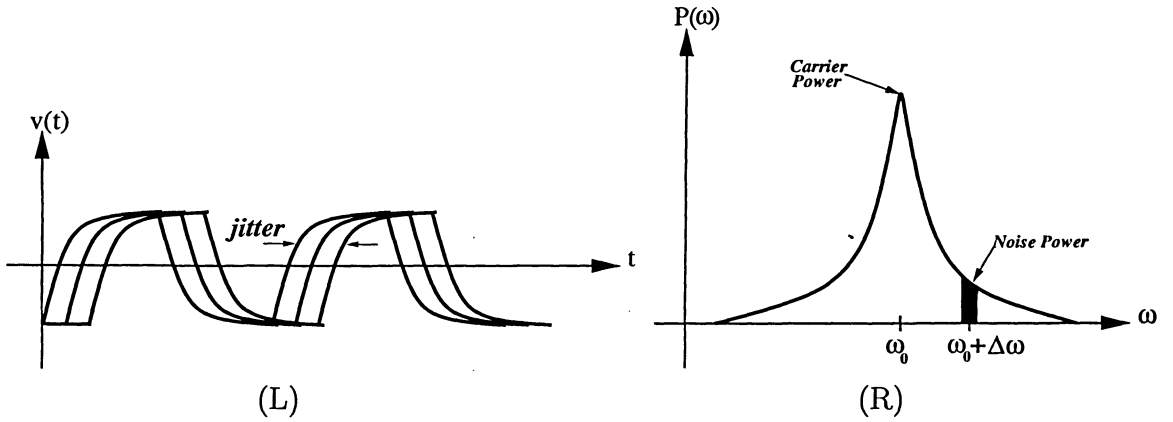

Figure 2.8: (L) Jitter in a periodic signal, and (R) Frequency spectrum of a signal with Phase noise.

Phase noise is defined as the ratio of the power of the sideband noise P_{SB} in a $1Hz$ bandwidth at a given offset frequency $\Delta\omega$ to the carrier power P_c:

$$L\{\Delta\omega\} = 10\log_{10}\frac{P_{SB}(\omega_0 + \Delta\omega, 1HzBW)}{P_c}. \tag{2.29}$$

Phase noise in the frequency domain in specified in dBc/Hz at a given frequency offset $\Delta\omega$, and translates into jitter specified by its peak-to-peak time value (*picoseconds*) in the time domain. While all PLL blocks contribute to the overall phase noise, we will only present the more dominant noise sources, input referred phase noise, and VCO generated phase noise. In both cases, we assume that the phase noise is a random component of the excess phase that the PLL operates on.

Input Phase Noise: The input-output phase transfer function given in (2.9), indicates that for a constant input excess phase or a slowly varying input phase with respect to time, $H(s)$ is approximately equal to unity and consequently the output follows the input. As the input phase noise $\phi_{in}(t)$ varies at higher rates, the output phase depreciates to zero and the PLL fails to track. The input phase noise transfer function, obviously has a low pass characteristic. In order to reduce the input refereed phase noise, the PLL loop bandwidth must be reduced. The consequences of reducing the loop bandwidth are, a reduction in lock speed, a limited capture range, and a degradation in stability.

VCO Phase Noise: The phase noise generated by the VCO ϕ_{VCO} is modelled as an input signal. Assuming the VCO phase noise is uncorrelated to the input phase noise $\phi_{in}(t)$, then the VCO phase noise transfer function is:

$$\frac{\Phi_{out}(s)}{\Phi_{VCO}(s)} = \frac{s(s+\omega_{LPF})}{s^2+2\zeta\omega_n s+\omega_n^2}. \tag{2.30}$$

The VCO phase noise transfer function has a high pass characteristic, and in order to reduce the VCO-referred phase noise, a PLL with a wide loop bandwidth is preferred. Clearly, a tradeoff has to be made regarding the width of the PLL bandwidth and its effect on the noise contribution from the input and the VCO. The application will dictate the loop bandwidth. The VCO phase noise is caused by several sources: up-converted $1/f$ noise of the transistors, ripple in the control voltage, and power supply voltage fluctuations among other things. Chapter 5 will elaborate more.

2.4 Charge Pump Phase-Locked Loop CP-PLL

The charge-pump phase locked loop (CP-PLL) shown in Figure 2.9 is preferable to the conventional PLL for the following reasons:

- The CP-PLLs pull-in range is limited only by the VCO's tuning range [3].

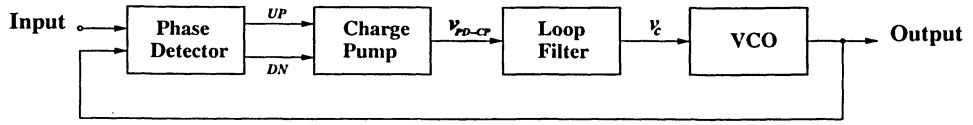

Figure 2.9: Charge-pump phase-locked loop.

- The CP-PLL locks to a phase error of zero, even if the reference input frequency is not equal to the center free-running frequency of the VCO, as was the case in the simple PLL [1].
- The CP-PLL displays more immunity to power supply variations [4].
- The CP-PLL does not experience charge decay as compared to the conventional PLL. This is because, in the simple PLL, charge is applied to the loop filter capacitor at every phase comparison, and between the phase comparison, the charge across the capacitor decays. With a charge pump in place, decay is minimized [2].

The CP-PLL, also referred to as the classical digital PLL uses the charge pump at the output of the phase-frequency detector. Only in this case, the phase-frequency detector produces two control signals UP and DN as opposed to one. The control signals will determine how much error current is applied to the loop filter. The charging and discharging of the loop filter will determine the value of the control voltage.

The combined response of a charge pump-phase frequency detector to a static phase difference is a linear ramp. In other words, the transfer function of the charge-pump and phase frequency detector combined, contains a pole at the origin and can be represented as:

$$H(s)_{PFD-CP} = \frac{K_{PD}}{s}. \tag{2.31}$$

Clearly, with the addition of the charge-pump and all its advantages, the stability and dynamics of the PLL have changed. In the following sections, we analyze the stability and dynamics of CP-PLL [1, 12].

2.4.1 Stability

To ensure that the CP-PLL is a stable system, care must be taken in the design of the loop filter. With solely a capacitor as the loop filter, the new PLL transfer function can be easily computed as:

$$H_c(s) = \frac{K_{PFD}K_{VCO}}{s^2 + K_{PFD}K_{VCO}}. \tag{2.32}$$

The above transfer function has two imaginary poles, rendering the system unstable. An added zero in the form of a resistor in series with the capacitor of the loop filter can help stabilize the system. The disadvantage of adding a resistor, is an increase in ripple at the control voltage. This ripple can be suppressed by a second capacitor C_2 in parallel with the $R-C_1$ combination. C_2 should be chosen in the order of one-tenth of C_1, so that the system can still be analyzed as a second order system.

2.4.2 Dynamics

Assuming that the loop is experiencing a phase difference of $\Delta\phi = \phi_{in} - \phi_{out}$, the charge pump will produce an average current equal to:

$$I_{ave} = \frac{I\Delta\phi}{2\pi}, \tag{2.33}$$

and the loop filter will produce a control voltage:

$$V_c(s) = \frac{I\Delta\phi}{2\pi}(R + \frac{1}{sC_p}). \tag{2.34}$$

Consequently, the VCO output phase will be equal to:

$$\Phi_{out}(s) = V_c(s)\frac{K_{VCO}}{s}. \tag{2.35}$$

The closed loop transfer function, can easily be computed to:

$$H(s) = \frac{\Phi_{out}(s)}{\Delta\Phi(s)} = \frac{\frac{I}{2\pi C_p}(RC_ps + 1)K_{VCO}}{s^2 + \frac{I}{2\pi}K_{VCO}Rs + \frac{I}{2\pi C_p}K_{VCO}}, \tag{2.36}$$

that has the form:

$$H(s) = \frac{K\omega_p(\frac{s}{\omega_z} + 1)}{s^2 + \omega_p(\frac{K}{\omega_z} + 1)s + K\omega_p}, \tag{2.37}$$

from which we can calculate:

$$\begin{aligned} \omega_n &= \sqrt{\frac{I}{2\pi C_p} K_{VCO}}, \\ &= \sqrt{K\omega_p}, \end{aligned} \tag{2.38}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{IC_p}{2\pi} K_{VCO}}. \tag{2.39}$$

We can also repeat the calculations seen in Section 2.3.4, to calculate

$$\begin{aligned} t_{settle} &= \frac{2}{\zeta\omega_n}, \\ &= \frac{8\pi}{RIK_{VCO}}. \end{aligned} \tag{2.40}$$

With the dynamics computed, we note the following observations:

- High frequency applications require high loop bandwidth, which is proportional to the natural frequency ω_n. Using the conventional PLL, ω_n could only be increased by increasing ω_{LPF} (see Equation 2.11), which is undesirable for low noise applications (see Section 2.3.6). In a CP-PLL, ω_n can be increased through the charge pump current I or VCO gain K_{VCO} as shown in (2.39).

- By comparing (2.27) and (2.40), we notice that with the CP-PLL design, t_{settle} is independent of the loop filter capacitor.

- The dynamic analysis of the simple PLL is based on the assumption that the system is a linear system. This assumption holds true on condition that the input reference frequency be much greater than the loop bandwidth. When the condition does not hold, discrete time analysis should be used. Since the loop bandwidth is directly proportional to the natural frequency ω_n, discrete time analysis leads to the stability

limit [5]:

$$\omega_n^2 < \frac{\omega_{in}^2}{\pi(RC_1\omega_{in} + \pi)}, \tag{2.41}$$

which puts a limit on the value of the resistor R. On the other hand, in the CP-PLL configuration, ω_n is independent of R, which eases the design constraint.

Chapter 3

Phase-Frequency Detectors

The dynamics of the PLL described in Chapter 2, conclude that the performance of the PLL -Tracking Range, Acquisition Range, Loop Gain, and Transient Response- depends on the properties of the PD in-use. Section 3.1 defines the performance evaluators of the PFD. This is followed by Section 3.2 that examines the different design techniques of phase detectors, phase-frequency detectors, and the dead-zone concept.

3.1 Functionality and Performance Evaluators

An ideal phase detector produces an output signal whose DC value is linearly proportional to the phase difference of the two input signals. The phase detector input-output characteristic should ideally be linear, non-periodic, and monotonic for a large range of phase difference $\Delta\phi$. In reality, the gain or slope K_{PD} of the characteristic is not constant and may depend on either the amplitude or duty-cycle of the input signals. The performance evaluators of a phase detector are illustrated below [1, 2, 3, 8].

Tracking Range: We can recall that the edge of the tracking range of a PLL is defined as: $\frac{\Delta\omega_L}{2}$, where $\Delta\omega_L = K_{PD}K_{VCO}\sin\frac{\pi}{2}$. Therefore, we have to ensure that the PD characteristic is monotone for a large phase difference $\Delta\phi$.

Acquisition Range: The acquisition range was defined as: $\Delta\omega_{acq} = K_{PD}K_{VCO} \mid G_{LPF}(j\Delta\omega) \mid$, the gain of the PD, K_{PD} is constant and independent of the amplitude and duty-cycle of the input signals. Moreover, the phase detector's ability to detect input signals of different frequencies can greatly enhance the acquisition range, and remove its dependance on the gain K_{PD} and loop-filter frequency ω_{LPF}.

Lock Condition: Ideally, in the locked state the phase detector's output is zero, the charge-pump is no longer switching, and the control voltage is fixed. In practice, the phase detector's output is not zero, and can create unwanted switching activity at the charge-pump which increase the jitter and ripple on the control voltage V_c.

Sensitivity to input data pattern: PDs usually require that the input data have a minimum timing content. Long strings of ones and zeros could result in high VCO output jitter, due to the activity introduced to the control voltage V_c, even while in lock.

Lock Speed: Lock speed is an evaluation parameter of PLLs, but the choice of PD can greatly affect the time needed for a PLL to lock, given a phase difference. For example, digital PDs operate at slow speeds and require sufficient time for the outputs to stabilize, they suffer from long Lock time. Analog PDs are more suitable for high-speed applications, but are slightly more complex.

3.2 Design Techniques

Phase detectors can be categorized into: (i) Combinational PDs, (ii) XOR PDs, and (iii) Edge-triggered PDs [8]. In the following section, we will examine PDs that are widely used, and highlight their advantages, disadvantages, and performance limitations.

3.2.1 Phase Detectors

Gilbert Cell PD

The schematic and transfer characteristics of the Gilbert cell based PD is shown in Figure 3.1 [1]. When the inputs of the cell are of small amplitude, the cell behaves as an analog multiplier, whose output is determined by

$$\overline{V_{out}} = \frac{\alpha AB}{2}\cos(\Delta\phi), \tag{3.1}$$

where α is a factor due to the multiplier, A and B are the amplitudes of the input signals. Although this implementation is characterized as having a high operating speed, its input-output characteristic is nonlinear, sinusoidal and periodic. For phase differences near 90^o, the relationship is approximately linear. While the characteristic of the cell in Figure 3.1 indicates that it has a limited tracking range of 90^o. Within the range, the PD's gain is a function of the amplitude of the input signals. Moreover, the cell suffers from high statistic power consumption, and can not detect frequency errors.

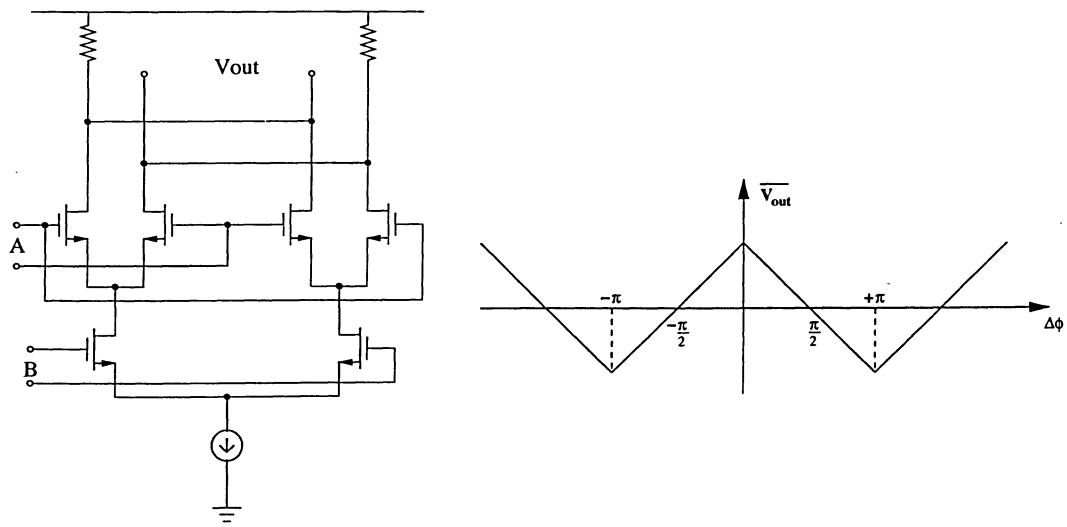

Figure 3.1: Gilbert cell PD and characteristic.

XOR PD

When the inputs of the cell shown in Figure 3.1 are of large amplitude, the cell behaves as a XOR gate or a digital multiplier [1], whose output is determined by the following equation:

$$\overline{V_{out}} = \frac{V_{DD}}{\pi}\Delta\phi. \tag{3.2}$$

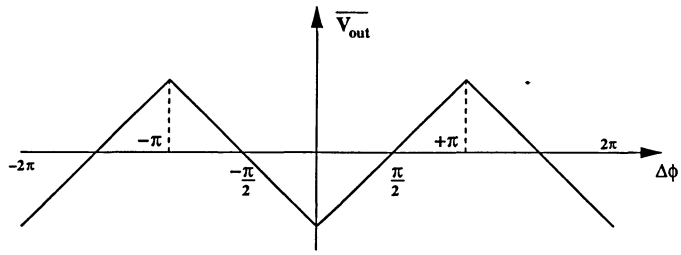

Figure 3.2: XOR characteristic.

As compared with the Gilbert cell PD, the tracking range has been improved to ($0^o \sim 180^o$) as shown in Figure 3.2, and the gain is no longer dependant of the amplitude of the input signals. A drawback of this circuit is the output's dependance on the duty-cycle of the inputs; i.e. when the phase difference between the inputs varies from 90^o, the output duty-cycle will no longer be 50%, resulting in an output DC value proportional to $\Delta\phi$. This manifests itself as a static phase error in the PLL.

SR-Latch PD

The SR-Latch [12], is an edge-triggered 2-state PD. The rising edge of A drives Q to '1' and the rising edge of B resets Q to '0'. Hence, the differential output changes sign for every consecutive rising edges of the inputs. Inherently, the input and output frequencies are the same.

The advantages of the SR-latch are: (1) Monotonic Acquisition range of $\pm 180^o$, and (2) a DC output independent of the duty-cycle of the inputs as shown in Figure 3.3. The drawbacks of this cell are: (1) For applications that require frequency multiplication/synthesis, equal

input and output frequencies is undesirable, (2) In cases where one of the input frequencies is an integer multiple of the other, the SR-latch generates a nonzero DC output. As a result, PLLs employing an SR-Latch may lock onto a higher harmonic, and (3) the SR-latch provides only two output states, giving rise to significant ripple on the control line in the locked condition and hence producing greater jitter at the VCO output.

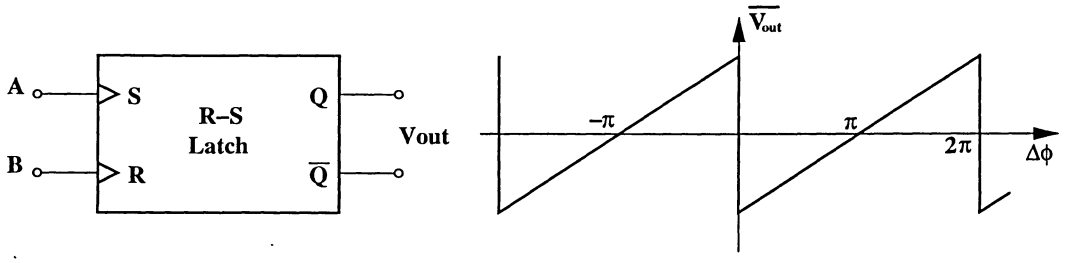

Figure 3.3: SR-latch PD and characteristic.

Sample-and-Hold PD

Linear PDs are characterized as having linear input-output characteristics, with minimal activity at the charge-pump after lock. Their drawback was in generating pulse-widths equal to a fraction of the clock period at high speeds. Digital PDs, on the other hand, employed simple flip-flops for the maximum speed, but provided only two output states creating significant ripple on the control line in the locked condition and hence producing greater jitter at the VCO output. The sample-and-hold PD proposed in [7], attempted to overcome these limitations.

The master-slave sample-and-hold (S&H) circuit is equivalent to an analog D-flipflop whereby each data transition samples the value of the VCO output as shown in Figure 3.4. The advantages of this topology are: (1) the master-slave configuration avoids a transparent path between D_{in} and V_{out} producing a voltage linearly proportional to phase difference for most of the period, and (2) the path with large switching transients operates at the data rate and not the VCO rate, minimizing the activity on the control voltage.

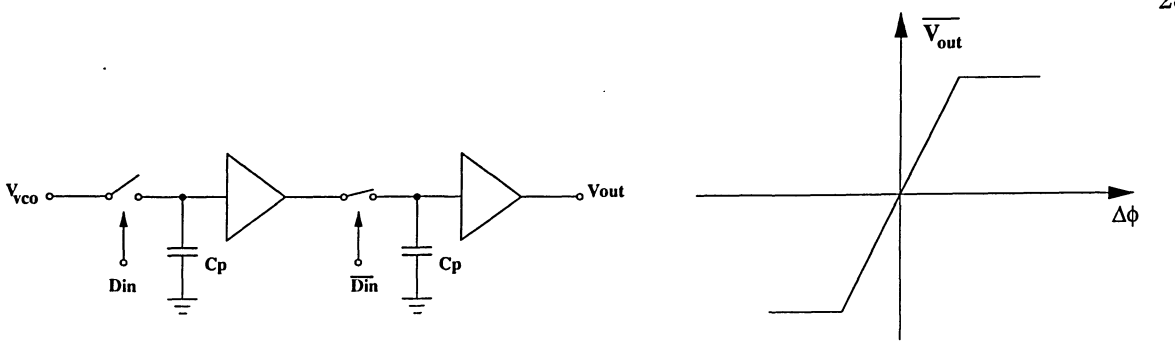

Figure 3.4: Sample-and-hold PD.

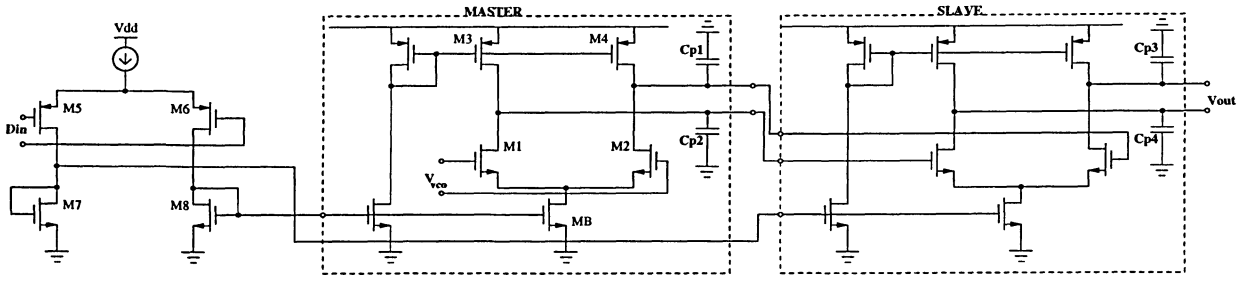

Figure 3.5: Sample-and-hold PD schematic.

An implementation of the S&H circuit is shown in Figure 3.5. The master and slave circuits are differential pairs whose tail current and load turn off simultaneously; storing the value of the VCO output on the parasitic capacitances C_{P1} to C_{P4}. The control circuit is implemented in PMOS transistors to allow for low-voltage operation.

The drawbacks of this circuit are: (1) limited acquisition range of $\pm 50^o$ [7], (2) sensitivity to the input data pattern, and (3) the speed is limited by the current steering circuit.

3.2.2 Phase-Frequency Detectors PFD

The main drawback of phase-detectors is their periodic transfer characteristic, which implies that phase-shifts of 2π cannot be distinguished. When the frequencies of the two input

signals are different, phase will accumulate, the output of PDs becomes unpredictable, depending on how far the loop is away from the lock state, acquisition time can suffer greatly if one of the PDs mentioned is used. A solution to extend the acquisition/tracking range and the lock speed of PLLs is to use phase-frequency detectors (PFDs) [1, 2, 12].

Phase-frequency detectors are able to sense phase as well as frequency differences when the loop is not locked. When in lock they behave as a PD, outputting a signal that is linearly proportional to the phase difference of the two input signals. In order to detect frequency differences, PFDs must contain memory, compared to the memoryless PDs. One possible solution is to implement PFDs as an edge-triggered sequential machine, as shown in Figure 3.6.

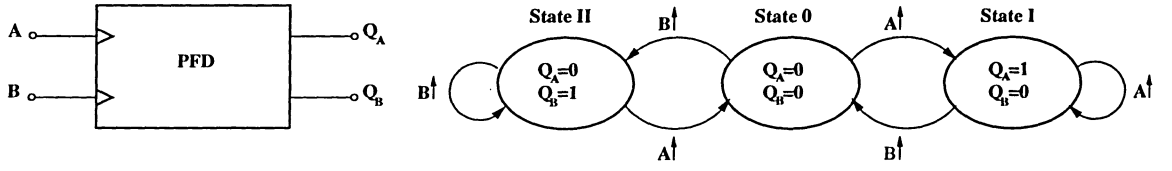

Figure 3.6: PFD state diagram.

The PFD functions as follows:

- $\omega_A < \omega_B$: PFD produces positive pulses at Q_A, while Q_B remains at zero.
- $\omega_A > \omega_B$: PFD produces positive pulses at Q_B, while Q_A remains at zero.
- $\omega_A = \omega_B$: PFD produces positive pulses at either Q_A or Q_B with a width proportional to the phase-difference between the two input signals.

Ideally, Q_A and Q_B are never high at the same time since they control the charging and discharging of the CP. Consequently, the three logical states are as seen in Figure 3.6. Assuming the circuit is rising-edge triggered, and we start in State 0, a transition on A takes it to State I, another transition on B takes it to State O and so on... Two possible implementations of the PFD are presented.

Two-XOR PFD

The Two-XOR PFD is used in conjunction with a 4 stage ring VCO generating eight differential clock signals *CLK1* through *CLK4* spaced by 45°. The Data_Lead signal is the resultant of XORing the CLK1 and CLK3 signals and hence is a periodic signal that acts as a charge-down signal, while the Data_Lag signal is the non-periodic signal, resultant of XORing the CLK1 and Data signals and acts as the charge-up signal. Figure 3.7 illustrates the operation of the Two-XOR PFD [6].

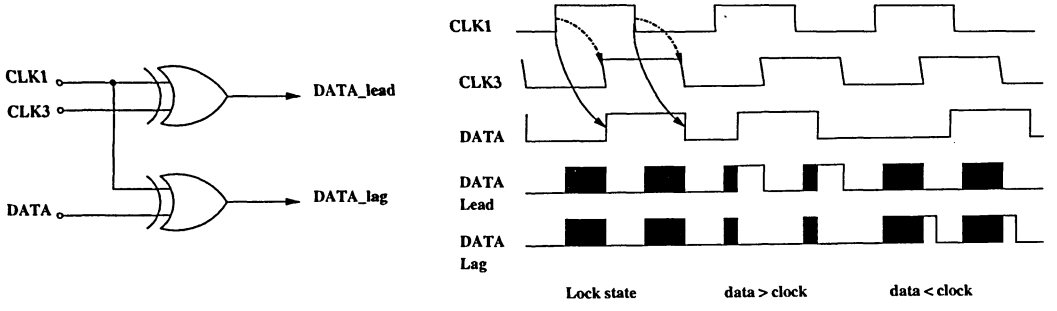

Figure 3.7: 2-XOR PFD.

The PFD achieves locked state when the signals *Data* and *CLK3* are phase-aligned as shown in Figure 3.7. The Data_Lead and Data_Lag signal transitions occur at the same time and the control voltage stays at the same level.

In the case of the input data is faster than CLK3, then the 'High' state of the lag signal is shorter than that of the lead signal, the CP discharges and the clock period becomes shorter to track the input. The opposite happens when the input data is slower than CLK3.

An example of frequency correction occurs when the frequency of the input data is faster than the clock, then the surplus part of the lead signal discharges current, so the clock can track the data.

The advantages of the Two-XOR PFD are its ease of implementation, its large acquisition range, and high lock speed. However, when it comes to long string of ones and zeros, the

lead and lag signals are generated alternately causing jitter at the control voltage.

D- Flipflop PFD

Another implementation of the PFD is shown in Figure 3.8 [9]. The PFD employs two edge-triggered resettable D-Flip-flops and an AND gate. The data inputs of the DFF are connected to logic 'ONE' with the clock inputs being the input signals A and B.

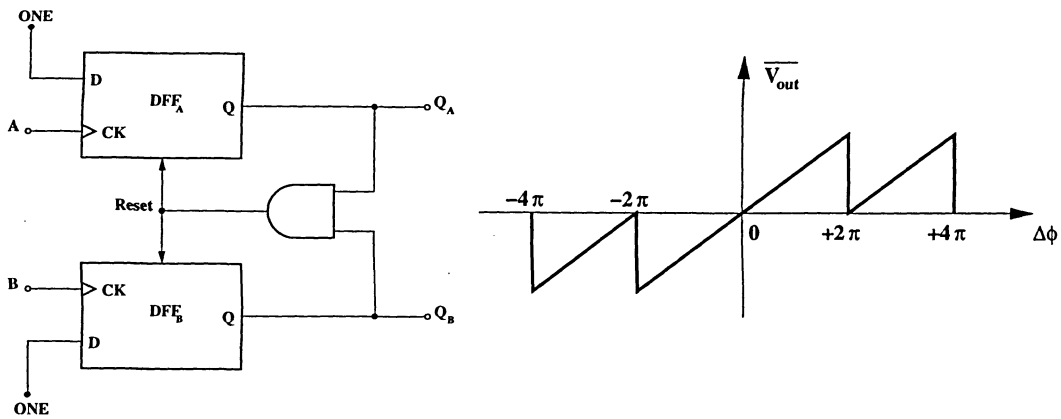

Figure 3.8: D-Flipflop PFD, and characteristic.

The PFD functions as follows: Starting in State 0 (Q_A=Q_B=0), a transition on A causes Q_A to go 'HIGH', further transitions on A will have no effect on Q_A. A transition on B, will cause Q_B to go 'HIGH', activating the AND gate and resetting both DFF. It is important to note the non-periodic behavior of the transfer characteristic for the PFD shown in Figure 3.8, when the phase difference is too large, the PFD enters the FD mode.

Since the PFD detects phase and frequency differences, it is characterized as having a wide Acquisition range, high lock speed, an output independent of input signal duty-cycle, and a constant gain over a phase error of $\pm 360^{o}$ as shown in Figure 3.8. Its drawbacks include: (1) output jitter due to the meta-stability during lock condition, and (2) Dead-Zone due to the delay associated with the DFF and AND gate to be explained in the following section.

Dead-Zone

The dead-zone problem occurs, when a PFD is used in conjunction with a Charge-Pump (CP). The delay associated with the DFF and AND gate compared to that of the charging of the capacitor at the CP switches, will determine whether the system is in the dead-zone region or not [1, 2].

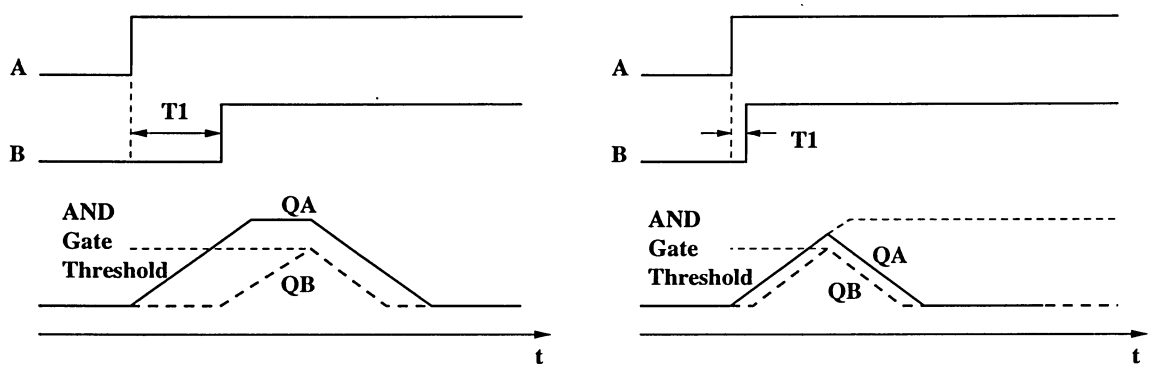

Figure 3.9: Dead-zone.

The dead-zone problem is better understood in conjunction with Figure 3.9. In the figure to the left, the phase difference between the two input signals A and B is large enough for the signals Q_A and Q_B to reach full logic levels of 'ONE'. In other words, there is enough time for the signal Q_A to charge the capacitor C_P. In the figure to the right, the time or phase-difference between the two input signals is too small, and the PFD resets before signal Q_A reaches a full logic level. In essence the CP switch fails to turn on for an ill-defined length of time. For such small phase differences, the gain of the PFD drops drastically as shown in Figure 3.10.

If the phase difference is within the dead-zone, the PLL will fail to correct itself and the deadzone will manifest itself as peak-peak jitter at the output. To avoid the dead-zone, a short delay is inserted between the output of the AND gate and the reset pins of the DFF

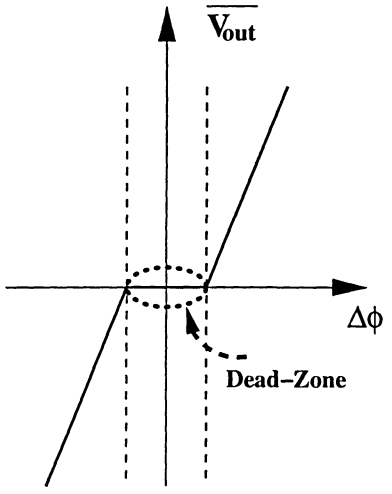

Figure 3.10: Dead-zone characteristic.

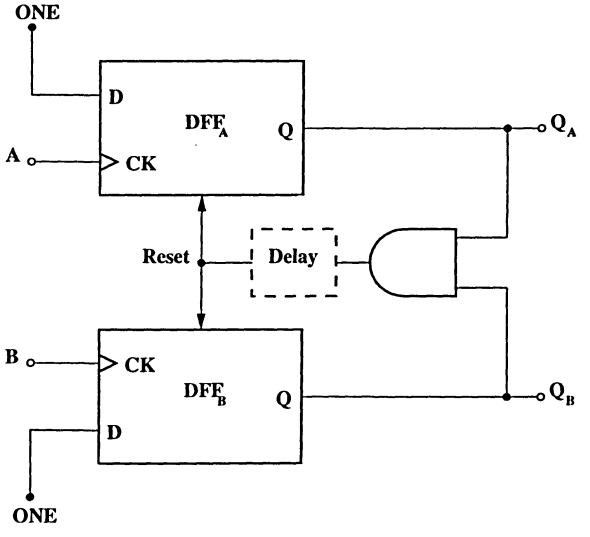

Figure 3.11: Dead-zone free PFD.

as shown in Figure 3.11 [10]. The delay for the reset signal must be long enough to allow for the full switching of the UP and DN pulses and CP switches. Caution should be exercised when choosing the length of the pulse as not to limit the operating frequency of the PFD to:

$$f_{max} = \frac{1}{2\Delta T}. \tag{3.3}$$

3.3 Conclusions

The architectures and design considerations of CMOS phase-frequency detectors for phase-locked loops have been presented. Basic PDs have simple configurations, however, they suffer from slow lock speed, narrow acquisition range, periodic input-output transfer characteristic and non-monotonic gain. PFDs have complex configurations but provide high locking speed, wide tracking range, linear, monotonic and non-periodic input-output transfer characteristic. However they suffer from the 'dead-zone' problem.

Chapter 4

Charge Pumps

Phase-locked loops play a critical role in mixed analog-digital systems, such as clock distribution networks and frequency synthesizers [1]. The noisy environment of these systems, mainly caused by the digital portion, imposes challenges on the design of phase-locked loops. Charge pumps that convert digital outputs from phase-frequency detectors into analog control signals for local oscillators are an essential component of phase-locked loops.

In Chapter 2, we explained the benefits of using a CP-PLL over a basic PLL. What concerns us in this chapter is the performance criteria of the charge-pumps and their effect on the performance of phase-locked loops. In clock and data recovery (CDR) applications, the maximum data bandwidth achievable is determined by the clock skew between the internal and external clocks. Clock skew is mainly determined by the non-idealities of charge pumps. Similarly, in frequency synthesis applications, phase-noise can be minimized by increasing the PLL's loop-bandwidth, hence the need for a high-speed CP. Moreover, charge pumps are the dominant block of a phase-locked loop that determines the level of unwanted FM modulation which gives rise to reference spur [13].

Many architectures of charge pumps have emerged recently. A comprehensive review of the architectures of CMOS charge pumps and an in-depth comparison of their characteristics such as, speed, minimum supply voltage, mismatch-induced errors, charge injection and clock

feed-through induced errors, and noise rejection, is presented in this chapter. Section 4.1 introduces the concept of a charge-pump and it's importance to a PLL. Section 4.2 elaborates on the performance evaluators as well as the non-idealities of a charge-pump. Section 4.3 analyzes the basic charge-pump configurations. The more advanced current-steering and differential current-steering charge-pumps are analyzed in Sections 4.4 and 4.5. Miscellaneous charge-pumps are presented in Section 4.6 and the chapter is summarized in Section 4.7.

4.1 Functionality

A CP consists of two switched current sources driving the loop filter, as shown in Figure 4.1. Ideal switching is realized by a three-state phase-frequency detector. The UP and DN signals are non-overlapping.

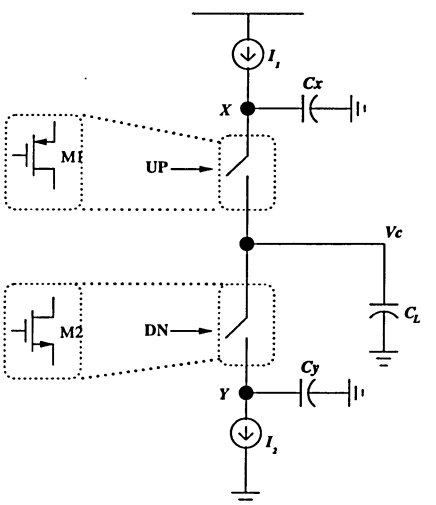

Figure 4.1: Conceptual representation of a charge pump.

Depending on which switch is activated, the CP will either charge or discharge the load capacitor according to Table 4.1. The third state is known as the locked state in which both switches are open and the voltage across the load capacitor remains unchanged.

Table 4.1: Charge Pump Functionality.

UP	DN	Output State V_c
High	Low	Charge
Low	High	Discharge
Low	Low	Locked

In reality, MOS transistors implementing these switches suffer from device mismatches and current-leakage that give rise to clock-skew and reference spurs in the output of the PLL.

These non-ideal effects are explained in greater detail in the following section.

4.2 Non-ideal Effects

As mentioned before, device mismatches and current-leakage result in a phase error that translates into timing jitter or modulation at the VCO output. These errors are analyzed below.

4.2.1 Mismatches

Current Mismatch

The current sources $I1$ and $I2$ in the CP are essentially transistors biased in the saturation region. Non-idealities in the current mirrors or biased transistors causes static current mismatches between the two transistors. The difference between the charging and discharging currents causes a change or ripple in the control voltage V_c at each phase comparison as shown in Figure 4.2 (L).

The current mismatch and consequent ripple voltage translates to a phase-error defined as:

$$\phi_\epsilon = 2\pi \frac{\Delta t_{on}}{T_{ref}} \frac{\Delta i}{I}, \qquad [rad] \tag{4.1}$$

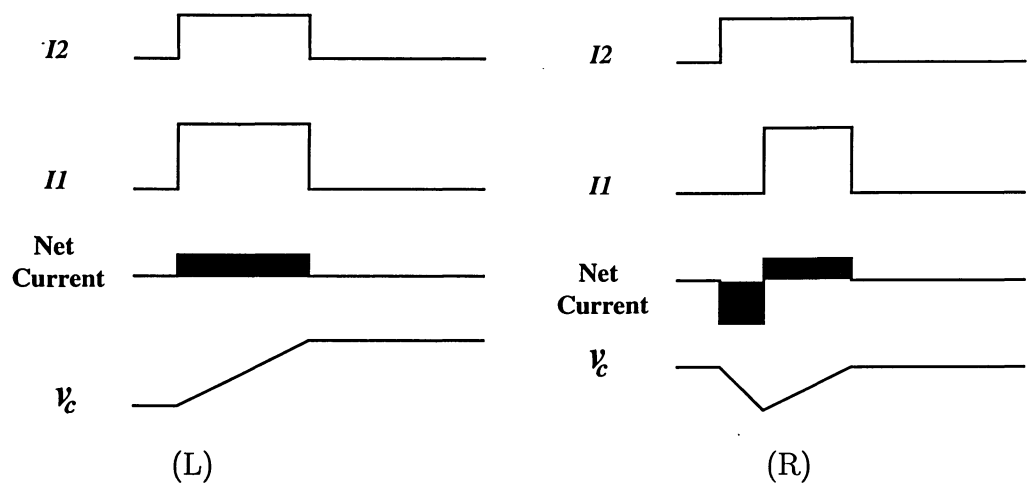

Figure 4.2: (L) Current mismatch, and (R) Pulse-width mismatch.

where T_{ref} is the reference clock period, I is the charge-pump current, Δi is the current mismatch assumed to be greater than zero and Δt_{on} is the turn on time of the PFD. It is important to note that to avoid the dead zone, Δt_{on} has a minimum limit.

For a third order PLL, the phase-error ϕ_ϵ translates to a reference spur P_r(noise) [13] :

$$P_r = 20\log(\frac{1}{\sqrt{2}}\frac{f_{BW}}{f_{ref}}N\phi_\epsilon) - 20\log(\frac{f_{ref}}{f_{p1}}), \qquad [dBc] \tag{4.2}$$

where N is the division value, f_{BW} is the loop bandwidth, f_{ref} is the reference clock frequency and f_{p1} is the frequency of the pole in the loop filter.

Moreover, due to the inhibited low output impedance property of short-channel Mosfets [12], dynamic current mismatch occurs, where the current mismatch Δi varies with V_c. To counter this error, the PLL locks with a finite phase error as shown in Figure 4.2(R) such that the average current per cycle is zero.

Timing Mismatch

The UP signal in Figure 4.1 must be active-low, hence the need for an inverter between the PFD and the charge pump (CP). The timing mismatch that is a resultant of the delay introduced by the inverter produces a phase error and a consequent spur that equals [13] :

$$P_r = 20\log(\frac{f_{BW}}{f_{ref}} N\frac{(2\pi)^2}{\sqrt{2}}\frac{\Delta t_{on}}{T_{ref}}\frac{\Delta t_d}{T_{ref}}) - 20\log(\frac{f_{ref}}{f_{p1}}), \qquad [dBc] \tag{4.3}$$

where Δt_d, the inverter delay is much less than Δt_{on}.

A simple solution to the delay problem is to insert a complementary pass gate before the DN signal to equalize the delay [1].

4.2.2 Switch Induced Errors

Charge Injection (ON $\Rightarrow$ OFF)

Charge injection occurs when a switch moves from an ON state to an OFF state. When a MOS switch is ON, it operates in the triode region. During that time it holds mobile charges in its channel. Upon turning OFF, the charge must flow out of the channel and into the drain and source.

For the DN switch depicted in Figure 4.1, the total charge it holds in an ON state is:

$$Q_{on} = -WLC_{ox}(V_{DN} - V_{tn} - V_Y), \tag{4.4}$$

where W, L, C_{ox}, are the width, length, and oxide capacitance of the DN switch. V_{DN}, V_{tn}, and V_Y are voltage of the DN signal, the threshold voltage of the DN switch, and the voltage at node Y.

When turned OFF, a portion of this charge will flow back to V_Y, while the rest, a fraction K will flow into the load capacitance C_L. The fraction K is the charge injection error. The

voltage-error at the output due to charge injection is calculated by:

$$\Delta V'_{out} = \frac{\Delta Q_{on}}{C_L} = \frac{-KWLC_{ox}(V_{DN} - V_{tn} - V_Y)}{C_L}. \qquad [V] \tag{4.5}$$

Clearly, charge injection introduces a non-linear signal dependent error at the output voltage (V_{tn} has a non-linear relationship with V_Y). It was shown in [14] that if a MOS transistor is turned OFF while in saturation, all the channel charge flows into the source, leaving the drain terminal unaffected (K = 0). As a result, charge injection is avoided. As we shall see later on, positioning the switch relative to the current-sources will determine the severity of charge-injection.

Clock Feedthrough

Clock feedthrough is due to the overlap parasitic capacitances C_{ov}. The error occurs when the fast rise and fall edges of a clock signal at the gate is coupled into the output node via the gate-to-source and gate-to-drain overlap capacitances, causing a sufficient rise of the signal level above the supply voltage. This rise in signal level could forward bias the junction diodes resulting in a electron injection into the substrate that can potentially lead to faulty operation, if it is conducted by a nearby high-impedance node [14][26]. It is important to note that clock feedthrough error is signal independent and manifests itself as an offset voltage $\Delta V''_{out}$ that is calculated according to:

$$\Delta V''_{out} = \frac{-C_{para}(V_{DD} - V_{SS})}{C_{para} + C_L}, \qquad [V] \tag{4.6}$$

where C_{para} is the parasitic capacitances, V_{DD} and V_{SS} are the high and low voltage levels of the clock.

4.2.3 Charge Sharing (OFF⇒ ON)

Charge sharing occurs when switches in a CP move from an OFF state to an ON state. While the input of the CP is the output of a three-state PFD, where-by the UP and DN

switches of the CP can not be ON simultaneously, charge-sharing is the accumulative effect of output voltage non-compliance due to each switch moving from the OFF to ON state. Charge sharing is the resultant of the finite drain capacitances C_Y and C_X of the charging and discharging currents respectively.

The process is best explained in conjunction with Figure 4.1. When the switches are OFF, the voltage at node X and Y are V_{dd} and *ground*, respectively. The output node V_c is floating. When the switches are turned ON, the voltage at node X will decrease and that on node Y will increase, resulting in charge sharing between C_L, C_X, and C_Y, which causes a deviation in the output voltage V_c.

It is important to note, that even if the voltage drop across the two switches is equal, I_1 and I_2 are equal and in-phase and the parasitics at node X and Y are equal, this will not avoid charge-sharing. To see why, let us consider the case where V_c is high (larger than the equilibrium midpoint voltage $V_{dd}/2$) when the switches are OFF. Turning ON the switches will lead to a voltage fluctuation at node Y that is much larger than the fluctuation at node X, this difference in voltage change must be supplied from C_L resulting in charge-sharing.

The effect of charge or current leakage can be mathematically computed. Eq. 7.5 conveys the phase-offset due to charge-sharing and Eq. 7.6 gives the consequent reference spur in a third-order PLL [20].

$$\phi_\epsilon = 2\pi \frac{I_{leak}}{I_{cp}}, \qquad [rad] \tag{4.7}$$

$$P_r = 20\log(\frac{1}{\sqrt{2}}\frac{f_{BW}}{f_{ref}} N\phi_\epsilon) - 20\log(\frac{f_{ref}}{f_{p1}}). \qquad [dBc] \tag{4.8}$$

In later sections, it will become clear that by moving the position of the switches away from the output node, the effect of charge-sharing can be minimized.

To better understand how the structure of a charge-pump can affect the performance due to the non-ideal effects mentioned prior, the following sections will present the basic charge-pumps, current-steering charge-pumps, and differential charge-pumps.

4.3 Basic Charge Pumps

Figure 4.3 presents three single ended charge-pumps, differing only in the location of the switches. From Left to Right, each CP will be analyzed, its defects explained, setting the stage to explain the advantages of using the more advanced CP's.

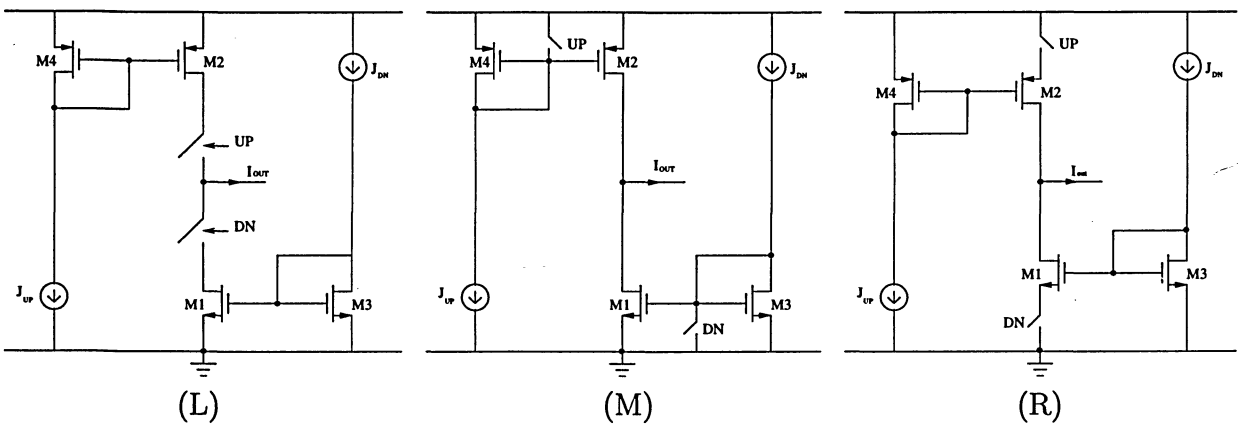

Figure 4.3: (L)Switch at Drain CP, (M)Switch at Gate CP, and (R)Switch at Source CP.

4.3.1 Switch-at-Drain

By concentrating on the middle branch of the circuit in Figure 4.3(L), one should notice its similarity to the conventional CP in Figure 4.1. Clearly the circuit suffers from charge-injection. Moreover, having the switches close to the output, makes the circuit susceptible to charge-sharing at $D1$ and $D2$ and clock feedthrough errors. Mismatches such as current, voltage-drop across the NMOS and PMOS transistors and their parasitics are obvious errors.

4.3.2 Switch-at-Gate

To eliminate the drawbacks of Figure 4.3(L), the switches are moved from the drain to the gate, as shown in Figure 4.3(M) [15]. By changing the switch location, the mirrors and more specifically M1 and M2 are assured to be in saturation, minimizing charge-injection.
This design, however, suffers from reduced switching speed due to the large parasitic capacitances at the gates of M1 and M2. To compensate for speed, the bias currents and hence power-consumption will have to be significantly increased.

4.3.3 Switch-at-Source

The Switch at the Source CP shown in Figure 4.3(R) has less power consumption than the switch at the gate in Figure 4.3(M) without compromising switching speed. By placing the switch at the source, the parasitic capacitance at the gates of M1 and M2, no longer affect the switching speed, and therefore the bias currents can be lowered, consequently reducing power consumption. In addition, given the position of the switches away from the output, charge-sharing is minimized, M1 and M2 are assured to be in saturation, minimizing charge-injection.

To illustrate the effect of charge-sharing and charge-injection, the Switch at Source and Switch at Drain CPs were analyzed using Spectre, and simulated during conditions where charge-sharing and charge-injection occur, as illustrated in Figures 4.4 and 4.5.

4.4 Current-Steering Charge-Pumps

Current-Steering CP's utilize current switches to improve switching speed. The conventional current-steering CP Figure 4.6(L) is composed of the switch at the drain CP with extra switches (M1 and M3). Even though the circuit improves switching speed, the problems that plagued the switch at the drain CP still exist here.

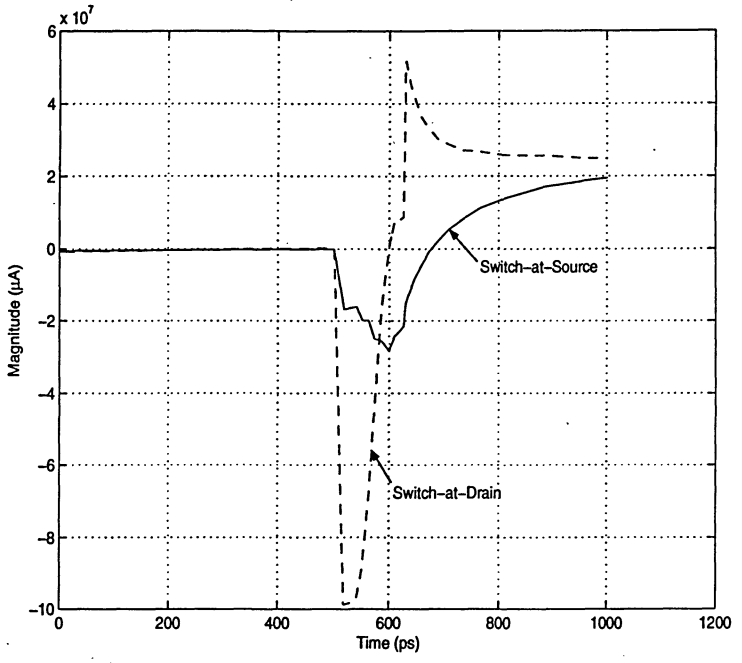

Figure 4.4: Charge sharing comparison.

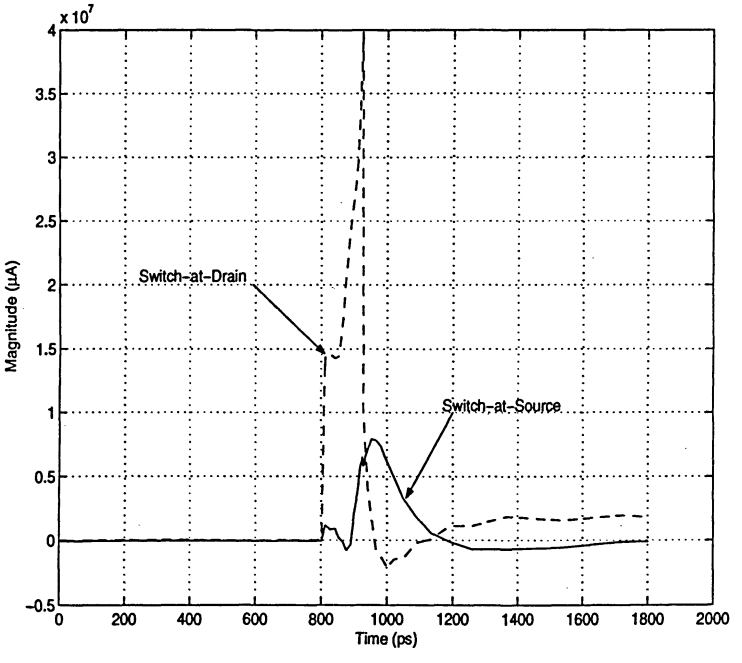

Figure 4.5: Charge injection comparison.

In order to avoid the PMOS and NMOS mismatches of CP in Figure 4.6(L), an NMOS-Switches Only CP Figure 4.6(R) was proposed [16]. This CP, however, suffers from a slow-path node at the gate of transistor M5. That is, when M4 is ON, M3 is OFF, but M6 still conducts current until the parasitic capacitance at the slow-node is fully discharged. Moreover, When M3 is Off, current is wasted in the M4-I_{cp} branch resulting in unnecessary Power-Consumption.

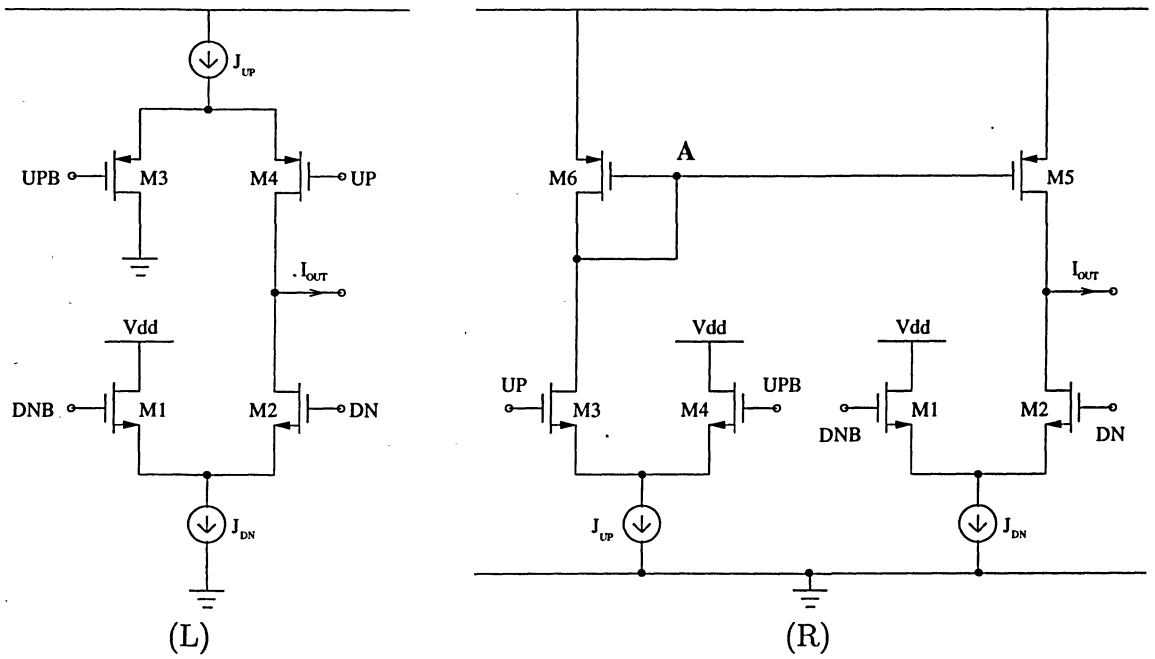

Figure 4.6: (L) Conventional current-steering CP, and (R) NMOS switch only CP.

To solve the slow-node problem, Chang proposed a current-steering CP with a "Pull-Up" mirror as shown in Figure 4.7(L) [17]. The pull-up mirror increases the charging/discharging speed at node A. The drawback of this design is that in order to increase charging speed at A, I_s must be increased. This, however, will decrease the net charge/discharging current of CP, subsequently, the speed of the circuit. In order to maintain speed, one would have to increase I_b and consequently the power consumption. Moreover, when M2 is Off, there is current/power wasted through M1.

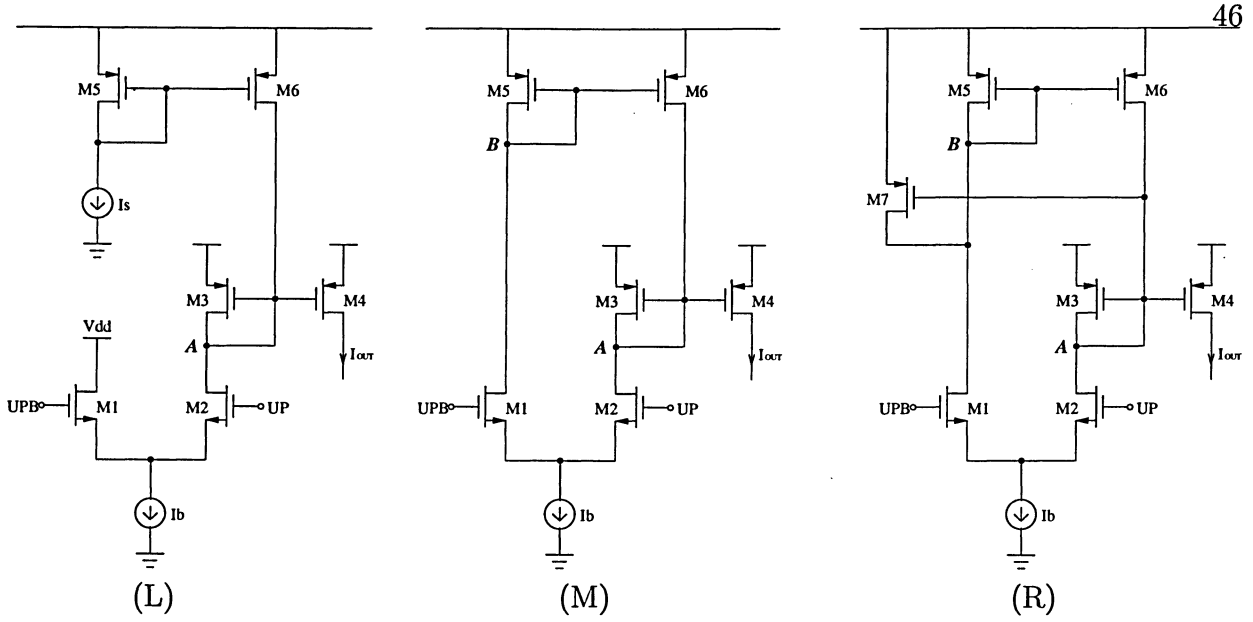

Figure 4.7: (L) Chang's CP, (M) Current reuse, and (R) Current reuse and positive feedback.

Sanchez et all [11] modified Chang's CP by removing the current-source I_s and connecting the drain of M5 directly to that of M1, as shown in Figure 4.7(M). I_b is now used to charge node A and since I_b is greater than I_s, M4 will turn OFF faster. In addition, current/power waste problem was resolved. One disadvantage of this design is the new slow-path node B. To fix this problem, Sanchez proposed using positive feedback by means of a Pull up transistor M7, as shown in Figure 4.7(R). Positive feedback, however, puts a restriction on the input signal UPB, for M1 to stay in saturation, UPB signal must be less than VDD; this requires additional circuitry.

The current steering circuits proposed by Chang and Sanchez were implemented in a 0.13 μm CMOS technology and analyzed using Spectre. Figures 4.8 and 4.9 show the effect of the pull-up transistor on CP.

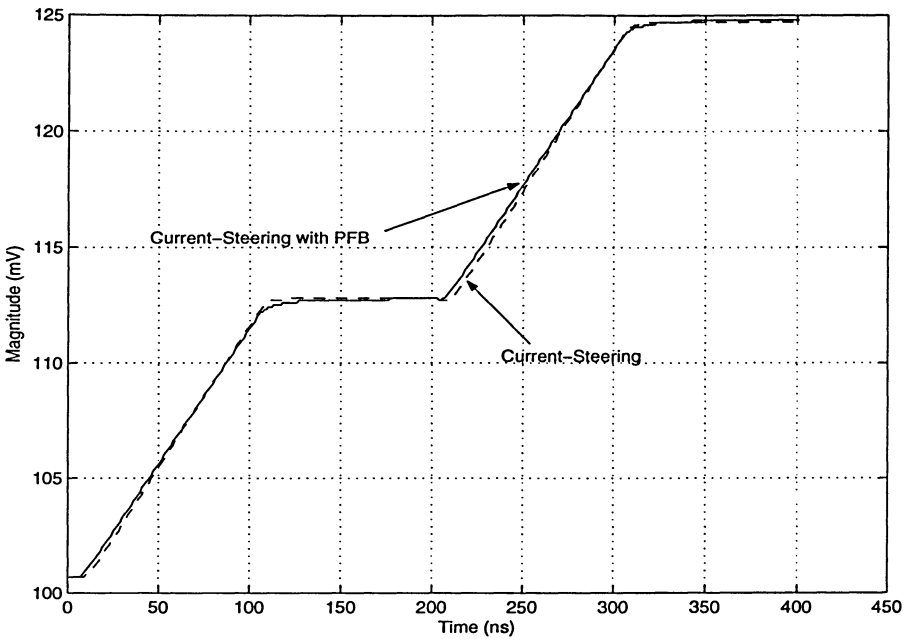

Figure 4.8: Charge up of current-steering CPs.

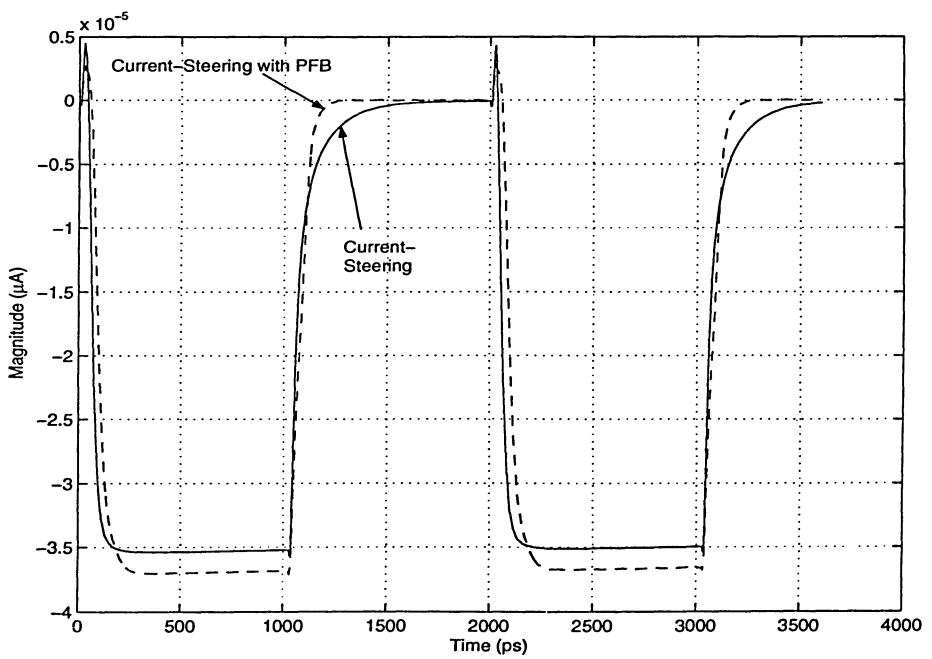

Figure 4.9: Output current of current-steering CPs.

4.5 Differential Current-Steering Charge Pumps

For any IC block, differential circuits will always prove to be more noise immune, and charge-pumps are no exception.

Differential CPs have the following advantages: (i) NMOS and PMOS mismatches will no longer have the same significant effect on the overall performance of CPs. (ii) Due to its symmetric layout, differential CPs are immune to the timing mismatch. (iii) leakage currents are common-mode signals and the output stage is less sensitive to leakage current. (iv) differential CPs provide better immunity to voltage supply, ground and substrate noise [13]. On the negative side, differential CP's consume more silicon area, consume more power, and need a common-mode feedback circuit (CMFB).

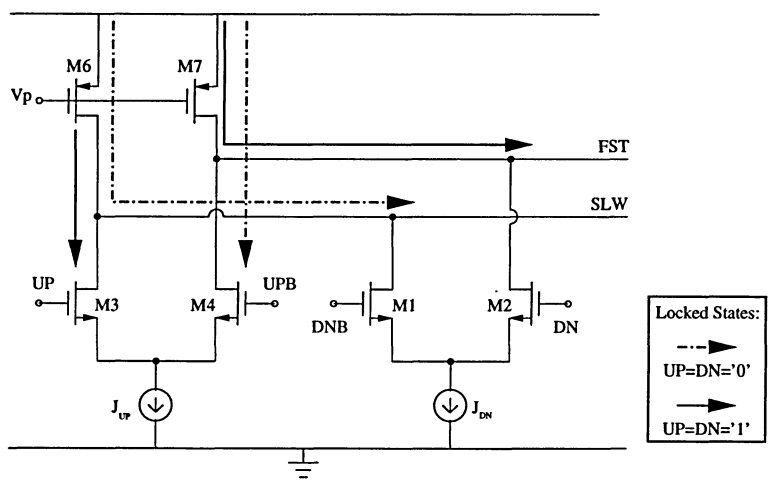

Figure 4.10: Differential current-steering CP.

Figure 4.10 shows a conventional differential current-steering CP. It is important to note that the CMFB circuit takes FST and SLW as input and V_p as its output. The circuit suffers from excessive power consumption during either of the locked states [18].

Figure 4.11 is a Self-Biased differential current-steering CP. In addition to reducing PLL

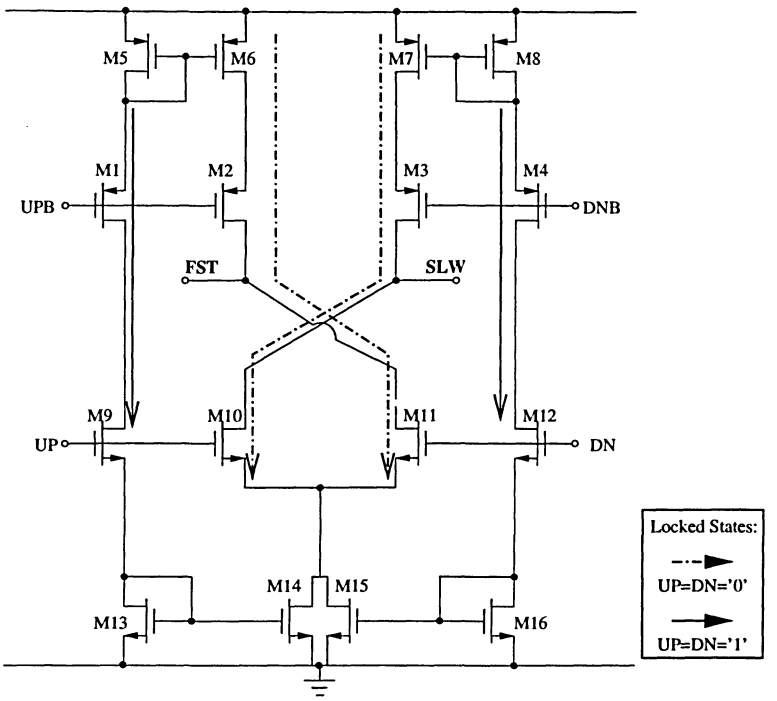

Figure 4.11: Self-biased differential current-steering CP.

noise, the new self-biased CP improves the power consumption, mainly because, when the PLL is locked, the current paths of the CP are blocked.

4.6 Miscellaneous Charge Pumps

This section will present miscellaneous charge-pumps that are not new techniques in themselves but provide some valuable insight on how charge-pump issues have at sometimes been resolved.

4.6.1 Charge-Pump with Active Amplifier

Figure 4.12 is that of a CP utilizing an active amplifier with unity gain to reduce the charge-sharing effect experienced in switch at the drain CP's [19]. The amplifier holds the node voltages of A and B constant when the switch moves from OFF to ON.

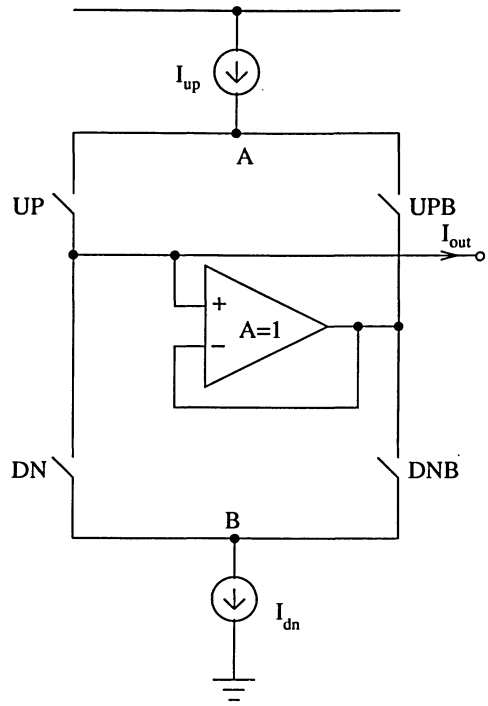

Figure 4.12: Charge-pump with active amplifier.

The disadvantage of this circuit lies in the common-mode input voltage restriction of the opamp. In addition, the op-amps output current, must support I_{UP} and I_{DN}. Such a complex op-amp will make the CP illustrated above not suitable for low voltage operation.

4.6.2 Charge-Pump with Error Amplifier

Most charge-pump topologies try to reduce current mismatch by using cascode configurations to increase the output impedance. As voltages become lower, using cascode configurations to increase output impedance, will no longer be possible. The CP in Figure 4.13 uses a switch at the source CP as one branch in conjunction with a differential amplifier and a reference mirror branch with replica biasing. As long as the amplifier has sufficient gain, the CP output will follow the reference [20].

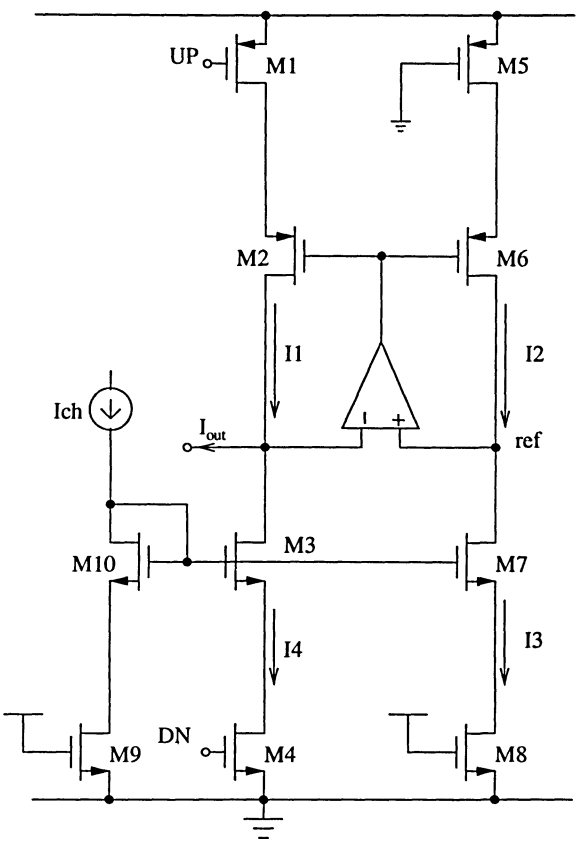

Figure 4.13: Charge-pump with error amplifier.

4.6.3 Charge-Pump with Complementary Switches

The Charge-Pumps in Figure 4.14 are merely Switch at drain and Switch at source charge-pumps with a similar modification. The transistors M1 and M2 in Figure 4.14 (L) are used to discharge and charge nodes P and N when M3 and M4 are inactive [21]. Similarly the transistors M14 and M15 in Figure 4.14 (R) where inserted to reduce switching glitches by providing paths to ground [22].

This method of using complementary switches, although extensively used, does not take into account the fact that leakage at node P is greater than that at node N.

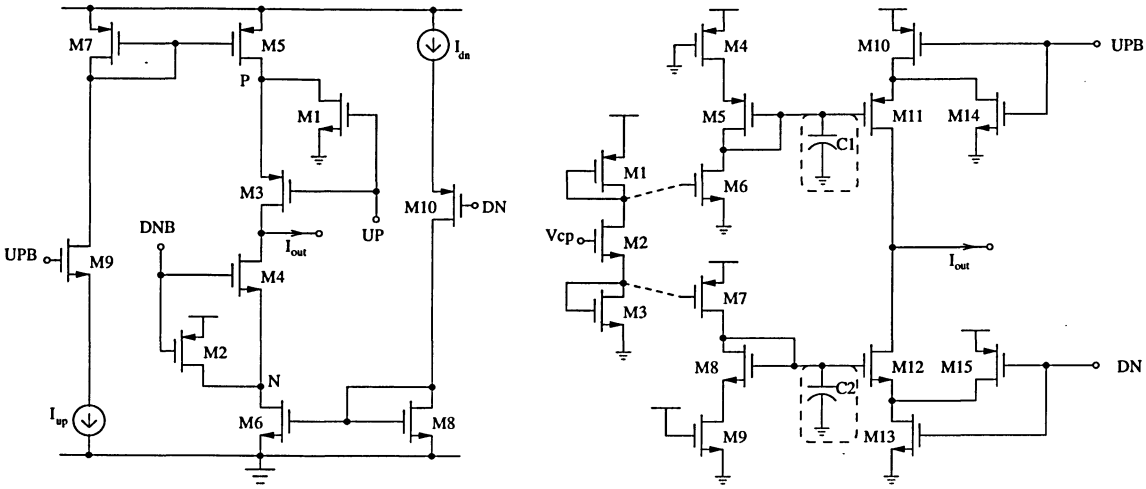

Figure 4.14: (R)Improved switch at drain CP, and (R)Improved switch at source CP.

4.6.4 Charge-Pump with AC Coupling transistors

The Charge-pump shown in Figure 4.15 is a switch at the source CP modified. Other than the cascoded mirrors, this CP utilized replica biasing in M2, M3 and M15 to reduce current mismatch. The other modification is the use of MC1 and MC2 to reduce the charge coupling to the gate and increase switching speed [13].

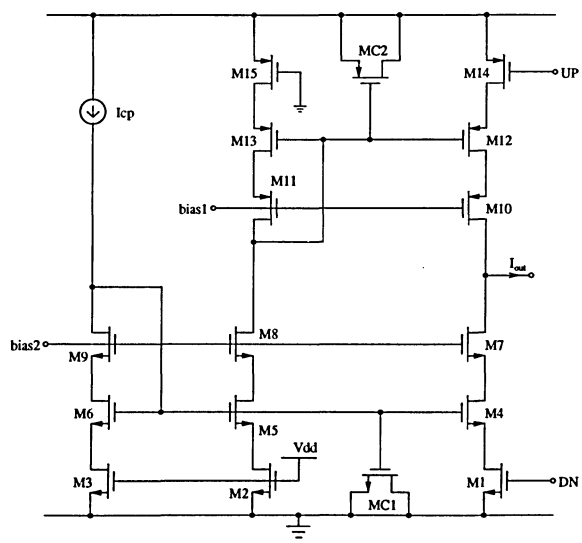

Figure 4.15: Charge-pump with AC coupling transistors.

4.6.5 High-Speed Charge-Pump

The charge-pump in Figure 4.16 is switch at the drain CP with its switches permanently closed. The charging and discharging operation is controlled by the two additional transistors Ma and Mb, the only difference being, is that Ma and Mb are never fully ON or OFF, but they absorb more or less current [23]. This structure avoids switching glitches and is intended for high speed applications.

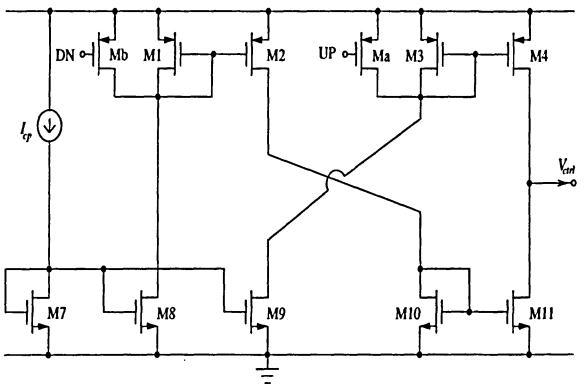

Figure 4.16: High-speed charge-pump.

4.6.6 Fully Balanced Charge-Pump

The CP in Figure 4.17 uses a balanced load and complementary circuits approach to minimize current mismatches [24]. The idea is for each PFD output to see the same number of NMOS and PMOS switches. The use of dummy transistors although useful in reducing current mismatches, requires careful timing of the control signals.

4.6.7 Charge Amplifier Charge-Pump

The CP in Figure 4.18, utilizes a small stand by current to improve switching speed and remove charge-sharing. It is important to note that the standby current does not affect the output current [25]. Also, the UP and DN switches are separated from the output thus reducing clock feedthrough.

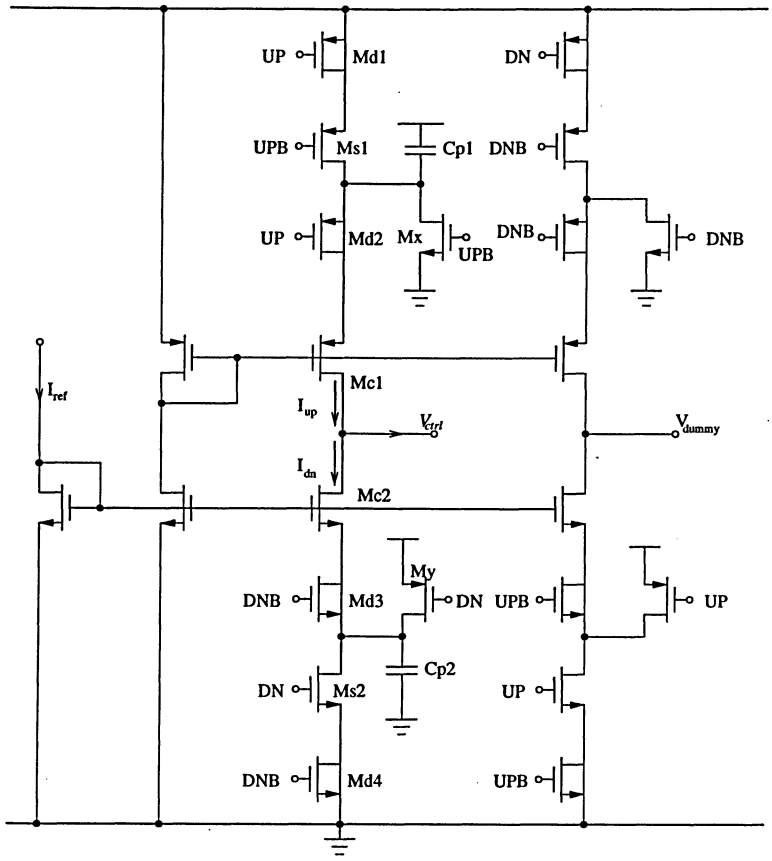

Figure 4.17: Fully balanced charge-pump.

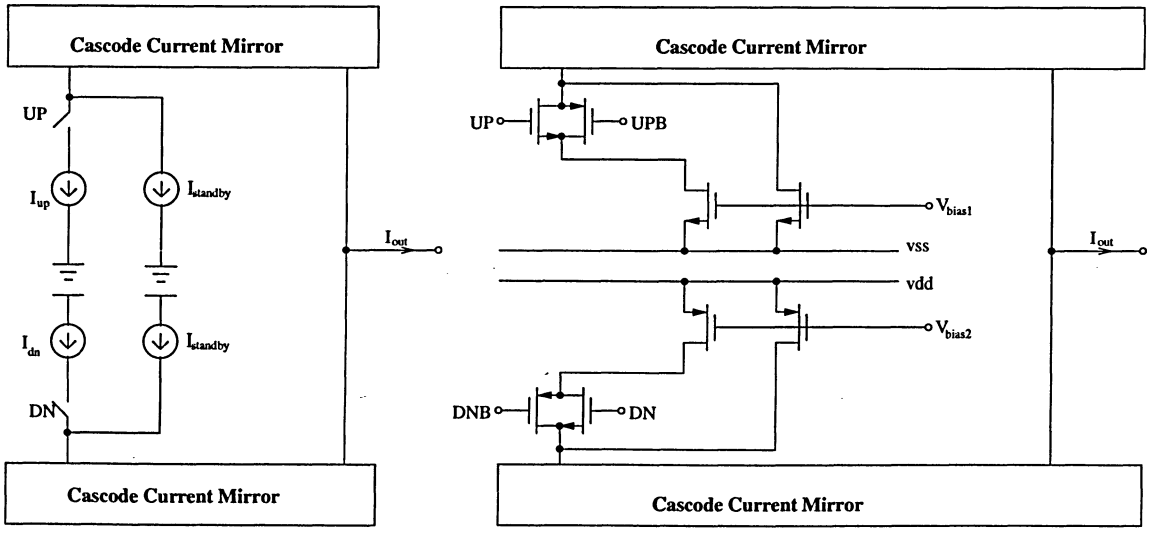

Figure 4.18: Charge amplifier charge-pump.

4.7 Conclusion

The architectures and design considerations of CMOS charge pumps for phase-locked loops have been presented. Basic charge CPs have simple configurations. They, however, suffer from non-ideal effects and low speed. Current-steering CPs have complex configurations but provide high operation speed. Differential current-steering CPs provide better immunity to both power/ground variation and other common-mode disturbances, such as leakage current. These CPs, however, require large silicon areas and common-mode feedback.

This chapter explained in great detail, the importance of the charge-pump to a PLL, it's performance parameters and non-ideal effects. Moreover, a wide array of CP's was presented, and different topologies were compared. In conclusion, it is important to employ the appropriate CP depending on the clock-skew, reference-spur, VCO input range and maximum leakage current criteria.

Chapter 5

Analysis of Supply Noise Sensitivity of VCO Delay Cells

The noisy environment, mainly due to the switching noise generated by the digital portion of these systems, imposes stringent constraints on the design of VCOs, especially phase noise or timing jitter. Although LC tank-based VCOs offer inherent low phase-noise, the compact size, wide tuning range, multiple clock phases, and ease of implementation of ring-VCOs have gained considerable attention most recently. The phase noise or timing jitter of ring-VCOs is a critical Figure of merit quantifying the performance of ring-VCO based PLLs. Recent studies have shown that the dominant source of the timing jitter is the switching noise originated in the digital portion of the systems and coupled to the supply and ground rails of VCO of PLLs. To better understand the effect of the switching noise on the timing jitter, the worst-case timing jitter of various delay cells of ring oscillator-based VCOs is explored in this chapter.

This chapter presents a comparative study of the architecture and timing jitter of the delay-cells of low-voltage CMOS ring-VCOs. In Section 5.1, design considerations, such as noise, single-ended versus differential configuration, linearity and symmetry of load, and the output voltage swing of delay cells are examined in detail. Section 5.2 analyzes the worst-case sensitivity of the delay time of the delay cells (see) and that of the oscillation frequency of corresponding ring-VCO implemented in TSMC 0.18μm CMOS technology using Cadence's

Spectre with BSIM3v3 device models. Simulation results are presented in Section 5.3. The chapter is summarized in Section 5.4.

5.1 Noise Sources

VCO noise sources, can be categorized into two main sources: (i) device noise that consists of thermal noise and $\frac{1}{f}$ flicker noise of MOSFETs, and (ii) supply noise that is due to the switching of on-chip digital circuits. In the following section(s), we will present these noise sources and their effect on the phase noise and jitter of VCOs.

5.1.1 Device Noise

Device noise of ring-VCOs includes wide-band thermal noise and frequency-dependent flicker noise of MOSFETs. The power of flicker noise is significantly higher than that of thermal noise at low frequencies. Due to the nonlinearities of the VCO, low frequency flicker noise is up-converted to frequencies in the vicinity of the oscillation frequency f_{osc}, according to [27]:

$$f_{\frac{1}{f^3}} = f_{\frac{1}{f}} \frac{\Gamma_{dc}^2}{\Gamma_{rms}^2}, \tag{5.1}$$

where $f_{\frac{1}{f^3}}$ and $f_{\frac{1}{f}}$ represent the corner frequencies of the phase noise and flicker noise respectively. Γ_{dc} is the dc value of the *impulse sensitivity function* (ISF), whose value is determined by the magnitudes of the positive and negative lobes of the ISF. Since the slopes of the rising and falling edges of the output waveform of the VCO determine the magnitude of the lobes, an output waveform with equal rise and fall times will not suffer from the up-conversion of $\frac{1}{f}$ noise.

Due to the up conversion of the flicker noise arising from the periodic oscillation of ring oscillators, flicker noise greatly affects the phase noise of ring oscillators, especially those

with tail biasing current sources. The cycle-to-cycle timing jitter ($\Delta\tau$) of a differential ring oscillator due to its intrinsic device noise is given by [36]:

$$\frac{\Delta\tau^2}{T_{osc}^2} = f_{osc}\frac{KT}{I}\cdot\frac{a_v\cdot\chi^2}{V_{on}}, \tag{5.2}$$

where T_{osc} is the oscillation period, V_{on} is the on-voltage, f_{osc} is the oscillation frequency, K is Boltzmann's constant, T is temperature, I is the tail current of the differential pair delay cell, a_v is the voltage gain, and χ is the delay cell noise contribution factor.

We already know that the up-conversion of low frequency flicker noise can be minimized by matching the rise and fall times of the output waveform of the VCO. To reduce the amount of thermal noise that is transformed into jitter, Eq.(5.2) indicates that V_{on} must be maximized. Eq.(5.2) also indicates that better phase noise performance can be achieved by using long and narrow devices that constitute lower threshold voltages in order to minimize gain, maximize the on-voltage and ensure the dominance gate capacitance of the differential pair. This, however, increases with the device capacitance and subsequently lowers the oscillation frequency.

5.1.2 Supply Noise

Supply noise is mainly due to $di(t)/dt$ of the bond wires for the power and ground rails, and is also called switching noise. As current densities increase and power supply voltage decreases, supply fluctuations become critical, especially for mixed analog-digital systems. Maneatis [33] pointed out that supply noise can be classified into (i) *static supply noise* and (ii) *dynamic supply noise.*

Static supply noise arises from the changes in the DC value of the supply, and its sensitivity is measured as the percent difference in the buffer delay at two different supply voltages divided by the supply voltage difference. To see how static supply noise translates to output jitter, let us consider the differential delay cell shown in Figure 5.2(L). The cell is a simple

differential amplifier whose output voltage swing is a function of the loads and tail current. Moreover, the delay of the differential amplifier is a function of the effective load resistance and output capacitance. Linear resistive loads give high static supply noise rejection, since the value of the loads is independent of the supply voltage V_{dd}. In order to control the oscillation frequency, the delay cell should have a mechanism to control the value of the delay. In most designs[1], this is done by varying the value of the load resistors. Adjustable loads are nonlinear, and their effective resistance is a function of the bias current of M0: I_{bias}. Consequently, the static supply noise sensitivity of the delay cell is determined by the sensitivity of I_{bias} to V_{dd}. A variation of the supply voltage will lead to a change in the drain voltage of the NMOS biasing current source M0. Due to the finite output impedance of the current source, a change in the drain voltage of M0 will lead to a change in the value of the current source, and consequently a change in the delay of the cell. Hence, the static supply noise couples to the output through the output impedance of the current-source.

Dynamic supply noise is caused by a transient change in the supply voltage, and its sensitivity is measured as the percent difference in the buffer delay due to an *instantaneous* change in supply voltage divided by the supply voltage difference, minus the static supply sensitivity. Consider the differential delay cell shown in Figure 5.2(L). An ideal differential amplifier will have resistive loads that are independent of the common-mode voltage that carries the dynamic supply noise. In this case, a common-mode shift in the output voltage due to dynamic supply noise can not affect the delay of the cell. Unfortunately, variable loads do not provide a constant output differential resistance. As a result dynamic supply noise will affect the output voltage and a consequent change in the delay. The effect of dynamic supply noise can be limited, by a mechanism that restores the output voltage in a short amount of time. To reduce the recovery time of the output voltage, one can reduce the capacitive coupling to the output. Thus, the dynamic supply noise affects the output via capacitive coupling.

[1]Controlling the delay via the bias current is sensitive to substrate noise coupling to the control voltage.

5.2 Design Considerations

5.2.1 Single-ended and Differential Configurations

Conventional single-ended ring oscillator delay cells are either current-starved or weighted current-adder inverter cells as shown in Figure 5.1(L). Due to the absence of a tail current, these cells exhibit low intrinsic device noise. The full output voltage swing of these cells provides a high signal-to-noise ratio (SNR). These cells, however, have a poor power supply rejection ratio (PSRR).

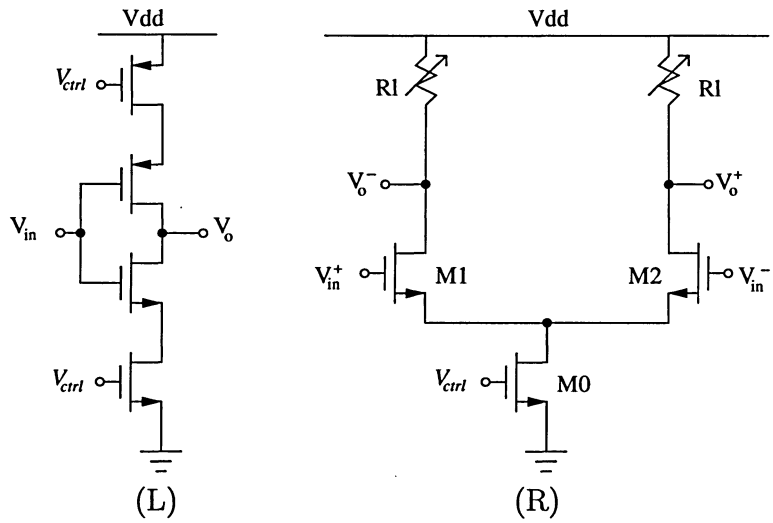

Figure 5.1: Delay cells: (L) Single-Ended, and (R) Differential.

The tail current source of differential delay cells is independent of common-mode variations. Differential delay cells are less sensitive to common-mode voltage variations, such as supply voltage fluctuations. This common-mode noise rejection, however, is limited by the finite output impedance of the tail current source and the linearity of the load. Moreover, due to the existence of a tail current source, differential delay cells experience a limited output voltage swing and a consequent low SNR. Furthermore, the asymmetry of the two branches in differential delay cells, results in an increase in Γ_{dc} and a subsequent increase in the up-conversion of the $\frac{1}{f}$ flicker noise of the tail current source.

5.2.2 Linearity of Load

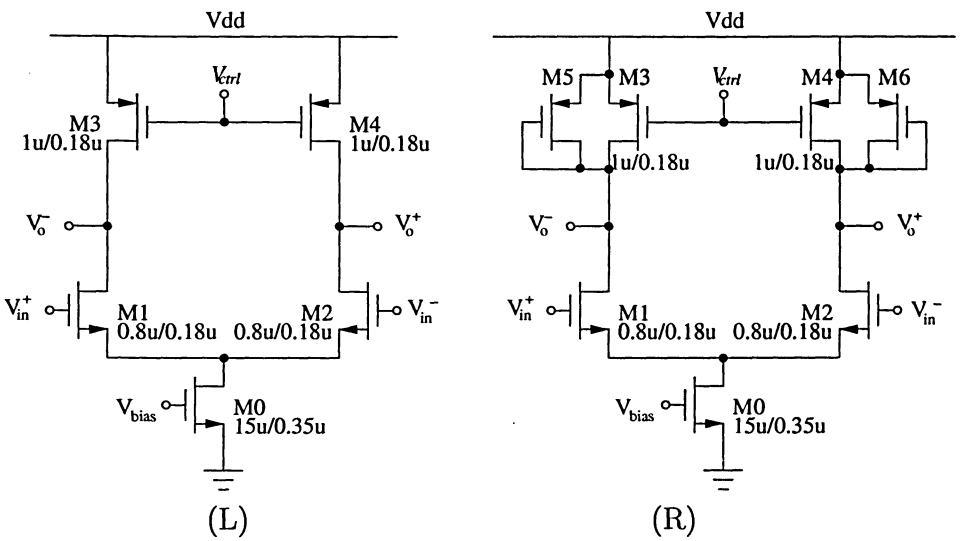

Figure 5.2: Delay Cells: (L) Triode or Current source load, and (R) Symmetric load.

The delay cell with *resistive loads* in Figure 5.1(R) achieves a high dynamic PSRR. In practice, monolithic variable resistors are usually realized using MOSFETs biased in the triode region as shown in Figure 5.2(L). It was shown in [33] that this type of variable resistors exhibits poor linearity once the frequency range is large. In addition, because the effective resistance of triode load resistors is determined by the bias conditions, i.e. $V_{DD} - V_{ctrl}$, the resistance is heavily affected by the fluctuation of the supply voltage. Furthermore, as mentioned earlier this cell suffers from a small output voltage swing.

As compared with variable resistive loads, current source loads[2] have a larger output voltage swing and are less sensitive to the supply fluctuation, owing to the large output impedance of current sources. The disadvantage of using current-source loads is that in order to ensure that the current source MOSFETs are in saturation, the current range of the current source

[2]Figure 5.2(L) with loads biased in saturation.

is usually small, resulting in a small tuning range.

Delay cells with symmetric loads, shown in Figure 5.2(R) combine both current-source and triode loads, to achieve a better PSRR due to improved linearity of the loads. Although not perfectly linear, the I-V characteristic, shown in Figure 5.3, of the symmetric load is symmetric about the center point of the output voltage swing. This symmetry ensures a first-order cancellation of the common-mode noise from the supply voltage [33].

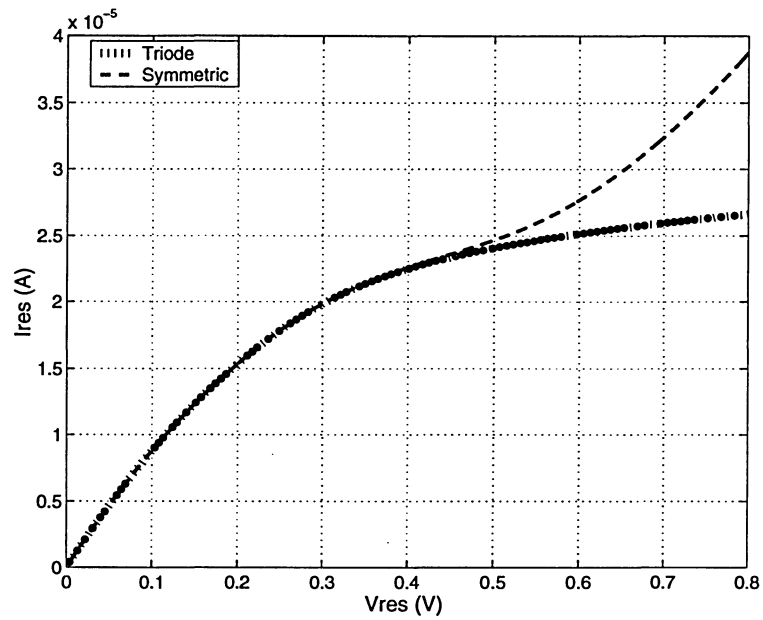

Figure 5.3: IV characteristic of symmetric loads.

5.2.3 Voltage Swing

Delay cells with a full voltage swing offer high SNR but lower oscillation frequencies [29]. It was illustrated by [34, 35] that the single-sided phase noise $L(\Delta\omega)$ of a three-stage ring oscillator is given by:

$$L(\Delta\omega) \approx 10 \log \left[\frac{8F\gamma KTg_{ds0}}{9I_{rms}^2} \left(\frac{\omega_0}{\Delta\omega} \right)^2 \right], \tag{5.3}$$

where $\Delta\omega$ is the offset frequency from the carrier frequency, F is the excess noise factor, γ is a coefficient[3], K is Boltzmann's constant, T is absolute temperature, g_{ds0} is conductance, and I_{rms} is the RMS value for the internal current swing. Low phase noise can be achieved by decreasing F and g_{ds0}, and increasing I_{rms}. I_{rms} can only be increased by increasing current-switching efficiency by increasing voltage swing. F and g_{ds0} can be decreased by minimizing the number of devices with small transistor widths which counters efficient current switching; a trade-off has to be made.

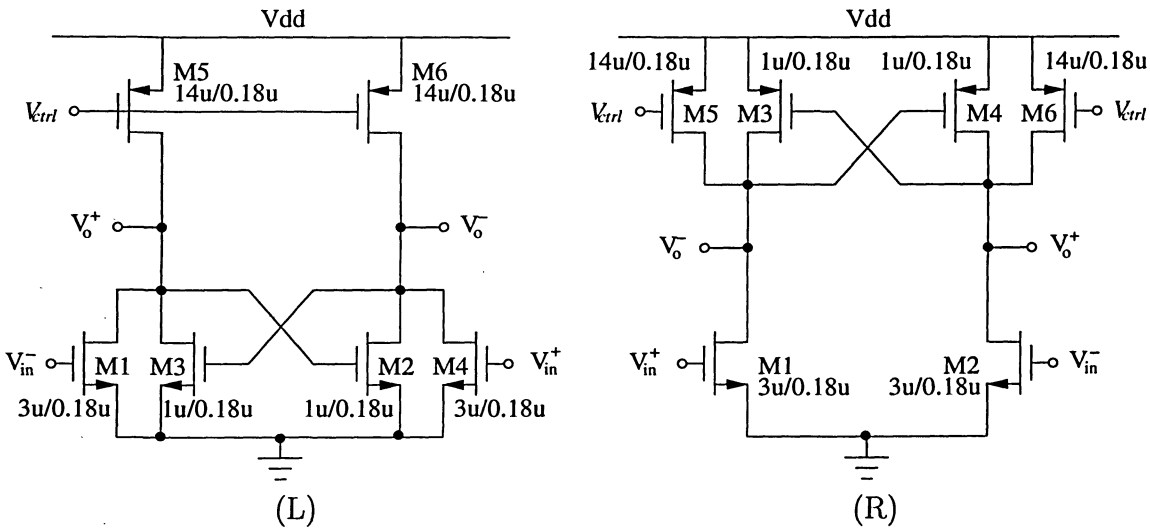

Figure 5.4: Cross-coupled delay cells: (L) P-Latch, and (R) N-Latch.

Figure 5.4 shows full-swing delay cells. These cells employ positive feedback latches, a P-latch [31] or a N-Latch [30], to speed up the transition of the output signal, and to ensure that logic state, once established, is insensitive to dynamic supply voltage variations (high dynamic PSRR). Furthermore, the sharpening of the transition edges reduces the amount of noise converted to timing jitter. As compared the delay cells shown in Figure 5.2, the elimination of the biasing tail current source removes the effect of the up conversion of the flicker noise of the tail current source on the timing jitter. Also, voltage swing limit is no longer

[3] γ should not be confused with the body effect coefficient. The value for γ is dependant on the technology used and the drain-source voltage. The theoretical value is still under research [1]

an issue and the cell has the capability to operate at a lower voltage. Note that in order to break the latch, the input transistors of the cells have to be sufficiently large, resulting in a lower oscillation frequency, therefore the strength of the latch is inversely proportional to the oscillation frequency.

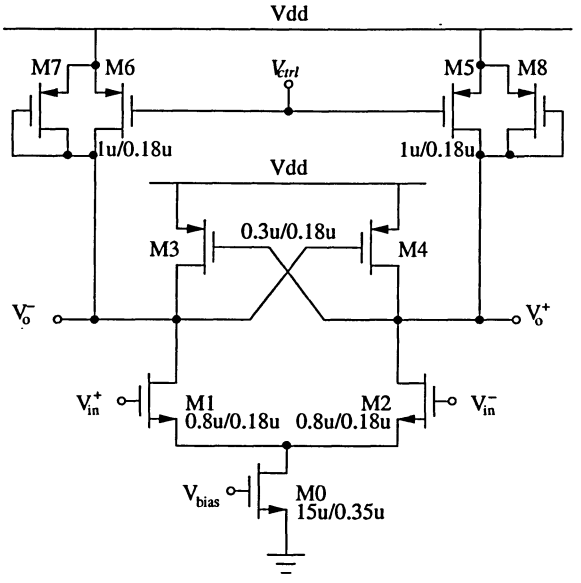

Figure 5.5: Cross-coupled delay cell with symmetric loads.

The delay cell shown in Figure 5.5 [37] takes the advantages of both the symmetric load and cross-coupling, and is capable of achieving a high dynamic PSRR while maintaining reasonable oscillation frequency at the expense of increased intrinsic device noise. The PMOS transistors M3 and M4 exhibit a negative resistance of $-2/g_m$ that increases the symmetry of the load. As a result, the output impedance and subsequently delay, are increased [1].

To further reduce the delay, the skewed delay cell shown in Figure 5.6 was proposed [32]. The negative delay is implemented by applying the premature output of preceding delay cell two-stages-before to skew transistors M5' and M6'. By introducing a negative delay at the input of transistors $M5'$ and $M6'$, the switching time of the loads is reduced. The rise time of the output and hence operating frequency are increased. As a result, timing jitter

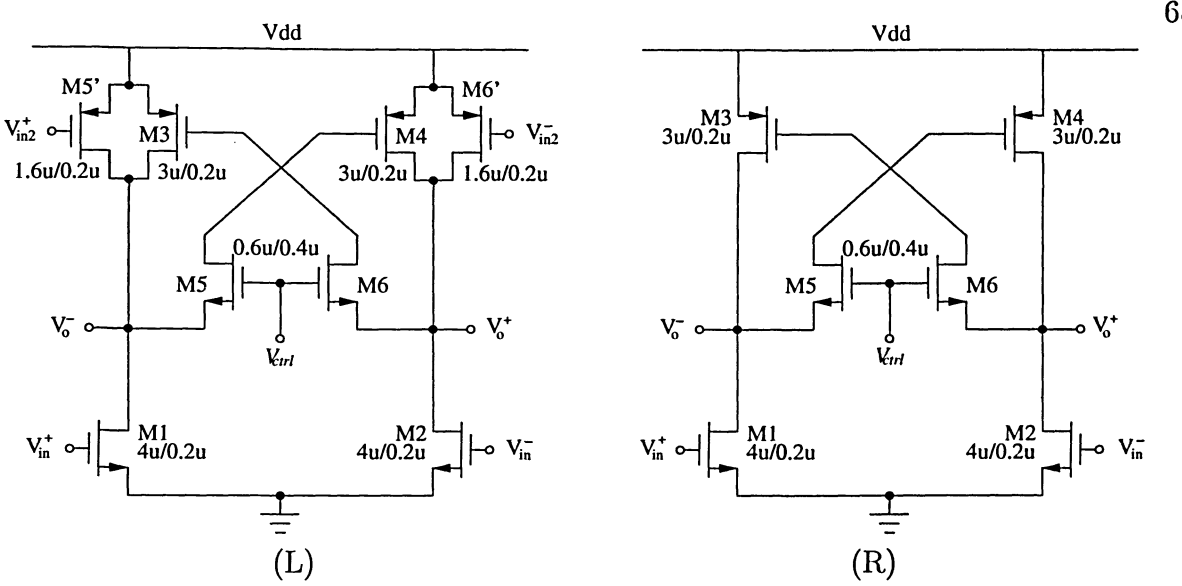

Figure 5.6: Cross-coupled delay cells: (L) without skewed delay, and (R) with skewed delay.

is reduced. Moreover, positive feedback sharpens the transition edges to improve dynamic PSRR. The disadvantage of this delay cell is its high power dissipation when both the input NMOS transistors and skew transistors are ON at the same time.

5.3 Simulation Results

While this chapter is focused on the effect of supply noise on VCO jitter only, it is important to understand the behavior of the PLL in the presence of supply noise. Let us consider first, how a PLL reacts to dynamic supply noise of a VCO. At a constant supply voltage, the PLL will ensure that the oscillation period/frequency is equal to that of the reference signal at the input. A transient change in supply voltage will cause a transient change in the output period/frequency that will lead to a phase accumulation/depreciation at the output. The phase error in the VCO will translate to a phase step between the reference signal and the output of the PLL. This phase step is corrected by the feedback loop of the PLL at a rate limited by its loop bandwidth. The absolute jitter[4] will be equal in magnitude to the phase step.

[4]The difference between periodic jitter and absolute jitter is the reference signal. Periodic jitter is referenced to one period of the VCO output, and absolute jitter is referenced to the PLL input reference

When it comes to static supply noise, a DC change in the supply voltage will have a more significant effect on the absolute jitter. A DC change in the supply voltage will lead to a change in the delay of every buffer stage, and a consequent change in the oscillating period/frequency. This change in oscillation period, will cause an accumulation or depreciation of phase at the output. As opposed to dynamic supply noise that is limited to the duration of the transient, this phase error will accumulate with time until the PLL compensates at a rate limited by the loop bandwidth. The resultant absolute jitter from the static supply noise is measured as the change in the supply voltage multiplied by the static sensitivity, divided by the PLL loop bandwidth. Recalling from Chapter 2 the stability limit (see Eq. (2.41)) to the natural frequency (i.e. loop bandwidth), we can conclude that the effect of the static supply noise is more significant than that of the dynamic supply noise. For the reasons mentioned above, the simulations are strictly for worst case static supply noise sensitivity.

The delay cells presented in this paper have been implemented in TSMC 0.18μm CMOS technology and analyzed using Cadence's Spectre with BSIM3v3 device models. Figure 5.7 shows the test of one delay stage in a multistage ring oscillator with a varying supply voltage ΔV_{DD}. Five-stage ring VCOs employing the different delay cells were implemented, their control voltage was set to the center of the tuning range and the supply voltage was varied by $\pm$ 10% and the corresponding parametric changes were measured.

The rise and fall times, the average propagation delay, the oscillation frequency, and their normalized[5] sensitivity to the supply voltage of these delay cells are analyzed and the results are presented in this section.

To ensure a fair comparison, transistors in the delay cells are sized properly. The inverter

signal.

[5]While sensitivity is measured as a percent change in the respective parameter divided by a 1 *unit* change in voltage, in this thesis sensitivity was measured as percent change in parameter over percent change in voltage, given that *1V* change is extreme in low voltage designs.

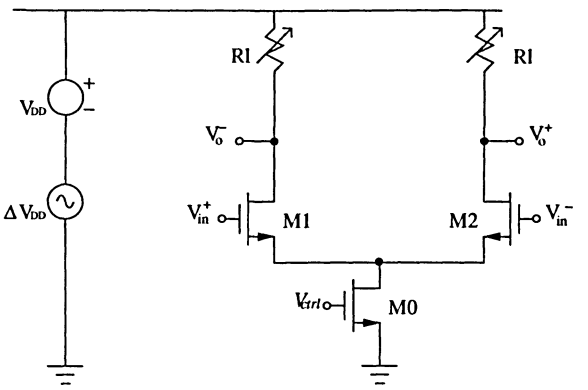

Figure 5.7: Supply Sensitivity test of a differential delay cell.

based delay cells have a full-swing voltage input. The input of differential pair-based cells, on the other hand, has a limited swing to ensure that the loads are in the triode.

The oscillating waveforms of a five-stage ring oscillator with symmetric loads and cross-coupled N-Latch delay cell are shown in Figure 5.8 and Figure 5.9, respectively. One can observe how the differential cell employing symmetric loads is sensitive to a reduced supply voltage due to its limited output voltage swing. As for the cross-coupled N-latch, the compromise between PSRR and oscillation frequency is clear.

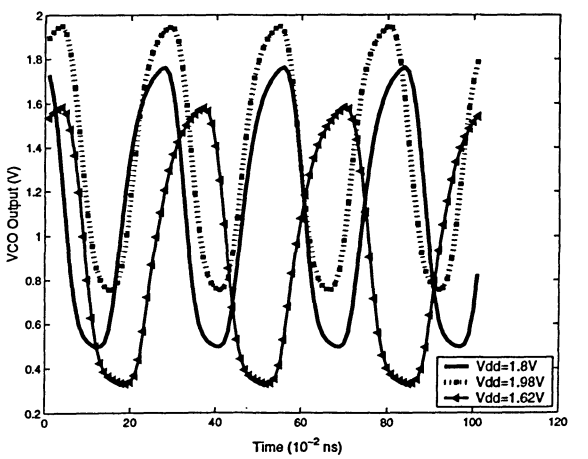

Figure 5.8: VCO output: Symmetric Load.

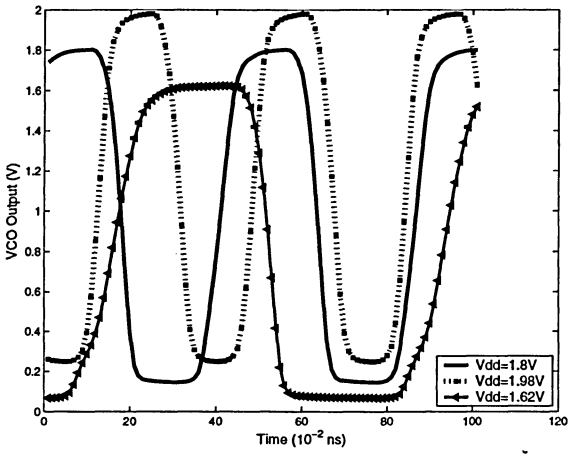

Figure 5.9: VCO output: Cross-coupled N-Latch.

Table 5.1 tabulates the rise time of the delay cells and the normalized sensitivity of the rise time to the supply voltage.

Table 5.1: Rise time of delay cells and its normalized worst-case sensitivity.

Delay cells	Rise Time (ps)		$\frac{\frac{\Delta t_r}{t_r}}{\frac{\Delta V_{DD}}{V_{DD}}}$
	V_{DD}	$V_{DD} \pm 10\%$	
Triode Load	27.80	19.40, 40.40	3.77
Symm. Load	28.10	21.45, 36.40	2.66
Cross Coupled-P	28.60	17.16, 54.15	6.46
Cross Coupled-N	29.50	28.40, 66.73	6.49
Symm. Load-P latch	34.00	26.07, 46.21	2.96
Cross-coupled w/o skew	41.00	33.00, 51.00	2.19
Cross-coupled w skew	31.06	23.13, 51.85	4.62

Table 5.2 shows the fall time of the delay cells and the normalized sensitivity of the fall time to the supply voltage.

Table 5.2: Fall time of delay cells and its normalized worst-case sensitivity.

Delay cells	Fall Time (ps)		$\frac{\frac{\Delta t_f}{t_f}}{\frac{\Delta V_{DD}}{V_{DD}}}$
	V_{DD}	$V_{DD} \pm 10\%$	
Triode Load	33.50	48.80, 22.40	3.94
Symm. Load	29.92	27.79, 27.85	0.70
Cross Coupled-P	29.00	40.00, 22.09	3.08
Cross Coupled-N	40.00	36.26, 20.90	2.85
Symm. Load-P latch	35.80	33.00, 34.75	0.53
Cross-coupled w/o skew	11.00	12.00, 10.28	0.78
Cross-coupled w skew	12.50	15.43, 10.15	2.11

Table 5.3 compares the delay of the delay cells and the normalized delay sensitivity to the supply voltage.

Table 5.3: Average delay of delay cells and its normalized worst-case sensitivity.

Delay cells	Delay (ps)		$\frac{\frac{\Delta \tau}{\tau}}{\frac{\Delta V_{DD}}{V_{DD}}}$
	V_{DD}	$V_{DD} \pm 10\%$	
Triode Load	30.65	34.10, 31.40	0.68
Symm. Load	29.01	24.62, 32.12	1.29
Cross Coupled-P	29.00	28.58, 38.12	1.64
Cross Coupled-N	34.30	32.33, 43.81	1.67
Symm. Load-P latch	34.90	29.53, 40.48	1.56
Cross-coupled w/o skew	26.05	22.50, 30.64	1.56
Cross-coupled w skew	22.05	19.28, 31.00	2.65

Table 5.4 tabulates all the oscillation frequency and the normalized sensitivity of the oscillation frequency to the supply voltage.

Table 5.4: Oscillation frequency of delay cells and its normalized worst-case sensitivity.

Delay cells	Osc. Frequency (GHz)		$\frac{\frac{\Delta\omega_{osc}}{\omega_{osc}}}{\frac{\Delta V_{DD}}{V_{DD}}}$
	V_{DD}	$V_{DD} \pm 10\%$	
Triode Load	3.78	4.39, 3.06	1.76
Symm. Load	3.56	3.91, 3.00	1.27
Cross Coupled-P	3.31	3.85, 2.31	2.35
Cross Coupled-N	2.87	3.51, 2.39	1.95
Symm. Load-P latch	2.99	3.29, 3.06	0.61
Cross-coupled w/o skew	3.67	4.20, 3.16	1.41
Cross-coupled w skew	4.05	4.46, 3.53	1.14

5.4 Conclusions

A comparative study of the architecture and timing jitter of the delay-cells of low-voltage CMOS ring-VCOs has been presented. Design considerations of delay cells have been examined in detail, and the worst-case sensitivity of the delay time of the delay cells and that of the oscillation frequency of corresponding ring VCO have been analyzed. Simulation results presented in this chapter provide an in-depth comparison of the characteristics of the delay cells, in particular, power sensitivity, of low-voltage CMOS ring-VCOs.

Chapter 6

New Active Inductor VCO Delay Cell

Of all the building blocks of PLLs, the voltage controlled oscillator is the main bottleneck in achieving high operation speed. The most exploited configurations of VCOs are ring oscillators and LC-tank oscillators. The compact size, wide tuning range, multiple clock phases, and the ease of implementation of ring-VCOs have gained their popularity. On the other hand, LC tank-based VCOs operate at higher frequencies and offer inherent low phase-noise. However, they suffer from a narrow frequency tuning range. In addition, monolithic spiral inductors have a low quality factor and consume a large inflexible on-chip area. While active inductors generate higher noise than their spiral counterparts, their smaller on-chip area, wide tuning range, and the capability of integration with digital CMOS circuitry makes their use appealing [46].

In order to exploit only the advantages of both the types of oscillators, a four-phase differential ring oscillator with active inductor loads is presented in this chapter. Section 6.1 details the oscillation criteria and design process of oscillator systems. In order to quantify the speed merit of inductive loads, the oscillation speed of a conventional RC ring oscillator is derived and its limitations are analyzed in Section 6.2. Section 6.3 highlights the inductive loading technique and the advantages of using active inductors over passive inductors. Delay cells with slightly different active inductive techniques are scrutinized and the new delay cell is proposed in Section 6.4. A comparative speed analysis is given in Section 6.5, and simulations

and conclusions are presented in Sections 6.6 and 6.7.

6.1 Oscillation Frequency Estimation

In the process of designing an oscillator, certain criteria has to be met. The necessary but not sufficient criteria[1], *Barkhausen criteria*, states that for a feedback system to oscillate, two conditions must be met. The first condition is that the loop gain of the system at the oscillation frequency should be greater than unity. The second condition is that the phase shift of the system at the oscillating frequency should equal [2]-180^o. In order to estimate the delay of a cell, or the speed of the oscillatory system, it is essential that the design process be dissected. For an N-stage ring oscillator compromised of N delay stages, the design process is as follows:

- *Step1:* Identify N, the number of stages, and the transfer function of the delay cell, in addition to the magnitude and phase transfer functions.
- *Step2:* Calculate the phase shift per stage as $\frac{180^o}{N}$ and equate it to the phase shift given in the phase transfer function of the delay cell. The result will be a relation between the oscillation frequency and delay-cell parameters.
- *Step3:* Set the magnitude transfer function of the delay cell greater than unity and simplify the equation by substituting the relation found in *Step2*. This step will give the parametric condition that every delay cell must satisfy for the system to oscillate.

6.2 Oscillation Frequency of RC Ring Oscillator

In this section, we will derive the oscillation speed of a conventional RC ring oscillator. The design process mentioned above is used in conjunction with a linearized model of ring oscillators seen in Figure 6.1.

[1]Meeting the exact criteria is not always sufficient due to parasitics, process and temperature variations.
[2]For a positive feedback system, the condition changes to a phase shift of 360^o.

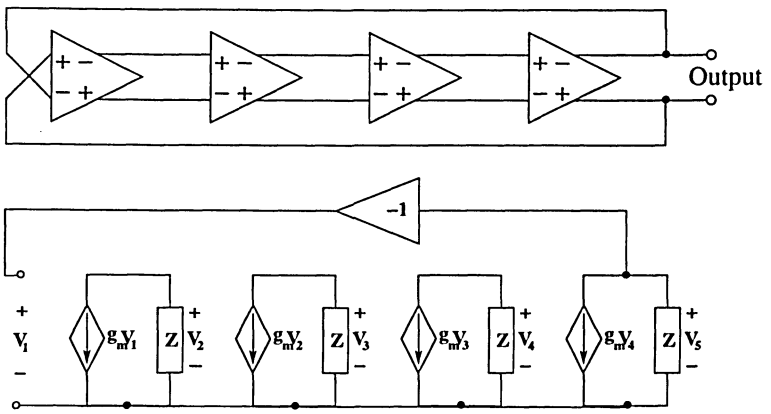

Figure 6.1: Ring oscillator and its linear model.

Depending on the delay stage used, the load Z in Figure 6.1 can be modelled differently. Let us take the basic differential delay cell seen in Figure 6.2(L) as an example. In Chapter 5, we mentioned that the differential delay cell is characterized as having a limited output voltage swing. The VCO frequency can be obtained by using the small signal model of the delay cell seen in Figure 6.2(R).

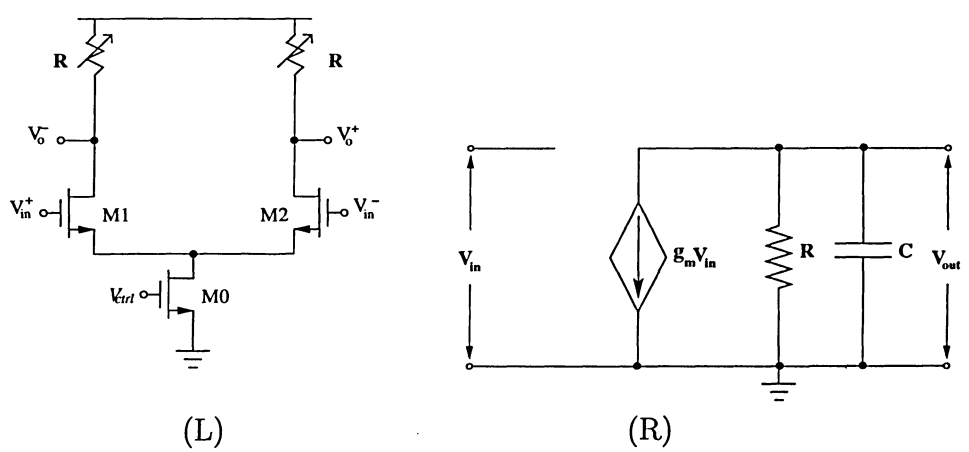

Figure 6.2: (L)Differential Delay cell, and (R) Small signal model of cell.

Noting the similarities between Figures 6.1 and 6.2(R), obviously in the case of the differential pair delay cell, the load Z is modelled as a parallel combination of R and C, where C is the total capacitance seen at the output node, and is equal to the sum of the diffusion capacitance

at the drain of the input NMOS pair, the load capacitance, and the gate capacitance of the next delay stage. By following the design procedure outlined earlier, the transfer function of one delay stage can be obtained from:

$$H(s) = \frac{V_3}{V_2} = g_m Z = \frac{g_m R}{1 + sCR}, \tag{6.1}$$

where g_m is the transconductance of the input transistors M1 and M2.
The phase shift per delay stage can be calculated as:

$$\phi = \frac{-180^o}{N} = -\tan^{-1}(\omega_{osc} RC), \tag{6.2}$$

and for a given N, a relationship can be formulated between ω_{osc}, R, and C.
The magnitude transfer function can be calculated as:

$$\mid H(s) \mid = \frac{g_m R}{\sqrt{1 + (\omega_{osc} CR)^2}}. \tag{6.3}$$

For a given N, by setting the gain to be greater than unity, the following oscillation condition is obtained:

$$R > \frac{1}{g_m}\sqrt{1 + \tan^2(\frac{\pi}{N})}. \tag{6.4}$$

From the above analysis, we can determine the oscillation frequency and oscillation condition (e.g. N=4, $\omega_{osc} = \frac{1}{RC}$, and $R > \frac{\sqrt{2}}{g_m}$). With the combination of the load resistance R and output capacitance C, the transfer function of the delay stage has a single pole. The oscillation frequency can be increased using the following approaches[38]:

- Minimize the total output capacitance seen at the output node.
- Minimize the load resistance.
- Minimize the number of delay stages N.

- Maximize the transconductance per unit capacitance[3] $\frac{g_m}{C}$ of the input transistors and load transistors.

The limitation in reducing the load resistance is given in Eq. (6.4), where a reduction in the load resistance necessitates an increase in the pair's transconductance, to maintain the necessary gain and ensure oscillation. Moreover, an increase in gain will consequently increase power dissipation, phase noise, and reduce the tuning range. In applications such as clock and data recovery (CDR) that demand quadrature outputs, reducing the number of delay stages is not an option.

In order to maximize the transconductance per unit capacitance, one can replace the PMOS transistors with NMOS transistors. Since the transconductance per unit capacitance of NMOS transistors is larger than that of PMOS.

6.3 Active Inductor Loads

Shunt-Peaking [39] is often used to enhance the bandwidth of circuits, by utilizing inductors to tune out the capacitive load. The bandwidth extension is accomplished by the resonance of network formed by the inductor and the load capacitance. In order to get the bandwidth extension effect, the resonance frequency should be near the desired 3-dB frequency [40]. Since the value of the load capacitance is determined by the parasitic capacitance, the inductance value needed for the resonance frequency to be near the bandwidth of the circuit, is high. Using spiral inductors to achieve a large inductance value would consume a large chip area.
Active inductors, on the other hand, are preferred over spiral passive inductors for a number of reasons [42, 41]

- Active inductors are tuneable, while spiral inductors are not.

[3] Also known as the unity gain frequency f_u.

- Passive spiral inductors require a large chip area, while active inductors occupy a significantly smaller chip area.
- Passive spiral inductors contribute significant parasitic capacitance due to their large chip area.
- The value of passive spiral inductance is proportional to the area, whereas the value of active inductance is independent of area.
- Due to substrate and resistive losses, spiral inductors have a low quality factor Q, while active inductors can achieve high Q.
- Passive spiral inductors are prone to high-frequency electro-magnetic noise coupling.

The drawbacks of active inductors are their large DC voltage drop which is a nuisance in low-voltage design, power consumption and noise [44].

6.4 Delay Cells with Active Inductor Loads

Figure 6.3 shows delay cells with active inductor loads. In Figure 6.3(L), transistors M3 and M4 operate in the saturation region, with the drain-gate feedback resistor R_G[4] providing an additional zero in the cells transfer function, which counter balances the simple-pole gain roll-off transfer function. This loading structure suffers from an excessive voltage headroom loss required for the load to exhibit an inductive behavior[7]. This large voltage requirement reduces the circuit's common-mode voltage. Furthermore, this large voltage drop, reduces the voltage headroom needed for the current-control source I_{ctrl}. The consequence is a reduction in the tuning range and the maximum achievable value for I_{ctrl}. In essence, this limits the maximum operation speed of the cells.

The load in Figure 6.3(M), has a similar structure to that of Figure 6.3(L), except that M3 is now an NMOS device with a lower threshold voltage and a higher transconductance per unit

[4] R_G is actually a PMOS device operating in the triode region

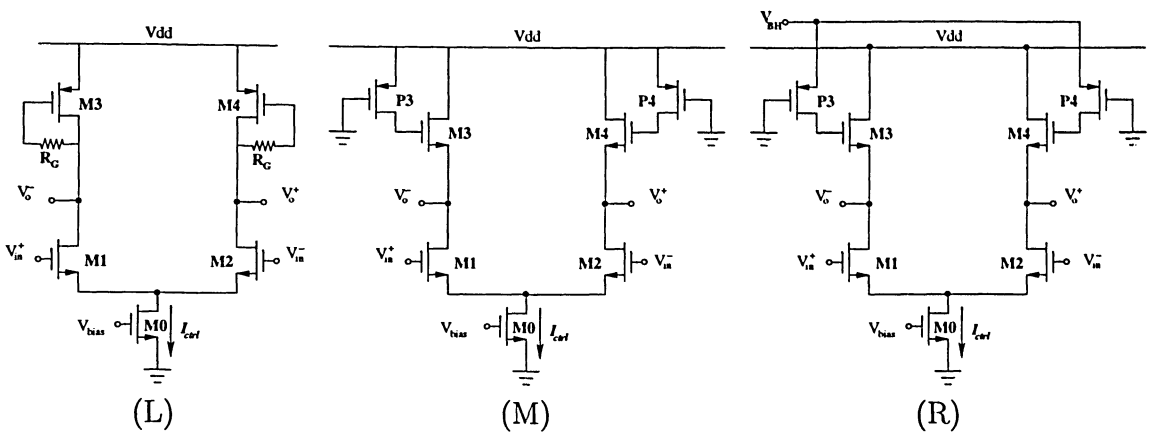

Figure 6.3: Inductive load delay cells: (L) PMOS, (M) NMOS, and (R) NMOS-low voltage.

capacitance. The improvements introduced to the operating frequency and voltage drop by the NMOS active inductor are minor.

In order to reduce the voltage headroom even further, the cell in Figure 6.3(R) biases one terminal of the resistive device P3 at V_{BH}, one threshold voltage above the supply voltage V_{dd}. This reduces the voltage drop across M3 to its gate-overdrive voltage. the disadvantage of this topology is the need for an auxiliary circuit to produce the voltage V_{BH}, and its effect on jitter.

The proposed delay cell in Figure 6.4 utilizes an active inductor load that avoids the restrictions associated with supply voltage and control range. The *current-reused* active inductor [45] employed in the proposed circuit, is composed of devices P1, P2 and biased current-source I_b. Transistors P1, P2 and their biasing current I_b form a shunt-shunt feedback loop that will allow the input impedance to emulate an inductor. At low frequencies, the input impedance ($1/g_{m2}$ divided by the feedback loop gain) is very small because of the shunt feedback. At high frequencies, the loading effect of the gate-source capacitance C_{gs1}, will decrease the feedback loop gain and increase impedance, thereby generating an inductive effect.

This active inductor offers tuning flexibility over the cells in Figure 6.3 by utilizing both

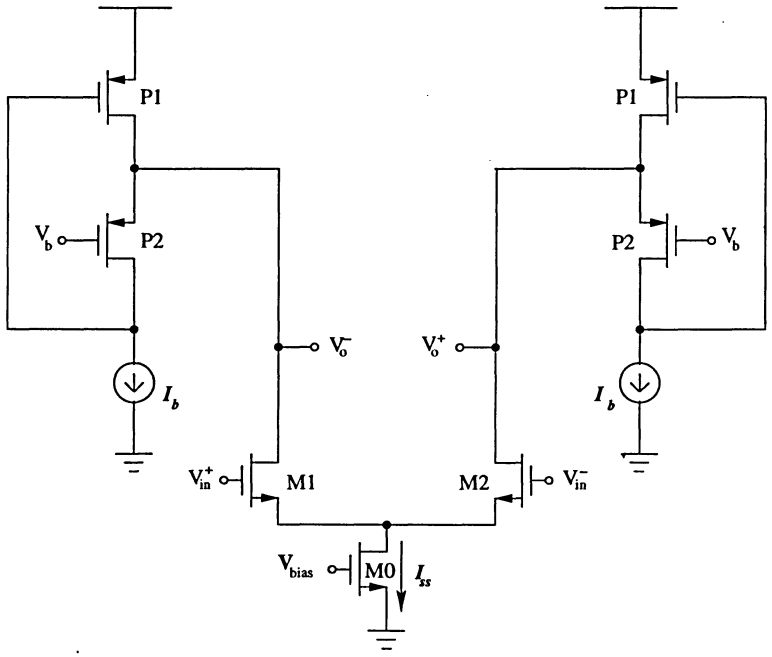

Figure 6.4: Proposed differential delay cell with active inductive loads.

I_b and half of I_{ss}[5]. Moreover, the resonance frequency of this active inductor is $\omega_t = \sqrt{\omega_{t1}\omega_{t2}} = \sqrt{\frac{g_{m1}}{C_{gs1}} \cdot \frac{g_{m2}}{C_{gs2}}}$, where ω_{t1} and ω_{t2} are the unity gain frequencies of transistors P1 and P2, respectively[6]. Given the current-reuse structure, the resonance frequency and inductance value can be tuned by varying the drain currents of P1 or P2 via I_b or I_{ss}. This property allows this active inductor to operate at higher frequencies. Furthermore, the minimum supply voltage needed for this active inductor itself is $max(v_{gs1} + v_{ds}, v_{ds1} + v_{ds2} + v_{dsb})$, which makes its use favorable in low-voltage designs.

The disadvantage of the current-reuse method is the correlation between frequency tuning and quality factor Q tuning. This lack of independence in tuning is evident since Q is given by:

$$Q = \frac{R_p}{\omega_t L_p} \tag{6.5}$$

[5] I_{ss} was referred to as I_{ctrl} in the delay cells of Figure 6.3
[6] See Appendix A.

$$= \sqrt{\frac{\omega_{t1}}{\omega_{t2}}}, \tag{6.6}$$

where R_p and L_p are the values of the equivalent passive resistance and inductance, respectively.

In addition, the Q for this active inductor is quite small given the small value of R_p. With the use of a negative impedance circuit (NIC), Q can be enhanced at the cost of a reduced resonance frequency, increased power consumption and noise. For these reasons, an NIC is not employed in the proposed delay cell.

6.5 Comparative Speed Analysis

Following the same design process, let us now find the oscillation frequency of the proposed delay cell with active inductor loads. The load impedance Z of the proposed cell is the combination of the load capacitance C_L in parallel with the equivalent passive circuit[7] of the active inductor as shown in Figure 6.5.

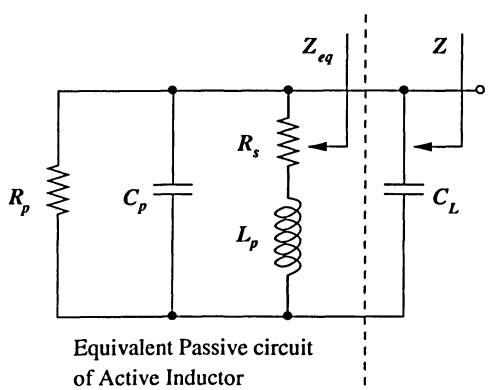

Figure 6.5: Load impedance of delay cell employing active inductors.

The transfer function of the new delay cell can easily be computed:

[7]See Appendix A for a full analysis of the active inductor equivalent circuit and the derivation of equations relating to the equivalent passive components R_p, C_p, L_p, and R_s with the active parameters of P1, P2 and I_b.

$$H(s) = \frac{V_3}{V_2} = g_m Z = g_m \frac{L_p R_p [s + \frac{R_s}{L_p}]}{[R_s + R_p] + s[L_p + R_p C_p R_s + R_p C_L R_s] + s^2[R_p C_p L_p + R_p C_L L_p]}. \tag{6.7}$$

The above transfer function can be simplified further by substituting the equivalent passive components R_p, C_p, L_p, and R_s with the active parameters of P1, P2 and I_b according to the *simplified* equations:

$$C_p = C_{gs2}, \tag{6.8}$$

$$R_p = \frac{1}{g_{m2}}, \tag{6.9}$$

$$R_s = \frac{g_{o2} + g_{o3}}{g_{m1} g_{m2} + g_{m1} g_{o2}}, \tag{6.10}$$

$$L_p = \frac{C_{gs1}}{g_{m1} g_{m2}}. \tag{6.11}$$

From the above equations, we can neglect R_s and simplify the transfer function of (6.7) to:

$$\begin{aligned} H(s) &= \frac{g_m}{C_p + C_L} \frac{s}{s^2 + s\frac{1}{R_p[C_p + C_L]} + \frac{1}{L_p[C_p + C_L]}} \\ &= \frac{g_m}{C_{gs2} + C_L} \frac{s}{s^2 + s\frac{g_{m2}}{C_{gs2} + C_L} + \frac{g_{m1} g_{m2}}{C_{gs1}[C_{gs2} + C_L]}}. \end{aligned} \tag{6.12}$$

The above equation has the form of a bandpass biquadratic transfer function of the form $H(s) = K.\frac{s}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2}$, and whose bode plots are shown in Figure 6.6.

The resonant frequency ω_o and quality factor Q of the delay cell can be detected to be:

$$\begin{aligned} \omega_o &= \sqrt{\frac{1}{L_p(C_p + C_L)}} \\ &= \sqrt{\frac{g_{m1} g_{m2}}{C_{gs1}(C_{gs2} + C_L)}}, \end{aligned} \tag{6.13}$$

$$Q = \sqrt{\frac{g_{m1}}{g_{m2}} . \frac{C_{gs2} + C_L}{C_{gs1}}}. \tag{6.14}$$

For differential oscillators to generate quadrature outputs, the minimum number of stages required for maximum oscillation frequency is N=4. Therefore, the phase shift required per delay stage is -45^o. The frequency dependant phase shift for the given transfer function is given by:

$$\angle H(j\omega) = \frac{\pi}{2} - \tan^{-1}\left[\frac{\omega\omega_o}{Q(\omega_o^2 - \omega^2)}\right]. \tag{6.15}$$

The bode phase plot in Figure 6.6, shows that at -45^o, the oscillation frequency is approximately equal to $5\omega_o$.

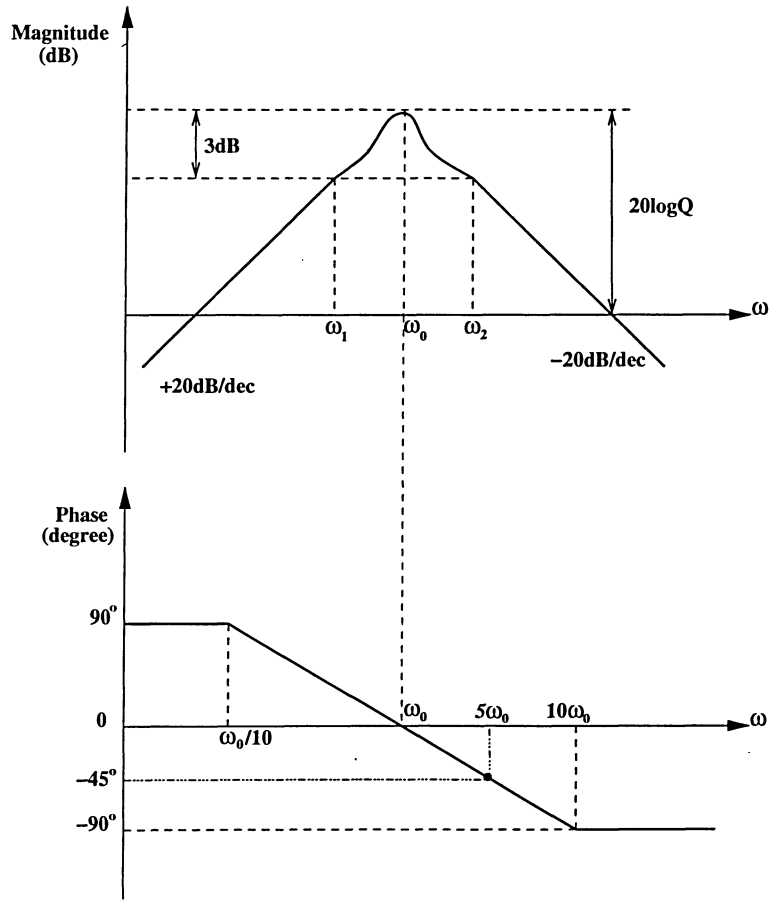

Figure 6.6: Bode plots of $H(s) = \frac{s}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}$.

For comparison purposes, we simplify the oscillation frequencies for both the conventional *RC* delay cell and that of the delay cell with active inductor loads:

$$\omega_{oscL} = 5\omega_o = 5\sqrt{\frac{1}{L_p[C_p + C_L]}} = 5\sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}[C_{gs2} + C_L]}} = 5\sqrt{\frac{k\sqrt{I_b[I_b + I_{ss}/2]}}{C_{gs1}[C_{gs2} + C_L]}}, \tag{6.16}$$

$$\omega_{oscR} = \frac{1}{RC_L} = \frac{g_m}{\sqrt{2}C_L} = \frac{\sqrt{kI_{ss}}}{C_L}, \tag{6.17}$$

where k is a factor determined by the size ratio of the respective loads. ω_{oscL} and ω_{oscR} are the oscillation frequencies of a four stage ring oscillator utilizing an inductive load and resistive load, respectively.

Clearly the oscillation frequency of a four-stage ring oscillator using the proposed delay cell exceeds the frequency of an oscillator using the conventional RC delay cell.

As a final step, let us find the oscillation condition for the proposed delay cell. The magnitude of the transfer function at the oscillation frequency should be greater than unity. The magnitude of the transfer function is:

$$\mid H(j\omega) \mid_{\omega=5\omega_o} = K.\frac{\omega}{\sqrt{[\omega_o^2 - \omega^2]^2 + [\frac{\omega_o\omega}{Q}]^2}}. \tag{6.18}$$

Setting the gain to be greater than unity yields:

$$g_m > \frac{24}{5}\sqrt{\frac{g_{m1}g_{m2}[C_{gs2} + C_L]}{C_{gs1}}}, \tag{6.19}$$

$$g_m > \frac{24}{5}Qg_{m2}. \tag{6.20}$$

6.6 Simulation

A 4-stage ring oscillator was designed using the proposed delay cell of Figure 6.4. The cell was designed in TSMC 0.18μm CMOS technology and analyzed using Cadence's Spectre with BSIM3v3 device models. To estimate the speed benefit of the proposed delay cell, a

4-stage ring oscillator using the conventional RC delay cell was also constructed using the same CMOS technology.

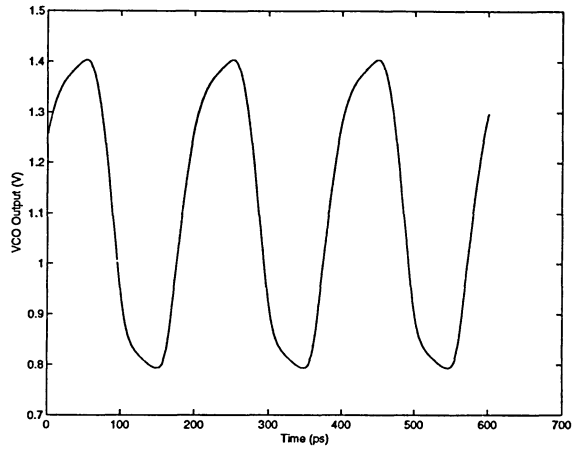

Figure 6.7: Conventional VCO output waveform at 5 GHz.

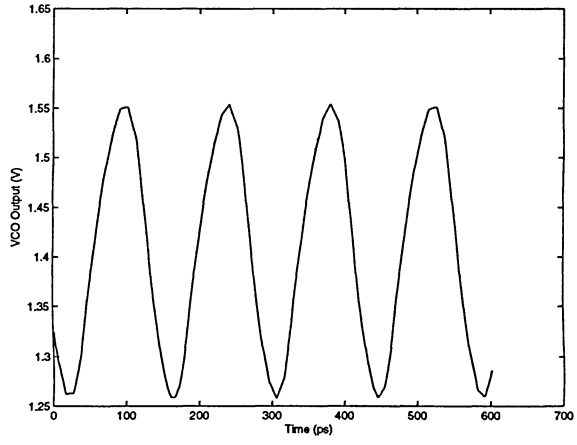

Figure 6.8: Proposed VCO output waveform at 7 GHz.

Figures 6.7 and 6.8 present the simulated output waveforms of a four-stage oscillator utilizing the conventional RC delay cell and the proposed delay cell, respectively. Only one output of the quadrature signals is plotted. The maximum simulated oscillation frequency achieved using the conventional cell is 5 GHz, while the maximum achievable using the proposed delay stage is 7.1 GHz. The new approach offers an improvement of approximately 42% in the

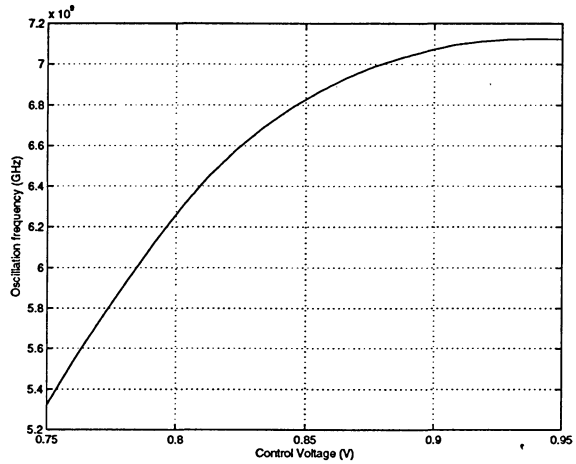

Figure 6.9: Simulated frequency tuning characteristic of the proposed VCO.

operating frequency of the cell.

The frequency tuning range of the proposed delay stage is plotted in Figure 6.9 to be from 5.2 GHz to 7.1 GHz, or equivalently ±15%.

6.7 Conclusions

A high speed ring oscillator suitable for quadrature clock signal generation was constructed. The design achieves frequency enhancement through the use of high frequency low voltage active inductors as loads of the delay cells. The new delay cell proved an improvement in oscillation frequency by about 42%, while exhibiting a tuning range of ±15%.

Chapter 7

Phase-Locked Loop Design

This chapter presents the design procedure for a third-order charge-pump PLL and its simulation results. Before proceeding, it is important to realize that the design procedure is an iterative process. This is mainly due to the difficulty in matching the design parameters of the system level to that of the transistor level.

7.1 Design Procedure

The design procedure presented in this section deals only with the system level parameters.

Of the basic specifications given when designing a PLL is the frequency range, which the VCO tuning range should cover. In our case, we intend to design a PLL that will accommodate the tuning range of the VCO (5.3 GHz - 7.1 GHz). The input reference frequency is given as 6.3 GHz and the power supply is 1.8 V. The steps below illustrate the design procedure:

1. Determine the VCO gain (K_{VCO}) : The VCO gain is a function of the VCO tuning range and the control voltage range which is limited by the power supply and the voltage levels necessary to keep the charge-pump in saturation.

$$K_{VCO} = 2\pi.\frac{VCOtuningrange}{VCOcontrolvoltagerange} = 2\pi.\frac{7.1-5.3}{0.2} = 53, [Grad/sV] \qquad (7.1)$$

2. Determine the damping factor (ζ_{mean}) : The damping factor affects speed and stability. As a compromise, for a third order PLL, ζ_{mean} is often set to 0.707.

3. Determine the natural frequency (ω_n) : Since the loop bandwidth has to be less than one-tenth of the reference frequency, but at the same time, as wide as possible to improve noise performance, a compromise between stability and noise performance, will set:

$$BW_{loop} = (0.75)\frac{F_{ref}}{10} = 2.98, \qquad [Grad/s] \tag{7.2}$$

The natural frequency has a significant effect on loop bandwidth. For a third order PLL whose damping factor equals 0.707, the natural frequency is related to the loop bandwidth according to:

$$BW_{loop} = \omega_n[\sqrt{2\zeta^2+1+\sqrt{(2\zeta^2+1)^2+1}}]; \tag{7.3}$$

$$\omega_n = \frac{BW_{loop}}{2.06} = 1.45, \qquad [Krad/s] \tag{7.4}$$

4. Determine the charge-pump current (I_{cp}) and loop filter capacitor(C_1) : I_{cp} and C_1 can be determined by the relationship between the natural frequency ω_n, and the VCO gain K_{VCO}. It is desirable to have a high I_{cp} which will ensure a high loop gain and consequently a stable system. However, a large I_{cp} will dictate a large capacitor C_1 and consequently a large chip area. Therefore, a design tradeoff in the value of I_{cp} is necessary to ensure a stable yet area-efficient PLL system. However, the VCO designed has an extremely large gain due to the narrow voltage control range, therefore the capacitor size will be small. Lets set $I_{cp} = 2.45$ mA[1] and the Loop filter capacitor is determined by:

$$C_1 = \frac{I_{cp}K_{VCO}}{2\pi\omega_n^2} = 10, \qquad [pF] \tag{7.5}$$

5. Determine the Loop Filter Components (R and C_2) : The Loop filter resistor is used to set the damping factor:

$$R = 2\frac{\zeta}{\omega_n C_1} = 98, \qquad [\Omega] \tag{7.6}$$

[1]While this value is large, it is necessary to ensure practical values for C_1 and C_2

The second loop filter capacitor C_2 is used to suppress the ripple in the control voltage. To maintain the order of the loop filter (second order), C_2 is set to less than one-tenth of C_1:

$$C_2 < \frac{C_1}{10} = 1, \qquad [pF] \tag{7.7}$$

The design process has defined all the key system level parameters. In the following sections, we will present the design and simulation of the different blocks, followed by the simulations of the overall PLL system.

7.2 Phase-Frequency Detector

The PFD circuit used is the one seen in Figure 7.1 and presented in section 3.2.2.

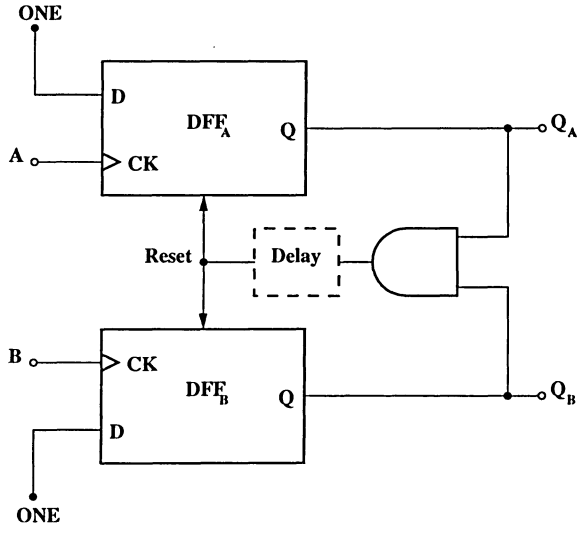

Figure 7.1: Dead-zone free PFD.

The D flip-flops used are optimized specifically for operation in the PFD. Since the data signals D is always set to high, a smaller number of devices in the signal path can be used to increase speed. The schematic of the flip-flop is shown in Figure 7.2. The circuits output Q goes high on a rising edge of the CLK signal. The output signal stays high as long as the reset signal R stays low. For maximum speed, the transistors are sized to the minimum,

while ensuring that effective pull-up and pull-down resistances are matched.

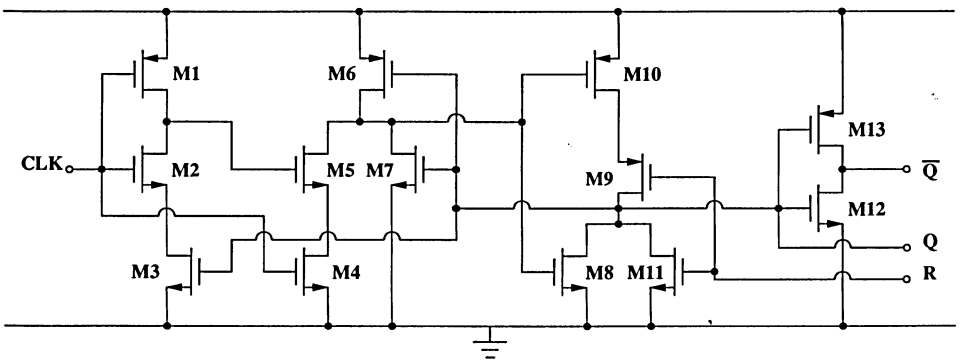

Figure 7.2: Transistor implementation of DFF.

The schematic of the AND gate is shown in Figure 7.3.

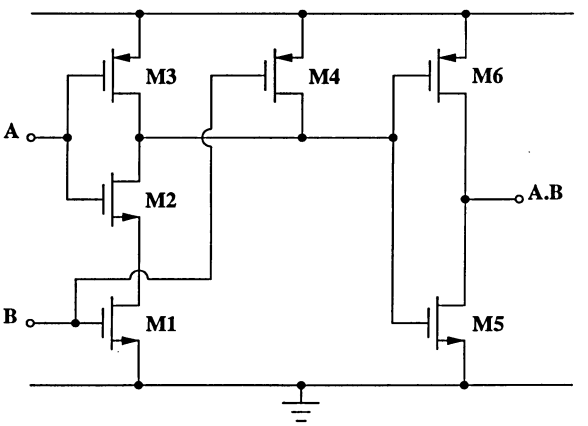

Figure 7.3: Transistor implementation of AND gate.

The PFD was implemented in TSMC 0.18μm CMOS technology and analyzed using Cadence's Spectre with BSIM3v3 device models. Figure 7.4 demonstrates the proper operation of the PFD. The frequency of one of the inputs was set to twice the frequency of the second signal.

Unfortunately, due to the delays in the signal path, this circuit failed to operate at frequen-

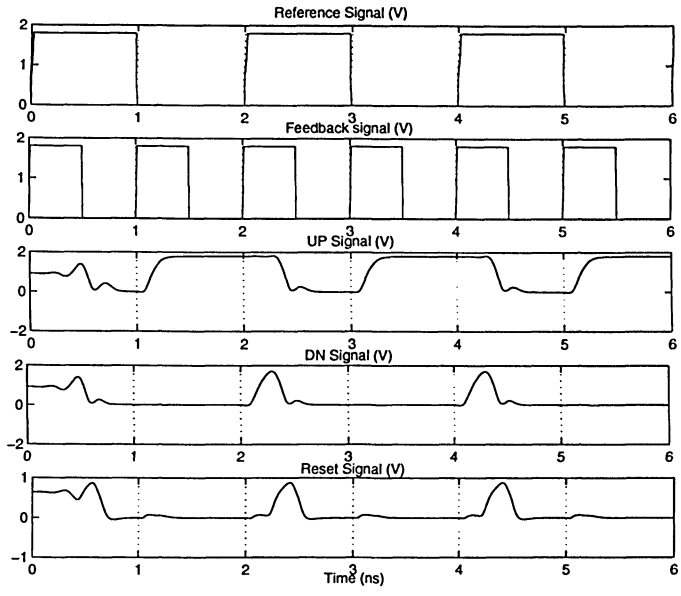

Figure 7.4: Phase frequency detector simulation results.

cies of 7 GHz. Increasing the drive strength of the transistors (M2, M5 and M10) in the signal path can slightly improve the operating speed, but not to the required frequency. Dynamic flip-flops that operate at a frequency of about 6 GHz have been reported in [47], but not implemented in this thesis.

7.3 Charge-Pump

Numerous charge-pump topologies were presented in chapter 4, given the high operating speed, and narrow control voltage range of the VCO, the choice of charge-pump has to take into account fast switching and minimal charge injection. The charge-pump used in our phase-locked loop design is an NMOS switches only current-steering charge pump employing a current-reuse technique presented in Section 4.4 [11]. The full transistor charge-pump circuit is shown in Figure 7.5. The circuit consists of NMOS current switches(M1, M2, M7 and M8), current-mirror loads (M3, M4, M9 and M10) and pull-up current mirrors (M5, M6, M11 and M12) that increase the discharge speed. Given that both the UP and DN signals

use NMOS only current switches, current converter (M13-M14) is used to ensure the proper direction of the discharge current. The addition of the current converter will introduce a new slow node that can slow down the discharge speed of the charge-pump, this problem can easily be remedied via a small discharge transistor [31].

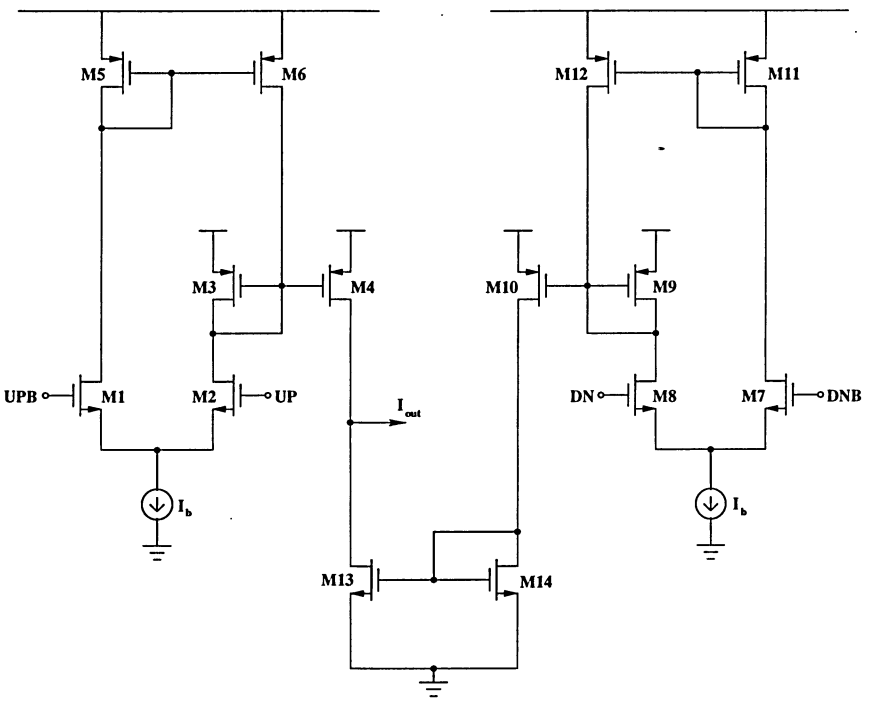

Figure 7.5: Current reuse charge-pump implemented.

Since the designed PFD failed to work at the high frequency of the VCO, an ideal PFD from Cadence "ahdl" library was imported to test the phase-frequency detector and charge-pump combination. The input reference signal was set at 7 GHz, and a second-order low-pass loop filter was used as the output load. Figure 7.6 illustrates the charging of the loop filter, when the feedback signal lags in phase the reference signal. Similarly, Figure 7.7 demonstrates the charging of the loop filter when the feedback signal leads the reference signal.

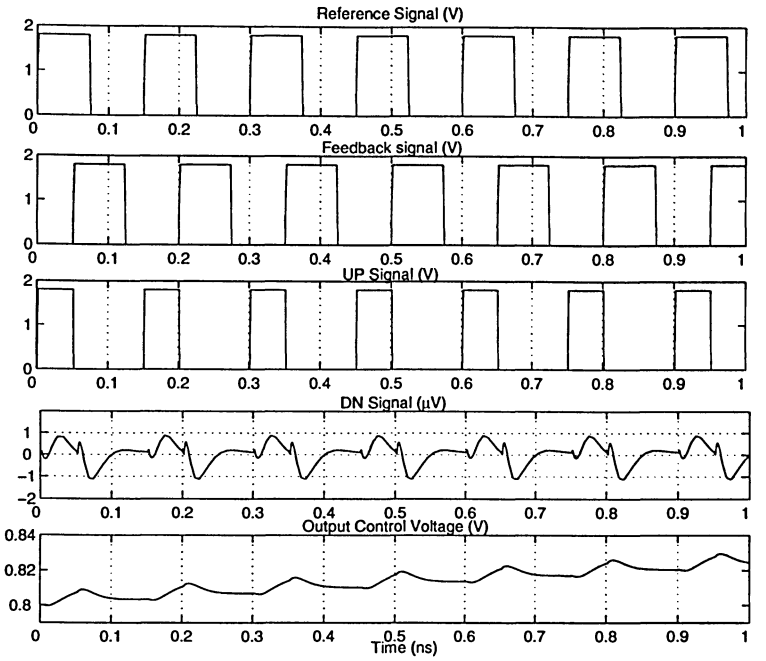

Figure 7.6: The PFD and CP signals when the feedback signal *lags* reference signal.

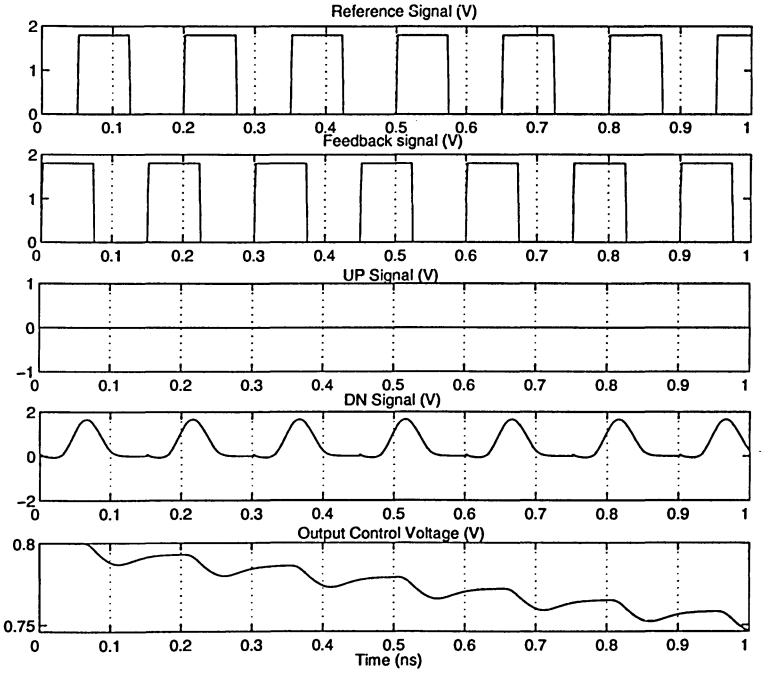

Figure 7.7: The PFD and CP signals when the feedback signal *leads* reference signal.

7.4 Simulation Results

The full charge-pump PLL was constructed and designed in 0.18μm CMOS technology. To simulate the tracking of the PLL, the input reference frequency was set to 6.3-GHz, and the frequency of the oscillator's output waveform was varied to simulate two different cases. In the first case, the frequency of the VCO output was set to 5.7-GHz. Figure 7.8 illustrates how tracking operation of the PLL by increasing the control voltage until lock. Figure 7.9 shows a zoomed in view of both the input reference signal and the VCO output at two different time intervals, before lock and in-lock. In the second case, the frequency of the VCO output waveform was set to lead at 6.7-GHz. Similarly, Figure 7.10 illustrates how tracking operation of the PLL by decreasing the control voltage until lock. Figure 7.11 shows a zoomed in view of both the input reference signal and the VCO output at two different time intervals, before lock and in-lock.

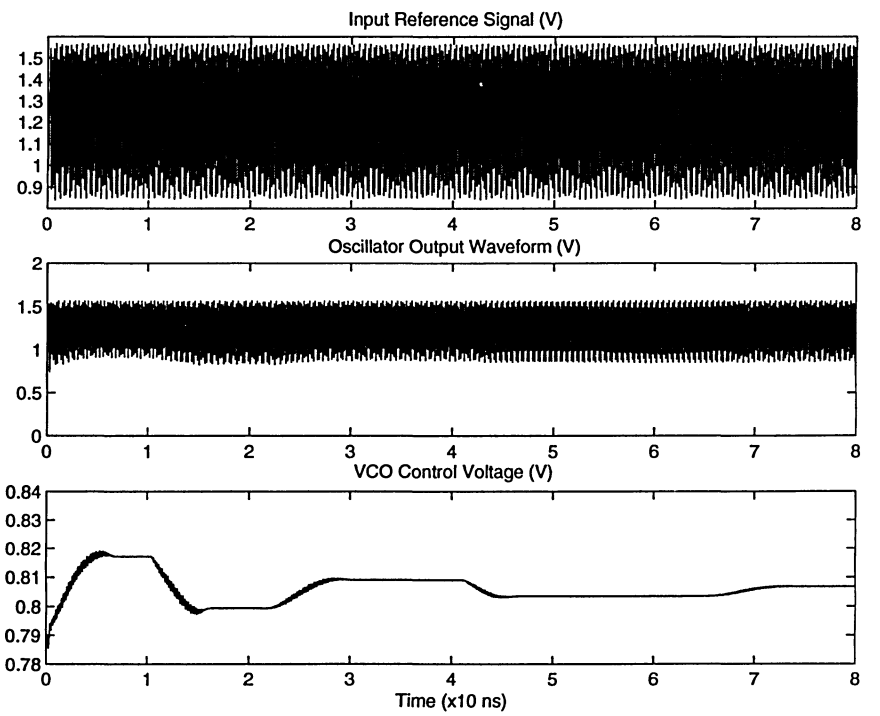

Figure 7.8: *PLL simulation: VCO output lags input reference signal.*

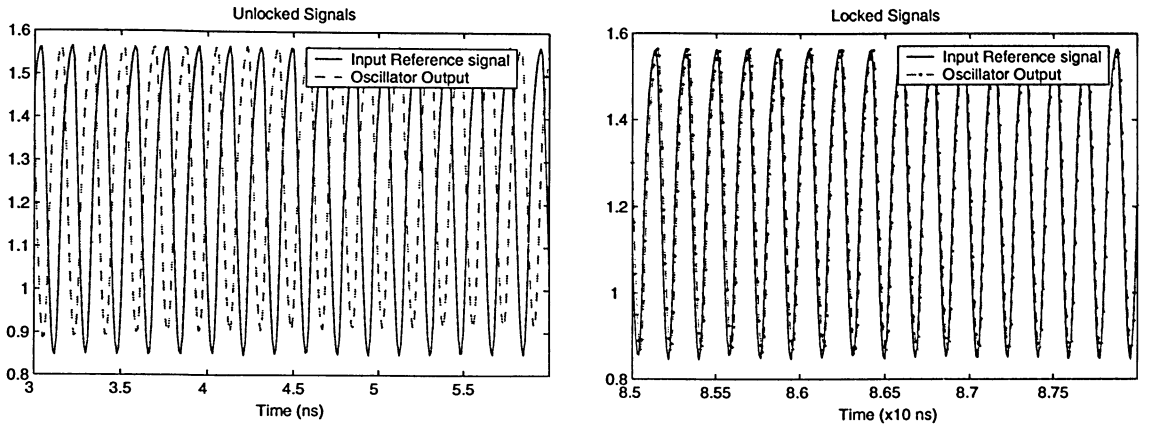

Figure 7.9: Reference and feedback signals before and after lock.

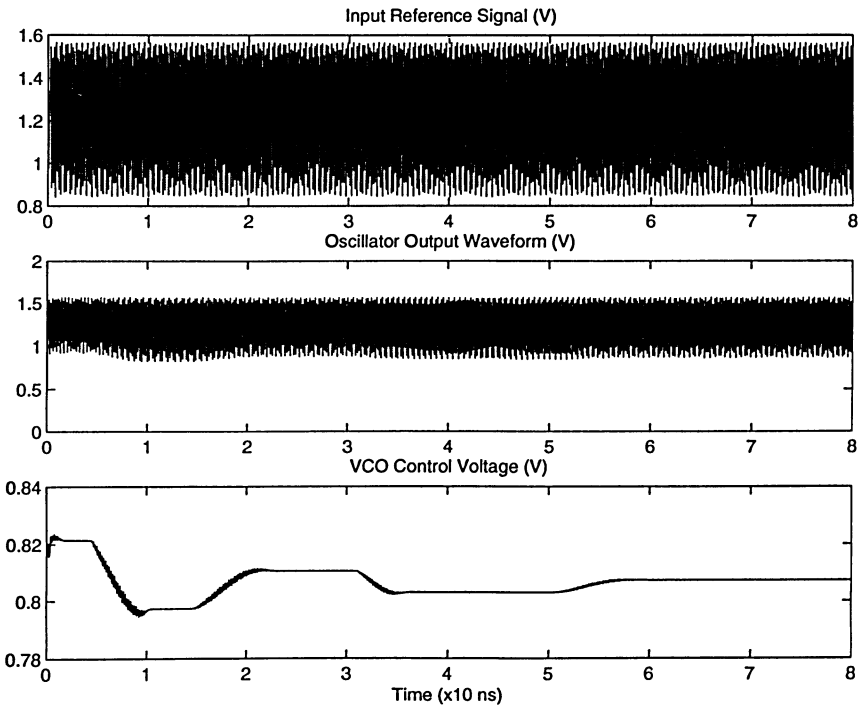

Figure 7.10: PLL simulation: VCO output leads input reference signal.

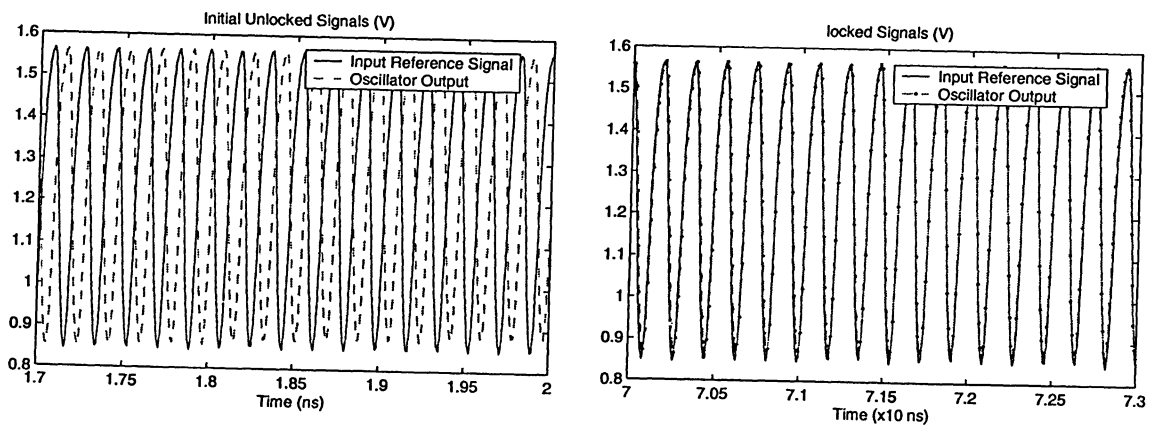

Figure 7.11: Reference and feedback signals before and after lock.

Chapter 8

Conclusions

8.1 Conclusions

In conclusion, a PLL was designed using a new active inductor 6.3-GHz ring oscillator, with a tuning range of $\pm 15\%$ was designed in 0.18μm CMOS technology. The ring oscillator employed active inductor loads that resulted in an improvement of about 42% in oscillation frequency when compared to the conventional resistor loaded ring oscillator.

Moreover, a wide array of charge-pumps was presented, and different topologies were compared and an in-depth comparison of their characteristics such as, speed, minimum supply voltage, mismatch-induced errors, charge injection and clock feed-through induced errors, and noise rejection was established.

Furthermore, a comparative study of the architecture and timing jitter of the delay-cells of low-voltage CMOS ring-VCOs was featured. Design considerations, such as noise, single-ended versus differential configuration, linearity and symmetry of load, and the output voltage swing of delay cells were examined in detail. The worst-case sensitivity of the delay time of the delay cells and that of the oscillation frequency of corresponding ring-VCO were verified.

8.2 Future Research

At high performance levels, demands for low power, high speed and noise efficiency run counter to each other and compromises have to be made. As CMOS technology continues to diminish in size, current densities will increase, supply voltages will drop, and sensitivity to supply voltage fluctuation will become more important. During the course of my research, I came across a many paths that I chose, for the sake of time, not to explore.

Moreover, designing a high frequency VCO as part of a PLL, dictates the design of a PFD capable of operating at similar speeds. As of today, there are no known PFDs that are capable of operating at such speeds in 0.18 μm CMOS technology. Had the application been frequency synthesis, the need for a high-speed PFD would be overcome by a high speed frequency divider or pre-scaler, which introduces a significant amount of switching noise. Researching either of the topics considering the speed and noise trade-offs would prove beneficial.

For one, the output waveforms of the VCO experienced limited swing that is undesirable in certain applications. High frequency differential buffers can alleviate this problem. Designing buffers to operate at the frequency of the VCO is a challenge in itself, given the available 0.18 μm CMOS technology.

Furthermore, while the proposed VCO achieved high frequency operation and had a reasonable tuning range, its gain K_{VCO} was very high, which makes it susceptible to jitter at the control voltage. Further research is required in order to improve the VCO's immunity to variations in the control voltage.

Designing all of the sub-circuits mentioned in the thesis at low supply voltages was challenging, one way to relax the constrain on design low-supply voltage is to bias the body of the active devices in order to lower their threshold voltage levels. Off course doing so will have

significant repercussions on the noise performance of the circuit at hand. Moreover, whether the body bias voltage can be used as a control node to the VCO, is a research path, few have chosen to research and one that might proof to be fruitful.

While the feasibility of using an active inductor was presented, and the results were positive, more research could have gone into analyzing the noise performance of the new delay cell, given the new load structure. How the quality factor Q of the active inductor affects the noise performance of the VCO, is a topic worth further exploration.

Furthermore, several researchers have developed current-mode active filters. Whether an active current-mode filter is a suitable replacement to the conventional passive low-pass filters used in PLLs is a topis worth researching. While clearly, there is benefit in reduction of on-chip area, whether the PLL jitter performance is better or worst due to the active filter has not been researched.

Bibliography

[1] B. Razavi, *Monolithic Phase-Locked Loops and Clock Recovery Circuits,* pp.1-39, IEEE Press, 1996.

[2] B. Razavi, *Design of Analog CMOS Integrated Circuits,* pp. 532 - 569, McGraw-Hill, 2001.

[3] R.E. Best, *Phase-Locked Loops, Fourth Ed.,* McGraw-Hill, 1999.

[4] R. J. Baker, H. W. Li, and D. Boyce, *CMOS: Circuit Design, Layout, and Simulation,* IEEE Press, 1998.

[5] F. M. Gardner, "Charge Pump Phase-lock loops," *IEEE Transactions on Communications,* Vol. 28, No. 11, pp. 1849 - 1858, Nov 1980.

[6] J. Kang and D. Kim, "A CMOS clock and data recovery with two-XOR phase-frequency detector circuit," *Proc. of ISCAS'01, IEEE Int. Symposium on Circuits and Systems,* Vol. 4, pp. 266 - 269, May 2001.

[7] S. Anand and B. Razavi, " A CMOS clock recovery circuit for 2.5-Gb/s NRZ data," *IEEE J. Solid-State Circuits,* Vol. 36, No. 3, pp. 432 - 439, March 2001.

[8] S. Soliman, F. Yuan, and K. Raahemifar, "An overview of design techniques for CMOS phase detectors," *Proc. of ISCAS'02, IEEE Int. Symposium on Circuits and Systems,* Vol. 5, pp. 457 - 460, May 2002.

[9] C.A. Sharpe, "A 3-state phase detector can improve your next PLL design," *EDN Mag,* pp. 55 - 59, September 20, 1976.

[10] M. Soyuer and R. G. Meyer, "High-Frequency phase-locked loops in monolithic bipolar technology," *IEEE J. Solid-State Circuits,* Vol. 24, No. 3, pp. 787 - 795, June 1989.

[11] E.J. Hernandez, and A.D. Sanchez, "A Novel CMOS Charge-Pump Circuit with Positive Feedback for PLL Applications," *Proc. of ICECS' 01, The* 8^{th} *IEEE Int. Conference on Electronics, Circuits and Systems,* Vol. 1, pp. 349 - 352, Sep 2001.

[12] B. Razavi, *Design of Integrated Circuits for Optical Communications,* pp. 260 - 280, Mcgraw-Hill, 2003.

[13] W. Rhee, 'Design of High-Performance CMOS charge-pumps in phase-locked loop," *Proc. of ISCAS' 99, IEEE Int. Symposium on Circuits and Systems,* Vol. 1, pp. 545 - 548, June 1999.

[14] L.Dai and R. Harjani, "CMOS Switched-Op-Amp-Based Sample-and-Hold Circuit," *IEEE J. Solid-State Circuits,* Vol. 35, No. 1, pp. 109 - 113, January 2000.

[15] A. Waizman, "A delay line loop for Frequency synthesis of deskewed clock," *Proc. of ISSCC' 94, IEEE Int. Conference on Solid State Circuits,* pp. 298 - 299, Feb 1994.

[16] J. Maneatis, "Low-Jitter and Process-Independant DLL and PLL based on Self-Biased Techniques," *Proc. of ISSCC' 96, IEEE Int. Conference on Solid State Circuits,* pp. 130 - 131, Feb 1996.

[17] R.C. Chang and L.C Kuo, "A new Low-Voltage Charge-Pump Circuit for PLL," *Proc. of ISCAS' 00, IEEE Int. Symposium on Circuits and Systems,* Vol. 5, pp. 701 - 704, May 2000.

[18] M.S. Lee, T.S. Cheung, and W.Y. Choi, "A Novel Charge-Pump PLL with reduced Jitter Characteristics," *Proc. of ICVC' 99, The* 6^{th} *IEEE Int. Conference on VLSI and CAD,* pp. 596 - 598, Oct 1999.

[19] M. Johnson and E. Hudson, "A Variable delay line PLL for CPU-coprocessor synchronization," *IEEE J. Solid-State Circuits,* Vol. 23, No. 5, pp. 1218 - 1223, Oct 1988.

[20] J.S. Lee, M.S. Keel, S.I. Lim, and S. Kim, "Charge pump with perfect current matching characteristics in phase-locked loops," *IEEE ELECTRONIC LETTERS,* Vol. 36, No. 23, pp. 1907 - 1908, November 2000.

[21] O.T. Chen and R.R.B. Sheen, "A Power-efficient Wide-Range Phase-Locked Loop," *IEEE J. Solid-State Circuits* Vol. 37, No. 1, pp. 51 - 62, Jan 2002.

[22] C.M. Hung and O.K. Kenneth, "A Fully Integrated 1.5-V 5.5-GHz CMOS Phase Locked Loop," *IEEE J. Solid-State Circuits,* Vol. 37, No. 4, pp. 521 - 525, April 2002.

[23] L. Wu, H. Chen, S. Nagavarapu, R. Geiger, E. Lee, and W. Black, "A Monolithic 1.25 Gbit/sec CMOS Clock/Data Recovery Circuit for Fibrechannel Transceiver," *Proc. of ISCAS' 99, IEEE Int. Symposium on Circuits and Systems,* Vol. 2, pp. 565 - 568, June 1999.

[24] J.M. Ingino and V.R. Kaenel, "A 4-GHz Clock System for a High-Performance System-on-a-chip Design," *IEEE J. Solid-State Circuits* Vol. 36, No. 11, pp. 1693 - 1698, Nov 2001.

[25] W.H. Lee, J.D. Cho, and S.D. Lee, "A High Speed and Low Power Phase-Frequency Detector and charge-pump," *Proc. of ASP-DAC' 99, IEEE Conference on Design Automation Conference, Asia and South Pacific,* Vol. 1, pp. 269 - 272, Jan 1999.

[26] Jan M. Rabaey, *Digital Integrated Circuits: a design Perspective,* pp. 227 - 231, Prentice-Hall, 1996.

[27] A. Hajimiri, S. Limotyrakis, and T.H. Lee, "Jitter and Phase noise in Ring Oscillators," *IEEE J. Solid-State Circuits,* Vol. 34, No. 6, pp. 790 - 804, June 1999.

[28] Y. Eken and J.P. Uyemura, "A 5.9-GHz Voltage-Controlled Ring Oscillator in 0.18 μm CMOS," *IEEE J. Solid-State Circuits,* Vol. 39, No. 1, pp. 230 - 233, Jan 2004.

[29] I.C. Hwang, C. Kim, and S.M. Kang, "A CMOS Self-Regulating VCO with Low Supply Sensitivity," *IEEE J. Solid-State Circuits,* Vol. 39, No. 1, pp. 42 - 48, Jan 2004.

[30] J.J. Kim, S.B. Lee, T.S. Jung, C.H. Kim, S.I. Cho, and B. Kim, "A Low-Jitter Mixed-Mode DLL for High-Speed DRAM Applications," *IEEE J. Solid-State Circuits,* Vol. 35, No. 10, pp. 1430 - 1436, Oct 2000.

[31] J. Lee and B. Kim, "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control," *IEEE J. Solid-State Circuits,* Vol. 35, No. 8, pp. 1137 - 1145, Aug 2000.

[32] C.H. Park and B. Kim, "A Low-Noise, 900-MHz VCO in 0.6-μm CMOS," *IEEE J. Solid-State Circuits,* Vol. 34, No. 5, pp. 586 - 591, May 1999.

[33] J.G. Maneatis and M.A. Horowitz, "Precise Delay Generation Using Coupled Oscillators," *IEEE J. Solid-State Circuits,* Vol. 28, No. 12, pp. 1273 - 1282, Dec 1993.

[34] L. Dai and R. Harjani, "Comparison and Analysis of Phase noise in Ring Oscillators," *Proc. of ISCAS' 00, IEEE Int. Symposium on Circuits and Systems,* Vol. 5, pp. 77 - 80, May 2000.

[35] L. Dai and R. Harjani, "Design of Low-Phase-Noise CMOS Ring Oscillators," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing,* Vol. 49, No. 5, pp. 328 - 338, May 2002.

[36] A. Maxim, "Low-Voltage CMOS Charge-Pump PLL Architecture for Low Jitter Operation," *Proc. of ESSCIRC' 02, European Solid-State Circuits Conference,* pp. 423 - 426, Sep 2002.

[37] C.Y. Chang, P.C. Chen, C.Y. Yang, and Y.H. Lee, "The CMOS on-chip oscillator based on level tracking technique," *Proc. of ASIC' 02, IEEE Asia-Pacific Conference on ASIC,* pp. 197 - 200, Aug 2002.

[38] H. Chen and R. Geiger, "Maximizing the Oscillation Frequency of CMOS VCOs," *Proc. of MWSCAS' 00, IEEE Mid-West Symposium on Circuits and Systems,* Vol. 3, pp. 1248 - 1251, Lansing, MI, Aug. 2000.

[39] S. Mohan, M. Hershenson, S. Boyd, and T.H. Lee, "Bandwidth Extension in CMOS with optimized On-Chip Inductors," *IEEE J. Solid-State Circuits,* Vol. 35, No. 3, pp. 346 - 355, March 2000.

[40] Y. Oh, S. Lee, and H. Park, "A 2.5Gb/s CMOS Transimpedance Amplifier Using Novel Active Inductor Load," *Proc. of ESSCIRC' 01, European Solid-State Circuits Conference,* Villach, Austrai, Sep. 2001.

[41] S. Hara, T. Tokumitsu, T. Tanaka, and M. Aikawa, "Broad-Band Monolithic Microwave Active Inductor and its Application to Miniaturized Wide-Band Amplifiers," *IEEE Transactions on Microwave Theory and Techniques,* Vol. 36, No. 12, pp. 1920 - 1924, December 1988.

[42] A. Thanachayanont, "CMOS Transistor-Only Active Inductor for IF/RF Applications," *Proc. of ICIT' 02, IEEE Int. Conference on Industrial Technology,* Vol. 2, pp. 1209 - 1212, Dec. 2002.

[43] A. Worapishet and M. Thamsirianunt, "An NMOS inductive loading technique for extended operating frequency CMOS ring oscillators," *Proc. of MWSCAS' 02, IEEE Mid-West Symposium on Circuits and Systems,* Vol. 1, pp. 116 - 119, Oklahoma, Aug. 2002.

[44] E. Sackinger and W. Fischer, "A 3-GHz 32-dB CMOS limiting Amplifier for SONET OC-48 Receivers," *IEEE J. Solid-State Circuits,* Vol. 35, No. 12, pp. 1884 - 1888, Dec. 2000.

[45] Y. Wu, M. Ismail, and H. Olsson, "A Novel CMOS Fully Differential Inductorless RF Bandpass Filter," *Proc. of ISCAS' 00, IEEE Int. Symposium on Circuits and Systems,* Vol. 4, pp. 149 - 152, Geneva, May. 2000.

[46] H. Xiao and R. Schaumann, "A Low-Voltage Low-Power CMOS 5-GHz Oscillator based on Active Inductors," *Proc. of ICECS' 02, IEEE Int. Conference on Electronics, Circuits and Systems,* Vol. 1, pp. 231 - 234, Sept 2002.

[47] S. Li and M. Ismail, "A 7 GHz 1.5-V Dual-Modulus Prescaler in 0.18μm Copper-CMOS Technology," *IEEE J. Analog Integrated Circuits and Signal Processing,* Vol. 32, No. 1, pp. 89 - 95, July, 2002.

Appendix A

Active Inductor and its equivalent circuit

The CMOS active inductor shown in Figure A.1 is composed of transistors P1, P2 and current source I_b. In order to find the equivalent circuit and equivalent impedance of the active inductor, the small signal equivalent circuit of the active inductor is shown in Figure A.2[1].

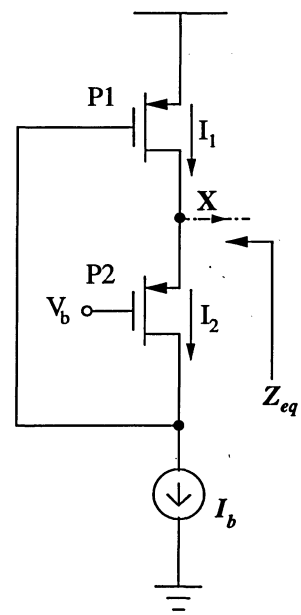

Figure A.1: Active Inductor.

[1]Assuming $C_{gs} \gg C_{gd}$, the gate-drain capacitance can be neglected for simplicity.

The equivalent impedance Z_{eq}, can easily be found by:

$$\begin{aligned} i_{in} &= V_1[g_{o1} + g_{m2} + sC_{gs2}] + g_{m1}V_1 + g_{o2}(V_2 - V_1), \\ &\approx V_1[g_{o1} + g_{m2} + sC_{gs2} + g_{m1}\frac{g_{m2} + g_{o2}}{g_{o2} + g_{o3} + sC_{gs1}}], \end{aligned} \tag{A.1}$$

where g_m, g_o, and C_{gs} are the transconductance, output conductance, and gate-to-source capacitance to the corresponding transistors. g_{o3} is the output conductance of the current source I_b.

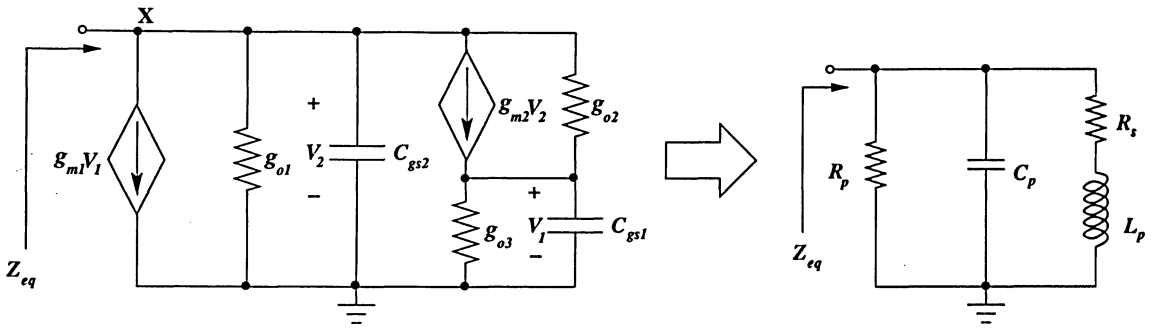

Figure A.2: Small signal equivalent circuit of Active inductor.

Similarly, the equivalent impedance of the passive circuit, can easily be found to be

$$i_{in} = V_{in}[\frac{1}{R_p} + sC_p + \frac{1}{R_s + sL_p}]. \tag{A.2}$$

By mapping the equivalent impedance of equation (A.1) to that of the passive equivalent circuit, we get

$$C_p = C_{gs2}, \tag{A.3}$$

$$R_p = \frac{1}{g_{o1} + g_{m2}}, \tag{A.4}$$

$$R_s = \frac{g_{o2} + g_{o3}}{g_{m1}g_{m2} + g_{m1}g_{o2}}, \tag{A.5}$$

$$L_p = \frac{C_{gs1}}{g_{m1}g_{m2} + g_{m1}g_{o2}}. \tag{A.6}$$

Assuming the transistors exhibit high output impedance, the passive circuit equivalent parameters can be simplified further to

$$C_p = C_{gs2}, \tag{A.7}$$

$$R_p = \frac{1}{g_{m2}}, \tag{A.8}$$

$$R_s = negligible, \tag{A.9}$$

$$L_p = \frac{C_{gs1}}{g_{m1}g_{m2}}, \tag{A.10}$$

whose quality factor Q and resonant frequency ω_t equal:

$$Q = \frac{R_p}{\omega_t L_p}, \tag{A.11}$$

$$= \sqrt{\frac{\omega_{t1}}{\omega_{t2}}}, \tag{A.12}$$

$$\omega_t = \sqrt{\omega_{t1}\omega_{t2}}, \tag{A.13}$$

$$= \sqrt{\frac{g_{m1}}{C_{gs1}}\frac{g_{m2}}{C_{gs2}}} \tag{A.14}$$

where ω_{t1} and ω_{t2} are the unity gain frequencies of transistors P1 and P2 respectively.

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PUBLICATIONS:

1. M. El-Hage and F. Yuan, "Timing jitter analysis of delay cells of CMOS voltage controlled oscillators," 2004 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE2004). Niagara Falls, May 2004.
2. M. El-Hage and F. Yuan, "Architectures and Design Considerations of CMOS Charge Pumps for Phase- Locked Loops,"2003 Canadian Conference on Electrical and Computer Engineering (CCECE2003), Montreal, May 2003.
3. M. El-Hage and F. Yuan, "A fully differential CMOS current-mode preamplifier for Gb/s optical communications," presented at International Conference for Up-Coming Engineers (ICUE 2002), Toronto, Ontario, Canada, April 2002.
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