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Multi-Modular Converters with Automatic Interleaving for Synchronous Generator Based Wind Energy System

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MULTI-MODULAR CONVERTERS WITH AUTOMATIC INTERLEAVING FOR SYNCHRONOUS GENERATOR BASED WIND ENERGY SYSTEM

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Multi-modular converters with automatic interleaving for Synchronous generator based wind energy system

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Abstract

Among different options available for wind energy system, this research is focused on direct driven Synchronous generator based variable speed wind turbines that are connected to power grid via modular converter units. Compared to single full size power converter, modular design has higher reliability/redundancy, better harmonic performance, lower developmental cost and higher efficiency.

Better harmonic performance of modular structure is possible through interleaving which effectively reduces ripple in the output current, enabling use of smaller sized filter components. Focus of this research is to design a controller that can perform automatic interleaving of modular three-phase converters used in above cited wind energy system. Developed control algorithm will have critical decisions carried out by local controllers. With minimum communication overhead the controller will ensure interleaved operation of parallel modules under all conditions. Developed control algorithm is verified through simulation and laboratory testing. Results prove effectiveness of the designed controller.

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List of Acronyms

AC	Alternating Current
DC	Direct Current
DSP	Digital Signal Processor
FFT	Fast Fourier Transform
FSWT	Fixed Speed Wind Turbine
GTO	Gate Turn-Off Thyristor
HVDC	High Voltage Direct Current
MPPT	Maximum Power Point Tracking
P & O	Perturb and Observe
PCC	Point of Common Coupling
PFC	Power Factor Correction
PI	Proportional Integral
PLL	Phase Locked Loop
PMSG	Permanent Magnet Synchronous Generator
PMSM	Permanent Magnet Synchronous Machine
PS-SPWM	Phase Shifting Sinusoidal Pulse Width Modulation
PWM	Pulse Width Modulation
SG	Synchronous Generator
SM	Synchronous Machine
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VRM	Voltage Regulator Module
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
VSWT	Variable Speed Wind Turbine
WECS	Wind Energy Conversion System
WES	Wind Energy System
WT	Wind Turbine

Chapter 1 Introduction

1.1 Background

Depletion of fossil fuel and adverse effects of their usage on the environment are the reasons that initially triggered interest in renewable energy sources. Wind is regarded as the most promising alternative source of energy. As of today wind power generation has emerged as a mature technology. Various electrical designs and control strategies have been developed over the period of years with the purpose of gaining better control over the power of wind.

Review of major trends over the past couple of decades reveal popularity of fixed speed wind turbines till early 90s, offering simplicity of design and robustness as its key features. The main disadvantage of using fixed speed turbines were inadequate control over power quality, increased level of mechanical stress and lack of control over reactive power consumption.

The predominant technology today is that of variable speed pitch control wind turbines which are preferred due to their enhanced power capture capability, better control feature, reduction in mechanical stress and low acoustical noise generation [1]. Previously, main drawbacks of variable speed wind turbines were the additional losses that incur due to the presence of power electronics, complexity of pitch control system and a higher price point. Advancement in the field of power electronics in past few years has led to considerable reduction in price of variable speed wind turbines lending immense room for further growth.

Another factor that has paved path for growth of variable speed technology is direct consequence of increasing penetration of wind power in the grid system. Grid integration of wind energy dictates wind turbine to follow strict grid codes with respect to reactive power supply and fault-ride through capability. Absence of power electronics in wind turbines will make them incapable of meeting grid code requirements and are therefore not pursued in present research work. Focus here is broadly related to wind power systems that involve variable speed wind turbines with power electronics interface.

Two popular options available in case of variable speed wind turbines use (i) doubly-fed induction generator with partial-scale frequency converter in the rotor and (ii) wind turbine coupled with multipole permanent magnet generator and a full-scale power converter. Ease of meeting grid code requirement is what makes use of full size frequency converter more

favourable [1]. Multipole design of the synchronous generator allows low speed operation without making use of gearboxes. This successfully reduces system's maintenance cost which is typically suitable for off shore wind power systems. Gearless construction also makes system light weight and more efficient.

Synchronous generators can be classified based on the method used for generation of rotor magnetic flux. First category i.e Wound Rotor Synchronous Generators (WRSG) uses DC excitation system and as reported in [2], this machine offers possibility of operation close to unity power factor which facilitates application of smaller sized power converters. Permanent magnet synchronous generator has its own set of plus points which are reduced losses because of no DC excitation system and lower maintenance due to the absence of sliprings. In yester years, the biggest disadvantage associated with use of permanent magnet synchronous machines was higher cost of permanent magnets which is less of a concern now due to marked reduction in price for rare-earth magnets in the last few years [3]. Also there has been improvement in characteristics of magnetic material which has led to an increased interest in multipole PMSG based wind energy systems by manufacturers like Jeumont, Lagerwey, Vensys, Leitner and MTorres [2], [4].

Two different converter topologies are popularly used in PMSG based wind energy systems. One of the set-up uses front-end diode Rectifier, DC-Chopper, DC-link, and an inverter while the other is combination of back-to-back PWM converter system which is connected via DC link capacitor [3]. Problem associated with the first versions is its lack of control over generator's power factor and high harmonic distortion in generator side current which causes reduction in efficiency and pronounced generator torque oscillations [4]. Second topology, shown in Fig. 1.1, though requires a more vigilant control for machine side converter but is preferred in most of

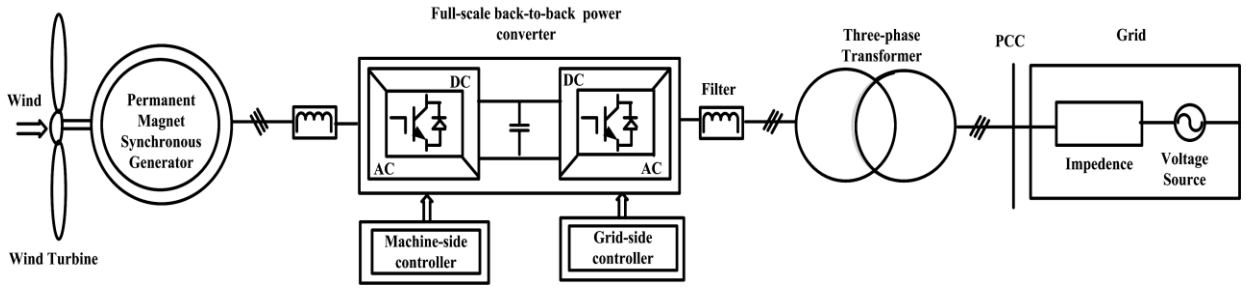


Figure 1.1 A gearless wind energy system with synchronous generator and full-scale converter.

the present day PMSG driven wind energy systems.

Variable speed wind turbines using PMSG technology has been studied quite extensively in the past few years with a lot of emphasis given to dynamic and transient characteristics analysis of this system [3]. However with growing trend of multi-megawatt turbine installations and an ever increasing contribution of wind power in the grid system, another issue of grave importance is reliability of PMSG driven wind energy systems.

Main issue of concern with single full-size converter technology is their reliability which is seriously jeopardized when due to equipment failure or for sake of maintenance, the entire WECS goes out of service. Also systems with single full-size converter exhibit reduced efficiency at low power levels and have tendency of injecting harmonics into the grid [3]. For reasons mentioned above, an alternative approach which replaces single unit with set of converter modules of smaller power rating is gaining popularity. Manufacturer like Gamesa have in their design of PMSG based variable speed wind turbine, utilized a multi-converter topology [3], [5].

Multi-converter topology integrated with a PMSG that has multiple 3-phase winding sets was discussed in [3] and main emphasis was given to the transient performance of the system during network disturbance. Pictorial representation of the multi-modular technology which is integrated with a multi-pole/multi-phase PMSG is shown in Fig. 1.2. Use of PMSG that has multiple three phase winding sets that are both electrically and magnetically independent, help in resolving issue of circulating currents. Independent control units for both machine and line side converters exist in all the parallel channels.

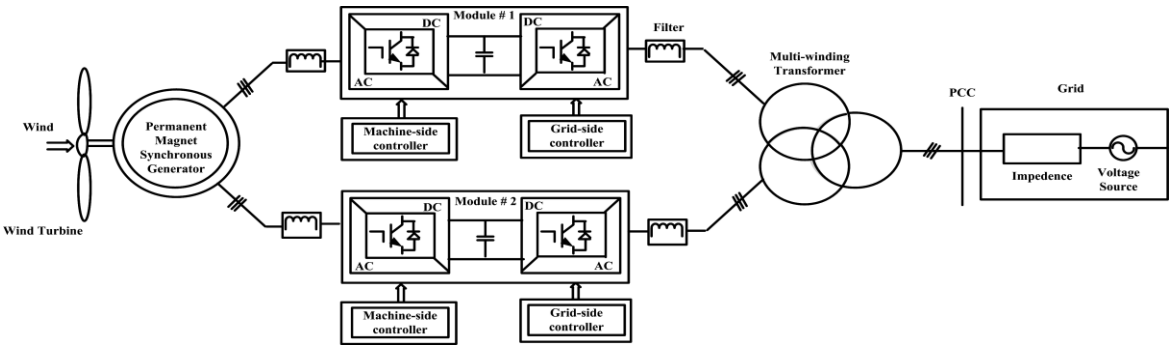


Figure 1.2 Multi-phase PMSG machine connected to the grid using modular converter system.

In view of the rising potential of direct driven PMSG based WECS using modular converters,

research work carried out here focuses broadly on development of control units used with such a system.

1.2 Features of modular design

1.2.1 Benefits of modular design

Limitations of semiconductor devices restrict power capacity of single full size converter. A way of overcoming this problem is by employing parallel operation of power modules which has tendency of delivering unlimited output power. Such an operation can be adopted by paralleling of switching devices or through parallel operation of converters [6]. The second of the two options is considered to be more advantageous, specifically due to the fact that such a system is more flexible for future expansion.

In [7], benefits of using modular inverter system were highlighted. The major plus points were increase in system reliability/ redundancy and higher level of stability offered against external disturbances. Also among list of benefits associated with modular design are reduced unit maintenance cost, lower harmonics and use of smaller sized filter components. Flexibility of modular system permits future extension/upgrade process a lot easier. With reliability and redundancy identified as most important feature of modular design, it is desirable to have modules that are equipped with independent controllers which share no critical control functions [7] as information sharing would require large-scale communication infrastructure which will jeopardize redundancy feature of modular system.

1.2.2 Extent of local control in modular design

To reap benefits of modularity emphasis is laid on local control of modules. Controllers used in conjunction with system of multiple parallel-operating converters are available mostly in centralized or master-slave configurations. The control structure we aim to develop here will have higher count of hardware allocated to local controller which is contrary to the central control configuration. The desired system will also not be totally distributed control scheme as is for the case of master-slave control. Though master-slave configuration does not have single-point-of-failure but it relies on extensive communication between the modules which increases system's complexity, operational interdependency and also slows down response time to external disturbances [8]. Development of a controller which is hybrid of the two extreme cases is the target to achieve. Aim is to develop a distributed control structure that has low communication overhead and encourages local control without compromising global control task. Reliance on

local control does not necessarily mean that source of information for each individual controller is limited to local measurements alone. Rather individual controllers may utilize load/line side voltage or current measurements. Also for achieving synchronization between modules some global reference signals causing minimal communication overload, may also be utilized by local controllers.

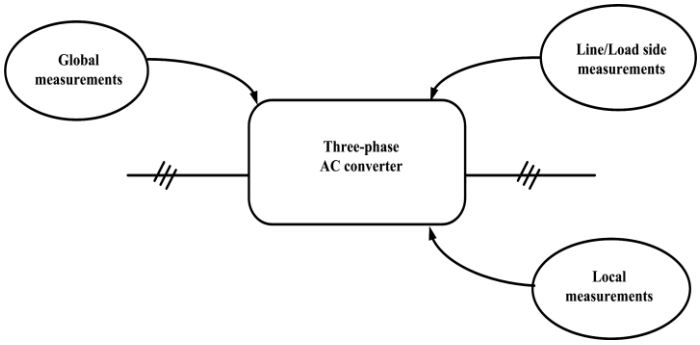


Figure 1.3 Sources of information used by individual controllers in modular converter system.

1.3 Literature review about switch interleaving

Switch interleaving also commonly referred to as interleaving is method in which switch turn on-times of parallel operating modules are spread evenly across the switching period [8]. Reason for mentioning this term here, is because some of the benefits such as lower harmonics and smaller sized filter components listed earlier with reference to modular converter technology are direct outcome of application of interleaving. Switch interleaving can be achieved using central control units deciding carrier phase shift for all the modules. However the modularity of design demands a distributed approach for carrier phase displacement. Distributed interleaving approach should have circuitry used in implementation of interleaved operation distributed among individual cells posing minimal interconnection within converter cells [9]. Subsections to follow will highlight benefits reported with reference to interleaving, some application where interleaving has been utilized and the practical implementation of this technique in modular converter system.

1.3.1 Benefits of interleaving

Mathematical background of distributed interleaved systems has been discussed in detail in [10]. It was concluded that distribution & interleaving (D & I) is an effective tool for rejecting harmonic components of periodic signals and performance of D&I system is greatly dependent on nature of signal under study, specifically its spectral composition. Drawing comparison

between a synchronous system and a set-up of interleaved converters cells, it was reported in [9] that broad category of topologies utilizing interleave technique exhibit N-folds rise in fundamental current ripple frequency and a decrease by the same factor in peak ripple magnitude. Numerous papers have been published regarding different approaches used for active interleaving of switching signals in parallel DC-DC converters. Majority of these schemes employ evenly spaced switching instants and same switching frequency for all the parallel modules [8]. Ripple cancellation effects of this technique has also been analyzed in case of [11]. Ripple estimation of paralleled DC-DC converter system revealed possibility of creating a zero ripple converter system provided duty ratio and number of modules in operation met some specific requirements [11].

Like the case of DC-DC converters, application of interleaving in three-phase AC converters and its effect on system harmonic have been topic of many publications. In [21] theoretical analysis of harmonic cancellation effect with reference to three-phase voltage-source converters (VSCs) was presented. A technique by the name of pulse train decomposition was employed for the purpose of analysis. Conclusion derived on the basis of it confirmed that inter-module harmonic cancellation effect experienced by modular three phase VSC is similar to the case of N-channel interleaved buck converter.

Systematic analysis of the effects of interleaving in three-phase VSCs was subject of study in [12] and analytical expressions were formulated for dc-link current, common-mode voltage, combined phase currents and for the current imbalance within parallel three-phase modules. Theoretical results accompanied by numerical simulation, confirmed that interleaving not only resulted in ripple cancellation of phase currents but also affected common-mode voltage and dc-link current of the system. Results were mainly derived using double-edge modulation technique but arguments were presented about generalization of developed analytical expressions for any carrier-based modulation method [12]. Interleaved operation of parallel three-phase VSC help in designing a system that uses smaller sized EMI filters and DC-link components [13].

1.3.2 Various applications of switch interleaving

Successful application of interleaving technique has been reported with reference to voltage regulator modules (VRM) used commonly with microprocessors. Composed to N-parallel operating buck converters, VRM through interleaving achieves maximum cancellation of switching ripple which promotes use of smaller sized filter components and a wider control

bandwidth of output voltage [14]. When applied to single or three-phase converters for Power Factor Correction (PFC), effectiveness of interleaving is yet again verified through marked reduction of input ripple current [12]. In [15] for a system of n-paralleled single-phase, un-interruptible power supply (UPS) inverters, displacement of carrier signals of individual PWM units resulted in low harmonic content of output voltage waveform with low switching frequency of power devices.

Phase-shifting Sinusoidal Pulse Width Modulation (PS-SPWM) technique is studied for gate turn-off thyristor (GTO) based force-commutated HVDC modular converters in [16] for cancellation of undesirable switching harmonics. Interleaved operation has also been employed in parallel inverter motor drive systems as accounted in [17] and for renewable energy systems [6]. Parallel topology comprising of two, three-phase interleaved power inverters sharing common DC-link capacitor was presented in [18]. Comparison of reactive power and harmonic compensation was made for the selected topology with regular three-phase inverter for the same application and results proved significant reduction in size of the passive components in case of interleaved operation [18].

1.3.3 Implementation of interleaving in modular converter system

Implementation of switch interleaving has been carried out extensively in DC-DC modular converters using both centralized and distributed technique with later of the two approaches proving more challenging in its execution [19]. For implementation of autonomous controller for three-phase VSC referral to distributed controller for DC-DC parallel converter system, acts as a relevant staring point.

One of the approaches used for automatic interleaving of modular DC-DC converters was reported in [20]. The scheme used filtered collective output of modules in order to detect appropriate switching instances. Experimental results verified that system had the capability of automatically regulating new interleaving status with occurrence of change in number of parallel operating cells. Implementation scheme of [9] made use of an interleaving bus in order to spread switching instants appropriately. Controller associated with each converter cell was attached to this bus and had its base clock placed 180 º out-of-phase with respect to systems aggregate clock signal.

Implementation of automatic interleaving is discussed with reference to three- phase VSC in case of [6]. Various control issues in connection with parallel operation of three-phase PWM

converters in PMSG driven wind power generation systems were also examined in the same paper. Master controller in this scheme had responsibility of determining active/reactive power reference as well as phase shift of individual units depending on the number of activated modules [6]. This scheme suffered from drawback of having all the critical control information delivered by a central command unit, failure of which will halt normal operation of entire WECS.

1.4 Research objectives

With rise of multi-mega watt turbine installation and fundamental limitations on power capability of semiconductor devices, pursuit of modular converter system in order to achieve high power level is inevitable. Besides the obvious benefits of scalability and redundancy, modular designs provides opportunity to significantly reduce harmonics in output of three-phase AC converters if carrier signals of modules are shifted evenly across the switching period. The mathematical definition of best interleave angle (θ_{best}) is given by (1.1).

$$\theta_{best}\ (\text{radians}) = \frac{2\pi}{N} \tag{1.1}$$

where N= Total number of operational units

Carrier phase shift for jth module in system of parallel inverters is adjusted as per (1.2).

$$\theta_{j}\ (\text{radians}) = \frac{2\pi(j-1)}{N} \tag{1.2}$$

where $j = 1,\ldots..,N$

Recent studies have demonstrated that interleaving also helps in controlling common-mode voltage and DC-link current in system with parallel operating channel. Main objective of this research work is to develop an interleaving control algorithm which promotes a decentralized control structure unlike the case of prevalent technique used for interleaving of three-phase parallel converters. Main computation of best interleave angle should be carried out locally by controllers of each module. The distributed approach does not disregard use of load/grid side parameters or utilization of global reference signals as long as the same does not impose an extensive communication overhead on the system. Autonomous controllers should have capability to automatically re-adjust its carrier phase shift as per (1.1) as soon as the system experiences change in number of operational units. Due to simplicity of its application sinusoidal

PWM will be used for machine and line-side converters.

Identified in [21] were some apprehensions regarding implementation of distributed interleaving technique in three phase converters, most important of which was varying nature of AC converters duty cycle. Discussed in the previous section were various distributed control schemes for automatic interleaving of DC-DC converters. Varying nature of AC signals will make application of these techniques very difficult for the case of three phase voltage source converters. Development of a de-centralized interleaving control algorithm for parallel VSC will therefore require a different approach altogether and will be discussed in detail in chapters to follow.

1.5 Thesis outline

Model of basic wind energy system will be discussed in Chapter 2. The chapter will include design of multi-phase PMSG machine and controllers for machine and grid-side controllers. Simulation results obtained by running the developed modular system for a test case (where all parallel channels stay in operational mode during entire course of simulation) will be included at the end of this chapter.

Controller for automatic interleaving of parallel three phase VSC will be topic of discussion in Chapter 3. Design of interleaving control algorithm starting from its concept development stage down to final execution in form of Simulink/MATLAB model will be unveiled in this chapter. Simulation results of complete PMSG based wind energy system incorporating this newly developed interleaving controller will be included in this chapter.

Laboratory testing of developed control algorithm using DSP-FPGA platform will be discussed in Chapter 4. System used for laboratory set-up was trimmed version of complete WECS and comprised of two parallel inverters, DC power supply, multi-winding transformer and a three phase resistive load. Test results verifying validity of design will be part of this chapter.

Chapter 5 will give an overview of what this research work has accomplished. Suggestions regarding future work will be provided at the end of this chapter.

Chapter 2 Model for multi-phase PMSG based wind energy system

2.1 Introduction

In the previous chapter it was mentioned that the main purpose of this research work is to develop an autonomous controller for modular converter system that would allow automatic interleaving of parallel converter units that are operating in a wind energy system equipped with direct driven Permanent Magnet Synchronous Generator (PMSG). Block diagram of the modular converter system to be used in this study was shown earlier in Fig. 1.2. Development of the interleaving control algorithm will be discussed in the chapters to follow, however the main objective of this chapter is construction of the basic system on which the control algorithm for automatic interleaving will be tested upon.

One of the features that stand out in Fig. 1.2 is the multi-phase design of PMSG. Reason for using PMSG with electrically and magnetically independent three phase winding sets is to prevent flow of circulating currents in modular converter structure [19]. The rectifier/inverter units in each of the parallel path will have independent controller that help generate PWM gating signals for their corresponding modules. The block diagram also reveals use of multi-winding transformer for connecting converter modules to the grid. Major portion of this chapter is dedicated to development of this modular converter system in Simulink. Results verifying accuracy of developed model will be provided in later half of Chapter 2.

2.2 Development of Simulink model for multi-phase PMSG

In MATLAB, model available for Permanent magnet synchronous machine is with single set of three phase windings. Our system requirement is for a PMSG that has multiple three phase winding sets. Hence the first and foremost step in development of system model would be to create in Simulink, model for a multi-phase (six phase) permanent magnet synchronous machine.

2.2.1 Types of Synchronous Generator

As implied by its name, synchronous generator (SG) has its rotor field aligned with the stator field. With rotor and stator fields operating at similar electrical speed, this type of machine operates without experiencing slip phenomena. Synchronous generator depending on the way its rotor magnetic flux is produced can mainly be divided into two categories, namely Wound Rotor

Synchronous Generator (WRSG) and Permanent Magnet Synchronous Generator (PMSG). In remaining part of this sub-section a brief overview will be provided about construction of these two types of synchronous generators.

2.2.1.1 Wound Rotor Synchronous Generator

With wounded rotor configuration, this type of synchronous machine can be further classified as salient pole and non-salient pole machine depending on the construction of its rotor. Another way of classifying WRSG, depicted in Fig. 2.1, is based on the method for supplying DC current to rotor windings. Referring to Fig. 2.1, in case of slipring fed WRSG, the rotor current is provided through brushes that in turn using sliprings are electrically connected to the rotor coil. The other category of WRSG has a small AC generator fixed around shaft of the synchronous machine and output of the same after rectification supplies dc-current to the rotor coils [22].

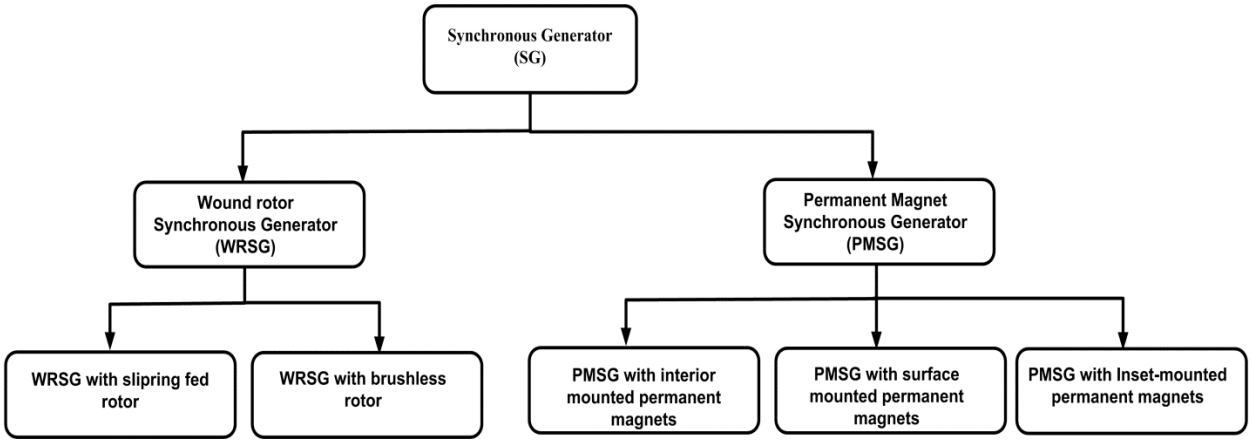


Figure 2.1 Different types of synchronous generators.

Coming back to classification of WRSG based on rotor saliency, machines with projected poles, on basis of construction exhibit a non-uniform distribution of air flux. Possibility of constructing WRSG with high number of poles, enable these machines to find application in areas where high torque/low speed operation is desired. One such application is that of direct connected wind energy systems where objective is to achieve a gearless transformation of wind power to electrical energy. Benefits of a direct connected WECS include low maintenance cost, reduced mechanical stresses and higher efficiency [22].

Although Synchronous Machines (SM) with very large number of pole pairs has high inertia loads attached to their shaft, and loss of synchronism is not a matter of concern here. However in

case of machines with smaller number of pole pairs, factors like torque fluctuation in shaft or voltage perturbations can jeopardize the rotor/stator synchronization of SM [22]. To help prevent this loss of synchronism, damper circuits in form of damper windings are placed in rotor frame.

2.2.1.2 Permanent Magnet Synchronous Generator

Unlike wound rotor machines, in case of a PMSG, it is the permanent magnets that are cause of production of rotor flux. As shown in Fig. 2.1 there are three sub-classes of PMSG and the division is made based on the placement of permanent magnets in machine's rotor. The most commonly used permanent magnet synchronous machine is the one that comes with surface mounted permanent magnets. Non-salient rotor configuration is possible if distribution of magnets is made evenly around perimeter of the rotor. This would result in a uniform/constant flux distribution in the air gap of surface mounted machine. The non-saliency of rotor structure results in approximately same value of synchronous reactances along d- and q-axis for the machine [23]. Main reasons for its popularity are simplicity and a lower price point when compared with other versions of PMSG. The downside of using surface mounted synchronous machine includes risk of detachment of magnet from the rotor surface and risk of demagnetization of pole magnets [22].

Synchronous machines with interior-magnet rotor have pole area at the rotor surface greater than pole area of magnet. Value of synchronous reactance measured along d-axis is smaller than synchronous reactance along the direction of quadrature axis of this machine [23]. Unlike the case of surface mounted PMSG, the version with interior magnets is found to be more rugged against centrifugal forces because of magnetic poles positioning in the rotor core [23]. For this reason interior-magnet PMSG's are ideal for use in high speed applications and fail to find a place in direct driven wind energy systems [22].

Lastly we have inset-type generators in which permanent magnets are embedded in shallow slots and gaps between the slots are partially filled with iron [22]. Due to this iron filling, rotor acquires a salient structure making this machine less susceptible to the effects of centrifugal forces. The salient structure dictates that synchronous reactance along q-axis is greater than its d-axis counterpart [23]. In addition to torque from magnets there is also a reluctance torque generated in inset mounted PMSG. Issue with inset-type generator as compared to surface mounted machines is the increased flux leakage at the ends of the magnets [22].

2.2.2 Reference frames for control

A synchronous machine can be described by a system of n+ 1equations. With the exception of one, the rest of the equations are electrical in nature and are obtained by applying Kirchoff's voltage law to all of the windings. Calculation of inductive voltage drop across a winding requires correct estimation of total magnetic flux linking it. For this purpose an inductance matrix is needed which gives relationship between flux linkages and all the windings currents. The magnetic asymmetry specifically of a salient-pole machine dictates that its inductance matrix will have dependence on rotor position. The main challenge faced in modelling of synchronous machine is dependence of its inductance matrix on this time varying quantity i.e rotor position .A possible solution of this problem is the change of reference frame for defining machine variables [24].

Generally control of generator systems are carried out using vector control techniques in which electrical quantities expressed in terms of qd0 components (aligned to a selected frame of reference) are controlled. Alignment of reference frame with space vector of certain generator quantity which is rotating as per vector's rotational speed helps in transforming generator quantities from sinusoidal to steady state making task of control system a lot easier [1]. The four different reference frames that are commonly used in analysis of electric machine and power system components [25] are listed in Table 2.1.

Table 2.1 Reference frames used for analyzing electric machine [25].

Speed of reference frame	Interpretation
w	Variables of stationary circuit referred to arbitrary reference frame.
0	Variables of stationary circuit referred to stationary reference frame.
w_r	Variables of stationary circuit referred to a reference frame that is fixed in rotor.
w_e	Variables of stationary circuit referred to reference frame that is rotating at synchronous speed.

Though it is possible to refer stator variables of synchronous machines to the arbitrary reference frame but this will offers no advantages during analysis. In fact the only way to eliminate dependence over time varying inductances of synchronous machine is to select a reference frame that is fixed in its rotor [25]. The rotor-oriented dq-reference frame (RRF) as its name implies has direct (d) axis of the reference frame aligned with vector of magnetic flux [1]. The stator current (i_s) in terms of its d and q components is expressed in (2.1). Illustrated in Fig. 2.2 is rotor reference frame [26] and d-component of stator current (i_d) is seen in full alignment with permanent magnet flux (λ_{rf}) of synchronous machine.

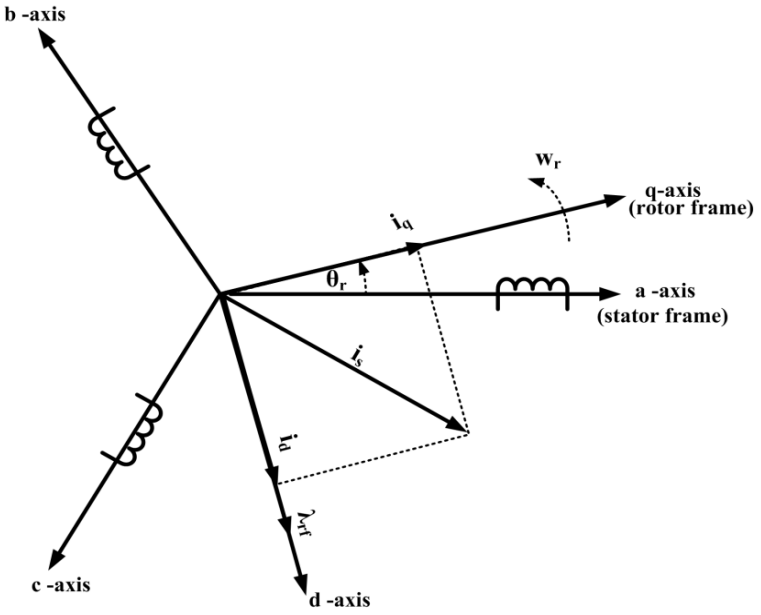


Figure 2.2 Space vector diagram for Synchronous generator.

Synchronous generator's dq-model can be obtained by decomposing space vectors into respective d-axis and q-axis components

$$\vec{i}_s = i_d + ji_q \tag{2.1}$$

Two conversion matrices given by (2.2) and (2.3) are used for conversion of variables between abc and qd0 reference frames, commonly referred to as Park and inverse Park transformation matrices.

$$\begin{bmatrix} f_q \\ f_d \\ f_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta_r) & \cos(\theta_r - \frac{2\pi}{3}) & \cos(\theta_r - \frac{4\pi}{3}) \\ \sin(\theta_r) & \sin(\theta_r - \frac{2\pi}{3}) & \sin(\theta_r - \frac{4\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{2.2}$$

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} \cos(\theta_r) & \sin(\theta_r) & 1 \\ \cos(\theta_r - \frac{2\pi}{3}) & \sin(\theta_r - \frac{2\pi}{3}) & 1 \\ \cos(\theta_r - \frac{4\pi}{3}) & \sin(\theta_r - \frac{4\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} f_q \\ f_d \\ f_0 \end{bmatrix} \tag{2.3}$$

In (2.2) and (2.3), the variable "f" can stand for voltage, flux linkage or current. The term θ_r which is angular displacement (radians) is defined in (2.4).

$$w_r = \frac{d\theta r}{dt} \tag{2.4}$$

where parameter w_r stands for rotor's electrical speed in radians/sec. A convenient approach for describing balanced steady state operation of synchronous machines is by making use of Parks equations. As for balanced system the 0s quantities will eliminate and simplified form of (2.2) and (2.3) are given by (2.5) and (2.6) respectively.

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta_r) & \cos(\theta_r - \frac{2\pi}{3}) & \cos(\theta_r - \frac{4\pi}{3}) \\ -\sin(\theta_r) & -\sin(\theta_r - \frac{2\pi}{3}) & -\sin(\theta_r - \frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{2.5}$$

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} \cos(\theta_r) & -\sin(\theta_r) \\ \cos(\theta_r - \frac{2\pi}{3}) & -\sin(\theta_r - \frac{2\pi}{3}) \\ \cos(\theta_r - \frac{4\pi}{3}) & -\sin(\theta_r - \frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} f_d \\ f_q \end{bmatrix} \tag{2.6}$$

Further simplification of the above two equations is possible by replacing the factor θ_r by θ_e. This is because in balanced steady state conditions the electrical angular velocity of rotor reference frame becomes constant and acquires the value of w_e. As defined earlier in Table 2.1, w_e is the electrical angular velocity of synchronously rotating reference frame [25]. Hence for balance steady state condition (2.7) holds true.

$$w_r = w_e \tag{2.7}$$

2.2.3 Model of multi-phase PMSG

Based on the overview of reference frames presented earlier, it is now possible to develop dynamic model of multi-phase permanent magnet synchronous machine. With the purpose of

simplifying dynamic model of PMSG, it is implemented using rotor reference frame [22]. Model of the machine that will be developed here is a six-phase PMSG machine for wind power systems, detailed parameters of it are given in Table A-1. Section of structural view of this machine is shown in Fig. 2.3 and dynamic model of the same in rotor frame of reference is given in Fig. 2.4 (i) and (ii). Like the case of three- phase PMSG, dynamic model of this multi-phase machine is developed making use of three sets of equations namely voltage equations, flux linkage equations and motion equations [22], [27].

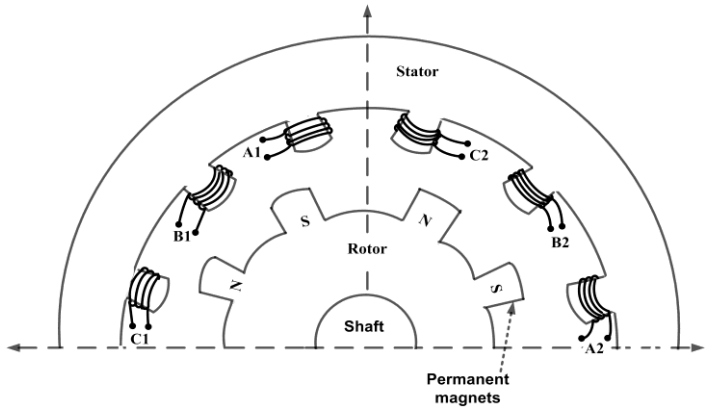


Figure 2.3 Structure of six- phase PMSG for wind power system.

Magnetizing inductance, PMSG's rotor flux and rotor electrical speed are represented by L_m, λ_{rf} and w_r respectively. Variables λ_{sd1}, λ_{sq1}, λ_{sd2} and λ_{sq2} are stator d- and q- axis flux linkages for three phase winding set 1 and 2 respectively and ***p*** represents the derivative operator (d/dt) . Data of the multi-phase machine that is used for development and testing of our Simulink model has for the two winding sets same values of stator self inductances along d and q axis. These two parameters are represented by variables L_{sd} and L_{sq} respectively.

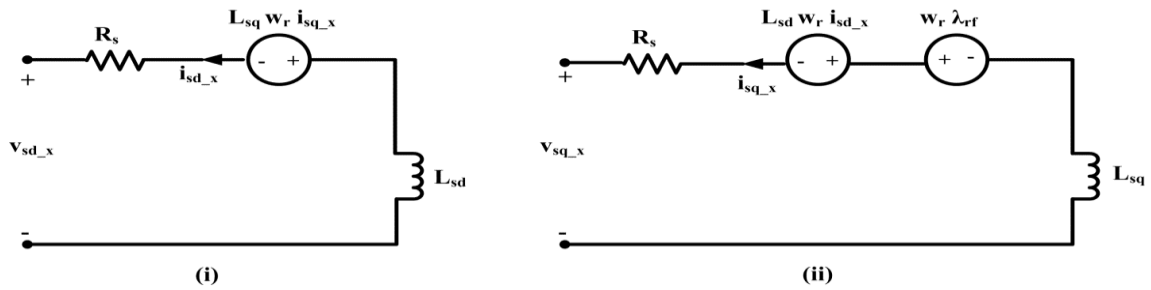


Figure 2.4 PMSM's dynamic model in rotor reference frame [22] (i) d- axis model (ii) q-axis model. (for n number of three phase winding sets, x= 1, 2..n).

Equations (2.8), (2.9), (2.12) and (2.13) are voltage and flux linkage equations that are relevant to 1st set of three phase windings and (2.10), (2.11), (2.14) and (2.15) represent 2nd set of three phase winding.

$$v_{sd1=} - R_s i_{sd1} - w_r \lambda_{sq1} + \boldsymbol{p}\lambda_{sd1} \tag{2.8}$$

$$v_{sq1=} - R_s i_{sq1} + w_r \lambda_{sd1} + \boldsymbol{p}\lambda_{sq1} \tag{2.9}$$

$$v_{sd2=} - R_s i_{sd2} - w_r \lambda_{sq2} + \boldsymbol{p}\lambda_{sd2} \tag{2.10}$$

$$v_{sq2=} - R_s i_{sq2} + w_r \lambda_{sd2} + \boldsymbol{p}\lambda_{sq2} \tag{2.11}$$

$$\lambda_{sd1=} - L_{sd} i_{sd1} + \lambda_{rf} \tag{2.12}$$

$$\lambda_{sq1=} - L_{sq} i_{sq1} \tag{2.13}$$

$$\lambda_{sd2=} - L_{sd} i_{sd2} + \lambda_{rf} \tag{2.14}$$

$$\lambda_{sq2=} - L_{sq} i_{sq2} \tag{2.15}$$

For a PMSG, field winding is replaced by permanent magnets and representation of that in the model can be in form of a fixed magnitude field current source (I_f) [22].

$$\lambda_{rf} = L_m I_f \tag{2.16}$$

By substituting equations for rotor flux and d and q axis flux linkages into (2.8) – (2.11), modified version of voltage equations are obtained.

$$v_{sd1=} - R_s i_{sd1} + w_r L_{sq} i_{sq1} - L_{sd} \boldsymbol{p} i_{sd1} \tag{2.17}$$

$$v_{sq1=} - R_s i_{sq1} - w_r L_{sd} i_{sd1} + w_r \lambda_{rf} - L_{sq} \boldsymbol{p} i_{sq1} \tag{2.18}$$

$$v_{sd2=} - R_s i_{sd2} + w_r L_{sq} i_{sq2} - L_{sd} \boldsymbol{p} i_{sd2} \tag{2.19}$$

$$v_{sq2=} - R_s i_{sq2} - w_r L_{sd} i_{sd2} + w_r \lambda_{rf} - L_{sq} \boldsymbol{p} i_{sq2} \tag{2.20}$$

Rotor mechanical speed denoted by w_m and electromagnetic torque (T_e) of multiphase PMSG are given by (2.21) and (2.22) where parameters T_m, N_p, J, and F stand for mechanical input torque, number of pole pairs, moment of inertia and friction factor respectively [22],[27]. In Laplace domain derivative operator is represented by ***s*** and 1/***s*** represent operator for integration.

$$w_m = \frac{1}{J}\left(\frac{1}{s}\left(T_e - T_m - w_m F\right)\right) \tag{2.21}$$

$$T_e = \frac{3}{2} N_p \left(\left(L_{sq} - L_{sd}\right) i_{sq1} i_{sd1} + \lambda_{rf} i_{sq1} + \left(L_{sq} - L_{sd}\right) i_{sq2} i_{sd2} + \lambda_{rf} i_{sq2}\right) \tag{2.22}$$

For computation of total active and reactive power of six phase machine (2.23) and (2.24) can be used.

$$P_{gen} = \frac{3}{2}\left[v_{sd1} i_{sd1} + v_{sq1} i_{sq1} + v_{sd2} i_{sd2} + v_{sq2} i_{sq2}\right] \tag{2.23}$$

$$Q_{gen} = \frac{3}{2}\left[v_{sq1} i_{sd1} - v_{sd1} i_{sq1} + v_{sq2} i_{sd2} - v_{sd2} i_{sq2}\right] \tag{2.24}$$

Using (2.16) to (2.22) model of six-phase PMSG is built in MATLAB and is shown in Fig.2.5.

2.3 Machine-side Controller

Beside wind regime, energy extracted from a wind turbine depends on the control strategy used for its implementation [27]. Control of synchronous machine is carried out through generator side converter. Preferred way of controlling generator is by using steady state signals instead of sinusoidal signals and for this reference frame has to be selected that rotates with one of the space vectors. Choice of three reference frames is available for control of PMSG. First of the lot is called rotor reference frame (RRF) which has its d-axis aligned with the rotor flux. The second choice of reference frame has its d-axis aligned with stator voltage vector, short form of it is SVRF. Last of the three choices is the Stator flux reference frame (SFRF) which is perpendicular to SVRF in orientation [1].

Three of the popular control strategies used in implementation of machine side controller are briefly discussed here and based on our requirement one of the most suitable scheme will be used for developing model of the generator side controller [1].Control strategies conventionally used for PMSG include constant stator voltage control, unity power factor control and maximum torque control [28], [29].

Constant stator voltage control is implemented mostly in SVRF (d-axis is aligned along the stator voltage space vector). Main purpose of this scheme is to control stator voltage at its rated value which helps in avoiding the chances of stator overvoltage occurring in case of an over speed [1]. Considering this control strategy applied to system modular converters, (2.25) up to (2.29) will hold true.

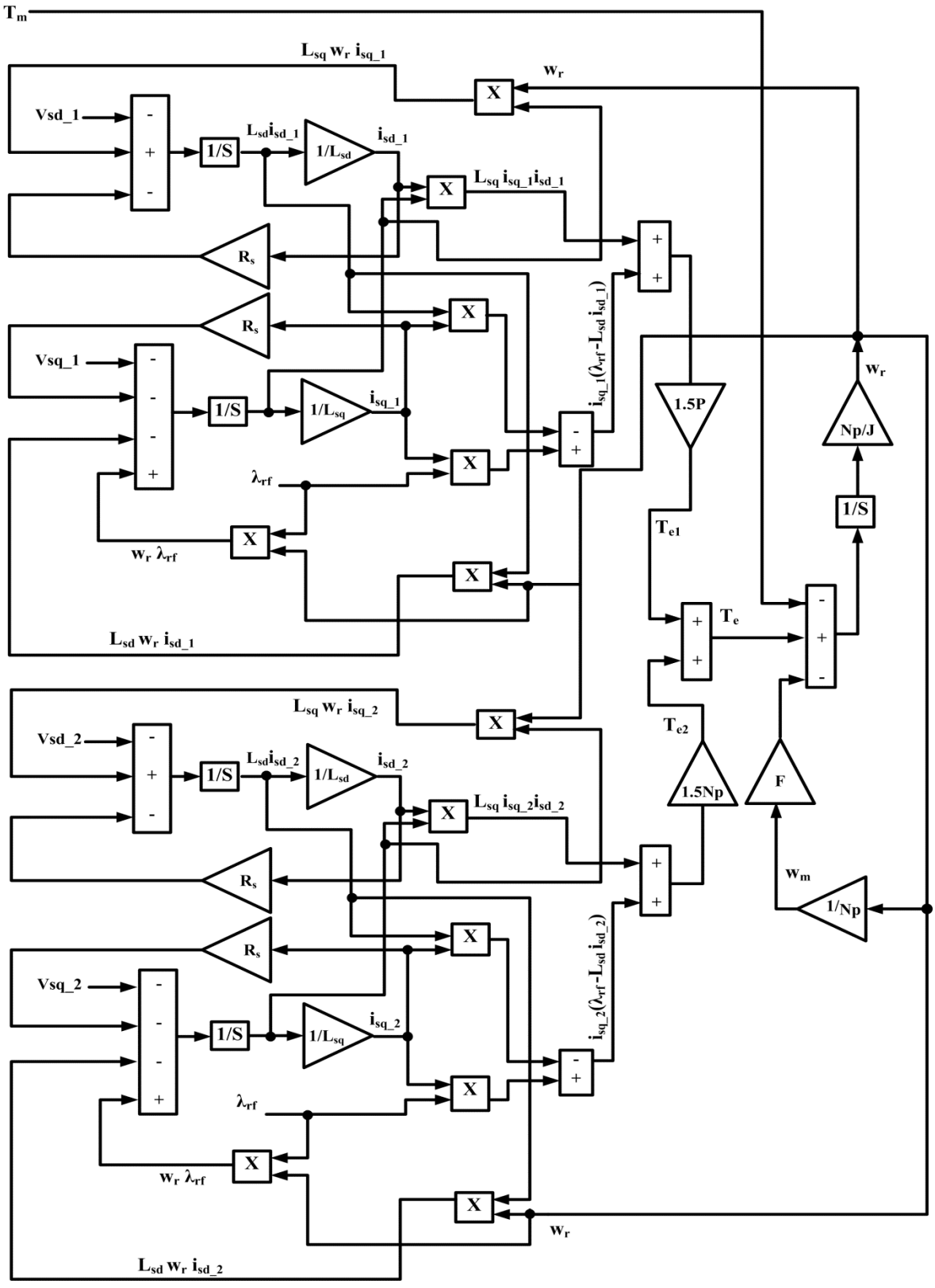


Figure 2.5 Model developed in rotor reference frame for a six -phase permanent magnet synchronous generator.

$$v_{s1} = v_{sd1} \tag{2.25}$$

$$v_{s2} = v_{sd2} \tag{2.26}$$

$$v_{sq1} = v_{sq2} = 0 \tag{2.27}$$

$$P_{gen} = \frac{3}{2}\left[v_{sd1} i_{sd1} + v_{sd2} i_{sd2}\right] \tag{2.28}$$

$$Q_{gen} = -\frac{3}{2}\left[v_{sd1} i_{sq1} + v_{sd2} i_{sq2}\right] \tag{2.29}$$

Looking at (2.28) and (2.29) it is clear that generators active and reactive powers have dependence on stator currents' direct and quadrature components respectively. Hence in this scheme active power is manoeuvred by d-axis component of the stator current while q-component tries to maintain stator voltage close to its rated value. The disadvantage faced by this control scheme is that in order to meet reactive power demands of generator a higher rating of converter module is required [1].

The objective of Unity power factor control is evident from its name. The scheme can be implemented in RRF and in order to compensate the generator's reactive power requirement the direct axis component of stator current is utilized. The zero reactive power demands allows use of smaller rating power converter on the generator side and this is the main advantage of using this control strategy. The problem with this scheme is lack of direct control over stator voltage which may cause stator voltage to surpass its rated value in case of an over speed [1], [28].

Aim of Maximum torque control strategy is to utilize stator side current in totality for control of machine torque which is done by setting d-axis current component equal to zero. By substituting zero against variables i_{sd1} and i_{sd2} in (2.22) up to (2.24), the following three modified equation implemented in RRF are obtained.

$$T_e = \frac{3}{2} N_p \left(\lambda_{rf} i_{sq1} + \lambda_{rf} i_{sq2}\right) \tag{2.30}$$

$$P_{gen} = \frac{3}{2}\left[v_{sq1} i_{sq1} + v_{sq2} i_{sq2}\right] \tag{2.31}$$

$$Q_{gen} = -\frac{3}{2}\left[v_{sd1} i_{sq1} + v_{sd2} i_{sq2}\right] \tag{2.32}$$

From (2.30) it is evident that this scheme allows optimal utilization of generator as stator current in its entirety is being used for torque generation, which would encourage use of smaller sized

generator for the same application. However looking at (2.32) it is noticed that reactive power requirement of generator is non-zero which is a disadvantage associated with this type of control strategy. Generator side converter will therefore have to cater for the reactive power requirement of the machine which will results in use of a power converter that has higher rating [1].

Based on criterion of optimal utilization of generator in mind the control strategy selected for implementation of machine side controller in our case is Maximum torque control. Structure of the same when implemented in rotor reference frame is presented in Fig. 2.6. Measured quantities include stator currents and rotor position. Later of the two measured quantities is determined via an encoder mounted on the machine shaft. Using MPPT controller optimal torque reference for the machine is identified which in turn helps in deciding set point for quadrature component of stator current. Reference of direct component of stator current is set equal to zero as dictated by maximum torque control scheme [19].

The nested loop structure of generator side converter is evident from Fig. 2.6. By comparing stator side d- and q-axis current reference signals with their measured values, voltage reference

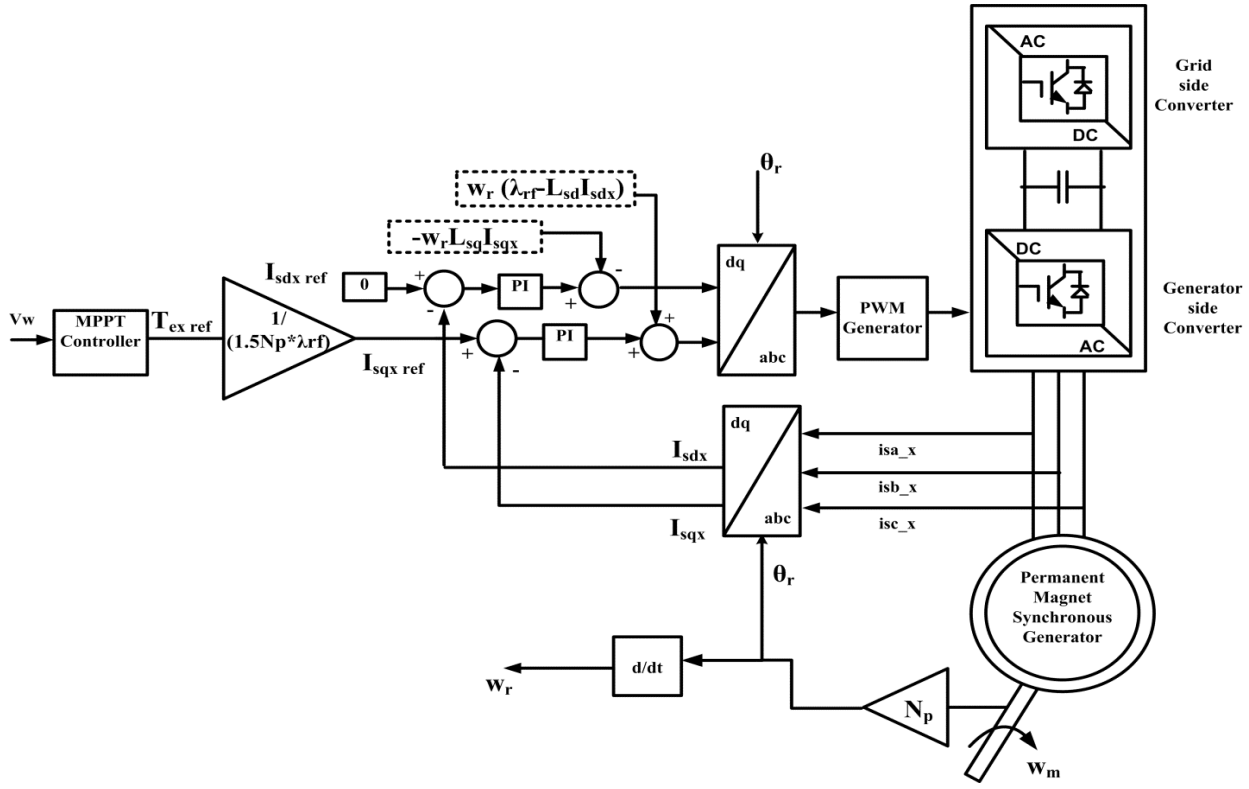


Figure 2.6 Block diagram of sub-controller for machine-side converter (for n number of three phase winding sets, x= 1, 2..n)

signals for the machine side converter are obtained [27]. Inclusion of compensation terms at outputs of the PI current regulators allows independent control of d- and q- axis currents [19]. PS-SPWM is used for generating gating signals for power converter.

2.4 Grid-side controller

With maximum torque control used for control of generator side converter it is possible to control reactive power supply to the grid independent from generator's operational point for reactive power. Hence line-side converter is responsible for meeting grid's reactive power demands. Additional responsibility of grid side converter is to ensure stable DC-link voltage that stays close to its reference level. This way no energy will get dissipated in the DC-link [1].

Various strategies have been developed for control of grid-side converter. These strategies are classified on the basis of the reference frame used for their implementation [30]. In this case grid side controller is developed making use of synchronous reference frame in which d-axis of reference frame is aligned with grid voltage vector. As frame rotates synchronously with grid voltage space vector hence transformation angle (θ_g) is detected by using Phase Locked Loop (PLL) [3]. The d and q axis component of grid voltage vector is given by (2.33) and (2.34).

$$v_{qg1} = v_{qg2} = 0 \tag{2.33}$$

$$v_{dg1} = v_{dg2} = vg \tag{2.34}$$

It is possible to express total active and reactive power flow to the grid from the six-phase PMSG machine in terms of grid voltage and currents of the two parallel channels (v_{dg1}, v_{qg1} – d/q component of voltage at output of inverter in channel #1, v_{dg2}, v_{qg2} – d/q component of voltage at output of inverter in channel#2, i_{dg1}, i_{qg1} – d/q component of current flowing towards the grid from inverter in channel #1, i_{dg2}, i_{qg2} – dq component of current flowing towards the grid from inverter in channel #2). By looking at (2.35) and (2.36) it is evident that active and reactive power can be controlled by controlling direct and quadrature components of grid current [4].

$$P_{grid} = \frac{3}{2}(v_{dg1}i_{dg1} + v_{dg2}i_{dg2}) \tag{2.35}$$

$$Q_{grid} = -\frac{3}{2}(v_{dg1}i_{qg1} + v_{dg2}i_{qg2}) \tag{2.36}$$

The control structure for the grid side converter controller is shown in Fig. 2.7 and has cascaded loops using PI regulators. The outer loop which is responsible for regulating DC-link voltage and reactive power flow [30],[31] in turn decides reference points for d- and q-axis components of currents. Resultant of the current controllers output together with voltage feed-forward and cross coupling terms, are voltage reference signal for the PWM generator [19]. Like the case of machine-side converter, Carrier based PWM scheme is used for generation of gating signals for inverter modules. In Fig. 2.7, $Q_{gridref}$ stands for grid's reactive power reference point which is dictated by Grid management services. In case no reactive power compensation is required then grid operator sets value of $Q_{gridref}$ as zero.

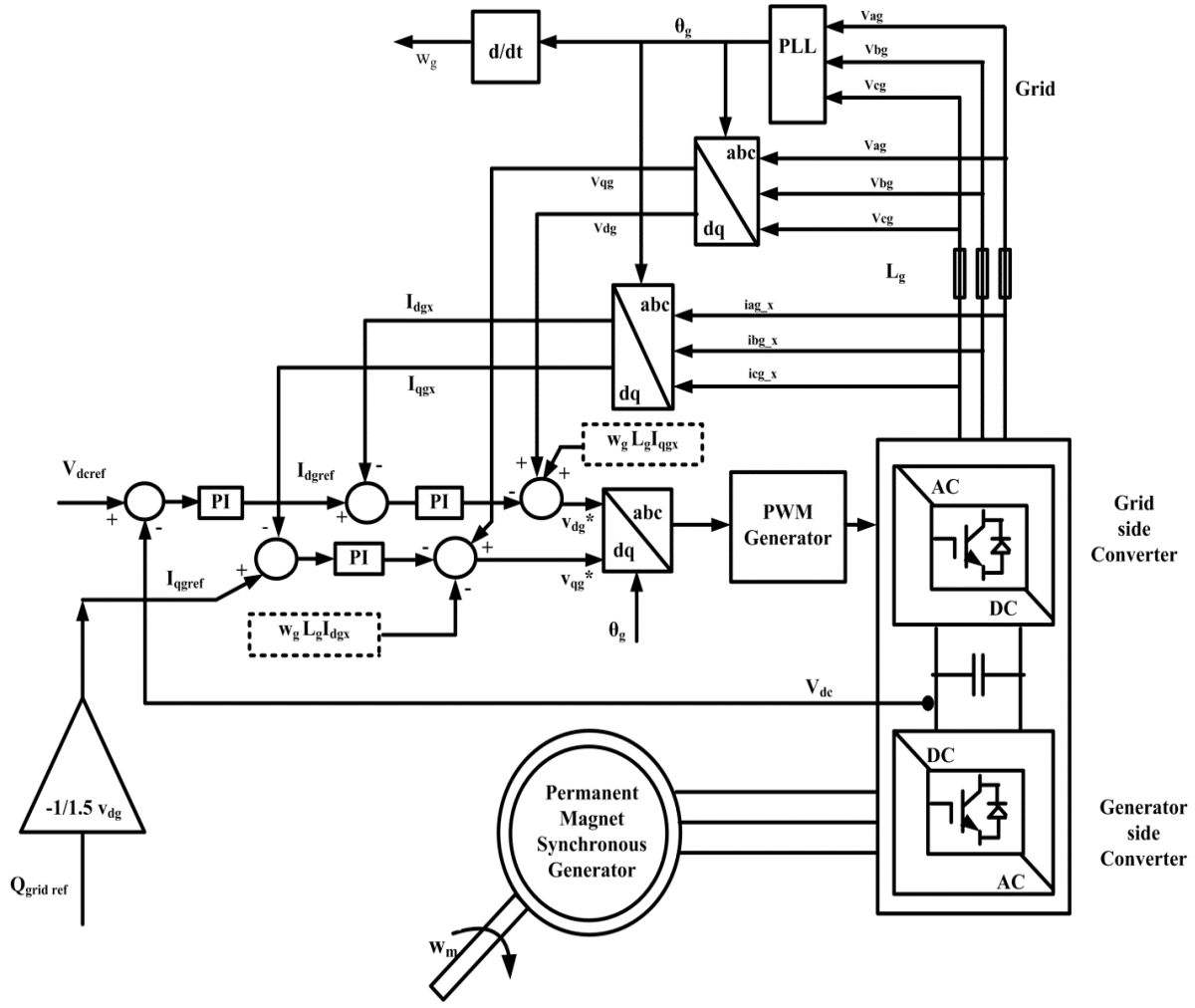


Figure 2.7 Block diagram of sub-controller for grid-side converter (for n number of three-phase winding sets, x= 1, 2..n)

2.5 Simulation results

In order to test the developed control strategy, wind energy system connected to a stiff grid through a six phase permanent magnet machine and two parallel operating converter modules is implemented using Simulink. Parameters of the test system are listed in Table A-1 of appendix section for reference. Simulation results obtained by running the above cited system are given in Fig. 2.8 up to Fig. 2.17.

As mentioned in design of generator-side controller, q-axis component of stator current is responsible for controlling Electromagnetic torque of the PMSG. Reference value of electromagnetic torque which is obtained in the Simulink model using MPPT controller is shown in Fig. 2.8. This reference is given individually to each of the two rectifier controller. Based on the given reference signal , electromagnetic torque actually developed in each of the three-phase winding set is plotted under Fig. 2.9. Comparing the reference signal of T_e with the measured value, a close coherence is observed in the two waveforms.

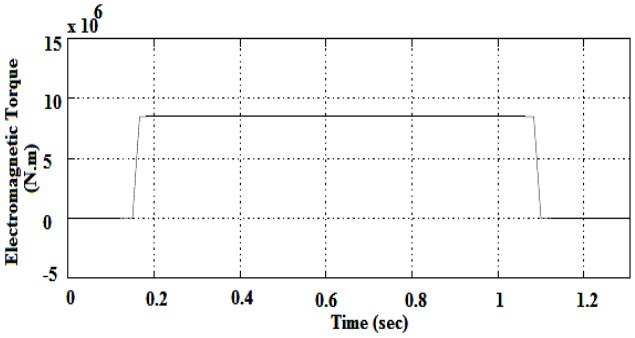


Figure 2.8 Electromagnetic torque (T_e) reference given to each of the three-phase winding sets.

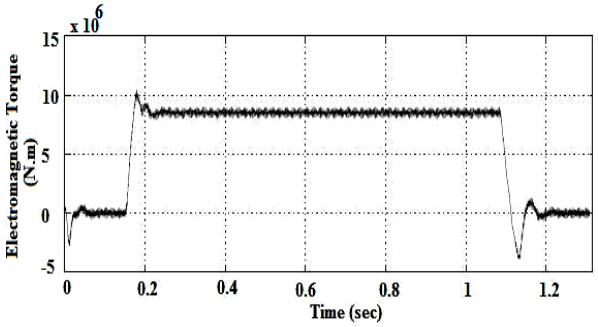


Figure 2.9 Electromagnetic torque developed in each of the three-phase winding sets.

It is important to mention here that the total electromagnetic torque developed by the six-phase machine as seen in Fig. 2.5, is sum of the electromagnetic torque generated by each of the three-phase winding sets and turns out to be 1.691 M N.m (Te_1=Te_2=0.845 M N.m, where Te_1 and Te_2 are electromagnetic torque produced by winding set 1 and 2 respectively). This value of total electromagnetic torque corresponds accurately to the PMSG's power rating i.e 4MW when w_m is set equal to 2.365 rad/sec.

The simulation results are for the system operating at unity power factor where reactive power

reference ($Q_{gridref}$) set by grid management services is zero. Looking at Fig. 2.11 it is observed that reactive power delivered to gird through each of the channels is close to its reference value. The same plot also features the active power flow to the grid from each of the parallel operating paths and as expected, for a 4MW machine, active power delivered to the grid through each converter modules is 2MW.

Total grid-side phase current for WECS is shown in Fig.2.10. Control of DC-link voltage as seen in Fig. 2.7 is responsibility of grid side converter module. In the simulated system, reference value set for DC-link voltage is 1220 V and is shown in Fig. 2.12. Measured DC link voltage follows its reference value in each of the two channels as seen in Fig. 2.13. It is worth mentioning that during entire course of simulation both channels stayed in ON state.

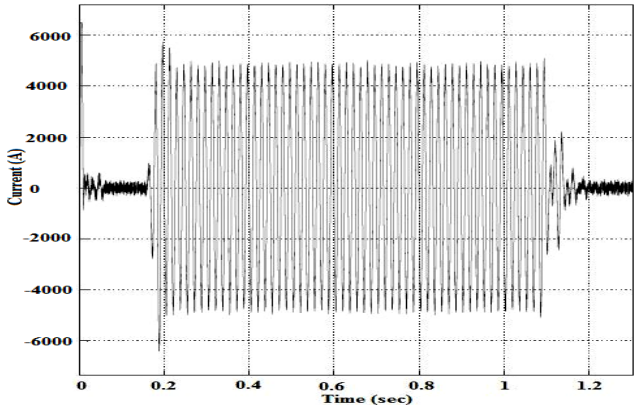


Figure 2.10 Total grid side current flowing in phase-A of the six phase PMSG wind energy system.

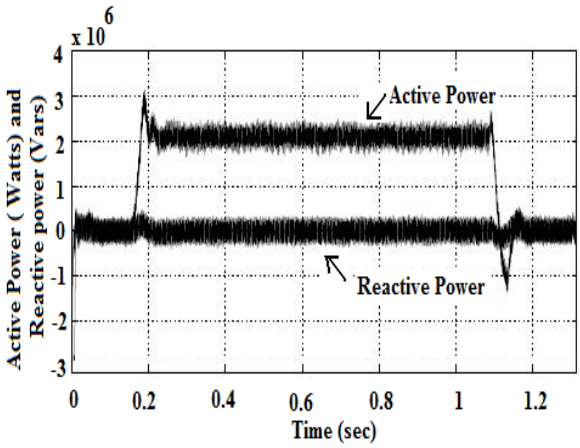


Figure 2.11 Active power and reactive power delivered to grid through each channel.

Carrier phase displacement for converter modules of the two channels, were adjusted keeping in view principle of best interleaving angle, presented earlier in Chapter 1. Hence for converter of channel #1 this angle is fixed at 0º while for rectifier/inverter placed in path #2, carrier phase is set as 180 º. Controller that allows automatic adjustment of carrier phases of individual unit relative to the others in operation is main objective of this thesis and will be discussed in the following chapter. Simulation results shown in this section are therefore for the system that does not have such a controller in place yet and fixed carrier phases are defined by the designer at start of simulation run.

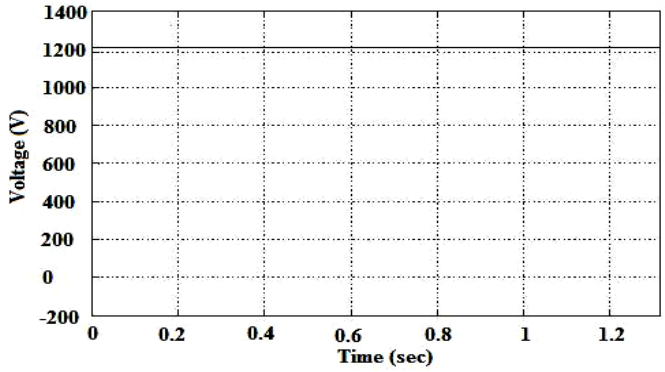


Figure 2.12 DC-link voltage reference given to each channel.

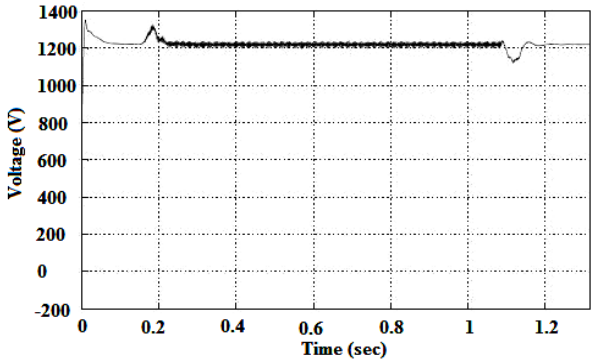


Figure 2.13 DC-link voltage measured in each of the two channels.

Stator current flowing in phase-A of one of the three-phase winding sets is shown in Fig. 2.14. Similarly current flowing towards grid through phase-A of one of the channels is given in Fig. 2.15. Comparing two plots it is seen that amplitude of currents is same for both the cases, difference is in frequency of the two signals. This is expected, keeping in view that stiff grid is operating at 60Hz and frequency of stator current as per system parameters is around 11.3 Hz.

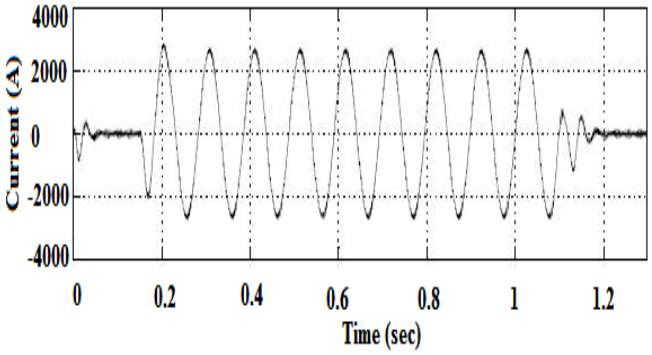


Figure 2.14 Stator side phase-A current, flowing in each channel.

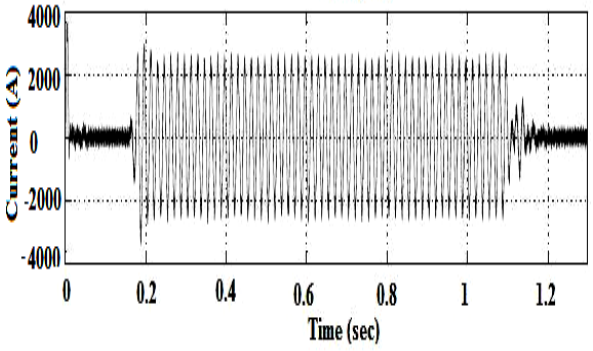


Figure 2.15 Grid side current in phase-A of each channel.

Keeping in view the control strategy developed for machine-side converter it was mentioned that the d-axis component is set equal to zero in order to allow control of Electromagnetic torque (T_e) solely by quadrature component of stator current. Given in Fig. 2.16 and Fig. 2.17 are the measured values of stator side q- and d- axis currents components for each of the two channels. It is seen in Fig. 2.17 that d-axis component stays close of its reference value more or less during

entire course of simulation, with a transitional bump appearing at the time of channel start-up and shut-down. The similarity in shapes of the two plots given by Fig. 2.9 and Fig. 2.16 it is verified that electromagnetic torque per channel is controlled via quadrature component of its stator side current.

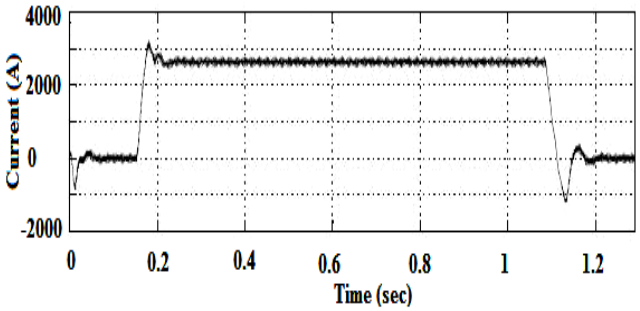


Figure 2.16 Quadrature axis component of stator current valid for each channel.

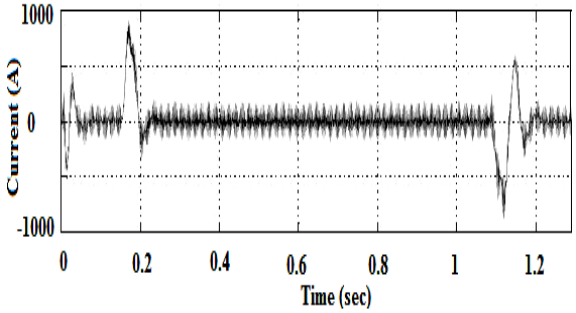


Figure 2.17 Direct axis component of stator current for each channel.

2.6 Summary

Main objective of this chapter was development of system model that utilizes a multi-phase PMSG machine that has parallel operating converter modules connected to a stiff grid. The initial section of the chapter discusses the types of synchronous generators and the reference frames most commonly used in construction of dynamic model for the same. Un-availability of multi-phase machine model in Simulink was reason why by using voltage, flux linkage and motion equations of PMSG, a dynamic model in rotor reference frame was created for a six-phase permanent magnet synchronous generator.

Controller for machine-side generator was developed based on Maximum torque control strategy and this was followed by controller design of grid-side converter that can perform the task of controlling DC-link voltage as well as reactive power flow to the grid. Finally the developed six-phase PMSG based WECS with two parallel operating channels was tested for the case when during entire course of simulation the two channels stayed in operational condition.

Results for the same were included in preceding section of this chapter and revealed satisfactory performance of the system. The channels followed their electromagnetic torque reference with measured d-axis current set equal to zero. The grid side converter also efficiently maintained the DC-link voltage close to its reference level which was 1220 V. Basic WECS developed in this chapter will be used later on for testing interleaving controller.

Chapter 3 Development of interleaving control algorithm

3.1 Introduction

Model developed in Simulink so far has been tested for the case where AC/DC and DC/AC converters present in all the parallel channels are always operational and a fixed carrier phase shift between the units is defined before the start of simulation. Such a system is not capable of handling dynamic conditions where the number of units operating in parallel may vary. A model that is capable of dealing with scenarios involving channel failure should have the ability to re-establish best possible interleaving angle for the remaining working modules. Objective of this chapter is to develop a control algorithm that has ability to spontaneously adjust interleaving angle for system of modular converters, as soon as the status of any of the unit in the system changes from ON to OFF or vice versa.

It is possible to have a setup for dynamic adjustment of carrier phases depending on number of operational units but that can either have a centralized control structure or master-slave configuration. However presence of central command unit will jeopardize system's redundancy factor. Hence in order to make system independent and autonomous, interleaving controller should have a distributed structure. In an arrangement that is totally distributed in nature, converter in each of the parallel paths would be able to come up with the best value of carrier phase shift employing no communication link between the modules in operation. If it is not possible to achieve an entirely distributed configuration then efforts should be made to develop a control algorithm where the crucial components of algorithm are run independently by controllers associated with each parallel module.

Techniques for interleaving of switching signals have been studied extensively with reference to modular DC-DC converters. Their implementation has proven to be advantageous as it effectively reduces ripple in output current which in turn encourages use of smaller sized filter components [8]. Distribution of carrier phase evenly across switching period has been carried out using either a centralized or distributed approach in parallel connected DC-DC converters with later approach found more challenging than the other.

An overview of popular distributed interleaving techniques developed for modular DC-DC was presented earlier in chapter 1 which included method that employed separate control bus for

carrying out interleaving operation, use of filtered collective output of parallel converter modules for identification of desired switching instances and setting up of a bus voltage signal, V_{mod} which helped in introduction of appropriate phase delay between the operational units [8], [32], [19].
Review of various method used for interleaving of DC-DC converters revealed that their direct application is not possible for modular Rectifier/Inverter units. Hindrance offered mainly is the varying nature of the AC signal encountered in case of rectifier or inverter modules. It is for this reason that a different approach is explored for achieving active/distributed interleaving of AC/DC or DC/AC converter units [19].

3.2 Main design challenges

First step in development of automatic control algorithm for rectifiers / inverters modules is identification of major design challenges and the same are listed as under:

- Each module should be able to determine best possible interleaving angle independently. This decision should be based on a feedback signal that is easily accessible to all of the parallel connected units.
- By using information acquired in the previous step each converter should adjust its corresponding carrier phase shift relative to other units in operation.
- A change in status of any of the parallel operating modules should trigger process of re-estimation of best interleaving angle in each module that is still operational.

For developing control algorithm it was decided to use a trimmed down/modified version of the Wind Energy Conversion System (WECS) developed previously. Main reason for doing so is to reduce simulation time for each trial as elaborate system like that of Fig. 1.2 may take longer time to complete a simulation run. During development stages of the algorithm, when system will be simulated over and over again a shorter time per trial is ideal for the designer. Once the algorithm is developed, it will then be incorporated into the model for entire WECS to verify its operation.
The system that is used for initial development of interleaving control algorithm is shown in Fig. 3.1 and it consists of three DC/AC converter units operating in parallel. Each module is connected to a 400V DC power supply at one end and with an L- filter on the other side. Outputs of the three inverters feed a common RC load which draws 3000 Watt active power and 500 Var reactive (capacitive) power at nominal frequency of 60 Hz, with line to line voltage (V_{L-L}) set

equal to 208V (rms). The three inverters are controlled in open loop manner and have PWM signals generated using sinusoidal PWM technique. The six PWM signals for each inverter are generated using individual Discrete PWM Generator block from Simulink library. All the three parallel channels, besides having same DC voltage level also have similar carrier frequency, modulation index (m = 0.85) and modulating frequency (f_1) which is 60 Hz. Harmonic filtering for the system is achieved through combination of L- filter and load side capacitance.

An important decision made before model development is about systems sampling frequency (f_{samp}) and switching/carrier frequency (f_s). In this case, values selected for f_{samp} and f_s are 194.553 kHz and 1980 Hz respectively, and frequency modulation index (m_f) which is defined as the ratio between carrier and modulating frequency turns out to 33 in this case. It is to be noted that converter's switching frequency is not selected randomly. Rather special consideration is given to the fact that this number should be a multiple of 3 and an odd multiple of modulating frequency (f_1), this way even order harmonics will be minimal in the output of VSI [33].

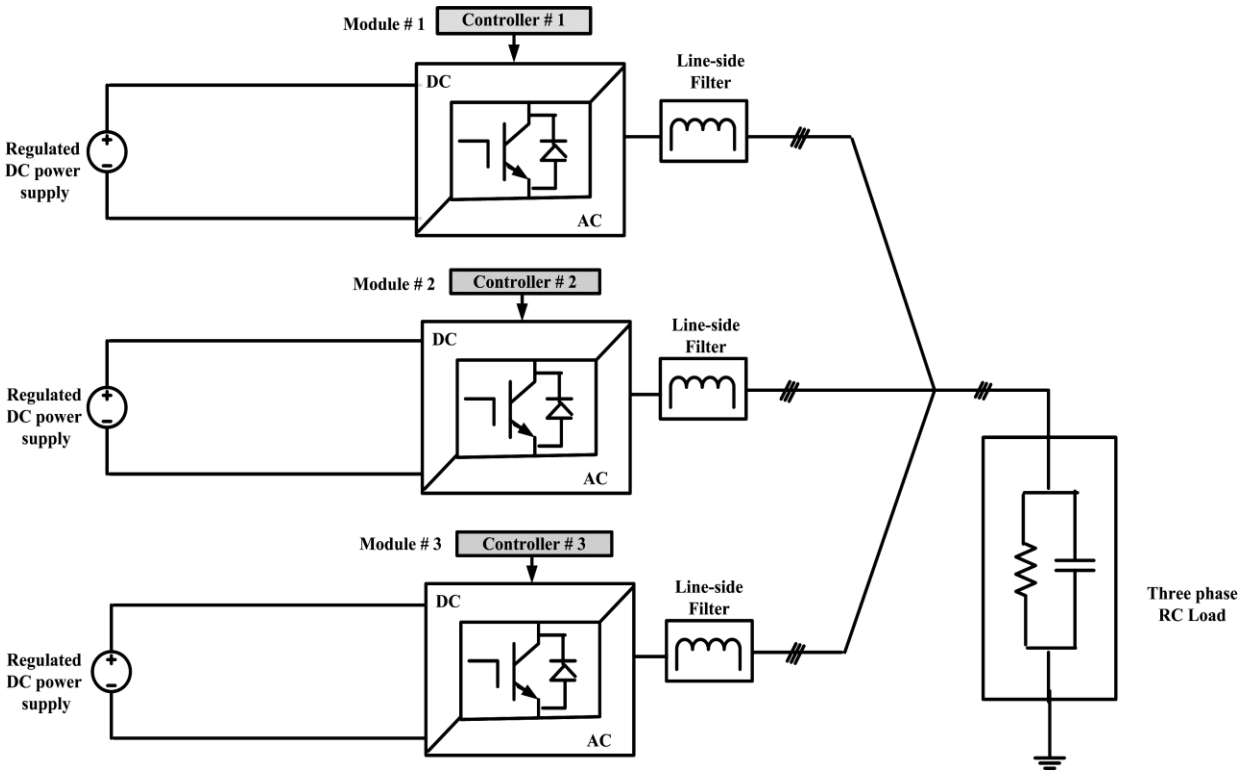
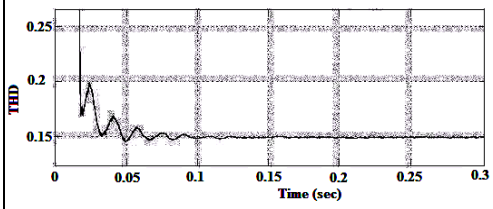
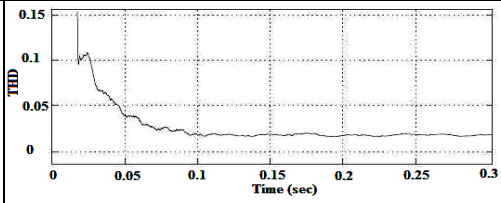
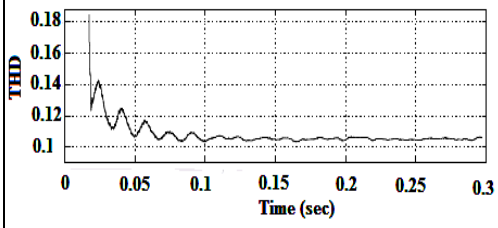
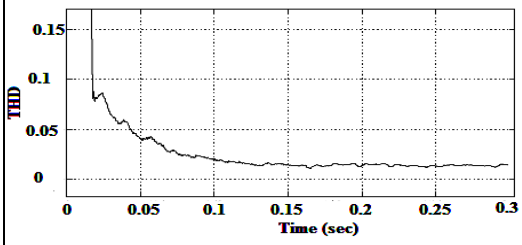
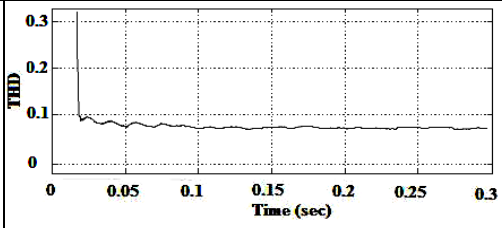
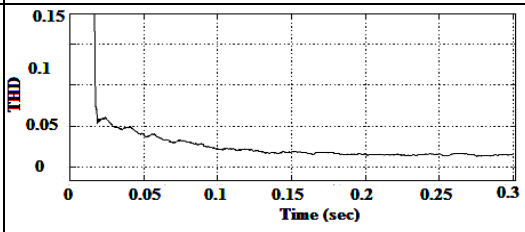


Figure 3.1 Modular Inverter system connected to RC load.

Referring back to the first challenge faced in development of interleaving control algorithm, an emphasis is laid on the fact that feedback signal used for determination of appropriate carrier phase should be equally accessible to every parallel operating unit. Two possible signals that meet this accessibility criterion are load side voltage and current. Other important quality the signal of choice should have is its noticeable dependence on number of modules in operation. In order to make this decision, simulations were carried out for system of modular inverters with two, three and five channels operating in parallel and in each of the case the load connected at the output was kept the same for the sake of uniformity. A quantity called Total harmonic Distortion (THD) for both load side phase current and voltage was recorded for each simulation set up and results for the same are listed in Table 3.1.

Table 3.1 Total Harmonic Distortion (THD) recorded for load- side phase current and voltage for different modular inverter systems.

Number of parallel modules	THD of Load side phase current	THD of Load side phase voltage
2		
3		
5		

Reason for recording THD level for the two signals is because this quantity reflects amount of distortion in voltage or current waveform [33]. Looking at the results it can be seen that a prominent difference in THD level is recorded for measured load side phase current for all the three cases. On the other hand change in number of parallel modules does not influence THD measurement of load side phase voltage in significant manner. Based on this observation the feedback signal that is best suited for implementation of interleaving control algorithm would be the load side phase current. Once this current is measured, the next question that comes to mind is about the index that will be determined using this measured current so as to determine best possible interleave angle. In order to find answer to this question it won't be illogical to refer back to a quantity that is strongly affected by selection of interleave angle i.e THD.

For mathematical definition of the term THD we first need to define an additional term which is called distortion component of current and is represented by variable $i_{Dist.}$ As evident from its name this factor represents the harmonics in current and is given by (3.1).

$$i_{Dist} = (i_a(t) - i_{a1}(t)) = \sum_{n \neq 1} i_{an}(t) \tag{3.1}$$

Variable i_{a1} in the equation above stands for the fundamental component of instantaneous current. In terms of rms values the distortion component of current represented by I_{Dist} is given by (3.2).

$$I_{Dist} = (I_a^2 - I_{a1}^2)^{\frac{1}{2}} = (\sum_{n \neq 1} I_{an}^2(t))^{\frac{1}{2}} \tag{3.2}$$

We are now in position of giving a mathematical definition of THD and it is given by (3.3). In order to signify it as THD associated with current a subscript *i* appear next to the acronym:-

$$\%\,THD_i = 100\,x\,\frac{I_{Dist}}{I_{a1}} \tag{3.3}$$

$$\%\,THD_i = 100\,x\,\frac{\sqrt{(I_a^2 - I_{a1}^2)}}{I_{a1}} \tag{3.4}$$

$$\%\,THD_i = 100\,x\sqrt{\sum_{n \neq 1} (\frac{I_{an}^2}{I_{a1}^2})} \tag{3.5}$$

$$\%\,\mathrm{THD_i} = 100\,\mathrm{x}\sqrt{\sum_{n\neq 1}\left(\frac{I_{an}}{I_{a1}}\right)^2} \tag{3.6}$$

A modification can be made in (3.6) and that is expressing the equation in terms of peak values instead of its rms values.

$$\%\,\mathrm{THD_i} = 100\,\mathrm{x}\sqrt{\sum_{n\neq 1}\left(\frac{\sqrt{2}I_{an}}{\sqrt{2}I_{a1}}\right)^2} \tag{3.7}$$

We know that energy of a harmonic component is proportional to the square of its magnitude [34] as given by (3.8).

$$E_{an} \propto (|\,I_{an}\,|)^2 \tag{3.8}$$

Looking at (3.7) and (3.8) it can be inferred that if ratio of energy is taken for different harmonic components relative to the energy of fundamental component, then the index we obtain will be proportional to THD. Mathematically it is represented as (3.9).

$$\mathrm{THD_i} \propto \sum_{n\neq 1}\frac{E_{an}}{E_{a1}} \tag{3.9}$$

Hence like the case of $\mathrm{THD_i}$, the ratio on the right hand side of (3.9) will also prove to be a measure of harmonics existing in a system. The selection of interleave angle will affect this ratio in the same way as it does the value of $\mathrm{THD_i}$. While developing the model in Simulink, determination of energy of harmonic will not be problematic as there exists a block named *Discrete Fourier* which gives information about magnitude and phase of a harmonic component for the signal of interest. Retrieving information about energy of harmonic component would therefore mean squaring of magnitude output of this block.

Although in (3.9) the order of harmonic can vary up to infinity but practically it is impossible to take into consideration, effect of infinite harmonic components. Hence for studying the effects of carrier phase shift on energy content, harmonics that are lying in the band of frequencies around m_f and $2m_f$ are analyzed initially. Energy contents of harmonic components of grid side phase around m_f and $2m_f$ are denoted by symbols E_{mf} and E_{2mf} respectively. In order to compare different systems together the two terms E_{mf} and E_{2mf} are added together and expressed as ratio of

energy of fundamental harmonic component (E_{a1}). Name given to this term is *Energy ratio* (E_H) and mathematical definition of the same is given by (3.10).

$$E_H = \frac{E_{mf} + E_{2mf}}{E_1} \tag{3.10}$$

This newly defined term will be referred to repeatedly in the forthcoming section of this chapter and will act as a measure for estimating best possible interleaving angle for the system of parallel operating inverters. In the model of three inverter system shown in Fig. 3.1 a sub-system that is responsible for determining quantities E_{mf} , E_{2mf} and E_H is included, and Simulink model for the same is shown in Fig. 3.2 . The harmonics that are considered in evaluation of E_{mf} , span from m_f-6 to m_f+6 (m_f is equal to 33), and for the case of E_{2mf} the range of frequency components formulating it lie in the band of frequencies from $2m_f$-5 up to $2m_f$+5.

In Fig 3.2 there are some additional tags appearing in the diagram that require some explanation. The tag E_mf_even and E_mf_odd are sum of energy contents of even and odd harmonics lying

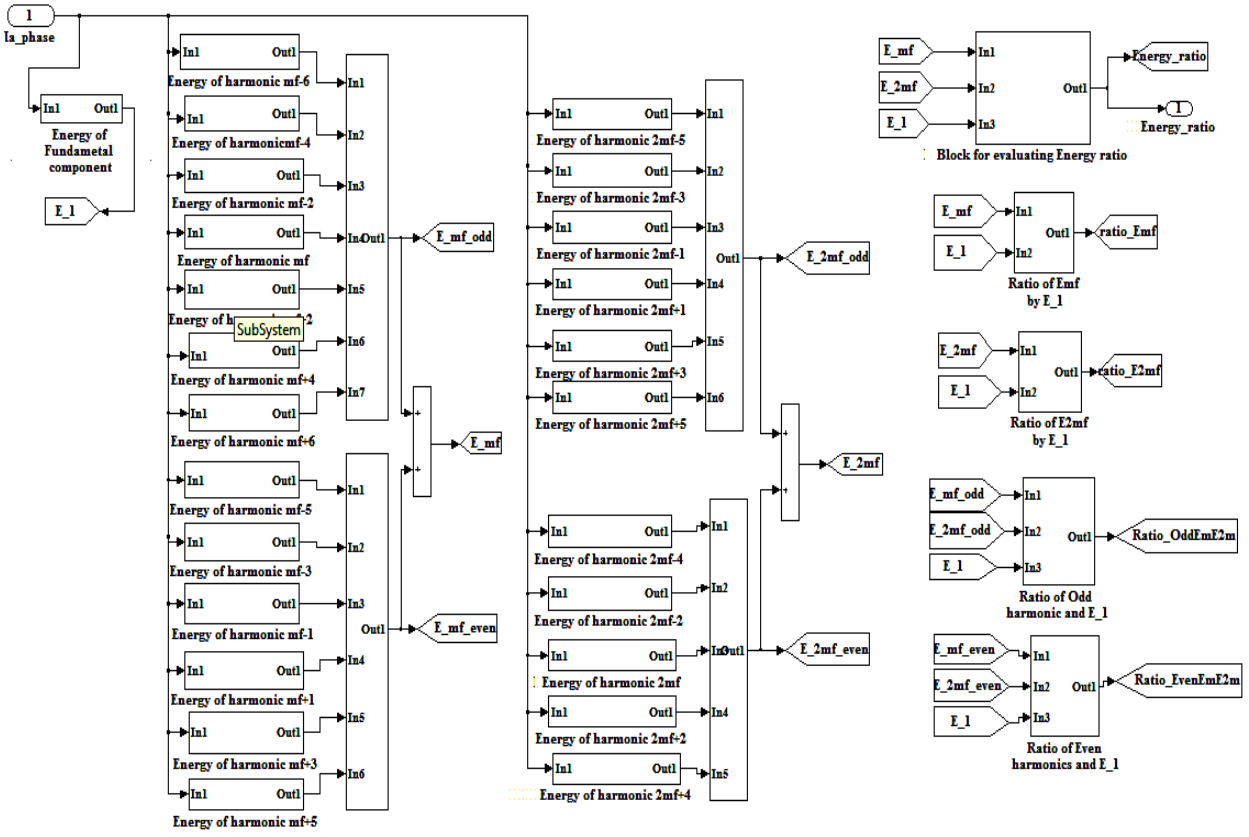


Figure 3.2 Section of Simulink model that is responsible for determination of factors E_{mf}, E_{2mf} and E_H.

in the harmonic band around m_f. Similarly E_2mf_even and E_2mf_odd represent the sum of energy residing in even and odd harmonics around the $2m_f$ region. These newly defined quantities are used for detailed analysis on effects of change of interleave angle on the total energy residing in even and odd harmonics in the output phase current. For sake of uniformity energy of even and odd harmonics are expressed as ratio of energy of fundamental component and tags named as Ratio_EvenEmf2Emf and Ratio_OddEmf2Emf are representing these two quantities.

For the system of three parallel inverters, simulation is carried out for the test case which has inverters in all the three channels staying ON during entire course of simulation. In order to verify theoretical concept presented earlier about Energy ratio it is required that the system be tested for different settings of interleave angle. A change in carrier phase shift resulting a change in Energy ratio(E_H) of the measured load side phase current would verify authenticity of the concept and will pave the path for development of final interleave control algorithm.

Simulation results shown in Fig. 3.3 up to Fig. 3.8 are pertinent to the case when 0º carrier phase shift is set between triangular wave generators associated with each of the three inverters. All the three channels stay in operational state during entire course of simulation which is set as 0.2 sec. Energy in fundamental harmonic component (E_1) is shown in Fig 3.3 and the corresponding Energy ratio (E_H) is illustrated in Fig. 3.4. Although the results tend to show an oscillatory behaviour in the start but after 0.12 sec magnitude of bounce seems to be more controlled.

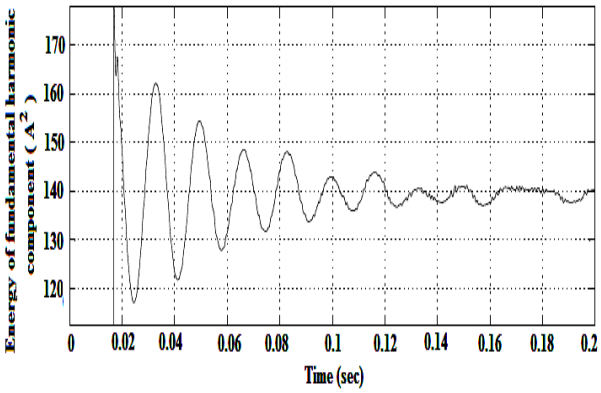


Figure 3.3 Energy recorded in E_1 for three channel system with 0º phase shift set between the three carrier signals.

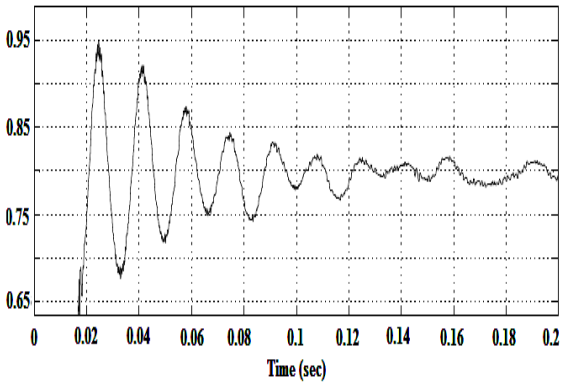


Figure3.4 Energy ratio for a three channel modular inverter system with interleave angle set equal to 0º.

The final steady values of E_1 and E_H are recorded in Table 3.2 for reference. The two ratios $Em_f/E1$ and $E2m_f/E1$ are shown in Fig 3.5 and 3.6 respectively and comparison between the two show that energy of harmonic around m_f tend to be is higher as compared to energy of harmonic around $2m_f$.

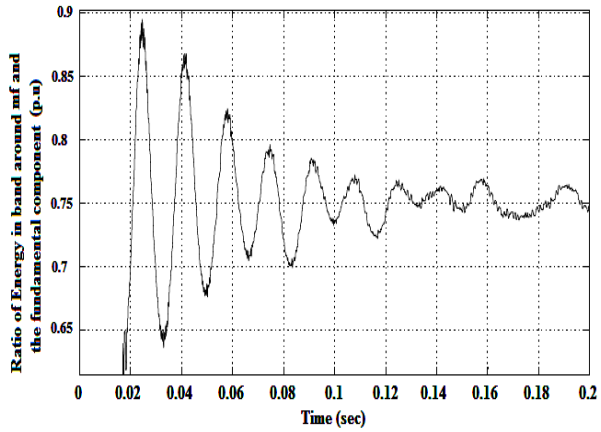


Figure 3.5 Ratio between E_{mf} and E_1 recorded for three channel modular inverter system with 0º interleave angle.

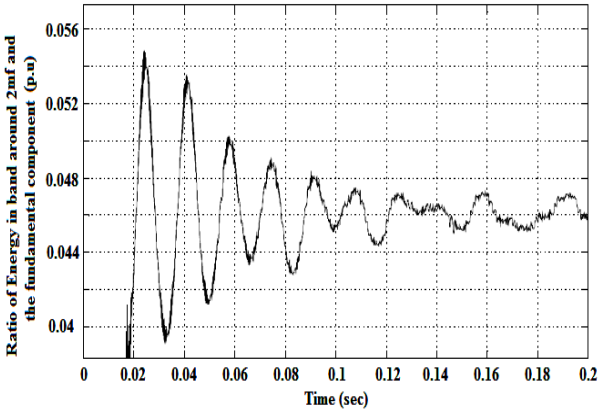


Figure 3.6 Ratio between E_{2mf} and E_1 recorded for three channel modular inverter system with 0º interleave angle.

Also in the model is provision made for recording total energy residing in the odd order and even order harmonics residing in the two bands. For sake of comparison these quantities are also expressed in terms of E_1 and are shown in Fig. 3.7 and 3.8 respectively.

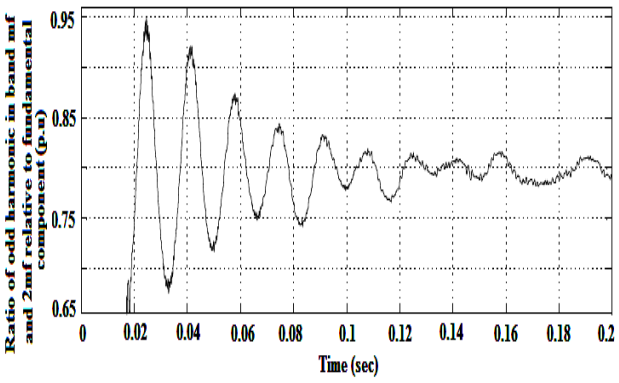


Figure 3.7 Ratio between sum of energy of all the odd harmonic in m_f and 2 m_f band with respect to energy of fundamental harmonic component.

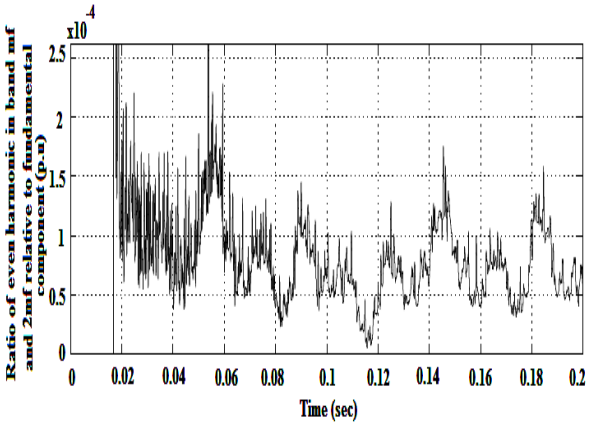


Figure 3.8 Ratio between sum of energy of all the even order harmonic in m_f and 2 m_f band with respect to energy of fundamental harmonic component.

By looking at the last two figures it can be seen that amount of energy in even order harmonics is negligible compared to the energy content of the odd order harmonics which is in agreement with the fact that the carrier frequency chosen for simulation is multiple of 3 and an odd multiple of systems nominal frequency of 60 Hz. The more steady value of all these different energies are obtained close to the end of simulation period and are listed in Table 3.2 for reference.

Simulation of the same system is also carried out for various setting of interleaving angle. This is done in order to see how the carrier phase shift affects the measured Energy ratio. The different values of interleave angles chosen are 60º, 72º, 90º, 120º and 180º and for all these angles waveforms of both energy E_1 and E_H are recorded. These waveforms are pasted in column#2 and 3 of Table 3.3. Looking at the entries of this table we find that oscillatory behaviour of the two signals tend to become pretty steady close to the end of simulation. The steady values of E_1 and E_H alongside other measured quantities are listed in Table 3.4. Following important observations are made when the entries of Table 3.4 are reviewed:

- For the system of inverters with three parallel channels that stay operational during entire course of simulation Energy ratio (E_H) is found to be lowest for the case when interleaving angle set between the units is 120º.
- Ratio of sum of energy in harmonics around m_f relative to fundamental is lowest when interleaving angle between the parallel operating units is set equal to 120º.
- Ratio of sum of energy of all odd harmonics around band m_f and $2m_f$ relative to fundamental is also lowest for the case of 120º interleaving angle.

Table 3.2: Harmonic analysis of a system of three inverters feeding a common RC load and carrier phase shift set equal to 0º between the parallel operating units.

Energy in Fundamental component (E_1)	140.2 A^2
Ratio of Energy in band m_f relative to fundamental component (E_{mf} / E_1)	0.746
Ratio of Energy in band $2m_f$ relative to fundamental component (E_{2mf} /E_1)	0.046
Ratio of Energy of odd harmonic relative to fundamental component (E_{odd}/E_1)	≈ 0.792
Ratio of Energy of even harmonic relative to fundamental component (E_{even}/E_1)	0.000064
Ratio of Sum of Energy in band m_f and $2m_f$ relative to fundamental component i.e Energy Ratio (E_{mf}+E_{2mf}/E_1)	***0.792***

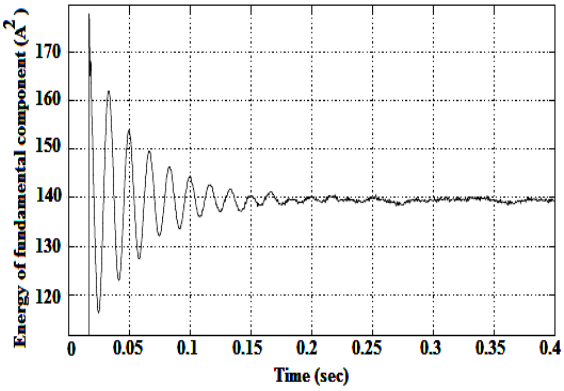
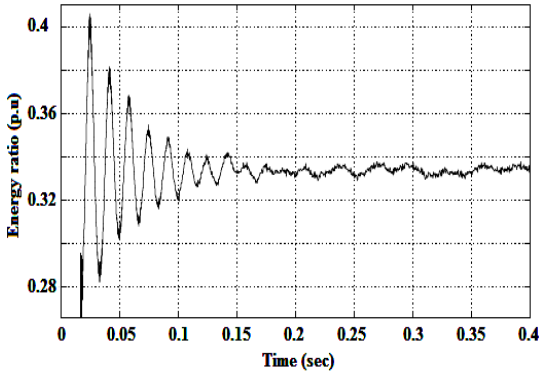
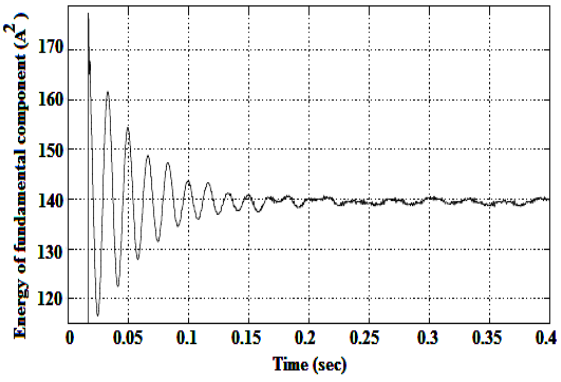
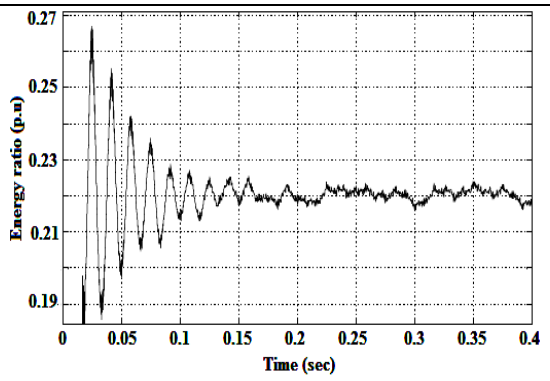
Observations made with reference to the three parallel inverter system is very important as it verifies our idea that Energy ratio (E_H) is affected by selection of carrier phase shift between units of the modular converter system. Also value of E_H is minimum for the case when the interleave angle satisfies the criterion given by (3.11).

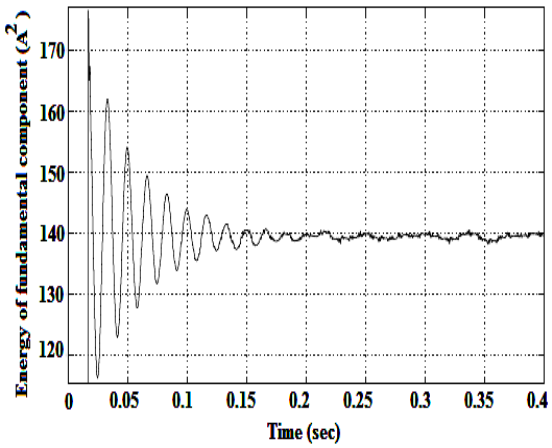
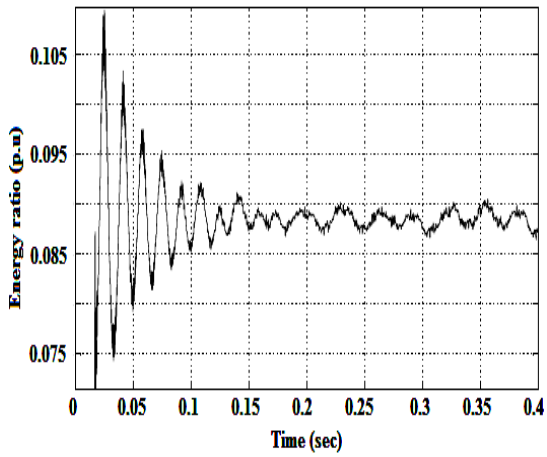
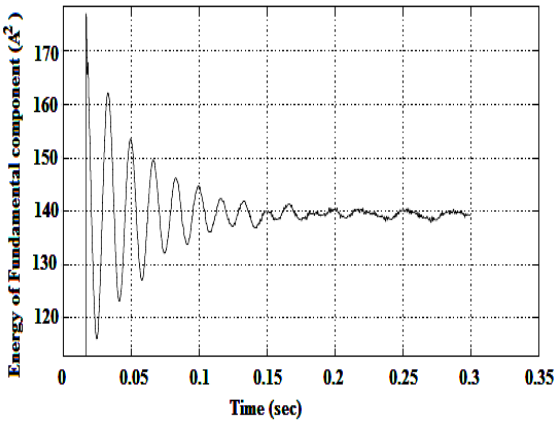
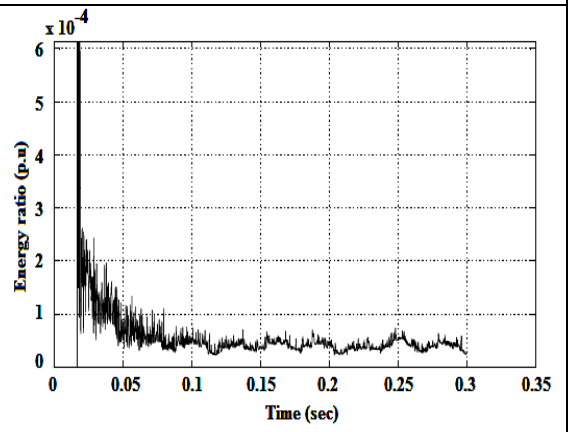
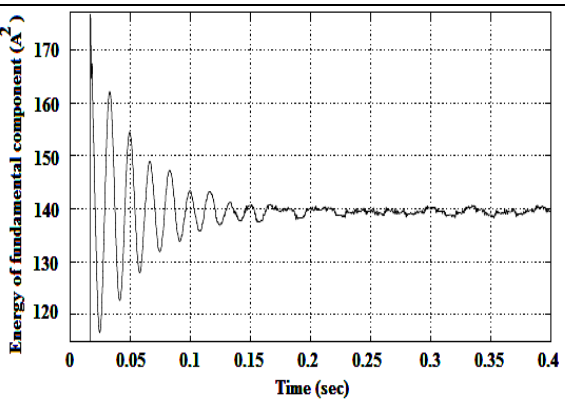
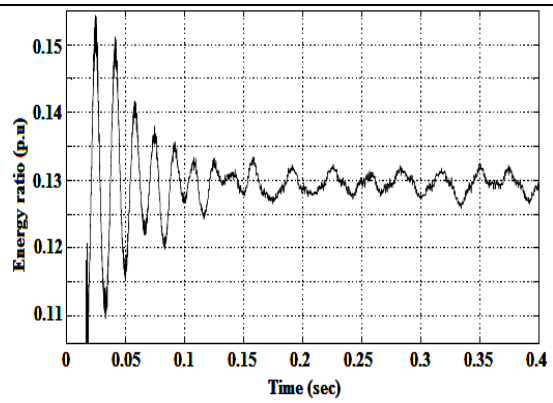
$$\text{Best interleaveangle} = \frac{360^\circ}{n} \tag{3.11}$$

where n = number of parallel units in operation

Before generalizing the result it is important to verify the idea on a system of inverters that has parallel modules other than three. For this reason models were developed for five as well as two channel inverter system. Simulations were carried out in both cases and results were analyzed.

Table 3.3 Energy ratio (E_H) and energy of fundamental component (E_1) recorded for three inverter system by setting different values of interleaving angle between the units.

Angle	Energy of fundamental component of load side phase current.	Energy ratio recorded for load side phase current.
60º		
72º		

Angle	Energy of fundamental component of load side phase current.	Energy ratio recorded for load side phase current.
90º		
120º		
180º		

In Table 3.5 and Table 3.6, results obtained by running simulation for modular inverter system with five and two channels respectively are listed. Like the previous case simulation for both these systems were carried out by setting different values of interleaving angles between the units in operation.

Table 3.4: Analysis of a system of three inverters conducted by setting different values of carrier phase shift between the parallel operating units.

Interleaving Angle	0º	60 º	72 º	90 º	120 º	180 º
Energy in Fundamental component (E_1)	140.2 A^2	139.3 A^2	139.9 A^2	139.6 A^2	139.2 A^2	139.5 A^2
Ratio of Energy in band m_f relative to fundamental component (E_{mf} / E_1)	0.746 p.u	0.3352 p.u	0.2179 p.u	0.08226 p.u	0.000025 p.u	0.083 p.u
Ratio of Energy in band $2m_f$ relative to fundamental component (E_{2mf} /E_1)	0.046 p.u	0.000005 p.u	0.00204 p.u	0.00517 p.u	0.0000047 p.u	0.046 p.u
Ratio of Energy of odd harmonic relative to fundamental component (E_{odd}/E_1)	≈ 0.792 p.u	0.3351 p.u	0.2199 p.u	0.08741 p.u	0.000022 p.u	≈0.1291 p.u
Ratio of Energy of even harmonic relative to fundamental component (E_{even}/E_1)	0.000064 p.u	0.000038 p.u	0.000031 p.u	0.000019 p.u	0.0000077 p.u	0.0000258 p.u
Ratio of Sum of Energy in band mf and $2m_f$ relative to fundamental component i.e Energy Ratio (E_H=(E_{mf}+E_{2mf})/E_1)	0.792 p.u	0.3352 p.u	0.22 p.u	0.08743 p.u	0.0000297 p.u	0.1291 p.u

Table 3.5: Analysis of a system of five inverters conducted by setting different values of carrier phase shift between the parallel operating units.

Interleaving Angle	0º	60 º	72 º	90 º	120 º	180 º
Energy in Fundamental component (E_1)	142 A^2	140.4 A^2	141.6 A^2	141.4 A^2	140.6 A^2	141.2 A^2
Ratio of Energy in band m_f relative to fundamental component (E_{mf} / E_1)	2.529 p.u	0.1023 p.u	0.0000536 p.u	0.1009 p.u	0.1026 p.u	0.1002 p.u
Ratio of Energy in band $2m_f$ relative to fundamental component (E_{2mf} /E_1)	0.1311 p.u	0.00537 p.u	0.0000145 p.u	0.005263 p.u	0.005219 p.u	0.1322 p.u
Ratio of Energy of odd harmonic relative to fundamental component (E_{odd}/E_1)	2.66025 p.u	0.107668 p.u	0.0000503 p.u	0.10616 p.u	0.10776 p.u	0.23239 p.u
Ratio of Energy of even harmonic relative to fundamental component (E_{even}/E_1)	0.0000384 p.u	0.0000187 p.u	0.0000178 p.u	0.0000279 p.u	0.0000218 p.u	0.0000211 p.u
Ratio of Sum of Energy in band mf and $2m_f$ relative to fundamental component i.e Energy Ratio (E_H=(E_{mf}+E_{2mf})/E_1)	2.66029 p.u	0.107687 p.u	0.0000681 p.u	0.10619 p.u	0.10778 p.u	0.23241 p.u

Table 3.6: Analysis of a system of two inverters conducted by setting different values of carrier phase shift between the parallel operating units.

Interleaving Angle	0º	60 º	72 º	90 º	120 º	180 º
Energy in Fundamental component (E_1)	139.5 A^2	138.8 A^2	139.3 A^2	139.2 A^2	138.5 A^2	138.8 A^2
Ratio of Energy in band m_f relative to fundamental component (E_{mf} / E_1)	0.3002 p.u	0.2271 p.u	0.1964 p.u	0.1506 p.u	0.0761 p.u	0.00001138 p.u
Ratio of Energy in band $2m_f$ relative to fundamental component (E_{2mf} /E_1)	0.01984 p.u	0.00507 p.u	0.001865 p.u	0.0000048 p.u	0.00499 p.u	0.02002 p.u
Ratio of Energy of odd harmonic relative to fundamental component (E_{odd}/E_1)	0.319986 p.u	0.23215 p.u	0.198227 p.u	0.150602 p.u	0.081073 p.u	0.0200245 p.u
Ratio of Energy of even harmonic relative to fundamental component (E_{even}/E_1)	0.0000045 p.u	0.0000124 p.u	0.0000035 p.u	0.0000074 p.u	0.00000397 p.u	0.00000307 p.u
Ratio of Sum of Energy in band mf and $2m_f$ relative to fundamental component i.e Energy Ratio (E_H=(E_{mf}+E_{2mf})/E_1)	0.31999 p.u	0.23216 p.u	0.198231 p.u	0.150609 p.u	0.081077 p.u	0.02003p.u

By comparing entries of different columns in Table 3.5 it is seen that the lowest values of Energy ratio is obtained when the carrier phase shift between five parallel units is adjusted equal to 72º

which is in agreement with the criterion given in (3.11). It is important to mention that during entire course of simulation all the five inverters remained in operational mode. Looking at the entries of Table 3.6 it is seen that energy ratio turns out to be minimum for the interleave angle set equal to 180 º between the two parallel operating inverter units. Hence the observations made previously for the case of three inverter system, seems to remain valid even in case of set up with five and two channels. Based on this result we can generalize our observation and say that the Energy ratio is reflective of system harmonics and yields lowest value for the case of best possible interleaving angel set between units in operation. Using Energy ratio in determination of appropriate carrier phase shift between the units of modular converter system is therefore justified. This result is of prime importance as based on the Energy ratio calculation interleaving control algorithm for modular converter system will be developed.

3.3 Different stages of algorithm development

Based on the information acquired from preceding section, it is now possible to move forward with the developmental phase of the control algorithm for interleaving of parallel operating inverter system. There are three main stages in which model for interleaving controller will be developed in Simulink. Each development stage is aimed at providing solution for one of the three challenges identified earlier in this chapter.

3.3.1 First stage

Partial answer to the first challenge in design of controller was given in the last section and controllers associated with each of the inverter module will determine Energy ratio of the total load-side phase current. Usually the modular system is designed keeping in view redundancy criteria of n-1 in mind. Meaning that failure of one of the channels will still allow the system to supply the network it is connected to without any interruption. However while designing the interleaving controller we will look at all the possible scenarios which can be encountered in modular converters. For system shown in Fig. 3.1, we have three possible values of interleave angle which are listed as under:-

- All the three modules are operating leading to best possible interleave angle of 120º.
- Two of the three units remain operational after failure of one of the channels. In this case the interleave angle between the units in operation will be 180º.
- The third possibility (which is non-existent for three inverter system with n-1 redundancy)

is when only one of the unit is operational and the other two modules are shut down. Concept of carrier phase shift is pointless in this case however for defining a generalized control algorithm we assume the carrier phase for the working unit be 0º in this situation.

As Energy ratio is very sensitive to the harmonics generated in the system and varies significantly with the change in interleave angle hence one possible approach in design of automatic interleaving control algorithm will be:-

- Set different values of interleaving angles. It is important to mention here that an exhaustive selection of interleave angle is totally un-necessary. Based on the discussion made earlier, for three inverter system possible values of carrier phase shift is limited to three only, namely 0º, 120º or 180º.
- Record the Energy ratio (E_H) of the total load side phase current for each of the case.
- Compare the values of E_H and determine the minimum of the lot.
- Angle corresponding to minimum E_H will be the best possible value for interleaving.
- Maintain the selected value of interleave angle unless there is change in total number of modules in operation.

The approach used above is based on the Perturb and Observe algorithm also popularly referred to as P&O algorithm. Hence applying selected values of interleave angle and observing the effect of each case on Energy ratio would lead to determination of correct interleave angle for system of parallel modules.

From the simulation results shown in last section it was noted that E_H took some time in settling down to a relatively steady value after start of simulation. As change in E_H is consequence of the change in harmonics hence for accurate prediction of interleave angle it is important to give a time gap between change of angle and recording of corresponding value of Energy ratio. The value of time gap selected is at least T_1sec ($T_1=1/f_1$, where f_1 is frequency of fundamental component of inverters output i.e 60 Hz) giving enough time for E_H to settle down. Flow chart of the developed interleave control algorithm for a three channel system is shown in Fig. 3.9.

Extending this algorithm to any number of parallel operating units is possible. Consider case of five inverter system the only difference compared to this one will be in the number of search points. The possibilities of interleaving angle for five converter system are limited to five search points which are 72º, 90 º, 120 º, 180 º or 0 º. With all the five units in ON state the angle will be set to 72º and scenario in which only one of the channels is working while the other four are non-

operational will correspond to 0 º carrier phase for the working module.

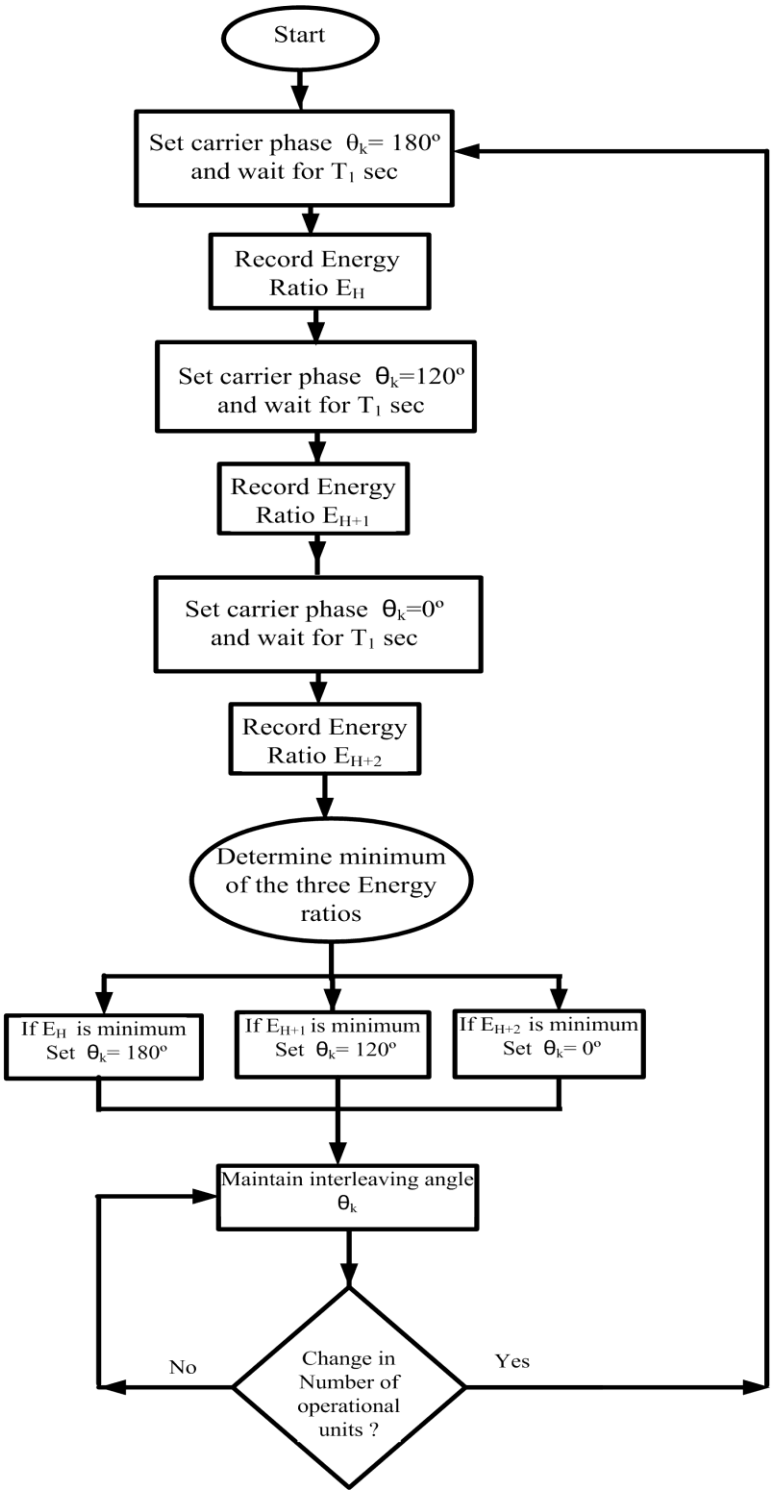


Figure 3.9 P & O algorithm for determining best interleaving angle for system of three parallel inverters.

Matlab implementation of this section of the model will be discussed once the solution to all three design challenges has been provided.

3.3.2 Second stage

Knowledge of best interleave angle depending on the number of operational units, is not enough for completing the task of automatic interleaving. The next step in the process requires each converter to exactly adjust its carrier phase relevant to other units. In order to understand the idea let us consider the case of three parallel connected inverters. When inverters in all the three channels are in ON state then based on (3.11), the best interleave angle should be 360º/3 (i.e 120 º). With successful implementation of 1st stage in design of interleaving algorithm the controller associated with each of the converter unit will successfully establish the correct value of interleaving angle however carrier phase of all the inverters cannot be set equal to 120 º. Rather the carrier phase of the three converters should be evenly spread over the entire switching period with carrier phase offset for converter number 1, 2 and 3 set equal to 0º, 120º and 240 º respectively.

A simple approach used for resolving this issue is based on allocation of a token number for each of the unit in operation. Carrier phase of an inverter will be decided based on the product of its token number with the best interleave angle discovered earlier. Hence for a three inverter system token number assigned to the first inverter in the top down fashion will be zero and for the following modules, their token number will be set one greater than their predecessor unit. Section of control algorithm dealing with token generation has a centralized structure with one unit responsible for generating token numbers for all the inverters in operation. The only information token generator needs is the ON/OFF status of all the inverters units.

It is important to consider the scenario when all the converters in the group are not operational. The algorithm deals with such a scenario in two different ways:

- If inverter that is non-operational is the first in the chain of inverters then token number allocated to it will be “-1”.
- If the converter other than the first in the chain is OFF then its token number will remain equal to its predecessor’s token ID.

These tokens once determined are maintained until a change in the number of converter modules takes place. Flow chart of the section of algorithm responsible for token generation is shown in Fig. 3.10.

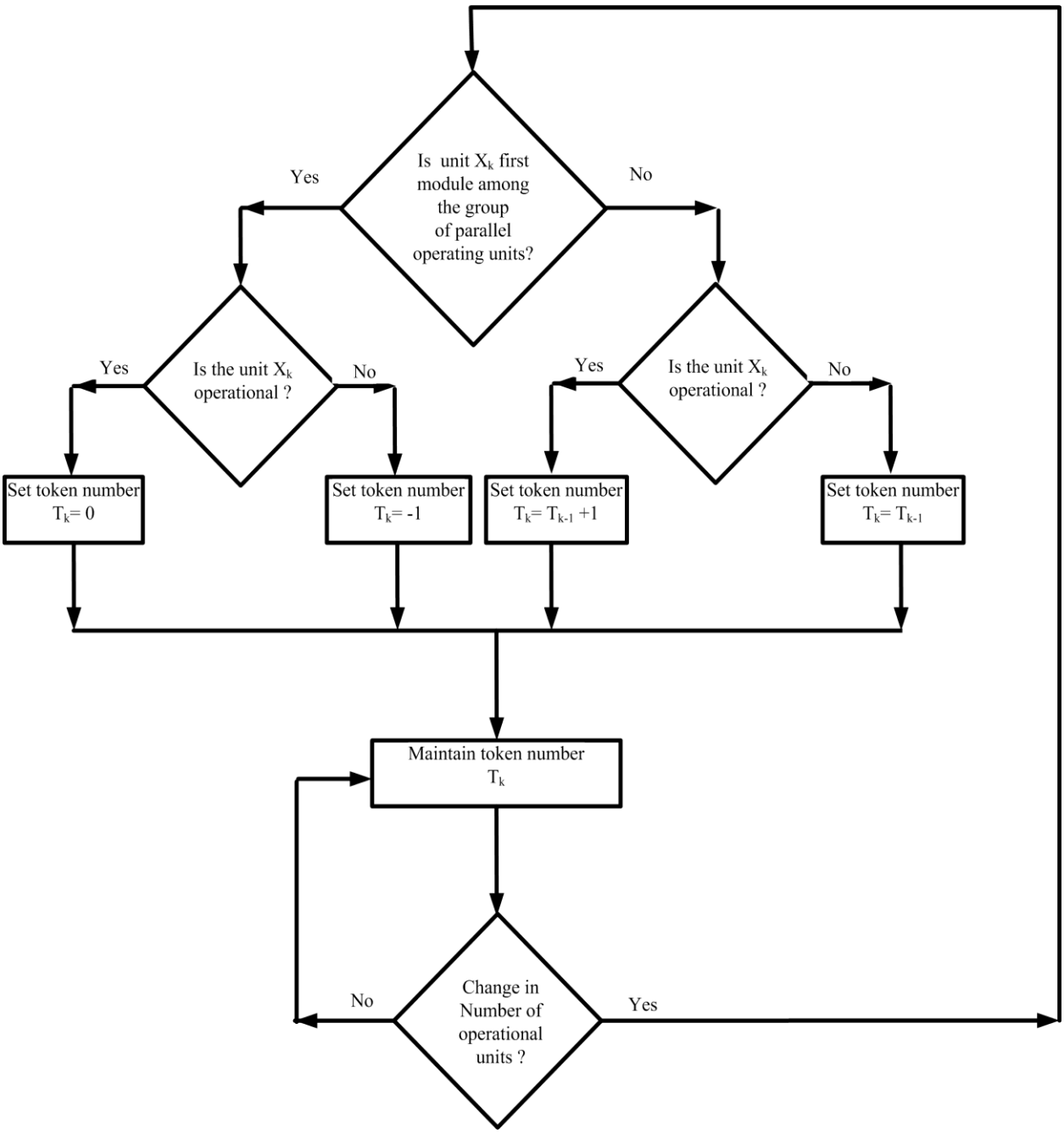


Figure 3.10 Section of algorithm responsible for determination of token number.

The last stage of block diagram Fig. 3.10 deals with updating of token numbers whenever a change in ON/OFF status of any of the inverter in the system occurs. To emphasize importance of this step, consider case when in a three inverter system all units are in operational mode in the start. According to the algorithm token number allocated to the three units will be 0, 1 and 2. The relative carrier phase for the three units will be set equal to 0º, 120º and 240º respectively. If after

a while inverter #2 is shut down then the interleave angel evaluated by control algorithm will be 180 º. However if the system fails to update the corresponding token numbers then carrier phase for the inverters will turn out to be 0 º, 180 º and 360 º respectively. The two inverters that are operational are inverter #1 and #3 and it is evident that with these token numbers in place, carriers for the two units are operating in a synchronized fashion which ultimately lead to an increased level of harmonics produced in the system. Based on this argument it is concluded that re-estimation of token numbers as soon as the system experiences a change in number of operational units is a must for control algorithm to work accurately.

3.3.3 Third stage

From the discussion of last two sub-sections one thing is found to be common in both cases. The commonality lies in the fact that both sections of the controller should be in active mode at the start of simulation and should also get triggered whenever system experiences a change in operational status of any of the modules. Resetting feature comes naturally to the token generator unit due to its direct dependence on the ON/OFF status of individual inverter units. However part of control algorithm dealing with the determination of best interleave angle should have some sort an external reset signal provided to it whenever a change in the any of the converter status takes place. Keeping this in view a reset block is needed in the controller that will have a centralized structure. Inputs to this block will be signals depicting ON/OFF status of each and every module present in the system and its single output named RESET will be shared by all the individual controllers in the set up.

3.3.4 Simulink model based on developed control algorithm

Keeping in view the algorithm established in the last three subsections, Simulink model is constructed for automatic interleaving of system of three inverters. Overview of interleaving controller developed in MATLAB for such a system is shown in Fig. 3.11. The subsystem on top left side of this figure with tag named Ia_Load has the structure similar to Fig. 3.2 and evaluates Energy ratio of the system by conducting harmonic analysis of load-side phase current. Energy ratio (E_H) determined is given as input to each controller that is associated with one of the parallel inverter unit. Inner view of controller block titled *controller for converter #1* is shown in Fig 3.12. This block determines best possible interleaving angle and then combines the information provided by it with the central token generator to decide carrier phase in radians for the first inverter. The other two blocks which are responsible for performing the same function

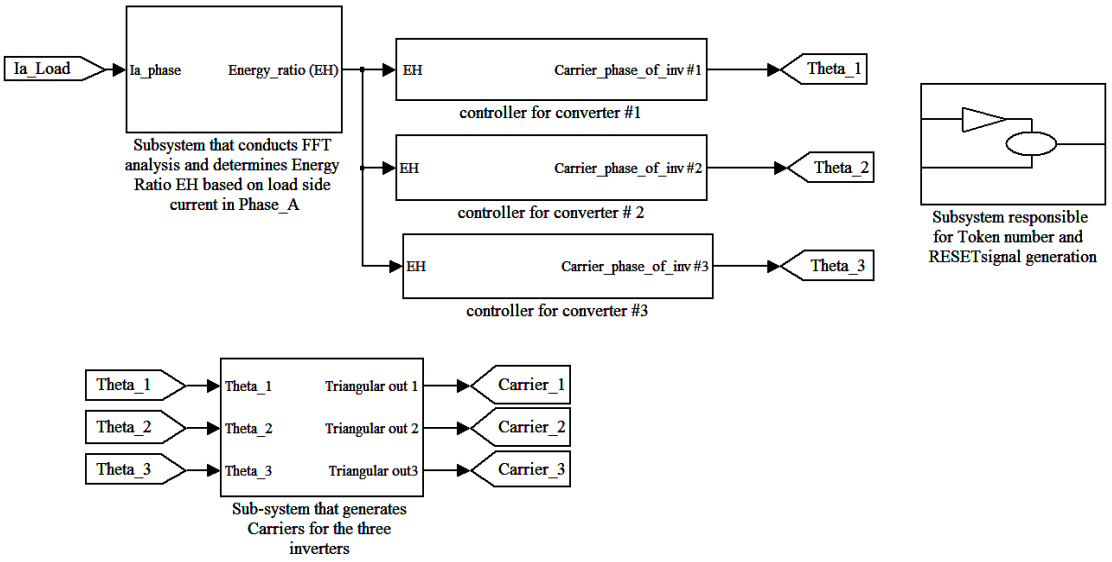


Figure 3.11 Complete Simulink model of Automatic Controller for Interleaving of modular inverter system having three channels.

for their respective inverter modules are titled *controller for converter #2* and *controller for converter #3* and can be seen in Fig. 3.11. Section of the model with centralized structure which is responsible for token generation and reset signal is shown in Fig.3.13. It can be seen that the only inputs both in case of token generator and reset block are the on/off status of the three inverters represented by tags *Gate_1, Gate_2* and *Gate_3*.

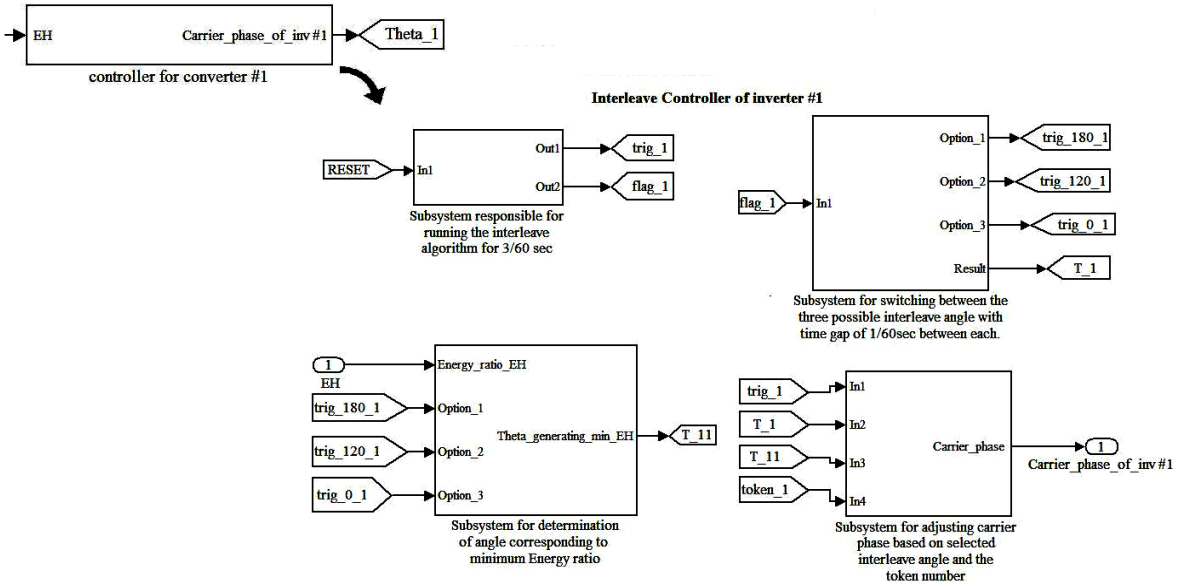


Figure 3.12 Inner view of model for controller evaluating carrier phase for inverter #1.

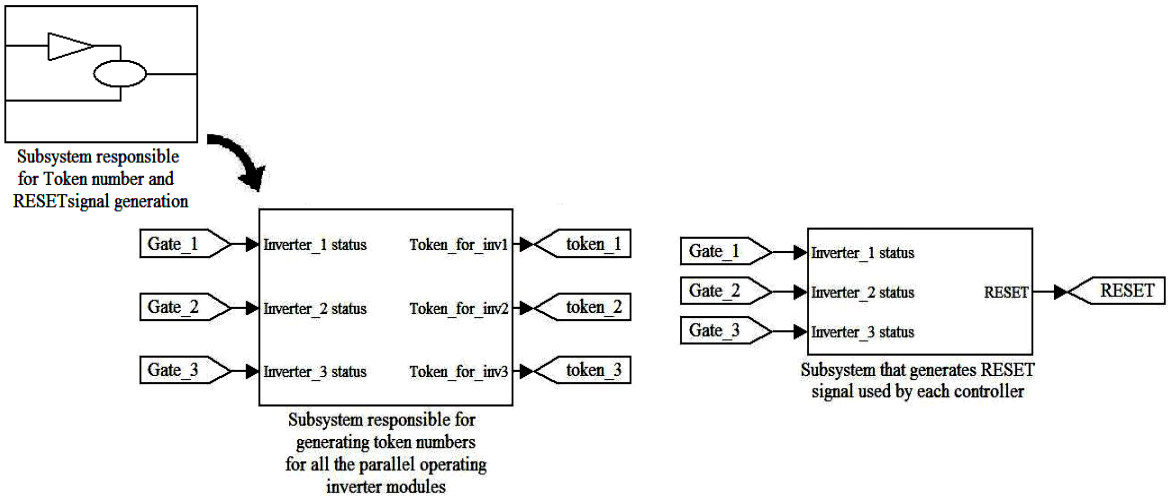


Figure 3.13 View of section in the model that generates token numbers and reset signal for all the controllers.

In Fig 3.14 is shown inner view of the subsystem that decides the value of best interleaving angle. Possible interleave angle for a three module system i.e 180º, 120º and 0º are selected one after the other and the energy ratio for each of the three cases is recorded making use of D latches available in Simulink library. On comparison, minimum of the three energy values is selected by the block appearing in the right most corner of Fig 3.14. In the same block, angle pertinent to lowest E_H is selected, hence best interleave angle is the only output of this block and is named as *Theta_1*.

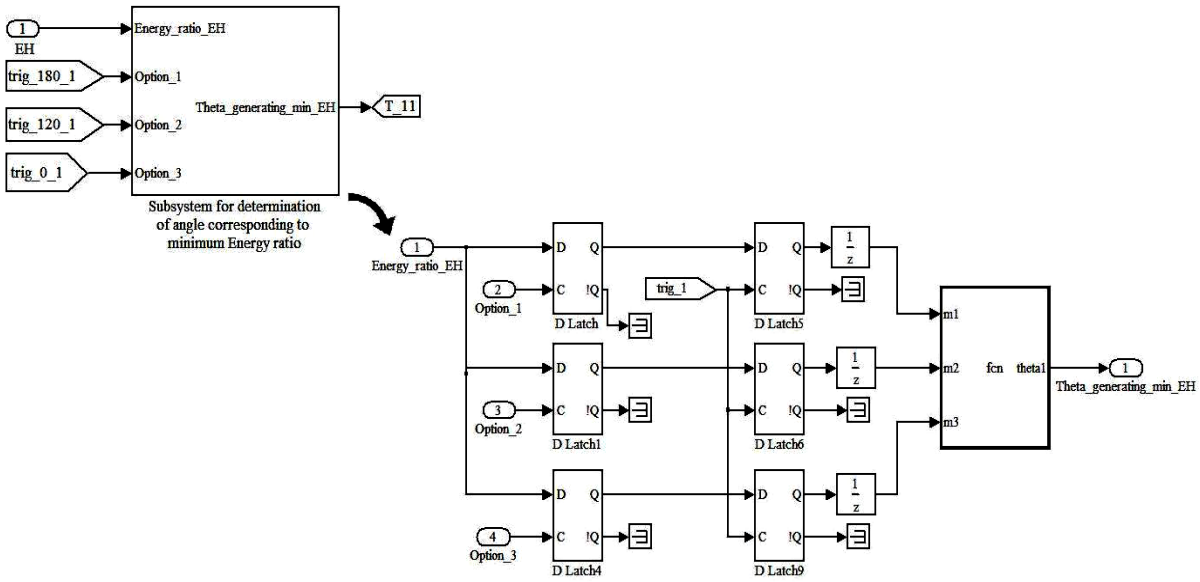


Figure 3.14 Part of model that determines best interleaving angle based on values of E_H.

In Fig. 3.15 is shown subsystem that generates three carrier signals for the three inverters present in the system. Inputs to this block are carrier phases generated by the controllers for three inverters.

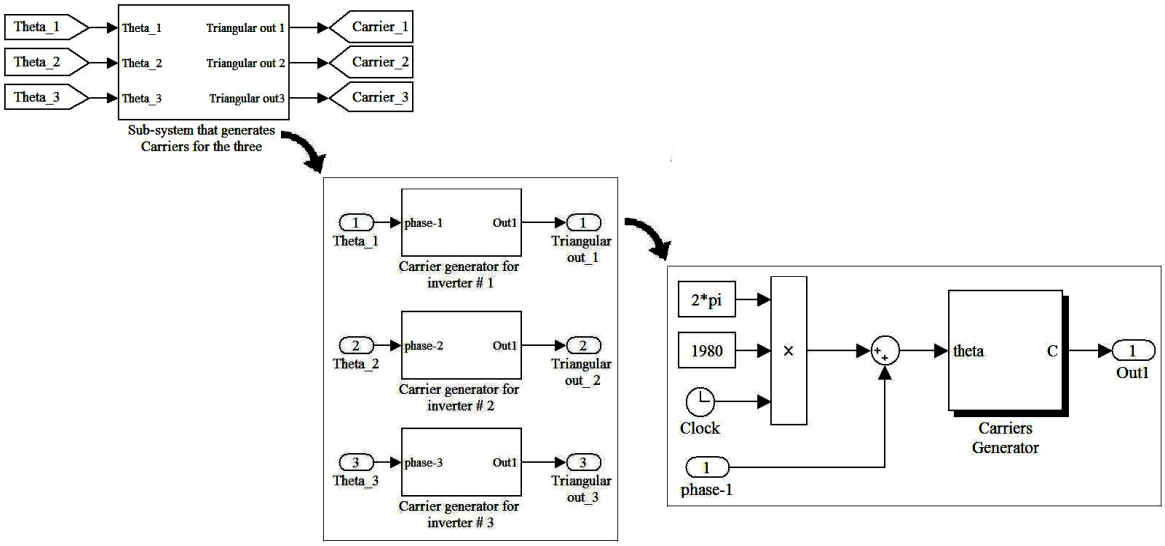


Figure 3.15 Part of the Simulink model that is responsible for generation of carrier signals for inverter modules operating in the system.

This concludes discussion on the section of the Simulink model for automatic interleaving of modular inverters. In the coming section results obtained by running the model will be discussed.

3.4 Simulation results

3.4.1 System of parallel inverters feeding common RC load

To test functionality of developed control algorithm, parallel inverter system of Fig. 3.1 was tested with all three inverters in ON state at the start of simulation. In order to see if the controller is able to respond accurately in case of a channel failure, inverter # 3 is shutdown at 0.14 sec for a time period of 0.12 sec. The current flowing in phase-A at the load end is given in Fig. 3.17 and the Energy ratio measured using this current is shown in Fig. 3.18. The carrier phase in radians for all three inverters are shown Fig 3.19 up to Fig. 3.21.

As per previous discussion it is expected that the interleaving control algorithm should be triggered three times during entire course of simulation and the simulation results support this fact. Whenever the controllers gets triggered the system is tested by setting the three possible interleave angles (180º, 120º and 0º) and the one yielding minimum value of E_H is selected.

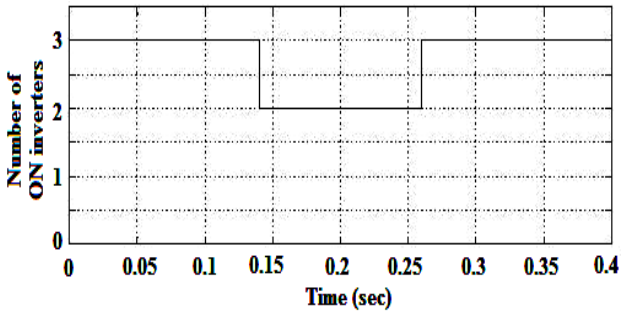


Figure 3.16 Number of inverters in ON state for system with three channels.

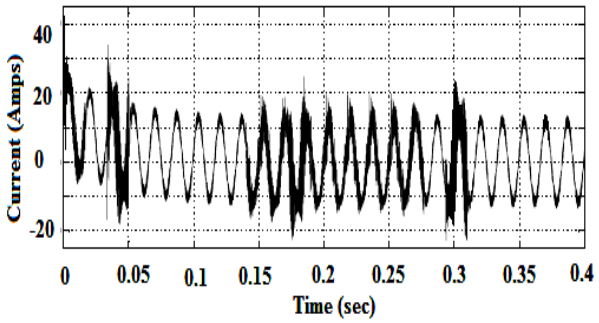


Figure 3.17 Total load-side phase-A current for a three channel inverter system.

The decision about best interleave angle is reached after 3/60 sec (i.e 0.05 sec) of the change in status of the number of operational units and angle once decided is maintained till a change in any of the inverter's status is experienced by the system. Total number of operational units at one time is depicted in Fig. 3.16. By looking at Fig. 3.18 and Fig. 3.17 it is noted that when carrier phase displacement is equal to its desired value, the Energy ratio is prominently low and waveform of load side current is smoother because of low level of system harmonics.

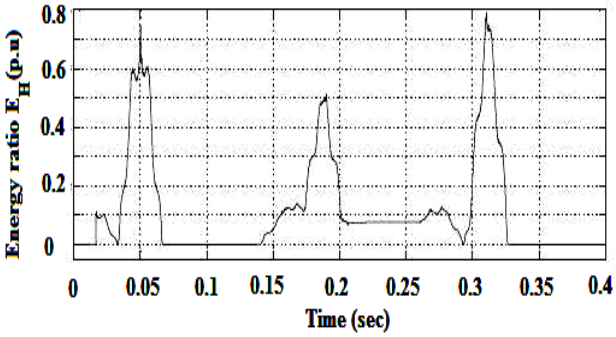


Figure 3.18 Energy ratio measured for the case of a three channel modular inverter system.

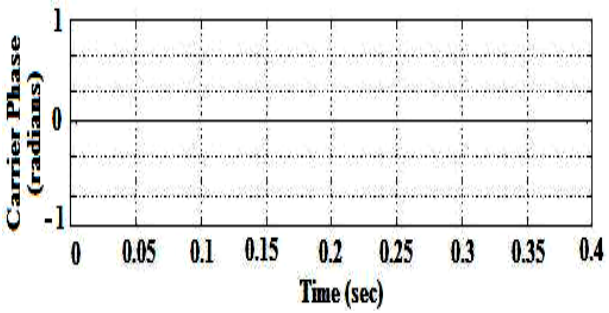


Figure 3.19 Carrier phase of first inverter recorded in case of a three channel inverter system.

Token generator is also working as per designed algorithm of Fig. 3.10. Token numbers allocated to the three inverter are 0,1 and 2 respectively in case when all three units are ON. The carrier phase of inverter # 2 and # 3 are similar to one another during the time gap when inverter # 3 was turned off. This is also in accordance with the devised algorithm for token generation which states that when an inverter is off (and if it is not the first inverter in the chain) then its

token number will be similar to its predecessor unit. The results show satisfactory performance of system with automatic interleaving controller deciding carrier phase displacement between the three parallel operating inverters.

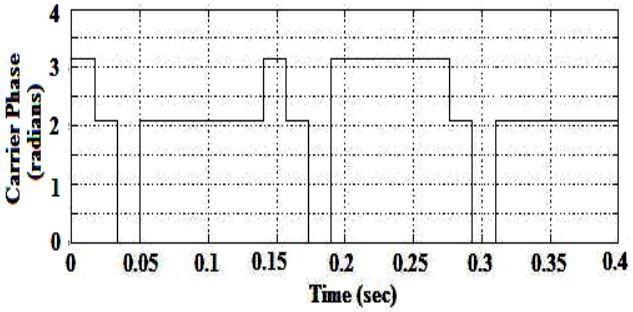


Figure 3.20 Carrier phase of second inverter recorded in case of a three channel system.

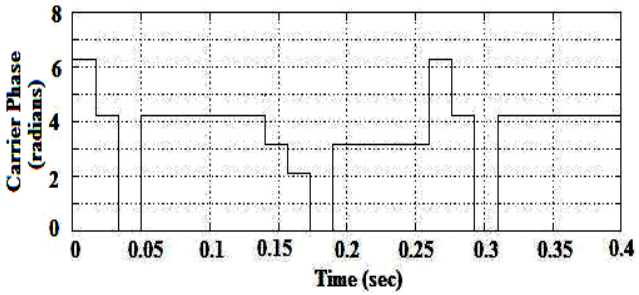


Figure 3.21 Carrier phase of third inverter recorded in case of a three channel system.

To further verify the developed controller, system with five parallel operating units was also simulated and the test results for the same are shown in Fig. 3.22 up to Fig. 3.29. The system has all five units operating in the start and the best interleaving angle is decided accurately as being 72º (1.2566 radians). Numbers of inverters operational at one time are shown in Fig. 3.22.

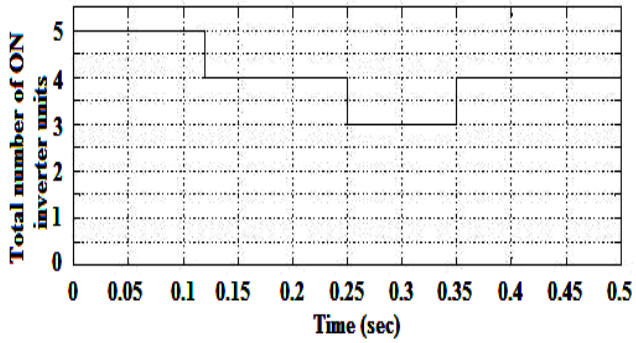


Figure 3.22 Number of inverters in ON state for a system with five channels.

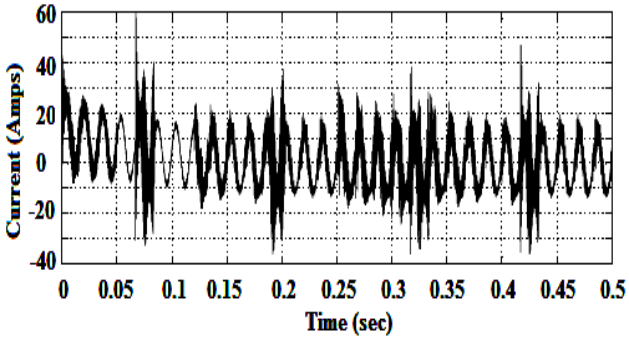


Figure 3.23 Total load-side phase-A current for a five channel inverter system.

For the test case inverter at position no.4 is turned off at time 0.12 sec and remains off till the end of simulation. However inverter no.3 is turned off at time 0.25 sec and gets back in operational mode at 0.35 sec. Control algorithm as expected is triggered four times during the entire course

of simulation and looking at the carrier phases for the five inverters the system has been successful in determination of interleave angle all the four times.

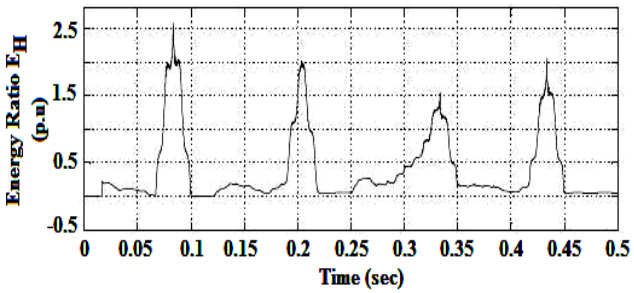


Figure 3.24 Energy ratio measured for the case of a five channel modular inverter system.

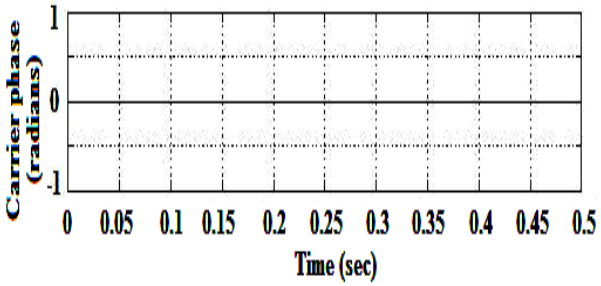


Figure 3.25 Carrier phase of first inverter recorded in case of a five channel inverter system. .

Total time that the algorithm takes for reaching the decision about best interleave angle is 5/60 sec (0.0833 sec). Reason for longer decision time by five inverter system is because this set up has to test five possible interleave angles namely 180º, 120º, 90º, 72º and 0º before verdict about most suitable angle is reached.

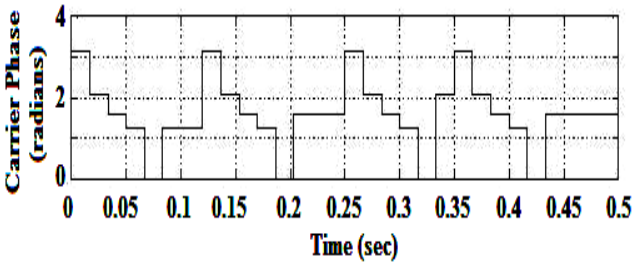


Figure 3.26 Carrier phase of second inverter recorded in case of a five channel modular inverter system.

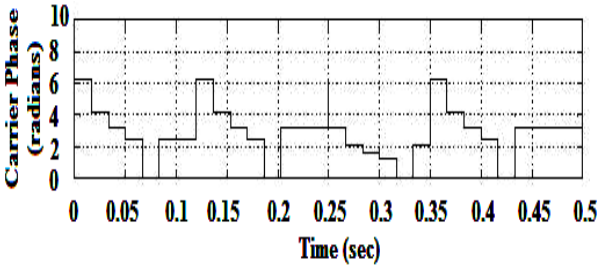


Figure 3.27 Carrier phase of third inverter recorded in case of a five channel modular inverter system.

Looking at Fig. 3.23, it is seen that the waveform of load side current in phase A is smoother in the time span when the system is operating with carrier phase displacement according to the criterion described by (3.11). Similarly Fig. 3.24 shows minimal value of Energy ratio obtained for this system when the carrier phase depending on the number of ON inverters at that time is equal to its most suitable value.

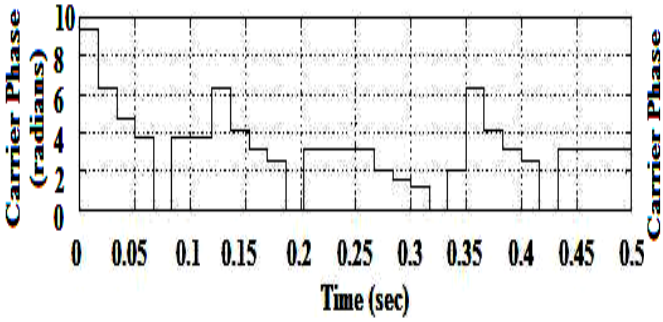


Figure 3.28 Carrier phase of fourth inverter recorded in case of a five channel modular inverter system.

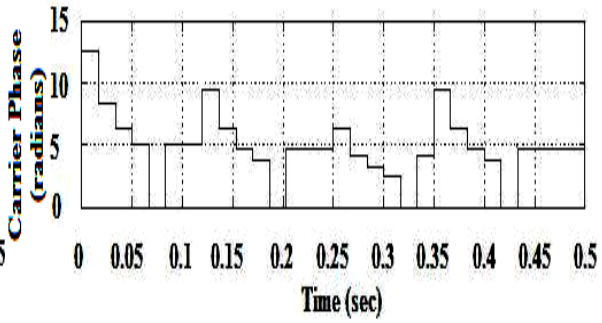


Figure 3.29 Carrier phase of fifth inverter recorded in case of a five channel modular inverter system.

3.4.2 Results of WECS with interleaving controller

System developed in the previous section is now incorporated with a 4MW, six-phase, PMSG based WECS with two converter modules operating in parallel and Simulink model for the same is shown in Fig. 3.30. Parameters for this system are given in appendix A-1 for reference. As seen in the model, setup is composed of two parallel channels with AC/DC and DC/AC converters present in each path. With controllers for determination of interleaving angle of converter unit in place, the system is simulated in discrete mode with sampling time of 10^{-5} sec and carrier frequency of 1980 Hz.

This model for WECS is tested for different scenarios such as the case when both the converters stay ON during entire course of simulation or when one of the converters is temporarily shut down and resumes normal operation later on and lastly when one of the channels after being disabled stay in OFF state till the end of simulation. For all the test cases the system performed satisfactorily and correct interleave angle was selected by the interleaving control algorithm based on harmonic analysis conducted using total grid-side phase current. The results included here are for one the test case when converters (both rectifier and inverter module) of channel 1 remain ON throughout the simulation time period of 0.12 sec.

From Fig. 3.31, it is seen that one of the converter (i.e converter # 2) is turned off (at time t =0.5 sec) and back on again after a while (i.e at t=0.65 sec). Reference signal for Electromagnetic Torque used for each machine-side controller is given in Fig. 3.32, which is followed closely by channel-1 converter module as is evident from Fig. 3.33. Measured electromagnetic torque for the other channel is shown in Fig. 3.34 which seems to follow its reference value throughout, except

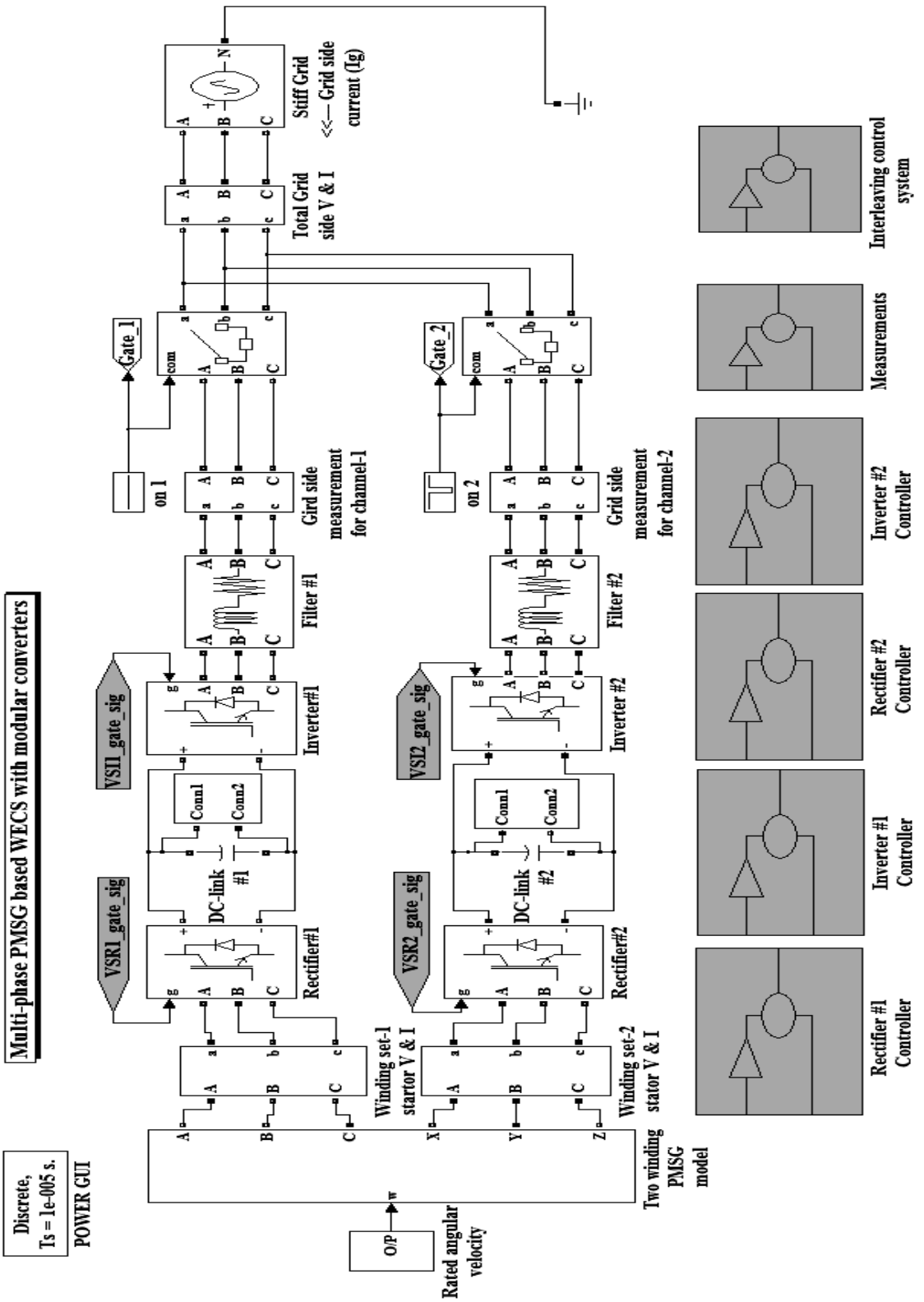


Figure 3.30 Simulink model for six-phase PMSG based WECS with automatic interleaving of modules.

for a time span of 0.15 sec when this channel is non-operational. Measured stator side current for channel-1 and 2 are shown is Fig. 3.35 and Fig. 3.36 respectively and as per system parameters frequency of this signal is 11.3 Hz.

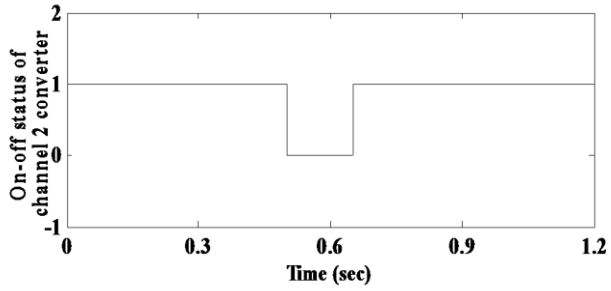


Figure 3.31 On/off status of converter in channel #2.

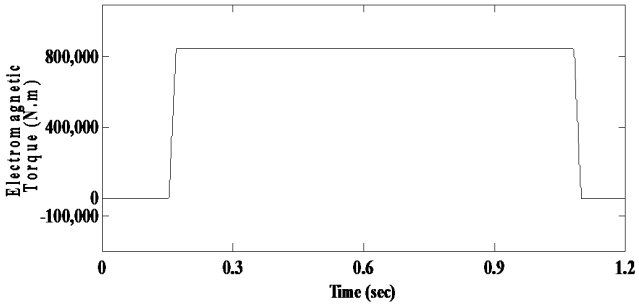


Figure 3.32 Reference Electromagnetic torque for each machine side converter.

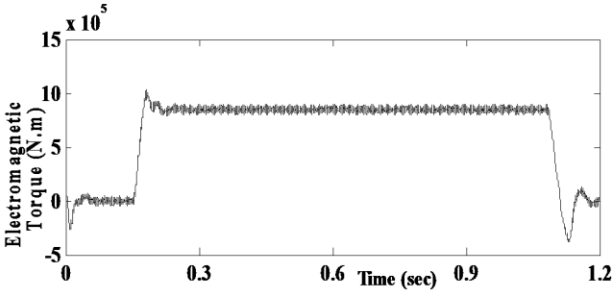


Figure 3.33 Measured Electromagnetic torque of channel #1.

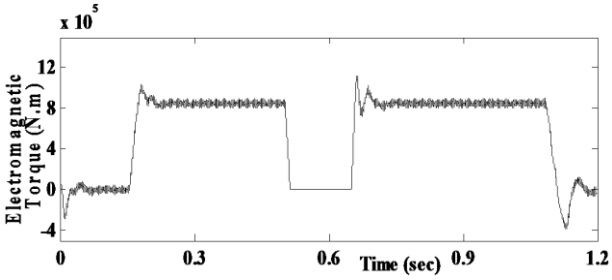


Figure 3.34 Measured Electromagnetic torque of channel #2.

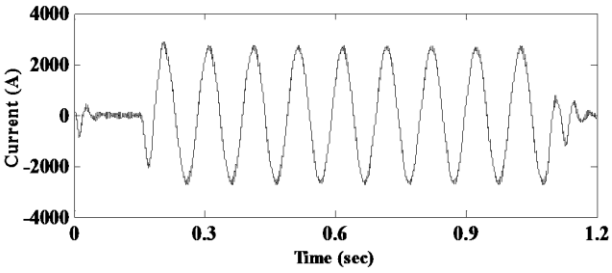


Figure 3.35 Stator phase current for channel-1.

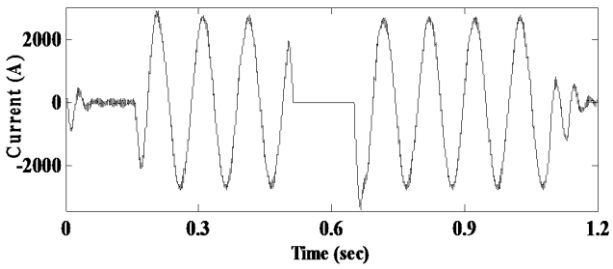


Figure 3.36 Stator phase current for channel-2.

Total grid-side phase current is shown in Fig. 3.38. Adjustment made in carrier phase for channel #2 converter during entire course of simulation, is shown in Fig. 3.37. As carrier phase for converter #1 remains 0º throughout simulation run hence it is not shown here. Looking at Fig. 3.37, it is evident that interleaving control circuitry is triggered once at start of simulation and

later on whenever a change occurred in operational status of converter module in path #2. Criterion for selection of best interleaving angle is based on energy ratio computation and for the time span when both modules are ON, interleaving angle selected by the control algorithm is pi radians for converter in channel #2.

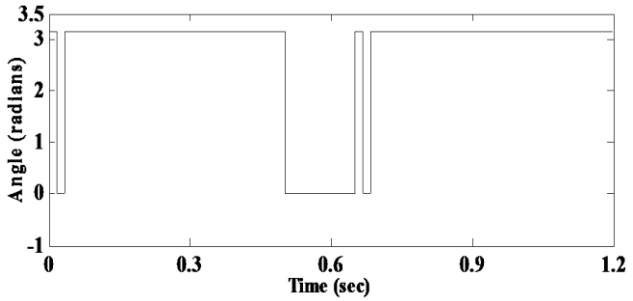


Figure 3.37 Carrier phase for converter module in channel-2.

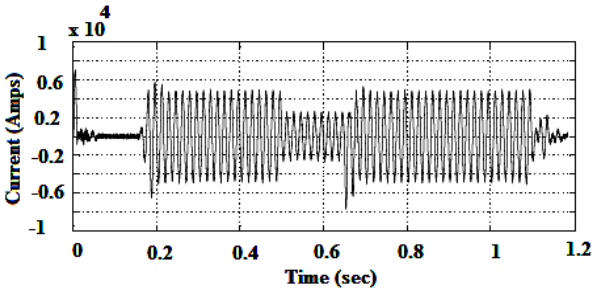


Figure 3.38 Total grid side current flowing in phase-A.

DC-link voltage measurement for the two channels is shown in Fig. 3.39 and Fig 3.40. Reference value of DC-link voltage is set at 1220 V, and as seen in Fig. 3.39, for the case of channel #1, DC-link voltage measurement is quite stable and is close to its reference value. For the case of the other channel, DC-link voltage shoots up from its reference level at time converter #2 is shut down. But as soon as module in path #2 is back in operational mode, DC-link voltage for the same is quickly restored back to its reference voltage.

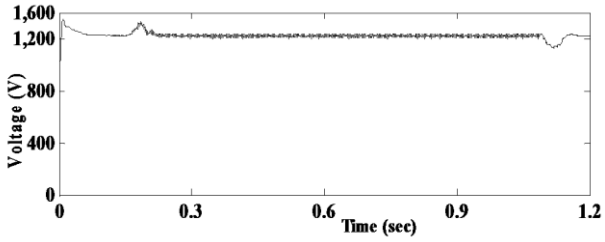


Figure 3.39 Measured DC-link voltage for channel-1.

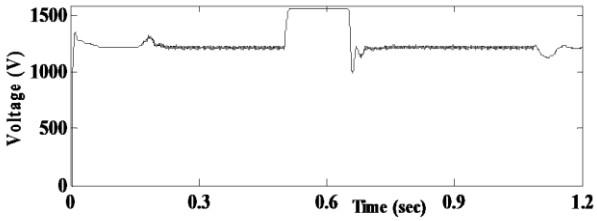


Figure 3.40 Measured DC-link voltage for channel-2.

Simulation results above showed satisfactory performance of automatic interleaving controller when incorporated with 4MW wind energy conversion system for all the different test scenarios.

Experimental verification of the developed algorithm is tested in laboratory and test results obtained are discussed in detail in the proceeding chapter of this thesis.

3.5 Summary

Development of algorithm for automatic interleaving of rectifier/inverter modules was main objective of this chapter. In development phase of the algorithm system of parallel inverters feeding a common RC load was utilized. Main challenges faced in design of a distributed controller were identified and quantity known as Energy ratio (E_H) was defined. This ratio when evaluated for total load-side phase current for various interleaving angles, revealed lowest possible value occurring when appropriate carrier phase shift was adjusted between parallel operating modules. Algorithm to determine best possible interleave angle was finalized using the E_H criterion. As the value of carrier phase of an inverter module is product of its token number and interleave angle hence algorithm with centralized control structure for token number evaluation was also developed. Simulations were carried out for system of three, five and two parallel operating inverter modules and the results showed satisfactory performance of the developed controller. Later on the controller for automatic interleaving was incorporated with a WECS developed earlier in Chapter 2 and the simulation results once again were as desired.

Chapter 4 Experimental verification

4.1 Introduction

Simulation results included in the latter half of Chapter 3 were for wind energy system comprising of a Multi-phase permanent magnet synchronous generator alongside rectifier, inverter, line side filter and a multi-winding three phase transformer facilitating flow of energy between wind turbine and the stiff grid. During developmental stage of the controller for automatic interleaving, system of parallel inverters connected to a common RC load was used. Later on when this controller was incorporated with complete WECS of Fig. 1.2, it exhibited a satisfactory overall performance. In both scenarios the feedback signal utilized by controllers of individual modules was the total grid/load side phase current. Hence experimental verification of designed controller is possible if simpler of the two systems i.e the one composed of parallel operating inverter units feeding a common resistive load is utilized. Block diagram of test system is shown in Fig. 4.1 in which current transducer is used for sensing load side phase current which is sent to analog input port of digital signal processor for further processing. FPGA board fitted with Texas Instruments (TI) eZdsp TMSF2812 which is available in laboratory is used for implementation of control algorithm.

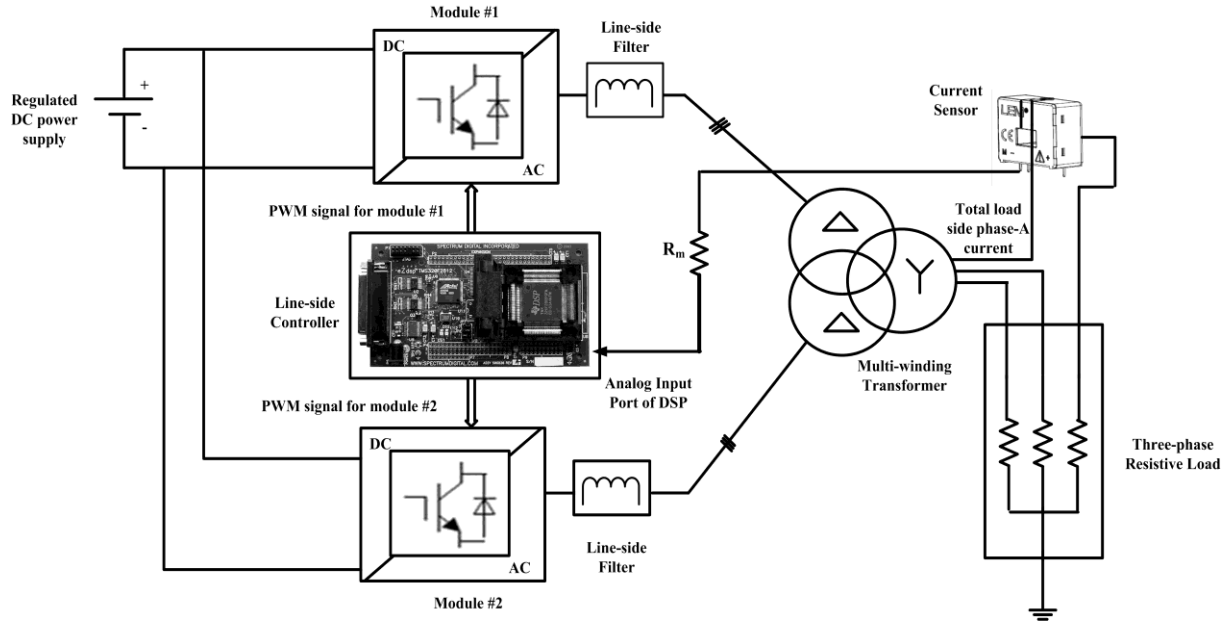


Figure 4.1 Experimental set up for testing autonomous controller.

Parameters of the system under test are listed in Table. 4.1.

Table 4.1 System parameters of Laboratory set up.

DC input voltage (V_{dc})	30 V
Line side filter inductance per phase (L_f)	10 mH
Load resistance per phase (R_{load})	24 Ω
Output frequency (F)	60 Hz
Load side Line-Line voltage ($V_{L\text{-}L\ peak}$)	22.08 V
Switching frequency (F_{sw})	660 Hz
Sampling frequency (F_{sp})	6600 Hz
Amplitude Modulation index (ma)	0.85
Frequency modulation index (mf)	11

The DSP-FPGA controller board available in laboratory is generally used in testing of systems with back-to-back converters. However it is possible to use this set up as per our requirement of Fig. 4.1 i.e as a pair of parallel operating inverters units. Transformer used in the lay-out is not a phase shifting transformer. This multi-winding transformer provides isolation and eliminates circulating current from flowing between the two parallel channels. In the laboratory set-up multi-winding transformer is used in Δ-Y configuration.

Current transducer has been applied in order to measure the feedback signal which is total load side phase current. Sensor selected for this purpose is a closed loop (compensated) hall-effect current sensor, type LA 100-P by LEM®. In compensated closed loop current sensors, Hall voltage is used for regulating secondary current ($I_{secondry}$) which in turn generates a compensated magnetic field in the toroid. The compensated version of hall current sensors are known to consume more power but are capable of delivering precise measurement throughout the entire temperature range. Use of this current sensor also enhances safety of measuring/control unit by providing galvanic isolation between power and control circuitry.

From data sheets of transducer given in appendix A-5, it is found that number of its secondary turns ($N_{secondry}$) is fixed; however by setting appropriate number of turns of primary current cable ($N_{primary}$), measuring range of the transducer can easily be adjusted. The voltage drop across measuring resistor (R_m) is the signal fed to the analog input port of the DSP board. As per [35] eZdsp TMS320F2812 supports 3.3V Input/ Output voltage levels and connecting it to a system with voltage levels above 3.3 can damage the DSP beyond repair. In view of this limitation it is important to ensure that output of transducer when fed to analog input port of the eZdsp is scaled appropriately. Scaling of the sensor output signal can be done by making use of voltage divider and current buffer.

In the present scenario DC voltage level used is 30 V, if primary side turns are chosen as 11 then with fixed secondary number of turns, the voltage drop across measuring resistor R_m is calculated as under:

$$N_{primary} = 11 \tag{4.1}$$

$$N_{secondry} = 2000 \text{ (fixed)} \tag{4.2}$$

$$I_{secondry\ (rms)} = I_{primary\ (rms)} \text{ x } 11/2000 \tag{4.3}$$

$$V_{secondry\ (rms)} = R_m \text{ x } I_{secondry\ (rms)} \tag{4.4}$$

Measuring resistor R_m is selected keeping in view the fact that its value will affect the amplitude of signal $V_{secondry}$ which should stay well within the tolerant range of DSP board.

4.2 Platform used for embedded controller

The C28x™ DSP generation provides high-performance solutions for wide range of demanding control applications. TMS320F2812 (commonly referred to as F2812) belongs to family of C28x™ processors and is Flash version of the device containing 128K x 16 of embedded flash memory [35]. TMS320F2812 digital signal processor (DSP) besides being cost effective, have proven itself as an efficient C/C++ engine allowing users to develop system control software and math algorithms in high-level language [36]. Also its 32 x 32-bit MAC capabilities allow handling of higher numerical resolution problems, which would otherwise require expensive floating-point DSP's. Standard IEEE 1149.1 JTAG interface supports real-time mode of operation which is helpful especially during debug phase of project. TMSF2812 comes with a

number of integrated peripherals that are listed below [36]:

- Three 32-bit timers (CPU-Timers 0, 1, and 2).
- Two event-manager modules (EVA and EVB)
- Digital I/O and shared pin functions
- Analog-to-digital converter (ADC) module
- Serial communications interface modules (SCIA, SCIB)
- Serial peripheral interface (SPI) module
- Enhanced controller area network (eCAN) module
- Multichannel buffered serial port (McBSP) module

One advantage of using DSP from C28x™ family of processors is availability of extensive support offered by Texas Instruments (TI) in form of software and hardware development tools. The very useful software development tool called Code Composer Studio™ Integrated Development Environment (IDE) is combination of C/C++ Compiler, Assembler/Linker and Cycle Accurate Simulator. On hardware end, tools such as multi-layered printed circuit board eZdsp F2812, JTAG-based emulators and universal power supplies [36] make design process a lot easier. Detailed view of un-socketed version of this board is shown in Fig. 4.2 (a).

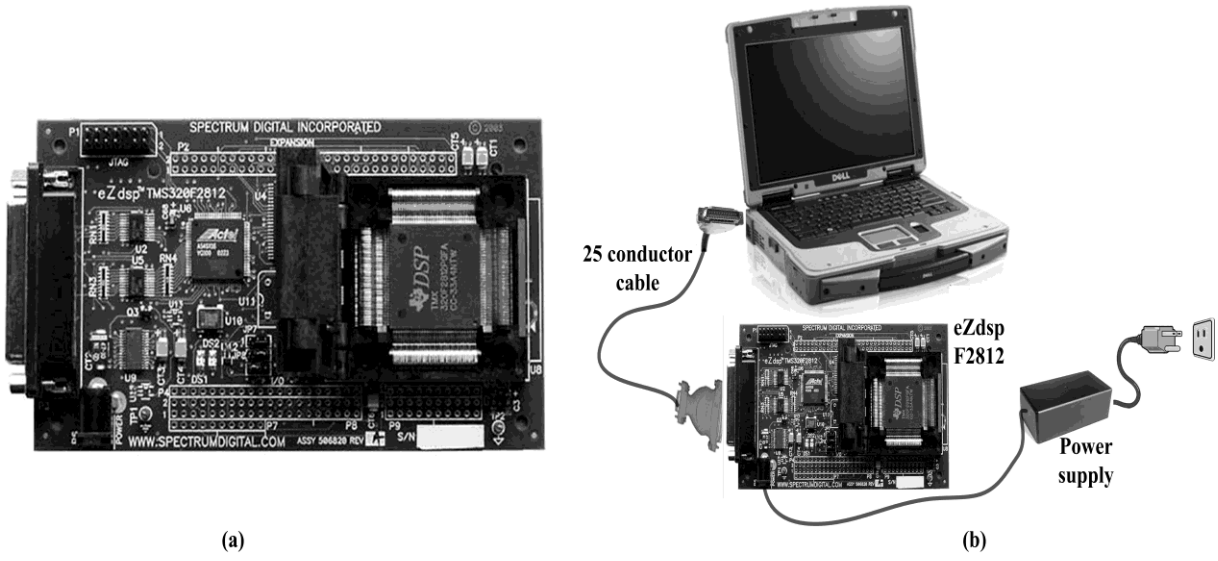


Figure 4.2 (a) eZdsp F2812 board (b) Connecting eZdsp F2812 to personal computer.

Key features of eZdsp include DSP TMS320F2812, 150 MIPS operating speed, 30 MHz clock, 18K words of on-chip RAM, 128K words of on-chip Flash, Expansion Connectors, on-board

IEEE 1149.1 JTAG Controller/emulation connector and Code Composer Studio driver for F28xx processor. The eZdsp board acts as excellent platform to develop and run software for TMS320F2812 processor, and is used here for implementation of interleaving control algorithm.

4.3 Code generation for TI microcontroller

4.3.1 Introduction to VisSim

For experimental verification of interleaving control algorithm, conventional approach would require an in depth knowledge of DSP architecture followed by the tedious process of code writing and debugging. It is important to note that this control algorithm relies heavily on FFT analysis of feedback signal and implementation of the same using fixed-point DSP demands a highly efficient source code. Keeping time limitation and efficient code generation in mind, alternative approach is explored which involves commercial software tools for design and analysis of control systems such as VisSim (by Visual Solutions) or Real Time Workshop-RTW (by MathWorks).

VisSim being an integrated development platform allows successful transition between different stages of design, letting user to create virtual prototypes on a PC and commit to the design only after verification. Due to its capability of generating a very efficient, readable and scaled-fixed point code at the register level, preference was given to VisSim. It also has capability of integrating Mathcad, Maple and MATLAB files/variables/functions within its simulation environment.

VisSim has great support features such as vast collection of sample models, detailed user guides, and online help available to the users. Though VisSim comes a comprehensive set of add-on products (overview provided in appendix A-2), but most important of these is Embedded Controls Developer (ECD). ECD is combination of C-Code generator, Fixed-Point tool-set and Target Support package and serves as an excellent platform for development of embedded control algorithm [37].

4.3.2 Stages of embedded control design

Successful implementation of DSP-based control algorithms in VisSim, was made possible when design process was carried out in three major steps [38]:-

- The very first stage is development of block diagram. It is possible to import model developed in Simulink to VisSim environment using VisSim-MATLAB interface. But as

some of the advanced Simulink functional blocks do not have their exact counterparts available in VisSim hence re-implementation of the same using VisSim block-sets is required. Use of integer format is recommended at this stage as this will make transition from computer based block design to fixed-point DSP executable version, much easier [38].

- The next step involves breaking down the developed block diagram into selected sections and running them on the DSP of choice. For instance, section of control algorithm which generates duty cycle for PWM signals is tested by replacing the non-embedded version of the diagram with embedded PWM block of VisSim. This will allow PWM block to run on eZdspF2812 while rest of the algorithm will run on the personal computer.
- The final stage of design process requires conversion of complete controller design into a format that can run solely on the DSP. This requires conversion of all floating point values into fixed-point format and replacement of all non-embedded blocks with DSP-compatible blocks [38]. Blocks formulating the embedded controller are then encapsulated as a single compound block.

Before start of code compilation, user needs to configure certain DSP related options available in the menu such as simulation step size, auto-restart, VisSim communication interface etc. During compilation stage VisSim works in conjunction with Code Composer Studio so as to compile and build a DSP executable program. VisSim first converts the functional blocks into a C-language based source code which is later converted to native C2000 assembly instruction by Code Composer Studio. A **.out* file is generated at the end of the linking process which can run entirely on the DSP [38]. Successful completion of above three steps ensures conversion of control algorithm to DSP executable version.

It is important to mention here that the controller board used in laboratory is composed of eZdsp F2812 mounted on an FPGA board and proper configuration of FPGA is necessary for the system to work accurately. Correct configuration of FPGA requires that DSP output named XCLOCKOUT should be enabled to work at frequency of 75MHz, with SYSCLOCK and XTIMCLK configured at 150MHz. At the register level 0x000A is written to PLL register (address: 0x7021), 0x7 is written onto XINTCNF2 (address: 0xB34) and 0x358AC is written in XTIMING0 (address: 0xB20). Completion of these steps is vital for bringing controller board in working condition.

Shown in Fig.4.3 is the VisSim window with inner view of embedded-version of control

algorithm designed for automatic interleaving of parallel inverters. Detailed description of different section of the model is presented in appendix A-3 for reference.

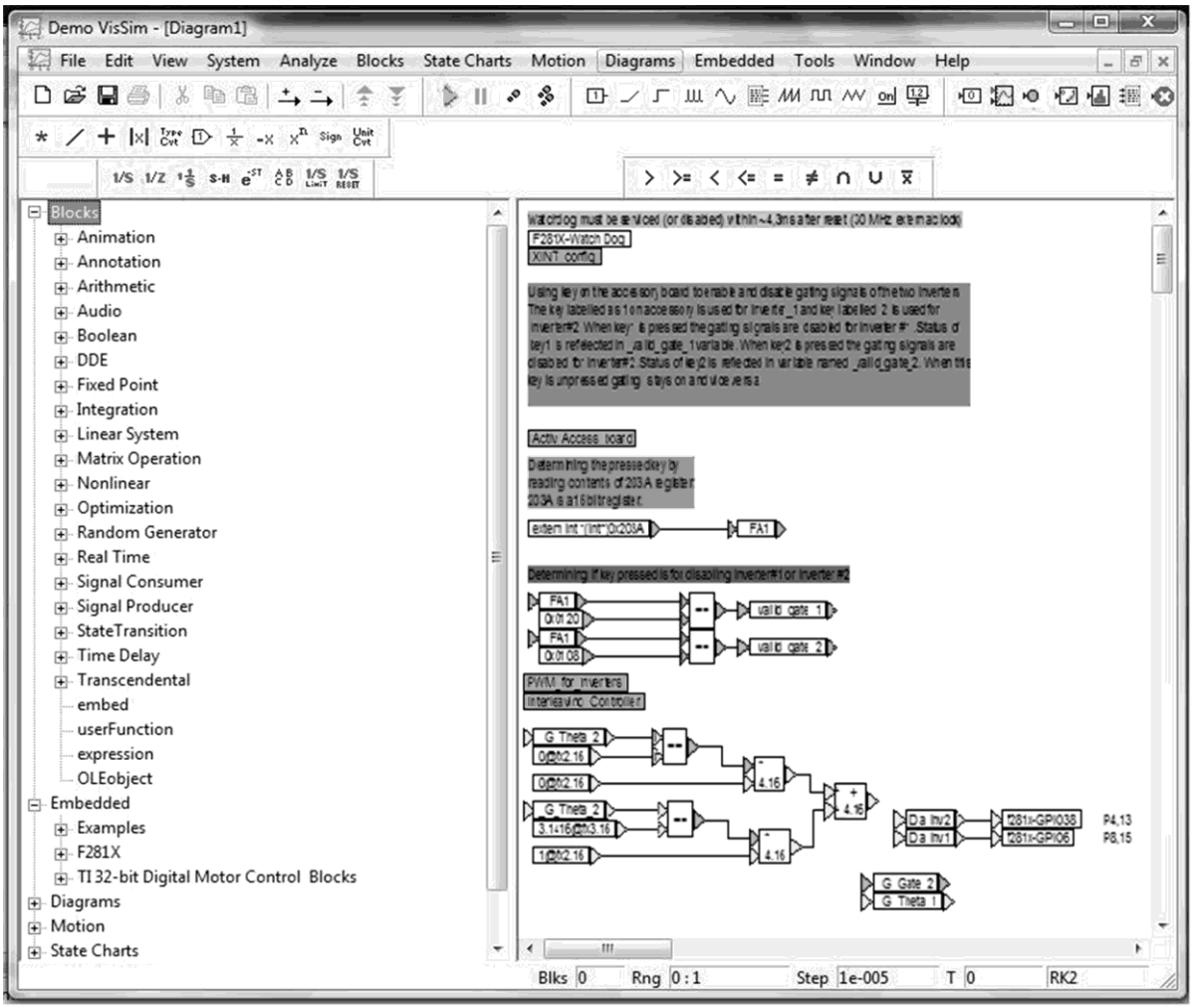


Figure 4.3 VisSim window with complete model of embedded controller for automatic interleaving of parallel inverters.

4.4 Experimental results

Embedded controller designed using VisSim/ECD platform was tested in the laboratory. Following the layout shown earlier in Fig. 4.1, test bench was established and different views of the same are shown in Fig.4.4. Important components of the setup as seen in the figure, includes multi-winding transformer, three phase resistive load, DSP-FPGA controller board, DC power supply, accessory board, filter, current sensor and the PC station where the source code is compiled, and downloaded onto the target board.

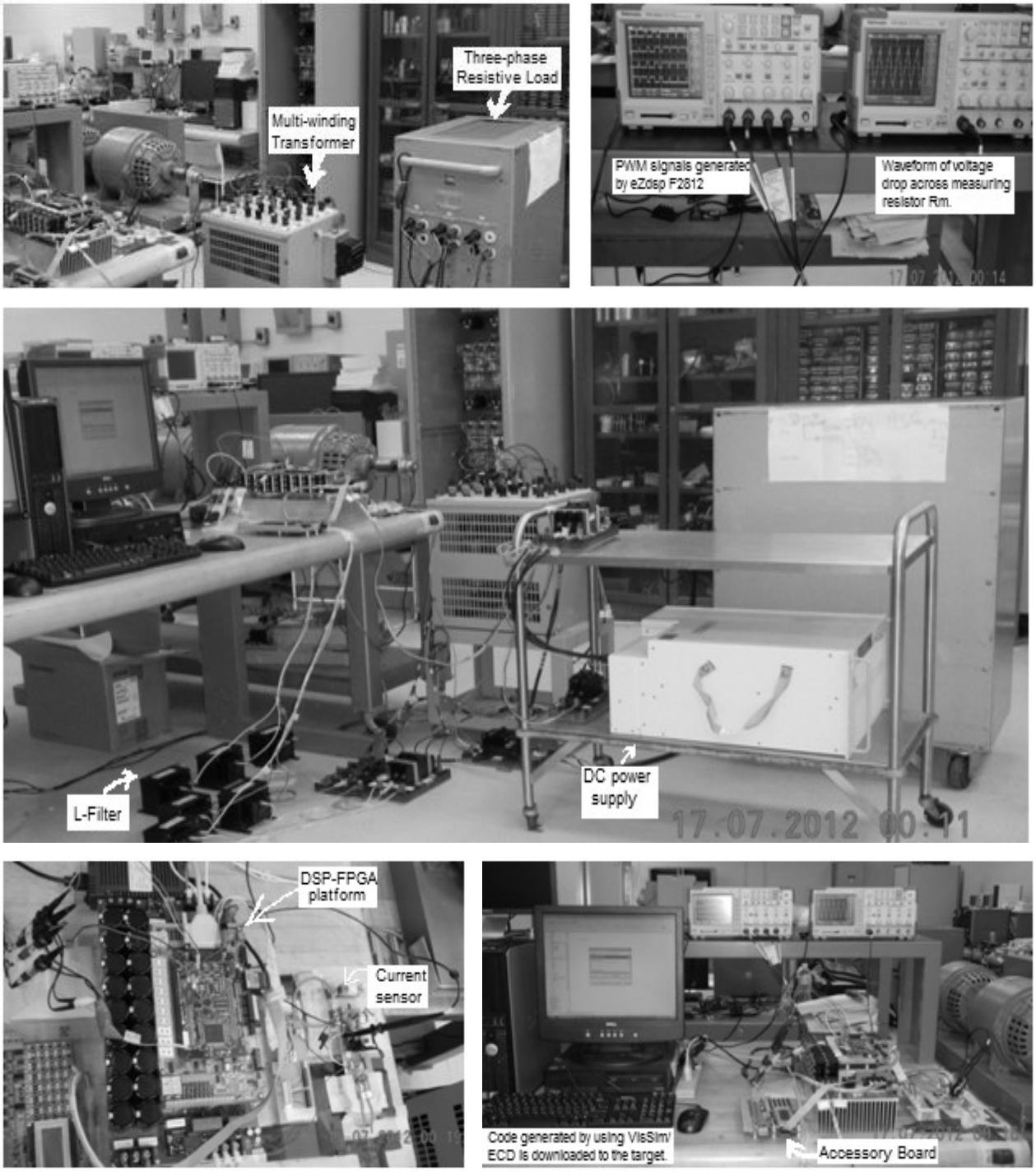


Figure 4.4 Experimental set-up used in testing of interleaving algorithm.

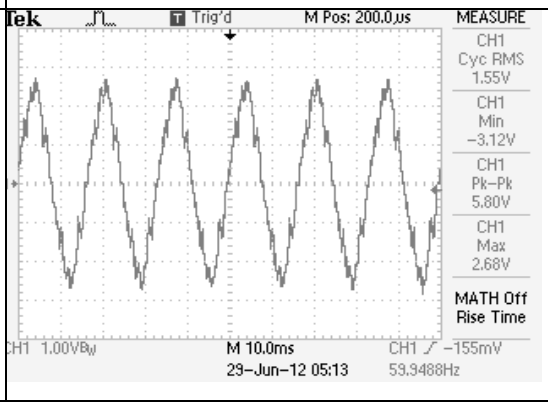
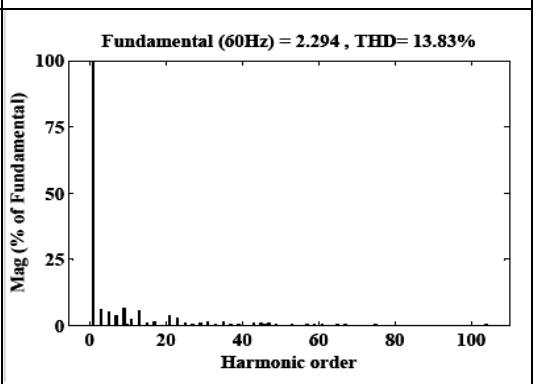
Based on schematics for back-to-back converter modules available in lab there are only two free analog input ports available on DSP-FPGA controller board, namely ADCINA0 and ADCINB0. Hence analog feedback signal i.e total load side phase current will be supplied through

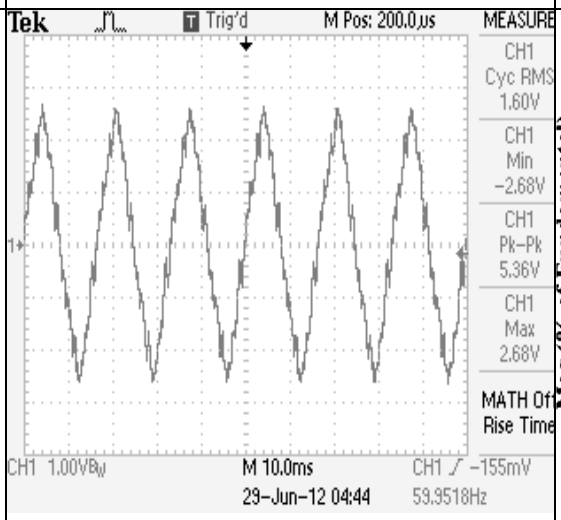
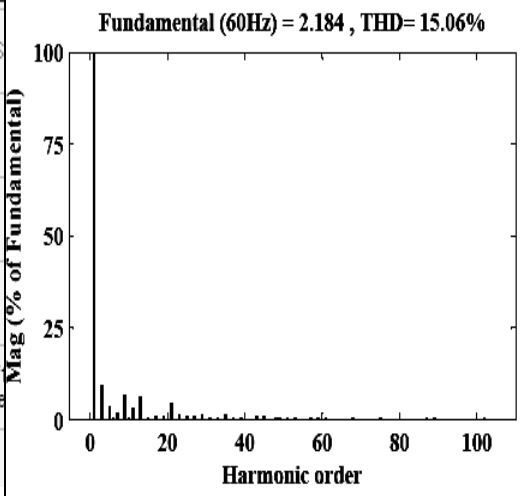
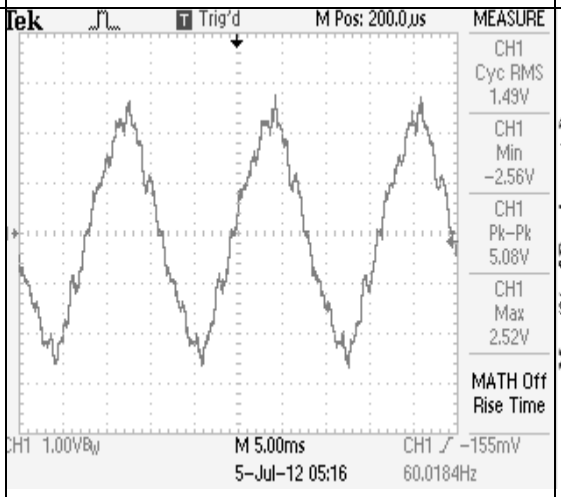
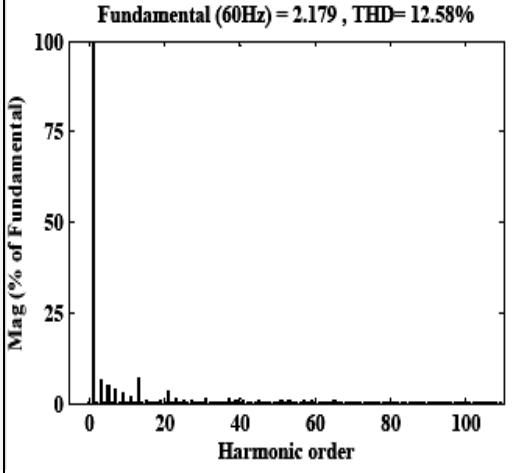
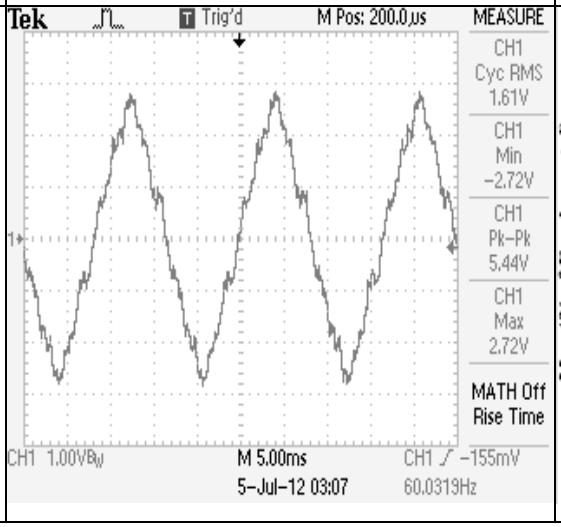
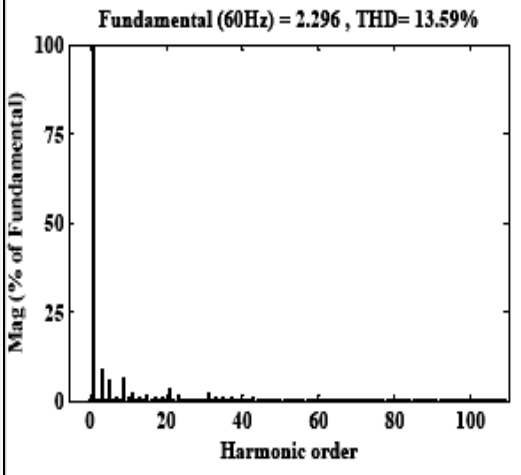
one of the available free ports i.e ADCINA0. In one of the views of Fig. 4.4 are seen two scopes that are used for viewing/recording of waveforms. The sinusoidal signal appearing on screen of one of the scope is the voltage drop ($V_{secondry}$) across the measuring resistor $R_{m.}$ Being proportional to total load side phase-A current, $V_{secondry}$ is the signal that is sent to the DSP board via analog input port ADCIN0 for determination of correct interleaving angle.

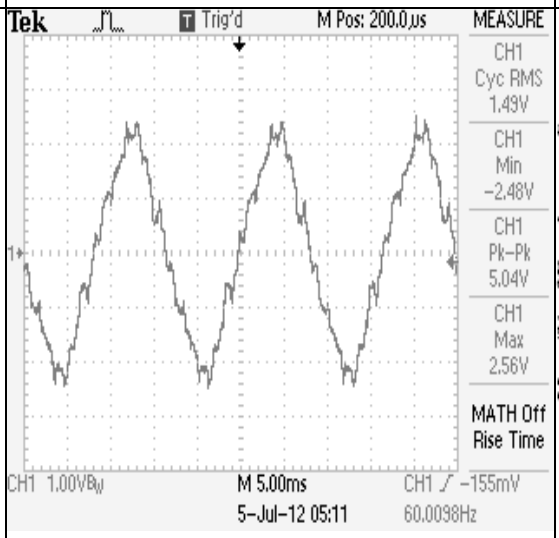
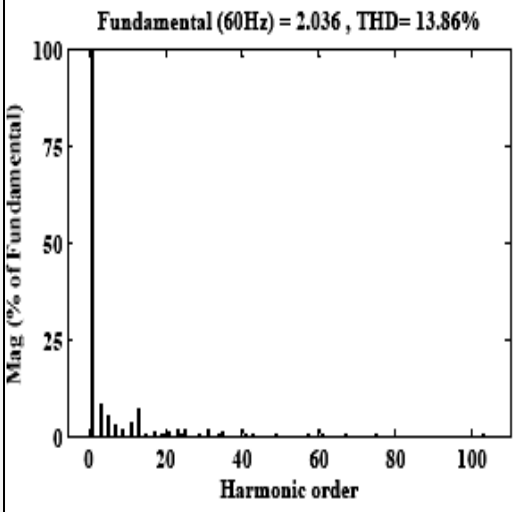
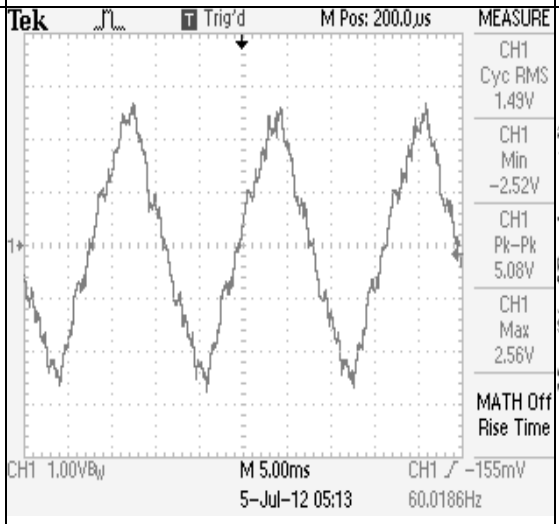
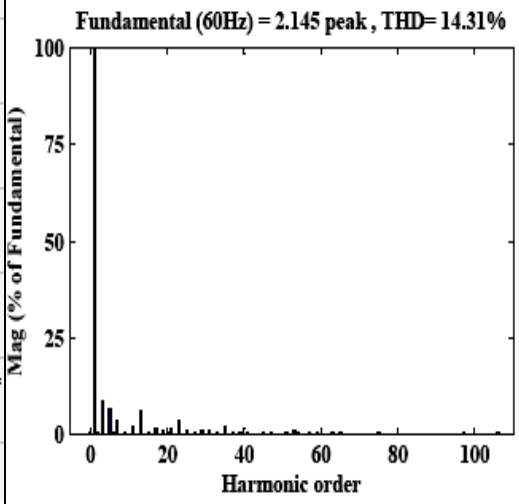
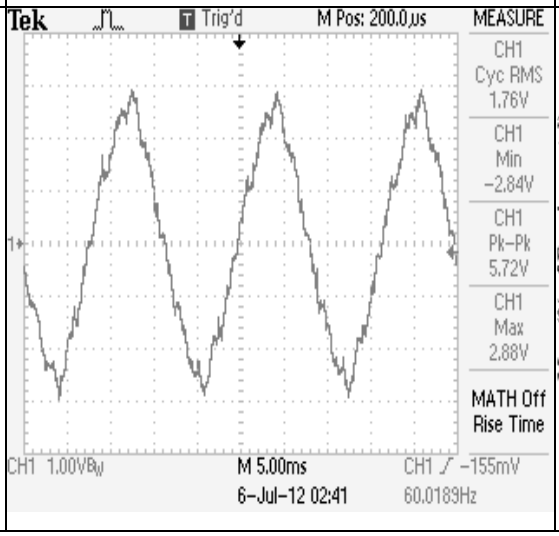
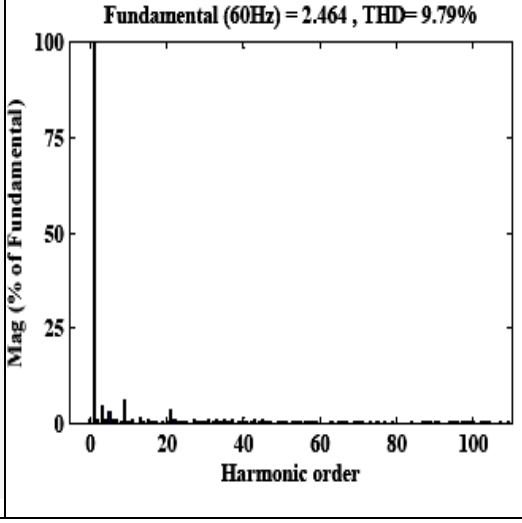
Best way of demonstrating the importance of interleaving angle will be to test the system of parallel inverters for different interleaving angles including the case of best interleaving angle determined via developed control algorithm. Evaluation of system's performance for all these cases is made using criterion of percentage Total Harmonic Distortion (%THD). Testing system for different carrier phases is very easy when using software tool like VisSim as by making a minor adjustment in the model, the system is ready for the new trial. In Table 4.2 under column 2 the recorded waveform $V_{secondry}$ is shown for various interleaving angles. Data for each of these waveforms is analyzed using MATLAB.

Results of FFT analysis for each of the carrier phase shift is in form of bar graph and is pasted in column 3 of Table 4.2. Various frequency components have their magnitude expressed as percentage of fundamental harmonic component. Peak value of the fundamental harmonic component and the recorded % THD value are expressed on top of each of the bar graph. For the sake of uniformity, single cycle starting at 0.0168 sec is selected for recording THD value for different cases.

Table 4.2 FFT analysis of voltage drop across resistor (R_m) for different interleave angles.

Interleaving Angle	Voltage signal ($V_{secondry}$) fed to analog input port ADCIN0	FFT analysis of voltage waveform
0º		

Interleaving Angle	Voltage signal ($V_{secondry}$) fed to analog input port ADCIN0	FFT analysis of voltage waveform
36º		
72º		
90º		

Interleaving Angle	Voltage signal ($V_{secondry}$) fed to analog input port ADCIN0	FFT analysis of voltage waveform
108º		
144º		
180º *(selected using control Algo.)*		

4.5 Analysis of results

Comparing bar graphs shown in Table 4.2 for different interleaving angles it is observed that value of % THD is minimum for the case when carrier phase shift between the two inverters is kept 180 º (selected using interleaving control algorithm) and is in accordance with the theoretical results. Another comparison is made using %THD for the different cases, for multiple cycles of recorded voltage waveform $V_{secondry}$. This is done by making use of MATLAB's block named *THD (Discrete)*. It is important to mention that *THD (Discrete)* block starts giving non-zero output only after completion of one cycle of the input signal which translates to 1/60 sec. It is for this reason that in Fig. 4.5 the horizontal scales starts at 0.01666 sec.

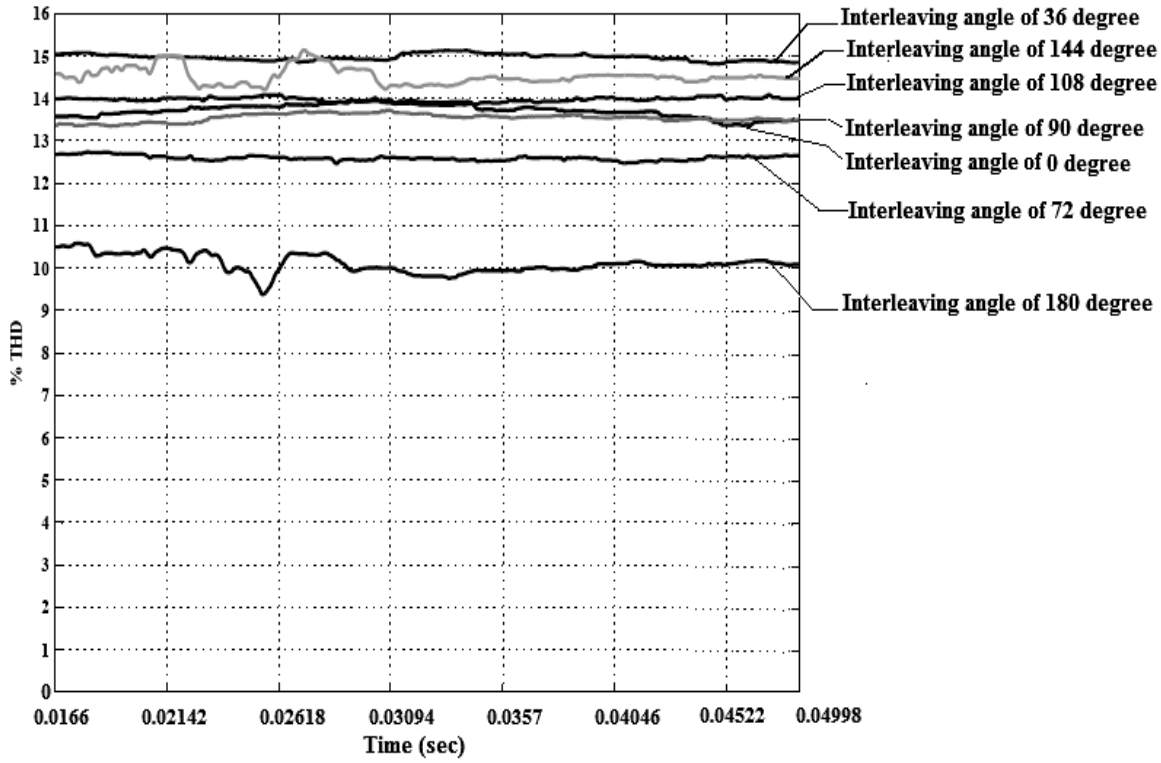


Figure 4.5 Comparison of %THD values obtained experimentally by testing the system for different interleaving angles.

Looking at Fig. 4.5, the idea of 180 º being the best value of carrier phase shift for system of two inverters is once again verified. From Table 4.2 it is found that if efforts are not made to interleave the modules in operation and the two inverters are allowed to operate with zero displacement between the carriers, then %THD of recorded waveform would be approximately

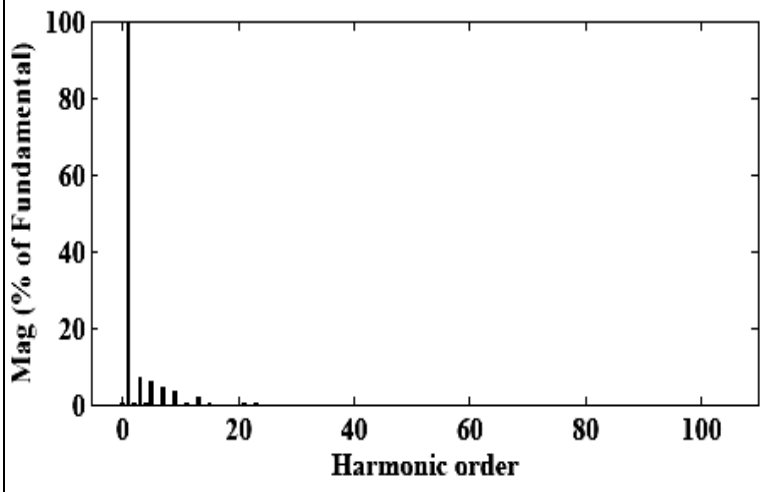
1.41 times more than the %THD value, if inverters were made to operate with carriers displaced at an angle of 180 º relative to each other.

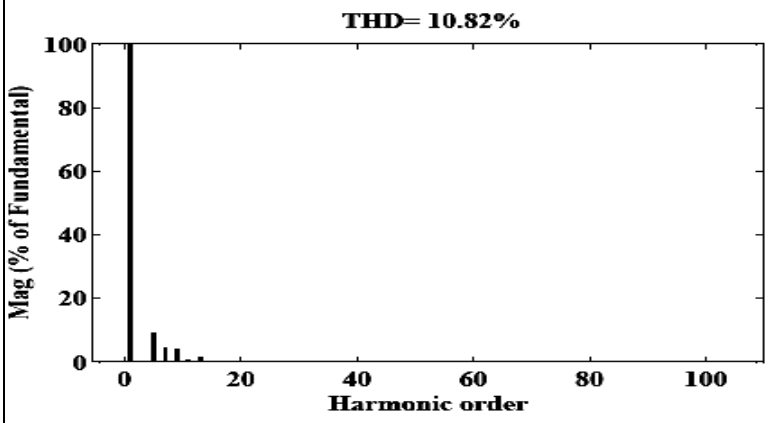
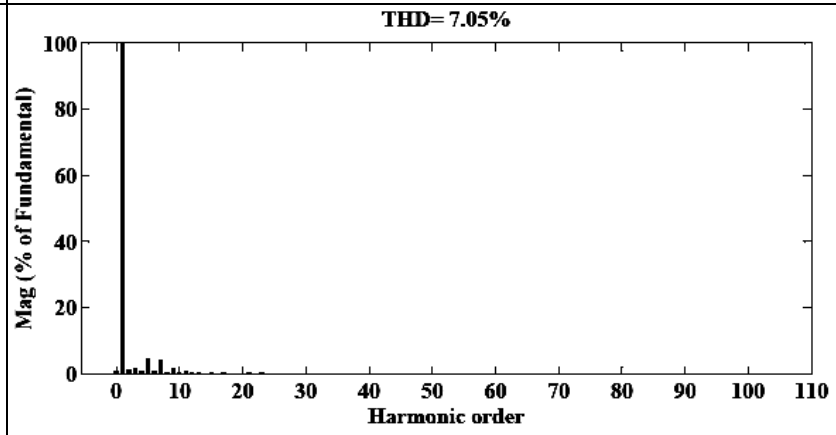
In Table 4.3 system with parameters as per Table 4.1 is simulated using MATLAB/Simulink. This table is generated by setting three different values of carrier phase shift in order to compare behaviour of ideal system with the real one. Simulations are carried out for three different interleaving angles 0º, 72º and 180º and FFT analysis of the simulated waveform for the three cases are shown under column 2 of this table. Once again for the sake of uniformity, single cycle that has been selected for recording %THD is the one starting at 0.0168 sec.

By comparing the three results we find that even in this case, value of %THD computed for load side phase current is lowest, when the carriers of the two inverter modules are displaced by an angle of 180 º. If the two carriers are synchronized, then %THD is approximately 1.6 times higher than the case when inverters were simulated with appropriate phase shift between them.

Percentage THD recorded for multiple cycles of the phase current are shown in Fig. 4.6 and it also confirms the best interleaving angle as 180º. Hence both simulation and the experimental results are in agreement over the choice of best interleaving angle for a two inverter system.

Table 4.3 Simulation results showing %THD of total load-side phase current for different phase shifts between the two carrier signals.

Interleaving angle	Percentage THD of total load-side phase current
0º	

Interleaving angle	Percentage THD of total load-side phase current
72º	
180º	

By viewing values in column 2 and 3 of Table 4.4, general trend of experimental results being higher than their simulation counterpart is observed. Possible reasons for this trend are listed as under:-

- In real systems, unlike the case of simulation, are present many non-idealistic factors which cause the experimental results to differ from the readings acquired by running model in Simulink. For instance, in simulation L- filter used has inductance equal to 10mH. In real systems it is impossible to have a 100% pure inductance. Hence it will not be wrong to assume that the L-filter used in the practical will have some resistance associated with it. The results of the real systems therefore tend to be less efficient and more prone to losses in comparison to simulation results. Another undesirable effect of having non-ideal inductance present in the system is increase in level of harmonics injected in the measured output signal.

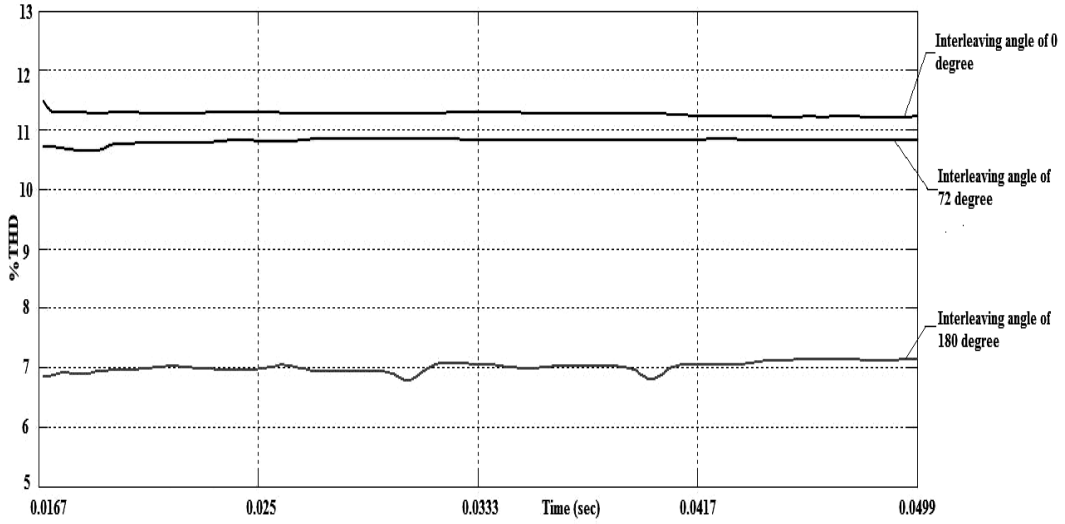


Figure 4.6 Comparison of %THD values obtained by carrying out simulations for three different values of interleaving angles.

- Through programmable deadband-generator circuit it is possible to produces two outputs of each compare units with or without inclusion of a deadband zone [41]. This feature of TMSF2812 was utilized during implementation stage and a deadband of 3.2 μ sec was introduced in outputs of compare units. This gap is essential for IGBT based VSI in order to avoid risk of conduction overlap of same leg switches [39]. Although the insertion of dead-time guarantees safe operation and has duration which is relatively short as compared to PWM period but it is cause of serious waveform distortion in inverter's output [40]. Another effect of dead time inclusion is reduction in fundamental component of VSI's output especially if inverter is operating at low voltage levels [39].

Table 4.4 Comparison of %THD values obtained through experiment and by simulation.

Interleaving angle	**%THD (Experimental result)**	**%THD (Simulation result)**	**Percentage by which experimental value is higher than the simulation result**
0º	**13.83**	**11.28**	**18.43%**
72º	**12.58**	**10.82**	**13.99%**
180º	**9.79**	**7.05**	**27.98%**

Three phase voltage source inverter with load connected at the output terminal is shown in Fig. 4.7. Detailed analysis carried out in [39] revealed that main reason for dead time related voltage distortion in VSI is freewheeling current flow during the dead-time period. To illustrate this point, gating signal for switches S_1 and S_4 for VSI of Fig. 4.7 are shown both with dead time (S_{w1}^* and S_{w4}^*) and without dead time (S_{w1} and S_{w4}) in Fig. 4.8. Considering one complete cycle of phase current at the inverter output, it is observed that during the positive half cycle of current there is a decrease equal to T_{delay} in positive width of voltage waveform. Contrary to this in the negative half cycle of output phase current, an increase by T_{delay} sec is observed in positive width of voltage waveform. The inclusion of dead-time has led to an asymmetrical change in waveform of output voltage signal [39]. Consequently, undesirable harmonic components especially low order harmonics appear in output causing an overall distortion of the VSI's voltage waveform [39].

4.6 Summary

Experimental verification of designed controller is done using a system composed of two parallel operating inverter units feeding a common resistive load. Phase current at the load end is used as feedback signal which the controllers utilize for determination of best possible interleaving angle.

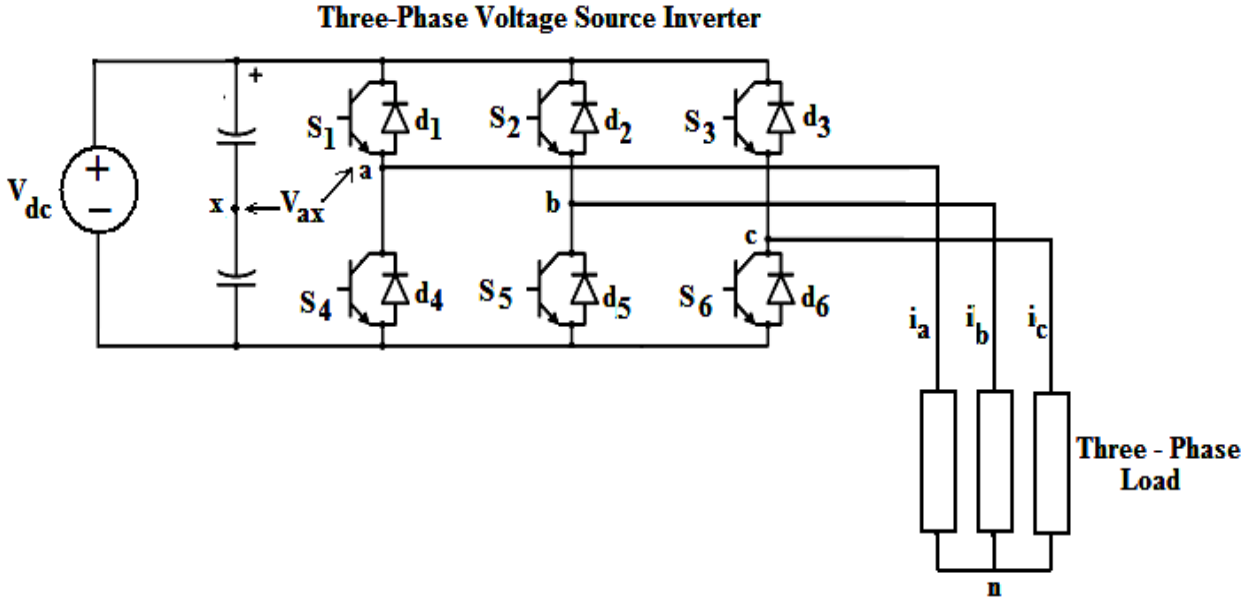


Figure 4.7 A three-phase voltage source inverter [39].

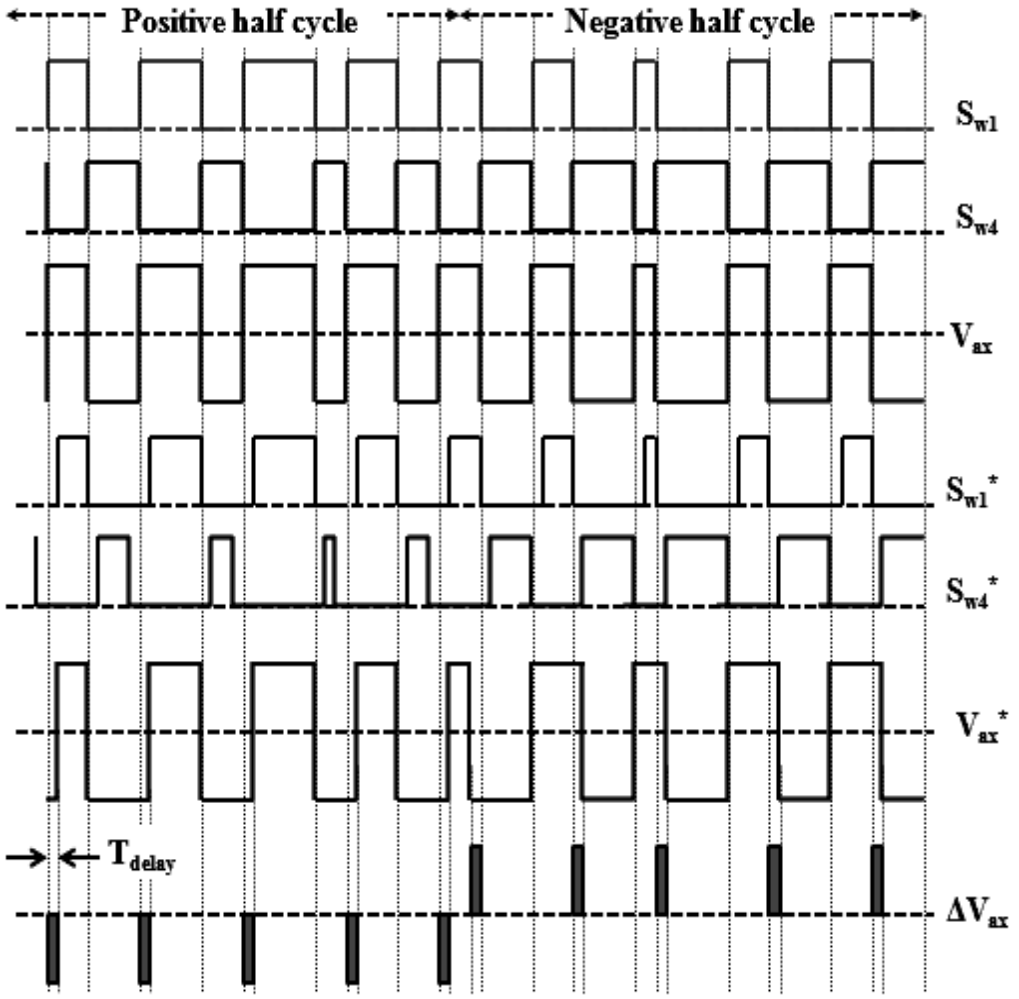


Figure 4.8 Effects of deadband on output voltage of three-phase voltage source inverter [39].

For implementation of control algorithm platform used is eZdsp TMF2812 which is a stand-alone card that comes with DSP from C28x™ family of TI processors. Main reason for selecting TMSF2812 for controller implementation is its ability for being an efficient C/C++ engine, which would allow the users to develop both system control software and math algorithms in high-level language.

Keeping in view time limitation and need of an efficient code, alternative approach was used for code development. VisSim with its comprehensive set of add-on products and a proficient C-code generator acts as an ideal platform for model-based embedded system development.

In the chapter after discussion about general design procedure in VisSim, results obtained by testing developed embedded controller for system of two parallel inverters were shown.

Comparisons were made between simulation and laboratory results. Like the case of simulation, experimental results also verified idea of interleaving, as lowest %THD in output current was obtained when interleaving angle of 180 º was used for system of two parallel inverters. Overall, percentage THD obtained experimentally was higher than the simulation results. Main reasons for this deviation could be non-ideal behaviour of system components and inclusion of dead time in PWM switching of voltage source inverters.

Chapter 5 Conclusions

5.1 Conclusions

Main attraction associated with use of modular converters is redundancy and reliability of design. Use of modular converters also provides opportunity to significantly reduce harmonics in VSC's output through interleaving technique where switch turn-on times of operating modules are displaced evenly across the switching period. Focus of this thesis was on development of a control algorithm that can automatically interleave, modules operating in parallel in a wind energy system which is directly driven by a multi-phase PMSG.

5.1.1 Major contributions

Following are main contributions of this research:

- Detailed harmonic analysis was carried out for system of parallel inverters and impact of carrier phase displacement on energy of harmonic components of output phase current was studied. Term Energy ratio was defined which proved to be an important parameter in determination of best interleave angle.
- Control algorithm was developed for automatic interleaving of three-phase voltage source converters. Algorithm used load/grid side phase current as feedback signal for estimation of Energy ratio. With the intention of maintaining redundancy that comes with modularity of design, algorithm was developed with maximum computations carried out by the local controller. Exchange of information between the neighboring modules is not promoted and synchronization between parallel modules was achieved with minimum possible communication overhead. Simulation results verified that for any number of parallel operating inverter units the developed control algorithm was capable of tracking the best interleave angle and the modules appropriately adjusted their carrier phases using this information. Interleaving controller when used in wind energy system comprising of six-phase PMSG and two parallel operating channels, once again delivered results as per requirement.
- Experimental verification of the developed control algorithm was carried out using system of two parallel inverters feeding resistive load. Lowest % THD was recorded in the total load side phase current, when carriers of the two modules were displaced using embedded

interleaving controller, following criterion of best interleave angle. Experimental results were in agreement with simulation results and proved effectiveness of developed control technique.

5.1.2 Future work

- Simulating system of modular converters using PMSG without multiple three-phase winding sets is recommended.
- Experimental verification of automatic interleaving algorithm using the wind energy system connected to grid is also suggested.
- Idea of achieving synchronization in operation of parallel modules without employing any means of communication can also be investigated.

Appendix A-1

Table A-1 Parameters of multi-phase, salient-pole PMSG based WECS.

Rated Shaft power	4 MW
Rated phase voltage	398.37 V (rms)
Rated Stator current	3346.9 A
Rated Torque (T_e)	1.69 M N.m
Rated stator frequency	11.29 Hz
Rated rotor flux linkage (λ_{rf})	6.76 Wb (peak)
Stator Resistance (R_s)	7.3mΩ
d-axis Syn. Inductance (L_{sd})	0.3 mH
q-axis Syn. Inductance (L_{sq})	0.5 mH
DC-link voltage	1220 V
Number of pole pairs (N_p)	30
Line side Filter inductance	0.126 mH

Appendix A-2

Important features of VisSim

A high performance mathematical engine working in conjunction with user friendly block diagram interface, enables VisSim to provide prompt/precise solutions for variety of systems and makes it a perfect choice for not only hardware-in-loop testing but also for off-line controller tuning. It has over 120 built-in linear and nonlinear blocks with several libraries of pre-constructed components and dedicated toolbox functions designed for control, electromechanical design, signal processing, and digital power systems etc [41].

VisSim contains a number of functional blocks that are placed under different block-sets such as Matrix Operations, Nonlinear, Fixed-point, Arithmetic, Boolean, Signal producer etc depending on their functionality [41]. Familiarity and proficiency of using these functional units is very important as they form basic building block for creating model for embedded controller.

VisSim offers a comprehensive set of add-on products which are shown in Fig. A.2.1, these products help in extending VisSim's functionality to applications involving frequency domain analysis and real-time hardware-in-the-loop prototyping.

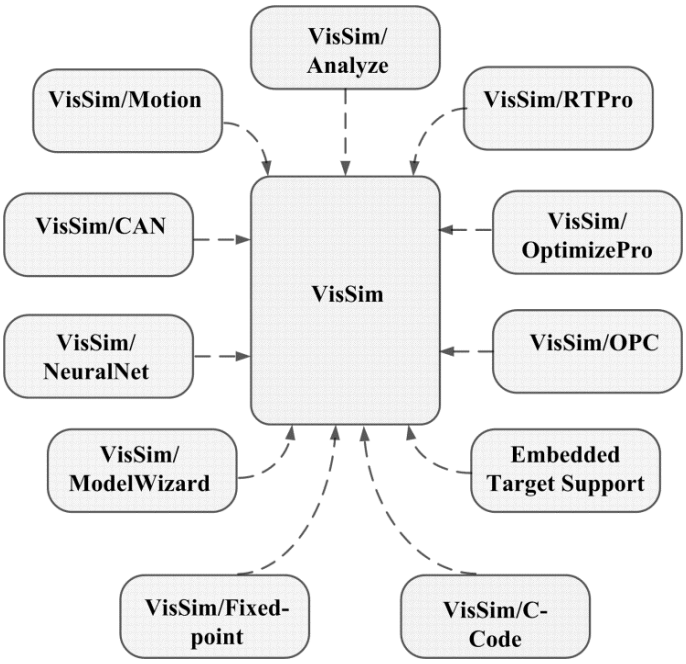


Figure A.2.1 Add-ons available in VisSim.

Most important add-on from our perspective is Embedded Controls Developer (ECD), which is combination of VisSim/C-Code, Fixed-Point and target Support package. ECD acts as a comprehensive platform where user can model, simulate, and develop controller for embedded systems [37]. ECD has many general purpose functional blocks that are written specifically for popular digital signal processor used in industry including TMSF2812.

DSP blocks supporting on-chip peripherals like PWM, encoders, capture, ADC and SPI are available. These blocks are highly optimized as they contain hand-written assembly routines which are specifically developed for Texas Instruments DSP. Due to this reason execution speed of these blocks when running on F2812 is a lot faster than an equivalent user created compound block [37]. The controller block diagram is converted automatically by ECD to ANSI C code. After successful completion of compilation and linking stages, code is made ready for execution on embedded target.

Appendix A-3

Embedded controller for interleaving modular converters

Complete VisSim model for automatic interleaving is shown in Fig. A.3.1 and many of the constituent blocks are compound in nature which will be discussed individually in the remaining part of this appendix.

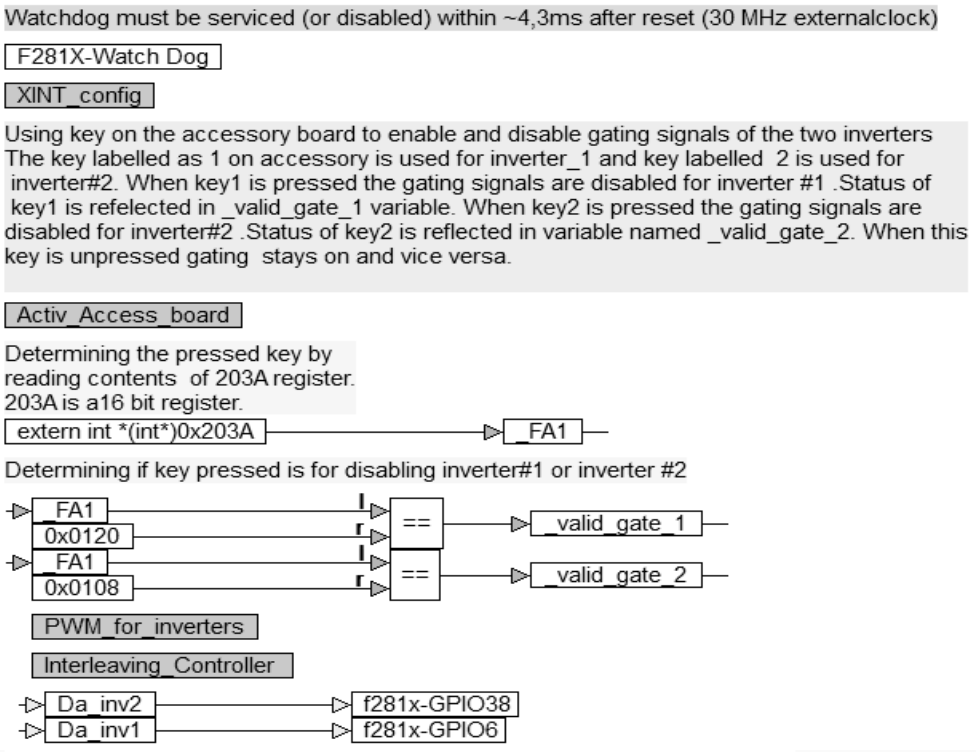


Figure A.3.1 Complete VisSim model of embedded interleaving controller.

- **F281X-Watch Dog**: The block enables a hardware watchdog and expanded view of it is shown in Fig. A.3.2. Watch dog can force an automatic restart of the system in case it acts mischievously [37]. One of the better options for avoiding system restart without disabling watchdog is through software resetting of watchdog timer module at regular intervals. In VisSim watchdog block, user can define this interval against the drop down menu titled *Time Until Reset*. The maximum time for resetting watchdog in TMSF2812 processor is 4.3 msec. The minimum time limit for reset is dependent on sampling time selected for the design, with reset not being smaller than the sampling time.

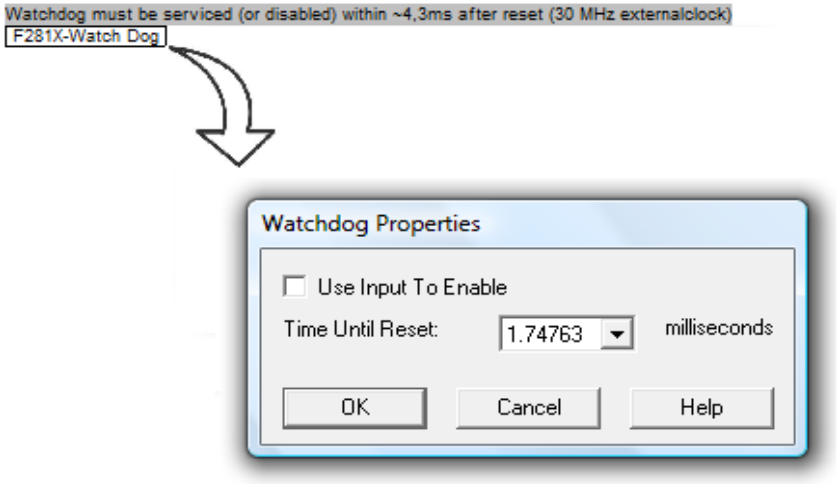


Figure A.3.2 VisSim block for resetting watchdog timer module.

- **XINT_config**: Expanded view of this compound block is shown in Fig. A.3.3 and is mainly composed of two VisSim blocks namely externRead and externWrite block [37]. Both these blocks are used for reading or writing directly to hardware registers. Placement of these blocks along the vertical defines their order of execution in the algorithm. Reasons for creating this compound block lies in the fact that controller board used in lab is composed of eZdspF2812 mounted on an FPGA board. For controller board to work it is important to properly configure FPGA and this means enabling DSP output named XCLOCKOUT at frequency of 75MHz, both SYSCLOCK and XTIMCLK should be configured at 150MHz. At register level 0x000A is written to PLL register (address: 0x7021), 0x7 is written onto XINTCNF2 (address: 0xB34) and 0x358AC is written in XTIMING0 (address: 0xB20).

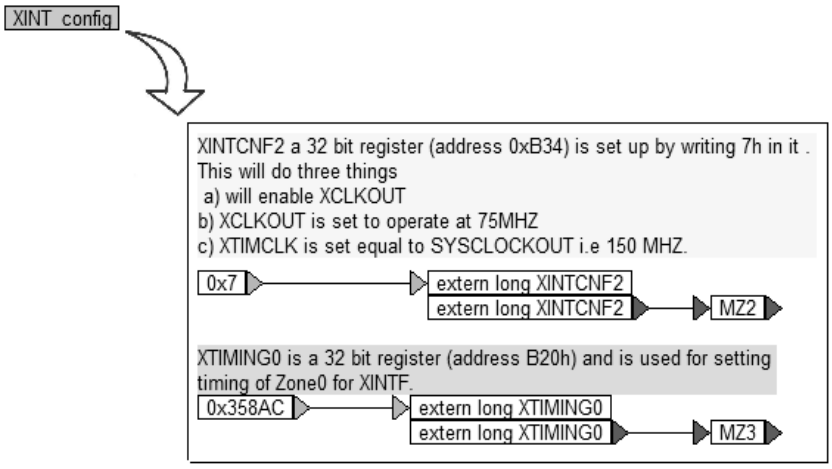


Figure A.3.3. Compound block created in VisSim for proper configuration of FPGA.

- **Activ_Access_Board**: During testing of the developed control algorithm it is required to turn ON or OFF the parallel operating inverter units. VisSim PWM blocks have an input called *enable* which allows software control over enabling/disabling of PWM unit. By using DSP's general purpose input/output ports and accessory board available in laboratory it is possible to generate physical signals that can control operational state of PWM blocks for respective inverter modules. Accessory board is connected to the controller board at JP27 via a 24 pin connector. In order to make controller board receive data from Accessory Board user needs to write code 6 Hex in a 16 bit register, RX_CODE (address: 203B) . Once again for writing on to the register VisSim's externWrite block is utilized. Section of model in which Accessory board is configured is shown in Fig.A.3.4.

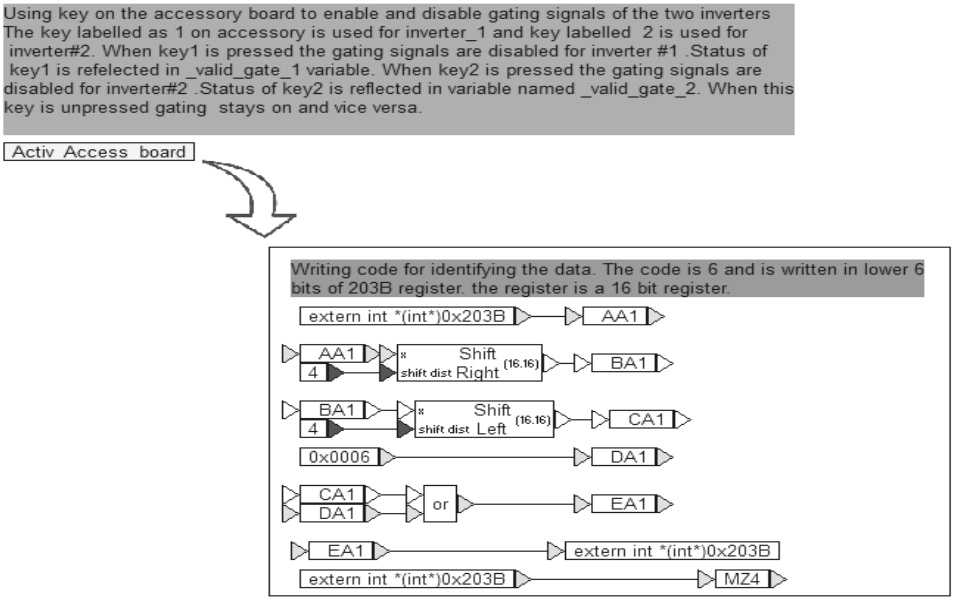


Figure A.3.4 Section of VisSim model responsible for configuration of Accessory board.

Accessory board has thirty five pushbutton installed in a 5 x 7 array formation. There is a row and column number associated with each of the push button and as soon as its pressed, information of its respective location is stored in a 16 bit register named RX_DATA (address : 203A). As seen in Fig. A.3.5 by using VisSim's externRead block contents of RX-DATA register are read and stored in variable _FA1 for comparison. The two pushbuttons selected for enabling/disabling PWM outputs of inverter #1 and inverter #2, have code 0120 hex and 0108 hex respectively. By comparing contents of variable _FA1 with either of the two hex numbers cited above will determine if any of the two inverters has been disabled.

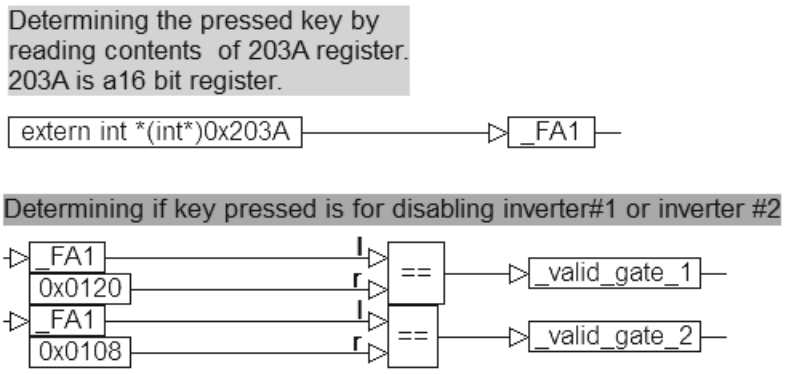


Figure A.3.5 Identifying pressed key of Accessory board.

- **PWM_for_inverters**: The compound block named PWM_for_inverters and its internal view is shown in Fig. A.3.6. Since TMSF2812 can generate six pairs of PWM output signals hence it is possible to use PWM1 up to PWM6 for one of the inverters and PWM7 up to PWM12 for the second inverter module. VisSim block that performs this job is named as F281X_Full Compare PWM [37].

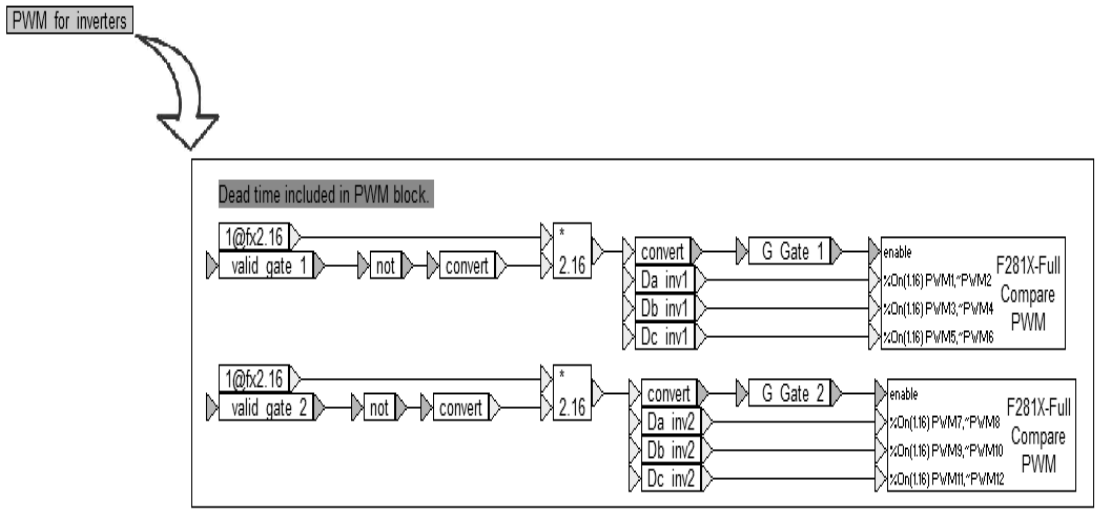


Figure A.3.6 VisSim fullCompare PWM block used for generation of PWM signals.

Main segments of compound block shown in Fig.A.3.6 are the two F281X_Full Compare PWM blocks, and each of these units has four inputs. Three of these inputs control duty cycle of the PWM waveforms scaled as per 1IQ16 format. The fourth pin is enable pin which if at logic zero would result in de-activation of the PWM block. Inside each Full Compare PWM block there are several parameters that user has to specify based on his systems requirements,

such as definition of event that cause loading of compare register, count mode, timer source, timer period, timer scaling and initial time count for the timer etc [37].

Voltage Source Inverters (VSIs) due to their excellent performance are widely used in the Industry. Presence of IGBT's in the inverter legs demands that a small time delay be applied between turn-on/turn-off times of the two switches sharing same leg of the inverter. This time gap is known as *deadband* and it helps in avoiding short-circuiting of low-side and high-side power devices [40].

Keeping this in view, VisSim has this important feature incorporated in its PWM block. There is provision of defining deadband between the two complimentary PWM outputs. In this case dead zone selected is 3.2 μ sec, which is sufficient for an IGBT based inverter. For adjusting this deadband, parameters such as *deadband- pre-scaler* and *deadband-tick-count* have to be defined inside each F281X_Full Compare PWM block [37].

- **Interleaving_Controller**: Internal view of compound block named Interleaving-Controller is shown in Fig. A.3.7. Outputs of this block are the duty cycle information which serves as input for the previously discussed F281X_Full Compare PWM units. This compound block is composed of many important units which are compound in nature as well. Two such units are *controller_for_inverter_1* and *controller_for_inverter_2*. Input of these two blocks is resultant of the block labelled *FFT*, details of the same will follow shortly. Internally, construction of *controller_for_inverter_1* and *controller_for_inverter_2* are similar to their Simulink version given in Chapter 3 and are therefore not discussed in detail here. As seen in Fig. A.3.7, outputs of these two blocks are variables named G_Theta_1 and G_Theta_2 respectively, which represent carrier phase in radians for the two inverters.

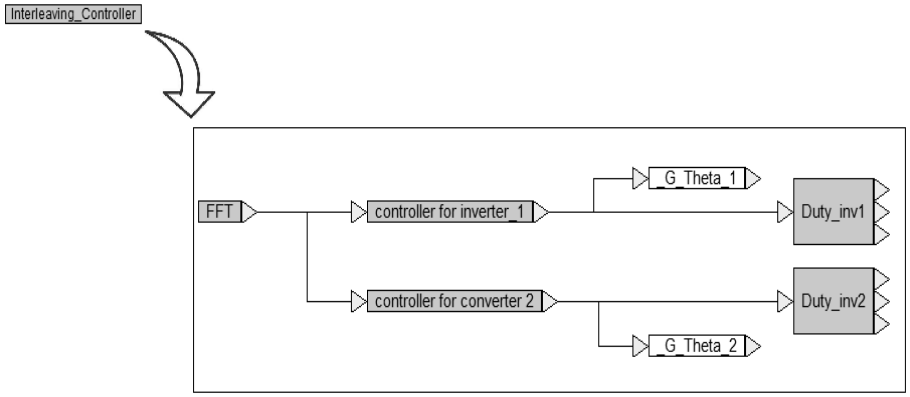


Figure A.3.7 Detailed view of compound block named Interleaving_Controller.

- **Duty_inv1**: Block shown in Fig.A.3.8 is responsible for generating duty cycle information which is fed to VisSim's Full Compare PWM unit associated with the first inverter. Second block similar in construction is *Duty_inv2,* which is used for generation of PWM signals for inverter#2. Referring back to Fig. A.3.8, block appearing in the top left corner called *Modulating_ signal* is constructed using pre-built model available under VisSim's *fixed-point* toolbox. As suggested by its name *Modulating_ signal* block is responsible for production of modulating sine waves of 60 Hz frequency for each of the three phases.

  Carrier waveform is generated making use of compound block named *Carrier_1*. Main constituent of it is triangular wave generating unit which also has a pre-built model available under fixed-point tool box. The only input of Carrier_1 block is phase information G_Theta_1 which was mentioned in the previous section.

  By comparing outputs of *Modulating_ signal* block with the output of *Carrier_1*, three signals (A1, A2 and A3) carrying duty cycle information for six switches of the full bridge inverter module, are generated. The difference between duty values stored in variables A1 and Da_inv1 is the format of the variables, with A1 being in integer format whereas Da_inv1 is in scaled integer format 1IQ16. Conversion to 1IQ16 format is a must as F281X_Full Compare PWM blocks of VisSim will only accept input that meets this specific criterion.

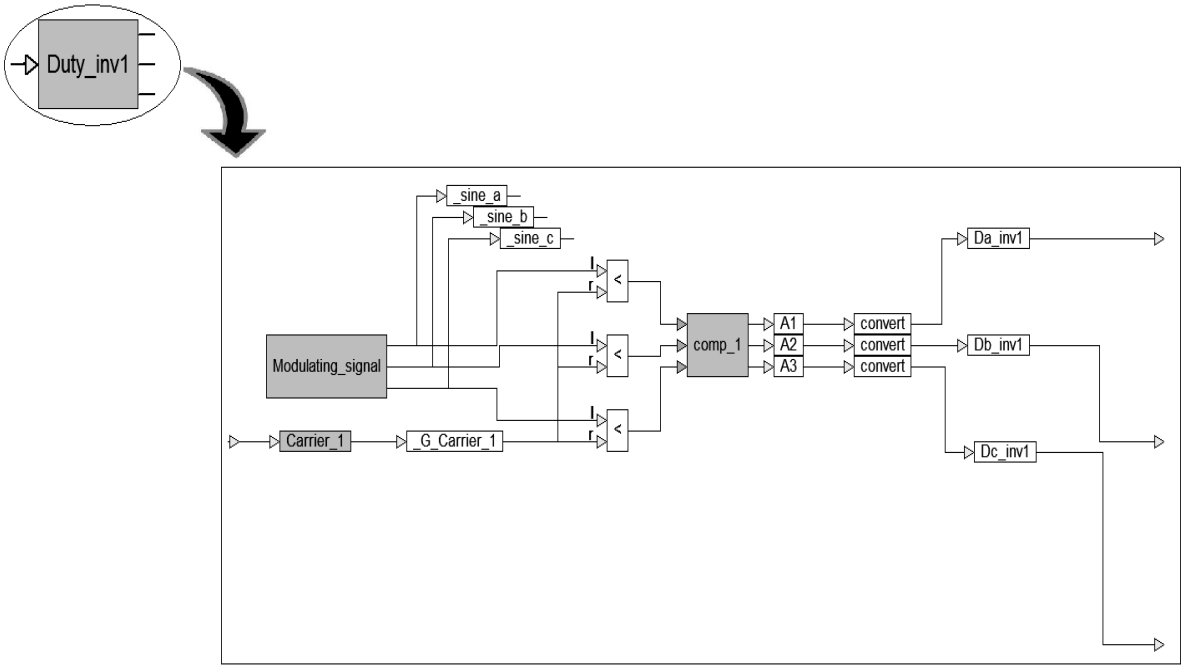


Figure A.3.8 VisSim compound block responsible for generating duty cycle information for the two full compare units.

- **FFT**: This block is composed of several smaller units and internal view of it is shown in Fig. A.3.9. Block named *AnalogInput* of VisSim is used for sending analog data to the block diagram. Based on the schematics of back-to-back converter modules available in laboratory, there are only two free analog input ports on the DSP-FPGA controller board namely ADCINA0 and ADCINB0. As in case of developed control algorithm the only analog feedback signal used by controller is total load side phase current, hence only one AnalogInput block is used inside FFT compound unit which will read the value of signal applied at analog input port 0.

  It can be noticed in Fig.A.3.9 that analog input is forwarded to a buffer block. This buffer unit falls under VisSim's block category called *matrix operations* and is useful in performing basic signal processing operations, FFT analysis being one of them. This block helps to produce a single vector output of a sequence of values available in the buffer, depending on selected buffer length and time gap between successive samples [41]. Time gap between samples is dictated by sampling time chosen for embedded controller design. Importance of converting input signal in vector format becomes evident from the fact that VisSim's block which performs Fast Fourier Transform of input signals named *fft*, processes information if and only if it is presented to it in vector form.

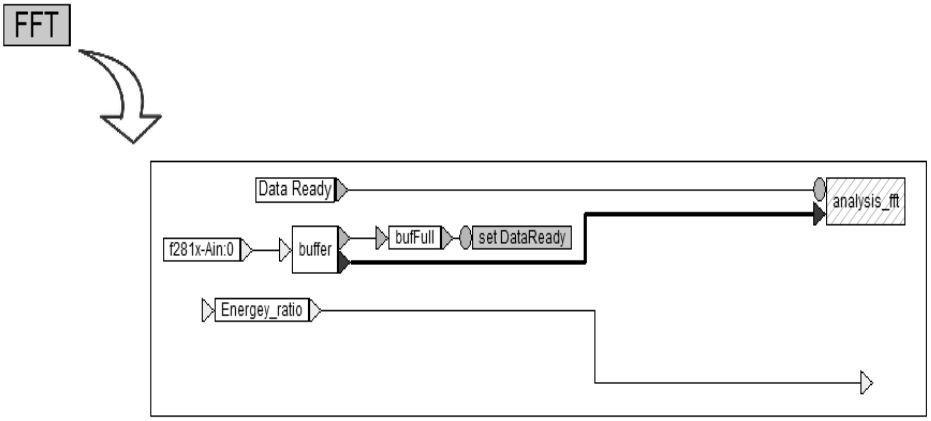


Figure A.3.9 Expanded view of FFT compound block.

Internal view of *analysis_fft* is shown in Fig.A.3.10. This compound unit is defined as an enabled block operating only once the buffer block is full. Extreme left block of Fig. A.3.10 converts output of buffer block into 128-sample-FFT of original signal at a sampling rate of 6600 Hz [41]. Hence resulting output of this block are Fourier coefficients that are further

utilized for carrying out mathematical computations for determination of Energy ratio. Definition of Energy ratio was presented earlier in Chapter 3 and as known through Simulink version of interleaving controller, this parameter is used in determination of best interleaving angle for system of parallel inverters.

Seen in Fig.A.3.10 are two other blocks named *reshape* and *magPhase*. Both these blocks are vital for proper operation of FFT compound unit. Function of *reshape* is to re-define dimensions of input matrix into number of rows and columns specified in its block properties [41]. In this case input matrix was arranged in two rows of 128 columns each. Block to the right of *reshape* i.e *magPhase* is available under VisSim's block category named *Arithmetic* and its function is to return magnitude and phase of an input signal that is in complex number format [41]. For sake of computing Energy ratio, the only output of *magPhase* block which is of our interest is magnitude of complex number and it is for this reason that phase output of this block is left un-utilized.

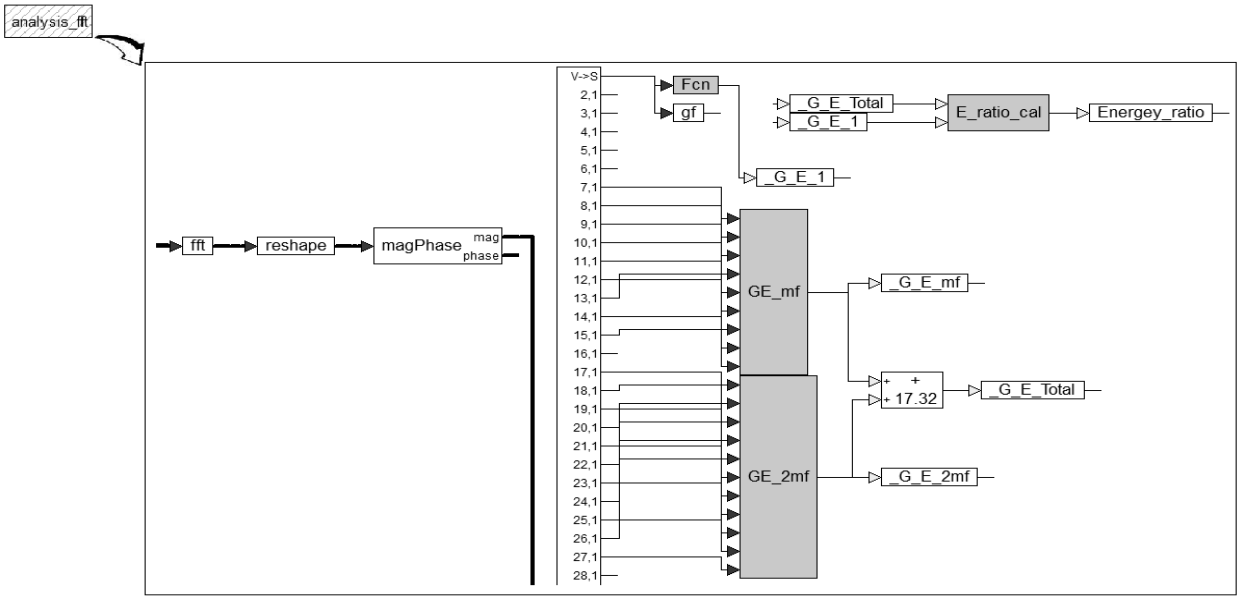


Figure A.3.10 View of compound block responsible for determination of Energy ratio.

This concludes discussion on model that is developed in VisSim for implementation of embedded version of autonomous interleaving controller. The finalized design was put to test with all power components of system in place and results obtained have been included in Chapter 4 of this thesis.

Appendix A-4

Code generated using VisSim for interleaving control algorithm

```
/*** VisSim Automatic C Code Generator Version 8.0B3 ***/
/*  Output for C:\Documents and Settings\user\Desktop\786finalexp5thJuly2012\
786_Inter_algomodelwith_bufferfull.vsm at Thu Jul 05 15:13:45 2012 */

#include "math.h"
#include "cgen.h"
#include "c2000.h"
#include "c2000.h"
#include "DMC32.h"
static MATRIX_DECL(256) _vt456_data={0,1,256,0};
static MATRIX * vt456=(MATRIX*)&_vt456_data;
static MATRIX_DECL(256) _vt454_data={0,2,128,0};
static MATRIX * vt454=(MATRIX*)&_vt454_data;
static MATRIX_DECL(128) _vt455_2_data={0,1,128,0};
static MATRIX * vt455_2=(MATRIX*)&_vt455_2_data;
static MATRIX_DECL(128) _vt455_1_data={0,1,128,0};
static MATRIX * vt455_1=(MATRIX*)&_vt455_1_data;
static char _vbufferCnt514=0;
static MATRIX_DECL(256) _vt514_2_data={0,1,256,0};
static MATRIX * vt514_2=(MATRIX*)&_vt514_2_data;
static int t514_1=0;
static void initMatVars() {
}

int _maxAnalogInChan=0;
int digitalInState[]={0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0};
int digitalOutState[]={0x40,0x40,0x0,0x0,0x0,0x0,0x0,0x0};
int fftDataReady;
extern int fftDataReady;
extern int fftDataReady;
static int _AA1;
static int _CA1;
static int _BA1;
static int _EA1;
static int MZ4;
static int _FA1;
static int _valid_gate_1;
static int _valid_gate_2;
```

```
static long _G_Theta_1;
static long _G_Theta_2;
static long _G_token_2;
static long _G_flag_1;
static long _G_trig_180_1;
static long _G_trig_0_1;
static long _G_T_1;
static long _G_trig_1;
static long _G_T_11;
static long _G_flag_1a;
static long _G_token_1;
static long _clock_4;
static int _G_Gate_1;
static long _G_T_2;
static long _G_T_22;
static long _G_trig_2;
static long _G_flag_2;
static long _G_trig_0_2;
static long _G_trig_180_2;
static int _G_Gate_2;
static long theta2_out;
static long ghq;
static int Dc_inv1;
static int Db_inv1;
static int Da_inv1;
static int Dc_inv2;
static int Db_inv2;
static int Da_inv2;
static int Source_2;
static int Source_1;
static int A1;
static int A2;
static int A3;
static int _G_Carrier_1;
static long MZ2;
static long MZ3;
static long Energey_ratio= 0;
static int data;
static int bufFull;
static CGDOUBLE gf= 0;
static long _G_E_sat= 0;
static long _G_E_1= 0;
static long _G_E_mf= 0;
static long _G_E_2mf= 0;
static long _G_E_Total= 0;
static CGDOUBLE _G_E_inverse= 0;
```

```
static int _sine_a;
static int _sine_b;
static int _sine_c;
static long __Out_559;
static long __step_558;
static int __rangePlusMinus1_561= 1;
static long __Out_597;
static long __step_596;
static int __rangePlusMinus1_599= 1;
static long __Out_635;
static long __step_634;
static int __rangePlusMinus1_637= 1;
static int __sum_673;
static int __sum_712;
static int _G_Carrier_2;
static int B1;
static int B2;
static int B3;
extern CGDOUBLE Zed;

/* set DataReady */
static void subsystem439()
{
  fftDataReady = 1;


}
static void subsystem443();
static ARG_DESCR outArgInfo443[]={
0};
static ARG_DESCR inArgInfo443[]={
  { T_MAT_DOUBLE,0,1,256},
};
static SIM_STATE tSubsystem443={0, 0.0001515, 0.8,0,0.0001515,0,0,0,0,0,0,0,0
,outArgInfo443, inArgInfo443,1,0,0,0,0,subsystem443,0,0,0,0,0,0,1};
SIM_STATE *hSubsystem443=&tSubsystem443;

/* FFT */
static void subsystem443()
{
  long t476;
  long t502;
  long t508;
  CGDOUBLE t510;
  matFft2( vt456,  hSubsystem443->inSigS[0]->u.m);
  memcpy( vt454->d,  vt456->d, sizeof(CGDOUBLE)*256);
```

```
  matMag( vt455_1,  vt454);
  matPhase( vt455_2,  vt454);
  t476 = ((((MUL_SHIFT32((MX(vt455_1, 0, 6)*0x10000),( MX(vt455_1, 0,
6)*0x10000),16))>>1)+((MUL_SHIFT32(( MX(vt455_1, 0, 8)*0x10000),(
          MX(vt455_1, 0, 8)*0x10000),16))>>1)+((MUL_SHIFT32(( MX(vt455_1, 0,
10)*0x10000),( MX(vt455_1, 0, 10)*0x10000),16))>>1)+((MUL_SHIFT32((
          MX(vt455_1, 0, 12)*0x10000),( MX(vt455_1, 0,
12)*0x10000),16))>>1)+((MUL_SHIFT32(( MX(vt455_1, 0, 14)*0x10000),( MX(vt455_1, 0,
14)*0x10000),16))>>1))+
         (((MUL_SHIFT32(( MX(vt455_1, 0, 7)*0x10000),( MX(vt455_1, 0,
7)*0x10000),16))>>1)+((MUL_SHIFT32(( MX(vt455_1, 0, 9)*0x10000),( MX(vt455_1, 0,
9)*0x10000),16))>>1)+((
          MUL_SHIFT32(( MX(vt455_1, 0, 10)*0x10000),( MX(vt455_1, 0,
10)*0x10000),16))>>1)+((MUL_SHIFT32(( MX(vt455_1, 0, 11)*0x10000),( MX(vt455_1, 0,
11)*0x10000),16))>>1)+((
          MUL_SHIFT32(( MX(vt455_1, 0, 13)*0x10000),( MX(vt455_1, 0,
13)*0x10000),16))>>1)));
  t502 = ((MUL_SHIFT32(( MX(vt455_1, 0, 17)*0x20000),( MX(vt455_1, 0,
17)*0x20000),17)+MUL_SHIFT32(( MX(vt455_1, 0, 19)*0x20000),(
          MX(vt455_1, 0, 19)*0x20000),17)+MUL_SHIFT32(( MX(vt455_1, 0, 21)*0x20000),(
MX(vt455_1, 0, 21)*0x20000),17)+MUL_SHIFT32(( MX(vt455_1, 0, 23)*0x20000),(
          MX(vt455_1, 0, 23)*0x20000),17)+MUL_SHIFT32(( MX(vt455_1, 0, 25)*0x20000),(
MX(vt455_1, 0, 25)*0x20000),17))+(MUL_SHIFT32(( MX(vt455_1, 0, 16)*0x20000),(
          MX(vt455_1, 0, 16)*0x20000),17)+MUL_SHIFT32(( MX(vt455_1, 0, 18)*0x20000),(
MX(vt455_1, 0, 18)*0x20000),17)+MUL_SHIFT32(( MX(vt455_1, 0, 20)*0x20000),(
          MX(vt455_1, 0, 20)*0x20000),17)+MUL_SHIFT32(( MX(vt455_1, 0, 22)*0x20000),(
MX(vt455_1, 0, 22)*0x20000),17)+MUL_SHIFT32(( MX(vt455_1, 0, 24)*0x20000),(
          MX(vt455_1, 0, 24)*0x20000),17)+MUL_SHIFT32(( MX(vt455_1, 0, 26)*0x20000),(
MX(vt455_1, 0, 26)*0x20000),17)));
  _G_E_Total = ( t476+(( t502)>>2));
  _G_E_1 = MUL_SHIFT32(( MX(vt455_1, 0, 0)*0x10000),( MX(vt455_1, 0, 0)*0x10000),16);
  t508 =  _G_E_1 ;
  t508 = MIN(327680000L,t508);
  t508 = MAX(t508,65536L);
;
  t510 = 1./(( t508 * 1.52587890625e-005));
  Energey_ratio = MUL_SHIFT32( _G_E_Total ,( t510*0x100),15);
  fftDataReady = 0;


}
static int threadTimer443=0;

/* vsmIdleLoop for background threads */
void idleLoop()
{
```

```
  if (hSubsystem443->isEnabled && (unsigned)(sim->tickCount-threadTimer443)<0x7fff) {
    threadTimer443 = sim->tickCount + 7;
    subsystem443();
  }
}
static INTERRUPT void cgMain();
static SIM_STATE tSim={0, 0.0001515, 0.8,0,0.0001515,0,0,0,0,0,0,0,0
,0,0,0,0,0,0,0,cgMain,0,0,0,0,0,0,0};
SIM_STATE *sim=&tSim;
static INTERRUPT void cgMain()
{
static long _delayOutBuf557=0;
static char _pulseCnt147=1;
  char t147;
static long _delayOutBuf142=0;
static long _delayInBuf142=0;
static int _delayOutBuf259=0;
static int _delayOutBuf252=0;
static int _delayOutBuf56=0;
static int _delayOutBuf49=0;
static long _delayOutBuf75=0;
static long _delayOutBuf68=0;
static long _delayOutBuf277=0;
static long _delayOutBuf270=0;
  long t146;
static long _delayOutBuf289=0;
static long _delayInBuf289=0;
  int t330;
  long t333;
static long _delayOutBuf240=0;
static long _delayInBuf240=0;
  int t337;
static long _delayOutBuf242=0;
static long _delayInBuf242=0;
static char _pulseCnt357=-1;
  char t357;
static long _delayOutBuf358=0;
static long _delayInBuf358=0;
  long t326;
static long _delayOutBuf244=0;
static long _delayInBuf244=0;
static long _delayOutBuf246=0;
static long _delayInBuf246=0;
static char _pulseCnt366=-1;
  char t366;
static long _delayOutBuf367=0;
```

```
static long _delayInBuf367=0;
static int _delayOutBuf708=0;
static int _delayOutBuf669=-32768;
static long _delayOutBuf595=357913941;
static long _delayOutBuf633=715827882;
static long _delayOutBuf154=0;
static long _delayInBuf154=0;
  int t172;
  long t175;
static long _delayOutBuf110=0;
static long _delayInBuf110=0;
  int t165;
static long _delayOutBuf106=0;
static long _delayInBuf106=0;
static char _pulseCnt193=-1;
  char t193;
static long _delayOutBuf194=0;
static long _delayInBuf194=0;
  long t183;
static long _delayOutBuf108=0;
static long _delayInBuf108=0;
static long _delayOutBuf104=0;
static long _delayInBuf104=0;
static char _pulseCnt202=-1;
  char t202;
static long _delayOutBuf203=0;
static long _delayInBuf203=0;
  int t530;
  long t551;
  int t555;
  long t537;
  int _inSig_255;
  int _inSig_248;
  int _inSig_52;
  int _inSig_45;
  long t126;
  long t237;
  long _inSig_71;
  long _inSig_64;
  int t58;
  long t61;
  int t77;
  long t80;
  long t155;
  long _inSig_273;
  long _inSig_266;
```

```
  int t261;
  long t264;
  int t279;
  long t282;
  long t314;
  int t286;
  long t285;
  int t717;
  int t731;
  int t678;
  int t692;
  long t589;
  int t593;
  long t575;
  long t627;
  int t631;
  long t613;
  int t151;
  long t150;
  int t718;
  int t728;
static int _sampBuf727=0;
  int t679;
  int t689;
static int _sampBuf688=0;
  int t433;
  int t649;
  int t657;
  long t565;
  int t653;
  int t650;
  long t312;
  long t348;
  int _out_707;
  int _out_668;
  int t398;
  int t758;
  int t759;
  long t139;
  int t663;
  int t519;
  int t527;
  long t603;
  int t651;
  long t641;
  int t652;
```

```
  ADCTRL2 = 0x140;  // Reset ADC Seq
  ADCTRL2 = 0x120;  // Trigger ADC
  t147 = (++_pulseCnt147 > 1?_pulseCnt147=0,1:0);
if ( t147) _delayOutBuf142=_delayInBuf142;
  t146 = ( _delayOutBuf142+((1073741824 /* 1@fx2.32 */)>>30));
  _clock_4 =  t146;
if ( _clock_4 ) _delayOutBuf289=_delayInBuf289;
  _G_flag_2 =  _delayOutBuf289;
  t330 =  _G_flag_2 ?( _G_flag_2>((116391936 /* 111@fx12.32 */)>>20)):(
_G_flag_2<=((116391936 /* 111@fx12.32 */)>>20));
  t333 = ((long)( t330)<<30);
  _G_trig_180_2 =  t333;
if ((int)(( _G_trig_180_2 )>>30)) _delayOutBuf240=_delayInBuf240;
  t337 =  _G_flag_2 ?( _G_flag_2<=((116391936 /* 222@fx13.32 */)>>19)):(
_G_flag_2>((116391936 /* 222@fx13.32 */)>>19));
  _G_trig_2 = ((long)( t337)<<30);
if ((int)(( _G_trig_2 )>>30)) _delayOutBuf242=_delayInBuf242;
  t357 = (++_pulseCnt357 > 0?_pulseCnt357=0,1:0);
if ( t357) _delayOutBuf358=_delayInBuf358;
  t326 = MUL_SHIFT32(((((int)( _G_flag_2 >((116391936 /* 111@fx12.32 */)>>20)))&((int)(
_G_flag_2<=((116391936 /* 222@fx13.32 */)>>19))))*0x1),
          1073741824 /* 1@fx2.32 */,30);
  _G_trig_0_2 =  t326;
if ( _G_trig_0_2 ) _delayOutBuf244=_delayInBuf244;
if ((int)(( _G_trig_2 )>>30)) _delayOutBuf246=_delayInBuf246;
  t366 = (++_pulseCnt366 > 0?_pulseCnt366=0,1:0);
if ( t366) _delayOutBuf367=_delayInBuf367;
if ( t146) _delayOutBuf154=_delayInBuf154;
  _G_flag_1 =  _delayOutBuf154;
  t172 =  _G_flag_1 ?( _G_flag_1>((116391936 /* 111@fx12.32 */)>>20)):(
_G_flag_1<=((116391936 /* 111@fx12.32 */)>>20));
  t175 = ((long)( t172)<<30);
  _G_trig_180_1 =  t175;
if ((int)(( _G_trig_180_1 )>>30)) _delayOutBuf110=_delayInBuf110;
  t165 =  _G_flag_1 ?( _G_flag_1<=((116391936 /* 222@fx13.32 */)>>19)):(
_G_flag_1>((116391936 /* 222@fx13.32 */)>>19));
  _G_trig_1 = ((long)( t165)<<30);
if ((int)(( _G_trig_1 )>>30)) _delayOutBuf106=_delayInBuf106;
  t193 = (++_pulseCnt193 > 0?_pulseCnt193=0,1:0);
if ( t193) _delayOutBuf194=_delayInBuf194;
  t183 = MUL_SHIFT32(((((int)( _G_flag_1 >((116391936 /* 111@fx12.32 */)>>20)))&((int)(
_G_flag_1<=((116391936 /* 222@fx13.32 */)>>19))))*0x1),
          1073741824 /* 1@fx2.32 */,30);
  _G_trig_0_1 =  t183;
if ( _G_trig_0_1 ) _delayOutBuf108=_delayInBuf108;
if ((int)(( _G_trig_1 )>>30)) _delayOutBuf104=_delayInBuf104;
```

```
  t202 = (++_pulseCnt202 > 0?_pulseCnt202=0,1:0);
if ( t202) _delayOutBuf203=_delayInBuf203;
  t530 = 1920 /* 60@fx11.16 */;
  __step_558 = MUL_SHIFT32(162671,((long)( t530)<<16),20);
  t551 = ( _delayOutBuf557+(( __step_558 )>>1));
  t555 = (1073741716 /* 1@fx2.32 */< t551);
  __Out_559 =  _delayOutBuf557;
  t537 = ( t555?(( t555?-1073741824:0 /* 0@fx2.32 */)+((( __step_558 )>>1)+ __Out_559 )):
t551);
  _FA1 =  *(int*)0x203A;
  _valid_gate_2 = ( _FA1 ==264);
  _G_Gate_2 = (int)((long)(MUL_SHIFT16(16384 /* 1@fx2.16 */,(int)((long)(!((int)
_valid_gate_2 ))<<14),14))>>14);
  _inSig_255 =  _G_Gate_2 ;
  _inSig_248 =  _G_Gate_2;
  _valid_gate_1 = ( _FA1 ==288);
  _G_Gate_1 = (int)((long)(MUL_SHIFT16(16384 /* 1@fx2.16 */,(int)((long)(!((int)
_valid_gate_1 ))<<14),14))>>14);
  _inSig_52 =  _G_Gate_1 ;
  _inSig_45 =  _G_Gate_1;
  t126 = (MUL_SHIFT32((( _G_Gate_1 ==0 /* 0@fx3.32 */)*0x20000000),-1073741824 /* -
1@fx2.32 */,30)+MUL_SHIFT32((( _G_Gate_1==1073741824 /* 1@fx2.32 */)*0x20000000),
          0 /* 0@fx1.32 */,31));
  _G_token_1 =  t126;
  t237 = (( _G_token_1 >=((0 /* 0@fx1.32 */)>>2))?(( _G_Gate_2 *0x20000000)+ _G_token_1
):(MUL_SHIFT32((( _G_Gate_2 ==1073741824 /* 1@fx2.32 */)*0x20000000),
          0 /* 0@fx1.32 */,31)+MUL_SHIFT32((( _G_Gate_2==0 /* 0@fx1.32
*/)*0x20000000),-1073741824 /* -1@fx2.32 */,30)));
  _G_token_2 =  t237;
  _inSig_71 =  _G_token_2 ;
  _inSig_64 =  _G_token_2;
  t58 = (int)((long)(( _inSig_52 < _delayOutBuf56))<<8);
  t61 = ((long)((((int)(int)((long)( t58)>>8))|((int)( _inSig_45 > _delayOutBuf49))))<<30);
  t77 = (int)((long)(( _inSig_71 < _delayOutBuf75))<<8);
  t80 = ((long)((((int)(int)((long)( t77)>>8))|((int)( _inSig_64 > _delayOutBuf68))))<<30);
  t155 = (((((long)(( t61)>>30))|((long)(( t80)>>30))))<<30);
  _G_flag_1a =  t155;
  _inSig_273 =  _G_flag_1a ;
  _inSig_266 =  _G_flag_1a;
  t261 = (int)((long)(( _inSig_255 < _delayOutBuf259))<<8);
  t264 = ((long)((((int)(int)((long)( t261)>>8))|((int)( _inSig_248 > _delayOutBuf252))))<<30);
  t279 = (int)((long)(( _inSig_273 < _delayOutBuf277))<<8);
  t282 = ((long)((((int)(int)((long)( t279)>>8))|((int)( _inSig_266 > _delayOutBuf270))))<<30);
  t314 = (((((long)(( t264)>>30))|((long)(( t282)>>30))))<<30);
  t286 = 0 /* 0@fx16.16 */;
  t285 = ((int)(( t314)>>30)?((long)( t286)):( _delayOutBuf289+1 /* 1@fx32.32 */));
```

```
  __sum_712 = ( _delayOutBuf708+( _sampBuf727?-6552:6552));
  t717 = ( __sum_712 <6552);
  t731 = ( t717?0 /* 0@fx1.16 */: __sum_712 );
  __sum_673 = ( _delayOutBuf669+( _sampBuf688?-6552:6552));
  t678 = ( __sum_673 <6552);
  t692 = ( t678?0 /* 0@fx1.16 */: __sum_673 );
  __step_596 = MUL_SHIFT32(162671,((long)( t530)<<16),20);
  t589 = ( _delayOutBuf595+(( __step_596 )>>1));
  t593 = (1073741716 /* 1@fx2.32 */< t589);
  __Out_597 =  _delayOutBuf595;
  t575 = ( t593?(( t593?-1073741824:0 /* 0@fx2.32 */)+((( __step_596 )>>1)+ __Out_597 )):
t589);
  __step_634 = MUL_SHIFT32(162671,((long)( t530)<<16),20);
  t627 = ( _delayOutBuf633+(( __step_634 )>>1));
  t631 = (1073741716 /* 1@fx2.32 */< t627);
  __Out_635 =  _delayOutBuf633;
  t613 = ( t631?(( t631?-1073741824:0 /* 0@fx2.32 */)+((( __step_634 )>>1)+ __Out_635 )):
t627);
  t151 = 0 /* 0@fx16.16 */;
  t150 = ((int)(( t155)>>30)?((long)( t151)):( _delayOutBuf154+1 /* 1@fx32.32 */));
  t718 = (((int) t717)|((int)( __sum_712 >32440 /* 0.99@fx1.16 */)));
  t728 = !((int) _sampBuf727);
  t679 = (((int) t678)|((int)( __sum_673 >32440 /* 0.99@fx1.16 */)));
  t689 = !((int) _sampBuf688);
  t433 = (ADCRESULT0>>4);
  _AA1 =  *(int*)0x203B;
  _BA1 = ( _AA1  >> 4);
  _CA1 = ( _BA1  << 4);
  _EA1 = (((int) _CA1 )|((int)6));
  t649 = 2048 /* 0.5@fx4.16 */;
  t657 = 2048 /* 0.5@fx4.16 */;
  t565 = 1?(MUL_SHIFT32( __Out_559 ,1073741824L,29)/* 2@fx2.32 */+-1073741824 /* -
1@fx2.32 */): __Out_559;
  t653 = 3481 /* 0.85@fx4.16 */;
  t650 = ( t649+MUL_SHIFT16(MUL_SHIFT16( t657,(short)((fxSin32( t565))>>16),15),
t653,12));
  _sine_a =  t650;
  _G_T_2 = (MUL_SHIFT32(1686633657 /* 3.1416@fx3.32 */, t333,30)+(0 /* 0@fx3.32 */*
t326));
  _G_T_22 = (MUL_SHIFT32((( _delayOutBuf358<
_delayOutBuf367)*0x20000000),1686633657 /* 3.1416@fx3.32 */,29)+MUL_SHIFT32((( 
_delayOutBuf358>
          _delayOutBuf367)*0x20000000),0 /* 0@fx1.32 */,31));
  t312 = MUL_SHIFT32((MUL_SHIFT32(((((  _G_trig_2 )>>1)==0 /* 0@fx3.32
*/)*0x20000000), _G_T_2 ,29)+MUL_SHIFT32(((((  _G_trig_2)>>1)!=
        0 /* 0@fx3.32 */)*0x20000000), _G_T_22 ,29)), t237,29);
```

```
  theta2_out =  t312;
  t348 = (( t312<0 /* 0@fx3.32 */)? -( theta2_out ): theta2_out );
  _out_707 =  _delayOutBuf708;
  Source_1 =  _out_707 ;
  _out_668 =  _delayOutBuf669;
  Source_2 =  _out_668 ;
  t398 = (( t348==((long)(0 /* 0@fx1.16 */)<<14))? Source_1 : Source_2 );
  _G_Carrier_2 =  t398;
  t758 = 0 /* 0@fx2.16 */;
  t759 = 16384 /* 1@fx2.16 */;
  B1 = (( _sine_a <(int)((long)( _G_Carrier_2 )>>3))? t758: t759);
  Da_inv2 = (int)((long)( B1 )<<1);
  _G_T_1 = (MUL_SHIFT32(1686633657 /* 3.1416@fx3.32 */, t175,30)+(0 /* 0@fx3.32 */*
t183));
  _G_T_11 = (MUL_SHIFT32((( _delayOutBuf194<
_delayOutBuf203)*0x20000000),1686633657 /* 3.1416@fx3.32 */,29)+MUL_SHIFT32(((
_delayOutBuf194>
          _delayOutBuf203)*0x20000000),0 /* 0@fx1.32 */,31));
  t139 = MUL_SHIFT32((MUL_SHIFT32((( _G_trig_1 ==((0 /* 0@fx1.32
*/)>>1))*0x20000000), _G_T_1 ,29)+MUL_SHIFT32((( _G_trig_1!=((0 /* 0@fx1.32
*/)>>1))*0x20000000),
          _G_T_11 ,29)),(( t126>=0 /* 0@fx3.32 */)? _G_token_1 :0 /* 0@fx3.32 */),29);
  t663 = (( t139==((long)(0 /* 0@fx1.16 */)<<14))? Source_1 : Source_2 );
  _G_Carrier_1 =  t663;
  t519 = 0 /* 0@fx2.16 */;
  t527 = 16384 /* 1@fx2.16 */;
  A1 = (( t650<(int)((long)( _G_Carrier_1 )>>3))? t519: t527);
  Da_inv1 = (int)((long)( A1 )<<1);
  t603 = 1?(MUL_SHIFT32( __Out_597 ,1073741824L,29)/* 2@fx2.32 */+-1073741824 /* -
1@fx2.32 */): __Out_597;
  t651 = ( t649+MUL_SHIFT16(MUL_SHIFT16( t657,(short)((fxSin32( t603))>>16),15),
t653,12));
  A2 = (( t651<(int)((long)( _G_Carrier_1)>>3))? t519: t527);
  Db_inv1 = (int)((long)( A2 )<<1);
  t641 = 1?(MUL_SHIFT32( __Out_635 ,1073741824L,29)/* 2@fx2.32 */+-1073741824 /* -
1@fx2.32 */): __Out_635;
  t652 = ( t649+MUL_SHIFT16(MUL_SHIFT16( t657,(short)((fxSin32( t641))>>16),15),
t653,12));
  A3 = (( t652<(int)((long)( _G_Carrier_1)>>3))? t519: t527);
  Dc_inv1 = (int)((long)( A3 )<<1);
  _sine_b =  t651;
  B2 = (( _sine_b <(int)((long)( _G_Carrier_2)>>3))? t758: t759);
  Db_inv2 = (int)((long)( B2 )<<1);
  _sine_c =  t652;
  B3 = (( _sine_c <(int)((long)( _G_Carrier_2)>>3))? t758: t759);
  Dc_inv2 = (int)((long)( B3 )<<1);
```

```
  bufFull =  t514_1;
  if ( bufFull  )
  { /* set DataReady */
    subsystem439();
  }
;
  { EALLOW; WDKEY=0x55; WDKEY=0xAA; EDIS; /* Reset watchdog ctr */ };
  XINTCNF2 = 7L;
  XTIMING0 = 219308L;
  *(int*)0x203B =  _EA1 ;
  if ((int)((long)( Da_inv2 )>>15))
    GPBSET = 0x40;
  else
    GPBCLEAR = 0x40;
  if ((int)((long)( Da_inv1 )>>15))
    GPASET = 0x40;
  else
    GPACLEAR = 0x40;
  if ( _G_Gate_1 )
    { GPTCONA |= 0x40;  COMCONA |= 0x200;}
    else
    { GPTCONA &= 0xFFCF; COMCONA &= 0xFDFF;}
  CMPR1 = (int)(((long) Da_inv1 *710)>>15);
  CMPR2 = (int)(((long) Db_inv1 *710)>>15);
  CMPR3 = (int)(((long) Dc_inv1 *710)>>15);
;
  if ( _G_Gate_2 )
    { GPTCONB |= 0x40;  COMCONB |= 0x200;}
    else
    { GPTCONB &= 0xFFCF; COMCONB &= 0xFDFF;}
  CMPR4 = (int)(((long) Da_inv2 *710)>>15);
  CMPR5 = (int)(((long) Db_inv2 *710)>>15);
  CMPR6 = (int)(((long) Dc_inv2 *710)>>15);
;
    hSubsystem443->inSigS[0]->u.m =  vt514_2;
  hSubsystem443->isEnabled =  fftDataReady;
;

  t514_1 = matCircBuffer( vt514_2,  t433);
  _delayOutBuf557= t537;
  if ( t147)
    _delayInBuf142= t146;
  _delayOutBuf259= _inSig_255 ;
  _delayOutBuf252= _inSig_248 ;
  _delayOutBuf56= _inSig_52 ;
  _delayOutBuf49= _inSig_45 ;
```

```
  _delayOutBuf75= _inSig_71 ;
  _delayOutBuf68= _inSig_64 ;
  _delayOutBuf277= _inSig_273 ;
  _delayOutBuf270= _inSig_266 ;
  if ( _clock_4)
    _delayInBuf289= t285;
  if ((int)(( _G_trig_180_2)>>30))
    _delayInBuf240= Energey_ratio ;
  if ((int)(( _G_trig_2)>>30))
    _delayInBuf242= _delayOutBuf240;
  if ( t357)
    _delayInBuf358= _delayOutBuf242;
  if ( _G_trig_0_2)
    _delayInBuf244= Energey_ratio;
  if ((int)(( _G_trig_2)>>30))
    _delayInBuf246= _delayOutBuf244;
  if ( t366)
    _delayInBuf367= _delayOutBuf246;
  _delayOutBuf708= t731;
  _delayOutBuf669= t692;
  _delayOutBuf595= t575;
  _delayOutBuf633= t613;
  if ( t146)
    _delayInBuf154= t150;
  if ((int)(( _G_trig_180_1)>>30))
    _delayInBuf110= Energey_ratio;
  if ((int)(( _G_trig_1)>>30))
    _delayInBuf106= _delayOutBuf110;
  if ( t193)
    _delayInBuf194= _delayOutBuf106;
  if ( _G_trig_0_1)
    _delayInBuf108= Energey_ratio;
  if ((int)(( _G_trig_1)>>30))
    _delayInBuf104= _delayOutBuf108;
  if ( t202)
    _delayInBuf203= _delayOutBuf104;
  if ( t718)
    _sampBuf727 =  t728;
  if ( t679)
    _sampBuf688 =  t689;
  sim->tickCount++;
  endOfSampleCount = TIMER2TIM;

}

main()
```

```
{
 noIntegrationUsed = 1;
 EALLOW;
 PLLSTS = 0x10; // reset clk check
 WDCR=0x00ef;       // Disable Watchdog
 asm(" clrc DBGM");
 if (!(PLLSTS&8))     // Skip PLL set if OSC failure
   { PLLSTS = 0x40;  //Disable OSC check
     PLLCR = 0xa;      // set PLL to 5xOSC = 150 MHZ;
     PLLSTS = 0x0;     //Enable OSC check (&F283xx /2 mode)
   }
 PCLKCR |= 0xb;
 HISPCP = 0x0;    // HCLK  = 150 MHZ
 LOSPCP = 0x0;    // LSPCLK  = 150 MHZ
 EDIS;
 T1PR = 0x2c6;
 T1CNT = 0;
 T3PR = 0x2c6;
 T3CNT = 256;
 GPTCONA = 0x100;
 ACTRA = 0x666;
 CMPR1 = CMPR2 = CMPR3 = 0;
 COMCONA = 0x8200;
 DBTCONA = 0xff4;
 GPTCONB = 0x40;
 ACTRB = 0x666;
 CMPR4 = CMPR5 = CMPR6 = 0;
 COMCONB = 0x8200;
 DBTCONB = 0xff4;
 ADCTRL1_VAL = 0x300;
 ADCTRL2_VAL = 0x100;
 ADCTRL3_VAL = 0x6;
 ADCTRL3 = 0xE0;  // Power up ADC
 ADCCHSELSEQ1 = 0x3210;
 ADCCHSELSEQ2 = 0x7654;
 ADCCHSELSEQ3 = 0xba98;
 ADCCHSELSEQ4 = 0xfedc;
 ADCMAX_CONV = 0x0;
 hSubsystem443 = cgInitSubsystem(hSubsystem443, &tSubsystem443);
simInit( &tSim );
 initMatVars();
 startSimDsp();
 installInterruptVec(-2,7,cgMain);
 TIMER2PRD = 0x58c5; // 32-bit Timer Period Low
 TIMER2PRDH = 0x0; // 32-bit Timer Period High
 TIMER2TCR |= 0x4020; //Interrupt enable, Timer Reset
```

```
  EALLOW;
  PIECTRL = 1; // Enable PIE Interrupts
  EDIS;
  IER |= 0x2000; //CPU Interrupt enable
  resetInterrupts();
  enable_interrupts();  // Global Start Interrupts
  T1CON = 0x8c40; // Start timer
  T3CON = 0x8c40; // Start timer
  EALLOW;
  WDCR = 0x2A; /* Enable watchdog */
  EDIS;
  dspWaitStandAlone();
  return 0;
}
```

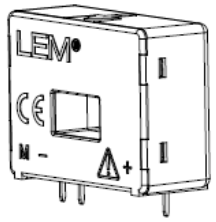
Appendix A-5

Current Transducer LA 100-P

I_{PN} = 100 A

For the electronic measurement of currents: DC, AC, pulsed..., with galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).

16019



Electrical data

I_{PN}	Primary nominal current rms			100			A
I_{PM}	Primary current, measuring range			0 .. ± 150			A
R_M	Measuring resistance @		T_A = 70°C		T_A = 85°C		
			$R_{M\,min}$	$R_{M\,max}$	$R_{M\,min}$	$R_{M\,max}$	
	with ± 12 V	@ ± 100 A_{max}	0	50	0	42	Ω
		@ ± 120 A_{max}	0	22	0	14	Ω
	with ± 15 V	@ ± 100 A_{max}	0	110	20	102	Ω
		@ ± 150 A_{max}	0	33	20	25	Ω
I_{SN}	Secondary nominal current rms			50			mA
K_N	Conversion ratio			1 : 2000			
V_C	Supply voltage (± 5 %)			± 12 .. 15			V
I_C	Current consumption			10 (@ ± 15 V) + I_S			mA

Accuracy - Dynamic performance data

X	Accuracy @ I_{PN}, T_A = 25°C	@ ± 15 V (± 5 %)	± 0.45		%
		@ ± 12 .. 15 V (± 5 %)	± 0.70		%
ε_L	Linearity error		< 0.15		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.10	mA
I_{OM}	Magnetic offset current [1] @ I_P = 0 and specified R_M, after an overload of 3 x I_{PN}			± 0.15	mA
I_{OT}	Temperature variation of I_O	- 25°C .. + 85°C	± 0.05	± 0.30	mA
		- 40°C .. - 25°C	± 0.10	± 0.50	mA
t_{ra}	Reaction time to 10 % of I_{PN} step		< 500		ns
t_r	Response time [2] to 90 % of I_{PN} step		< 1		µs
di/dt	di/dt accurately followed		> 200		A/µs
BW	Frequency bandwidth (- 1 dB)		DC .. 200		kHz

General data

T_A	Ambient operating temperature		- 40 .. + 85	°C
T_S	Ambient storage temperature		- 40 .. + 90	°C
R_S	Secondary coil resistance	@ T_A = 70°C	120	Ω
		@ T_A = 85°C	128	Ω
m	Mass		18	g
	Standards [3]		EN 50178: 1997	

Notes: [1] Result of the coercive field of the magnetic circuit
[2] With a di/dt of 100 A/µs
[3] A list of corresponding tests is available.

Features

- Closed loop (compensated) current transducer using the Hall effect
- Printed circuit board mounting
- Insulated plastic case recognized according to UL 94-V0.

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Application domain

- Industrial.

Current Transducer LA 100-P

Isolation characteristics

V_d	Rms voltage for AC isolation test, 50 Hz, 1 min	2.5	kV
$\hat{V}_w$	Impulse withstand voltage 1.2/50 µs	4.5	kV
		Min	
dCp	Creepage distance	3.8	mm
dCl	Clearance distance	3.8	mm
CTI	Comparative Tracking Index (group IIIa)	175	

Applications examples

According to EN 50178 and IEC 61010-1 standards and following conditions:

- Over voltage category OV 3
- Pollution degree PD2
- Non-uniform field

	EN 50178	IEC 61010-1
dCp, **dCl**, $\hat{V}_w$	Rated isolation voltage	Nominal voltage
Single isolation	300 V	300 V
Reinforced isolation	150 V	150 V

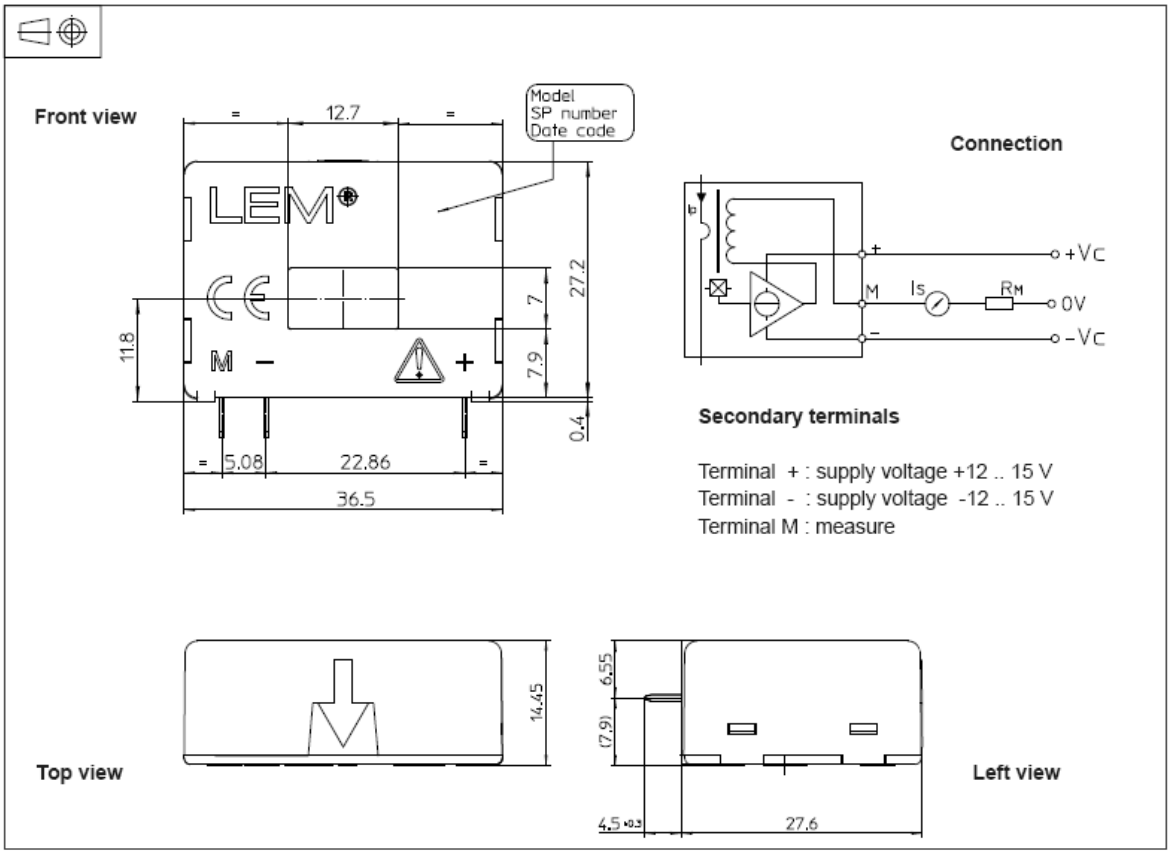
Safety

This transducer must be used in electric/electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.

Caution, risk of electrical shock

When operating the transducer, certain parts of the module can carry hazardous voltage (eg. primary busbar, power supply).
Ignoring this warning can lead to injury and/or cause serious damage.
This transducer is a build-in device, whose conducting parts must be inaccessible after installation.
A protective housing or additional shield could be used.
Main supply must be able to be disconnected.

Dimensions LA 100-P (in mm. 1 mm = 0.0394 inch)



Mechanical characteristics

• General tolerance	± 0.2 mm
• Primary through-hole	12.7 x 7 mm
• Fastening & Connection of secondary	3 pins 0.63 x 0.56 mm
• Recommended PCB hole	0.9 mm

Remarks

- I_S is positive when I_P flows in the direction of the arrow.
- Temperature of the primary conductor should not exceed 100°C.
- Dynamic performances (di/dt and response time) are best with a single bar completely filling the primary hole.
- In order to achieve the best magnetic coupling, the primary windings have to be wound over the top edge of the device.
- This is a standard model. For different versions (supply voltages, turns ratios, unidirectional measurements...), please contact us.

References

[1] Michalke G. (2008). Variable Speed Wind Turbines Modeling, Control, and Impact on Power Systems. Ph.D. Thesis. Institute of Electrical Power Systems, TU Darmstadt, Germany.

[2] Binder A., Schneider T., "Permanent magnet synchronous generators for regenerative energy conversion – a survey, " European Conference on Power Electronics and applications, EPE 2005, 11-14 September, Dresden, Germany, 2005.

[3] S.M.Muyeen,Junji Tamura,Toshiaki Murata, Stability Augmentation of Grid-connected Wind Farm, Springer-Verlag,London,Oct 2008.

[4] Chinchilla, M.; Arnaltes, S.; Burgos, J.C.;, "Control of permanent-magnet generators applied to variable-speed wind-energy systems connected to the grid," *Energy Conversion, IEEE Transactions on* , vol.21, no.1, pp. 130- 135, March.

[5] J. Birk and B. Andresen, "Parallel-connected Converters for Optimizing Efficiency, Reliability and Grid Harmonics in a Wind Turbine," 12th European Conference on Power Electronics and Applications (EPE 2007), Aalborg, Denmark, 2007.

[6] Zhuang Xu; Rui Li; Hui Zhu; Dianguo Xu; Zhang, C.C.H.; , "Control of Parallel Multiple Converters for Direct-Drive Permanent-Magnet Wind Power Generation Systems," *Power Electronics, IEEE Transactions on* , vol.27, no.3, pp.1259-1270, March 2012.

[7] Shah S., (2008). Design & Implementation of Parallel Operation of Inverters with Instantaneous Current Sharing Scheme using Multi-loop Control Strategy on FPGA Platform, Master of Technology, Indian Institute of Technology, Kanpur, India.

[8] P. Shenoy, "Local control of multiple module converters with ratings based load sharing," MS thesis. University of Illinois at Urbana Champaign, Illinois, 2010.

[9] D. J. Perreault and J. G. Kassakian, "Distributed interleaving of paralleled power converters," IEEE Trans. Circuits Syst. I, Fundamental Theory Appl., vol. 44, no. 8, pp. 728-734, Aug. 1997.

[10] S. Ozeri, D. Shmilovitz, S. Singer, and L. Martinez-Salamero, " The mathematical foundation of distributed interleaved system ," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 3, pp. 610-619, Mar. 2007.

[11] Kohama, T.; Ninomiya, T.; , "Automatic interleaving control for paralleled converter

system and its ripple estimation with simplified circuit model," *Power Electronics, 2007. ICPE '07. 7th International Conference on* , vol., no., pp.238-242, 22-26 Oct. 2007.
COMPEL '06. IEEE Workshops on , vol., no., pp.275-281, 16-19 July 2006.

[12] Miller, S.K.T.; Beechner, T.; Jian Sun; , "A Comprehensive Study of Harmonic Cancellation Effects in Interleaved Three-Phase VSCs," *Power Electronics Specialists Conference, 2007 PESC 2007. IEEE* , vol., no., pp.29-35, 17-21 June 2007.

[13] Beechner, T.; Jian Sun; , "Optimal interleaved pulse-width modulation considering Sampling effects," *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE* , vol., no., pp.1881-1887, 6-11 March 2011.

[14] Miller S.K.T, (2008). Analysis of three-phase rectifiers with AC-side switches and interleaved three-phase Voltage-Source Converters, Rensselaer Polytechnic Institute. Troy, New York, U.S.A.

[15] J. Holtz, W. Lotzkat and K-H Werner, "A high-power Multitransistor-inverter Un-interruptible power supply system," *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 278-285, July 1988.

[16] Z. Zhang, J. Kuang, X. Wang and B. T. Ooi, "Force commutated HVDC and SVC based on phase-shifted multi-converter modules," *Power Delivery, IEEE Transactions on Power Delivery, IEEE Transactions on*, vol.8, pp. 712-718, 1993.

[17] J. Thunes, R. Kerkman, D. Schlegel, and T. Rowan, "Current regulator instabilities on parallel voltage-source inverters," *IEEE Transactions on Industry Applications*, vol. 35, No. 1, pp. 70-77, Jan. 1999.

[18] Asiminoaei, L.; Aeloiza, E.; Kim, J.H.; Enjeti, P.; Blaabjerg, F.; Moran, L.T.; Sul, S.K.; , "Parallel Interleaved Inverters for Reactive Power and Harmonic Compensation," *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE* , vol., no., pp.1-7, 18-22 June 2006.

[19] Zulqarnain, Maira; Xu, David; Yuwen, Bo; , "Multi modular converters with automatic interleaving for synchronous generator based wind energy system," Power Electronics and Motion Control Conference (IPEMC), 2012 7th International, vol.3, no., pp.2255-2261, 2-5 June 2012.

[20] L. Feng and Q. Wenlong, "Implementation of an automatic interleaving approach for parallel dc/dc converter without interleaving bus," in Proc. IEEE Elect. Mach. Syst.

Conf., vol. 1, Nov. 2003, pp. 368- 371.

[21] Casablanca, C.; Jian Sun;, "Interleaving and Harmonic Cancellation Effects in Modular Three-Phase Voltage-Sourced Converters," *Computers in Power Electronics, 2006.*

[22] B.Wu, ELE806 Lab work and Lecture notes on "Wind Generators and Modeling ," Winter 2010.

[23] Jacek F. G., "Permanent Magnet Motor Technology- Design and Applications", Third Edition, CRC Press 2009.

[24] Jadric .I, (1998).Modelling and control of a synchronous generator with electronic load, MA. Sc. Thesis, Virginia Polytechnic Institute and State University, Blacksburg, VA, U.S.A.

[25] Krause P.C., Wasynczuk O., Sudhoff S. D., "Analysis of Electric Machinery and Drive Systems", 2nd Edition, IEEE Press, John Wiley and Sons, 2002.

[26] M.O. Mora . "Sensorless vector control of PMSG for wind turbine applications," MS thesis. Aalborg university, Aalborg, 2009.

[27] Zulqarnain, M.; Xu, D.; Bo Yuwen; , "Synchronous generator based wind energy conversion system (WECS) using multi-modular converters with autonomous controllers," Electric Machines & Drives Conference (IEMDC), 2011 IEEE International , vol., no., pp.819-824, 15-18 May 2011.

[28] S. Li, T.A. Haskew and Ling Xu, "Conventional and novel control designs for direct driven PMSG wind turbines, " *Electric Power Systems Research* 80 (March (3)) (2010), pp. 328-338.

[29] G. Michalke, A.D. Hansen, T. Hartkopf, "Control strategy of a variable speed wind Turbine with multipole permanent magnet synchronous generator, ", in: 2007European Wind Energy Conference and Exhibition, Milan (IT), 7–10 May, 2007.

[30] D. Mehrzad et. al. "Vector Control of PMSG for grid-connected wind turbine Applications," MS thesis. Aalborg university, Aalborg,2009.

[31] Keyuan Huang; Shoudao Huang; Feng She; Baimin Luo; Luoqiang Cai; "A control strategy for direct-drive permanent-magnet wind-power generator using back-to-back PWM converter," *Electrical Machines and Systems, 2008. ICEMS 2008. International Conference on* , vol., no., pp.2283-2288, 17-20 Oct. 2008.

[32] X. Zhang, Z. Huang, "A novel distributed interleaving scheme to achieve scalable phase

design for microprocessor power management," in Proc. IEEE Power Electron. Spec. Conf., June 2006, pp. 1-7.

[33] Robbins, William P. Mohan. "Power Electronics: Converters, Applications and Design". 2nd ed. New York: John Wiley & Sons, 1995.

[34] B.P. Lathi, "Modern Digital and Analog Communication Systems", 3rd ed. New York: Oxford University Press, 1998.

[35] eZdsp TM F2812 Technical Reference 506265-0001 Rev. F.

[36] TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812, Digital Signal Processors Data Manual, Literature Number: SPRS174S April 2001–Revised March 2011.

[37] VisSim/Embedded Controls Developer User's Guide Version 8.0, Visual Solutions, Inc. Copyright © 2010 Visual Solutions, Inc.

[38] DSP-Based Electromechanical Motion Control, Steven Campbell and Hamid A . Toliyat, CRC Press 2003, Print ISBN: 978-0-8493-1918-1, eBook ISBN: 978-0-203-48633-7.

[39] Hongliang W.,; Xuejun P.,; Yu C., ; Yong K., ; Xiumei Y., ; "An adaptive dead-time compensation method for sinusoidal PWM-controlled voltage source inverter with output LC filter," *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE* , vol., no., pp.778-785, 6-11 March 2011.

[40] Zhang Jin; Fang Lin Luo; , "An accurate approach of dead-time compensation for three-phase DC/AC inverter," *Industrial Electronics and Applications, 2009. ICIEA 2009. 4th IEEE Conference on* , vol., no., pp.2929-2934, 25-27 May 2009.

[41] VisSim User's Guide Version 8.0, Visual Solutions, Inc. VisSim User's Guide Version 8.0.