## Ryerson University Digital Commons @ Ryerson

Theses and dissertations

1-1-2012

# A Novel Hybrid Active Anti-Islanding Method For Multi-Converter Fed Distributed Generation Systems

Sasan Mostafaei *Ryerson University* 

Follow this and additional works at: http://digitalcommons.ryerson.ca/dissertations Part of the <u>Electrical and Computer Engineering Commons</u>

#### **Recommended** Citation

Mostafaei, Sasan, "A Novel Hybrid Active Anti-Islanding Method For Multi-Converter Fed Distributed Generation Systems" (2012). *Theses and dissertations*. Paper 1422.

This Thesis is brought to you for free and open access by Digital Commons @ Ryerson. It has been accepted for inclusion in Theses and dissertations by an authorized administrator of Digital Commons @ Ryerson. For more information, please contact bcameron@ryerson.ca.

## A NOVEL HYBRID ACTIVE ANTI-ISLANDING METHOD FOR MULTI-CONVERTER FED DISTRIBUTED GENERATION SYSTEMS

by

## SASAN MOSTAFAEI

Bachelor of Science, Electrical Engineering, Isfahan University of Technology, IRAN, 1995

A thesis

presented to Ryerson University in partial fulfillment of the requirements for the degree of Master of Applied Science in the Program of Electrical and Computer Engineering

> Toronto, Ontario, Canada, 2012 © Sasan Mostafaei, 2012

## **AUTHOR'S DECLARATION**

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I authorize Ryerson University to lend this thesis to other institutions or individuals for the purpose of scholarly research.

I further authorize Ryerson University to reproduce this thesis by photocopying or by other means, in total or in part, at the request of other institutions or individuals for the purpose of scholarly research.

I understand that my thesis may be made electronically available to the public.

## **BORROWER'S PAGE**

Ryerson University requires the signatures of all persons using or photocopying this thesis. Please sign below, and give address and date.

Name	Address	Date	Signature

### ABSTRACT

#### A Novel Hybrid Active Anti-Islanding Method For Multi-Converter Fed Distributed Generation Systems

© Sasan Mostafaei, 2012 Master of Applied Science in the program of Electrical and Computer Engineering Ryerson University

This thesis presents a novel active anti-islanding detection scheme for the three phase gridconnected converters. The proposed hybrid method works based on the combination of Positive Feedback Frequency Shift (PFFS) and Reactive Power Variation (RPV) methods, and therefore it combines the features of both methods. Unlike the RPV scheme, this method is capable of synchronizing all power converters with each other in a distributed generation (DG) system. Therefore, it can effectively detect islanding when the DG system has multiple renewable energy sources interfaced to the system by multiple converters.

The proposed method can also be combined with other active methods, such as the active frequency drift method. This minimizes the power quality degradation since the scheme is called upon only when 0.1Hz deviation in the grid frequency is detected. Moreover, unlike other positive feedback methods, this scheme has little impact on the stability of the DG system, since the positive feedback reference is only limited to  $\pm 0.5\%$  of the converter generated power. The performance of the proposed method is verified by simulation and experiments.

#### ACKNOWLEDGMENTS

First and foremost, I offer my sincerest gratitude to my supervisor, Dr. Bin Wu, who has supported me throughout my thesis with his patience and knowledge. His personality will be a source of inspiration to me for the rest of my life. I would also like to express my deepest gratitude to my co-supervisor, Dr. Soosan Beheshti, for her valuable suggestions and help during the last two years.

I am grateful to Dr. Amir Nasr Yazdani for his guidance and support. I am also indebted to Mr. Venkata Yaramasu for sharing his knowledge in the experimental procedures of my thesis.

Finally, this thesis is dedicated to my family members, especially my wife, Parastoo, for supporting and encouraging me to pursue this degree.

## **TABLE OF CONTENTS**

ABSTRARCT iv
ACKNOWLEDGMENTSv
TABLE OF CONTENTSvi
LIST OF FIGURESx
LIST OF TABLESxiii
NOMENCLATURExiv
CHAPTER 1 Introduction
1.1 Power quality1
1.2 Islanding
1.3 Islanding detection methods4
1.4 Motivation
1.5 Organization of thesis
CHAPTER 2 Control and Design of the Grid-connected Converters
2.1 Grid-connected Converters
2.2 Grid requirements
2.2.1 Grid frequency9
2.2.2 Grid voltage
2.2.3 DC current injection10
2.2.4 Current harmonic11
2.2.5 Islanding11
2.3 Voltage source inverter
2.4 PWM modulator
2.4.1 Harmonic spectrum of SPWM14
2.4.2 Selection of switching frequency15
2.5 Grid filter
2.5.1 L-Filters
2.5.2 LCL-Filters
2.5.3 Sizing of LCL filters
2.6 Current controller

2.6.1 Tuning of PI controllers	26
2.6.2 Phased locked loop (PLL)	
2.7 Case study	30
2.7.1 Sizing of LCL filter	30
2.7.2 PI tuning of the voltage-oriented controller (VOC)	32
2.7.3 PI tuning of the phase locked Loop (PLL)	32
2.7.4 Simulation	33
2.8 Summary	34
CHAPTER 3 Islanding Detection Methods for the Grid-connected Converters	
3.1 Islanding	
3.2 Anti-islanding requirements in IEEE Std. 1547	
3.3 Non-detection zone (NDZ)	41
3.4 Anti-islanding (AI) detection methods	42
3.5 Passive anti-islanding detection methods	44
3.5.1 Over/under voltage/frequency Detection (OUF-OUV)	44
3.5.2 Phase jump detection (PJD)	46
3.5.3 Harmonic detection method (HD)	46
3.5.4 Summary of the passive methods	47
3.6 Active anti-islanding detection methods	47
3.6.1 Frequency drift methods	
3.6.2 Voltage drift methods	57
3.6.3 Impedance estimation (IE)	59
3.6.4 Negative sequence detection	62
3.6.5 PLL based methods	63
3.7 External impedance insertion (EII)	63
3.8 Grid-resident anti-islanding detection methods	64
3.8.1 Power line carrier communication (PLCC)	64
3.8.2 Supervisory control and data acquisition (SCADA)	65
3.9 Comparison of anti-islanding detection methods	65
3.10 Summary	65
CHAPTER 4 Novel Anti-Islanding Method for Multiple-Converters Applications	

4.1	Problem statement	68
4.2	Novel anti-islanding method	72
	4.2.1 Positive feedback frequency shift scheme (PFFS)	73
	4.2.2 Positive feedback gain	74
	4.2.3 Low pass filter	76
	4.2.4 Finite impulse filter (FIR)	76
	4.2.5 Pre-detection time $(T_0)$	77
	4.2.6 RPV method	79
4.3	Computer simulation	80
	4.3.1 Simulation model	82
4.4	Simulation result	83
	4.4.1 Islanding with zero mismatch in active and reactive power	83
	4.4.2 Positive feedback frequency shift (PFFS) scheme	86
	4.4.3 Performance of anti-islanding scheme when $Q_f = 1$	89
	4.4.4 Performance of anti-islanding scheme when $Q_f = 2.5$	90
	4.4.5 Performance of anti-islanding scheme when $P_{GCC} = 50\%$	91
	4.4.6 Performance of anti-islanding scheme with three converters paralleled	91
4.5	Anti-islanding scheme performance comparison	92
	4.5.1 Reliability	93
	4.5.2 Maintaining power quality	93
	4.5.3 Multiple-converters application	93
4.6	Summary	94
CHAI	PTER 5 Experimental Verification	95
5.1	Hardware implementation	95
5.2	Software implementation	96
5.3	Experimental results	97
	5.3.1 Converter connected to the grid	99
	5.3.2 Islanding with zero mismatch in active and reactive power	100
	5.3.3 Positive feedback frequency shift (PFFS) scheme	102
	5.3.4 Performance of anti-islanding scheme when $Q_f = 1$	103

5.4 Summary	105
CHAPTER 6 Conclusion	107
REFERENCES	110

## LIST OF FIGURES

Fig. 1.1	Grid-connected converter for photovoltaic system	2
Fig. 1.2	Islanding formation in the DG system	3
Fig. 1.3	Islanding detection methods	4
Fig. 2.1	Structure of the grid-connected converter	10
Fig. 2.2	Simplified two-level voltage source inverter VSI)	12
Fig. 2.3	Sinusoidal pulse width modulation (SPWM)	14
Fig. 2.4	Harmonic content of v <sub>ab</sub>	15
Fig. 2.5	Grid filters	17
Fig. 2.6	Transfer functions of L and LCL filters	18
Fig. 2.7	Block diagram of voltage oriented control (VOC)	23
Fig. 2.8	Grid angle in VOC scheme	25
Fig. 2.9	The Current loop of PI	26
Fig. 2.10	PLL based on synchronous reference frame (SRF)	29
Fig. 2.11	Block diagram of the grid-connected converter discussed in the case study	32
Fig. 2.12	The grid-connected converter operating at nominal power	35
Fig. 2.13	Harmonic spectrum of the converter's current	36
Fig. 2.14	VOC response to the step change of the converter's active power reference	36
Fig. 2.15	PLL response to the step change of the grid frequency	37
Fig. 3.1	Unintentional islanding test configuration, source IEEE Std. 1547	40
Fig. 3.2	Interconnection of grid-connected converter	43
Fig. 3.3	Non-Detection zone (NDZ)	43
Fig. 3.4	Anti-islanding methods	45
Fig. 3.5	GEFS method	49
Fig. 3.6	AFD method	51
Fig. 3.7	Modifying grid angles in PLL for AFD method	51
Fig. 3.8	AFD implementation	51
Fig. 3.9	THD versus chopping factor	54
Fig. 3.10	Chopping factor in AFDPCF	54
Fig. 3.11	Phase versus frequency in SMS	56

Fig. 3.12	RPV method	57
Fig. 3.13	GEVS method	59
Fig. 3.14	Changing active and reactive power for measuring grid impedance	62
Fig. 3.15	Measuring of grid impedance with two working points	62
Fig. 3.16	External impedance insertions	63
Fig. 3.17	Power line carrier communications to detect islanding	63
Fig. 4.1	PLL based on synchronous reference frame (SRF)	69
Fig. 4.2	Variation of frequency after islanding	72
Fig. 4.3	The proposed active AI scheme	75
Fig. 4.4	Variation of frequency with positive feedback	78
Fig. 4.5	Analytical approach to estimate the pre-detection time	79
Fig. 4.6	The proposed active scheme combined with RPV	80
Fig. 4.7	One cycle reactive power injection pattern	81
Fig. 4.8	Detection time in the proposed AI scheme	81
Fig. 4.9	Circuit diagram of AI test-setup	84
Fig. 4.10	Circuit diagram of AI test-setup for three converters	85
Fig. 4.11	The islanding with zero mismatches in active and reactive power	87
Fig. 4.12	Converter output voltage dq components	88
Fig. 4.13	Positive feedback frequency shift (PFFS) scheme to pre-detect islanding	88
Fig. 4.14	Reactive power references when PFFS scheme is enabled	89
Fig. 4.15	Detection of islanding when $Q_f = 1$	89
Fig. 4.16	Detection of islanding when $Q_f = 2.5$	90
Fig. 4.17	Detection of islanding when $P_{GCC} = 50\%$	91
Fig. 4.18	Positive feedback frequency shift (PFFS) scheme for three converters paralleled	92
Fig. 5.1	Prototype of AI test-setup based on dSPACE	96
Fig. 5.2	the grid-connected converter operating at nominal power	99
Fig. 5.3	VOC response to the step change of active power reference	100
Fig. 5.4	Converter output set at 100% of its nominal value	100
Fig. 5.5	Converter output set at 50% of its nominal value	101
Fig. 5.6	PLL response during start-up	101
Fig. 5.7	The islanding with zero mismatches in active and reactive power	.102

Fig. 5.8	PFFS scheme to pre-detect islanding	103
Fig. 5.9	Reactive power supplied by converter	103
Fig. 5.10	Detection of islanding when $Q_f = 1$ (over frequency)	104
Fig. 5.11	Detection of islanding when $Q_f = 1$ (under frequency)	104

## LIST OF TABLES

Table 2.1	Interconnection system response to abnormal voltages	11
Table 2.2	Maximum current harmonics specified by IEEE Std. 1547	12
Table 2.3	System specification of the grid-connected converter Estimated	30
Table 2.4	Simulation system specification of the grid-connected converter	34
Table 3.1	Performance comparison for AI methods	67
Table 4.1	Simulation system specification of the grid, transformer and the load	85
Table 4.2	Simulation system specification of the grid-connected converter	86
Table 5.1	Experimental system specification of the grid, transformer and the load	97
Table 5.2	Experimental system specification of the grid-connected converter	98

## NOMENCLATURE

i	Current
v	Voltage
f	Frequency
ω	Angular frequency
R	Load resistance of load
L	Load inductance
С	Load capacitance
h	Harmonic order
THD	Total harmonic distortion
$C_{dc}$	DC-link capacitor
I <sub>dc</sub>	DC-link current
V <sub>dc</sub>	DC-link current
$f_{SW}$	Switching frequency
$f_{cr}$	Carrier frequency
$f_m$	Modulation frequency
$m_f$	Frequency modulation index
m <sub>a</sub>	Amplitude modulation index
$\hat{V}_{cr}$	Peak of carrier wave
$\hat{V}_m$	Peak of modulation wave
vg	Converter output voltage
i <sub>g</sub>	Converter output current
Pref	Converter active power reference
$Q_{ref}$	Converter reactive power reference
$P_{GCC}$	Active power supplied by grid-connected converter
$Q_{GCC}$	Reactive power supplied by grid-connected converter

S	Laplace operator
$L_g$	Grid-side inductor
L <sub>i</sub>	Inverter-side inductor
$C_f$	Filter Capacitor
$R_d$	Damping resistor
f <sub>res</sub>	Resonance frequency
L <sub>grid</sub>	Imaginary part of grid impedance
R <sub>grid</sub>	Real part of grid impedance
$Z_b$	Base impedance of converter
V <sub>n</sub>	Nominal voltage of converter
I <sub>n</sub>	Nominal current of converter
$f_n$	Nominal frequency of converter
$P_n$	Nominal power of converter
i <sub>i</sub>	Inverter current
$P_g^*$	Active power reference set by operator
$Q_g^*$	Reactive power reference set by operator
v <sub>dg</sub>	d component of converter output voltage
v <sub>qg</sub>	q component of converter output voltage
i <sub>qg</sub>	q component of converter output current
i <sub>dg</sub>	d component of converter output current
$i_{qg}^*$	Set-point of $i_{qg}$
$i_{dg}^*$	Set-point of <i>i</i> <sub>dg</sub>
v <sub>qi</sub>	q component of inverter output voltage
v <sub>di</sub>	d component of inverter output voltage

k <sub>iVOC</sub>	Integral gain of PI controllers utilized in VOC
k <sub>pVOC</sub>	Proportional gain of PI controllers utilized in VOC
$\omega_g$	Grid angular frequency
$G_d(s)$	Transfer function delay caused by digital signal processor
$G_f(s)$	Transfer function of the LCL-filter
$G_{PI}(s)$	Transfer function of the PI controller
$T_i$	Time constant of integrator
$T_s$	Sampling time of digital signal processor
$T_{fi}$	Delay caused by utilizing low pass digital filters
$R_g$	Resistance of the grid filter
$T_p$	Time constant of grid filter
k <sub>pPLL</sub>	Proportional gain of PI controllers utilized in PLL
T <sub>iPLL</sub>	Integral gain of PI controllers utilized in PLL
t <sub>s</sub>	Settling time of PLL
$Q_f$	Quality factor
Pload	Active power consumed by load
$\Delta P$	Active power mismatch
$Q_{load}$	Reactive power consumed by load
$\Delta Q$	Reactive power mismatch
$V'_g$	Converter output voltage after islanding
f'	Converter frequency after islanding
$f_{\max}$	Maximum allowable operating frequency for converter
$f_{\min}$	Minimum allowable operating frequency for converter
V <sub>max</sub>	Maximum allowable operating voltage for converter
V <sub>min</sub>	Minimum allowable operating voltage for converter

$\theta_{thershold}$	Threshold phase angle
$c_f$	Chopping factor
Î	Peak of current
$f_k$	Measured frequency at $k^{th}$ sample
$c_{f(k)}$	Calculated chopping factor at $k^{th}$ sample
$\theta_{load}$	Phase angle of load
$\omega[n]$	Measured angular frequency at $n^{th}$ sample
$i_{f1}$	Injected current at frequency of <i>f1</i>
$Z_{f1}$	Impedance measured at frequency of <i>fl</i>
$\omega'$	Converter angular frequency after islanding
$K_{pf}$	Positive feedback gain
$T_0$	Islanding pre-detection time
<i>T</i> <sub>3</sub>	Islanding detection time
ff	Feed-forward

# Chapter One Introduction

In the last few years, Distributed Generation (DG) based on Renewable Energy Sources (RES) has experienced over 30% growth per year [1]. The large centralized power plants have excellent economies of scale. However the size of investment, environmental impacts and long distance transmission lines are problematic, whereas in the Distributed Generation (DG), the total investment can be spread over many owners. The security of the supply may be improved and the environmental impacts are reduced. Obviously the shift from large centralized production units connected at high voltage levels at network to small decentralized units connected at lower voltage levels will have some barriers to overcome. These barriers include economic, technical, and regulatory issues [2]. Among them, *power quality* and *islanding* are the two most important technical issues in the DG systems.

## 1.1 Power quality

Power quality issues are becoming more pronounced as the renewable distributed generation systems utilize power electronic converters [3]. Grid-connected converters are utilized as the main interface between energy sources (such as photovoltaic or wind generation units) and the grid. These converters should be able to control active and reactive power, to operate within a wide range of voltage and frequency, to support voltage ride-through capability, to inject reactive current during faults, and to support the grid code requirements [1]. A typical grid-connected converter for the photovoltaic (PV) system is illustrated in Figure 1.1, where solar PV modules

are connected in a series–parallel configuration to match the required DC link voltage. A single stage DC/AC inverter is utilized to control power flow from the PV system to the grid and the harmonic filter is employed to reduce current distortion. If the harmonics generated by the converter are not filtered properly, they could cause operating problems and possible malfunction of the connecting loads and therefore are limited to 5% by IEEE Std 1547 [3].



Figure 1.1 Grid-connected converter for photovoltaic system

## **1.2 Islanding**

A simplified distribution system is shown in Figure 1.2 where the substation transformers step down the transmission line voltage (400 kV) to the primary distribution voltage level (13.8 kV). One of the feeders is connected to the secondary distribution feeder (0.6 kV) through a utility transformer. Two distributed generators (DG1 and DG2) are directly connected to the secondary feeders. As can be seen, when circuit breaker CB1 opens, DG1 and DG2 continue to feed the local loads existing marked as island area in Figure 1.2.

In IEEE Std. 1547-2008, an island is defined as "a condition in which a portion of an area of the electric power system is energized solely by one or more local electric power systems

through the associated PCCs (Point of Common Coupling) while that portion of the area of the electric power system is electrically separated from the rest."[4].



Figure 1.2 Islanding formation in the DG system

Islanding can pose a risk to utility workers as it leaves a line to remain energized when it is considered disconnected. The voltage and frequency of the islanded grid might shift considerably from rated values which can bring about damage to customer equipment. Closing the upstream breakers again during islanding can also cause major damage to converters due to their unsynchronized reconnection to the grid. Therefore, islanding is a hazard to people and customers' equipment and to the grid-connected converters themselves [5]. The converter can detect islanding and cease to inject current within two seconds of formation of the island as mandated by IEEE Std. 1547 [4].



Figure 1.3 Islanding detection methods

## **1.3 Islanding detection methods**

Islanding detection methods as shown in Figure 1-3 can be classified into three categories [1]:

- 1- Converter-resident methods can be divided further into passive and active methods. Passive methods are based on monitoring and detection of any abnormality in the parameters of voltage at the point of PCC caused by disconnection from the grid. Active methods deliberately generate a disturbance in the PCC and then monitor the response to detect whether the utility is disconnected.
- 2- *External impedance insertion* can be implemented by connecting low value impedance, usually via a capacitor bank at the utility side of PCC when the grid is disconnected,

which creates a step change in the phase between current and the voltage of the converter at PCC.

3- *Grid-resident methods* require means of communication between the grid and converter such as the *PLCC* (power line carrier communication) or *SCADA* (supervisory control and data acquisition).

## **1.4 Motivation**

Motivation for this research is to propose a new active anti-islanding method with no impact on power quality, and the stability of the network which can be utilized when multiple converters are connected to the PCC.

The proposed method has the following features:

- Many of the active AI methods degrade power quality, since they continuously inject disturbance into the network. In the proposed method, the active process to detect islanding is triggered only when it is called upon. Therefore this method will not affect the power factor (PF), total harmonic distortion (THD) or the stability of the network. As a result, this method exhibits superior performance in terms of maintaining power quality when compared to other AI methods.
- Many of the active AI methods could fail when multiple converters are connected to the grid. This happens because the disturbance injected by one converter can cancel the other one due to lack of synchronization between them. The proposed scheme

introduces a unique method to synchronize converters together. Therefore, it can be combined with other active methods when multiple converters are paralleled to the grid.

### **1.5 Organization of Thesis**

The contents of this thesis are divided into six chapters. Chapter 1 is an introduction to the research. Chapter 2 describes the structuring blocks of a grid-connected converter. The grid requirements mandated by IEEE Std. 1547 are then introduced. A step-by-step design procedure for sizing of harmonic filter, selection of switching frequency and tuning of PI controllers in the Voltage Oriented Control (VOC) scheme and the phase locked loop (PLL) are presented. A Case study with simulation is given to verify the design guidelines.

Chapter 3 details about islanding formation, and its potential hazards. Various proposed antiislanding detection methods and the criteria for their evaluation are then discussed.

Chapter 4 presents the main contribution of this thesis: a novel hybrid active anti-islanding method based on combining the Positive Feedback Frequency Shift (PFFS) and Reactive Power Variation (RPV). The intent of the research is to develop a robust active AI method with no impact on power quality or stability of the network that can be utilized in multi-converter applications. This unique method can also be combined with other active methods to reduce the power quality degradation. The performance of the proposed method is then verified in single and multiple-converter applications by simulation in Simulink/Matlab.

Chapter 5 presents the experimental verification of the proposed anti-islanding detection method for the three-phase grid-connected converter. A prototype of the low-power grid-connected converter is built based on the dSPACE prototyping system.

And finally, Chapter 6 draws conclusions based on the research for this thesis.

## **Chapter Two**

## **Control and Design of Grid-connected Converters**

Grid-connected converters are the key element in renewable energy integration. They can be envisioned as electronic power interfaces between energy sources (such as fuel cell, photovoltaic or wind generation units) and the grid. They should be able to control active and reactive power, to operate within a wide range of voltage and frequencies, to support voltage ride-through capability, to inject reactive current during faults, and to detect islanding and support the grid code requirements [1].

In this chapter the block diagram of a grid-connected converter is presented. Based on the grid requirements given by relevant standards, a step-by-step design procedure for a grid-connected converter is discussed. The designed converter is later simulated in Chapter 5 and implemented in Chapter 6.

## 2.1 Grid-connected converters

The block diagram for a grid-connected converter is illustrated in Figure 2.1, where the photovoltaic or wind system is replaced by a DC power supply  $(V_{dc})$ . The current controller is based on the setting given for active power  $(P_{ref})$  and reactive power  $(Q_{ref})$ . Measuring voltages  $(v_g)$  and currents  $(i_g)$  at the output terminal determines control signals for the pulse width modulator (PWM). Based on the switching pattern from the PWM modulator, the voltage source inverter (VSI) controls the power flow from the DC side to the grid. A harmonic filter is

utilized to remove high switching frequency distortion which is usually required by grid code. Phase locked loop (PLL) ensures that the frequency and phase of injected current is synchronized with respect to the grid voltage. Finally, the maximum power point tracking block (MPPT) continuously ensures that the maximum power is captured from the wind or PV system. Since most of the design criteria for the converter systems are dictated by the grid requirements, relevant international standards are introduced in the following section.

### 2.2 Grid requirements

The two main standards addressing the connection of converters to the grid are [1]:

- IEEE Std. 1547-2008: Standard for Interconnecting Distributed Resources with Electric Power Systems [1]; and
- IEC 61727 2004: Photovoltaic (PV) Systems Characteristics of the Utility Interface [6].

The IEEE Std. 1547 addresses all types of distributed resources (including grid-connected converters) up to 10MW and establishes mandatory regulations. It covers technical specifications islanding, design, commissioning, and testing of the interconnection. Requirements mandated by IEEE Std. 1547 for designing a grid-connected converter are investigated in the following sections.

#### 2.2.1 Grid frequency

The frequency of the grid is measured at the interconnection point of converter and grid,

either by phase locked loop (PLL) or zero crossing detectors (ZCD). When the measured frequency is out of the range (>60.5Hz or <59.3Hz), this will be considered an abnormal grid connection, and the converter must stop injecting current to the grid within 0.16sec.

#### 2.2.2 Grid voltage

As specified in Table 2.1, the converter must cease injecting current to the grid within a given clearing time when the grid voltage measured at the interconnection point is detected as being abnormal.



Figure 2.1 Structure of the grid-connected converter

#### 2.2.3 DC current injection

DC current injected by the converter shall be limited to 0.5% of the rated RMS current under

any operating conditions.

Voltage range	Clearing time
(% of base voltage)	(sec)
V < 50	0.16
50 < V < 88	2.00
110 < V < 120	1.00
V > 120	0.16

Table 2.1 Interconnection system response to abnormal voltage, IEEE Std. 1547[4]

#### 2.2.4 Current harmonics

Odd order harmonics in the injected current shall be limited, as specified in Table 2.2, to reduce adverse effects to other equipment connected to the grid [1]. Even order harmonics are limited to <sup>1</sup>/<sub>4</sub> of the odd harmonic limits given in the table [4].

### 2.2.5 Islanding

In IEEE Std. 1547, an island is defined as "a condition in which a portion of an area of the electric power system is energized solely by one or more local electric power systems while that portion of the area of the electric power system is electrically separated from the rest" [4]. The standard states that an island shall be detected, and the converter shall cease injecting current to the grid within 2 seconds after the formation of an island.

Odd						
Harmonic	<i>h</i> < 11	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$h \ge 35$	THD
order						
%	4.0	2.0	1.5	0.6	0.3	5.0

 Table 2.2 Maximum current harmonics specified by IEEE Std. 1547[4]

#### 2.3 Voltage source inverter

Central PV inverters are typically built in a three-phase two-level voltage source inverter configuration, as shown in Figure 2-2 [7]. This consists of six IGBTs,  $S_1 \sim S_6$ , with an antiparallel free-wheeling diode with each switch. Typical power ratings for the small-central and central inverters are 6 to 15kW and 100 to1000kW, respectively [1]. For the high power converter, a utility transformer is usually connected between the converter and the grid, as shown in Figure 2.1, to achieve galvanic isolation. Such isolation is often needed in order to ground the PV system properly, but in commercial small-central inverters a transformer-less approach is preferred.



Figure 2-2 Simplified two-level voltage source inverter (VSI)

#### 2.4 PWM modulator

Sinusoidal PWM (SPWM) and space vector modulation (SVM) are the most common PWM modulators utilized in the PV inverters. In this research, SPWM is employed and studied in this section. The sinusoidal PWM scheme for the two-level converter is shown in Figure 2.3 [6]. In this scheme, three-phase sinusoidal modulating signals ( $v_{ma}$ ,  $v_{mb}$  and  $v_{mc}$ ) are compared with a triangular carrier wave ( $v_{cr}$ ) to generate logical signals ( $v_{g1}$ ,  $v_{g2}$ ,  $v_{g3}$ ,  $v_{g4}$ ,  $v_{g5}$ ,  $v_{g6}$ ) that control the six switches ( $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$ ,  $S_5$ ,  $S_6$ ). Considering that  $\hat{V}_m$  and  $\hat{V}_{cr}$  are the peak values of the modulating and carrier waves respectively ,  $\hat{V}_{cr}$  is normally kept fixed and the control signal  $\hat{V}_m$  is varied; therefore voltage of the fundamental component in the inverter output terminal can be controlled by the amplitude modulation index which is defined by [6]:

$$m_a = \frac{\hat{V}_m}{\hat{V}_{cr}} \tag{2.1}$$

And line-to-line output voltage of fundamental component will be

$$V_{AB1} = 0.612m_a V_{dc}$$
 for all  $m_a \le 1$  (2.2)

In addition, the frequency of the fundamental component in the inverter output terminal can be controlled by keeping the frequency of carrier wave  $(f_{cr})$  constant as the frequency of control signal  $(f_m)$  is varied. The frequency modulation index is defined by:

$$m_f = \frac{f_{cr}}{f_m} \tag{2.3}$$

The carrier frequency determines the frequency of switching of each IGBT (in a two level converter); therefore, it is called "switching frequency."



Figure 2.3 Sinusoidal pulse width modulation (SPWM)

#### 2.4.1 Harmonic spectrum of SPWM

When the carrier wave is synchronized with the modulating wave, the modulation scheme is known as synchronous PWM. In contrast, switching frequency in the asynchronous PWM switching frequency is always fixed and  $m_f$  could be non-integer, and therefore may generate non-characteristic harmonics [6]. For  $m_f \ge 9$  with  $m_f$  in a multiple of 3, all the harmonics in  $v_{ab}$ with the order lower than  $(m_f - 2)$  are eliminated, and the harmonics are centered around  $m_f$  and its multiples, such as  $2m_f$  and  $3m_f$  [6]. The harmonic content of the voltage source inverter based on SPWM for line-to-line output voltage is given in Figure 2.4 [6].Another approach is using variable switching frequency and distributing harmonics throughout the frequency spectrum, since this helps to reduce acoustic noise. However it has not been commercialized yet due to the fact that it is more difficult to design the grid filter [1].

#### 2.4.2 Selection of switching frequency

By selecting higher switching frequency, the spectrum of harmonics is shifted to the higher frequency values, thereby requiring a smaller low pass. On the other hand, greater switching frequency means greater switching losses; therefore, there is a trade-off between selecting the size of filter and switching frequency. By looking at commercial products on the market, one can see that for a typical high power (500kW) grid-connected converter, the 5kHz switching frequency is typically selected, whereas for a 3kW converter, 17kHz is chosen [1].



Figure 2.4 Harmonic content of  $v_{ab}$ 

### 2.5 Grid filters

In order to filter out high frequency harmonics created by PWM and to meet the power quality requirement given in Table 2.2, a grid filter is employed. L and LCL filters are introduced in the following section.

#### 2.5.1 L-filters

The L-filter as illustrated in Figure 2.5(a) is a first order filter with an attenuation of 20dB/decade for the entire range of frequencies. Assuming the grid voltage is considered an ideal voltage source, the transfer function for L-filter can be derived by:

$$H(s) = \frac{i}{v} = \frac{1}{L_g s}$$
(2.5)

Therefore, to meet the requirement given in Table 2.2, either the switching frequency selected should be very high; for example more than 50kHz, which is not possible with IGBT or the inductor selected should be very large. Using a large inductor reduces the dynamics of the converter, and in addition will be bulky and expensive; thus L-filters are seldom used in grid-connected converters.

#### 2.5.2 LCL-filters

The LCL-filter, as shown in Figure 2.5(b), is a third order filter with an attenuation of 60dB/decade for any frequency above resonant frequency (Figure 2.6). Therefore a lower

switching frequency can be selected. Figure 2.6 depicts the transfer functions for L and LCL filters with the same amount of inductors. Assuming the grid voltage is considered an ideal voltage source, the transfer function for LCL-Filter can be derived by:

$$H(s) = \frac{i}{v} = \frac{1}{L_i L_g C_f s^3 + (L_i + L_g) s}$$
(2.6)

Therefore the resonant frequency will be[1]:

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_i + L_g}{L_i L_g C_f}}$$
(2.7)



Figure 2.5 Grid filters

To avoid resonance, either passive or active damping is employed. Passive damping utilizes a small resistor connected in series/parallel with capacitor or in series/parallel with the grid-side inductor. Passive damping decreases the overall system efficiency and also reduces the filter attenuation at switching frequency, but it is easy to implement. Active damping emulates the damping resistor by modifying the current controller, but it needs an extra current sensor and a more complex controller [1].



Figure 2.6 Transfer functions of L and LCL filters

#### 2.5.3 Sizing of LCL filter

Constraints for sizing of inductors and capacitors are summarized as follows:

- 1. Capacitor value  $(C_f)$  is typically selected at less than 5%, to limit reduction of the power factor [8].
- 2. Resonant frequency should be selected at a level between 10 times the grid frequency and half the switching frequency. The former is to avoid any resonance with existing harmonics in the network (for instance  $3^{rd}$ ,  $5^{th}$ ,  $7^{th}$  harmonics), and the latter is due to the fact that the filter should have enough attenuation in the switching frequency [8]. It is worth mentioning that grid impedance can be seen as part of  $L_g$ , and therefore with
change of grid impedance, resonance frequency can vary up to 40% [1]. The variation of resonance frequency when grid impedance varies can be derived as [1]:

$$\Delta \omega_{res} = \frac{1}{2\omega_{res}C_f} \left(\frac{1}{L_g + L_{grid1}} - \frac{1}{L_g + L_{grid2}}\right)$$
(2.8)

From Equation 2.8, it can be seen that when a higher filter capacitor is chosen, less variation in resonance frequency will occur [1]. Another important factor is that in the LC-filter (without the grid-side inductor) variation of resonance frequency will be considerable and, in fact, this is the main reason that LC-Filters are not employed in practical situations.

- 3. The LCL filter is part of the packaging in low power inverters, so they must be as small as possible. Therefore when employing high switching frequency, small inductors are selected (less than 5%) [1]. In contrast, the main issue with sizing of LCL-filter in high power inverter is the saturation of the inductor [1]. At the same time, switching frequency should be lower (due to losses); therefore a higher value of inductor is employed (typically around 20%, including leakage inductance of the utility transformer).
- 4. The inverter-side inductor is sized to limit the ripple in the inverter currents, and the core should also be designed to carefully avoid any saturation. The grid-side inductor is sized based on harmonic requirements. Therefore, the design approach in the inverter-side inductor is a time-domain analysis, while the grid-side inductor is designed with a frequency-domain approach [1].
- 5. The damping resistor (*Rd*) is usually selected at one-third of the capacitor's impedance at the resonant frequency [8].

6. The position of current and voltage sensors can have an effect on the sizing of the capacitor and inductors. If the voltage and current sensors are placed as shown in Figure 2.1, then the optimum value for the capacitor to minimize absorbed reactive power and therefore not to over-rate the inverter will be [8]:

$$C_f = \frac{L_i - L_g}{Z_h^2} \tag{2.9}$$

where  $Z_b$  is the base impedance of the inverter.

Assuming that the desired harmonic attenuation factor in the inverter-side inductor for the first harmonic, i.e.,  $(m_f - 2)$ , is named  $\alpha$ , and the desired harmonic attenuation factor in the grid-side inductor for the first appeared harmonic is called  $\beta$ :

$$\alpha.\beta. \le 0.003 \tag{2.10}$$

By looking into Figure 2.4:

$$\frac{V_{ab(mf-2)}}{Vdc} = 0.195$$
(2.11)

Therefore with substituting of Equation 2.2:

$$L_{i} \geq \frac{V_{ab(mf-2)}}{\sqrt{3}(m_{f}-2)(2\pi f) \times I_{n} * \alpha} \approx \frac{\frac{0.195}{0.612}V_{n}}{\sqrt{3 \times 2\pi \times f_{sw}I_{n}\alpha}}$$
(2.12)

where  $V_n$  and  $I_n$  are nominal voltage and current of the converter respectively. Selection of  $\alpha$  in Equation 2.12 depends on the saturation level of the inverter-side inductor and the effects on the design of its core.

From [8]:

$$\beta = \left| \frac{i_g(f_{sw})}{i_i(f_{sw})} \right| \approx \frac{1}{\sqrt{\left( (2\pi \times f_{sw})^2 L_g C_f - 1 \right)^2}}$$
(2.13)

where  $i_g$  and  $i_i$  are the inverter and the grid currents respectively.

Therefore,

$$L_{g} = \frac{1 + \sqrt{\frac{1}{\beta^{2}}}}{(2\pi \times f_{sw})^{2} C_{f}}$$
(2.14)

Knowing  $L_i, L_g$  and  $C_f$ , resonant frequency shall be calculated to verify whether the second constraint is fulfilled. Otherwise the calculations should be repeated with the new values for  $\alpha$  and  $\beta$ .

## 2.6 Current controller

The grid-connected converter with PWM modulator can be controlled by various current control schemes, such as resonant control, predicative control, and voltage oriented control [1]. In this research, voltage oriented control (VOC) is introduced, and design guidelines are discussed. The objective of the controller is to adjust the injected current (phase and amplitude) by adjusting the modulation index to achieve references given for active and reactive power; moreover, the injected current should meet the harmonic requirements given in Table 2.2.

Before going into detail about VOC, it should be noted that, as already shown in Figure 2.6, the frequency characteristic of the LCL-filter in the frequencies smaller than the resonant

frequency are similar to L-filter (considering the same amount of inductor is utilized in both filters). Therefore the LCL-Filter can be replaced by the L-filter in the steady state condition.

The principal of the VOC scheme is illustrated in Figure 2.7. The first step in implementation of VOC is detection of grid angle  $\theta_{g}$ , as illustrated in Figure 2.8(b) [9]. The grid angle is required to transform all three phase voltages and currents from *abc* stationary frame to *dq* synchronous frame and also to transform voltages in *dq* synchronous frame back to the *abc* stationary frame. This angle, in fact, is utilized for synchronizing the converter to the grid and is measured by the PLL which will be covered in detail in the next section.

In the second step, as illustrated in Figure 2.8(a), the *d*-axis of the synchronous frame is aligned with the grid voltage vector; therefore, the *q*-axis voltage will be equal to zero and the *d*-axis voltage will be equal to the grid voltage magnitude. Three-phase currents set of converters also can be transformed as:

$$\begin{bmatrix} i_{dg} \\ i_{qg} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta_g) & \cos(\theta_g - 2\pi/3) & \cos(\theta_g - 4\pi/3) \\ -\sin(\theta_g) & -\sin(\theta_g - 2\pi/3) & -\sin(\theta_g - 4\pi/3) \end{bmatrix} \begin{bmatrix} i_{ag} \\ i_bg \\ i_{cg} \end{bmatrix}$$
(2.15)

In the third step, reference for reactive  $(Q_g^*)$  and active power  $(P_g^*)$  which are going to be transferred is determined. In a low power converter, the reactive power's reference is usually set to zero, but in the wind converter and high power PV converter it might be set differently.

$$Q_g^* = \frac{3}{2} (v_{qg} i_{dg} - v_{dg} i_{qg})$$
(2.16)

As  $v_{qg}$  is set to zero intentionally (*d*-axis is aligned with grid voltage vector), therefore the *q*-axis current reference  $i_{qg}^*$  can then be obtained by:

$$i_{qg}^{*} = \frac{Q_{g}^{*}}{-1.5v_{dg}}$$
(2.17)



Figure 2.7 Block diagram of voltage oriented control (VOC)

On the other side, the Maximum Power Point Tracking controller (MPPT) continuously ensures that maximum power is transferred to the grid as the solar irradiation or wind speed vary all the time. The MPPT controller, as shown in Figure 2.7, monitors the DC-Link current and voltage; by regulating either of them it tracks the maximum power point (MPP). The reference for active power is,

$$P_g^* = \frac{3}{2} (v_{dg} i_{dg} - v_{qg} i_{qg}) = \frac{3}{2} v_{dg} i_{dg} = V_{dc} I_{dc}$$
(2.18)

Therefore the *d*-axis current reference  $i_{dg}^*$  can then be obtained by:

$$i_{dg}^{*} = \frac{P_{g}^{*}}{1.5v_{dg}} = \frac{V_{dc}I_{dc}}{1.5v_{dg}}$$
(2.19)

Therefore as already shown, "the three-phase line currents in the *abc* stationary frame  $i_{ag}$ ,  $i_{bg}$  and  $i_{cg}$  are transformed to the two-phase currents  $i_{dg}$  and  $i_{qg}$  in the *dq* synchronous frame, which are the active and reactive components of the three-phase line currents, respectively. The independent control of these two components provides an effective means for the independent control of system active and reactive power" [9]. To build three phase modulating signals from  $i_{dg}$  and  $i_{qg}$ , KVL equations for the grid-side circuit of the inverter in the *abc* stationary reference frame can be written as [9]:

$$\frac{di_{ag}}{dt} = \left(v_{ag} - v_{ai}\right)/L_g$$

$$\frac{di_{bg}}{dt} = \left(v_{bg} - v_{bi}\right)/L_g$$

$$\frac{di_{cg}}{dt} = \left(v_{cg} - v_{ci}\right)/L_g$$
(2.20)

The above equations can then be transformed into the dq synchronous reference frame:

$$\begin{cases}
\frac{di_{dg}}{dt} = \left(v_{dg} - v_{di} + \omega_g L_g i_{qg}\right) / L_g \\
\frac{di_{qg}}{dt} = \left(v_{qg} - v_{qi} - \omega_g L_g i_{dg}\right) / L_g
\end{cases}$$
(2.21)

where  $\omega_g$  is the speed of the synchronous reference frame, designed to achieve better dynamic performance; the current in *d*-axis and the *q*-axis current shall be de-coupled.



Figure 2.8 Grid angle in VOC scheme

$$\begin{cases} v_{di} = -\left(k_{pVOC} + k_{iVOC} / S\right)\left(i_{dg}^{*} - i_{dg}\right) + \omega_{g}L_{g}i_{qg} + v_{dg} \\ v_{qi} = -\left(k_{pVOC} + k_{iVOC} / S\right)\left(i_{qg}^{*} - i_{qg}\right) - \omega_{g}L_{g}i_{dg} + v_{qg} \end{cases}$$

$$(2.22)$$

where  $k_{pVOC}$  and  $k_{iVOC}$  are proportional and integral constants of PI controllers. Therefore:

$$\begin{cases} \frac{di_{dg}}{dt} = \left(k_{pVOC} + k_{iVOC} / S\right) \left(i_{dg}^* - i_{dg}\right) / L_g \\ \frac{di_{qg}}{dt} = \left(k_{pVOC} + k_{iVOC} / S\right) \left(i_{qg}^* - i_{qg}\right) / L_g \end{cases}$$

$$(2.23)$$

The above equation indicates that the current in the *d*-axis current and *q*-axis become de-coupled, and the current controller can be implemented as shown in Figure 2.7 [9].

### 2.6.1 Tuning of PI controllers

The current loop of the PI controller is shown in Figure 2.9, where  $G_{PI}(s)$  is PI controller,  $G_d(s)$  is the delay due to elaboration of the computation device, and to the PWM, and  $G_f(s)$  is the transfer function of the LCL-filter [1].



Figure 2.9 The current loop of PI controller

$$G_{PI}(s) = k_{pVOC} + k_{iVOC} / s = k_{pVOC} (1 + \frac{1}{T_i s})$$
(2.24)

 $T_i$  is the time constant of integrator in the PI controller. The time delay associated with sampling time of the digital signal processor DSP, filtering, and modulator are combined here in  $G_d(s)$ . Therefore,

$$G_d(s) = \frac{1}{1 + T_{eq}s}$$
(2.25)

where  $T_{eq}$  is the summation of the following terms:

- 1. Sampling time of digital signal processor  $(T_s)$ ;
- 2. PWM modulator delay, when sampling time and switching frequency are adopted equally, the delay associated with PWM modulator will be  $T_s/2$  [10]; and
- 3. Delay caused by utilizing digital filters  $(T_{fi})$ , in the VOC scheme. It was assumed that three-phase voltage and current are ideal, which is not the case in the real world; therefore to avoid noise and harmonics, digital filters are utilized.

The plant transfer function, is defined as  $G_f(s)$ :

$$G_f(s) = \frac{i(s)}{v(s)} = \frac{1}{R_g + L_g s} = \frac{1/R_g}{1 + \frac{L_g}{R_g} s} = \frac{1/R_g}{1 + T_p s}$$
(2.26)

where

$$T_p = \frac{L_g}{R_g} \tag{2.27}$$

where  $T_p$  is time constant of the grid filter.

Delays in the current loop should be compensated in the PI controller to avoid overshoot and also to increase the stability margin. It can be seen that the time delay consists of one large delay ( $T_p$ , caused by the LCL filter,) and several small delays ( $T_{eq}$ ). Therefore, modulus optimum can be applied [11], which means a large constant time can be compensated by the PI controller's phase advance (pole-zero cancellation). Hence:

$$T_{iVOC} = T_p \tag{2.28}$$

It should be taken into account that to reject any disturbance existing in the grid,  $T_{iVOC}$  might be selected up to 10 times larger than  $T_p$  [12]. Writing a closed-loop transfer function of the current loop[1]:

$$H(s) = \frac{\frac{k_{pVOC}}{(L_g + L_i)T_{eq}}}{s^2 + \frac{s}{T_{eq}} + \frac{k_{pVOC}}{(L_g + L_i)T_{eq}}}$$
(2.29)

which means the process will have an optimal damped system with  $\xi = 0.707$  [1]:

$$k_{pVOC} = \frac{L_g + L_i}{2T_{eq}} \tag{2.30}$$

#### 2.6.2 Phase locked loop (PLL)

The principle of three-phase synchronous reference frame PLL (SRF-PLL) is illustrated in Figure 2.10. Grid voltage is transformed to dq rotating reference frame by Park transformation.

$$\begin{bmatrix} v_{dg} \\ v_{qg} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta_g) & \cos(\theta_g - 2\pi/3) & \cos(\theta_g - 4\pi/3) \\ -\sin(\theta_g) & -\sin(\theta_g - 2\pi/3) & -\sin(\theta_g - 4\pi/3) \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_bg \\ v_{cg} \end{bmatrix}$$
(2.31)

The fundamental voltage vector will be translated to DC variables. Since the *d*-axis of the synchronous frame is aligned with the grid voltage vector, the *q*-axis voltage will be equal to zero and the *d*-axis voltage will be equal to grid voltage magnitude. **n** order positive-sequence harmonic manifests itself as **n**-1 order harmonic in *d*q rotating reference frame, and **n** order negative-sequence harmonic exhibit **n**+1 order harmonic in *d*q rotating reference. Therefore, unbalanced voltage in the grid is transformed to second order harmonics in the *d*q rotating reference frame. High order harmonics can be filtered out easily by low pass filter from  $V_{ag}$ , but

for the filtering of the second order harmonic, a notch filter is usually employed for achieving fast dynamic performance and not compromising the PLL closed-loop bandwidth [13].

Then a PI controller is utilized to reduce the error between reference value (zero) and measured value for  $V_{qg}$ , and a feed-forward frequency  $\omega_{ff} = 2\pi * 60 Hz$  is added to the output to improve initial dynamic performance. Finally an integrator will be employed for converting  $\omega_g$ to  $\theta_g$ .

As demonstrated [1], having an optimal damped system with  $\xi = 0.707$ , and settling time of  $t_s$ , the proportional and integral constants for PLL shall be selected :

$$k_{pPLL} = \frac{9.2}{t_s} \tag{2.32}$$

$$T_{iPLL} = \frac{t_s}{4.6} \tag{2.33}$$



Figure 2.10 PLL based on synchronous reference frame (SRF)

## 2.7 Case study

The goal of this section is to design a grid-connected converter based on the design guidance and procedures provided in the previous sections in this chapter. The system specifications are given in Table 2.3 and a block diagram of the converter is illustrated in Figure 2.11.

## 2.7.1 Sizing of LCL filter

As given in Section 2.5.3, the filter capacitor shall be sized :

$$C_f \le 0.05 \times C_b = 15.75 \,\mu F \tag{2.34}$$

where  $C_b$  is the base capacitance of the system.

Therefore,

$$C_f = 10\mu F \tag{2.35}$$

Table 2.3 System specification of the grid-connected converter

Converter rated Power $P_n$	1.2 <i>kW</i>	Converter rated voltage $V_n$	102 V
Converter rated frequency $f_n$	60 Hz	Converter rated current $I_n$	7 A
Switching frequency $f_{SW}$	5 kHz	Sampling time $T_s$	0.1 <i>ms</i>

From Equation 2.12, the inverter-side inductor shall be selected:

$$L_{i} \geq \frac{\frac{0.195}{0.612}V_{n}}{\sqrt{3 \times 2\pi \times f_{sw}I_{n}\alpha}} = \frac{0.318 \times 102}{\sqrt{3 \times 6.28 \times 5000 \times 7 \times \alpha}}$$
(2.36)

Considering  $\alpha = 0.04$ :

$$L_i \ge 2.1 \, mH \tag{2.37}$$

Therefore,

$$L_i = 2.5 \, mH \tag{2.38}$$

To meet the inequality of 2.10,  $\beta$  is selected 0.05. Therefore from Equation 2.14 the grid-side inductor can be calculated as:

$$L_g = \frac{1 + \sqrt{\frac{1}{\beta^2}}}{\left(2\pi \times f_{sw}\right)^2 C_f} = \frac{21}{\left(2\pi \times 5000\right)^2 \times 10\mu F} = 2.1 \ mH$$
(2.39)

Thus,

$$L_g = 2.5 \, mH \tag{2.40}$$

To calculate the resonant frequency (Equation 2.7):

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_i + L_g}{L_i L_g C_f}} = 1554 \, Hz \tag{2.41}$$

It can also be seen that resonant frequency meets inequality 2.42:

$$10f_n \le f_{res} \le \frac{f_{sw}}{2} \tag{2.42}$$

From section 2.5.3, damping resistor can be sized as,

$$R_d = \frac{1}{3 \times 2\pi \times f_{res} \times C_f} = 3.41 \ \Omega \tag{2.43}$$

Power dissipation in the damping resistor is,

$$P_d \approx 3R_d \left(\frac{V_n}{\sqrt{3}} \times 2\pi f_n C_f\right)^2 = 0.5 W$$



Figure 2.11 Block diagram of the grid-connected converter discussed in the case study

## 2.7.2 PI tuning of the Voltage-Oriented Controller (VOC)

By adopting a digital filter with the cut-off frequency of 1 kHz in the VOC, equivalent delay caused by the current controller (introduced in Section 2.6.1) is,

$$T_{eq} = T_{fi} + T_s + \frac{T_s}{4} = 1.125 \ ms \tag{2.44}$$

And delay caused by the grid filter (see Equation 2.27) is,

$$T_p = \frac{L_g}{R_g} = \frac{0.0042}{0.8} = 5.25 \ ms \tag{2.45}$$

Therefore the integral time constant of the VOC controller is,

$$0.00525 \le T_{iVOC} \le 0.0525 \ ms$$
 (2.46)

From equation 2.30, proportional gain of the VOC controller can be calculated,

$$k_{pVOC} = \frac{L_g + L_i}{2T_{eq}} = \frac{4.2}{2.25} = 1.86$$
(2.47)

Hence integral gain of the VOC controller can be selected,

$$35 \le k_{iVOC} \le 354 \ s^{-1} \tag{2.48}$$

### 2.7.3 PI tuning of the Phase Locked Loop (PLL)

To achieve 50 ms settling time in PLL, proportional gain of the PLL can be selected,

$$k_{pPLL} = \frac{9.2}{t_s} = 184 \tag{2.49}$$

The integral time constant of the PLL is chosen by:

$$T_{iPLL} = \frac{t_s}{4.6} = 10.9 \, ms \tag{2.50}$$

Therefore, the integral time constant of the PLL,

$$K_{iPLL} = 16928 \ s^{-1}$$
 (2.51)

## 2.7.4 Simulation

To summarize, the complete specification of the designed grid-connected converter is given in Table 2.4; moreover, to verify the design guidelines, the grid-connected converter is simulated in the Simulink/Matlab environment.

The result obtained for the voltage, current, active and reactive power, when the converter operating at nominal power, is given in Figure 2.12. Reactive power reference is intentionally set

at zero. In Figure 2.13, the harmonic spectrum of the converter's current is shown, where  $I_{gn}$  the RMS value of nth-order harmonic is current and  $I_{g1}$  is the RMS value of the fundamental frequency current. This verifies that the harmonic required level given in Table 2.1 is satisfied. In Figure 2.14, VOC response to the step change of the converter's active power reference is illustrated. As shown in Figure 2.15, PLL response to the step change of the grid frequency is depicted. It is verified that settling time of the PLL is 50 milliseconds.

Converter rated Power $P_n$	1.2 <i>kW</i>	Damping resistor $R_d$	3Ω
Converter rated frequency $f_n$	60 Hz	DC power supply $V_{dc}$	230 V
Converter rated voltage $V_n$	100 V	DC-link Capacitor C <sub>dc</sub>	1000 µF
Converter rated current $I_n$	7 A	PLL Proportional gain K <sub>pPLL</sub>	184
Grid-side inductor $L_g$	2.5 <i>mH</i>	PLL Integral gain K <sub>iPLL</sub>	16928
Inverter-side inductor $L_i$	2.5mH	VOC Proportional gain <i>K</i> <sub>pVOC</sub>	1.5
Filter Capacitor $C_f$	10 μF	VOC Integral gain <i>K</i> <sub><i>iVOC</i></sub>	50 $s^{-1}$
Grid-Filter resistance $R_g$	0.8 Ω	Sampling time $T_s$	(1/10000) s

Table 2.4 Simulation system specification of the grid-connected converter

# 2.8 Summary

In this chapter the structure of the grid-connected converter was presented. In addition, design guidelines for sizing of the LCL-Filter, selection of switching frequency and tuning of PI

controllers in the voltage oriented control (VOC) scheme and phase locked loop (PLL) were addressed. Moreover since most of the above-mentioned design criteria are specified by the grid codes, IEEE Std. 1547 was discussed as the main standard for the grid-connected converters. A case study with simulation was given to verify the design guidelines.



Figure 2.12 The grid-connected converter operating at nominal power



Figure 2.13 Harmonic spectrum of the converter's current



Figure 2.14 VOC response to the step change of the converter's active power reference



Figure 2.15 PLL response to the step change of the grid frequency

# **Chapter Three**

# **Islanding Detection Methods for the Grid-connected Converters**

As discussed in Section 2.2.5, detection of islanding is one of the requirements mandated by IEEE Std. 1547 for the grid-connected converters. Islanding detection methods have recently received a great deal of attention in research where higher penetration of the Distributed Power Generation Systems (DPGSs) is restructuring the face of the power system.

This chapter focuses on the anti-Islanding (AI) detection methods. First, islanding and its consequences are discussed; then anti-islanding requirements and its detection methods are investigated.

## 3.1 Islanding

In IEEE Std.1547-2008, an island is defined as "a condition in which a portion of an area of the electric power system is energized solely by one or more local electric power systems through the associated PCCs while that portion of the area of the electric power system is electrically separated from the rest" [4].

For a grid-connected converter, islanding happens if, after tripping the grid, the converter does not stop itself from injecting current within a short period of time and continues to feed local loads. Islanding can pose a risk to utility workers as they assume that the line is deenergized after disconnecting it for maintenance, and the converter location could be an unknown for them. Moreover, re-closing of upstream breakers during islanding can cause major damage to converters due to their unsynchronized reconnection to the grid. Another issue is that due to a mismatch between active and reactive power delivered by converters and consumed by loads, the voltage and frequency of the islanded grid might shift considerably from rated values. Therefore islanding is a hazard to people, equipment and grid-connected converters, and should be properly detected and avoided [5]. As a result of these risks, anti-islanding (AI) requirements have been issued and embodied in the standards [1].

# 3.2 Anti-islanding requirements in IEEE Std. 1547

Based on IEEE Std. 1547, which is applicable for converters with rated power of less than 10MVA connected to primary or secondary distribution systems, the following AI requirement is given: "For an unintentional island in which the converter energizes a portion of the electric power system through the PCC, the converter interconnection system shall detect the island and cease to energize the area within two seconds of formation of island."[4]

The test procedure for meeting the AI requirement described is shown in Figure 3.1 [4]:

- 1- Equipment under test (EUT) (here it applies to grid-connected converter) is set to deliver 100% rated output power ( $P_n$ ) and connected to the grid. Grid nominal voltage is set to nominal voltage of converter ( $V_n$ ), with a maximum 2% deviation, and the grid nominal frequency is set to the nominal frequency of converter ( $f_n$ ), with a maximum 0.1Hz deviation.
- 2- The RLC load should be adjusted according to Equation 3.1, 3.2 and 3.3, which means R is selected to dissipate all the power delivered by the converter at nominal voltage. LC circuit will resonate at nominal frequency, which means reactive power generated by C will be the same as reactive power absorbed by L. The required quality factor for this

standard is  $Q_f = 1$ , which means the reactive power stored in L or C is equal to the active power consumed by R. The higher value of  $Q_f$ , the stronger the tendency to work or remain at the resonant frequency.

$$R = \frac{V_n^2}{P_n} \tag{3.1}$$

$$L = \frac{V_n^2}{2\pi f_n P_n Q_f} \tag{3.2}$$

$$C = \frac{P_n Q_f}{2\pi f_n V_n^2} \tag{3.3}$$

- 3- Having all switches closed (S1, S2, and S3), the RLC load should be fine-tuned until the grid current is less than 2% of rated value in each phase. Then S3 is opened and the time between the opening of S3 and the time period when the converter ceases to energize the RLC load is recorded. This should be less than two seconds.
- 4- This test must be repeated ten times with active power references set at 100%, 75%, 50% and 25% of nominal value.



Figure 3.1 Unintentional islanding test configuration, source IEEE Std. 1547-1

### **3.3 Non-detection zone (NDZ)**

Anti-islanding (AI) is a protective scheme for the grid-connected converters; therefore its performance can be measured in a manner similar to power system protective relays. It should be robust enough to discriminate between islanding and disturbance in the network which can be implied as *selectivity*. *Dependability* of protection is also tested with the test procedure described previously in 3-2, which can be considered as the worst case scenario. *Reliability* is also defined as the ability of the scheme to detect islanding under any given conditions within a given time interval [1].

Figure 3.2 shows the typical interconnection of utility, load and grid-connected converter (GCC), where load is actually the summation of total available local loads and GCC represent all operating converters connected to the PCC, therefore:

$$P_{load} = P_{GCC} + \Delta P$$

$$Q_{load} = Q_{GCC} + \Delta Q$$
(3.4)

where  $P_{load}$  and  $Q_{load}$  are active and reactive powers of load,  $P_{GCC}$  and  $Q_{GCC}$  are active and reactive power delivered by converters, and  $\Delta P$  and  $\Delta Q$  are active and reactive power delivered by grid at PCC.

When the grid is connected, voltage and frequency of PCC are fixed in a steady state condition. However, once the grid is disconnected from PCC, based on the power balance equation given in 3.4, active power of the load has to follow the active power delivered by converters. Since active power is only tied to voltage, the voltage at PCC should have to change as described below [1]:

$$V'_g = V_g \sqrt{\frac{P_{GCC}}{P_{load}}}$$
(3.5)

On the other hand, reactive power is a function of both frequency and voltage. Therefore based on the power balance equation, islanding frequency can be calculated as [1]:

$$Q_{GCC} = V_g'^2 (\frac{1}{2\pi f' L} - 2\pi f' C)$$
(3.6)

Therefore,

$$f' = \frac{-\frac{Q_{GCC}}{CV'_{g}^{2}} + \sqrt{\left(\frac{Q_{GCC}}{CV'_{g}^{2}}\right)^{2} + \frac{4}{LC}}}{4\pi}$$
(3.7)

In the IEEE Std.1547, the acceptable operating range of distributed resources for voltage has been defined as 88% to 110% of nominal voltage and an acceptable frequency is between 59.4 to 60.5 Hz. The worst case scenario in islanding happens when  $\Delta P = 0$ ,  $\Delta Q = 0$ . Hence no change in frequency or voltage of PCC is detected. On the other hand, if active and reactive power required by the load remains close enough to the active and reactive power delivered by the gridconnected converters, voltage and frequency still cannot drift out of an acceptable window during islanding. Thus, as shown in Figure 3.3, a non-detection zone (NDZ) appears. In other words, the NDZ for each method of AI is a range of local loads connected to the PCC for which the AI method under consideration can fail to detect islanding properly [1].

## 3.4 Anti-islanding (AI) detection methods

Islanding detection methods as shown in Figure 3-4 can be classified into three categories:

1- *Converter-resident methods* can be divided further into passive and active methods. Passive methods are based on monitoring and detection of any abnormality in the parameters of voltage at the point of PCC caused by disconnection of the grid. Active methods deliberately generate a disturbance in the PCC and then monitor the response to detect whether the utility is disconnected.

- 2- *External impedance insertion* can be implemented by connecting low value impedance, usually a capacitor bank at the utility side of PCC when the grid is disconnected, which creates a step change in the phase between current and voltage of converter at PCC.
- 3- Grid-resident methods require means of communication between the grid and converter such as the PLCC (power line carrier communication) or SCADA (supervisory control and data acquisition).



Figure 3.2 Interconnection of grid-connected converter



Figure 3.3 Non-Detection zone (NDZ)

## 3.5 Passive anti-islanding detection methods

Passive methods rely on changes of voltage, frequency phases or THD of voltage at PCC when the grid is disconnected to detect the islanding.

## 3.5.1 Over/under voltage/frequency Detection (OUF-OUV)

As discussed earlier, converters, to protect the equipment of consumers, are required to have a OUF/OUV (over/under voltage, over/under frequency) protective scheme to stop the converter from supplying power to the grid if the voltage or frequency at PCC are not in the permissible range. Based on [21], NDZ for OUF:

$$Q_f \left( 1 - \left(\frac{f'}{f_{\min}}\right)^2 \right) \le \frac{\Delta Q}{P_{GCC}} \le Q_f \left( 1 - \left(\frac{f'}{f_{\max}}\right)^2 \right)$$
(3.8)

And NDZ for OUV:

$$\left(\frac{V'_g}{V_{\max}}\right)^2 - 1 \le \frac{\Delta P}{P_{GCC}} \le \left(\frac{V'_g}{V_{\min}}\right)^2 - 1$$
(3.9)

According to IEEE Std. 1547,  $V_{\text{max}} = 1.1 V_{nom}$ ,  $V \min = 0.88 V_{nom}$ , and  $f_{\text{max}} = 60.5$  Hz and  $f_{\min} = 59.3$  Hz,  $Q_f = 1$ . Therefore NDZ for OUF:

$$-2.37\% \le \frac{\Delta Q}{P_{GCC}} \le 1.64\%$$
(3.10)

And NDZ for OUF:

$$-17.36\% \le \frac{\Delta P}{P_{GCC}} \le 29.13\% \tag{3.11}$$

As can be seen, NDZ for reactive power mismatch is much smaller than that of the active power

mismatch (2.37% vs. 29.13%); also NDZ boundaries for the mismatch in reactive power become larger when  $Q_f$  is increased.



Figure 3.4 Anti-islanding methods

### 3.5.2 Phase jump detection (PJD)

This method monitors the phase difference between converter voltage terminals and current for a sudden change. As long as the converter is connected to the grid, the set-point for reactive power is given by the operator; therefore, the phase difference and power factor at the converter terminal voltage is fixed. As soon as the islanding takes place, the power factor is dictated by load; Moreover, the converter output current is fixed and the frequency has not changed yet. As a result, voltage of the converter must jump to a new phase immediately. If the sudden jump in the phase is greater than threshold value, a shutdown signal immediately stops the converter from supplying power to the grid.

The NDZ of PJD is derived as [14]:

$$\left| \arctan\left(\frac{\frac{\Delta Q}{P_{GCC}}}{1 + \frac{\Delta P}{P_{GCC}}}\right) \right| \le \theta_{thershold}$$
(3.12)

As can be seen, NDZ in PDJ, similar to the OUV/OUF method, is very insensitive to an active power mismatch. However it is independent from  $Q_f$ . One drawback here is that a phase shift can also happen due to other issues in the grid like the switching reactive load, and therefore  $\theta_{threshold}$  in practice needs to be selected with the safety margin between 2 to 5 degrees [14]. As a result NDZ cannot be eliminated.

### 3.5.3 Harmonic detection method (HD)

This method monitors specific harmonics such as 3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup> or THD level at PCC's voltage.

As long as the grid is connected, since the equivalent impedance seen at PCC is low, the harmonic created by converter's current does not have a considerable effect on the harmonic level in PCC. However once the grid is disconnected, the equivalent impedance seen at PCC is replaced by the load impedance which is much higher. Therefore the harmonic spectrums that exist in the converter's current show themselves in the voltage at PCC.

In theory, this method can reduce NDZ to zero and does not depend on the power mismatch However, the problem is that in the polluted grid, it is not easy to determine a threshold level; in addition, the harmonic condition in the grid might change due to nonlinear load and no-load transformers [1].

### 3.5.4 Summary of the passive methods

It is noted that passive methods have the same common problem for adjusting proper threshold, since having too-sensitive settings may increase the chance of nuisance trip and otherwise NDZ remains non-zero.

## 3.6 Active anti-islanding detection methods

Active methods deliberately inject a small disturbance into certain parameters at PCC and then monitor the response to detect whether the utility is disconnected. Since the voltage source converter behaves as a controlled current source, this disturbance can be implemented by changing the amplitude, phase or frequency of the injected current [4]. While the grid power is available, these small changes have little effect besides a small degradation of power quality. Once the grid is lost, frequency and voltage of PCC are not stiff anymore, as equivalent impedance seen by the converter terminals increase significantly. Thus any small disturbance created by active methods can present itself at PCC. Active methods, usually in combination with the passive method, can reduce NDZ to zero, but the challenge here is to minimize the degradation of power quality and also to avoid instability in the network. The other issue is a dilution of the active method when multiple converters are connected to the grid, as disturbances created by converters might cancel each other out [15].

#### **3.6.1 Frequency drift methods**

In these methods, the frequency or phase of the current generated by the converter is modified, usually with positive feedback. In the instance of islanding, the disturbance will push the frequency out of the normal range and it detects by OUF. Frequency shift methods are not sensitive to the grid impedance; however, they become less effective with loads that have a high quality factor [1].

#### **3.6.1.1 General electric frequency shift (GEFS)**

With this approach, frequency is measured in the PLL loop. When the estimated frequency goes up, the control scheme increases the set-point for reactive power in the converter. As a result, based on Equation 3.7, the frequency keeps going higher to balance the reactive power. In fact, the increased frequency will further increase the reactive power and eventually it will hit the OUF relay [15].

As shown in the Figure 3.5, the estimated frequency goes through a low pass (10Hz) and high pass filter (1Hz) to remove DC offset and noise respectively. After that, the output of the

filter is amplified by a gain and restricted by a limiter and then is added to the operator's setpoint of reactive power in the converter. The gain selected should be small enough to minimize instability when the grid is connected and large enough to detect islanding. According to [16],

$$\Delta \omega \approx -\frac{\Delta Q_{GCC}}{R.P_{GCC}(C + \frac{1}{\omega^2 L})}$$
(3.13)

where  $\omega$  is the angular frequency; therefore, gain and limiter setting directly depend on the quality factor of the load and the actual active power of converter. In this method, THD degradation is very small and thus with increasing gain, NDZ can be reduced to zero. This method has good potential when multiple converters are involved but according to GE this can be problematic for the stability of the network [15].



Figure 3.5 GEFS method

### **3.6.1.2** Active frequency drift (AFD)

As illustrated in Figure 3.6, by setting the frequency of the injected current slightly higher (or lower) than the frequency of voltage at PCC, there will always be a tendency for the converter to change the frequency, but the presence of the grid does not allow any change in the frequency. The distorted current exhibits itself only with low harmonics' ( $3^{rd}$ ,  $5^{th}$ ,  $7^{th}$ ,  $9^{th}$ , ...) components in the current. In the islanding condition, the drift in the frequency of the current will shift the frequency of voltage, and eventually this frequency will drift and hit OUF relay [17].



Figure 3.6 AFD method

The chopping factor is defined as:

$$c_f = \frac{T_z}{T/2} = \frac{\delta f}{\delta f + f} \tag{3.14}$$

As shown in [18], to reduce the THD less than 5 % (maximum limit mandated by IEEE Std.1547), chopping factor should be less than 0.05. Therefore, the converter current is calculated each time in the microprocessor:

$$i_g = \hat{I}\sin(2\pi(f_{k-1} + \delta f)t)$$
 (3.15)



Figure 3.7 Modifying grid angles in PLL for AFD method



Figure 3.8 AFD implementation

In practise, this method can easily be implemented by building  $\theta_i$  from  $\theta_g$  (grid angle), as depicted in Figure 3.7, and then utilizing  $\theta_i$  as a phase reference to make PWM outputs as shown in Figure 3.8.

As can be seen, in the steady state phase the shift of current with respect to voltage will be:

$$\theta_i \cong T_z \pi f = \frac{\pi}{2} c_f \tag{3.16}$$

AFD would fail to detect islanding, If for any frequency between 59.3 Hz to 60.5 Hz (normal operating range), the load phase matches the current phase, i.e.:

$$\arctan\left(R(\omega C - \frac{1}{\omega L})\right) = \frac{\pi}{2}c_f$$
(3.17)

In other word, the phase difference introduced by the current is compensated with load phase and results in a steady state condition with no further drift in the frequency. In fact, with an analytical approach it has been shown that this method is only effective with resistive and inductive loads [19]. Another problem with AFD is degradation of power quality, as shown in [18]: to reduce the THD to less than 5 % (maximum limits given by IEEE Std.1547), chopping factor should be less than 0.05.

### 3.6.1.3 Sandia frequency shift (SFS)

This method employs AFD with a linear positive feedback from frequency deviation to increase the chopping factor [20]:

$$c_f = c_{f(k-1)} + k(\Delta \omega_k) \tag{3.18}$$

The phase criterion here is:

$$\arctan\left(R(\omega C - \frac{1}{\omega L})\right) = \frac{\pi}{2} \left[c_{f(k-1)} + k(\Delta \omega_k)\right]$$
(3.19)

And according to [15], by selecting an initial chopping factor of 0.05 and k equal to 0.1, NDZ will be zero for all loads with  $Q_f \le 4.8$ .

SFS employs a fast clock to measure the frequency in each half-cycle with zero crossing detectors (ZCD). In theory, the chopping factor should be zero when the grid is available; however, frequency in the grid changes all the time within +/- 0.01 Hz and most of the time within +/- 0.03Hz. Furthermore, with noise and harmonics available in the network, the measured frequency with ZCD is changing all the time. Thus, in practice the chopping factor will not be zero, and SFS will degrade the power quality in the normal operating condition. Also, when multiple converters are equipped with this scheme, the system behaviours caused by the harmonics and their interactions will be unpredictable [15].

### 3.6.1.4 Active frequency drift with pulsating chopping factor (AFDPCF)

This method is an improved AFD scheme [18], based on the following criteria in design:

- 1- Maximum detection time should be less than 2 seconds, based on IEEE Std. 1547 standard.
- 2- Absolute value of chopping factor should be always less than 0.05% to meet the IEEE
   Std. 1547 5% THD limit as illustrated in Figure 3.9.

The method as proposed in [10] is an AFD method with a variable chopping factor. As illustrated in Figure 3.10, the chopping factor changes between 0.05, -0.05 and zero periodically (20 cycles, 20 cycles, 60 cycles respectively), so when  $\Delta Q < 0$ , but is not in the detectable range

by OUF protection, negative chopping factor in seven cycles can push the frequency out of the range. In addition, if  $\Delta Q > 0$ , but is not in the detectable range by OUF protection, a positive chopping factor in seven cycles can force the frequency to drift up and hit the OUF relay.

When multiple converters are equipped with AFDPCF, one converter might work with a positive chopping factor, while the other one works with a negative chopping factor. As a result the scheme fails in detection of islanding.



Figure 3.9 THD versus chopping factor



Figure 3.10 Chopping factor in AFDPCF
### 3.6.1.5 Slip mode frequency shift (SMS)

Normally the phase of the injected current of converter is kept at zero with respect to the voltage at PCC. However, in the SMS scheme phase the current is controlled to be a function of frequency, with a positive feedback. For example, if the frequency of the PCC voltage reduces when islanding happens, the phase angle of the current goes down, this reduces the time to the next zero crossing of the PCC voltage. This is interpreted by the controller as a frequency decrease, so the phase angle of the current is decreased again, and so on, until the frequency hits the OUF relay [21].

Considering that:

$$i_g = I \sin(2\pi f_{k-1}t + \theta_{SMS}) \tag{3.20}$$

the phase of the current is calculated in each sampling time as the function of frequency :

$$\theta_{SMS} = \theta_m \sin(\frac{\pi}{2} \frac{f_{k-1} - 60}{f_m - 60}) \tag{3.22}$$

where  $f_m$  is maximum frequency at which maximum shift of  $\theta_m$  occurs [19]. As shown in Figure 3.11, it is obvious that the frequency of the islanded system drifts from the nominal value frequency only if:

$$\left[\frac{\delta\theta_{load}}{\delta f}\right]_{60Hz} < \left[\frac{\delta\theta_{SMS}}{\delta f}\right]_{60Hz}$$
(3.23)

Knowing that:

$$\theta_{load} = \arctan\left(R(\omega C - \frac{1}{\omega L})\right)$$
(3.24)

and substituting Equation 3.22 and 3.24 into Equation 3.23:

$$\frac{\theta_m}{f_m - 60} \ge \frac{12Q_f}{\pi^2} \tag{3.25}$$

Having  $Q_f = 1$ , and selecting  $f_m = 63$ Hz, for  $\theta_m \ge 3.7^\circ$  NDZ will be zero. In this method, similar to other drift methods for the load with large quality factors, performance will be equal to OUV/OUF passive method [19].



Figure 3.11 Phase versus frequency in SMS

### 3.6.1.6 Reactive power variation (RPV)

The principle of RPV scheme [22] is illustrated in Figure 3.12. As shown already in Equation 3.13:

$$\Delta \omega \approx -\frac{\Delta Q_{GCC}}{R.P_{GCC} \left(C + \frac{1}{\omega^2 L}\right)}$$
(3.26)

by altering the reactive power reference typically seen at low frequency (1Hz to 15Hz), when the grid is disconnected the frequency can be pushed out of the nominal range and will hit OUF relay. The more the active power and the greater the quality factor of the load, the more variation in reactive power is required to push the frequency out of the window. The problem with this method is that the variations of reactive powers in the converters cannot be synchronized and therefore will not be effective in drifting the frequency [1].



Figure 3.12 RPV method

### 3.6.2 Voltage drift methods

These methods rely on changing the voltage at PCC either by disturbing the injected current or by varying active power. Voltage at PCC is stiff while the grid is present; however, once the grid is disconnected, the disturbance can drift the voltage out of the normal range where it can be detected by OUV. Voltage shift methods are sensitive to impedance grid. Two methods given in the following figure are typically combined with their frequency shift counterparts to make the schemes more robust [1].

### 3.6.2.1 General electric voltage shift (GEVS)

In this method, when the measured voltage at PCC goes down, the control scheme decreases the set-point for active power in the converter. Based on equation 3.5, the voltage keeps going lower to balance the active power, and the decreased voltage will further diminish the active power and eventually will hit the OUV relay. As shown in Figure 3.13, the measured voltage goes through a low pass (10Hz) and high pass filter (1Hz) to remove DC offset and noise respectively; then the output of the filter is amplified by a gain and confined by a limiter. Finally, the signal is added to the active power reference calculated in MPPT. In this approach THD degradation is very small, and therefore by increasing gain, NDZ can be reduced to zero. This also has good potential when multiple converters are involved, but according to GE it can be problematic for network stability [15].

### 3.6.2.2 Sandia voltage shift (SVS)

Here, amplitude of the output current waveform is perturbed in response to utility voltage fluctuations. When the voltage goes up, output current is increased. When voltage goes down, output current is reduced; therefore, when the utility is connected, this method exhibits small fluctuations in output power and output current. However when the grid is absent, voltage at PCC eventually hits the OUV relay. The control signal is selected as the difference between filtered average voltage and cycle-by-cycle measurements of RMS voltage [20].



Figure 3.13 GEVS method

### 3.6.3 Impedance estimation (IE)

By perturbing the injected current of the converter and measuring its response on the voltage at PCC, and equivalent impedance seen from the converter terminal can be measured. As already discussed in 3.6.3, during islanding the impedance of the grid is replaced by impedance of the load at a higher rate. Thus, islanding can be detected when the measured impedance at converter's terminal increases significantly.

# 3.6.3.1 Impedance estimation at chosen frequency

In this method, the converter's current is:

$$i_g = I_{\max} \sin(2\pi f t) \tag{3.27}$$

This is intermittently added in the specific intervals with one cycle of

$$i_{f1} = I_{f1} \sin(2\pi f_1 t) \tag{3.28}$$

And one cycle of

$$i_{f2} = I_{f2} \sin(2\pi f_2 t) \tag{3.29}$$

Here f1 and f2 are non-characteristic frequencies in the grid, for instance, 400Hz and 600Hz as utilized in [23]. The reason for having two different frequencies is that two unknown parameters in impedance need to be estimated ( $R_g$  and  $L_g$ ). By measuring voltages components at frequencies of f1 and f2 ( $V_{f_1}$  and  $V_{f2}$ ),

$$Z_{f1} = \frac{V_{f1}}{I_{f1}}$$
(3.30)

$$Z_{f2} = \frac{V_{f2}}{I_{f2}}$$
(3.31)

where  $Z_{f1}$  and  $Z_{f2}$  are impedance of the grid at frequencies of f1 and f2 respectively. The real and imaginary parts of grid impedance are calculated as [23]:

$$L_{grid} = \frac{1}{2\pi} \sqrt{\frac{Z_{f1}^2 - Z_{f2}^2}{f_1^2 - f_2^2}}$$
(3.32)

$$R_{grid} = \sqrt{\frac{f_1^2 Z_{f2}^2 - f_2^2 Z_{f1}^2}{f_1^2 - f_2^2}}$$
(3.33)

If multiple converters are equipped with this scheme, this method will fail to measure the grid impedance accurately, when two or more of them inject the harmonic current simultaneously.

### 3.6.3.2 Impedance estimation at time domain

In this approach [24], instead of injecting current at two different frequencies, two stationary working points are created with the changing reference for active and reactive power at specific intervals, as shown in Figure 3.14.

By having two sets of voltage and current at the converter's terminal, impedance can be estimated.

Looking at Figure 3.15, it can be seen that:

$$V_1 = I_1 Z_{grid} + Vg \tag{3.34}$$

$$V_2 = I_2 Z_{grid} + Vg \tag{3.35}$$

Assuming that Vg remains constant between two working points,

$$Z_{grid} = \frac{\vec{V}_1 - \vec{V}_2}{\vec{I}_1 - \vec{I}_2}$$
(3.36)

$$R_{grid} = \frac{\Delta V_d \Delta I_d - \Delta V_q \Delta I_q}{\Delta I_d^2 + \Delta I_q^2}$$
(3.37)

$$L_{grid} = \frac{\Delta V_q \Delta I_d - \Delta V_d \Delta I_q}{(\Delta I_d^2 + \Delta I_q^2)\omega^2}$$
(3.38)

It is obvious that when two converters changed their working points simultaneously, this scheme might still fail.



Figure 3.14 Changing active and reactive power for measuring grid impedance



Figure 3.15 Measuring of grid impedance with two working points

### 3.6.4 Negative sequence detection

In this approach, another VOC controller is working parallel with the main VOC controller, injecting 3%, negative sequence current to the PCC. When the utility is disconnected, it manifests itself by imbalanced voltage at PCC [25]. Also as it can be seen in [26] this method can detect islanding when multiple converters are involved.

### 3.6.5 PLL based methods

These methods deliberately perturb the derived grid phase angle and then measure its response in the voltage at PCC. For example as one specific example, the phase grid derived by PLL will be augmented with a zebra signal, and the same pattern is expected to be observed during the islanding by monitoring the voltage at PCC [1].

# 3.7 External impedance insertion (EII)

As illustrated in Figure 3.16, once the grid circuit breaker becomes disconnected, within a small delay, another circuit breaker connects a capacitor bank to the PCC and creates a phase jump, which can be detected with PJD. Implementation of this method is expensive and needs additional equipment.

Therefore, it cannot be considered as a solution for small PV converters due to the high cost of implementation [5].



Figure 3.16 External impedance insertions

## 3.8 Grid-resident anti-islanding detection methods

Grid-resident methods require means of communication between grid and converter such as PLCC (power line carrier communication) or SCADA (supervisory control and data acquisition).



Figure 3.17 Power line carrier communications to detect islanding

### **3.8.1** Power line carrier communications (PLCC)

This method is depicted in Figure 3.17; here by sending a low-energy low-frequency signal transmitted from the grid (T) over the power line. Continuity of the circuit is tested. If the signal cannot be detected by the receiver (R), it means that islanding has already happened.

The signal should be sent continuously to fulfill the two seconds detection time required by IEEE Std.1547. It should be also low frequency to propagate from transformers in the circuit [5]. PLCC can eliminate NDZ completely and can work without any problem when multiple converters are involved. The only problem associated with this method is the cost of implementation.

### **3.8.2** Supervisory control and data acquisition (SCADA)

By installing a separate voltage sensor at PCC, voltage information is sent to the SCADA system. Existing voltage in the disconnected area means islanding has already happened. This method's barriers include major utility involvement and the high cost of implementation [1].

### 3.9 Comparison of anti-islanding detection methods

Islanding detection methods can be benchmarked, as demonstrated in Table 3.1, based on the three main criteria: 1) *Reliability*, 2) *Maintaining power quality*, and 3) *Multiple-converters application* [1]. *Reliability* is the main concern for all passive methods, as having too sensitive settings may increase the chance of a nuisance trip and otherwise NDZ remains non-zero. Therefore the passive methods are only utilized in combination with the active methods. Among the active methods, the positive feedback schemes exhibit better performance to fulfil the trade-off between *reliability* and *maintaining power quality*. Frequency shift methods become less reliable with the loads using high quality factors. Voltage shift methods become less effective with the high impedance networks. However, the main challenge for all active methods is *multiple-converter application* as there is not a consensus among the manufacturers for adopting a common scheme.

### **3.10 Summary**

In this chapter, islanding and the risks associated with it have been discussed. Anti-islanding

detection methods and the criteria for their evaluation were presented. Passive methods cannot eliminate NDZ and must be combined with active methods.

Active methods work on drifting of frequency or voltage or grid impedance measurement. Frequency drifting methods become ineffective when the load has a high quality factor. Voltage drift methods cannot work properly with a high impedance grid. The impedance measurement technique fails to detect islanding when multiple converters are involved.

Active methods are benchmarked based on reliability, degradation of power quality, and their performance, when multiple converters are equipped with the same scheme. GE and Sandia methods are more promising here, but there is still no consensus among the manufacturers to adopt a common platform.

Grid-resident methods rely on communication between the grid and converters, and they have a good potential for standardization in the long term.

AI method	Reliability	Maintaining	Maintaining Multiple converter	
		Power quality	in parallel	
OUV/OUF	Non-zero NDZ	High	High	
PJD	Non-zero NDZ, and susceptible for parasitic trips	High	High	
HD	Not good	High	High	
GEFS+GEVS	Very high, as NDZ can be eliminated	High, no influence on THD, stability of network can be affected	High	
AFD	Non-zero NDZ	Low, introduces low harmonics	Low, can-not handle concurrent detections	
SFS+SVS	Very high, as NDZ can be eliminated.	Medium, as continuous drifting can affect PQ	High	
AFDPCF	High	Low, introduce low harmonics	Limited , when one Converter is increasing frequency while another decreasing it	
SMS	Non-zero NDZ	Medium, only PF is affected.	Low, can not handle concurrent detections	
RPV	High	High	Low, injection of reactive powers can reduce its effect due to averaging	
IE	Medium, there is potential for parasitic trip depending on grid impedance level	Medium,	Low, as reading can be wrong during parallel injection	
EII	High, but cost for implementation is high	High	Low	
PLCC/SCADA	High, but cost for implementation is high	High	High	

# Table 3.1 Performance comparison for AI methods

# **Chapter Four**

# Novel Anti-Islanding Method for Multiple-Converters Application

Anti-islanding is an important feature in the low-power grid-connected converters. The main criteria are reliability, power quality degradation, and suitability for parallel operation. In the passive methods, a zero non-detection zone cannot be achieved. Therefore the reliability of passive methods is limited. In the active methods, a null NDZ can be met. However, the main challenges are to reduce the power quality degradation and to make sure that the scheme works in the multiple-converters application.

In this chapter a novel active anti-islanding method is proposed. The intent is to develop a robust, active AI method with no impact on power quality and stability of the network that can be utilized in multi-converter applications.

### 4.1 Problem statement

There are two major problems that occur with the existing AI methods. First, as illustrated in Table 3.1, most of the active AI methods, such as Sandia Frequency Shift (SFS), Sandia Voltage Shift (SVS), Active Frequency Drift with Pulse Chopping Factor (AFDPCF), and Active Frequency Drift (AFD) degrade power quality, since they continuously inject disturbance into the network. The second issue with some of the active AI methods is the dilution effect when multiple converters are paralleled. For instance, both the RPV and AFDPCF scheme fail in multi-converter applications because the disturbance injected by one converter can cancel the other due to lack of synchronization between them.

To solve the former problem, a novel method is proposed for injecting disturbance only when a potential for islanding is sensed. At the same time this method will synchronize converters with each other to fix the latter issue. As already discussed in chapter 3, when the grid is connected, the frequency is a stiff parameter. In fact, the frequency in comparison with voltage and phase is the most robust parameter in the network.



Figure 4.1 PLL based on synchronous reference frame (SRF)

Therefore  $\Delta \omega$  which is measured in PLL (as shown in Figure 4.1) is either zero or a constant value (under steady state condition). When the grid is disconnected, it can be shown as follows that the frequency will no longer be a stiff parameter [27]:

 $Z_{LC}$ , impedance of LC branch of load can be written as:

$$Z_{LC} = \frac{\omega' L}{1 - {\omega'}^2 LC} \tag{4.1}$$

Where  $\omega'$  is also the angular frequency of the grid after grid disconnection. Alternatively  $Z_{LC}$  can be expressed as:

$$Z_{LC} = \frac{R.P_{GCC}}{Q_{GCC}} \tag{4.2}$$

where  $P_{GCC}$  and  $Q_{GCC}$  are the active and reactive power supplied by the grid-connected converter, respectively. By equating (4.1) and (4.2) we arrive at:

$$\omega'^2 - \frac{Q_{GCC}}{RCP_{GCC}}\omega' - \frac{1}{LC} = 0 \tag{4.3}$$

Therefore:

$$\omega' = \frac{\frac{Q_{GCC}}{RCP_{GCC}} + \sqrt{\left(\frac{Q_{GCC}}{RCP_{GCC}}\right)^2 + \frac{4}{LC}}}{2}$$
(4.4)

The quality factor of the load is defined as:

$$Q_f = R_{\sqrt{\frac{C}{L}}}$$
(4.5)

Also

$$\frac{4}{LC} \gg \left(\frac{Q_{GCC}}{RCP_{GCC}}\right)^2 \tag{4.6}$$

Therefore (4.4) can be rewritten as:

$$\omega' \cong \frac{1}{\sqrt{LC}} \left(1 + \frac{1}{2Q_f} \frac{Q_{GCC}}{P_{GCC}}\right) \tag{4.7}$$

In the worst case scenario in the islanding,

$$\omega = \frac{1}{\sqrt{LC}} \tag{4.8}$$

Therefore:

$$\omega' \cong \omega + \frac{\omega}{2Q_f} \frac{Q_{GCC}}{P_{GCC}}$$
(4.9)

$$\frac{\Delta\omega}{\omega} \approx \frac{1}{2Q_f} \frac{\Delta Q_{GCC}}{P_{GCC} + \Delta P_{GCC}}$$
(4.10)

where  $\Delta \omega$  is defined as

$$\Delta \omega = \omega' - \omega \tag{4.11}$$

Also

$$\Delta P_{GCC} \ll P_{GCC} \tag{4.12}$$

As a result, we find:

$$\frac{\Delta\omega}{\omega} \cong \frac{1}{2Q_f} \frac{\Delta Q_{GCC}}{P_{GCC}}$$
(4.13)

Equation 4.13 states that when there is no mismatch in reactive power,  $\Delta \omega$  still fluctuates slightly all the time around the nominal frequency. In practice, due to the presence of harmonic distortion and unbalanced supply voltages, a low pass filter and notch filter are employed in PLL. Thus a very high bandwidth could not be achieved, and the response time of PLL usually has to be set to 50 to 100 milliseconds [1], whereas the response time of the current loop is much faster (less than 5 milliseconds). The discussed phenomenon is best shown in Figure 4.2 when one converter is involved.

However, when multiple converters are paralleled, 4.13 can be rewritten as

$$\frac{\Delta\omega}{\omega} \approx \frac{1}{2Q_f} \frac{\sum \Delta Q_{GCC}}{\sum P_{GCC}}$$
(4.14)

Due to the averaging effect,  $\sum \Delta Q_{GCC} \ll \sum P_{GCC}$ ; therefore, changes in frequency will be very small when a large number of the converters are paralleled. Even in the RPV method where  $Q_{GCC}$  is changed intentionally, the changes in each converter still cannot be synchronized with the rest. Therefore the RPV method may fail in the multiple- converters application.



Figure 4.2 Variation of frequency after islanding

# 4.2 Novel anti-islanding method

The principle of the proposed hybrid method is illustrated in Figure 4.3, where the photovoltaic or wind system is replaced by a DC power supply. Three-phase voltages at the grid side ( $v_g$ ), and three-phase currents at the converter output terminals ( $i_g$ ), are detected for use in the converter controller. The Maximum Power Point Tracking (MPPT) block ensures that the maximum power is captured from PV or wind system. Based on which it generates a reference for active power ( $P_{ref}$ ). The reactive power ( $Q_{ref}$ ) is usually set to zero by the operator. The voltage source inverter (VSI) controls the power flow from the DC side to the grid. A harmonic filter is utilized to remove the switching harmonics to meet the grid code. A digital phase-locked loop (PLL) block ensures that the frequency and phase of the injected current is synchronized with respect to the grid voltage. A utility transformer is employed to step up the voltage of the distributed generation and also to eliminate the DC current injection into the grid.

The proposed active AI method consists of a combination of Positive Feedback Frequency Shift (PFFS) and Reactive Power Variation (RPV) as illustrated in Figure 4.3(b). In the PFFS method, the reactive power reference  $(Q_{ref})$  is augmented by positive feedback derived from the changes of grid frequency as measured by the PLL. When the measured frequency  $\omega$  increases, the anti-islanding scheme will proportionally increase the amount of reactive power supplied by the converter  $(Q_{GCC})$ . As a result, the frequency keeps increasing in order to balance the reactive power. The increased frequency will further drive the converter's reactive power up, which is known as the positive feedback frequency shift method. To maintain the stability of the DG system, the maximum positive feedback reference is only limited to  $\pm 0.5\%$  of the converter supplied power.

The PFFS scheme in the proposed AI method is only employed to pre-detect potential islanding in advance and to synchronize the converters for initiating the main active islanding detection method. When 0.1Hz frequency shift is detected, as shown in Figure 4.3(b), the RPV scheme or the other active islanding detection method is triggered by an RS flip-flop for a short period of time to push the frequency or voltage out of the acceptable range. Therefore, as all active methods embedded in the converters are triggered simultaneously, the proposed scheme will not fail at the multiple-converter applications. The details of the proposed AI method and selection of its parameters and boundaries are addressed in the following subsections.

### 4.2.1 Positive feedback frequency shift scheme (PFFS)

According to Equation (4.13),  $\pm 0.5\%$  variation of reactive power is adequate to change the frequency by 0.1Hz when islanding takes place with the load quality factor of one (1.0) as required by IEEE Std. 1547.

Considering  $\theta$  and  $\Delta t$  are the phase shift and its associated time delay generated in each cycle due to variation in reactive power [22],

$$\Delta t = \frac{\theta}{\omega} = \frac{\tan^{-1}(0.005)}{2\pi.60} = 14.9\,\mu\text{s} \tag{4.15}$$

The required time to shift the frequency by 0.1Hz,  $T_Q$ , when the reactive power has already changed by 0.5% can be calculated by

$$T_{Q=}\left(\frac{1}{60} - 14.9\,\mu\right) + \left(\frac{1}{60} - 2 \times 14.9\,\mu\right) = 33.3ms \tag{4.16}$$

#### 4.2.2 Positive feedback gain

The variation of the measured grid frequency  $\omega$  related to the variation of the reactive power is given by:

$$\Delta Q_{GCC} = K_{pf} \Delta \omega \tag{4.17}$$

where  $K_{pf}$  is the gain of the PFFS pre-islanding detection scheme shown in Figure 4.3(b). According to [28], the lower limit of  $K_{pf}$  can be derived as:

$$K_{pf}(\min) = \frac{2Q_f P_{GCC}}{\omega_n} = \frac{2}{2\pi.60} = 0.005$$
(4.18)

A higher value of  $K_{pf}$  means that a larger disturbance is added to the reactive power reference when the same frequency variation occurs, which will positively contribute to the reliable detection of islanding. However, selecting a gain that is too high has a negative impact on the power quality of the grid [28]. In this research, the gain is selected equal to 0.08, which according to Equation (4.13) corresponds to a 0.5% variation in the reactive power for the 0.01Hz step change in the grid frequency.



Figure 4.3 The proposed active AI scheme

### 4.2.3 Low pass filter (LPF)

A low pass filter is employed to filter out the high frequency disturbance and noises that might exist in the measured grid frequency. In this paper the LPF with a corner frequency of 25Hz is utilized, which gives a response time of 0.04 seconds.

### 4.2.4 Finite impulse filter (FIR)

To remove any possible DC offset that might exist in the measured grid frequency and to monitor any frequency changes in each of the 0.2 second intervals, a FIR difference filter is proposed, as shown in Figure 4.3(b). The output of the FIR filter utilized in this study is at the  $n^{th}$  sample:

$$u[n] = \omega[n] + \omega[n-1] + \omega[n-2] + \omega[n-3] + \dots$$

$$n = 1, 2, 3, \dots, m$$
(4.19)

where  $\omega[n]$  is the measured angular frequency at the  $n^{th}$  sample. Considering the sampling time of 1/5000 seconds for the system, m is chosen to be 999.

This implies that the FIR block integrates continuously from the measured frequency in a definite time of 0.2 seconds. The output of the FIR difference filter is:

$$y[n] = u[n] - u[n-1]$$
(4.20)

Substituting u[n] and u[n-1] into (4.19) yields:

$$y[n] = \omega[n] - \omega[n - 1000] \tag{4.21}$$

The PFFS pre-islanding detection method works based on the deviation between the measured frequency of each sample and the sample acquired 0.2 seconds earlier. Moreover, the PFFS filters out any DC offset in the measured frequency.

As shown in Figure 4.3(b), if the measured grid frequency  $\omega$  changes more than 0.1Hz in each 0.2 seconds interval, the RS flip-flop is set by the comparator, and the RPV or other active islanding detection schemes are triggered to detect the islanding.

### **4.2.5** Pre-detection time $(T_0)$

Pre-detection time ( $T_0$ ), as shown in Figure 4.4, is defined as the time required by the PFFS scheme to shift the frequency by 0.1Hz after islanding occurs. In Figure 4.5, an analytical approach to estimate the maximum pre-detection time is presented. The frequency of the injected current ( $f_{mea}$ ) is calculated by PLL from the frequency of the grid voltage ( $f_{act}$ ). The variation in the measured frequency, with a delay caused by utilizing a low pass filter ( $T_{LPF}$ ) multiplied by the gain ( $K_{pf}$ ), will be utilized as the reactive power reference. The converter reactive power reference ( $Q_{ref}$ ). The converter reactive power with a delay given in Equation 4.16 ( $T_Q$ ) drifts the frequency. Therefore if the settling time of PLL selected is smaller than the pre-detection time, the maximum value for  $T_0$  can be calculated by:

$$T_0 \le T_{LPF} + T_{VOC} + T_O \tag{4.22}$$

where  $T_{LPF}$  is the time delay introduced by the low pass filter, and  $T_Q$ , is the time required for a 0.5 % shift in the reactive power with 0.1Hz shift in the frequency when the grid is disconnected.  $T_{VOC}$  is the current-control settling time, and as discussed in Section 2.6.1 can be approximated by:

$$T_{voc} = 5 T_p \approx 5 \frac{L_g}{R_g} \tag{4.23}$$

where  $T_p$  is the time constant of the harmonic filter in Figure 4.3, and  $L_g$  and  $R_g$  are total inductance and resistance of the filter, respectively [3].  $T_P$  is typically between 0.5-5ms [13]. Therefore,

$$T_0 \le T_{LPF} + T_{VOC} + T_O \approx 100 \ ms \tag{4.24}$$

A settling time of 50 ms can be chosen in the PLL, which is smaller than the pre-detection time and yet is still large enough to filter out the switching harmonics and the unbalanced supply voltages existing in the DG system.



Figure 4.4 Variation of frequency with positive feedback



Figure 4.5 Analytical approach to estimate the pre-detection time

### 4.2.6 RPV Method

Once a 0.1Hz deviation (in an interval of 0.2 seconds) in the grid frequency is detected, the RPV method (or other active AI methods) is initiated for all the power converters for a short period of time. As a result, all of the converters are synchronized and islanding can be detected. Obviously, if a 0.1Hz change in the grid frequency has occurred due to a disturbance in the system (but not islanding), enabling the active AI method for a short period of time have a little impact on the power quality of the system.

In Figure 4.6, PFFS and RPV schemes are combined. The reactive power reference  $Q_{ref}$  for one cycle is augmented with the reactive power pattern shown in Figure 4.7, where the required variation in  $Q_{RPV}$  from 0 to 2.5% is achieved by a ramp ( $T_1$ ).  $Q_{RPV}$  is kept constant at 2.5% for ( $T_2$ ), which can drift frequency out of the range and will hit the over/under frequency protective relay in less than 50 milliseconds [22]. Moreover,  $T_2$  compensates for any delay that might exist between converters in the pre-detection time.



Figure 4.6 The proposed active scheme combined with RPV

As shown in Figure 7, the proposed method detects the islanding within  $T_3$ , where

$$T_3 < T_0 + T_1 + 50ms \tag{4.25}$$

This method, similar to other frequency shift methods, is affected by quality factor of the load. Therefore, as already shown in 4.13, the greater quality factor of load, the higher variation of reactive power is required to push the frequency out of the window. For example, for a load with a quality factor of 2.5, the maximum RPV reference shall be increased to  $\pm$ -6.25% (of  $P_{GCC}$ ).

## **4.3** Computer simulation

This section presents the computer simulation and verification of the proposed anti-islanding

scheme discussed earlier. The simulation model is developed in the Simulink/Matlab environment. Simulation is performed according to IEEE Std. 1547 test setup with one converter connected to the grid with zero mismatches in active and reactive power followed by verification of the method in multiple converter applications.



Figure 4.7 One cycle reactive power injection pattern



Figure 4.8 Detection time in the proposed AI scheme

### 4.3.1 Simulation Model

The circuit diagram for test setup of the anti-islanding requirement for the grid-connected converter is shown in Figure 4.9, where the photovoltaic or wind system is replaced by a DC power supply. Three-phase voltages at grid side  $(v_g)$  and three-phase currents  $(i_g)$  at the converter output terminals are used to sense for the VOC controller. Three-phase voltage and current sets are transformed to DC variables by *abc/dq* block. The VOC controller is based on the setting given for active power  $(P_{ref})$  and reactive power  $(Q_{ref})$  which determines control signals for the pulse width modulator (PWM). PLL block ensures that the frequency and phase of injected current is synchronized with respect to the grid voltage. The utility transformer is employed to isolate grid voltage from DC power supply and also to reduce the operating voltage of the grid-connected converter for safety. LCL-filter  $(L_i, L_g, C_f)$  along with damping resistor  $(R_d)$  are adopted to meet grid code. RLC load is sized with unity quality factor and based on the nominal power of the converter as required by IEEE Std. 1547 (as shown in equation 3.1, 3.2, and 3.3).

In AI block the reactive power reference  $(Q_{ref})$  is augmented with a positive feedback derived from the changes of measured frequency in PLL in 0.2 second intervals. To maintain stability of the network, the positive feedback reference is only limited to +/- 0.5% (of  $P_{GCC}$ ) which is enough to change the frequency by 0.1Hz when the grid is disconnected. Upon detection of 0.1Hz changes in the measured frequency, RPV for only one cycle is initiated to shift the frequency out of the window. Small mismatches in active and reactive power are finetuned by adjusting active and reactive power references ( $P_{ref}$ ,  $Q_{ref}$ ) as described below: While CB2 is closed,  $P_{ref}$  and  $Q_{ref}$  are set to 1 (pu) and 0 (pu) respectively, CB1 is used to connect the converter to the grid. Then  $P_{ref}$  is fine-tuned based on trial and error so that  $v_g$  does not present any changes with the opening of CB2. And finally  $Q_{ref}$  is adjusted so that frequency does not show any discrepancies with the opening of CB2. New values for  $P_{ref}$  and  $Q_{ref}$  are considered as the new references for active and reactive power. To verify the proposed method when multiple converters are connected to the grid, simulation is performed when three converters are equipped with PFFS schemes as shown in Figure 4.10.

### 4.4 Simulation results

In this section, results obtained from the following simulations are provided: 1) Islanding with zero mismatch in active and reactive powers, 2) PFFS scheme, 3) Anti-islanding scheme when  $Q_f = 1$ , 4) Anti-islanding scheme when  $Q_f = 2.5$ , 5) Anti-islanding scheme when  $P_{GCC} = 50\%$  and, 6) PFFS scheme with three converters paralleled. Simulation system specifications of the grid, transformer, load and grid-connected converters are listed in Table 4.1 and 4.2 respectively.

### 4.4.1 Islanding with zero mismatch in active and reactive power

In this sub-section, the islanding with no mismatches between active and reactive power of the grid-connected converter and the load is simulated. In Figure 4.11, the islanding happens at t=0.7s (CB2 is opened at t=0.7s). With selection of  $P_{ref} = -1195$  W (0.97 pu) and  $Q_{ref} = -21$ Var (-0.017 pu) mismatches in active and reactive power are set to zero, as shown in Figure 4.11(a) and 4.11(b) respectively. Therefore voltage and frequency keep their nominal value after the islanding as shown in Figure 4.11(d) and 4.11(e) respectively. Figure 4.12 states that although the fundamental component of the converter's output voltage does not change after islanding, the profile of the HD of voltage will change during islanding. This is verified as simulated in Figure 4.11(e), which demonstrates that even when there is not a mismatch in reactive power and active power, still  $\Delta \omega$  fluctuates slightly all the time around the nominal frequency, based on equation (4.13). As discussed earlier, these variations are utilized in positive feedback frequency shift (PFFS) schemes as will be shown in the next section.



converter controller

Figure 4.9 Circuit diagram of AI test-setup

Grid voltage	208 V	Grid frequency $f$	60 Hz
Transformer rated Power	10 kVar	Resistance of load <i>R</i>	8.4 Ω
Transformer rated primary voltage	208 V	Capacitance of load C	330 µF
Transformer rated secondary voltage	100V	Inductance of load L	20 mH
Transformer leakage impedance	4%	Quality factor of load $Q_f$	1.07

 Table 4.1 Simulation system specification of the grid, transformer and the load



Figure 4.10 Circuit diagram of AI test-setup for three converters

Converter rated Power $P_n$	1.2 <i>kW</i>	Damping resistor $R_d$	3 Ω
Converter rated frequency $f_n$	60 Hz	DC power supply $V_{dc}$	230 V
Converter rated voltage $V_n$	100 V	DC-link Capacitor C <sub>dc</sub>	1000 µF
Converter rated current $I_n$	7 A	PLL Proportional gain K <sub>pPLL</sub>	184
Grid-side inductor $L_g$	2.5mH	PLL Integral gain K <sub>iPLL</sub>	16928
Inverter-side inductor $L_i$	2.5mH	VOC Proportional gain <i>K</i> <sub>pVOC</sub>	1.5
Filter Capacitor $C_f$	10 µF	VOC Integral gain <i>K</i> <sub><i>iVOC</i></sub>	50
Grid-Filter resistance $R_g$	0.8 Ω	Sampling time $T_s$	(1/10000) s

 Table 4.2 Simulation system specification of the grid-connected converter

### 4.4.2 Positive feedback frequency shift (PFFS) scheme

In this sub-section, the islanding with PFFS scheme enabled is simulated. In Figure 4.13, the islanding happens at t=0.7s (CB2 is opened at t=0.7s), while the measured frequency and the variation of frequency are given in Figure 4.13(a) and Figure 4.13(b) respectively.

It is verified that PFFS shifts the frequency by 0.1Hz when the reactive power reference is changed by +/- 0.005% as illustrated in Figure 4.14. In addition, the pre-detection time ( $T_0$ ) is smaller than 100ms.



Figure 4.11 The islanding with zero mismatches in active and reactive power



Figure 4.12 Converter output voltage dq components



4.13 Positive feedback frequency shift (PFFS) scheme to pre-detect islanding



Figure 4.14 Reactive power references when PFFS scheme is enabled.



**Figure 4.15** Detection of islanding when  $Q_f = 1$ 

# **4.4.3** Performance of Anti-islanding scheme when $Q_f = 1$

In this sub-section, the anti-islanding scheme is simulated when  $Q_f = 1$ . The PFFS scheme shifted the frequency by 0.1Hz as shown in Figure 4.15(a) and pre-detects the islanding in less than 100ms, which triggers RPV. The boundary for reactive power reference,  $Q_{RPV}$ , is set at +/-0.03%;  $T_1$  and  $T_2$  are set 0.12s, and 0.1s respectively, as shown in Figure 4.15(b). At this point, the frequency is shifted out of the acceptable range (i.e. 60.5Hz). Moreover, it can be seen that the detection time  $(T_3)$  is smaller than 2s .It is also verified that  $T_3 < T_0 + T_1 + 50ms$ .

# 4.4.4 Performance of Anti-islanding scheme when $Q_f = 2.5$

In this sub-section, the anti-islanding scheme is simulated when  $Q_f = 2.5$ . The PFFS scheme shifted the frequency by 0.1Hz as shown in Figure 4.16, and pre-detects the islanding in less than 100ms, which triggers RPV. The boundaries for  $Q_{PFFS}$  and  $Q_{RPV}$  are increased to +/- 1.25%, and +/- 0.0625% respectively;  $T_1$  and  $T_2$  are set to 0.22s, and 0.1s respectively. Therefore, the frequency is shifted out of the acceptable range (i.e. 60.5Hz). Moreover, it can be seen that the detection time ( $T_3$ ) is smaller than 2s. In addition, it is verified that  $T_3 < T_0 + T_1 + 50ms$ . The non-detection zone can be adjusted by changing the boundaries for  $Q_{PFFS}$  and  $Q_{RPV}$ .



**Figure 4.16** Detection of islanding when  $Q_f = 2.5$
# **4.4.5** Performance of Anti-islanding scheme when $P_{GCC} = 50\%$

In this sub-section, the anti-islanding scheme is simulated when  $P_{GCC} = 50\%$  and  $Q_f = 1$ . The PFFS scheme shifted the frequency by 0.1Hz, as shown in Figure 4.17, and pre-detects the islanding in less than 100ms, which triggers RPV. The boundary for  $Q_{PFFS}$  and  $Q_{RPV}$  are decreased to +/- 0.0025 %, and +/- 0.015 % respectively;  $T_1$  and  $T_2$  are set 0.12s, and 0.1s respectively. It is verified that the frequency is shifted out of the acceptable range (i.e. 59.3Hz); moreover, it can be seen that the detection time ( $T_3$ ) is smaller than 2s. It is also verified that  $T_3 < T_0 + T_1 + 50ms$ .



**Figure 4.16** Detection of islanding when  $P_{GCC} = 50\%$ 

## 4.4.6 Performance of PFFS scheme with three converters paralleled

In this sub-section, the PFFS scheme when three converters are connected to the grid is simulated (Figure 4.10). In Figure 4.13, the islanding happens at t=0.7s (CB2 is opened at t=0.7s), while the measured frequencies are illustrated in Figure 4.17(a), (b) and (c).

It is verified that the PFFS shifts the frequency by 0.1Hz for every converter as illustrated in Figure 4.17. It is also demonstrated that pre-detection time ( $T_0$ ) is smaller than 100 ms for all converters.



Figure 4.17 Positive feedback frequency shift (PFFS) scheme for three converters paralleled.

# 4.5 Anti-islanding performance comparison

As shown earlier in Table 3.1 anti-islanding methods are benchmarked based on the three main criteria 1) *Reliability*, 2) *Maintaining power quality* and 3) *multiple-converters application* [1].

#### 4.5.1 Reliability

The PFFS pre-detection scheme, similar to other frequency shift methods like GEFS, RPV, SFS, and SMS, is affected by the quality factor of the load. Therefore, as already shown in Equation 4.13, the more quality factor of load, the higher the variation of reactive power is required in order to change the frequency by 0.1Hz. As a result, this method exhibits similar performance in terms of *reliability* compared to other frequency shift methods and the NDZ can be eliminated in all practical situations.

#### 4.5.2 Maintaining power quality

Many of the active AI methods, such as the Sandia Frequency Shift (SFS), Sandia Voltage Shift (SVS), Active Frequency Drift with Pulse Chopping Factor (AFDPCF), and Active Frequency Drift (AFD) degrade power quality, since they continuously inject disturbance into the network. In the proposed method, the active method to detect islanding is triggered only when is called upon by PFFS. Therefore this method will not have an effect on the power factor (PF), total harmonic distortion (THD) and the stability of the network. As a result, this method exhibits superior performance in terms of *maintaining power quality* compared to other AI methods.

#### 4.5.3 Multiple-converters application

Many of the active AI methods such as Active Frequency Drift with Pulse Chopping Factor

(AFDPCF), Active Frequency Drift (AFD), Reactive Power Variation (RPV), and Slip Mode frequency Shift (SMS) could fail when multiple converters are connected to the grid. This happens since the disturbance injected by one converter can cancel the other due to lack of synchronization between them. The PFFS scheme introduces a unique method to synchronize converters. Therefore the PFFS scheme can be utilized in combination with other active methods when multiple converters are paralleled to the grid.

# 4.6 Summary

In this chapter, a hybrid AI method based on the combination of PFFS and RPV was proposed. Unlike the RPV scheme, this method is capable of synchronizing converters with each other; therefore, it can detect islanding when the multiple converters are paralleled. This novel proposed method can also be combined with other active methods (such as AFDPCF) to reduce the power quality degradation since the scheme is called upon only when 0.1Hz deviation in the grid frequency is detected. Moreover unlike GEFS, this scheme does not impact the stability of the network as the positive feedback reference is only limited to +/- 0.5% (of  $P_{GCC}$ ). Here the positive feedback frequency shift (PFFS) is only utilized to pre-detect the islanding in less than 100 ms when 0.1Hz deviation in the frequency is detected in the 0.2s time interval. The active method to detect islanding is triggered only when it is called upon by the PFFS. Thus, the proposed active AI method has no impact on power quality and stability of the network. Additionally, it can be utilized in multi-converter applications. Performance of the proposed method was verified in the single and multiple-converters application by simulation in Simulink/Matlab.

# **Chapter Five Experimental Verification**

This chapter presents the experimental verification of the proposed anti-islanding detection method for the three-phase grid-connected converter. A prototype of the low-power grid-connected converter is built based on the dSPACE prototyping system. Details of hardware and software for the system are presented. Experimental results are provided to verify the performance of the proposed active anti-islanding scheme.

## 5.1 Hardware implementation

Hardware configuration for the three-phase, grid-connected converter based on the dSPACE prototyping system is given in Figure 5.1, where the photovoltaic or wind system is replaced by a DC power supply. A small resistor ( $R_i$ ) in the series with DC power supply limits the charging current of the DC-link capacitor and also decouples voltage between the DC power supply and PWM rectifier. Three-phase voltages at grid side ( $v_g$ ) and three-phase currents ( $i_g$ ) at the converter output terminals are sensed, which are used for VOC controller. The Utility transformer is employed to isolate grid voltage from the DC power supply and also to reduce the operating voltage of the grid-connected converter for safety. An LCL-filter ( $L_i$ ,  $L_g$ ,  $C_f$ ) along with a damping resistor ( $R_d$ ) are adopted to meet the grid code. An RLC load is sized with unity quality factor and based on nominal power of a converter as required by IEEE Std. 1547.



Figure 5.1 Prototype of AI test-setup based on dSPACE

The interface between the controller and the converter is achieved through a dSPACE CP1103 I/O board and TTL/CMOS voltage level conversion board. The TTL/CMOS board converts dSPACE CP1103 I/O PWM signals of 0/+10 V to 0/+15 V as required by Semiteach Three-phase IGBT inverter. Voltage and current samples are also acquired by CP1103 I/O board and fed as digital signals into the dSPACE DS1103 PPC controller board. The dSPACE DS1103 functions as the real time controller for the grid-connected converter. The microprocessor of the DS1103 board is a PowerPC 604e/333MHz. The controller communicates with the PC through a DS814 board installed in the ISA slot.

# 5.2 Software implementation

The control program is written in the MATLAB/Simulink environment. The dSPACE real-time interface installed in the Simulink software converts a written program in the MATLAB/Simulink into assembly instructions readable for the DS1103 board.

ControlDesk software from dSPACE is used as a human machine interface (HMI) and serves to provide instrumentation, parameterization, measurements and experiment control.

# **5.3 Experimental results**

To verify the proposed anti-islanding method, experiment results are provided in this section for, 1) Converter connected to the grid, 2) Converter Islanding with zero mismatch in active and reactive powers, 3) PFFS scheme, 4) Anti-islanding scheme when  $Q_f = 1$ .

The experimental system specification of the grid, transformer, load and grid-connected converter are listed in Table 5.1 and 5.2 respectively.

Grid voltage	208 V	Grid frequency $f_n$	60 Hz
Transformer rated Power	10 kVar	Resistance of load <i>R</i>	8.4 Ω
Transformer rated primary voltage	208 V	Capacitance of load C	330 µF
Transformer rated secondary voltage	102 V	Inductance of load L	20 mH
Transformer leakage impedance	4%	Quality factor of load $Q_f$	1.07

**Table 5.1** Experimental system specification of the grid, transformer and the load

Small mismatches in active and reactive power are fine-tuned by adjusting active and reactive power references ( $P_{ref}$ ,  $Q_{ref}$ ) as explained below.

While CB2 is closed,  $P_{ref}$  and  $Q_{ref}$  are set to 1 (pu) and 0 (pu) respectively. CB1 is used to connect the converter to the grid.  $P_{ref}$  is then fine-tuned based on trial and error so that  $(v_g)$  does not present any changes with opening of CB2, And finally  $Q_{ref}$  is adjusted so that the frequency does not show any discrepancies with opening of CB2. New values for  $P_{ref}$  and  $Q_{ref}$  are considered, as the new references for active and reactive power.

Converter rated Power $P_n$	1.2 <i>kW</i>	Damping resistor $R_d$	3 Ω
Converter rated frequency $f_n$	60 Hz	DC power supply $V_{dc}$	230 V
Converter rated voltage $V_n$	102 V	DC-link Capacitor C <sub>dc</sub>	1000 μF
Converter rated current $I_n$	7 A	PLL Proportional gain K <sub>pPLL</sub>	184
Grid-side inductor $L_g$	2.5mH	PLL Integral gain K <sub>iPLL</sub>	16928
Inverter-side inductor $L_i$	2.5mH	VOC Proportional gain <i>K</i> <sub>pVOC</sub>	1.5
Filter Capacitor $C_f$	10 µF	VOC Integral gain <i>K</i> <sub><i>iVOC</i></sub>	50
Grid-Filter resistance $R_g$	0.8 Ω	Sampling time $T_s$	(1/10000) <i>s</i>
IGBT module voltage	1200 V	IGBT module Current	50 A

Table 5.2 Experimental system specification of the grid-connected converter

#### 5.3.1 Converter connected to the grid

The results obtained for the voltage, current and the grid phase angle when the converter operates at nominal power, is given in Figure 5.2. The reactive power is set to zero, therefore a 180 degree phase shift is observed between the converter's current and the grid voltage. It is also verified that THD of the current is smaller than 2%. In Figure 5.3, the VOC response to the step change of the converter's active power reference is illustrated.

The converter's current and its *dq* components when the converter outputs are set to 100 and 50% of its nominal value are illustrated in Figure 5.4 and 5.5 respectively. PLL response during start-up is presented in Figure 5.6. It is verified that the settling time of PLL is 50 milliseconds.



Figure 5.2 the grid-connected converter operating at nominal power



Figure 5.3 VOC response to the step change of active power reference



Figure 5.4 Converter output set at 100% of its nominal value

## 5.3.2 Islanding with zero mismatch in active and reactive power

In this sub-section, experiments with islanding with no mismatches between active and reactive power of the grid-connected converter and load are reviewed. As shown in Figure 5.7, voltage (and therefore power), reactive power (and therefore frequency) and the current are equal before and after islanding.



Figure 5.5 Converter output set at 50% of its nominal value



Figure 5.6 PLL response during start-up



Figure 5.7 The islanding with zero mismatches in active and reactive power

Research also demonstrates that when there is not a mismatch in reactive power and active power,  $\Delta \omega$  still fluctuates slightly all the time around the nominal frequency after islanding, and these variation are utilized in the positive feedback frequency shift (PFFS) scheme as will be shown in the next sub-section.

#### 5.3.3 Positive feedback frequency shift (PFFS) scheme

In this sub-section, islanding with the PFFS scheme enabled is investigated. The measured  $\Delta \omega$  and the variation of frequency at 0.2 second intervals  $(\Delta f|_{0.2 \text{ sec}})$  are given in 5.8. It is verified that PFFS shifts the frequency by 0.1Hz when the reactive power reference is changed by +/- 0.5%, as illustrated in Figure 5.8. Confirmation has been made that the pre-detection time  $(T_0)$  is smaller than 100ms. As shown in Figure 5.9, the PFFS scheme has a negligible effect on the reactive power and the power factor.

# **5.3.4** Performance of anti-islanding scheme when $Q_f = 1$

In this sub-section, the anti-islanding scheme is simulated when  $Q_f = 1$ . The PFFS scheme shifted the frequency by 0.1Hz as shown in Figure 5.10, and pre-detects the islanding in less than 100ms, which triggers RPV.



Figure 5.8 PFFS scheme to pre-detect islanding



Figure 5.9 Reactive power supplied by converter

The boundary for reactive power reference,  $Q_{RPV}$ , is set at +/- 0.03%;  $T_1$  and  $T_2$  are set at 0.1 s. Experiments demonstrated that frequency is shifted out of the acceptable range (i.e. 60.5Hz) and the converter stops itself from injecting the current. It can be seen that the detection time ( $T_3$ ) is smaller than 2s.



**Figure 5.10** Detection of islanding when  $Q_f = 1$  (over frequency)



**Figure 5.11** Detection of islanding when  $Q_f = 1$  (under frequency)

In Figure 5.11, the proposed scheme detects the islanding when the frequency drifts downward, which is different as the minimum required frequency shift is 0.7 Hz, whereas it is 0.5 Hz when the frequency drifts upward.

## 5.4 Summary

The proposed anti-islanding method based on the combination of PFFS and RPV are experimentally verified in this chapter. The prototype of a grid-connected converter equipped with the proposed AI scheme was built in the laboratory, based on the dSPACE prototyping system. Experiments are grouped into four categories: 1) steady state and start-up performance of the grid-connected converter, 2) islanding with zero mismatch in active and reactive power, 3) converter is only equipped with positive feedback frequency shift (PFFS), 4) performance of the proposed AI scheme, based on the experimental results obtained in this chapter. The following conclusion can be made:

The positive feedback frequency shift (PFFS) is only utilized to pre-detect the islanding in less than 100 ms when 0.1Hz deviation in the frequency is detected in the 0.2s time interval. The active method to detect islanding is triggered only when is called upon by the PFFS. Therefore, it will not have an effect on the power factor (PF), total harmonic distortion (THD) and the stability of the network. Most of the active AI methods, such as Sandia Frequency Shift (SFS), Sandia Voltage Shift (SVS), Active Frequency Drift with Pulse Chopping Factor (AFDPCF), and Active Frequency Drift (AFD) degrade power quality, since they continuously inject disturbance into the

network. As a result, this method exhibits superior performance in terms of maintaining power quality compared to other AI methods.

# Chapter Six Conclusion

Islanding refers to the condition in which distributed generators (DGs) continue to power a part of the network while the grid is no longer present. If islanding forms, repair crews may be faced with unexpected live wires. The equipment of end-users could be damaged because of changes in operating parameters. In addition, utility equipment and the islanded DGs might be damaged during re-closing. Therefore as required by IEEE Std. 1547, the distributed generators (including grid-connected converters) shall detect islanding and cease to inject current within two seconds of formation of an island [1].

Converter-resident anti-islanding methods are the subject of considerable research as they can be implemented inside converter firmware without any extra cost to the utility service provider. They can be classified into passive and active methods. Passive methods work based on monitoring and detection of any abnormality in the parameters of voltage measured at the converter output terminals, whereas active methods deliberately generate a disturbance and then monitor the response for detection.

Converter-resident anti-islanding methods are compared based on three main criteria: 1) reliability, 2) maintaining power quality and 3) multiple-converters application. The reliability of the passive methods is limited and therefore passive methods cannot be utilized as stand-alone entities. In active methods the main challenges are to reduce the power quality degradation and to make sure that the scheme is working in the multiple-converters application.

In this thesis, a novel active anti-islanding method for a three-phase, grid-connected converter has been developed, simulated and investigated.

The main contributions of the thesis are summarized as follows:

1) A novel active anti-islanding detection scheme, for the three phase grid-connected converters, has been developed. The proposed hybrid method works based on the combination of Positive Feedback Frequency Shift (PFFS) and Reactive Power Variation (RPV) methods, and therefore it combines the features of both methods. The majority of the active AI methods such as Active Frequency Drift (AFD), Active Frequency Drift with Pulse Chopping Factor (AFDPCF), Sandia Frequency Shift (SFS), Sandia Voltage Shift (SVS) degrade power quality, since they continuously inject disturbance into the network. In the proposed method, the active method to detect islanding is triggered only when it is called upon by PFFS. Therefore this method will not have an effect on the power factor (PF), total harmonic distortion (THD) or the stability of the network. As a result, this method exhibits superior performance in terms of *maintaining power quality* compared to other AI methods.

Moreover, the proposed scheme introduces a unique method to detect islanding when multiple converters are paralleled where many of the AI methods such as Active Frequency Drift with Pulse Chopping Factor (AFDPCF), Active Frequency Drift (AFD), Reactive Power Variation (RPV), or the Slip Mode frequency Shift (SMS) could fail. The proposed method employs the PFFS scheme to synchronize the injection of the disturbance among converters, whereas in the other mentioned methods the disturbance injected by one converter can cancel the effect of the other one due to lack of synchronization between them.

- 2) The performance of the proposed anti-islanding scheme, when single and multiple inverters are involved, has been verified with simulation in a Matlab/Simulink environment.
- 3) The proposed anti-islanding scheme, for a three phase grid-connected converter, has been experimentally verified. A laboratory prototype of a low-power grid-connected converter, based on the dSPACE rapid prototyping system, was built. Experiments were performed to verify the performance of the proposed anti-islanding method.

# References

- Teodorescu, R.; Liserre, M.; Rodríguez, P. "Grid Converters for Photovoltaic and Wind Power Systems", IEEE/Wiley, 2011.
- [2] Bollen, M.H.; Hassan, F., "Integration of Distributed Generation in the Power System", Wiley-IEEE Press, August 2011.
- [3] Nehrir, M.H.; Wang, C., "Modeling and Control of Fuel Cells: Distributed Generation Applications", Wiley-IEEE Press, March 2009.
- [4] IEEE Std. 1547-2003, Standard for Interconnecting Distributed Resources with Electric Power Systems, IEEE, June 2003.
- [5] Bower, W., and Ropp, M., 'Evaluation of Islanding Detection Methods for Utility-Interactive Inverters in Photovoltaic Systems'. SANDIA Report SAND2002-3591, Albuquerque, NM: Sandia National Labs, November 2002.
- [6] IEC 61727 Ed. 2, Photovoltaic (PV) Systems Characteristics of the Utility Interface, December 2004.
- [7] Wu, B., "High-Power Converters and AC Drives", Wiley-IEEE Press, March 2006.
- [8] Liserre, M.; Blaabjerg, F.; and Hansen, S. 'Design and Control of an LCL-Filter Based Three-Phase Active' Rectifier'. IEEE Transactions on Industrial Applications, 41(5), September/October 2005, 1281–1291.
- [9] Wu, B.; Lang, Y.; Zargari, N. and Kouro, S., "Power Conversion and Control of Wind systems", Wiley-IEEE Press, 2011
- [10] Buso, S.; Mattavelli, P. "Digital Control in Power Electronics", Morgan & Claypool Publisher, 2006.

- [11] Evju, E. 'Fundamentals of Grid Connected Photo-Voltaic Power Electronic Converter Design' Master of Science in Energy and Environment Thesis, Norwegian University of Science and Technology, June 2007.
- [12] Liserre, M., Blaabjerg, F. and Dell'Aquila, A., 'Step-by-Step Design Procedure for a Grid-Connected Three-Phase PWM Voltage Source Converter'. International Journal of Electronics, 91(8), August 2004, 445–460.
- [13] Yazdani A. and Iravani R., Voltage-Sourced Converters in Power Systems. Piscataway, NJ: IEEE/Wiley, Feb. 2010.
- [14] Ye, Z., Kolwalkar, A., Zhang, Y., Du, P. and Walling, R., 'Evaluation of Anti-islanding Schemes Based on Nondetection Zone Concept'. IEEE Transactions on Power Electronics, 19(5), September 2004, 1171–1176.
- [15] Ye, Z., Walling, R., Garces, L., Zhou, R., Li, L. and Wang, T., 'Study and Development of Anti-Islanding Control for Grid-Connected Inverters'. Report NREL/SR-560-36243, Golden, CO: National Renewable Energy Laboratory, May 2004.
- [16] S.-K. Kim, J.-H. Jeon, H.-K. Choi, and J.-B. Ahn, "Design of frequency shift acceleration gain for anti-islanding of an inverter-based DG," in Proc. 13th EPE-PEMC, Sep. 2008, pp. 2555–2560.
- [17] Ropp, M. E., Begovic, M. and Rohatgi, A., 'Analysis and Performance Assessment of the Active Frequency Drift Method of Islanding Prevention'. IEEE Transaction on Energy Conversion, 14(3), September 1999, 810–816.
- [18] Jung, Y., Choi, J., Yu, B., So, J. and Yu, G., 'A Novel Active Frequency Drift Method of Islanding Prevention for the Grid-Connected Photovoltaic Inverter'. In IEEE 36th Power Electronics Specialists Conference, PESC'05, 2005, pp. 1915–1921.

- [19] Lopes, L. A. C. and Sun, H., 'Performance Assessment of Active Frequency Drifting Islanding Detection Methods'. IEEE Transactions on Energy Conversion, 21(1), March 2006, 171–180.
- [20] Stevens, J.; Bonn, R.; Ginn J.; and Sigifredo Gonzalez Development and Testing of an Approach to Anti-Islanding in Utility-Interconnected Photovoltaic Systems SANDIA Report SAND2000-1939, Albuquerque, NM: Sandia National Labs, August 2000.
- [21] Lopes, L. A. C. and Sun, H., 'Performance Assessment of Active Frequency Drifting Islanding Detection Methods'. IEEE Transactions on Energy Conversion, 21(1), March 2006, 171–180.
- [22] Jeong, J.B., Kim, H.J., Ahn, K.S. and Kang, C.H., 'A Novel Method for Anti-Islanding Using Reactive Power'. in 27th International Telecommunications Conference, INTELEC '05, September 2005, pp. 101–106.
- [23] Ciobotaru, M., Teodorescu, R. and Blaabjerg, F., 'On-line Grid Impedance Estimation Based on Harmonic Injection for Grid-Connected PV Inverter'. In IEEE International Symposium on Industrial Electronics, ISIE 2007, 4–7 June 2007, pp. 2437–2442.
- [24] Ciobotaru, M., Teodorescu, R., Rodriguez, P., Timbus, A. and Blaabjerg, F., 'Online Grid Impedance Estimation for Single-Phase Grid-Connected Systems Using PQ Variations'. In IEEE Power Electronics Specialists Conference, PESC 2007, 17–21 June 2007, pp. 2306– 2312.
- [25] Karimi, H.; Yazdani, A.; Iravani, R.; , "Negative-Sequence Current Injection for Fast Islanding Detection of a Distributed Resource Unit," *Power Electronics, IEEE Transactions on*, vol.23, no.1, pp.298-307, Jan. 2008

- [26] Bahrani, B.; Karimi, H.; Iravani, R.; , "Nondetection Zone Assessment of an Active Islanding Detection Method and its Experimental Evaluation," *Power Delivery, IEEE Transactions on*, vol.26, no.2, pp.517-525, April 2011
- [27] Jeraputra, C.; Aeloiza, E.C.; Enjeti, P.N.; Choi, S.; , "An improved anti-islanding algorithm for utility interconnection of multiple distributed fuel cell powered generations," Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE, vol.1, no., pp.103-108 Vol. 1, 6-10 March 2005.
- [28] Seul-Ki Kim; Jin-Hong Jeon; Jong-Bo Ahn; Byongjun Lee; Sae-Hyuk Kwon; , "Frequency-Shift Acceleration Control for Anti-Islanding of a Distributed-Generation Inverter," Industrial Electronics, IEEE Transactions on , vol.57, no.2, pp.494-504, Feb. 2010.