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Current-mode techniques for UWB frequency synthesizers

Dominic DiClemente
Ryerson University

CURRENT-MODE TECHNIQUES FOR UWB FREQUENCY SYNTHESIZERS

by

Dominic DiClemente

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Abstract

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Current-Mode Techniques for UWB Frequency Synthesizers

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This thesis deals with current-mode techniques for ultra-wide band applications.

An overview of ultra-wide band (UWB) wireless communications is presented. Two standards for UWB data communications, namely direct-synthesis UWB (DS-UWB) and Multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB are presented. MB-OFDM UWB devices must hop among 14 UWB channels within 9.5 ns, imposing stringent constraints on design of frequency synthesizers. A review of the state-of-the-art frequency synthesizers for MB-OFDM UWB applications is provided.

Current-mode phase-locked loops with active inductors and active transformers employed in both loop filters and voltage-controlled oscillators are proposed and their performance is analyzed. Current-mode phase-locked loops decouple the PLL dynamic range from the scaling down of the supply voltage.

An active-inductor VCO with both coarse and fine frequency adjustment, a hybrid VCO with a step-down passive transformer loaded with an active inductor, and a hybrid VCO with a step-up passive transformer loaded with a varactor are proposed and their performances are analyzed. These VCOs obtain wide frequency tuning ranges without relying on

switched back networks.

To meet the timing constraint of UWB frequency synthesizers, Current-mode techniques are further developed for UWB frequency synthesizers. An active inductor with a bank of switched capacitors is proposed to provide fast locking. The bank of switched capacitors eliminates the frequency acquisition locking time of the frequency synthesizer, allowing 9.5 ns phase locking time.

The proposed current-mode phase-locked loops, active-inductors oscillators and hybrid oscillators were designed and implemented in TSMC-0.18μm and IBM-0.13μm CMOS technologies.

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First and foremost I would like to thank my advisor Dr. Fei Yuan for his guidance and inspiration during my tenure at Ryerson. His professionalism and enthusiasm during our weekly meetings always spurred me on to improve my work and provide inspiration to my research. I would also like to thank him for providing me with the freedom and atmosphere that allowed me to flourish and to take many tangents in my studies.

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Chapter 1

Introduction

With the explosive growth of the popularity in the unlicensed 2.4 GHz Industrial, Scientific and Medical (ISM) band, the demand for wireless connectivity in electronic devices is ever increasing. High quality multimedia require high data rates in addition to a better Quality of Service (QoS). When the Federal Communications Commission (FCC) created the ISM band they allocated 80 MHz centered at 2.4 GHz allowing for data rates up to 100 Mb/s. The continuous demand for better video and audio quality requires higher data rates than the ISM band can provide. With the advent of digital televisions on the horizon, existing wireless standards become inadequate for the required data rate of 25 to 935 Mb/s [1]. Current wireless standards cannot support the data rates of real-time high-definition videos due to limited bandwidth. Table 1.1 tabulates existing wireless standards and their data rate parameters.

1.1 Ultra Wide-Band

The maximum capacity of a channel is defined by the Shannon-Hartley theorem,

Table 1.1: Parameters of commercially available wireless networks [2].

Protocol	Frequency (GHz)	Data Rate (Mb/s)	Throughput (Mb/s)	Range (m)
802.11a	5	54	23	35
802.11b	2.4	11	4.3	38
802.11g	2.4	25.8	19	38
802.11n	2.4/5	54	74	70
802.11y	3.7	54	23	50

$$C = W \log_2(1 + SNR), \tag{1.1}$$

where C is the theoretical channel capacity limit, W is the bandwidth of the channel, and SNR is the signal-to-noise ratio of the channel. To increase the channel capacity two options exist. The first is to increase SNR, but this is limited by the noise of electronic circuits and propagation media. The second option is to increase the channel bandwidth.

In 2002, the FCC approved the operation of certain types of wireless devices utilizing ultra wide-band technologies for commercial use. Ultra wide-band systems differ from traditional narrow-band systems by employing low-power high-bandwidth signals in place of high-power low-bandwidth signals. The reduction in the signal power reduces the SNR, but the channel capacity is increased due to the substantial bandwidth increase.

The first transmission of an ultra wide-band signal was in fact the first wireless transmission and dates back to Marconi in 1890 with a spark gap generator. The spark gap generator produces a very narrow pulse that has a very large bandwidth due to the time-frequency duality (a narrow pulse in the time domain translates to a large bandwidth in

the frequency domain). Ultra wide-band systems continued to be developed in radar systems where narrow pulses allow for the accurate distance measurement of aircrafts. Ultra wide-band systems also found use in military communications due to the difficulty in the detection and reception of very narrow pulses. Meanwhile narrow-band systems prospered in the commercial market due to their lower cost and ease of implementation. With the narrow bandwidth used in traditional systems the data rates were severely limited. This gave rise to a renewed interest in ultra wide-band technology for commercial applications. The FCC proposed the largest frequency allocation spanning from 3.1 GHz to 10.6 GHz to be called 802.15.3 UWB. The applications of UWB include [3]:

- Wireless Personal Area Networks (WPANs) - Wireless personal area networks allow the high-speed transmission of signals up to a maximum distance of two meters. An example of WPAN is shown in Fig.1.1, consisting of a multi-media system that allows HDTV signals to be shared between cable/sat set top boxes, HD ready televisions, audio systems, Blu-ray DVD players, and personal computers all without wires.

- Sensor Networks - The desired characteristics of any UWB device are a low fabrication cost, low complexity and low power consumption. With these three attributes it is advantageous to create an array of transceivers that allow for accurate positioning. A transducer or other sensors can be included in the transceiver to allow for an array of measurements to be taken. An example of an UWB sensor network is the tracking of participants in an endurance race, which allows automatic time tracking and remote heart beat monitoring of participants.

- Imaging Systems - Similar to sensor networks the ultra short pulses that define the UWB can be used for imaging due to a large penetration depth at UWB wavelengths.

Figure 1.1: An example of an UWB wireless personal area network.

Imaging systems can allow rescuers at the scene of a natural disaster to locate victims without wasting time to dig or endanger the rescuers themselves.

- Vehicular Radar Systems - A leading cause of death in North America is car collisions. By using UWB devices as an automated radar warning system a warning tone can be emitted whenever a car or an object approaches the vehicle alerting or applying the breaks automatically.

UWB was the first frequency allocation to span over existing wireless standards. The proposed frequency spectrum of UWB and the existing standards are shown in Fig. 1.2. Since the existing standards cannot be changed, the FCC placed stringent restrictions on UWB devices. Any UWB "device may not cause harmful interference, and must accept

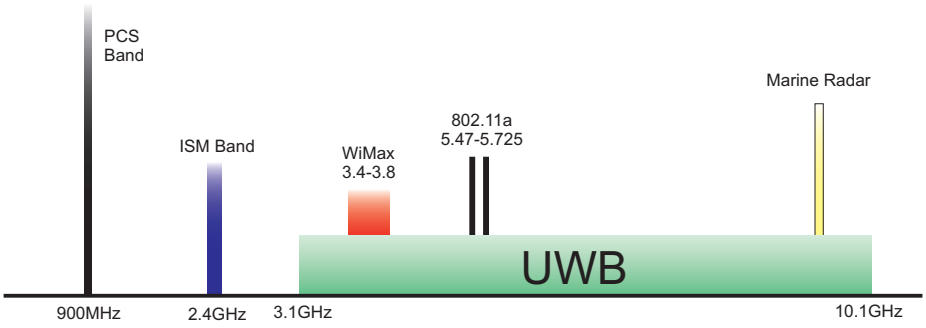

Figure 1.2: Spectral allocations showing the proposed UWB and existing narrow-band interferers.

any interference received, including interference that may cause undesired operation."[1] A harmful interference is defined as "interference that ... seriously degrade, obstruct or repeatedly interrupts a radio communication service."[2] To ensure that UWB devices do not interfere with existing networks under any circumstance UWB devices have severely limited power to transmit. The spectral mask defined by the FFC is shown in Fig. 1.3 [4]. Outside of the UWB spectrum the power must not be greater than -75 dBm/MHz. The small signal power of the GPS signal places perhaps the most stringent power restriction on UWB devices in this spectrum. GPS is a network consisting of many satellites used to send time signals to receivers for accurate positioning. The attenuation caused by traveling through the atmosphere results in small signal power that is easily corrupted by other devices.

The UWB spectral mask allows for power transmission of -41.3 dBm/MHz in-band, this low power spectrum ensures that it will not cause interference to existing narrow-band systems sharing part of the same spectrum (In-band interferers). In-band interferers can

[1]FCC 47 C.F.R. Sec 15.5(b).
[2]FCC 47 C.F.R. 1.907, Sec 2.1.

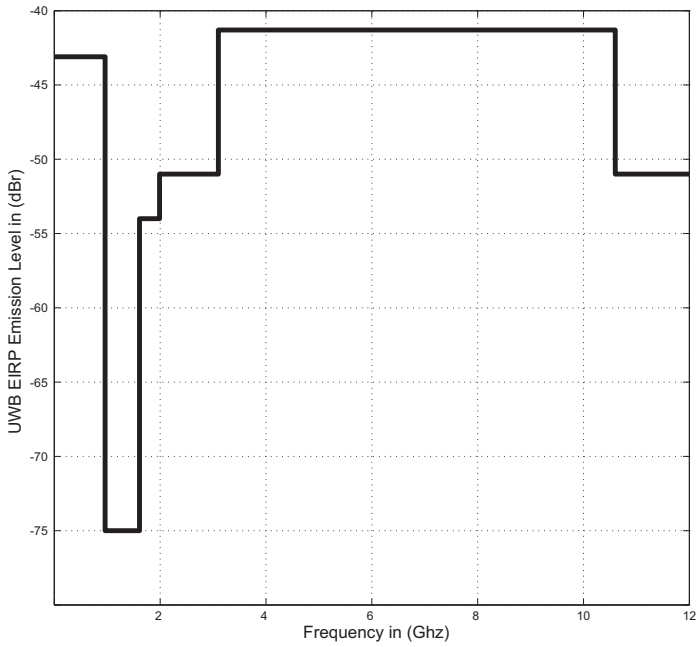

Figure 1.3: FCC specified spectral mask for indoor UWB commercial devices, severely limiting the output spectrum outside of 3.7-10.3 GHz.

cause interference in UWB devices due to their large signal that may saturate amplifiers and other RF components. As a comparison, cellphones operate at transmission power of +30 dBm/MHz, which is ten million times greater than that of UWB signals. The small signal power of UWB will mean a very low SNR ratio. Recalling from the Shannon-Hartley capacity theorem, a low SNR can be compensated by large bandwidth to maintain the same channel capacity. Out-of-band interferers can also cause interference even though they do not share the same spectrum. This is due to the common practice of using non-linear power amplifiers that create harmonic components inside the UWB spectrum [5] .

1.2 Objectives

The objective of this thesis is to develop current-mode techniques and circuits for application in ultra wideband. The current-mode techniques will be applied to PLLs and frequency synthesizers to combat the following challanges:

- Integrability: The proposed current-mode techniques should have less reliance on on-chip passive components. On-chip passive components add additional masking layers and expense. Passive components also have high tolerances which require digitally assisted analog blocks.

- Wide frequency Tuning range: VCOs should have a frequency tuning range over 30% without relying on switched bank networks. With a large frequency tuning range the current-mode frequency synthesizer can be applied to new wireless standards that rely on spread spectrum techniques or multi-standard radios.

- Quick Hopping: The MB-OFDM UWB quick channel hopping scheme has a 9.5 ns guard time. This short quard time makes it impractical to use integer frequency synthesizers, because it would require a closed loop bandwidth of several gigahertz. The proposed current-mode frequency synthesizer should be able to lock in under 9.5 ns without resorting to direct frequency synthesis.

1.3 Contributions

In this thesis, several current-mode techniques for wideband applications are proposed, and implemented to conform to the objectives stated above. The major contributions of this thesis are:

- Current-mode phase-locked loop - The proposed current-mode phase-locked loop decouples control signal dynamic range from the scaling of the supply voltage of CMOS technologies. In voltage-mode PLLs the dynamic range of the control signal is limited to the supply voltage, a reduction in the dynamic range will require a higher VCO gain. The increased VCO gain will result in a higher tolerance and increased noise response.

- Active Inductor and active transformer current-mode filtering - The inductance required for current-mode PLLs makes passive on-chip spiral inductors impractical, requiring active circuits to mimic inductance. Active inductors and active transformers previously used for bandwidth enhancement are used for current-mode filters.

- Wideband Oscillators - This thesis will propose three wideband oscillators. The three oscillators are capable of frequency tuning ranges of over 30% without using switched bank networks. Without relying on switched bank networks, along with the complexity and problems associated with a discontinuous frequency tuning curve are avoided.

- Quick hopping scheme - The 9.5 ns locking time of the MB-OFDM UWB channel hopping scheme makes it impossible to use traditional PLL based frequency synthesizers. This thesis proposes using a deterministic frequency hopping scheme to allow a PLL to lock in the required time. The quick hopping scheme eliminates the frequency acquisition time required by PLL based frequency synthesizers. By only requiring a phase lock the proposed frequency synthesizer is able to lock frequency and phase in the required time.

1.4 Thesis Organization

Chapter 2 (Frequency Synthesizers for Ultra WideBand devices) provides a brief introduction to Multiple-Band OFDM UWB devices. The locking time challenges of MB-OFDM UWB frequency synthesizers are explored. State-of-the-art UWB frequency synthesizers including a DLL based frequency synthesizer, a modified miller frequency divider and direct synthesis are introduced. Performance comparison of published MB-OFDM frequency synthesizers is included at the end of the chapter.

Chapter 3 (Current-Mode Phase Locked Loops) introduces modern techniques for battling the problem of supply scaling in voltage-mode PLLs. Current-mode filtering will be used to replace voltage-mode filtering. The inductance of the current-mode filter will be implemented using active inductors. A detailed analysis of active inductors will follow. Closed-loop expressions for current-mode PLLs are derived. The phase noise of current-mode PLLs is investigated. The simulation results of an active inductor based current-mode PLL are provided.

Chapter 4 (Current-Mode Phase Locked Loops with Transformers): introduces the concept of current-mode filtering using transformers. The inductance of the transformer will be implemented using active inductors. A detailed analysis of the winding inductance, mutual inductance, noise, and multiple windings is provided in the chapter. Closed-loop expressions for the active transformer based current-mode PLLs are derived. The phase noise of current-mode PLLs is also investigated. The simulation results of the transformer current-mode are presented.

Chapter 5 (Wide-Band VCOs for Frequency Synthesizers) starts with a brief introduction to the existing wide band VCOs that utilize switched banks to increase the frequency tuning range. This chapter introduces three new wideband VCOs that do not

use switched networks. An active inductor that provides large frequency tuning range is investigated. A hybrid oscillator that utilizes the superior phase noise performance of a passive transformer and the wide frequency tuning range of an active inductor is developed. A modified hybrid oscillator that uses the impedance scaling property of a passive transformer to increase the frequency tuning range of varactors is created. A comparison of the three presented wide band oscillators and existing wide band oscillators that use switched banks is provided.

Chapter 6 (Current-Mode Frequency Synthesizer UWB) introduces a current-mode frequency synthesizer for MB-OFDM UWB. A quick hopping scheme that will enable the frequency synthesizer to hop within 9.5 ns is developed. The frequency synthesizer will utilize an ILO as the frequency divider. By forcing the CCO's oscillation frequency to the different regions of the frequency tuning curve the ILO will lock to different UWB channels. Simulation results and a comparison to existing UWB frequency synthesizers are provided.

Chapter 7 (Conclusions) Summarizes the contributions of this research and suggests the future directions of research on wideband devices.

Chapter 2

Frequency Synthesizers for Ultra WideBand devices

This chapter starts with a brief introduction of Multiple-Band OFDM UWB. Section 2 describes the locking time challenges of MB-OFDM UWB frequency synthesizers. Section 3 introduces DLL based frequency synthesizer for UWB devices. Section 4 introduces a modified miller frequency divider used as an UWB frequency synthesizer. Section 5 introduces direct synthesis, including both parallel synthesis and single side-band mixing. Section 6 is a performance comparison of published MB-OFDM frequency synthesizers. The chapter is concluded in Section 7.

Two proposals for the adoption of an UWB standard were presented in [6] [7]. The first is called Direct Sequencing Ultra Wide-band (DS-UWB) and uses classical ultra wideband techniques. DS-UWB is a carrier-less modulation scheme. Unlike traditional narrow-band wireless standards that modulate a base-band signal by a carrier, the base-band is applied to shaped pulses. Time and frequency have an inversely proportional nature, i.e. the narrower a pulse in the time domain the larger the bandwidth it will occupy in the frequency domain.

By taking the advantage of UWB's large bandwidth the resulting pulses are ultra narrow in width, allowing for a high data-rate. The pulses can be modulated using traditional modulation techniques such as pulse position modulation or pulse amplitude modulation. DS-UWB devices have the advantage of simple RF front ends due to the absence of a carrier. Synchronization, however, is difficult due to the requirement of near perfect phase alignment with the receiver's correlators.

The second proposal is called Multi-Band Orthogonal Frequency Division Multiplexing Ultra WideBand (MB-OFDM UWB). An ultra wide-band signal is defined as a signal with fractional bandwidth greater than 0.2. Fractional bandwidth is defined as [8]

$$\text{Fractional Bandwidth} = \frac{F_H - F_L}{\frac{F_H + F_L}{2}}, \tag{2.1}$$

where F_H and F_L are the upper and lower boundaries of the frequency range over which 90% of the signal energy is contained, respectively. An UWB fractional bandwidth of 0.2 translates into a bandwidth of 500 MHz. Instead of trying to utilize the entire UWB band for a single device, MB-OFDM UWB divides the UWB band into 14 bands with equal channel width of 528 MHz. MB-OFDM UWB uses more traditional wireless techniques to effectively combat multipathing.

2.1 Multi-Band OFDM UWB

Multi-Band OFDM UWB consists of 14 bands, each has 528 MHz bandwidth. Each band has 128 OFDM subcarriers. The characteristics of 128 subcarriers are shown in Table. 2.1. Only 100 of the 128 carriers are used to carry data. 12 of the subcarriers are called pilots and used for synchronization and channel estimation. An additional 10 subcarriers are used as guard carriers. The guard carriers are used on either sides of the data carrying subcarriers

Table 2.1: Subcarriers of MB-OFDM UWB.

Number of data subcarriers	100
Number of defined pilot carriers	12
Number of guard carriers	10
Null subcarriers	6
Number of total subcarriers used	122
Subcarrier frequency spacing	4.125 MHz
IFFT/FFT period	242.42 ns

to prevent ICI with other UWB devices. The null carriers are used beside the guard carriers and used to relax the filter requirements. A subcarrier frequency spacing of 4.125 MHz is used. An IFFT/FFT sampling period of 242.42 ns ensures subcarrier orthogonality. Table. 2.2 shows the data rates of MB-OFDM.

Table 2.2: Data-rates of MB-OFDM.

Data Rate (Mb/s)	Modulation Scheme	Code Rate	Conjugate	Time Spreading	Coded Bits Per Symbol
53.3	QPSK	1/3	Yes	2	100
80	QPSK	1/2	Yes	2	100
110	QPSK	11/32	No	2	200
160	QPSK	1/2	No	2	200
200	QPSK	5/8	No	2	200
320	QPSK	1/2	No	1	200
400	QPSK	5/8	No	1	200
480	QPSK	3/4	No	1	200

The code rate is the convolutional encoder rate that introduces memory into the system to allow for error detection and correction. At lower data rates the last 50 subcarriers are

the conjugate of the upper 50 subcarriers. The use of conjugate subcarriers introduces redundancy that allows for error correction by sending the same bits sequence twice in every OFDM frame. The use of conjugate rather than a simple duplication of the base-band data results in an output signal having no imaginary component. An output signal without an imaginary component reduces the hardware requirement of the transmitter, as only a Q path is required.

Table 2.3: Time-Frequency Codes for a Group 1 MB-OFDM hopping sequence.

TFC	Hopping Sequence
1	1, 2, 3, 1, 2, 3
2	1, 3, 2, 1, 3, 2
3	1, 1, 2, 2, 3, 3
4	1, 1, 3, 3, 2, 2
5	1, 2, 1, 2, 1, 2
6	1, 1, 1, 2, 2, 2

To provide multi-user access and channel diversity an UWB device will hop among multiple channels. Since each mode is composed of 3 channels, a pico-net of UWB devices will hop around using one of the Time Frequency Codes (TFC) shown in Table. 2.3, allowing for three UWB devices to co-exist in the same space. Fig. 2.1 shows an example of an UWB device hopping around using the first TFC code from the Table. 2.3. There is a 9.5 ns interval between hopping from one channel to another during which the transmitter and receiver must be ready to send and receive MB-OFDM signals. After the guard interval there is a 60 ns cycle prefix and finally a 312.5 ns ODFM signal consisting of 128 subcarriers.

Due to the ultra wide-band nature of the signals present in MB-OFDM UWB devices

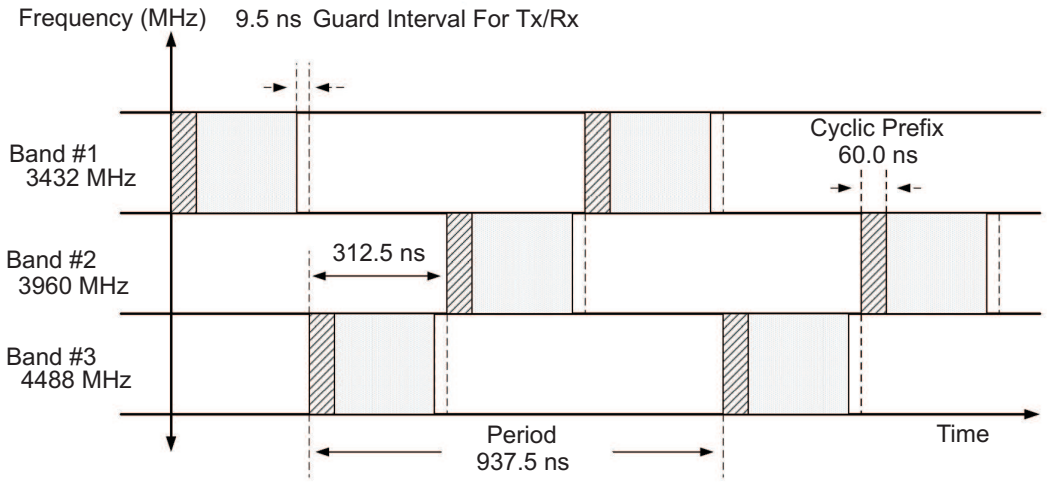

Figure 2.1: Time-frequency kernel example code used for multiple user access as well as high channel efficiency.

there are unique design challenges that are not encountered in traditional narrow-band wireless systems [9]. Traditionally, phase noise, which is a measure of signal purity is the most important design parameter for frequency synthesizers. With the tight spacing between channels the spectrum of the carrier outside of the channel bandwidth must be sufficiently attenuated. A less important design constraint is the settling time, the time required to hop from one frequency to another.

The design constraints of MB-OFDM UWB frequency synthesizers are different from those of frequency synthesizers for narrow-band RF systems. Due to the wide bandwidth of each channel (subcarrier generation is done in the digital domain), phase noise requirement is greatly relaxed. Phase noise requirement for a MB-OFDM UWB frequency synthesizer is only -105 dBc/Hz (plateau) while typical phase noise of narrow-band synthesizers is below -110 dBc/Hz at 1 MHz offset. Unlike traditional phase noise measurements that

specify the phase noise at some offset from the carrier such as 100 KHz or 1 MHz, UWB phase noise requirement is based on a plateau. This is because phase noise has a flat profile within the loop bandwidth, and MB-OFDM UWB has a large loop bandwidth. The cutoff point of a phase noise plot where the phase noise is no longer corrected by the closed loop is equal to the closed loop bandwidth of the PLL. A wide bandwidth is required for UWB synthesizers in order to have a short lock time

2.2 Lock Time and Bandwidth Requirements of UWB

MB-OFDM UWB uses spread spectrum by means of an ultra-fast frequency hopping scheme [10][11][12]. In MB-OFDM UWB there is only a 9.5 ns guard period in which the transmitter/receiver must quit transmitting in one channel and be ready to begin transmission in another. The 9.5 ns guard period places a strict constraint on the synthesizer. The setting time, which is the time required for the synthesizer to hop to one frequency, is governed by the synthesizer's 2nd order closed loop expression and is given by [13]

$$T_s = -\frac{\ln(\text{tolerance})}{\zeta\omega_n}, \tag{2.2}$$

where ζ is the damping factor, ω_n is the loop bandwidth, and tolerance is the allowed steady-state error. If we assume a 1% tolerance, a damping ratio $\frac{2}{\sqrt{2}}$, and a loop bandwidth 50 MHz, the required settling time is at least 100 ns. Eq.(2.2) shows that an increase in the loop bandwidth will decrease the settling time. One may wonder whether it is possible to increase the bandwidth until the synthesizer meets the settling time requirement. Unfortunately there is an upper limit on the bandwidth of the synthesizer that will limit the settling time to well above what is required by MB-OFDM UWB. This limit is due to a 528 MHz channel spacing mandating a maximum loop bandwidth of 52.8 MHz. Frequency

synthesizers are almost exclusively composed of charge-pump type-II PLLs that use a frequency/phase detector for a quick phase and frequency acquisition. Due to the sampling nature of the frequency/phase detector the system becomes unstable if the loop bandwidth approaches the reference frequency. Garder defined the upper limit of stability [13]

$$K\tau_2 = \frac{(\omega_c\tau_2)^2}{\pi(1 + \frac{\omega_c\tau_2}{\pi}\frac{1-a}{1+a}\frac{b-1}{b})} \tag{2.3}$$

where $a = exp(\frac{-2\pi b}{\omega_c\tau_2})$, ω_c is the reference frequency of the synthesizer, b is the ratio of the pole frequency to that of the zero frequency, and τ_2 is the time constant of the stabilizing zero added by the resistor of the loop filter. With $K = \frac{\omega_c}{10}$ the gain margin is 10 dB, resulting in a minimally stable closed-loop response of the PLL. With the reference frequency of the UWB synthesizer being 528 MHz (a 528 MHz reference frequency was chosen to allow for an integer frequency synthesizer to be used), the upper limit of the loop bandwidth is approximately 50 MHz.

The inability of narrow-band frequency synthesizers to lock in 9.5 ns sparks the search for new techniques, which include:

- A delay-locked loop with an edge combiner [14] - Instead of using a high-frequency oscillator to generate the output signal, a low frequency DLL is used and the outputs of the individual delay cells are summed by an edge combiner. By selecting how many delay cells are used in the feedback loop, the desired frequency multiplication factor can be obtained.

- A high frequency PLL with a frequency divider at the output [15] - By having a fixed frequency synthesizer with a programmable frequency divider, multiple output frequencies can be generated. The synthesizer only needs to lock to the fixed frequency at power-up, resulting in fast locking.

- Direct synthesis utilizes the frequency translation function of single side band mixing [16] [17] [18] [19] [20] [21] [22] [23] [24]. By multiplying multiple fixed frequency synthesizers the sum or difference of their output frequencies is generated. By having one of the fixed frequency synthesizers set to the middle carrier of mode-1 and the second fixed frequency synthesizer set to 528 MHz, we can generate all 3 of the mode-1 carriers. Because the fixed frequency synthesizers only need to achieve frequency and phase lock at the power-up the channel hopping of a direct synthesis frequency synthesizer has a short lock time.

2.3 Delay-Locked Loop Frequency Synthesizer

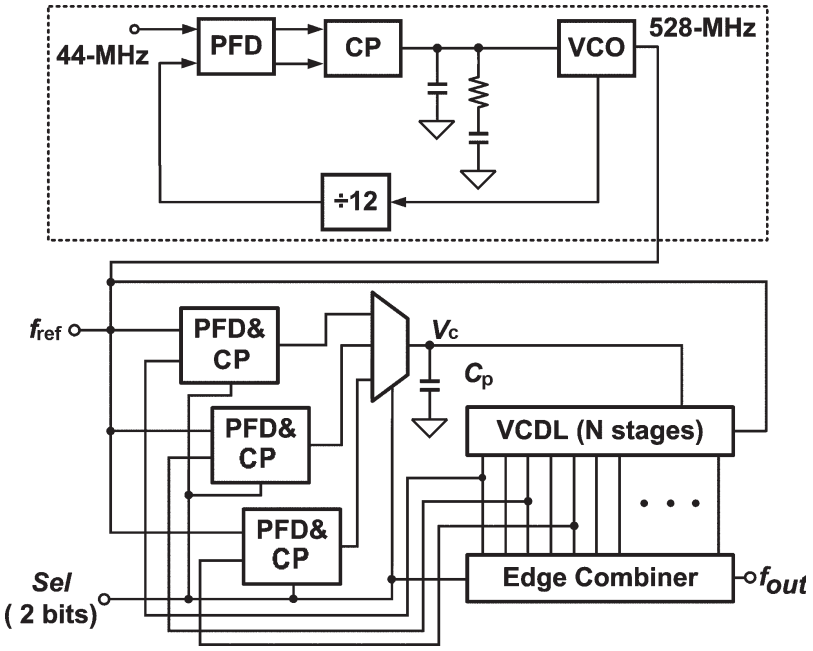

Figure 2.2: DLL based frequency synthesizer [14].

The basic DLL frequency synthesizer is shown in Fig. 2.2. It consists of a phase detector, a charge pump, a loop filter, delay line, and edge combiner. In the place of the voltage controlled oscillator in a PLL, a DLL uses a voltage controlled delay line driven by a reference oscillator. The DLL is a first-order system, yet still capable of fast locking. The short locking time makes DLL-based frequency synthesizers attractive for MB-OFDM UWB.

No frequency multiplication occurs in the loop of a DLL because the frequency of the reference oscillator is fixed and the delay line cannot alter the frequency of the signal . The multiplication of the reference frequency is obtained by using an edge combiner. When the DLL is locked the reference oscillator and the output of the delay line are shifted by 180 degrees. The 180 degree phase shift is equally divided among the delay cells of the delay line. Each delay cell has a phase shift of $\frac{\pi}{N}$, where N is the number delay cells in the delay line. When the edges of the delay cell of the DLL are combined the resulting frequency is multiplied by a factor of N. Mismatches in the delay times and layouts of the delay cells and edge combiner will cause spurs in the output spectrum and can cause ISI.

2.4 Miller Divider Based Frequency Synthesizer

The reason classical frequency synthesizers cannot lock in 9.5 ns guard period is due to a finite closed-loop bandwidth. As described previously, the closed-loop bandwidth is limited to a 10^{th} of the reference oscillator's frequency. Instead of having frequency hopping occurring inside the closed loop of the PLL, the frequency divider can be placed outside the loop therefore not requiring the PLL to re-acquire phase and frequency lock during channel hopping [25]. A classical PLL locks to a fixed frequency at the start-up. It is followed by a programmable frequency divider [15]. The architecture of the frequency synthesizer is

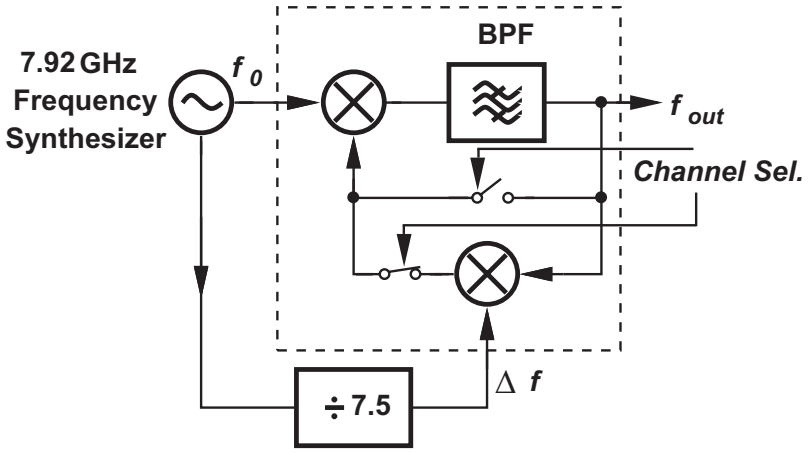

Figure 2.3: Architecture of [15] showing a fixed synthesizer and modified Miller frequency divider.

shown in Fig. 2.3. It consists of a fixed frequency synthesizer producing a 7.92 GHz reference signal, which is used to drive a divided-by-7.5 frequency divider and a programmable Miller frequency divider.

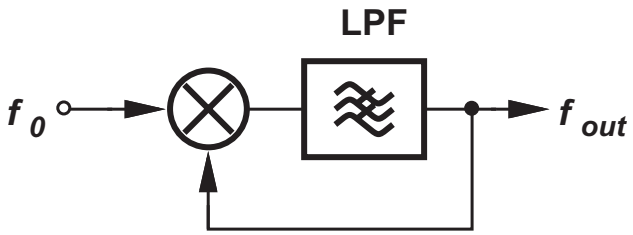

Figure 2.4: Miller frequency divider.

Miller frequency divider shown in Fig. 2.4 consists of a mixer and a bandpass filter. The mixer mixes the output of the reference oscillator with its own output. The output of the mixer is given by

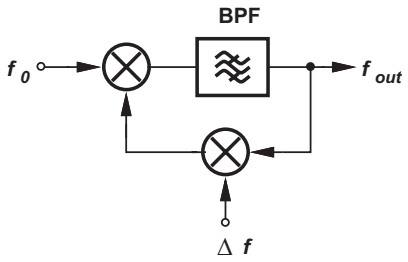

Figure 2.5: Modified Miller divider [15].

$$f_o - f_{out} = f_{out}, \quad f_{out} = \frac{f_o}{2}. \tag{2.4}$$

Eq.(2.4) shows that once the Miller divider has reached an equilibrium state, its output will be half the reference frequency. The modified Miller frequency divider presented in [15] is shown in Fig. 2.5. The feedback mixer modifies (2.4) into

$$f_o - (f_{out} \pm \Delta f) = f_{out}, \quad f_{out} = \frac{f_o}{2} \pm \frac{\Delta f}{2}. \tag{2.5}$$

By using the modified Miller frequency divider in the architecture presented in [15] the first 3 channels of UWB can be synthesized. The modification to the Miller frequency divider that allowed the additional 2 UWB channels also resulted in spurs in the output spectrum.

2.5 Direct Synthesis Frequency Synthesizers

The most common method for generating carrier signals of MB-OFDM is direct synthesis [16] [17] [18] [19] [20] [21] [22] [23] [24]. Direct synthesis modifies the output of a fixed frequency synthesizer but doesn't require a carrier twice that of the desired output

frequency. Direct synthesis falls into two categories: (i) Parallel synthesis shown in Fig. 2.6 [26] [27], and (ii) single side band mixing. For parallel synthesis no locking is required by using a separate RF path for all the required channels. The drawback of this architecture is the high silicon area and power consumption. The need for a synthesizer and a mixer in every channel is difficult for mandatory mode-1 devices and impractical for a UWB with all 14 channels.

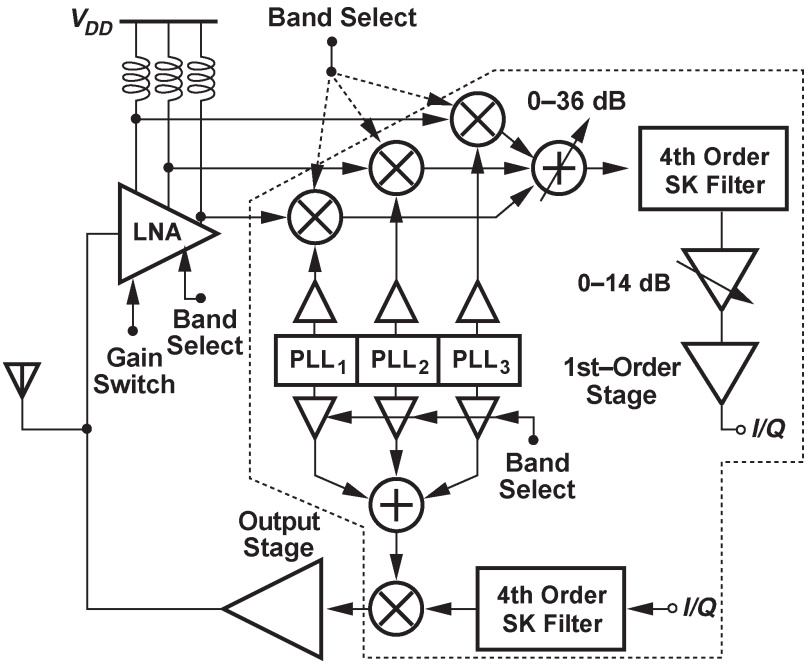

Figure 2.6: UWB receiver using multiple RF paths tuned to each of their respective bands [26].

A more common architecture for direct synthesis is by means of single side band (SSB) mixing. By using a SSB mixer a high frequency carrier can be frequency translated by the channel frequency offset of 528 MHz. An example of a SSB mixer-based frequency synthesizer is shown in Fig. 2.7.

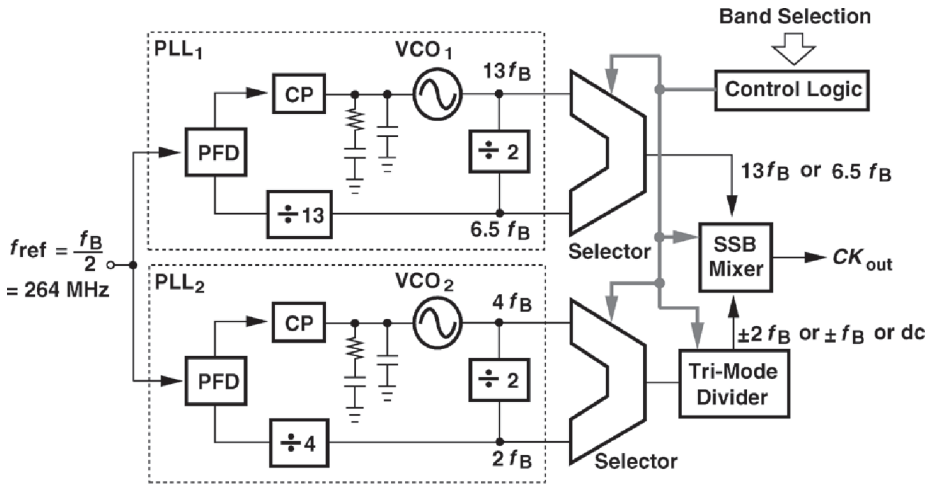

Figure 2.7: MB-OFDM frequency synthesizer based on direct synthesis [28].

While SSB allows for the creation of all 14 channels of MB-OFDM with settling time well under 1 ns, SSB mixers create sidebands located at the center of the adjacent channels that might cause ISI. These spurs are due to the non-linearities of the SSB mixer, and I/Q mismatch from the oscillators. An example of the generated spurs is shown in Fig. 2.8.

2.6 Performance Comparison

Table. 2.4 compares the performance of published MB-OFDM UWB frequency synthesizers. Several trends are observed:

- Most of the frequency synthesizers are fabricated on low cost CMOS processes, with 0.18 μm CMOS the most widely used.
- All of the MB-OFDM UWB frequency synthesizers suffer from the generation of spurs, with the largest spurs occurring directly ontop of adjacent channels. These

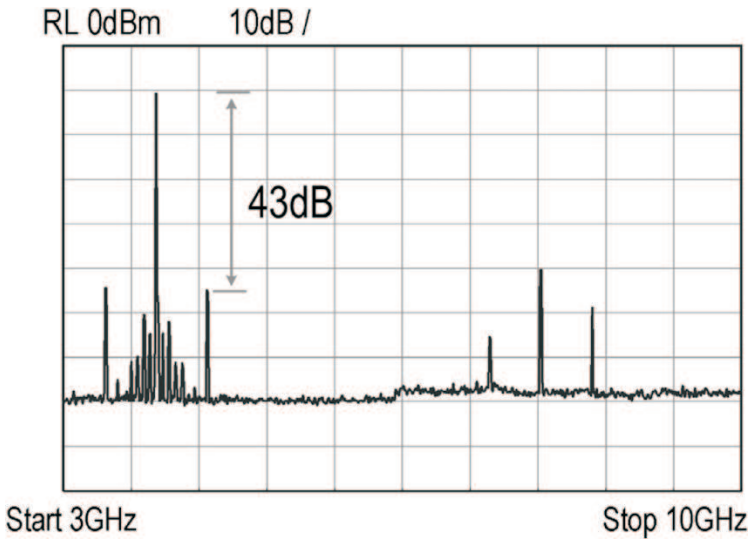

Figure 2.8: The output spectrum of [22] showing spurs

spurs are due to the open-loop architectures being used to generate the UWB carrier with lock time under 9.5 ns. These spurs will reduce the sensitivity of the receiver.

- MB-OFDM UWB frequency synthesizes have an average power consumption of 11.2 mW per channel. These power consumption figures are a result the necessity of multiple PLLs and SSB mixers, both require large power consumption for proper performance.

2.7 Chapter Summary

An overview of UWB for wireless communications has been presented. The two standards for UWB transmission namely DS-UWB and MB-OFDM have been discussed. DS-UWB uses the direct modulation of narrow pulses to represent the base-band data. It is difficult

Table 2.4: Comparison of state-of-the-art UWB frequency synthesizers.

Ref.	Technology	Lock time [ns]	Spur Level [dBc]	Phase Noise [dBc/Hz]	Total Power [mW]	Power per Band [mW]
[14]	0.18um CMOS	8	-35	-120	54	18
[15]	0.18um CMOS	4	-25	-109	47	15.6
[25]	90nm CMOS	9	-32	-120	55	3.9
[16]	0.18um CMOS	2	-40		65	16.25
[17]	0.18um CMOS	1	-37	-103	48	6.85
[19]	0.18um CMOS	2.4	-20		34	11.3
[21]	0.18um CMOS	2	-26	-98	68	22.6
[29]	0.18um SiGe	3	-40	-130	88	12.6
[28]	0.18um CMOS	1	-37	-110		
[22]	65nm CMOS	6	-43	-128	43	4.8
[23]	0.18um CMOS	3	-30		45	3.2
[24]	0.18um CMOS	3	-33	-98	117	8.3

to synchronize the transmitter and receiver. MB-OFDM uses more traditional narrow-band techniques by sub-dividing the ultra wide-band into small bands of bandwidth 528 MHz. MB-OFDM uses orthogonal frequency division multiplexing for high channel efficiency.

A state-of-the-art review of existing MB-OFDM UWB frequency synthesizers has been presented. MB-OFDM places a greater constraint on lock time and less constraint on phase noise. We have shown that the lock time is the greatest challenge for MB-OFDM UWB frequency synthesizers. A guard time of 9.5 ns requires loop bandwidth larger than that set by the stability of PLL based frequency synthesizers. The common approaches to perform frequency synthesis for MB-OFDM UWB have been investigated.

The first approach is DLL based frequency synthesis. A DLL is incapable of frequency multiplication, with the addition of an edge combiner, frequency multiplication can be performed. By controlling the number of the delay cells in the delay line a programmable DLL

based frequency synthesizer can be created. Low-frequency DLLs are able to establish a very quick lock because only phase lock is required. DLL frequency synthesizers generate spurs due to mismatching in the delay cells and edge combiner.

The second approach is the fixed frequency synthesizer with a programmable frequency divider. By having the programmable frequency divider at the output of the VCO and not in the VCO feedback loop phase and frequency lock only needs to be established during power-up. The modification of the miller frequency divider also results in spurs at the output of the divider.

The third and also most common frequency synthesis for MB-OFDM UWB is direct synthesis. There are two approaches for direct synthesis, namely parallel synthesis and SSB mixing. Parallel synthesis requires the generation of all UWB channels using multiple frequency synthesizers, resulting in a large silicon area and high power consumption. SSB mixing is the most common approach for MB-OFDM frequency synthesis. It suffers from spur generation due to the use of SSB mixing of multiple fixed frequency synthesizers.

It is evident that existing MB-OFDM UWB frequency synthesizers suffer from the generation of spurs due to the use of open loop architectures. Direct synthesis frequency synthesizers suffer from high power consumption due to the use of multiple frequency synthesizers and single side band mixers.

Chapter 3

Current-Mode Phase Locked Loops

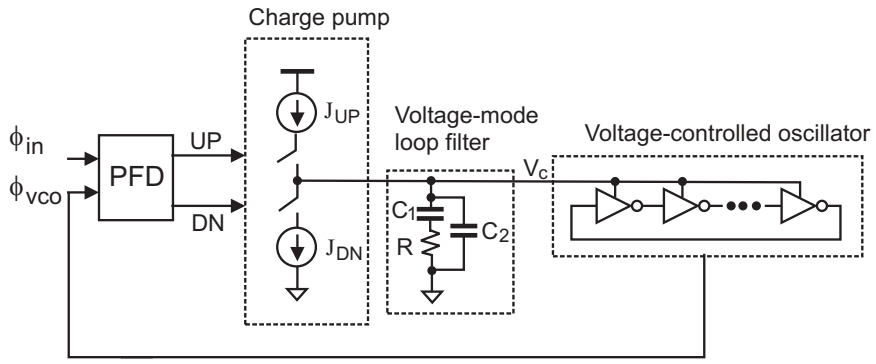

Figure 3.1: Configuration of type II voltage-mode PLLs.

A typical configuration of conventional type II PLLs is shown in Fig. 3.1. We shall term these PLLs voltage-mode PLLs as the oscillation frequency of the oscillator is voltage-controlled. Many new topologies of and design techniques for voltage-mode PLL, such as supply-regulated PLLs [30], PLLs with dual-slope phase-frequency detectors [31], PLLs

with frequency tracing circuits [32], [33], PLLs with adaptive loop dynamics for fast locking [34], a half-duty sampled feed-forward loop filter for reference spur suppression [35], calibrated phase/frequency detectors [36], and glitch-free charge pumps [37], to name a few, emerged. One of the main drawbacks of voltage-mode PLLs is the limited dynamic range of the control voltage. The current-mode PLLs proposed in this chapter and shown in Fig. 3.2 replaces the conventional voltage-mode RC loop filter with a current-mode RL loop filter. Using current as a control signal the dynamic range of the control signal is no longer limited by the supply voltage. The magnitude of the control signal is not limited by the output of the active inductor gyrators.

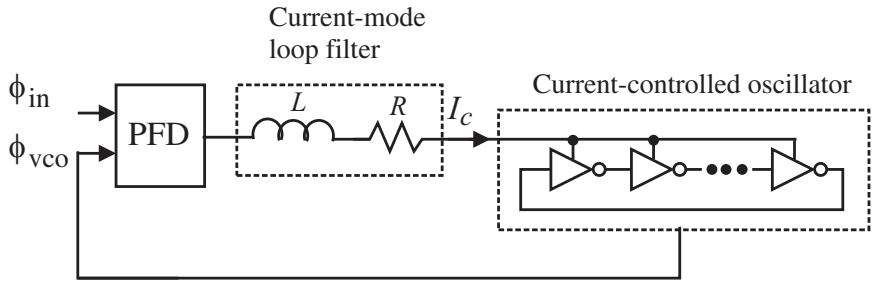

Figure 3.2: Configuration of current-mode phase-locked loops.

Section 1 of this chapter introduces modern techniques for battling the problem of supply scaling in voltage-mode PLLs. Section 2 introduces the concept of current-mode filtering that will be used to replace voltage-mode filtering. The inductance of the current-mode filter will be implemented using active inductors. A detailed analysis of active inductors will follow. Current-controlled oscillators are studied in Section 3. Section 4 develops closed-loop expressions for current-mode PLLs. The phase noise of current-mode PLLs is investigated in Section 5. Section 6 provides the simulation results of an active inductor based current-mode PLL. The chapter is summarized in Section 7.

3.1 Low-Voltage Voltage-Mode PLLs

The different scaling factors of the supply and threshold voltages reduces the control voltage range. The noise present on the control signal remains unchanged. To compensate for the drop of supply voltage, VCO sensitivity has to increase in order to maintain the same frequency tuning range. The increase in VCO gain makes the VCO more susceptible to noise. Two techniques for combating the reduction of the dynamic range of the control signal are supply regulated PLLs [38, 39, 40, 41, 42, 43] and differentially tuned PLLs [44, 45, 46, 47].

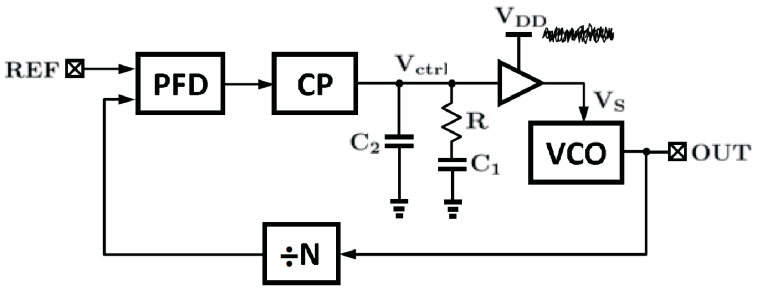

Figure 3.3: Configuration of a supply regulated PLL.

A supply regulated PLL is shown in Fig. 3.3. The VCO's supply voltage is a buffered replica of the control signal. By using the control signal as the VCO's supply voltage the VCO is decoupled from the noisy VDD of the system. Using a regulator to supply the VCO limits the topology of the VCO to ring oscillators. One of the challanges in the design of a supply regulated PLL is highlighted in Fig. 3.4. The regulator consists of an op-amp and a large pMOS M_p. A large decoupling capacitor C_d is usually added to filter the VDD of the VCO. The addition of the decoupling capacitor and large pMOS creates two poles ω_a and ω_o. Both poles ω_a and ω_o must be an order of magnitude higher than the loop bandwidth of

the PLL. If the bandwidth of the regulator is not sufficiently higher than the loop bandwidth they will degrade the phase margin. To have ω_o higher than the loop bandwidth and still effectively filter the VDD of the VCO, an op-amp is required.

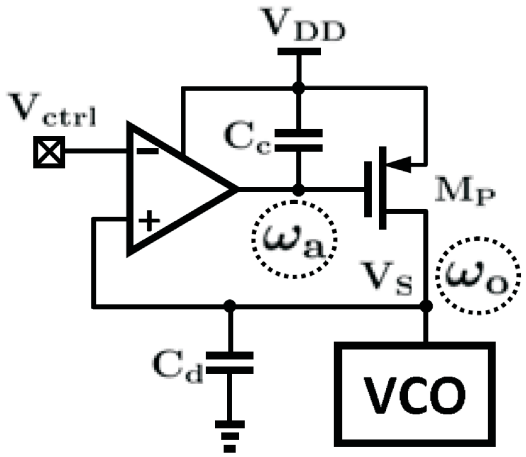

Figure 3.4: Configuration of a supply regulated VCO.

A differentially tuned PLL is shown in Fig. 3.5. The differentially tuned PLL uses a differential control signal. By having a differential control signal the dynamic range is effectively doubled. To generate the differential control signal the PLL must have two PFDs and two charge pumps, and a differential loop filter, doubling power and silicon consumption. Having two charge pumps also creates a problem of matching, a mismatch between the two charge pumps generates considerable spurs in differentially tuned PLLs. Another challenge with a differentially tuned PLL is that the VCO must be differentially tuned, requiring a unique VCO topology.

Supply regulated PLLs are not suitable for UWB frequency synthesizers due to power consumption. The large loop bandwidth of a UWB frequency synthesizer will require a high powered op-amp with an output pole of tens of gigahertz. Differentially tuned PLLs

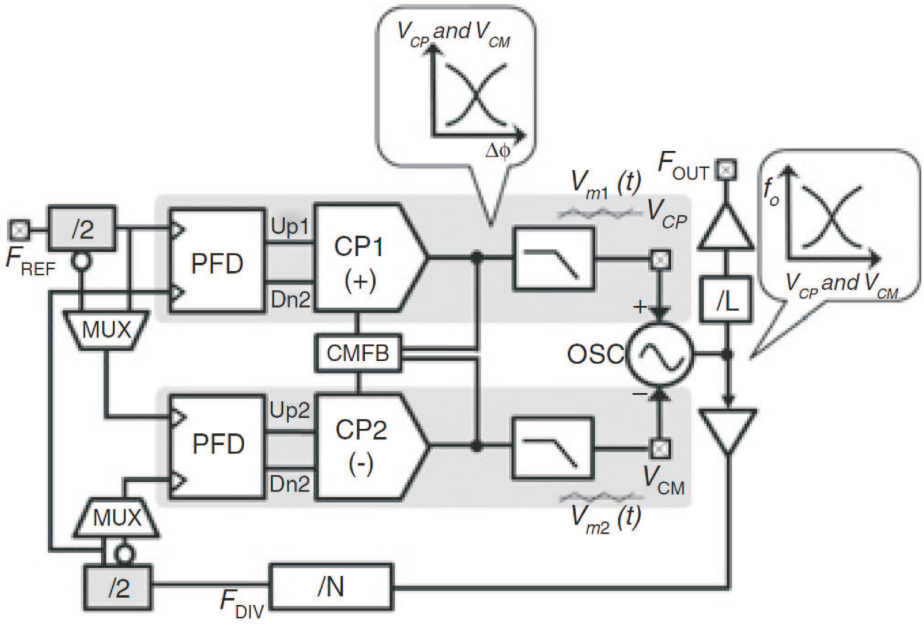

Figure 3.5: Configuration of a differentially tuned PLL.

are also not suitable for UWB frequency synthesizers. This chapter explores current-mode techniques for frequency synthesizers.

3.2 Current-Mode Filtering

3.2.1 Current-Mode Loop Filter

Current-mode filtering is widely used in power electronics for dc-dc conversion where a constant output current is required. Current-mode filtering differs fundamentally from voltage-mode filtering where sustaining a constant output voltage is the objective. A typical current-mode low-pass filter consists of an inductor and a resistor in series, as shown in Fig. 3.6. Let the input voltage source $v_{in}(t)$ be a square-wave generator with amplitude V_m and

duty cycle t_{on}/T, where T is the period and t_{on} is the ON time. The inductor current is given by

$$i_L(t) = \begin{cases} \frac{V_m}{R}(1 - e^{-t/\tau}) + i_L(0^-)e^{-t/\tau}, & 0 \leq t \leq t_{on}, \\ i_L(t_{on}^-)e^{-(t-t_{on})/\tau}, & t_{on} \leq t \leq T, \end{cases} \tag{3.1}$$

where $\tau = \frac{L}{R}$ is the time constant, $i_L(0^-)$ and $i_L(t_{on}^-)$ are the initial current of the inductor at $t = 0$ and $t = t_{on}$, respectively. If τ is sufficiently large, we have $e^{-\frac{t}{\tau}} \approx 1 - \frac{t}{\tau}$ and (3.1) is simplified to

$$i_L(t) \approx \begin{cases} \frac{V_m}{R}\frac{t}{\tau} + i_L(0^-)(1 - \frac{t}{\tau}), & 0 \leq t \leq t_{on}, \\ i_L(t_{on}^-)(1 - \frac{t-t_{on}}{\tau}), & t_{on} \leq t \leq T. \end{cases} \tag{3.2}$$

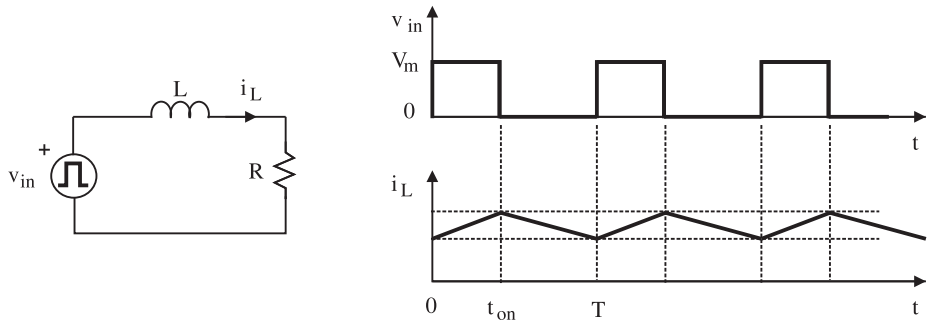

Figure 3.6: Characteristics of current-mode loop filter.

For fixed V_m, the dc component of the inductor current is a function of the duty cycle.

3.2.2 Gyrator-C Floating Active Inductors

Active inductors synthesized using active devices offer the advantages of a large and tunable inductance and virtually no silicon area requirement over their spiral counterparts [48, 49, 50, 51]. Two back-to-back connected transconductors, known as gyrators, with one port terminated with a capacitive load, as shown in Fig. 3.7(a), exhibit an inductive characteristic at the other port. In the ideal case where the input impedance of the transconductors is infinite, the admittance looking into port 1 of the gyrator is given by

$$Y(s) = sC_2 + G_{o2} + \frac{1}{s\left(\frac{C_1}{g_{m1}g_{m2}}\right) + \frac{G_{o1}}{g_{m1}g_{m2}}}. \tag{3.3}$$

Eq.(3.3) can be represented equivalently by the RLC network shown in Fig.3.7 with

$$R_p = \tfrac{1}{G_{o2}}, \quad R_s = \tfrac{G_{o1}}{g_{m1}g_{m2}}, \quad C_p = C_2, \quad L = \tfrac{C_1}{g_{m1}g_{m2}}. \tag{3.4}$$

To find out the effective frequency range over which the gyrator is inductive, we examine the impedance of the inductor:

$$Z(s) = \left(\frac{R_s}{C_pL}\right)\frac{s\frac{L}{R_s} + 1}{s^2 + s\left(\frac{1}{R_pC_p} + \frac{R_s}{L}\right) + \frac{R_p+R_s}{R_pC_pL}}. \tag{3.5}$$

When complex conjugate poles are encountered, the impedance has its resonant frequency $\omega_o \approx \sqrt{\frac{1}{LC_p}} = \sqrt{\omega_{t1}\omega_{t2}}$, where $R_p \gg R_s$ was utilized and $\omega_{t1,2} = \frac{g_{m1,2}}{C_{1,2}}$ is the cut-off frequency of the transconductors. Observe that $Z(s)$ has a zero at the frequency $\omega_z = \frac{R_s}{L} = \frac{G_{o1}}{C_1}$. The Bodé plots of $Z(j\omega)$ are sketched in Fig. 3.7(b). It is evident that the gyrator is resistive when $\omega < \omega_z$, inductive when $\omega_z < \omega < \omega_o$, and capacitive when $\omega > \omega_o$.

Fig.3.8 shows the inductance of the active inductor measured at 3 GHz with the dc voltage of the input node of the active inductor swept. Most published work on active

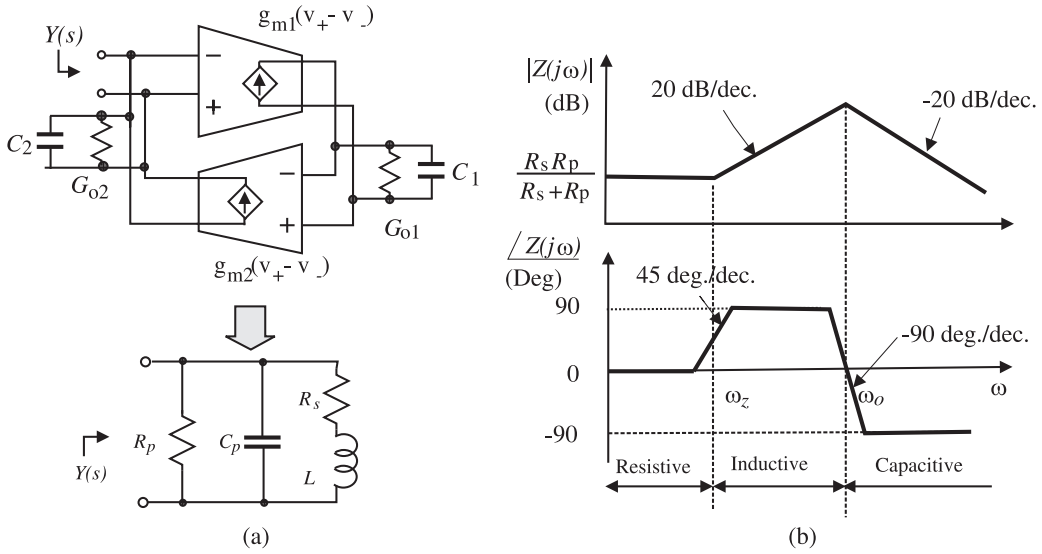

Figure 3.7: (a) Configuration of floating gyrator-C active inductors. G_{o1} and C_1 are the output conductance of transconductor 1 and the input capacitance of transconductor 2, respectively. (b) Bodé plots of gyrator-C active inductors.

inductors assumes that the transistors of the two transconductors are in saturation. When the devices are biased near the pinch-off, g_m is reduced. Further, when the devices are in the triode, they behave as a conductor with its nearly constant conductance $g_{ds} < g_m$. The preceding analysis reveals that even when the transistors of the active inductors enter the triode region, they still behave as an inductor, except with a larger inductance. It should also be noted that although the output voltage of the preceding phase detector could be rail-to-rail swing, the resistor preceding the active inductor in the loop filter and the gate capacitance of the transistors forming the active inductor limit the swing of the voltage at the input of the active inductor to a rather small range.

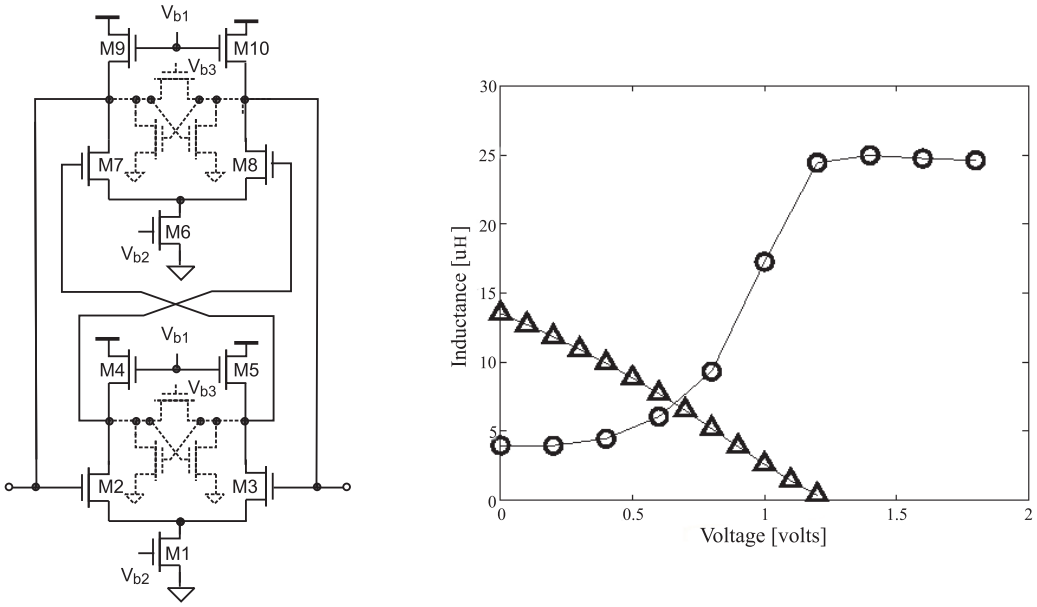

Figure 3.8: Fully differential gyrator-C active inductor circuit. Circuit parameters : $W_{1,6} = 5\mu m$, $W_{2,3,7,8} = 0.5\mu m$, $W_{4,5} = 100\mu m$, and $W_{9,10} = 0.5\mu m$. $L = 0.18\mu m$ for all transistors. ◯ - Dependency of the inductance of the floating active inductor on the biasing voltage V_{b2} at 3 GHz. △ - Large-signal behavior of the floating active inductor at 3 GHz.

3.3 Current-Controlled Oscillator

Unlike voltage-mode phase-locked loops, the phase/frequency adjustment of current-mode phase-locked loop is achieved by a current-controlled oscillator with its control signal being the output current of the preceding current-mode loop filter. The schematic of a CCO is shown in Fig. 3.9a. It is an LC-tank oscillator with active inductors proposed by Ismail et al. in [52, 53, 54]. The tuning of the self-resonant frequency of the tank is achieved by tuning the bias current of $M_{3,6}$. $M_{7,8}$ form the trans-impedance amplifier that converts the

control current I_c to a control voltage. The use of M_8 is to reduce the capacitance seen by I_c. Without M_8, a large capacitance will exist at the input of the CCO. This capacitance will form an LC network with the large inductor of the preceding current-mode loop filter. The low resonant frequency of the LC network given by $\omega_o = \sqrt{\frac{1}{LC}}$ results in low-frequency ripples on the control line of the CCO. These low-frequency ripples are then up-converted to the high-frequency carrier output of the CCO, resulting in systematic phase noise. Fig. 3.9b shows the frequency tuning range of the current-controlled oscillator.

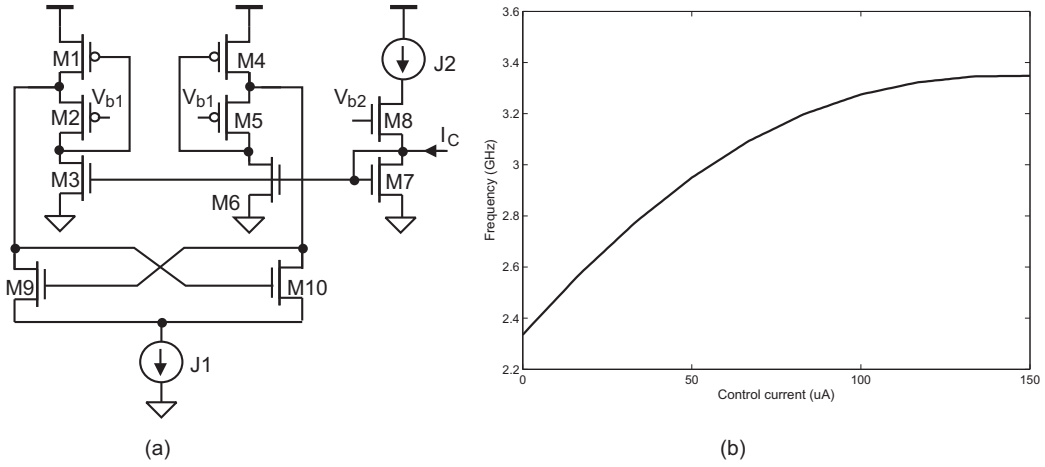

Figure 3.9: (a) Current-controlled oscillator with current reuse active inductors. Circuit parameters : $W_1 = 10\mu$m,$W_2 = 3\mu$m, $W_{3\sim4} = 10\mu$m,$W_{5\sim6} = 5\mu$m,$W_7 = 5\mu$m,$I_b = 1$ mA,$I_{b2} = 100\mu$A,$V_b = 1$ V,$V_{b2} = 0.2$ V. (b) Frequency tuning range of the current-controlled oscillator

3.3.1 Replica Bias for Active Inductor VCOs

One of the major disadvantages of using active circuits to synthesize the behavior of passive components is the voltage dependency of the transconductance on the supply voltage. To

reduce the effect of this dependency, a technique known as replica bias was employed in design of the loop filter [55]. The replica bias circuit applied to the active loop filter is shown in Fig.3.10. The active loop filter is formed by M_{1-10}, the half replica is formed by M_{11-13} and the op-amp is realized by M_{14-18}.

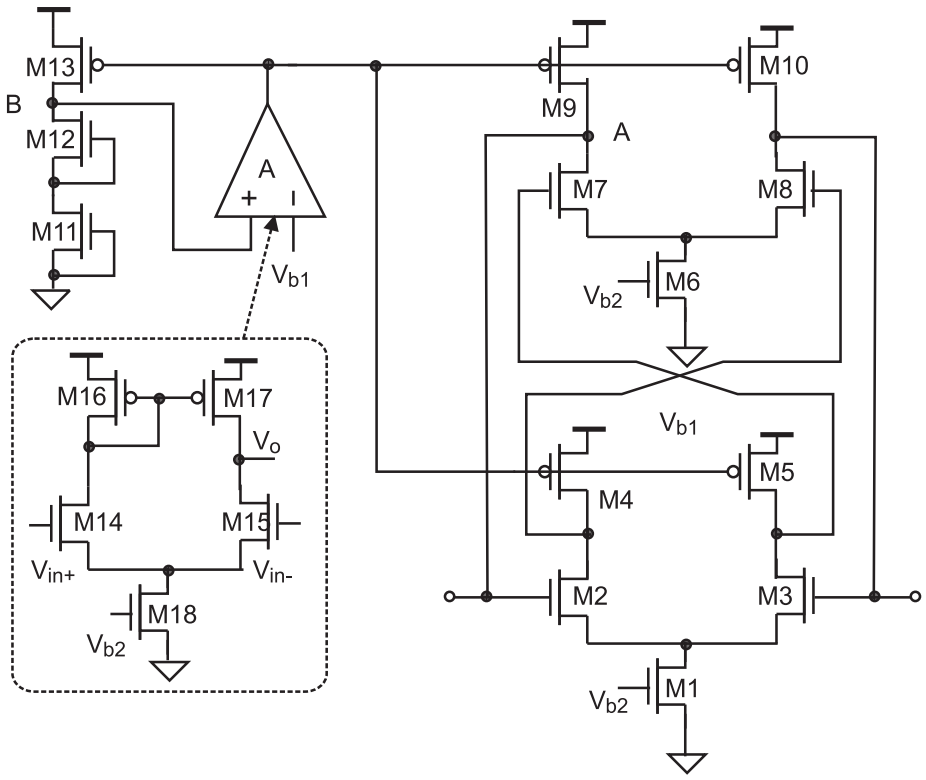

Figure 3.10: Fully differential gyrator-C active inductor with replica biasing.

The half replica circuit replicates the DC bias condition of the circuit to be used as a reference to minimize the effect of V_{DD} fluctuation on the circuit. With the replica circuit being equally affected by V_{DD} fluctuation V_{gs} of the load transistors is the same. By comparing V_{gs} to the reference voltage the error can be used to adjust the bias so as to maintain

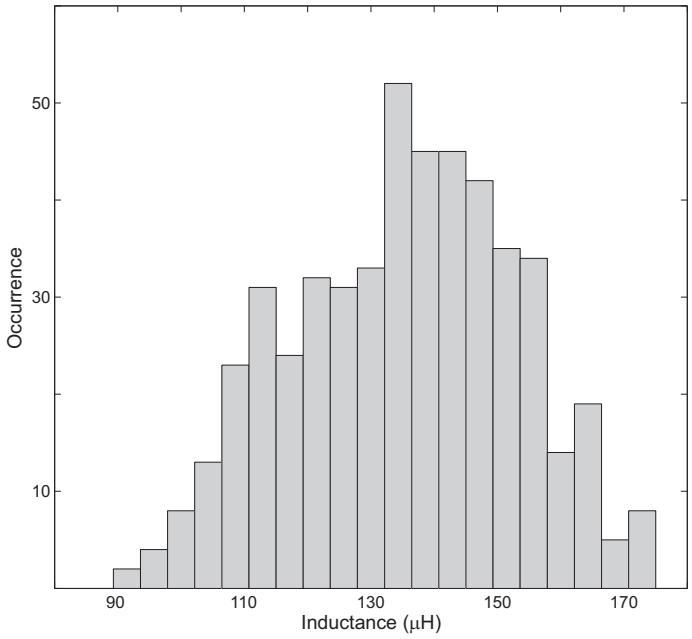

Figure 3.11: Distribution of the inductance of the active inductor without replica biasing due to process variations (500 samples in Monte Carlo simulation)

a constant V_{gs}. The constant V_{gs} maintains a constant load, a constant gain, subsequently a constant inductance.

Table 3.1 compares the effect of the fluctuation of the supply voltage on the inductance of the active inductor with and without replica biasing. It is seen that the inductance of the active inductor without replica biasing is sensitive to V_{DD} fluctuation with a sensitivity of 0.167 nH/mV. It is reduced to 0.0235 nH/mV when replica biasing is used. The effect of process spread on the inductance of the active inductor is investigated using Monte Carlo simulation. The non-replica bias and replica bias inductances are shown in Fig.3.11 and 3.12 respectively. It is clear that the replica bias gives a more constant inductance. It is seen that a large degree of the spread of the inductance of the active inductor without replica

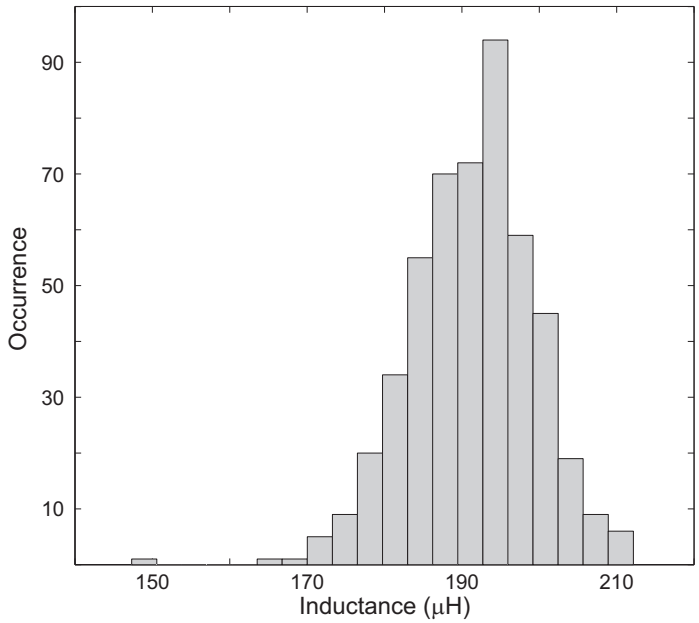

Figure 3.12: Distribution of the inductance of the active inductor with replica biasing due to process variations (500 samples in Monte Carlo simulation)

biasing exists. When replica biasing is employed, the feedback mechanism significantly reduces the effect of process spread on the spread of the inductance of the active inductors.

3.4 Loop Dynamics of Active-Inductor based Current-Mode PLL

Fig.3.13 shows the basic configurations of current-mode loop filters for types I and II current-mode PLLs. In the vicinity of the lock state, because the phase variation is small, PLLs can be considered as linear systems and conventional s-domain approaches can be used to analyze PLLs.

Table 3.1: Effect of V_{DD} fluctuation on the inductance of active inductors with and without replica biasing.

V_{DD} (V)	Inductance with replica (nH)	Inductance without replica (nH)
1.70	193.2	154.2
1.74	193.7	146.6
1.78	192.8	139.6
1.82	191.4	133.4
1.86	189.8	126.9
1.90	188.5	120.7

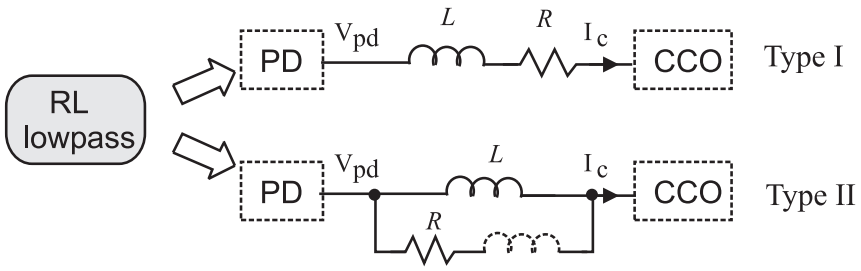

Figure 3.13: Current-mode filters for type I and type II current-mode PLLs.

3.4.1 Type I Current-Mode PLLs

Consider type I current-mode PLLs shown in Fig.3.14. Let us neglect the series resistor R for the time being. The closed-loop transfer function of the PLL is given

$$H_c(s) = \frac{\Phi_o(s)}{\Phi_{in}(s)} = \frac{K_{pd}K_{cco}}{L}\frac{1}{s^2 + \frac{K_{pd}K_{cco}}{L}}, \tag{3.6}$$

where K_{pd} and K_{cco} are the gain of the phase detector and that of CCO, respectively. It is

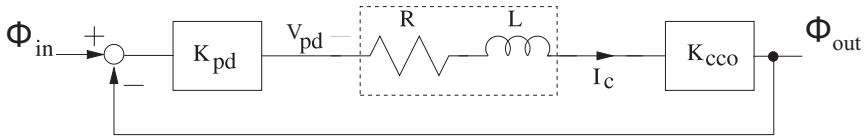

Figure 3.14: Phase diagram for type I current-mode PLLs.

seen that the system has two purely imaginary poles and is, therefore, marginally stable. To stabilize the system, a resistor can be added in series with the inductor. The closed-loop transfer function becomes

$$H_c(s) = \frac{K_{pd}K_{cco}}{L}\frac{1}{s^2 + s\frac{R}{L} + \frac{K_{pd}K_{cco}}{L}}. \tag{3.7}$$

The added resistor moves the poles from the imaginary axis to the left half of s-plane and stabilize the PLL. The system is now a Type I PLL. The loop bandwidth ω_n and damping factor ξ are given by $\omega_n = \sqrt{\frac{K_{pd}K_{cco}}{L}}$ and $\xi = \sqrt{\frac{R^2}{4K_{pd}K_{cco}L}}$. The damping factor ξ can be tuned by varying R without affecting the loop bandwidth.

3.4.2 Type II Current-Mode PLLs

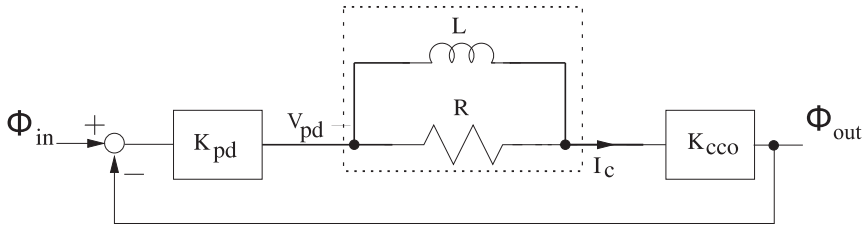

Figure 3.15: Phase diagram for type II current-mode PLLs.

The loop can also be stabilized by adding a resistor in parallel with the inductor, as shown in Fig. 3.15. The closed-loop transfer function in this case is given by

$$H_c(s) = \frac{K_{pd}K_{cco}}{RL}\frac{sL+R}{s^2 + s\frac{K_{pd}K_{cco}}{R} + \frac{K_{pd}K_{cco}}{L}}. \tag{3.8}$$

The system is now a type II PLL with loop bandwidth ω_n and damping factor ξ given by $\omega_n = \sqrt{\frac{K_{pd}K_{cco}}{L}}$ and $\xi = \sqrt{\frac{K_{pd}K_{cco}L}{4R^2}}$. It should be noted that the resistor R provides a direct path for high-frequency disturbances from the phase detector to bypass the loop-filtering inductor, deteriorating the phase noise. To eliminate this drawback, an inductor with a small inductance (L_1) can be added in series with the resistor as to block high-frequency ripple currents passing through the resistor shown in Fig. 3.16. It is evident that these configurations bear a strong resemblance to their voltage-mode counterparts.

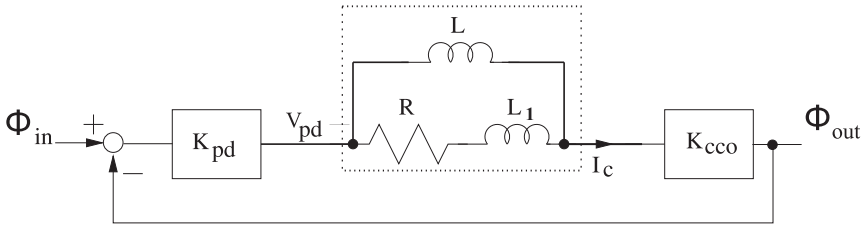

Figure 3.16: Phase diagram for type II current-mode PLLs with additional inductor.

3.4.3 Non-ideal Cases

As shown earlier that active inductors have parasitics (R_p, R_s, C_p). In this section, we investigate the effect of these parasitics on the loop dynamics of current-mode PLLs. Consider type I current-mode PLLs first. Because typically $R_p \gg R$ and $R \gg R_s$ hold, R_s can be neglected. It can be shown that the phase transfer function with C_p neglected is given by

$$H_c(s) = \frac{K_{pd}K_{cco}}{LR_p}\frac{sL + R_p}{s^2 + s(\frac{R}{L} + \frac{K_{pd}K_{cco}}{R_p}) + \frac{K_{pd}K_{cco}}{L}}. \tag{3.9}$$

The loop bandwidth and the damping factor are given by

$$\omega_n = \sqrt{\frac{K_{pd}K_{cco}}{L}}\sqrt{\frac{R_p}{R_p + R}}, \tag{3.10}$$

$$\xi = \frac{R}{2}\sqrt{\frac{1}{K_{pd}K_{cco}L}} + \frac{1}{2R_p}\sqrt{K_{pd}K_{cco}L}. \tag{3.11}$$

The loop bandwidth is approximately the same as that of the ideal case and the damping factor is increased slightly. When C_p is considered, because it is in parallel with R_p, the phase transfer function in this case is given by (3.9) with R_p replaced with $Z_p = R_p||\frac{1}{sC_p}$. The results of both the loop bandwidth and damping factors remain nearly the same as the case when C_p is neglected. Let us now consider type II cases. Neglect R_p as $R_p \gg R$. The phase transfer function when C_p is neglected is given by

$$H_c(s) = \frac{K_{pd}K_{cco}}{LR_p}\frac{sL + (R + R_s)}{s^2 + s(\frac{R_s}{L} + \frac{K_{pd}K_{cco}}{R}) + \frac{K_{pd}K_{cco}}{L}(1 + \frac{R_s}{R})}. \tag{3.12}$$

The loop bandwidth and the damping factor are given by

$$\omega_n = \sqrt{\frac{K_{pd}K_{cco}}{L}}\sqrt{1 + \frac{R_s}{R}}, \tag{3.13}$$

$$\xi = \frac{R}{2}\sqrt{\frac{1}{K_{pd}K_{cco}L}} + \frac{1}{2}\sqrt{\frac{LK_{pd}K_{cco}}{R^2}}. \tag{3.14}$$

It is seen that the bandwidth remains approximately unchanged and the damping factor is increased slightly. When C_p is considered, it can be shown that both the loop bandwidth

and damping factors remain nearly unchanged.

3.5 Phase Noise of Current-Mode Active Inductor PLLs

To analyze the phase noise of the current-mode PLLs in the lock state, consider the type I current-mode PLL of Fig. 3.17 where the noise from the input, the noise of the active loop filter and that of the CCO are considered. The phase noise at the output of the PLL is given by

$$N_o(s) = \frac{s(sL+R)}{\Delta} N_{cco}(s) + \frac{K_{pd}K_{cco}}{\Delta} N_{in}(s) + \frac{K_{cco}}{\Delta} N_{LP}(s),$$

where $\Delta = s^2L + sR + K_{pd}K_{cco}$. It is seen that noise from the input and that from the loop filter to the output of the PLL have a low-pass characteristic whereas that from the CCO to the output of the PLL has a band-pass characteristic. These noise transfer characteristics bear a strong resemblance to those of voltage-mode PLLs. The phase noise of type II current-mode PLLs can be analyzed in a similar way.

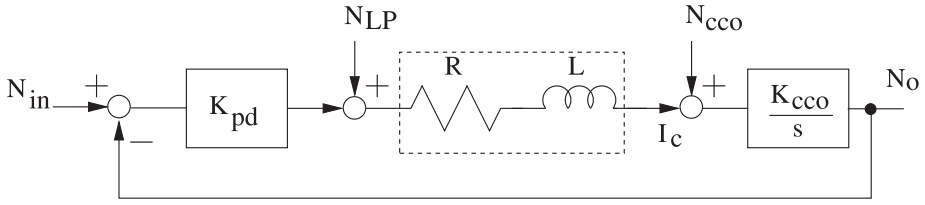

Figure 3.17: Phase noise analysis of Type I current-mode PLLs in the lock state.

3.6 Simulation Results of Active-Inductor Current-mode PLL

A current-mode PLL has been implemented in TSMC-0.18μm 1.8V 6-metal 1-poly CMOS technology and analyzed using SpectreRF from Cadence Design Systems with BIM3.3v device models. The simplified schematic of the PLL is shown in Fig. 3.18. A differential voltage buffer is inserted between the CCO and phase detector to restore the voltage swing. The PLL is designed to operate at 3 GHz. The current-mode loop filter consists of a 3 μH active inductor with an output current capability exceeding the required 46 μA to achieve lock. Each side of the inductor is connected to a 2.25 kΩ poly resistor. The parasitic series resistance of the active inductor R_s whose value is usually much smaller than 2.25k Ω has a negligible impact on the loop dynamics of the PLL. The parasitic parallel resistor R_p and capacitor C_p of the synthesized inductor, however, provide direct paths from the phase detector to the CCO for high-frequency disturbances to bypass the loop filter, deteriorating the phase noise of the PLL. The layout of the PLL is shown in Fig. 3.19.

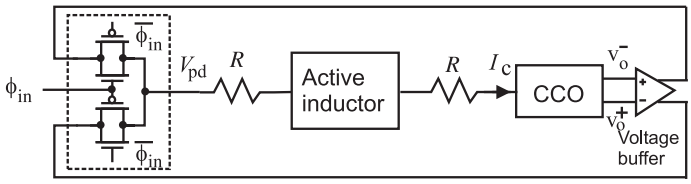

Figure 3.18: Simplified schematic of the proposed current-mode PLL.

Fig. 3.20 shows the output current of the current-mode loop filter with various duty cycles of the input voltage. It is seen that the dc component of the output current of the loop filter varies with the duty cycle of the input voltage. Fig. 3.21 shows the effect of the fluctuation of the supply voltage on the cut-off frequency of the loop filter. It is seen that the cut-off frequency is sensitive to V_{DD} fluctuation, calling for replica biasing. This differs from RL loop filters employing spiral inductors whose cut-off frequency is independent of supply voltage fluctuation. Fig. 3.22 compares

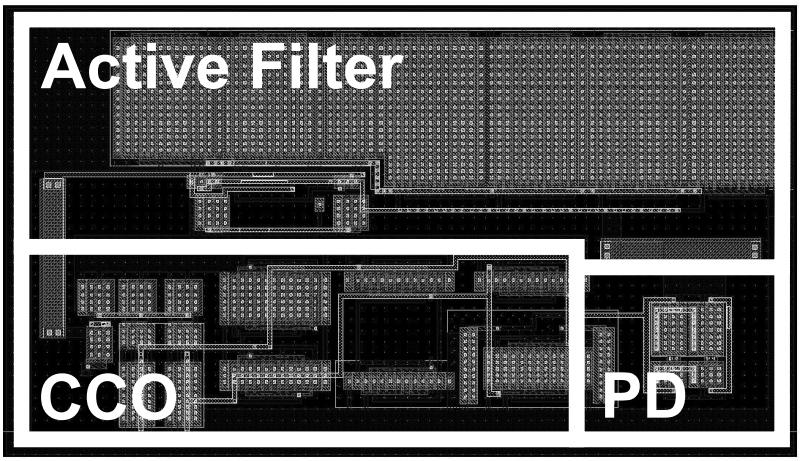

Figure 3.19: Layout of the proposed current-mode PLL.

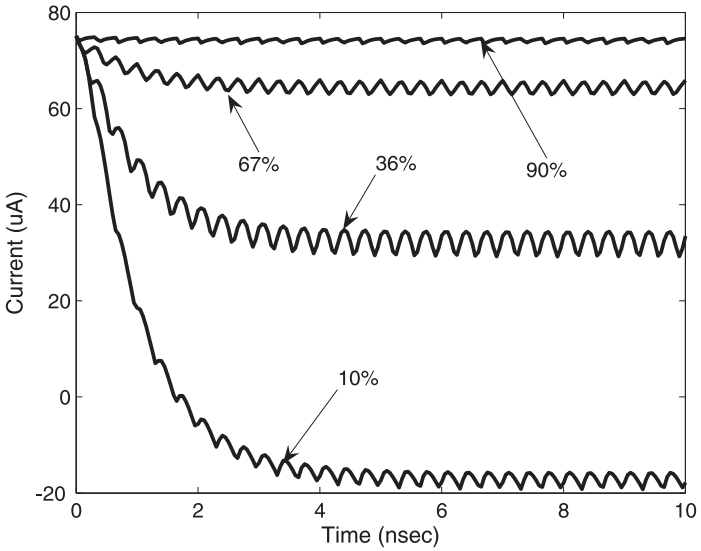

Figure 3.20: Dependence of the output current of current-mode loop filter on the duty cycle of the input voltage (post-layout).

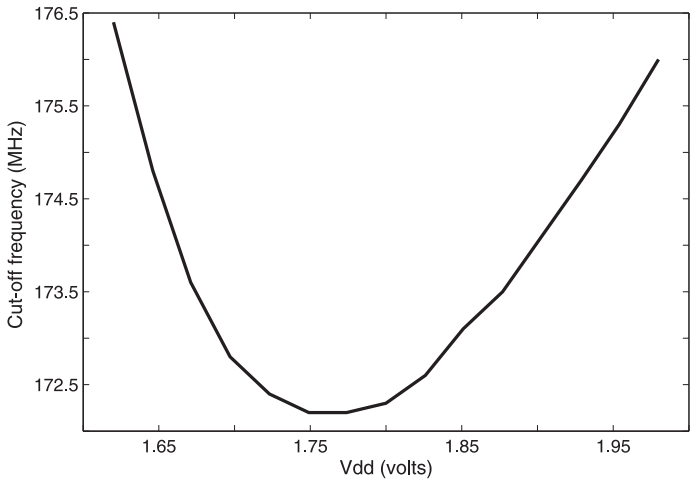

Figure 3.21: Effect of the fluctuation of supply voltage on the cut-off frequency of the current-mode loop filter (post-layout).

the effect of V_{DD} fluctuation on the oscillation frequency of CCOs with (i) passive inductors and (ii) active inductors. It is observed that LC-tank CCOs with active inductors are more sensitive to V_{DD} fluctuation, revealing that the minimization of switching noise is critical to the operation of active inductor-based LC-tank CCOs. Fig. 3.23 plots the control current of the current-mode PLL. The PLL reaches the lock state in 50 ns approximately. The phase noise plot is shown in Fig. 3.24. The phase noise of the PLL is -84.5 dBc at 1 MHz frequency offset and -70 dBc reference spurs at 125 MHz. The effect of process variations on the performance of the proposed PLL is investigated using corner analysis and the results are tabulated in Table 3.2. Fig. 3.25 shows the effect of V_{DD} fluctuations on the phase noise of the proposed current-mode PLL. The power consumption of the phase detector, the current-mode loop filter, and the CCO are 90.5 μW, 100.1 μW, 12.2 mW, respectively. The power consumption of the current-mode loop filter is negligible, mainly due to its small dc biasing current required for obtaining a large inductance. The layout area of the PLL is 2800 μm^2.

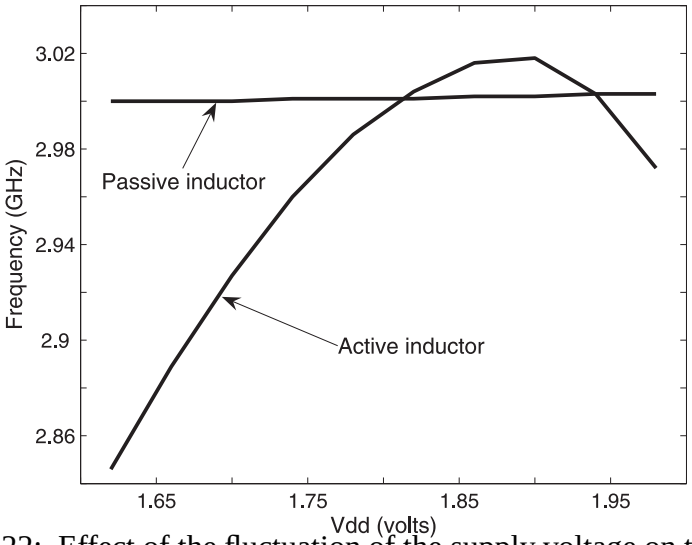

Figure 3.22: Effect of the fluctuation of the supply voltage on the oscillation frequency of CCO (post-layout).

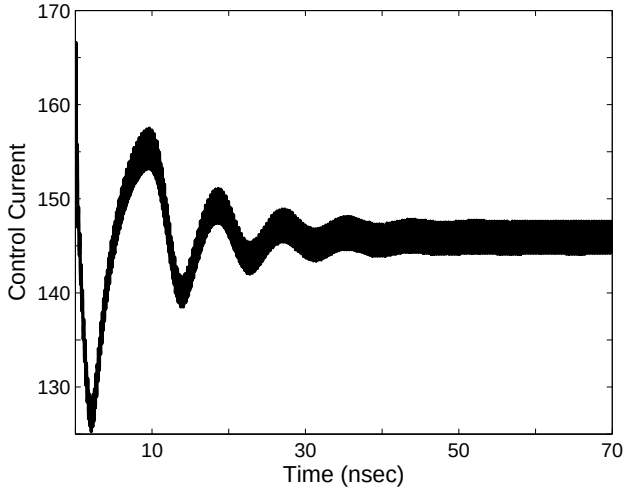

Figure 3.23: Control current of the proposed current-mode PLL (post-layout).

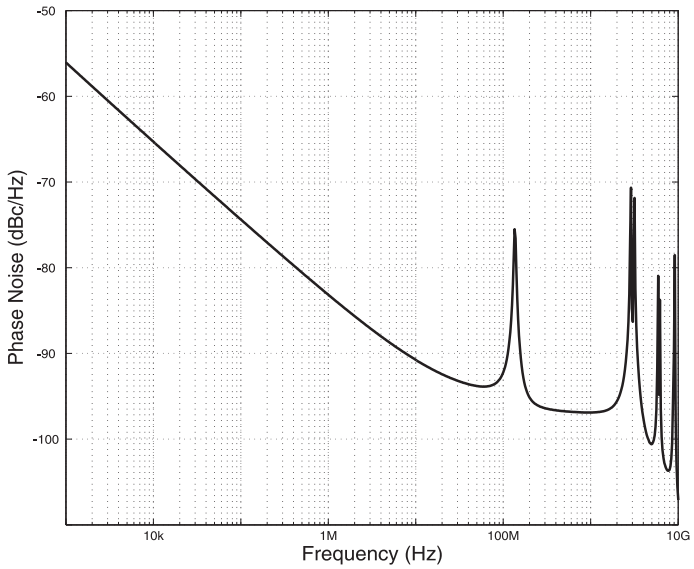

Figure 3.24: Simulated Phase noise of the proposed current-mode PLL (post-layout).

Table 3.2: Corner analysis results of the PLL (post-layout).

Process corner	Phase noise at 1MHz frequency offset (dBc)	Loop bandwidth (MHz)	Lock time (nsec)
TT	-84.5	125	50
FF	-76.5	220	63
SS	-93	117	116
FS	-90.8	140	46
SF	-72.9	85	150

3.7 Chapter Summary

An in-depth examination of the principle of current-mode filtering and its application to PLLs have been presented. Current-mode PLLs use currents as control signals. By using currents as control

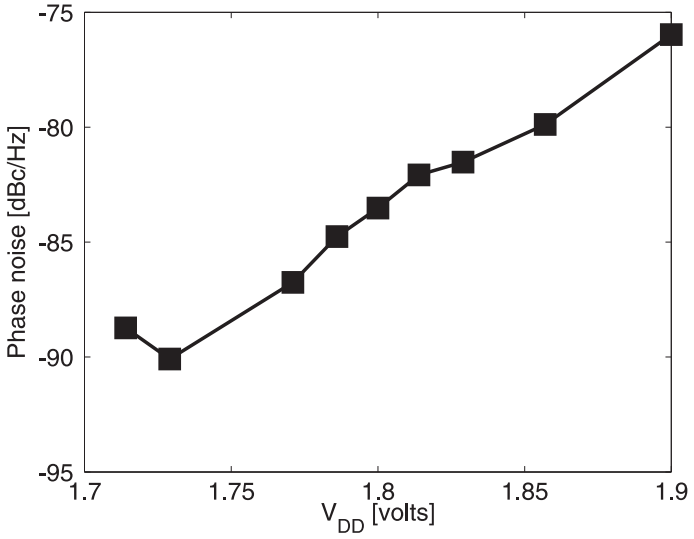

Figure 3.25: Effect of V_{DD} fluctuation on the phase noise of the proposed current-mode PLL at 1MHz frequency offset (post-layout).

signals instead of voltage the dynamic range of the control signals is decoupled from the voltage supply scaling.

We have shown that using current-mode filtering to replace voltage-mode filtering yields current-mode PLLs. The oscillator of the PLLs must also be changed from a voltage controlled oscillator to a current controlled oscillator. We have shown that current-mode filtering can be implemented using inductors. An RL filter effectively filters the signal from the phase detector and controls the oscillation of the CCO. We have also shown that the current filtering inductors can be implemented using active inductors.

The second part of this chapter focused on the use of active inductors current-mode filtering in PLLs. We have shown that type I and type II current-mode PLLs have the same loop bandwidth and damping parameters as those of their voltage-mode counterpart. We have also shown that the phase noise performance of current-mode PLLs bears a strong resemblance to that of voltage-mode PLL.

Chapter 4

Current-Mode Phase Locked Loops with Active Transformers

One of the drawbacks of inductor-based current-mode PLLs is the need for a large inductor in the loop filter. This chapter proposes the use of transformers in the loop filter of current-mode PLLs to utilize the mutual inductances of the transformer to improve the performance of the loop filter. The transformers are implemented using coupled active inductors. Section 1 introduces current-mode filtering using transformers. A detailed analysis of the self-inductances, mutual inductances, and noise of active transformers is provided in Section 2. Section 3 develops the closed-loop expression of active transformer current-mode PLLs. The phase noise of Section 5 provides the simulation results of active-transformer current-mode PLLs. The chapter is summarized in Section 6.

4.1 Current-Mode Filtering

4.1.1 Current-Mode Loop Filter with Transformers

A transformer-based current-mode low-pass filter can be constructed by connecting a resistor in series with the primary winding of a transformer, as shown in Fig. 4.2. For current-mode circuits,

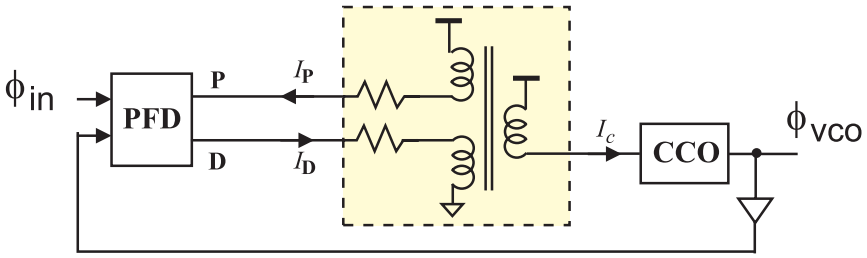

Figure 4.1: Configuration of current-mode phase-locked loops using transformer filtering.

the load of the secondary winding R_2 is ideally zero, this leads to $V_2(s) = 0$. Because

$$\begin{aligned} V_{in}(s) &= R_1 I_1(s) + V_1(s), \\ V_1(s) &= sL_{11} I_1(s) + sM_{12} I_2(s), \\ V_2(s) &= sL_{22} I_2(s) + sM_{21} I_1(s), \end{aligned} \tag{4.1}$$

where L_{11} and L_{22} are the self-inductance of the primary and secondary windings, respectively, M_{21} and M_{12} are the mutual inductance from the primary winding to the secondary winding and that from the secondary winding to the primary winding, respectively, we arrive at

$$\frac{I_2(s)}{V_{in}(s)} = -\frac{M_{21}}{R_1 L_{22}} \frac{1}{s(\frac{L_{11}L_{22} - M_{12}M_{21}}{R_1 L_{22}}) + 1}. \tag{4.2}$$

It is evident that the filter is a low-pass with its cutoff frequency given by

$$\omega_{-3dB} = \frac{R_1}{L_{11}} \frac{1}{\left(1 - \frac{M_{12}M_{21}}{L_{11}L_{22}}\right)}. \tag{4.3}$$

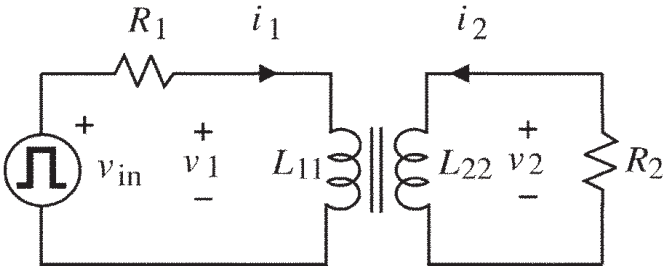

Figure 4.2: Current-mode loop filter using passive transformers.

4.2 CMOS Active Transformers

The active transformer proposed in this chapter evolves from Wu's current-reuse active inductors of Fig.4.3(a) [56] and consists of two coupled active inductors, as shown in Fig.4.3(b). Active transformers are two-port networks depicted by

$$\begin{aligned} V_1 &= Z_{11}(s)I_1 + Z_{12}(s)I_2, \\ V_2 &= Z_{21}(s)I_1 + Z_{22}(s)I_2, \end{aligned} \tag{4.4}$$

where $Z_{11}(s)$ and $Z_{22}(s)$ are the self-impedances, $Z_{12}(s)$ and $Z_{21}(s)$ are the transimpedances.

4.2.1 Self-inductance of Primary Winding

The input impedance of the primary winding with M1 and M2 identical is given by

$$Z_{11}(s) = \frac{g_o}{C_{gs}^2} \frac{s\frac{C_{gs}}{g_o} + 1}{s^2 + s\frac{g_m}{C_{gs}} + \frac{g_m^2}{C_{gs}^2}}. \tag{4.5}$$

The frequency of the zero and the self-resonant frequency of the primary winding are given by $\omega_{z,11} = \frac{g_o}{C_{gs}}$ and $\omega_{o,11} = \frac{g_m}{C_{gs}}$, respectively. The primary winding is inductive when $\omega_{z,11} < \omega < \omega_{o,11}$. The self-inductance, parasitic series and parallel resistances, and the parallel capacitance of the primary winding, denoted by L_{11}, $R_{11,s}$, $R_{11,p}$, and $C_{11,p}$, respectively, are obtained from the

admittance of the primary winding : $R_{11,p} \approx \frac{1}{g_m}$, $R_{11,s} \approx \frac{g_o}{g_m^2}$, $C_{11,p} = C_{gs}$, and $L_{11} \approx \frac{C_{gs}}{g_m^2}$. Note $g_m \gg g_o$ was utilized. Also note $Z_{11}(0) = R_{11,s}||R_{11,p} \approx g_o/g_m^2$. The preceding results show that a small dc biasing current is needed in order to obtain a large self-inductance of the primary winding. It should be noted that when C_{gd} is considered, $C_{11,p}$ and L_{11} increase slightly while R_p and R_s remain unchanged.

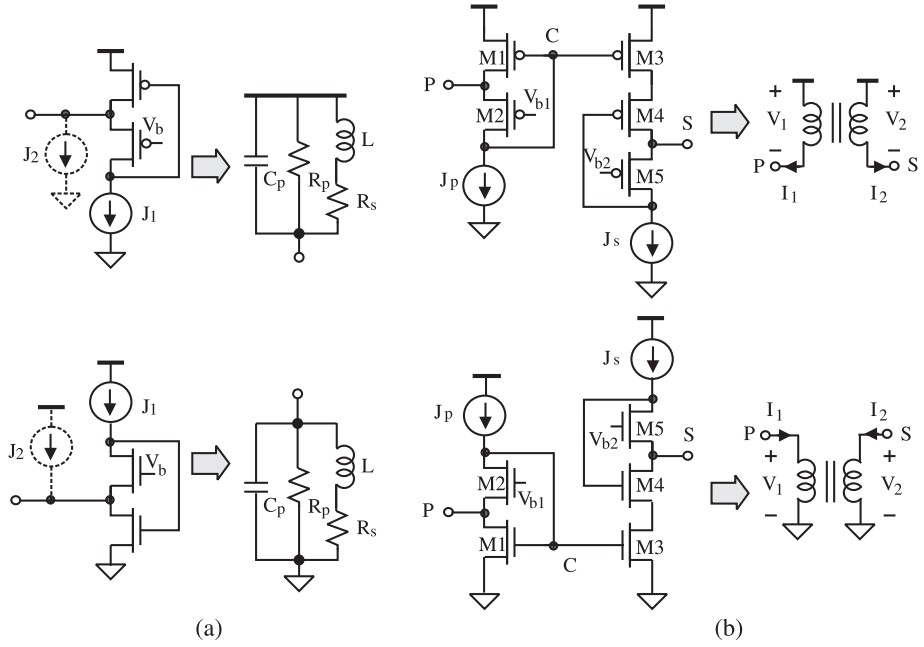

Figure 4.3: (a) Wu's current-reuse active inductors. (b) Proposed CMOS active transformers.

4.2.2 Self-inductance of Secondary Winding

The impedance looking into the secondary winding is given by

$$Z_{22}(s) = \frac{g_o}{C_{gs}^2} \frac{s\frac{C_{gs}}{g_o} + 1}{s^2 + s\frac{g_m}{C_{gs}} + \frac{g_m g_o}{C_{gs}^2}}. \tag{4.6}$$

It has a zero at frequency $\omega_{z,22} = \frac{g_o}{C_{gs}}$ and the self-resonant frequency $\omega_{o,22} = \frac{\sqrt{g_m g_o}}{C_{gs}}$. The secondary winding is inductive when $\omega_{z,22} < \omega < \omega_{o,22}$.The self-inductance, parasitic series and parallel resistances, and the parallel capacitance of the secondary winding, denoted by L_{22}, $R_{22,s}$, $R_{22,p}$, and $C_{22,p}$, respectively, are given by $R_{22,p} \approx \frac{1}{g_m}$, $R_{22,s} = \frac{1}{g_o}$, $C_{22,p} = C_{gs}$, and $L_{22} = \frac{C_{gs}}{g_o^2}$. Also note $Z_{22}(0) = R_{22,s}||R_{22,p} \approx 1/g_m$.

4.2.3 Mutual inductance from primary to secondary windings

The voltage at the secondary winding terminal is obtained from the small-signal equivalent circuit of the winding

$$V_2(s) \approx \frac{sC_{gs} + g_o}{s^2C_{gs}^2 + sC_{gs}g_m + g_m g_o} I_2 - \frac{g_m^2(sC_{gs} + g_o)}{(sC_{gs} + g_m)(s^2C_{gs}^2 + sC_{gs}g_m + g_m g_o)} V_c.$$

The voltage at the coupling node C is obtained by solving the primary winding

$$V_c(s) \approx \frac{g_m}{2C_{gs}^2} \frac{I_1}{s^2 + s\frac{g_m}{C_{gs}} + \frac{g_m g_o}{C_{gs}^2}}. \tag{4.7}$$

The transimpedance can be quantified by substituting (4.7) into (4.7) with $I_2 = 0$

$$Z_{21}(s) = -\frac{g_m^3}{2} \frac{(sC_{gs} + g_o)}{(sC_{gs} + g_m)(s^2C_{gs}^2 + sC_{gs}g_m + g_m g_o)^2}. \tag{4.8}$$

The cutoff frequency of the mutual inductance is given by $\omega_{o,21} = \frac{\sqrt{g_m g_o}}{C_{gs}}$ approximately.
We comment on the preceding development : (i) $\omega_{z,22} = \omega_{z,11}$. The lower frequency bound of the inductive region of both the primary and secondary windings is the same. (ii) $\omega_{o,22} < \omega_{o,11}$. The primary winding has a higher upper frequency bound, as is evident in Fig.4.4. (iii) $L_{22} > L_{11}$. This agrees with the simulation results shown in Fig.4.4.

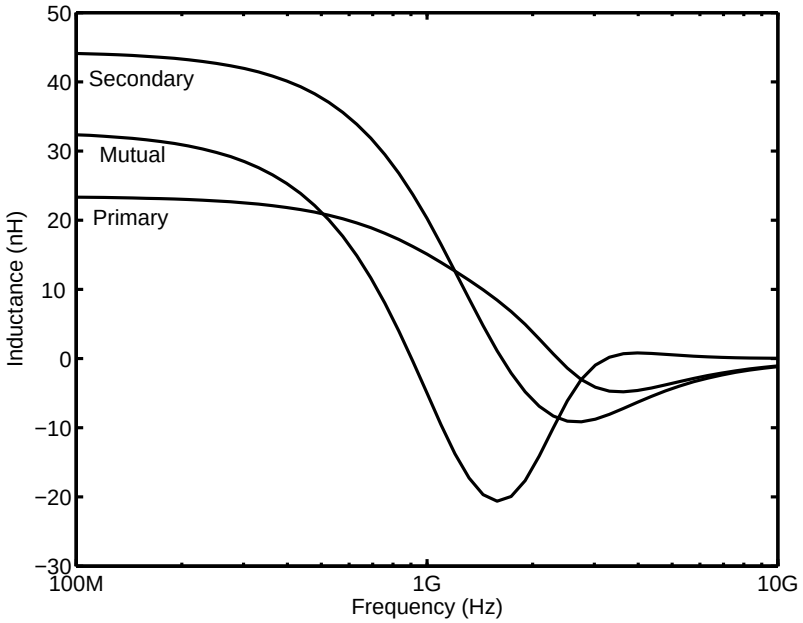

Figure 4.4: Simulated self-inductance of the primary and secondary windings and mutual inductance from the primary winding to the secondary winding of the active transformer. Circuit parameters : $W = 50\mu$m, $L = 0.18\mu$m for all transistors, $J_p, J_s = 150\mu$A, $V_{b1} = 0.8$ V, and $V_{b2} = 0.2$ V.

4.2.4 Current-Mode Loop Filter Using Active Transformers

The schematic of the current-mode loop filter is shown in Fig. 4.5. The transformer is replica biased to reduce its sensitivity to V_{DD}. Fig. 4.6 shows the dependence of the output current of the loop filter on the duty cycle of the input voltage. Fig. 4.7 plots the dependence of the bandwidth of the loop filter on V_{DD}. The loop filter with the replica-biased nMOS active transformer exhibits the lowest sensitivity and was chosen in this design. Fig. 4.8 shows the dependence of the bandwidth of the loop filter on the reference voltage V_{b3} of the auxiliary amplifier of the replica-biasing circuit at all process corners (SS, SF, FS, FF) and in the nominal process conditions (TT). V_{b3} is an external voltage that can be tuned manually. For each process corner, the following tuning range of the cutoff

frequency of the loop filter can be obtained by varying V_{b3} from 0 to 0.6V : (i) FF : 50-900 MHz, (ii) SS : 1-300 MHz, (iii) TT : 3-600 MHz, (iv) SF : 2-400 MHz, and (v) FS : 27-770 MHz. The location of the poles of the proposed PLL can be changed by varying the bandwidth of the loop filter. This allows us to tune the loop bandwidth ω_n and loop dynamics of the PLL. The tunability of the bandwidth of the loop filter provides an effective and economic way to offset the effect of process variation.

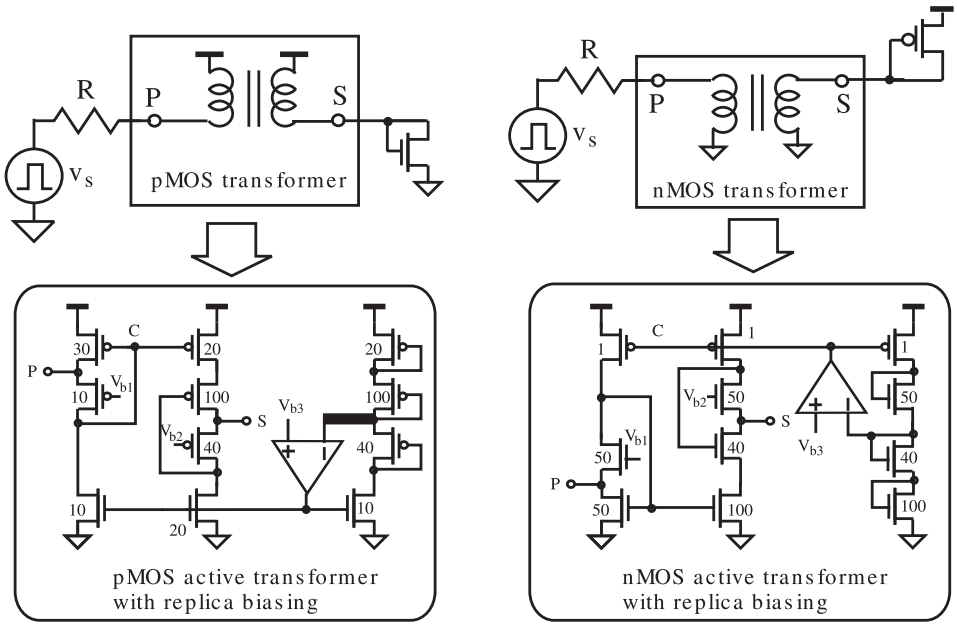

Figure 4.5: Current-mode loop filter. pMOS active transformer: $V_{b1} = 1.2$ V, $V_{b2} = 1.2$ V, $V_{b3} = 1.3$ V. nMOS active transformer: $V_{b1} = 0.7$ V, $V_{b2} = 0.7$ V, $V_{b3} = 0.5$ V. $R = 6k\Omega$. $L = 0.18\mu$m for all transistors. The numbers in the figures are transistor width.

The inductances of the active transformer are inversely proportional to the transconductance of the gyrators. Normally the transistors of the gyrators are biased in the saturation. When the transistors are in the triode, they behave as a transconductor with its transconductance $g_{ds} < g_m$.

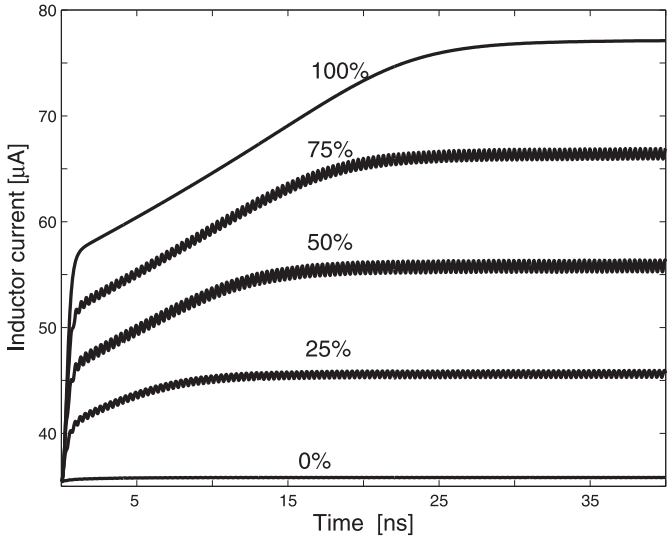

Figure 4.6: Simulated dependence of the output current of active-transformer loop filter on the duty cycle of the input voltage.

In this case, an inductive characteristic exists with a larger inductance. It should be noted that the resistor and the input capacitance of the primary winding of the active transformer limit the swing of the voltage at the input of the transformer to a rather small range, ensuring that transistors connected to the primary winding node remain in the saturation.

4.2.5 Quality Factors

The quality factor of the primary winding is obtained from [57]

$$Q_1(\omega) = \frac{\omega L}{R_s} = \frac{\omega}{\omega_z}, \tag{4.9}$$

$$Q_2(\omega) = \frac{R_p}{R_p + R_s\left[1 + (\frac{\omega L}{R_s})^2\right]} = \frac{1}{1 + \frac{R_s}{R_p}\left[1 + Q_1^2(\omega)\right]}, \tag{4.10}$$

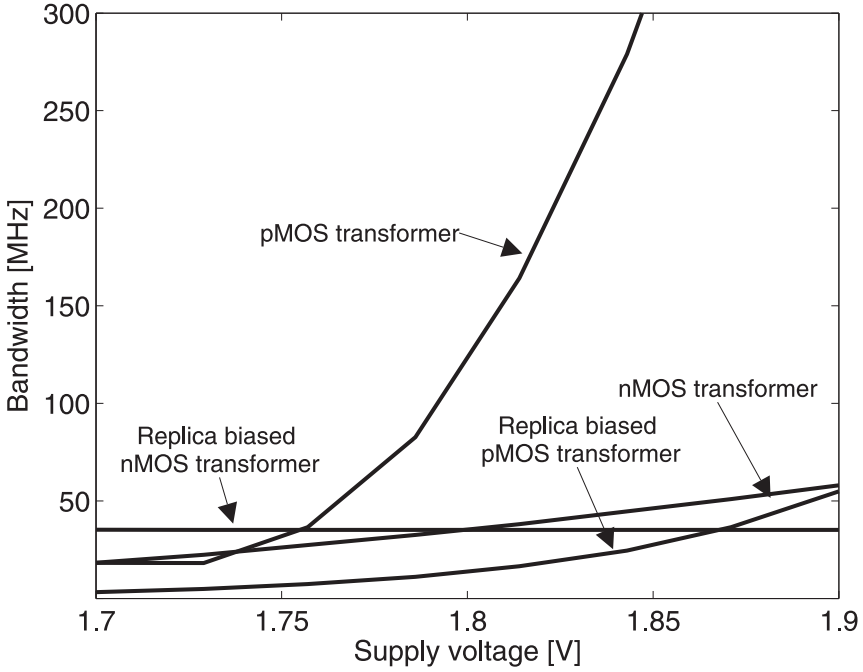

Figure 4.7: Simulated sensitivity of the bandwidth of active-transformer loop filter to supply voltage.

$$Q_3(\omega) = 1 - \frac{R_s^2 C_p}{L} - \omega^2 L C_p = 1 - \left(\frac{\omega}{\omega_o}\right)^2 - \left(\frac{\omega_z}{\omega_o}\right)^2. \tag{4.11}$$

$Q_1(\omega)$ quantifies the quality factor at low frequencies, $Q_2(\omega)$ accounts for the effect of the finite output impedance of MOSFETs, and $Q_3(\omega)$ shows that the quality factor vanishes when approaching ω_o. To boost $Q(\omega)$, $\frac{R_s}{R_p}$ should be reduced.

4.2.6 Noise of Active transformers

The thermal noise and flicker noise of transistor j are represented by an equivalent noise current source with its power $\overline{i_{nj}^2} = \left(4kTg_m\gamma + \frac{K_f I_j}{f}\right)\Delta f$, where K is Boltzmann constant, T is the temperature of the semiconductor junction, g_m is the transconductance of the semiconductor device,

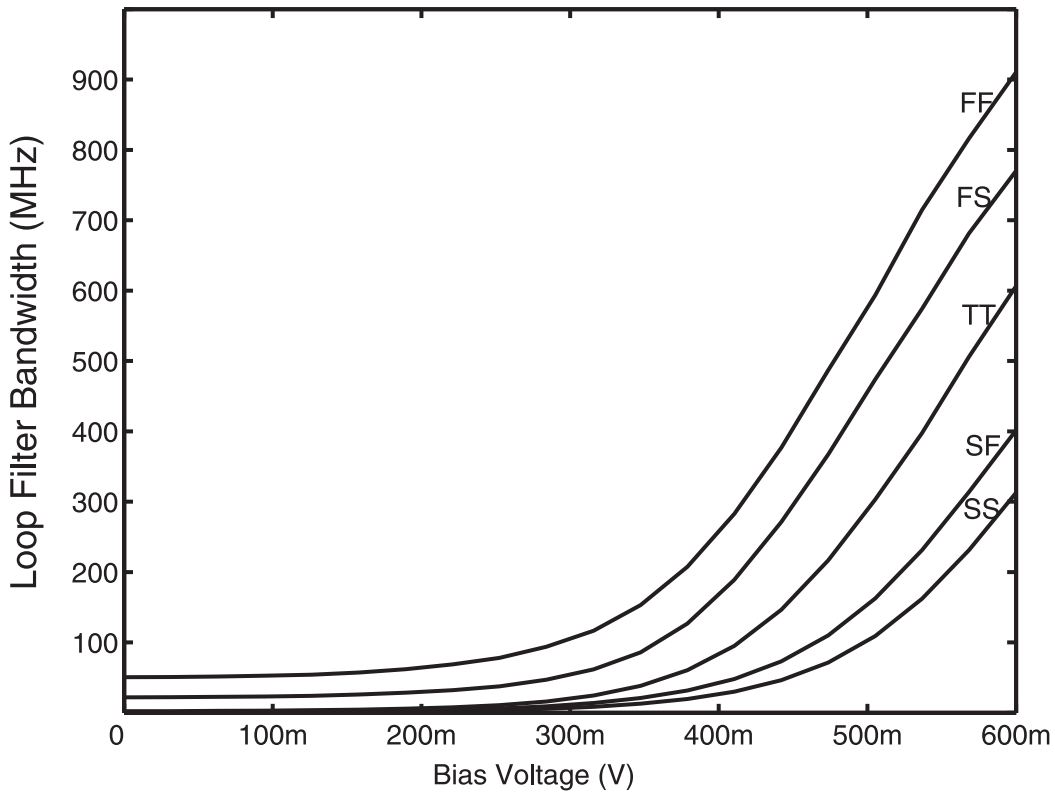

Figure 4.8: The dependence of loop filter bandwidth on replica bias reference voltage at process corners and in nominal conditions.

K_f is the flicker-noise coefficient, I_j is the junction current, and f is frequency. To quantify the total noise of the active transformer, a noise-voltage generator $\overline{v_n^2}$ and a noise-current generator $\overline{i_n^2}$ at the input of the primary winding are employed, as shown in Fig. 4.9. At low frequencies the noise current and noise voltage are given by

$$\overline{i_n^2} = \overline{i_{n1}^2} + \overline{i_{n3}^2} + \overline{i_{n5}^2} + \left(\frac{g_o}{g_m}\right)^2 \left[\overline{i_{n2}^2} + \overline{i_{n4}^2}\right] \tag{4.12}$$

and

$$\overline{v_n^2} = (\frac{g_o}{g_m})^2 \frac{1}{g_m^2} \left[\overline{i_{n2}^2} + \overline{i_{n3}^2} + \overline{i_{n5}^2} + (\frac{g_o}{g_m})^2 \overline{i_{n4}^2} \right]. \tag{4.13}$$

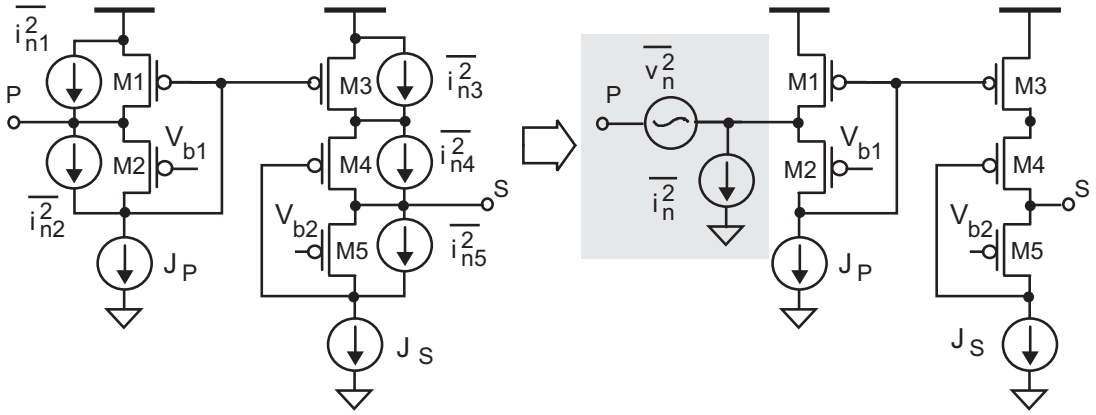

Figure 4.9: Noise equivalent circuit of active transformer.

4.2.7 Active Transformers with Multiple Windings

The configurations of active transformers with multiple windings are shown in Fig.4.10.

4.3 Loop Dynamics of Transformer Based Current-Mode PLLs

From Fig.4.11, we have

$$V_{pd}(s) = RI_1(s) + sL_{11}I_1(s) + sM_{12}I_2(s). \tag{4.14}$$

Because the active transformer is uni-directional, $M_{12} = 0$. For the secondary winding, $V_2(s) =$

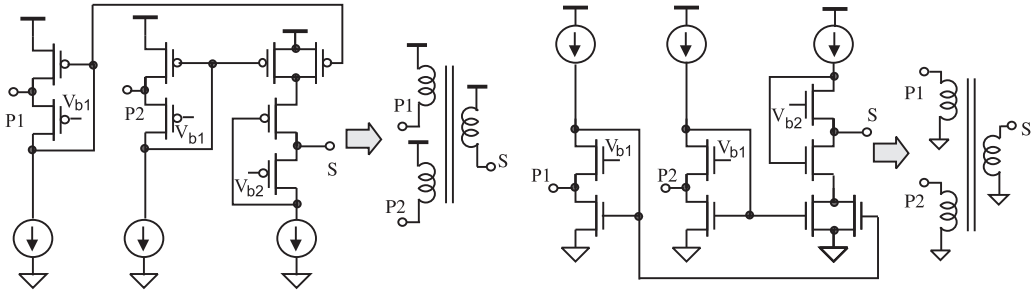

Figure 4.10: Active transformers with multiple windings.

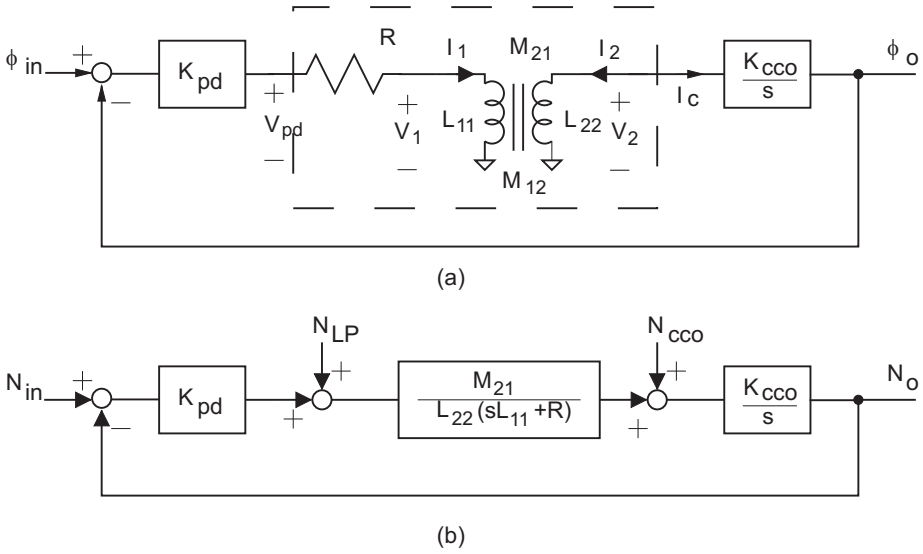

Figure 4.11: Block diagram with noise sources of the PLL in lock state.

$sL_{22}I_2(s)+sM_{21}I_1(s)$. Because the load of the secondary winding is a CCO whose input impedance is zero ideally, we have $V_2(s) = 0$. Further noting $I_c(s) = -I_2(s)$, we arrive at

$$I_c(s) = \frac{M_{21}}{L_{22}(sL_{11} + R)} V_{pd}(s). \tag{4.15}$$

The cutoff frequency of the current-mode loop filter is obtained from (4.15) : $\omega_{LF} = \dfrac{R}{L_{11}}$. The transfer function of the PLL is given by

$$\frac{\Phi_o(s)}{\Phi_i(s)} = \frac{K_{pd}K_{cco}M_{21}}{\Delta}, \tag{4.16}$$

where $\Delta = s^2L_{11}L_{22} + sRL_{22} + K_{pd}K_{cco}M_{21}$. The loop gain-bandwidth product ω_n and damping factor ς of the PLL are given by

$$\omega_n = \sqrt{\frac{K_{pd}K_{cco}M_{21}}{L_{11}L_{22}}}, \tag{4.17}$$

$$\xi = \frac{R}{2}\sqrt{\frac{L_{22}}{K_{pd}K_{cco}L_{11}M_{21}}}. \tag{4.18}$$

We comment on the preceding development : (i) The PLL is type I. (ii) The damping factor ξ can be tuned by varying R without affecting the loop bandwidth. (iii) $\omega_n\xi = \omega_{LF}/2$. (iv) The higher the self inductances, the smaller the loop bandwidth, the better the suppression of the transient disturbances encountered at the input. (v) The larger the mutual inductance, the larger the loop bandwidth, the weaker the suppression of transient disturbances at the input because large M_{21} allows these disturbances to couple to CCO more easily.

4.4 Phase Noise of Current-Mode Active Transformer PLLs

To analyze the phase noise of the PLL in the lock state, consider Fig. 4.11 where the noise from the input, the noise of the loop filter, and the noise of the CCO are considered. The phase noise of the PLL is given by

$$N_o(s) = \frac{sL_{22}(sL_{11}+R)}{\Delta}N_{cco}(s) + \frac{K_{cco}L_{22}(sL_{11}+R)}{\Delta}N_{LP}(s) + \frac{K_{cco}K_{pd}M_{21}}{\Delta}N_{in}(s).$$

It is seen that the noise from the input has a low-pass characteristic with the cutoff frequency ω_n. The noise from the loop filter has a band-pass characteristic with $\frac{N_o}{N_{LF}}(j0) = \frac{L_{22}R}{K_{PD}M_{21}}$, low corner frequency $\omega_z = \frac{R}{L_{11}}$ and the center frequency ω_n. The noise from the CCO has a high-pass characteristic with the corner frequency ω_n. These observations reveal that the contribution of the noise from the input to the phase noise of the PLL is mainly at frequencies below ω_n. The contribution of the noise from the CCO to the phase noise of the PLL is mainly at frequencies beyond ω_n. The contribution of the noise from the loop filter to the phase noise of the PLL is mainly in the vicinity of ω_n.

4.5 Simulation Results of Active-Transformer Current-Mode PLL

A 3.0 GHz active transformer current-mode PLL with its building blocks presented earlier has been implemented in TSMC-0.18μm 1.8V 6-metal CMOS technology. The layout of the PLL is shown in Fig.4.12. Fig. 4.13 plots the control current of the PLL. The PLL reaches the lock state in 60 ns approximately. The phase noise of the PLL was analyzed using the time-domain behavioral simulation techniques proposed in [58, 59, 60], specifically, (i) the phase noise of the CCO was analyzed using Cadence's SpectreRF with the consideration of the fold-over of the broad-band noise sources. The amplitude of the timing jitter of the CCO was obtained from its phase noise. In Verilog-AMS time-domain simulation of the PLL, the oscillation period of the CCO was disturbed using the extracted timing jitter, together with a normally distributed random generator with zero mean and unity variance. (ii) The active transformer loop filter is modeled as a series RL network with the inductance, resistance, and noise extracted from its SpectreRF simulation results. (iii) The PFD was modeled using Verilog-AMS with delays extracted from its schematic-level SpectreRF simulation results. (iv) Time-domain analysis of the PLL was carried out and a large number of oscillation periods were recorded after the PLL reached the lock state. The phase noise of the

PLL was obtained from FFT analysis of the recorded period of the CCO with 512K samples and Hanning window using Matlab. The results are shown in Fig.4.14. The phase noise of the PLL is approximately -100 dBc/Hz at 1 MHz frequency offset, higher than that of the CCO at the same frequency offset. The power consumption of the CCO, the filter, and the PFD is 15 mW, 0.138 mW, and 0.864 mW, respectively.

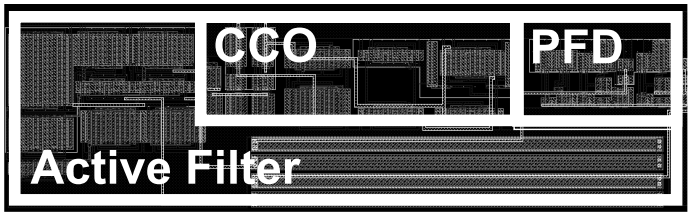

Figure 4.12: Layout of the PLL.

4.6 Chapter Summary

An in-depth examination of the principle of active CMOS transformers has been presented. The primary winding self-inductance, secondary winding self-inductance, and mutual inductance have been derived. The application of the active transformer to current-mode filter has been highlighted. The quality factor and the noise of active transformers have been derived.

It has been shown that active transformers can be used as current-mode filters for use in current-mode PLLs. The loop dynamics of the transformer based current-mode PLLs have been analyzed, clearly showing the addition of the mutual coupling factor in the loop bandwidth and damping. The phase noise of the transformer current-mode PLL has also been analyzed. The noise generated by the active transformer is bandpass filtered by the PLL's closed loop transfer function. Finally, the performance of an active transformer current-mode PLL has been presented.

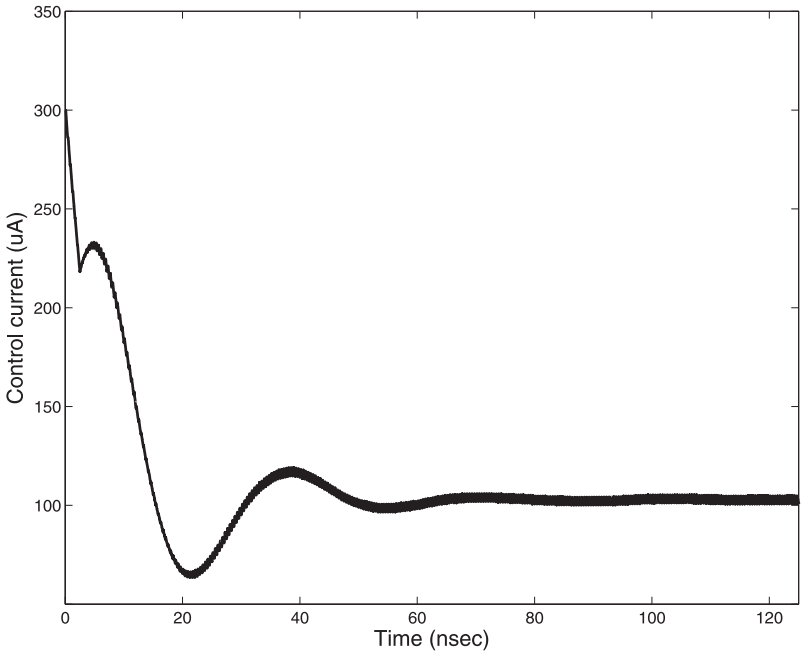

Figure 4.13: Simulated control current of the PLL (post-layout).

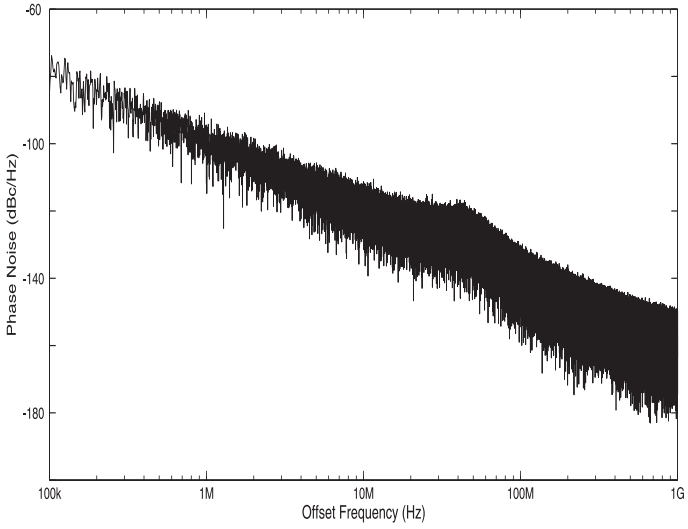

Figure 4.14: Simulated phase noise of the PLL.

Chapter 5

Wide-Band VCOs for Frequency Synthesizers

VCOs for wireless communications are mainly passive LC tank oscillators due to their superior phase noise performance. These VCOs, however, suffer from the drawback of a small frequency tuning range. Several mechanisms exist to tune the oscillation frequency of passive LC-tank oscillators, with varactors being the most widely used. The frequency tuning range of LC oscillators with varactors is limited by the ratio of the capacitance of the varactor to the total capacitance at the node to which the varactors are connected. The typical frequency tuning range of varactor LC VCOs is less than 10%.

This chapter starts with a brief introduction of existing wide band VCOs that utilize switched banks to increase the frequency tuning range. Section 2 describes an active inductor VCO that provides a large frequency tuning range. Section 3 introduces a hybrid oscillator that utilizes the superior phase noise performance of a passive transformer and the wide frequency tuning range of an active inductor. Section 4 introduces a modified hybrid oscillator that uses the impedance scaling property of a transformer to increase the frequency tuning range of varactors. Section 5 compares the performance of three aforementioned oscillators. The chapter is concluded in Section 6.

5.1 Wide-band VCOs

The most common method to increase the frequency tuning range of LC tank oscillators is to employ a switched capacitor bank [61][62][63][64][65]. An LC tank oscillator with a switched capacitor bank is shown in Fig. 5.1. The VCO uses a binary weighted capacitor bank. It is also common to use a grey encoded switched capacitor bank. The composition of the switches used to connect the switched capacitors to the LC tank network are also shown in the figure. The use of nMOS or transmission gate devices as switches introduces unwanted parasitic resistances and reduces the quality factor of the LC network.

The tuning range of the switched capacitor bank is limited by two factors: switch capacitance, and varactor capacitance ratio. The switches used to connect the capacitors will introduce their source/drain-to-substrate capacitances to the LC tank and limit the highest frequency of oscillation. A large switch is required to reduce the series resistance. This, however, will result in high source/drain capacitances. The second limitation of the switched capacitor bank occurs when the fixed capacitors are introduced into the LC tank and reduce the varactor's fixed-to-variable capacitance ratio subsequently.

To overcome the problem of limiting the varactor's frequency tuning range by the additional fixed capacitance to the LC tank is to switch passive inductors instead of capacitors [67]. By changing the inductance of the LC tank the fixed capacitance seen by the varactor is nearly constant resulting in a higher frequency tuning range than using switched capacitors. An example of inductor switching is shown in Fig. 5.2. The current alternating between the inductor and capacitors is the bias current of the VCO scaled up by the quality factor, requiring the switches to handle large current. The second disadvantage is the silicon area required to include multiple spiral inductors on chip.

There are two very important design considerations when using switched banks on wide band VCOs. The first consideration is that there must be overlap of the tuning curves from each switched value. An example of a single bit switched capacitor bank's tuning curves are shown in fig. 5.3. The figure clearly shows two independent tuning curves, one for the capacitor switched in and the other

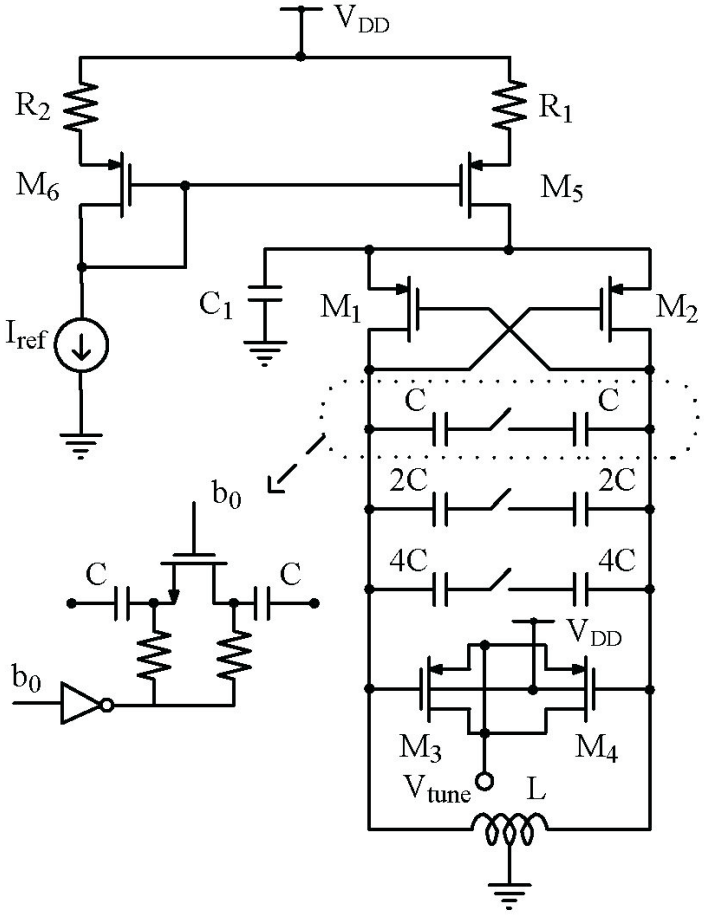

Figure 5.1: Schematic of a wide-band VCO using a switched capacitor bank [66].

capacitor switched out. The highest frequency of the lower curve must overlap the lowest frequency of the top curve to ensure continuous frequency tuning.

The second consideration in the design of PLLs using bank switched VCO is the control circuit. The control circuit must automatically switch in the fixed capacitors or inductors when the required frequency is outside the range of the existing switch structure. When the PLL tunes from the highest frequency of a lowest curve to the bottom frequency value of a higher curve the PLL's control

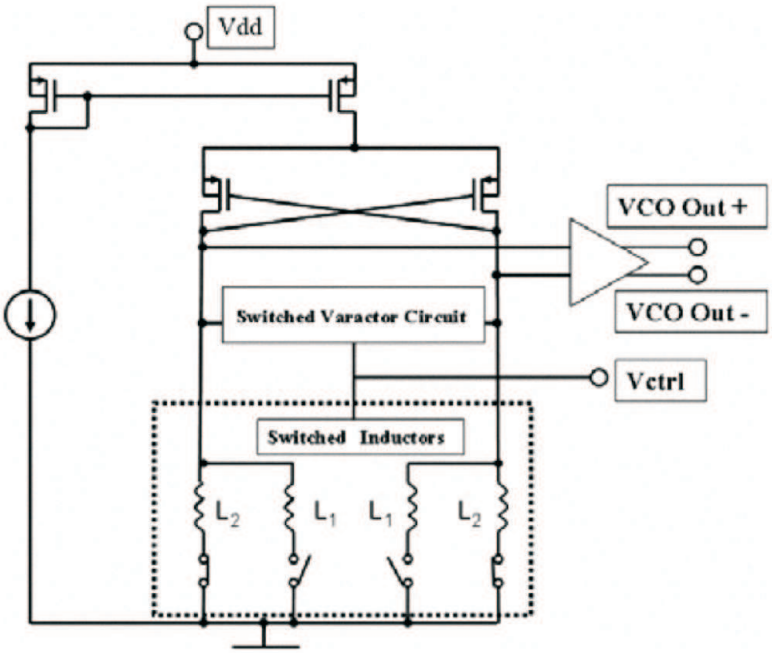

Figure 5.2: Schematic of a wide-band VCO using a switched inductor bank [68].

voltage must cover the entire PLL's control range voltage. The worst case scenario is if the PLL must lock to a frequency that translates into a frequency near the transition between two switched curves. A normal property of a locking PLL is a 2nd order oscillation, and it is possible the overshooting can cause the control circuitry to switch between the two tuning curves.

5.2 Active-Inductor Ultra Wide-band VCO

An active inductor LC-tank voltage-controlled oscillators with an ultra wide frequency tuning range was investigated in [70] as an alternative to switched banks to achieve a large frequency tuning range . Two inductance tuning mechanisms, namely the wide-band tuning mechanism for coarse

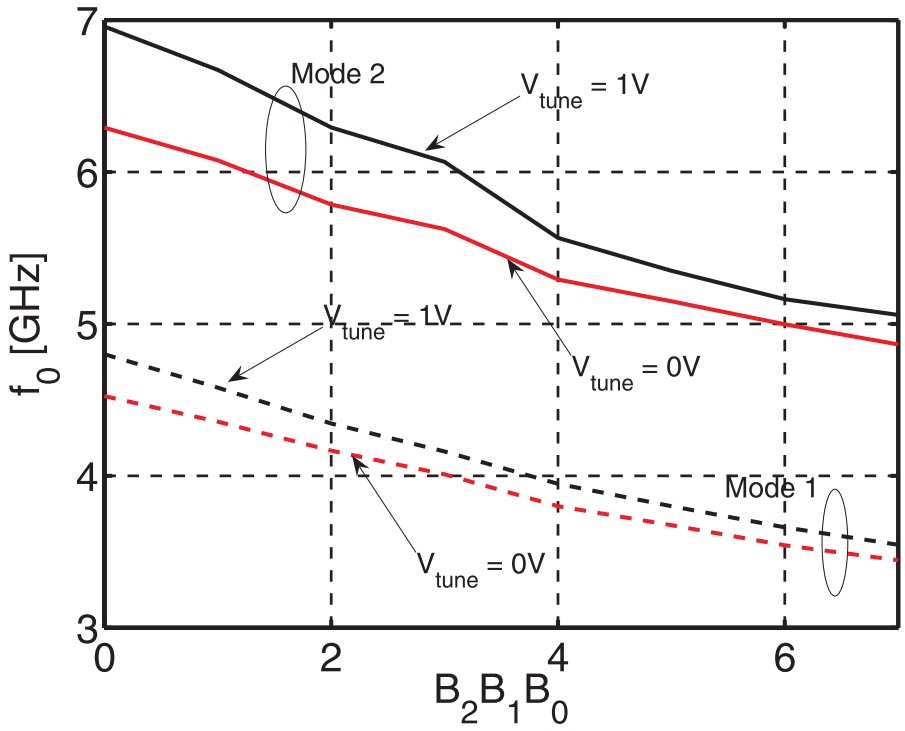

Figure 5.3: VCO tuning curves of a 1-bit switched capacitor bank [69].

frequency adjustment over a large frequency range for band selection and the primary tuning mechanism for the fine frequency tuning in closed loop control systems are developed in this thesis for the proposed UWB frequency synthesizer VCO. The absence of spiral inductors significantly reduces the silicon consumption of the oscillator and the tunability of the quality factor of the active inductor using two negative resistors results in good phase noise performance.

The proposed ultra wide-band VCO is a fully differential active inductor LC oscillator utilizing the active inductor proposed by Lu *et. al* [71]. Lu active inductor shown in Fig. 5.4 is a differentially configured gyrator-C active inductor. The input gyrator is a pair of pseudo-differential common-gate amplifiers composed of $M_{1,3,4,6}$ and the output gyrator is a pair of source followers consisting of $M_{2,5}$. A negative resistor network is formed by cross-coupled $M_{7,8}$ to compensate for the resistive

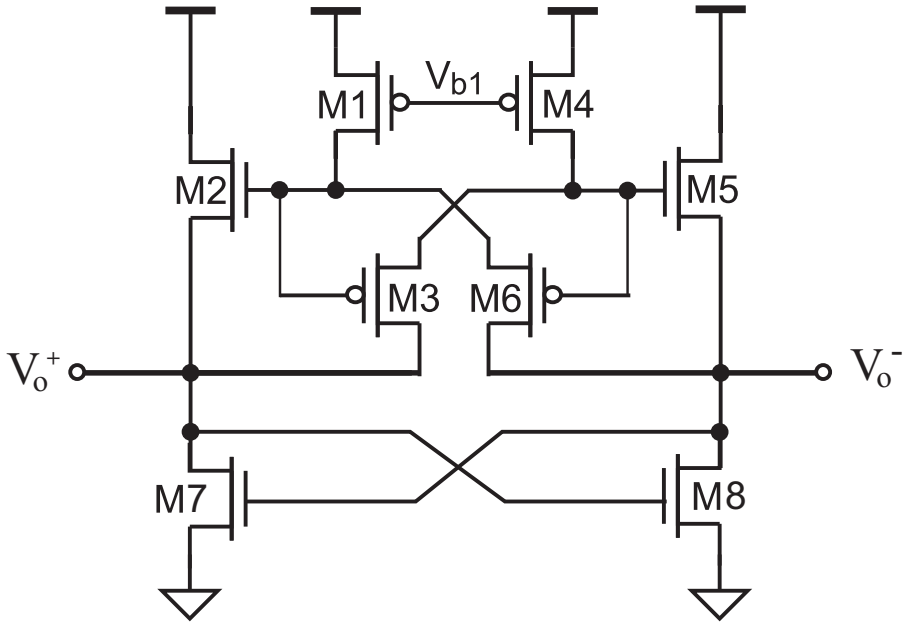

Figure 5.4: Schematic of Lu *at. al* active inductor VCO.

loss of the active inductor. Transistors $M_{1,4}$ are biased in the triode and behave as a pair of voltage-controlled resistors whose resistance is controlled by V_{b1}. It was shown in [71] that the differential input impedance of the active inductor (looking into output V_o^+ and V_o^-) is given by

$$Z_{in} = \frac{2[s(C_{gs3} + C_{gs2}) - g_{m3} + g_{ds1}]}{g_{ds1}[g_{m3} + g_{m2} + s(C_{gs3} + C_{gs2})]}. \tag{5.1}$$

The inductance of the active inductor is given by

$$L_{eq} = \frac{2(C_{gs3} + C_{gs2})}{g_{ds1}(2g_{m3} + g_{m2} - g_{ds1})}. \tag{5.2}$$

It is evident that the inductance is dependent of g_{m2}, g_{m3} and g_{ds1}. Although the inductance of the active inductor can be tuned by varying these parameters, the most convenient way is to vary V_{b1}, which will in turn tunes $g_{ds1,4}$.

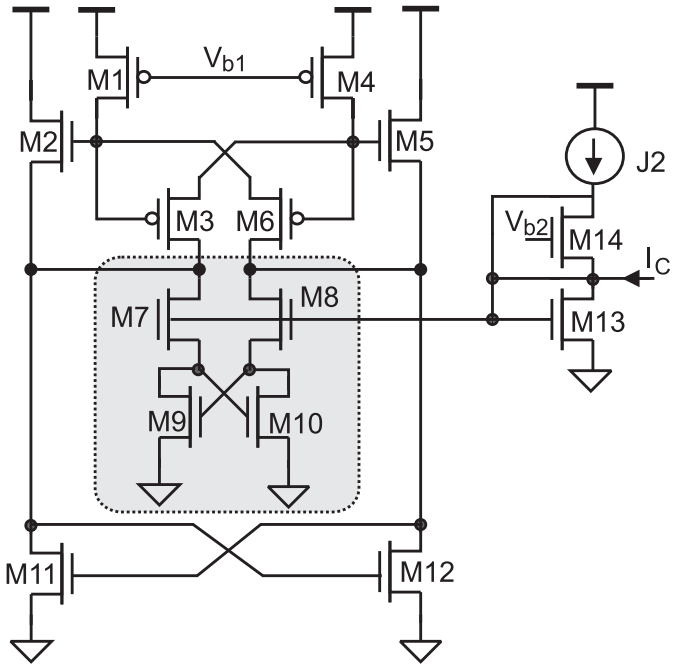

Figure 5.5: Schematic of the proposed ultra wide-band VCO with dual tuning mechanisms.

The schematic of the proposed ultra wide-band VCO is shown in Fig.5.5 with the modification to Lu active inductor highlighted. Two frequency tuning mechanisms are utilized in the proposed VCO. The first tuning mechanism, called the wide-band tuning mechanism, tunes the oscillation frequency of the oscillator by varying V_{b1}, which in turn tunes $g_{ds1,4}$. It is seen that V_{b1} provides a frequency range from 0.2 $\sim$ 6.5 GHz as shown in Fig. 5.6.

The modification to Lu active inductor adds an additional tuning element and will be called the primary frequency tuning mechanism. The primary frequency tuning element is composed of $M_{7,8,9,10}$. V_{b2} controls the inductance of the active inductor by adjusting the current drawn by $M_{7,8,9,10}$ subsequently the transconductances of $M_{2,3,5,6}$:

$$L_{eq} = \frac{2(C_{gs3} + C_{gs2})}{g_{ds1}(\beta_3\sqrt{I_{DS3}} + \beta_2\sqrt{I_{DS2}} - g_{ds1})}, \tag{5.3}$$

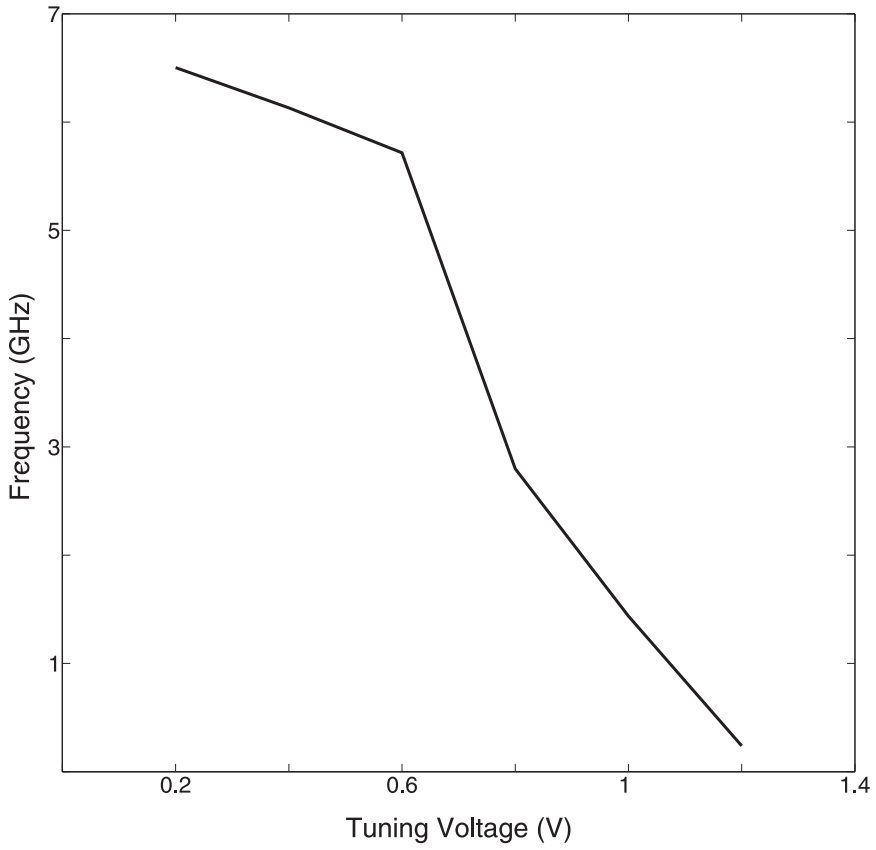

Figure 5.6: Dependence of the oscillation frequency of VCO on V_{b1}.

where β_2 and β_3 are the transconductance parameters of M_2 and M_3 and are given by

$$\beta_{2,3} = \sqrt{2\mu_n C_{ox}\Big(\frac{W}{L}\Big)_{2,3}}. \tag{5.4}$$

Fig.5.7 shows the dependence of the oscillation frequency of VCO on V_{b2} for different $M_{7,8}$ sizes.

The additional bias current from $M_{7,8}$ does not flow through the negative resistance network of $M_{11,12}$. This will reduce the quality factor of the oscillator subsequently increase the phase noise performance. To reduce the dependence of the phase noise performance on the additional

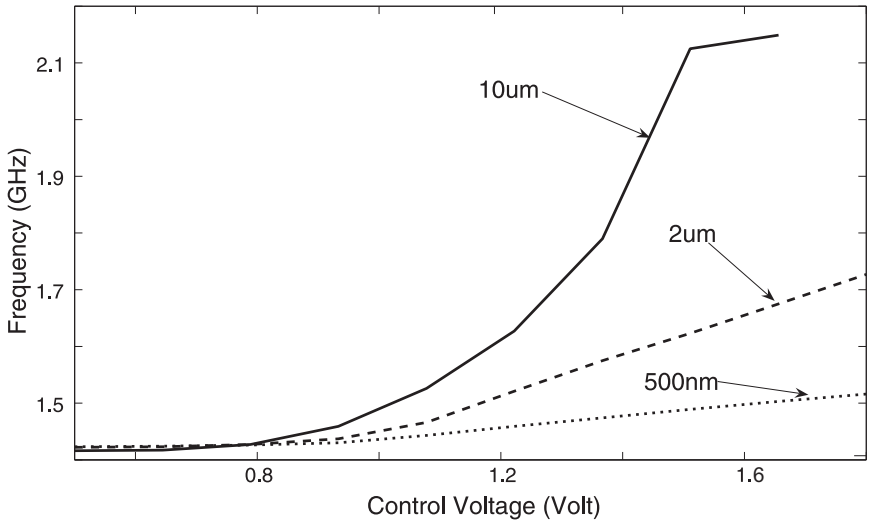

Figure 5.7: Dependence of the oscillation frequency of VCO on V_{b2}.

bias current a second negative resistance network $M_{9,10}$ is added. As bias current is directed away from the negative resistance network of $M_{11,12}$ its resistance value will be reduced. The redirected bias current will cause the negative resistance of $M_{9,10}$ to increase. The sum total of the negative resistance formed by $M_{11,12}$ and $M_{9,10}$ networks will remain constant regardless of the tuning value. The quality factor of the active inductor is obtained from the ratio of the imaginary part of the impedance of the active inductor to the real part of the impedance.

$$Q = \frac{\omega(C_{gs3} + C_{gs2})(2g_{m3} + g_{m2} - g_{ds1})}{(g_{m3} + g_{m2})(g_{ds1} - g_{m3}) + \omega^2(C_{gs3} + C_{gs2})^2}. \tag{5.5}$$

It becomes evident that the quality factor of the active inductor is dependent of the biasing condition of the devices of the active inductor and the frequency tuning voltages $V_{b1,b2}$. Fig. 5.8 shows the dependence of the phase noise of the oscillator on V_{b2}.

The proposed VCO has been designed and implemented in TSMC-0.18μm 1.8V 6-metal 1-poly CMOS technology. The layout of the VCO is shown in Fig. 5.9. The output is buffered with an open drain PMOS matched to 50 Ω for wafer probe measurement. The oscillator is analyzed using

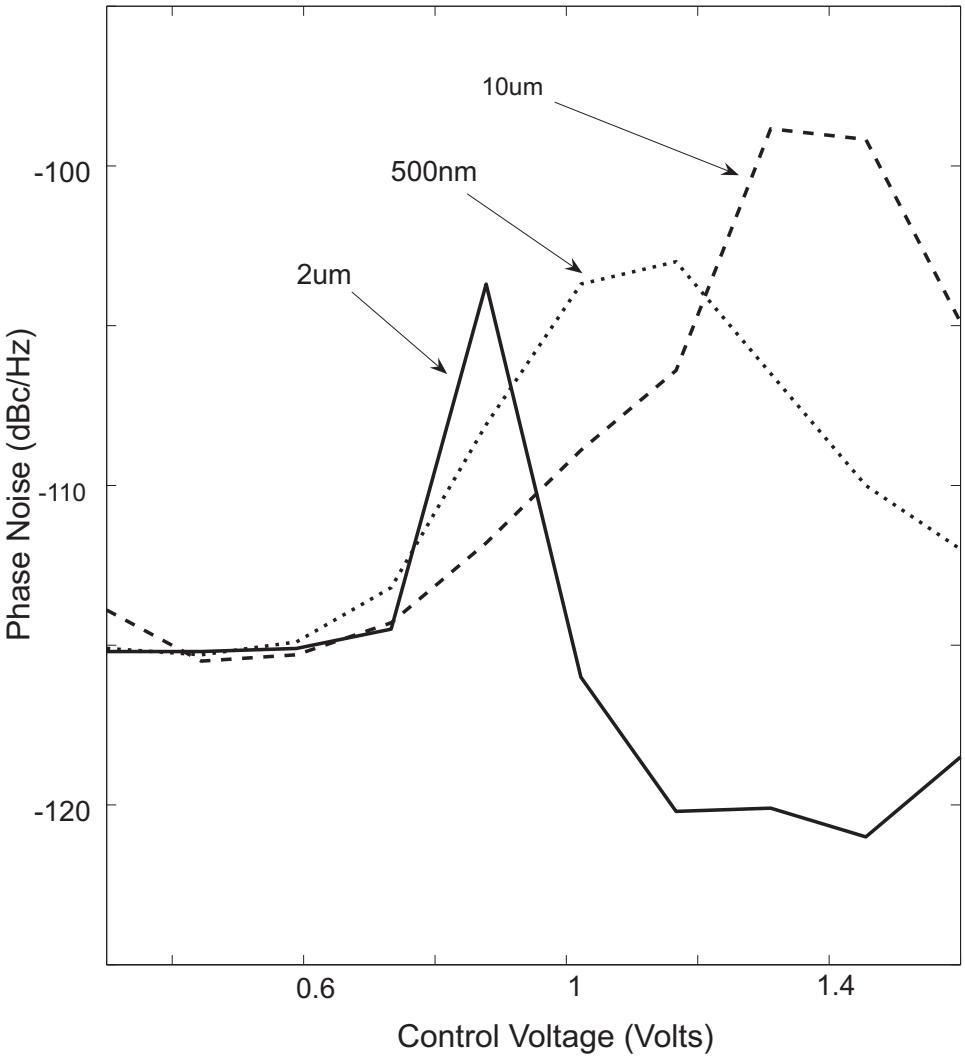

Figure 5.8: Dependence of the phase noise of VCO on V_{b2} and nMOS size.

SpectreRF from Cadence Design Systems with BSIM3V3 device models. The output of the VCO is shown in Fig. 5.10. The simulated phase noise of the VCO is shown in Fig. 5.11 with the VCO tuned to 1.6 GHz. It is seen that the phase noise is -118.5 dBc/Hz at 1 MHz frequency offset. The power consumption of the VCO is 45 mW.

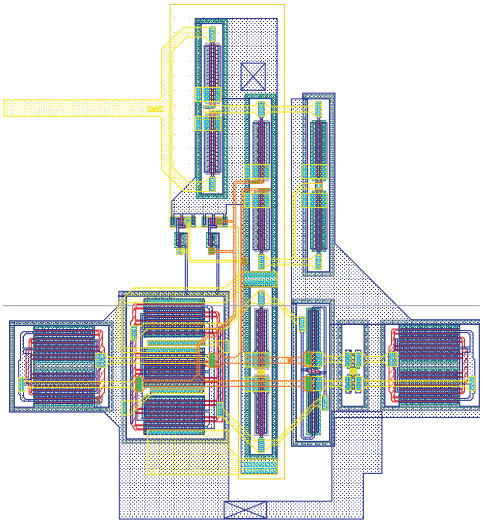

Figure 5.9: Layout of VCO.

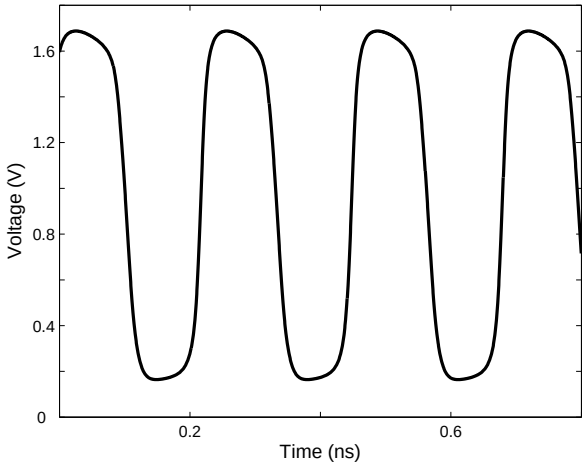

Figure 5.10: Waveform of the output voltage of VCO.

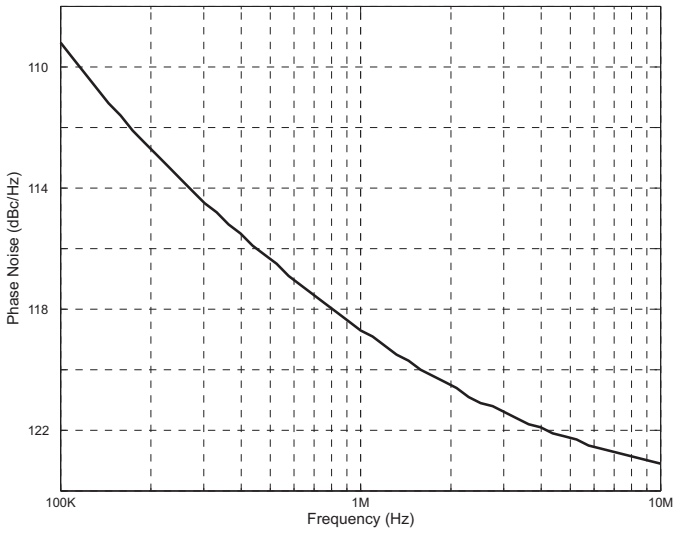

Figure 5.11: Simulated phase noise of VCO.

Active inductor VCOs are a viable option for UWB frequency synthesizers. They offer a large tuning range and meet the phase noise specification of UWB. The major problem using active inductor VCOs is high power consumption, mainly due to the large bias current. While a large bias current is not required for the operation of the VCO, it is, however, necessary for phase noise performance. If the signal swing is a large portion of the bias current then the active devices become highly non-linear and the inductance varies largely with the signal current, which shifts the resonance frequency of the LC tank. This shift causes the quality factor of the tank to drop at a low bias current. As a result, a high power consumption is required to ensure that the phase noise meets the specifications.

5.3 Wide-Band Hybrid VCO with Active-Inductor Load

The active inductor VCO presented in the previous section has a large frequency tuning range but suffers from high-power consumption. Large power consumption is required to reduce phase noise

performance. The active devices that compose the active inductor become highly non-linear when the VCO has a large output voltage swing. To minimize the phase noise reduction due to the large signal swing the bias current must be increased. With a low bias current the large frequency tuning range is still maintained, so a means to obtain both good phase noise performance and a large frequency tuning range, and low-power consumption will be explored.

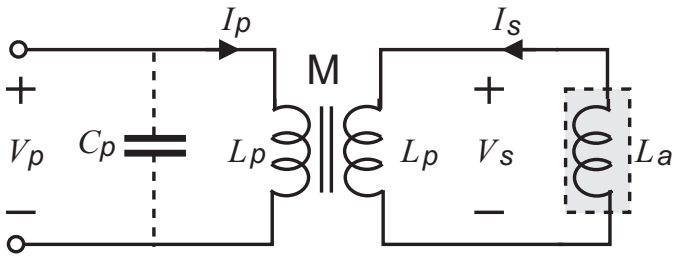

Figure 5.12: Ideal transformer loaded with an active inductor.

Fig.5.12 shows a transformer loaded with an active inductor. To simplify the analysis of the total inductance, both the transformer and the active inductor are assumed to be ideal. Writing KCL for both the primary and secondary windings without considering the capacitors yields

$$\begin{aligned} V_p &= sL_pI_p + sMI_s, \\ sMI_p + sL_sI_s + \frac{I_s}{sC_v} &= 0, \end{aligned} \tag{5.6}$$

where L_p , L_s , and L_a are the self inductance of the primary winding, that of the secondary winding of the transformer, and the inductance of the active inductor, respectively, M is the mutual inductance of the transformer. Note that $M = k\sqrt{L_pL_s}$ where k is the coupling factor. The current of the secondary winding is obtained from (5.6)

$$I_s \approx \frac{M}{L_a}I_p, \tag{5.7}$$

where we have assumed $L_a > L_s$ to simplify analysis. The equivalent inductance seen from the primary winding of the transformer is given by

$$L_{eq} = L_p(1 + k_a^2), \tag{5.8}$$

where $k_a = \frac{M}{\sqrt{C_p L_a}}$ is the effective coupling factor of the transformer loaded with the active inductor. It is seen from (5.8) that the equivalent inductance L_{eq} can be tuned by varying the inductance of the active inductor. The resonant frequency of the LC network formed by C_p and the inductance seen from the primary winding of the transformer is given by

$$\omega_o = \frac{1}{\sqrt{C_p L_p}} \left(\frac{1}{\sqrt{1 + k_a^2}} \right). \tag{5.9}$$

The first term on the right hand side of (5.9) quantifies the self-resonant frequency of the transformer network without the active inductor while the second term specifies the amount of the shift of the resonant frequency when the active inductor is connected to the secondary winding of the transformer. The tuning range of the resonant frequency of the transformer loaded with the active inductor can be determined from the tuning range of L_{eq} . Assuming that the inductance tuning range of the active inductor is given by $L_{a,min} \leq L_a \leq L_{a,max}$, Eq. (5.8) becomes

$$\Delta L_{eq} = L_p \frac{M^2}{L_{a,min} L_{a,max} C_p} \Delta L_a, \tag{5.10}$$

where $\Delta L_{eq} = L_{eq,max} - L_{eq,min}$ and $\Delta L_a = L_{a,max} - L_{a,min}$. Eq.(5.10) reveals that to increase the frequency tuning range, the mutual inductance M and inductance tuning range of the active inductor ΔL_a should be maximized.

Active inductors exhibit a high level of noise as compared with their spiral counterparts. The contribution of the noise of the active inductor connected to the secondary winding of the transformer to the noise seen at the primary winding of the transformer can be determined by assuming that the transformer is noiseless and representing the noise of the active inductor with its noise-voltage generator $\overline{V_a^2}$ and noise-current generator $\overline{I_a^2}$, as shown in Fig.5.13. Consider Fig.5.13

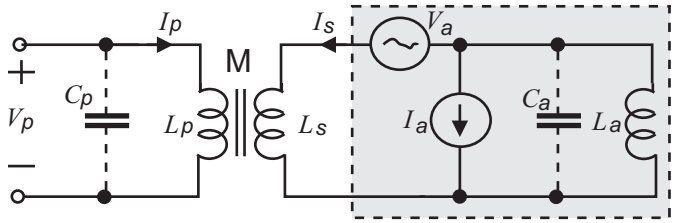

Figure 5.13: Noise analysis of noiseless passive transformer loaded with a noisy active inductor.

without the capacitance of the active inductor. We assume that V_a and I_a are uncorrelated to simply analysis. The noise voltage on the primary as a result from noise sources on the secondary are given by

$$V_p = sL_p(1 + k_a^2) + \frac{M}{L_1}V_a + sMI_a. \tag{5.11}$$

The first term on the right hand side of (5.11) is the voltage of the primary winding without considering the noise of the active inductor while the remaining terms quantify the contribution of the noise of the active inductor to the noise seen at the primary winding of the transformer with its power given by

$$\overline{V_{np}} = \left(\frac{M}{L_a}\right)\overline{V_a^2} + (\omega M)^2\overline{I_a^2}. \tag{5.12}$$

Eq.(5.12) reveals that the contribution of the noise of the active inductor can be reduced by lowering the mutual inductance. This, however, will also lower the frequency tuning range, providing a trade off between noise and tuning range. Also observed is that the larger L_a , the lower $\overline{V_{np}^2}$.

To quantify the effect of the active inductor connected to the secondary winding of the transformer on the overall quality factor of the transformer network, we assume that the transformer is ideal and representing the active inductor is modeled with an ideal inductor L_a in series with a resistor R_a , as shown in Fig.5.13. We neglect R_p , the series resistance of the primary winding for

the time being. The impedance looking into the primary winding of the transformer is given by

$$Z_p = \frac{1}{R_a}\frac{s^2(L_aL_p - M^2) + sL_pR_a}{\frac{s}{\omega_z} + 1}, \tag{5.13}$$

where $\omega_z = \frac{R_a}{L_a}$ is the lower frequency bound of the active inductor. Since the active inductor is inductive only when $\omega_z < \omega < \omega_a$, (5.13) can be simplified by utilizing $\frac{s}{\omega_z} + 1 \approx \frac{s}{\omega_z}$.

$$Z_p \approx sL_p(1 + k_a^2) + n_aR_a, \tag{5.14}$$

where $n_a = \frac{L_p}{L_a}$ is the effective turn ratio of the transformer. Eq.(5.14) reveals that the transformer network can be represented by an inductor of inductance $L_{eq} = L_p(1 + k_a^2)$ in series with a resistor of resistance $R_{eq} = n_aR_a$. The quality factor of the transformer network is obtained from

$$Q = \frac{\omega L_{eq}}{R_{eq}} = Q_a(1 + k_a^2) \tag{5.15}$$

where $Q_a = \frac{\omega L_a}{R_a}$ is the quality factor of the active inductor. Eq. (5.15) reveals that the quality factor of the transformer network is better than that of the active inductor. It should be emphasized that the preceding results were derived without considering the loss of the windings of the transformer and the parallel parasitic resistance of the active inductor.

When the series resistance of the primary winding is considered, the impedance looking into the primary winding of the transformer becomes

$$Z_p \approx sL_p(1 + k_a^2) + (n_aR_a + R_p) + \frac{R_aR_p}{sL_a}. \tag{5.16}$$

Eq. (5.16) was derived by assuming $L_a \gg L_s$ and $R_p \gg R_s$ where R_s is the series resistance of the secondary winding. The quality factor of the transformer network in this case is estimated from

$$Q \approx Q_a\left(\frac{1 + k_a^2}{1 + \frac{R_p}{R_a}\frac{L_a}{L_p}}\right). \tag{5.17}$$

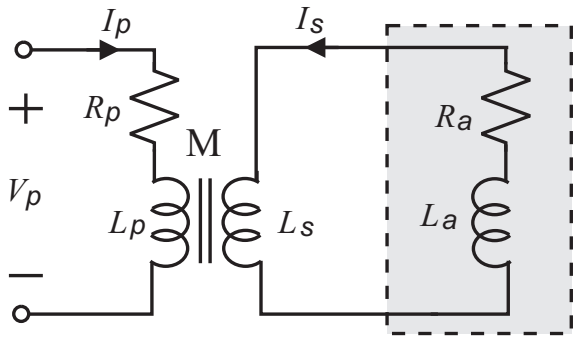

Figure 5.14: Quality factor analysis of passive transformer loaded with an active inductor.

The schematic of the proposed passive transformer VCO with active inductor frequency tuning is shown in Fig. 5.15. The spiral transformer is stack-configured to maximize the coupling factor. Further, it is step-down configured with turn ratio $\frac{N_p}{N_s} = \frac{3}{2}$ such that the voltage swing of the primary winding can be large in order to cope with the large voltage swing of the oscillating nodes while the voltage swing of the secondary winding is kept small to minimize the nonlinear effect of voltage swing on the inductance of the active inductor. For the purpose of comparison, the spiral VCO shown in Fig. 5.15(b) and the active inductor VCO shown in Fig.5.15(c) have also been designed in IBM CMRF8SF-0.13m 1.2V CMOS technology. The oscillators are analyzed using Spectre from Cadence Design Systems with BSIM4 device models.

Fig. 5.16 shows the frequency tuning curve of the proposed VCO. The frequency tuning range of the proposed VCO is approximately 6.5-10 GHz. The frequency tuning range of the active inductor VCO is found to be 0-7 GHz approximately. Fig. 5.17 shows the phase noise of these VCOs. The phase noise of the spiral inductor VCO and that of the proposed VCO are evaluated at 7.9 GHz whereas that of the active inductor VCO is evaluated at 4 GHz. It is seen that the phase noise of the proposed VCO is significantly lower as compared with that of the active inductor VCO. The phase noise of the active inductor VCO, the spiral inductor VCO, and the proposed VCO at 1 MHz frequency offset is -80.18 dBc/Hz, -106.9 dBc/Hz, and -100.5 dBc/Hz, respectively. The

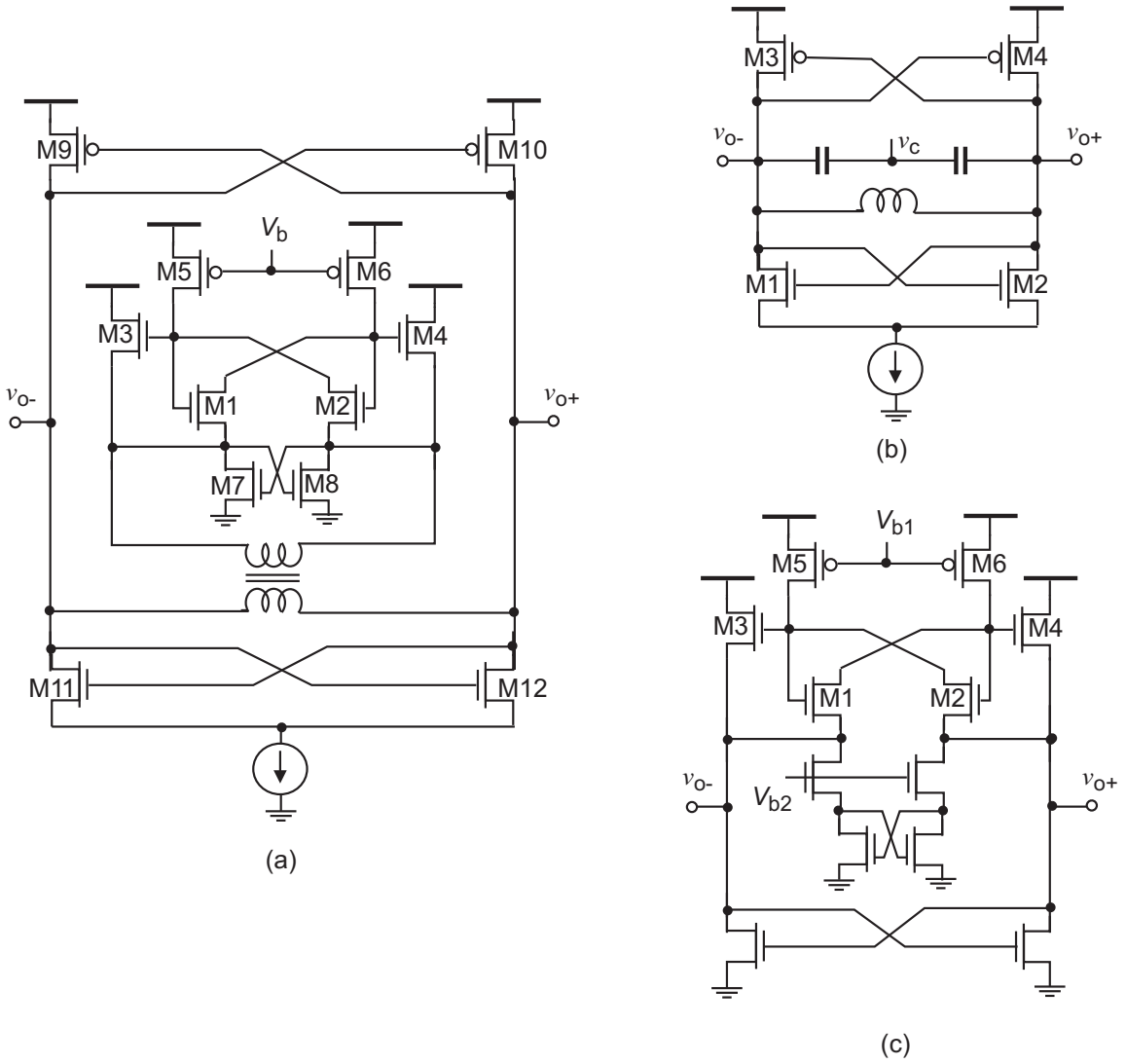

Figure 5.15: (a) Proposed VCO. (b) Spiral inductor VCO. (c) Active inductor VCO.

layout of the transformer is shown in Fig. 5.18. The output of the VCO is buffered with two source followers that are loaded with spiral inductors to boost the amplitude of the output voltage. The power consumption of the passive VCO, active inductor VCO, and the proposed VCO is 4 mW, 25

mW, and 29 mW, respectively.

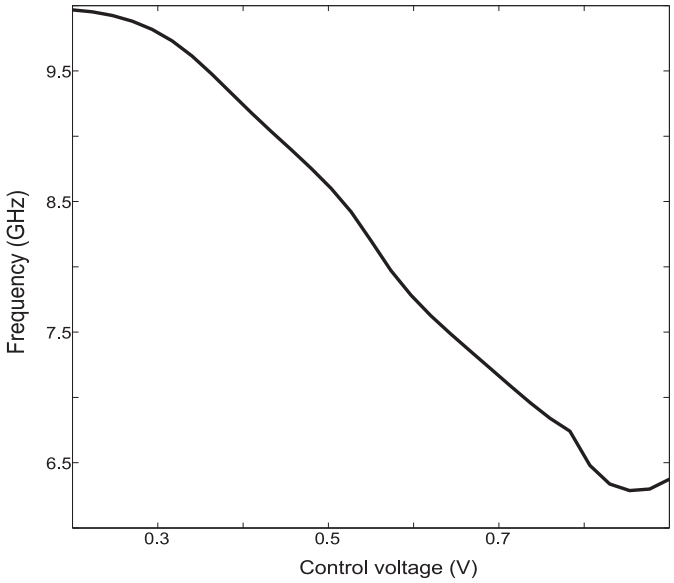

Figure 5.16: Simulated frequency tuning of proposed VCO.

5.4 Wide-Band Hybrid VCO with Varactor Load

Varactors are characterized by their high quality factor. The effective quality factor of an LC-tank constituted by a spiral inductor and a varactor is mainly determined by that of the spiral inductor. Various techniques such as pattern-shielding in the substrate and using thick metals for spirals have been proposed to increase the quality factor of spiral inductors. The former has limited improvement while the latter is typically not available in low-cost CMOS technologies. Spiral transformers have also been used as a viable means to improve the quality factor [72]. The increase of the quality factor is achieved by increasing the overall inductance of the winding by including the mutual inductance with a small increase in the winding resistance. This is known as transformer feedback [19, 73].

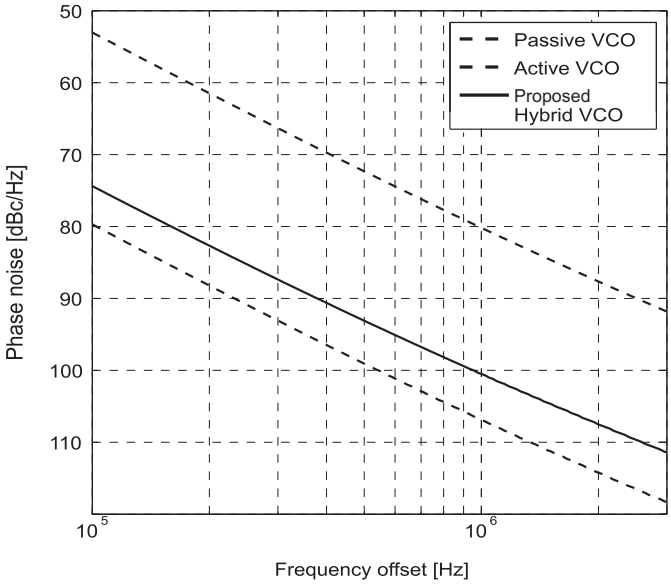

Figure 5.17: Simulated phase noise of spiral inductor VCO, active inductor VCO, and proposed VCO (labeled Hybrid VCO).

Several design techniques have been proposed to increase the frequency tuning range of transformer VCOs [74, 75, 76].

In this thesis, we propose a new technique to increase the frequency tuning range of LC-tank oscillators without sacrificing phase noise performance [77]. The proposed technique employs a step-up transformer loaded with a varactor at the secondary winding. By placing the varactor at the secondary winding, its impedance is reflected to the primary winding, increasing the desired variable capacitance.

Fig. 5.19 shows a transformer loaded with a varactor. To simplify the analysis, both the transformer and the varactor are assumed to be ideal. Writing KCL for both the primary and secondary windings without considering the winding capacitance yields

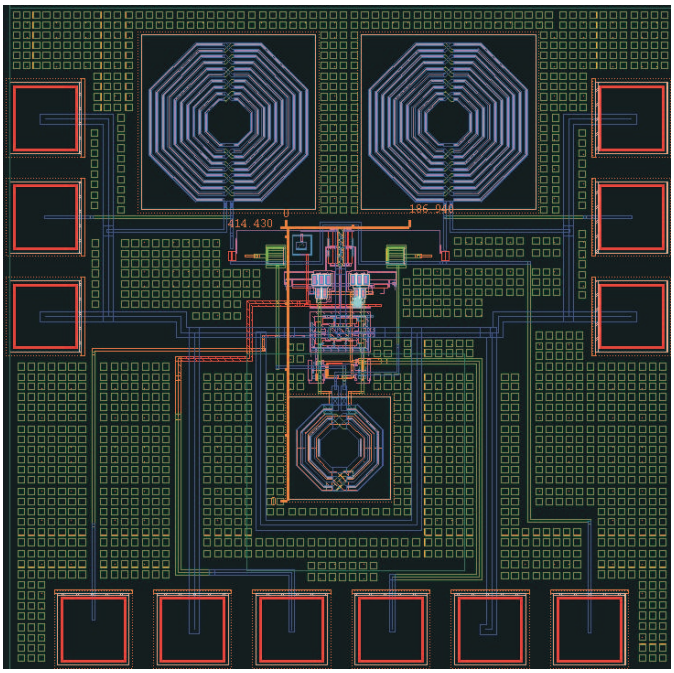

Figure 5.18: Layout of proposed VCO.

$$V_p = sL_pI_p + sMI_s,$$
$$sMI_p + sL_sI_s + \frac{I_s}{sC_v} = 0, \tag{5.18}$$

where L_p, L_s and C_v are the self inductance of the primary winding, that of the secondary winding, and the capacitance of the varactor, respectively, and M is the mutual inductance. The current of the secondary winding is obtained from (5.18)

$$I_s = \frac{MI_p}{L_s}\left(\frac{1}{s^2 + \omega_{o,s}^2}\right), \tag{5.19}$$

where $\omega_{o,s} = \dfrac{1}{\sqrt{L_sC_v}}$ is the self-resonate frequency of the secondary winding. The inductance

seen from the primary winding is given by

$$L_{eq} = L_p \left(1 + \frac{k^2}{s^2 + \omega_{o,s}^2}\right). \tag{5.20}$$

It is seen from (5.20) that L_{eq} can be tuned by varying the capacitance of the varactor. The resonant frequency of the primary winding is given by

$$\omega_{o,p} = \frac{1}{\sqrt{C_p L_p}} \left(\frac{1}{\sqrt{1 + \frac{k^2}{s^2+\omega_{o,s}^2}}}\right). \tag{5.21}$$

The first term on the right hand side of (5.21) quantifies the self-resonant frequency of the primary winding without the varactor while the second term specifies the amount of the shift of the resonant frequency when the varactor is connected to the secondary winding. The tuning range of the resonant frequency of the primary winding of the transformer loaded with the varactor can be determined from the tuning range of L_{eq}. Assuming that the capacitive tuning range of the varactor is given by $C_{v,min} \leq C_v \leq C_{v,max}$, (5.19) becomes

$$\Delta L_{eq} \approx \frac{M^2 \omega_o}{(s^2 + \omega_o^2)^2} \Delta C_v, \tag{5.22}$$

where $\Delta L_{eq} = L_{eq,max} - L_{eq,min}$ and $\Delta C_v = C_{v,max} - C_{v,min}$. Eq. (5.22) reveals that to increase the frequency tuning range, the mutual inductance M and capacitance tuning range of the varactor ΔC_v should be maximized.

The contribution of the noise of the varactor to the noise seen at the primary winding can be determined by assuming that the transformer is noiseless and representing the noise of the varactors with its noise-voltage generator $\overline{V_n^2}$ and noise-current generator $\overline{I_n^2}$, as shown in Fig. 5.20. If we assume that V_n and I_n are uncorrelated to simply analysis the noise voltage on the primary resulting from a noise source on the secondary is given by

$$V_p = sL_p(1 + \chi) + \frac{M}{L_s} V_n + sMI_n, \tag{5.23}$$

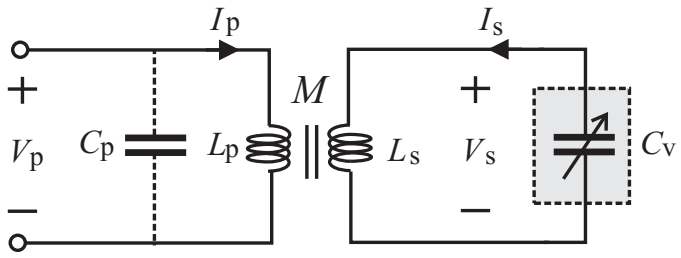

Figure 5.19: Ideal transformer loaded with a varactor.

where

$$\chi = \frac{k^2}{s^2 + \omega_{o,s}^2}. \tag{5.24}$$

The first term on the right hand side of (5.23) is the voltage of the primary winding without considering the noise of the varactor while the remaining terms quantify the contribution of the noise of the varactor to the noise seen at the primary winding. The noise power at the primary winding is given by

$$\overline{V_{np}^2} = \left(\frac{M}{L_s}\right)^2 \overline{V_n^2} + (\omega M)^2 \, \overline{I_n^2}. \tag{5.25}$$

Eq.(5.25) reveals that the contribution of the noise of the varactor can be reduced by lowering the mutual inductance. This, however, also lowers the frequency tuning range, providing a trade off between noise and frequency tuning range.

Spiral inductors typically have a quality factor ranging from 5-15 while quality factors larger than 50 are common for varactors. The quality factor of an LC tank is therefore dominated by that of the spiral inductor. However, using the reflected impedance of the varactor to increase the tuning range no longer warrants neglecting of the quality factor of the varactor. To quantify the effect of the varactor connected to the secondary winding on the overall quality factor of the primary winding, we assume that the transformer is ideal and we represent the varactor with an ideal capacitor C_v in series with a resistor R_s, as shown in Fig. 5.21. By neglecting R_p the impedance looking into the

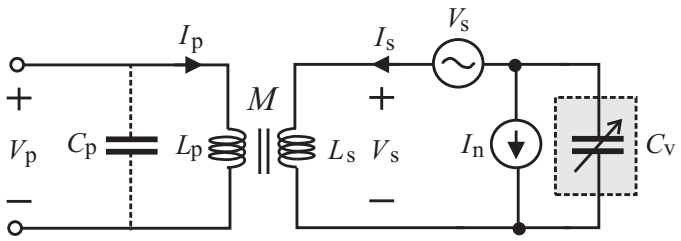

Figure 5.20: Noise analysis of noiseless passive transformer loaded with a noisy secondary circuit.

primary winding is given by

$$Z_p \approx sL_p(1+\chi) + nR_s, \tag{5.26}$$

where the turn ratio n is

$$n = \frac{L_p}{L_s}. \tag{5.27}$$

Eq. (5.26) reveals that the primary winding can be represented by an inductor of inductance $L_{eq} = L_p(1+\chi)$ in series with a resistor of resistance $R_{eq} = nR_s$. The quality factor of the primary winding is obtained from

$$Q_p = \frac{\omega L_{eq}}{R_{eq}} = Q_s(1+\chi), \tag{5.28}$$

where the quality factor of the secondary winding is given by

$$Q_s = \frac{\omega L_s}{R_s}. \tag{5.29}$$

When the series resistance of the primary winding is considered, the impedance looking into the primary winding of the transformer becomes

$$Z_p \approx sL_p(1+\chi) + (nR_s + R_p) + \frac{R_s R_p}{sL_s}. \tag{5.30}$$

Eq.(5.30) was derived by assuming $R_p \gg R_s$ where R_s is the series resistance of the secondary winding. The quality factor of the primary winding in this case is estimated by

$$Q_p \approx Q_s \left(\frac{1+\chi}{1 + \frac{R_p}{R_s}\frac{L_s}{L_p}} \right). \tag{5.31}$$

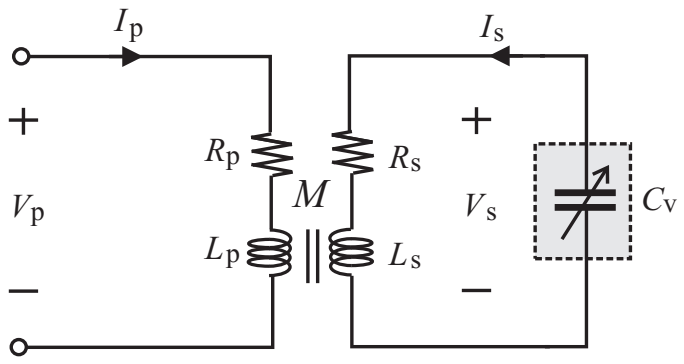

Figure 5.21: Quality factor analysis of transformer loaded with varactor.

The schematic of the proposed transformer VCO with reflected capacitance frequency tuning is shown in Fig. 5.22. The output of the VCO is buffered with two source followers that are loaded with spiral inductors to boost the output voltage. The transformer is stack-configured to maximize its coupling factor. Furthermore, it is step-up configured with a $\frac{N_p}{N_s} = \frac{2}{3}$ turn ratio such that an up-scaling of the secondary winding impedance into the primary winding is obtained. This increases the frequency tuning range of the VCO. The self-inductance of the secondary winding functions to tune out the fixed capacitance of the varactor, preventing it from being multiplied back to the primary winding circuit and reducing the frequency tuning range of the oscillator. The proposed VCO has been designed in IBM CMRF8SF-0.13μm 1.2V CMOS technology and analyzed using

Spectre from Cadence Design Systems with BSIM4 models. For the purpose of comparison, another VCO utilizing the same transformer with the same varactor loading to the primary winding was also designed and analyzed.

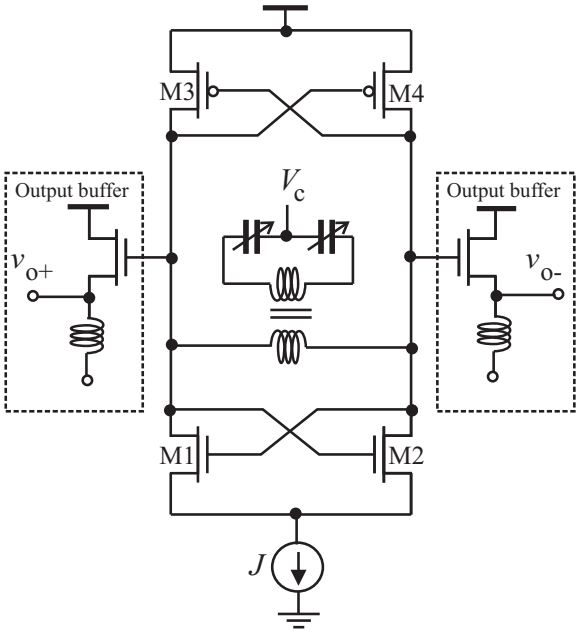

Figure 5.22: Schematic of transformer VCO with reflected capacitance frequency tuning. Circuit parameters : $W_{1,2} = 60\mu$m, $W_{3,4} = 80\mu$m, tail current source : nMOS transistor with $W = 250\mu$m $L = 2\mu$m, V=1V. The buffer is a differential pair with a balun load, the nMOS transistors are the same size as the core ones, and the balun is 9.8 nH. Varactor : $L = 2\mu$m, $W = 64\mu$m.

Fig.5.23 shows the frequency tuning curve of the proposed VCO. The frequency range of the VCO with the varactor loading the primary winding is 8.2-10.1 GHz. The frequency tuning range of the proposed VCO with the varactor loading the secondary winding is 7.25-10.2 GHz. A 64% increase in the frequency tuning range is obtained.

Fig.5.24 compares the phase noise of the two VCOs. It is seen that the phase noise of the

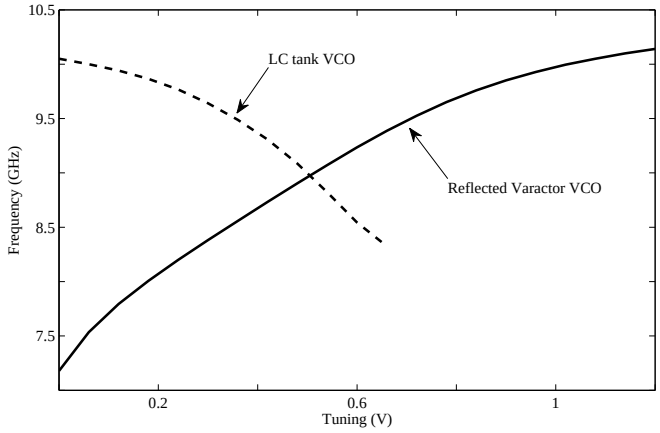

Figure 5.23: Simulated frequency tuning of VCO with varactor loading the secondary and primary windings.

proposed VCO is comparable to that with varactor loading the primary winding. The phase noise of the VCO with varactor loading the primary winding and that of the VCO with varactor loading the secondary winding are - 109 dBc/Hz and -111 dBc/Hz at 1 MHz frequency offset, respectively.

The layout of the proposed VCO is shown in Fig. 5.28. The configuration of the stacked transformer is shown in Fig.5.28 and the micro photo of the fabricated chip in Fig. 5.29. The primary winding stacked on the top of the secondary winding.

5.5 Performance Comparison

Table. 5.1 tabulates the performance metrics of the three presented wide band oscillators and compares them to existing wide band VCOs. It is clear from the performance comparison that the active inductor is able to achieve a large frequency tuning range with good phase noise performance. The cost of high phase noise performance is high power consumption. The active inductor hybrid takes advantage of the large frequency tuning range of the active inductor and the phase noise performance of the passive transformer. The varactor loaded hybrid VCO is able to achieve good phase

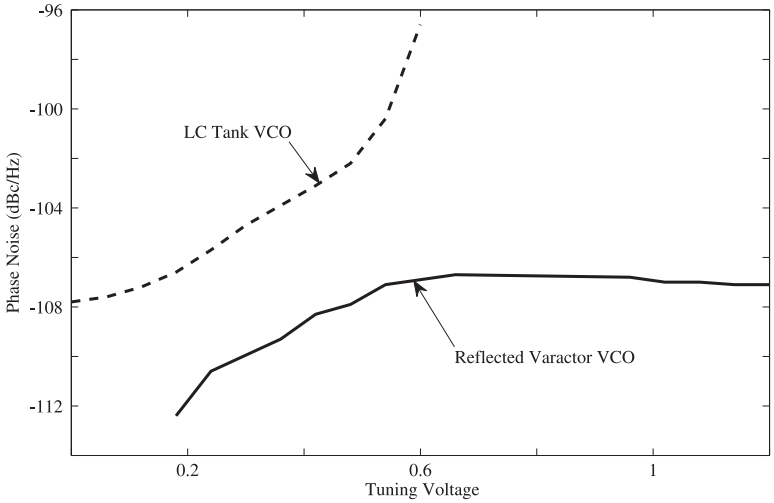

Figure 5.24: Phase noise of VCO with varactor loading the secondary and primary windings.

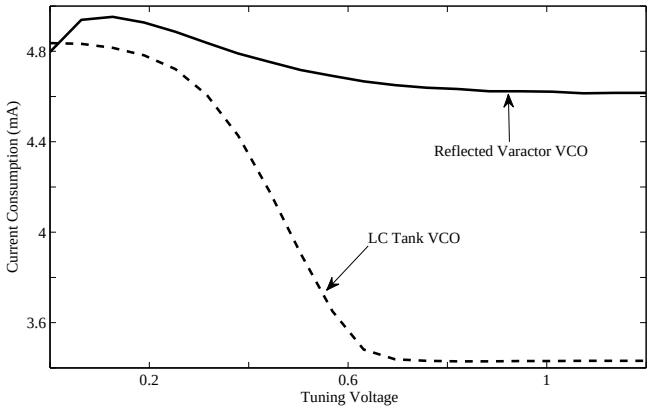

Figure 5.25: Power consumption of VCO with varactor loading the secondary and primary windings.

noise performance, low power consumption and still retains a wide frequency tuning. All of the

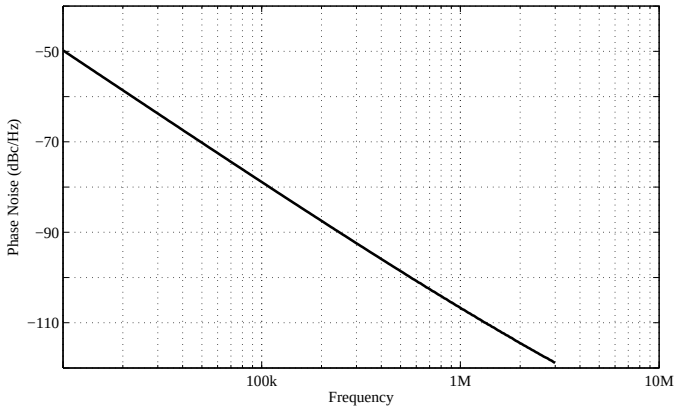

Figure 5.26: Phase noise plot of the proposed VCO.

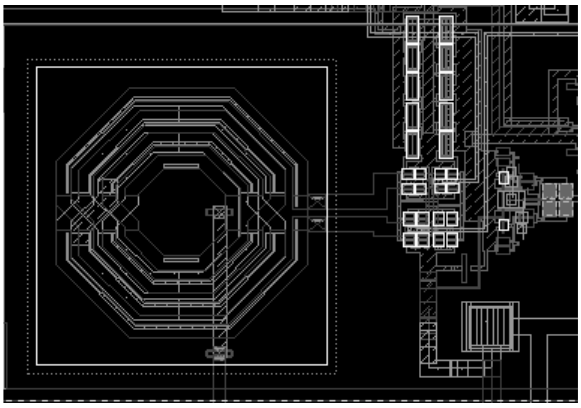

Figure 5.27: Layout of proposed VCO.

VCOs are capable of providing a large frequency tuning range without resorting to bank switching networks.

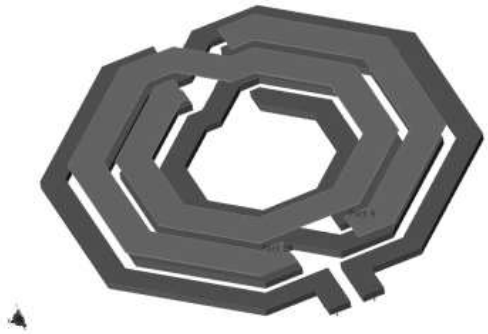

Figure 5.28: Configuration of the transformer used in the hybrid VCO.

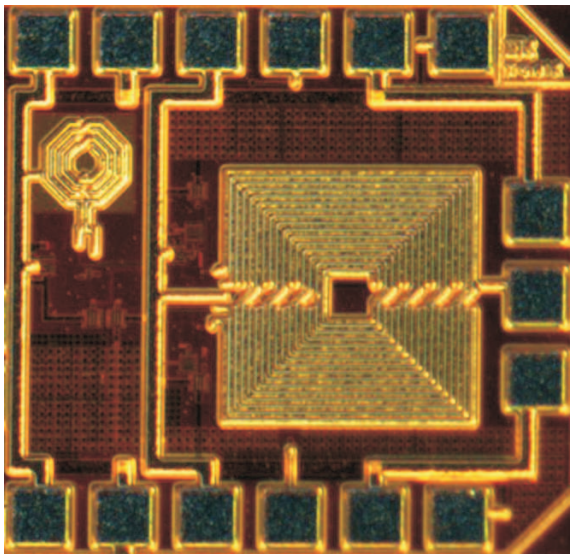

Figure 5.29: Die photo of the transformer used in the hybrid VCO.

5.6 Chapter Summary

The development of wide frequency tuning range VCOs without switched bank networks has been presented. We have shown that active-inductor VCOs exhibit good phase noise performance and

Table 5.1: Comparison of wide band VCOs .

Ref.	Technology	Center freq. [GHz]	Power [mW]	Phase Noise [dBc/Hz]	Bit Select	Tuning Range [%]
[65]	0.13um CMOS	4	10.5	-120	9	37
[78]	0.18um CMOS	5.6	30.9	-75	n/a	64
[63]	0.18um CMOS	1.12	9	-118	6	64
[67]	65nm CMOS	11.45	3.48	-99	6	126
[61]	0.13um CMOS	4.28	5	-119	3	39
[62]	0.13um CMOS	4.8	1.2	-113	3	37
[66]	0.18um CMOS	3.71	7.02	-124	3	39
[68]	0.13um CMOS	3.2	n/a	-124	2	87
[69]	0.13um CMOS	5.2	8	-101	3	69
Active Inductor	0.18um CMOS	1.6	45	-118	n/a	69
Active Inductor Hybrid	0.18um CMOS	8	29	-100	n/a	43.7
Varactor Hybrid	0.13um CMOS	8.73	5.76	-111	n/a	33.8

provide a wide frequency tuning range, at the cost of high power consumption. Hybrid oscillators that utilize the wide frequency tuning of active inductors and the low noise of passive transformers have been proposed. Hybrid oscillators that employ a passive transformer loaded with a varactor have also been proposed. The impedance transformation of the transformer boosts the frequency tuning range of the oscillators while maintaining low phase noise. These hybrid VCOs meet the specifications of the first mode of UWB.

Chapter 6

UWB Current-Mode Frequency Synthesizer

This chapter proposes a frequency synthesizer for UWB. The proposed frequency synthesizer uses current-mode architecture investigated in Chapter 5. It introduces a new hopping scheme for fast locking. This chapter starts with an introduction of the fast hopping scheme that will be utilized for the MB-OFDM UWB current-mode frequency synthesizer. The quick hopping scheme will allow a traditional integer PLL based frequency synthesizer to lock in 9.5 ns, as required by MB-OFDM UWB. Section 6.2 discusses a wide frequency tuning range VCO that is suitable for current-mode MB-OFDM UWB frequency synthesizers. Section 6.3 studies a bang-bang phase detector for MB-OFDM frequency synthesizers. Section 6.4 investigates an injection loxking frequency divider. Section 6.5 contains simulation results of the entire current-mode UWB frequency synthesizer, and comparisons to published works. The chapter concludes in Section 6.6

6.1 Quick Hopping for UWB Frequency Synthesizer

A fast-locking frequency synthesizer consists of a phase detector, a CCO, an ILO and a loop filter with a controllable switching current, as shown in Fig. 6.1. Usually an ILO pre-scaler is used to reduce the frequency and power consumption of the $\frac{1}{N}$ frequency divider, but in the quick hopping scheme the ILO acts as a programmable divider.

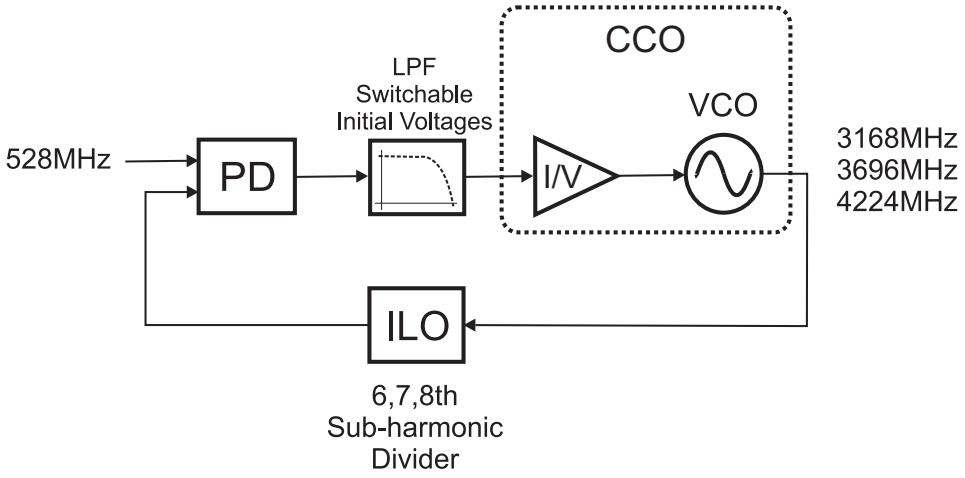

Figure 6.1: Architecture of a frequency synthesizer utilizing the quick hopping scheme.

The loop filter is a typical current-mode loop filter, and can switch to a fixed current output. By switching to this prefixed current the CCO is instantly forced to oscillate at a pre-set frequency. By having multiple prefixed values to jump to, the CCO frequency can be rapidly shifted. The schematic of the fast-hopping current-mode loop filter is shown in Fig. 6.2. The filter differs from normal current-mode loop filters by adding a switched-capacitor bank. By switching in a capacitor with a pre-charged value and the old capacitor out a new loop filter current is generated. Each UWB sub-channel is assigned a capacitor and each capacitor is precharged with a specific voltage.

As the capacitors are switched out of the circuit they can be slowly trickle charged or discharged

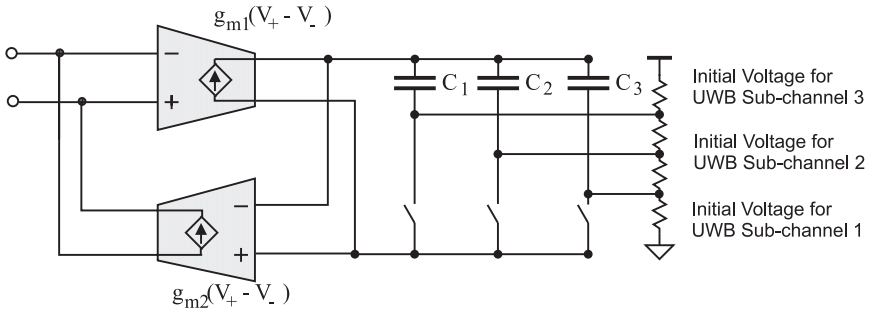

Figure 6.2: Schematic of proposed Mixer for frequency translation.

to the proper voltage. The prefixed value stored on the capacitor will cause the CCO to jump to a new frequency, which is approximately the frequency of a UWB sub-channel. Fig. 6.3 shows a typical tuning curve of a VCO transposed on top of the sub-harmonic lock range of the ILO. In the tuning range of the VCO there are three sub-harmonics in the ILO locking range. In the lower tuning range of the VCO there is the tuning range of the 6th subharmonic. As the control signal increases VCO frequency will exceed the lock range of the 6th sub-harmonic. As the control signal continues to increase VCO frequency will fall into the 7th sub-harmonic lock range. These sub-harmonics spread across the tuning range of the VCO. If the UWB frequency synthesizer is locked to the 6th sub-harmonic, a command will be sent to switch out the current capacitor and the 2nd capacitor will be switched in. The 2nd capacitor is pre-charged and causes the frequency synthesizer to shift VCO frequency. The new frequency will be within the lock range of the ILO's 7th sub-harmonic. The frequency synthesizer's feedback will cause the VCO to shift and lock to the 7th sub-harmonic of the reference frequency. This process is repeated and the UWB frequency synthesizer hops from one channel to another.

Unfortunately, UWB sub-channels are not an integer multiple of any reference frequency. With a reference frequency of 528 MHz, the required division ratios for the first three UWB sub-channels are 6.5, 7.5 and 8.5. The 0.5 division ratio is difficult to realize. Instead of trying to add an additional 0.5 division in the feedback loop the proposed frequency synthesizer will operate at twice

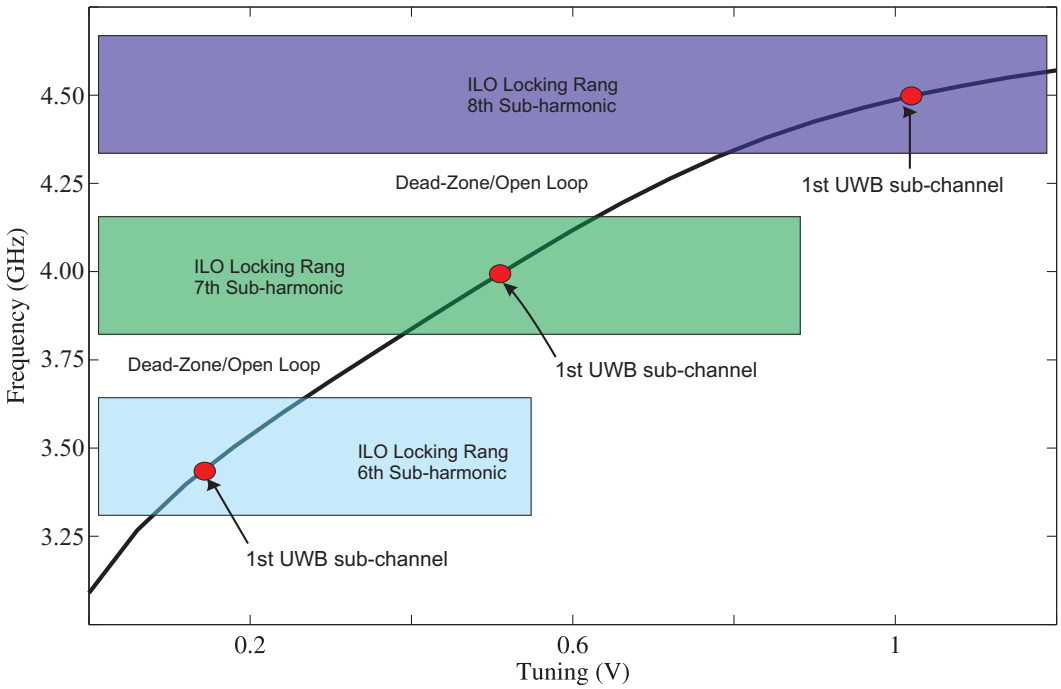

Figure 6.3: CCO tuning curve showing the UWB sub-channels including the locking range of the ILO.

the required frequency. By doubling the reference frequency the division ratios become 6, 5, and 8. Doubling the frequency will require the CCO to have twice the frequency tuning range, requiring over 3 GHz frequency range for the first 3 UWB channels. Doubling the frequency has two key advantages, increased loop bandwidth and quadrature generation. By doubling the reference frequency we can double the loop bandwidth, which will decrease the lock time. The second advantage is that the output divide-by-2 will provide a quadrature output, eliminating the need for a phase shifter or quadrature VCO. The final frequency synthesizer topology is shown in Fig. 6.4.

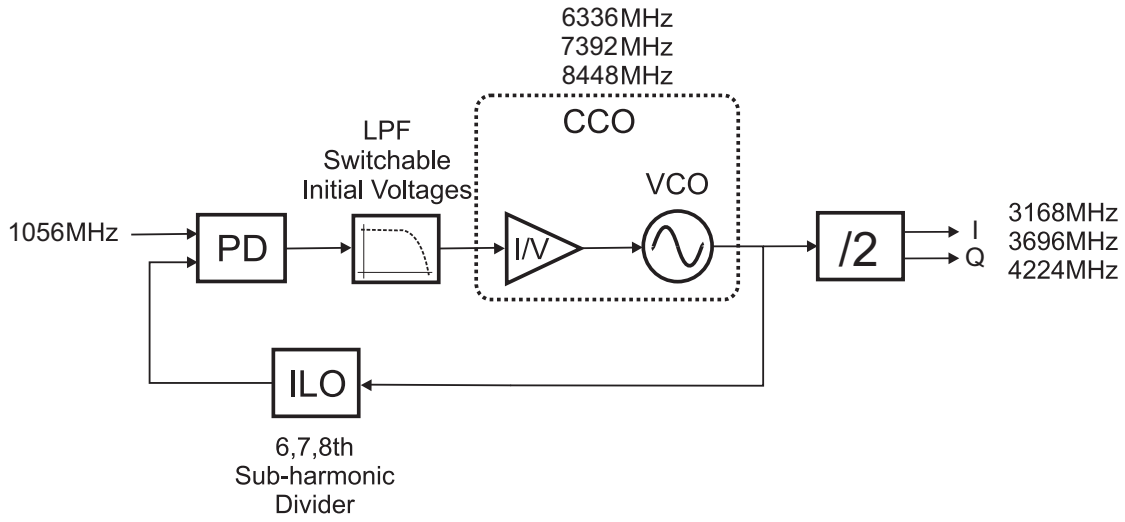

Figure 6.4: Final topology of the current-mode UWB frequency synthesizer.

6.2 Wide-Band VCO

The wide-band hybrid VCO with varactor load from chapter 5 will be used in the UWB Current-Mode Frequency Synthesizer and is redrawn in Fig. 6.5 for convenience. The VCO uses the impedance scaling properities of a passive spiral transformer to increase the capacitance tuning range of a varactor used to load the secondary winding. The increased capacitance tuning range results in a large frequency tuning range of the primary winding circuit.

Additional varactors were added to the secondary winding from the VCO presented in chapter 5 to reduce the VCO's center oscillation frequency to the second UWB band. The re-tuned frequency tuning range is shown in Fig. 6.6. The VCO is able to span XX GHz, allowing it the ability to tune to all three of the lower UWB bands.

The phase noise of the wide-band hybrid VCO with varactor load is shown in Fig. 6.7, the phase noise at 1 MHz is -108 dBc/Hz, which is lower than that required by the UWB specification.

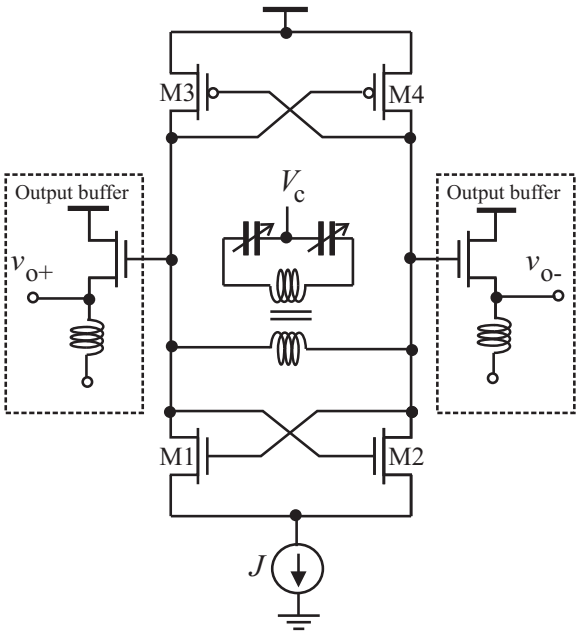

Figure 6.5: Schematic of transformer VCO with reflected capacitance frequency tuning. Circuit parameters : $W_{1,2} = 60\mu$m, $W_{3,4} = 80\mu$m, tail current source : nMOS transistor with $W = 250\mu$m $L = 2\mu$m, V=1V. The buffer is a differential pair with a balun load, the nMOS transistors are the same size as the core ones, and the balun is 9.8 nH. Varactor : $L = 2\mu$m, $W = 64\mu$m.

6.3 Bang-Bang Phase Detector

The phase detector for the proposed current-mode frequency synthesizer is a bang-bang phase detector, with the schematic shown in Fig. 6.8. The bang-bang phase detector is composed of two back-to-back TSPC latches to form a D Flip-Flop. The transfer function of the bang-bang phase detector is shown in Fig. 6.9. The ouput is either high or low depending on which phase is leading. The bang-bang phase detector has a very large gain, resulting in a fast lock. When the frequency synthesizer is phase and frequency locked the output of the bang-bang phase detector output will toggle as the VCO and reference phase will alternate between leading and lagging.

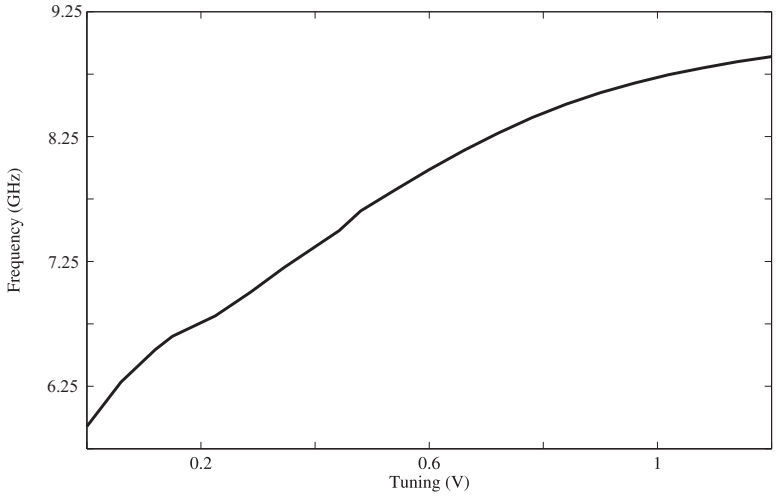

Figure 6.6: Simulated frequency tuning of VCO with varactor loading the secondary and primary windings.

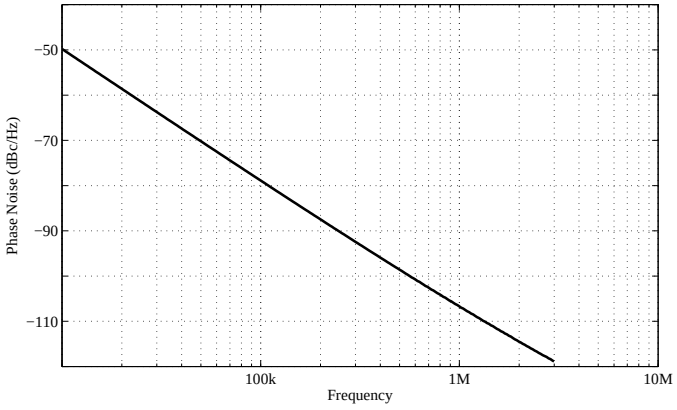

Figure 6.7: Phase noise plot of the Wide-Band Hybrid VCO with Varactor Load.

6.4 Injection locked Oscillator for Frequency Division

The schematic of the ILO used for frequency division is shown in Fig. 6.10. It consists of a pseudo-differential pair. An RC relaxation oscillator is used instead of an LC-tank oscillator because the

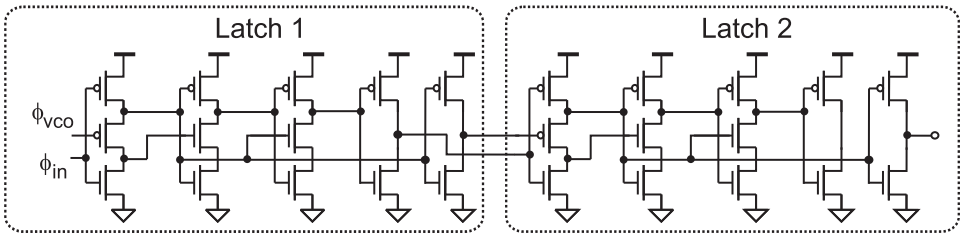

Figure 6.8: Schematic of bang-bang phase detector.

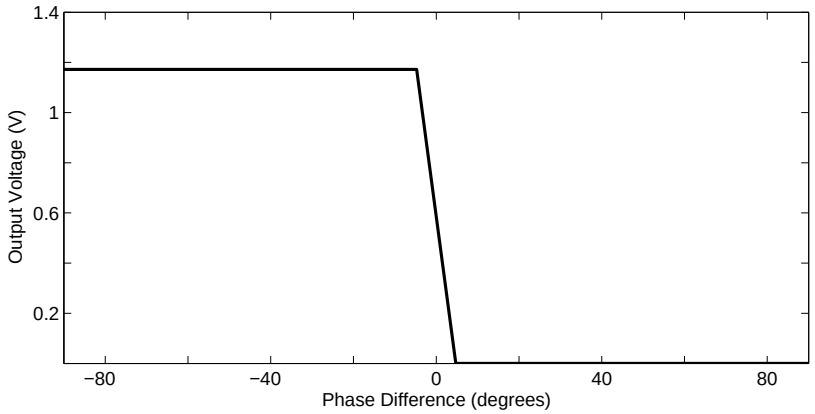

Figure 6.9: Output voltage of Bang-Bang phase detector.

locking range of LC-tank ILOs is small.

A large lock range is required for the proposed frequency divider ILO because the larger the lock range the lower the dead-zone in the VCO's tuning curve between the ILO's subharmonic lock ranges. When the VCO is inside the dead-zone, the frequency synthesizer is open loop and will drift to the channel above the dead-zone. To ensure that the VCO will not fall inside the dead-zone, the ILO's lock range must be maximized. The lock range of the proposed ILO is shown in Table. 6.1.

As the frequency difference increases the ILO requires more time to lock. The locking time of the ILO can be increased by increasing the bias current of the ILO, at the cost of power consumption.

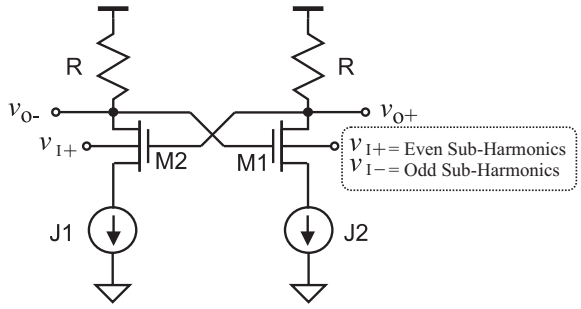

Figure 6.10: Schematic of proposed ILO.

Table 6.1: Locking range of ILO harmonics

Harmonic Number	Lower Frequency (GHz)	Upper Frequency (GHz)
6	6.145	6.559
7	7.152	7.666
8	8.310	8.655

The locking transient of the ILO is shown in Fig. 6.11. The layout of the ILO is shown in Fig.6.12.

6.5 Simulation Results

A current-mode UWB frequency synthesizer has been implemented in TSMC-0.13μm 1.2V 8-metal 1-poly CMOS technology and analyzed using SpectreRF from Cadence Design Systems with BIM3.3v device models. The frequency synthesizer is able to lock in the required 9.5 ns guard period. The locking transient is shown in Fig. 6.13, the synthesizer is switched between the first and third UWB bands. Due to the switching capacitor network the capacitances can be individually tuned to optimize the loop bandwidth and damping for each of the UWB bands.

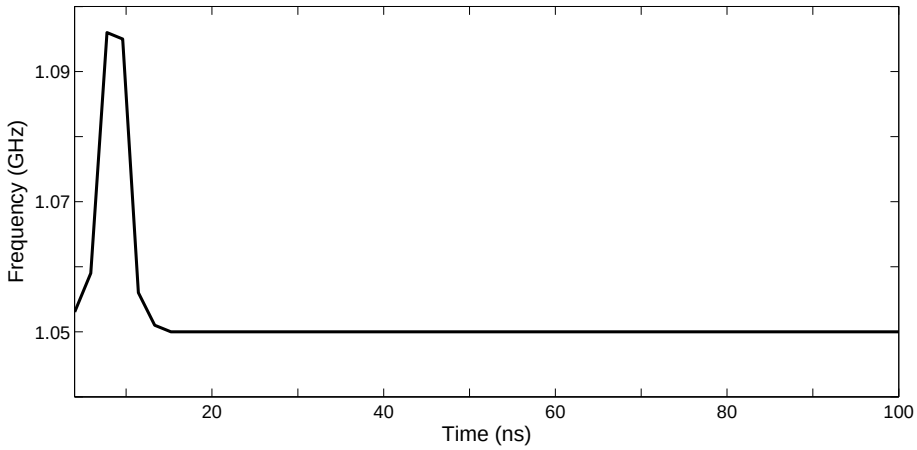

Figure 6.11: Locking transient of ILO.

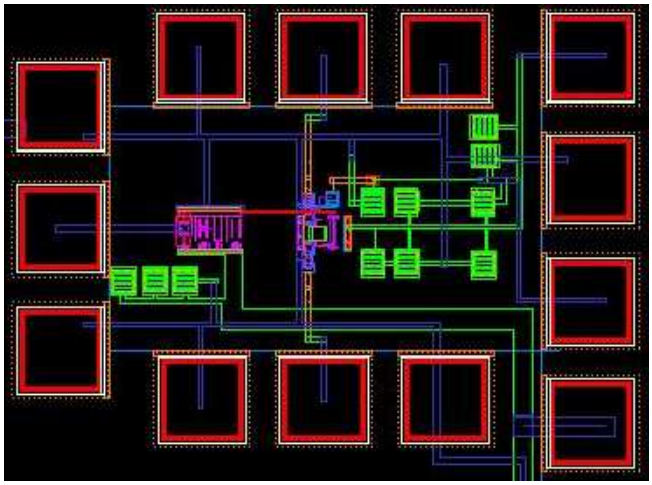

Figure 6.12: Layout of proposed ILO.

Table. 6.2 compares the proposed current-mode UWB frequency synthesizer to published UWB frequency synthesizers. Several key advantages proposed frequency synthesizer over published

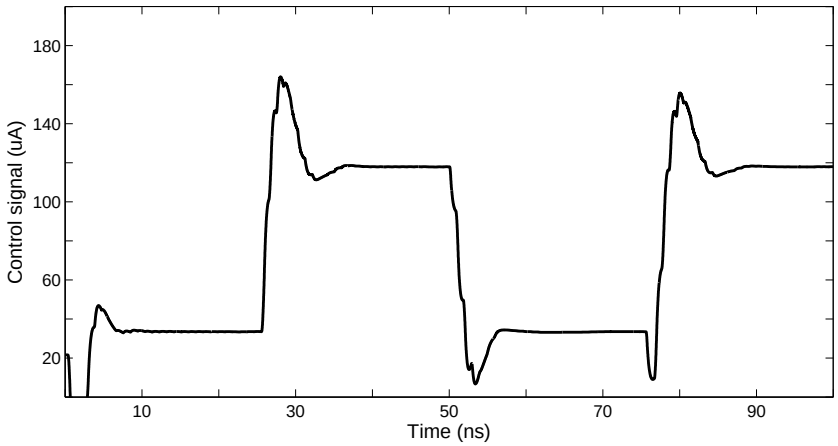

Figure 6.13: Locking characteristics of the proposed UWB Current-mode frequency synthesizer.

works becomes apparent:

- Low power consumption - because the proposed UWB frequency synthesizer does not use multiple single side band mixers its power is much lower than direct synthesis based UWB frequency synthesizers.
- No spur generation - because the proposed frequency synthesizer uses a closed loop PLL instead of frequency translation or non-linear frequency multiplication or division it does not generate significant spurs.

6.6 Chapter Summary

A current-mode frequency synthesizer for MB-OFDM UWB has been presented. It was shown that the proposed quick hopping scheme allowed the frequency synthesizer to hopping under 9.5 ns, meeting the MB-OFDM UWB requirement. The frequency synthesizer uses an ILO as its frequency divider. The frequency synthesizer doesn't contain a programmable divider to channel hop. Instead,

Table 6.2: Comparison of state-of-the-art UWB frequency synthesizers.

Ref.	Technology	Lock time [ns]	Spur Level [dBc]	Phase Noise [dBc/Hz]	Total Power [mW]	Power per Band [mW]
[14]	0.18um CMOS	8	-35	-120	54	18
[15]	0.18um CMOS	4	-25	-109	47	15.6
[25]	90nm CMOS	9	-32	-120	55	3.9
[16]	0.18um CMOS	2	-40	n/a	65	16.25
[17]	0.18um CMOS	1	-37	-103	48	6.85
[19]	0.18um CMOS	2.4	-20	n/a	34	11.3
[21]	0.18um CMOS	2	-26	-98	68	22.6
[29]	0.18um SiGe	3	-40	-130	88	12.6
[28]	0.18um CMOS	1	-37	-110	n/a	n/a
[22]	65nm CMOS	6	-43	-128	43	4.8
[23]	0.18um CMOS	3	-30	n/a	45	3.2
[24]	0.18um CMOS	3	-33	-98	117	8.3
This Work	0.13um CMOS	9	n/a	-108	8.5	2.83

it uses the sub-harmonic injection locking of an ILO to lock to a select sub-harmonics of the CCO output. To select which sub-harmonic the ILO locks to the CCO's oscillation frequency is forced to a new region of the frequency tuning curve. By applying a pre-set control signal value onto the loop filter the CCO can be shifted close to the UWB band. Once the CCO is in the proximity of the UWB band the feedback mechanism will ensure fast phase lock.

Chapter 7

Conclusions

7.1 Thesis Summary

This thesis dealt with the design of current-mode techniques for ultra wideband applications.

The FCC's two proposed standards for UWB transmission namely DS-UWB and MB-OFDM UWB had been discussed. DS-UWB uses the direct modulation of narrow pulses to represent the base-band data. It, however, is difficult to synchronize. MB-OFDM UWB uses more traditional narrow-band techniques by sub-dividing the ultra wide-band into a set of small bands of 528 MHz. A quick hopping protocol allows 9.5 ns guard time. The short guard time requires a loop bandwidth greater than the stability limit of PLL based frequency synthesizers. Three state-of-the-art UWB frequency synthesizers were presented: A DLL with edge combiner, a fixed frequency synthesizer with a programmable output frequency divider, and direct synthesis. All of the existing UWB frequency synthesizers suffer from output spurs.

An in-depth examination of the principle of current-mode filtering and its applications to PLLs was presented. Current-mode PLLs use currents as the control signal. The use of a current-mode signal allowed the decoupling of the control signal dynamic range from supply voltage scaling. Current-mode filtering can be accomplished using active inductors or active transformers. Active

inductors and active transformers offer the advantages of a small silicon area and a tunable inductance. Active inductors and active transformer current-mode filtering for PLLs was examined in detail. Type I and type II current-mode PLLs were developed using active inductors and active transformer. Type I and type II current-mode PLLs have similar loop bandwidth and damping parameters as their voltage-mode counterparts. Active transformer current-mode PLLs also have additional mutual coupling parameters in the tuning of the loop bandwidth and damping. The phase noise shaping from the noise sources in the PLL of a current-mode PLL was analyzed. The simulation results of an active inductor current-mode PLL and an active transformer current-mode PLL were presented.

Three wide frequency tuning range VCOs for MB-OFDM UWB were developed. It was shown that active inductor VCOs exhibit good phase noise performance and provide a wide frequency tuning range, at the cost of high power consumption. A hybrid oscillator that utilized the wide frequency tuning of an active inductor and the low noise of a passive transformer was analyzed. Another hybrid oscillator that employed a passive transformer loaded with a varactor was also developed. It was shown that the impedance transformation of transformers can boost the frequency tuning range of the oscillator while maintaining low phase noise. All three wideband VCOs were capable of providing large frequency tuning ranges without restoring to switch banked networks.

A current-mode frequency synthesizer for MB-OFDM UWB was developed. The quick hopping scheme enabled the frequency synthesizer to hop within 9.5 ns. The frequency synthesizer used an ILO as the frequency divider. The frequency synthesizer doesn't contain a programmable divider to channel hop. It uses sub-harmonic injection locking of an ILO to lock to a selective sub-harmonics of the CCO output. The CCO's oscillation frequency is forced to a new region of the frequency tuning curve to accomplish channel hopping. By applying a pre-set control signal value to the loop filter the CCO was forced to the proximity of the UWB band in which the feedback mechanism will result in phase and frequency lock.

7.2 FUTURE RESEARCH

The work reported in this thesis can be extended in the following directions:

1. Extending the active inductors and active transformers to compensate for process spread and supply voltage variation. This will allow the inductance of the active components to be better defined, especially when a large input is encountered.

2. Extending the pre-set voltage concept to adjust the VCO frequency directly instead of changing the control signal value. A common technique to extend the frequency tuning range of VCO is to switch capacitors in the LC-tank circuit. This will increase the tuning range of the VCO while reducing the VCO sensitivity leading to better phase noise.

3. Improving the design flow of hybrid varactor loaded oscillators. The design of hybrid oscillators requires laying out the proposed transformer in Cadence Virtuoso. The layout is imported into ADS finite element solver to generate an equivalent circuit network. Once ADS creates the equivalent circuit network the network is then imported back into Cadence to simulate VCO's frequency tuning range. This design procedure is slow and required a great effort to fine tune the transformer to adjust the free running frequency.

Appendix A

Publications

- D. DiClemente and F. Yuan, “A low phase noise large frequency tuning range CMOS voltage-controlled oscillator using spiral transformer and active inductor,” *Analog Integrated Circuits and Signal Processing*. Submitted in May 2011.

- D. DiClemente, F. Yuan, and A. Tang, “Current-mode phase-locked loops with CMOS active transformers,” *IEEE Transactions on Circuits and Systems II - Express Briefs*, Vol.55, No. 8, pp.771-775, August 2008.

- D. DiClemente and F. Yuan, “Current-mode phase-locked loops : a new architecture,” *IEEE Transactions on Circuits and Systems II - Express Briefs*, Vol. 54, No. 4, pp. 303 - 307, Apr. 2007

- D. DiClemente and F. Yuan, “A passive transformer voltage-controlled oscillator with reflected impedance frequency tuning,” Proc. IEEE Mid-West Symp. on Circuits Syst., pp.80-83, Seattle, August 2010.

- D. DiClemente and F. Yuan, “A passive transformer voltage-controlled oscillator with active inductor frequency tuning for ultra wideband applications,” *Proc. 2nd Microsystems and Nanoelectronics Research Conf.*, pp.80-83, Ottawa, Oct. 2009.

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- D. DiClemente and F. Yuan, “Current-mode phase-locked loops,” *Presented at CMC Microsystems Annual Symp.* Ottawa, Oct. 2007.

- D. DiClements, F. Yuan, and A. Tang, “CMOS active transformer current-mode phase-locked loops,” *Proc. IEEE Mid-West Symp. Circuits and Systems*, pp.1528-1531, Montreal, Aug. 2007.

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Appendix B

Glossary

BER	Bit Error Rate
CCO	Current-Controlled Oscillator
CP	Charge Pump
DAC	Digital to Analog Convertor
DS-UWB	Direct Sequencing Ultra Wide-Band
FCC	Federal Communication Commission
GPS	Global Positioning System
HDTV	High Definition Television
ICI	Inter-Channel Interference
IF	Immediate Frequency
IFFT	Inverse Fast Fourier Transform
IP3	Third-order Intercept Point
ISM	Instrument, Scientific, and Medical
MB-OFDM	Multiple Band Orthogonal Frequency Division Multiplexing
PD	Phase Detector
PFD	Phase/Frequency Detector
PLL	Phase Locked Loop

QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
SSB	Single Side Band mixing
SNR	Signal to Noise Ratio
TFC	Time Frequency Code
TSPC	True Single Phase Clocked
WPAN	Wide Personal Area Network
VCO	Voltage-Controlled Oscillator

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