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10-bit double-segmented thermometer-coded current steering DAC

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10–BIT DOUBLE–SEGMENTED THERMOMETER–CODED CURRENT–STEERING DAC

by

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Abstract

10–BIT DOUBLE–SEGMENTED THERMOMETER–CODED CURRENT STEERING DAC

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Master of Applied Science
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This design describes a 10–Bit, 200–MHz Double–Segmented Thermometer–Coded Current–Steering digital to analog converter. A current–steering DAC is a power–efficient architecture, and also highly suitable for high–speed operation, but suffers from poor linearity characteristics. The problem can be prevented with a thermometer–coded technique. The DAC includes two–stage folded–cascode Op–Amp. The 10–bit DAC architecture consists of a 4 least significant bits entering to 4–bit thermometer–coded decoder and 6 most significant bits entering 6–bit thermometer–coded decoder, driving 960 equally weighted current sources. The double–segmented architecture allows the designed DAC to reduce not only the complexity of decoding logic, but also a number of current sources. The differential non–linearity (DNL) and integral non–linearity (INL) are 0.15 and 0.3 of least significant bits, respectively. Although designed to operate well about 1 GHz, Op–Amp limited the speed of the device to a 200–MHz clock rate. Low linearity errors (DNL and INL), 200–MHz conversion rate, low glitch energy, and 1.8V from a single voltage supply by using 0.18 μm CMOS technology makes this DAC suitable for graphic systems.

Acknowledgment

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Chapter 1

Introduction

Digital-to-Analog converters (DACs) are essential components of a large number of modern electronic systems. Linear digital-to-analog data converters are key building blocks in a wide range of applications. High-speed digital-to analog converters are used in many applications such as digital video, signal processing, test equipment and wireless communications. The key performance parameter of the DAC is emphasized by its applications. For instance, spectral purity is required in applications such as wireless transmitters and local oscillators. DC behavior, such as monotonicity and linearity, as well as dynamic behavior such as settling time and glitch energy, directly affect the distortion of the analog output.

For high-speed and high-resolution applications (>10 bits, > 50MHZ), the current source switching architecture is preferred since it can drive a resistive load directly without the need for a voltage buffers. Modern high-speed and high-resolution DAC's all use variations of this basic architecture. Current steering digital-to-analog converters are also very suited for circuit integration in standard digital CMOS processes.

Thermometer decoding has the well-known advantages of monotonicity and reduction of glitch energy[1]. But full thermometer decoded architectures are impractical to implement for high-resolution. A circuit implementation of a converter will suffer from a number of non-idealities, e.g., component matching, limited output impedance, noise, etc. This causes the output to become distorted and noise to be added to the signal. In the next chapter, we describe some typical performance measures for communications, such as signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), signal-to-noise-and-distortion ratio (SNDR), etc.

The behavior of errors due to circuit non-idealities, e.g., distortion and noise, can be of several different types. One can distinguish between static and dynamic properties of the errors. The

[1] It is explained in section 2.2.2.2.

static properties are signal-independent (memory-less) and the dynamic properties are signal-dependent. A typical static error is the deviation from the wanted straight-line input/output DC transfer characteristics, such as gain error, offset, differential (DNL) and integral nonlinearity (INL), etc. The dynamic errors mostly become more obvious and dominating as the signal and clock frequencies increase, whereas the static errors are dominating at lower frequencies. Dynamic performance is determined by signal-dependent errors such as slewing, clock feedthrough (CFT), glitches, settling errors, etc. In some sense, the static errors determine the best-case performance of the converter. The performance of the DAC can be determined using measures in both the time and frequency domain. Although static errors are signal-independent, they may give rise to (linear) distortion at frequencies that are multiples of the fundamental signal frequency. CFT in DACs generates frequency components at multiples of the Nyquist frequency (half the sample frequency) and glitches influence the higher frequency band.

The contributions of this thesis are:

- Development of the double-segmented technique with a unique combination of thermometer-coded decoder.
- Four and six bits thermometer-coded decoders.
- Implementing a very low resistor to reduce voltage fluctuation in output node.
- Fast two stage folded-cascade operational amplifier (Op-Amp).

The design of a CMOS DAC with an intrinsic accuracy of more than 10 bits is a difficult task mainly because for each extra bit of accuracy, the gate-area of the current-source transistors in the cell matrix must increase by a factor of 4 so that the transistor matching is within the desired accuracy [1], [2]. In addition, the area overhead due to the interconnect lines and the additional circuitry roughly doubles. Consequently, the cell matrix has dimensions of several hundred microns, and it becomes increasingly difficult to minimize the impact of systematic mismatch sources on the DAC accuracy due to process, temperature, and electric gradients.

1.1 Thesis Outlines:

This thesis is organized as follows. The Digital-to-Analog converter types and operation are described in chapter 2. In chapter 3 the proposed 10-bit DAC architecture is discussed. Each section of the proposed design including schematics and layout design is discussed in chapter 3. Chapter 4 reports the simulation results of the proposed design. The noise effect and different measurement results of errors are discussed as well. Chapter 5 elaborates the conclusion.

Chapter 2

Digital-To-Analog Converter Types and Operation

Throughout this chapter we present the basics of general digital-to-analog converters (DACs). Digital words[1] are input to a digital-to-analog converter (DAC) for conversion to a proportional analog signal level. The typical digital-to-analog voltage converter consists of four major elements: (1) the logic circuitry, (2) some type of resistor, capacitor or active element network depending on the applied theory, (3) switching network to drive either voltage or current to the proper input terminals of the network, (4) a reference voltage. Next, we mention the different types of digital-to-analog converters without describing their operation's details.

2.1 Scaled Converter

1) Resistor Scaled DAC

Discrete resistors are used to implement reference scales in D-to-A converters [3].

2) Unit-element Scaled

This model of scaled converter uses a large number of identical unit-capacitors or transistors instead of resistors [3].

In our proposed design we use transistor scaling D-to-A converter. Each current source inside the arrays of unit-current sources is a common emitter or a common source transistor controlled by the same base-to-emitter or gate-to-source voltage. The collector or drain currents are combined to implement the analog output. Both binary and thermometer coded converters are implemented this way. The outputs are added to track the magnitude of the input word. Larger input implies more transistors in parallel. This is what makes thermometer-coded converters monotonic and achieves good DNL performances regardless of the resolution.

[1] Digital inputs entering to DAC.

The need to access every unit-transistor requires row and column decoders. The logic gate is required in every cell to acknowledge the signals delivered by the decoders.

The following section introduces a number of performance measures that are commonly used to represent the DAC's performance characteristics. We, then, briefly discuss a number of DAC architectures reported in the literatures.

2.2 DAC's Performance Characteristics

2.2.1 Static performance

Depending on application, different performance measures are used to characterize the quality and performance of a D/A converter [3]. In many telecommunication applications, multi-tone signaling is used and in those cases (or in general), static measures or even single-tone measurements will not give all the necessary information to fully characterize the DAC. In this section we outline some of the most common static performance measures, such as the monotonicity, gain and offset error, differential nonlinearity (DNL), and integral nonlinearity (INL). A common source of static errors is component mismatch in the implementation. The following errors are the main static errors appearing in DAC.

2.2.1.1 Differential Nonlinearity (DNL)

The step size in the non-ideal converter diverges from the ideal size Δ (quantization error) [3]. This error is called the differential nonlinearity (DNL) error. For a DAC the DNL can be defined as the difference between two adjacent analog outputs minus the ideal step size

$$DNL_k = \tilde{X}_{a,k+1} - \tilde{X}_{a,k} - \Delta, \tag{2-1}$$

where $X_{a,k}$ corresponds to the ideal analog value for digital code $X_{d,k}$ while $\tilde{X}_{a,k}$ corresponds to the actual value and Δ is the ideal step size equal to analog value of the LSB. The normalized DNL with respect to the step size to get the relative error, is described as

$$DNL_k = \frac{\tilde{X}_{a,k+1} - \tilde{X}_{a,k} - \Delta}{\Delta}. \tag{2-2}$$

These definitions are most practical for DAC since the analog values can be directly measured at the output. Fig. (2-1) illustrates DNL error in DAC.

2.2.1.2 Integral Nonlinearity (INL)

The total deviation of an analog value from the ideal value is called integral nonlinearity (INL) [3]. The normalized INL is expressed as

$$INL_k = \frac{\tilde{X}_{a,k} - X_{a,k}}{\Delta}. \tag{2-3}$$

The relation between DNL and INL can be demonstrated as

$$INL_k = \sum_{l=1}^{k} DNL_l \,. \tag{2-4}$$

The nonlinearities errors are usually measured using a low frequency input signal to exclude dynamic errors appearing at the high signal frequencies. Although INL and DNL are used to characterize the static nonlinearity, in some applications offsets and linear gain errors are accountable. INL error is illustrated in Fig. (2-1).

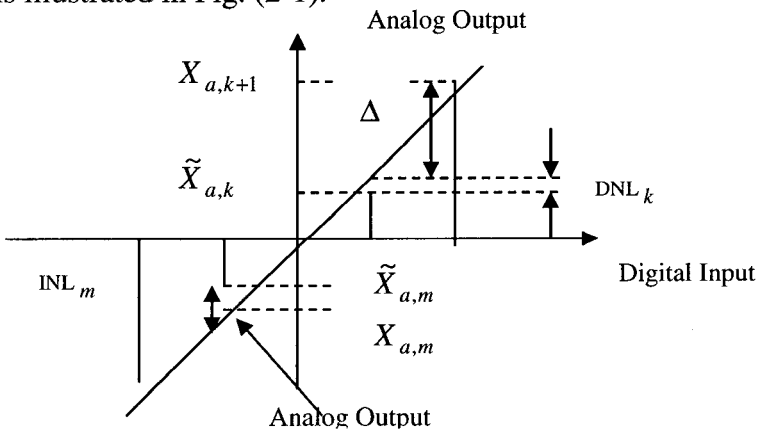


Figure 2-1: Non-linear transfer functions with INL and DNL errors

2.2.1.3 Offset Error

The offset, X_{offset}, is often calculated by minimizing the expression $\tilde{X}_{a,k} - X_{a,k} - X_{offset}$ for all k, with the least square method [3]. Minimization can be obtained by equaling the derivative to zero with respect to X_{offset}:

$$\frac{\partial}{\partial X_{offset}} \sum_{k=0}^{2^N-1} (\tilde{X}_{a,k} - X_{a,k} - X_{offset})^2 = 0.$$

This results in

$$X_{offset} = \frac{1}{2^N} \cdot \sum_{k=0}^{2^N-1} (\tilde{X}_{a,k} - X_{a,k}). \tag{2-5}$$

The above expression shows that the offset corresponds to the average of all the errors in the converter. To eliminate the offset from the INL calculations, the offset should be subtracted from all the analog values, $\tilde{X}_{a,k}$.

2.2.1.4 Gain Error

The gain error can be either linear or nonlinear as illustrated in Fig. 2-2.
As observed from Fig 2-2, the actual output has a linear gain error (a) and also non-linearity (b). The actual output with a linear gain and offset error can be expressed as

$$\tilde{X}_a = A \cdot X_a + X_{offset}, \tag{2-6}$$

where A is the gain error while the actual output for a non-linear gain can be written as

$$\tilde{X}_a = A_1 \cdot X_a + A_2 \cdot X_a^2 + A_3 \cdot X_a^3 + ... + X_{offset}. \tag{2-7}$$

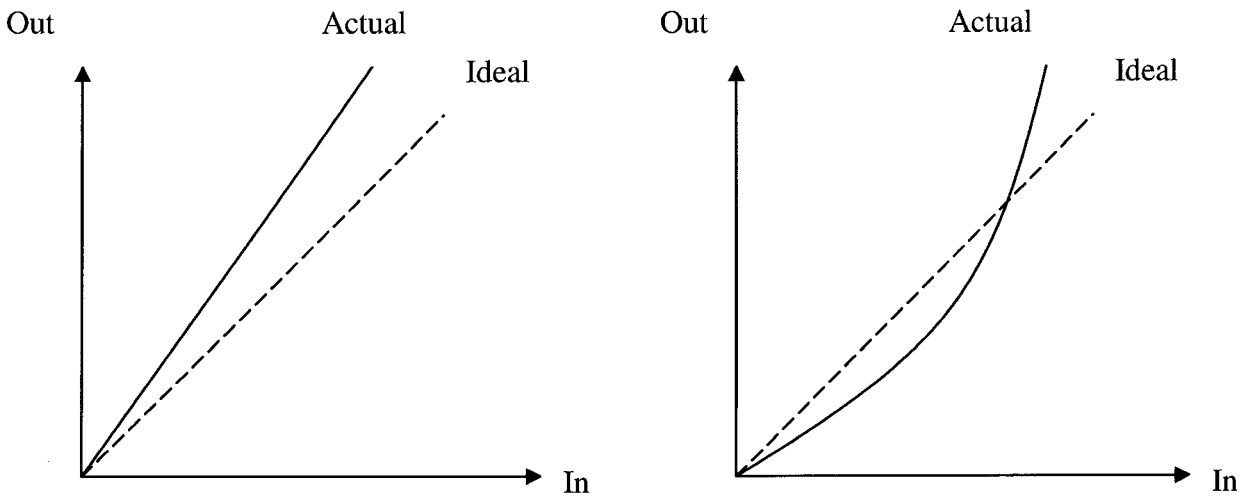


Figure 2-2: Characteristics of a) linear and b) non-linear gain error

2.2.1.5 Monotonicity

A converter is often described as monotonic converter if the amplitude level of the analog output increases when the input digital code is step up. An example of non-monotonic DAC is shown in Fig.2-3. Monotonicity is guaranteed if the deviation from the best-fit straight line is less than half an LSB as described in (2-8):

$$\left|INL_k\right| \le \frac{1}{2} LSB \text{ for all } k. \tag{2-8}$$

This implies that the DNL errors are less than one LSB:

$$\left|DNL_k\right| \le 1LSB \text{ for all } k.$$

There are some data converter architectures that are monotonic by design such as thermometer-coded DAC. In these converters, monotonicity can be earned without meeting the above conditions for INL and DNL [4].

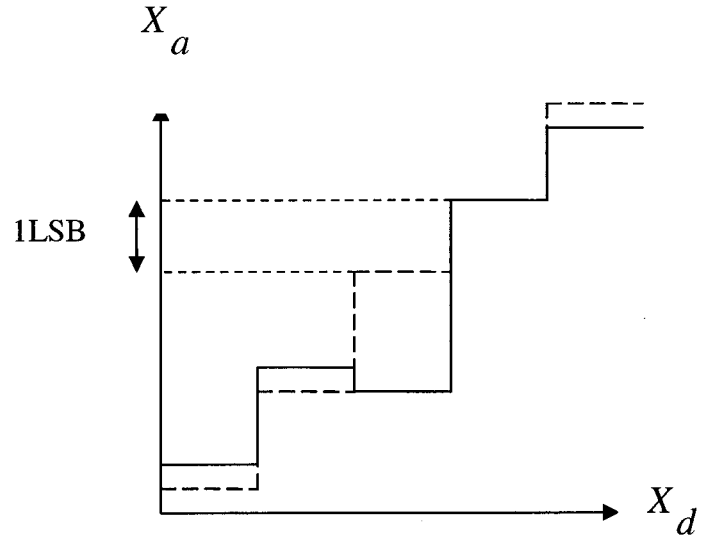


Figure2-3: A non-monotonic DAC

2.2.2 Dynamic performance

In addition to static errors, there are several other source of errors that appear when the input signal changes rapidly [3]. Dynamic nonlinearities increase in magnitude with increasing signal frequency since the output's value is changed more frequently and a larger part of the clock cycle is occupied by nonlinear switching transients. To find the true performance we must consider the entire shape of the analog output waveform. Typically, we have transients due to switching of analog elements. These transients are signal-dependent and hence of dynamic nature. Due to the finite update period, there will be settling errors which may be of both linear and nonlinear character. Other phenomena, such as glitches and clock feedthrough (CFT) also count as dynamic errors. The dynamic error sources will have a large impact on the DAC performance and it will become even more dominating for higher signal levels and higher signal and clock frequencies.

2.2.2.1 Settling Errors

When the input of the DAC is changed, the analog output should ideally change from the ideal start value, $X_{a,k}$, to the ideal final value, $X_{a,m}$, as shown in Fig 2-4. $\tilde{X}_{a,k}$ and $\tilde{X}_{a,m}$ are the actual initial and final value respectively. The time it takes for the output to settle within a certain accuracy of the final value is called settling time, T_s, and it determines the highest possible speed of the circuit. The slewing phases, linear and nonlinear, should be as small as possible to reduce distortion in the analog waveform.

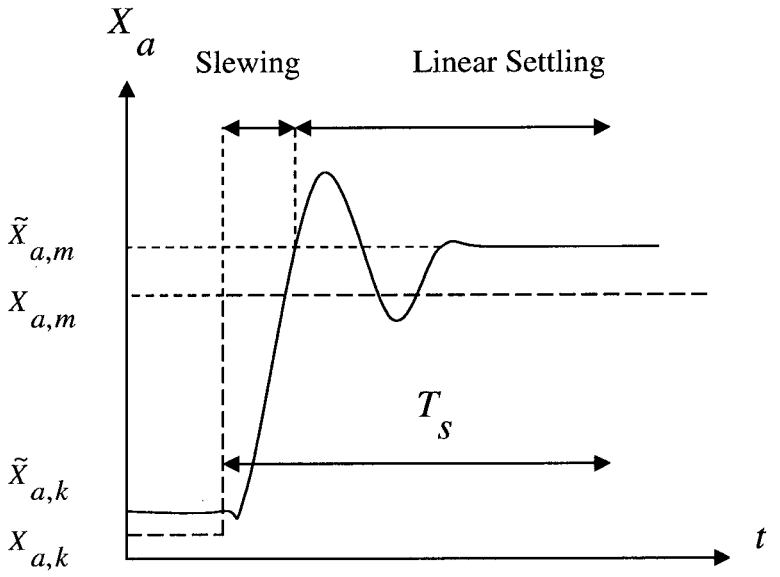


Figure 2-4: Actual output signal and ideal output signal (dashed) of a DAC

2.2.2.2 Glitches

Glitches are often occurred in the analog output between transitions of different digital input code caused by the unmatched switching time of different bits [3]. For example if the code transition is

0111...111 → 1000...000,

and the MSB switches faster than LSB, the code 11…111 may be present for a short time. This results in a large glitch at the output. The effect of glitch on the output signal is often determined by the energy of the glitch. If the glitch is modeled as a pulse, as shown in Fig. 2-5, with amplitude, X_g, and with time duration, T_g, the normalized average power, P_g, of the glitch over clock period $T_s = 1/f_s$ (the shortest possible code duration) is

$$P_g = X_g^2 \cdot \frac{T_g}{T_s}. \tag{2-9}$$

If the amplitude of MSB is considered as the maximum peak glitch

$$X_{g,\max} = 2^{N-1} \cdot \Delta, \tag{2-10}$$

then the maximum glitch power over one clock cycle is determined as

$$P_{g,\max} = 2^{2N-2} \cdot \Delta^2 \cdot \frac{T_g}{T_s}. \tag{2-11}$$

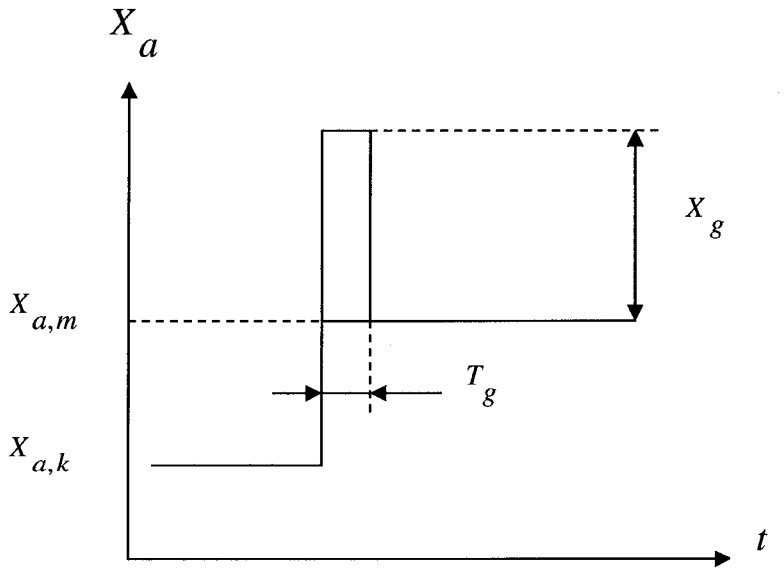


Figure 2-5: Glitch modeled as a pulse

2.2.2.3 Clock Feedthrough (CFT)

The clock affects the analog output signal due to capacitive coupling in switches [3]. The CFT error can be modeled in the similar way as glitches for current steering DACs. The CFT can be decreased by reducing the capacitive coupling and, therefore, the switching transistor sizes should be small to decrease the parasitic capacitance.

One conceptual solution to the dynamic linearity problem is to eliminate all of the DAC dynamic nonlinearities, which are associated with the switching behavior by placing a track/hold circuit at the DAC output [4]. The track/hold would hold the output constant while the DAC is still in the switching stage, and track when the current sources have settled to their DC value. In this way, only the static characteristics of the DAC appear at the output and the dynamic ones would be eased or completely eliminated. The drawback of this approach is that the track/hold circuits practically generate dynamic nonlinearities of its own, sometimes worse than those of the DAC alone. The other problem with using of the track/hold circuits is the significant reduction of speed due to the loading effect of the capacitors used to hold the DC value.

2.2.2.4 Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio of the power of the fundamental signal and the total noise power within a certain frequency band, excluding the harmonic components [3].

$$SNR = 10 \cdot \log_{10} \frac{P_s}{P_n}, \tag{2-12}$$

where is the signal power and is the noise power. The SNR is sometimes expressed in dBFS to relate the noise level to the full-scale input power.

2.2.2.5 Signal-to-Noise and Distortion Ratio (SNDR)

The signal-to-noise-and-distortion ratio (SNDR) is the ratio of the power of the fundamental signal and the total noise and distortion power within a certain frequency band [3].

$$SNDR = 10 \cdot \log_{10} \frac{P_s}{P_n + \sum_{k=2}^{\infty} P_k}. \tag{2-13}$$

The SNDR is sometimes expressed in dBFS.

2.3 DAC Architectures

In this section we introduce different techniques for converting a digitally coded signal into an analog signal representation. The approaches differ in speed, chip area, power efficiency, achievable accuracy, etc. However, the trade-off in converter design is normally between resolution and bandwidth.

2.3.1 Nyquist-Rate D/A converters

The Nyquist-rate converter is preferred for wide band applications where oversampling techniques are impossible due to the high clock frequency. In Nyquist-rate DAC the input signal bandwidth f_B is equal to the Nyquist frequency, $f_B \leq f_N = f_s/2$, where f_s is the update frequency of the DAC. The update frequency is defined as the entire possible frequency range for fully recoverable signals. To reduce attenuation of output signal due to sinc weighting, either anti-sinc filters or oversampling strategy is needed.

2.3.2 Nyquist-Rate DACs with oversampling

Almost all of the Nyquist-rate DACs are oversampled due to the difficulties in the realization of anti-sinc and low pass image rejection filters and the signal bandwidth, which is $f_B < f_N = f_s/2$ [3].

2.3.3 Binary weighted DAC

The binary weighted DAC utilizes binary weighted reference elements. The elements may be current sources, resisters or capacitors. The advantage is that the number of switches and digital encoding circuits are minimal compared with thermometer[1]. The drawback is that in the large number of bits, the large difference between the MSB and LSB weight causes mismatch errors in the converter. The output signal in this converter can be written as:

$$X(nT) = A_{offset} + A_0(b_0(nT) + 2b_1(nT) + \cdots + 2^{N-1}b_{N-1}(nT))^{2}, \quad (2\text{-}14)$$

[1] Thermometer code will be discussed in section 2.3.4.
[2] (nT) is the time point.

where A_0 is the reference, A_{offset} is the offset, $\{b_i(nT)\}_{i=0}^{N-1}$ are the input bits, and T is the update period of the DAC. Fig.2-6 shows the concept of the binary weighted DAC.

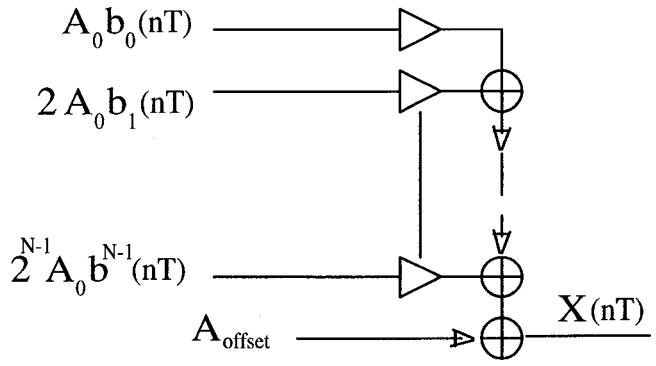


Figure 2-6: Binary weighted DAC with an offset level

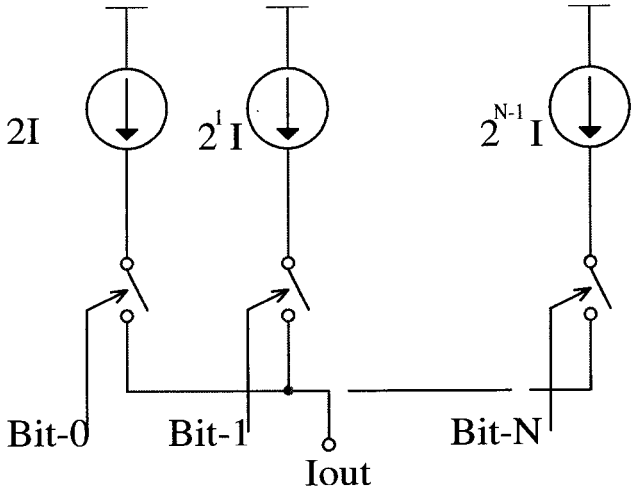
The three following DAC architectures, described below are subsets of binary weighted DAC architecture.

2.3.3.1 Current steering DAC

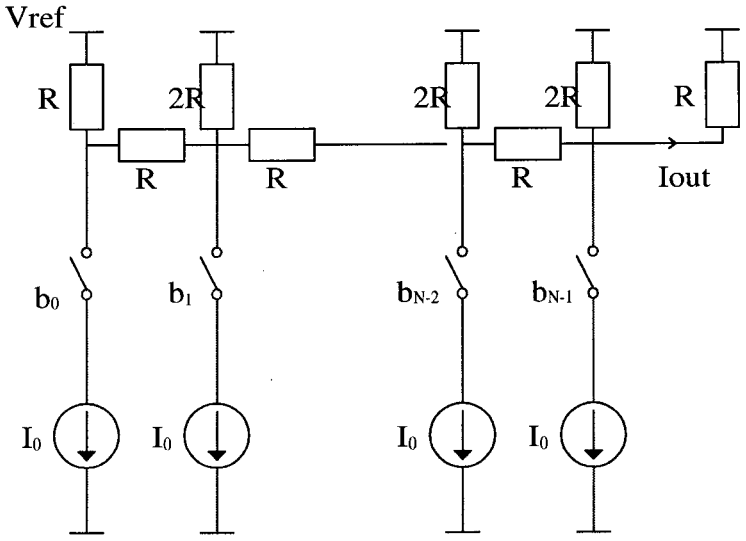
The switched-current or current steering DAC's are relatively easy to implement in a CMOS process. Fig.2-7 (a) shows the general architecture of binary current-steering DAC. The current switches are controlled by digital input bits. The use of unit element sources increases the matching of the sources. Small area chip and high speed are the advantages of the current-steering DAC. The major drawback is its sensitivity to device mismatch, glitch and large output impedance for higher number of bits.

2.3.3.2 R2R Ladder DAC

Construction of binary weighted resistor is easy but impractical for higher resolutions since resistors become very large in size. R2R ladder DAC overcomes this problem. An N-bit R2R ladder architecture is shown in Fig.2-7 (b). The resistive network divides the current from the individual current sources to the output and the output current is given by



(a)



(b)

Figure 2-7: a) SI DAC b) R2R DAC

$$I_{out}(k) = \frac{I_o}{2^N - 1} \cdot \sum_{l=0}^{N-1} b_l \cdot 2^l = \frac{I_o}{2^N - 1} \cdot k \,. \tag{2-15}$$

The matching is improved when component sizes to implement are in small range. Power inefficiency is the drawback of this architecture, however.

2.3.3.3 Charge Redistribution DAC

The charge redistribution DAC implements a switch capacitor (SC) circuit so that the conversion is performed by using the charge stored on a number of binary weighted capacitors. Fig.2-8 is an example of an N-bit SC converter. The phases $\phi 1, \phi 2$ are non-overlapping and the weighted capacitors are created using a number of unit capacitors. The most significant capacitor C_{N-1} is 2^{N-1} times larger than the least significant capacitor C_0.

2.3.4 Thermometer Coded DAC

This technique employs a number of equally weighted elements. The same number of switches controlled by the signal coming from the binary-to-thermometer decoder, derive either current or voltage of these element to output. The analog output at the time nT is given by:

$$X(nT) = A_{offset} + A_0 \sum_{i=1}^{M} C_i(nT), \tag{2-16}$$

where $C_i(nT) \in \{0,1\}, 1 \le i \le M$ are the thermometer-coded bits.

The matching requirement is much relaxed than that of binary weighted technique because of the large size of reference elements. Monotonicity, DNL and the INL are improved. Glitch problem is greatly reduced as only one element switches when the digital input increases by only one digit. Moreover, the glitch is strictly proportional to the signal step, so it will not cause any non-linearity in the DAC output signal.

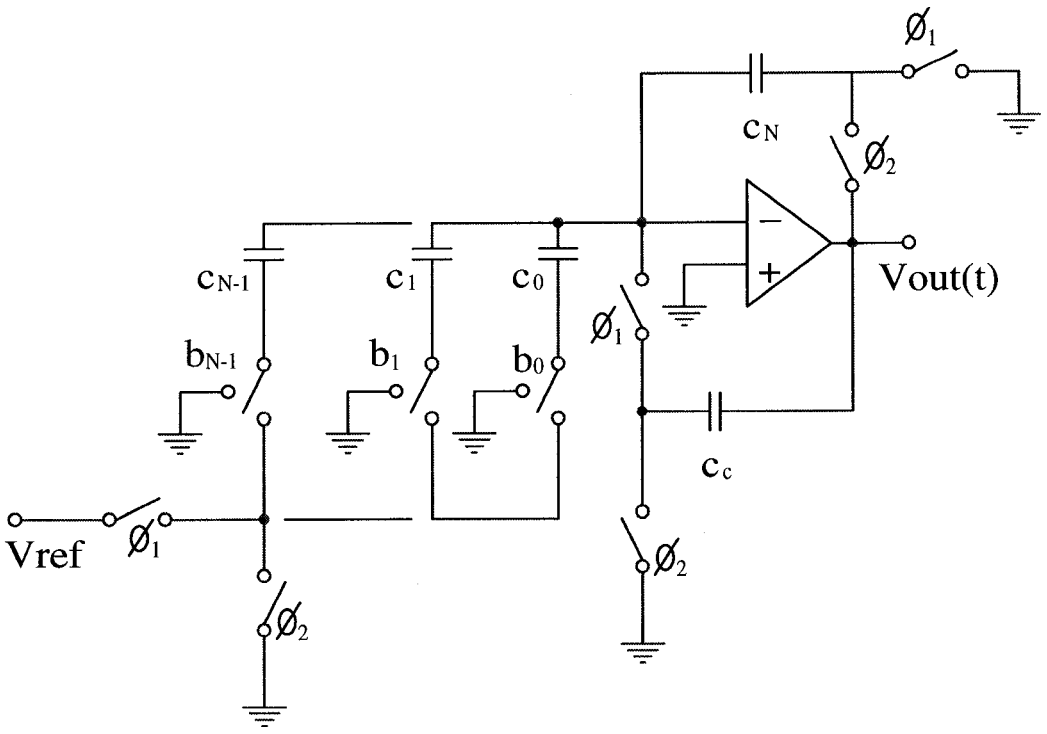


Figure 2-8: SC DAC

2.3.5 Encoded DAC

This architecture is very similar to the thermometer-code architecture. The difference is that linearly weighted references are used instead. "Walking-one[1]" code is used to switch the reference source elements and only allows one reference to be switched simultaneously.

2.3.6 Hybrid DAC

Combination of different types of DAC architectures allows us to add up the advantages together and retard the disadvantages in order to improve the performance. A number of sub-DAC usually with different architectures forms the complete DAC. Fig.2-9 shows the hybrid DAC where the different sub-DAC[2] can be of completely different type.

The total resolution is equal to the sum of converted bits in sub-DAC. Segmented DAC is a popular hybrid architecture and is included in thermometer and binary weighted architecture.

[1] Shown in Table 3-1 in Chapter 3.
[2] Each partition of segmented DAC.

2.3.7 Pipelined DAC

Pipelined DAC architecture implies low-speed, clocked circuits pipelined to boost the throughput of the whole system. The trade-off is consuming more power and implementing more hardware. This architecture can be achieved by breaking the loop in the previous architecture, into a pipeline as shown in Fig.2-10.

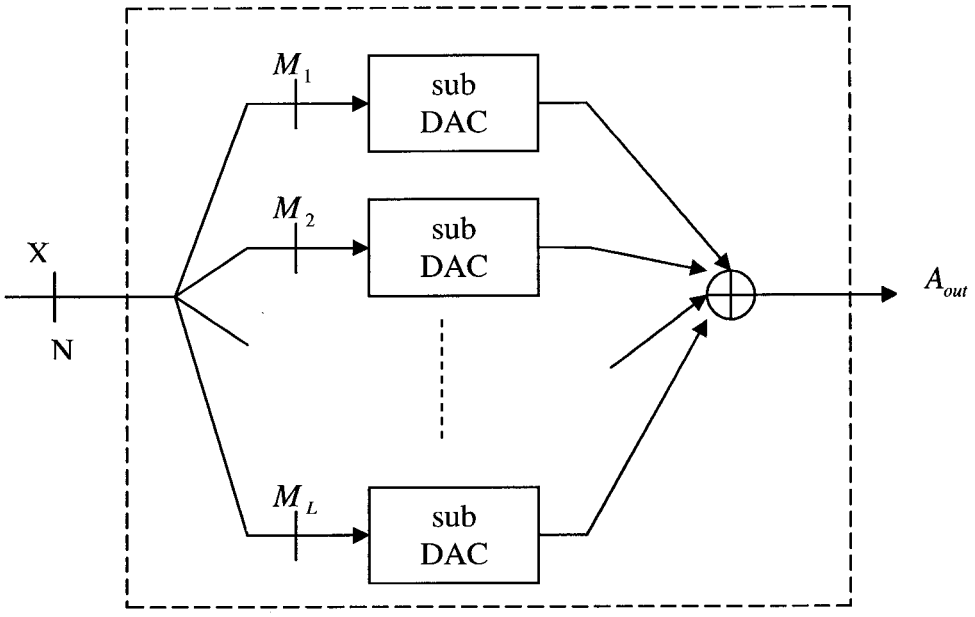


Figure 2-9: Hybrid DAC

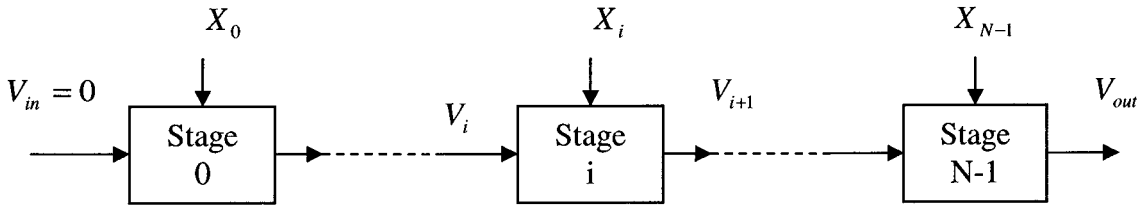


Figure 2-10: An N-stage pipelining DAC

Each stage in the pipeline uses an adder, a ½ amplifier and a switched current circuit.

2.3.8 Oversampling D/A converter (OSDAC)

In all OSDAC the input signal to the DAC is interpolated so that the maximum achievable resolution is given by the preceding digital circuits. The oversampling ratio (OSR) is the Nyquist frequency to the signal bandwidth ratio:

$$OSR = \frac{f_N}{f_B} = \frac{f_s}{2f_B}. \tag{2-17}$$

In order to reach a high-resolution we must choose a large OSR. For each doubling of the OSR, the effective number of bits is increased by half a bit. High-Pass (HP) filter is used to move the quantization noise power outside of the signal band. Low-Pass filter (LP) filter with cut-off frequency f_B, is used to attenuate this noise. The HP and LP together would accomplish the noise shaping of oversampling converter. Fig.2-11 illustrates the block diagram of OSDAC.

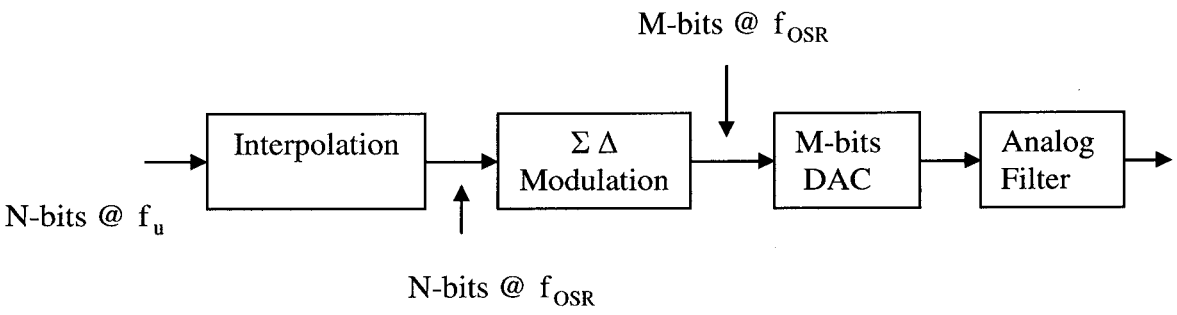


Figure 2-11: General OSDAC structure

The interpolator increases the update frequency of the input signal to $f_{OSR} = OSR \cdot f_U$. The modulator truncates the N-bits input signal into an M-bits signal. The M-bit DAC converts M-bits digital to analog output, which becomes *sinc* weighted [3] in the frequency domain due to the inherent S/H.

There are other architectures as Pipeline, Nyquist Rate, and Algorithmic DAC, which are not suitable for high-speed DAC.

2.4 Additional Improvement Techniques

Above sections described some of the very suitable architectures for high-speed and high-resolution DAC. However, to improve performance, some extra techniques are needed or must be added to previous architectures. Calibration, trimming of internal reference values, randomization, etc are some of the suggested techniques introduced in literatures [5], [6].

In the Table 2-1, we show a list of the DACs used in the latest literatures with a brief description of the DAC architecture and it can be used as a quick reference guide for proper choice of converter architecture depending on the specific application. In the literature current-steering converters are found as suitable candidates for high-speed and high-resolution applications.

No	Ref	Implementation	Res. [bits]	Supply [V]	Process	Fsignal [MHz]	Fsample [MS/s]	SFDR [dBc]
1	[7]	Double-segmented Plus R-2R	14	—	—	—	1000	—
2	[8]	binary weighted current steering	14	1.8	0.18 μm	—	100	84
3	[9]	Double segmented current steering	12	3.3	0.5 μm	—	300	—
4	[10]	Segmented current steering	10	3.3	—	—	500	55
5	[3]	Over sampling and interpolation	8	3.3	0.35 μm	3.79	100	54
6	[11]	Binary current steering	10	2.7	0.35 μm	—	800	60
7	[12]	Curve interpolation	10	5	0.8 μm	—	500	—
8	[13]	Sigma-delta Oversampling	24	5	0.5 μm	—	0.194	—
9	[14]	Q^2 Random Walk	14	2.7	0.5 μm	—	150	84

Table 2-1: DAC's Comparison in the latest literatures

Chapter 3

The Proposed 10-bit DAC Design

To achieve a good DNL specification and glitch energy, the number of bits implemented in the binary weighted part of the DAC has to be small. For every extra bit implemented in the unity decoded part, however, the number of control lines needed to select the current sources doubles, and the decoding logic complexity increases significantly. A direct consequence is often a reduction in the maximum operating speed. Another important fact is that the area used by the decoding and interconnections inside the matrix increases, and consequently the process and systematic errors become more difficult to compensate. The key point to preserve a very high update rate is to keep an intrinsically simple and compact decoding logic. The best alternative consists of implementing a fast row-column decoding scheme without any binary-weighted segment. Furthermore, the number of decoded bits with this scheme should be kept low, otherwise pipeline stages might be required.

It is well known that segmenting current sources in a DAC design provides better linearity for given element mismatches than other DAC design techniques approach [15]. It is also well known that segmenting an entire 10-bit DAC would consume a large amount of area [15]. This DAC utilizes the performance advantages of double-segmentation in order to optimize the area consumption and decoder complexity. It is very difficult to use a full thermometer code representation for all bits in high-resolution converters, since the number of switches and the complexity of the interconnection wires, etc., grows exponentionally with increasing number of bits. The DAC can be laid out more regularly and it becomes simpler to distribute the sources to minimize the influence of the graded matching errors. We can also use the same size on the switches for the thermometer-coded bits, which further improves matching. A fully thermometer-coded DAC guarantees montonicity and minimal glitches. However, for high resolution this is not feasible and there is a trade-off between the number of bits to segment and the impact on layout complexity, glitches, mononicity, etc.

3.1 Design Overview

The DAC circuit diagram is shown in Fig.3-1. Input digital bits (B0-B9) are decoded by row thermometer-coded decoder and column thermometer-coded decoders. A thermometer code differs from a binary code because it has 2^{N-1} digital inputs to represent 2^N different digital value. The thermometer-based converter has advantages over binary counterpart, such as low differential non-linearity (DNL), guaranteed-monotonic and reduced glitch noise. If D1 to D10 are used to control current sources, then moving from one code to the next, one additional current is turned on, which increases the total output current, hence guaranteeing monotonicity. The DAC has a $6+4$ segmented architecture: first, the six most significant bits (MSB's) are linearly decoded after the four least significant bits (LSB's) are linearly decoded. The decoded data (R_j, R_{j+1}, C_i) pass through matrix switching decoders and generates SEL and –SEL. The generated SEL and –SEL signals are applied to a latch and then latch output signals SET and –SET are inputted to switched current source which produces two currents, Io and $\overline{Io}$. The resulting output current, I_{out}, and output voltage, V_{out}, are obtained from (3-1) and (3-2) respectively.

$$I_{out} = I_{LSB}[(2^6 - 1)(2^4 - 1) + (2^4 - 1)], \tag{3-1}$$

where I_{LSB} is an LSB current, $(2^6 - 1)$ and $(2^4 - 1)$ are 6-bit and 4-bit thermometer digital outputs respectively.

$$V_{out} = A_V (I_{OUT} * R_{LOAD}), \tag{3-2}$$

where R_{LOAD} and A_V are a load resistor and Op-amp voltage gain respectively.

The total of 960 current sources are combined to form a 15×64 matrix structure. There are three fundamental building blocks required by the DAC: 1) the decoding logic; 2) the latches; and 3) the current source and switching elements. The final stage to provide DAC output voltage is a current-to-voltage converter using two-stage differential folded-cascade op-amp.

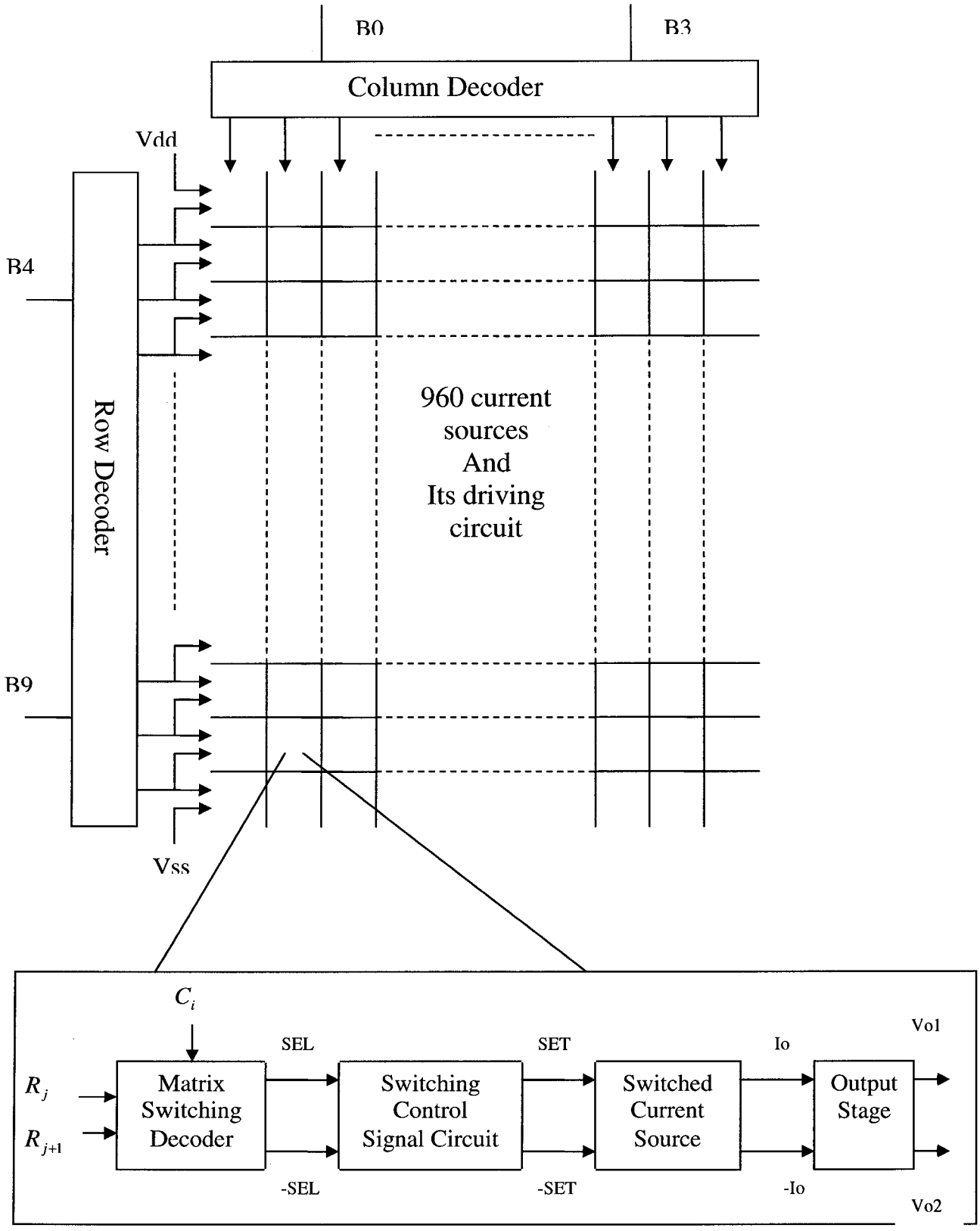


Figure 3-1: Proposed DAC circuit diagram

3.2 Double-Segmented DAC Architecture Overview

It has been very popular to partition the DAC into a segmented sub-DAC. A segmented architecture is traditionally chosen for current-steering DAC topologies because of the better differential non-linearity (DNL) specifications. This segmentation can be implemented into a segmented coarse sub-DAC and a binary-weighted fine sub-DAC whose output currents are simply added. The level of segmentation used in the current-steering D/A converter is an important decision in the realization of this technique. To achieve a good DNL specification and glitch energy, the binary-weighted implementation is entirely eliminated.

For every extra bit implemented in the unity decoded part, however, the number of control lines needed to select the current sources doubles, and the decoding logic complexity increases significantly. A direct consequence is often a reduction in the maximum operating speed. Equally important is the fact that the area used by the decoding and interconnections inside the matrix increases, and consequently the process and electric systematic errors become more difficult to compensate. Good trade offs between these specs have been obtained for 8-bit and 10-bit DAC's [16], [17]. Another advantage of using segmentation is to reduce the effects of too large currents through the current switches, which imply difficulties with matching and resistance ratios. The MSBs are encoded from a binary representation into a thermometer code. By segmenting implementation the DAC can be laid out more regularly and it becomes simpler to distribute the sources to minimize the influence of the graded matching errors. We can also use the same size switches for the thermometer-coded bits, which further improves matching. Another major advantage is that with this approach matching enhancement techniques, such as dynamic randomization, current source calibration, averaging, etc., become much simpler. It was found out in the previous works that up to five or six segmented bits gives a large improvement in performance. Higher degree of segmentation needs more digital circuits and, hence, higher complexity, power consumption and induced noise, and the gain is not as significant.

In order to obtain 10-bit resolution in this thesis, a double-segmented architecture including two sub-DAC with the same architecture has been used. For a resolution of $m = k_1 + k_2$, the k_1 most significant bits and k_2 least significant bits are converted to a thermometer code, which are driving the associated segment arrays. Fig.3-2 shows a double-

segmented decoding architecture that will be used for 10 bit DAC implementation, where $k_1 = 6$ and $k_2 = 4$. The double-segmented architecture decoding technique increases the resolution without requiring large decoder size.

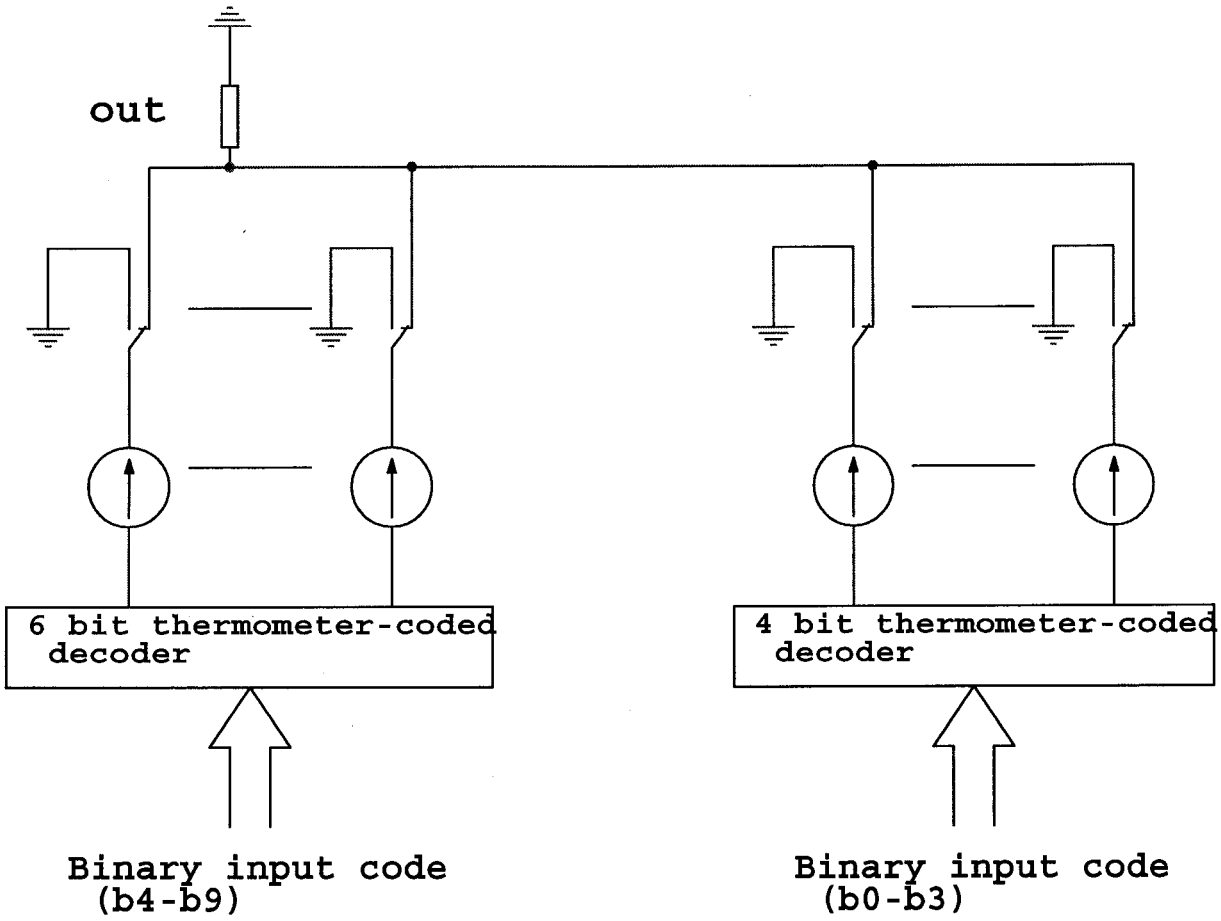


Figure 3-2 A double-segmented decoding 10-bit DAC architecture

3.3 Thermometer Coded Decoder

The thermometer code is used in high-speed converter. With this coding the number of ones in the code determines the corresponding analog value in DAC's output. This is illustrated in Table 3-1 showing the thermometer codes for N=7 and the corresponding index K. Four and six bit thermometer decoders are implemented as row and column decoder respectively.

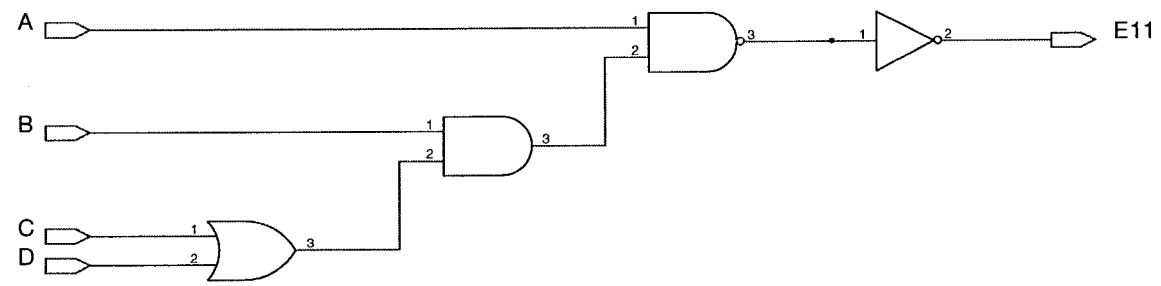
The double-segmented decoding technique increases the resolution without requiring large decoder size. For example, in this design, we need 2^4-1 and 2^6-1 decoder cells in implementing the decoder logic for 10 bit DAC. However, we need $2^{10}-1$ decoder cells when we implement the decoder logic of 10 bit DAC using a single-segmented decoder rather than a double-segmented decoder.

K	Binary Code	Thermometer Code	Walking-one Code
0	000	0000000	0000000
1	001	0000001	0000001
2	010	0000011	0000010
3	011	0000111	0000100
4	100	0001111	0001000
5	101	0011111	0010000
6	110	0111111	0100000
7	111	11111111	1000000

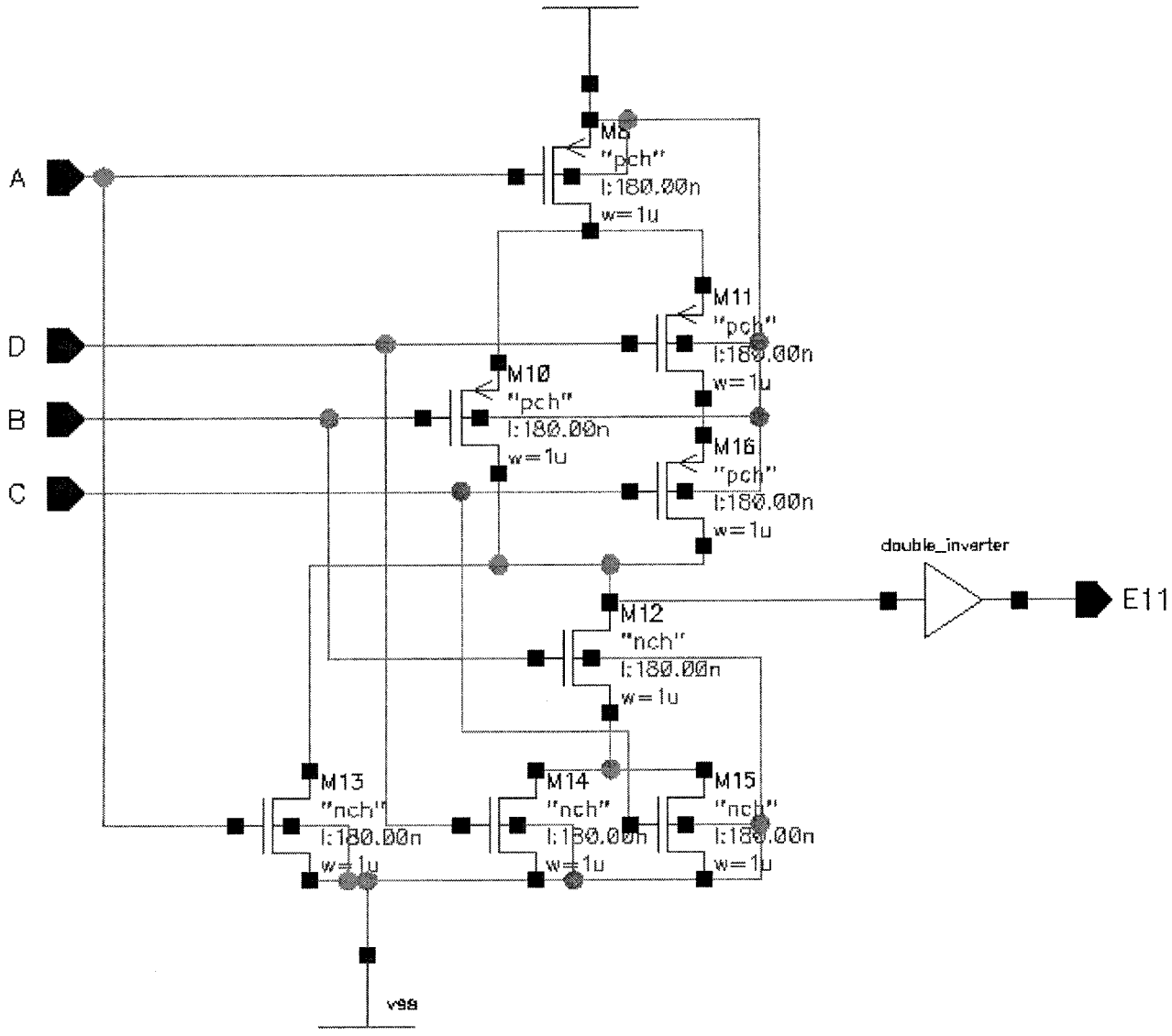
Table 3-1: Thermometer-code representation for 3 bit binary values

Fig. 3-3 (a) shows the thermometer-code decoder logic for $E11 = A \cdot B(C + D)$ in 4-bit thermometer-code decoder and Fig. 3-3 (b) shows the schematic for the same logic circuit. The complete thermometer-code decoder for 4-bit binary is demonstrated in Fig. 3-4.

Fig. 3-5 represents the layout design for the same logic cell (E11) from 4-bit thermometer. The floor plan has been designed to occupy the least space in chip area.



(a)



(b)

Figure 3-3: The thermometer-code decoder for 4-bit binary (a) logic for E11 (b) schematic for E11

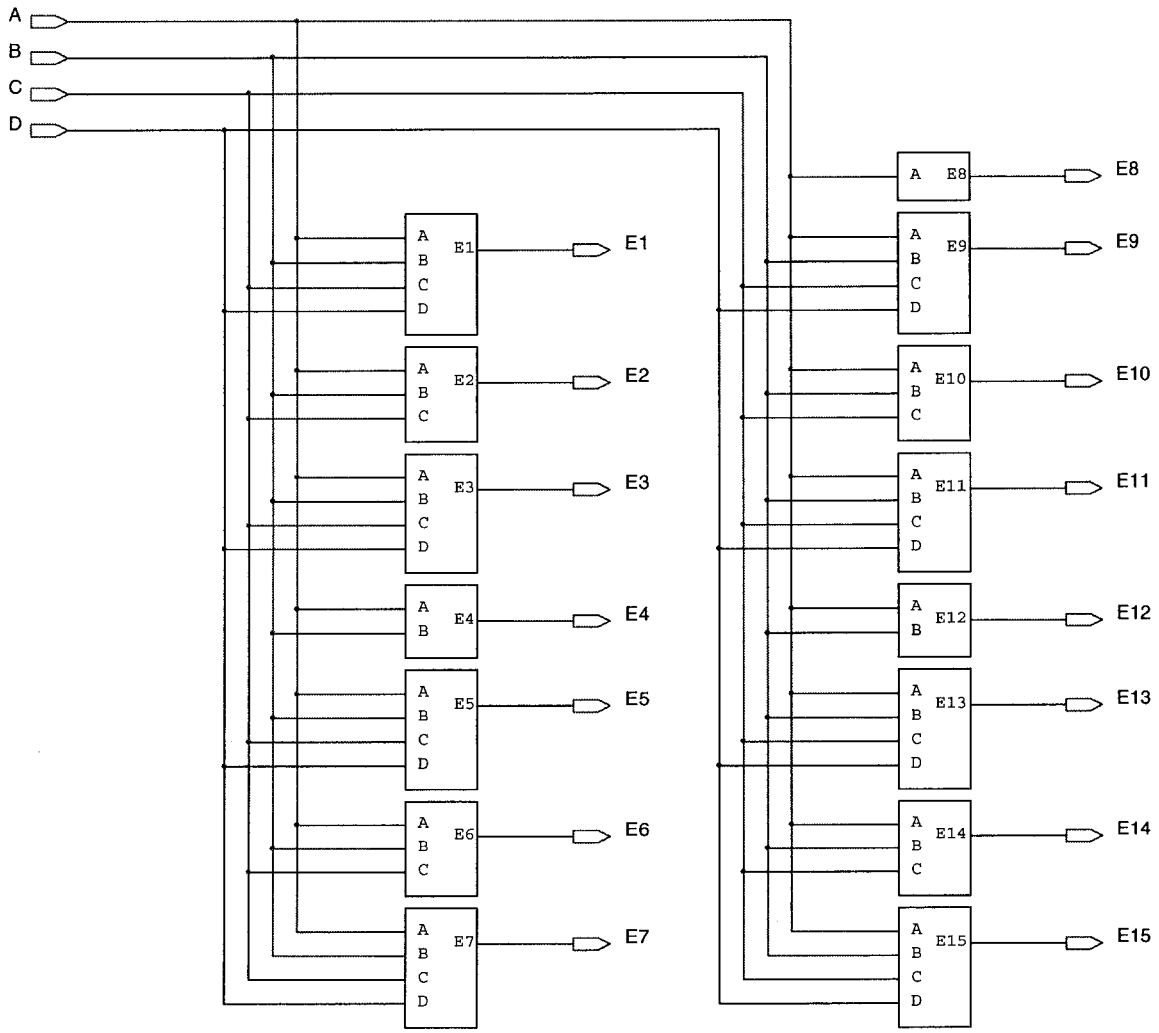


Figure 3-4: The block diagram of 4-bit thermometer-code decoder

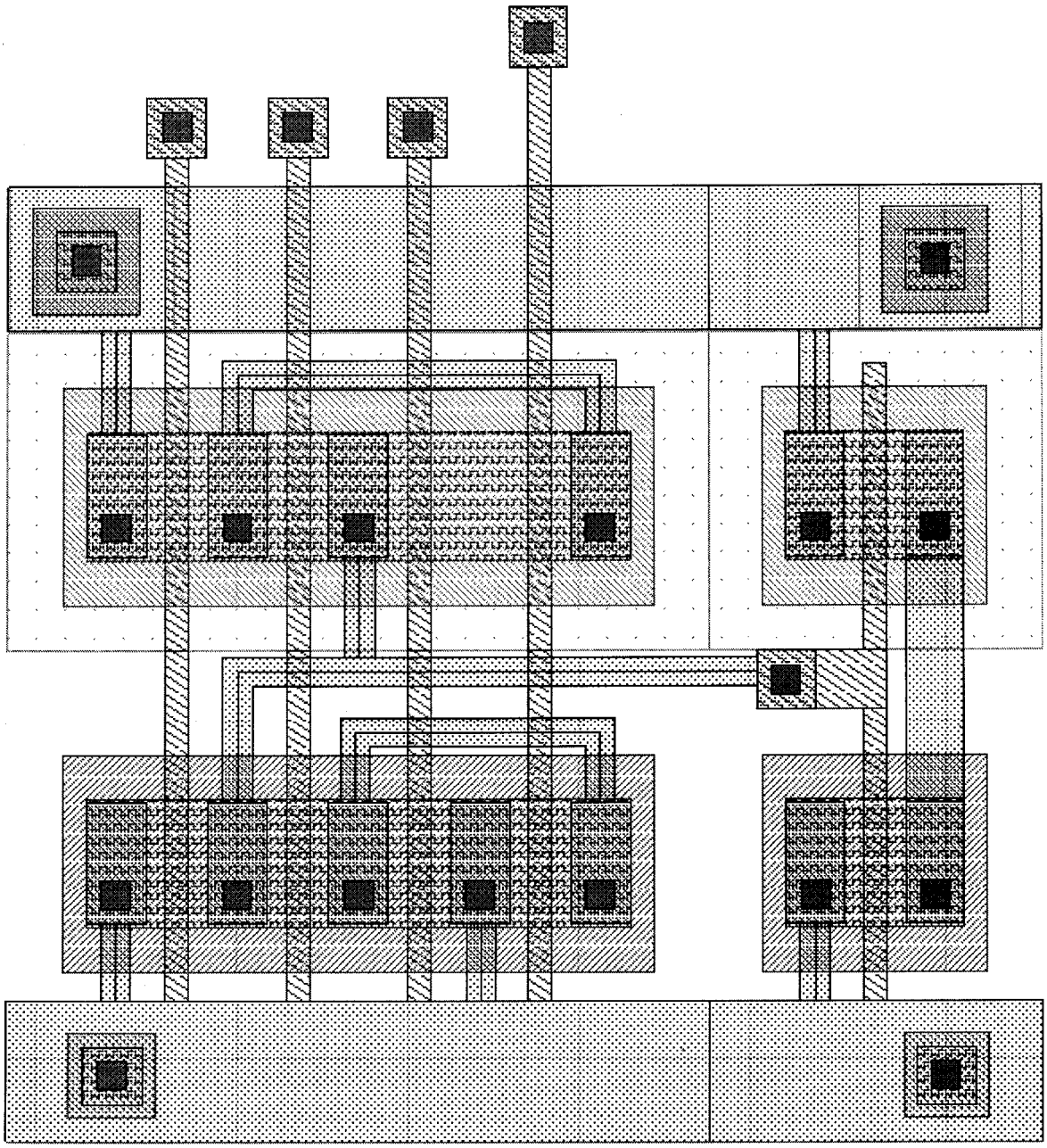


Figure 3-5: 4-bit thermometer Layout (E11)

Fig. 3-6 (a) shows the thermometer-code decoder logic for $E27 = A \cdot B(C + D)$ in 6-bit thermometer-code decoder and Fig. 3- 6 (b) shows the schematic for the same logic circuit.

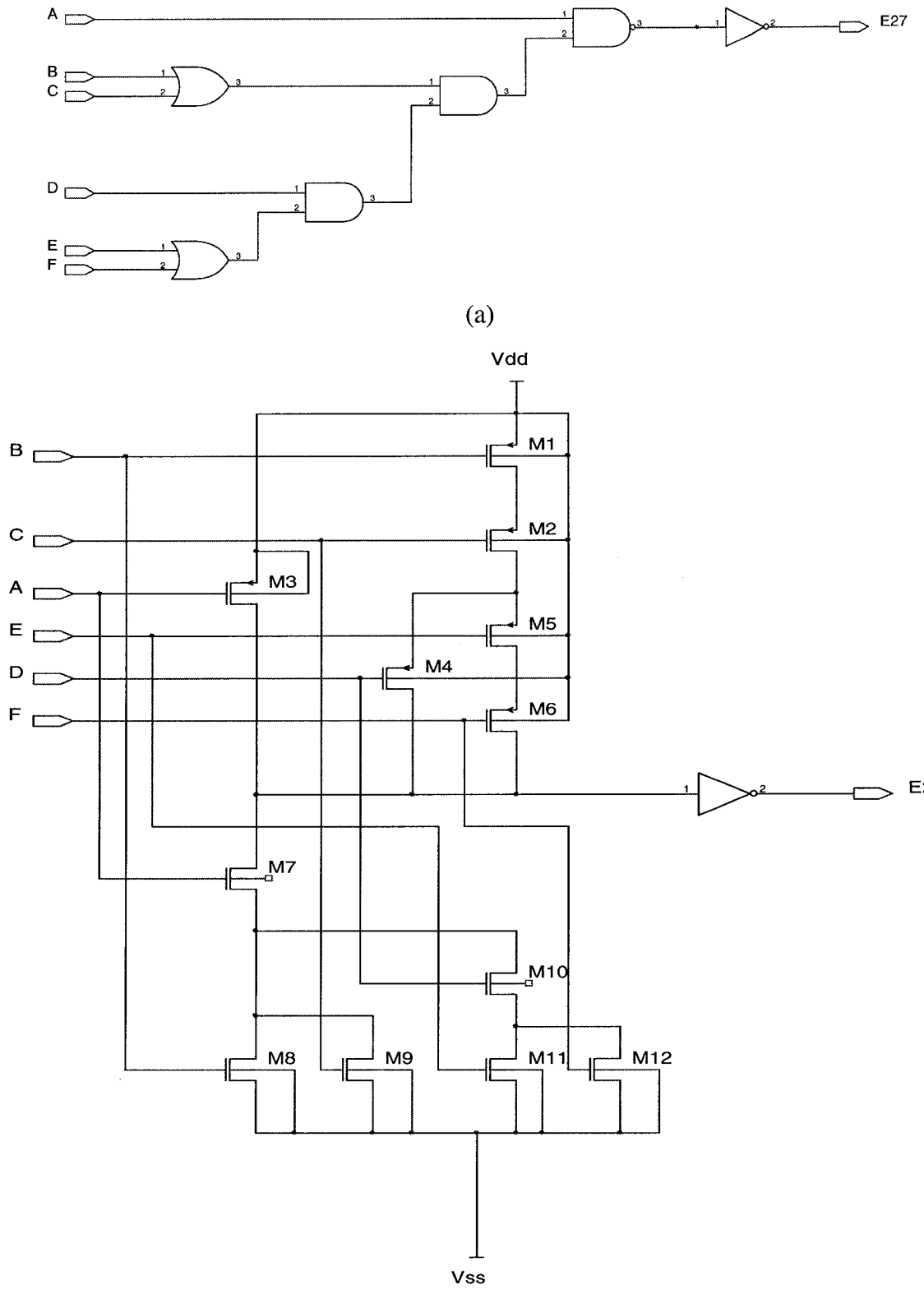


Figure 3-6: 6-bit thermometer-code decoder (a) logic for E27 (b) schematic for E27

The layout photo of E27 is shown in Fig. 3-7.

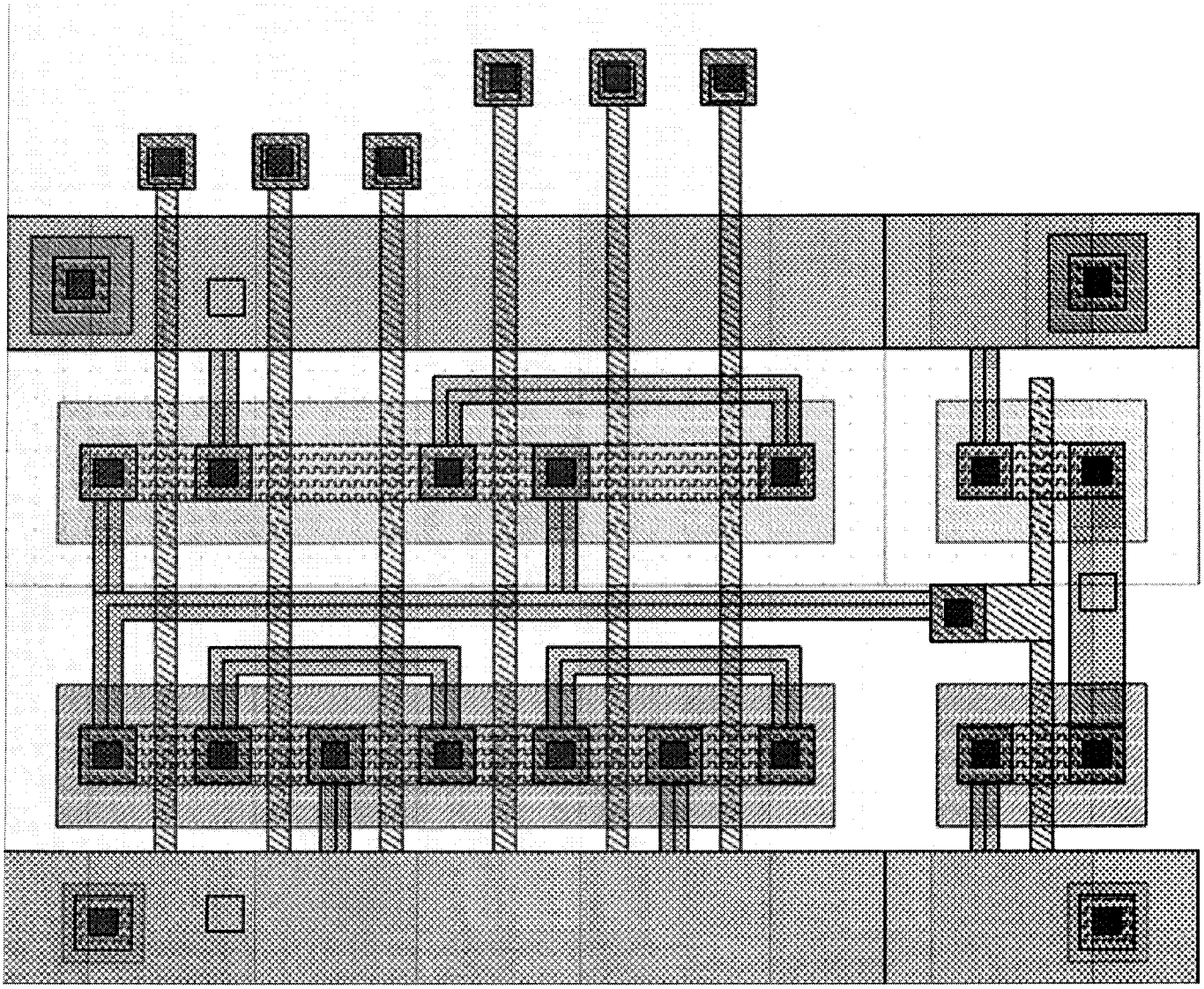


Figure 3-7: 6-bit thermometer Layout photo (E11)

3.4 Matrix Switching Decoder

The segmented DAC architecture is used in the proposed design to allow good matching strategies, reduced glitching, and easy calibration. The digital input bits are thermometer coded in two separated parts; hence two binary to thermometer decoder are required. These decoders convert the binary code into the bits of the thermometer code representation according to Table 3-1. On the other hand, there is a need for a logic design to combine two thermometer-coded decoder outputs in order to generate a single signal to turn on/off a current source. In our case, when the digital input code increases by one, a single cell inside current matrix is turned on consequently [18].

The output voltage, $V_{o,i,j}$ (=SEL) of the matrix switching decoder, as shown in Fig. 3-8, is represented as:

$$V_{o,i,j} = R_j (R_{j+1} + C_i). \tag{3-3}$$

The logic state of $V_{o,i,j}$ depends on C_i only if R_j is high and R_{j+1} is low. In order to synchronize the rising time and falling time in the decoder, the following two conditions should be met.

The first condition is satisfied when the gate capacitance on each input node, R_j, R_{j+1}, C_i become identical as:

$$C_{OX}(W_1 L_1 + W_4 L_4) = C_{OX}(W_2 L_2 + W_5 L_5) = C_{OX}(W_3 L_3 + W_6 L_6), \tag{3-4}$$

where C_{OX}, W_i and L_i are gate oxide capacitor, the channel width and length of the MOSFET M_i respectively.

The second condition is that, the rising time, T_r should be equal to the left hand falling time, T_{f1}. This condition can be expressed as:

$$A_p \frac{C_L}{K_p(\frac{1}{\frac{1}{(\frac{W}{L})_1 + (\frac{W}{L})_2}})} = A_n \frac{C_L}{K_n(\frac{W}{L})_5}, \tag{3-5}$$

where C_L is the load capacitance, A_p and A_n are process dependant parameter of PMOS and NMOS transistors, K_p and K_n are transconductance parameters of PMOS and NMOS transistors, respectively and can be determined as:

$$K_p = \mu_p C_{OX} \ , \ K_n = \mu_n C_{OX} \, , \tag{3-6}$$

where μ_p and μ_n are mobility of electrons in PMOS and NMOS, respectively.

The falling time, T_{f1} should be equal to the right hand falling time, T_{f2}. It can be written as:

$$A_n \frac{C_L}{K_n(\frac{W}{L})_5} = A_n \frac{C_L}{K_n(\frac{1}{\frac{1}{(\frac{W}{L})_6 + (\frac{W}{L})_4}})}. \tag{3-7}$$

The device aspect ration of all transistors in matrix switching decoder can be determined by (3-4), (3-5), and (3-7) with an assumption that:

$$(\frac{W}{L})_1 = (\frac{W}{L})_3 = (\frac{W}{L})_3 \text{ and } (\frac{W}{L})_5 = (\frac{W}{L})_6 . \tag{3-8}$$

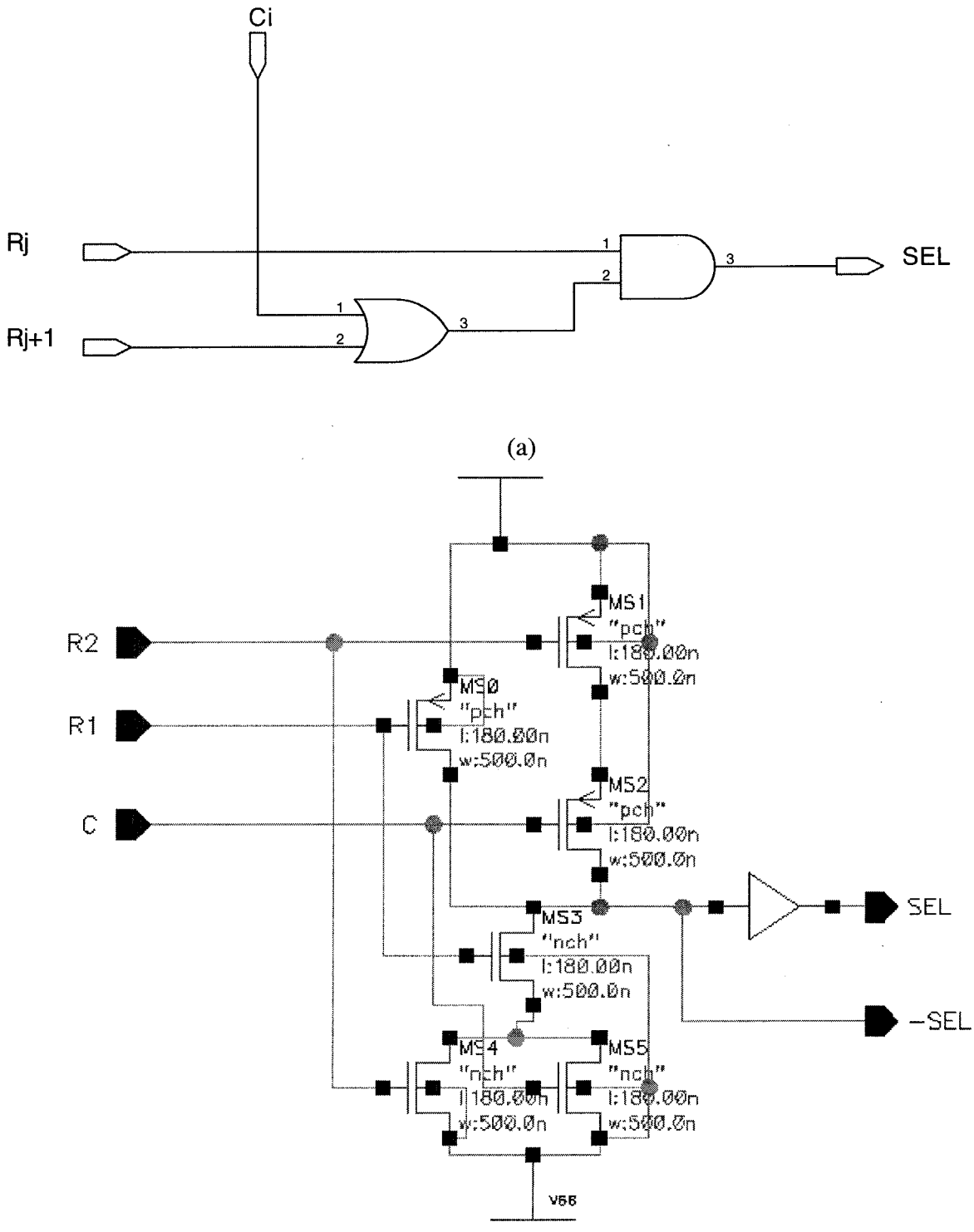


Figure 3-8: a) The logic gates and b) The schematic diagram of matrix switching decoder

The layout photo of matrix switching decoder appears in Fig. 3-9

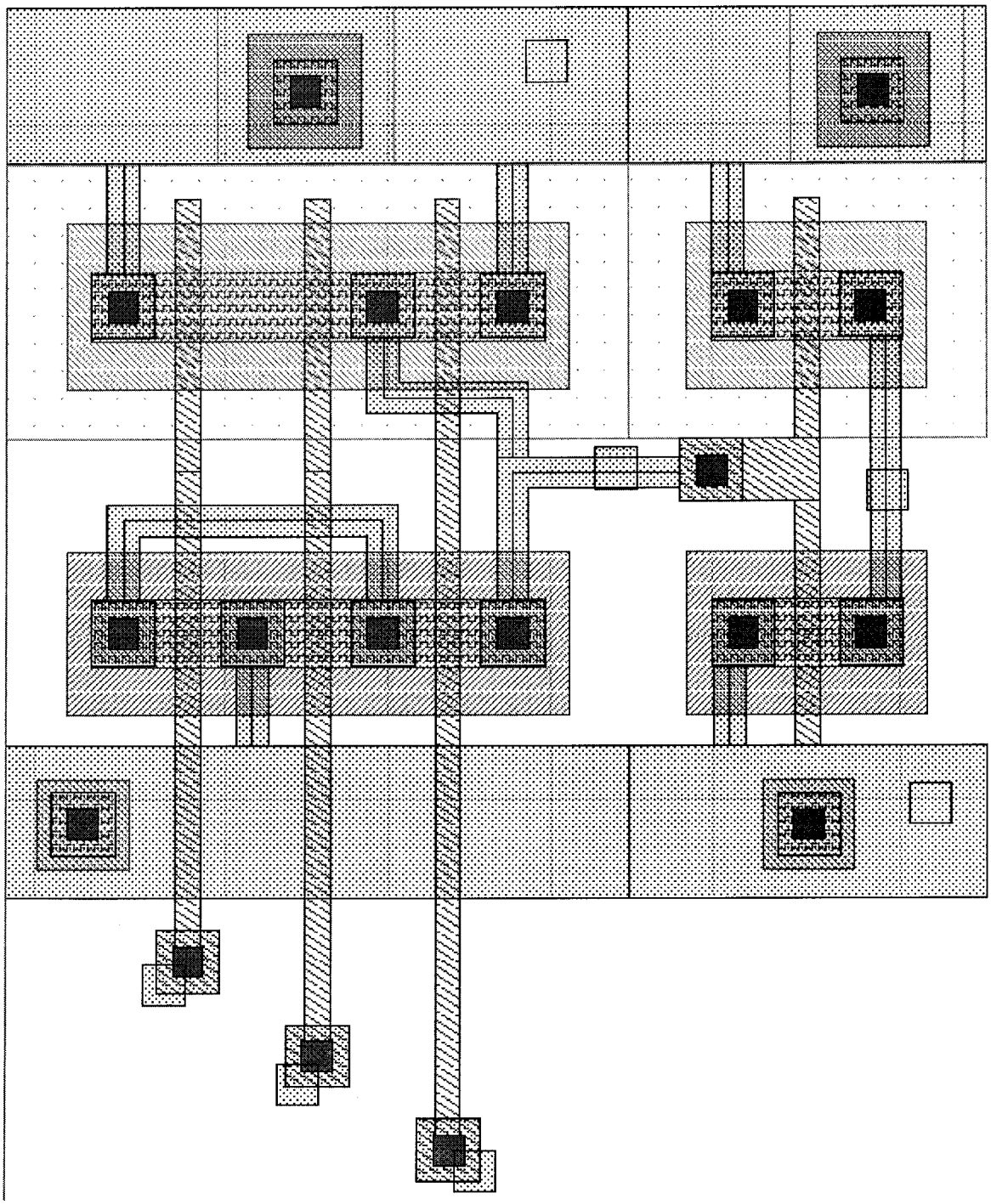


Figure 3-9: Layout photo of matrix switching decoder

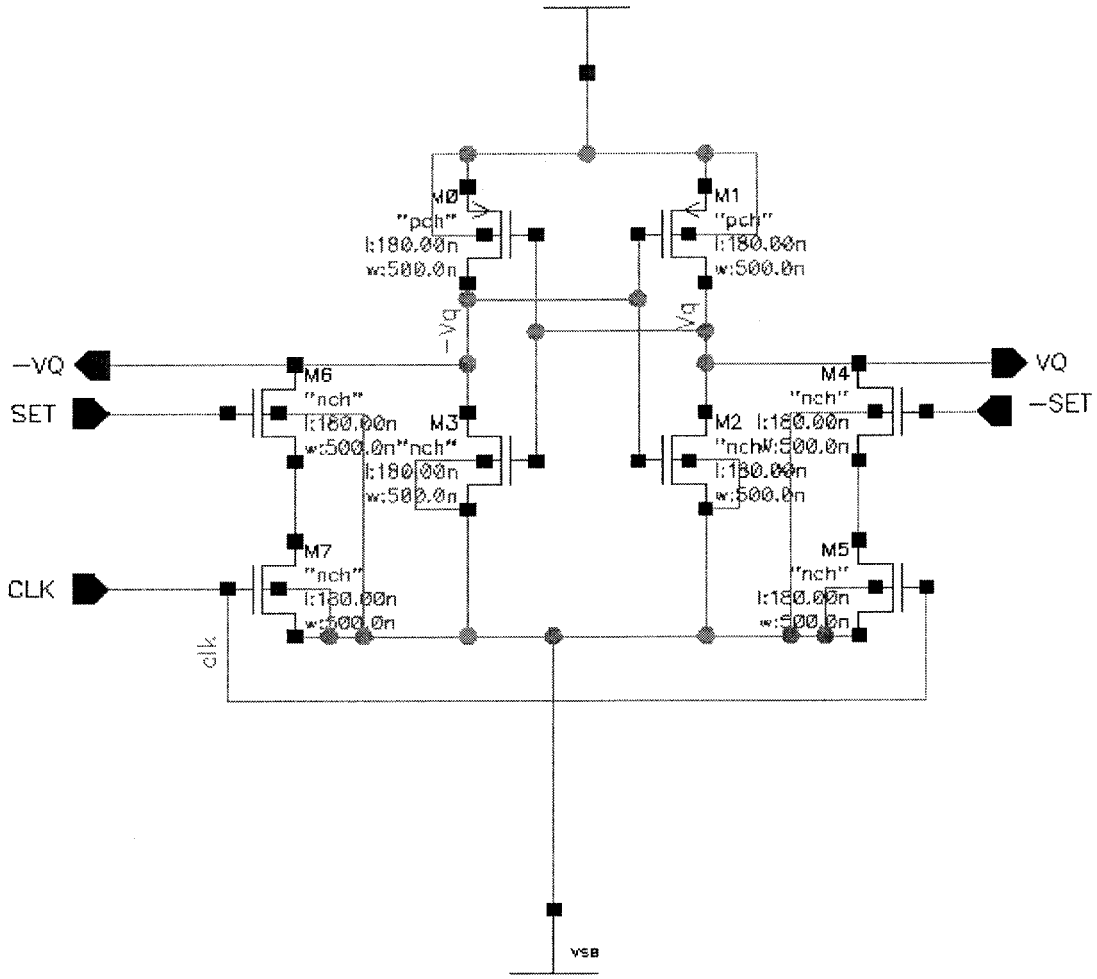
3.5 Switching Control Signal Circuit

Since we are switching a current source, we must ensure that the current switch does not switch the current source completely off. Otherwise, this would force the output voltage of the current source to drift towards the power supply voltage as it is switched off. When it switches on again, the voltage drop between the current source output and the DAC output is large and a glitch is induced. In extreme cases, the current source transistor may also get into the linear operation region and will then have much worse output impedance. To avoid this, we use differential switches, so that the current source always delivers current. The switching signals also have to be properly matched to reduce the glitches. The switching signals can be generated by using a set-reset latch (SR).

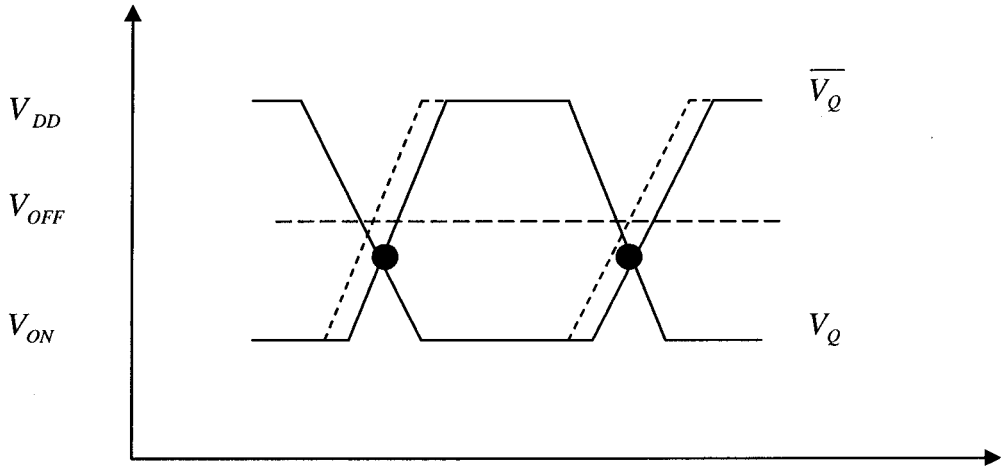
A compact ratioed logic latch [19] using only eight transistors is implemented in this design to generate the switching control signals. The delay between the two complementary outputs in this latch is used to decrease the crossing point voltage of the switching control signals, improving the timing of the signals. By changing the supply voltage of latches, V_{BB}, that is kept independent from the main power supply voltage, we can adjust the crossing switching control signals.

Fig. 3-10 (a) represents the schematic of the latch and Fig. 3-10 (b) presents the control signal waveform. The optimum cross-point voltage is $\Delta V/2$ where ΔV represents the minimum voltage necessary to completely steer the current from one output to the complementary output.

To overcome skew between row and column select signals, one latch is used per current cell immediately before the switching transistors, ensuring synchronization of the signals for all input codes. The intrinsic delay between the complementary latch outputs reduces the crossing-point voltage of the switching control signals, putting one switching transistor at the edge of turning on when the other is at the edge of turning off, reducing significantly glitches generated during code transitions. Moreover, the voltage swing at the drain node of the current source transistors is also reduced, and therefore, the fluctuation in the nominal value of the current source due to the transistors finite output impedance is decreased. The latch layout is shown in Fig. 3-11.



(a)



(b)

Figure 3-10: a) Latch schematic diagram b) Switching control signals

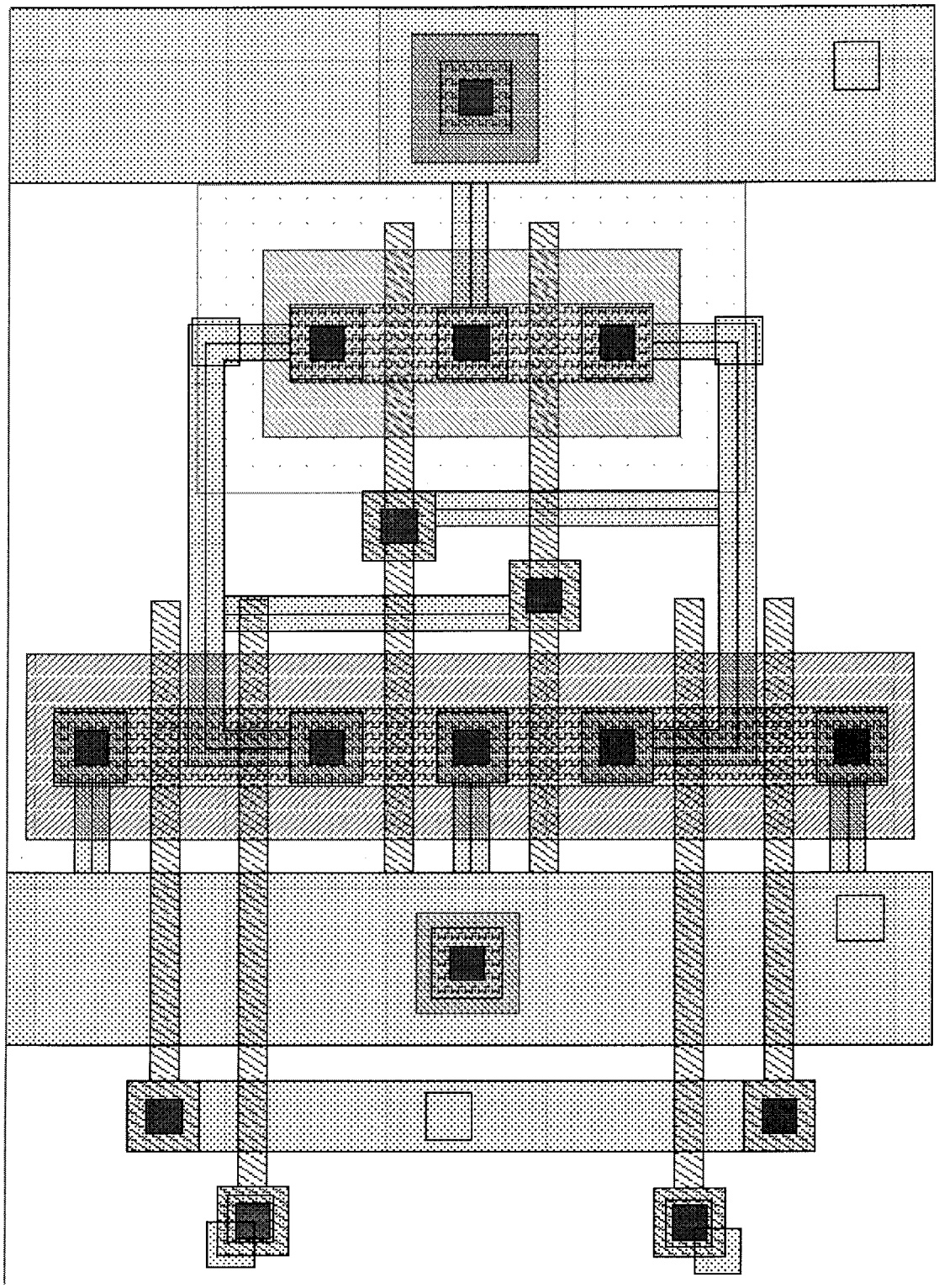


Figure 3-11: Latch layout diagram

3.6 Current Sources and Isolation

Fig.3-12 shows the schematic of a conventional cascade current source circuit used in this design. We try to keep the unit array current source as simple as possible since 960 current cells driven by four and six double segmented thermometer decoder cost a vast area in chip die. A cascade current cell easily satisfied the necessary requirements, such as high-speed and simplicity for this design.

In general, the resolution and errors (DNL and INL) in DAC are determined by current source. The DNL results from device mismatches in current source and can be reduced by increasing the device channel length M1 and M2, and careful layout for device match. However, increasing the device channel length comes by the effective gate area expansion and eventually, increasing parasitic capacitance and consequently, settling time. Therefore, the optimization of the device size is required for both a device mismatch and a fast settling time.

However, in this design, DNL error caused by the device mismatch is not as crucial as the low settling time is. Therefore, the device size is kept as small as possible.

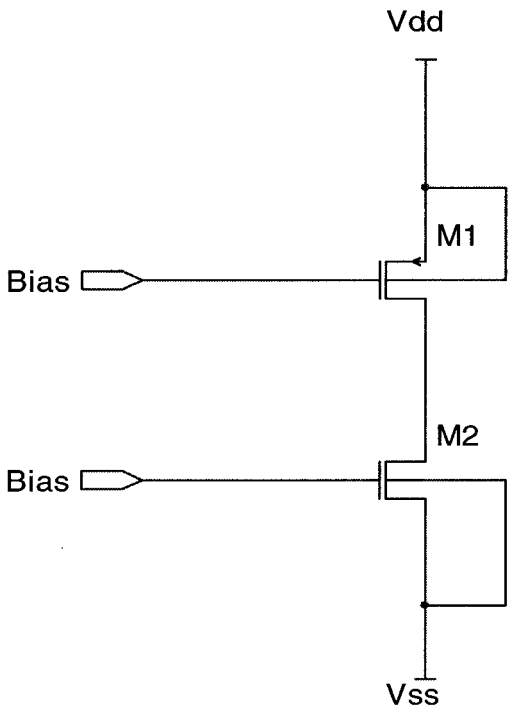


Figure 3-12: Current Source Circuitry

The layout photo of current source is shown in Fig. 3-13.

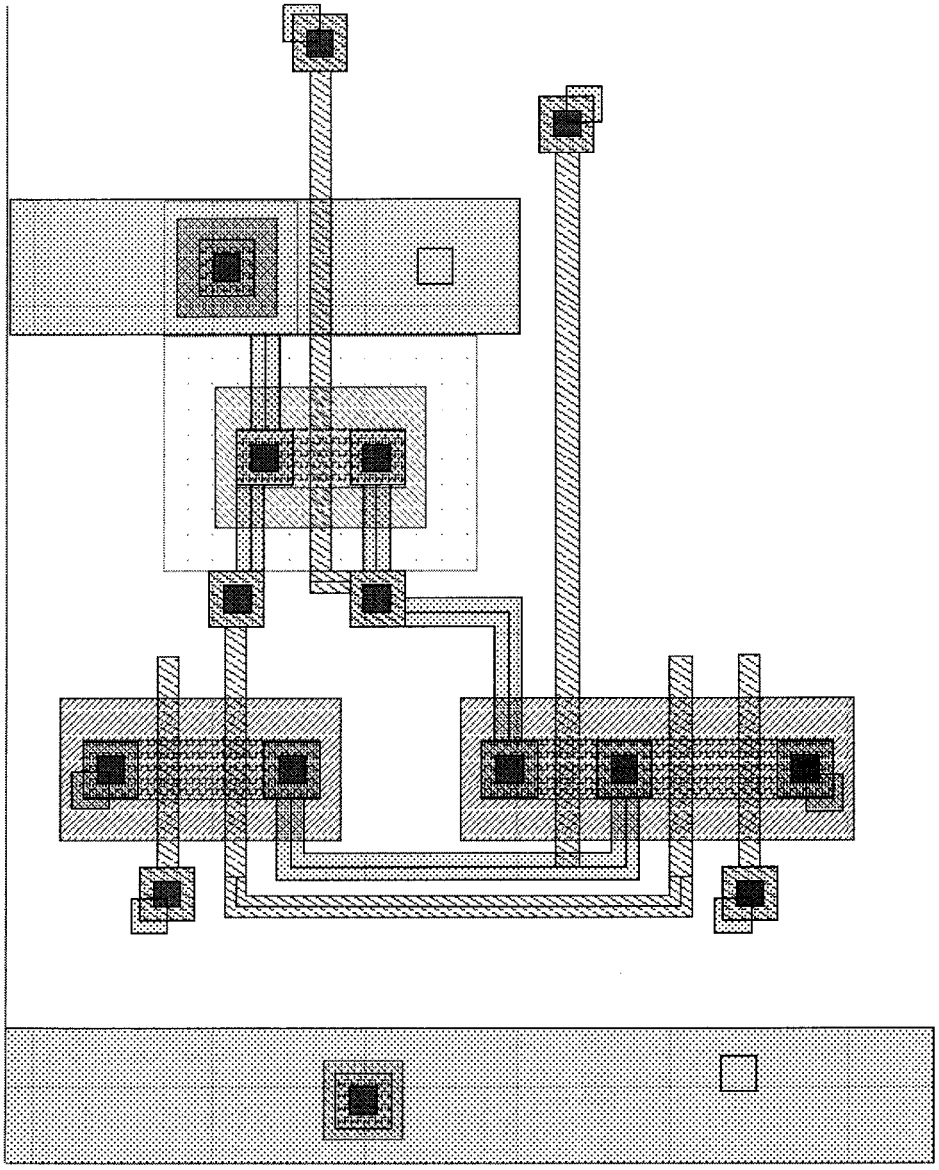


Figure 3-13: Current source layout design

The accumulated DNL error and output resistance variation of the current source cause the INL error. Fig. 3-14 shows the equivalent circuit diagram of the current source matrix. r_L is

representing the current source output resistance. If the numbers of the current source turned on is K, V_{OUT} and INL can be expressed as:

$$V_{OUT} = -(KI_L)(R_{LOAD} \parallel \frac{r_L}{K}), \tag{3-9}$$

$$INL = (KI_L)\left[(R_{LOAD} \parallel \frac{r_L}{960}) - (R_{LOAD} \parallel \frac{r_L}{K})\right]. \tag{3-10}$$

The INL can be minimized by increasing the output resistance of each current source. The cascade current mirror is a good choice to obtain high output resistance as mentioned above.

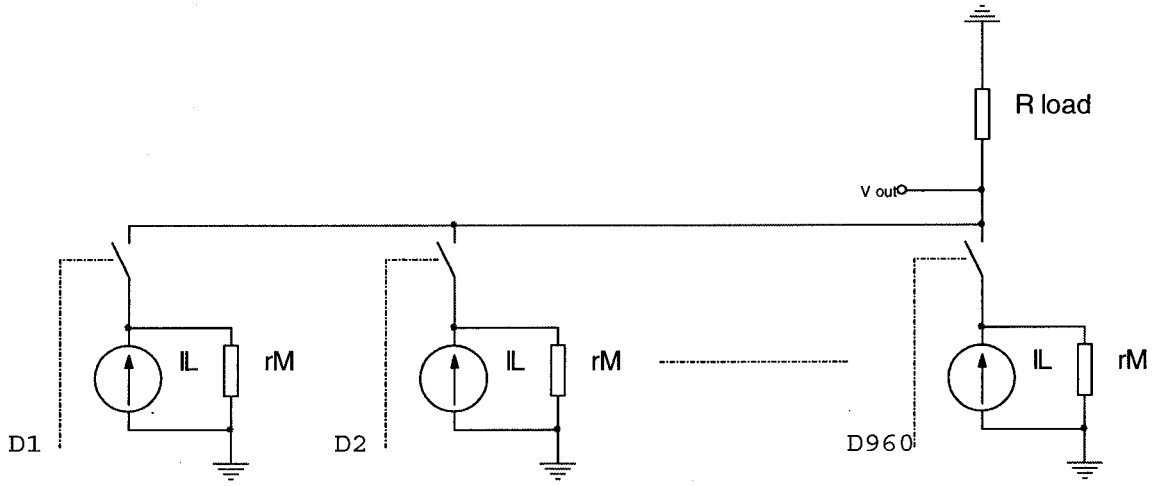


Figure 3-14: Equivalent circuit diagram of current source matrix

3.6.1 Choice of Switch Device

The switching of the output stage from current sources increases DAC nonlinearity by disturbing the settled position of DAC. Isolating of the switching section from the current sources can be achieved by different isolation circuitry. A double cascade circuit composed of

M1 and M2 is present between output stage and current sources, thus forming isolation circuitry for each cell in current source matrix [20].

All switches are implemented using the minimum-length NMOS devices operating in the saturation region. The important performance parameters of these switches from the dynamic linearity viewpoint can be summed up as the on-resistance R_{ON}, the channel charge Q_{CH}, and the junction capacitance C_J. All of these parameters are somehow reliant on switch size in the N-well process. The use of NMOS transistors optimizes the switch size as compared to PMOS transistors in terms of dynamic linearity performance.

The NMOS device will have smaller R_{ON} than PMOS device for the same device dimensions, while showing similar Q_{CH} and C_J to first order. Alternatively, it is possible to obtain the same R_{ON} with smaller NMOS device size, while profiting from smaller Q_{CH} and C_J. The size of the NMOS switches in this design is 500n/180n. Implementation of PMOS device in current switches also has its own beneficial reasons such as, better shielding from substrate noise, hence lower g_m and spurious fluctuation in their gate bias voltage. Since having low R_{ON} in this work is very crucial for us, we prefer to sacrifice PMOS advantages over NMOS ones.

3.6.2 Control Signal Feedthrough

Another advantage of using cascade switch transistors is reducing a main source of glitch energy, which is penetration of control signals to the output lines. The coupling of the switching control signals to the output lines through the parasitic gate-drain capacitance of the switching transistors is also a source of glitches. The voltage variation at the DAC output is approximately given by

$$\Delta V \approx \frac{nC_{gs2}}{C_L + C_{stot2}} \Delta V_{G2}, \tag{3-11}$$

where ΔV_{G2} is the control voltage swing, C_{stot2} is the total parasitic source capacitance of the switching transistors, and nC_{gs2} is the total gate-source capacitance of n switching transistors

being driven simultaneously. When n is large, significant glitch appears at the DAC output. Furthermore, since the glitches are code dependent, they cause distortion of the input signal. One solution to minimize this variation is to reduce ΔV_{G2} to the minimum necessary amplitude. In this work, this solution is not implemented because of fast control switching signals requirement. Nevertheless, by decreasing the voltage supply of the latches, the swing of V_{G2} can be reduced, with a consequent reduction of the coupling to the output lines. The second solution is to operate the switching transistors in the linear region and to attempt to compensate the signal feedthrough by connecting in parallel dummy transistors driven by the complementary control signal [21]. This alternative has also drawbacks: 1) the internal pole is moved to lower frequencies and 2) the compensation is only partial. To minimize the feedthrough to the output lines, the source of the switching transistors is isolated from the output lines by adding two cascaded transistor (with the same dimension as the switching transistors) in the proposed design, as shown in Fig. 3-15. For low-to-high transition of the control signal, while the switching transistor is forming a channel, the cascade transistors are off and the signal path from the source of the switching transistor to the output node is open. The coupling is, therefore, avoided. For high-to-low transition some coupling exists at the beginning, but since the switching transistor cuts off very fast, the voltage at the drain of the cascade transistor drops, turning it off, and isolating the output node for the remaining of the transition of the control signals.

3.6.3 Voltage fluctuation

Ideally, the voltage at the output nodes of current sources should be constant. During the switching phase, however, a significant voltage variation can occur. The parasitic capacitance at the output node of current sources can be very large, producing a relatively low frequency pole.
In the discussed current source, voltage variation in the drain node of output section can significantly degrade the dynamic characteristics of the DAC. There are several circuits designed to minimize the impact of the voltage fluctuation on the dynamic characteristics of the DAC. Cascade configuration is one of the most popular solutions to isolate the output nodes of the current sources. This solution is only effective, however, provided that cascade transistor remains in saturation. There is another assistance to solve the corresponding problem in this design.

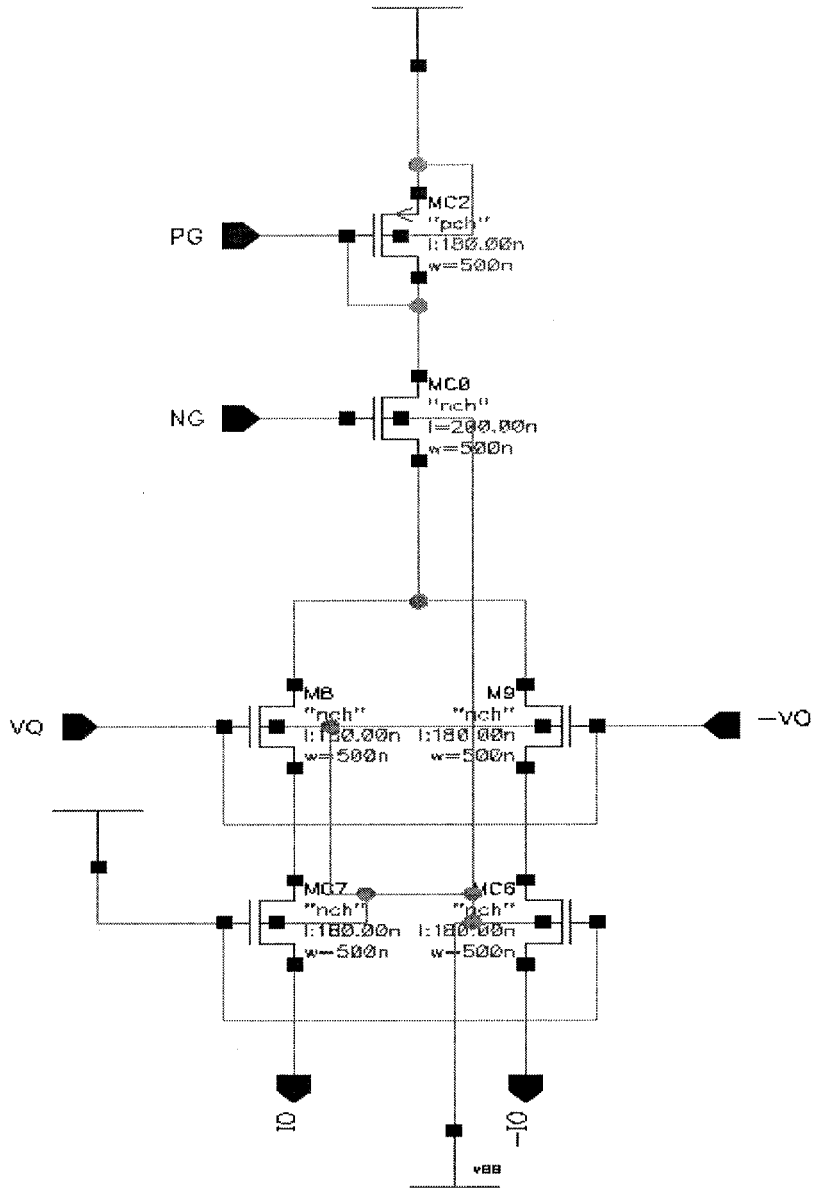


Figure 3-15: Current cell with cascade transistors

High-speed conversion rate is achieved by a current source with a delayed driving scheme. In this driving scheme, a current switch is turned off slightly after the other current switch is turned on. This driving scheme reduces fluctuation of internal node voltage of the current source and high-speed switching is realized. In this driving scheme, a NOT gate generates delay in one of the matrix switching decoder outputs so that one current switch is turned off slightly after the other current switch is turned on. Therefore the cross point of gate voltage in current source switches becomes lower and the fluctuation is reduced.

3.6.4 Biasing the Current sources Matrix

As shown in Fig. 3-16, the biasing circuit is composed of two transistors, which provide two biasing voltages PG and NG for all of the current sources. Changing the biasing voltages can adjust the output current of each current cell.

Fig. 3-17 presents layout of bias current circuit. The current matrix cell comprised of current source, latch and matrix switching decoder is simulated as shown in Fig. 4-3. This simulation is performed in order to determine the settling time and maximum update frequency only for a single current matrix cell. The result is very close when using a full current matrix.

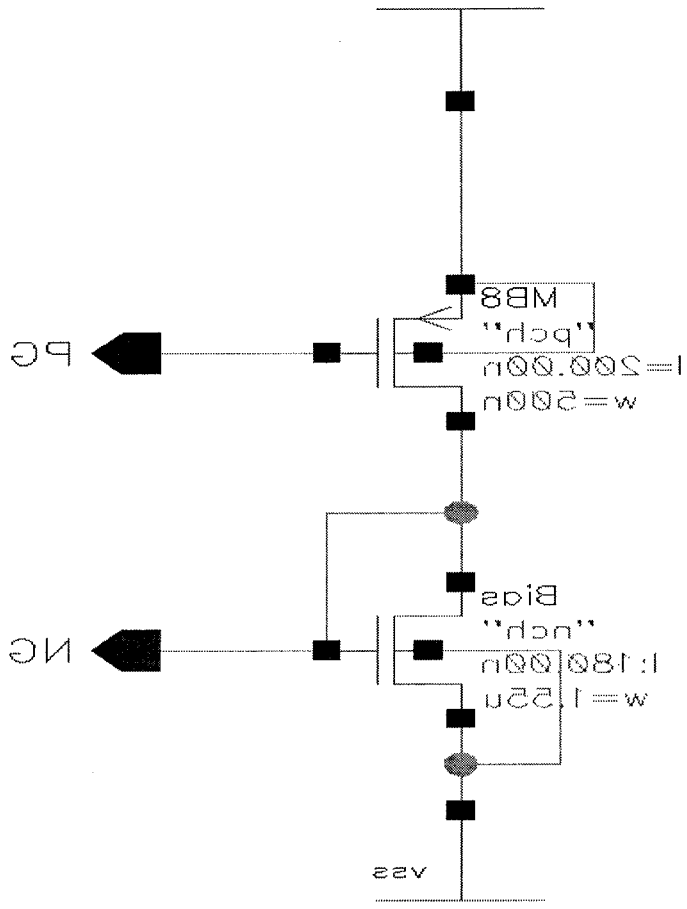


Figure 3-16: Proposed biasing circuit

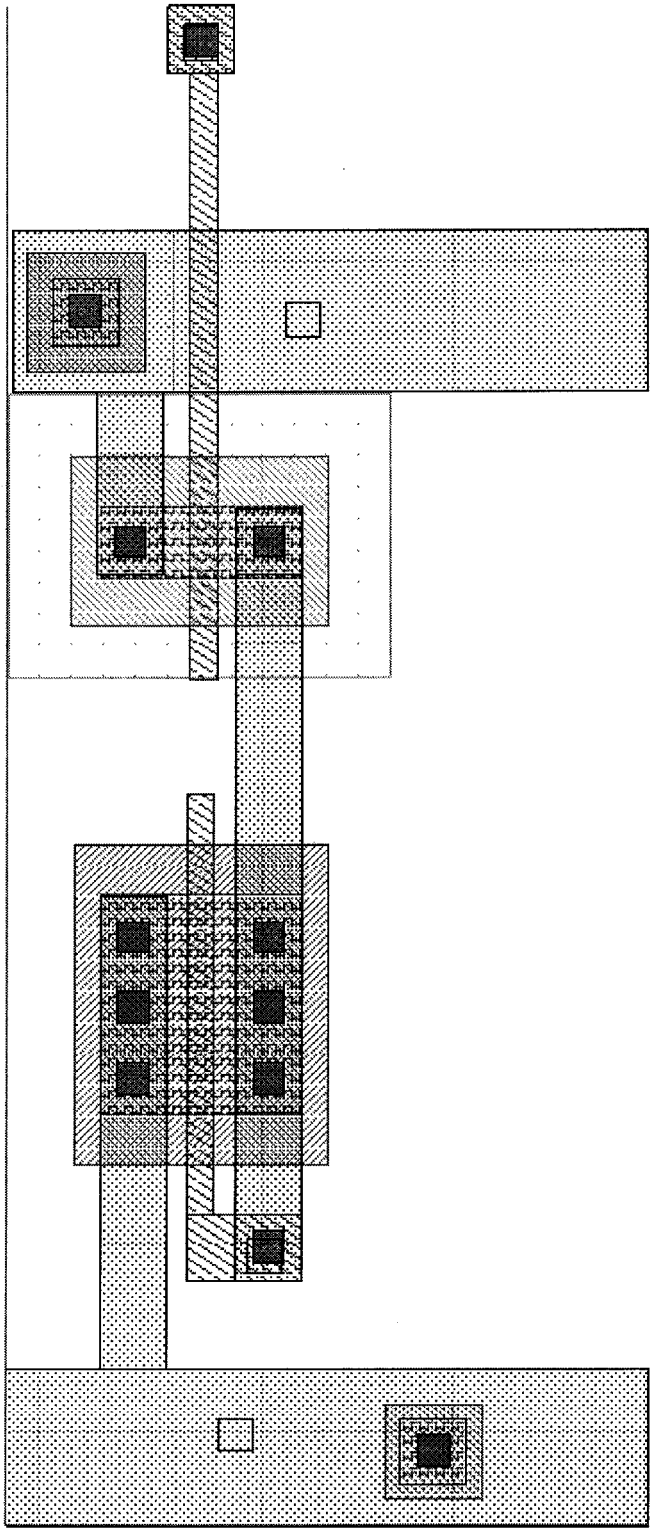


Figure 3-17: Bias circuit layout design

3.7 Load Resistor

Due to current source constraints we need a very small resistor as load to minimize the output voltage range, entering to the op-amp. A single transistor can be used to achieve 2-Ohm resistor. However it would result in a huge transistor, which is out of range for Cadence simulation tools. In order to have very small resistor without involving the accuracy issues related to fabrication, we implement 10 parallel 20 Ohm resistors, constructed from NMOS transistors in deep triode region. The size of these transistors has been chosen to produce. Fig. 3-18 (a) represents the schematic of the discussed resistor and Fig. 3-18 (b) shows the transient response to 1GHz input pulse.

As we observe from output voltage and current waveforms in Fig. 3-18 (b), settling time of NMOS resistor is less than 1ns which is fast enough for this design and also there is no disturbance from parasitic capacitance. The resistor is tested for different input pulse amplitudes to make sure its linearity.

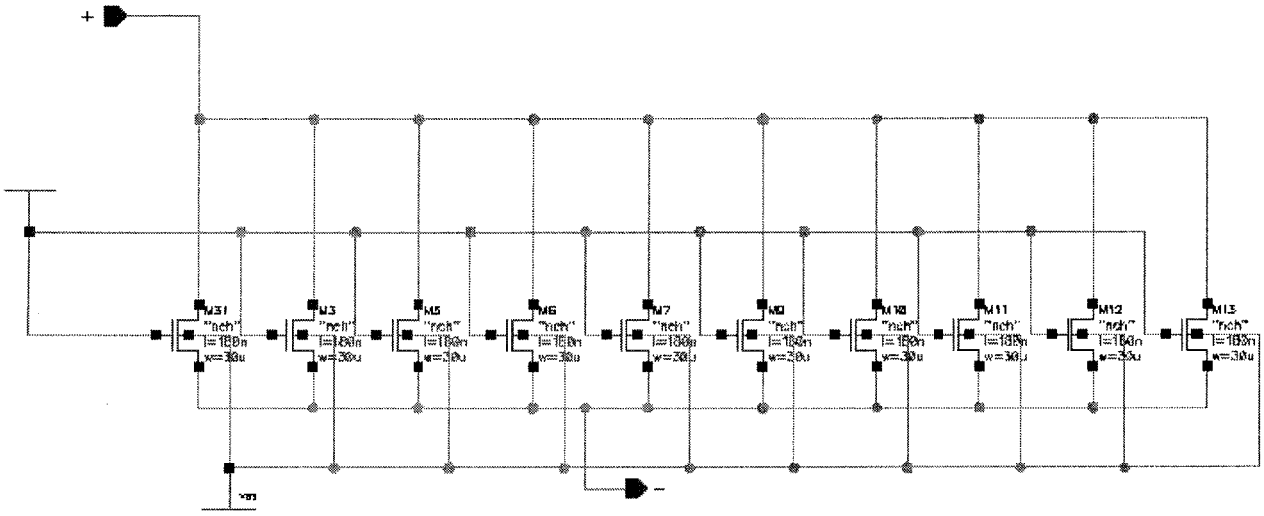


Figure 3-18 (a): Schematic of NMOS Resistor

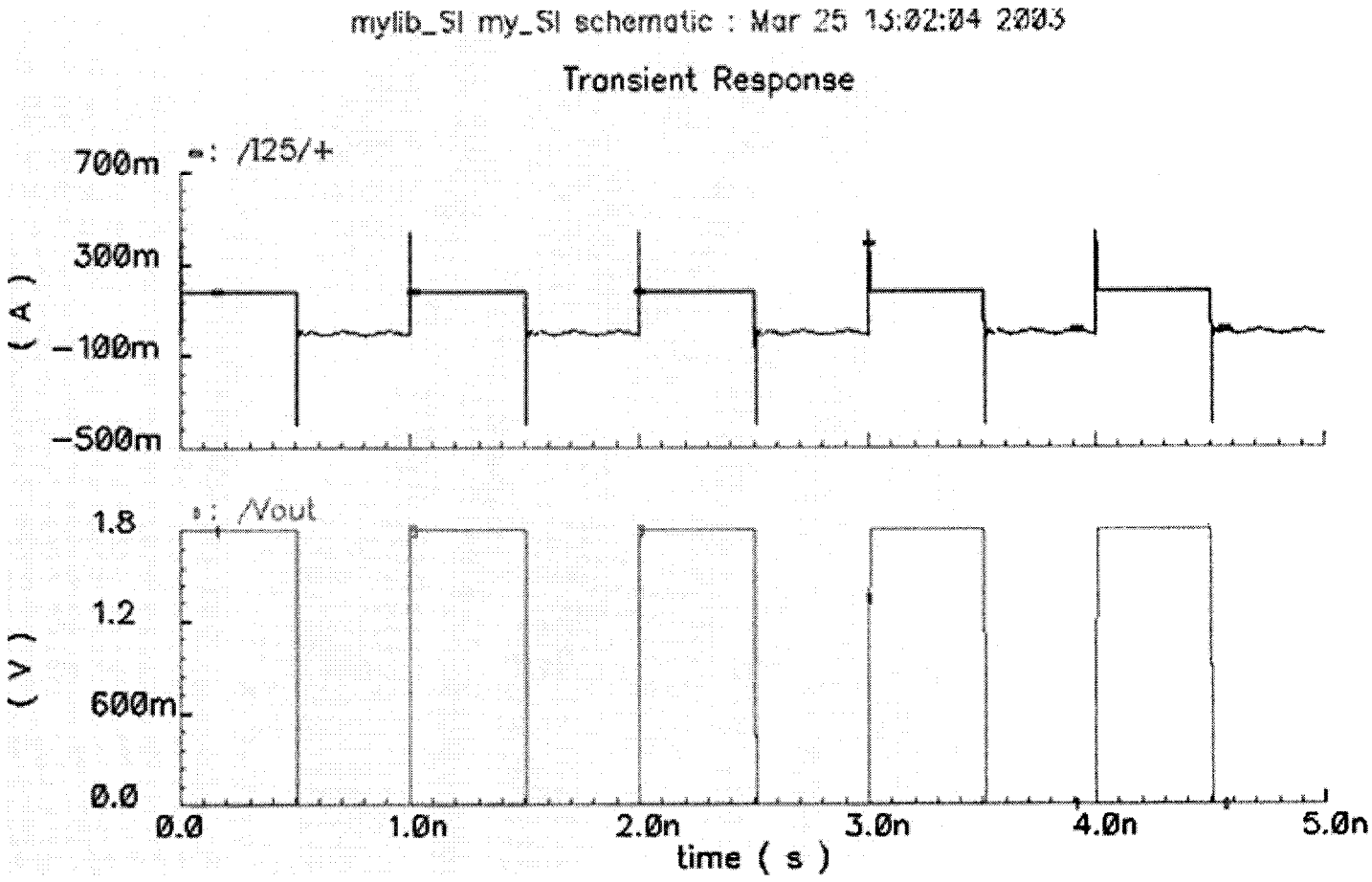


Figure 3-18 (b): NMOS Resistor transient response to 1GHz input

Fingering is a solution to the limitation of the maximum width of a transistor [22]. Fingering technique is used to finger a large transistor into multiple transistors that are connected in parallel. Another reason to use fingering is to optimize the resistance of the gate poly along the width of the transistor. Since the gate poly is driven from one end and gate poly is resistive, there may be reason to have a guide line that states the minimum width of a single finger.

Fingering the PMOS devices is straightforward; however, fingering the series NMOS devices is more difficult because the order of connectivity of the devices must be maintained. Fig. 3-19 shows the layout design of ten 30 μm wide parallel transistors where each of them is fingered into ten 3 μm wide transistors in parallel.

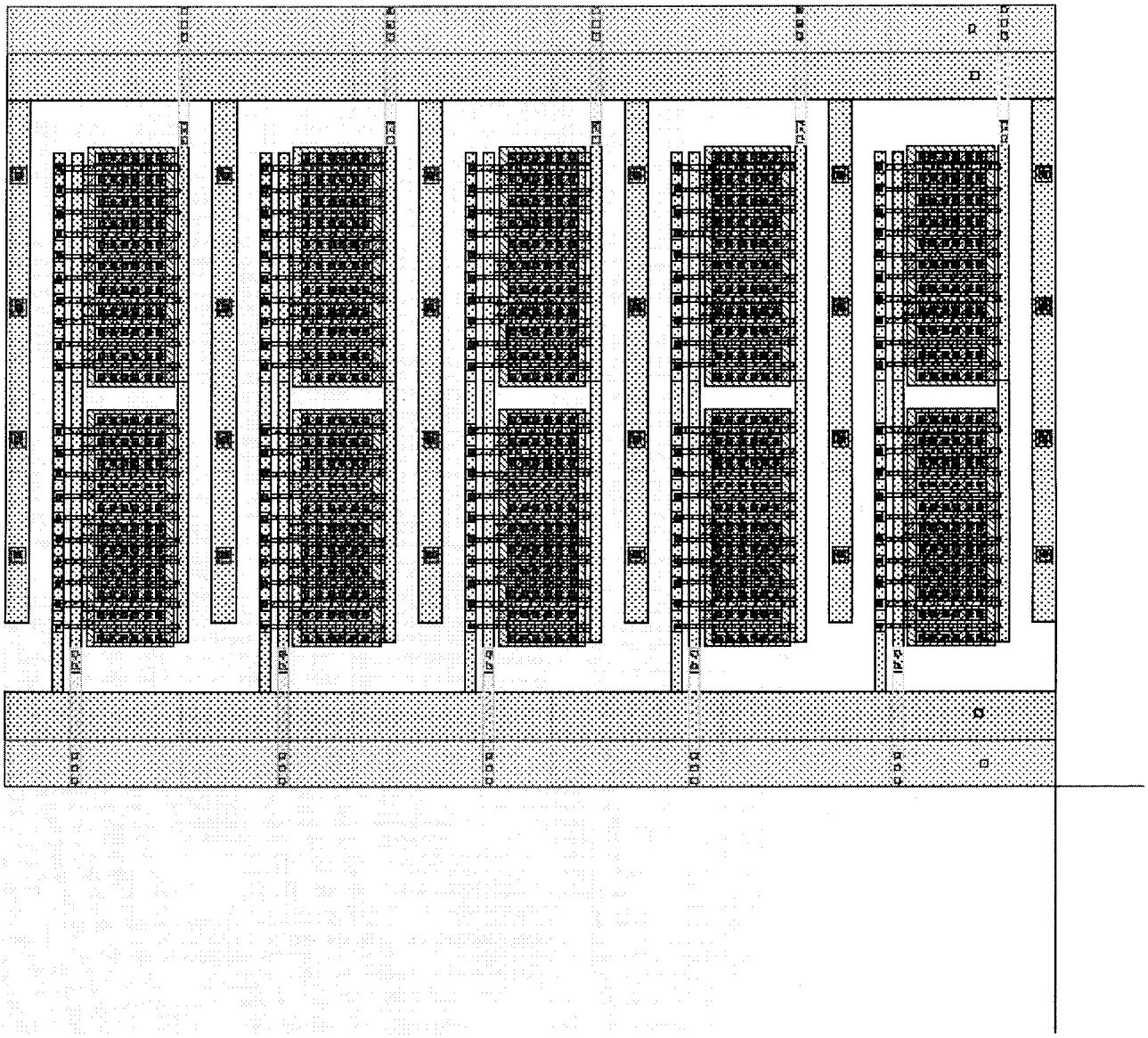


Figure 3-19: Layout of NMOS resistor using fingering technique

3.8 Output stage

The design of output stage is aimed to convert the output current from current source matrix into voltage. The current-to-voltage topology and the advantages of the differential implementation are discussed next.

3.8.1 The current-to-voltage converter

If the output of the current-source array were fed only into a normal resistor, its voltage would be sensitive to the load impedance and also wouldn't provide the required output voltage range for a standard DAC. Therefore, a two stage operational amplifier is used to convert current from DAC to voltage. This operational amplifier should have very high input impedance, low output impedance, high open-loop gain and high slew rate to achieve high-speed DAC.

3.8.2 Differential Implementation

The output circuit is implemented differentially to take advantage of the differential outputs current of DAC. In this differential arrangement, the gain and linearity are substantially improved over basic single-end amplifiers.

The advantages of using differential output can be summarized as:

- High gain.
- Low noise for the amount of gain developed
- Good high frequency bandwidth
- Low distortion

and the main disadvantage is: High output impedance.

3.8.3 Op-Amp Design

Operational amplifiers are an integral part of many analog and Mixed-signal systems. In this section, we describe a number of op-amp design parameters which are critical in the output stage of this particular DAC architecture.

Gain

The required gain in this design may not be as critical as other design parameter. Trading with parameters such as speed and output voltage swings, the minimum required gain must, therefore, be known.

Small-Signal Bandwidth

As the frequency of operation increases, the open-loop gain begins to drop, creating larger errors in the feedback system. The small-signal bandwidth is usually defined as the "unity-gain" frequency, f_u, which exceeds 1 GHz in today's CMOS op-amps.

Large-Signal Bandwidth

When op-amps operate with large transient signals, nonlinear phenomena makes it difficult to characterize the speed by merely small-signal properties such as open-loop response. If we apply a large step voltage at the input, the output voltage cannot change instantaneously. The large signal behavior is usually quite complex, mandating careful simulation.

Output Swing

As the chip operates at 1.8V power supply voltage, large output swing is very crucial in this design to accommodate a wide range of signal amplitudes. The maximum voltage swing trades with device size and bias current and, hence, speed.

Linearity

Linearity is the main characteristic parameter that helps this architecture over the other DAC architectures. In this circuit, the linearity requirement, rather than the gain error requirement, governs the choice of open-loop gain.

The op-amp tends to be the major bottleneck in limiting the overall conversion speed of DAC. Op-Amps introduce several dynamic nonlinearities of their own, due to their nonlinear transconductance transfer functions. The requirement for the Op-amp is a gain of 500 with a 0.5-V_{PP} swing into a $100K\Omega$ load.

The DAC applications often require an op-amp with exceptionally high DC gain. While high DC gain is often accomplished with the use of cascading and gain boosted output stages, 1.8 volt

operation limits the use of these techniques. The common approach to achieving high gain with a low supply voltage is to cascade several gain stages.

A two stage Op-amp with a folded cascade input stage and NMOS cascade amplifier output stage was found optimal for high linearity with adequate voltage gain.

3.8.3.1 First Stage

In order to achieve a high gain, the differential cascade topology can be used in stage 1 [23]. A folded-cascade op-amp incorporating NMOS input devices and PMOS cascade transistors is shown in Fig. 3-20. To minimize the device capacitances, we select the minimum length for each transistor, and calculate the width. The output PMOS-devices was designed for the optimum V_{dssat} voltage and for a short channel length to minimize the parasitic capacitance at the node A (B). A cascade connection has very high output impedance, so it needs a second stage to be connected to the output in order to reduce output impedance.

Common-Mode (CM) Feedback

In high-gain amplifiers, the output CM level is quite sensitive to device properties and mismatches and current cannot be stabilized by means of differential feedback. Thus a common-mode feedback network must be added to sense the CM level of the two outputs and accordingly adjust one of the bias currents in the amplifier. In the first stage, CMFB is implemented by applying the feedback to the tail current of the input differential pair. Common-mode output voltage, $V_{out,CM}$, is somewhat sensitive to the value of V_{b3}: if V_{b3} is higher than expected, the tail current of M9 and M10 increases and the CM output level falls. Since the feedback through M12 and M13 attempts to correct this error, the overall change in $V_{out,CM}$ depends on the loop gain in the CMFB network.

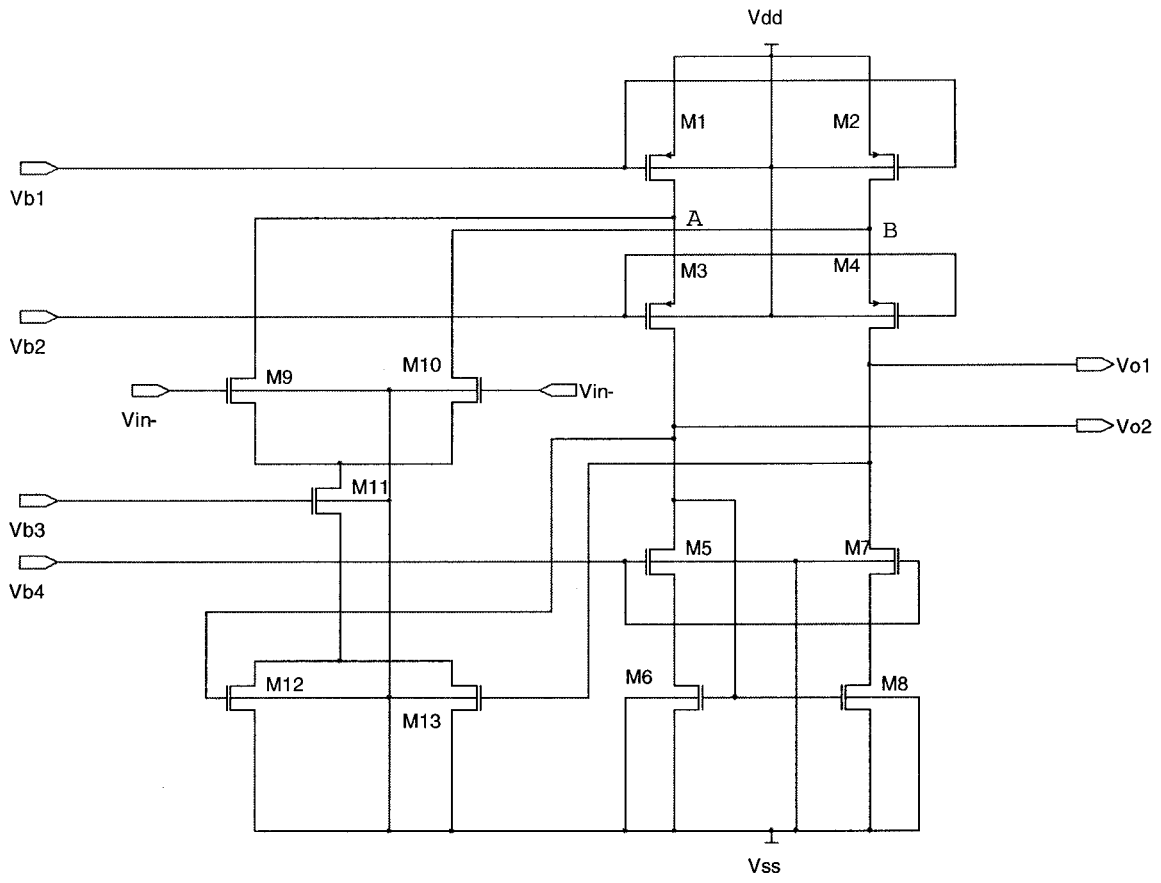


Figure 3-20: Folded-cascade topology implemented in the first stage

3.8.3.2 Second Stage

A large voltage gain requirement leads us to choose a common-source with current source load for the implementation of the second stage. The circuit is shown in Fig. 3-21, where all transistors operate in saturation. $r_{35} \parallel r_{36}$ and $r_{29} \parallel r_{30}$ are the total impedances seen at the output nodes 1 and 2 respectively. The gain for each output is calculated by

$$A_v = -g_{30,36}(R_O), \qquad (3\text{-}12)$$

where R_O is output impedance.

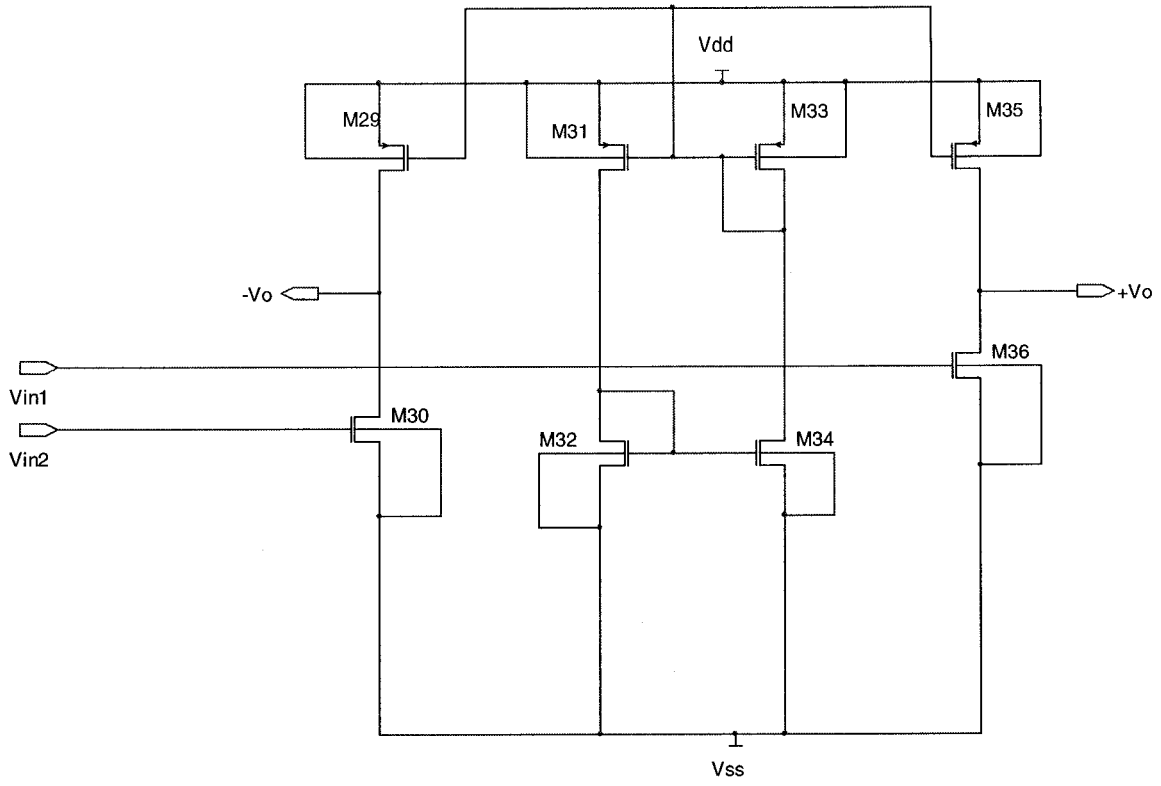


Figure 3-21: CS with current-source load used in the second stage of op-amp

The size of transistors M30 and M36 from the second stage have been properly allocated to reduce the output capacitance of the first stage. This results in minimum raise time for the op-amp and eventually higher update frequency for the DAC. In Fig. 3-22, two stages have been attached in order to provide high gain with the first stage and large swing with the second stage. The bias circuit comprised of transistors M21-M24 and M25-M28 are sized such that the voltage on first stage output node is set to value nominally equal to VDD/2.

Due to transistors M14-M16, which provide biasing voltages for transistor M1-M8, the current in the bias branch M14-M15 is mirrored in the input branch M9 and M10. Another important issue in the analog design is the voltage reference. In this design, the gate of M19 is connected to an external voltage reference in order to adjust the output dynamic range.

A transient simulation with an increasing input step current from 0 to 600 μA is illustrated in Fig. 3-23. V_{in} is the voltage in the resistor node and V_{o1}, V_{o2} are the output voltage for stage 1 and 2 respectively. The settling time is less than 5 ns.

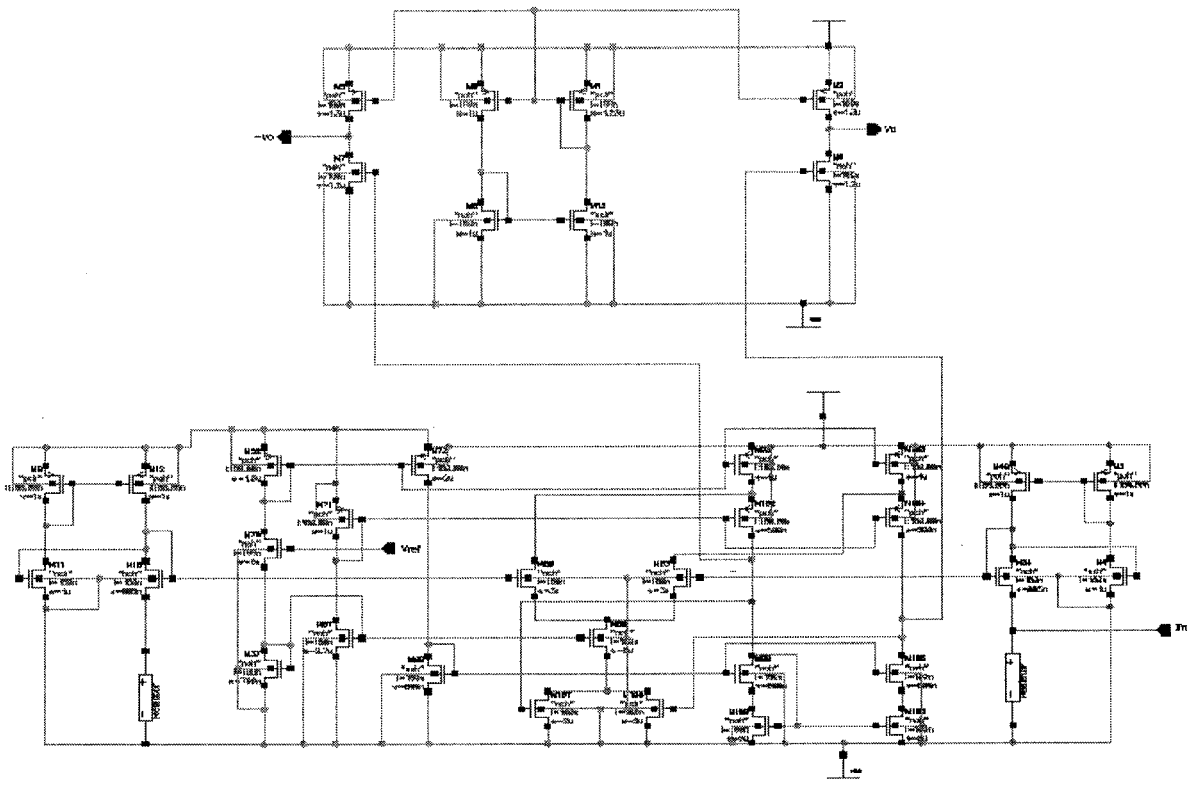


Figure 3-22: Two-stage folded-cascade op-amp

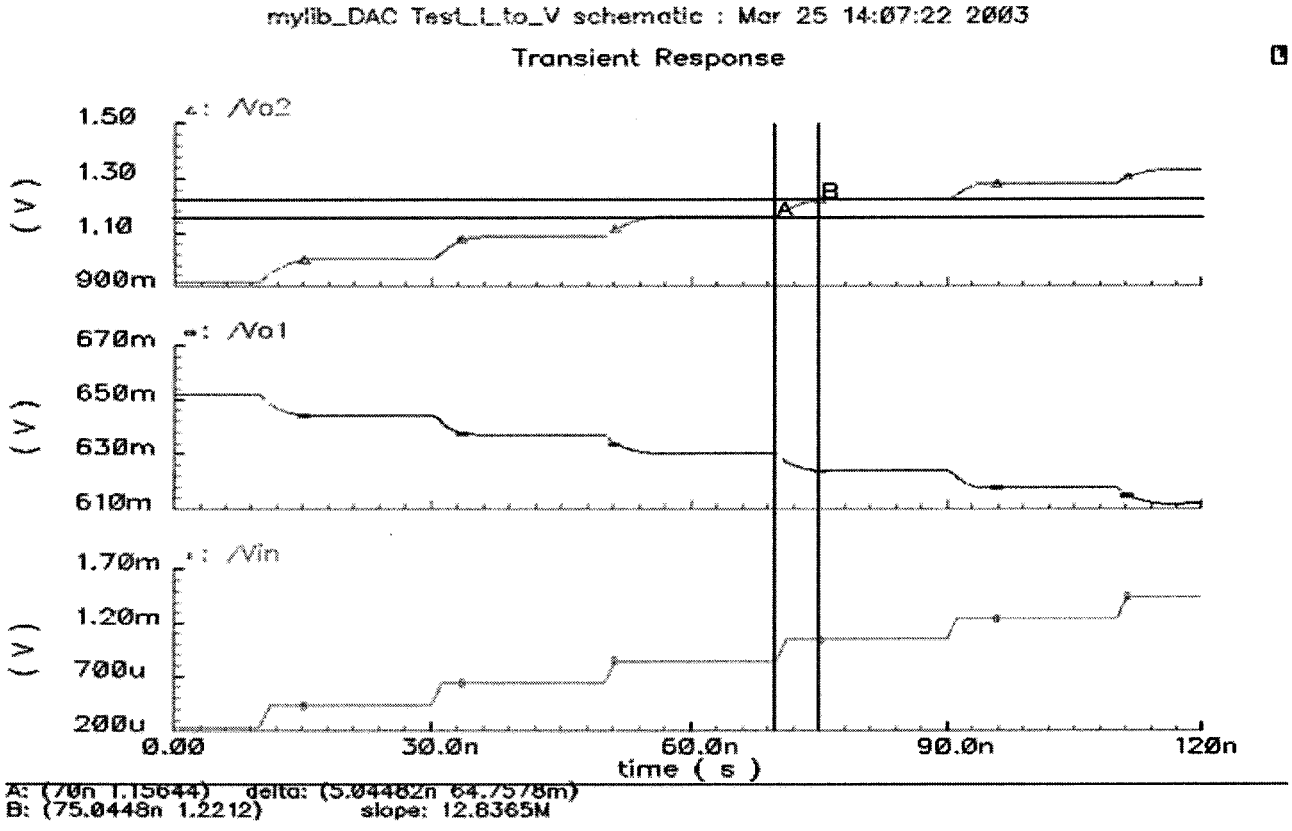


Figure 3-23: Output voltage waveforms of two stages

Fig. 3-24 shows the layout of the op-amp, using fingering technique for NMOS resistor layout.

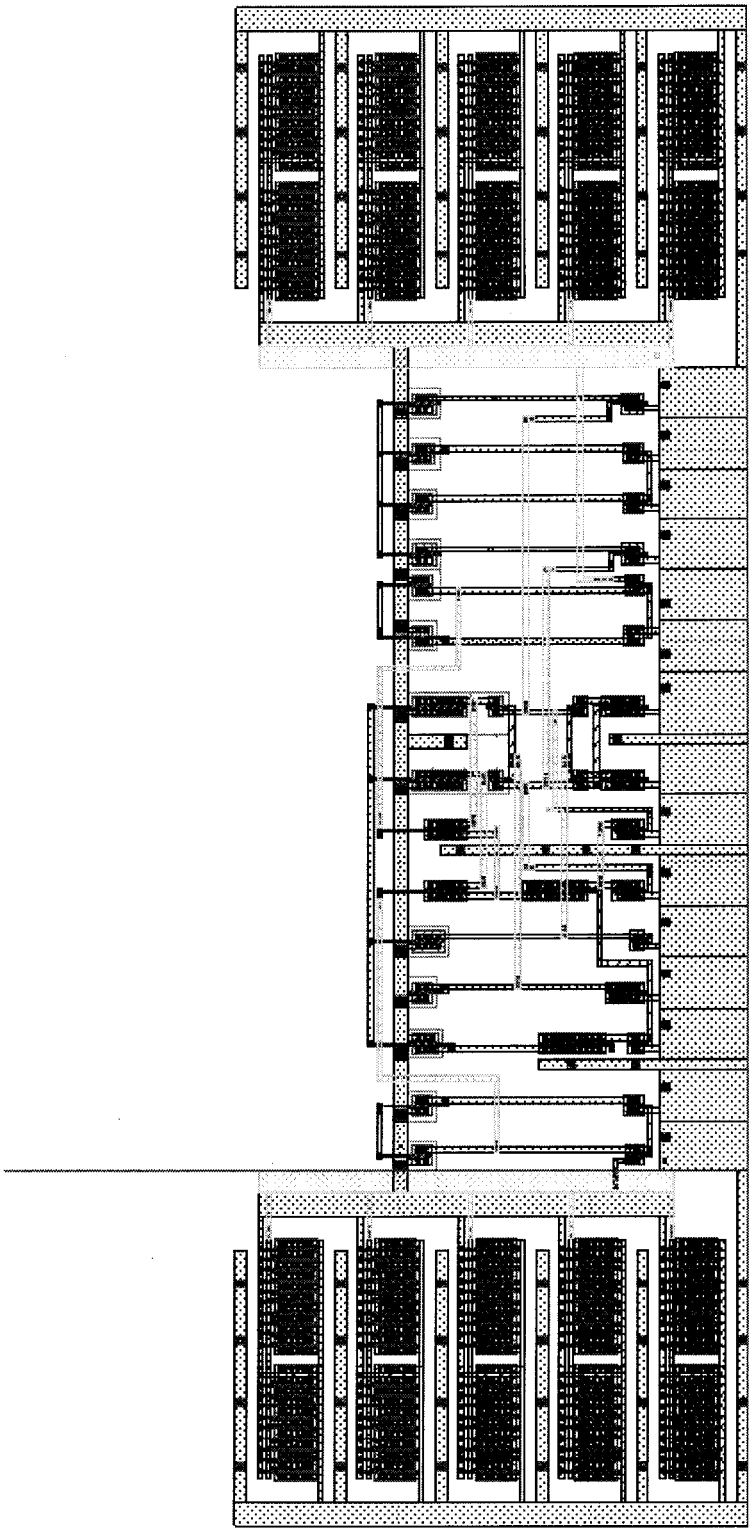


Figure 3-24: Layout design of two-stage folded-cascade op-amp

Chapter 4

Simulation Results

The noise effect in proposed designed DAC and present different measurement results of DNL and INL, which are main contributions in this design are presented and discussed. Simulation results confirm the maximum update frequency and linearity.

4.1 Noise Effect in DAC Performances

Designing DACs with linearity of 10 bits and higher requires that the random and systematic errors are reduced to a level well below the noise floor. Intrinsic 10-bit linearity can only be achieved by tackling all possible random and systematic errors.

4.1.1 Static Errors

There are in principal two types of static errors 1) random errors 2) systematic errors. In the following we first discuss the source of these errors and then mention the solution used in this design.

4.1.1.1 Random Errors

Random errors in DAC are due to random variations in the fabrication process. Typically in CMOS processes, capacitor matching up to 0.1% and transistor matching up to 0.1% are achievable. Using these elements in a current source DAC will provide at best 10 bits of linearity. Trimming and/or calibration can be used to improve this linearity, but it requires either manufacturing adjustments or a measurement and calibration cycle during operation [24].

An alternative technique for reducing the effects of random component mismatches in DACs is to use dynamic element matching (DEM). Dynamic Element Matching does not require prior knowledge of the component mismatches, thus spreading the errors out over the frequency spectrum. The DEM algorithm controls the selection of the elements in the DAC so that the mismatch errors are attenuated at low frequency. There are several DEM algorithms, which have been developed that provide first-order shaping of the DAC mismatch errors.

A minimum requirement to meet a 10-bit accuracy specification is that the current sources controlled by each bit of the digital input word have an error less than ½ LSB. While this requirement is easy to meet for the current sources controlled by the LSB's, it becomes very difficult to achieve for the current source controlled by the MSB as it requires this current source to have a relative accuracy of

$$\frac{\Delta I_{MSB}}{I_{MSB}} \leq \frac{1/2LSB}{2^{N-1}LSB} = 0.097\%, \tag{4-1}$$

where N is the DAC accuracy. When the MSB current source is implemented by connecting in parallel 2^{N-1} unit current sources of I, an approximate expression for the DAC INL specification as function of the random fluctuation in the nominal value of the unit current sources is simply given by adding the variances of the 2^{N-1} unit current sources

$$INL \approx \sqrt{2^{N-1}}\left(\frac{\sigma_I}{I}\right)LSB, \tag{4-2}$$

where (σ_I / I) is the unit current source relative standard deviation, and assuming that each unit current source has a value that follows a normal distribution.

4.1.1.2 Systematic Errors

The systematic errors, such as finite output resistance in current-mode DACs can limit the linearity as well as the random Errors. The fundamental building block of a current-mode DAC is the current source. In order for the DAC to achieve high resolution and linearity, good matching between the different current sources is needed. Fig. 4-1 (a) shows a 2-bit DAC

constructed from n ideal current sources. The magnitude of each current source is exactly I_{LSB} amps, and the voltages at the output are linearly related as $V_{dac} = nI_{LSB}R_{dac}$. Fig. 4-1 (b) shows the same DAC implemented with simple PMOS current mirrors. With actual devices, V_{dac} is dependent upon the finite output resistance R_{out_n} of each current source connected to R_{dac}. This results in the following,

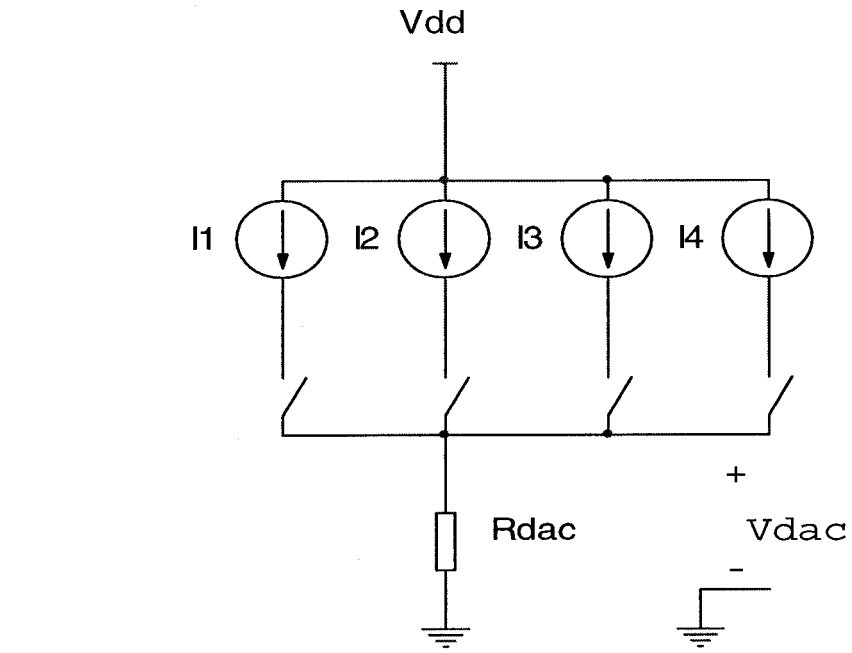
$$V_{dac\,n} = \frac{\sum_{i=1}^{n} I_{LSB_i}}{\frac{1}{R_{dac}} + \sum_{i=1}^{n}\left[\frac{1}{R_{out_i}}\right]}. \tag{4-3}$$

As more current sources are connected to R_{dac}, the overall output resistance drops thus producing nonlinearity in the output voltage, and contributing a systematic errors. To minimize the systematic error, the output resistance of the current sources must be maximized. The expression for the output resistance of the simple current mirror in Fig. 4-1 (b) is $R_{out} = (1/g_{ds})$. Increasing the output resistance of the current sources by using cascade topology, as shown in Fig. 4-2, increases the linearity significantly. The output resistance of the cascade current mirror is $R_{out} = (g_{mc1}/g_{ds1}g_{dsc1})$, which results an increase in the self-gain of the cascade device over the simple current mirror.

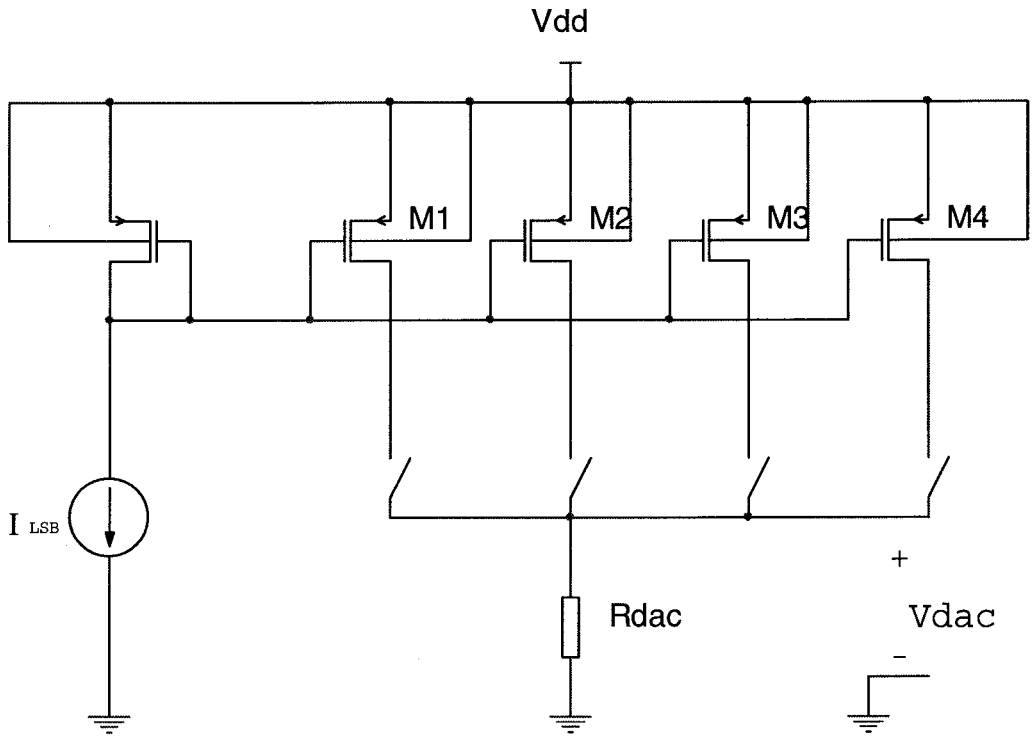
4.1.2 Dynamic Errors

The dynamic performance of this DAC can be characterized by the dynamic nonlinearities associated with current source switching. These nonlinearities are mainly caused by the following effects:

- An imperfect synchronization of the input signals of the current switches,
- Current variation due to a drain voltage variation of the current sources caused by the fact that both current switches are simultaneously in the off-state,
- Transient output response of the current source.



(a)



(b)

Figure 4-1: 2 bit DAC implemented with (a) ideal current sources, (b) simple current mirrors

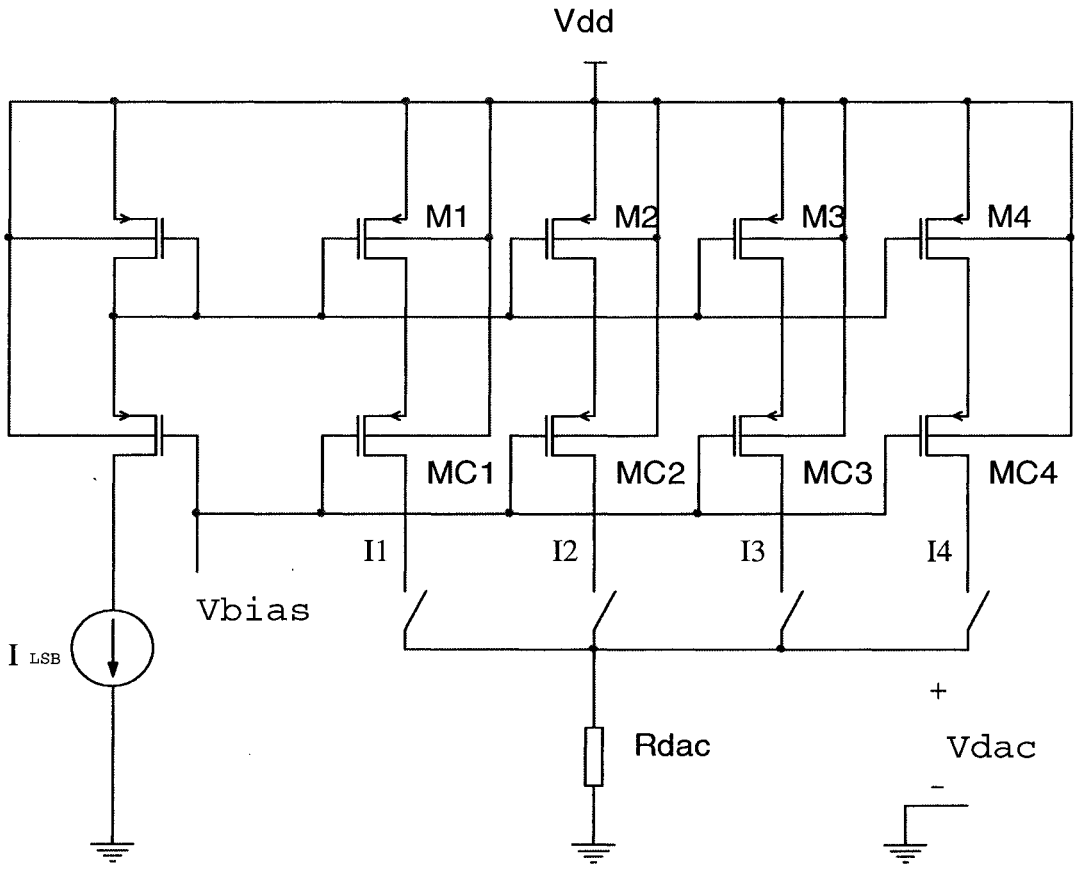


Figure 4-2: 2-bit DAC implemented with cascade current mirrors

The following measures are taken to reduce the dynamic nonlinearities. To improve the synchronization, a latch is placed directly in front of current switches. This latch provides two complementary signals needed at the input of current switches. This latch also reduces the current variation due to the drain voltage variation of the current sources.

4.1.3 Noise in Current Source

Since the analog section constantly deal with the problem of noise more than the digital part, we focus on the noise measurement of the current source in the proposed design.

Assuming the devices in Fig. 4-3 operate in saturation and the circuit is symmetric, input-referred noise voltage is calculated as follows:

To calculate the input-referred noise voltage, we short the input to the ground, obtaining

$$\overline{i_{nD1}^2} = \frac{2}{3} \cdot 4 \cdot kTg_{m1}\Delta f + \frac{kg_{m1}^2}{C_{ox}(wl)_1}\frac{\Delta f}{f}, \tag{4-4}$$

where k is the Boltzmann constant, T is the absolute temperature, and C_{ox} is the gate oxide capacitance per unit area. $\overline{i_{nD2}^2}$, $\overline{i_{nD5}^2}$, $\overline{i_{nD6}^2}$ are calculated in the same way as above. Since the thermal and $1/f$ noise of M_3 and M_4cab be modeled as voltage sources with the input, we only need to refer the noise of M_1, M_2, M_5 and M_6 to the input.

The thermal noise exhibited from load resistors is given by

$$\overline{i_{nD7}^2} = \frac{4kT}{R_{load}}\Delta f \quad \text{where } R_{load} = R_{load1} + R_{load2}. \tag{4-5}$$

Thus, the total input-referred noise voltage is calculated as

$$\overline{V_{n1}^2} = \frac{\overline{i_{nD1}^2}}{g_{m1}^2}, \overline{V_{n2}^2} = \frac{\overline{i_{nD2}^2}}{g_{m2}^2}, \overline{V_{n5}^2} = \frac{\overline{i_{nD5}^2}}{g_{m5}^2}, \overline{V_{n6}^2} = \frac{\overline{i_{nD6}^2}}{g_{m6}^2}, \overline{V_{n7}^2} = \frac{\overline{i_{nD7}^2}}{g_{m1}^2}, \tag{4-6}$$

$$\overline{V_n^2} = \overline{V_{n1}^2} + \overline{V_{n2}^2} + \overline{V_{n5}^2} + \overline{V_{n6}^2} + \overline{V_{n7}^2}, \tag{4-7}$$

$$\overline{V_n^2} = K\,\Delta f\left[\frac{8}{3}T\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}} + \frac{1}{g_{m5}} + \frac{1}{g_{m6}} + \frac{3}{2}\frac{1}{g_{m1}^2 R_{load}}\right) + \frac{1}{C_{ox}\cdot f}\left(\frac{1}{(wl)_1} + \frac{1}{(wl)_2} + \frac{1}{(wl)_5} + \frac{1}{(wl)_6}\right)\right] \tag{4-8}$$

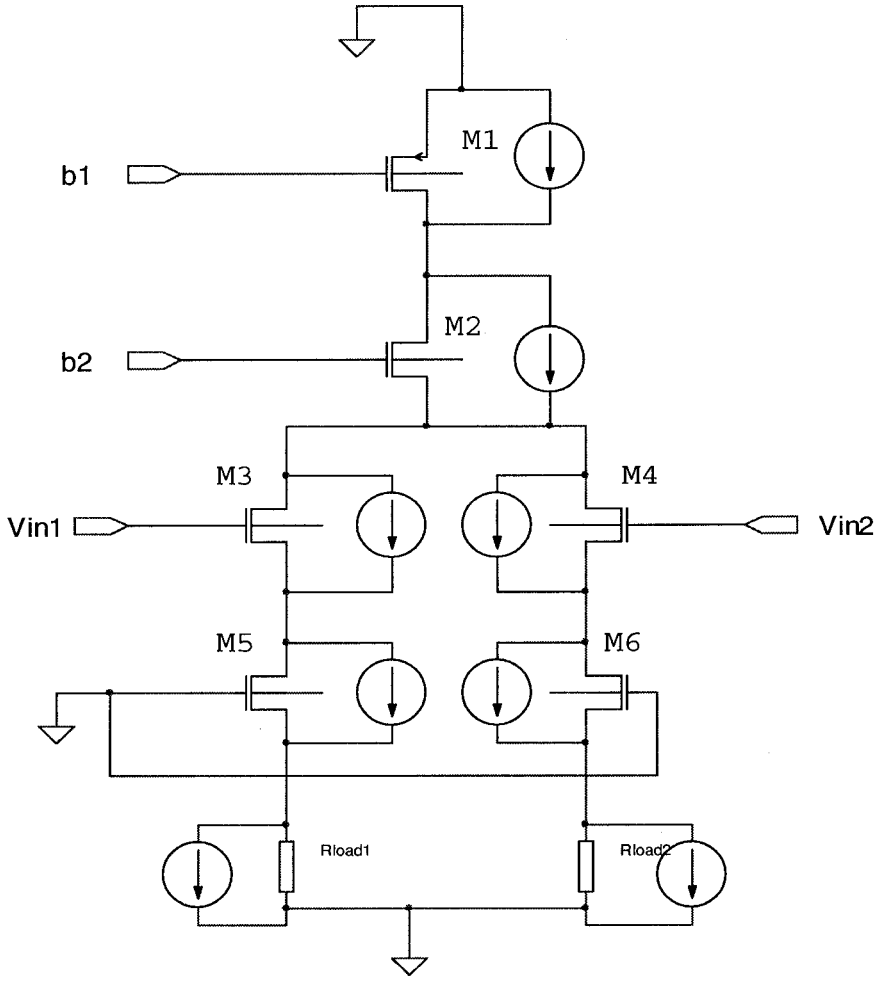


Figure 4-3: Current source circuit including noise sources

4.2 DNL and INL analysis

Random error is introduced by random mismatch difference that exists between any two current source transistors. Unlike that of INL specification, the random performance of the DNL specification depends on the segmentation level. The more current sources that switch at the same moment, the larger variation in transition occurs [25].

Fig. 4-4 shows the expected DNL values as a function of the resolution for this architecture. The DNL values are expressed as a linear function of the unity current source. The peak DNL is better than ± 0.15 LSB, while the peak-to-peak DNL is better than 0.17 LSB.

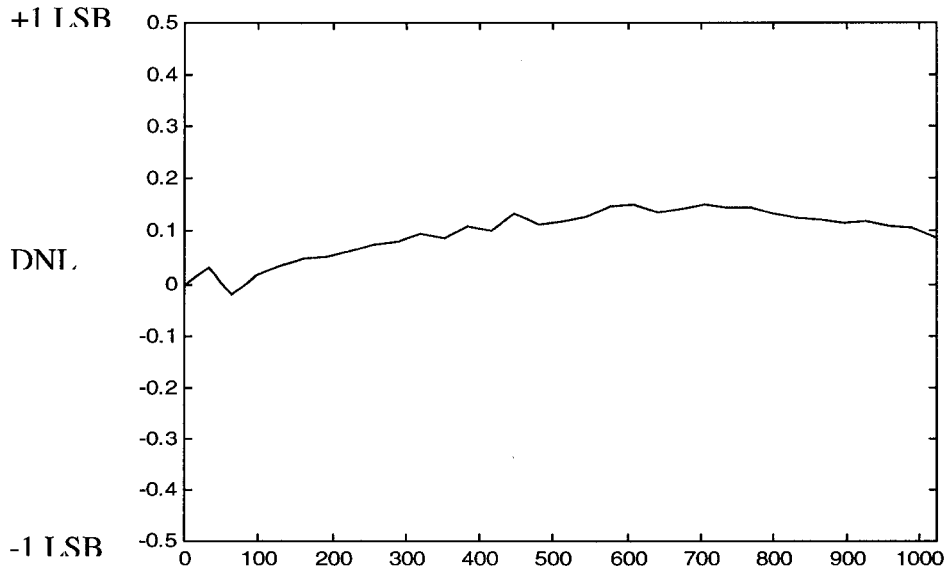


Figure 4-4: Measured DNL

An effective test method is used to sweep through the complete set of 2^{10} digital codes, and to gather and analyze the output data corresponding to each current source on the current source matrix. Repeated measurements are taken to eliminate calculation oversight that may have been induced by observation errors.

One can observe from Fig. 4-4 that the expected DNL performance for this architecture is almost independent of the number of bits and is always better than the required ½ LSB accuracy. Note the jump in DNL value at the middle of the diagram. This can be attributed to the nonlinearity of the Op-amp's gain in the corresponding digital input.

The DAC architecture presented here significantly reduces the amplitude of the INL errors. By implementing thermometer technique, a selected current source located inside the current matrix is turned on when the digital input increases one bit. This results in a very low linear error due to current source mismatch. Fig. 4-5 shows the variation of INL as a function of digital code sweep.

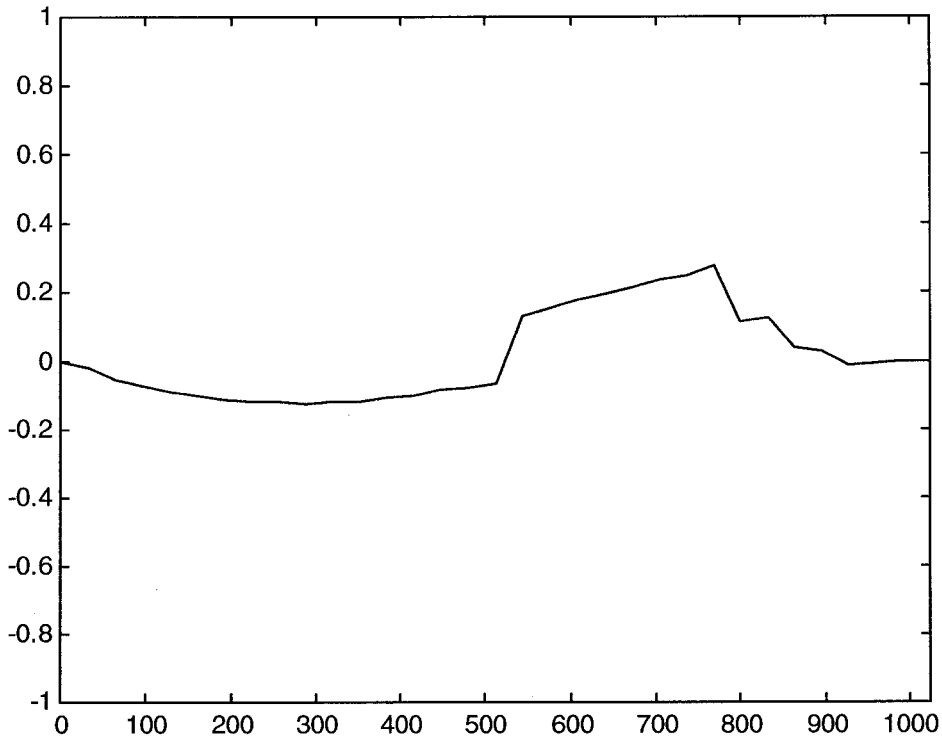


Figure 4-5: Measured INL

4.3 Layout Considerations

The 10-bit linearity requirement has strong influence on the layout of the chip. The chip has been implemented in $0.18\mu m$ CMOS process. The thermometer-code decoder was placed around the current source matrix. Each current source matrix cell includes current source-and-switches, latch and matrix switching decoder as shown in Fig. 4-6.

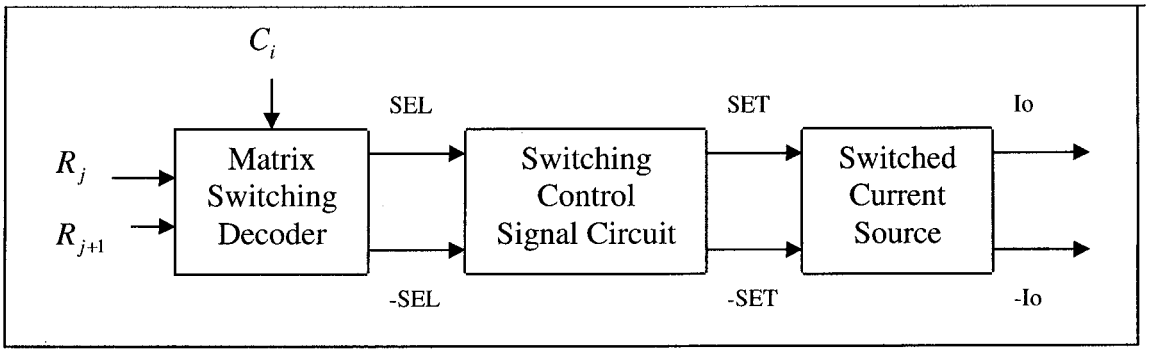


Figure 4-6: Current source matrix cell diagram

Four blocks of current source matrices are formed so that each one of them consists of 16×15 current source matrix cells. Separation of these blocks allows better placement and routing conditions for signal and power lines. The layout was made in six metal layers technology. The data converter is fabricated in a $0.18-\mu m$ CMOS process. Fig. 4-7 shows the layout of the chip, which shows the current source matrix, two-stage folded-cascade op-amp, and thermometers.

In mixed analog/digital design, disturbances from the digital to the analog part (or vice versa) spread along supply lines and the substrate. The substrate coupling may be strong. It is therefore necessary to do careful designs with proper shielding, which can be done in several different ways, i.e., guard rings, grounding, etc. The guard rings are typically implemented by N and P diffusion. These diffusions are connected to a quiet analog ground or common-mode voltage. It is important that the layout of the guard rings is symmetrical so that the shielding is equal for the analog components. As shown in Fig. 4-7, analog section has been ring-guarded.

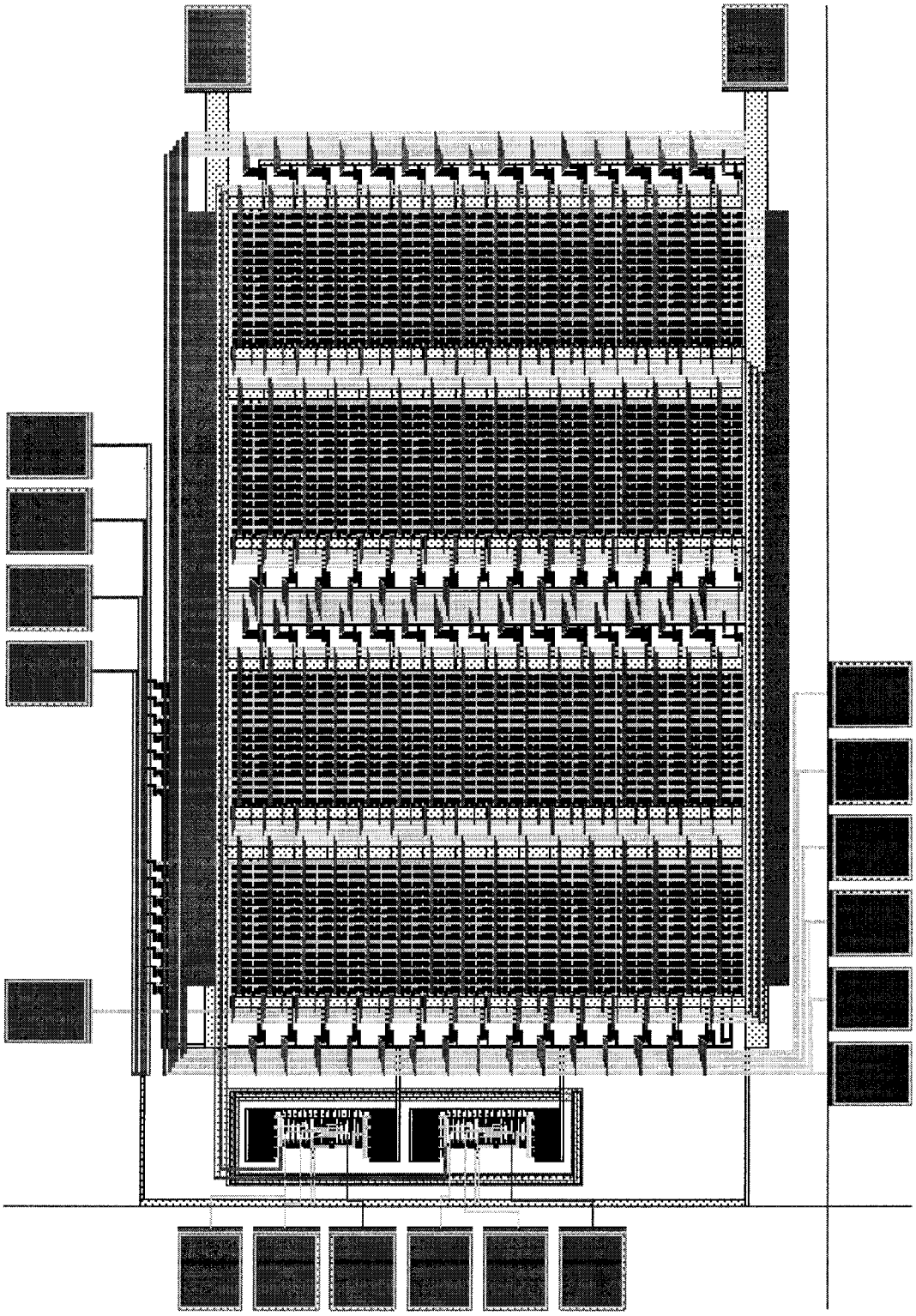


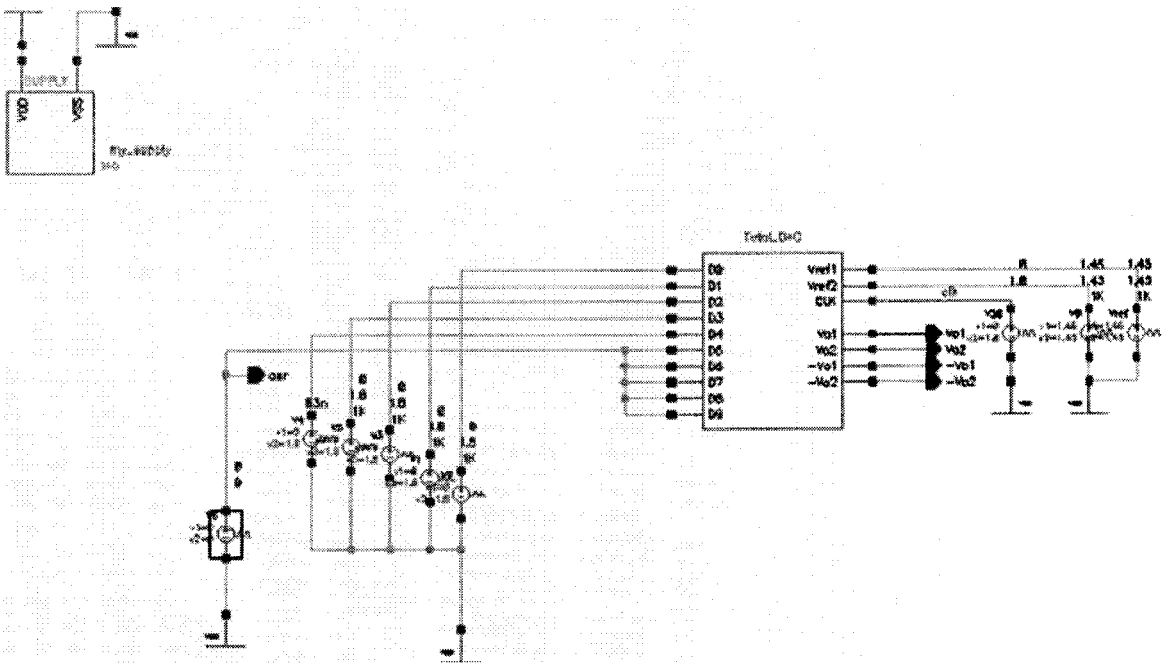
Figure 4-7: Layout of the proposed 10-bit DAC

4.4 Simulation Results

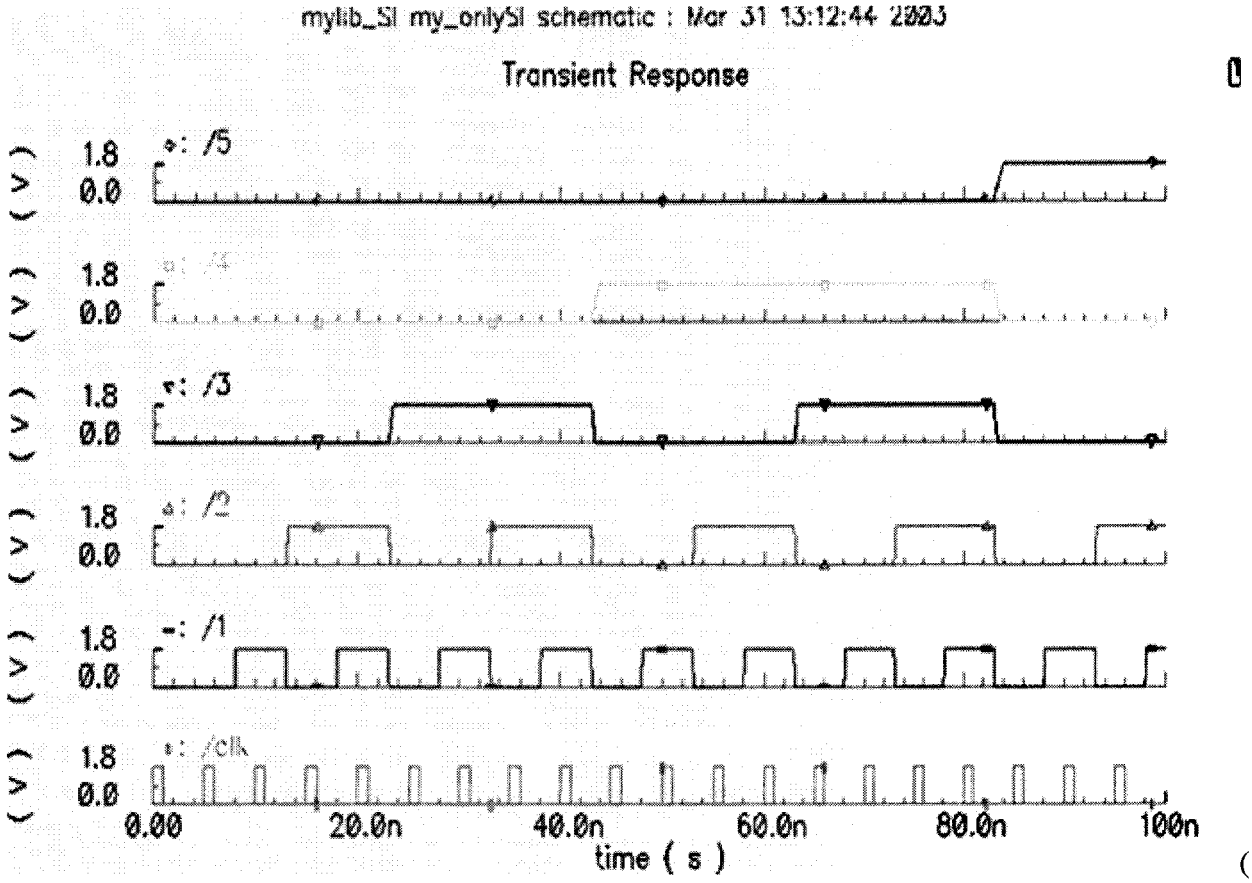
Naturally, there are several different ways of measuring the performance of the DACs. However, since we are measuring the outputs of high-speed and high-resolution converters, a suitable way is to use an input data generator (pattern generator) together with a low-jitter clock generator, a spectrum analyzer and a high-bandwidth oscilloscope. We measure the single-ended and/or differential outputs. Still a proper input signal has to be guaranteed to allow proper analysis of the output signal.

The output voltage of DAC is measured in two stages in order to reduce the simulation period. As shown in Fig 4-8 (a), five voltage sources provide a sequence of digital input for the five least significant bits. Fig. 4-8 (b) depicts the digital waveform entering to the DAC. The 200MHz pulse frequency is assigned to clock input in order to fully capture the settling time period.

Fig. 4-9 shows the plot of differential output of DAC for 200MHz clock input. Cadence simulation result shows that the low-to-high settling time is 4 ns. As shown in Fig. 4-8,9, the monotonicity requirement is entirely satisfied and glitch error is almost negligible. By assigning a certain digital input code to the most significant bits (MSB), then repeating the same test, we will observe the same result for LSB transient response as shown in Fig. 4-9. Increasing the op-amp voltage gain in order to increase the dynamic range will affect the linearity of DAC. That outlines the establishment trade off between linearity and op-amp dynamic range. The raise/settling time measured in Fig. 4-9 and Fig. 4-10 cannot represent the update frequency of DAC. The update frequency has to be measured when digital input is increased by only two levels, 0 and 10-bit full scale. This allows us to measure the update frequency in worst-case scenario. The load resistance is 100KOhm and the load capacitance is approximately 50pF.



(a)



(b)

Figure 4-8: DAC LSB measurement setup (a) test fixture (b) digital input waveforms

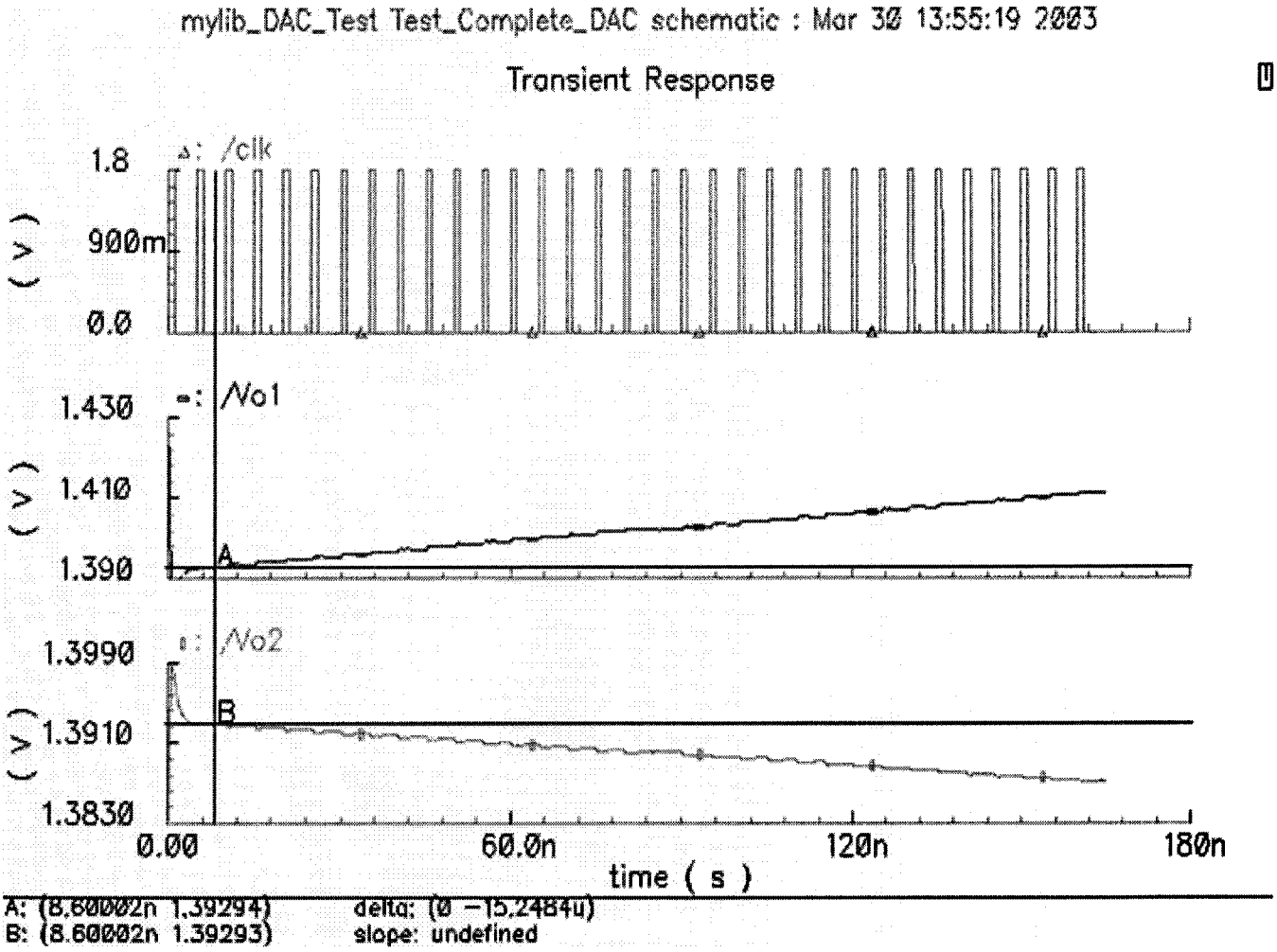


Figure 4-9: DAC differential outputs for LSB and clock waveforms

Fig. 4-10 shows the DAC differential output signals for consecutive code transitions with five most significant bits. The test runs in the similar way with 200MHz clock frequency using five pulse voltage sources to generate the digital input signals. Each output step voltage shown in Fig. 4-10 is $2^5 = 32$ LSB, which is limiting our test accuracy to measure INL and DNL for MSB, but good enough to evaluate glitch error.

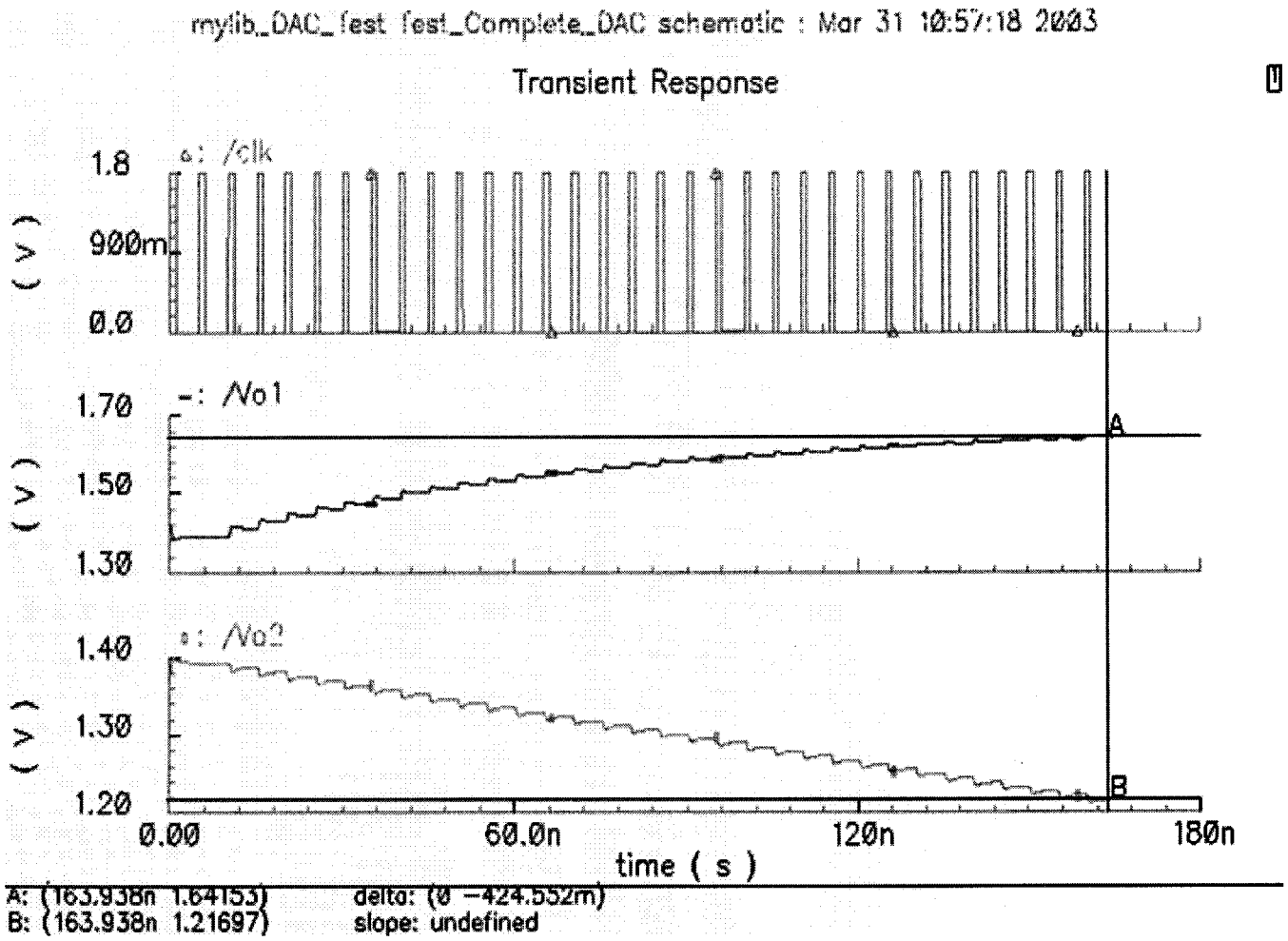
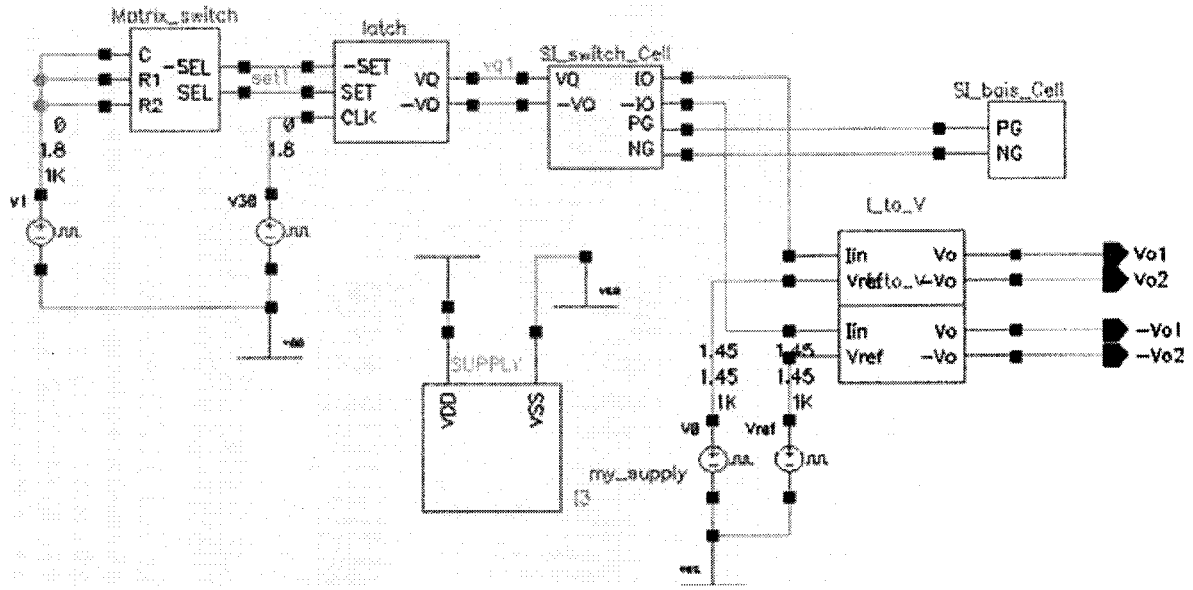
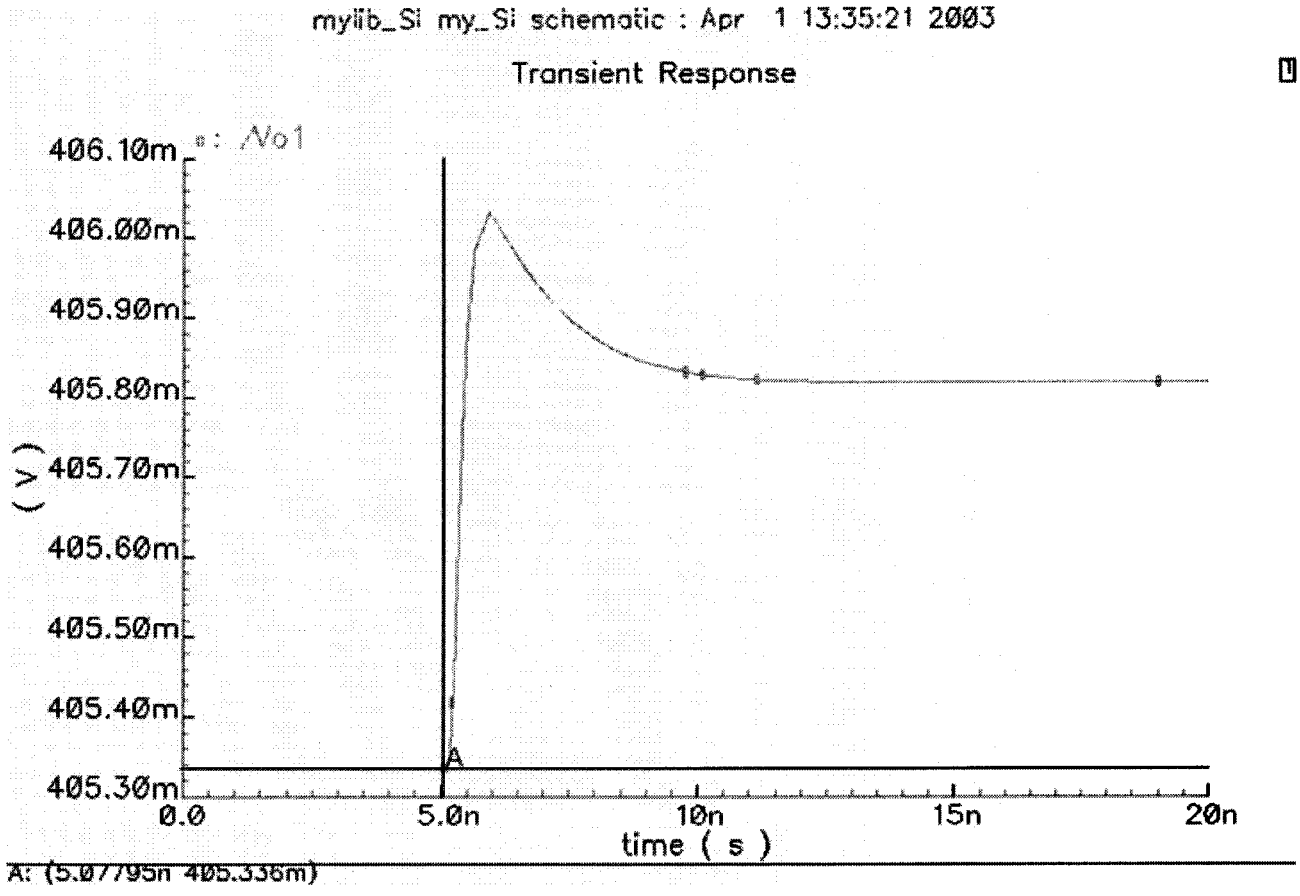


Figure 4-10: DAC differential outputs waveform for MSB

The test fixture set up in Fig. 4-11 (a) is very similar to full DAC test fixture in terms of input and output stages. The full-scale transient simulation plot of a single current source matrix cell is shown in Fig. 4-11 (b). It can be seen that rising/settling time is very close to what we had for the full DAC transient response. This concludes that the number of current source has no limiting effect on the update frequency rate. Op-amp and/or low-impedance followers as output buffer can play significant role in reducing the update frequency. As we observe from the plot, the settling time and raising time together is less than 5ns where clock frequency is set at 200MHz.



(a)



(b)

Figure 4-11: Proposed current matrix cell (a) schematic (b) transient response

Chapter 5

Conclusions

A novel DAC architecture presented is this work is the combination of double-segmented and thermometer-coded decoder. A 10-bit, 200MSamples/s update rate, double-segmented current steering DAC has been designed in $0.18-\mu m$ CMOS technology for use in graphic system applications. The segmented DAC architectures used in the proposed design, allows good matching strategies, reduced glitching, and easy calibration. A 4+6 segmented topology has allowed obtaining a very significant low DNL, INL, and glitch error. Four and six bit thermometer decoders are implemented as row and column decoder respectively. The thermometer code is used to increases the resolution without requiring large decoder size. Matrix Switching Decoder is a logic circuit used in the proposed design in order to combine two thermometer-coded decoder outputs and generate a single signal to turn on/off a current source.
A compact ratioed logic latch using only eight transistors is implemented in this design to generate the switching control signals. To improve synchronization, the latch is placed directly in front of the current switches. The intrinsic delay between the complementary latch outputs reduces the crossing-point voltage of the switching control signals, putting one switching transistor at the edge of turning on when the other is at the edge of turning off, reducing significantly glitches generated during code transitions.

A cascade current cell easily satisfied the necessary requirements, such as high-speed and simplicity for this design. A double cascade circuit is presented between output stage and current sources, thus forming isolation circuitry for each cell in current source matrix. The simplicity of current sources and switches in the proposed design, minimizes the size of chip and error effect on DAC.
The advantages of the differential implementation in a two stage operational amplifier are used to convert current from DAC to voltage. In this differential arrangement, the gain and linearity

are substantially improved over basic single-end amplifiers. A two stage Op-amp with a folded cascade input stage and NMOS cascade amplifier output stage was found optimal for high linearity with adequate voltage gain. The DAC is implemented in $0.18\,mm^2$ and operates from single 1.8-V power supply.

Although the Op-amp's slow settling time limited full speed operation of the DAC to 200-MHz, it's possible to reach higher speed by designing a low-voltage high-speed Op-amp with large dynamic range. Another future challenge for this design is to minimize the voltage fluctuation in the current output node. If the voltage variation in output node reduces, the current source can be designed somehow to drive more current through load resister. The larger transistors use in current source, the more linearity will achieve for the DAC.

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