A NOVEL PREDICTIVE CONTROL STRATEGY FOR NEUTRAL-POINT CLAMPED CONVERTER WITH HARMONIC SPECTRUM SHAPING

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A Novel Predictive Control Strategy for Neutral-Point Clamped Converter with Harmonic Spectrum Shaping

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Abstract

This thesis proposes a new predictive control strategy to achieve fixed-switching frequency operation for a neutral-point clamped (NPC) inverter. The classical fixed-sampling frequency finite control-set model predictive control (FSF-FCS-MPC) operates with variable switching frequency, and thus produces spread-spectrum in an output current. The classical method also suffers from high computational complexity as the number of converter voltage levels increases. To overcome these issues, a high performance variable sampling frequency finite control-set model predictive control (VSF-FCS-MPC) strategy is proposed to control the power converters.

The proposed control technique combines the advantages of space vector modulation (SVM) with a newly introduced mechanics to determine the appropriate sampling frequency. With these features the major requirements such as balancing of DC-link capacitor voltages, switching frequency minimization and common-mode voltage mitigation have been achieved with simultaneous elimination of even-order and inter-harmonics in the load current harmonic spectrum. The VSF-FCS-MPC strategy for current control with decoupled active/reactive power regulation of grid-connected multilevel converter was also analyzed.

Moreover, a novel DC-link voltage balancing technique is presented which eliminates the need for balancing the capacitor voltages through cost function, and thus alleviates the weighting factor design. An introduction of SVM highly reduces the calculation time by considering only

adjacent vectors, rendering FCS-MPC more suitable for implementation with multi-level converters with a number of voltage levels higher than three.

Finally, the proposed control technique has been validated through simulation and experimental verification and a detailed comparison of VSF-FCS-MPC with FSF-FCS-MPC and SVM is presented.

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CHAPTER 1
INTRODUCTION

1.1 Introduction

The field of high-power converters has been one of the most active areas in research and development of power electronics in the last few decades. Several industrial processes have increased their power-level needs, driven mainly by economies of scale (production levels and efficiency), triggering the development of new power semiconductors, converter topologies, and control methods. The development of high-power converters started in the mid- 1980s when 4500-V gate-turn-off (GTO) thyristors became commercially available. The GTO was the standard for high power applications until the advent of insulated-gate bipolar transistors (IGBTs) and gate-commutated thyristors (GCTs) in the late 1990s [1], [2]. These switching devices are now extensively used in high-power converters and drives due to their superior switching characteristics, reduced power losses, ease of gate control, and snubberless operation. High-power converters have found widespread applications in industry. They can be used for pipeline pumps in the petrochemical industry or water pumping stations, fans in the cement industry, traction applications in the transportation industry, steel rolling mills in the metals industry, grid integration of renewable-energy sources, reactive-power compensation, and other applications.

The most important requirements for these converters are: high efficiency, overload capability, high reliability and operation in harsh environments. The converters can be generally classified into a few significant families: Cycloconverters (CCV), Current Source Converters (CSC) and Voltage Source Converters (VSC). All of these families have shown important advances in design, performance and control strategies. The VSI converts the DC voltage to a three-phase AC voltage with adjustable magnitude and frequency whereas the CSC converts the DC current to an adjustable three-phase AC current. Mostly used topologies in the industry include three-phase VSI topologies, consisting of a conventional two-level converter, a three-level and four-level neutral-point clamped converter, a seven-level cascaded H-bridge converter and a four-level flying-capacitor converter [3-11]. Either IGBT or GCT can operate in these converters as a switching device.

The control of power converters is one of the most elaborate fields in power electronics due to its pivotal importance for proper operation of converters. Properly designed control mechanisms may increase reliability, efficiency and the overall robustness of an entire system. More often, various issues in the operation of power converters can be solved through judicious control optimization rather than using more complex and expensive hardware solutions. The control of power converters is a topic undergoing intense study and is constantly evolving according to technological developments in power quality standards, control requirements, grid code requirements, semiconductor devices, control platforms, etc.

During the 1960s, analog control platforms based on operational amplifiers and passive components were developed to control the firing angles of thyristors in order for an output voltage to be controlled [12]. A few years later, fully controllable device named IGBT has been developed [3], improving power converters and requesting more complex control systems. The converters in the past used analog control circuits, where a single-phase pulse width modulator or hysteresis controller generates the gating signals. Analog control platforms present several drawbacks such as a large number of components, reduced system reliability and poor computational capability to name a few [13]. To achieve high performance operation, digital control techniques were developed during the 1970s which involved powerful calculations, complex strategies and math-intensive algorithms. Introduction of digital signal processors (DSPs) has created the basis for the implementation of digital control techniques. The digital control platforms evolved rapidly and revolutionized the industrial control area by allowing the user to develop sophisticated control algorithms. A few examples of modern real-time (RT) digital control platforms include: microcontrollers, DSP, and field programmable gate array (FPGA). These platforms have been used widely in the control of various power electronic converters and they feature low cost, more reliability and high computational power [13-19].

Highly exploited and very well studied control techniques include the hysteresis and linear controllers. Over the years they have become widely accepted by the power electronics industry. More recent and advanced control techniques include sliding-mode, intelligent and predictive control techniques. The predictive control uses the system model to predict the future responses of a plant. These predictions are then used to generate the optimal control action. This control philosophy emerged during the 1970s for the process control which are normally very slow in nature. The application of predictive control in power electronics is a rather recent topic due to the

fast processing time required to control the electric variables. With the evolution in DSPs, a wide range of predictive controllers have been developed which includes deadbeat and hysteresis-based predictive control, trajectory-based predictive control, and model-based predictive control.

1.2 Converter Topologies

The design of power converters is faced with a number of challenges that relate to topologies and control as well as power semiconductor switching devices. One of the major requirements is to produce high quality waveforms and this is particularly important in a grid connected operation to reduce the device switching impact. In inverters and rectifiers, the waveforms are affected by the following factors: 1) the topology used; 2) the application; 3) the control algorithm; 4) the size of the filter; and 5) the choice of switching frequency [3, 20, 21]. Based on a method of achieving variable output in terms of magnitude and frequency the high-power converters can be classified into two main categories: direct AC–AC converters and indirect AC-DC-AC converters. The latter group introduces a link between two converters which can be of voltage or current nature. Both groups with their representatives have certain advantages and disadvantages, which should be taken into account when selecting the topology for a given application. The general classification of high power converters is provided in Figure 1.

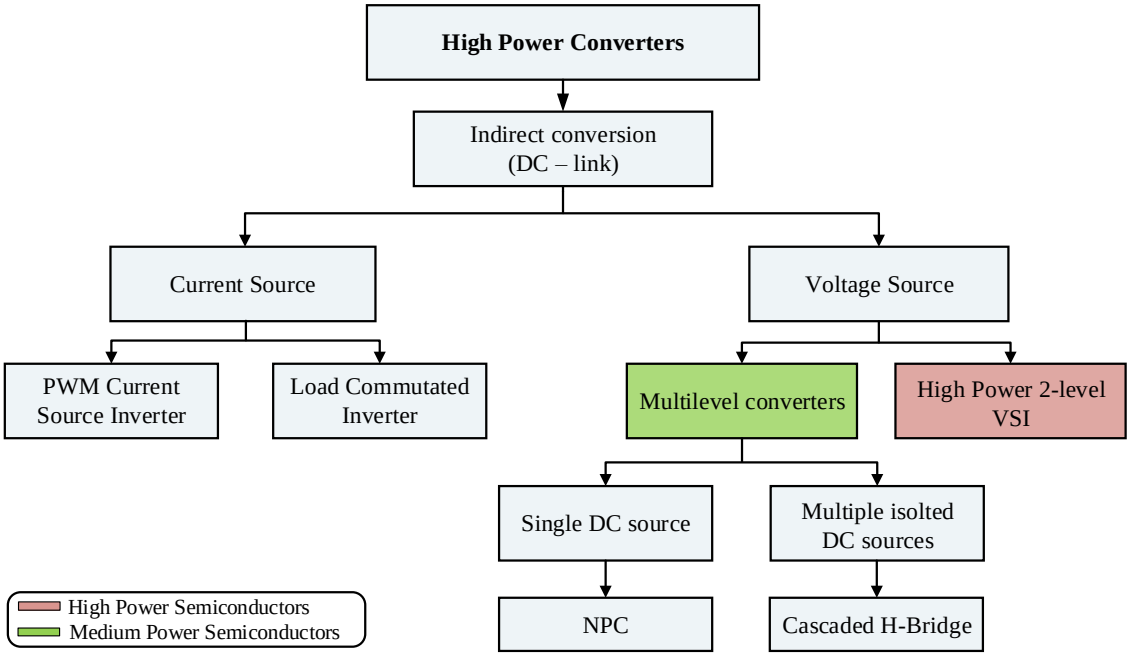


Figure 1 - High power converter classification

At low voltage, a single topology that still dominates the market is the voltage-source two-level converter. However, at medium and high voltages the situation is completely different. Multilevel converter technology started with the introduction of the multilevel stepped waveform concept with a series-connected H-bridge, which is also known as cascaded H-Bridge converter, in the late 1960s [22]. This was closely followed by low-power development of an FC topology the same year [23]. Finally, in the late 1970s, the diode-clamped converter (DCC) [24] was first introduced. The DCC concept evolved into the three-level NPC (3L-NPC) converter we know today as it was proposed in [8, 25] and can be considered as the first real multilevel power converter for medium-voltage applications.

Multi-level converters provide a wide range of advantages over two-level topology such as better waveform quality, lower *dv/dt* operation, reduced switch stress levels and many more. They are finding increased attention in industry and academia as one of the preferred choices of electronic power conversion for high-power applications. They have successfully made their way into the industry and therefore can be considered a mature and proven technology. Although it is an enabling and already proven technology, multilevel converters present a great deal of challenges, and even more importantly, they offer such a wide range of possibilities that their research and development is still growing in depth and width. Researchers all over the world are contributing to further improve energy efficiency, reliability, power density, simplicity, and cost of multilevel converters, and broaden their application field as they become more attractive and competitive than classic topologies.

1.2.1 Two-Level Voltage Source Converter

The primary function of a voltage source converter is to convert a fixed DC voltage to a three-phase AC voltage with variable magnitude and frequency. The two-level VSI is the main building block for AC-DC and AC-DC-AC converter systems for low- and medium-power applications. The two-level topology presented in Figure 2 is one of the most commonly used topologies in the industry.

The converter is composed of an array of six switching devices, typically IGBTs and a capacitor as a DC-link. The presence of these active switches along with a proper control scheme, allows the generation of sinusoidal currents at the input side, a fully adjustable power factor and a bidirectional power flow. Both carrier based pulse-width modulation (PWM) and space vector

modulation can be applied to generate the switching patterns for the 2L-VSC [3]. In addition, variable switching frequency methods as table or prediction based methods can also be used [12].

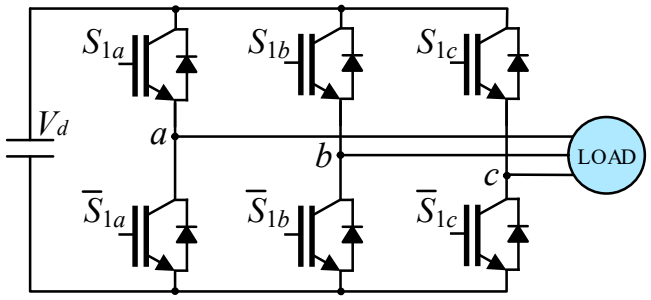


Figure 2 – Two-level voltage source converter

As its name suggests this converter generates a binary pulse train, alternating between 0 and V_d, while the line-to-line voltage presents a three-level waveform. This impacts the total harmonic distortion (THD) of the input current, as larger active/passive filters or higher switching frequencies are needed in order to meet the limits imposed by the grid code. Even though the main features of this converter are its simplicity, modularity and low number of power components, they suffer from unwanted traits such as high *dv/dt*, static and dynamic voltage sharing and common-mode voltage (CMV). Some of these problems are solved with the invention of multilevel topologies. However, these topologies require a higher number of power devices, which increases the complexity of the design.

Multilevel Voltage Source Converters

Another option for a VSI system to accommodate the voltage requirements of a high-power application is to utilize a multilevel voltage synthesis strategy. Conceptually, the multilevel VSC configurations can be divided into:

- Diode-clamped multilevel VSC,
- H-bridge-based multilevel VSC,
- Capacitor-clamped multilevel VSC.

1.2.2 Three-Level NPC VSC

These types of converters employing clamping diodes and cascaded DC capacitors to produce AC voltage waveforms with multiple levels can be generally configured as a three-, four-,

or five-level topology, but only the three-level converter, often known as the neutral-point clamped converter has found a wide application in high-power medium-voltage drives [7,8]. The schematic of the NPC converter is presented in Figure 3.

Compared to a two-level converter with a direct series connection of devices the NPC VSC features two additional diodes per phase leg. These diodes link the midpoint of the "indirect series connection" of the main switches to the neutral point of the converter. This allows the connection of the phase output to the converter neutral point and enables the three-level characteristic of the topology. There are 27 switch states, whereas the two-level converter allows eight switch states not comprising a "0" state. Hence, the clearly superior output voltage quality is the most distinct advantage over the two-level converter. The three-level converter compared to a two-level VSC of the same rating can achieve reduced *dv*/*dt* and THD in its AC output voltages, lower switching losses, reduced switch stress levels and it does not have dynamic voltage sharing problem.

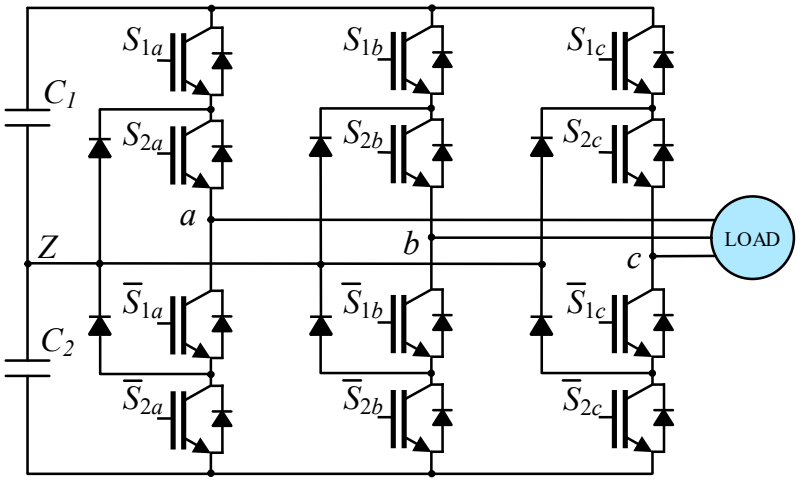


Figure 3 - Three-level neutral-point clamped voltage source converter

One main technical requirement for proper operation of the NPC converter is to maintain the voltages of its DC-bus capacitors at their prescribed (usually equal) levels and to prevent voltage drifts during the steady-state and dynamic regimes. Conceptually, there are two approaches to deal with the DC capacitor voltage drift phenomenon. The first approach is to utilize an auxiliary power circuitry. The auxiliary circuitry can be a set of independent power supplies for capacitors, or it can be a dedicated electronic converter that injects current into the capacitors and regulates their voltages. The approach is, however, not appealing for power systems applications due to its cost and complexity. The second approach to equalize the voltages of the DC-side capacitors of a NPC

converter is to enhance the converter control strategy and, to modify the switching patterns of the switches such that the capacitor voltages are regulated at their corresponding desired values. Another drawback of this topology is an increased number of components and complicated PWM switching pattern.

1.2.3 Four-Level Diode Clamped VSC

Four-Level NPC converter is an extension of the three-level NPC converter which means it carries similar features. The number of components is increased to 6 switches and 6 diodes per leg. The clamping diodes withstand different reverse voltages and thus a series connection of two diodes is necessary.

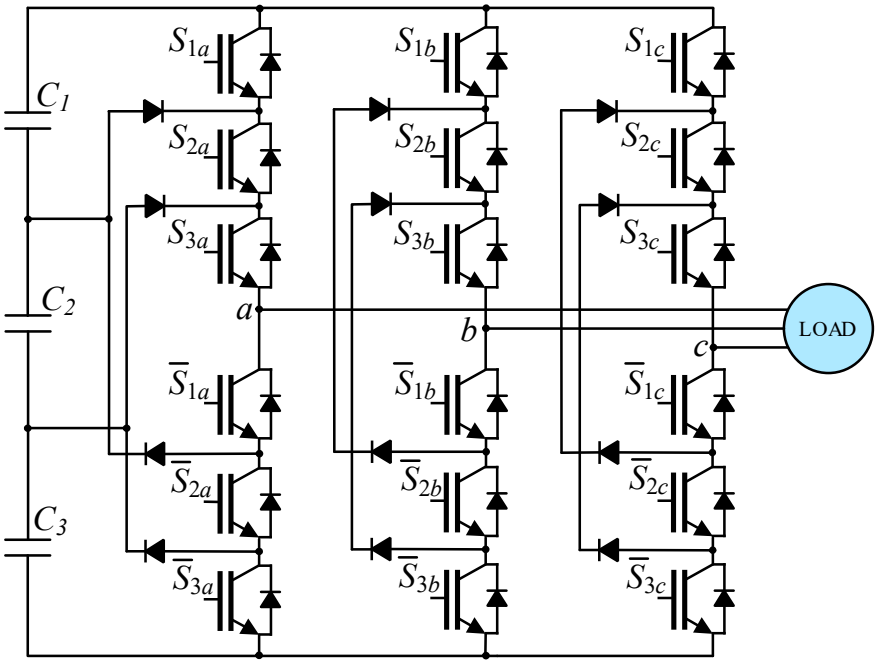


Figure 4 – Four-level voltage source converter

The DC-link voltage is divided between 3 capacitors connected in series forming two neutral point voltages that need to be balanced. The balancing techniques are similar to those used with the 3-level converter. The converter is presented in Figure 4. In the topology, only three switches conduct at any time and the switch pairs $(S_{1X},\overline{S_{1X}})$, $(S_{1X},\overline{S_{1X}})$, $(S_{1X},\overline{S_{1X}})$ operate in a complementary manner. A total of 37 voltage vectors with 64 switching combinations are available for the converter. The main advantage of this converter is an increased switching frequency, which leads to a better power

quality or grid code compliance in case of grid connection. The converter can also be operated at higher voltage levels without connecting the switching devices in series.

A brief summary of the number of power components required in most common multilevel topologies versus the 2-level VSC is presented in Table I.

Table I – Comparison of required power components

	2L-VSC	**3L-NPC VSC**	**3L-FLC VSC**	**4L-FLC VSC**	**5L-CHB VSC**
Number of IGBTs	6 x 6.5 kV	12 x 3.3 kV	12 x 3.3 kV	18 x 2.5 kV	24 x 1.7 kV
Number of diodes	6	18	12	18	24
Number of flying capacitors	-	-	3	6	-
Number of LC filter capacitors / inductors	-	3/3	3/3	3/3	3/3
Total component count	23	36	33	48	54

1.2.4 AFE NPC Rectifier

Rectifiers are by far the most widely used converters in power electronics. The transformation from alternating current to direct current performed by rectifiers is used in a large variety of applications (from small power up to several megawatts). There are three distinct types of rectifiers, the first of which is the diode rectifier. The main advantages of the diode rectifier are its simplicity and extremely low cost.

The disadvantages and limitations of the three-phase diode rectifier are that:

- it does not offer the possibility to control the power flow,
- it generates high harmonics at the input current, especially when it supplies a capacitive load,
- it does not allow regeneration of power.

The second topology of importance is the thyristor rectifier which introduces the possibility of control of power flow by changing the angle of the gate pulses α for the thyristors. Through angle α control, it is possible to change the mean value of the load voltage, regulating the control of power delivered to the load. Thyristor rectifiers have in general the same advantages and limitations as the diode rectifiers. An additional negative feature is that an increase in the value of α increases the phase

displacement of the input current with respect to the source AC voltage, increasing the amount of fundamental reactive power. An advantage of thyristor rectifiers is that, in operating with $\alpha > 90$, they can regenerate power from the DC load to the power supply.

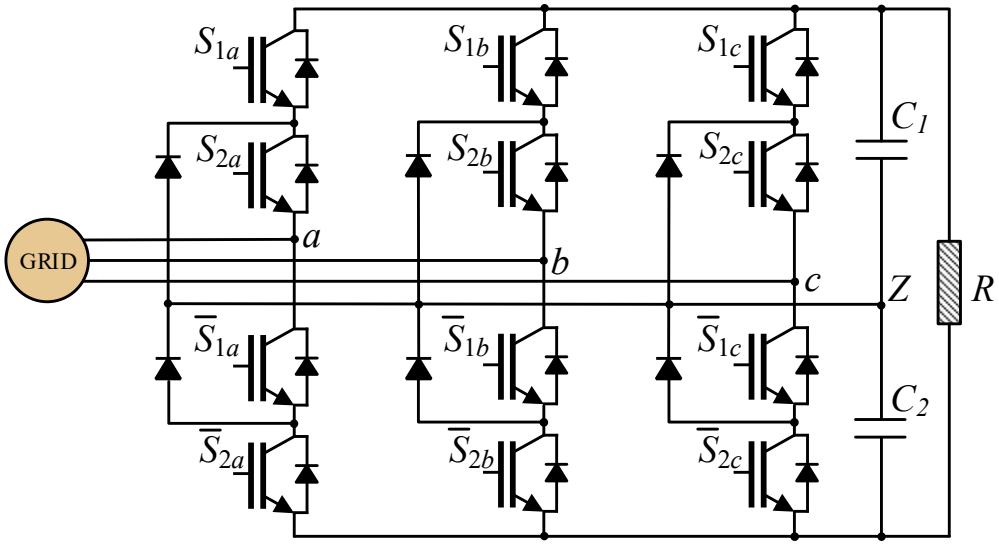


Figure 5 - NPC AFE rectifier

The third important rectifier topology includes power transistors with antiparallel diodes as the main power switches. This rectifier operates with high switching frequency and is also known as an active front-end (AFE) rectifier. A three-level NPC AFE rectifier is presented in Figure 5. It carries all the same features as the NPC converter, as it shares the 3-level topology, except for the power flow which is inverse. The AFE rectifier overcomes all the problems and limitations of the diode and thyristor rectifiers. Its main features are:

1. Controlled DC voltage.
2. Controlled input currents with sinusoidal waveform (reduced harmonics).
3. Operation with high power factor.
4. Full regenerative operation.

1.3 Current Control Methods for the Converters

One of the most studied topics in power converters control is a current control, for which there are two classical control methods that have been extensively studied over the last few decades: namely, linear control using pulse width modulation and hysteresis control [21, 26, 27].

1.3.1 Linear Control with PWM or SVM

Considering a modulator stage for the generation of control signals for the power switches of the converter allows one to linearize the nonlinear converter. In this way, any linear controller can be used. The most common choice being used is the proportional–integral (PI) controller.

1.3.1.1 Pulse Width Modulation

In a pulse width modulator, the reference voltage is compared to a triangular carrier signal and the output of the comparator is used to drive the inverter switches. A sinusoidal reference voltage is compared to the triangular carrier signal generating a pulsed voltage waveform at the output of the inverter. The fundamental component of this voltage is proportional to the reference voltage. In a three-phase inverter, the reference voltage of each phase is compared to the triangular waveform, generating the switching states for each corresponding inverter leg, as in Figure 6.

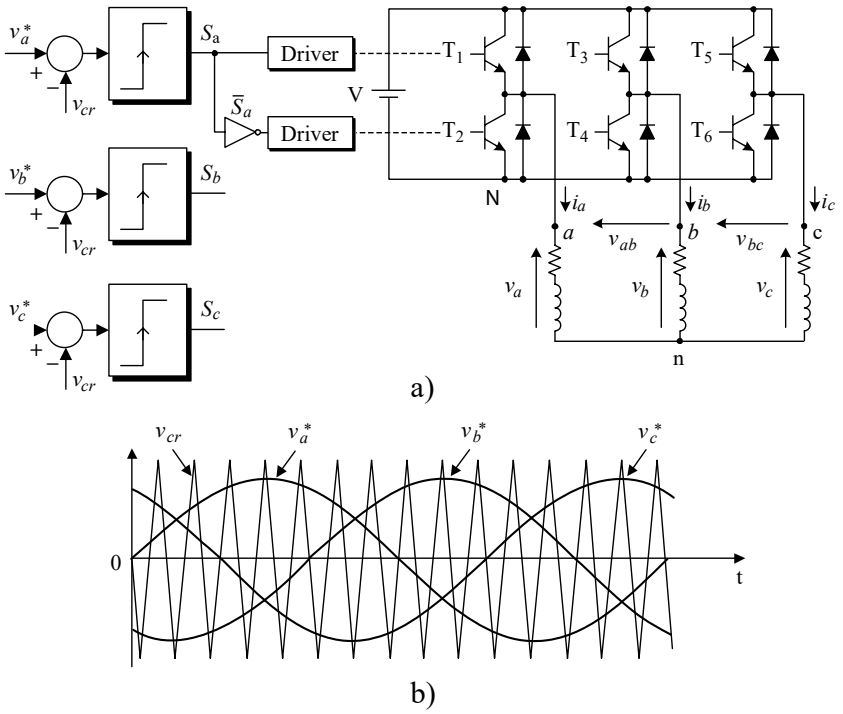


Figure 6 – Pulse width modulator for a three-phase inverter

1.3.1.2 Linear Control with Space Vector Modulation

A variation of PWM is called space vector modulation, in which the application times of the voltage vectors of the converter are calculated from the reference vector. It is based on the vector representation of the three-phase voltages, defined as

$$\mathbf{v} = \frac{2}{3}(v_{aN} + \mathbf{a}v_{bN} + \mathbf{a}^2 v_{cN}) \quad (1)$$

where v_{aN}, v_{bN} and v_{cN} are the phase-to-neutral voltages of the inverter and $\mathbf{a} = e^{j2\pi/3}$. The output voltages of the inverter depend on the switching state of each phase and the DC-link voltage, $v_{xN} = S_x V_{dc}$, with $x = \{a, b, c\}$. Then, taking into account the combinations of the switching states of each phase, the three-phase inverter generates the voltage vectors listed in Table II.

Table II - Switching states and voltage vectors

S_a	S_b	S_c	Voltage vector **V**
0	0	0	$\mathbf{V}_0 = 0$
1	0	0	$\mathbf{V}_1 = \frac{2}{3} V_{dc}$
1	1	0	$\mathbf{V}_2 = \frac{1}{3} V_{dc} + j\frac{\sqrt{3}}{3} V_{dc}$
0	1	0	$\mathbf{V}_3 = -\frac{1}{3} V_{dc} + j\frac{\sqrt{3}}{3} V_{dc}$
0	1	1	$\mathbf{V}_4 = -\frac{2}{3} V_{dc}$
0	0	1	$\mathbf{V}_5 = -\frac{1}{3} V_{dc} - j\frac{\sqrt{3}}{3} V_{dc}$
1	0	1	$\mathbf{V}_6 = \frac{1}{3} V_{dc} - j\frac{\sqrt{3}}{3} V_{dc}$
1	1	1	$\mathbf{V}_7 = 0$

Considering the voltage vectors generated by the inverter, the $\alpha - \beta$ plane is divided into six sectors, as shown in Figure 7(a). In this way, a given reference voltage vector $\mathbf{v}^*$, located at a generic sector k (Figure 7b), can be synthesized using the adjacent vectors $\mathbf{V}_k$, $\mathbf{V}_{k+1}$ and $\mathbf{V}_0$, applied during t_k, t_{k+1} and t_0, respectively. This can be summarized with the following equations:

$$\mathbf{v}^* = \frac{1}{T}(\mathbf{V}_k T_k + \mathbf{V}_{k+1} T_{k+1} + \mathbf{V}_0 T_0) \quad (2)$$

$$T = t_k + t_{k+1} + t_0 \quad (3)$$

where T is the carrier period and t_k/T, t_{k+1}/T and t_0/T are the duty cycles of their respective vectors. Using trigonometric relations the application time for each vector can be calculated, resulting in

$$t_k = \frac{3T|\boldsymbol{v}^*|}{2V_{dc}}\left(\cos(\theta - \theta_k) - \frac{\sin(\theta - \theta_k)}{\sqrt{3}}\right) \quad (4)$$

$$t_{k+1} = \frac{3T|\boldsymbol{v}^*|}{V_{dc}} \frac{\sin(\theta - \theta_k)}{\sqrt{3}} \tag{5}$$

$$t_0 = T - t_k - t_{k+1} \tag{6}$$

where θ is the angle of the reference vector $\mathbf{v}^*$and θ_k is the angle of vector $\mathbf{V}_k$.

A classical current control scheme using SVM is shown in Figure 8. Here, the error between the reference and the measured load current is processed by a PI controller to generate the reference load voltages.

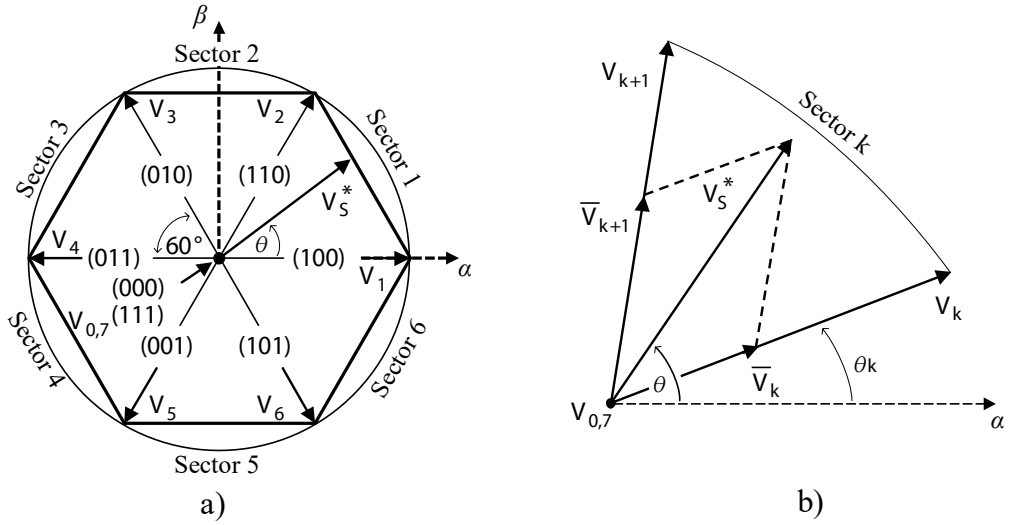


Figure 7 – Principles of space vector modulation. (a) Voltage vectors and sector definition, (b) Generation of the reference vector in a generic sector

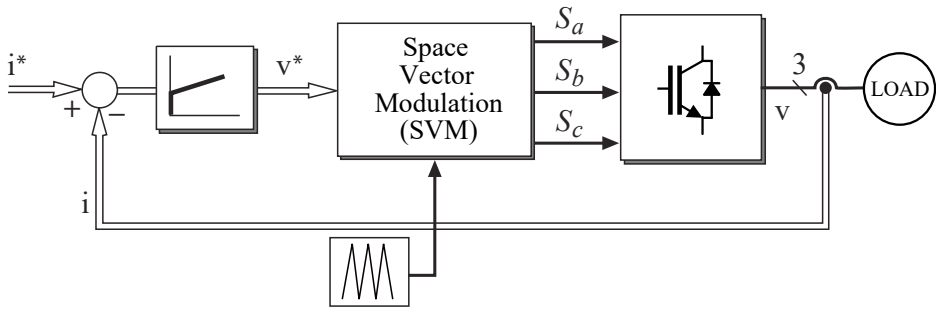


Figure 8 – Classical control scheme using SVM

With this method, constant switching frequency, fixed by the carrier, is obtained. The performance of this control scheme depends on the design of the controller parameters and on the frequency of the reference current.

Although the PI controller assures zero steady state error for continuous reference, it can present a noticeable error for sinusoidal references. This error increases with the frequency of the

reference current and may become unacceptable for certain applications [27]. To overcome the problem of the PI controller with sinusoidal references, the standard solution is to modify the original scheme considering a coordinate transformation to a rotating reference frame in which the reference currents are constant values.

1.3.2 Hysteresis Current Control

The basic idea of hysteresis current control is to keep the current inside the hysteresis band by changing the switching state of the converter each time the current reaches the boundary. Figure 9(a) shows the hysteresis control scheme for a three-phase inverter.

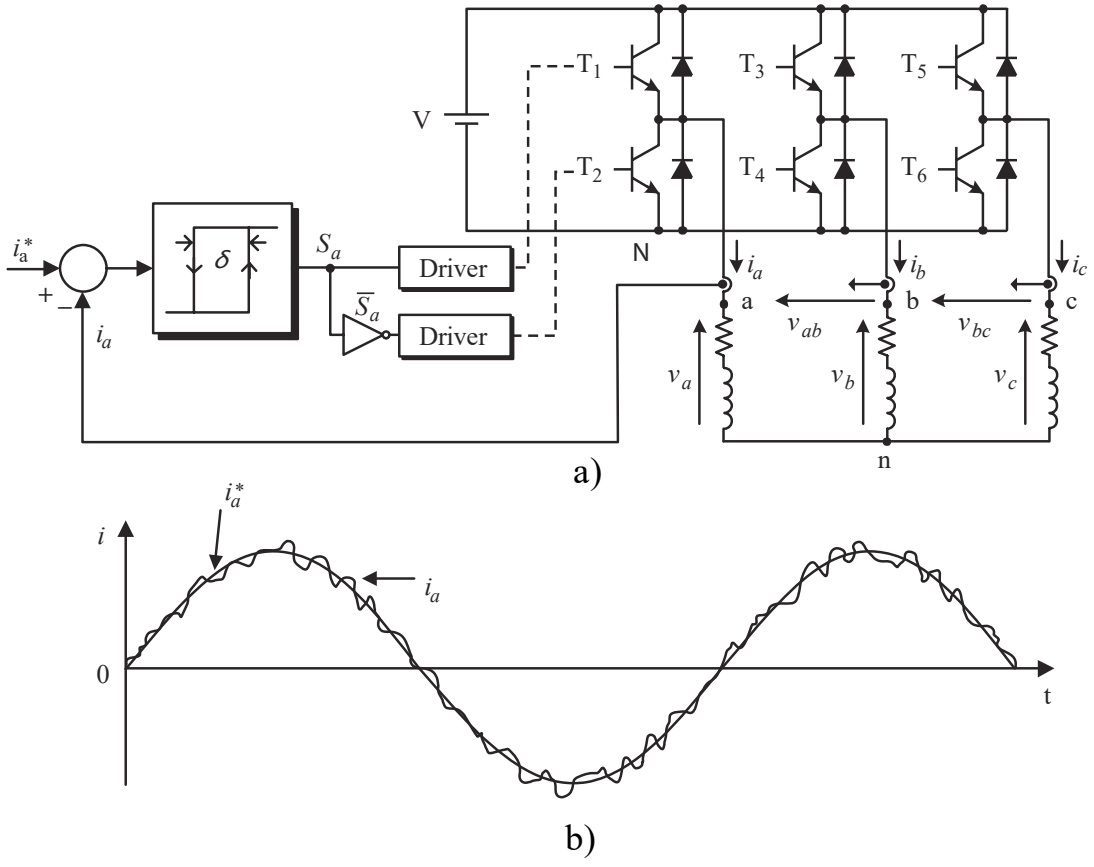


Figure 9 – Hysteresis current control for a three-phase inverter

Here, the current error is used as the input of the comparator and if the current error is higher than the upper limit *δ/2*, the power switch T_1 is turned on and T_2 is turned off. The opposite switching states are generated if the error is lower than *-δ/2*. It can be observed in Figure 9(b) that with this simple strategy the load current i_L follows the waveform of the reference current i_L^* very well, which in this case is sinusoidal.

For a three-phase inverter, measured load currents of each phase are compared to the corresponding references using hysteresis comparators. Each comparator determines the switching state of the respective inverter leg (S_a, S_b and S_c) such that the load currents are forced to remain within the hysteresis band. Due to the interaction between the phases, the current error is not strictly limited to the value of the hysteresis band.

This method is conceptually simple and the implementation does not require complex circuits or processors. The performance of the hysteresis controller is good, with a fast dynamic response. The switching frequency changes according to variations in the hysteresis width, load parameters, and operating conditions. This is one of the major drawbacks of hysteresis control, since variable switching frequency can cause resonance problems. In addition, the switching losses restrict the application of hysteresis control to lower power levels [27]. Several modifications have been proposed in order to control the switching frequency of the hysteresis controller. When implemented in a digital control platform, a very high sampling frequency is required in order to keep the controlled variables within the hysteresis band all the time.

1.4 Control Requirements

Traditionally, control requirements were mainly associated with the dynamic performance and stability of the system. Currently, industry requires more demanding technical specifications and constraints, and in many cases it is subject to regulations and codes. Many of these requirements enforce operating limits and conditions that cannot be dealt with by the hardware only, but also need to be addressed by the control system. This shift in trend has driven the development of more advanced control methods. The design of an industrial power electronic systems can be seen as an optimization problem where several objectives must be fulfilled at the same time. Among these requirements, constraints, and control challenges, the following are especially important:

- provide the smallest possible error in the controlled variables, with fast dynamics for reference following and disturbance rejection;
- operate the power switches in such a way that switching losses are minimized. This requirement leads to increased efficiency and better utilization of the semiconductor devices;

- power converters are switched systems that inherently generate harmonic content. Usually this harmonic content is measured as THD. Many power converter systems have limitations and restrictions on the harmonic content introduced by the modulation stage. These limits are usually specified in standards that can change from one country to another;
- the electromagnetic compatibility (EMC) of the system must be considered, according to defined standards and regulations;
- in many systems, common-mode voltages must be minimized due to the harmful effects that they can produce. These voltages induce leakage currents that reduce the safety and lifetime of some systems;
- good performance for a wide range of operating conditions. Due to the nonlinear nature of power converters, this is difficult to achieve when the controller has been adjusted for a single operating point of the linearized system model;
- some converter topologies have their own inherent restrictions and constraints such as forbidden switching states, voltage balance issues, power unbalances, mitigation of resonances, and many other specific requirements.

1.5 Motivation for the Research

Considering the trends in control of power converters it can be seen that predictive control is making a significant impact in research field as well as in the market. Among predictive techniques, deadbeat control and MPC stand out due to their good properties. An implementation of MPC for power converters can be difficult due to the large number of calculations. A solution is found in FCS-MPC, which takes into account only the finite number of possible switching states, and can be easily implemented using standard control hardware. The FCS-MPC has so far been successfully implemented on various converters and rectifiers, uninterruptible power supplies, active filters and motor control. Some of the dominant features of FCS-MPC, such as simple and convenient algorithm for digital implementation, absence of linear controllers and the ability to easily include different control objectives make its research potential constantly growing. Despite of this good features, the FCS-MPC has two main drawbacks which make its application in industrial power converters difficult. The FCS-MPC needs a high sampling frequency to achieve high performance and, a large number of calculations required for high-level converters combined with an extended prediction horizon could make implementation impossible. Another significant issue of FCS-MPC is a non-

constant switching frequency producing widespread spectrum frequencies of generated currents and voltages. This fact leads to necessity for large passive filters, increasing the weight, volume and cost of power converters.

This thesis aims to investigate and solve some of the current issues associated with FCS-MPC. Variable sampling frequency model predictive control has been proposed to achieve spectrum-shaping for the NPC converter. The proposed control technique simultaneously considers load current control, balancing of DC-link capacitor voltages, mitigation of common-mode voltage, elimination of even-order and inter-harmonics in the load current harmonic spectrum, and fixed-switching frequency operation. The challenges associated with weighting factor design are also addressed. Through simulation and experimental verification on a low-power NPC converter, it has been demonstrated that the proposed method preserves high dynamic performance nature of MPC, and predefined harmonic spectrum characteristic of space vector modulation.

1.6 Organization of the Thesis

The thesis is divided into five chapters. Chapter 1 provides a brief introduction to power converter topologies and most established control techniques in industry. This section also provides the motivation for the research in field of model predictive control. Chapter 2 presents detailed analysis of MPC, its operating principles, application and current issues. Chapter 3 is the main body of the thesis which presents a theoretical background with proposed solutions to the addressed issues in MPC presented in Chapter 2. Simulation results are also provided in this chapter. Chapter 4 presents experimental results and analysis along with DSP implementation of variable sampling frequency. Chapter 5 makes an overview of main contributions of this work and provides conclusions.

CHAPTER 2
MODEL PREDICTIVE CONTROL

2.1 Introduction

Considering the increasing demands in performance and efficiency of power converters, the development of new control schemes must take into account the real nature of these kinds of systems. Power converters and especially drives are nonlinear systems of a hybrid nature, including linear and nonlinear parts and a finite number of switching devices. The input signals for power electronic devices are discrete signals that command the turn-on and turn-off transitions of each device. Several constraints and restrictions need to be considered by the control, some of which are inherent to the system, like the maximum output voltage of the converter, while others are imposed for security reasons, like current limitations to protect the converter and its loads.

All the characteristics of power converters, as well as the characteristics of the control platforms, converge in a natural way to the application of model predictive control. The main characteristic of MPC is to use a model of the system to predict future behavior of the controlled variables. The main body of the model predictive control is the cost function. In case of a finite number of switching states, minimization of the cost function through multiple iterations produces the optimal actuation for the switches. MPC may easily consider numerous control objectives, just by inclusion of appropriate terms into the cost function. In such a way, the design of the controller becomes alleviated. Combined with modern digital processors it became prosperous control technique with ever growing potential.

This chapter extends the discussion on control methods to one of newly introduced control strategies in power electronics, model predictive control. Different classes of predictive control algorithms, operating principles, algorithms, block diagrams, advantages and flexibility, as well as challenges are discussed in this chapter. It further provides an example of the design process for current control of two-level converter with necessary discretization steps. Digital implementation as well as defining appropriate prediction horizon are also discussed. Finally, up-to-date challenges in MPC are presented. This chapter builds the foundations for the research which is focused on solving problems in predictive control applied to multi-level VSC.

2.2 Predictive Control in Power Electronic

Nowadays, practically all control strategies are implemented in digital control platforms running at discrete time steps. Design of any control system must take into account the model of the plant for adjusting the controller parameters, which in the case of power converters is well known. Control platforms offer an increasing computational capability thus more calculation-demanding control algorithms are feasible today.

As described before, due to the nature of predictive control, various constraints and objectives could be easily implemented. Along with the known mathematical models of the converters and considering the finite number of switching states, predictive control has stand up as a mighty alternative to classical control methods. The main features converging toward predictive control are summarized in Figure 10, which highlights the characteristics that lead to simple control schemes for the control of power converters and drives.

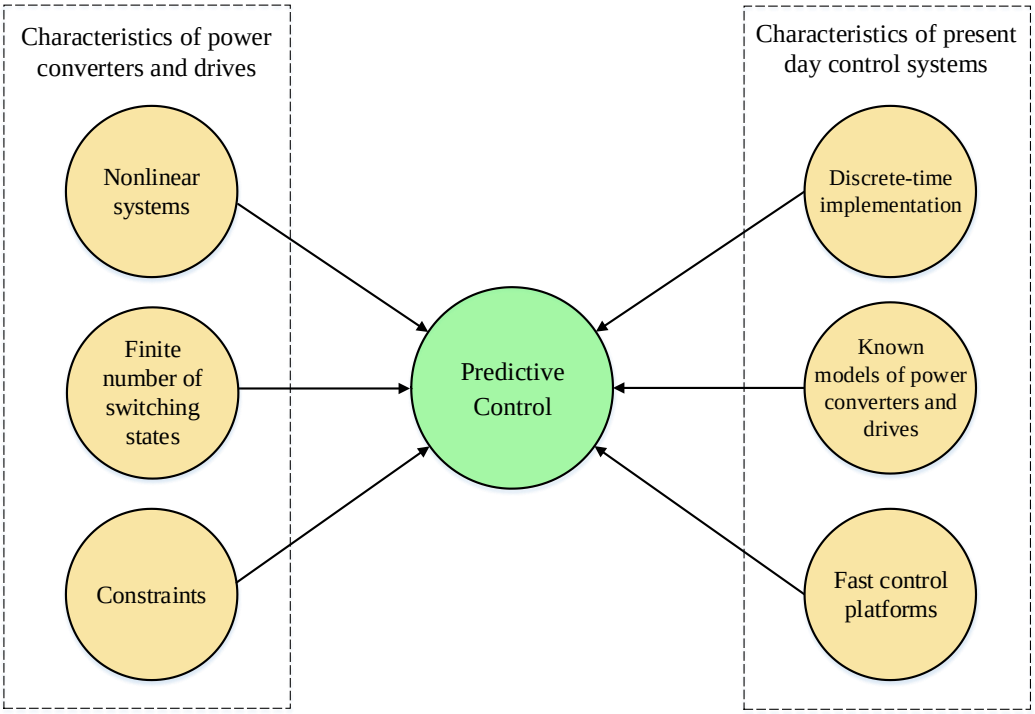


Figure 10 - Characteristics of predictive control

Predictive control includes a wide class of controllers that have found rather recent application in power converters. It avoids the cascaded structure, which is typically used in a linear control scheme, obtaining fast transient responses. Nonlinearities of a system can be included in the

model, thus avoiding the need to linearize the model for a given operating point and improving the operation of the system for all conditions. It is also possible to include restrictions to some variables when designing the controller.

2.2.1 Predictive Control Types

The classification of different predictive control methods is shown in Figure 11. The main feature of predictive control is to use the model of the system in order to predict future values of controlled variables. This information is used by the controller to obtain the optimal actuation, according to a predefined optimization criterion. The optimization criterion in the hysteresis-based predictive control is to keep the controlled variable within the boundaries of a hysteresis area, while in the trajectory based control the variables are forced to follow a predefined trajectory.

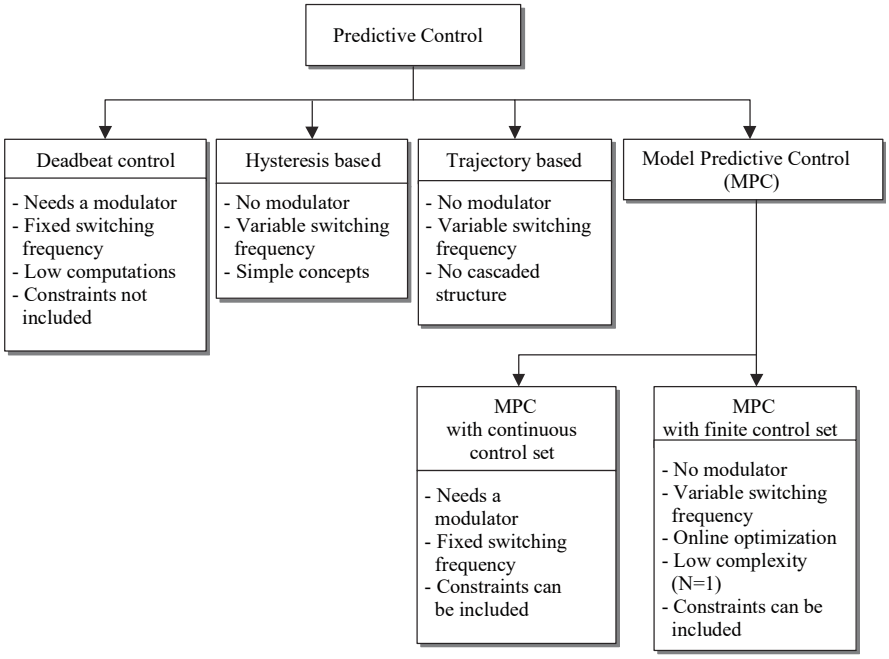


Figure 11 – Classification of predictive control

One of the earlier predictive controllers used in power converters, so-called dead-beat control, eliminates the classic linear controller by using a predictive model of the system. This model is used to calculate the required reference voltage in order to reach the desired reference value for a certain variable (usually the current). The predicted reference voltage is later generated by the converter via a modulation stage. This scheme has been applied for current control of inverters [28]–[34], rectifiers [35, 36], active filters [37, 38], and uninterruptible power supplies (UPSs) [39, 40].

Another approach emerged called model predictive control, in which a model of the system is considered in order to predict the future behavior of the variables. MPC is based on a minimization of the cost function which may include different control objectives and constraints. Using discretized equations, it is possible to predict the future value of the controlled variables, obtaining the future control actions.

The difference between these groups of controllers is that deadbeat control and MPC with continuous control set need a modulator, in order to generate the required voltage. This will result in having a fixed switching frequency. The other controllers directly generate the switching signals for the converter, do not need a modulator, and present a variable switching frequency.

MPC has several advantages, such as easy inclusion of nonlinearities and constraints. This scheme has few applications in power converter control due to high amount of calculations needed to solve the optimization problem online, which is incompatible with small sampling times used in converter control. One solution in order to reduce the calculation time is to solve the optimization problem offline, as presented in [41], where MPC is implemented as a search tree and the calculation time is reduced, making it possible to use the MPC in drive control. Another solution is the use of Generalized Predictive Control (GPC) [42], where the optimization is solved analytically, obtaining a linear controller. Nevertheless, with GPC, it is very difficult to include system constraints and nonlinearities.

Another approach to implement MPC for power converters takes advantage of the inherent discrete nature of power converters. Since power converters have a finite number of switching states, the MPC optimization problem can be simplified and reduced to the prediction of the system behavior only for those possible switching states. Then, each prediction is used to evaluate a cost function (also known as quality or decision function), and consequently, the state with minimum cost is selected and generated. This approach is known as a finite control set MPC since possible control actions (switching states) are finite. This method is also known as finite alphabet MPC or simply as predictive control, and it has been successfully applied to a wide range of power converters [12].

2.2.2 Control Requirements and Challenges for Three-Level Converters

Multilevel converters are recognized as among the most suitable and efficient candidates to be used in high-power, medium-voltage industrial applications. They can synthesize near sinusoidal voltages while increasing the number of levels, leading to good power quality and

smaller output filters. In addition, higher levels of MV operation can be achieved without connecting the switching devices in series. The most popular and well-known multi-level topologies are flying capacitor, cascaded H-bridge and diode-clamped converters. By using clamping diodes to divide the DC-link voltage among several capacitors, different configurations, ranging from three-level to m-level diode-clamped converters can be obtained.

Multi-level diode-clamped converters are suitable for many industrial applications such as: STATCOM, train traction, ship propulsion, regenerative conveyors, wind and photovoltaic energy systems, and general MV motor drive applications (pumps, fans, etc.) In these applications, current control is one of the most important issues and it has been widely studied in literature.

DC-link capacitor voltage balancing is one of the main issues in diode-clamped converters. Especially when the number of levels increases, the switching actions in three-level converters lead to an imbalance among the DC-link capacitor voltages. Usually, redundant switching states are used for proper balancing. Another important challenge for diode-clamped converters is the operation at low switching frequency in order to minimize the switching losses and to allow proper heat dissipation. This requirement can be accomplished with the PWM and SVM techniques by simply changing the carrier frequency. Unfortunately, low order harmonics are produced by the PWM and SVM techniques when operated below 1 kHz leading to poor output current quality. One more critical issue is that fast switching actions of the semiconductor devices cause high *dv/dt* in the converter output voltages and this leads to higher common-mode voltage. The common-mode voltage is undesirable when multi-level converters are used in motor drives. Mitigation of common-mode voltage through improvements in PWM/SVM techniques is a cost effective and attractive solution. However, the complexity of the SVM increases with the number of converter levels.

The finite control-set model predictive control takes over the functions of linear regulators and SVM/PWM modulators. To accomplish the aforementioned control requirements, they can be described in a single cost function and the importance of each term can be weighted by using assigned coefficients. This leads to fast and convenient implementation on digital processors.

2.3 The Concept of FCS-MPC

The common elements of FSC-MPC are: 1) using a model of the system to predict the future behavior of the variables (until a predefined horizon in time), 2) and selection of optimal actuations

by minimizing a cost function for a finite number of states. This structure has several important advantages:

- concepts are intuitive and easy to understand;
- it can be applied to a great variety of systems;
- the multivariable case can be easily considered;
- dead times can be compensated;
- easy inclusion of nonlinearities in the model;
- simple treatment of constraints;
- the resulting controller is easy to implement;
- this methodology is suitable for the inclusion of modifications and extensions depending on specific applications.

However, there are certain disadvantages that are stated below:

- larger amount of calculations for high-level converters;
- the quality of the model has a direct influence of the quality of the resulting controller;
- variable switching frequency caused by absence of a modulator.

The quality of the model has a direct influence on the quality of the resulting controller. If parameters of the system change with time, some adaptation or estimation algorithm must be considered.

2.3.1 FSC-MSC Operating Principle

The control problem for power converters can be defined as determining of an appropriate control action $S(t)$ (usually the gate signals of the converter) that will drive a generic system variable $x(t)$ as close as possible to a desired reference value $x^*(t)$. Consider the qualitative behavior of $x(t)$ and its regularly sampled value $x(t_k)$ over a sample period T_s for a system with a finite number of control actions n, as shown in Figure 12(a), where measurements, computations, and control actions are performed instantly (i.e., ideal case). Since the control actions or control set is finite in number S_i with $i = 1, \ldots, n$, they can be evaluated together with the measured value $x(t_k)$, based on a prediction function f_p, to predict all possible system transitions $x_{pi}(t_{k+1}) = f_p\{x(t_k), S_i\}$, for $i = 1, \ldots, n$.

This prediction function is directly derived from the discrete model and parameters of the system. To determine which of the control actions is to be selected, a decision or cost function f_g predictions can be defined, usually dependent on the desired reference value and the prediction $g_i = f_g\{x^*(t_{k+1}), x_i(t_{k+1})\}$ for $i = 1, \ldots, n$. Note that a future reference value is needed $x^*(t_{k+1})$, which can be assumed to be equal to the actual value $x^*(t_k)$, since T_s is sufficiently small compared with the dynamic behavior of the system, and thus, the reference can be considered constant over T_s. If needed for highly dynamic systems, the future reference value $x^*(t_{k+1})$ can be estimated via appropriate extrapolation methods. A typical example for f_g would be the absolute error between the predictions and the reference $g_i = |x^*(t_{k+1}) - x_{pi}(t_{k+1})|$. The evaluation of the cost function with n predictions leads to n different costs. Naturally, control action leading to the minimum cost ($\min\{g_i\}$, for $i = 1, \ldots, n$) is selected to control the system.

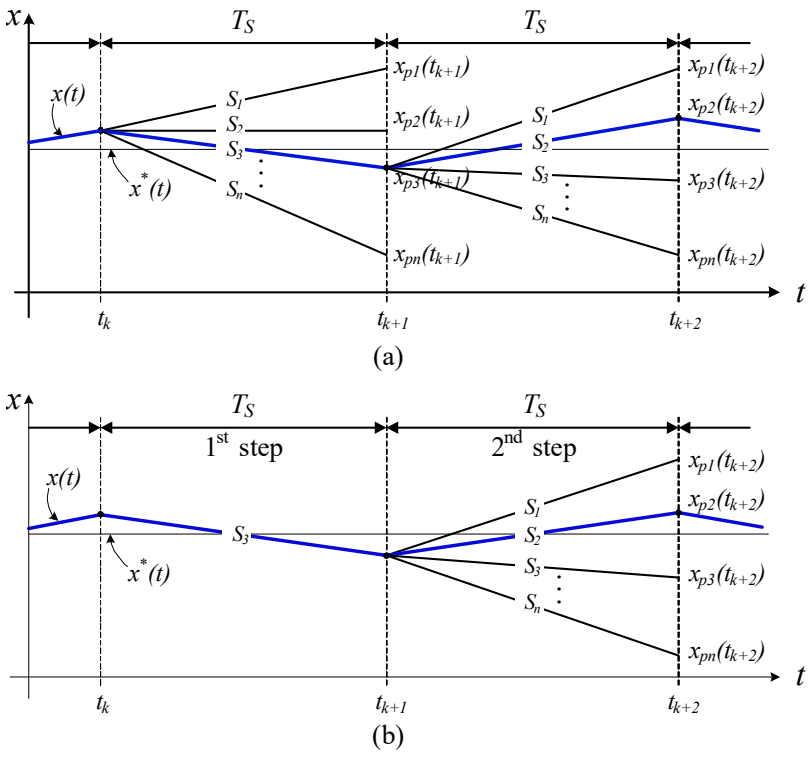


Figure 12 – FCS-MPC operating principle: (a) ideal theoretical case (b) implementation case

Based on the example shown in Figure 12(a), the predicted value $x_{p3}(t_{k+1})$ is the closest to the reference $x^*(t_{k+1})$, hence, S_3 is selected and applied at $t = t_k$. Following the same criterion, S_2 is selected and applied in $t = t_{k+1}$. However, the ideal theoretical case in which the variables can be measured, predicted, and controlled instantly in $t = t_k$ is not feasible in real-time applications.

Nevertheless, this problem can be overcome if a two-step-ahead prediction is considered, as shown in Figure 12(b), in which the control action to be applied in the following sample time $S(t_{k+1})$ is determined. This way, a complete sample period T_s is available to perform the algorithm.

Naturally, the sample period T_s has to be greater than the measurement, computation, and actuation times added together. Assume that on a sample time t_k, a measurement $x(t_k)$ is made and the previously computed control action $S(t_k)$ is applied. With this information and the system model, a first prediction can be made to obtain the future value $x(t_{k+1})$ (this is the first step prediction).

Now, from the predicted value $x_p(t_{k+1})$, the FCS-MPC algorithm is performed for n possible control actions, leading to one optimal selection $S(t_{k+1})$ (this is second step prediction). Both predictions are performed during the first sample period, and then, at $t = t_{k+1}$, the optimal selected control action $S(t_{k+1})$ is applied, while $x(_{tk+1})$ is measured to perform the algorithm again. As shown in the example in Figure 12(b), there is only one prediction for the first step, given by the applied control action $S(t_k) = S_3$ determined in the previous execution of the algorithm, while $S(t_{k+1}) = S_2$ is selected from n predictions for the second step.

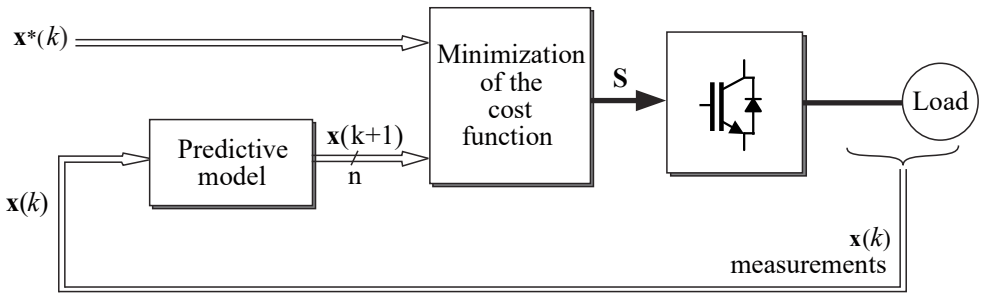


Figure 13 – FSC-MPC generic control diagram

A simplified control block diagram for the real-time implementation of FCS-MPC is shown in Figure 13, considering a generic system variable $x(t)$. It is worth mentioning that this control method is not limited to a single variable; on the contrary, multiple variables, system constraints, perturbations, saturations, and, basically, every characteristic that can be mathematically modeled and measured can be included in the predictive model and cost function. This is the basis of a great flexibility and control potential that can be achieved with FCS-MPC. Moreover, the fact that power converters have a reduced and limited number of switching states (or control set) makes this method feasible for implementation with presently available microprocessing resources. Since only a discrete model of the system is necessary, rather than approximated linear models (together with

control system design theory and modulation algorithms), a simpler and more direct design and implementation of the controller are achieved.

2.3.2 Controller Design

In the design stage of FCS-MPC for the control of a power converter, the following steps are identified:

- modeling of the power converter with identifying all possible switching states and its relation to the input or output voltages or currents,
- defining a cost function that represents the desired behavior of the system,
- obtaining discrete-time models for prediction of the future behavior of the variables to be controlled.

When modeling a converter, the basic element is the power switch, which can be an IGBT, a thyristor, a gate turn-off thyristor (GTO), or others. The simplest model of these power switches considers an ideal switch with only two states: on and off. Therefore, the total number of switching states of a power converter is equal to the number of different combinations of two switching states of each switch. However, some combinations are not possible, for example, those combinations that short-circuit the DC-link. As a general rule, the number of possible switching states N is

$$N = x^y \tag{7}$$

where x is the number of possible states of each leg of the converter, and y is the number of phases (or legs) of the converter. In this way a three-phase, two-level converter has $N = 2^3 = 8$ possible switching states, a three-phase, three-level converter has $N = 3^3 = 27$ switching states, and a five-phase, two-level converter has $N = 2^5 = 32$ switching states. In some multilevel topologies the number of switching states of the converter can be very high, as in a three-phase, nine-level cascaded H-bridge converter, where the number of switching states is more than 16 million.

Another aspect of converter model is the relation between the switching states and the voltage levels, in the case of single-phase converters, or voltage vectors, in the case of three-phase or multi-phase converters. For current source converters, the possible switching states are related to current vectors instead of voltage vectors. It can be found that, in several cases, two or more switching states generate the same voltage vector.

For example, in a three-phase, two-level converter, the eight switching states generate seven different voltage vectors, with two switching states generating the zero vector. In a three-phase, three-level converter there is a major redundancy, with 27 switching states generating 19 different voltage vectors. Figure 14 depicts the relation between switching states and voltage vectors for two different converter topologies. In some other topologies, the method of calculating possible switching states may be different.

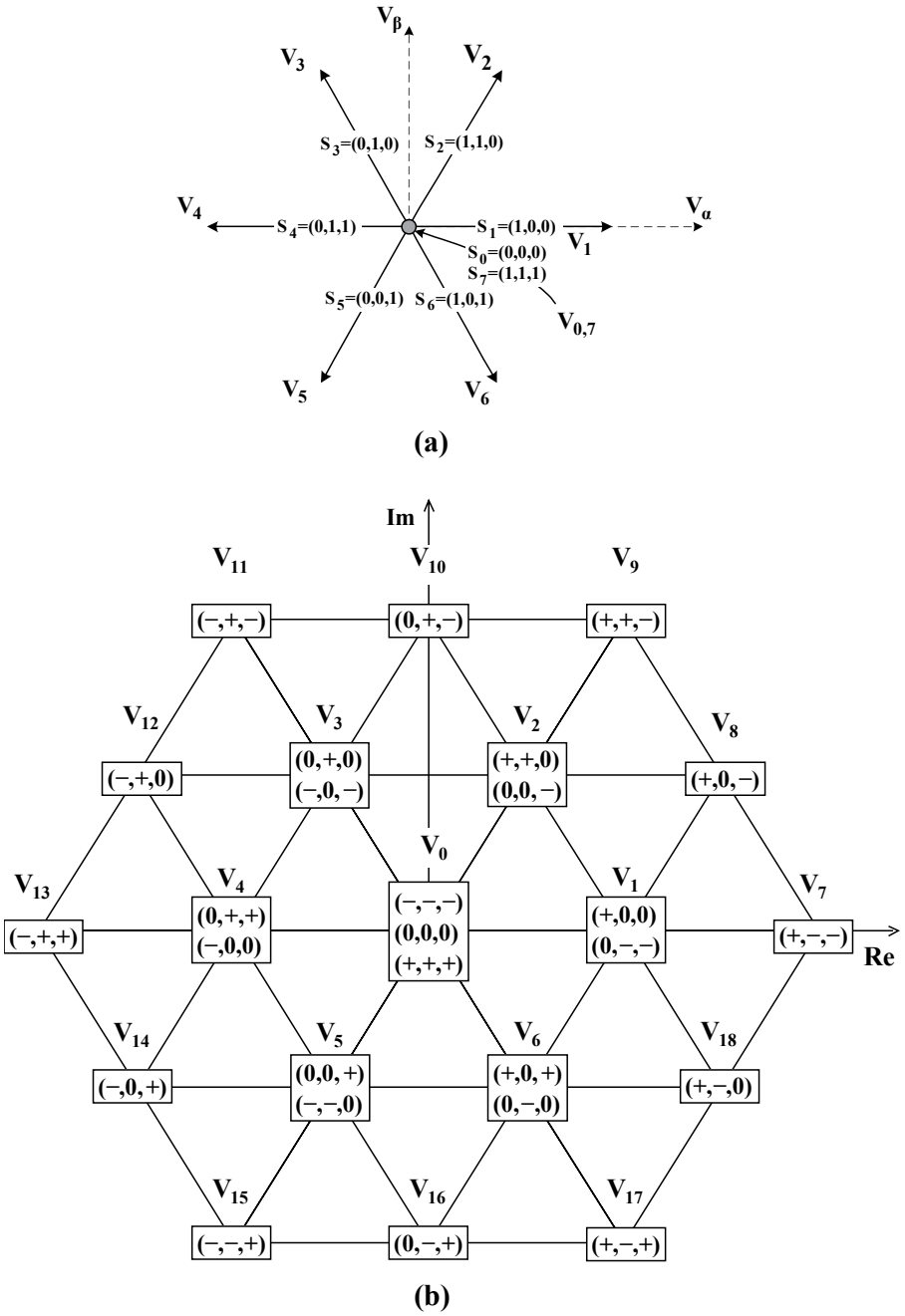


Figure 14 – Voltage vectors generated by a) two level converter, b) three-level converter

Each application imposes several control requirements on the systems such as: current control, torque control, power control, low switching frequency, etc. These requirements can be expressed as a cost function to be minimized. The most basic cost function measures the error between a reference and a predicted variable, for example, load current error, power error, torque error, etc. However, one of the advantages of the predictive control methods is the possibility to control different types of variables and include restrictions in the cost function. In order to deal with different units and magnitudes of the controlled variables, each term in the cost function is multiplied by a weighting factor that can be used to adjust the importance of each term.

When building a model for prediction, the controlled variables must be considered in order to get discrete-time models that can be used for prediction of these variables. It is also important to define which variables are measured and which ones are not measured, because in some cases variables that are required for the predictive model are not measured and some kind of estimation will be needed. To get a discrete-time model it is necessary to use some discretization methods. For first-order systems it is simple to approximate the derivatives using the Euler forward method, i.e., using

$$\frac{dx}{dt} \approx \frac{x(k+1)-x(k)}{T_s} \tag{8}$$

where T_s is the sampling time. However, when the order of the system is higher, the discrete-time model obtained using the Euler method is not precise because the error introduced by Euler's method for higher order systems is significant. For these higher order systems, an exact discretization must be used.

2.3.3 Current FCS-MPC of a 2L-VSI

The FCS-MPC current control problem can be easily derived from the generic operating principle analyzed in this section. The variable $x(t)$ would be the current i_s; the control action $S(t)$ represents the switching states (S_i, with $i = 0, \ldots, 7$) of the converter. The predictive model corresponds to the discrete time model of the load, with Euler approximation of the current derivative, which leads to

$$i_{sp}\{S_i\} = \frac{Li_s(t_k)+T_sV_i(t_{k+1})}{RT_s+L} \tag{9}$$

$$V_i(t_{k+1}) = \frac{2}{3}V_{dc}(S_i[1\ a\ a^2]^T) \tag{10}$$

where $\mathbf{i}_s(t_k)$ is the measured current and $\mathbf{v}_{i(t_{k+1})}$ is the voltage vector generated by the switching states S_i, with $i = 0, \ldots, 7$. Additionally, note that $\mathbf{i}_{ps} = i_{\alpha p} + j i_{\beta p}$. Finally, the cost function that needs to be minimized is

$$g_i(t_k) = \left|i_\alpha^* - i_{\alpha p}\{S_i\}\right| + \left|i_\beta^* - i_{\beta p}\{S_i\}\right| \tag{11}$$

The corresponding simplified block diagram of the current FCS-MPC is shown in Figure 15 as a flow diagram.

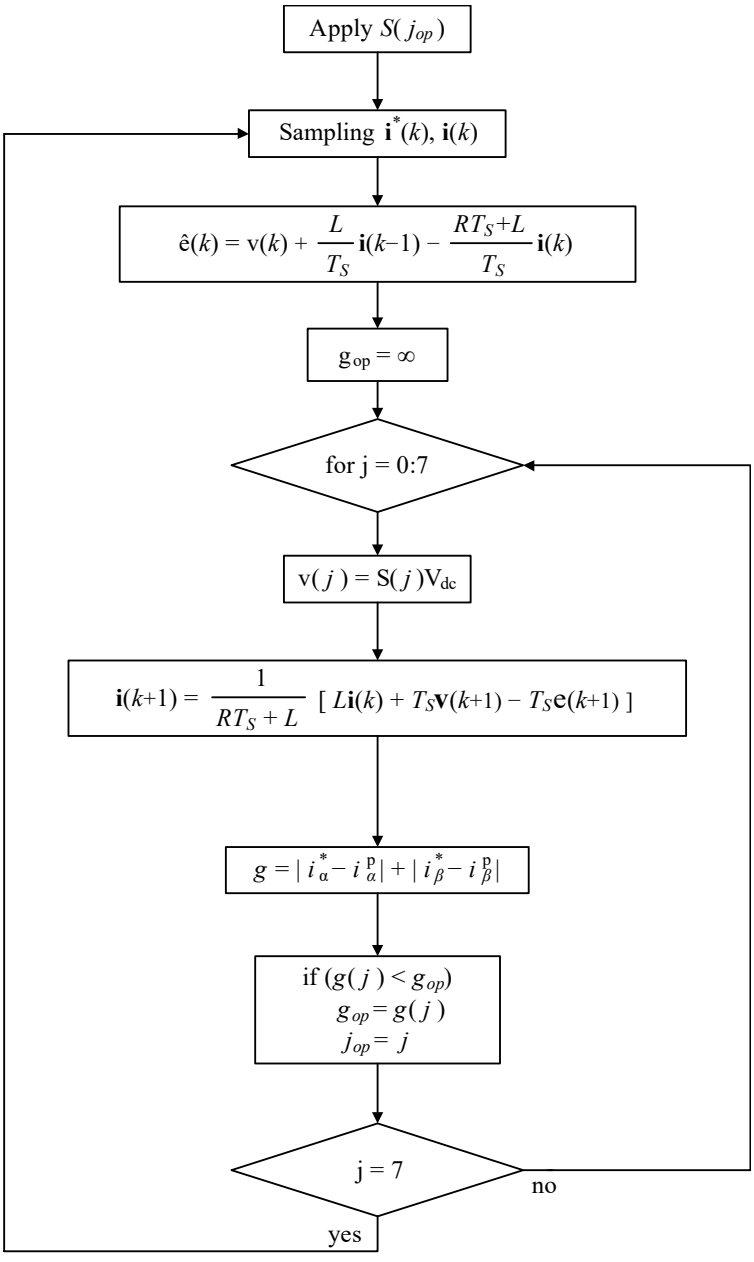


Figure 15 – Flow diagram of implemented control algorithm

The FCS-MPC does not force a commutation in each sample period. Hence, the average switching frequency is variable, leading to a spread current spectrum. As shown in the flow diagram, this current control is performed in the following steps:

1. the value of reference current is obtained and the load current is measured;
2. the model of the system is used to predict the value of the load current in the next sampling interval for each voltage vector;
3. the quality function *g* evaluates the error between reference and predicted currents in the next sampling interval. The voltage that minimizes the current error is selected and applied to the load.

As shown in the diagram, the minimization of the quality function can be implemented as cyclical prediction for each voltage vector, evaluating the quality function, and storing the minimum value and the index value of the corresponding switching state.

2.4 Applications of Model Predictive Control and Challenges

For power conversion systems in the megawatt range, device average switching frequencies over 1 kHz are considered inconvenient. In fact most common switching frequencies are found around 500 Hz for IGBT and IGCT based converters. The use of lower switching frequencies introduces a mayor trade-off between efficiency and high dynamic performance, and has been a challenge in power electronics for decades.

Model predictive control is a powerful control strategy that uses the model of the system to pre-calculate the behavior of the system for a predefined horizon in the future. The standard implementation of predictive current control calculates the voltage required by the load to get the desired current. Then this voltage is applied using pulse width modulation. This scheme has been used for the control of single-phase and three-phase inverters, inverters with output LCL filter, rectifiers and active filters, and uninterruptible power supplies. This concept has also been used for torque control of induction machine. It is also possible to calculate the duty cycles for the converter instead of the voltages. Some works have been presented using this scheme for current control in a three-phase inverter and a matrix converter, flux and torque control of an induction machine [43], and direct power control in an active front end rectifier [44].

It is also possible to include and control different variables using a single cost function. For instance, while the current is controlled, at the same time, the cost function minimizes the switching

frequency and balances the DC-link voltages in a neutral point clamped converter. This approach is easily extended to the drives, where the entire system can be easily modelled including nonlinearities. The fact is that the versatility and universality of MPC approach delivers great potential for a wide range of application and an ever growing research potential.

In all applications the switching states are changed at equidistant time instants. However, lack of modulation stage leads to a variable switching frequency producing spread voltage spectrum over a range of frequencies. This is certainly one of the most significant issues in MPC which reduces its potential for practical implementation. As discussed above, high number of converter voltage levels generates many possible switching states. Due to extensive calculation required, real-time implementation of MPC for high-level converters becomes troublesome. Moreover, weighting factor design faces significant problems as an optimized procedure has not been presented up-to-date. The work in Chapter 3 presents solutions to some of the problems stated.

2.5 Summary

In this chapter state-of-the-art converter control techniques are reviewed followed by the discussion of various classes of predictive control techniques. The operating principle of FCS-MPC is discussed for ideal and implementation cases. The implementation of current control strategy has been discussed for 2-level converter through a flow diagram. Furthermore, the applications of model predictive control and technical challenges are also presented.

The strategy introduced in this chapter leverages the discrete nature of power converters and microprocessors. The predictive control has proven to be effective with a good dynamic response and compares well with the classical methods. The use of linear and nonlinear controllers is avoided. In addition, it is not necessary to include any type of modulator. The high calculation power of today's existing DSPs makes this method attractive to control power converters. Even though the method might be simple in case of 2-level converter, the control algorithm might become difficult to implement for some multilevel converters due to the extensive number of calculations.

The results and analysis show that predictive control is a strong tool with a conceptually different approach that opens up new possibilities for power converters control, especially in the field of multi-level converter based systems.

CHAPTER 3
VARIABLE SAMPLING FREQUECNY MODEL PREDICTIVE CONTROL

3.1 Introduction

As discussed in a previous chapter, various control strategies can be used to control rectifiers and inverters. One of the newest control methods with numerous advantages over classical control is certainly model predictive control. As many of control objectives could be simultaneously considered and easily implemented without the need for a cascaded control, MPC becomes promising solution to control the converters in the future.

Spread spectrum and variable switching frequency is a well-known problem with model predictive control that still has not been fully solved. The work in [45] proposes preliminary study on using a discrete Fourier transform (DFT) in the cost function to solve this issue. The authors in [46] presented a frequency weighted cost function to shape the harmonic spectrum. The addition of secondary control objectives to cost function reduces the relative importance of primary control objective, i.e., load current control. As a result, the quality (total harmonic distortion) of the load current deteriorates. The variable switching frequency nature with these two works is still unanswered. In [47] the authors incorporate duty-cycle calculation into cost function which determines the time each vector will be applied for. This method is able to concentrate the spectrum around certain frequency. However, the authors use a very high inverter switching frequency. It is not clear how the method performs if the switching frequency was lower. Furthermore, the experimental results are not provided to support theoretical analysis. The work in [48] proposes selective harmonic elimination for predictive control. This concept fixes the switching frequency but only mitigates certain harmonics in the spectrum. The current waveform is not half-wave symmetrical and some low-order triplen harmonics are still present.

This work aims to solve the challenges associated with the FCS-MPC such as spread spectrum and variable switching frequency by introducing variable sampling frequency concept. This method uses an auxiliary algorithm to calculate the number of sampling points to be used in the main predictive control algorithm. This approach combines the working principles of the FCS-MPC and space vector modulation to achieve high dynamic performance as in FCS-MPC and fixed switching frequency operation as in SVM.

In this chapter a variable sampling frequency model predictive control is presented for the elimination of even-order harmonics and spectrum shaping. The proposed strategy was verified with the NPC converter, since it presents more challenges compared to a standard two-level converter. Multiple objectives are considered at the same time, such as: load current control, balancing of the DC-link capacitor voltages, common-mode voltage mitigation and elimination of even-order harmonics in the load current harmonic spectrum. The corresponding simulation results are presented for both NPC rectifier and inverter configurations.

3.2 Virtual System Simulator Model for Harmonic Spectrum Shaping

The very well-known characteristic of FCS-MPC is that a switching pattern does not exists as the control does not use a modulator. This issue leads to a variable switching frequency. Due to unsynchronized sampling between the measurements and output fundamental frequency, the chosen states (voltage vectors) vary from the selected switching states in the preceding cycle. The resulting switching does not fit into a pattern, leading to a spectrum with spread frequencies, containing integer and non-integer multiples of the fundamental frequency.

To solve the spectral problem, a novel variable sampling frequency finite control-set model predictive control (VSF-FSC-MPC) is proposed for spectrum shaping and fixed switching frequency operation. The objectives of the proposed control strategy can be summarized as:

- even-order harmonic elimination and spectrum shaping for inverters and rectifiers;
- ability to maintain primary control objective with minimum error during fixed switching frequency operation for spectrum shaping;
- ability to fulfill secondary control objectives, such as voltage balancing or common-mode voltage mitigation/elimination while maintaining primary control objective and spectrum shaping;
- rectifier active and reactive power control and capacitor voltage balancing with even-order harmonic elimination for grid-friendly operation;
- inverter/rectifier switching frequency control.

Variable sampling operation requires sampling frequency to be continuously adjusted based on the operating conditions. The proposed concept whose general block scheme is presented

in Figure 16 introduces a control algorithm named virtual system simulator (VSS). The function of the VSS block is to simulate the power converter system with its load and locate an appropriate sampling frequency based on a simulated waveforms of required variables. It uses MPC to develop the data which will be analyzed on the existence of harmonics which should be eliminated from the spectrum. The VSS operates in parallel with main MPC and is implemented as its subroutine. The VSS entity is fully described in C/C++ language and therefore reflects the FCS-MPC concept providing convenient implementation on modern control hardware.

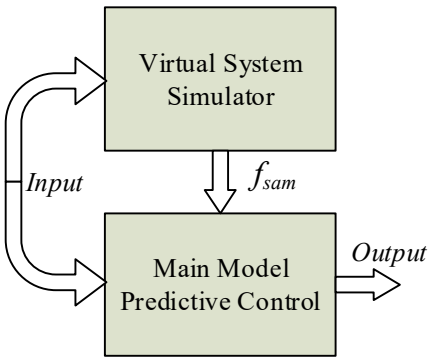


Figure 16 – General concept of MPC with VSS

A more detailed version of the VSS is presented in Figure 17. The VSS structure can be visually separated into four stages based on their function. First stage uses SVM concept to determine the position of the reference vector (v_{ref}) and to locate the nearest three vectors that surround the reference vector. Secondly, the VSS uses an internal MPC to simulate the behavior of a power converter system. This module was named auxiliary model predictive control (AMPC) and is clocked at a sampling rate fed from the sampling frequency shifter block.

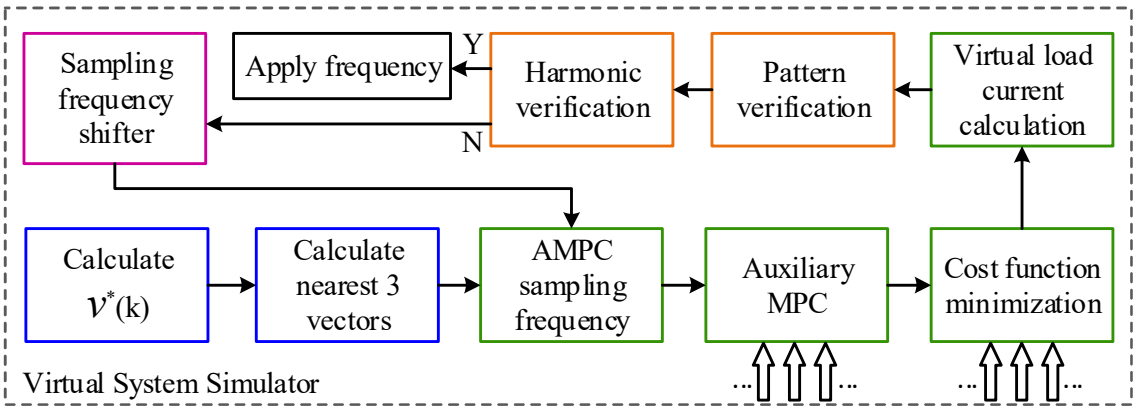


Figure 17 – Model of Virtual System Simulator

This module also carries the VSS waveform simulator/plotter which calculates the load waveforms. Subsequently, the produced waveforms are subjected to harmonic analysis which is done in third stage. Finally, the last stage is a frequency shifter and its function is to control the sampling frequency with respect to setup operating conditions and restrictions. Each of these segments is explained with more details in the upcoming sections.

3.2.1 Vector Selection Using SVM

The space vector hexagram is used to select the vectors available to predictive controller at any time instant for a given reference current. The intensity and position of reference vector v^* is calculated based on the reference current i^*. Then as presented in figure 18, three vectors V_a, V_b and V_c are selected based on nearest-three criterion with regard to the position of v^*. The limitation imposed on the vectors has a significant impact on shape of the produced waveforms. If the controller in not allowed to randomly select vectors from a group of 27 available for the three-level converter, but is forced to use only three selected vectors, a pattern begins to appear in the switching sequence inside a fundamental cycle.

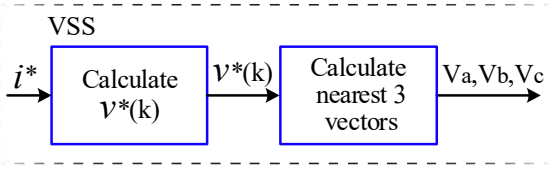


Figure 18 – VSS module for reference calculation and nearest vector selection

The appearance of a pattern during steady-state operation is due to the fact that SVM prevents the cost function from considering the vectors arbitrarily. Performance-wise, in integration of SVM into MPC yields significant improvements by reducing the time needed for cost function assessment. For instance, if a number of available vectors at any point in time is not greater than three, the calculation burden on the processor could be reduced up to 9 times for three-level converter.

Using SVM diagram presented in Figure 19(a) with all possible vectors and their states for the NPC converter, the intensity of v_{ref}, i.e., the position of the peak of the vector is calculated through the following expression:

$$v_{ref} = i^* * \frac{V_{dc}}{I_{B^*}\sqrt{6}} \tag{12}$$

where, i^* is the reference current, V_{dc} is the converter DC-link voltage and I_B is the base current. Based on the intensity of the vector and its angular distance from the x-axis it is possible to assess its exact position, i.e. the region the vector is located in. All the lengths in Figure 19(b) are assumed to be multiplied by V_{dc}, but for the sake of simplicity the multiplication is not pictured in the figure. By using trigonometry expressions, the following dynamic models are derived:

$$X_{3al} = \frac{\left(V_{dc*}\frac{\sqrt{3}}{6}\right)}{\sin\left(\frac{2\pi}{3}-\theta\right)} \tag{13}$$

$$X_{3bl} = \frac{\left(V_{dc*}\frac{\sqrt{3}}{6}\right)}{\sin\left(\frac{\pi}{3}-\theta\right)} \tag{14}$$

$$X_{3cl} = \frac{\left(V_{dc*}\frac{\sqrt{3}}{6}\right)}{\sin(\theta)} \tag{15}$$

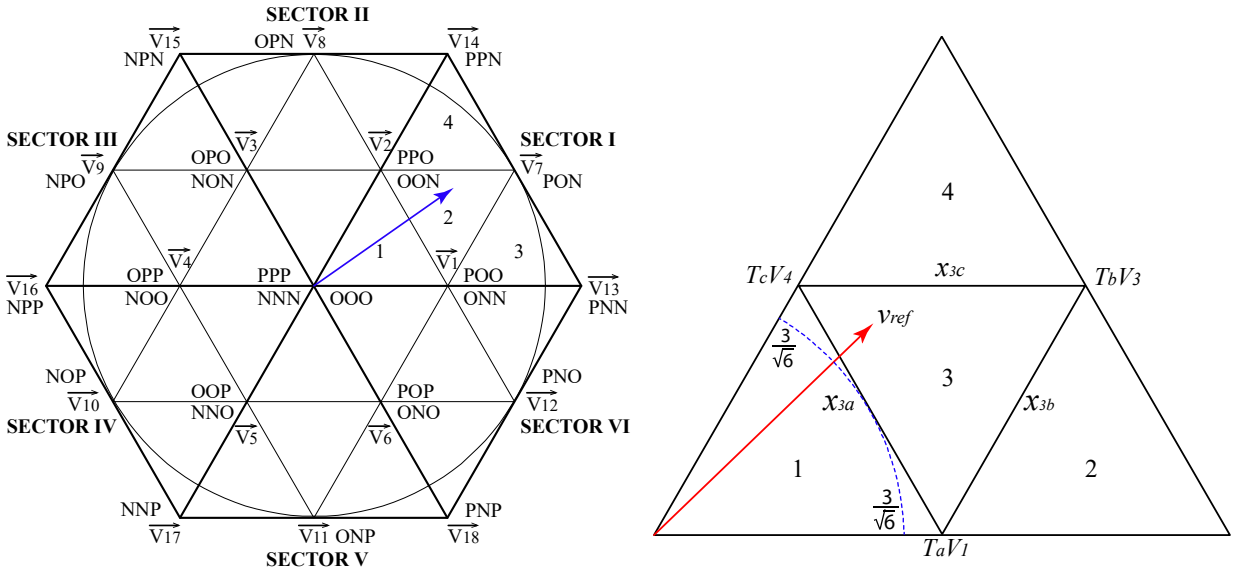


Figure 19 – Two-level SVM: a) Division of sectors and regions, b) Regions 1 to 4 in Sector I

The expressions in (13)-(15) need angle θ which is obtained from $\alpha\beta$-frame coordinates and it is calculated during each sampling period T_s. The above expressions are used to calculate the length from the origin to any point located on the sides of triangle 3 (Figure 19b). The intensity of the reference vector is then compared with the calculated length to determine its position. For instance, to determine if v_{ref} is located in region 1, expression (13) is used to find the length from the origin to the point on x_{3a}-side for the given θ. If the intensity (length) of v_{ref} is less than the

length from the origin to the point on x_{3a}-side, v_{ref} is located in region 1. Further, if the intensity is higher than x_{3a} and if θ is less than 30^{o}, then expression (14) is used to calculate the dot on x_{3b}-side to determine whether v_{ref} is located in region 3 or 2. We conclude that if the intensity of v_{ref} is higher than the calculated length, v_{ref} is located in region 2. If it is less, it is positioned in region 3. The same principle is used for determining the position in regions 3 and 4.

The conventional SVM scheme uses a predefined switching sequence. In the design of a switching sequence a special care has to be taken to the distribution of the dwell times and their correct arrangement. There are two possible cases that have to be considered. First, there is only one small vector among the nearest three and, secondly when the reference vector is located in region 1, there are two small vector of whom one is dominant half of the time.

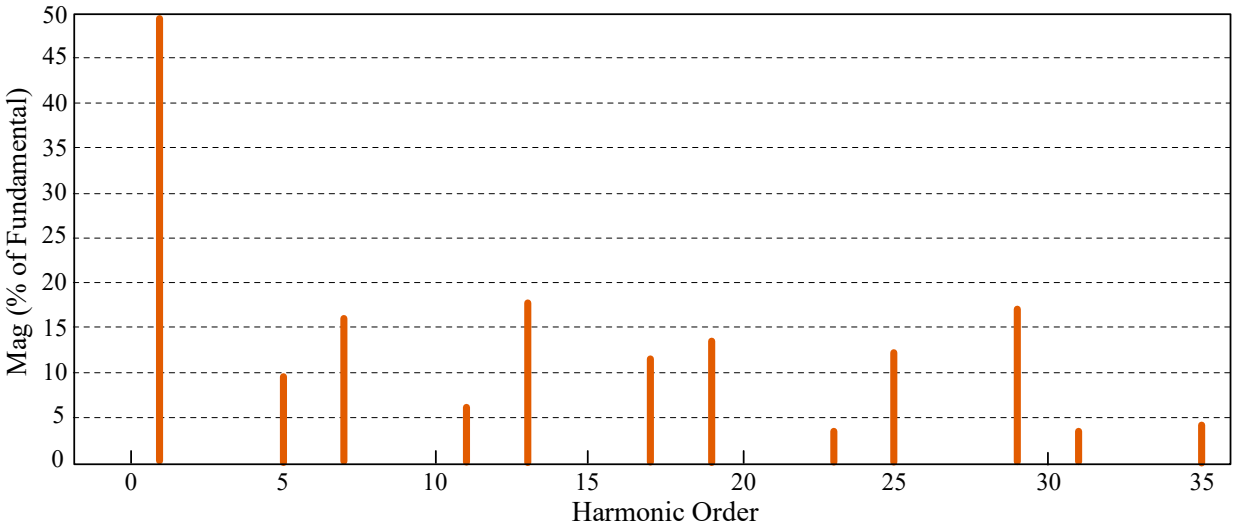


Figure 20 – General current spectrum with SVM

For even-order harmonic elimination two types of sequences should exist: sequence A and sequence B. It can be observed that type-A sequence should start with an N-type small vector while type-B sequence should commence with a P-type small vector. Combining sequence A and B even-order harmonics can be eliminated with a slight increase in current THD. Figure 20 presents a THD of the line-to-line voltage with implemented even-order harmonic elimination, obtained by using SVM.

Even though the SVM combined with FCS-MPC represents a significant step toward spectrum shaping, it is only the combination of the variable sampling frequency and applied restrictions in SVM-based operation that establishes the right conditions for complete elimination

of undesired spectral components in the load current. Therefore, further techniques constitute necessary steps toward final pattern design.

3.2.2 Auxiliary MPC and Virtual Load Current Calculation

The VSS concept employs auxiliary model predictive control as a separate control mechanics inside the VSS. It is important to note that the AMPC operates only in VSS and therefore is not directly related to the main MPC, i.e., AMPC does not control the converter. The AMPC however uses the same power converter model as MPC. An internal loop of the AMPC is presented in Figure 21. The sampling frequency f_{sample} determined by the frequency shifting block is fed to the AMPC. The AMPC is then executed until one full fundamental cycle of the load current is calculated and stored for analysis. Cost function minimization delivers actuation for the switches S_{1x} and S_{2x}, which produces virtual currents i_{av}, i_{bv} and i_{cv}.

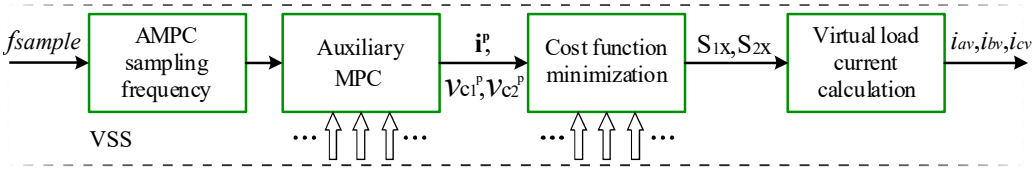


Figure 21 – VSS module for virtual load current generation

If stored 3-phase current waveforms after analysis contain harmonics to be removed from the spectrum, the data storing registers will be flushed and the AMPC is restarted to develop new virtual current at a different internal sampling frequency. The flow diagram of the AMPC is presented in Figure 22. It can be observed that AMPC considers only 3 vectors according to the implemented SVM. Selected vectors are applied to the virtual load and the measurements are fed back to the AMPC.

Since THD estimation requires at least one complete fundamental cycle it is required to generate a set of values that will be analyzed on existence of various harmonic frequencies. The block generates virtual currents and stores the data by dynamically assigning memory space for the arrays. Subsequently, these values are used by the AMPC and compared with their virtual references to calculate the error whose attempt of minimization will deliver required virtual voltage vector to be applied at $k+1$ horizon. Continuing in this fashion, we obtain an actual extrapolation of the currents for one or more complete cycles. Once the train of information is formed, it is used

for harmonic analyzes. To develop the current waveforms, the virtual load current calculation block uses time domain load model.

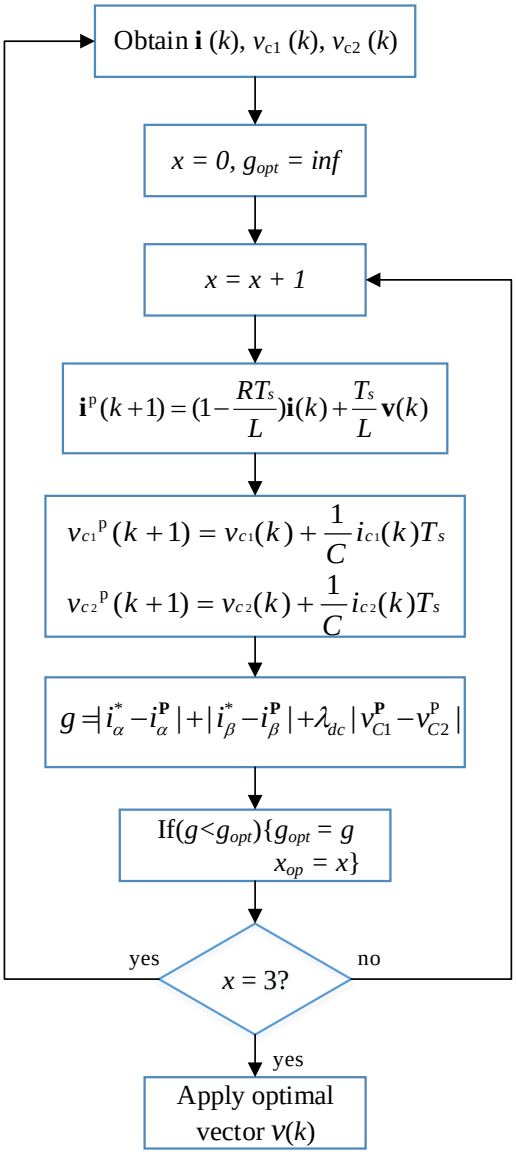


Figure 22 – Auxiliary MPC flow diagram for the NPC inverter

Virtual load currents are calculated using expressions (16)-(18):

$$I_a = \frac{V_{an}}{R} - \left(\frac{V_{an}}{R} - I_{oa}\right) * e^{-\frac{R}{L}t} \tag{16}$$

$$I_b = \frac{V_{bn}}{R} - \left(\frac{V_{bn}}{R} - I_{ob}\right) * e^{-\frac{R}{L}t} \tag{17}$$

$$I_c = \frac{V_{cn}}{R} - \left(\frac{V_{cn}}{R} - I_{oc}\right) * e^{-\frac{R}{L}t} \tag{18}$$

where V_{an}, V_{bn} and V_{cn} are the phase to neutral voltages whose values are to be calculated based on selected switching signals S_a, S_b, S_c and known DC-link voltage V_{dc} as:

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \left\{ v_{dc} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \right\} \tag{19}$$

Furthermore, I_{oa}, I_{ob} and I_{oc} are the initial conditions that must to be known at the point in time where the switching signals change. The initial conditions are calculated using the same expressions (16)-(18) but with previously used vector, right before the calculation of the currents I_a, I_b and I_c using new assigned vector. In order for the algorithm to function properly, these expressions are calculated with each VSS clock.

Even though the load equations introduce time t and not sample time T_s, it is important to note that t is also discretized, as the VSS eventually gets implemented on a digital processor. The recommended resolution of the calculated virtual output current is 64 times higher than the AMPC sampling frequency. Knowing that both AMPC and the waveform plotting part are parts of VSS, AMPC has to be internally slowed down in a ratio of 64:1.

In the next stage of VSS the currents are passed through a pattern/harmonic verification blocks. If this test passes, the correct f_{sample} is determined and the counter compare registers of the DSP are set accordingly to match the new sampling rate.

3.2.3 Load Current Verification

The main part of the VSS which assures that the produced output waveforms in the converter controlled by the MPC contain only the harmonics of interest is the verification module. This module utilizes two-step verification and is presented in Figure 23. The first step consists of analyzing the sequence of vectors across 6 SVM sectors in a fundamental cycle based on calculated virtual load currents i_{av}, i_{bv} and i_{cv}. This kind of verification is fast since it only requires a comparison between arrays of integers. The block output is a signal which defines if the verification process continues or the pattern have failed to appear in the switching sequence. If the pattern exist, further verification is required since establishing a pattern does not necessarily assume the current spectrum does not contain even or triplen harmonics. However, if the pattern

does not exist the loop process is reset and starts from the beginning with different sampling frequency.

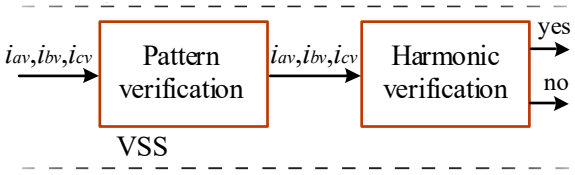


Figure 23 – VSS module for virtual load current verification

The second block in the chain performs a thorough harmonic verification. The algorithm uses the Discrete Fourier Transform (DFT) on a window with a high number of samples taken per virtual current fundamental cycle. Finally, the output result of the harmonic verification block approves or discards current sampling frequency, depending on spectrum content. If the block outputs a positive value, the sampling frequency used in the VSS is correct for the given operating conditions. If not, the sampling frequency is marked not optimal and the sampling frequency shifter will provide the new sampling frequency based on given requirements and constraints.

3.2.4 Sampling Frequency Shifter and Constrains

The frequency shifter block presented in Figure 24 provides variable sampling frequency for the entire VSS. The block calculates the new frequency each time the VSS indicated current sampling frequency as not optimal through sampling frequency shift request.

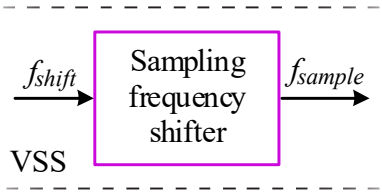


Figure 24 – VSS module for sampling frequency control

In order to provide the data to the controller in equidistant time points, the sampling frequency has been synchronized with the fundamental frequency of output load current. Considering the space-vector diagram, there are 6 sectors, each phase shifted by 60 degrees. The correct synchronization requires the number of samples (N_s) to be the same integer in each of 6 sectors. Therefore, the sampling frequency can be obtained through equation (20),

$$f_{sample} = f_{fund} * 6 * N_S \quad (20)$$

where N_s stands for the number of samples per sector and f_{fund} is the required load current fundamental frequency or the grid frequency. It is required to provide N_s dynamically to obtain the switching pattern under any condition, producing spectrum content without even or triplen order harmonics.

3.2.5 Capacitor Voltage Balancing using P/N/O States

The proposed VSS concept opens an alternative way for balancing the capacitor voltages. Since pattern in the switching sequence can be created by using the VSS, it is now possible to balance the DC-link voltages by judiciously sorting the *P* and *N* states of small vectors. The influence of each type of vectors to the DC-link voltage can be analyzed as follows. Since the neutral point *Z* is left unconnected, the switching state PPP does not affect V_Z. Similarly, the other two zero switching states, OOO and NNN, do not cause V_Z to shift either. With the *P*-type switching state the three-phase load is connected between the positive DC bus and neutral point *Z*, therefore, the neutral current i_z flows into *Z* causing V_Z to increase. On the contrary, the *N*-type switching state makes V_Z decrease. The medium-voltage vectors also affect the neutral-point voltage. Depending on the converter operating conditions, the neutral-point voltage V_Z may rise or drop. Considering large vectors the load terminals are connected between the positive and negative DC buses. The neutral point *Z* is left unconnected, and thus the neutral voltage is not affected.

To minimize the neutral-point voltage deviation, the dwell time of a given small vector can be equally distributed between the *P*- and *N*-type switching states over a sampling period. According to the triangular region that the reference vector is in, the following two cases are investigated. In the first case there is one small vector among three selected vectors. To minimize the neutral voltage deviation, the dwell time for the small vector should be equally distributed between the *P*- and *N*-type states. In the second case two out of three selected vectors are small vectors. Again, to reduce the neutral voltage deviation, the dwell time should be equally distributed.

If the states are correctly arranged it is possible to maintain the voltages balanced under normal operating conditions. This way a nice feature emerges to control the inverter switching frequency. For instance, by sorting the states in a different order, but keeping the distribution of

the dwell-times equal, the operating switching frequency can be utilized differently. The resulting action will only affect the capacitor voltage ripple.

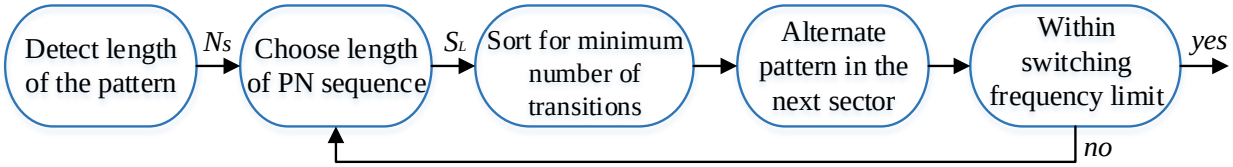


Figure 25 – P/N/O state sorting

In a sense, the DC-link capacitor voltage ripple becomes decoupled from load current control in terms of converter switching frequency. Only a slight increase in current THD is expected with the increase in voltage ripple. The algorithm for sorting the vectors is presented in Figure 25.

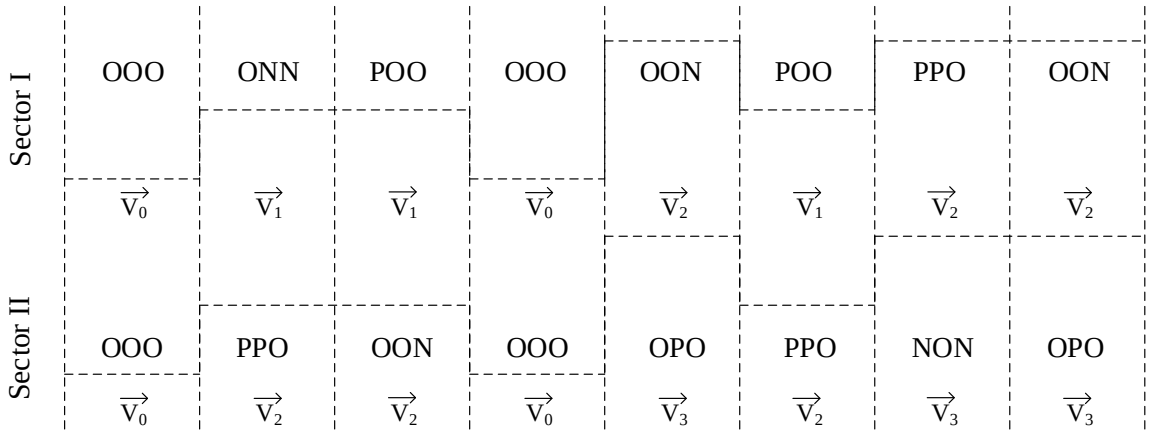


Figure 26 – P/N/O states arranged by the cost function

The algorithm consists of a several stages. Once the pattern is defined by the VSS it can go through P/N/O states arrangement and the desired switching frequency versus DC-link voltage ripple will be calculated. In the first stage it is required to detect N_s that was decided by the control. The next stage is to choose S_L, i.e., how many identical *P* or *N* states can appear in series. At least 2 same states need to be positioned next to each other in order to minimize the switching frequency. After the length of the sequence is determined the algorithm proceeds with sorting the states of the vectors in such a manner that reduces the switching frequency as much as possible. In the next stage, the sequence inverses and will be applied in the forthcoming sector. An average switching frequency is calculated to check if the pattern with newly sorted states satisfies the switching frequency criterion.

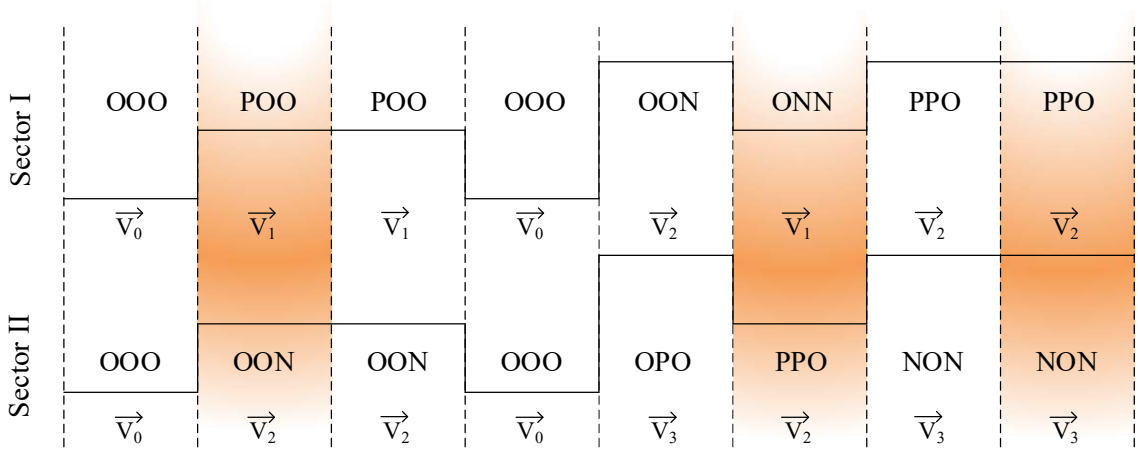


Figure 27 – P/N/O states arranged using an external algorithm

The simulation analysis shows the comparison between the cost function voltage balancing and algorithmic P/N/O balancing. The pattern in Figure 26 was created by the control for the given references and the VSS was applied to shape the spectrum. In Figure 27, the same pattern is depicted, except the states of the small vectors are arranged by the algorithm for switching frequency minimization. The P/N/O sorting resulted in decrease of the switching frequency from 1150 Hz to 850 Hz. The DC-link voltage was set to 10780V and the voltage ripple increased from 80V to 150V.

3.3 Inverter – Side Predictive Control with Load Current Spectrum Shaping

To verify the feasibility of the proposed control scheme, the neutral-point clamped inverter was considered as a case study, and this approach can be easily extended to any other power converter configuration. The NPC inverter presents more challenges compared to a standard two-level voltage source inverter. The NPC inverter needs to maintain constant DC-link capacitor voltages in addition to excellent load current regulation. The control concept for the inverter is presented in Figure 28. It contains MPC which is a converter control block. The other block carries the VSS which provides the correct sampling frequency for the MPC. The proposed VSS algorithm for the NPC inverter is given in Figure 29.

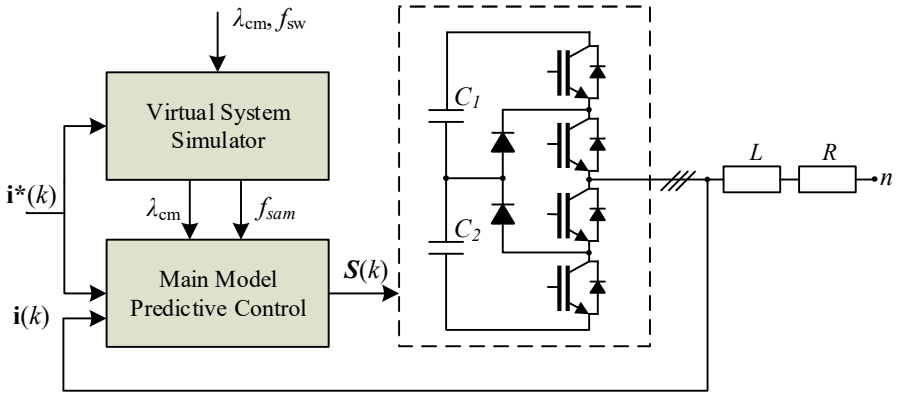


Figure 28 – Inverter side control, VSS with MPC

Upon giving new current reference values to the control, the VSS function will be called to determine an appropriate sampling frequency. The algorithm starts by determining the position of the reference vector and the nearest three vectors. Only these vectors will be used in AMPC during one sample. The sampling frequency shifter starts from previously used sampling frequency and sets a value for AMPC.

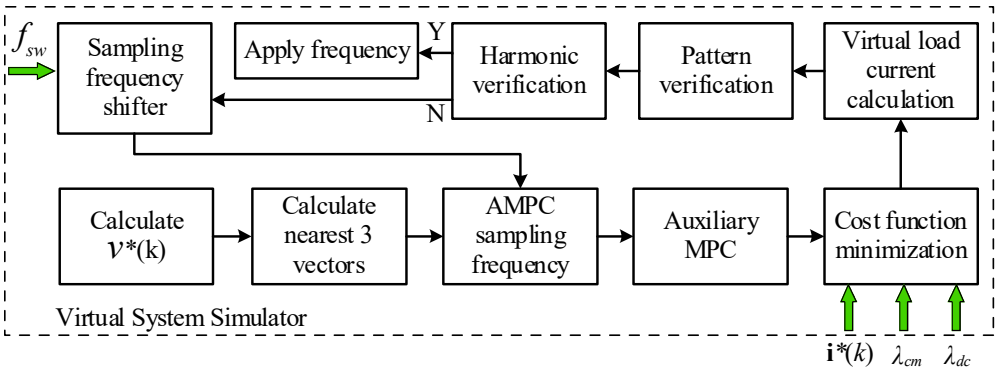


Figure 29 – Internal VSS structure for inverter

Immediately following, the AMPC algorithm is executed together with the virtual load simulator to obtain the virtual load current waveforms. This part of the algorithm repeats itself until enough data points are obtained for the execution of pattern and harmonics verification. First verification stage is to run a pattern verification on the obtained switching vectors. If this block allows further verification, the DFFT will be done to extract the harmonics of interest.

If the switching pattern exists but is formed in such a way that certain unwanted harmonics appear in the spectrum or if the spectrum has spread frequencies, an execution of VSS repeats

itself with the sampling frequency shifted up or down. The process repeats until the right frequency is obtained and the desired harmonics are removed from the spectrum. It should also be noted that in case common-mode voltage needs to be mitigated, the VSS must receive the same request. Therefore, the VSS cost function will add and process another term and the algorithm will obtain f_{sample} which allows fixed switching frequency operation with common-mode voltage mitigation.

The sampling frequency shifter allows certain restrictions and optimizations such as control of switching frequency of the converter or speed optimization of the algorithm. If the switching frequency has to be maintained constant across the entire range of load, the algorithm will target the switching frequency. The VSS does not provide fixed switching frequency operation for all load values, but will select f_{sample} to fix the switching frequency close to the desired value for all operating conditions and load ranges.

Once the value of f_{sample} is known, the algorithm will automatically change the sampling frequency of the MPC to a valid number. It is assumed that the calculations for f_{sample} are going to be completed within one sampling period T_s. That way, the converter will always operate with a presumed switching pattern and the dynamics of the system are preserved as well.

3.3.1 Mathematical Model of NPC Inverter

Considering the unitary vector $\mathbf{a} = e^{j2\pi/3}$ which represents the 120 phase displacement between the phases, the output voltage vector can be defined as

$$\mathbf{v} = \frac{2}{3}(v_{aZ} + \mathbf{a}v_{bZ} + \mathbf{a^2}v_{cZ}) \tag{21}$$

Different switching states will generate different configuration of the three-phase load connected to the DC source. Consequently, 27 switching states and 27 voltage vectors are obtained. Taking into account the definitions of variables from the NPC converter circuit presented in Figure 30, the equations for load current dynamics for each phase can be written as

$$v_{aZ} = L\frac{di_a}{dt} + Ri_a + v_{nZ} \tag{22}$$

$$v_{bZ} = L\frac{di_b}{dt} + Ri_b + v_{nZ} \tag{23}$$

$$v_{cZ} = L\frac{di_c}{dt} + Ri_c + v_{nZ} \tag{24}$$

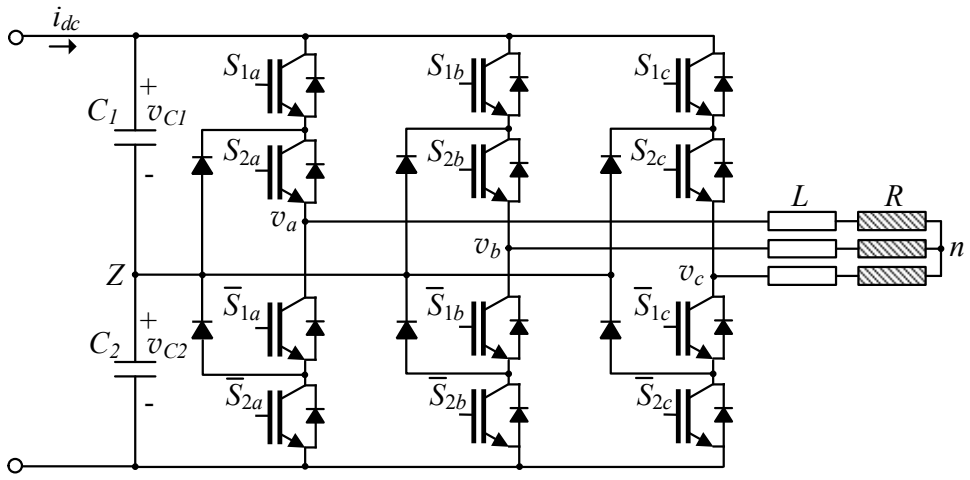


Figure 30 – NPC inverter circuit

By substituting (22)–(24) into (21) a vector equation for the load current dynamics can be obtained:

$$\mathbf{v} = L\frac{d}{dt}\left(\frac{2}{3}(i_a + \mathbf{a}i_b + \mathbf{a}^2 i_c)\right) + R\left(\frac{2}{3}(i_a + \mathbf{a}i_b + \mathbf{a}^2 i_c)\right) + \frac{2}{3}(v_{nZ} + \mathbf{a}v_{nZ} + \mathbf{a}^2 v_{nZ}) \quad (25)$$

Considering the space vector definition for the inverter voltage given by (21), and the following definitions for load current

$$\mathbf{i} = \frac{2}{3}(i_a + \mathbf{a}i_b + \mathbf{a}^2 i_c) \quad (26)$$

and assuming the last term of (25) equal to zero

$$\frac{2}{3}(v_{nZ} + \mathbf{a}v_{nZ} + \mathbf{a}^2 v_{nZ}) = 0 \quad (27)$$

then the load current dynamics can be described by the vector differential equation

$$\mathbf{v} = L\frac{di}{dt} + R\mathbf{i} \quad (28)$$

where $\mathbf{v}$ is the voltage vector generated by the inverter and $\mathbf{i}$ is the load current vector.

3.3.2 Discrete-Time Model for Prediction

If the load current derivative *di/dt* is replaced by a forward Euler approximation, that is, if the derivative is approximated as follows:

$$\frac{d\boldsymbol{i}}{dt} \approx \frac{\boldsymbol{i}(k+1) - \boldsymbol{i}(k)}{T_s} \quad (29)$$

and then substituted in (28), we obtain an expression that allows prediction of the future load current at time *k+1*. This expression is

$$\mathbf{i}^{p}(k+1) = \left(1 - \frac{RT_s}{L}\right)\mathbf{i}(k) + \frac{T_s}{L}\mathbf{v}(k) \tag{30}$$

3.3.3 Cost Function Evaluation

The future values of load currents and voltages in the capacitors are predicted for 27 switching states in a general case and generated by the inverter. For this purpose, it is necessary to measure present load currents and voltages in the capacitors. After obtaining the predictions, a cost function *g* is evaluated for each switching state.

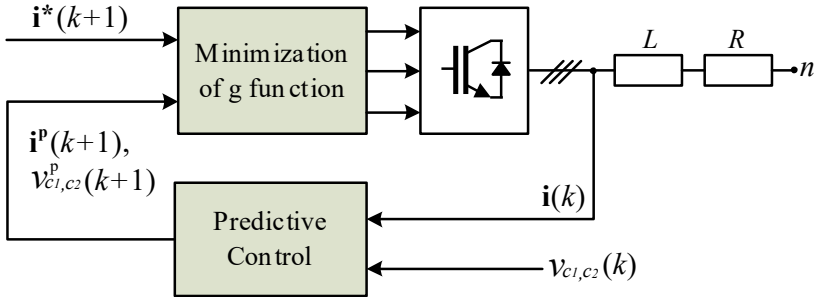


Figure 31 - Predictive current control method for the NPC inverter

The switching state that minimizes the cost function is selected and applied during the next sampling period. The predictive control scheme for the NPC inverter is shown in Figure 31. The control requirements for the NPC inverter are:

- Load current reference tracking
- DC-link capacitor voltages balance
- Reduction of the switching frequency

These requirements can be formulated as a cost function to be minimized. The cost function for the NPC inverter has the following composition:

$$g = |i_\alpha^* - i_\alpha^P| + \left|i_\beta^* - i_\beta^P\right| + \lambda_{DC}|v_{c1}^P - v_{c2}^P| \tag{31}$$

where the first two terms are the load current errors in orthogonal coordinates and the third term in the cost function measures the difference in the predicted values of the DC-link capacitor

voltages. The reduction of switching frequency can be obtained either through changing N_s or by using P/N/O balancing algorithm.

3.3.4 Capacitor Voltage Balancing

As it is already known, an NPC inverter may have neutral point (*NP*) balancing issues, which are caused by the current that flows back to the *NP*. This problem arises due to tolerances of the converter components and asymmetries of gating commands of the switches and leads to a continuous unsymmetrical power flow between the positive and negative DC-link. The two DC-link voltages may deviate from each other continuously and may finally destroy the components.

Model predictive controls allows balancing of the DC capacitors to be done in a very elegant way. Starting from the capacitor differential equations

$$\frac{dv_{c1}}{dt} = \frac{1}{C} i_{c1} \tag{32}$$

$$\frac{dv_{c2}}{dt} = \frac{1}{C} i_{c2} \tag{33}$$

and by approximating the derivatives as

$$\frac{dv_{cx}}{dt} \approx \frac{v_{cx}(k+1) - v_{cx}(k)}{T_s} \tag{34}$$

the following discrete-time equations are obtained:

$$v_{c1}^{P}(k+1) = v_{c1}(k) + \frac{1}{C} i_{c1}(k) T_s \tag{35}$$

$$v_{c2}^{P}(k+1) = v_{c2}(k) + \frac{1}{C} i_{c2}(k) T_s \tag{36}$$

Currents $i_{c1}(k)$ and $i_{c2}(k)$ depend on the switching state of the inverter and are calculated using the following expressions:

$$i_{c1}(k) = i_{dc}(k) - H_{1a} i_a(k) - H_{1b} i_b(k) - H_{1c} i_c(k) \tag{37}$$

$$i_{c2}(k) = i_{dc}(k) - H_{2a} i_a(k) - H_{2b} i_b(k) - H_{2c} i_c(k) \tag{38}$$

where variables H_{1x} and H_{2x} depend on the switching states and are defines as:

$$H_{1x} = \begin{cases} 1 \text{ if } S_x = "+" \\ 0 \text{ otherwise} \end{cases} \tag{39}$$

$$H_{2x} = \begin{cases} 1 \text{ if } S_x = " - " \\ 0 \text{ otherwise} \end{cases} \tag{40}$$

where $x = a,b,c$.

The cost function can then be modified to include the balancing term $\lambda_{dc}|V_{c1}^{P} - V_{c2}^{P}|$ where λ_{dc} coefficient has a certain range of values.

3.3.5 Common-mode Voltage Reduction

The common-mode voltage can be mitigated or completely eliminated by adding V_{cm} term into cost function which considers common-mode voltage with dedicated appropriate value of the weighting factor λ_{cm}. The common-mode voltage is defined as:

$$v_{cm} = \frac{v_{an} + v_{bn} + v_{cn}}{3} \tag{41}$$

where the voltages V_{an}, V_{bn} and V_{cn} are phase to neutral voltages. The cost function to consider V_{cm} is given as:

$$g = |i_{\alpha}^{*} - i_{\alpha}^{P}| + \left|i_{\beta}^{*} - i_{\beta}^{P}\right| + \lambda_{cm}\,|v_{cm}^{P}(k)| \tag{42}$$

3.3.6 Simulation Results with High Power Inverter

To verify the proposed theory the inverter was simulated using Matlab/Simulink. The following simulations verify the steady-state and dynamic response, common-mode voltage mitigation and switching frequency regulation using P/N/O state balancing with high power inverter. The setup parameters are given in Table III.

Table III – Simulation setup parameters for high power inverter

Converter Parameter	Value SI	Value pu
Converter rating	5 (MVA)	1
DC-Link voltage	10784 (V)	2.45
DC-Link capacitance	1000 (μF)	3.65
Output frequency	50 (Hz)	1
Filter inductance	16.1 (mH)	0.43
Load resistance	10.5 (Ω)	0.9

3.3.6.1 Steady-state and transient characteristics

Multilevel converter dominant area of operation is in high power applications. Therefore, a high power NPC inverter was simulated to verify the control actions similar to real-application environment. The steady-state response of the inverter controlled with VSF-MPC is provided in Figures 32 and 33.

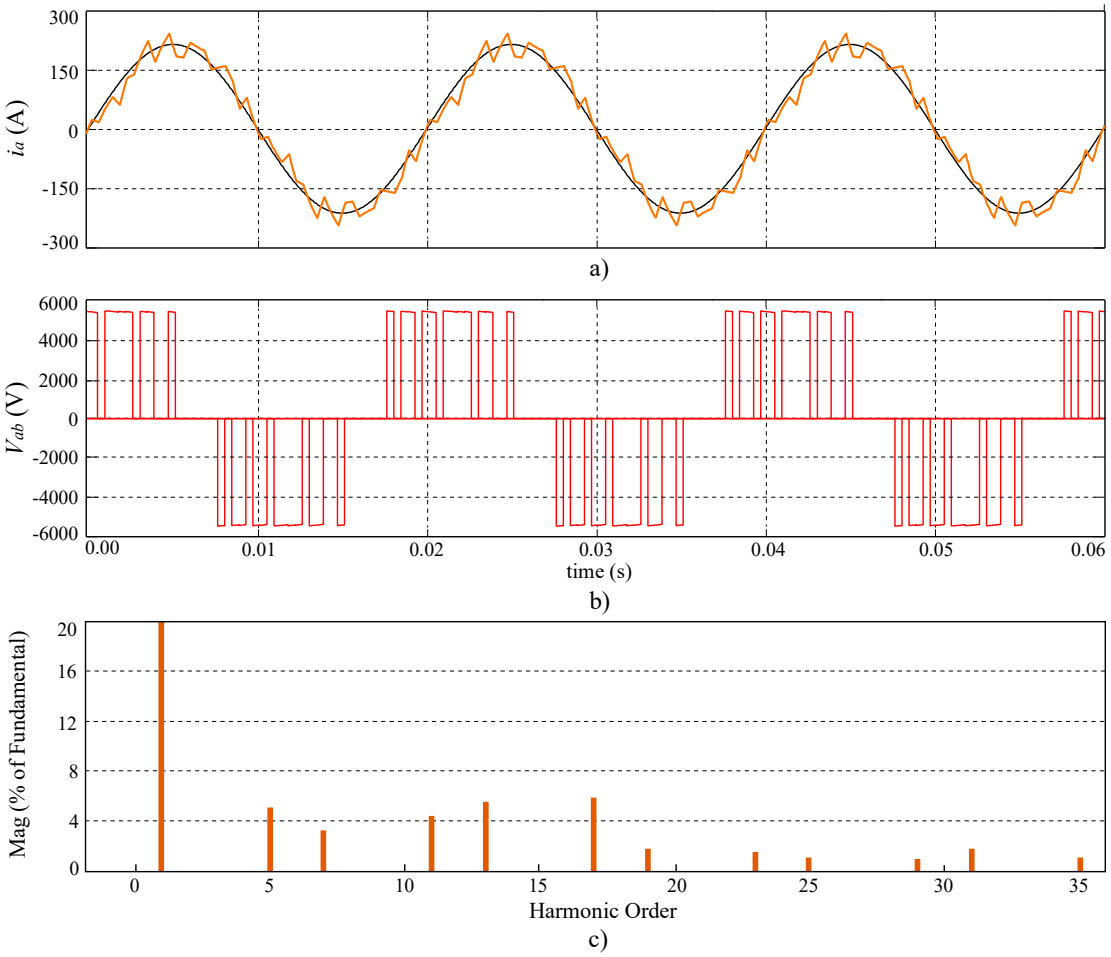


Figure 32 - Steady-state response at 50 Hz: a) i_a, b) V_{ab} and c) harmonic spectrum

Figure 32 presents the inverter load current waveform generated at a fundamental frequency of 50 Hz, corresponding line-to-line voltage and current harmonic spectrum, while the inverter operates at 0.4 pu of a rated current. It can be observed that for given operating conditions, VSS achieves fixed switching frequency operation and a half-wave symmetry, leading to SVM-based shape of spectrum with even-order harmonic elimination. A different fundamental frequency of 25 Hz is further selected to confirm the control ability to properly handle fundamental frequency reference changes. The results are provided in Figure 33. The switching frequency was kept

constant leading to doubling the number of switchings per fundamental cycle in the second case. However, VSF-MPC successfully achieves fixed switching frequency operation with spectrum shaping. For both operating conditions it can be stated that current waveforms do not display cycle to cycle oscillations, which means the switching frequency is fixed for given operating conditions. Also, it is easily noticed that both current and voltage waveforms are half-wave symmetrical leading to even-order harmonic elimination. Thus, Figures 32 and 33 confirm steady-state operation for VSF-MPC with high power inverter.

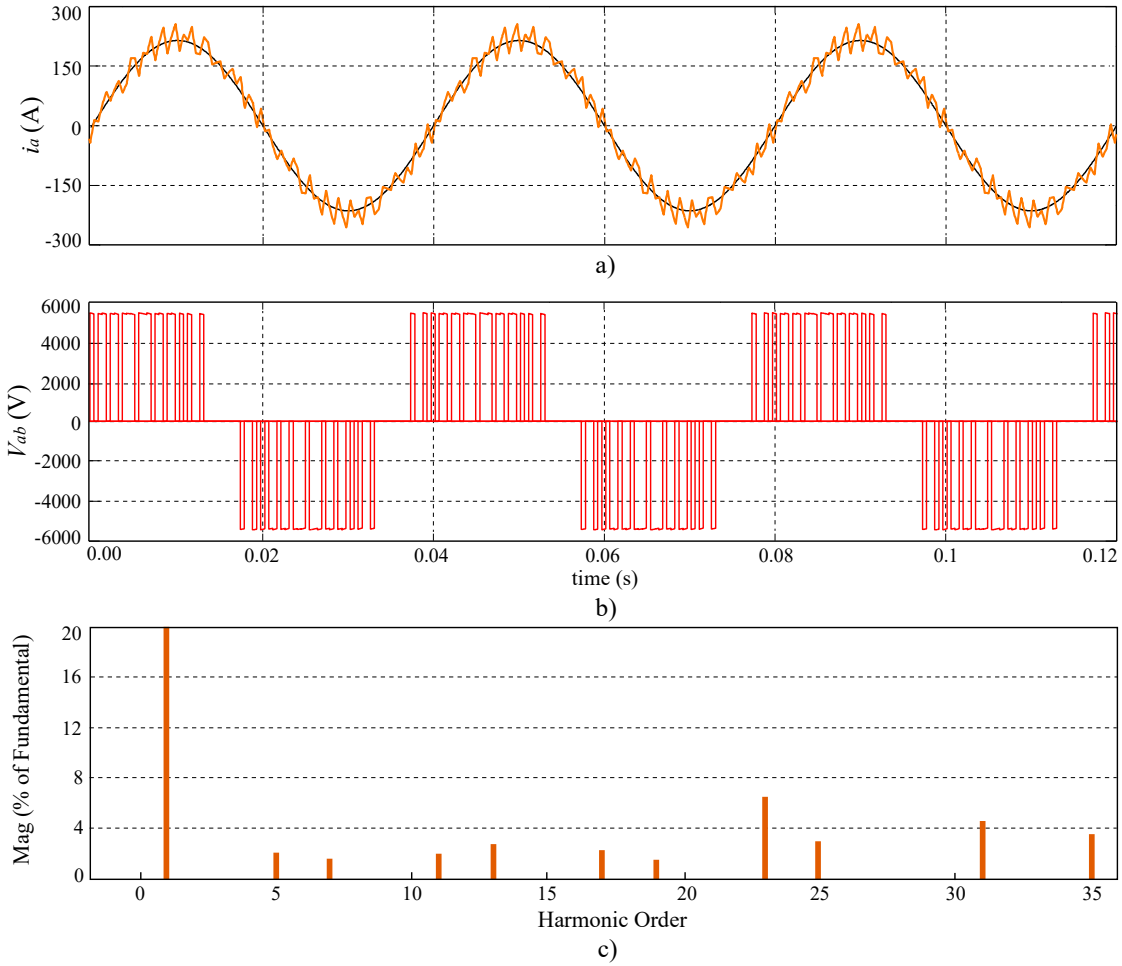


Figure 33 - Steady-state response at 25 Hz: a) i_a, b) V_{ab} and c) harmonic spectrum

The same setup was also tested with a step change in current reference and the results are presented in Figure 34. This test verifies the VSF-MPC with VSS using current step change from 0.4 pu to 0.8 pu. After receiving new reference values, the VSS successfully calculated new sampling frequency, in such way maintaining constant switching frequency operation. This can also be noticed by observing the capacitor voltages, which display symmetrically balanced values

before and after the transient. During transient, there is a very short drift in the DC-link voltages due to sudden relatively large current step. However, this behaviour was properly corrected by the control.

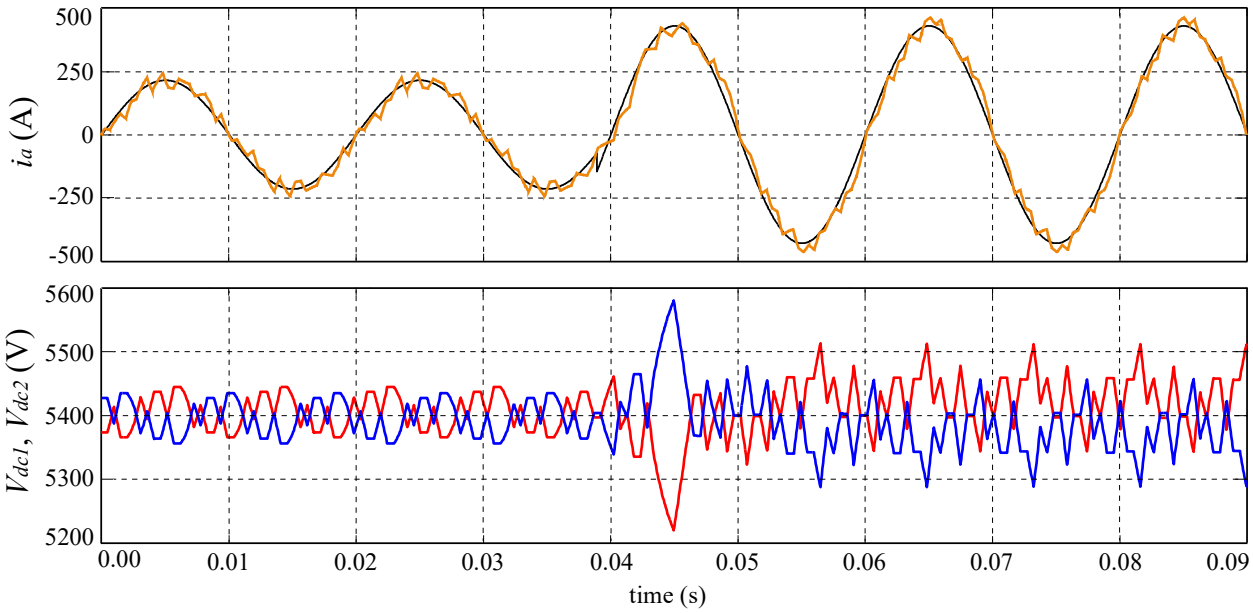


Figure 34 – Transient response of a high power NPC inverter

3.3.6.2 P/N/O Voltage Balancing

This test confirms the ability of the control to achieve proper DC-link voltage balancing when switched from auto λ_{dc} balancing through cost function to P/N/O balancing using an external algorithm. Figure 35 presents and verifies that the switching frequency can be adjusted through the selection of P/N/O states. At t=0.03 s λ_{dc} value was changed from 0.01 to 0 at. The auxiliary algorithm chooses P/O/N states such that the capacitor voltages are balanced even though the cost function omits this task. Due to the transfer of capacitor voltages balancing to the auxiliary controller, the switching frequency was changed from 1050Hz to 700Hz, and this can be noticed by looking into the inverter output voltage waveform with respect to the mid-point of DC-bus (v_{az}).

The ripple in the capacitor voltages is also increased; however their mean value is equal to half the total DC-bus voltage. The ripple in the load current waveform is not affected by this phenomenon, because the overall control scheme forces the load current to follow predefined

harmonic profile. This test verifies the fixed switching frequency operation of the NPC inverter and the ability to influence the switching frequency both ways.

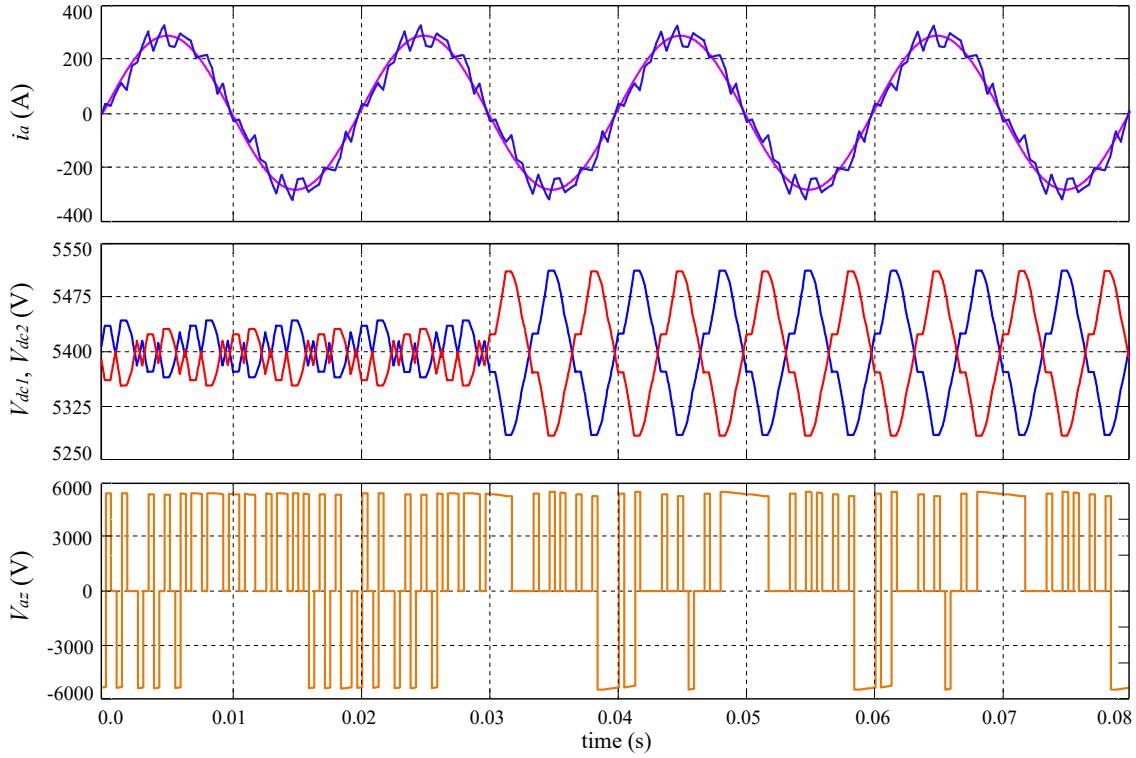


Figure 35 – DC-link voltage balancing by switching from auto λ_{dc} balancing to P/N/O

3.3.6.3 Common-mode Voltage Elimination

Figure 36 shows the effectiveness of the proposed control algorithm in mitigation of CMV in an NPC inverter and also simultaneous elimination of even-order harmonics. The inverter was initially running with a switching frequency of 1050Hz, and the cost function considered the load current control, balancing of capacitor voltages and even-order harmonic elimination. At t=0.035 s, the weighting factor λ_{cm} was changed from 0 to 0.1, mitigating the CMV to a few volts by choosing only medium voltage vectors and zero vector.

To facilitate such procedure, the switching frequency of the inverter decreases to 600 Hz. Due to use of medium vectors and zero vector only, the load current THD has increased slightly. However, the current ripple shape is still symmetrical to eliminate the even-order harmonics and inter-harmonics. Load current follows the predefined harmonic profile and thus the even-order and inter-harmonics are eliminated completely despite the changes in λ_{cm} value. This test verifies the

effectiveness of the proposed scheme in eliminating even-order harmonics and CMV simultaneously.

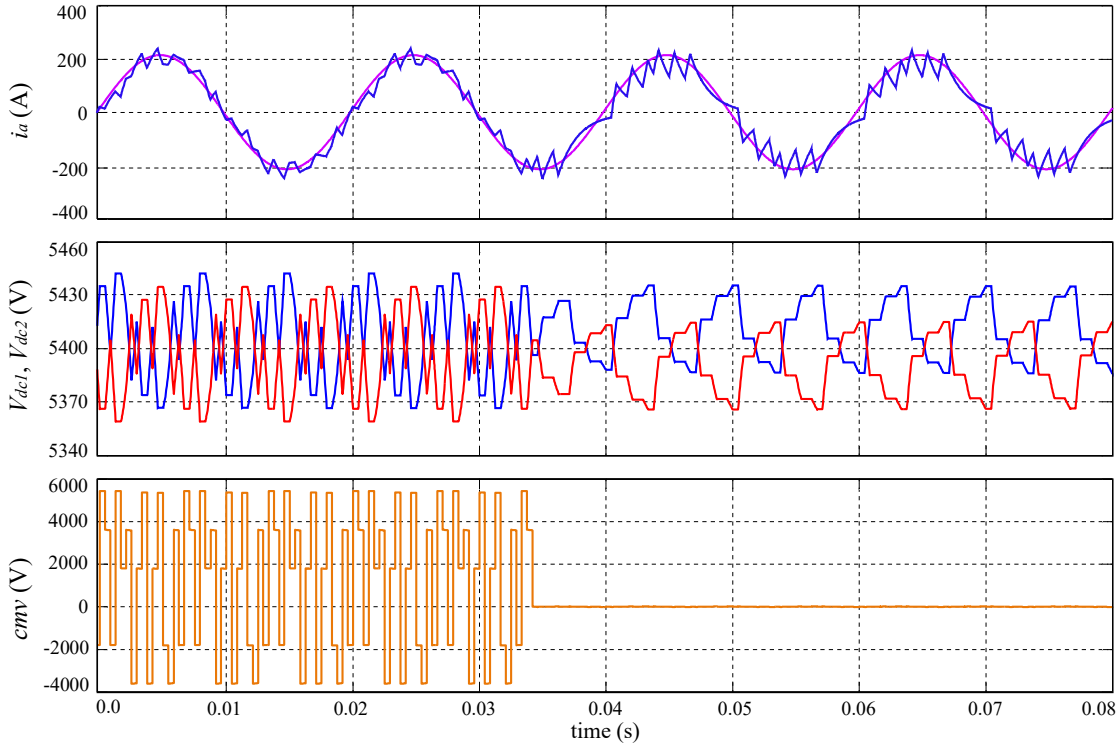


Figure 36 – Common-mode voltage elimination through cost function minimization

In this case the voltage balancing of the DC-link capacitors in not achievable. However, not only this algorithm achieves balanced voltages in steady state, but the overall control loop displays a self-balancing effect as described in [49]. The strength of the self-balancing effect depends on the sampling frequency, but is independent of the power rating of the system assuming the per-unit impedance of the load is constant.

3.4 Rectifier – Side Predictive Control with Grid Current Spectrum Shaping

If the predictive control is selected as a control method for the rectifier, spread spectrum due to variable switching frequency is not suitable for a grid connection. Every converter interacting directly with the grid must respect grid code guidelines such is IEEE Std 519-1992, in terms of harmonic profile or Total Demand Distortion (TDD).

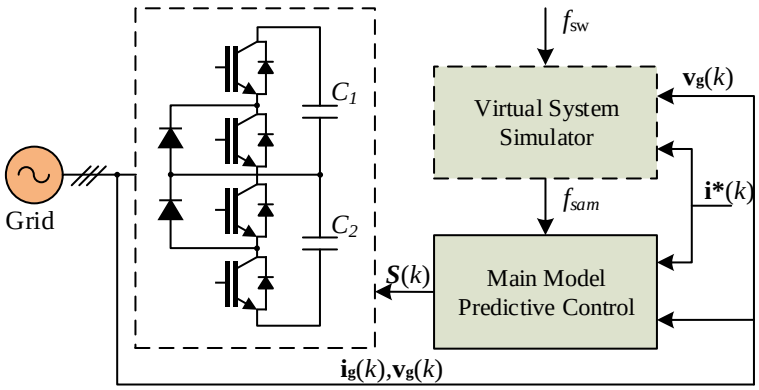


Figure 37 - Rectifier side control, VSS with MPC

In addition, to minimize the impact on the grid, rectifiers may use more complex filters, such as *LCL* filter. Variable switching frequency produces various harmonic frequencies in the spectrum which may induce oscillation and damage the equipment. Therefore, fixed switching frequency operation is of a great significance for proper operation of rectifiers and minimal negative impact on the grid.

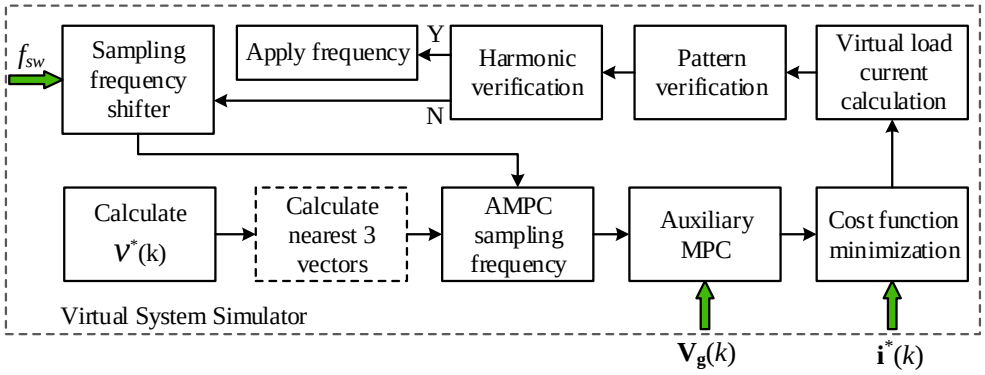


Figure 38 – Internal VSS structure for rectifier

The proposed control system for the rectifier is presented in Figure 37. The concept is similar to previously used method to control the inverter, with a few modification required by the rectifier configuration. In addition to previously considered in VSS, it is now required to consider the grid voltage and frequency as well. The frequency of the grid is an important parameter which has to be determined precisely in order for the sampling frequency to synchronize properly. The grid frequency if fairly constant but the VSS monitors its value using an additional PLL block. The other parameter used to determine the correct f_{sample} is the grid voltage. The VSS internal structure is presented in Figure 38 with the inputs adjusted for rectifier operation.

3.4.1 Mathematical Model of NPC AFE Rectifier

Based on the circuit shown in Figure 30, the equations for each phase can be written as:

$$v_{sa} = L\frac{di_a}{dt} + Ri_a + v_{aZ} - v_{nZ} \tag{43}$$

$$v_{sb} = L\frac{di_b}{dt} + Ri_b + v_{bZ} - v_{nZ} \tag{44}$$

$$v_{sc} = L\frac{di_c}{dt} + Ri_c + v_{cZ} - v_{nZ} \tag{45}$$

Then, considering the space vector definition for the grid voltage

$$\mathbf{v_s} = \frac{2}{3}(v_{sa} + \mathbf{a}v_{sb} + \mathbf{a}^2 v_{sc}) \tag{46}$$

where $\mathbf{a} = e^{j2\pi/3}$, and by substituting (43)-(45) into (46) the vector equation for the grid current dynamics can be obtained as

$$\mathbf{v_s} = L\frac{d}{dt}\left(\frac{2}{3}(i_a + \mathbf{a}i_b + \mathbf{a}^2 i_c)\right) + R\left(\frac{2}{3}(i_a + \mathbf{a}i_b + \mathbf{a}^2 i_c)\right)$$
$$+\frac{2}{3}(v_{aZ} + \mathbf{a}v_{bZ} + \mathbf{a}^2 v_{cZ}) - \frac{2}{3}(v_{nZ} + \mathbf{a}v_{nZ} + \mathbf{a}^2 v_{nZ}) \tag{47}$$

The last term of (47) is equal to zero

$$\frac{2}{3}(v_{nZ} + \mathbf{a}v_{nZ} + \mathbf{a}^2 v_{nZ}) = 0 \tag{48}$$

The input current dynamics equation (47) can be simplified by considering the following definitions for the grid current vector and the voltage vector generated by the AFE:

$$\mathbf{i} = \frac{2}{3}(i_a + \mathbf{a}i_b + \mathbf{a}^2 i_c) \tag{49}$$

$$\mathbf{v}_{\text{afe}} = \frac{2}{3}(v_{aZ} + \mathbf{a}v_{bZ} + \mathbf{a}^2 v_{cZ}) \tag{50}$$

Voltage $\mathbf{V}_{\text{afe}}$ is determined by the switching state of the converter and the DC-link voltage, and can be expressed by the equation

$$\mathbf{v}_{\text{afe}} = \mathbf{S}_{\text{afe}} * V_{dc} \tag{51}$$

where V_{dc} is the DC-link voltage and S_{afe} is the switching state vector of the rectifier, defined as

$$\mathbf{S}_{\text{afe}} = \frac{2}{3}(S_1 + \mathbf{a}S_2 + \mathbf{a}^2 S_3) \tag{52}$$

where S_1, S_2, and S_3 are the switching states of each rectifier leg, and can take value of 0 if S_x is off, or 1 if S_x is on (x = 1, 2, 3).

The input current dynamics equation (47) can be rewritten in the stationary $\alpha\beta$-frame as the following vector equation:

$$L\frac{d\mathbf{i}}{dt} = \mathbf{v}_s - \mathbf{v}_{\text{afe}} - R\mathbf{i} \tag{53}$$

where $\mathbf{i}$ is the input current vector, $\mathbf{v}_s$ is the supply line voltage and $\mathbf{v}_{\text{afe}}$ is the voltage generated by the converter.

3.4.2 Discrete-time Model of NPC AFE Rectifier

The predicted current is calculated using the discrete-time equation obtained from discretizing (53)

$$\mathbf{i}^{\boldsymbol{p}}(k+1) = \left(1 - \frac{RT_s}{L}\right)\mathbf{i}(k) + \frac{T_s}{L}(\mathbf{v_s}(k) - \mathbf{v}_{\text{afe}}(k)) \tag{54}$$

for a sampling time T_s. Discretization is done by approximating the derivative as the difference over one sampling period as considered in the previous part with the NPC converter.

3.4.3 Rectifier Simulation Results

In a back-to-back system, the current reference for the rectifier is usually provided by the PI controller in charge of the DC-link voltage regulation and by required load power on inverter side. In order to verify the proposed concept, the rectifier with L filter was selected as a study case and controlled with the VSS. The current reference was manually selected according to system parameters which are the same as in case of inverter. The results for the investigated system are presented in Figure 39. The NPC rectifier is drawing 0.4 pu of active power from the grid respecting zero reactive power reference.

It can be noticed that the current is in phase with the grid voltage, thus taking power at unity power factor. Furthermore, the voltages at the DC-link side are properly balanced. The current is half-wave symmetrical and therefore does not contain even-order harmonics, which can be seen from an associated harmonic spectrum of grid current waveform given in Figure 39c).

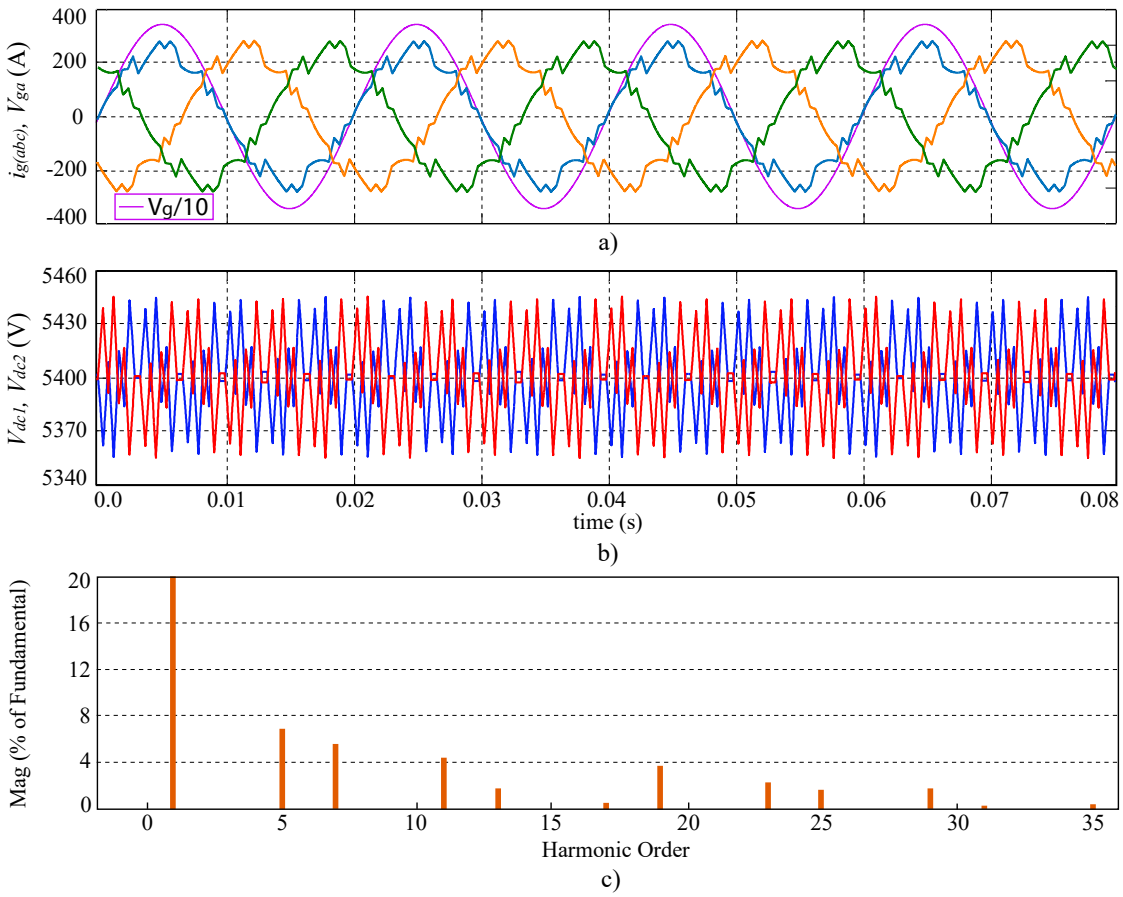


Figure 39 – Rectifier operation: a) grid currents, b) DC-link capacitor voltages, c) harmonic spectrum

3.5 Switching Frequency Targeting versus Number of Samples

It is known that the inverter switching frequency changes with load current ranging from low to high values. In classical fixed sampling frequency FSC-MPC, the inverter switching frequency varies with the load current. Figure 40 shows the proposed VSF-MPC forcing constant sampling rate, where N_s was targeted for 14.

The cost function in this case includes load regulation term and capacitor voltage balancing through λ_{dc}. At certain operating points, the requested sampling frequency cannot provide either even-order harmonic elimination or fixed switching frequency operation. Thus, the sampling rate is changed by the VSS to first nearby sampling frequency at which primary control objective can be achieved. N_s could either increase (orange line) or decrease (blue line) depending on the VSS settings. An increase in N_s would naturally raise an inverter switching frequency while lowering N_s will decrease f_{sw}.

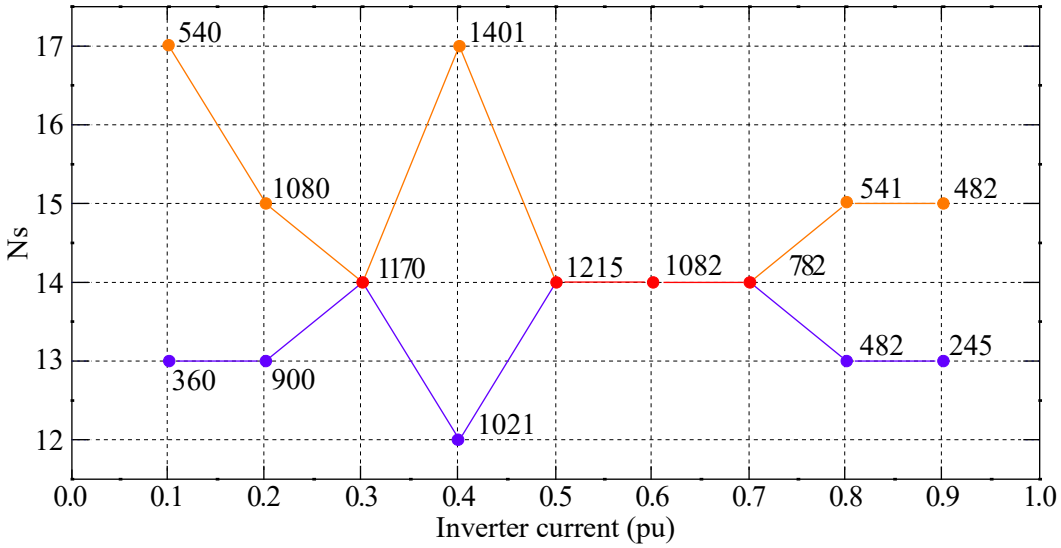


Figure 40 – N_s versus inverter switching frequency targeting N_s = 14

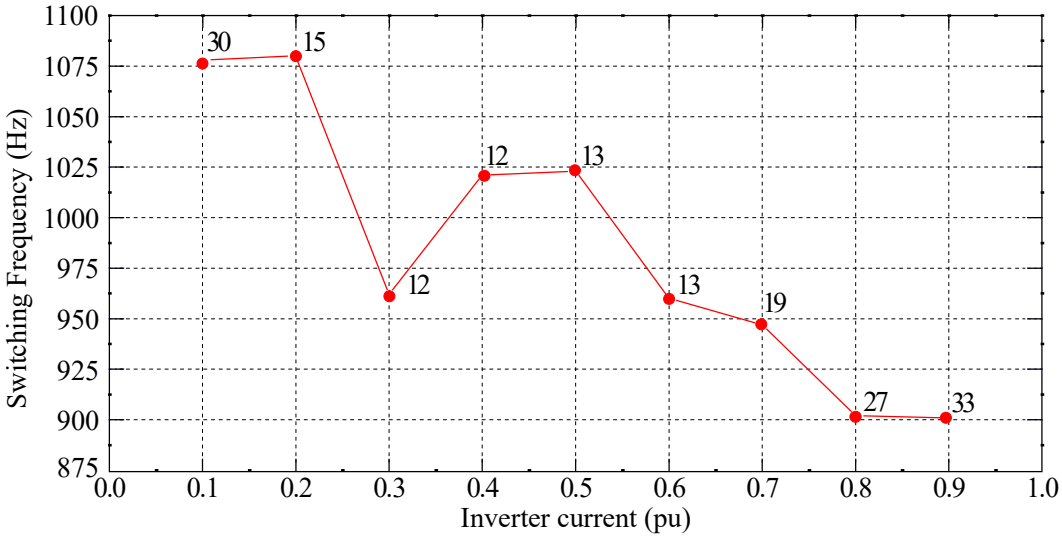


Figure 41 – N_s versus inverter switching frequency targeting f_{sw} = 1000 Hz

On the other hand, Figure 41 presents the control behavior when the inverter switching frequency was targeted at 1000 Hz within an allowed range of 10 % of fluctuation around the targeted value. The VSS was configured to automatically adjust the sampling rate to meet the requested criterion while maintaining fixed switching frequency with even-order harmonic elimination. Figures 40 and 41 show the flexibility of the proposed control scheme to fulfill various objectives and simultaneously shape the harmonic spectrum.

3.6 Summary

In this chapter a novel VSF-FCS-MPC scheme for inverter and rectifier is proposed. The technique employs variable sampling frequency and a virtual system simulator to determine the appropriate sampling frequency for spectrum shaping with even-order harmonic elimination. To verify the proposed method, an NPC converter is considered as a study case. Through simulations it has been proved that the spectrum can be shaped with eliminations of even-order harmonics in addition to the current regulation and balancing of DC-link capacitor voltages. The strategy is further verified with common-mode voltage mitigation, as an important aspect in motor drives. From the grid side prospective, simulation were performed with the rectifier as well, which confirms the control is able to maintain requested active power flow with simultaneous even-order harmonic elimination and DC-link voltage balancing.

CHAPTER 4
DSP IMPLEMENTATION AND EXPERIMENTAL VERIFICATION

4.1 Introduction

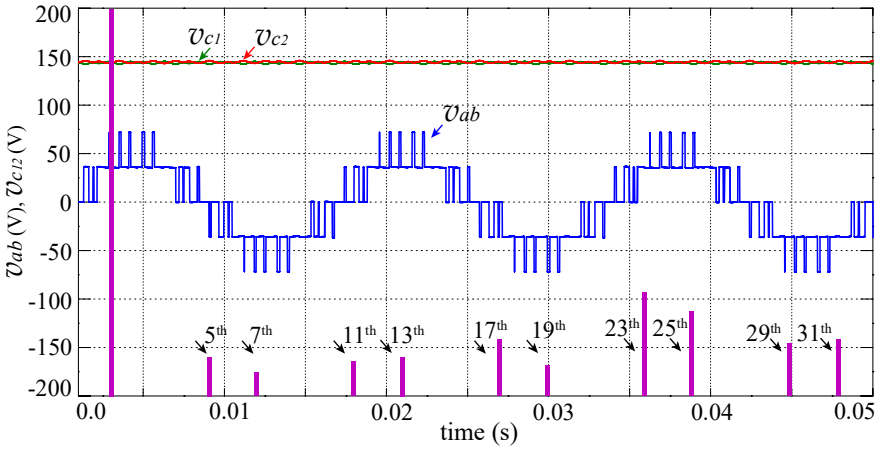
The proposed VSF-FCS-MPC control scheme has been experimentally verified with the laboratory NPC inverter and compared with FSF-FCS-MPC and conventional control methods, in this case, SVM. Classical current control techniques for a three level VSI use PI regulators to eliminate the steady-state error and a modulation stage to generate the gating signals. Even though SVM provides fixed switching frequency operation regardless of operating conditions, the design complexity is no match to its predictive counterpart. The complexity of the design and tuning process for SVM increase even further when another PI loop is added to balance the capacitor voltages. In FCS-MPC, on the other hand, current control and capacitor voltage balancing objectives are defined in a single cost function. Simulation and experimental results for low-power setup are both presented in this chapter for easier comparison, showing dynamic and steady-state performances of NPC inverter. More specifically, the objective was to experimentally assess the performance of the proposed technique in terms of percentage total harmonic distortion (%THD) and average switching frequency under various load and reference conditions. This chapter also covers the DSP implementation of FSF-MPC using fixed-speed digital processor.

4.2 Inverter Simulation Results with Low Power

A low power setup was simulated using MATLAB-Simulink to observe the behavior of the control when multiple objectives need to be fulfilled, such as current control, capacitor voltage balancing and spectrum shaping. The parameters of the system are given in Table IV.

Table IV – Setup parameters for low power inverter

Converter Parameter	Value SI	Value pu
Converter rating	3.6 (kVA)	1
DC-Link voltage	370 (V)	3.08
DC-Link capacitance	1000 (μF)	4.52
Output frequency	60 (Hz)	1
Filter inductance	7.5 (mH)	0.24
Load resistance	11 (Ω)	0.92



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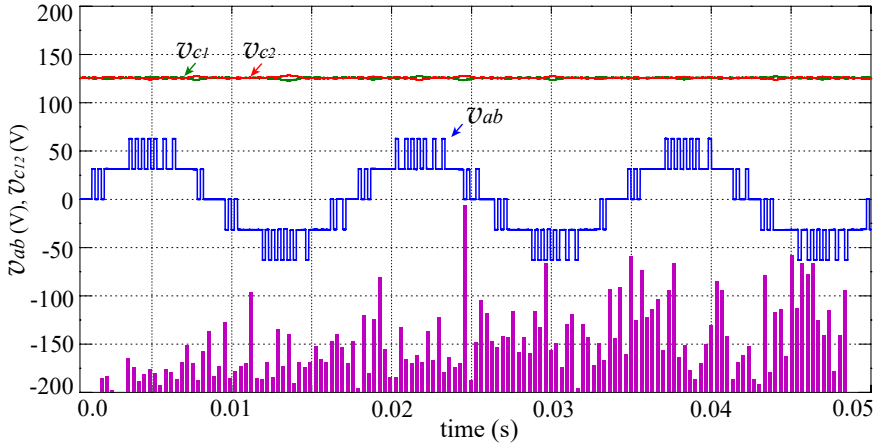

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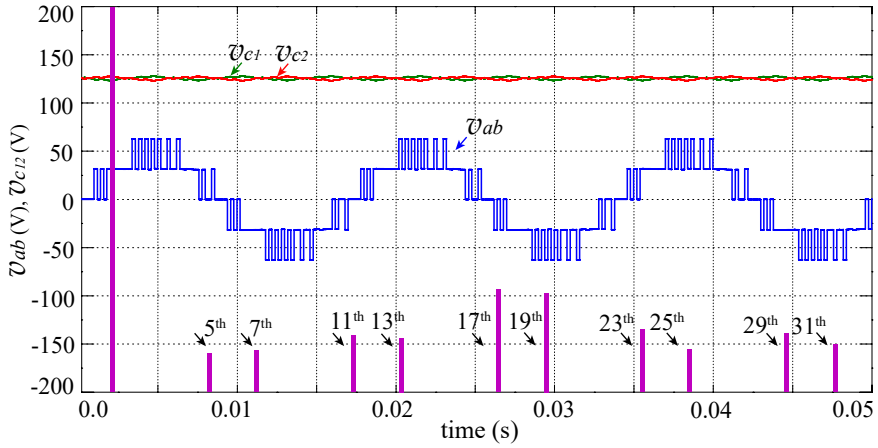
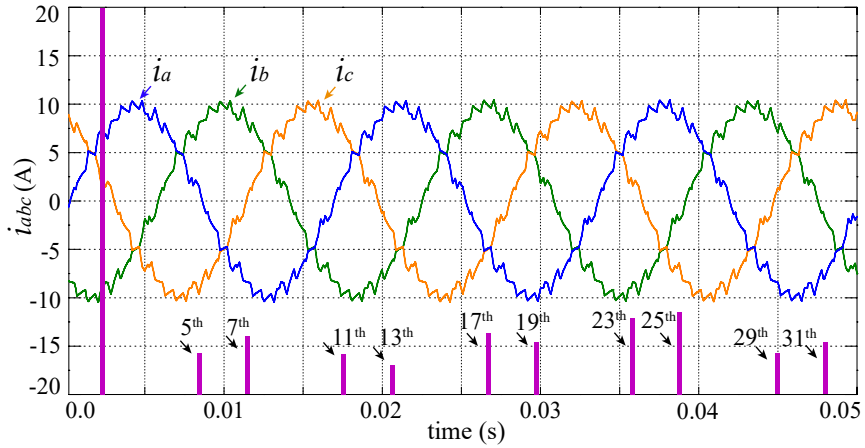
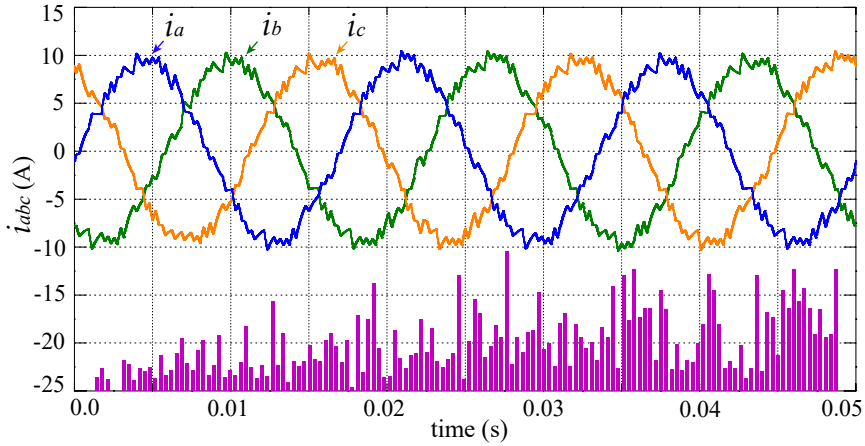


c)

Figure 42 - Steady-state comparison of line-to-line voltages: a) SVM; b) FSF-MPC; c) VSF-MPC



a)



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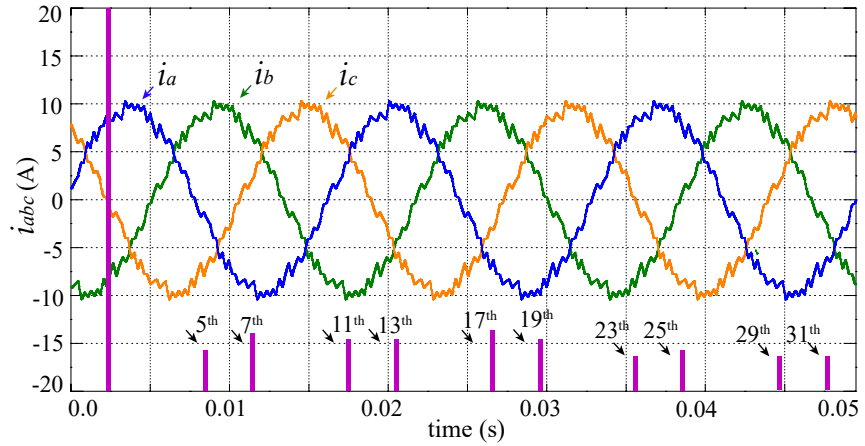
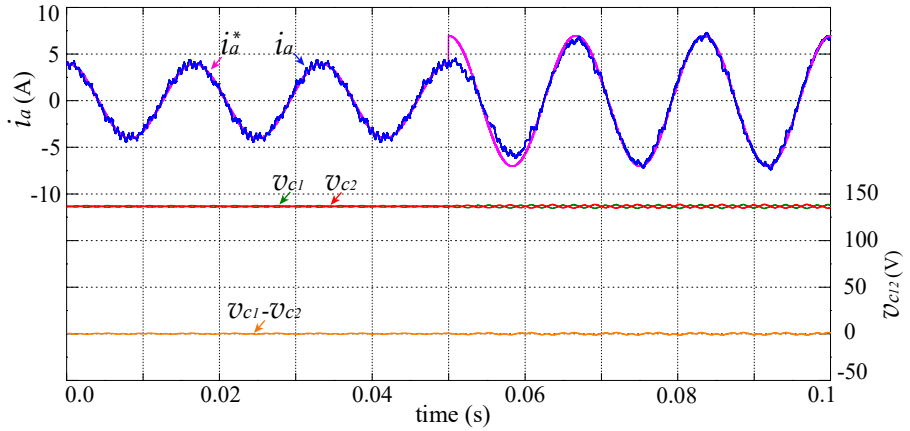
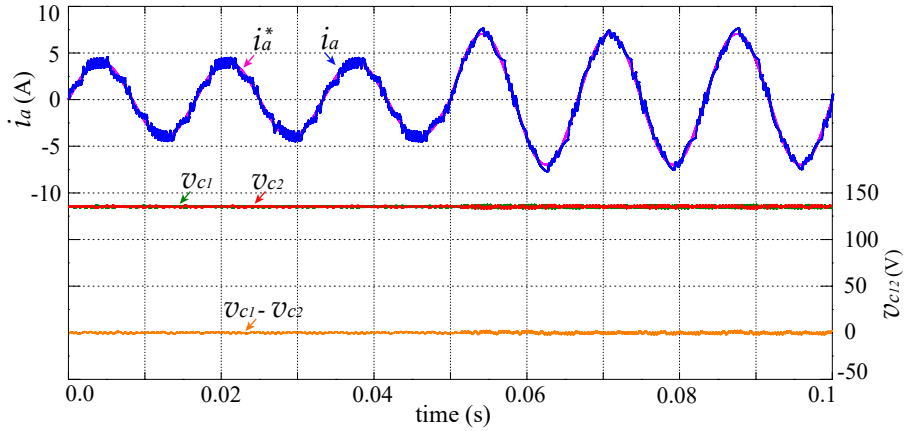


c)

Figure 43 - Steady-state comparison of 3-phase currents: a) SVM; b) FSF-MPC; c) VSF-MPC



a)



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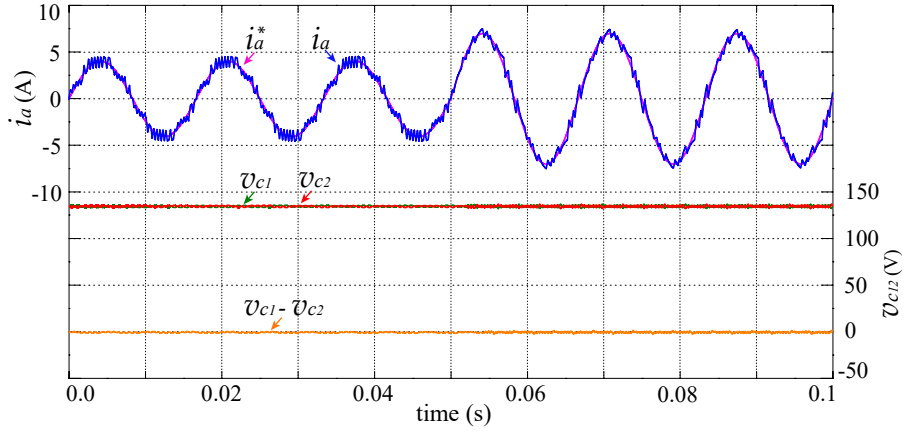


c)

Figure 44 - Transient response comparison: a) SVM; b) FSF-MPC; c) VSF-MPC

The simulation results provided in Figures 42-44 compare SVM current control with FSF- and VSF-MPC. Simulated waveforms in Figure 42 represent the inverter line-to-line voltage and DC-link voltages during steady-state operation. The corresponding voltage spectrum is provided in each figure. The graph in Figure 42a) presents SVM operation of NPC inverter. As expected, SVM operates with fixed-switching frequency and due to implemented even-order harmonic elimination achieves shaped spectrum including only the following harmonics: 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd}, 25^{th}, 29^{th} and 31^{st}. Figure 42b) presents FSF-MPC operating at constant sampling rate. It displays common MPC issue such as spread-spectrum due to variable switching frequency. The control is able to properly balance the DC-link voltages. However, line-to-line voltage contains various harmonic frequencies. The graph in Figure 42c) displays variable sampling frequency method. The proposed method fully removes even-order harmonics and achieves spectrum shape similar to SVM in terms of individual harmonic frequencies. Capacitor voltages are properly balanced during operation.

Moreover, Figure 43 presents the inverter 3-phase steady-state current waveforms for all three simulated control schemes, with dedicated spectrum profiles. In Figure 43a), SVM operation is presented with fixed switching frequency operation. Similar to Figure 42b), 3-phase currents generated by fixed sampling frequency MPC are pictured in Figure 43b). This kind of operation leads to variable switching frequency producing spread harmonic spectrum. Finally, in Figure 43c), the proposed VSF-MPC algorithm achieves spectrum shaping while simultaneously accomplishing reference current tracking and capacitor voltage balancing.

The dynamic performances are further analyzed in Figure 44. The graph in Figure 44a) shows SVM response to a step change in current reference. Due to linear control and fairly complex modulation stage a considerable time is required to achieve steady-state operation compared to MPC response time. Both MPC techniques reveal superior predictive response performances against SVM. However, VSF-MPC establishes shaped harmonic spectrum after transient which can be observed in current waveform shape. It should also be stated that all three control methods can properly balance the capacitor voltages during transients and achieve reference current tracking with zero error. Simulation results obtain above are experimentally verified and presented in the following sections.

4.3 DSP Implementation

The control algorithm has been implemented on the laboratory dSPACE DS1103 control board with a PPC750GX digital processor clocked at 1 GHz. An internal architecture of the CPU

supports 3 hardware interrupts controlled by two 32-bit counters and one 64-bit counter. The resolution of the counters is 15 ns and 30 ns according to the system bus clock to CPU clock ratio. All three counters are actively monitored with each system clock and their values are actively compared with counter compare registers.

The algorithm has been written inside an interrupt routine and all calculations, transformations and control equations are executed once with each interrupt cycle. However, the VSS part of the algorithm in charge of finding f_{sample} is implemented as a function which is called whenever there is a change in input parameters. The DSP supports complex task priority management. Since controlling the primary cost function objectives is a pivotal role, the VSS function was ranked second in the priority queue. This is required from the control point of view and the associated Forward-Euler discretization for proper operation. However, the code execution is optimized for fast calculation, thus all predictions can be completed in one T_s. If under certain conditions the calculation time for f_{sample} would take longer than one T_s, the transient response of the system would not be affected because the MPC has the highest priority in an interrupt routine. Also, after a step change in current reference a certain time is required by the system to respond. This time adds to the available calculation time for f_{sample}. Finally, when f_{sample} is calculated the counter compare registers are automatically loaded with the appropriate value.

In order to speed up the function execution time the VSS can be started with non-zero initial conditions. A practical equivalent of such action would be an instantaneous pre-charge of the inductors to some finite current value. Therefore, the initial conditions in (16)-(18) could be set to any assumed value according to the operating conditions.

4.3.1 Delay Compensation

In experimental setup, the delay provided by the digital signal processor, gate drivers, and switching devices is inevitable. In a cumulative delay, the portion provided by the digital signal processor is most significant. The gate drivers, switching devices and sensors introduce a delay of less than 2 μs. Considering that both MPC and VSS require 10-20 μs to complete, the reference is adjusted using vector angle compensation to minimize the impact of the processing time. Taking into account vector representation of the variables of a three-phase system, it is convenient to estimate the future reference by considering the change in the vector angle during one sample time. The load current vector $\mathbf{i}^*$ can be described by its magnitude I^* and angle θ

$$\mathbf{i}^*(k) = I^*(k)e^{j\theta(k)} \tag{55}$$

Assuming this vector rotates at an angular speed ω and that the magnitude remains constant, the angle for the reference vector at t_{k+1} can be estimated as

$$\theta(k+1) = \theta(k) + \omega T_s \tag{56}$$

where T_s is the sampling time. Considering $I^*(k+1) = I^*(k)$ the value of the future reference vector can be estimated as

$$\mathbf{i}^*(k+1) = I^*(k)e^{j(\theta(k)+\omega T_s)} \tag{57}$$

Combining (55) and (57) the final equation to be implemented is

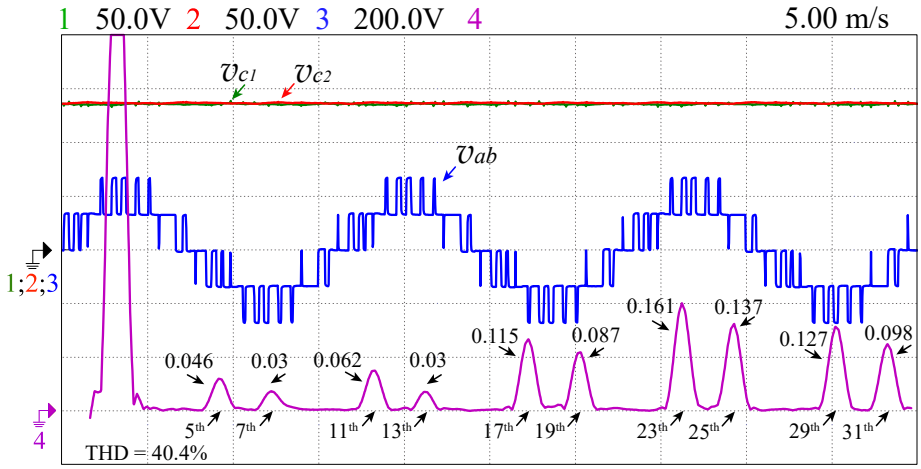
$$\mathbf{i}^*(k+1) = \mathbf{i}^*(k)e^{j\omega T_s} \tag{58}$$

4.4 Experimental Results and Analysis

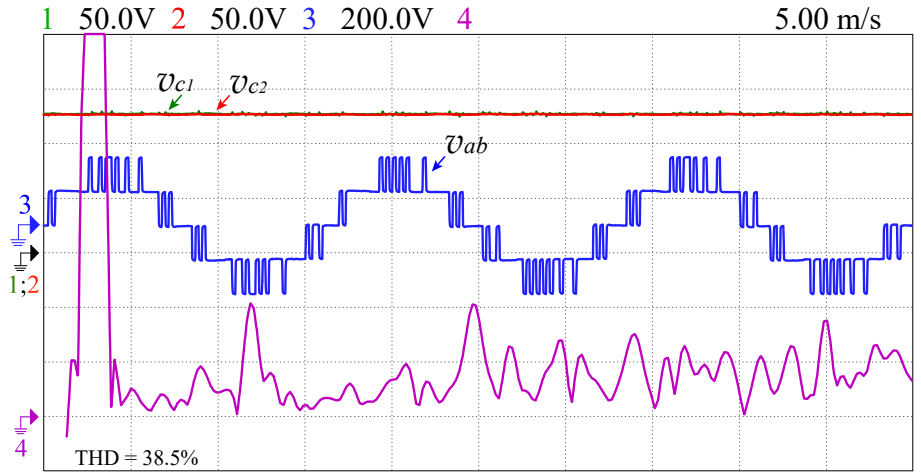
The control algorithm has been implemented using a host PC running MATLAB/Simulink 2006a software through a real-time interface. The dSPACE DS1103 controller is used to handle the control processes such as load current prediction, load voltage estimation, and cost function minimization. The load currents and DC-link voltages were measured using LEM LA55-P and LV25-P transducers, respectively. The feedback from the sensors has been sent to the controller through a CP1103 I/O connector. The prototype has been built with a Semikron SKM75GB123D dual-pack insulated-gate bipolar transistor (IGBT) modules. The IGBT gate drivers are based on a six SKHI22B dual-core modules powered by 15 V supply. The experimental setup parameters are provided in Table V.

Table V – Experimental setup parameters

Converter parameter	Value SI	Value pu
Converter rating	3.6 (kVA)	1
DC-link voltage	370 (V)	3.08
DC-link capacitance	1000 (μF)	4.52
Load resistance	11 (Ω)	0.92
Filter leakage resistance	0.065 (Ω)	0.005
Filter inductance	7.5 (mH)	0.24
Reference frequency	60 (Hz)	1
Proportional gain	1	-
Integral gain	1000	-



a)



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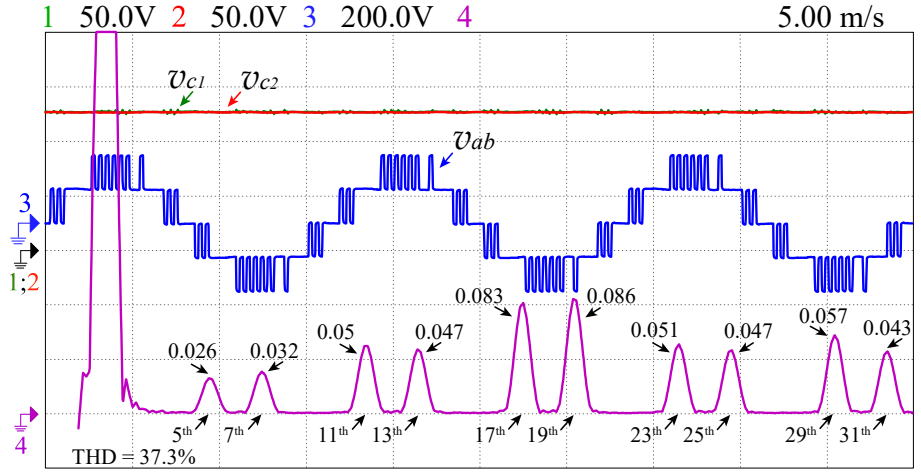
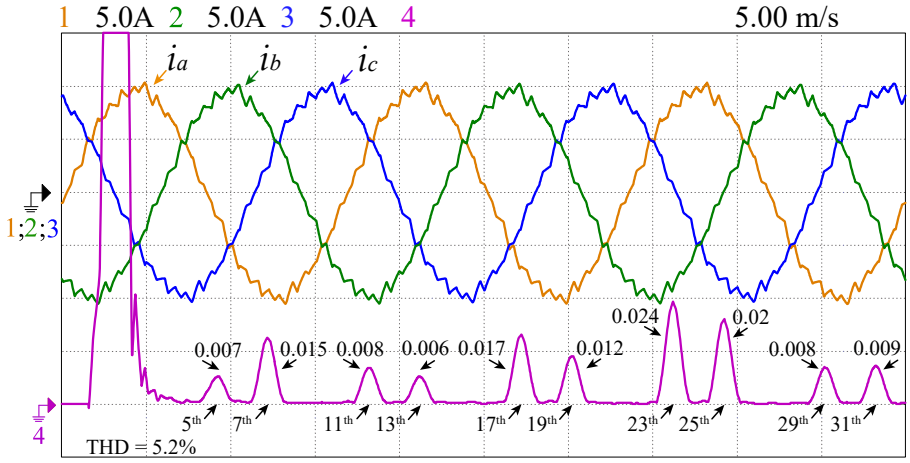
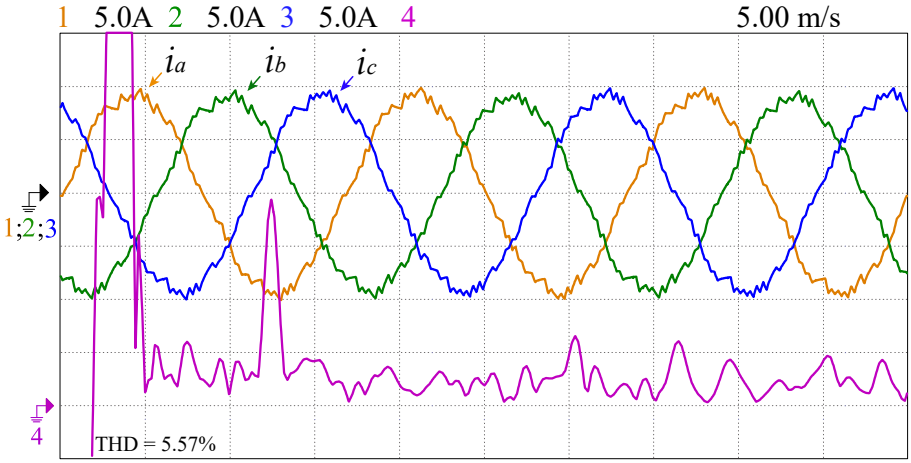


c)

Figure 45 - Steady-state comparison of line-to-line voltages: a) SVM; b) FSF-MPC; c) VSF-MPC



a)



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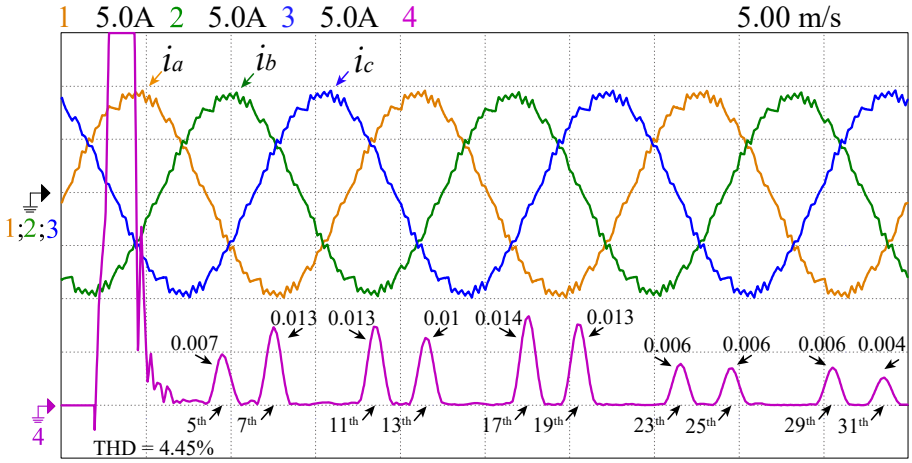


c)

Figure 46 - Steady-state comparison of 3-phase currents: a) SVM; b) FSF-MPC; c) VSF-MPC

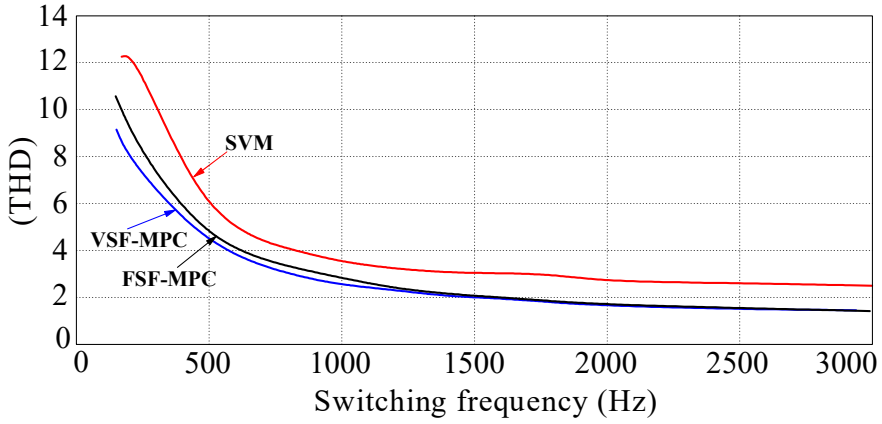
❖ Analysis of Steady-State Performance

In order to represent the efficiency of the control to shape the spectrum and eliminate even-order harmonics while following other required objectives, the steady-state performance has been assessed and compared with SVM and FSF-MPC. The graphs in Figure 45 represent line-to-line voltages and their harmonic spectrum in steady-state. Due to modulations stage, the SVM in Figure 45a) achieves fixed switching frequency operation including only the following harmonics: 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd}, 25^{th}, 29^{th} and 31^{st}. This is according to simulated waveforms. Even-order harmonics are not present since SVM was implemented as a 7-segment switching sequence optimized for reduction of switching frequency and even-order harmonic elimination. Further analysis reveals that FSF-MPC performs with variable switching frequency (Figure 45b)). Cycle to cycle difference between the gating signals delivers spectrum profile with frequencies spread across an entire spectrum. The switching pattern does not exist and cannot be established due to unsynchronized sampling times. When FSC-MPC gets accompanied with VSS to achieve optimal sampling period, the switching pattern becomes evident, rendering VSF-MPC similar to SVM as the same harmonic frequencies appear in both spectrums which can be observed in Figure 45c). The graphs in Figure 45 also reveal that all three control techniques successfully balance the DC-link capacitor voltages. Therefore, the experimental results in this test corroborate the theory, as an obtained waveforms agree closely with simulation results.

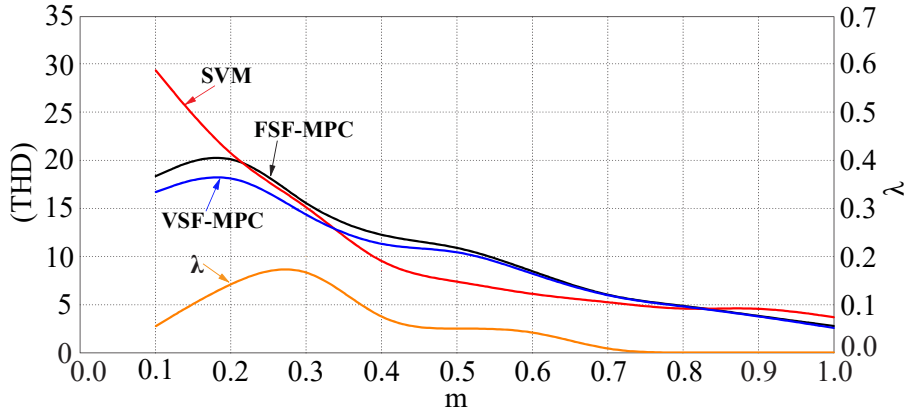
Further measurements in steady-state were carried out to include 3-phase currents with associated spectrum analysis. The results are presented in Figure 46. As in previous experiment in Figure 45, the SVM and VSF-MPC achieve fixed switching frequency operation without indicating inter- or even-order spectral components, while FSF-MPC delivers spread harmonic frequencies due to non-constant switching frequency. Therefore, it can be concluded that VSF-FCS-MPC is able to achieve fixed switching operation for given operating conditions, as such, producing similar results to SVM. Again, experimentally obtained results are consistent with simulated low-power waveforms.

From current THD analysis of plots in Figures 45 and 46 it is deduced that both MPCs achieve lower %THD compared to SVM. This can be attributed to significantly less complex predictive control mechanics and control effort concentrated into a single cost function. On top of that, VSF-MPC stands out as a method delivering the lowest %THD of all three experimented techniques. This behavior is notices in both voltage and current THD percentage. From

experimentally obtained values for different operating conditions, a thorough THD analysis and comparison were performed and the results are presented in Figure 47.



a)



b)

Figure 47 - Performance comparison: a) THD versus switching frequency; b) THD versus modulation index

❖ THD Comparison

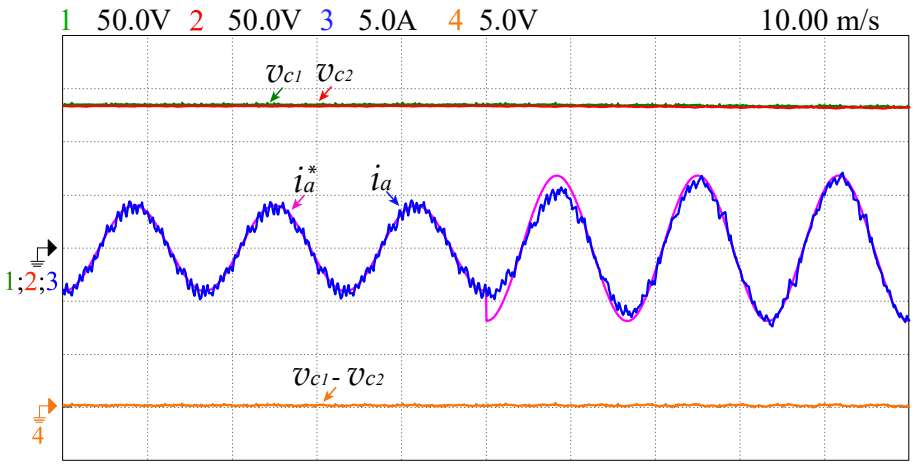
The comparative analysis was performed in case of the inverter operating at rated conditions while the switching frequency was spanned from lowest possible to 3 kHz. Furthermore, the setup was tested with variable modulation index ranging from 0.1 to 1 at constant switching frequency. All three control techniques were compared against the %THD of load current they achieve under tested conditions and the results are presented in Figure 47. As VSF-FCS-MPC uses the VSS to adjust the switching frequency through modifying the control sampling frequency, the sampling frequency of SVM was manually adjusted to always be 10 times higher

than the carrier frequency. This provides high sampling rate for SVM and therefore a fair comparison between tested control algorithms. Figure 47(a) shows that at rated conditions VSM-FCS-MPC outperforms both SVM and FSM-FCS-MPC. Clearly, predictive control achieves better vector utilization at full load. Also, both MPCs were able to achieve lower sustainable inverter operating frequency than SVM, achieving only 150 Hz, while SVM was able to go as low as 175 Hz. It should be noted that all switching frequencies measured in the experiment are device switching frequencies.

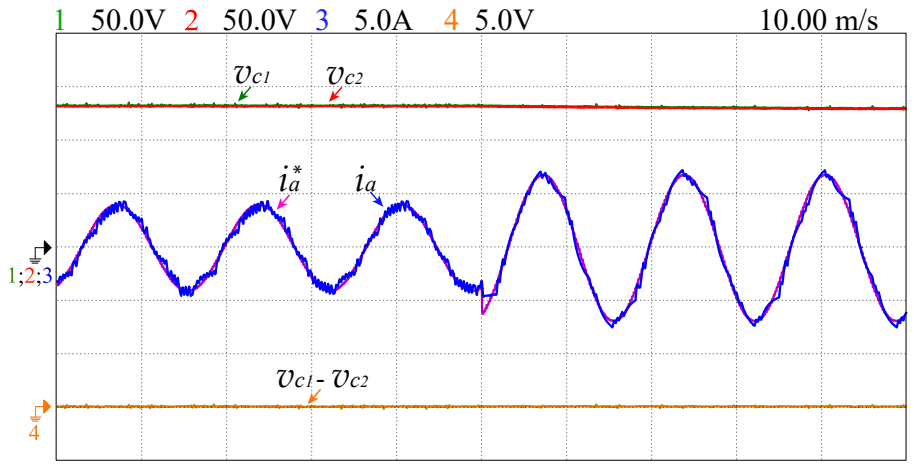
The graph in Figure 47(b) presents modulation index change versus THD. At high and low m predictive control achieves lower THD than SVM, but in range of 0.3 to 0.7, SVM performs with lower overall THD. Such a phenomenon can be attributed to the fact that MPC requires λ_{dc} to increase for adequate voltage balancing at lower m rates. At m=0.7, λ_{dc} was increased from 0 to 0.05. The switching frequency was still kept at 1 kHz, but increasing λ_{dc} effectively decreased the switching frequency ”dedicated” toward current reference tracking, as a certain number of switchings in small vectors became attributed only to DC-link capacitor voltage balancing. However, the SVM operating principle is different from MPC, since the capacitor voltages are balanced by extending or shrinking the dwell-times of certain small vectors. Balancing through dwell-time correction does not interfere with switching frequency, providing this mechanism with less impact on THD. However, MPC still performs better at light loads due to absence of modulation stage and lower complexity, which in turn enables better vector handling and better THD performance, even though the switching frequency is effectively less than with SVM.

❖ Analysis of Dynamic Performance

The dynamic performances of the system were also verified and presented in Figure 48. This set of measurements aims at stressing the response time of the system to determine the ability of each control mechanism to quickly and accurately follow a step change in current reference. It can be noticed that both VSF- and FSF-FSC-MPC outperform SVM when it comes to dynamic performance. Both predictive controls achieved almost instantaneous correction of load currents, accurately following the reference. On the other hand, SVM required over one and half fundamental cycles to nullify the error in reference tracking. Such a difference in response time is due to the fact that the overall SVM current control employs classical PI (proportional-plus-integral) compensators using a dq-frame transformation followed by a fairly complex modulation stage.



a)



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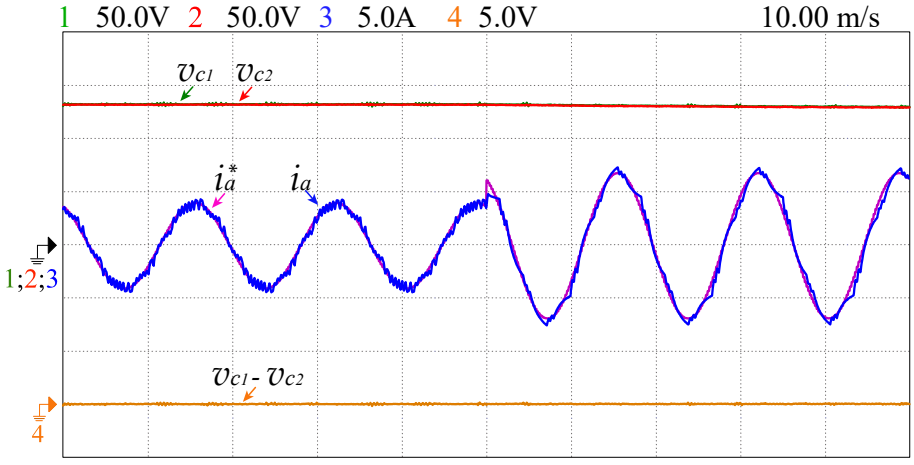

c)

Figure 48 - Transient response comparison: a) SVM; b) FSF-MPC; c) VSF-MPC

The modulation stage uses a built-in look-up table based on the vectors with previously optimized switching sequence. The fact that SVM relies on a carrier and generates the dwell-times according to the position of the reference vector does not allow sudden changes to be accurately followed, making the response a bit sluggish. On the other hand, predictive control single cost function-based operation is able to momentarily respond and apply vectors to minimize the error in the next sampling period. Thus, the response curves clearly reveal superior FCS-MPC characteristics when it comes to dynamic performance. Figure 48 also compares the DC-link voltage balancing abilities. All three control techniques behaved similarly and were able to maintained balanced condition during reference step change, displaying similar behavior as observed in simulation. In conclusion, VSM-FCS-MPC combines advantages of both techniques, providing fast response of FSC-MPC and fixed-switching frequency operation of SVM.

4.5 Summary

This chapter presents simulation verification for a low power NPC inverter and subsequently gives the experimental results with low power setup. The novel technique using variable sampling frequency and a virtual system simulator to determine an appropriate sampling frequency for spectrum shaping with even-order harmonic elimination is thoroughly examined. The presented simulation graphs in Figures 42-44 correlate closely with experimental results given in Figures 45, 46 and 48, displaying expected behavior for all control methods. The steady-state performance reveals accurate current tracking and proper voltage balancing in both simulation and experimental verification. The dynamic performances display no difference in speed and accuracy of response with similar DC-link voltage balancing during transients. Further, this chapter provides the DSP implementation procedure used in the experiment.

CHAPTER 5
CONCLUSION

5.1 Technical Challenges and Work Contributions

An implementation of MPC to control modern power converters has numerous benefits as it allows easy inclusion of various control objectives. A flexible formulation of the cost function permits optimization of several important parameters, such as: number of switchings, switching losses, reactive power control, motor torque ripple minimization, etc. Thus, the predictive controller takes over the functions of PWM block and cascaded multi-loop PI control, and can offer flexible and simple alternative to classical control systems.

One of the main challenges in the concept of FCS-MPC is achieving fixed-switching frequency operation while maintaining good dynamic performance. Variable switching frequency leads to spread spectrum which causes difficulties in the design and operation of power converters. In grid-interactive converter systems with LCL filtering, spread spectrum might excite certain harmonic frequencies rendering the system unstable or hardly controllable.

This work aims at solving variable switching frequency by introducing variable sampling frequency operation. It has been confirmed through simulations and experiments that the concept is feasible and that spectrum shaping can be achieved for both inverter and rectifier configurations.

5.1.1 Technical Challenges with Model Predictive Control

Aside from variable switching frequency and spread spectrum issues, there are other technical challenges associated with FCS-MPC. One of significant aspects nowadays is available digital computation power which in certain cases might still fail to handle all predictive control requirements. A practical implementation of MPC for multilevel converters with too many levels is still impossible due to extensive number of iterations. Adding up to this problem is a very complex programming required for the proposed VSS implementation in terms of describing a system and building a simulator that will precisely replicate its behavior.

Besides that, issues associated with predictive control, but not tightly related to the proposed control technique are determination of the cost function weighting coefficients and bandwidth analysis. Nowadays, the coefficients are still determined by empirical procedure. There

is no analytical or numerical solution proposed yet to obtain an optimal solution. When it comes to effective bandwidth analysis, related theoretical approach or frequency-response measurements have not been reported to date. This is not trivial, considering the fact that FCS-MPC is inherently a nonlinear control algorithm, in the same sense as the hysteresis controllers are. Hence, the traditional concept and theory of bandwidth available for linear controllers cannot be directly applied to FCS-MPC.

5.1.2 Work Contributions

This work proposes variable sampling frequency model predictive control to achieve fixed-switching frequency operation. The contributions of the study are summarized below:

- **Spectrum Shaping with Even-Order Harmonic Elimination**

  A complete elimination of even-order harmonics and inter-harmonic frequencies in the load current spectrum has been achieved with VSF-FCS-MPC. The proposed algorithm was verified with the NPC converter. The cost function simultaneously considered balancing of DC-link capacitor voltages and load current control. Common-mode voltage elimination in the NPC inverter was also verified, and this has been achieved without altering the predefined harmonic profile. Furthermore, the algorithm was simulated with an NPC rectifier, where the harmonic profile was maintained constant while following active and reactive power references.

- **Novel Switching Frequency Control Feature**

  Another important feature of the proposed control strategy is to arrange small vectors automatically through an auxiliary algorithm such that DC-link capacitor voltages and inverter switching frequency can be controlled independently without involving cost function. This feature introduces one more degree of freedom for switching frequency regulation and alleviates weighting factor design.

- **Extension of Variable Sampling Frequency FCS-MPC to Other Topologies**

  Variable switching frequency MPC with integrated VSS has a universal approach to power converters. With SVM included, only certain vectors are deemed appropriate for cost

function minimization. An application of this work can be easily extended to other higher-level voltage source converters. Variable sampling frequency can also find its application in current-source inverters since same optimization method can be used with topology-related modifications. Another field that can highly benefit from MPC with fixed-switching frequency is indeed the drives. As these systems employ both rectifiers and converters, predictive control can offer convenient and easy way to control the drives through a single cost function. At the same time, the rectifiers in drives may substantially benefit from fixed-harmonic profile if control with FSF-MPC, as this method delivers the performance in compliance with the grid codes.

- **Simple and Flexible Converter Control**

Since the switching frequency can be controlled by controlling the P/N/O states of small vectors and by regulating the sampling frequency, the cost function can consider fewer terms, i.e., λ_n factor previously used for switching frequency reduction can now be omitted. Therefore, problems associated with weighting factor design are mitigated. Moreover, inclusions of only current tracking into the cost function produces less error in reference tracking and lower overall THD.

- **Faster DSP Execution Time**

Especially with higher level converters, predictive control requires a large amount of calculation to predict the behavior of currents and voltages for all possible switching states. An involvement of SVM into predictive control narrows down the number of vectors used for prediction. This leads to significant reduction in calculation delay which will greatly improve performance. In such case, *k+2* prediction horizon may not need to be used, which in turn, increases performances even further.

APPENDIX

Discretization methods

A discrete-time systems should mimic the continuous-time controllers. We assume that a continuous-time controller is given as a transfer function, $C(s)$. It is desired to find an algorithm (difference equation) for microprocessors so that the digital controller $C(z)$ approximates the continuous-time controller, Figure 49.

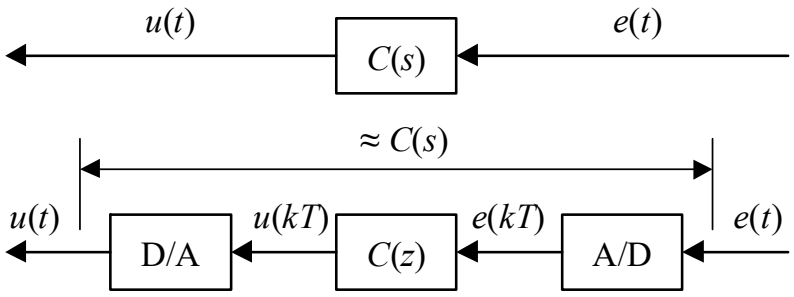

Figure 49 - Approximating Continuous-Time Controller

Approximate solution using numerical integration

To look for methods to approximate the transfer function, we start by examining a simpler question: what is the equivalent of the differential operator (*d/dt* or *s*) in terms of the shift operator (*z*)? Let's start with a single integrator system, i.e.

$$\dot{u}(t) = e(t) \text{ or } C(s) = \frac{U(S)}{C(S)} = \frac{1}{S} \tag{59}$$

The solution to this system is

$$u(t) = u(t_0) + \int_{t_0}^{t} e(\tau)d\tau \tag{60}$$

At the sample instants

$$u((k+1)T) = u(T) + \int_{T}^{(k+1)T} e(\tau)d\tau \tag{61}$$

There are three apparent choices to approximate the above integral in discrete time, i.e. using values only at the sample instants and not in between. Figure 50 illustrates these approximations.

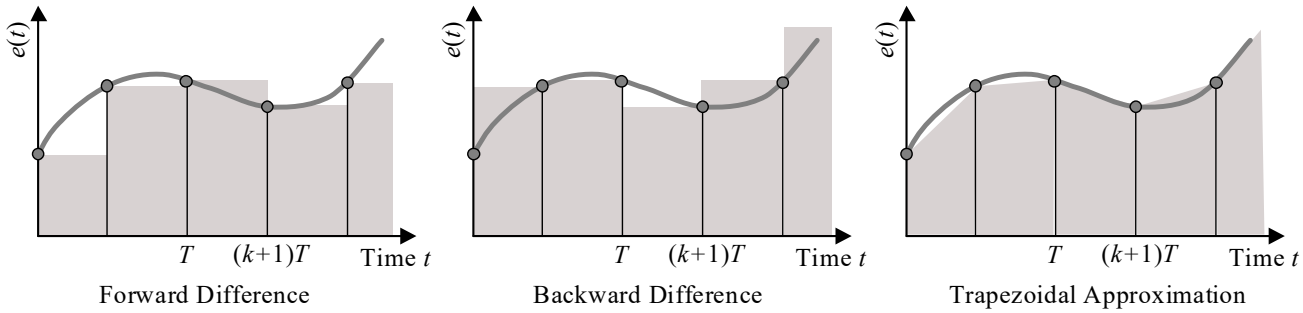

Figure 50 - Different Types of Integral Approximations

Mathematically, the discrete approximations of equation (61) can be summarized as follows:

Forward difference: $u(k+1) \approx u(k) + e(k)T$

Backward difference: $u(k+1) \approx u(k) + e(k+1)T$

Trapezoidal approximation: $u(k+1) \approx u(k) + \frac{[e(k+1)+e(k)]}{2}T$

The pulse transfer function from input $E(z)$ to output $U(z)$ is:

Forward difference: $C(Z) = \frac{U(Z)}{E(Z)} = \frac{T}{Z-1} = \frac{TZ^{-1}}{1-Z^{-1}}$

Backward difference: $C(Z) = \frac{U(Z)}{E(Z)} = \frac{TZ}{Z-1} = \frac{T}{1-Z^{-1}}$

Trapezoidal Approximation: $C(Z) = \frac{U(Z)}{E(Z)} = \frac{T}{2}\frac{Z+1}{Z-1} = \frac{T}{2}\frac{1+Z^{-1}}{1-Z^{-1}}$

Comparing with the pulse transfer functions above with the continuous-time transfer function we see that the discrete-time approximation of the continuous-time transfer function can be obtained by substituting the Laplace operator s with the following:

Forward difference: $s \to \frac{Z-1}{T}$

Backward difference: $s \to \frac{Z-1}{TZ}$

Trapezoidal Approximation: $s \to \frac{2}{T}\frac{Z-1}{Z+1}$

Exact solution

A mathematically exact calculation of the matrices of the discrete-time state space representation is of course not possible with the simple method described above. Let's start with

$$\boldsymbol{x}(t) = e^{\boldsymbol{A}t}\boldsymbol{k} \tag{62}$$

The matrix $e^{\boldsymbol{A}t}$ is called matrix exponential function. It is defined by the following Taylor series:

$$e^{\boldsymbol{A}t} = \sum_{i=0}^{\infty} \frac{\mathbf{A}^i t^i}{i!} = \mathbf{I} + \mathbf{A}t + \frac{\mathbf{A}^2}{2!}t^2 + \frac{\mathbf{A}^3}{3!}t^3 + \frac{\mathbf{A}^4}{4!}t^4 + \cdots \tag{63}$$

Combining state-space representation with equation (62) the following equation is obtained:

$$\boldsymbol{x}(t) = \boldsymbol{\Phi}(t)\boldsymbol{x_0} + \int_0^t \boldsymbol{\Phi}(t-\tau)\mathbf{B}\mathbf{u}(\tau)d\tau \tag{64}$$

with

$$\boldsymbol{\Phi}(t) = e^{\boldsymbol{A}t} \tag{65}$$

Φ is called transition matrix. If the time is set to $t = (k+1)T_0$, the following equation results:

$$\boldsymbol{x}((k+1)T_0) = e^{\boldsymbol{A}(k+1)T_0}\boldsymbol{x_0} + \int_0^{(k+1)T_0} e^{\mathbf{A}(k+1)T_0-\tau}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{66}$$

Since the value of **u**(t) is constant for $kT_0 \leq t \leq (k+1)T_0$ and using the substitution $\alpha = (k+1)T_0 - \tau$

$$\boldsymbol{x}((k+1)T_0) = e^{\boldsymbol{A}T_0}\boldsymbol{x}(\boldsymbol{kT_0}) + \int_0^{T_0} e^{\mathbf{A}\boldsymbol{\alpha}}d\alpha\mathbf{B}\mathbf{u}(kT_0) \tag{67}$$

By comparing the coefficients of the above equation with space-state matrixes, $\mathbf{A_d}$ and $\mathbf{B_d}$ which present the discrete-time *state* and *input* matrix can be determined directly:

$$\mathbf{A_d} = e^{\mathbf{A}T_0} \tag{68}$$

$$\mathbf{B_d} = \int_0^{T_0} e^{\mathbf{A}\alpha}d\alpha\mathbf{B} \tag{69}$$

Assuming a continuous system, it can be stated that $det\mathbf{A} \neq 0$; the input matrix of the discrete-time system thus results to:

$$\mathbf{B_d} = \mathbf{A}^{-1}(e^{\mathbf{A}T_0} - \mathbf{I})\mathbf{B} \tag{70}$$

With the help of the equation (68) and (70), the state matrix $\mathbf{A_d}$ and the input matrix $\mathbf{B_d}$ of the discrete-time system can be calculated.

Reference following

A measure of distance between reference and predicted value usually can be implemented as an absolute value, square value, or integral value of the error for one sampling period:

$$g = |x^* - x^P| \tag{71}$$

$$g = (x^* - x^P)^2 \tag{72}$$

$$g = \left| \int_k^{k+1} (x^*(t) - x^p(t))dt \right| \tag{73}$$

Absolute error and squared error give similar results when the cost function considers only one error term. However, if the cost function has two or more different terms, results can be different. Squared error presents a better reference following when additional terms are included in the cost function. Cost function (73) considers the trajectory of the variable between time t_k and t_{k+1}, not just the final value at instant t_{k+1}, leading to the mean value of the error to be minimized. This then leads to more accurate reference tracking.

Delay compensation

As the three-phase inverter has twenty seven different voltage vectors, the predicted current and the cost function are calculated seven times. In this way, depending on the sampling frequency and the speed of the microprocessor used for the control, the time between measurement of the load currents and application of the new switching state can be considerable. If the calculation time is significant compared to the sampling time, there will be a delay between the instant at which the currents are measured and the instant of application of the new switching state.

A simple solution to compensate this delay is to take into account the calculation time and apply the selected switching state after the next sampling instant. In this way, the control algorithm is modified as follows:

1. Measurement of the load currents.
2. Application of the switching state (calculated in the previous interval).

3. Estimation of the value of the currents at time t_{k+1}considering the applied switching state.

4. Prediction of the load currents for the next sampling instant t_{k+2} for all possible switching states.

5. Evaluation of the cost function for each prediction.

6. Selection of the switching state that minimizes the cost function.

The measured currents and the applied switching states at time t_k are used to estimate the value of the load currents at time t_{k+1}.

$$\mathbf{i^p}(k+1) = \left(1 - \frac{RT_s}{L}\right)\mathbf{i}(k) + \frac{T_s}{L}\mathbf{v}(k) \tag{74}$$

Then, this current is used as a starting point for the predictions for all switching states. These predictions are calculated using the load model shifted one step forward in time:

$$\mathbf{i^p}(k+2) = \left(1 - \frac{RT_s}{L}\right)\mathbf{i}(k+1) + \frac{T_s}{L}\mathbf{v}(k+1) \tag{75}$$

where **i**(k+1) is the estimated current vector and **v**(k+1) is the actuation to be evaluated. The cost function is modified for evaluation of the predicted currents $\mathbf{i^p}$(k + 2), resulting in:

$$g = |i_\alpha^*(k+2) - i_\alpha^P(k+2)| + \left|i_\beta^*(k+2) - i_\beta^P(k+2)\right| \tag{76}$$

Calculation of future reference using Lagrange extrapolation

For sinusoidal references and large sampling times, the use of extrapolation methods for the reference can compensate the delay in the reference tracking in predictive control schemes. A possible solution is to calculate the one-step-ahead prediction using the actual current reference in the nth-order formula of the Lagrange extrapolation by:

$$\hat{\mathbf{i}}^*(k+1) = \sum_{i=0}^{n}(-1)^{n-1}\begin{bmatrix} n+1 \\ l \end{bmatrix}\mathbf{i}^*(k+l-n) \tag{77}$$

For sinusoidal references, *n*=2 or higher is recommended. Using the extrapolation formula, the future reference can be predicted $\mathbf{i}^*(k+1)$ can be predicted, for *n*=2, with

$$\hat{\mathbf{i}}^*(k+1) = 3\mathbf{i}^*(k) - 3\mathbf{i}^*(k-1) + \mathbf{i}^*(k-2) \tag{78}$$

Calculation of the future reference $\mathbf{i}^*(k+2)$ is required when cost function (76) is considered. This estimate can be calculated by shifting forward (78), giving

$$\hat{\mathbf{i}}^*(k+2) = 3\mathbf{i}^*(k+1) - 3\mathbf{i}^*(k) + \mathbf{i}^*(k-1) \tag{79}$$

And, by substituting (78) into (79), the future reference can be calculated using only present and past values of the reference current. The resulting expression for the calculation of $\mathbf{i}^*(k+2)$ is

$$\hat{\mathbf{i}}^*(k+2) = 6\mathbf{i}^*(k) - 8\mathbf{i}^*(k-1) + 3\mathbf{i}^*(k-2) \tag{80}$$

Calculation of future references using vector angel compensation

Taking into account vector representation of the variables of a three-phase system, it is possible to implement and estimate the future reference by considering the change in the vector angle during one sample time.

The load current vector $\mathbf{i}^*$can be described by its magnitude I^* and angle θ:

$$\mathbf{i}^*(\mathrm{k}) = I^*(k)e^{j\theta(k)} \tag{81}$$

At steady state, it can be assumed that this vector rotates at an angular speed ω and that the magnitude remains constant. In this way, the angle of the reference vector for time t_{k+1} can be estimated as

$$\theta(k+1) = \theta(k) + \omega T_s \tag{82}$$

where T_s is the sampling time.

Considering (82) and $I^*(\mathrm{k}+1) = I^*(k)$, the value of the future reference vector can be estimated as

$$\mathbf{i}^*(k+1) = I^*(k+1)e^{j\theta(k+1)} = I^*(k)e^{j(\theta(k)+\omega T_s)} \tag{83}$$

and inserting (81) into (83)

$$\mathbf{i}^*(k+1) = \mathbf{i}^*(k)e^{j\omega\ s} \tag{84}$$

The same procedure can be used for the estimation of $\mathbf{i}^*(k+2)$, assuming

$$\theta(k+2) = \theta(k) + 2\omega T_s \tag{85}$$

and $I^*(k+2) = I^*(k)$, resulting in

$$\mathbf{i}^*(k+2) = \mathbf{i}^*(k)e^{2j\omega T_s} \tag{86}$$

Weighting Factors Adjustment for cost functions with secondary terms

This is the easiest case for weighting factor adjustment, since the system can be first controlled using only the primary control objective or term. This can be simply achieved by neglecting the secondary terms forcing the weighting factor to zero ($\lambda = 0$). Hence the first step of the procedure is to convert the cost function with secondary terms into a cost function without weighting factors. This will set the starting point for the measurement of the behavior of the primary variable.

The second step is to establish measurements or figures of merit that will be used to evaluate the performance achieved by the weighting factor. Several error measures for current can be defined, such as the root mean square (RMS) value of the error at steady state, or the total harmonic distortion (THD). At least one additional measure is necessary to establish the trade-off with the secondary term.

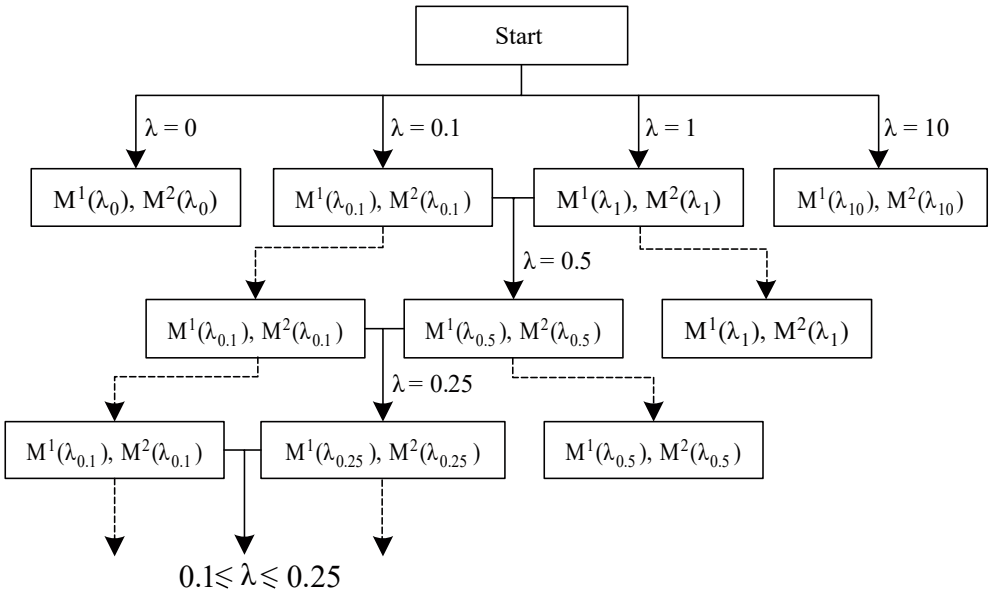

Figure 51 - Branch and bound algorithm to reduce the number of simulations required to obtain suitable weighting factors

Once the measures are defined, the procedure is as follows. Evaluate the system behavior with simulations starting with $\lambda = 0$ and increase the value gradually. Record the corresponding measures for each value of λ. Stop the increments of λ once the measured value for the secondary

term has reached the desired value for the specific application, or keep increasing λ until the primary variable is not properly controlled. Then plot the results and select a value of λ that fulfills the system requirements for both variables. This procedure can be programmed by automating and repeating the simulation, introducing an increment in the weighting factor after each simulation.

In order to reduce the number of simulations required to find a proper value for the weighting factor, a branch and bound algorithm can be used. For this approach, first select a couple of initial values for the weighting factor λ, usually with different orders of magnitude to cover a very wide range, for example, λ = 0, 0.1, 1, and 10. A qualitative example of this algorithm is illustrated in Figure 51. Then simulate these weighting factors and obtain the measures for both terms, M^1 and M^2, for the primary and secondary terms respectively. Then compare these results to the desired maximum errors admitted by the application and fit them into an interval of two weighting factors ($0.1 = \lambda = 1$ in the example). Then compute the measures for the λ in half of the new interval (λ = 0.5 in the example) and continue until a suitable λ is achieved. Note in Figure 51 that each solid line corresponds to a simulation and dashed lines correspond to values already simulated. This method reduces the number of simulations necessary to obtain a working weighting factor.

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