

PREDICTIVE CONTROL OF MULTILEVEL CONVERTERS FOR MEGAWATT WIND ENERGY CONVERSION SYSTEMS

By

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Abstract

This dissertation proposes two novel medium voltage (MV) multilevel converter configurations for use with permanent magnet synchronous generator (PMSG) based megawatt (MW) wind energy conversion systems (WECS). The classical control techniques, based on linear PI regulators and low band-width modulation, present several technical issues during lower switching frequency operation. To overcome these issues, a high performance finite control-set model predictive control (FCS-MPC) strategy is proposed to control the power converters employed in the MW-PMSG-WECS.

The proposed three-level and four-level converters combine the advantages of proven wind turbine technologies, such as low-cost generator-side passive converters, and efficient grid-side multilevel converters. The intermediate dc-dc multilevel converters ensure balancing of the capacitor voltages during all operating conditions. With this feature, the grid-side multilevel converters produce better grid current waveforms compared to the back-to-back connected converters.

A generalized approach for the predictive control of an n-level diode-clamped converter was investigated. The FCS-MPC strategy for current control and decoupled active/reactive power regulation of grid-connected multilevel converters was also analyzed. The major

WECS requirements such as maximum power point tracking, balancing of dc-link capacitor voltages, switching frequency minimization, common-mode voltage mitigation, regulation of net dc-bus voltage, and grid reactive power control have been modeled in terms of power converter switching states. These control objectives have been accomplished during each sampling interval by selecting the switching states which minimize the generator- and grid-side cost functions.

Issues related to the weighting factors selection, control delay compensation, accurate extrapolation of references, control of variable switching frequency nature, prediction of variables over two samples with reduced computational burden, and robustness analysis, are also addressed in this dissertation.

To keep the dc-bus voltage constant during low voltage ride-through operation, predictive control scheme is proposed for the power converters while storing surplus energy in the turbine-generator rotor inertia. The generation and exchange of reference control variables during symmetrical grid voltage dips is suggested to meet the grid code requirements. The proposed solution is efficient as no energy is dissipated in the dc-link crowbar.

The simulation and experimental results validate the proposed MV converters and predictive control schemes.

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Dedicated to my mother Subbayamma and father Veeraiah

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List of Publications

Papers in Refereed Journals¹

Papers Published

- [1] **V. Yaramasu**, M. Rivera, B. Wu, and J. Rodriguez, “Model Predictive Current Control of Two-Level Four-Leg Inverters – Part I: Concept, Algorithm and Simulation Analysis,” *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3459-3468, Jul. 2013.
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- [4] **V. Yaramasu**, B. Wu, and J. Chen, “Model Predictive Control of Grid-Tied Four-Level Diode-Clamped Inverters for High Power Wind Energy Conversion Systems,” *IEEE Trans. Power Electron.*, 2013, DOI: 10.1109/TPEL.2013.2276120.

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- [5] **V. Yaramasu**, and B. Wu, “A Model Predictive Decoupled Active and Reactive Power Control for High Power Grid-Connected Four-Level Diode-Clamped Inverters,” *IEEE Trans. Ind. Electron.*, 2013, DOI: 10.1109/TIE.2013.2278959.
- [6] **V. Yaramasu**, and B. Wu, “Predictive Control of a Three-Level Boost Converter and an NPC Inverter for High-Power PMSG-Based Medium Voltage Wind Energy Conversion Systems,” *IEEE Trans. Power Electron.*, 2013, DOI: 10.1109/TPEL.2013.2292068.
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- [11] **V. Yaramasu**, B. Wu, S. Alepuz, and S. Kouro, “Predictive Control for Low Voltage Ride-Through Enhancement of Three-Level Boost and NPC Converters based PMSG Wind Turbines,” *IEEE Trans. Ind. Electron.*, 2013. ([Minor revision submitted for review](#))

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- [15] L. Tang, B. Wu, **V. Yaramasu**, W. Chen, and H. S. Athab, “Novel DC/DC Choppers with Circuit Breaker Functionality for HVDC Transmission Lines,” *J. Electric Power Systems Research*, 2013. ([Manuscript submitted for review](#))

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- [16] **V. Yaramasu**, B. Wu, M. Narimani, M. Rivera, and J. Wang, “Comparative Assessment of Classical and Predictive Control Techniques for Two-Level Voltage Source Converters Based High-Power PMSG Wind Turbines,” *IEEE Trans. Power Electron.*, 2014.
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- [23] M. Narimani, **V. Yaramasu**, B. Wu, N. Zargari, G. Cheng, and G. Moschopoulos, “A Simple Method for Capacitor Voltages Balancing of Diode-Clamped Multilevel Converters using Space Vector Modulation,” in *IEEE Ind. Electron. Society (IECON)*, Nov. 2013, pp. 310-315, Vienna, Austria.
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- [38] M. Narimani, **V. Yaramasu**, B. Wu, and N. Zargari, “A New Simplified Approach for Capacitor Voltage Balancing of Flying Capacitor Multilevel Converters using Space Vector Modulation,” in *European Conf. on Power Electron. and Appl. (EPE’14-ECCE Europe)*, Aug. 2014, Lappeenranta, Finland.

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Glossary of Acronyms and Symbols

Abbreviations

3L	Three-Level
4L	Four-Level
AC	Alternating Current
ADC	Analog-to-Digital Conversion
ANPCC	Active Neutral-Point Clamped Converter
ANPCI	Active Neutral-Point Clamped Inverter
ANPCR	Active Neutral-Point Clamped Rectifier
BC	Boost Converter
BTB	Back-to-Back Connected
CCF	Changes to Controller and Filter
CCM	Continuous Current Mode
CF	Changes to Filter
CHB	Cascaded H-Bridge
CMOS	Complementary Metal-Oxide-Semiconductor
CMV	Common-Mode Voltage
CSC	Current Source Converter
CSI	Current Source Inverter
CSR	Current Source Rectifier
DAC	Digital-to-Analog Conversion
DC	Direct Current
DCC	Diode-Clamped Converter
DCI	Diode-Clamped Inverter
DCM	Discontinuous Current Mode
DCR	Diode-Clamped Rectifier
DD	Direct-Driven

DFIG	Doubly-Fed Induction Generator
DSO	Distribution System Operator
DSP	Digital Signal Processor
DTC	Direct Torque Control
EMF	Electro-Motive Force
FC	Flying Capacitor
FCC	Flying Capacitor Converter
FCI	Flying Capacitor Inverter
FCR	Flying Capacitor Rectifier
FCS-MPC	Finite Control-Set Model Predictive Control
FFT	Fast Fourier Transform
FOC	Field Oriented Control
FPGA	Field-Programmable Gate Array
FRT	Fault Ride-Through
FSC	Full-Scale Converter
GB	Gear Box
GCR	Grid-Code Requirements
GCT	Gate-Controlled Thyristor
GTI	Grid-Tied Inverter
HB	H-Bridge
HBI	H-Bridge Inverter
HBR	H-Bridge Rectifier
IG	Induction Generator
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
IM	Induction Machine
I/O	Input/Output
IPD	In-Phase Disposition
LCI	Load Commutated Inverter
LV	Low Voltage
LVRT	Low Voltage Ride-Through
ML	Multi-Level
MLDCC	Multi-Level Diode-Clamped Converter
MPC	Model Predictive Control
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking

MSC	Machine-side Converter
MV	Medium Voltage
MW	Megawatt
NPC	Neutral-Point Clamped
OTSR	Optimal Tip-Speed Ratio
PC	Predictive Control
PCC	Predictive Current Control
PE	Power Electronics
PF	Power Factor
PPC	Predictive Power Control
PVC	Predictive Voltage Control
PI	Proportional-Integral
PLL	Phase-Locked Loop
PMSG	Permanent Magnet Synchronous Generator
PWM	Pulse Width Modulation
RPG	Reactive Power Generation
RTI	Real-Time Interface
SCIG	Squirrel Cage Induction Generator
SGCT	Symmetric Gate-Controlled Thyristor
SHE	Selective Harmonic Elimination
SRF	Synchronous Reference Frame
SS	Steady-state
SVM	Space Vector Modulation
TLB	Three-Level Boost
THD	Total Harmonic Distortion
TSO	Transmission System Operator
TTL	Transistor-Transistor Logic
UPF	Unity Power Factor
VOC	Voltage Oriented Control
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
VSR	Voltage Source Rectifier
WECS	Wind Energy Conversion Systems
WRIG	Wound Rotor Induction Generator
WRSG	Wound Rotor Synchronous Generator
WT	Wind Turbine

Voltage Quantities

v_g	Grid <i>rms</i> phase-neutral voltage (V)
v_{gl}	Grid <i>rms</i> line-line voltage (V)
v_{ag}, v_{bg}, v_{cg}	Three-phase grid voltages (V)
v_{dg}, v_{qg}	<i>d</i> and <i>q</i> -axis grid voltages (V)
v_{an}, v_{bn}, v_{cn}	Three-phase inverter voltages with respect to grid/load neutral (V)
v_{aN}, v_{bN}, v_{cN}	Three-phase inverter voltages with respect to negative dc-rail (V)
v_{di}, v_{qi}	<i>d</i> and <i>q</i> -axis inverter voltages (V)
v_s	Generator <i>rms</i> phase-neutral voltage (V)
v_{sl}	Generator <i>rms</i> line-line voltage (V)
v_{as}, v_{bs}, v_{cs}	Three-phase generator voltages (V)
v_{ds}, v_{qs}	<i>d</i> and <i>q</i> -axis generator voltages (V)
e_a, e_b, e_c	Three-phase motor back emf (V)
v_{dc}	Net dc-bus voltage (V)
v_{dc}^*	Reference dc-bus voltage (V)
v_{cj}	Voltage across dc-link capacitors $j = 1, 2, \dots$ (V)

Current Quantities

i_g	Grid <i>rms</i> current (A)
i_{ag}, i_{bg}, i_{cg}	Three-phase grid currents (A)
i_{dg}, i_{qg}	<i>d</i> and <i>q</i> -axis grid currents (A)
i_{dc}	DC current (A)
i_{cj}	Current through dc-link capacitors $j = 1, 2, \dots$ (A)

Power Quantities

S_g	Grid apparent power (VA)
P_g	Grid active power (W)
Q_g	Grid reactive power (VAR)
Q_g^*	Reference grid reactive power (VAR)
P_M	Power output of wind turbine (W)
P_m	Mechanical input power to wind generator (W)
S_s	Wind generator apparent power output (VA)
P_s	Wind generator active power output (W)
Q_s	Wind generator reactive power output (VAR)
P_{dc}	Power stored in the dc-link elements (W)

Torque Quantities

T_M	Torque output of wind turbine (N.m)
T_m	Mechanical input torque to wind generator (N.m)
T_e	Electromagnetic torque of wind generator (N.m)
T_e^*	Reference electromagnetic torque for wind generator (N.m)

RLC Quantities

R_g	Internal resistance of grid-side inductive filter (Ω)
R_{dc}	Internal resistance of dc inductive filter (Ω)
L_g	Inductance of grid-side harmonic filter (H)
L_d, L_q	d and q -axis generator inductance (H)
L_{dc}	Inductance of dc filter (H)
C_{dcj}	Capacitance of dc-link capacitors $j = 1, 2, \dots$ (F)
C_{in}	Capacitance of input dc-link capacitor (F)

Frequency and Time Quantities

f_g	Grid frequency (Hz)
f_s	Generator frequency (Hz)
f_{sw}	Device switching frequency of power converter (Hz)
ω_g	Grid angular frequency (rad/s)
ω_s	Generator electrical angular frequency (rad/s)
ω_m	Generator mechanical angular frequency (rad/s)
θ_g	Grid voltage angle (rad)
θ_m	Generator mechanical position (rad)
T_s	Controller sampling time (s)

Generator Quantities

J	Moment of inertia (kg.m ²)
H	Inertia time constant (s)
PF_s	Power factor
PP	Number of pole pairs
n_m	Generator speed (rpm)

Wind Turbine Quantities

R_{gb}	Gearbox ratio
ρ	Air density (kg.m ²)
r_T	Turbine rotor radius (m)
C_p	Turbine power coefficient
λ_T	Turbine tip-speed ratio
n_M	Turbine speed (rpm)
v_w	Wind speed (m/s)

Predictive Controller Quantities

h	Prediction horizon
g	Cost function
s	Laplace operator (when not used as a subscript)
k	Discrete-time present sampling instant
$k - 1$	Discrete-time past sampling instant
$k + 1$	Discrete-time future sampling instant
t	Continuous-time
λ_{dc}	Weighting factor for dc-link capacitor voltages balancing
λ_{swc}	Weighting factor for switching frequency reduction
λ_{cmv}	Weighting factor for common-mode voltage reduction
$\frac{d}{dt}$	Derivative operator
S_x	Level of voltage vector of phase $x = a, b, c$
S_{jx}	Switching states of phase $x = a, b, c, j = 1, 2, \dots$
swc_x	Number of switch changes in inverter phase $x = a, b, c$
P, N	Positive and negative dc bus of a power converter

Vector Quantities

\mathbf{v}_g	Grid voltage vector	$[v_{ag} \ v_{bg} \ v_{cg}]^T$
\mathbf{i}_g	Grid current vector	$[i_{ag} \ i_{bg} \ i_{cg}]^T$
\mathbf{v}_i	Inverter voltage vector	$[v_{an} \ v_{bn} \ v_{cn}]^T$
\mathbf{v}_s	Generator voltage vector	$[v_{as} \ v_{bs} \ v_{cs}]^T$
\mathbf{i}_s	Generator current vector	$[i_{as} \ i_{bs} \ i_{cs}]^T$
\mathbf{v}_c	dc-link voltage vector	$[v_{c1} \ v_{c2} \ \dots]^T$
\mathbf{i}_c	dc-link current vector	$[i_{c1} \ i_{c2} \ \dots]^T$

Base Quantities

v_{bg}	Grid-side base voltage (V)
i_{bg}	Grid-side base current (A)
v_{bgp}	Grid-side peak base voltage (V)
i_{bgp}	Grid-side peak base current (A)
Z_{bg}	Grid-side base impedance (Ω)
L_{bg}	Grid-side base inductance (H)
C_{bg}	Grid-side base capacitance (F)
v_{bs}	Generator-side base voltage (V)
i_{bs}	Generator-side base current (A)
v_{bsp}	Generator-side peak base voltage (V)
i_{bsp}	Generator-side peak base current (A)
Z_{bs}	Generator-side base impedance (Ω)
L_{bs}	Generator-side base inductance (H)
C_{bs}	Generator-side base capacitance (F)
Λ_{bs}	Generator-side base flux-linkage (Wb)

Superscripts

p	Predicted quantity
e	Estimated quantity
\hat{x}	Estimation of x
$*$	Reference quantity

Subscripts

a, b, c	Natural frame quantities
d, q	Synchronous frame quantities
α, β	Stationary frame quantities
R	Rated quantity
op	Optimal quantity
g	Grid-side quantity
dc	dc quantity
s, m	Generator-side quantity
T, M	Turbine quantity

Chapter 1

Introduction

Due to depleting fossil fuels and environmental concerns, electricity production from renewable energy sources has attracted great attention in recent years. By 2012, the power production from renewable energy sources worldwide exceeded 1470 gigawatt (GW) representing approximately 19% of global energy consumption [1]. Among all the renewable energy sources, wind energy is increasingly becoming mainstream and competitive with conventional sources of energy. This success is mainly propelled by technological advancements, cost reduction and government incentive programs [2]. As of 2012, approximately 83 countries are using wind energy on a commercial basis to generate electricity [1].

The electricity production from wind turbines started during the 1980's. Over the past three decades, the size of wind turbines has steadily increased and currently reached a level of 7.5 megawatt (MW) per unit [3]. Due to the rapid integration of wind power into the electric grid, many concerns emerged related to the stable and secure operation of the existing electric power system. The grid codes have been updated and enforced in many countries on the grid-connection of large-scale wind turbines or wind farms.

The power electronic converters have been used in commercial wind turbines since the beginning of grid-connected operation, and this technology has changed dramatically over the past 30 years [4]. Since the 1980's, various combinations of wind generators and power electronic converters have been developed in commercial wind turbines to achieve fixed-speed, semi-variable and full-variable-speed operation. The latter has emerged as a successful configuration to increase wind energy conversion efficiency, improve grid power quality and to meet the grid codes. The power converter and its control are very crucial in the successful and efficient operation of variable-speed wind turbines.

In this dissertation, two novel power converter topologies have been proposed aimed at wind turbines rated at MW-level. The proposed power conversion systems were designed by combining the best qualities of existing solutions from the commercial wind turbine manufacturers. A qualitative analysis in terms of cost, weight, complexity, reliability and efficiency was carried out by comparing the proposed configurations with the existing technologies. To achieve high performance operation for the proposed converters based variable-speed wind turbines, an advanced control system founded on a finite control-set model predictive strategy is proposed. The theoretical analysis, discrete-time modeling, control scheme development and real-time implementation have been investigated in detail.

The organization of this Chapter is as follows: the overview of Wind Energy Conversion System (WECS) is given in Section 1.1 and the motivation for the Dissertation research is outlined in Section 1.2. The objectives of this Dissertation are presented in Section 1.3. Finally, in Section 1.4, the outline of the Dissertation is summarized.

1.1 Overview of Wind Energy Conversion Systems

In this section, the installed wind power capacity, global perspectives of WECS, evolution in the increase of turbine power rating, major components of grid-connected WECS, classification of WECS operating voltages, overview of grid code requirements and commercial configurations of WECS are discussed in detail.

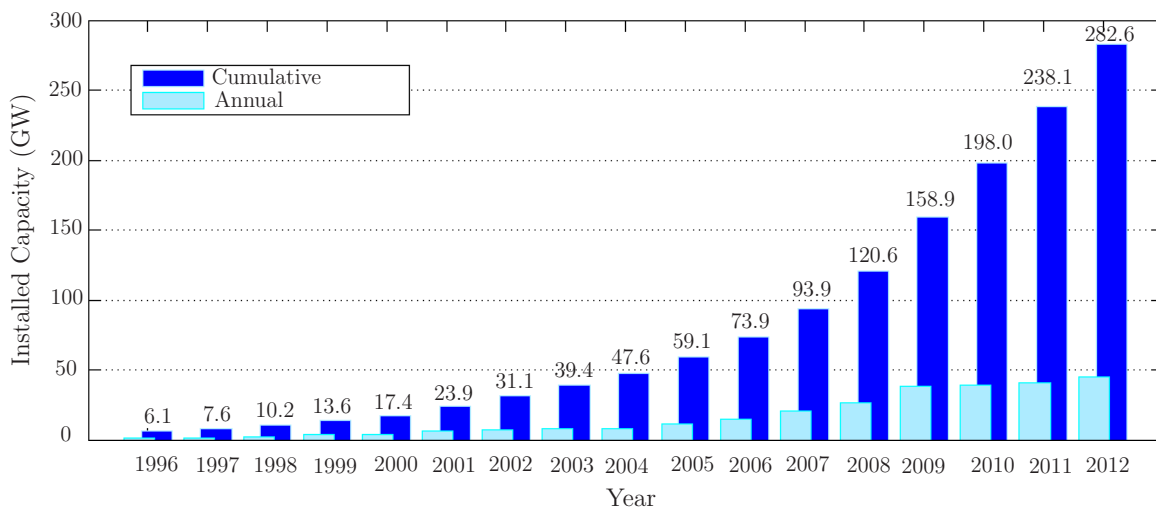


Figure 1.1: Global annual and cumulative installed wind power from 1996 to 2012 [source: Global Wind Energy Council (GWEC)].

1.1.1 Installed Wind Power Capacity and Growth Rate

The annual and cumulative installed wind power capacity worldwide is shown in Fig. 1.1 [5]. The cumulative installed capacity increased exponentially from 6100 MW in 1996 to 282.6 GW by 2012. It was anticipated on a moderate scale that the cumulative wind capacity would reach 760 GW by 2020 [1]. In 2012, approximately 45 GWs of new wind power was installed which represents investments of about €56 billion [5]. The wind energy industry demonstrated an excellent growth rate of more than 19 % by the end of 2012. The technological advancements in terms of wind turbine design, generator and power converters are some of the key reasons behind this impressive growth rate.

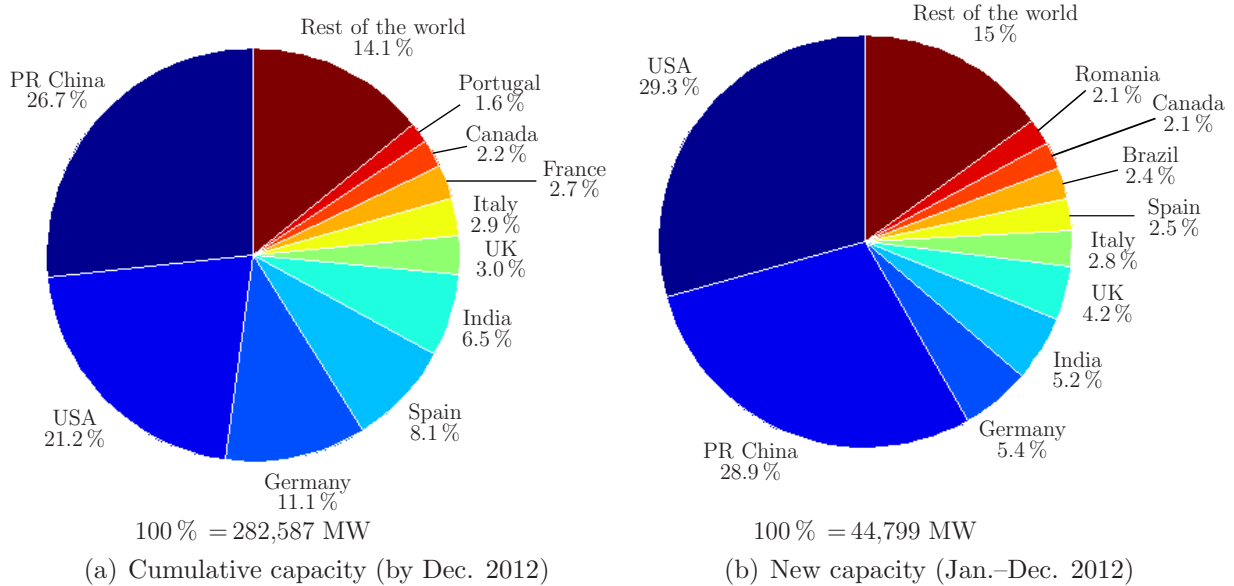


Figure 1.2: Top 10 countries in the installed wind power capacity.

1.1.2 Global Perspective of WECS

The top 10 countries in the cumulative and annual installed wind power capacity are shown in Fig. 1.2 [1,5]. The Chinese market maintained its top position in global cumulative installed wind power by tripling its capacity from 25.8 GW in 2009 to 75.3 GW by the end of 2012. The USA gained the top spot in 2012 by adding approximately 13.1 GWs of new wind power from 190 projects.

Approximately 24 countries have more than 1 GW cumulative installed wind power capacity, including 16 in Europe, 4 in the Asia-Pacific area (China, India, Japan, Australia), 3 in North America (Canada, Mexico, US) and 1 in Latin America (Brazil) [5]. Some countries have the highest penetration by wind power. For example, in Denmark more than 30 % of electricity consumption is covered from wind energy [4].

Canada is ranked top 9th in both cumulative and new installed capacity. The cumulative installed wind power capacity in Canada steadily increased from 137 MW in 2000 to 6.2 GW by the end of 2012. More than 2000 MW wind power has been installed in Ontario which accounts for 3 % of the province's electricity demand. Canada has ambitious plans to supply 20 % of net electricity consumption from wind by 2025.

1.1.3 Evolution of Megawatt WECS

The power output of a wind turbine is proportional to the square of a rotor diameter and a cubic of wind speed (refer to B.7). The large turbines can capture higher wind power with lower installation and maintenance costs compared to the group of small turbines. Owing to this fact, the size of commercial wind turbines has exponentially increased over the past 30 years as demonstrated in Fig. 1.3. The turbine size increased from 50 kW in 1980 to 7.5 MW in 2010 [2,3,6]. It is anticipated that 10-15 MW turbines will be developed in the near future with rotor diameters exceeding 150 m, which is approximately twice the length of a Boeing 747 airplane. The off-shore wind turbines are also gaining more attention now-a-days because the power production can be increased with the help of stronger and steady wind.

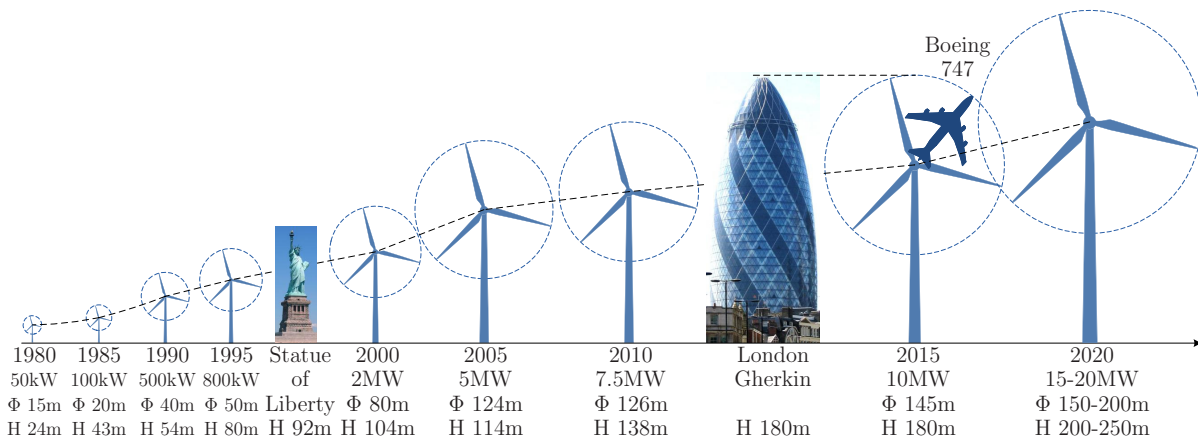


Figure 1.3: Evolution in the wind turbine size (Φ : rotor diameter, H: height).

1.1.4 Major Components of Grid-Connected WECS

The basic configuration of grid-connected MW-WECS is depicted in Fig. 1.4. The WECS is composed of several components that convert wind kinetic-energy into electric-energy in a controlled, reliable and efficient manner. The major components of a WECS can be broadly classified as mechanical and electrical. The mechanical components include tower, nacelle, rotor blades, rotor hub, gearbox, pitch drives, yaw drives, wind speed sensors, drive-train and mechanical brakes. The electrical components include electric generator, power electronic converter, generator-side harmonic filter, grid-side harmonic filter, step-up transformer and three-phase grid (collection-point).

The wind kinetic-energy is first converted to mechanical-energy with the help of rotor blades. The tower, nacelle and rotor hubs provide mechanical support to the rotor blades. The kinetic to mechanical energy conversion efficiency depends on many factors such as the shape of rotor blades, angle of blades, wind speed velocity, air density, etc. The wind velocity and direction are measured with the help of sensors, and a yaw drive is used to move the rotor blades along with nacelle towards the wind to extract the maximum possible energy. When the wind speed is more than the rated value, the pitch drives are used to change the angle of blades such that the electric power output is limited to the rated value. The MW wind turbines usually run at very low speed (typically 6-20 rpm) and high torque [2, 6].

An electric generator is used to convert rotational mechanical-energy into electric-energy. Many different wind generators such as the squirrel-cage induction generator (SCIG), wound rotor induction generator (WRIG), doubly-fed induction generator (DFIG), permanent magnet synchronous generator (PMSG) and wound rotor synchronous generator (WRSG) have

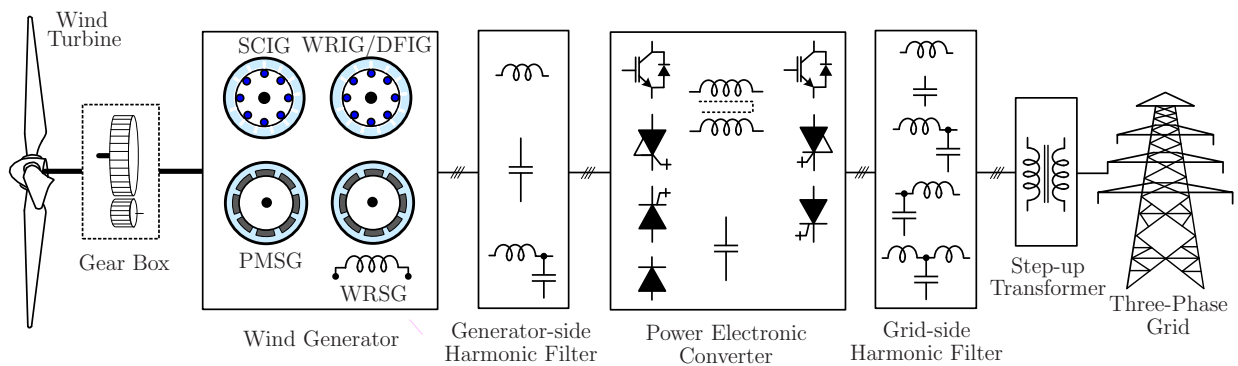


Figure 1.4: Basic configuration of a grid-connected WECS.

been developed over the past 30 years. The main features and disadvantages of each of these generators is summarized in Table 1.1.

The IG's usually operate at high rotational speeds, while the SG's can operate at low, medium or high speeds. To couple the low-speed, high-torque turbine shaft with the high-speed, low-torque IG/SG-shaft, a multi-stage (usually three-stage) gearbox is used. The gearbox presents with several serious issues such as high initial cost, high audible noise, extensive wear and tear, reduced life span, reduced efficiency and need for regular maintenance [2, 3].

The elimination of the gearbox (often referred to as gearless or direct-drive technology) helps to overcome the aforementioned problems, especially in off-shore wind turbines [7]. In recent years, many turbine manufacturers have used direct-drive technology in their commercial products. By matching the generator speed with the wind turbine speed, the need for the gearbox can be eliminated. In order to achieve lower operational speed, the generator needs to be equipped with a large number of poles, which is a feasible solution with SG's. In accommodating the large number of poles, the stator radius becomes 6 times larger and 4.5 times heavier compared to the three-stage gearbox based SCIG/WRIG/DFIG [2, 3, 8, 9]. To make a compromise between the high-speed and low-speed operation, a medium-speed SG can be used with the help of single-stage gear box. The list of few commercial turbines along with the gearbox details are given in Appendix A.

Table 1.1: Advantages and disadvantages of wind generators [source: J. A. Baroudi et. al. (2007)]

Generator	Advantages	Disadvantages
SCIG	<ul style="list-style-type: none"> • Simple and rugged in construction • Lower initial and maintenance cost • Lower torque oscillations • Widely available for MW application 	<ul style="list-style-type: none"> • Requires reactive power compensation • Large in-rush current during grid connection • Requires gearbox • Increased losses and control complexity
WRIG/ DFIG	<ul style="list-style-type: none"> • Reduced converter cost • Reduced losses and improved efficiency • Flexible reactive power compensation 	<ul style="list-style-type: none"> • High capital and maintenance cost • Slip rings are sensitive and need maintenance • Susceptible to grid disturbances
WRSG	<ul style="list-style-type: none"> • Independent active and reactive power control • High torque operation can be achieved • Eliminates the need for gearbox 	<ul style="list-style-type: none"> • High capital and maintenance cost • Requires additional excitation circuit • Huge weight if used as direct-drive
PMSG	<ul style="list-style-type: none"> • High power density with simple design • High torque operation can be achieved • Eliminates the need for slip rings, excitation and gearbox • Lower maintenance cost • Lower rotor losses and high efficiency 	<ul style="list-style-type: none"> • High capital cost due to PMs • Possible demagnetization of PMs • High weight if used as direct-drive

The generator output voltage and frequency change with respect to the wind speed. The generator can be directly coupled to the grid or it can be interfaced through a power electronic converter. As shall be detailed in Section 1.1.7, different combinations of electric generators and power electronic converters can be used to form a wide variety of WECS configurations. The switching harmonics are inevitable when using power converters, and to solve this issue, harmonic filters are used in generator- and grid-side converters. The harmonic filter on the generator side helps to reduce harmonic distortion of the generator currents and voltages. This leads to a reduction in harmonic losses incurred in the generator's magnetic core and winding. The harmonic filter in the grid-side converter helps to meet strict harmonic requirements specified by the grid codes [2, 10].

The output of the grid-side harmonic filter is connected to a three-phase grid (collection-point) through a step-up transformer. The regional classification of WECS operating voltages will be presented in Section 1.1.5. By operating the power electronic converter at collection-point voltage level, the need for the step-up transformer can be avoided.

1.1.5 Classification of WECS Operating Voltages

The definition of WECS operating voltages in the North American and European market is summarized in Table 1.2 [11]. These operating voltages are further classified according to low voltage (LV) and medium voltage (MV) operation. Due to the participation of European manufacturers in North America and vice versa, these regional classifications are becoming less important [11]. The North American collection-points are rated at 6.9/12.47/13.8/34.5 kV, while European collection-points are designed for 6.6/11/22/33 kV. The commercial wind turbines can be connected to the transmission lines through step-up transformers irrespective of the regional voltage classes.

Table 1.2: Voltage classifications by region [source: NREL (2012)]

Region	Standard	Voltage Class
Europe	IEC 60038	Low Voltage (< 1000 V) • 220, 400, 690 V
		Medium Voltage (1 – 35 kV) • 3.3, 6.6, 11, 22, 33 kV
North America	ANSI C84.1	Low Voltage (< 600 V) • 208, 120/240, 480, 575 V
		Medium Voltage (600 V–35 kV) • 2.4, 4.16, 6.9, 12.47, 13.8, 21, 34.5 kV

1.1.6 Grid Code Requirements

Due to the rapid development of wind power generation worldwide and its integration into the existing electric power system, many specific technical requirements often called as “grid codes” have been developed and regularly updated [4, 12–15]. The transmission and distribution system operators (TSOs and DSOs) of various regions and countries have defined grid codes based on the experience acquired through the operation of their power systems. These grid codes are based on the regional and geographical conditions, and they vary from one utility operator to another, and from one country to another [2]. These grid codes usually refer to large-scale wind turbines/farms which are connected to MV transmission networks [12]. These codes stipulate that despite the fluctuating and unpredictable nature of wind energy, the large wind turbines/farms should behave as active power generation units similar to the conventional power plants [4]. The main elements in grid codes include active/reactive power regulation, frequency/voltage control, power factor control, power quality, low voltage ride-through (LVRT) operation and system protection. The correct interpretation of these codes is crucial for wind turbine manufacturers as well as utility operators [16].

The grid disturbances, such as three-phase short-circuit faults, cause severe voltage drop/dips which might lead to disconnection of large-scale wind power generation units. The sudden disconnection of generation units stimulates instability of the utility network. The grid codes have dictated some special requirements such as LVRT operation to overcome the aforementioned scenario. Among all the grid codes, the LVRT, also called fault ride-through, is the major concern for the wind turbine/ power converter manufacturers. According to LVRT requirements, during grid faults, the WECS should remain connected to the grid regardless of the turbine/generator/converter configuration being used, and must supply reactive power to help the grid to recover from the voltage dip.

The TSOs and DSOs of diverse countries issued different LVRT profiles [13] as shown in Fig. 1.5. These profiles can be broadly classified into six different categories based on depth and duration of the grid voltage dips as summarized in Table 1.3. Despite their different shapes, they all share a common purpose and background, i.e., to keep the electric power system stable and secure during the grid fault conditions. Among all the LVRT profiles, the German Transmission and Distribution Utility (E.ON) regulation is likely to set the standard [17]. According to this code, the LVRT function should start when the grid voltage

falls below 90 % of its nominal value. Recently considerable research has been carried out addressing this issue [18–23].

Apart from the LVRT operation, another important requirement for WECS is that it should perform “reactive power control” similar to the conventional power plant. Many reactive power profiles are defined by diverse TSOs similar to the LVRT profiles [4, 12–15]. As an example, according to Danish grid code, when the WECS delivers rated (1.0 p.u.) active power, it should be able to supply ± 0.33 p.u. reactive power to support grid voltage. This case implies that the WECS should be able to adjust the grid power factor anywhere from 0.95 lagging to 0.95 leading when it delivers rated active power. This requirement can be easily fulfilled by properly designing the grid-side converter [2].

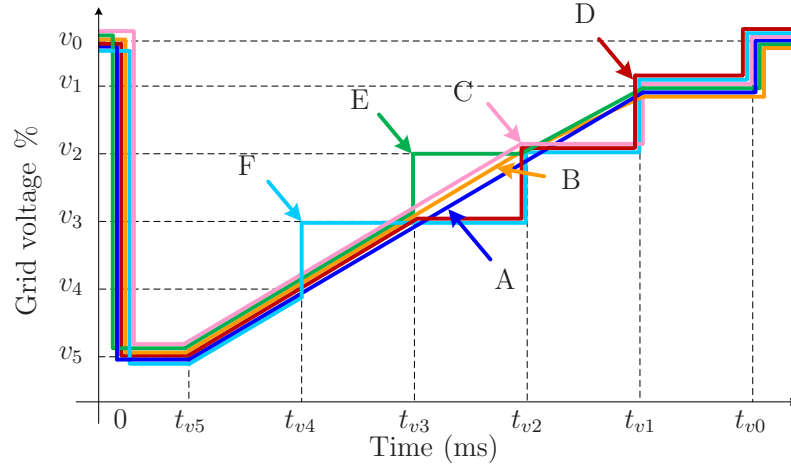
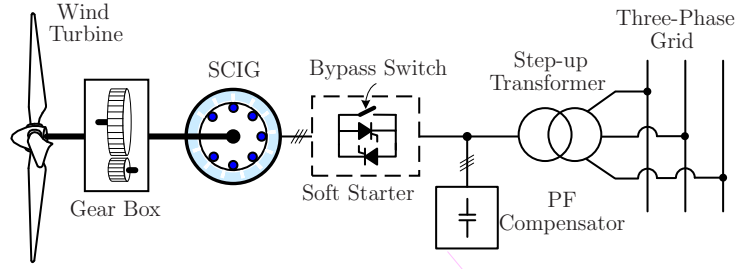


Figure 1.5: Overview of different LVRT profiles.

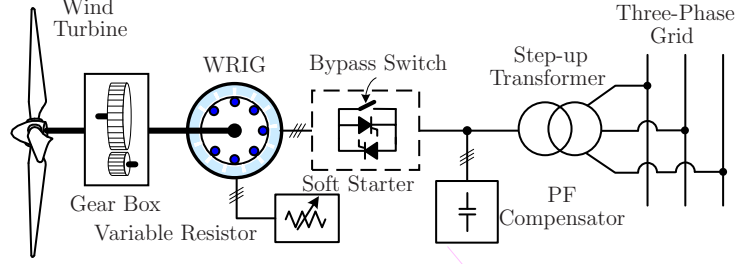
Table 1.3: Summary of national grid codes and different LVRT profiles

Pattern	Country	Grid voltages (%)						Time (ms)					
		v_0	v_1	v_2	v_3	v_4	v_5	t_{v5}	t_{v4}	t_{v3}	t_{v2}	t_{v1}	t_{v0}
A	Denmark	100	75	NA	NA	NA	25	100	NA	NA	NA	750	10000
	TSO Ireland	100	90	NA	NA	NA	15	625	NA	NA	NA	2800	—
	E. ON Germany	100	90	NA	NA	NA	0	150	NA	NA	NA	1500	—
	USA	100	90	NA	NA	NA	15	625	NA	NA	NA	2800	—
	AESO Alberta (Canada)	100	90	NA	NA	NA	15	625	NA	NA	NA	3000	—
	IESO Ontario (Canada)	100	—	NA	NA	NA	15	625	NA	NA	NA	—	—
B*	Spain	100	95	80	NA	NA	20	500	NA	NA	1000	15000	—
C	Italy	100	90	75	NA	NA	20	500	NA	NA	800	2000	—
D	Great Britain	100	90	85	80	NA	15	140	NA	1200	2500	3000	—
E	DSO Ireland	100	90	80	30	NA	15	625	NA	1000	2600	2800	—
F	Hydro Quebec (Canada)	100	90	85	75	25	0	150	1000	NA	2000	3000	—

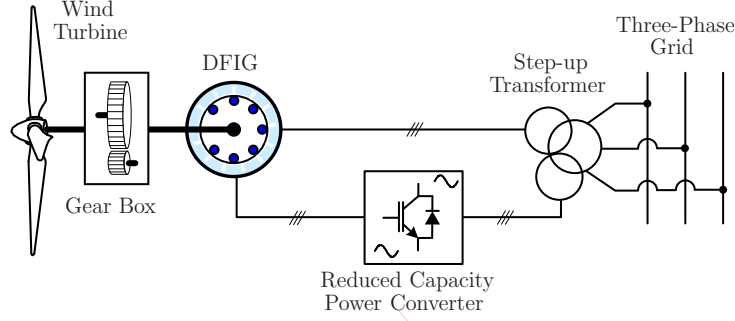
NA = Not applicable, — = Not available, * = same as A, but, with different slopes during t_{v5} to t_{v2} , and t_{v2} to t_{v1}



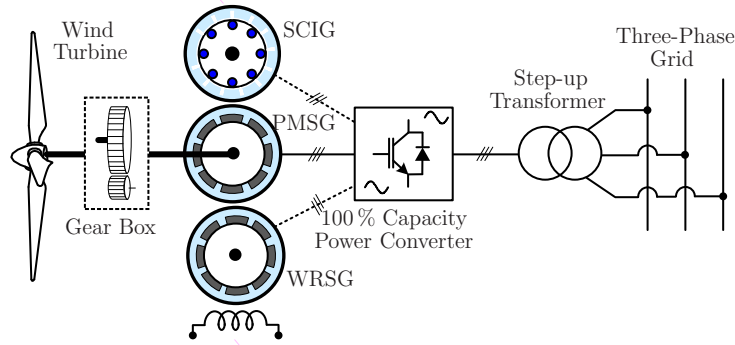
(a) Type-1: Fixed-speed ($\pm 1\%$) WECS with SCIG



(b) Type-2: Semi variable-speed ($\pm 10\%$) WECS with WRIG



(c) Type-3: Semi variable-speed ($\pm 30\%$) WECS with DFIG



(d) Type-4: Full variable-speed (0–100%) WECS with SCIG or PMSG or WRSG

Figure 1.6: State-of-the-art electric generator and power converter configurations for the commercial WECS.

1.1.7 Commercial Configurations of WECS

The major electrical components in WECS are the generator and power electronic converter. As shown in Fig. 1.6, using different designs and combinations with these two components, a wide variety of WECS configurations can be achieved such as [6, 8, 24–26]:

- **Type-1:** SCIG based WECS with $\pm 1\%$ speed-range
- **Type-2:** WRIG based WECS with $\pm 10\%$ speed-range
- **Type-3:** DFIG based WECS with $\pm 30\%$ speed-range
- **Type-4:** PMSG/WRSG/SCIG based WECS with 0–100% speed-range

A fixed-speed SCIG-based WECS without power converter interface (Type-1 turbine) is illustrated in Fig. 1.6(a), where the generator is connected to the grid through a soft starter and step-up transformer [6, 27]. The generator speed varies within 1% range at different wind speeds, and thus this configuration is called fixed-speed WECS. A gearbox is normally required to match the speed difference between the turbine and generator. After the start-up procedure, the soft-starter is bypassed by a switch, and the system essentially works without any power converter. The SCIG draws reactive power from the grid and to compensate for this, three-phase capacitor banks are usually employed [28]. This configuration features simplicity, low initial costs, and reliable operation. The major drawbacks include: (i) lower wind energy conversion efficiency, (ii) changes in the wind speed are reflected to the grid, and (iii) the grid faults cause severe stress on the mechanical components of the wind turbine [29]. The fixed-speed wind turbines are equipped with additional hardware, such as STATCOM, to comply with the grid codes [30]. Despite its drawbacks, this configuration has been accepted by the wind industry and commercial solutions are available in MW range such as (i) Vestas V82, 1.65 MW and (ii) Siemens SWT 2.3-101, 2.3 MW [2].

The variable-speed operation of the wind turbine increases the energy conversion efficiency, and reduces mechanical stress caused by wind gusts, reduces the wear-and-tear of gearbox and bearings, reduces the maintenance requirements, and increases the life cycle. The semi variable-speed WECS using WRIG and partial rated (10%) power converter is shown in Fig. 1.6(b) (Type-2 turbine). The change in the rotor resistance affects the torque/speed characteristic of the generator, enabling variable-speed operation of the turbine, and this configuration is often called Optislip control [31]. The rotor resistance is

normally made adjustable by a power converter composed of a diode-rectifier and chopper [32,33]. The speed adjustment range is typically limited to about $\pm 10\%$ of its rated speed. With variable-speed operation, the system can capture more power from the wind, but also has energy losses in the rotor resistance. This configuration also requires a gearbox, soft starter and reactive power compensation. The WRIG with variable rotor resistance has been on the market since the mid 1990's with a power rating up to a couple of megawatts. A few examples of commercial solutions are: (i) Vestas V90-3.0 MW, and (ii) Suzlon Energy S88-2.1 MW [2].

Another semi variable-speed WECS using DFIG is shown in Fig. 1.6(c) (Type-3 turbine) [34]. As the name implies, the power from the generator is fed to the grid through both stator and rotor windings [35,36]. A partial rated (30 %) power converter is employed in the rotor circuit to process the slip power, which is approximately 30 % of the rated generator power. Similar to those in Type-1 and 2 turbines, this configuration also uses the gearbox, but there is no need for a soft starter and reactive power compensation [37]. The use of the converters also allows bidirectional power flow in the rotor circuit and increases the speed range of the generator. This system features improved overall power conversion efficiency, extended speed range ($\pm 30\%$), enhanced dynamic performance and robustness against power system disturbances compared to the Type-1 and 2 turbines [38–40]. These features have made the DFIG WECS one of the dominating technologies in today's wind industry with a market share of approximately 50 % [3]. A few high power DFIG turbines are: (i) Repower 6M, 6.0 MW, (ii) Bard 5.0, 5 MW, and (iii) Acconica AW-100/3000, 3 MW [20].

The performance of WECS can be greatly enhanced with the use of full-scale (100 %) power converters as shown in Fig. 1.6(d) (Type-4 turbine) [41–46]. The PMSG, WRSG, and SCIG have all found applications in this type of configuration with a power rating of up to several megawatts [8, 26, 47, 48]. With the use of the power converter, the generator is fully decoupled from the grid, and can operate at full speed range [49–51]. This also enables the system to perform reactive power compensation and smooth grid connection [18, 21, 23, 50–52]. The main drawback is a more complex system with increased costs. The need for the gearbox can be eliminated by using a high-pole number PMSG/WRSG. This configuration is more robust against power system faults compared to the Type-1, 2 and 3 turbines [2, 14, 53, 54]. The typical commercial turbines include: (i) Enercon E126, 7.5 MW, (ii) Multibrid M5000, 5 MW, and (iii) Vestas V-112, 3 MW [2].

The top 10 wind turbine manufacturers as of Dec. 2012 and their main turbine configurations are summarized in Fig. 1.7. They account for approximately 77 % of the 45 GWs installed wind power capacity in 2012 [1, 5]. The details about the turbine configurations are obtained from the respective company product brochures and details from the previous survey papers [3, 20, 55–59]. The Type-3 turbines (DFIG) hold the highest market share and this technology has been used by 7 manufacturers among the top 10. Approximately 100 different DFIG turbine models are available from all the wind turbine manufacturers. The Type-4 turbines are produced by 6 manufacturers, while 4 of them are offering direct-drive solutions. This implies that the wind energy market is making progress towards full-scale power converters based on variable-speed technology.

The summary of all four types of turbines is given in Table 1.4. They are compared using power converters employed; speed-range achievable; requirement for soft-starter, gearbox and external reactive power compensation needed; and maximum power point tracking (MPPT) ability. Overall, the Type-4 turbines with gearless drive-train are most favorable for next generation MW-level wind turbines.

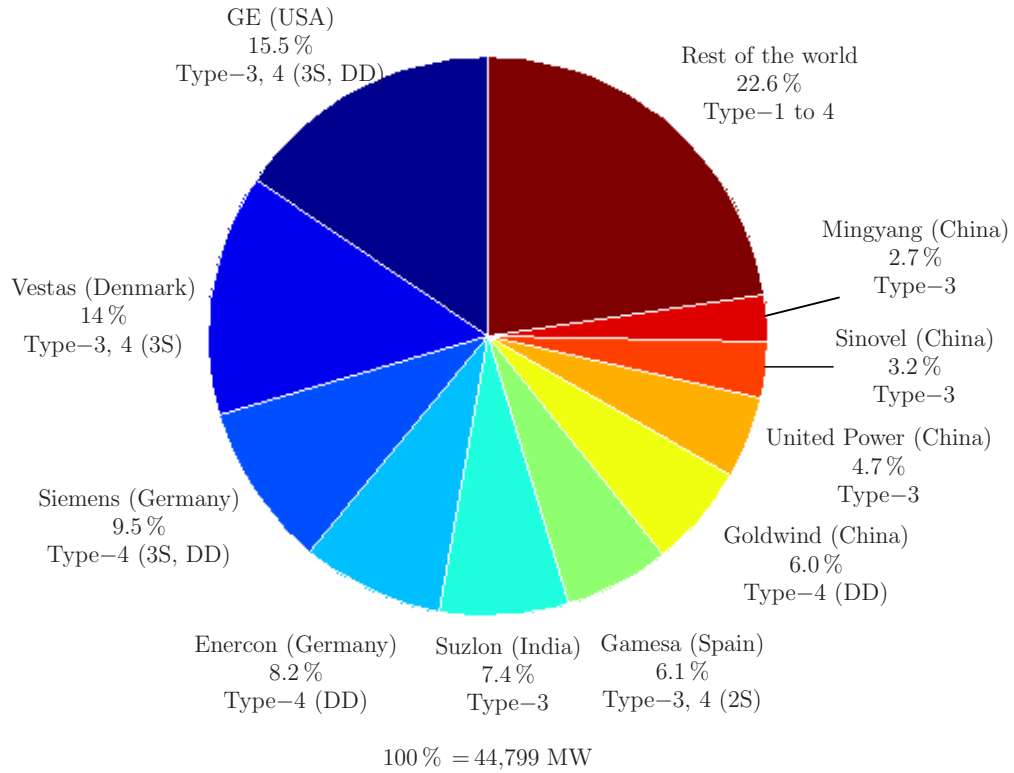


Figure 1.7: Summary of top 10 wind turbine manufacturers and their market share by Dec. 2012. [source: REN21 and GWEC] (2S/3S = two-/three-stage gearbox, DD = direct-drive).

Table 1.4: Summary of four types of wind turbine configurations

	Fixed-Speed, Type-1 Turbine	Semi-Variable Speed, Type-2 and 3 Turbines		Variable-Speed, Type-4 Turbine		
	SCIG	WRIG	DFIG	SCIG	PMSG	WRSG
Power Converter	None	Diode + Chopper	AC/DC+DC/AC (or) AC/DC+DC/DC+DC/AC (or) AC/AC			
Converter Capacity	0 %	10 %	30 %	100 %	100 %	
Speed Range	± 1 %	± 10 %	± 30 %	0–100 %	0–100 %	
Soft Starter	Required	Required	Not Required	Not Required	Not Required	
Gear Box	3–stage	3–stage	3–stage	3–stage	3– or 2– or 1– or 0–stage	
Aerodynamic Power Control	Active Stall, Stall, Pitch	Pitch	Pitch	Pitch	Pitch	
External Reactive Power Compensation	Needed	Needed	Not Needed	Not Needed	Not Needed	
MPPT Operation	Not applicable	Limited	Achievable	Achievable	Achievable	

1.2 Motivation for Dissertation Research

The motivation for this dissertation research is to study the state-of-the-art power converter configurations and control schemes, and to propose new technologies to: (1) absorb the best features of the practical technologies, (2) mitigate the problems associated with the current technologies, (3) decrease cost associated with the power converters, (4) improve wind energy conversion efficiency, and (5) achieve high-performance operation. In this section, both the power converters and control schemes are studied in detail.

1.2.1 Motivation from the Power Converters' Perspective

To enable the grid connection of Type-4 wind turbines, the variable voltage/frequency of the wind generator should be converted to fixed voltage/frequency. To accomplish this, a wide variety of power conversion stages can be employed as summarized in Fig. 1.8. Some of these configurations are adopted from the electric drives industry, while some other topologies have been proposed in literature with promising features for future development. A detailed discussion about these converters will be presented in Chapter 2. The most common full-scale converters employed in the present PMSG wind turbines are summarized in Fig. 1.9. This classification is carried out based on low voltage (LV) versus medium voltage (MV) operation, and generator-side active (PWM) converters versus passive converters. A list of the few commercial wind turbines employing these converters is given in Table 1.5.

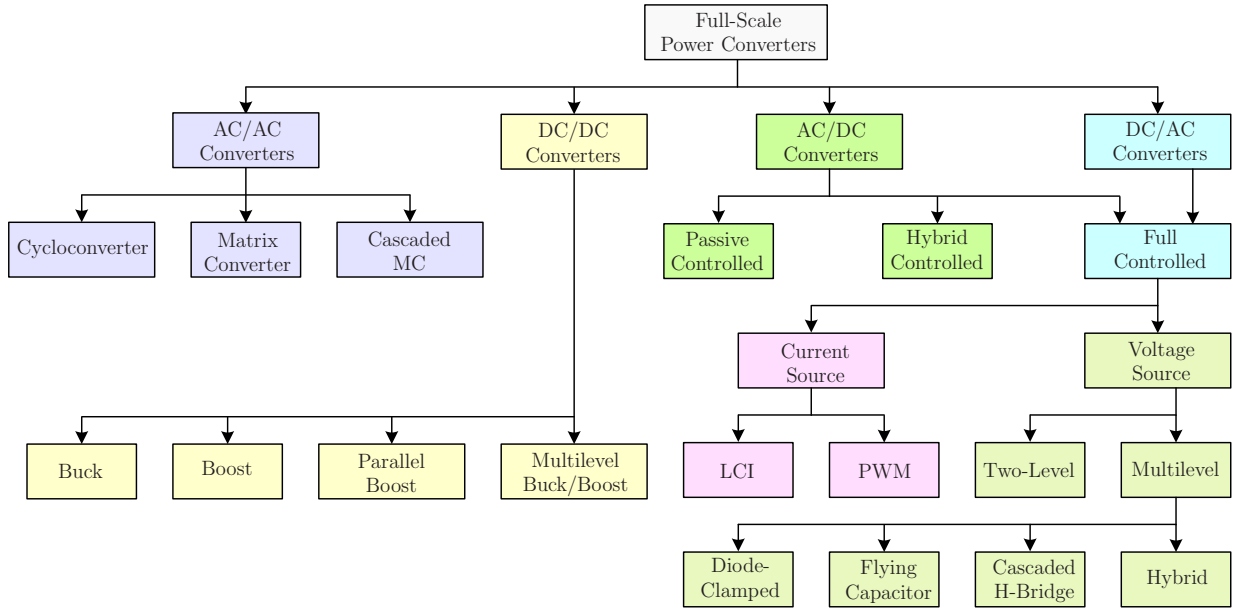


Figure 1.8: Classification of full-scale power converters used in Type-4 wind turbines.

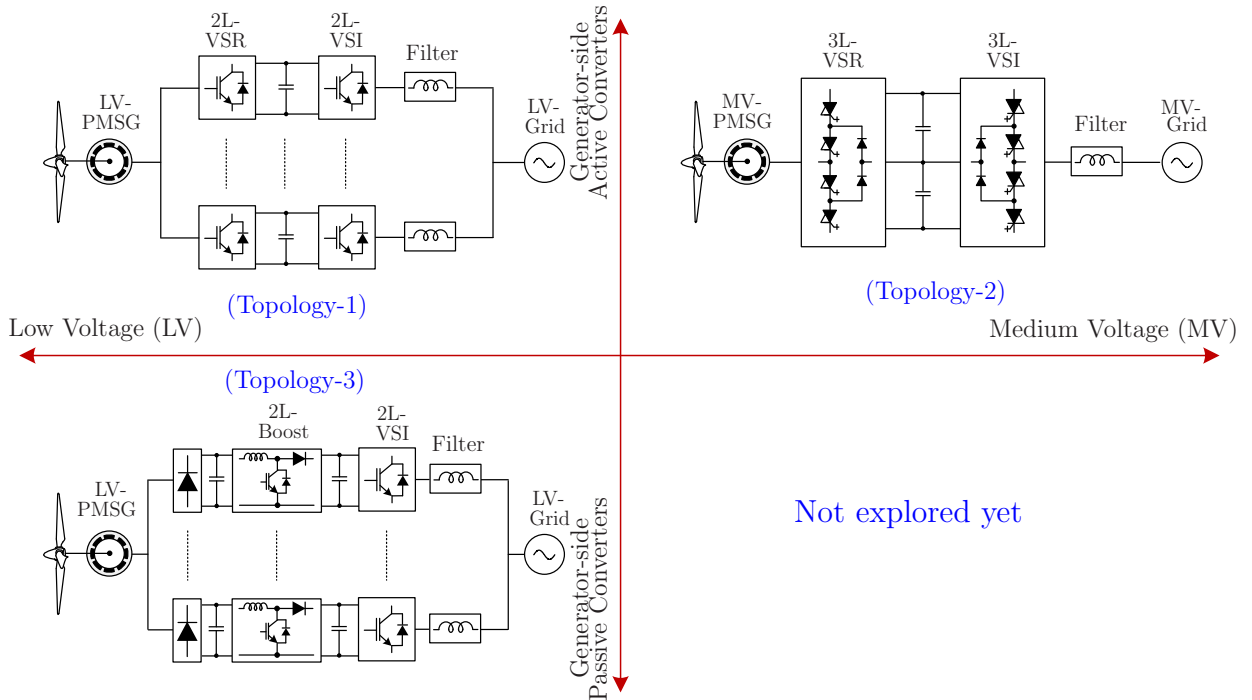


Figure 1.9: Review of commercial power converters for PMSG-WECS.

Table 1.5: List of few commercial PMSG wind turbines

Manufacturer	Model	Rating	Topology
Enercon	E126	7.5 MW, 690 V	1
Gamesa	G128	4.5 MW, 690 V	
Winwind	WWD3	3.0 MW, 660 V	
GE	2.5XL	2.5 MW, 690 V	
Avantis	AV928	2.5 MW, 690 V	
Areva	M5000	5.0 MW, 3300 V	2
Converteam [•]	MV7000	7.0 MW, 3300 V	
ABB [•]	PCS6000	6.0 MW, 3300 V	
Clipper [†]	C89	2.5 MW, 690 V	3
Vensys	V70/77	1.5 MW, 690 V	
Goldwind	GW70/77	1.5 MW, 690 V	

• = Converter suppliers, † = Without boost converter

The LV (typical rating is 690 V) two-level (2L) back-to-back (BTB) connected voltage source converters (VSCs) [43] (Topology-1 of Fig. 1.9) configuration is very popular and this technology is successfully applied by many manufacturers as summarized in Table 1.5. The voltage source rectifier (VSR) and voltage source inverter (VSI) are linked through a dc-link and thus decoupled operation can be achieved.

At higher power levels, the use of MV (typically 3-4 kV) converters offers many benefits over LV converters: reduced voltage ratings for the switches, better grid code compliance and higher efficiency [60, 61]. A detailed comparison between LV and MV operation of WECS will be presented in Chapter 2. Currently only one MV turbine is operational, using BTB 3L-VSCs (most popularly known as neutral-point clamped (NPC) converters) (Topology-2 of Fig. 1.9) [45, 62–67], but many manufacturers have announced their future projects based on MV technology (refer to Appendix A).

In WECS, the power flow is always unidirectional, i.e., from the generator to grid. To decrease the cost and complexity of the system, passive converters can be used at the generator-side instead of active converters, as shown in Topology 3 of Fig. 1.9. The passive converters are more reliable and economical compared to the generator-side active converters [68]. These active and passive generator-side converters will be compared in more detail in Chapter 2. The use of passive converters is feasible with the PMSG generation system as the machine does not need magnetizing current [47]. This technology is also being used by many manufacturers at the LV-level as summarized in Table 1.5.

As shown in Fig. 1.9, for MV-PMSG-WECS, the use of passive generator-side converters have not been explored yet. This gap in the commercial power converters is the motivation for the first direction explored by this dissertation research.

1.2.2 Motivation from the Control Schemes' Perspective

As mentioned earlier, development of sophisticated control schemes is crucial in increasing WECS efficiency and to comply with the grid code requirements. The development of control techniques for the power converters is an ongoing research topic. A summary of the most established control techniques is summarized in Fig. 1.10. The classical control methods include hysteresis and linear control, while the sliding-mode, intelligent and predictive control methods belong to the advanced control category.

The classical control techniques are widely accepted by the power electronics and wind energy industry. Many scholarly works have been presented based on classical control techniques for the multilevel converters based WECS [2, 14, 67, 69–73]. The classical control approach uses cascaded linear PI regulators and pulse width/ space vector modulation (PWM/SVM). The favorable approach to using the classical control method with PWM/SVM is fixed switching frequency. The lower switching frequency operation is an important requirement at MW-level to minimize switching losses. During such a condition, the classical control techniques impose several technical/operational challenges such as:

- Non-symmetrical performance characteristics due to the predominant nonlinear nature of power converters

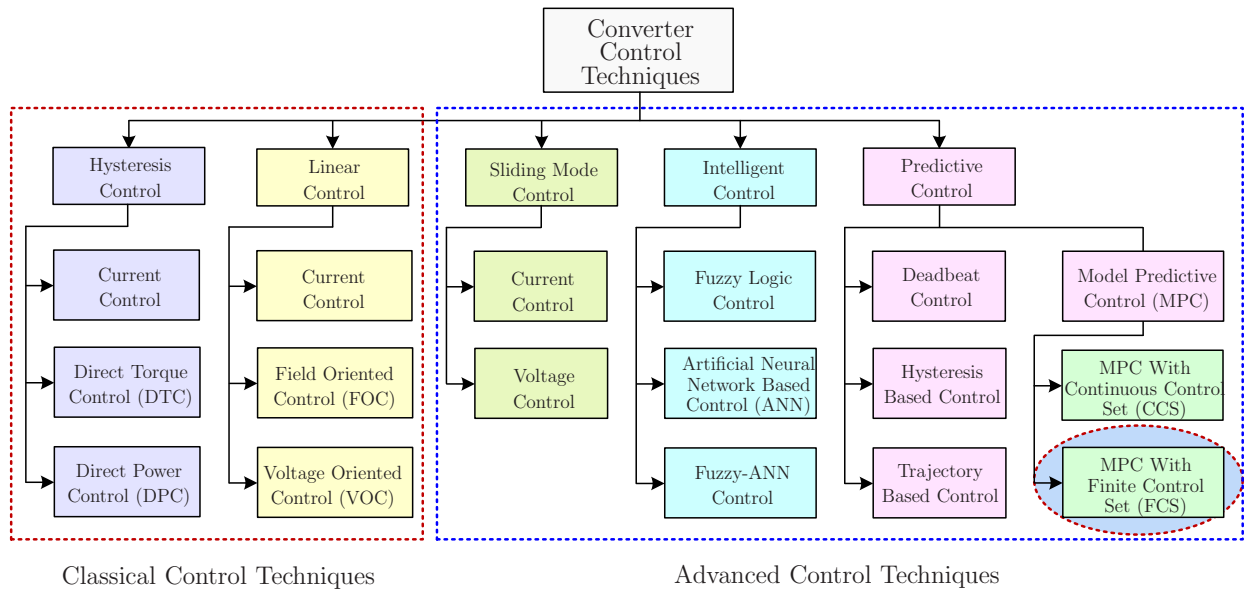


Figure 1.10: Classification of control techniques used for the power converters.

- Significant lower order harmonics which cause poor power quality and conflict to the grid codes [74]
- Sluggish transient response due to low-bandwidth modulation stage [75]
- Coupling of control variables such as d - and q -axis grid currents
- Degraded performance due to the grid voltage harmonics and control delay [76]
- Complicated approach to include system constraints in the design of controller [77]

The family of predictive control (PC) techniques includes deadbeat PC, hysteresis-based PC, trajectory-based PC and model-based PC (MPC) [78]. Recently, a finite control-set model predictive control (FCS-MPC) strategy appeared as an intuitive and promising alternative to control the power converters [75, 77, 79], and this method eliminates the need for linear regulators and modulators. The FCS-MPC is a nonlinear control method and provides a better suited approach to control the power converters while mitigating the aforementioned disadvantages associated with the classical control method [80, 81]. With an appropriate definition of cost function, several constraints and technical requirements can be incorporated in a straight-forward manner to the design and operation of the controller. The cost which is paid to use FCS-MPC is a higher computational burden, but the modern digital signal processors can perform large amount of calculations at low cost.

Most scholarly works on predictive control are related to the power electronics and motor drive applications. The modeling, design and analysis of the FCS-MPC strategy for the power converters employed in the MW-WECS have not been studied yet. Despite the simple and attractive nature of FCS-MPC strategy, several challenges exist in the state-of-the-art research which includes, but is not limited to: (1) accurate modeling of multilevel converters, (2) appropriate selection of weighting factors, (3) control delay compensation, (4) accurate extrapolation of references, (5) control of variable switching frequency nature, (6) prediction of variables over two samples with reduced computational burden, and (7) enhancement of robustness. All these issues have been motivations to investigate the high-performance FCS-MPC strategy for megawatt wind energy systems.

1.3 Dissertation Objectives

The target application for this dissertation research is DD-PMSG based MV-MW wind turbines. As summarized in Fig. 1.11, the research directions for this dissertation are twofold: the first one is to investigate next generation power converters; and the second one is to explore high-performance control schemes.

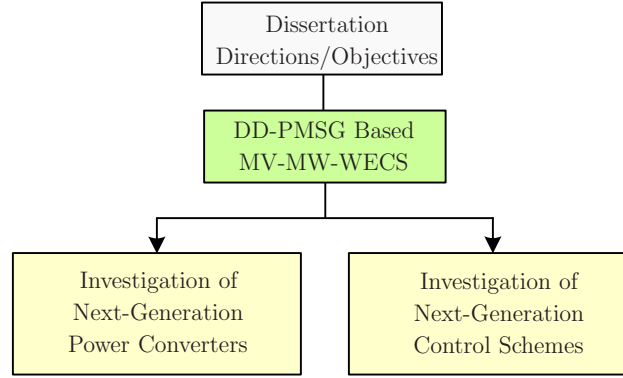


Figure 1.11: Summary of dissertation research directions and objectives.

1.3.1 Investigation of Next-Generation Power Converters

The first direction for the dissertation objectives is to investigate the next-generation power converters. The initiative of this work is to combine the advantages of proven wind turbine technologies (listed in Fig. 1.9) such as low-cost generator-side passive converters and efficient grid-side multilevel converters.

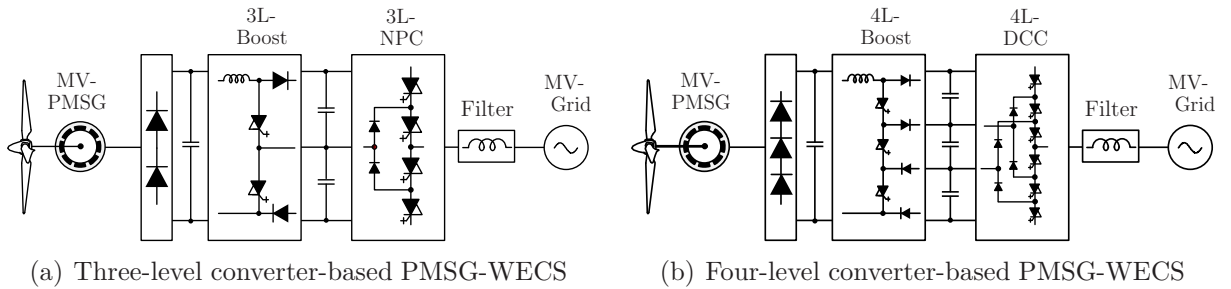


Figure 1.12: Next-generation power converters for the MW-MV-PMSG-WECS.

The dissertation objectives in this regard are summarized as follows:

1) Investigation of novel power converters for 3–4 kV class WECS

As demonstrated in Fig. 1.12(a), a diode rectifier, three-level boost (TLB) converter and neutral-point-clamped (NPC) inverter can be used for 3–4 kV class WECS without connecting the switching devices in a series. This configuration would be very promising if the dc-link capacitor voltages were balanced during all the operating conditions with the help of a TLB converter. This feature would help to simplify the control system for the NPC inverter while improving the grid current shape compared to the BTB-NPC converters.

The first objective is to investigate the feasibility of applying this configuration in megawatt wind energy systems, and to compare its performance with the BTB-NPC converters. Further studies must be performed to investigate the performance of converters during grid fault conditions. The maximum power point tracking (MPPT) must also be investigated with this configuration.

2) Investigation of novel power converters for 4–10 kV class WECS

Unlike the MV drives, which are fed by standard utility voltages of 2.3, 3.3, 4.16, 6.0, 6.6, 6.9, 7.2, 10, 11 and 13.8 kV, there is no such standard for wind turbines. To meet the future generation of 4–10 kV class WECS (as defined in [82]), four-level converters can be used as shown in Fig. 1.12(b). The requirement for the step-up transformer can be eliminated by directly connecting the wind turbine to 4–10 kV three-phase grid (collection-point). Compared to the three-level converters, the requirement for the grid-side filter is lower to achieve similar levels of grid power quality. Balancing the dc-link capacitor voltages is difficult with the four-level converters compared to three-level converters [83, 84]. However, similar to the TLB converter, the four-level boost (FLB) converter can balance the dc-link capacitor voltages during all the operating conditions.

In addition to the aforementioned objectives, the feasibility and performance of the four-level converters should be analyzed for wind energy application. The objectives are extended to compare the performance of four-level converters with the three-level converters [Fig. 1.12(a)] and BTB-NPC converters.

1.3.2 Investigation of Next-Generation Control Schemes

The FCS-MPC method is anticipated to be one of the next generation control tools, and thus is considered secondary subject matter for this dissertation. The main objectives with respect to the development of control schemes for the megawatt WECS are summarized as follows:

3) Continuous- and discrete-time modeling of power converters and WECS

The optimal control actions of the predictive control strategy are mainly based on the model of the system. A poor modeling of the system will lead to an inferior control performance. The continuous-time models should be converted to discrete-time with a suitable method such that control delay and prediction horizon can be incorporated.

In this work, the third objective is set to accurately model different control variables in terms of converter switching states.

4) Performance improvement of predictive control strategy

Despite many best features of FCS-MPC strategy, several challenges are reported in the state-of-the-art literature. A few examples include: weighting factors selection, control delay compensation, accurate extrapolation of reference control variables, variable switching frequency nature, prediction of variables over two or more samples with reduced computational burden, and enhancement of robustness against perturbations in the system model.

In this dissertation, the next objective is defined to address the above challenges, and to promote the FCS-MPC strategy as the one of the next generation control tools.

5) Development of generalized control strategy for multilevel diode-clamped converters (MLDCCs)

In this work, 3L and 4L converters are proposed for the MW-WECS, and thus the control scheme developed for one converter should work for the other, too. In classical control (which is a mature subject matter), many works have been presented to generalize the control of load current, dc-link capacitor voltages and common-mode voltage in MLDCCs. But in the current predictive control research area, this issue is not addressed yet.

Development of a generalized approach for the predictive control of MLDCCs is defined as the next objective. All the control goals must be treated in the modeling and design of the controller.

6) Development of efficient controllers for the grid-tied MLDCCs

The grid-tied MLDCCs play a crucial role in dispatching wind power and also to meet grid codes. The control techniques for the grid-side converter should perform multiple tasks to ensure proper and reliable operation of WECS.

The next objective is specified to design efficient controllers such that grid-tied MLDCC control requirements such as net dc-bus voltage/grid active power control, reactive power generation to meet grid operator request, dc-link capacitor voltages balancing, and lower switching frequency operation can be fulfilled simultaneously.

7) Design of decoupled control system for the PMSG-WECS

In order to achieve decoupled operation for the generator- and grid-side converters, the control systems should be properly designed. In addition to the aforementioned grid-side control requirements, the MPPT operation should be performed by the generator-side converter. The control systems should generate reference control variables in order for the WECS to operate at higher efficiency.

The next objective of this work is the design and implementation of sophisticated control systems for efficient operation of three-level and four-level converter-based WECS.

8) LVRT enhancement for the proposed WECS using FCS-MPC strategy

The state-of-the-art LVRT solutions for PMSG-WECS include pitch control system, over sizing of dc-link capacitors, dissipation of surplus energy in dc-link crowbar (resistor), storage of surplus energy in the battery banks and fly-wheel systems, use of power quality conditioning devices. The surplus energy can be stored in the mechanical system inertia during the grid voltage dips, and this issue is previously analyzed with CSC and NPC converters, and with classical control techniques. The complete WECS response with passive generator-side converters has not been explored yet.

The last objective is defined to develop a FCS-MPC control system such that the power converters operate in a safe mode (by maintaining constant dc-bus voltage), while meeting the grid code requirements.

1.4 Outline of Dissertation

The research presented in this dissertation is organized into 10 chapters. The outline of the research is summarized in Fig. 1.13. The work carried out in each chapter is summarized as follows:

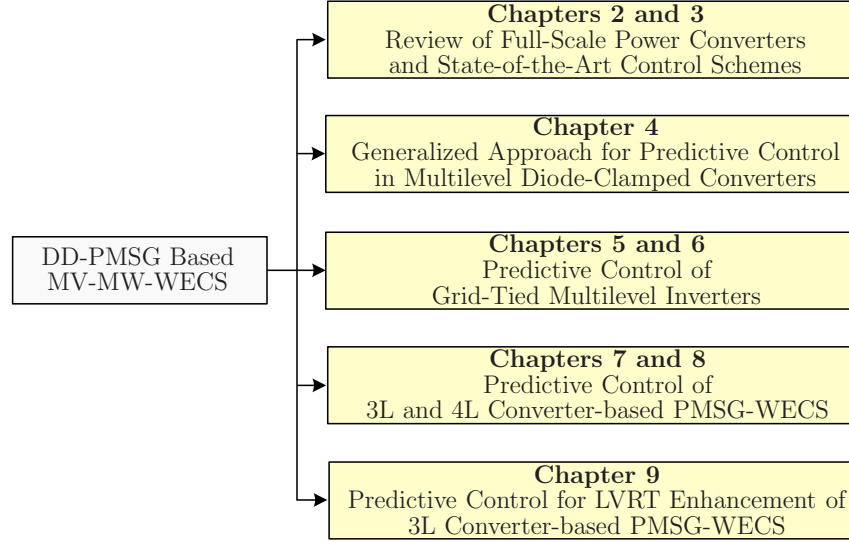


Figure 1.13: Organization of dissertation research.

Chapter–1: An overview of WECS is presented with additional details about major components of wind turbines, regional classification of operating voltages, grid code requirements and generator-converter configurations. Novel converters are investigated by combining the generator-side passive converters and grid-side multilevel inverters.

Chapter–2: This chapter reviews the state-of-the-art full-scale power converters employed in the Type-4 wind turbines. The BTB converters, passive generator-side converters, and converters for six-phase and open winding generators are presented and analyzed for megawatt application. The possible extensions to the proposed converters are also presented in each category.

Chapter–3: An overview of state-of-the-art converter control schemes are presented in this chapter and compared based on a simple example of load current control. The operating principle, design procedure, cost function flexibility, delay compensation strategies and extrapolation methods are presented for the FCS-MPC strategy.

Chapter–4: This chapter proposes a generalized approach based on FCS-MPC strategy for the current control, dc-link capacitor voltages balancing, switching frequency reduction and common-mode voltage mitigation in multilevel diode-clamped converters. The feasibility of the proposed method is verified by simulations in 3L- to 6L-converters, and by experiments in 3L- and 4L-converters.

Chapter–5: In this chapter, a model predictive control of MV, grid-tied 4L-inverter for use in MW-WECS is presented, assuming that the MPPT is performed by the generator-side converter. The regulation of net dc-bus voltage, reactive power generation to meet the grid operator request, dc-link capacitor voltages balancing, and switching frequency minimization, is discussed in detail.

Chapter–6: A FCS-MPC method is proposed in this chapter to directly control the active and reactive grid powers assuming that the grid-tied inverter performs the MPPT operation.

Chapter–7: This chapter introduces a three-level converter-based MV-MW-PMSG-WECS. The discrete-time modeling and control scheme development are discussed. The proposed topology and control strategy are verified through MATLAB simulations on 3 MW/3000 V/577 A system and dSPACE DS1103 based experiments on 3.6 kW/208 V/10 A prototype.

Chapter–8: The four-level converter-based WECS is presented in this chapter. The continuous- and discrete-time modeling of the proposed power conversion system is presented and analyzed. A two-step predictive scheme is developed to control the generator- and grid-side converters independently.

Chapter–9: In this chapter, a predictive control scheme is proposed for LVRT enhancement of DD-PMSG based MW-WECS. The power conversion system is realized using the three-level converters introduced in Chapter-7. Simulation and experimental results are presented to validate the proposed strategy.

Chapter–10: The main contributions of this dissertation are summarized. Possible extensions to the research presented in this dissertation are suggested.

Chapter 2

Review of Power Converters for High Power Wind Turbines

Many generator-converter configurations were developed over the past decades with the aim of increasing WECS efficiency, decreasing production costs and complying with grid code requirements. A summary of different power conversion stages has been previously analyzed in Fig. 1.8. The classification of wind turbine power converters is a complex matter and it is not possible to classify all the converters based on one parameter/operation. As shown in Fig. 2.1, the converter configurations are classified here into four different groups to facilitate easier discussion. Most of the power conversion stages have found commercial applications, and some have been proposed in the literature with promising features for future development. Based on the existing knowledge, new converter configurations are also proposed in each category.

The power converters discussed in the Fig. 1.8 can be employed with the PMSG and WRSG, but SCIG has restrictions on using passive generator-side converters. The gearbox model is not shown in all the figures, but a 3-stage gearbox is mandatory for SCIG. The main features and drawbacks of each configuration are also discussed in the following sections, with important survey results tabulated.

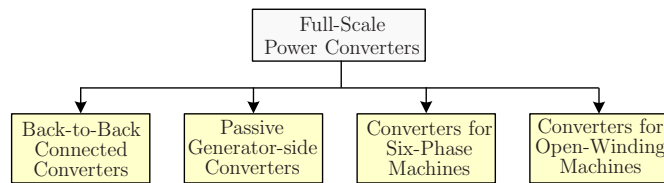


Figure 2.1: Classification employed in this chapter for full-scale power converters.

2.1 Back-to-Back Connected Converters

The power converters, which are identical on both the generator- and grid-side, and linked through a dc-link, are classified as back-to-back (BTB) connected converters. Different BTB converters which can be used in the commercial WECS are summarized in Fig. 2.2. They perform a conversion of variable voltage/frequency output of the generator to dc, and then dc to ac, with fixed voltage/frequency for the grid connection. The power flow is bidirectional, and thus the BTB converters can be used with SCIG, PMSG and WRSG. The BTB converters are classified as low voltage (< 1 kV) and medium voltage (1 – 35 kV) converters according to IEC 60038 standard given in Table 1.2. The most standard voltages used by many commercial wind turbine manufacturers for the LV grid connection are 690 V and 575 V.

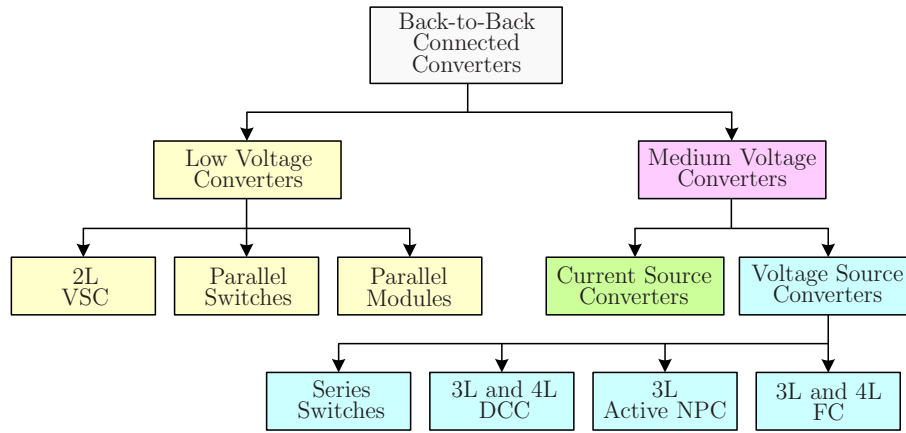


Figure 2.2: Classification of back-to-back connected converters.

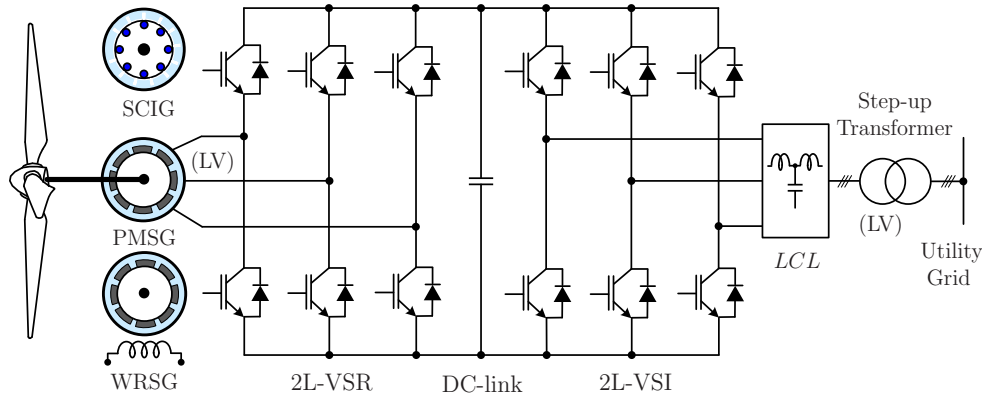


Figure 2.3: WECS with BTB connected 2L voltage source converters.

2.1.1 Low Voltage (LV) Converters

A typical WECS using BTB connected two-level (2L) voltage source converters (VSCs) is shown in Fig. 2.3 [41, 85]. The voltage source rectifier (VSR) and voltage source inverter (VSI) are linked by a dc-link composed of series/parallel connected capacitors [86]. The dc-link capacitors provide decoupling between the generator and grid, and thus the transients in the generator do not appear on the grid-side [42, 86]. The semiconductor switching devices are realized using LV Insulated Gate Bipolar Transistors (LV-IGBTs). The PMSG, WRSG [41, 85] and SCIG [87, 88] generators can be used with this configuration. This is the most widely used topology for high power wind turbines rated below 0.75 MW [2].

The switching frequency of VSR and VSI is maintained at 1–3 kHz to achieve lower switching losses [41, 66]. The grid current contains higher total harmonic distortion, and to meet the grid codes, *LCL* filters are used on the grid-side [10]. The generator-side harmonic filter is not shown. Due to the mass production of three-phase converter modules, the cost of these converters is low. One of the most widely used commercial VSC modules is SKiiP by Semikron which is equipped with its own heat sink, semiconductor switching devices and gate drivers, and thus they feature compact design with high power density [89, 90].

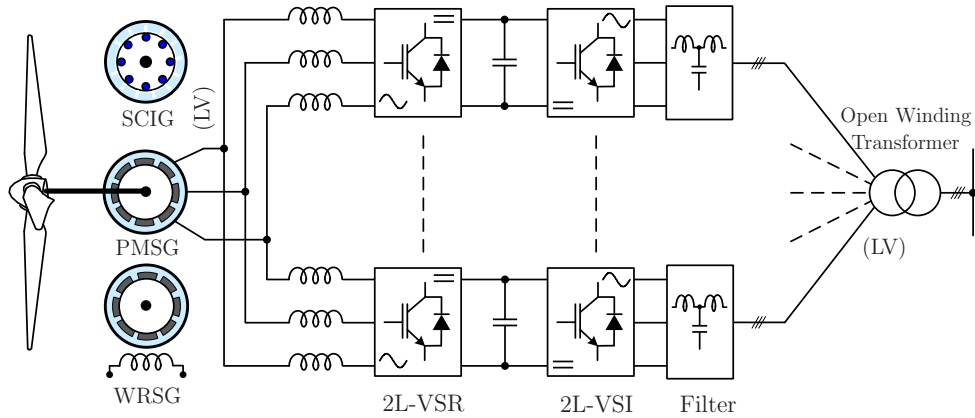


Figure 2.4: Parallel connected BTB 2L-VSCs and open winding transformer.

For power ratings greater than 0.75 MW, the current carrying capability can be increased by connecting IGBT modules in parallel. Some manufacturers such as Semikron provide IGBT modules for the parallel operation in order to reach megawatt-level [2, 90]. This configuration leads to derating of the power converter due to a mismatch in IGBT characteristics and non-symmetrical layout of the converter circuits. To minimize the circu-

lating currents among the switches, many design considerations such as static and dynamic sharing of IGBT's, and physical layout of gate drivers, IGBT modules and dc-link capacitors, should be properly treated. The circulating currents flow through the IGBT switches, increase losses in them and perhaps damage them.

To avoid the above-mentioned problems, the three-phase VSC converters along with harmonic filters can be connected in parallel instead of through IGBT modules. For example, two BTB VSC modules can be connected in parallel to achieve a power rating of 1.5 MW. For higher power ratings, more converter modules can be connected in parallel as shown in Fig. 2.4. The dc-link can also be configured as a common element for all the converters to reduce cost and space [91]. This configuration offers energy efficiency and redundancy. For example, when the wind speed is low, one or more converters can be turned-off leading to higher system efficiency. When a converter fails, other converters can still deliver the power, but with reduced capacity. Moreover, by operating converters in interleaving mode, the equivalent converter switching frequency can be increased, therefore producing less total harmonic distortion in generator- and grid-side currents. Due to a mismatch in converter and grid-side filter parameters, the circulating currents exist in both the generator and grid-side converters and this issue should be considered in the design of the controller. On the generator side, L filters are connected between each converter to reduce the circulating currents. Another alternative to reduce circulating currents is to use open-winding generators, which will be discussed in Section 2.4. To minimize the circulating currents, open winding transformers can also be used at the grid-side.

2.1.2 Medium Voltage (MV) Converters

The LV converters discussed before are efficient and cost effective at power levels lower than 3 MW. As the power rating increases, the number of converter modules increases and as a result, the size, cost and complexity of the system also increases. A summary is provided between the LV and MV operation of a 6 MW wind turbine in Table 2.1, where it has been noticed that the MV operation of WECS is the most suitable and economical approach for power ratings greater than 3 MW. The MV operation is a mature technology in the electric drive industry [92], but wind turbine manufacturers are reluctant to move from LV to MV technology due to the limited availability of MV generators and less knowledge available for the MV operation of turbines. In [11], a detailed cost analysis has been carried out between

the LV and MV operation of wind turbines, and the results show that the cost of energy production can be decreased by 2-4 % with MV operation. Currently only a few MV turbines are operational, but many manufacturers have announced their future projects based on MV technology (refer to Appendix A).

The two-level VSC shown in Fig 2.3 can also be used for MV applications by connecting the switching devices in a series. This is a simple solution for MV operation, but due to the mismatch in IGBT characteristics, the converter capacity decreases. The grid current quality does not improve compared to the standard two-level VSC, because the converter's output is essentially two-level.

Table 2.1: Summary of LV and MV operation for a 6 MW wind turbine

	LV WECS	MV WECS
Typical Converter	BTB 2L-VSC	BTB 3L-VSC
Recommended for [2]	0.5–3 MW	3–6 MW
Typical Voltage (V)	690	3000
Number of Converters	8	1
Active Switches	96	24
Switching Device [92]	LV-IGBT	MV-IGBT/IGCT IGET/GCT/SGCT
Clamping Diodes	0	12
DC Voltage (V) [2]	≈1200	≈5300
DC-link Capacitors*	8	5
Converter Complexity	High	Low
Controller Complexity	Medium	Low-Medium
Type of Generator	LV	MV
Cost of Generator	Medium	Medium-High
Rated Current (A)	5020	1155
Circulating Currents	High	None
Cable Type	LV	MV
Cable Size	Very High	Low
Cable Cost	Very High	Low
Transformer Size	High	Medium
Grid-Filter Size	High	Medium
Power Quality	Medium	Good
Grid Code Compliance	Good	Excellent
Converter Location [3]	In Nacelle	Bottom of Tower
Nacelle Weight [3]	High	Low
Converter Weight	Very High	Medium
Cost of Production [11]	100 %	96–98 %
Maintenance Cost [11]	Low	Low
Redundancy	High	Low
WECS Efficiency	Medium	High
Market Status	Mature	Available/ Emerging
Turbines	Enercon E-126	Multibrid M5000

* Based on 1200 V Rating

The neutral-point-clamped (NPC) converter has been widely studied in literature [45,61, 62,64,67,93–95]. As shown in Fig. 2.5, the NPC converters are used in commercial wind turbines, where the system power rating has reached 6 MW without connecting switching devices in series or parallel [62]. The switching devices, such as HV-IGBT or Insulated Gate-Commutated Thyristor (IGCT) with a voltage rating of 4.5–6.5 kV can be used. In the commercial wind turbines, the NPC converters are reported to have been used with the PMSG, but they can also be used with WRSG and SCIG. The switching actions of the semiconductor switches lead to the drift in the capacitor voltages. If the capacitor voltages are not balanced, it leads to higher stress on the semiconductor switches and damages them. To ensure equal voltage among the dc-link capacitors, external hardware can be used [96]. It is also possible that the carrier-based pulse with modulation (PWM) with zero-sequence voltage injection [97] or space vector modulation (SVM) with redundant switching states selection [98–105] can be used to balance the capacitor voltages.

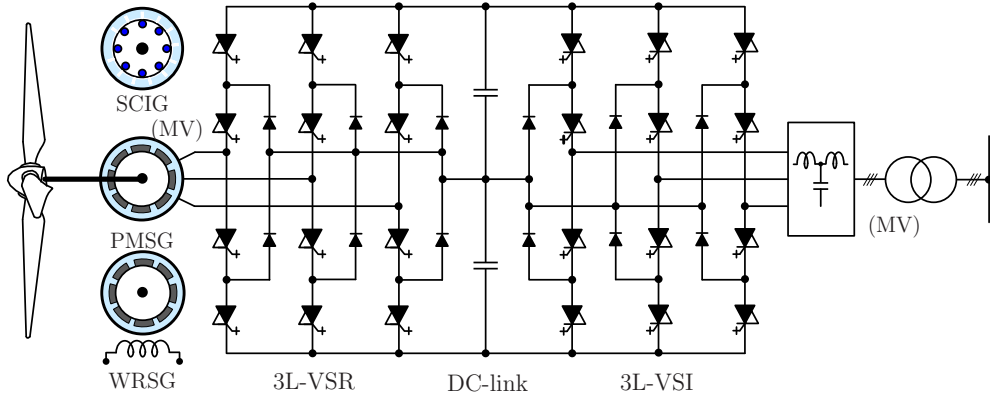


Figure 2.5: WECS with BTB connected 3L diode-clamped converters.

The NPC converters are most suitable for 3–4 kV class MV operation. To connect to the MV collection point of 6.9 kV (North America Standard) or 6.6 kV (Europe Standard) without using a step-up transformer, the switching devices in a NPC converter should be connected in a series [84,106], but this approach leads to derating the converter. As shown in Fig. 2.6, a four-level (4L) diode-clamped converter (DCC) is proposed in this work to achieve higher levels of MV operation. In comparison to the three-level (3L) DCC (NPC converter), the 4L-DCC offers added benefits such as: MV operation with greatly reduced device voltage rating, increased equivalent switching frequency, lower values for the grid-side filter, grid friendly waveforms, and better grid code compliance. However, the dc-link

capacitor voltages balancing becomes more complex and sophisticated, and therefore control techniques or external hardware should be used [81, 107, 108]. The semiconductor device count also increases. In particular, the clamping diodes increase from 12 to 36 in comparison to the BTB NPC converters. The four-level converters are not commercialized yet, but the basic power semiconductor switches are readily available in the market.

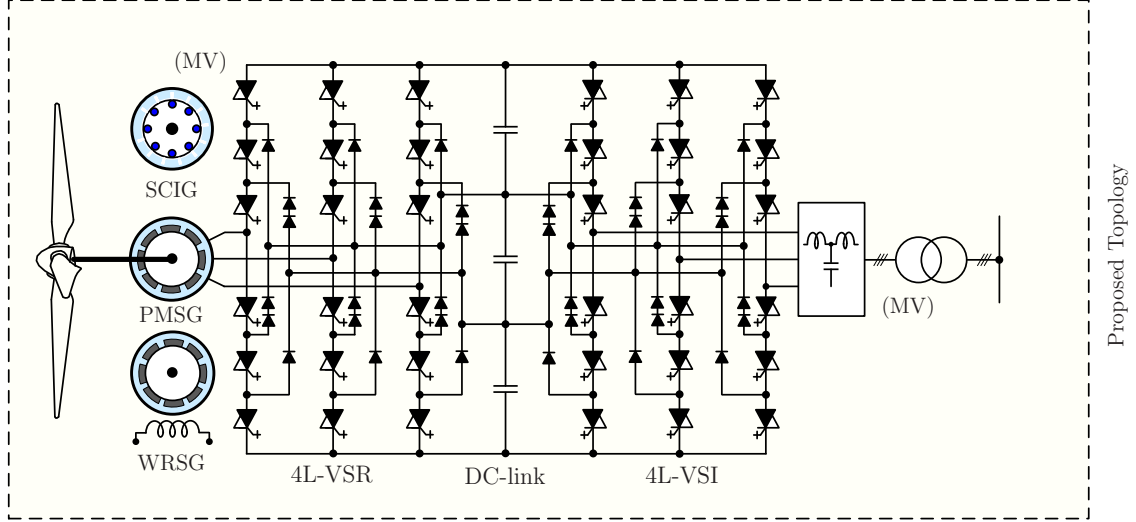


Figure 2.6: WECS with BTB connected 4L diode-clamped converters.

The semiconductor devices in the NPC converter operate with different switching frequencies and thus cause uneven power losses and heat dissipation. This leads to a difficulty in the design of the mechanical layout of the semiconductor switches. This problem can be solved by using active neutral-point clamped (ANPC) converters as discussed in [109]. This configuration is successfully applied in the MV drives industry, but not yet studied for WECS.

The clamped diodes in the BTB NPC converters can be replaced by the flying capacitors (FC) as shown in Fig. 2.8. This configuration offers a simplified structure and more redundant switching states in order to achieve easier control for the capacitor voltage balancing [110, 111]. This configuration requires a large number of capacitors and each of them requires pre-charging circuit. The diodes are more reliable than the capacitors, and thus this configuration has not found its commercial application in the wind energy industry yet, even though a successful topology in MV drives industry. The control scheme requires a greater number of sensors to send feedback signals from the FC's and these add cost and complexity to the system.

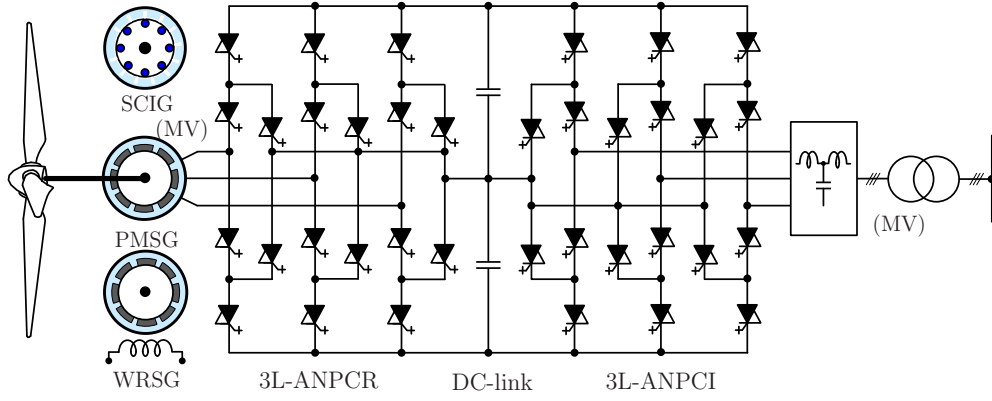


Figure 2.7: WECS with BTB connected 3L active neutral point clamped converters.

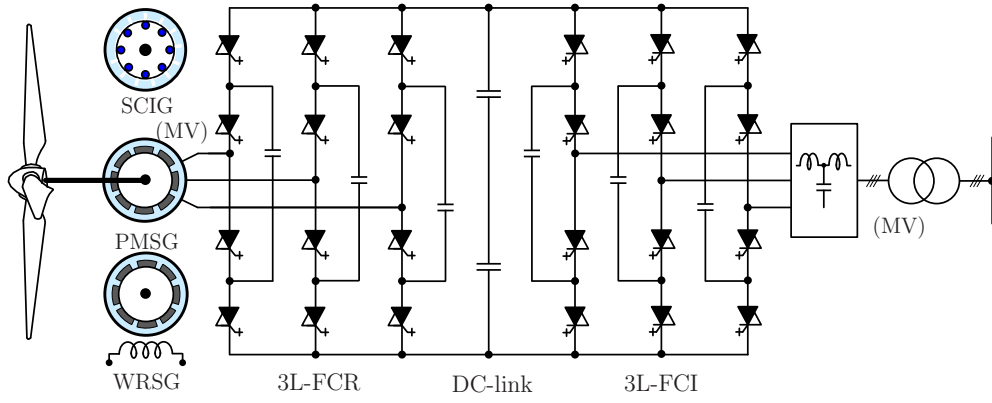


Figure 2.8: WECS with BTB connected 3L flying capacitor converters.

The previously discussed topologies belong to voltage source converters. The current source converters (CSC) can also be used in wind turbines as shown in Fig. 2.9. The topology consists of PWM current source rectifier (CSR) and current source inverter (CSI). The CSR and CSI are linked by a dc-choke and thus, similar to the VSCs, decoupling between the generator and grid can be achieved [49]. Three-phase capacitor banks are used on the ac-sides of CSR and CSI to assist the commutation of semiconductor devices and also to mitigate the switching harmonics. This topology features a simple structure, low dv/dt at the output terminals of the converter, and reliable short-circuit protection. In VSCs, the dc-link capacitors are bulky components, whereas in CSC, the dc-choke is the bulky component. The dynamic response of the CSC converters is slower compared to the VSC converters due to bulky dc-choke and lower switching frequency operation. The cost of CSC production is 1-2% lower compared to the VSC converters [11]. The CSC technology is successfully applied to the multi-megawatt MV drives [112], but it is not yet used in the MV-WECS.

2.2 Passive Generator-side Converters

The previously discussed BTB topologies enable a four-quadrant operation. But in the WECS, the power flow is unidirectional i.e., from the generator to the grid. To decrease the cost and complexity of the system, passive converters can be used at generator-side instead of PWM active converters. The diode-rectifiers are inherently more reliable than the PWM converters. It should be noted that the PMSG and WRSG do not need magnetizing current, and thus passive converters can be used [68]. The summary of comparison between the active and passive generator-side converters is given in Table 2.3. The control system development for the MPPT is less complicated with the passive converters. Due to the greatly reduced control complexity, a low cost control platform can be used. The cost and complexity associated with the gate drivers also decrease as the active switches decrease from 6 to 1. The only disadvantage with the diode rectifiers is that the generator torque contains higher ripples due to significant 5th and 7th harmonics in the generator current [113,114]. However, due to decoupling offered by the dc-link, these ripples do not cause any conflict to the grid-codes.

Table 2.3: Summary of active and passive generator-side converters for WECS

	Active Generator-side Converters	Passive Generator-side Converters
Typical Converter	VSC/CSC	Diodes
Cost	High	Low
Reliability	Medium	High
Converter Complexity	High	Low
Controller Complexity	High	Low
MPPT	Achievable	Achievable*
Generator Size	100 %	≈105 %
Gen. Torque Ripple	Low	Medium
Gen. Current	Sinusoidal	Non-Sinusoidal
Nacelle Weight	High	Low
Converter Weight	High	Medium
Maintenance Cost	Low	Very Low
Market Status	Mature	Available
Turbines	Enercon	Vensys
	E-126	V70/77

* Using Boost Converter

The WECS with diode-rectifier, boost converter and PWM inverter is shown in Fig. 2.10. The variable output voltage of the generator is converted to dc by the diode-rectifier and the boost converter performs the maximum power point tracking, which increases the energy capture and thus improves overall system efficiency [115,116]. The boost converter increases the unregulated dc-link voltage to a higher level that is suitable for the PWM inverter. To decrease the size of the dc choke, a two-channel boost converter [117] can be used as shown in Fig. 2.11. By using interleaving operation for the two channels, the inductor current ripple can be minimized. The voltage rating of the semiconductor switches is the same as of the dc-link voltage, but the current carrying capacity becomes half. The three-channel boost converters are also employed in commercial wind turbines (Vensys 70/77).

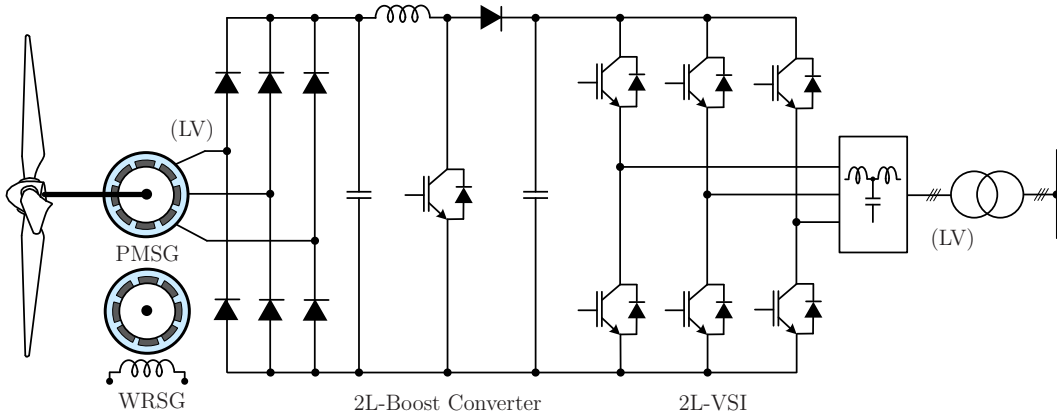


Figure 2.10: WECS with diode rectifier, 2L boost converter and 2L-VSI.

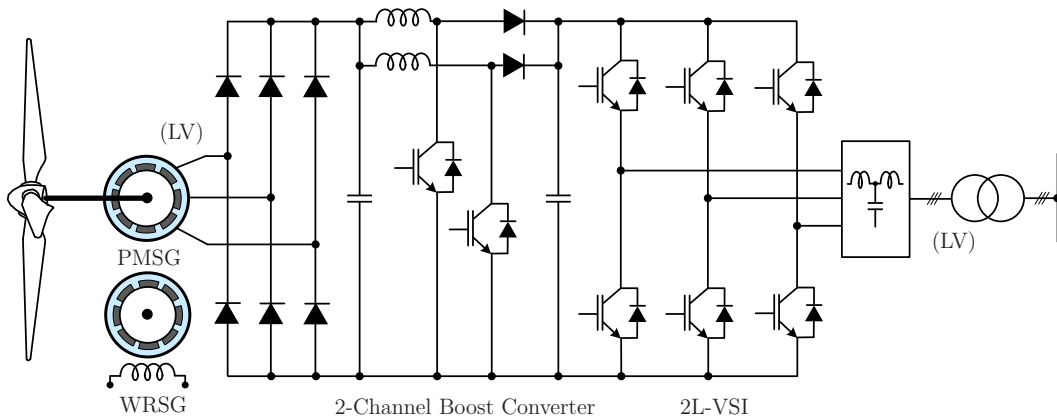


Figure 2.11: WECS with diode rectifier, two-channel boost converter and 2L-VSI.

The diode-rectifiers can also be used in MV WECS. As shown in Fig. 2.12, the generator-side NPC rectifier can be replaced with a diode-rectifier to achieve lower cost compared to the BTB NPC converters and to the parallel 2L-VSC converters. A standard two-level boost converter can be included as an intermediate stage to improve the wind energy conversion efficiency [94]. The voltage stress for the active switch and diodes used in the two-level boost converter is the same as the net dc-bus voltage, and thus they should be connected in a series.

Using the same number of active switches and diodes, the 2L-boost converter can be modified to 3L-boost converter as shown in Fig. 2.13. With this topology, the advantages of generator-side passive converters and grid-side multilevel converters are combined. The voltage rating for the IGBT/IGCT switch and diode are half of the net dc-bus voltage.

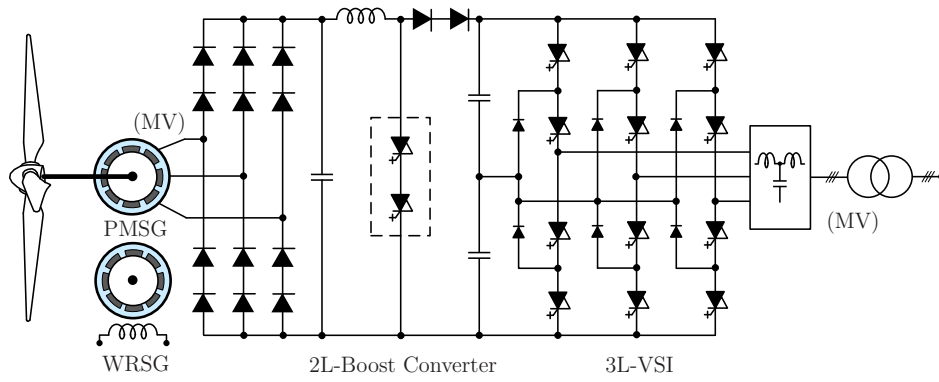


Figure 2.12: WECS with diode rectifier, 2L boost converter and 3L-VSI.

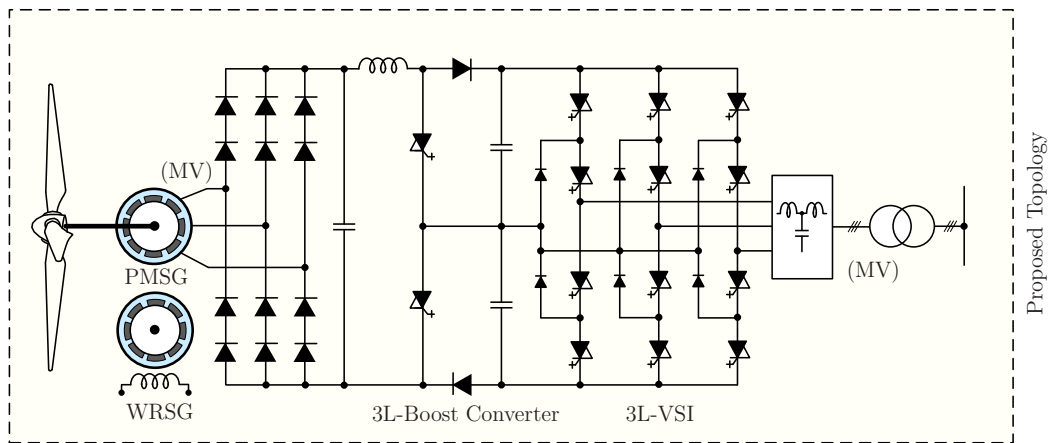


Figure 2.13: WECS with diode rectifier, 3L-boost converter and 3L-VSI.

The three-level boost converter offers many benefits compared to the standard boost converter: reduced switching losses and reduced reverse recovery losses [118]. Compared to the BTB NPC converters introduced in Fig. 2.5, the number of active switches in generator-side converter decrease from 12 to 2, and it leads to a cost-effective solution for MV turbines. The number of switching states also decrease from 27 to 4, and thus the control complexity and computational burden greatly decreases. As described in [67], in the BTB NPC converter-based WECS, both the generator- and grid-side converters should take precise switching actions so that the dc capacitor voltages are balanced. However with the proposed configuration, the dc capacitor voltages are controlled by the three-level boost converter during all the operating conditions, and this gives control flexibility for the NPC inverter to effectively track to the grid current references. This feature also leads to enhanced grid power quality and better compliance to the grid codes.

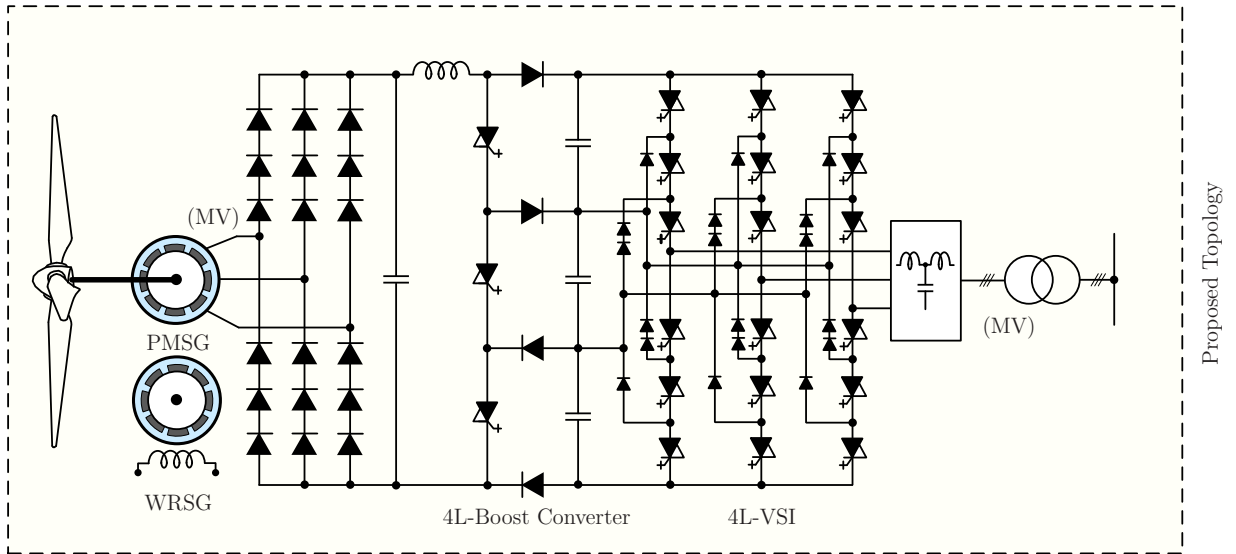


Figure 2.14: WECS with diode rectifier, 4L-boost converter and 4L-VSI.

Similar to the 3L boost converter, a 4L-boost converter can be used in conjunction with the four-level diode-clamped inverter as shown in Fig. 2.14. As mentioned earlier, the balancing of the dc-link capacitor voltages with the 4L-DCC is very complicated compared to the NPC converter [83,84]. But the intermediate 4L-boost converter ensures balancing of the dc-link capacitor voltages during all the operating conditions. The 4L-boost converter is composed of three active switches and four diodes. The voltage rating of these devices

is one third of those used in the standard boost converter. Thus the cost of this converter is approximately the same as that of a standard boost converter [119]. In comparison to the BTB 4L converters shown in Fig. 2.6, this configuration decreases the number of active switches and clamping diodes significantly in the generator-side converter. Even with the higher number of clamping diodes in the grid-side converter, the cost of this configuration becomes approximately equal to the 3L BTB converters.

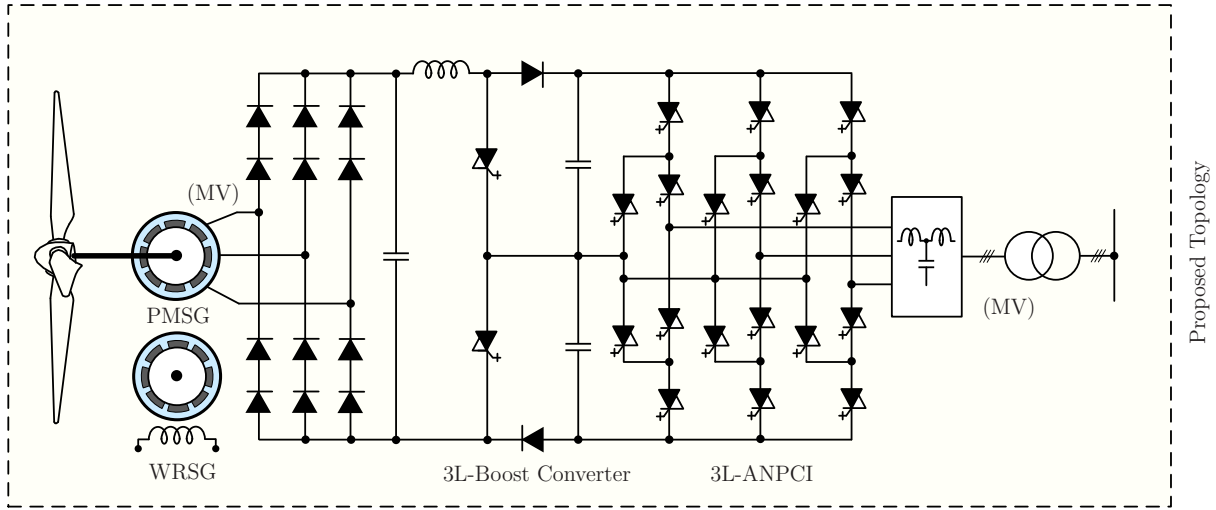


Figure 2.15: WECS with diode rectifier, 3L-boost converter and 3L-ANPCI.

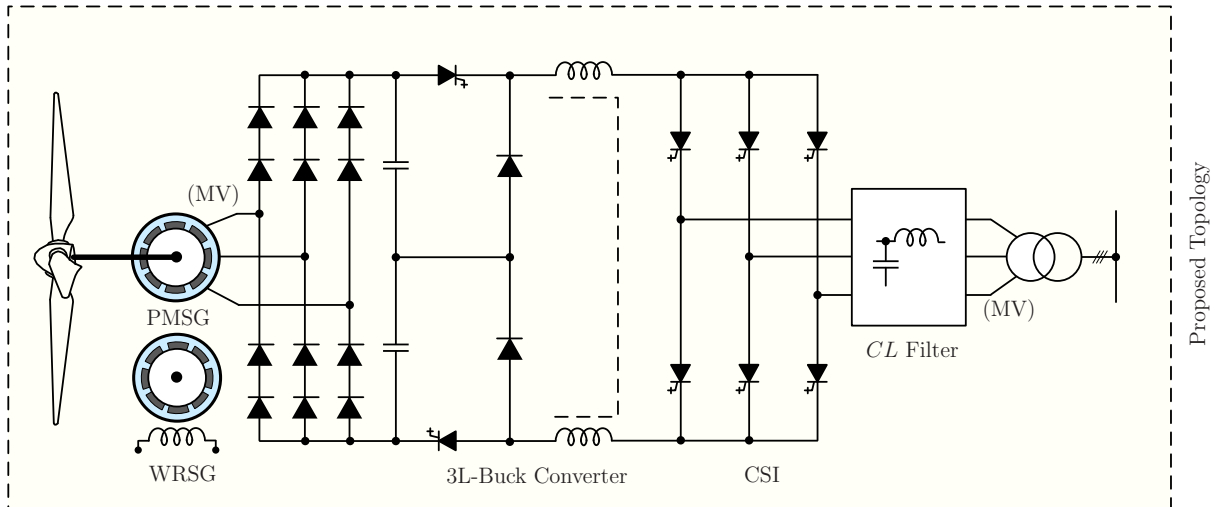


Figure 2.16: WECS with diode rectifier, 3L-buck converter and CSI.

To overcome the problem of uneven power losses and heat dissipation associated with the NPC converters, the grid-tied NPC converter can be replaced by the ANPC converter, as shown in Fig. 2.15. Since the capacitor voltages are balanced by the 3L-boost converter, the ANPC converter will have more control freedom in selecting the switching states which leads to better even power losses and heat dissipation. The cost and complexity of this configuration is much lower compared to the BTB-ANPC converters presented in Fig. 2.7.

The CSCs can also be designed with a passive generator-side converters as demonstrated in [120–122]. In VSCs the dc-link voltage should be boosted, while in CSCs, the dc-link current should be boosted. The duality of the proposed 3L-boost converter is a 3L-buck converter. The configuration using 3L-buck converter and CSI is shown in Fig. 2.16.

The high grid current quality is more important to comply with the grid codes and to achieve this 5L to 9L-ANPC converters can be used as demonstrated in [60, 123]. These configurations lead to excellent power quality and a filterless grid connection. However, in these configurations, the dc-link capacitor voltages need to be controlled by the grid-tied inverter. As mentioned earlier, this leads to higher control complexity for the grid-tied inverter. To overcome this challenge, a 3L-boost converter can be employed to directly fit the two dc-link capacitors of the grid-tied ANPC converter (shown in Fig. 2.17). In comparison to the works presented in [60, 123], the proposed configuration leads to a less complicated control scheme and grid-friendly waveforms.

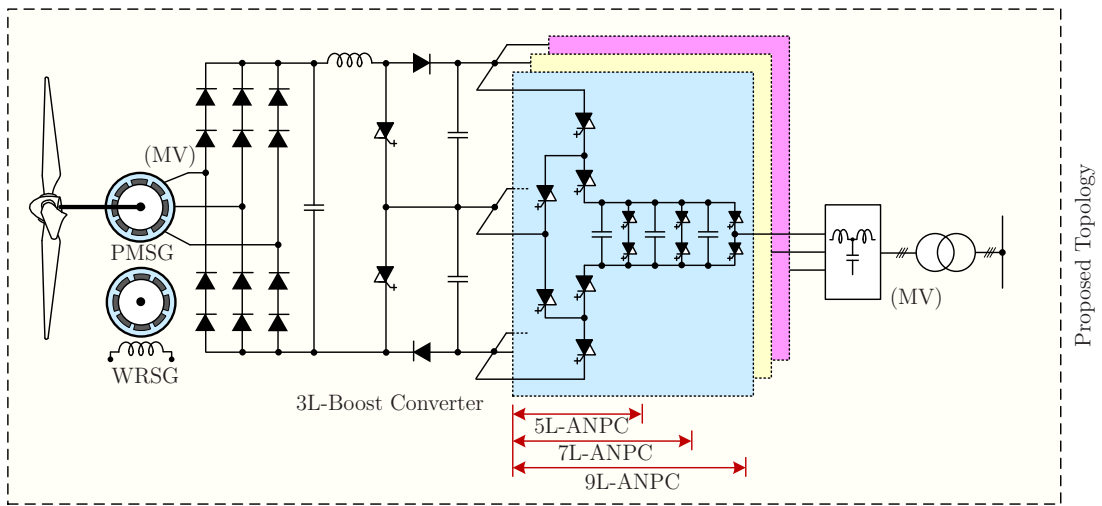


Figure 2.17: WECS with diode rectifier, 3L-boost converter and multilevel ANPC.

2.3 Converters for Six-Phase Machine Based WECS

The six-phase machines are also used in the commercial wind turbines. With the two sets of windings, the insulation level for each winding decreases. The power handling capacity can be improved two times as each set of winding carries half the rated current. A six-phase WRSG (PMSG) based WECS is shown in Fig. 2.18. The stator windings are separated by 30° and thus the stator voltages are phase shifted by 30° . This leads to cancelation of lower order harmonics in the stator currents with which the torque ripples can be minimized. Lower sized filters can then be used on the generator side. Since these two windings are separated, no circulating current flows and thus the complexity of control system decreases.

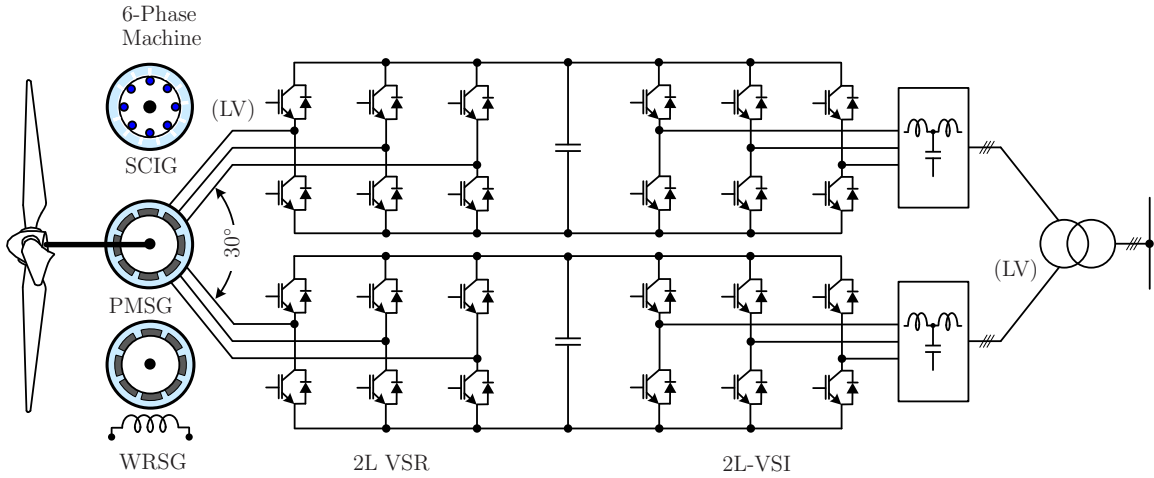


Figure 2.18: Six-phase machine based WECS with parallel 2L-VSC modules.

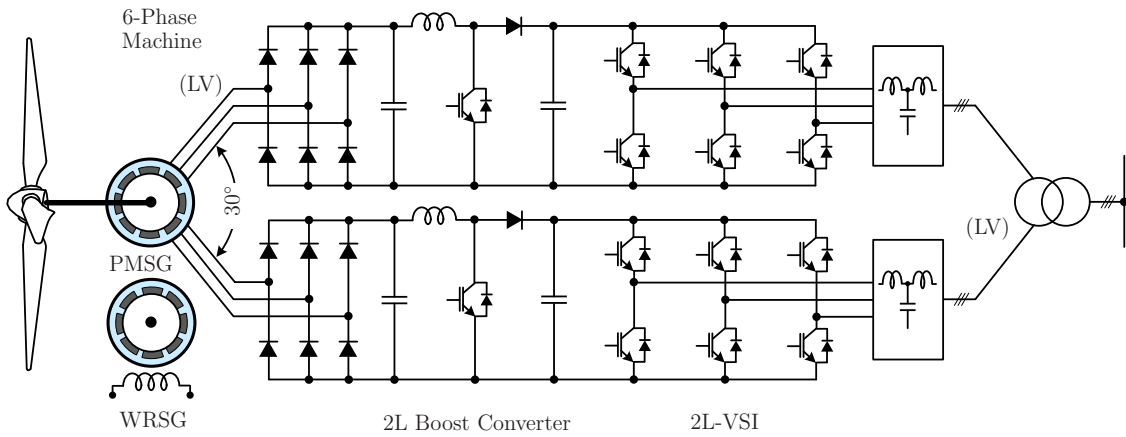


Figure 2.19: Six-phase machine based WECS with parallel 2L-boost + 2L-VSC modules.

A similar six-phase configuration with a passive generator-side converters is shown in Fig. 2.19 [124]. The disadvantage of high torque ripples with the diode rectifiers can be mitigated by employing a six-phase configuration with 30° phase shift.

The MV operation of wind turbines is cost effective and a promising solution for megawatt wind turbines. But, one of the shortcomings in the current wind energy industry is the lack of availability of the MV generators. The use of LV converters at the generator-side and MV converters at the grid side represents a very promising approach. A configuration with series-connected LV converters on the generator-side and the NPC converter on the grid-side is shown in Fig. 2.20 [73]. The LV outputs of the generator-side converters are connected in a series to achieve higher dc-link voltage. The capacitor voltages are balanced by the NPC converter. This configuration may not work during the whole wind speed range.

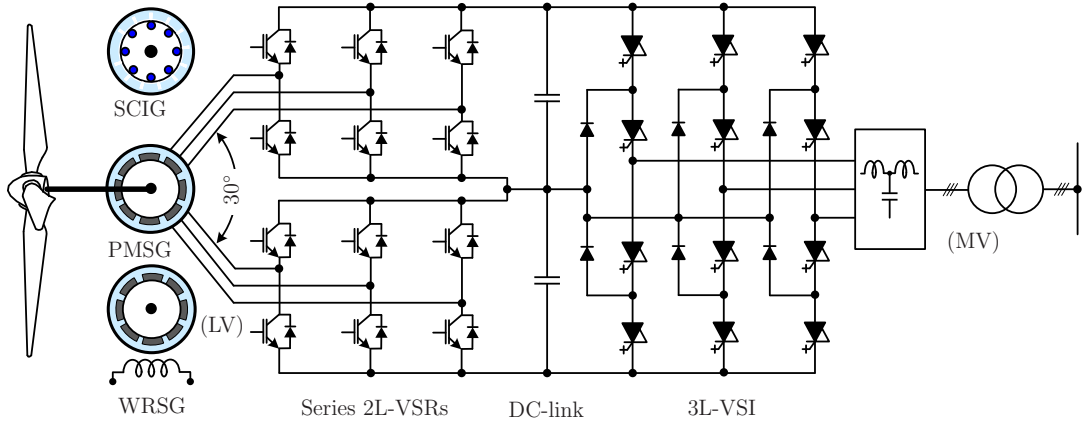


Figure 2.20: Series connected 2L-VSRs at generator-side and 3L-VSI at grid-side.

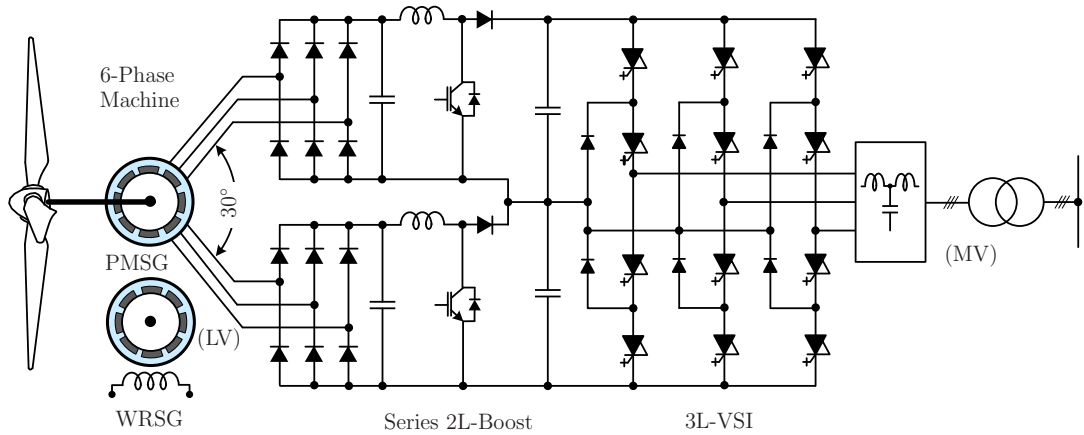


Figure 2.21: Series connected 2L boost converters at generator-side and 3L-VSI at grid-side.

As shown in Fig. 2.21, a passive generator-side converters can also be used to decrease the cost of the turbine and to operate during the whole wind speed range [125]. The torque ripples can be minimized while performing LV-MV operation. This configuration is more promising compared to the active generator-side converters because during low wind speed operation, the boost converters can operate with a higher duty cycle. As discussed in [125], the capacitor voltages are controlled by the boost converter and this leads to higher complexity for the NPC converter.

To overcome the problem of dc-link capacitor voltages balancing while performing LV-MV conversion, a new converter configuration is proposed as shown in Fig. 2.22. Instead of a series connection of 2L-boost converters, the outputs of the diode-rectifiers are connected in a series. The output voltage of the series-connected diode bridge rectifiers form the MV input dc-link [126]. The 3L-boost converter performs the MPPT with additional freedom to control the dc-link capacitor voltages with minimal switching and reverse recovery losses.

Similar to the VSC converters discussed, the LV to MV conversion can also be achieved by CSC converters as shown in Fig. 2.23. The CSI configuration is much simpler and there are no issues related to the balancing, unlike those in the NPC converters presented in Fig. 2.21. This configuration has already been introduced in the MV drives industry [127], and it is very promising for high power wind turbines.

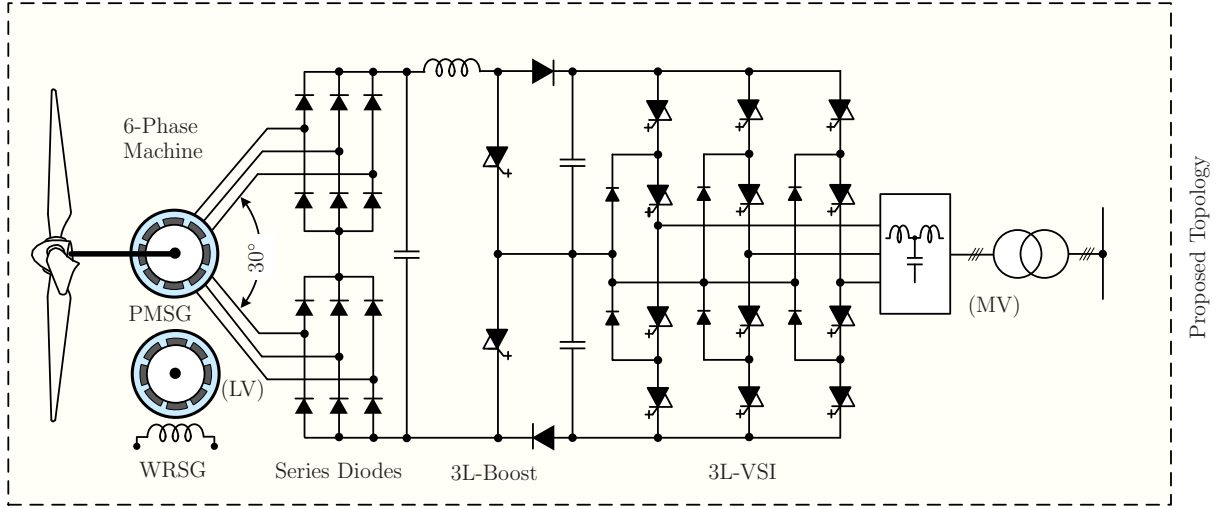


Figure 2.22: Series connected diode rectifiers, 3L-boost converter and 3L-VSI at grid-side.

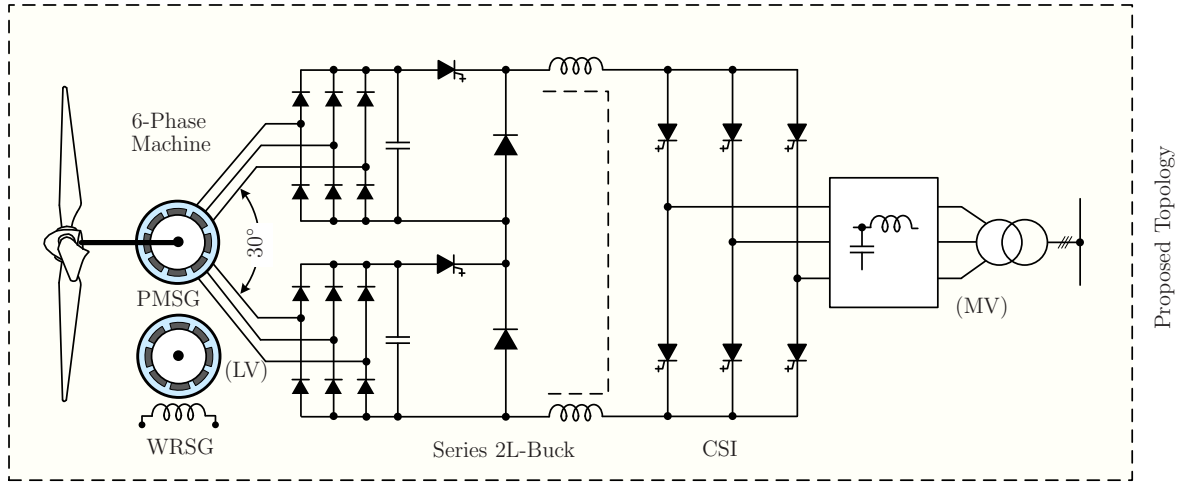


Figure 2.23: Series connected 2L-buck converters at generator-side and CSI at grid-side.

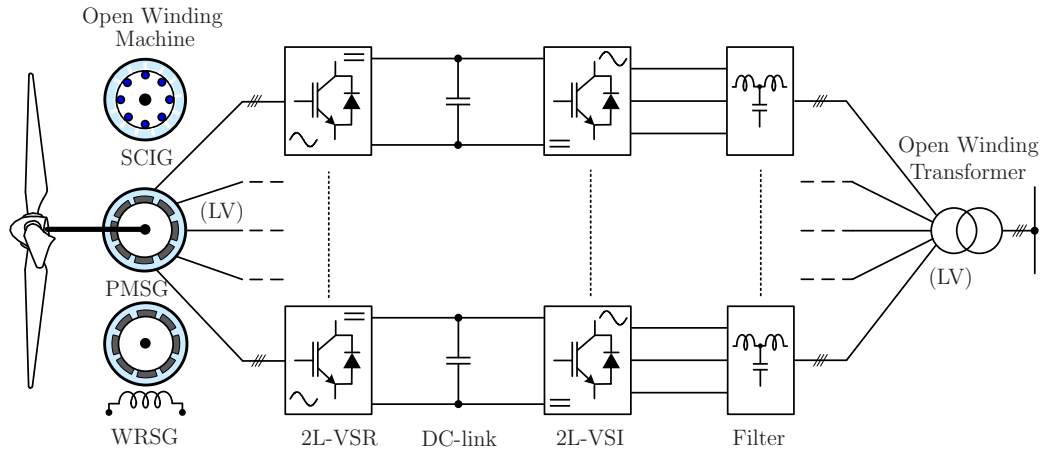


Figure 2.24: Open winding machine based WECS with multiple 2L VSC modules.

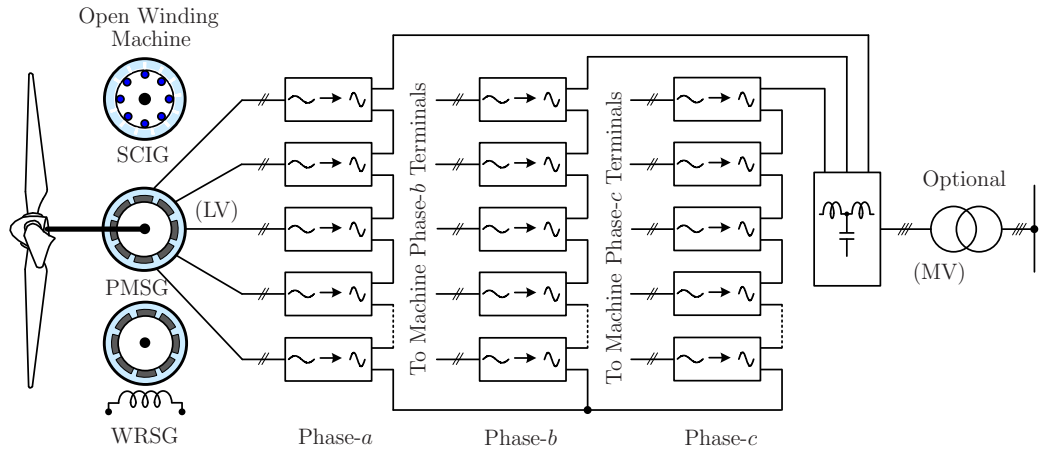


Figure 2.25: Open winding machine based WECS with cascaded converters.

2.4 Converters for Open Winding Machine Based WECS

Wind generators with open-winding structure are also used in the present wind turbines. The generator is equipped with more than one set of windings and offers new possibilities to connect the converters in different configurations [8, 128, 129]. One of the practical wind turbines, which use six sets of three-phase windings, is shown in Fig. 2.24. In comparison to the parallel VSC modules discussed earlier, the circulating currents in the generator-side converters can be eliminated. With zero circulating current, the power rating of the overall system increases, in proportion to the number of channels employed. The megawatt wind turbines can be realized using low power, mass produced VSC converters. The distributed windings also provide insulation between the converters. These generators are specially designed at a higher cost.

A higher power MV wind turbine using cascaded converters is shown in Fig. 2.25. The converters are connected in a cascaded connection to increase the system voltage and power rating. This configuration requires a generator with multiple sets of two-phase windings with a phase displacement of 90° . Each module can be realized using the power converters introduced in Figs. 2.26 [128, 129] to 2.27 [8]. The transformerless grid connection is possible with this configurations as system voltages of 10-35 kV can be reached by connecting more modules in the series. The modularity and redundancy are other added advantages of this configuration.

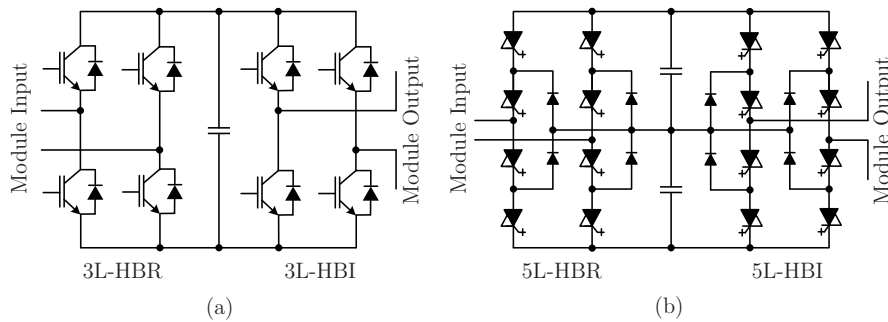


Figure 2.26: BTB connected 3L- and 5L-HB converters based module.

A three-level H-bridge converter is shown in Fig. 2.26(a). It is a simple structure and its output contains three levels. This converter can be realized by mass produced two-level VSCs. To achieve the higher system voltage operation with a lower number of modules, NPC

H-bridge modules can be used to form a 5L-HB converter as shown in Fig. 2.26(b). In this case, the generator windings should also be designed for medium voltage operation. The cost associated with the generator-side active converters can be decreased by using single-phase diode-rectifier and boost converter similar to the topology presented in Fig. 2.10 [128].

Another possibility is to use medium frequency transformers (MFTs) in the BTB H-bridge modules (Fig. 2.27). The transformer operates at several kHz to decrease its size [8]. Due to the increase in the number of components, the reliability is lower with this configuration.

As shown in Fig. 2.28, the module can also be realized using a single-phase diode bridge rectifier, 3L-boost converter and 5L-HB converter to decrease the cost of the overall system. Since several modules are used in cascaded connection, the overall cost of the converter becomes lower compared to the BTB converters shown in Fig. 2.26. Moreover, the dc-link capacitor voltages are well regulated by the 3L-boost converter in each module, and thus the control system complexity for 5L-HB becomes simplified.

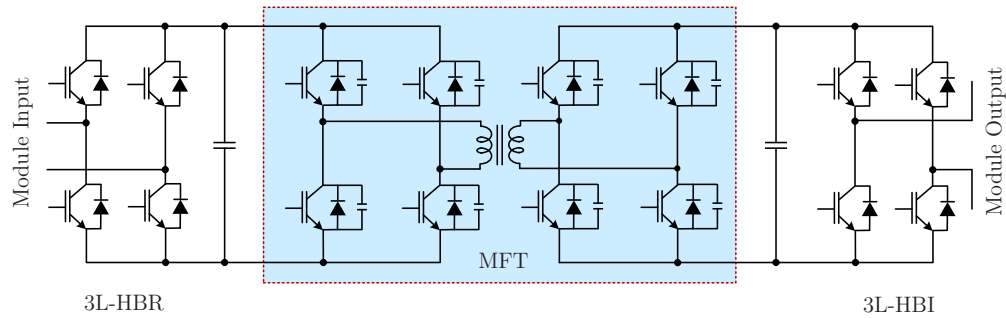


Figure 2.27: Back-to-back connected 3L H-bridge converters and MFT based module.

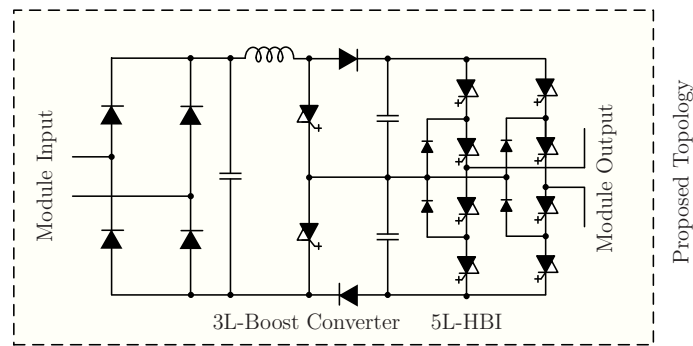


Figure 2.28: Diode rectifier, 3L-boost and 5L-HB converter based module.

2.5 Conclusion

In this chapter, an overview on WECS is presented with the main focus on full-scale power converters employed with a squirrel cage, permanent magnet and wound rotor synchronous generators. With the combination of different types of generators and power converters, a variety of WECS configurations have been investigated. The most common configurations for practical and emerging wind turbines are discussed. Various technical issues related to these configurations were discussed, including generator types, power converter topologies, active power control, energy conversion efficiency, and grid-side reactive power compensation. The back-to-back connected converters, passive generator-side converters, and converters for six-phase and open winding generators are presented, and their features and drawbacks are analyzed. In each category, new converter configurations are proposed based on the existing literature and commercial technologies.

Chapter 3

Review of Control Techniques in Power Converters

In efficient energy conversion, three main research areas play a crucial role: (1) semiconductor devices, (2) arrangement of these devices (called power converter configuration), and proper turn on/off of these devices (called the control scheme). In Chapter 2, the semiconductor devices and power converter configurations have been analyzed. The power converters' control is a very active research topic and is constantly evolving according to the technological developments in semiconductor devices and control platforms, control requirements, power quality standards, and grid code requirements, etc. [3, 4, 8, 9, 16, 24, 26, 28, 61, 92, 106, 112, 130–148]. An overview of classical and advanced digital control techniques is presented in Chapter 1.

In this chapter, the state-of-the-art converter control techniques, such as hysteresis control, linear control, sliding mode control, fuzzy logic control, artificial neural network (ANN) based control, deadbeat predictive control and finite control-set model predictive control (FCS-MPC) are discussed. The operating principle of these techniques is analyzed with an intuitive example of load current control. Various classes of the predictive control techniques are discussed along with their merits and demerits. The operating principle and design procedure of FCS-MPC strategy is discussed with an example of first-order system. The cost function flexibility to incorporate several primary and secondary control objectives is discussed. The delay compensation and extrapolation methods are discussed along with their advantages and disadvantages. The FCS-MPC method is compared with the classical control approach, and important observations are tabulated.

3.1 The Past, Present and Future of Control Platforms

In a search to obtain the ideal characteristics of a switch, many semiconductor devices have been developed [84, 149–151]. The diode rectifiers which belong to the first generation of semiconductor devices use natural commutation and do not need any control platform. In the second generation semiconductor devices, the gating terminals have been incorporated to turn on/off the switches according to the desired performance. As a result, many power switches have been developed and one of the earlier developments is the thyristor.

During the 1960s, analog control platforms based on operational amplifiers and passive components were developed to control the firing angles of thyristors in order for the output voltage to be controlled [77]. With thyristors, the turn-on instant can be controlled, but the turn-off instant is uncontrollable and is dependent on the line frequency. In an effort to achieve controllable turn-off, insulated-gate bipolar transistors (IGBTs) have been developed [84]. A simple example of using IGBT to achieve controllable performance is a buck converter whose output voltage can be regulated by adjusting the duty cycle [152]. For this converter, analog control circuits have been used in the past, where a single-phase pulse width modulator or hysteresis controller generates the gating signals. Analog control platforms present several drawbacks such as a large number of components, reduced system reliability and poor computational capability to name a few [153].

To achieve a high performance operation, digital control techniques were developed during the 1970s which involve powerful calculations, complex strategies and math-intensive algorithms [77, 153]. Introduction of digital signal processors (DSPs) by Texas Instruments in 1983 has brought the base to implement the digital control techniques. One example of the earlier DSPs is TMS320C14 which features a 16-bit processor and operational power of 10 million instructions per second (MIPS) [153]. To date, the technological advancements in semiconductor devices have resulted in many switching devices such as the power metal-oxide semiconductor field effect transistor (MOSFET), emitter turn-off thyristor (ETO), MOS-controlled thyristor (MCT), static induction thyristor (SIT), silicon-controlled rectifier (SCR), gate turn-off thyristor (GTO), insulated-gate bipolar transistor (IGBT), reverse blocking (RB) IGBT, injection-enhanced gate transistor (IEGT), gate commutated thyristor (GCT), insulated gate commutated thyristor (IGCT) and symmetrical gate commutated thyristor (SGCT). The digital control platforms also evolved rapidly and revolutionized the

industrial control area by allowing the user to develop sophisticated control algorithms. A few examples of modern real-time (RT) digital control platforms include: microcontrollers, DSP, field programmable gate array (FPGA), rapid prototyping systems. These platforms have been used widely in the control of various power electronic converters [153–159] and they feature low cost, more reliability and high computational power. For example, rapid prototyping controller dSPACE DS1103 performs 2500 MIPS which is very powerful compared to the earlier versions of DSP (TMS320C14).

It is anticipated that in the future more powerful digital control platforms will be developed leading to much lower costs and higher computational capacity. The user will not have to worry about the computational power needed to develop more advanced control schemes, and can incorporate many constraints to improve the system response.

In industry, fixed-point processors are used mainly due to cost considerations and computational power, but in academia, floating-point processors and rapid prototyping platforms are used to achieve flexibility in programming and RT implementation. In this dissertation, a DS1103 rapid prototyping platform is used to perform all the experimental tests. Since this platform uses the same microprocessor of industrial products, the software programming can be transferred to the industry “as is” or with slight modification [77, 153].

3.2 Overview of Digital Control Techniques

The development of control techniques for the power electronic converters is an ongoing research topic. A summary of the most established control techniques, and also those which are promising for future development are shown in Fig. 1.10. The hysteresis and linear controllers are widely accepted by the power electronics industry. The advanced control techniques include sliding-mode, intelligent and predictive control techniques. The block diagrams of these control techniques are shown in Figs. 3.1 to 3.8 to show their main principle, but many other classes or variations are available in each category. A two-level converter which is connected to the load/motor/grid is used as an example for the discussion of control techniques. The harmonic filter on the load/motor/grid side is not shown to simplify the diagrams 3.1 to 3.8. The control of variables is shown in natural frame (abc) to better compare the different controllers, but as demonstrated in the literature, it is also possible to control the variables in stationary ($\alpha\beta$) or synchronous (dq) reference frames.

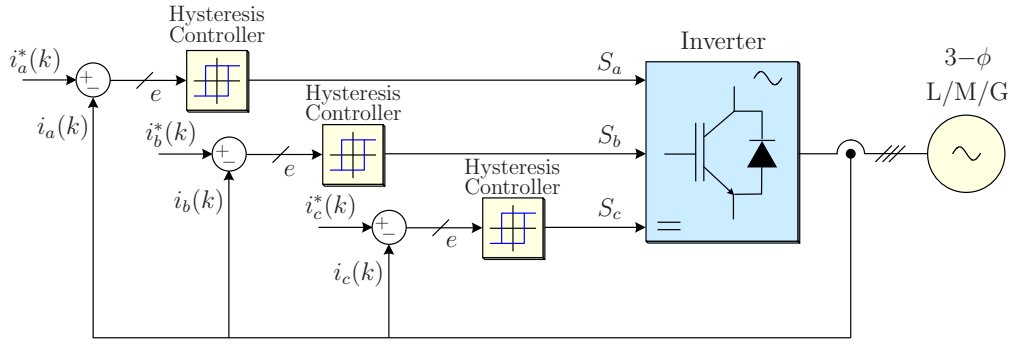


Figure 3.1: Hysteresis current control scheme for 3- ϕ load/motor/grid (L/M/G).

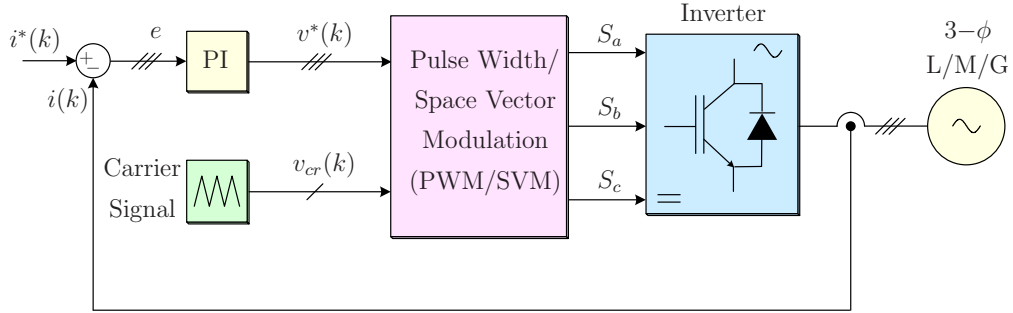


Figure 3.2: Linear current control scheme using PI regulators and SVM.

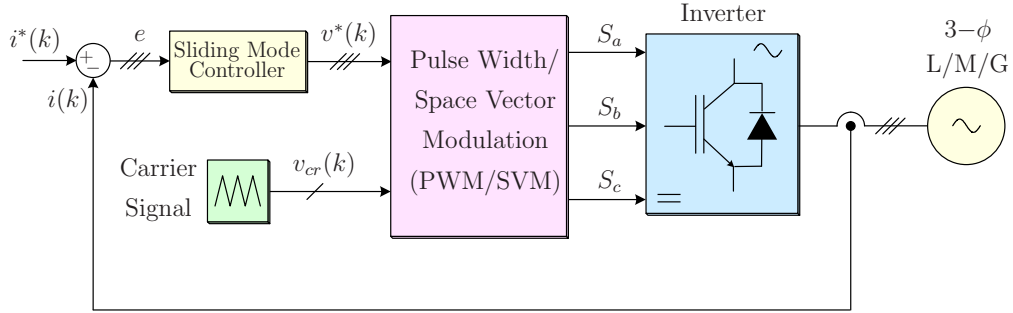


Figure 3.3: Sliding mode current control scheme using SVM.

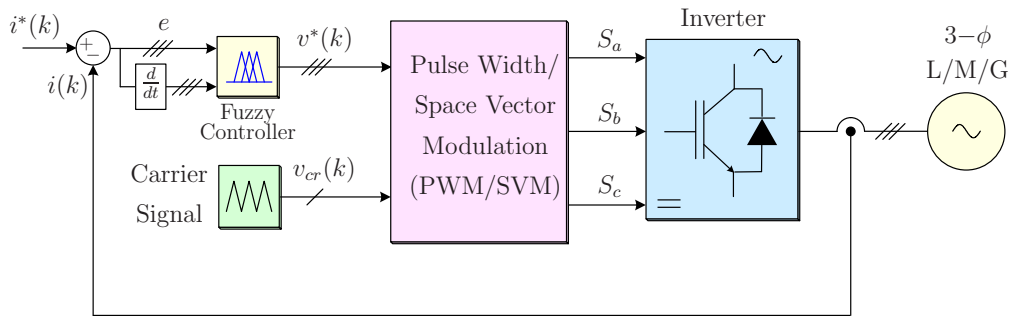


Figure 3.4: Fuzzy logic current control scheme using SVM.

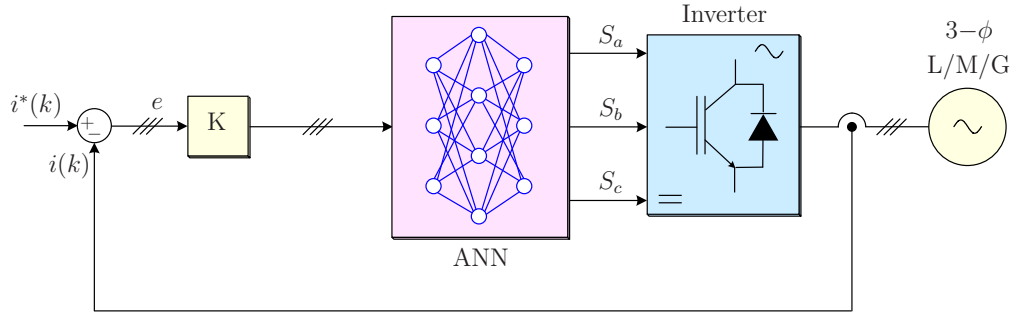


Figure 3.5: ANN based current control scheme.

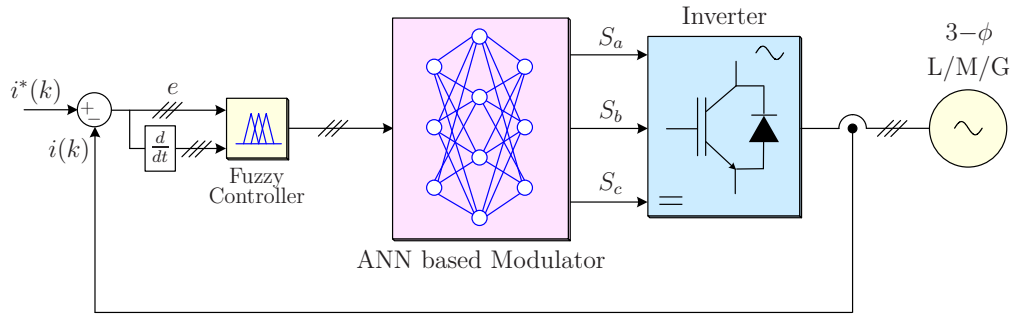


Figure 3.6: Fuzzy logic current control scheme using ANN modulation.

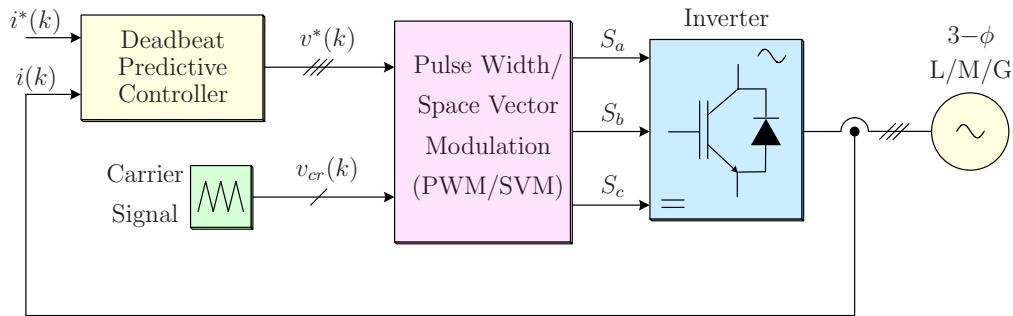


Figure 3.7: Deadbeat predictive current control with SVM.

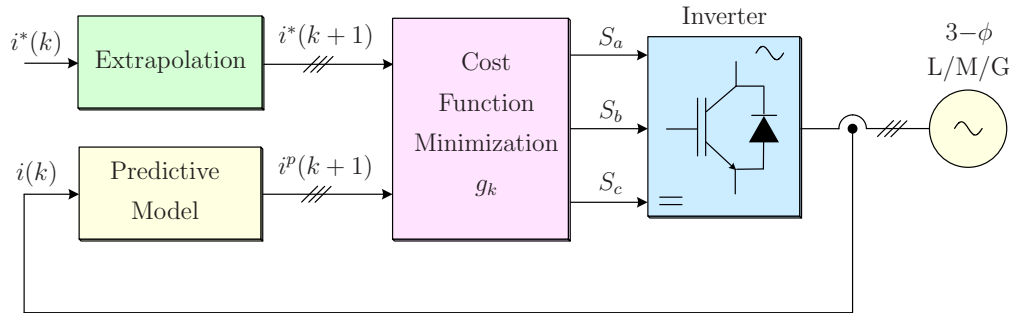


Figure 3.8: Finite control-set model predictive control (FCS-MPC) scheme.

3.2.1 Hysteresis Control Technique

A hysteresis current control scheme is shown in Fig. 3.1. This controller is recognized as a nonlinear method [149, 150, 160–164]. The measured currents are compared to the reference currents with the help of hysteresis (bang–bang) controllers, and the gating signals are generated based on the reference tracking. The error in reference tracking can be reduced by reducing the hysteresis band width. This is a simple concept and has been used since the era of analog control platforms. It is important to note that no modulator is required with this method and thus the converter’s switching frequency varies according to the filter parameters, operating conditions and hysteresis band width [77]. The uncontrollable switching frequency is one of the major drawbacks of this controller and many works have been presented in an effort to improve this controller.

More advanced versions of this method include direct torque control (DTC) [84, 149, 150, 165] and direct power control (DPC) [70, 71, 156]. In the DTC method, the torque and flux of the drive system are controlled, while in DPC the grid active and reactive power are controlled directly. The hysteresis controllers produce error signals and a look-up generates the switching signals to the converter based on the relative magnitudes of the error signals (torque and flux in DTC; active and reactive powers in DPC). In order to implement these methods on digital platforms, a very high-sampling frequency is needed to force the variables within the hysteresis band limits. In addition, the switching losses are higher with this method, and thus it is not suitable for high power applications [77].

3.2.2 Linear Control Technique

In an attempt to solve the major drawbacks of the hysteresis controller, linear control techniques have been proposed which linearize the nonlinear converter. To achieve this, cascaded linear regulators, usually proportional-integral (PI) controllers and a modulation stage have been developed. The most commonly used modulation schemes are pulse width modulation (PWM), space vector modulation (SVM) and selective harmonic elimination (SHE) [97–105, 108, 166–195]. A linear current control technique using SVM is shown in Fig. 3.2. The load currents are compared to their references, and the error signal is processed by the PI regulators, and the reference load voltage is generated accordingly. With PWM modulation, the reference signal $v^*(k)$ is compared with the triangular signal to generate the

gating signals for the converter [97, 166–176]. The SVM is recognized as an efficient method as it offers better harmonic performance and enhanced dc-bus voltage utilization compared to the PWM [84, 149]. With the SVM, the closest vectors to the reference voltage vector are selected based on dwell time calculation and switching scheme design [98–105, 108, 177–190]. The SVM involves several design steps and complex modeling, which leads to a higher computational burden compared to the PWM. The SHE is mainly based on switching angles calculation such that specific lower order harmonics in the output current can be eliminated [191–195].

The linear control scheme using PWM/SVM/SHE operates with fixed-switching frequency, and this value is dictated by the carrier frequency. The error value is minimal in dq frame compared to the $\alpha\beta$ and abc frames. The PI parameters are designed for one operating condition (usually rated condition), and if the converter operates at different operating conditions, then the control performance deteriorates, and stability-related problems arise [76, 196]. Since the linear controller is applied to the power converter which is nonlinear in nature, the performance obtained is unsymmetrical and it varies according to the operating condition [77]. The assumption of the linear model gives favorable performance only if a high band-width modulation is used. This scenario leads to a high switching frequency operation which consequently increases the switching losses. Moreover, when the converter operates at lower switching frequency, the magnitude of the lower order harmonics increases significantly and causes poor power quality [74]. Many research works have been carried out to solve this issue, and research is ongoing.

The linear control techniques have been widely used in the drives industry and energy systems. To control the motor torque and flux in a decoupled manner, field oriented control (FOC) is used. This involves reference frame transformations, several PI controllers, low pass filters and modulation stage. Similar to the FOC, voltage oriented control (VOC) is used to control the grid-connected converter [2, 14, 72]. Using the VOC scheme, decoupled control of the net dc-bus voltage and grid reactive power can be achieved. In VOC, the grid voltage harmonics deteriorate the control performance [76].

With both the hysteresis and linear control techniques, the system constraints and technical requirements such as maximum current, load voltage spectrum shaping, switching losses reduction and total harmonic distortion (THD) minimization, cannot be incorporated easily in the design of control scheme.

3.2.3 Sliding Mode Control Technique

The sliding mode control is an advanced power converter control technique and belongs to the family of variable structure control and adaptive control [197–201]. This control technique is nonlinear in nature and it can be applied to linear or nonlinear systems [197]. A sliding mode control method along with the PWM/SVM is shown in Fig. 3.2.3. The load voltage references are generated through the sliding controller. As the name implies, the control variable (load current) is forced to track or slide along the predefined trajectory [202–204]. With this method, the structure of the controller is intentionally changed to achieve robust and stable response even during the system parameter variations and load disturbances [151]. This control method gives robust response compared to the classical controllers discussed earlier.

3.2.4 Intelligent Control Techniques

The expert systems, fuzzy logic, artificial neural network (ANN), and genetic algorithms belong to the family of intelligent control techniques [151, 205–207]. As demonstrated in Fig. 3.4, in this control approach, the PI controller is replaced by the fuzzy logic controller. The load current reference tracking error and its derivative are used as the input to the fuzzy controller. This controller embeds the experience, knowledge and intuition of the converter operator/designer in the form of membership functions. Since the power converters are nonlinear in nature, the robustness of the system during parameter variations can be improved by using the fuzzy controller without knowing the exact converter model. It is also a class of nonlinear control techniques, and positively the best among the adaptive controllers [151, 205–207].

The ANN represents the most generic form of the human thinking process compared to the other intelligent controllers [151]. The ANN based load current regulation is shown in Fig. 3.5 [149, 208]. The tracking error signals are given as inputs to the ANN through a suitable gain or scaling factor (K), and the ANN controller produces switching signals to the power converter. A constant switching frequency operation can be achieved with this approach. The advantages of fuzzy and ANN can be combined as shown in Fig. 3.6 to achieve better control performance [151, 205, 206]. Even though the intelligent controllers do not need a converter model, they require precise knowledge about the converter operation/behavior.

3.2.5 Predictive Control Techniques

The predictive control (PC) uses the system model to predict the future responses of a plant. These predictions are then used to generate the optimal control action [209–216]. This control philosophy emerged during the 1970s for the process control which are normally very slow in nature [217]. With this approach, a systematic solution was provided to the multivariable constrained control problems of the oil and chemical industries, and due to its simplicity it was immediately welcomed by the industry [218–220]. The application of predictive control in power electronics is a rather recent topic due to the fast processing time required to control the electric variables [77]. With the evolution in DSPs, a wide range of predictive controllers have been developed which includes deadbeat PC, hysteresis-based PC, trajectory-based PC, and model-based PC (MPC) [78].

A deadbeat predictive control technique is shown in Fig. 3.7, where the PI regulators are replaced by the predictive controller to make the tracking error close to zero [221–241]. This is achievable by generating an appropriate reference load voltage during each sampling instant. A PWM/SVM modulator is then used to generate the gating signals to the power converter. This control strategy gives a better transient response compared to the classical controllers, but the system parameter variations and perturbations deteriorates the control performance. The system nonlinearities and constraints cannot be included in a straightforward way in the design of this controller [78]. The hysteresis and trajectory-based PC techniques combine hysteresis and sliding-mode controllers with the predictive controllers, and operate at variable switching frequency [75, 77, 78]. The MPC with continuous control-set [76] is similar to the deadbeat predictive control in terms of design and implementation [78].

The FCS-MPC is a simple and powerful control strategy that has been recently applied to power converters. A FCS-MPC strategy for the load current regulation is shown in Fig. 3.8. Compared to the classical control techniques, this scheme eliminates the need for linear PI regulators and the modulation stage, and offers a conceptually different approach to control the power converters. This is truly a model-based optimization control strategy, and involves a large number of calculations [75, 77, 78, 242–244]. However, the computational issue is not prominent due to the advanced digital control platforms (DSPs and FPGAs) available in the market. It is anticipated that this will be one of the next generation control tools, and thus is considered in this dissertation as a subject to control the megawatt WECS.

3.3 Finite Control-Set Model Predictive Control

To design an efficient controller, one needs to know about the true nature/behavior of the plant to be controlled. A power electronic converter exhibits the following properties, constraints and requirements [75, 77]:

- Nonlinear nature especially during low switching frequency
- Contains finite number of switching states, for example 8 switching states are available for 2L-VSC.
- Imposes restrictions on the maximum current, switching frequency, efficiency and THD, etc., to achieve safe and reliable operation
- Demands faster response for the electric control variables
- Favors discrete-time implementation using the industry standard digital control platforms

The FCS-MPC strategy has proved one of the best methods for treating all the above properties and conditions. Recent scholarly works demonstrated that FCS-MPC can easily be applied to a wide range of power converters, drives, power quality applications and energy systems [79]. The main features and challenges of the FCS-MPC are summarized as follows:

Main Features of FCS-MPC:

- Uses simple concepts and is easy to understand
- An intuitive approach for real-time implementation
- Uses the inherent discrete nature of the power converters
- Treats the power converter as a discontinuous and nonlinear model which is the closest approximation to the real-time scenario
- Optimizations are greatly simplified due to finite number of switching states
- Can be applied to a wide variety of systems
- Can handle multivariable control programs in a decoupled manner
- System perturbations and dead times can be compensated

- System nonlinearities and limitations can be incorporated in a straight forward manner in the model
- Constraint handling is naturally accommodated by the method
- Many technical and control requirements can be fulfilled at the same time
- This methodology is open to include modifications and extensions depending on specific applications

Challenges of FCS-MPC:

- Requires a large number of calculations
- Operates with the variable switching frequency
- Selection of weighting factors is not analytical or numerical
- Control performance will be poor if the model of the system and prediction horizon is not formulated correctly

The first challenge can be surpassed with the commercially available fast processors such as DSPs and FPGAs. The other control challenges are investigated rigorously in this dissertation research, and many solutions have been developed to promote the FCS-MPC strategy as the next generation high performance control tool.

3.3.1 Operating Principle and Design Procedure

Fig. 3.8 is considered here again to explain the operating principle and design procedure of the FCS-MPC scheme. Note that the explanation given here for the FCS-MPC is described in a broad sense, and not specific for the current control. It uses the system model to predict the future behavior of the variables to be controlled. The controller uses this information to obtain the optimal actuation, according to a predefined optimization criterion. A step-by-step procedure for the implementation is given below, which is intuitive to understand and easier to implement:

Design Step–1: Measurements

Obtain the feedback signals as per the requirement of predictive model or references generation.

Design Step–2: References Generation

Generate the reference control variable $x^*(k)$ according to the specific application.

Design Step–3: Extrapolation of References

Extrapolate the reference control variable to $(k + 1)$ instant. Different extrapolation methods will be discussed in the next section.

Design Step–4: Development of Continuous-Time Models

In this example, it is assumed that the power converter continuous-time model is of first-order nature:

$$\frac{dx}{dt} = Ax + Bu \quad (3.1)$$

where A and B denotes the parameters of the converter (filter inductance, load resistance, dc-link capacitance, etc.), x represents the variable to be controlled (voltage, current, power, torque, flux, etc.), and u is input variable (dc-voltage, grid voltage, etc.).

Design Step–5: Development of Discrete-Time Models

The FCS-MPC is basically an optimization algorithm. To implement this strategy on digital control platforms, the continuous-time models should be converted to discrete-time. In the control theory, many discretization methods are available such as: forward difference, backward difference, bilinear transformations (combination of forward and backward difference), impulse-invariant and zero-order hold [245]. Due to the first order nature of the state equations that describe the model in (3.1), a first-order approximation for the derivative can be obtained by forward or backward Euler method. The forward Euler method considers the future sample $(k + 1)$ and present sample (k) as described below:

$$\text{Forward Euler Method: } \frac{dx}{dt} = \frac{x(k+1) - x(k)}{T_s} \quad (3.2)$$

where T_s is the discretization sampling time.

By substituting (3.2) into (3.1), the discrete-time model for the control variable can be obtained as:

$$\begin{aligned} \frac{x(k+1) - x(k)}{T_s} &= Ax(k) + Bu(k) \\ x(k+1) &= (1 + AT_s)x(k) + BT_s u(k). \end{aligned} \quad (3.3)$$

The backward Euler method provides approximation for the derivative by considering present (k) and past ($k - 1$) samples:

$$\text{Backward Euler Method: } \frac{dx}{dt} = \frac{x(k) - x(k-1)}{T_s}. \quad (3.4)$$

Using the derivative approximation given in (3.4), the continuous-time system in (3.1) can be converted to discrete-time as:

$$\begin{aligned} \frac{x(k) - x(k-1)}{T_s} &= Ax(k) + Bu(k) \\ x(k) &= \frac{1}{(1 - AT_s)} x(k-1) + \frac{BT_s}{(1 - AT_s)} u(k). \end{aligned} \quad (3.5)$$

By shifting the above variables into one future sample,

$$x(k+1) = \frac{1}{(1 - AT_s)} x(k) + \frac{BT_s}{(1 - AT_s)} u(k+1) \quad (3.6)$$

where $u(k+1)$ is the extrapolated input. More details about the extrapolation methods will be given in Section 3.3.4.

The forward Euler method presents a simple approach for the discrete-time conversion, but stable poles in the s plane of continuous-time system may be mapped to unstable poles in z plane of discrete-time system. In other words, the positive real continuous system may be converted to non-positive real discrete-time system. However, the backward Euler method can convert stable poles in s plane to stable poles in z plane, and marginally stable poles to asymptotically stable poles. The non-positive real continuous system can also be transformed to a positive real discrete system with the backward Euler method [245, 246]. For this reason, in this dissertation, the backward Euler method is considered to convert the continuous-time systems to discrete-time.

Design Step–6: Prediction of Variables

Using the discrete-time models, present sampling instant (k) measurements and past sample optimal variable $x_{op}^p(k)$, predict the future behavior of the control variables. The operating principle for the prediction of variables using a one-step prediction horizon is shown in Fig. 3.9, assuming that the converter possesses 5 switching states. The 5 possible switching states lead to 5 predictions for the variable to be controlled (refer to

equation [3.6]]. Compared to the classical control techniques which observe past and present values of the variable, the FCS-MPC strategy observes the past, present and future of the variable.

Design Step–7: Cost Function Minimization

As a final stage, the predicted variables $x_1^p(k+1)$, $x_2^p(k+1)$, $x_3^p(k+1)$, $x_4^p(k+1)$ and $x_5^p(k+1)$ are compared with their reference $x^*(k+1)$ using a cost function g_k as follows:

$$g_k = ||x^*(k+1) - x^p(k+1)||. \quad (3.7)$$

The goal of cost function optimization is to achieve g value close to zero. The switching state which minimizes the cost function is chosen and then applied at the next sampling instant. As shown in the next section, additional constraints can also be incorporated into the cost function. During each sampling instant, the minimum value of g is selected from the 5 function values. At the (k^{th}) instant, the algorithm selects a switching state which would minimize the cost function at the $(k+1)$ instant, and then applies this optimal switching state during the whole $(k+1)$ period.

As a final note, the FCS-MPC method uses only the model of system. Unlike in classical control schemes, this method does not require any internal current control loops or a modulation stage.

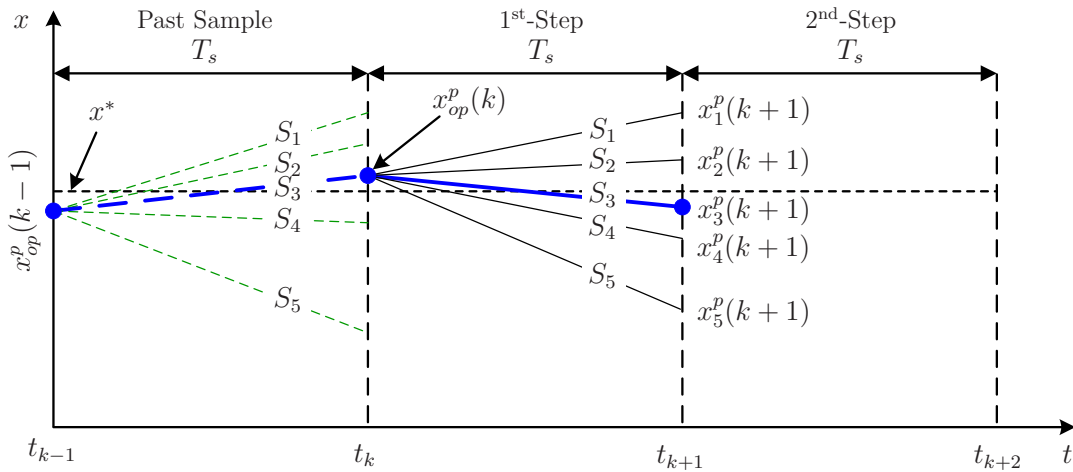


Figure 3.9: FCS-MPC strategy with one-step prediction horizon.

3.3.2 Cost Function Flexibility

One of the best features of FCS-MPC strategy is that several control objectives can be fulfilled at the same time as long as they are a mathematical function of the converter switching states. As demonstrated in Fig. 3.10, with an appropriate definition of cost function, a better control flexibility can be obtained with the optimization of several control goals. The control objectives for the power converter can be broadly classified as primary and secondary goals. The primary objectives include, but are not limited to, load current/voltage control, grid active/reactive power control, and machine torque/flux control. The fulfilment

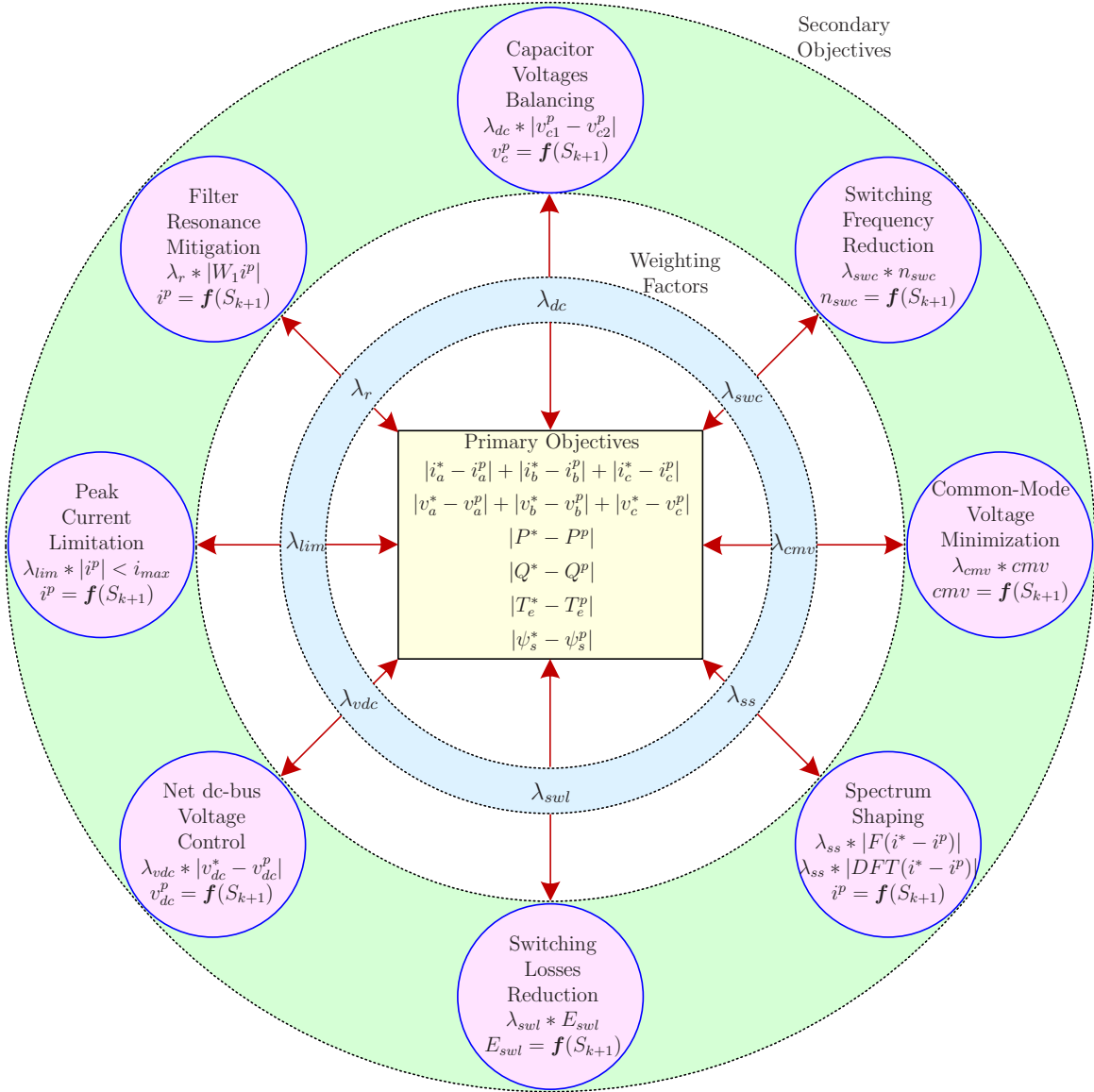


Figure 3.10: Overview of cost function definition with primary and secondary objectives.

of the primary objectives is essential to ensure the proper operation of a system involving the power converter. The cost function is shown as an absolute minimization function, but quadratic function can also be used to achieve over-proportionate control action against the reference tracking [75].

To improve the performance of the converter or to meet particular control/technical requirements, many secondary objectives such as the dc-link capacitor voltages balancing, switching frequency reduction in one or all phases, common-mode voltage minimization, load waveform spectrum shaping, switching losses reduction of any particular switch or whole converter, net dc-bus voltage control in the grid-connected case, peak current limitation in motor drives, and LC/LCL filter resonance mitigation can be easily included in the cost function as demonstrated in Fig. 3.10 [75, 77–79]. The relative importance of one objective over the other can be set through the weighting factors. Since the control variables possess a different physical nature (current, voltage, power, torque, flux, frequency, losses, etc.), they lead to coupling effects, and thus the selection of suitable weighting factors becomes tedious. The analytical or numerical procedure for the weighting factor selection is still an open topic for research. In [247], some guidelines are presented for the selection of the weighting factor. In this dissertation, a detailed empirical procedure for the selection of weighting factors is presented to help the reader develop a similar strategy in his/her works.

3.3.3 Delay Compensation Methods

The cost function presented earlier in Fig. 3.9 considers the minimization at $(k + 1)$ sampling instant which is suitable for computer simulations. The FCS-MPC strategy uses optimization algorithm and thus incurs a large number of online calculations. The computer simulations represent an ideal case where the time taken to compute these online calculations is zero [77]. According to this approach, the switching state which minimizes the error at the $(k + 1)$ instant is selected and applied at the (k^{th}) instant. This method is most commonly referred to as a one-step or one sample-ahead ($h = 1$) predictive controller.

In the real-time implementation of FCS-MPC algorithm, the large number of online calculations introduce a considerable time delay in the actuation [77, 248–252]. The delay caused by the digital signal processor is most significant and it must be compensated for. The delays associated with the response of the gate drive circuitry, sensors and switching of the devices can be disregarded due to their small magnitude, even for high sampling rates. The

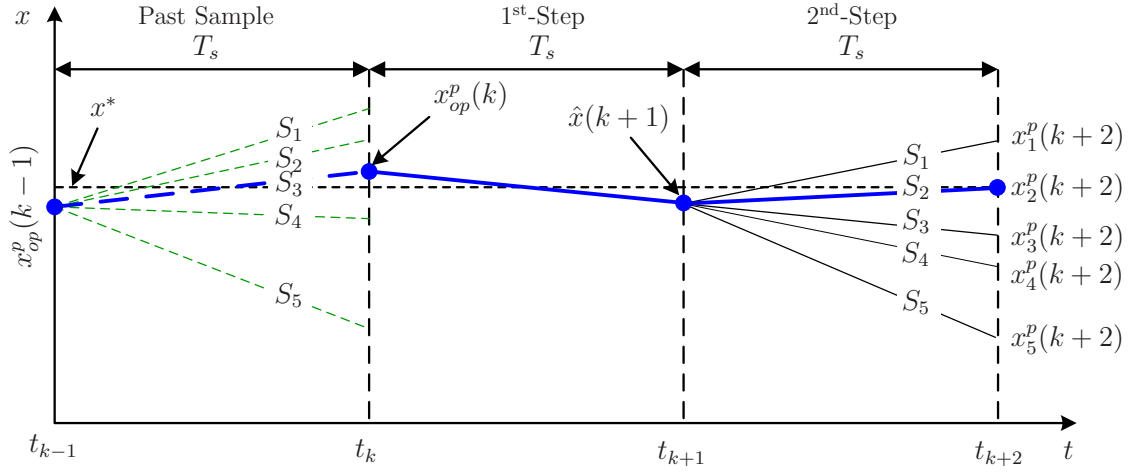


Figure 3.11: Delay compensation method-1 using modified one-step prediction horizon.

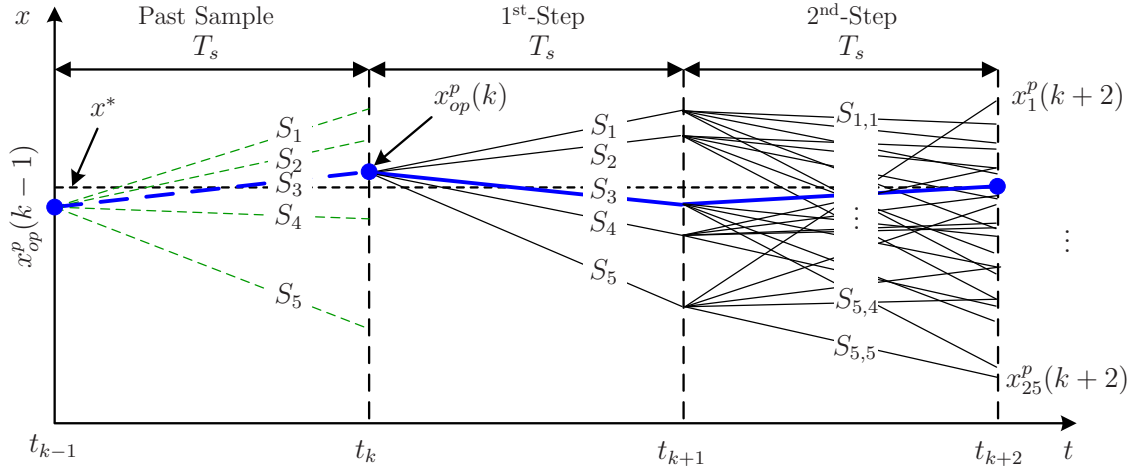


Figure 3.12: Delay compensation method-2 using standard two-step prediction horizon.

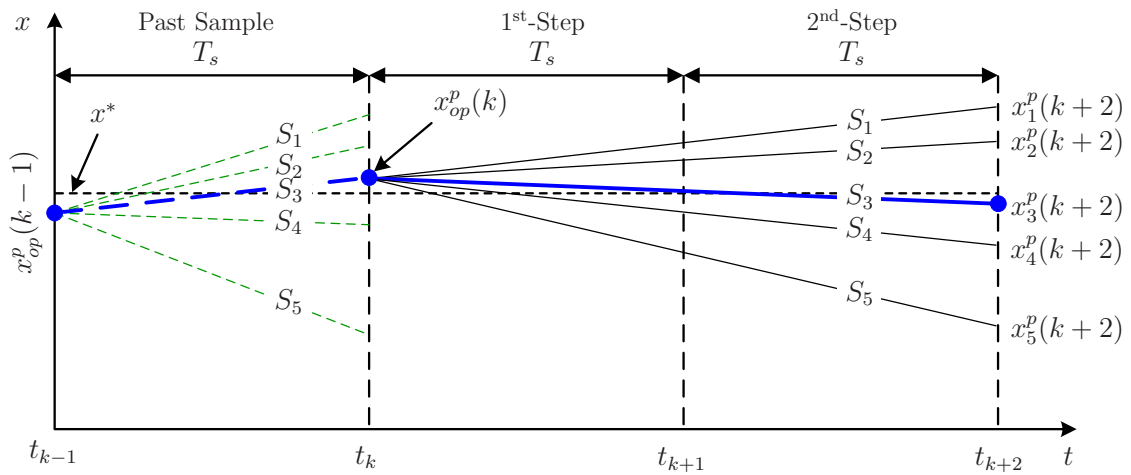


Figure 3.13: Delay compensation method-3 using simplified two-step prediction horizon.

computational delay deteriorates the performance of the system if it is not considered in the design of the controller. This delay can be compensated by calculating the cost function for two-samples ahead ($k + 2$). This approach allows one sampling period (T_s) for the control delay and another sampling period for the optimization algorithm. The selected optimal switching state can be applied at ($k + 1$) sampling instant. To achieve this, three different methods can be used as shown in Figs. 3.11, 3.12, and 3.13.

Delay Compensation Method–1: A modified one-step prediction as shown in Fig. 3.11 has been proposed in [248–252] to compensate the delay. According to this approach, the optimal switching state from the previous iteration [$x_{op}^p(k)$] is used to estimate the variables at ($k + 1$) instant [$\hat{x}(k + 1)$], and all the possible switching states are used to predict the variables at ($k + 2$) instant. The estimation of $\hat{x}(k + 1)$ leads to higher number of calculations and thus increases the switching frequency of power converter.

Delay Compensation Method–2: A standard two-step predictive horizon-based FCS-MPC strategy has been proposed in the literature [253–256] to achieve high control performance. As given in Fig. 3.12, this approach can also be used to compensate the delay, but with a higher computational burden. For example, if the converter has 5 switching states, then the number of ($k + 2$) predictions would become 25 (5^2). This approach is suitable for converters having a lower number of switching states, but is impractical for multilevel converters which have a large number of switching states. For an NPC converter, 729 (27^2) different combinations exist and the current DSPs cannot handle these large numbers of calculations.

Delay Compensation Method–3: A modification to the standard two-step prediction horizon is proposed in this dissertation. As shown in Fig. 3.13, the proposed approach minimizes the number of calculations while preserving the two-step prediction horizon. The predictions are projected to ($k + 2$) sampling instant, meaning that the same switching states are used in both ($k + 1$) and ($k + 2$) predictions. As shall be demonstrated in the next chapters, this approach gives a better performance than Method 1, and a performance almost similar to that of Method 2. The switching frequency obtained with the proposed approach is less than the one obtained with Methods 1 and 2. Even though the number of calculations is higher compared to Method 1, the switching frequency is lower because the calculations are performed over two samples.

The computational requirement is only a few μs higher than Method 1, and thus this approach can be implemented using the DSPs available in the market.

In the research being carried out over the past 5 years, both Methods 1 and 3 have been used in the experimental validation of FCS-MPC algorithms. The works presented in Chapters 5, 6 and 7 use Method 1, while the Chapters 4, 8 and 9 use Method 3.

3.3.4 Extrapolation Methods

One of the important requirements in the FCS-MPC strategy is reference tracking. The switching state which minimizes the reference tracking error in $(k + 1)$ or $(k + 2)$ sampling instant is selected and applied to the power electronic converter directly. When the sampling time T_s is sufficiently small ($< 20 \mu s$), no extrapolation is required. This implies that the sampling frequency is much higher than the fundamental frequency of the variables which need to be controlled. When the FCS-MPC strategy works with higher sampling times (lower sampling frequencies), the references should be extrapolated to $(k + 1)$ or $(k + 2)$ sampling instant to effectively minimize the tracking error. In the dq frame, the variables are dc in nature and thus no extrapolation is required during steady-state operation. However, during transient operation, a delay occurs between the reference and variable to be controlled, and to overcome this issue an extrapolation method should be used.

In the state-of-the-art FCS-MPC strategy, Lagrange and vector angle methods are used for the extrapolation of variables [77, 221, 257–261]. A third-order Lagrange method for one sample ahead $(k + 1)$ extrapolation is given as follows [77, 221]. This method uses present and two past sample values of the variable that needs to be extrapolated. The variable x represents either voltage, current or power. The estimated quantity is noted as \hat{x} .

$$\hat{x}(k + 1) = 3x(k) - 3x(k - 1) + x(k - 2). \quad (3.8)$$

For two-sample ahead $(k + 2)$ extrapolation, the following Lagrange method can be used:

$$\hat{x}(k + 2) = 3\hat{x}(k + 1) - 3x(k) + x(k - 1). \quad (3.9)$$

By substituting (3.8) in (3.9), the future value can be estimated using present and past sample values as demonstrated below:

$$\hat{x}(k+2) = 6x(k) - 8x(k-1) + 3x(k-2). \quad (3.10)$$

To increase the performance of FCS-MPC strategy, a higher-order extrapolation method can be employed [257–260]. A fourth-order Lagrange method for $(k+1)$ and $(k+2)$ extrapolation is given as follows [258, 259]:

$$\hat{x}(k+1) = 4x(k) - 6x(k-1) + 4x(k-2) - x(k-3) \quad (3.11)$$

$$\hat{x}(k+2) = 10x(k) - 20x(k-1) + 15x(k-2) - 4x(k-3). \quad (3.12)$$

For two-samples ahead $(k+2)$ extrapolation, the coefficients employed in two- and higher-order Lagrange methods are summarized in Table 3.1 [260].

Table 3.1: Coefficients for two-samples ahead $(k+2)$ Lagrange extrapolation method

Order	a_x	a_{x-1}	a_{x-2}	a_{x-3}	a_{x-4}	a_{x-5}	a_{x-6}
2	3	2	0	0	0	0	0
3	6	-8	3	0	0	0	0
4	10	-20	15	-4	0	0	0
5	15	-40	45	-24	5	0	0
6	21	-70	105	-84	35	-6	0
7	28	-112	210	-224	140	-48	7

Another possible approach for the extrapolation is the vector angle method. In this approach, during each sampling interval, the change in vector angle of the three-phase variables is considered as the basis for extrapolation. A n^{th} order vector angle extrapolation is given as follows [77]:

$$\hat{x}(k+h) = x(k) e^{j h \omega T_s} \quad (3.13)$$

where ω is the angular frequency of three-phase variables, and h is prediction horizon length.

The $x(k)$ in (3.13) can be a complex variable with real and imaginary quantities. This approach is best suited for the stationary frame ($\alpha\beta$) variables [261]. This method cannot be used in single-phase systems [77].

3.4 Comparison of FCS-MPC with Linear Control

A comparison between the classical and FCS-MPC strategy is performed based on the research results presented in the literature and summarized as shown in Table 3.2. The analysis suggests that the FCS-MPC strategy is an intuitive and powerful tool to control the power converters compared to the classical linear methods.

Table 3.2: Comparison between classical linear control and FCS-MPC

Description	Classical	FCS-MPC
Control diagram	Fig. 3.2	Fig. 3.8
Model [262]	Linear load model for PI & Inverter model for SVM	Discrete-time model of the complete system
Controller design [75]	PI adjustment (root locus) + Modulator design	Cost function definition
Nature of controller [78]	Linear	Nonlinear
Implementation platform [75]	Analog or digital	Digital
Modulation	PWM/SVM/SHE	Not required
Switching frequency [75]	Fixed	Variable (but controllable)
Multivariable [77]	Coupled	Decoupled
Constraints inclusion	Not possible	easy to include
Complexity of concept [263]	High with SVM	Simple and intuitive
Steady-state performance [77]	Good in dq frame	Good in abc , $\alpha\beta$ and dq frames
Transient performance [264, 265]	Moderate	Excellent
Computational burden	High with SVM	High
Robustness of controller [77, 266]	Poor	Excellent
Stability of controller [260, 267]	Moderate	Excellent

3.5 Conclusion

In this chapter, the state-of-the-art converter control techniques are reviewed, followed by the explanation of different classes of the predictive control techniques. The implementation of different control techniques for the output current control is presented along with their main features and challenges. The operating principle of the FCS-MPC strategy is presented for ideal and implementation cases. The cost function flexibility and potentiality in achieving different control and technical requirements is discussed. The issues and challenges related to the FCS-MPC strategy, such as the computational burden, development of control algorithm, delay compensation, and extrapolation of reference variables is discussed in detail. The analysis presented in this chapter favors the FCS-MPC strategy as the next generation control tool to achieve high performance operation for the power converters.

Chapter 4

Generalized Approach for Predictive Control in High-Performance Multilevel Diode-Clamped Converters

Multilevel converters are recognized as among the most suitable and efficient candidates to be used in high-power, medium-voltage (MV) industrial applications [8, 61]. They can synthesize near sinusoidal voltages while increasing the number of levels, leading to good power quality and smaller output filters. In addition, higher levels of MV operation can be achieved without connecting the switching devices in a series. The most popular and well-known multilevel topologies are flying capacitor, cascade H-bridge and diode-clamped converters (DCCs) [84, 106]. By using clamping diodes to divide the dc-link voltage among several capacitors, different configurations, ranging from three-level (3L) to m -level (ML) DCCs can be obtained.

This chapter proposes a generalized approach based on a finite control-set model predictive strategy for the current control, dc-link capacitor voltages balancing, switching frequency reduction and common-mode voltage mitigation in MLDCCs. The discrete-time model of an m -level DCC is presented, where all the control objectives are formulated in terms of the switching states. The control goals are expressed as a cost function and its minimization is used as a criterion to choose the best switching state which would be applied to the converter during the next sampling interval. The real-time digital control issues such as computational burden and delay compensation are also discussed. The feasibility of the proposed method is verified by simulations in 3- to 6-level converters and by experiments in 3- and 4-level converters.

4.1 Control Requirements and Challenges

The MLDCCs are suitable for many industrial applications such as: STATCOM, train traction, ship propulsion, regenerative conveyors, wind and photovoltaic energy systems, and general MV motor drive applications (pumps, fans, etc.) [84,106]. In these applications, current control is one of the most important issues and it has been widely studied in literature [104,105,160,268,269]. The most popular classical methods as introduced in Chapter 3 are: hysteresis control [160] and linear control (PI) with the space vector modulation (SVM) or pulse width modulation (PWM) [104,105,268,269].

The SVM method gives the best harmonic profile compared to the PWM approach, but its computational burden and complexity increases with the number of levels in DCC. Especially when the number of levels in DCC increase, the switching actions in the MLDCCs leads to an imbalance among the dc-link capacitor voltages [270]. In order to solve this issue, many methods have been proposed in the literature which can be classified as: use of external hardware [96], SVM with the redundant switching states selection [171], and PWM with zero sequence voltage injection [97]. All of these methods have widely been studied for 3L- to 6L-DCCs as reported in [104,105,268,269] where a generalized classical approach to control the MLDCCs have been proposed.

Another important challenge for MLDCCs is the operation at low switching frequency in order to minimize the switching losses and to allow proper heat dissipation [271]. This requirement can be accomplished with the PWM and SVM techniques by simply changing the carrier frequency. Unfortunately, low order harmonics are produced by the PWM and SVM techniques when operated below 1 kHz leading to poor output current quality [74].

One more critical issue with the MLDCCs is that the fast switching actions of the semiconductor devices cause high dv/dt in the converter output voltages and this leads to higher common-mode voltage (CMV). The CMV is undesirable when the MLDCC is used in motor drive and grid-connected applications [272–274]. The hardware (common-mode choke) [275,276] and/or software reconfigurations are considered as possible solutions for the CMV mitigation in MLDCCs. The latter process, with the improvement to PWM/SVM techniques, is a cost effective and attractive solution, and it is widely studied for MLDCCs [272–274,277,278]. The complexity of the improved SVM increases with the number of levels in DCC.

As mentioned in Chapter 3, the finite control-set model predictive control (FCS-MPC) takes over the functions of linear regulators and SVM/PWM modulators. To accomplish the aforementioned control requirements, many works based on FCS-MPC have already been reported for 3L-DCC [279, 280], 4L-DCC [80, 81, 107, 281], and 5L-DCC [282, 283].

The state-of-the-art research work being carried out for high performance control in the MLDCCs is summarized in Fig. 4.1. The software reconfiguration (changes to computer program) to achieve the control goals in MLDCCs is a recommended solution than the hardware reconfiguration (use of external hardware). The software reconfiguration using classical control methods has been widely studied in literature [104, 105, 268, 269]. Similar to the classical methods, the predictive control for the MLDCCs can be generalized, but this issue has not been addressed yet.

In this chapter, a generalized approach for the predictive control of MLDCCs is proposed. The discrete-time model of the converters and dc-link capacitor currents estimation is presented such that they can be applied to m -level DCC. The load/motor/grid current control, dc-link capacitor voltages balancing, lower switching frequency operation, and CMV reduction are expressed as a cost function. With the help of weighting factors, these control goals are met simultaneously.

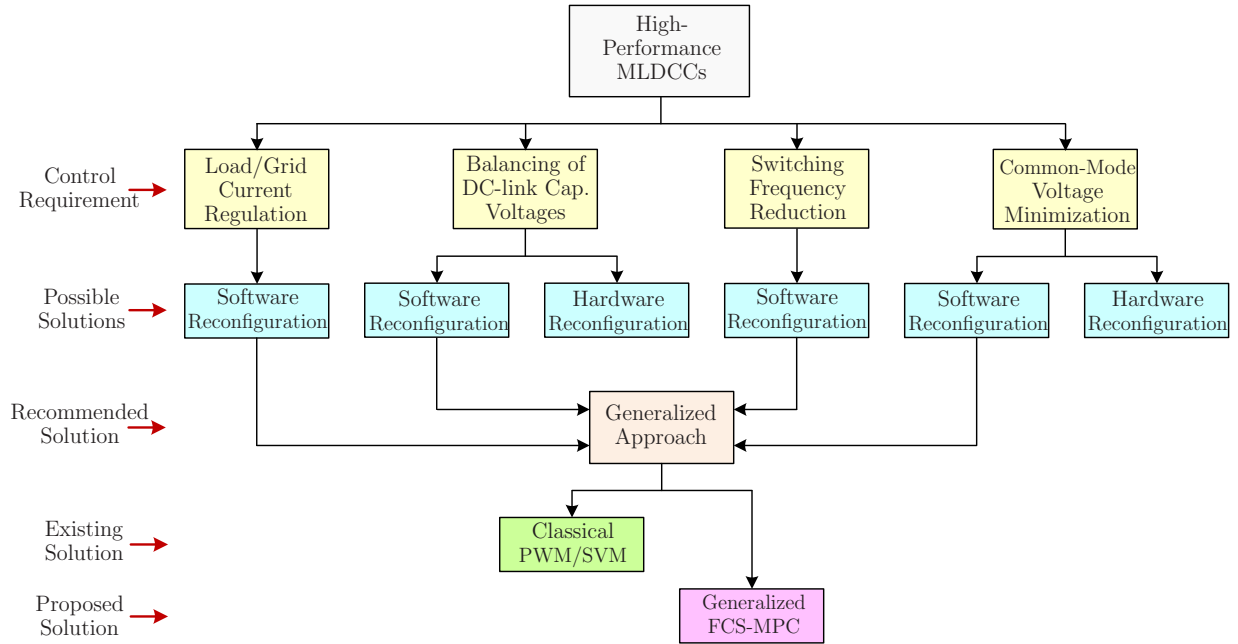


Figure 4.1: Overview of state-of-the-art and proposed solutions for high performance control in MLDCCs.

4.2 Review of Multilevel DCCs

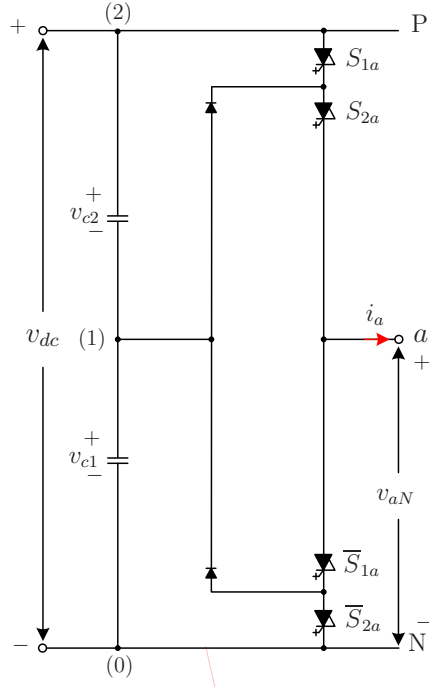
To facilitate the discussions leading to the generalized modeling and control in this section, a brief review of MLDCCs is presented. The per-phase diagram of 3L to 6L converters is shown in Fig. 4.2. For a given dc-link voltage rating, the voltage rating of active switches, clamping diodes and dc capacitors decreases with the increase in the number of levels. The clamping diodes are connected in a series to withstand the different reverse blocking voltages [84]. The component count and switching states of the MLDCCs are summarized in Table 4.1. As the number of converter voltage levels increase, the switching states increase proportionately and this leads to higher computational burden with the classical or predictive control method. The space vectors generated by an m -level converter is shown in Fig. 4.3 and it can be observed that the outer-most voltage vector contains only one redundancy. The switching states and corresponding converter terminal voltages are given in Table 4.2, where S_x represents the voltage level of the converter.

Table 4.1: Components, switching states and voltage vectors count for MLDCC

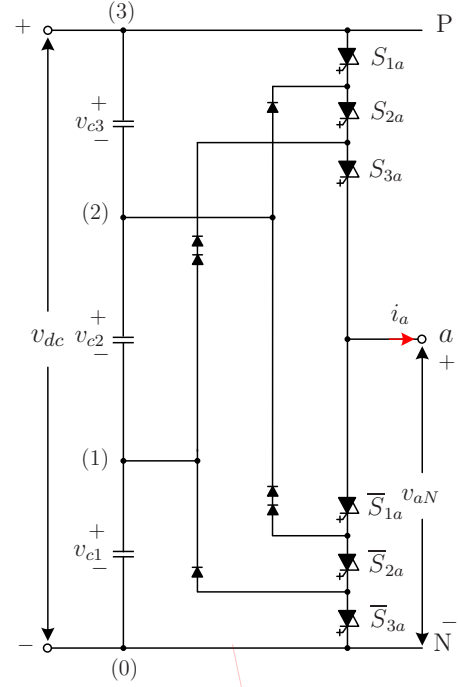
Voltage Levels	Active Switches	Clamping Diodes	DC-link Capacitors	Neutral Points	Switching States	Voltage Vectors
3	12	6	2	1	27	19
4	18	18	3	2	64	37
5	24	36	4	3	125	61
6	30	60	5	4	216	91
\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots
m	$6(m-1)$	$6(m-1)(m-2)$	$m-1$	$m-2$	m^3	$m^3 - (m-1)^3$

Table 4.2: MLDCC terminal voltages versus switching states ($x = a, b, c$)

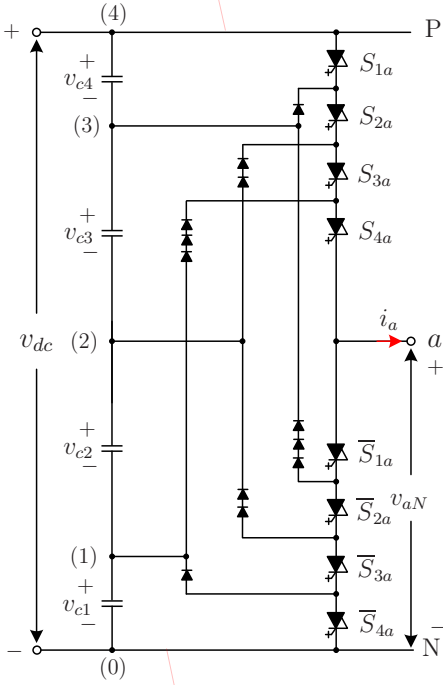
S_x	$S_{(m-1)x}$	$S_{(m-2)x}$	$S_{(m-3)x}$	$S_{(m-4)x}$	$S_{(m-5)x}$	\cdots	v_{xN}
0	0	0	0	0	0	\cdots	0
1	1	0	0	0	0	\cdots	v_{c1}
2	1	1	0	0	0	\cdots	$v_{c1} + v_{c2}$
3	1	1	1	0	0	\cdots	$v_{c1} + v_{c2} + v_{c3}$
4	1	1	1	1	0	\cdots	$v_{c1} + v_{c2} + v_{c3} + v_{c4}$
5	1	1	1	1	1	\cdots	$v_{c1} + v_{c2} + v_{c3} + v_{c4} + v_{c5}$
\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots



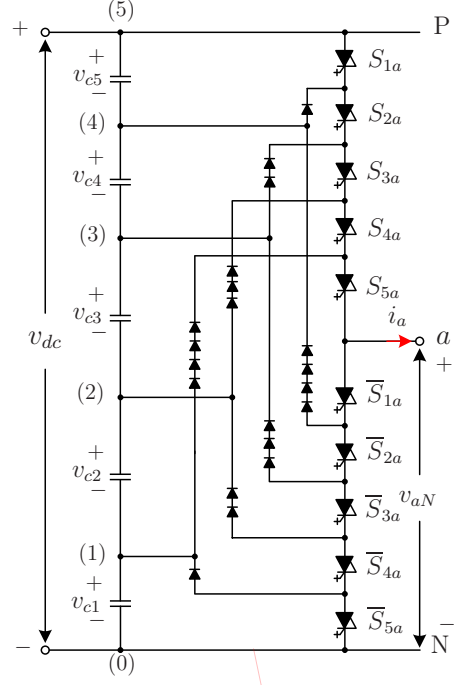
(a) Three-level ($m = 3$) DCC



(b) Four-level ($m = 4$) DCC



(c) Five-level ($m = 5$) DCC



(d) Six-level ($m = 6$) DCC

Figure 4.2: Per-phase diagram of multi-level diode-clamped converters.

4.3 Generalized Model of Multilevel DCCs

The FCS-MPC approach works on a different conceptual approach to control the power converters, and eliminates the need for linear regulators and SVM/PWM modulators. This approach is basically an optimization algorithm whose actions mainly depend on the discrete-time model of the converter, load/grid and dc-link. In this section, a generalized discrete-time model of the MLDC is formulated.

4.3.1 Model of Load/Motor/Grid Currents

One of the important requirements for the MLDCs is regulation of converter output current. Most of the applications, such as motor drives and grid-connected systems, can be simply represented as a *RLE* load. A MLDC with such a load is shown in Fig. 4.4, where, L_f and R_f represents the load filter inductance and its leakage resistance, respectively. Load resistance and back emf are represented as R and e respectively. To reduce the number of calculations, load current modeling is carried out in a stationary reference frame ($\alpha\beta$) [77].

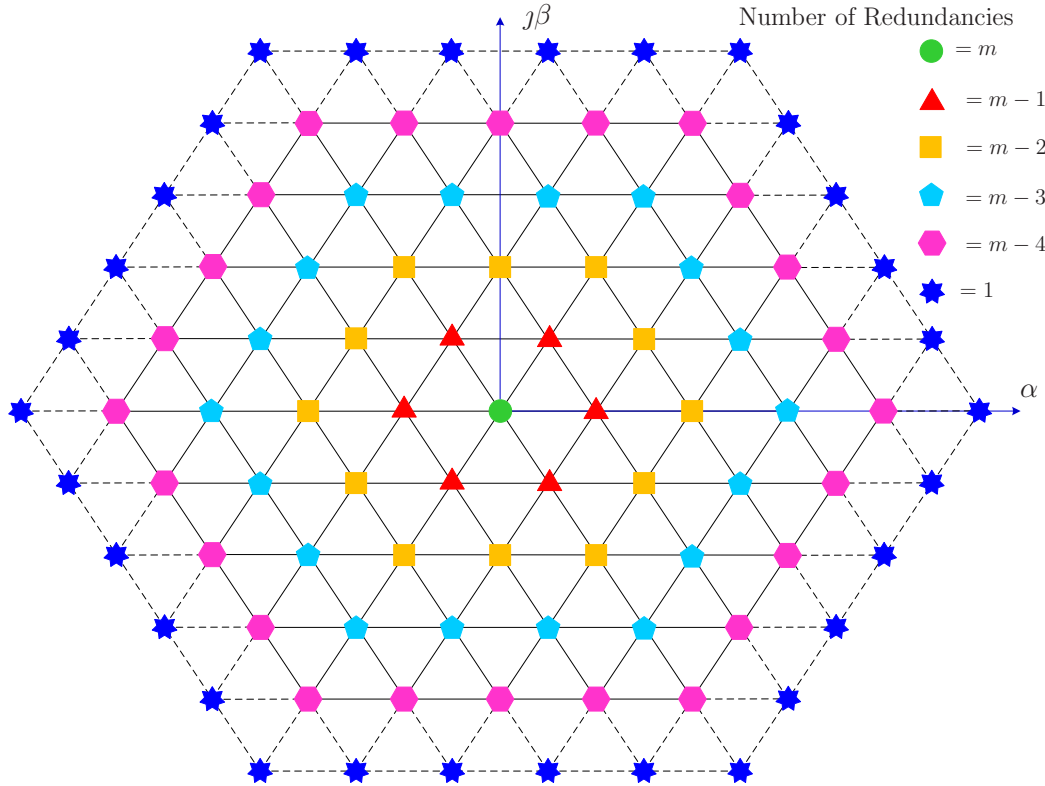


Figure 4.3: Space vectors generated by the multilevel diode-clamped converter.

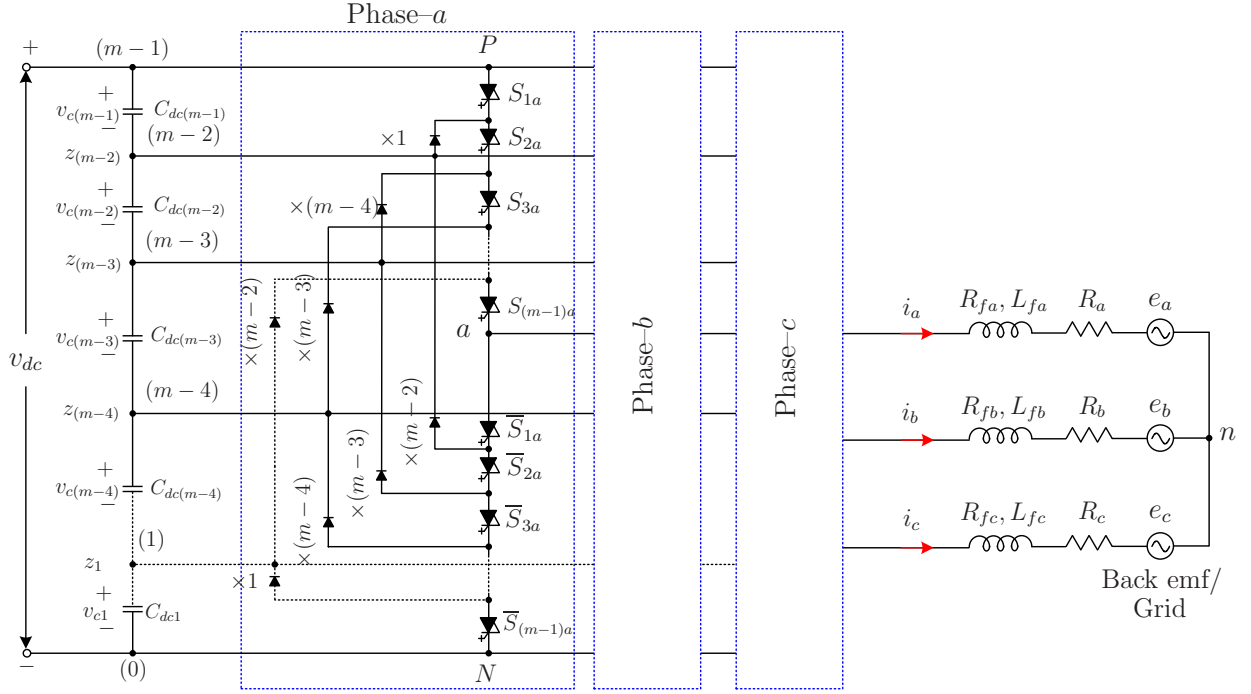


Figure 4.4: Topology of multi-level diode-clamped converter with RLE load.

The load currents can be represented as follows by applying the Kirchhoff's law to the Fig. 4.4 [262, 279]:

$$\begin{aligned} \frac{di_\alpha}{dt} &= \frac{1}{L_f} [v_\alpha - e_\alpha - (R_f + R) i_\alpha] \\ \frac{di_\beta}{dt} &= \frac{1}{L_f} [v_\beta - e_\beta - (R_f + R) i_\beta]. \end{aligned} \quad (4.1)$$

In (4.1), the three-phase measured load currents (i_a, i_b, i_c) and back emf (e_a, e_b, e_c) are converted to $\alpha\beta$ frame. For the motor drives application, the back emf can be estimated using the guidelines given in [262, 279]. v_α and v_β are stationary frame inverter voltages and they are obtained from the transformation of three-phase voltages (with respect to negative dc-rail N) given as follows:

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = [v_{c1}] \begin{bmatrix} S_a == 1 \\ S_b == 1 \\ S_c == 1 \end{bmatrix} + \cdots + [v_{c1} + \cdots + v_{c(m-1)}] \begin{bmatrix} S_a == (m-1) \\ S_b == (m-1) \\ S_c == (m-1) \end{bmatrix} \quad (4.2)$$

where v_{c1} and $v_{c(m-1)}$ are dc capacitor voltages. S_a, S_b and S_c represents the voltage levels of a three-phase converter. For a 5L-DCC, the relation between the S_x and switching states

can be summarized as:

$$\begin{aligned}
S_x &= 0 & \text{if } \overline{S}_{1x} \overline{S}_{2x} \overline{S}_{3x} \overline{S}_{4x} &= 1 \\
S_x &= 1 & \text{if } \overline{S}_{1x} \overline{S}_{2x} \overline{S}_{3x} S_{4x} &= 1 \\
S_x &= 2 & \text{if } \overline{S}_{1x} \overline{S}_{2x} S_{3x} S_{4x} &= 1 \\
S_x &= 3 & \text{if } \overline{S}_{1x} S_{2x} S_{3x} S_{4x} &= 1 \\
S_x &= 4 & \text{if } S_{1x} S_{2x} S_{3x} S_{4x} &= 1
\end{aligned} \tag{4.3}$$

where S_{1x} , S_{2x} , S_{3x} and S_{4x} are the switching signals of the phase $x = a, b, c$. The switching pairs $(S_{1x}, \overline{S}_{1x})$, $(S_{2x}, \overline{S}_{2x})$, $(S_{3x}, \overline{S}_{3x})$ and $(S_{4x}, \overline{S}_{4x})$ are complementary in nature. Similar analysis can be carried out for other MLDCCs.

The continuous-time model can be converted to discrete-time by approximating the derivative using the backward Euler method [258, 262, 279]:

$$\frac{dx}{dt} = \frac{x(k) - x(k-1)}{T_s} \tag{4.4}$$

where T_s is the sampling time used in the discrete-time conversion and control.

By substituting (4.4) in (4.1), the discrete-time model for the load currents can be obtained as [77, 258]:

$$\begin{aligned}
\frac{i_\alpha(k) - i_\alpha(k-1)}{T_s} &= \frac{1}{L_f} [v_\alpha(k) - e_\alpha(k) - (R_f + R) i_\alpha(k)] \\
\frac{i_\beta(k) - i_\beta(k-1)}{T_s} &= \frac{1}{L_f} [v_\beta(k) - e_\beta(k) - (R_f + R) i_\beta(k)].
\end{aligned} \tag{4.5}$$

The above expression can be simplified as,

$$\begin{aligned}
i_\alpha(k) &= K_v [v_\alpha(k) - e_\alpha(k)] - K_i i_\alpha(k-1) \\
i_\beta(k) &= K_v [v_\beta(k) - e_\beta(k)] - K_i i_\beta(k-1)
\end{aligned} \tag{4.6}$$

where K_v and K_i are defined as [258]:

$$\begin{aligned}
K_v &= \frac{T_s}{L_f + (R_f + R)T_s} \\
K_i &= \frac{L_f}{L_f + (R_f + R)T_s}.
\end{aligned} \tag{4.7}$$

By shifting the variables in (4.6) one-sample forward, the following system can be ob-

tained:

$$\begin{aligned} i_\alpha(k+1) &= K_v [v_\alpha(k+1) - e_\alpha(k+1)] - K_i i_\alpha(k) \\ i_\beta(k+1) &= K_v [v_\beta(k+1) - e_\beta(k+1)] - K_i i_\beta(k) \end{aligned} \quad (4.8)$$

where $e_\alpha(k+1)$ and $e_\beta(k+1)$ are extrapolated back emf values [77].

The variables in (4.8) can be expressed for a prediction horizon h as:

$$\begin{aligned} i_\alpha(k+h) &= K_v [v_\alpha(k+h) - e_\alpha(k+h)] - K_i i_\alpha(k+h-1) \\ i_\beta(k+h) &= K_v [v_\beta(k+h) - e_\beta(k+h)] - K_i i_\beta(k+h-1). \end{aligned} \quad (4.9)$$

The models in (4.1) to (4.9) correlate the output currents to the switching signals, and with the appropriate selection of switching signals, the converter output currents can be regulated precisely. Note that the model given in (4.7) and (4.9) can be used for grid connection as well, where the load inductor and resistor are replaced by the inductive grid filter and its internal resistance, and the back emf by the grid voltage (which is usually measured for synchronization).

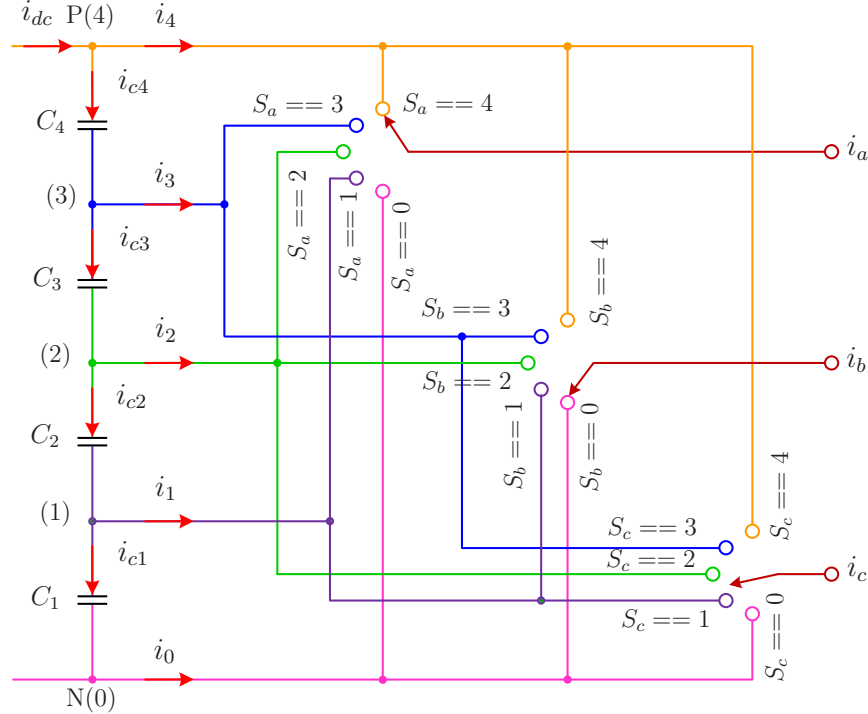


Figure 4.5: Simplified representation of the power circuit model for a 5L-DCC.

4.3.2 Model of DC-link Capacitor Voltages

Another important requirement in the MLDCCs is to balance the dc-link capacitor voltages; otherwise the semiconductor device voltage stress increases. To facilitate the discussion, a 5L-DCC is considered and its simplified dc-link model is represented in Fig. 4.5. The relationship between inverter branch currents (i_1, i_2, i_3, i_4) and capacitor currents $(i_{c1}, i_{c2}, i_{c3}, i_{c4})$ can be expressed as follows considering the representation given in Fig. 4.5:

$$\begin{aligned} i_{c4} &= i_{dc} - i_4, & i_{c3} &= i_{c4} - i_3 \\ i_{c2} &= i_{c3} - i_2, & i_{c1} &= i_{c2} - i_1. \end{aligned} \quad (4.10)$$

By solving the system in (4.10), the capacitor current can be given as:

$$\begin{aligned} i_{c4} &= i_{dc} - i_4 \\ i_{c3} &= i_{dc} - i_4 - i_3 \\ i_{c2} &= i_{dc} - i_4 - i_3 - i_2 \\ i_{c1} &= i_{dc} - i_4 - i_3 - i_2 - i_1. \end{aligned} \quad (4.11)$$

The common current i_{dc} does not contribute to the voltage drift of the capacitors, therefore, (4.11) can be simplified as:

$$\begin{aligned} i_{c4} &= -i_4 \\ i_{c3} &= -i_4 - i_3 \\ i_{c2} &= -i_4 - i_3 - i_2 \\ i_{c1} &= -i_4 - i_3 - i_2 - i_1. \end{aligned} \quad (4.12)$$

The inverter branch currents (i_1, i_2, i_3, i_4) can be expressed in terms of load currents (i_a, i_b, i_c) and MLDCC switching states as follows:

$$\begin{aligned} i_4 &= (S_a == 4) i_a + (S_b == 4) i_b + (S_c == 4) i_c \\ i_3 &= (S_a == 3) i_a + (S_b == 3) i_b + (S_c == 3) i_c \\ i_2 &= (S_a == 2) i_a + (S_b == 2) i_b + (S_c == 2) i_c \\ i_1 &= (S_a == 1) i_a + (S_b == 1) i_b + (S_c == 1) i_c. \end{aligned} \quad (4.13)$$

By substituting (4.13) in (4.12), the capacitor currents can be related to the load currents

as:

$$\begin{aligned}
i_{c4} &= K_{4a} i_a + K_{4b} i_b + K_{4c} i_c \\
i_{c3} &= K_{3a} i_a + K_{3b} i_b + K_{3c} i_c \\
i_{c2} &= K_{2a} i_a + K_{2b} i_b + K_{2c} i_c \\
i_{c1} &= K_{1a} i_a + K_{1b} i_b + K_{1c} i_c.
\end{aligned} \tag{4.14}$$

The gains $K_{4x}, K_{3x}, K_{2x}, K_{1x}$ are a function of voltage level of the phase $x = a, b, c$ as shown in Table 4.3. This approach can be summarized for an m -level DCC as follows:

$$i_{cj} = \sum_{x=a,b,c} K_{jx} i_x. \quad j = 1, \dots, m-1. \tag{4.15}$$

The gains K_{jx} for phase $x = a, b, c$ can be generalized as:

$$\begin{aligned}
K_{1x} &= \text{sgn}(0 - S_x) \\
K_{2x} &= \text{sgn}(1 - S_x) \text{sgn}(S_x) \\
K_{3x} &= \text{sgn}(2 - S_x) \text{sgn}(S_x) \text{sgn}(S_x - 1) \\
&\vdots \\
K_{(m-2)x} &= \text{sgn}((m-3) - S_x) \text{sgn}(S_x) \text{sgn}(S_x - 1) \cdots \text{sgn}(S_x - (m-4)) \\
K_{(m-1)x} &= \text{sgn}((m-2) - S_x) \text{sgn}(S_x) \text{sgn}(S_x - 1) \cdots \text{sgn}(S_x - (m-3))
\end{aligned} \tag{4.16}$$

where $\text{sgn}(\cdot)$ is a signum function:

$$\text{sgn}(x) = \begin{cases} -1 & \text{if } x < 0 \\ 0 & \text{if } x = 0 \\ 1 & \text{if } x > 0. \end{cases} \tag{4.17}$$

Table 4.3: Relationship between switching states and coefficients of capacitor currents for a 5L-DCC ($x = a, b, c$)

S_x	S_{1x}	S_{2x}	S_{3x}	S_{4x}	v_{xN}	K_{1x}	K_{2x}	K_{3x}	K_{4x}
4	1	1	1	1	$v_{c4} + v_{c3} + v_{c2} + v_{c1}$	-1	-1	-1	-1
3	0	1	1	1	$v_{c3} + v_{c2} + v_{c1}$	-1	-1	-1	0
2	0	0	1	1	$v_{c2} + v_{c1}$	-1	-1	0	0
1	0	0	0	1	v_{c1}	-1	0	0	0
0	0	0	0	0	0	0	0	0	0

The relation between the dc-link capacitor voltages and currents can be expressed in continuous time as:

$$\begin{aligned} \frac{v_{c1}}{dt} &= \frac{1}{C_1} i_{c1} \\ \vdots & \quad \quad \quad \vdots \\ \frac{v_{c(m-1)}}{dt} &= \frac{1}{C_{(m-1)}} i_{c(m-1)} \end{aligned} \quad (4.18)$$

where i_{c1} and $i_{c(m-1)}$ are the currents through the capacitors C_1 and $C_{(m-1)}$, respectively.

The above model can be expressed in discrete time as [81, 279, 281]:

$$\begin{aligned} v_{c1}(k) &= v_{c1}(k-1) + \frac{T_s}{C_1} i_{c1}(k) \\ \vdots & \quad \quad \quad \vdots \\ v_{c(m-1)}(k) &= v_{c(m-1)}(k-1) + \frac{T_s}{C_{(m-1)}} i_{c(m-1)}(k) \end{aligned} \quad (4.19)$$

and,

$$\begin{aligned} v_{c1}(k+1) &= v_{c1}(k) + \frac{T_s}{C_1} i_{c1}(k+1) \\ \vdots & \quad \quad \quad \vdots \\ v_{c(m-1)}(k+1) &= v_{c(m-1)}(k) + \frac{T_s}{C_{(m-1)}} i_{c(m-1)}(k+1) \end{aligned} \quad (4.20)$$

The above expression can be generalized for a prediction horizon h as:

$$\begin{aligned} v_{c1}(k+h) &= v_{c1}(k+h-1) + \frac{T_s}{C_1} i_{c1}(k+h) \\ \vdots & \quad \quad \quad \vdots \\ v_{c(m-1)}(k+h) &= v_{c(m-1)}(k+h-1) + \frac{T_s}{C_{(m-1)}} i_{c(m-1)}(k+h) \end{aligned} \quad (4.21)$$

These currents i_{c1} and $i_{c(m-1)}$ can be estimated using the measured load/grid currents (i_a, i_b, i_c) and switching states of the converter [81, 279, 281]. The generalized calculation for an m -level DCC is as follows:

$$i_{cj}(k+h) = \sum_{x=a,b,c} K_{jx}(k+h) i_x(k+h). \quad j = 1, \dots, m-1. \quad (4.22)$$

The dynamics in (4.16)-(4.22) suggests that the dc-link capacitor voltages are also a function of switching signals. The proper selection of switching signal leads to accurate balancing of the capacitor voltages.

4.3.3 Model of Common-Mode Voltage

The modeling of common-mode voltage (CMV) is different for odd-level (3L and 5L) and even-level (4L and 6L) DCCs. In odd-level DCCs, the CMV exists between the neutral-point of the load/motor/grid (n) and the mid-point of dc-link capacitors (o) [274,277]. The CMV in odd-level DCC can be expressed in terms of switching states as follows:

$$v_{cm} = v_{no} = \frac{1}{m-1} \sum_1^{m-1} v_{cj} \frac{1}{3} \sum_{x=a,b,c} \frac{S_x - m + 1}{2}. \quad (4.23)$$

For a 3L-DCC, the above expression can be simplified as:

$$v_{cm} = v_{no} = \frac{v_{c1} + v_{c2}}{2} \frac{(S_a - 2) + (S_b - 2) + (S_c - 2)}{6}. \quad (4.24)$$

In even-level DCCs, the number of dc-link capacitors is odd and there exists no mid-point. The CMV is measured between the neutral-point of the load/motor/grid (n) and the negative dc-rail (N) [276]:

$$v_{cm} = v_{nN} = \frac{v_{aN} + v_{bN} + v_{cN}}{3} \quad (4.25)$$

where v_{aN} , v_{bN} and v_{cN} are inverter terminal voltages [refer to Eq.(4.2)].

The systems in (4.2), (4.23) and (4.25) depict that the CMV is related to the switching signals. In odd-level DCCs, the CMV can be reduced to zero value with the proper selection of switching signals. In the even-level DCCs, there exists no switching state which would achieve a zero CMV value [276], but it can be reduced to some extent with the optimal selection of switching states. Additional hardware such as common-mode choke is required in even-level DCCs to reduce the CMV to zero.

4.4 Predictive Control of Multilevel Diode-Clamped Converters

Based on the generalized model discussed before, a predictive control approach is presented in this section for an m -level converter. The proposed predictive control scheme is shown in Fig. 4.6. As displayed, no PI controllers or modulators are used in the control loop. The main parts of the predictive control are discussed as follows:

4.4.1 Definition of Cost Function

All the control objectives are expressed as cost functions. By minimizing the cost functions during each sampling interval, the control goals can be met.

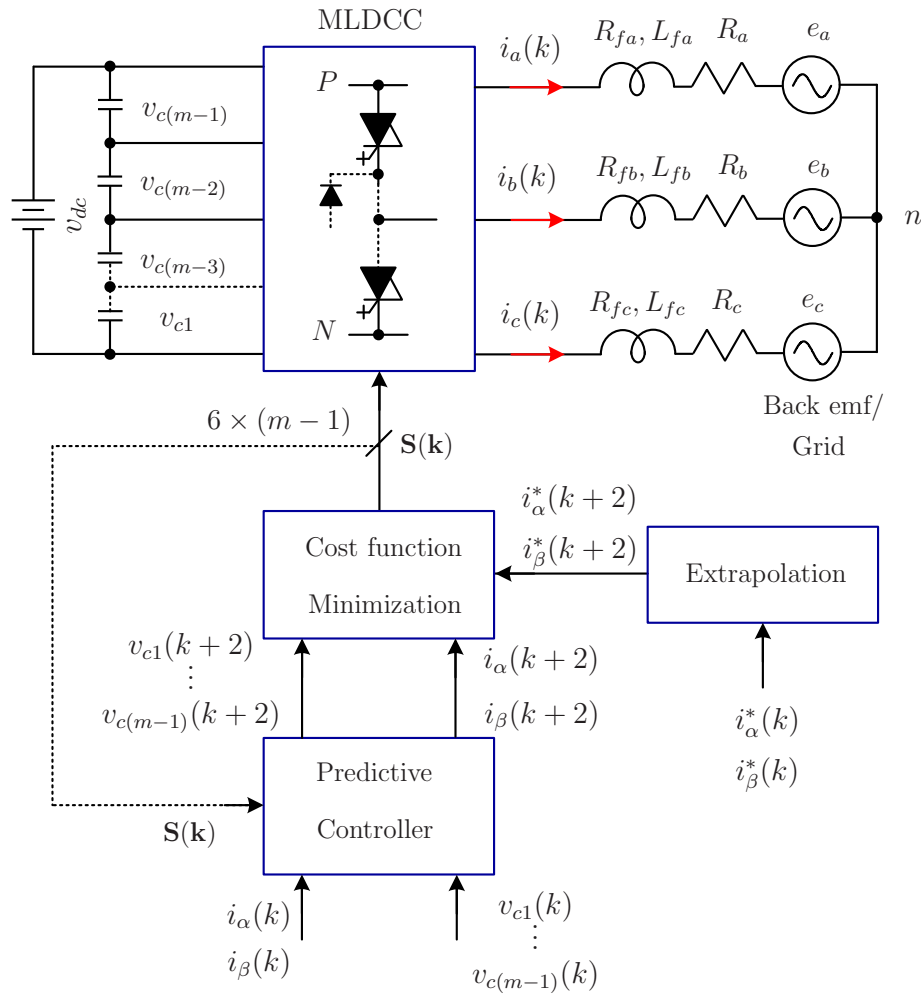


Figure 4.6: FCS-MPC scheme for multilevel diode-clamped converter.

The main objective for the DCC is to regulate the load/motor/grid current which is expressed as:

$$g_{track}(k) = [i_{\alpha}^*(k+h) - i_{\alpha}(k+h)]^2 + [i_{\beta}^*(k+h) - i_{\beta}(k+h)]^2 \quad (4.26)$$

where $i_{\alpha}^*(k+h)$ and $i_{\beta}^*(k+h)$ are the extrapolated references to the h -state. This can be performed using Lagrange or vector angle extrapolation [77, 258].

The dc-link capacitor voltages balancing objective is expressed as another cost function:

$$g_{dc}(k) = \lambda_{dc} \sum_{j=1, \dots, m-1} [v_{cj}(k+h) - v_{cj+1}(k+h)]^2 \quad (4.27)$$

where λ_{dc} is the weighting factor for the dc capacitor voltages balancing task.

The switching frequency minimization can be achieved by penalizing the cost function as:

$$g_{swc}(k) = \lambda_{swc} \sum_{x=a,b,c} swc_x \quad (4.28)$$

where λ_{swc} is the weighting factor for the switching frequency minimization. swc_x represents the number of switch changes involved in phase $x = a, b, c$, and they can be calculated as shown in Table 4.4. $S_{x,op}(k)$ is the optimal voltage vector in the previous sample.

Table 4.4: Calculation of number of switch changes for MLDCC ($x = a, b, c$)

swc_x	$S_x(k+1)$							
	0	1	2	3	4	5	\dots	(m-1)
$S_{x,op}(k) = \mathbf{0}$	0	2	4	6	8	10	\dots	$2(m-1)$
$S_{x,op}(k) = \mathbf{1}$	2	0	2	4	6	8	\dots	$2(m-2)$
$S_{x,op}(k) = \mathbf{2}$	4	2	0	2	4	6	\dots	$2(m-3)$
$S_{x,op}(k) = \mathbf{3}$	6	4	2	0	2	4	\dots	$2(m-4)$
$S_{x,op}(k) = \mathbf{4}$	8	6	4	2	0	2	\dots	$2(m-5)$
$S_{x,op}(k) = \mathbf{5}$	10	8	6	4	2	0	\dots	$2(m-6)$
\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots
$S_{x,op}(k) = (\mathbf{m-1})$	$2(m-1)$	$2(m-2)$	$2(m-3)$	$2(m-4)$	$2(m-5)$	$2(m-6)$	\dots	0

The CMV minimization objective can be expressed as:

$$g_{cmv}(k) = \lambda_{cmv} |v_{cm}| \quad (4.29)$$

where λ_{cmv} is the weighting factor for CMV reduction.

The final cost function combining (4.26)-(4.29) is given as:

$$g(k) = g_{track}(k) + g_{dc}(k) + g_{swc}(k) + g_{cmv}(k). \quad (4.30)$$

4.4.2 Selection of Weighting Factors

The selection of values for the weighting factors is very important. Unfortunately, in state-of-the-art predictive control, no analytical or numerical formulas are available for the calculation of weighting factor values, but the guidelines given in [247] can be used. The main objective of the controller is to regulate the load current, and thus the λ_{track} value can be set to 1 [262, 279].

The second requirement is balancing the dc-link capacitor voltages. A very high value for λ_{dc} will create perfect balance in the capacitor voltages, but with higher tracking errors and THD for the load currents. Similarly, a low value for λ_{dc} leads to a drift in the capacitor voltages, but very good regulation of load currents. A good compromise is to select λ_{dc} such that the drift in capacitor voltages is around 2% of nominal dc-link voltage.

The selection of λ_{swc} is specific to the applications involving the MLDCCs. For megawatt-level applications, the device switching frequency should be maintained below 1 kHz to allow proper heat dissipation [271]. From Table 4.4, it can be discerned that the number of switch changes increase with the increase in number of levels in the DCCs. To achieve a switching frequency value, the weighting factor λ_{swc} decreases with the increase in number of levels. In odd-level MLDCCs, a minimal value of λ_{cmv} should be selected such that the CMV becomes zero. In even-level MLDCCs, the selection criteria for λ_{cmv} should consider the load current tracking error and THD limit imposed by the application.

4.4.3 Selection of Prediction Horizon $-h$

Many FCS-MPC applications are reported to use the one-step prediction horizon ($h = 1$) [shown in Fig. 4.7(a)] along with the delay compensation method introduced in Fig. 3.11, as this approach involves a lower computational burden [77, 279, 281–283]. To compensate the computational delay caused by the digital signal processor, another approach based on a simplified two-step prediction horizon ($h = 2$) can be used, and this method is given in Fig. 4.7(b). With this approach, the switching state which minimizes the cost function at the $(k + 2)$ instant is selected and applied at the sampling instant (k) . As shown in Fig. 4.7(b), the same voltage vectors are used in the $(k + 1)$ and $(k + 2)$ predictions to reduce the number of calculations:

$$\begin{aligned} v_\alpha(k + 2) &= v_\alpha(k) \\ v_\beta(k + 2) &= v_\beta(k) \\ K_{jx}(k + 2) &= K_{jx}(k). \end{aligned} \tag{4.31}$$

To facilitate the two-step predictive strategy, the control variable behavior at the $(k + 2)$ instant should be predicted using all the possible switching states of the converter. The model in (4.9) is used to predict the future load/grid currents, $i_\alpha(k + 2)$ and $i_\beta(k + 2)$. The inverter voltages $v_\alpha(k)$ and $v_\beta(k)$ are obtained by converting the natural frame variables given in Eq.(4.2). The $(k + 2)$ instant dc-link capacitor voltages $[v_{c1}(k + 2) \cdots v_{c(m-1)}(k + 2)]$ are obtained according to the discrete-time models given in (4.21) and (4.22).

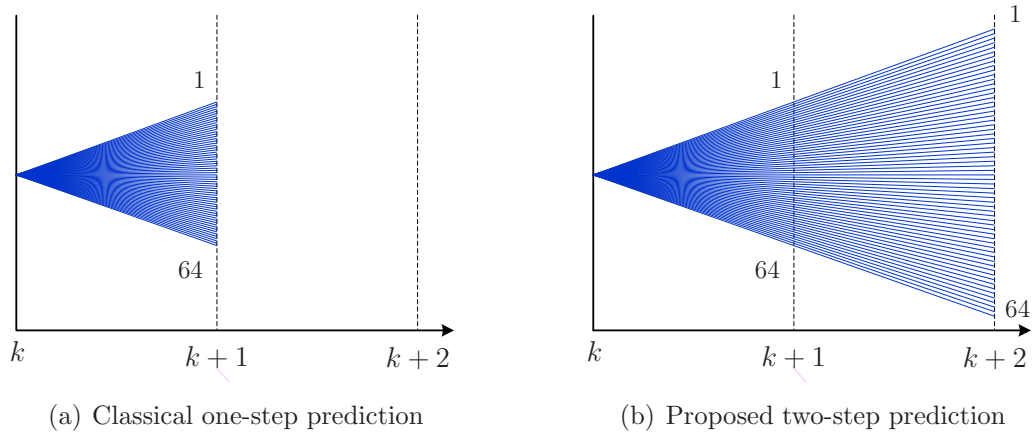


Figure 4.7: Prediction of control variables for a 4L-DCC.

4.4.4 Control Algorithm

The control algorithm with the two-step prediction is shown in Fig. 4.8. The measured load/grid currents and dc-link capacitor voltages are used by the predictive controller. The algorithm is initialized by setting the switching state number i to 0 and optimal g value to ∞ . Then the algorithm enters the loop. The variables at the $(k+1)$ and $(k+2)$ instant are predicted using all the possible switching states of the converter. The predicted variables at the $(k+2)$ instant are evaluated by a cost function $g(k)$. The optimal voltage vector in the previous sampling instant is used by the sub-cost function $g_{swc}(k)$. The switching state which produces a minimal value of g_{op} is chosen and applied to the converter directly. It should be emphasized that the proposed method can be applied to any level DCC without any change in the software configuration, except the switching states definition in the initialization file.

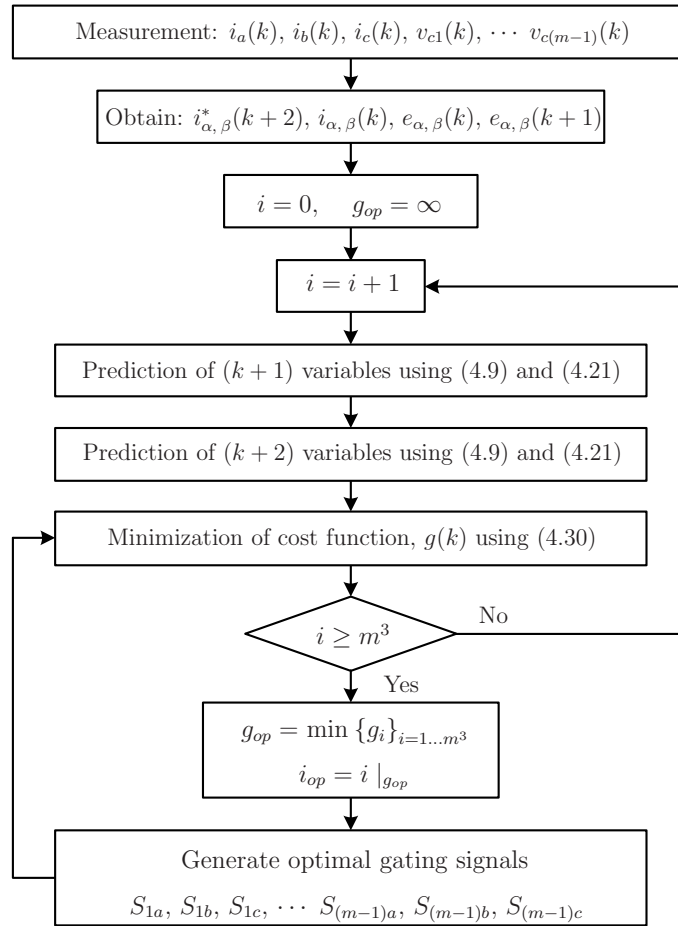


Figure 4.8: Two-step predictive control algorithm for an m -level DCC.

4.5 Simulation Results

To validate the proposed method, simulations are carried using MATLAB/Simulink software with the parameters as indicated in Table 4.5. To be able to validate experimental results under same conditions, low power converter parameters are used. The proposed approach can also be used for megawatt-level systems without any software modification. The sampling time is considered as $T_s = 100 \mu s$. A two-step prediction horizon ($h = 2$) is used and the control delay is ignored. The simulation results are presented for 3L- to 6L-DCCs under the same operating conditions. The load/grid current tracking error (e_i), total harmonic distortion (THD) and average device switching frequency (f_{sw}) are calculated according to the guidelines given in Appendix C.

Table 4.5: Parameters of the MLDCC and controller

Variable	Description	Value
C	dc-link capacitors value	1000 (μF)
R_f	Filter leakage resistance	0.045 (Ω)
L_f	Filter inductance	10 (mH)
i^*	Nominal reference load current	10 (A rms)
f^*	Nominal reference frequency	60 (Hz)
R	Nominal load resistance	10 (Ω)
T_s	Sampling time	100 (μs)
h	Prediction horizon	2
λ_{dc}	Weighting factor	0.1

4.5.1 Transient Analysis

The transient response with a step-change in load currents is studied for 3L- to 6L-DCCs and presented in Fig. 4.9. The switching frequency reduction and CMV suppression are not included in the cost function. The dc-link voltage v_{dc} is set to 300 V. At time $t = 0.0458$ s, a step change in i_α^* is applied from 10 to 5 A (rms). The load currents show good response in reference tracking. The i_β is continued to track to its reference and it is not affected by the changes in i_α . The dc capacitor voltages are well balanced before and after the step-change in load current. Due to the unbalanced load currents, the dc capacitor currents oscillate [refer to (4.22)], and as a consequence the dc capacitor voltages also oscillate [refer to (4.21)]. But the magnitude of the oscillations is very small and can be ignored.

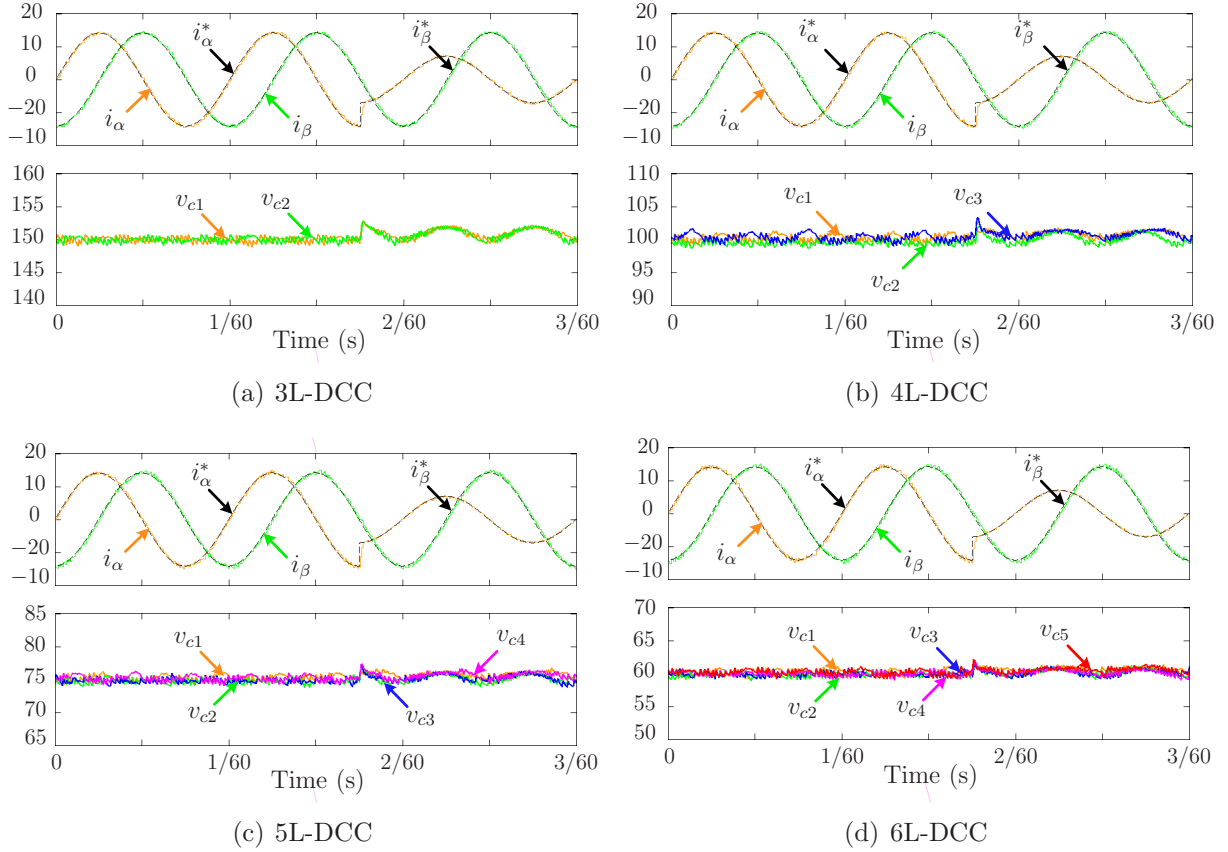


Figure 4.9: Simulation results during step-change in reference load current.

4.5.2 Robustness against DC-link Perturbations

In order to evaluate the performance of the controller, a resistor R_x ($200\ \Omega$) is connected in parallel with the top dc-link capacitor of 3L- to 6L-DCCs and the results are presented in Fig. 4.10. The weighting factors associated with the switching frequency and CMV reduction are set to zero. The v_{dc} and i^* are set to 300 V and 15 A (rms), respectively. Compared to the results presented in Fig. 4.9, the dc-link capacitor voltages contain a low frequency ripple due to the R_x . Even with the perturbation in the dc-link model, the controller chooses an optimal switching state leading to the minimum value of the cost function $g_{dc}(k)$ and thus accurate balancing of the dc-link capacitor voltages. As demonstrated in Fig. 4.10(a) for 3L-DCC, when the weighting factor is deactivated (means $\lambda_{dc} = 0$), the voltage across the top capacitor starts to discharge through the resistor R_x , while the bottom capacitor voltage starts to rise. At $t = 0.4$ s, the weighting factor is activated again ($\lambda_{dc} = 0.1$), and the dc-link capacitor voltages become balanced within a short interval. Similar analysis

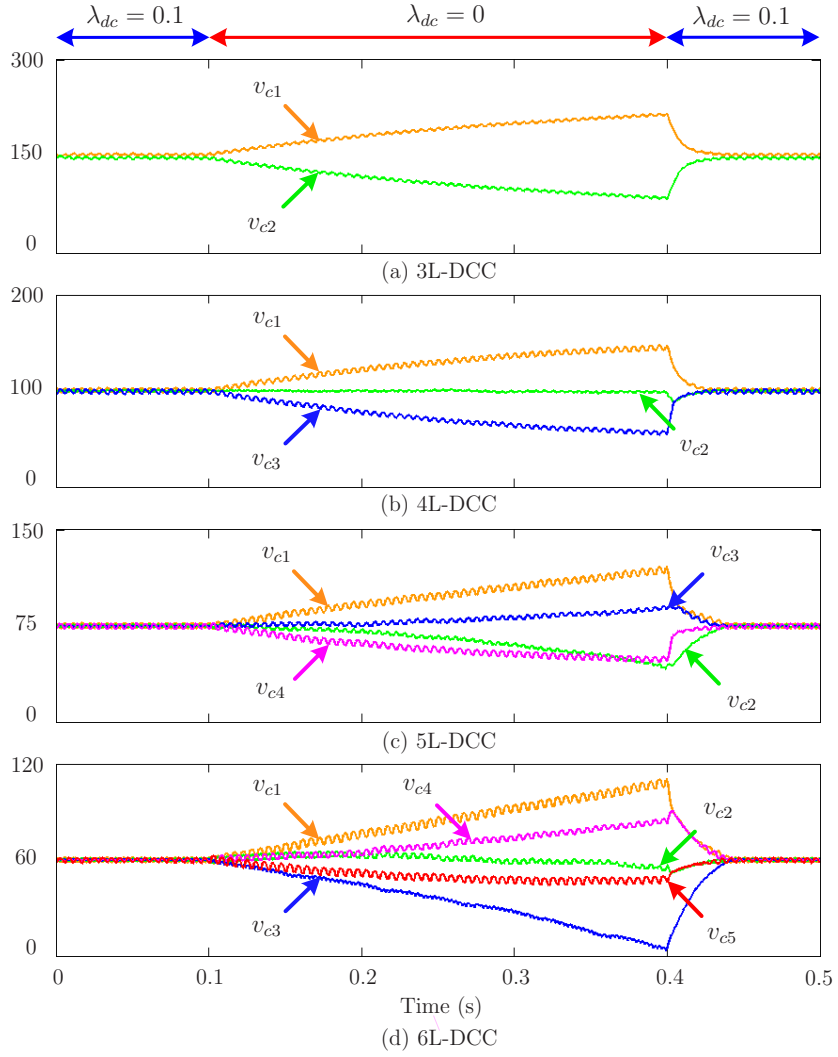


Figure 4.10: Simulation results for dc-link capacitor voltages behavior with and without the weighting factor λ_{dc} .

can be carried out for 4L- to 6L-DCCs. It should be noted that the recovery time from an unbalanced to a balanced condition is approximately the same for all the DCCs. This test verifies that similar to the classical controls, the predictive control method can also be generalized and can be applied to any level DCC.

4.5.3 Switching Frequency Reduction

The switching frequency versus the weighting factor λ_{swc} is studied for 3L- to 6L-DCCs and presented in Fig. 4.11. In order to facilitate the discussion of f_{sw} minimization and its impact on the converter output current quality among different DCCs, the dc-link voltages are assumed to be balanced (by external hardware) and thus $\lambda_{dc} = 0$. The CMV reduction

is also not considered. The v_{dc} and i^* are set to 300 V and 10 A (rms), respectively. At time $t = 2/60$ s, the weighting factor λ_{swc} is changed from 0 to a value suitable for each DCC. Referring to Table 4.4, the cumulative number of switch changes (swc_x) increase with the number of levels in DCC.

For this reason, the weighting factors used for each DCC are different. The performance of the DCC before and after switching frequency minimization is summarized in Table 4.6. It can be seen from Fig. 4.11, as the number of levels increases, the f_{sw} decreases along with the e_i and THD. For all DCCs, as the weighting factor λ_{swc} increases, the f_{sw} decreases, with a slight increase in e_i and THD.

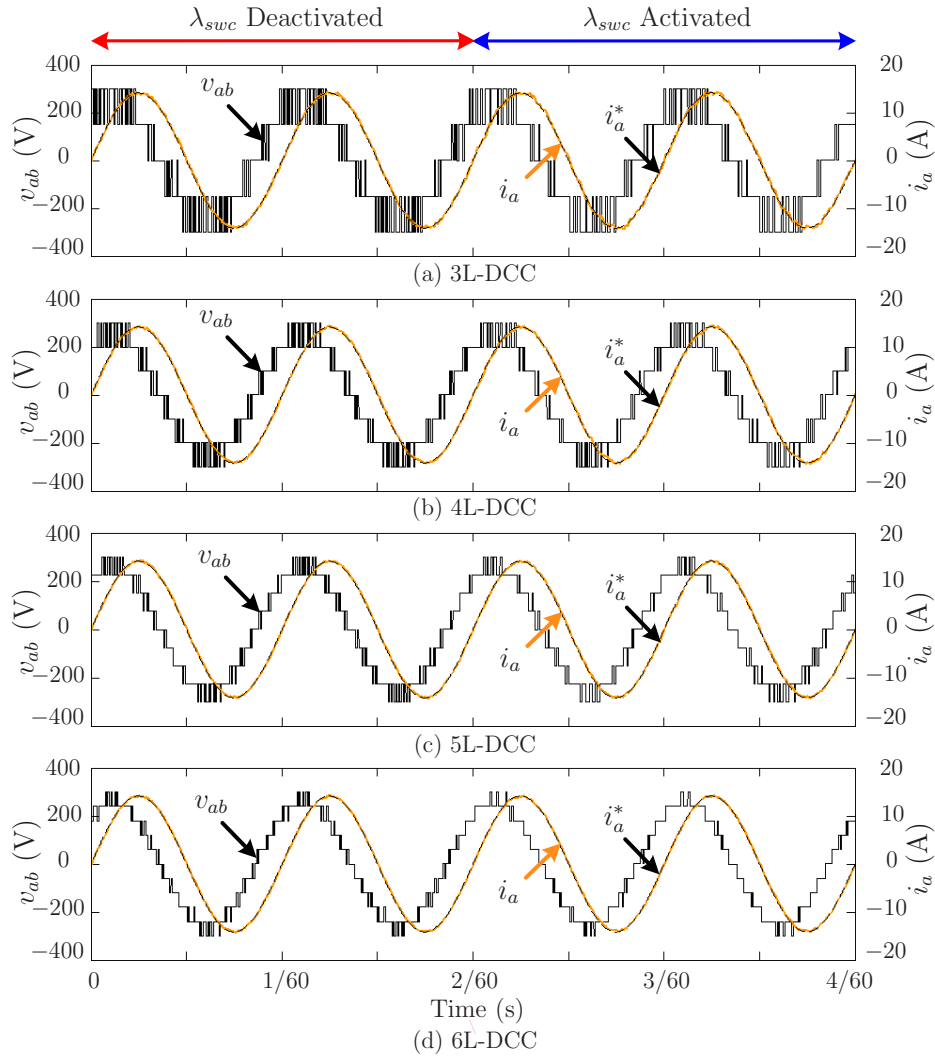


Figure 4.11: Simulation results for switching frequency minimization using the weighting factor λ_{swc} .

Table 4.6: Simulation analysis during f_{sw} minimization

DCC Level	λ_{swc}	e_i (%)	THD (%)	f_{sw} (Hz)
3L	0	2.71	2.11	938
	0.5	3.47	3.29	442
4L	0	2.35	1.41	657
	0.2	2.79	2.07	364
5L	0	2.17	1.14	421
	0.1	2.44	1.51	239
6L	0	2.02	1.01	266
	0.05	2.12	1.24	134

4.5.4 Common-Mode Voltage Mitigation

The CMV mitigation with odd-level (3L and 5L) DCCs are shown in Fig. 4.12, where it has been demonstrated that the CMV can be reduced to zero by choosing a best switching state. The dc supply voltage and load current references are set as 400 V and 10 A (rms), respectively.

At $t = 2/60$ s, the λ_{cmv} is changed from 0 to 0.12 and the CMV is dramatically decreased. At $t = 4/60$ s, the λ_{cmv} is further increased to 0.24 and zero values for the CMV is achieved with 3L and 5L DCCs. The phase- a load current is shown, where it can be observed that the reference tracking is good even with zero CMV. The THD in load currents increase slightly due to the additional weighting term λ_{cmv} . The capacitor voltages are affected due to the CMV reduction, and to maintain them within the ± 5 V range, the weighting factor λ_{dc} is changed from 0.1 to 0.2 at $t = 4/60$ s.

The CMV issue with even-level (4L and 6L) DCCs are presented in Fig. 4.13. The CMV is reduced to some extent with the help of λ_{cmv} . This helps to minimize the rating of additional CMV hardware circuitry (choke). It should be noted that non-zero CMV is the inherent property of even-level DCCs.

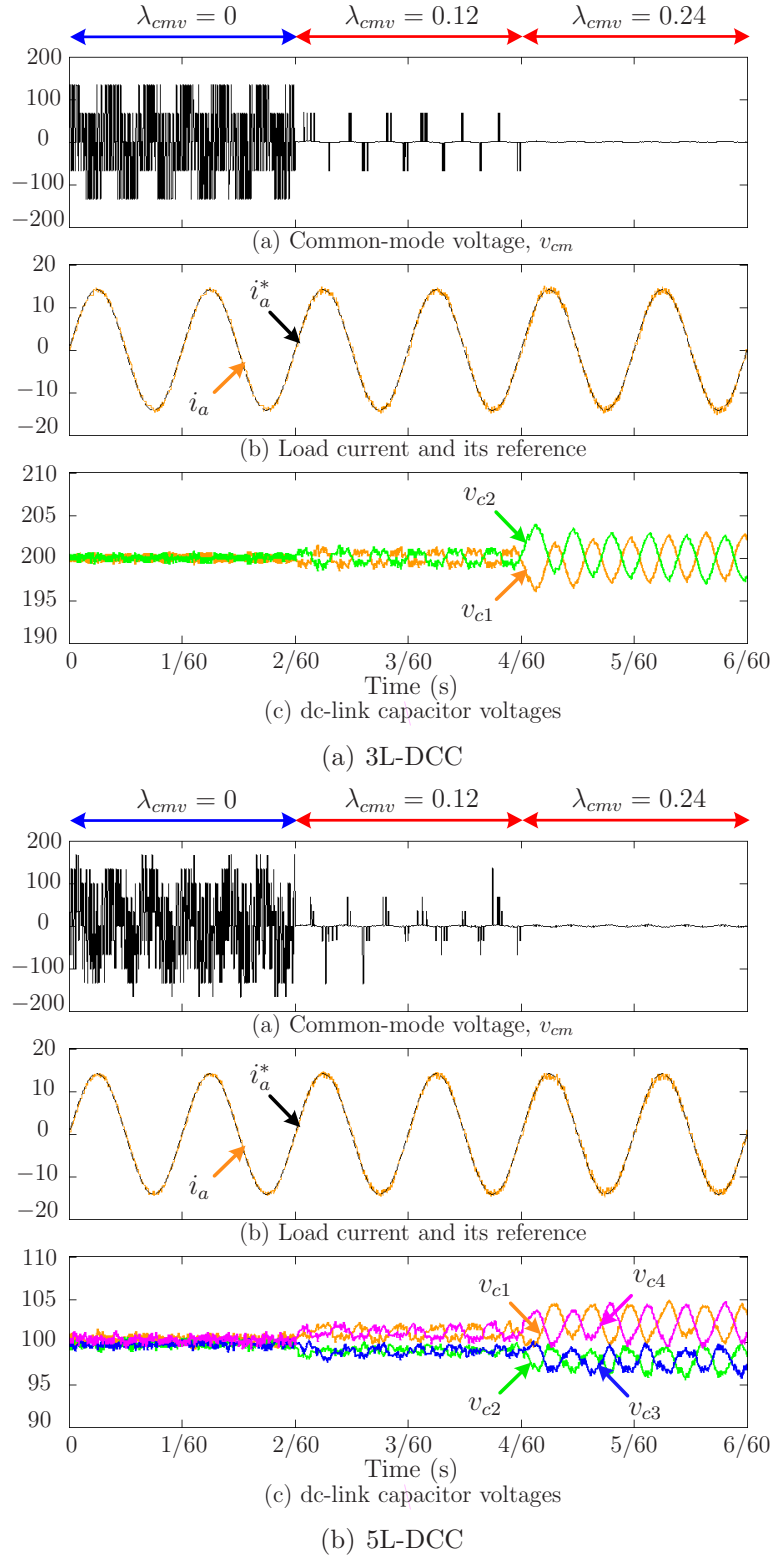
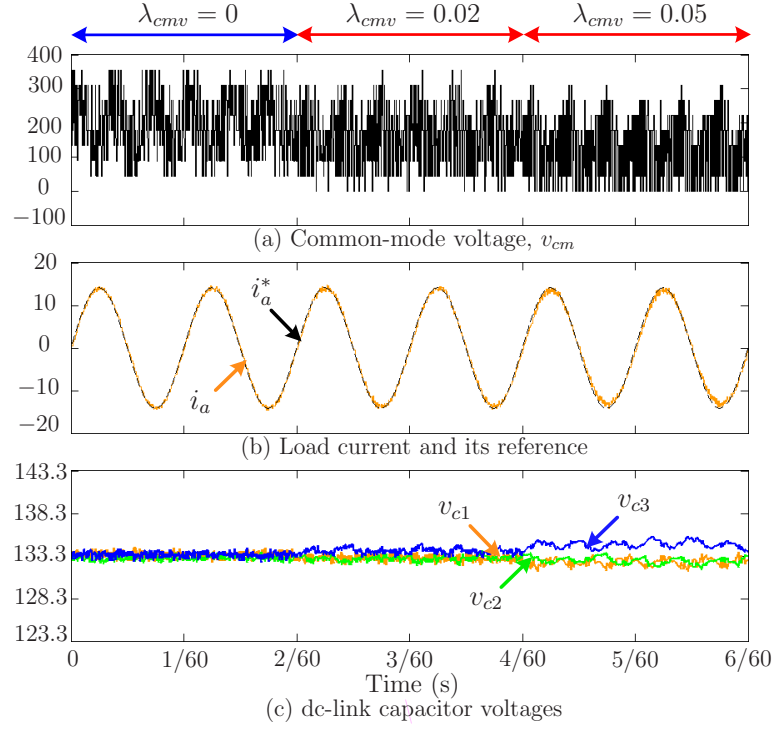
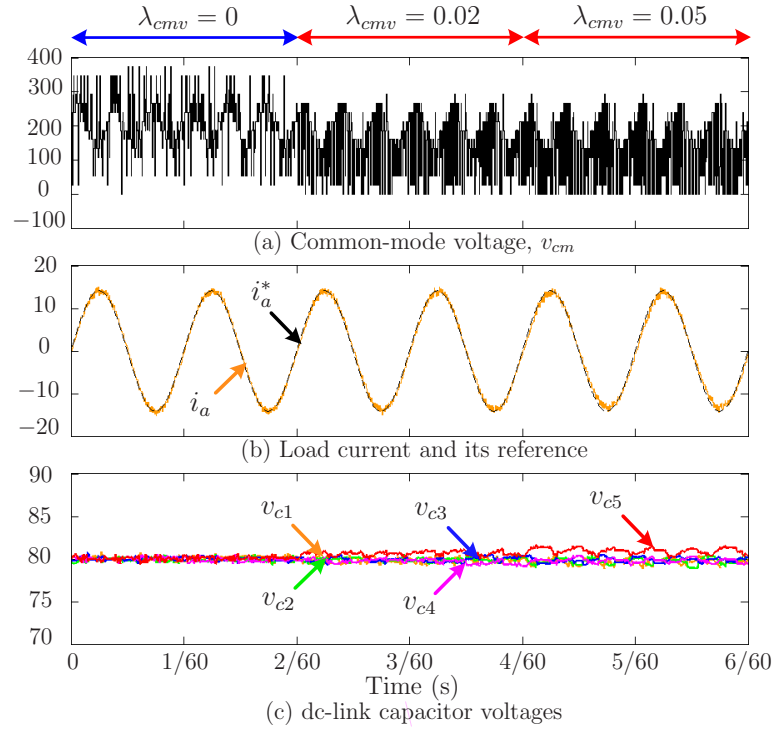


Figure 4.12: Simulation results for common-mode voltage minimization of odd-level converters using the weighting factor λ_{cmv} .



(a) 4L-DCC



(b) 6L-DCC

Figure 4.13: Simulation results for common-mode voltage minimization of even-level converters using the weighting factor λ_{cmv} .

4.6 Experimental Results

The experimental tests are carried out with one odd-level DCC (3L) and one even-level DCC (4L). The complete system parameters are indicated in Table 4.5 which are the same as the ones used in simulation tests. As in the simulations, a two-step prediction horizon ($h = 2$) is used. As the number of levels in the DCCs increase, the computational burden increases. The minimum sampling time (T_s) required to implement the proposed algorithm for 3L- to 6L-DCCs is noted and summarized in Table 4.7. The analysis also shows that the current DSPs can handle the computational requirement, even for 6L-DCC.

Table 4.7: Computational burden with MLDCCs

DCC Level	Number of Switching States	Minimum T_s (μs)
3L	27	18
4L	64	44
5L	125	93
6L	216	221

The experimental results with a step-change in i_α^* from 10 to 5 A (rms) are presented for 3L- and 4L-DCCs in Figs. 4.14(a) and 4.14(b). Again, as in the simulations, load currents track their references accurately. The dc-link capacitor voltages are also balanced with small oscillation (due to unbalanced load currents) after the step-change. The tracking error and load current THD are found to be a little higher than in simulations. This is due to the dead-time caused by the voltage and current transducers, IGBT gate drivers, and ADC units. These results validate the theory and simulation results presented earlier.

The robustness of the predictive controller in overcoming the system perturbations is experimentally validated for 3L- and 4L-DCCs, and presented in Figs. 4.15(a) and 4.15(b). A resistor of $200\ \Omega$ can be deliberately connected in parallel with the top dc-link capacitor to modify the system model. Even with the changes to the system model, the predictive controller works on the selection of best switching state which leads to the minimal value of the cost function. With this phenomenon, the load currents follow their references, and the dc-link capacitor voltages are balanced within set limits. When the controller deactivates, the capacitor voltages diverge similar to the results presented in Fig. 4.10. When the controller is activated, they become balanced with a small recovery time. This test validates that the proposed algorithm is robust and can be applied for any-level DCC.

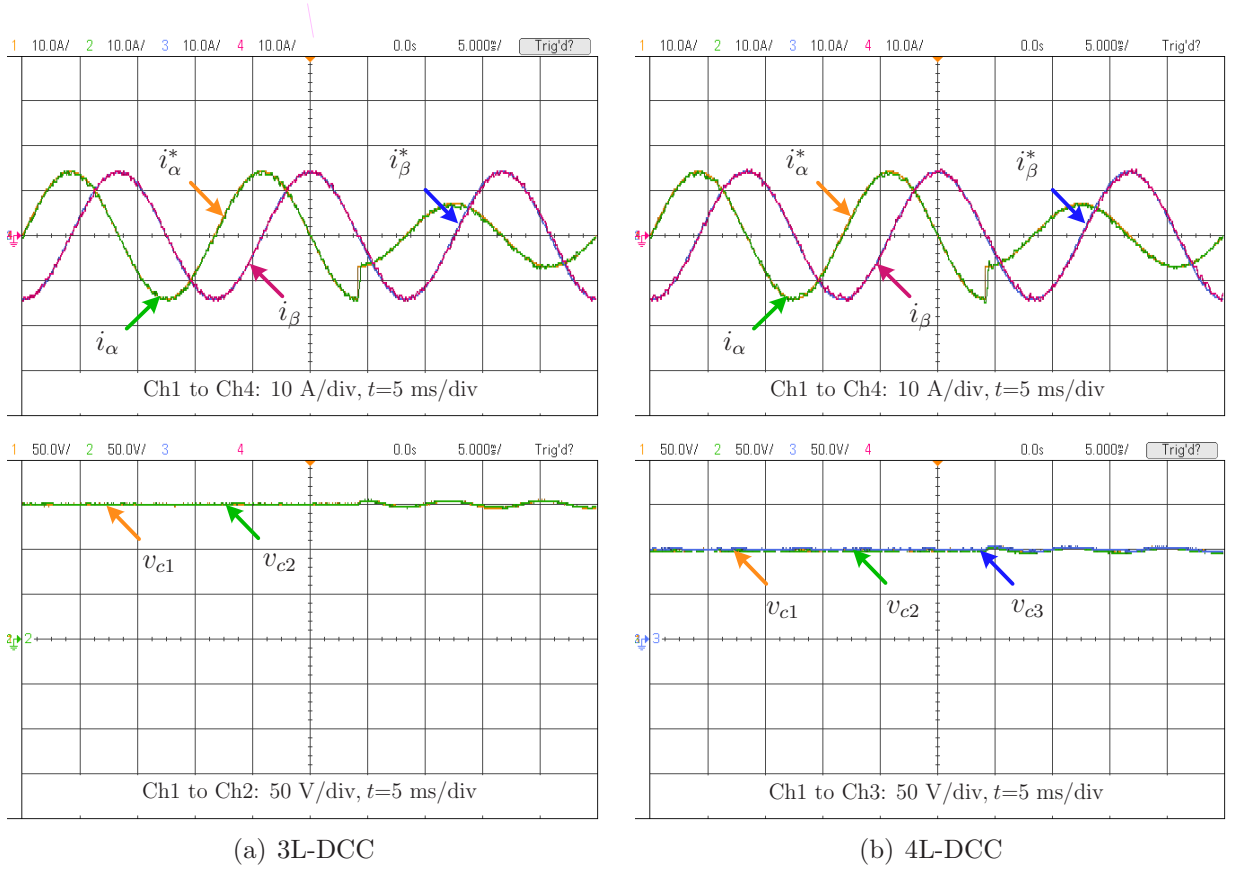
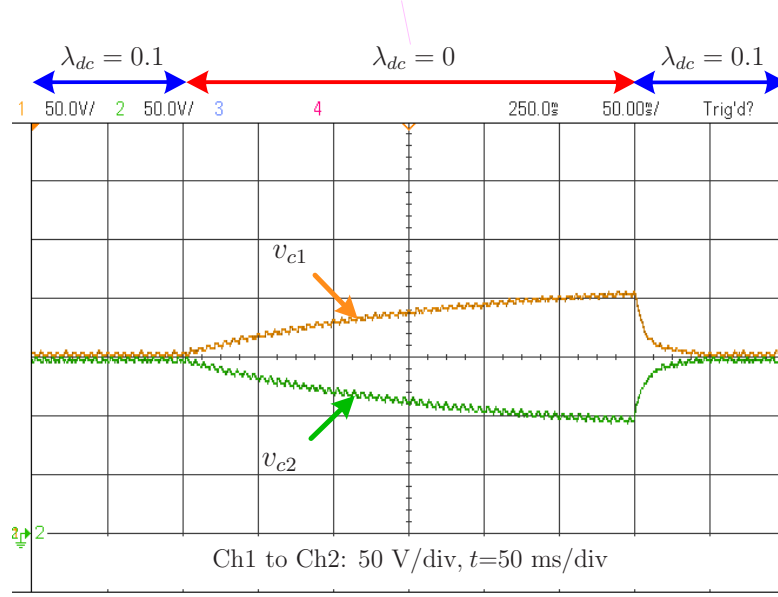


Figure 4.14: Experimental results during step-change in reference to load current.

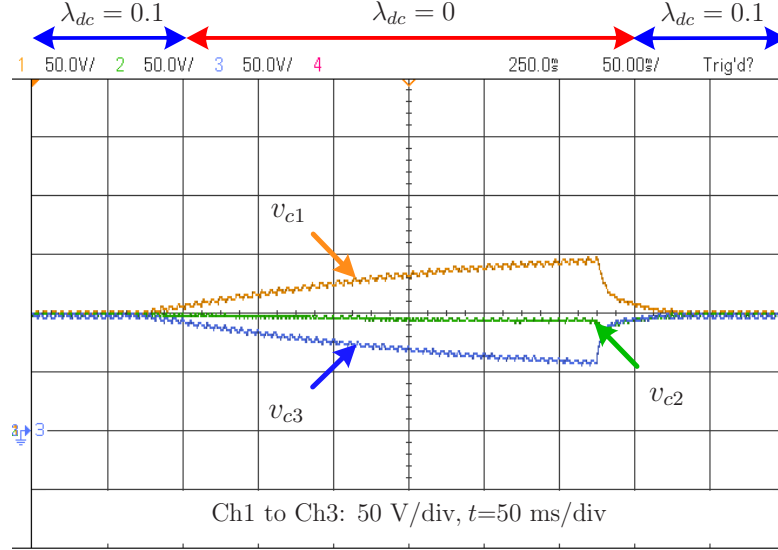
The switching frequency minimization algorithm is experimentally validated with the 3L- and 4L-DCCs and the results are presented in Figs. 4.16(a) and 4.16(b). The dc-link capacitor voltages are externally controlled and the weighting factor λ_{dc} is set to zero. With the increase in λ_{swc} , the switching frequency decreases with a slight increase in the e_i and %THD in converter output current. The analysis with 3L- and 4L-DCCs is summarized in Table 4.8. These results are in a close relation to the simulation analysis presented in Table 4.6.

Table 4.8: Experimental analysis during f_{sw} minimization

DCC Level	λ_{swc}	e_i (%)	THD (%)	f_{sw} (Hz)
3L	0	3.2	3.0	817
	0.5	4.3	4.0	417
4L	0	2.83	2.25	612
	0.2	3.41	3.18	306



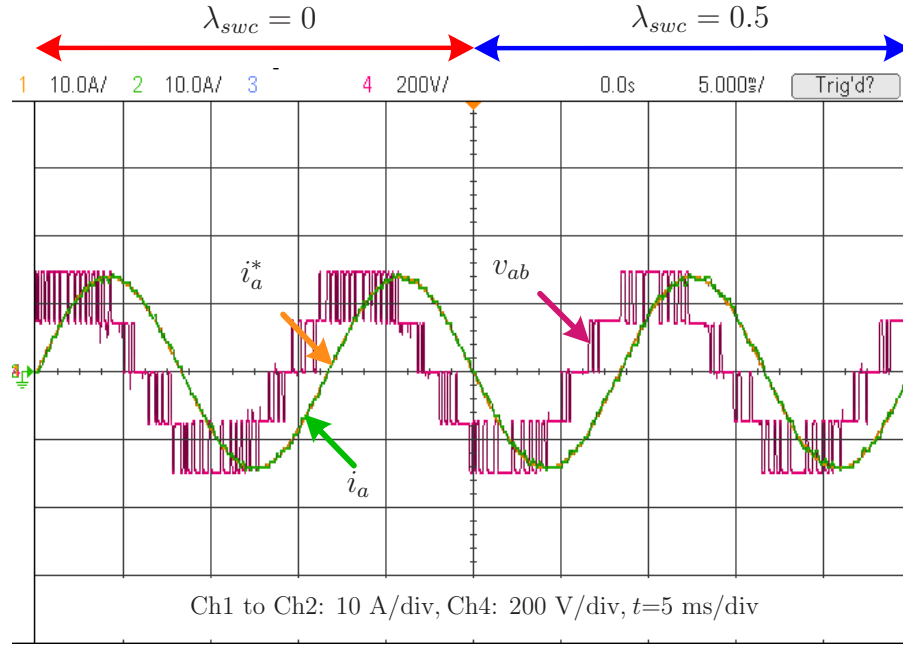
(a) 3L-DCC



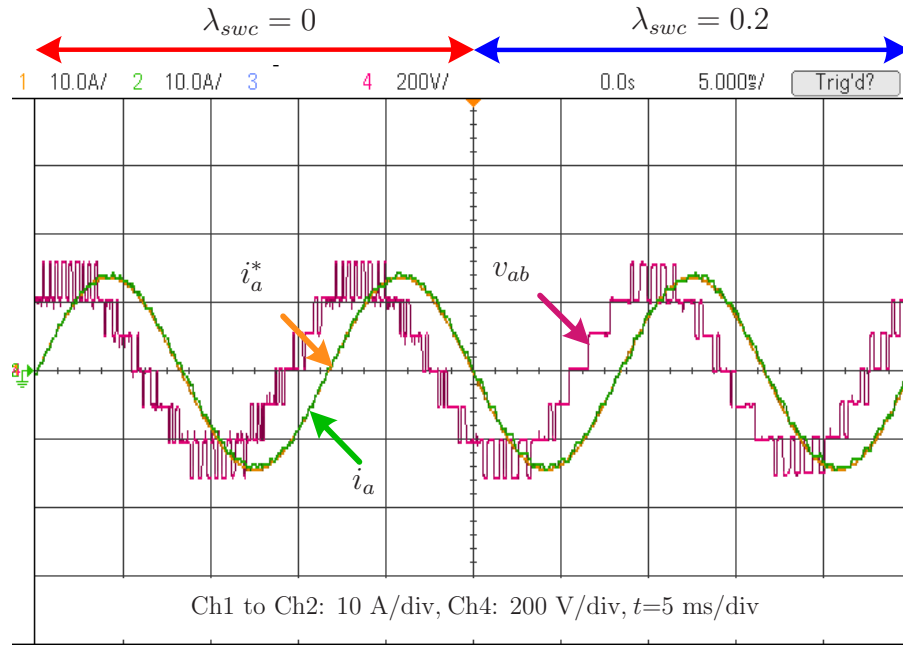
(b) 4L-DCC

Figure 4.15: Experimental results for dc-link capacitor voltages behavior with and without the weighting factor λ_{dc} .

The CMV suppression for 3L-DCC is presented in Fig. 4.17(a), where, with the help of the weighting factor λ_{cmv} , the CMV is reduced to zero. The value of the weighting factor and the system parameters are exactly the same as in simulation tests. While minimizing the CMV, the e_i , %THD and drift in capacitor voltages increased slightly. The experimental results with 4L-DCC are presented in Fig. 4.17(b) and thus, it is demonstrated that the CMV can be reduced to some lower value. These results validate the proposed CMV algorithm.



(a) 3L-DCC



(b) 4L-DCC

Figure 4.16: Experimental results for switching frequency minimization using the weighting factor λ_{swc} .

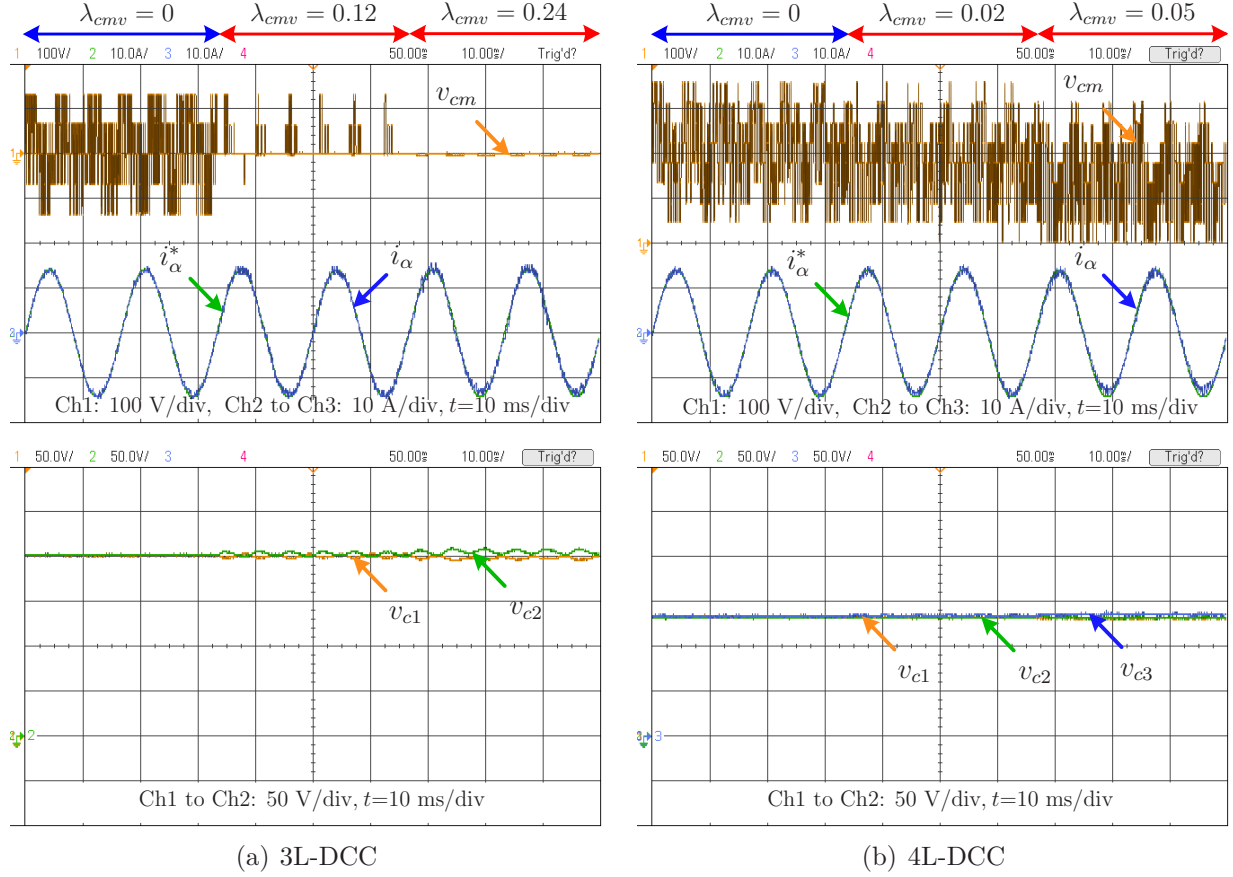


Figure 4.17: Experimental results for common-mode voltage reduction using the weighting factor λ_{cmv} .

4.7 Conclusion

In this chapter, a generalized approach based on finite control set model predictive strategy has been presented for multilevel diode-clamped converters. The dynamics of the load/motor/grid currents, dc-link capacitor voltages, switching frequency and common-mode voltage are formulated in terms of switching states and the mathematical model of the converter. A proper selection of switching state leads to a minimum value of cost function and with this, all four control objectives are accomplished simultaneously. The common-mode voltage is completely suppressed in odd-level converters by just adding a constraint to the cost function. The proposed method shows an intuitive and promising approach to balance the dc-link capacitor voltages, even with the perturbations in the system model and parameters.

Chapter 5

Predictive Current Control of Grid-Tied Diode-Clamped Inverters

In the Chapter 4, a generalized method for the predictive control of multilevel (ML) diode-clamped converters was presented. In this chapter, the predictive control approach is extended to the grid-tied diode-clamped inverters (DCIs). As discussed in Chapter 2, the three-level (3L) and four-level (4L) DCIs are the most suitable candidates for the grid connection of a medium voltage (MV) wind energy conversion systems (WECS). The implementation of predictive control is the same for 3L and 4L-DCIs as discussed in Chapter 4, and this is true for the grid-tied case as well. In comparison to the 3L-DCI [62, 72], the 4L-DCI for high power WECS offers added benefits such as: MV operation with greatly reduced device voltage rating [106], increased equivalent switching frequency [84], lower values for the grid-side filter, grid friendly waveforms, and grid code compliance. However, the complexity of control system increases compared to the 3L-DCI.

In this chapter, predictive control of a grid-tied 4L-DCI is presented. The control objectives, such as regulation of net dc-bus voltage, reactive power generation, dc-link capacitor voltages balancing, and switching frequency minimization are included in the cost function. During different operating conditions, the switching frequency is regulated between 750 and 850 Hz with the help of a lookup table based on the weighting factor. To validate the proposed method, MATLAB simulations are carried out on 4 MVA/4000 V system and dSPACE DS1103 based experiments are performed on 5 kVA/208 V prototype.

5.1 Overview of Grid-Tied Inverters

The configuration of Type-4 variable-speed WECS with full-scale power converters (two-level or multilevel) is shown in Fig. 5.1. The generator-side ac/dc converter is used to harvest more energy from wind, while the grid-tied dc/ac inverter is employed to deliver the generated power to a three-phase grid/collection point. The ac/dc power conversion can be achieved by active or passive generator-side converters as discussed in Chapter 2. The grid connection is usually performed through a harmonic filter L_g to reduce the grid current distortion, and a step-up transformer (not shown to simplify the figure) to increase the inverter output voltage to transmission level. In commercial wind turbines, the harmonic filter L_g value (combined with the leakage inductance of the transformer, if any) is chosen to be in the range of 0.1-0.25 p.u. [2, 10, 14]. The internal resistance of the harmonic filter is represented as R_g . The grid-tied inverter is a crucial element in wind turbines to comply with the stringent grid-codes. In this chapter, a detailed analysis is given related to the operation of grid-tied inverters. The analysis presented here is valid for two-level and multilevel converters.

In a complete WECS composed of full-scale power converters, the following variables needs to be regulated to achieve high-performance operation:

- Active power control
- Grid reactive power control
- Net dc-bus voltage control
- Balancing of dc-link capacitor voltages (in multilevel converters)

As shown in Fig. 5.1, the generator-side ac/dc converter performs the maximum power point tracking (MPPT) to harvest more energy from the wind. This operation is called active power control. More details about the MPPT algorithms can be found in [2, 6, 14, 47, 51, 284–289]. The grid reactive power and net dc-bus voltage are controlled by the grid-tied dc/ac inverter. The dc-link capacitor voltages are controlled by both ac/dc and dc/ac converters if back-to-back connected converters are employed [67]. If the generator-side power conversion is realized by a diode-rectifier, then the capacitor voltages control is performed by the dc/ac inverter alone. In this chapter, the analysis has been carried out assuming that the dc/ac inverter is responsible solely for balancing of dc-link capacitor voltages.

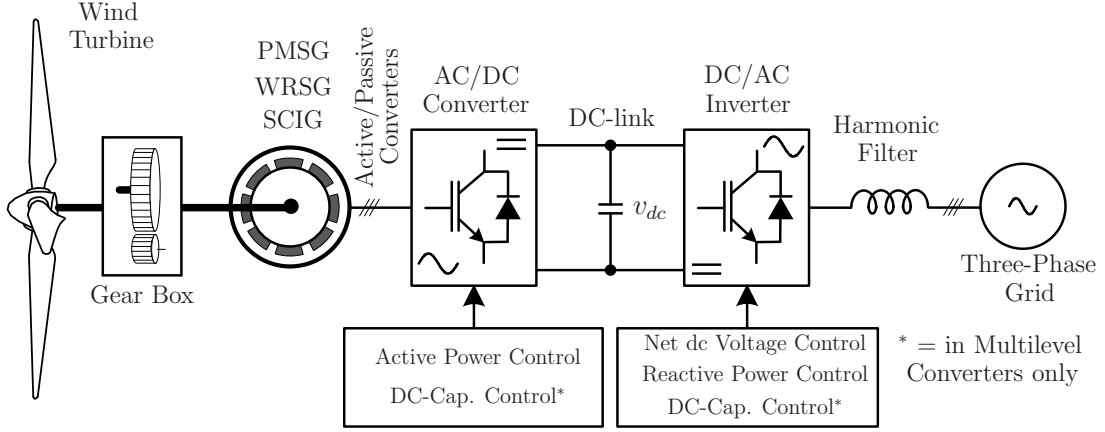


Figure 5.1: Configuration of Type-4 WECS with full-scale power converters.

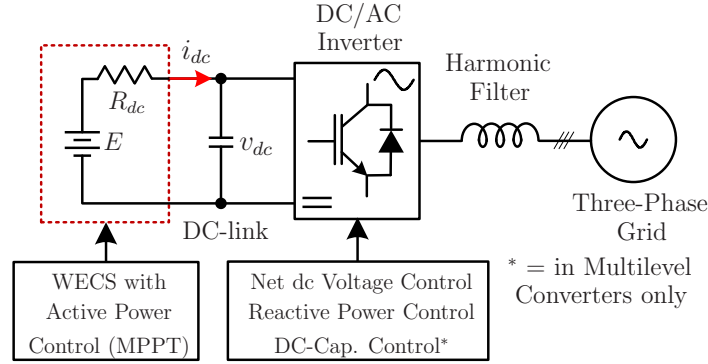


Figure 5.2: Simplified representation of Type-4 WECS.

In order to perform detailed analysis on the grid-tied inverter, a simplified Type-4 WECS is developed as shown in Fig. 5.2. In the complete WECS as represented in Fig. 5.1, the generator-side ac/dc converter, along with the active power control, injects current i_{dc} according to the maximum energy harvested from the wind. When the wind turbine operates below cut-in wind speed, the i_{dc} supplied by the generator-side converter is zero. Similarly, when the turbine operates at rated wind speed, the i_{dc} is rated. In order to simulate such a variable-speed wind energy system, a variable dc-current source is generated with the help of battery supply E and a resistor R_{dc} [2, 14]. The amount of active power injected into the grid can be varied by changing the value of i_{dc} . When the battery voltage $E > v_{dc}$, the i_{dc} $[=(E - v_{dc})/R_{dc}]$ becomes positive and power flows from the inverter to the grid, which is the usual case in WECS. For a given value of R_{dc} , by adjusting E value, the active power generation can be adjusted. During different active power levels, the grid-tied inverter should control the net dc-bus voltage and grid reactive power.

5.1.1 Definition of Grid-side Control Variables

In this section, the selection of grid-tied inverter control variables is discussed:

- **Definition of dc-link Voltage Reference:** To ensure the proper operation of the grid-tied inverter, the dc-bus voltage should be higher than the grid line-line voltage. In this work, the dc-bus voltage reference v_{dc}^* is selected such that the inverter operates with a 0.8 modulation index, leaving a 20 % margin for adjustment during transients and grid voltage variations. Following this discussion, the v_{dc}^* is defined as,

$$v_{dc}^* = \frac{\sqrt{6} v_g}{m_a} = \frac{\sqrt{6} v_g}{0.8} = 3.062 \times v_g \quad (5.1)$$

where v_g is *rms* value of the grid phase voltage, and m_a is the modulation index of the inverter. The control scheme for the grid-tied inverter should ensure that the v_{dc} is maintained at its reference value during all the operating conditions.

- **Definition of Grid Power Factor:** The power flow is bidirectional for the grid-tied inverter, but in WECS the power flow is unidirectional (from the dc-link to the grid). The active and reactive powers delivered to the grid can be calculated as:

$$\begin{aligned} P_g &= 3 V_g I_g \cos \phi_g \\ Q_g &= 3 V_g I_g \sin \phi_g \end{aligned} \quad (5.2)$$

where ϕ_g is the grid power factor angle. The angle between the grid voltage and current vectors is measured as ϕ_g . The grid power factor can be unity, lagging or leading based on the power factor angle:

Unity Power Factor: if $\phi_g = 0^\circ$

Lagging Power Factor: if $\phi_g = 0 - 90^\circ$ lagging

Leading Power Factor: if $\phi_g = 0 - 90^\circ$ leading

Following this assumption, the reference grid reactive power Q_g^* can be set as follows:

Unity Power Factor: if $Q_g^* = 0$

Lagging Power Factor: if $Q_g^* = \text{positive}$

Leading Power Factor: if $Q_g^* = \text{negative}$

5.1.2 Classical Control Schemes for Grid-Tied Inverters

The well-established classical control techniques for grid-tied inverters are the virtual flux-oriented control [69], direct power control [70, 71] and decoupled voltage-oriented control (VOC) [2, 14, 72]. The decoupled VOC has been widely adopted by the wind energy industry. The above-mentioned control techniques use PI regulators in their internal current control loop and a modulation stage to generate the gating signals. A complex modulation technique along with the dc-link capacitor voltages balancing [96, 290] is required to apply these techniques to multilevel inverters. The most common modulation techniques for the four-level inverters are: carrier-based pulse width modulation (PWM) [169, 269] and space vector modulation (SVM) [108, 270]. The device switching frequency reduction to below 1 kHz is another important issue at the megawatt-level to minimize the switching losses and to allow proper heat dissipation [271]. The PWM and SVM techniques produce significantly lower order harmonics when operated below 1 kHz and this causes poor power quality [74]. Moreover, the grid voltage harmonics and control delay will degrade the performance of the PWM/SVM-based controller [76]. The main idea of this work is to replace the PI controllers and modulation stage by predictive controller to achieve high performance operation. The reference control variables are generated similar to the classical VOC scheme.

5.1.3 Grid Voltage Orientation

In order to achieve grid voltage orientation as in VOC, the d -axis of the synchronous reference frame (SRF) is aligned with the grid voltage vector and as a result q -axis grid voltage becomes zero [2]. With this approach, the decoupled control for the grid active and reactive powers can be achieved. Moreover, the calculation of grid active and reactive powers becomes easier as demonstrated below:

$$\left. \begin{aligned} P_g &= \frac{3}{2} (v_{dg} i_{dg} + v_{qg} i_{qg}) = +\frac{3}{2} v_{dg} i_{dg} \\ Q_g &= \frac{3}{2} (v_{qg} i_{dg} - v_{dg} i_{qg}) = -\frac{3}{2} v_{dg} i_{qg} \end{aligned} \right\} v_{qg} = 0 \quad (5.3)$$

where v_{dg} and v_{qg} are d - and q -axis grid voltages, respectively. i_{dg} and i_{qg} are d - and q -axis grid currents, respectively.

5.2 Grid-Tied Four-Level Inverter Model

A simplified configuration of grid-tied 4L-DCI is shown in Fig. 5.3. The inverter is composed of 18 active switches and 18 clamping diodes. The clamping diodes withstand different reverse blocking voltages, and if the voltage rating for all the clamping diodes is selected to be same as the active switches, then a series connection of two diodes is necessary [84] as shown in Fig. 5.3. To simplify the analysis, the following assumptions are made:

$$\begin{aligned} R_{ag} &= R_{bg} = R_{cg} = R_g, & L_{ag} &= L_{bg} = L_{cg} = L_g, \\ v_{ag} + v_{bg} + v_{cg} &= 0, & i_{ag} + i_{bg} + i_{cg} &= 0. \end{aligned} \quad (5.4)$$

The switching states and the corresponding inverter terminal voltages are shown in Table 5.1, where it can be noted that: (a) only three switches conduct at any time, and (b) switch pairs (S_{1x}, \bar{S}_{1x}) , (S_{2x}, \bar{S}_{2x}) and (S_{3x}, \bar{S}_{3x}) operate in a complementary manner [84]. As shown in Fig. 5.4, for a 4L-DCI, 64 switching combinations and 37 voltage vectors are available.

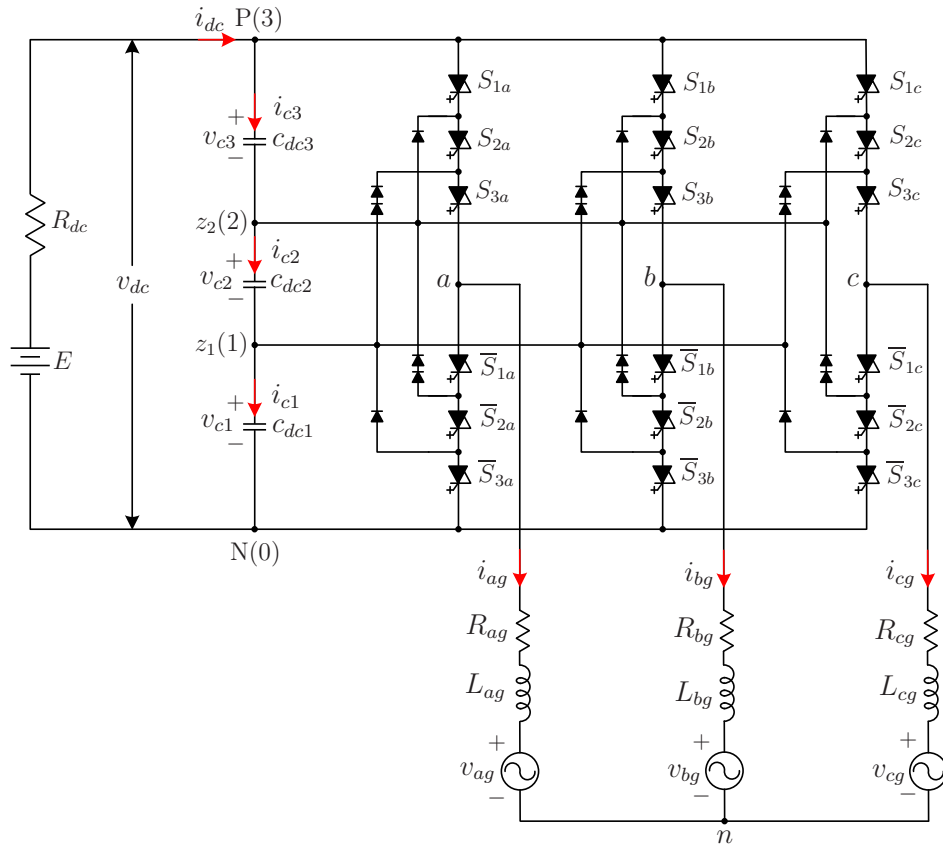


Figure 5.3: Topology of grid-tied 4L-DCI in MV-WECS.

Table 5.1: Switching states and inverter terminal voltages

S_x	S_{1x}	S_{2x}	S_{3x}	\bar{S}_{1x}	\bar{S}_{2x}	\bar{S}_{3x}	v_{xN}
3	1	1	1	0	0	0	$v_{c1} + v_{c2} + v_{c3}$
2	0	1	1	1	0	0	$v_{c1} + v_{c2}$
1	0	0	1	1	1	0	v_{c1}
0	0	0	0	1	1	1	0

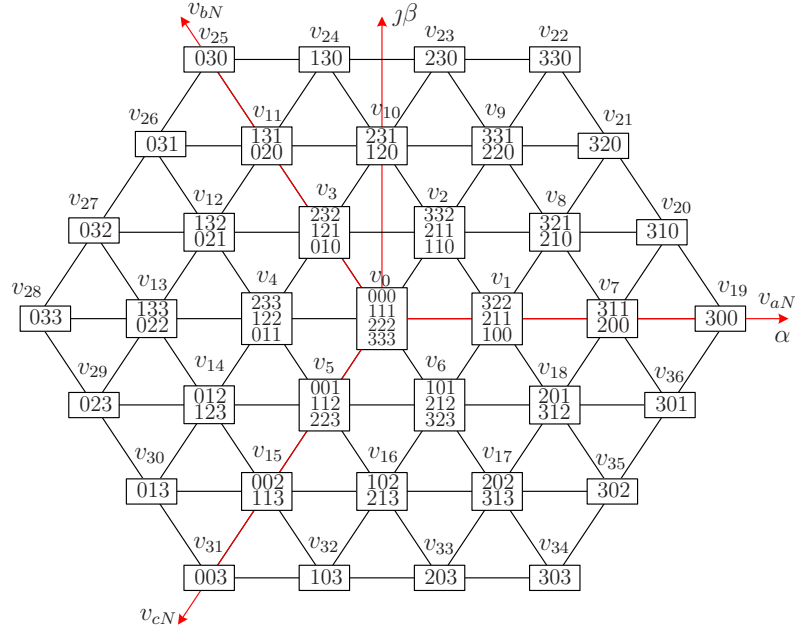


Figure 5.4: Space vector diagram and switching states for a four-level inverter.

As given in Table. 5.1, the voltage in any phase- x of the inverter, measured from the negative point of the dc-link (N), can be expressed in terms of switching signals and dc-link capacitor voltages as follows [108]:

$$\begin{aligned}
 v_{xN} &= (S_x == 0) (0) + (S_x == 1) (v_{c1}) \\
 &+ (S_x == 2) (v_{c1} + v_{c2}) + (S_x == 3) (v_{c1} + v_{c2} + v_{c3}). \quad x = a, b, c.
 \end{aligned} \tag{5.5}$$

With respect to the grid neutral (n) these inverter voltages can be expressed as [77]:

$$\begin{aligned}
 v_{an} &= +\frac{2}{3}v_{aN} - \frac{1}{3}v_{bN} - \frac{1}{3}v_{cN} \\
 v_{bn} &= -\frac{1}{3}v_{aN} + \frac{2}{3}v_{bN} - \frac{1}{3}v_{cN} \\
 v_{cn} &= -\frac{1}{3}v_{aN} - \frac{1}{3}v_{bN} + \frac{2}{3}v_{cN}.
 \end{aligned} \tag{5.6}$$

5.2.1 Modeling of Grid Currents in Synchronous Frame

The grid currents can be expressed in terms of inverter voltages, grid voltages and filter inductance in a natural frame (abc) as [291]:

$$\frac{d\mathbf{i}_g}{dt} = \frac{1}{L_g}[\mathbf{v}_i - \mathbf{v}_g - R_g \mathbf{i}_g]. \quad (5.7)$$

In order to facilitate easier design and control, the measured natural frame grid voltages and currents are converted to synchronous frame. The above natural frame currents can be converted to synchronous frame (dq) and expressed in state-space form as follows [14]:

$$\frac{d}{dt} \begin{bmatrix} i_{dg} \\ i_{qg} \end{bmatrix} = \mathbf{A} \begin{bmatrix} i_{dg} \\ i_{qg} \end{bmatrix} + \mathbf{B}_i \begin{bmatrix} v_{di} \\ v_{qi} \end{bmatrix} + \mathbf{B}_g \begin{bmatrix} v_{dg} \\ v_{qg} \end{bmatrix} \quad (5.8)$$

where

$$\begin{aligned} \mathbf{A} &= \begin{bmatrix} \frac{-R_g}{L_g} & \omega_g \\ -\omega_g & \frac{-R_g}{L_g} \end{bmatrix} \\ \mathbf{B}_i &= \begin{bmatrix} \frac{1}{L_g} & 0 \\ 0 & \frac{1}{L_g} \end{bmatrix} \\ \mathbf{B}_g &= \begin{bmatrix} -\frac{1}{L_g} & 0 \\ 0 & -\frac{1}{L_g} \end{bmatrix}. \end{aligned} \quad (5.9)$$

v_{di} and v_{qi} are the estimated d - and q -axis inverter voltages, respectively. They are obtained by applying abc/dq transformation (for more details refer to Appendix B.2) to the natural frame inverter voltages, v_{an} , v_{bn} , and v_{cn} given in (5.6).

The discrete-time model for d and q -axis grid currents can be obtained from (5.8) for a one-step prediction as follows:

$$\begin{bmatrix} i_{dg}(k+1) \\ i_{qg}(k+1) \end{bmatrix} = \Phi \begin{bmatrix} i_{dg}(k) \\ i_{qg}(k) \end{bmatrix} + \Gamma_i \begin{bmatrix} v_{di}(k) \\ v_{qi}(k) \end{bmatrix} + \Gamma_g \begin{bmatrix} v_{dg}(k) \\ v_{qg}(k) \end{bmatrix} \quad (5.10)$$

where

$$\begin{aligned} \Phi &= e^{\mathbf{A}T_s} \\ \Gamma_i &= \int_0^{T_s} e^{\mathbf{A}(T_s-\tau)} \mathbf{B}_i d\tau = \mathbf{A}^{-1}(\Phi - \mathbf{I}_{2 \times 2})\mathbf{B}_i \\ \Gamma_g &= \int_0^{T_s} e^{\mathbf{A}(T_s-\tau)} \mathbf{B}_g d\tau = \mathbf{A}^{-1}(\Phi - \mathbf{I}_{2 \times 2})\mathbf{B}_g. \end{aligned} \quad (5.11)$$

5.2.2 Modeling of DC-link Capacitor Voltages

From the modeling presented in the Chapter 4, the discrete-time model for dc-link capacitor voltages can be obtained for $j = 1, 2, 3$ as:

$$v_{cj}(k+1) = v_{cj}(k) + \frac{T_s}{C_{dcj}} i_{cj}(k+1) \quad (5.12)$$

where T_s is sampling time, and C_{dc} corresponds to the capacitance of dc-capacitors. The current through the dc-capacitors is denoted as i_{cj} . The dc-link capacitor currents can be expressed in terms of three-phase grid currents and gains K_{1x} , K_{2x} , and K_{3x} as follows:

$$\begin{aligned} i_{c3}(k+1) &= \sum_{x=a,b,c} K_{3x}(k+1) i_{xg}(k+1) \\ i_{c2}(k+1) &= \sum_{x=a,b,c} K_{2x}(k+1) i_{xg}(k+1) \\ i_{c1}(k+1) &= \sum_{x=a,b,c} K_{1x}(k+1) i_{xg}(k+1). \end{aligned} \quad (5.13)$$

The gains K_{1x} , K_{2x} , and K_{3x} are based on the inverter switching states as demonstrated below:

$$\begin{aligned} K_{1x} &= \text{sgn}(0 - S_x) \\ K_{2x} &= \text{sgn}(1 - S_x) \text{sgn}(S_x - 0) \\ K_{3x} &= \text{sgn}(2 - S_x) \text{sgn}(S_x - 0) \text{sgn}(S_x - 1) \end{aligned} \quad (5.14)$$

where sgn is a Signum function whose output value corresponds to -1 or 0 or $+1$.

The performance of the model in [281] and the model presented here are the same in terms of the dc-link capacitor voltages balancing, but the number of online calculations can be reduced with the presented method. The reason is that the gains K_{1x} , K_{2x} , and K_{3x} can be defined off-line along with the switching states.

From (5.10), it can be noticed that, the grid d and q -axis currents are a function of inverter voltages, v_{di} and v_{qi} . These inverter voltages (in natural frame) are related to the switching signals as described in (5.5). Similarly, the models in (5.12)-(5.14) demonstrate that the dc-link capacitor voltages are related to the switching signals. From the modeling presented in this section, it can be concluded that, the grid currents and capacitor voltages can be controlled by properly choosing a switching state.

5.3 Model Predictive Control

The proposed model predictive control scheme as represented in Fig. 5.5 is very easy and intuitive to understand. The implementation procedure is presented as follows:

- Measure grid voltages, $v_{ag}(k)$ and $v_{bg}(k)$, [$v_{cg}(k) = -v_{ag}(k) - v_{bg}(k)$]; grid currents $i_{ag}(k)$ and $i_{bg}(k)$, [$i_{cg}(k) = -i_{ag}(k) - i_{bg}(k)$]; and dc-link capacitor voltages $v_{c1}(k)$, $v_{c2}(k)$, $v_{c3}(k)$. In total 5 voltage sensors and two current sensors are required for a three-phase balanced system (symmetrical grid voltages).
- Obtain grid voltage angle, $\theta_g(k)$ using synchronous reference frame phase-locked loop (SRF-PLL) [14] (for details refer to Appendix B.4).
- Convert grid voltages and currents from natural (abc) frame to synchronous (dq) frame, $v_{dg}(k)$, $v_{qg}(k)$, $i_{dg}(k)$, $i_{qg}(k)$.
- Obtain q -axis reference current $i_{qg}^*(k)$ from $Q_g^*(k)$. By referring to (5.3), the $i_{qg}^*(k)$ can be calculated as:

$$i_{qg}^*(k) = \frac{Q_g^*(k)}{-1.5 v_{dg}(k)}. \quad (5.15)$$

- Obtain d -axis reference current $i_{dg}^*(k)$ which represents the active power of the system. Neglecting losses in the inverter, the active power P_g on ac-side equals dc-power and it is expressed as follows [2]:

$$P_g = \frac{3}{2} v_{dg} i_{dg} = v_{dc} i_{dc}. \quad (5.16)$$

During steady-state, the net dc-bus voltage, v_{dc} is maintained at its reference value v_{dc}^* by the PI controller. The $i_{dg}^*(k)$ is generated by this PI controller according to the operating conditions.

- Extrapolate reference currents from k^{th} state to $(k+1)$ state. The fourth-order Lagrange extrapolation method introduced in Section 3.3.4 is considered:

$$\begin{aligned} i_{dg}^*(k+1) &= 4 i_{dg}^*(k) - 6 i_{dg}^*(k-1) + 4 i_{dg}^*(k-2) - i_{dg}^*(k-3) \\ i_{qg}^*(k+1) &= 4 i_{qg}^*(k) - 6 i_{qg}^*(k-1) + 4 i_{qg}^*(k-2) - i_{qg}^*(k-3). \end{aligned} \quad (5.17)$$

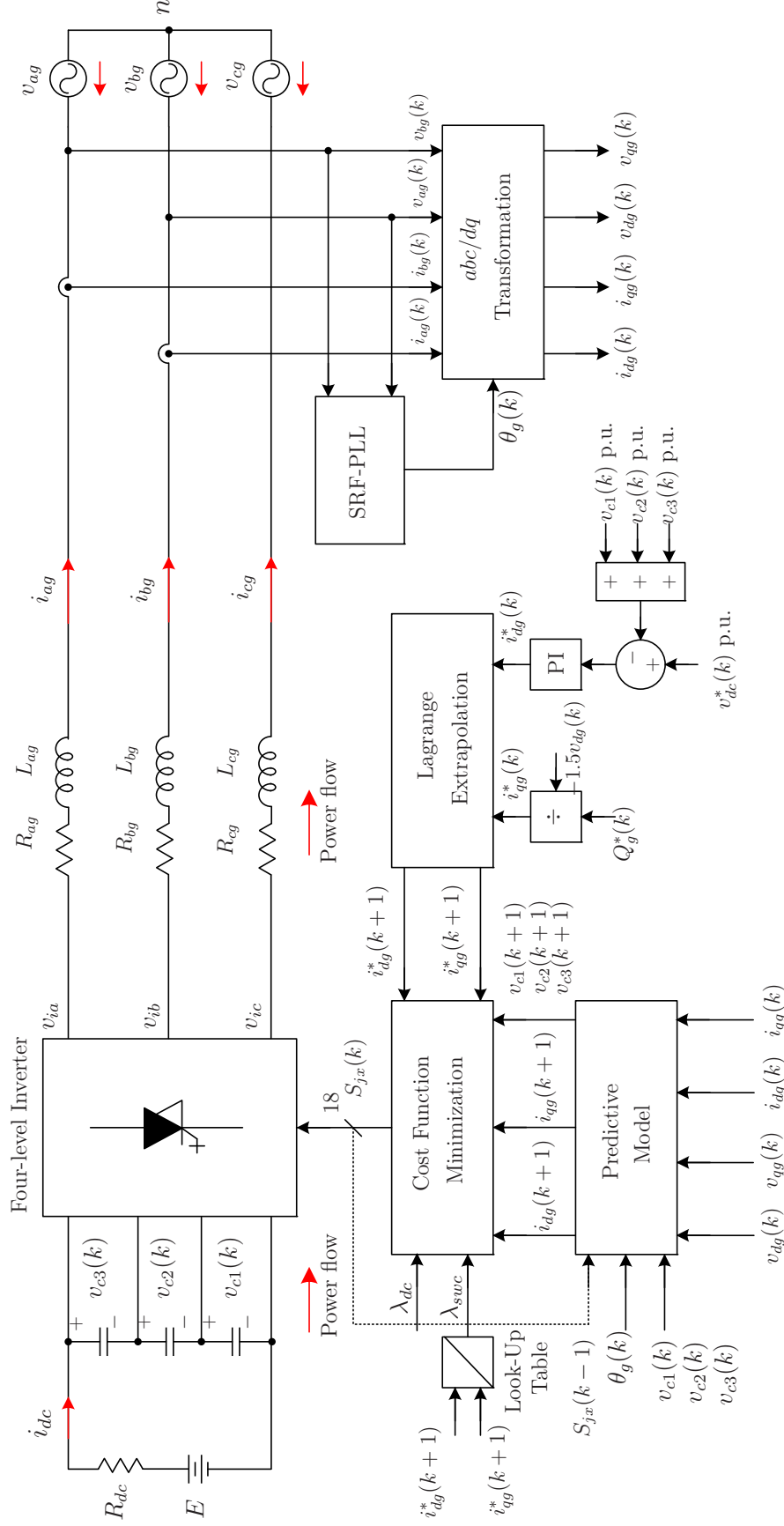


Figure 5.5: Proposed model predictive control algorithm for grid-tied four-level inverter.

- Predict the future behavior of the d and q -axis grid currents and dc-link capacitor voltages for all the possible switching states of the inverter using (5.10) and (5.12).
- Estimate λ_{swc} based on extrapolated reference currents $i_{dg}^*(k+1)$ and $i_{qg}^*(k+1)$.
- The predicted variables $i_{dg}(k+1)$, $i_{qg}(k+1)$, $v_{c1}(k+1)$, $v_{c2}(k+1)$, $v_{c3}(k+1)$, which are a function of switching signals, are used in the cost function. The gating signal $S_{jx}(k)$ ($j = 1, 2, 3$, $x = a, b, c$) which minimizes the cost function is chosen and applied to the inverter directly. It should be noted that any additional modulation stage is not required, unlike in the classical control techniques [2, 14, 69–71, 94, 292].

The control objectives of the proposed method are: (i) regulation of active power for which the d -axis current is controlled; (ii) regulation of reactive power for which q -axis current is controlled; (iii) balancing of dc-link capacitor voltages; and (iv) minimization of switching frequency for which the number of switch changes are penalized.

All these goals are included in a quadratic cost function for one-step prediction as follows:

$$\begin{aligned}
g_{grid}(k) = & (i_{dg}^*(k+1) - i_{dg}(k+1))^2 \\
& + (i_{qg}^*(k+1) - i_{qg}(k+1))^2 \\
& + \lambda_{dc} * [v_{c1}(k+1) - v_{c2}(k+1)]^2 \\
& + \lambda_{dc} * [v_{c2}(k+1) - v_{c3}(k+1)]^2 \\
& + \lambda_{dc} * [v_{c1}(k+1) - v_{c3}(k+1)]^2 \\
& + \lambda_{swc} * \sum_{x=a,b,c} swc_x
\end{aligned} \tag{5.18}$$

where λ_{dc} , and λ_{swc} are weighting factors for the dc-link capacitor voltages balancing and switching frequency reduction, respectively. The swc_x is the number of semiconductor commutations involved in phase- x , which can be calculated as follows [77]:

$$swc_x = |S_{jx}(k) - S_{jx,op}(k)|, \quad j = 1, 2, 3, \quad x = a, b, c \tag{5.19}$$

where $S_{jx}(k)$ is the predicted gating signal of phase- x , and $S_{jx,op}(k) = S_{jx}(k-1)$ is the optimal gating signal of phase- x in the previous sample. When $\lambda_{swc} > 0$, the switching frequency reduction can be achieved. In a similar manner, the dc-link capacitor voltages balancing can be accomplished with $\lambda_{dc} > 0$.

5.4 Simulation Results

To validate the proposed control scheme, simulations are carried out using Simulink software for different operating conditions with the parameters as indicated in Table 5.2. A one-step prediction horizon is considered in all the simulation tests. Unless otherwise stated, the cost function includes all four variables as mentioned in (5.18).

Table 5.2: Grid-tied four-level inverter and controller parameters

Variable	Description	Simulation		Experimental	
		SI	p.u.	SI	p.u.
S_g	Apparent Power (kVA)	4000	1.0	5	1.0
v_g	Grid L-L <i>rms</i> Voltage (V)	4000	—	208	—
i_g	Grid <i>rms</i> Current (A)	577.35	1.0	13.88	1.0
f_g	Grid Frequency (Hz)	60	1.0	60	1.0
R_g	Filter Resistance (Ω)	0.042	0.0105	0.091	0.0105
L_g	Filter Inductance (mH)	2.1	0.2	4.6	0.2
C_{dc}	DC-link Capacitance (μ F)	2596	3.914	1200	3.914
v_{dc}^*	Ref dc-bus Voltage (V)	7071	3.062	368.0	3.062
R_{dc}	DC-link Resistance (Ω)	0.4624	0.1156	1	0.1156
R_x	External Resistance (Ω)	46.24	11.56	100	11.56
λ_{dc}	Weight Factor	0.5	—	0.25	—
k_P, k_I	PI Parameters	1&200	—	1&200	—
T_s	Sampling Time (s)	90 μ	—	90 μ	—
Base Values					
v_{bg}	Base <i>rms</i> Voltage (V)	2309.4	1.0	120	1.0
i_{bg}	Base <i>rms</i> Current (A)	577.35	1.0	13.88	1.0
Z_{bg}	Base Impedance (Ω)	4.0	1.0	8.6528	1.0
L_{bg}	Base Inductance (mH)	10.6	1.0	23.0	1.0
C_{bg}	Base Capacitance (μ F)	663.15	1.0	306.56	1.0

Table 5.3: Summary of simulation steady-state analysis

Case	i_{dq}^* (p.u.)	Q_g^* (p.u.)	% e_{ig}	%THD	% e_{vc}	f_{sw} (Hz)
A1	1.0	0	3.26	3.20	1.02	798
A2	0.8	−0.6	3.68	3.88	1.41	799
A3	0.8	0.6	3.09	2.92	1.39	804
A4	0	0	—	—	0.03	798
A5	0	−1	2.18	2.07	0.96	804
A6	0	1	4.19	3.15	1.78	800

5.4.1 Steady-state Analysis

The steady-state analysis has been carried out for different d and q -axis reference currents as summarized in Table 5.3. The performance assessment parameters $\%e_{ig}$, $\%THD$, $\%e_{vc}$ and f_{sw} are calculated according to the guidelines given in Appendix C. The battery voltage E is adjusted as follows to obtain different d -axis reference currents:

$$E = v_{dc}^* + [i_{dg}^*(\text{p.u.}) \times i_{bg} \times R_{dc}]. \quad (5.20)$$

With the grid voltage orientation, the v_{dg} equals to the peak grid voltage and v_{qg} becomes zero during all operating conditions as shown in Fig. 5.6. The inverter phase voltage [refer to (5.5)] is also shown where it contains four levels: 0, $v_{dc}/3$, $2v_{dc}/3$ and v_{dc} . The operating condition A1 corresponds to the pure active power injection into the grid, which is the most common scenario in WECS [2]. The grid current is maintained in phase with the grid voltage as shown in Fig. 5.6(a)-(i). The active power component of the grid current, i_{dg} equals peak grid current and the reactive power component of grid current, i_{qg} becomes zero as demonstrated in Fig. 5.6(a)-(i). With $Q_g = 0$, the grid apparent power, S_g becomes equal to the grid active power, P_g as shown in Fig. 5.6(a)-(ii). The net dc-bus voltage, v_{dc} is maintained at its reference value with the perfect balancing of the capacitor voltages as shown in Fig. 5.6(a)-(iii). The dc-link capacitor voltage deviation can be further reduced by increasing the λ_{dc} , but at the expense of higher $\%e_{ig}$ and $\%THD$. With $\lambda_{swc} = 0$, the switching frequency is found to be 1338 Hz. By using $\lambda_{swc} = 1280$ (obtained from look-up table), the switching frequency, f_{sw} is reduced to 798 Hz. The reduced active power delivery with leading and lagging power factors are analyzed in Case A2 and A3, respectively. Case A4 corresponds to the operation of the WECS below the cut-in wind speed, where the active power generated and delivered to the grid is zero.

The fault ride-through capability of the proposed inverter is shown in Case A5. According to the grid codes [12,17], the high power WECS should remain connected to the grid during the grid faults and inject pure leading reactive power to help the grid recover from the fault [293]. The detection of grid fault and generation of corresponding current references [67] is beyond the scope of this paper. For simplicity, the current references are set by the user. The grid current leads the voltage by 90° as shown in Fig. 5.6(b)-(i). The i_{dg} becomes zero and the i_{qg} becomes equal to the peak grid current. The active power is maintained at zero as

shown in Fig. 5.6(b)-(ii), and the grid apparent power becomes equal to the absolute reactive power. The dc-link capacitor voltages are well-balanced, as shown in Fig. 5.6(b)(iii). This demonstrates the effectiveness of the proposed method to meet the grid codes. The injection of pure lagging reactive power, although rare in WECS, has been studied in A6. The inverter switching frequency f_{sw} variation is maintained in the range of 750-850 Hz during all the operating conditions while maintaining acceptable power quality and reference tracking.

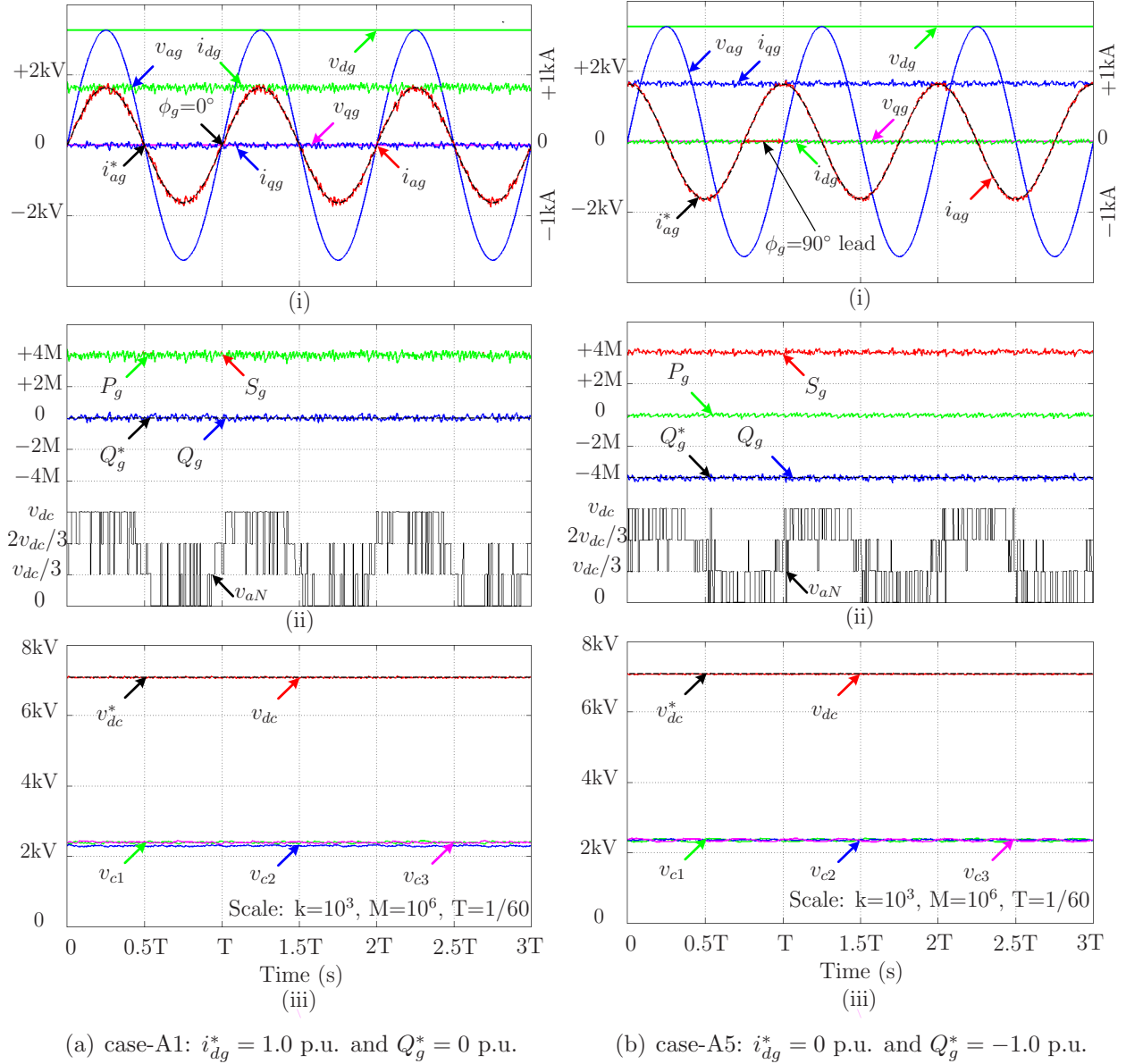


Figure 5.6: Simulation results during steady-state operation.

5.4.2 Transient Analysis

To analyze the decoupled nature of the d and q -axis currents, transient analysis has been carried out with trapezoidal changes in the Q_g^* . The d -axis reference current is set to 0.8 p.u. As shown in Fig. 5.7(a), the grid power factor changes in the order of: unity-leading-unity-lagging. The grid reactive power tracks to its reference within small interval and no overshoots. The decoupled control for active and reactive powers (thus for d and q -axis currents, respectively) has been achieved, as shown in 5.7(b). The net dc-bus voltage control and dc-link capacitor voltages balancing have been achieved as shown in 5.7(c).

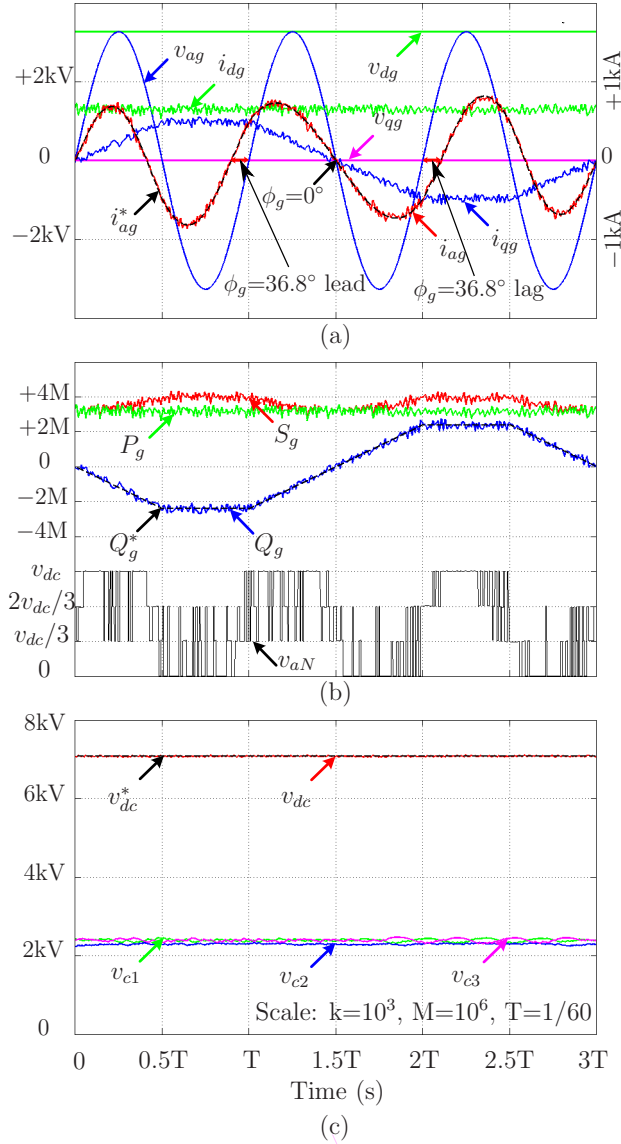


Figure 5.7: Simulation results during transient operation.

5.4.3 DC-link Dynamics

The dc-link dynamics are studied and presented in Fig. 5.8. In order to verify the proposed dc-link capacitor voltages balancing algorithm, an external resistor R_x (11.46 p.u.) is deliberately connected across the dc-link capacitor C_{dc3} at time $t = 1/60$ s. The d and q -axis current references are the same as in the Case A1. Even with the step-connection of the resistor, the controller takes action in a few sampling instants, and thus the capacitor voltages continue to be balanced as shown in Fig. 5.8(a). The current through the resistor, i_{Rx} is found to be 11.33 % of the base current. It is important to note that the grid currents continue to track to their references during this process.

As shown in Fig. 5.8(b), another test has been conducted where the weighting factor λ_{dc} is suddenly changed from 0.5 to zero at $t = 0.2$ s. With no penalty to the dc-link capacitor voltages balancing, the v_{c1} and v_{c3} gradually increases and v_{c2} gradually decreases and becomes zero at $t = 0.24$ s. At the time $t = 0.5$ s, the weighting factor has been changed to 0.5 and the dc-link capacitor voltages become balanced, with an acceptable recovery time of 0.06 s. These results validate the proposed dc-link modeling and control.

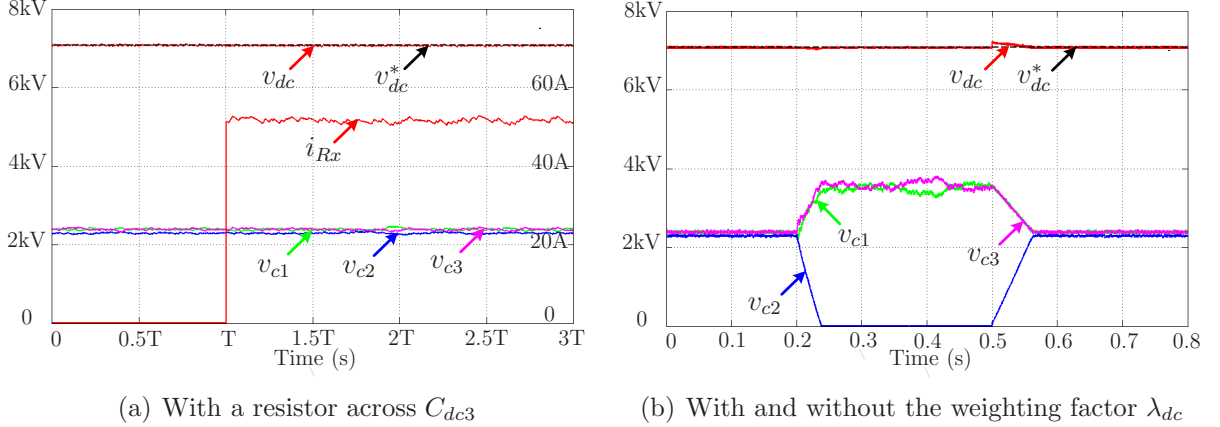


Figure 5.8: Simulation analysis for dc-link capacitor voltages balancing.

5.4.4 Switching Frequency Regulation

The variable switching frequency nature of the predictive control is studied with respect to the i_{dg}^* and Q_g^* , and presented in Fig. 5.9. The switching frequency increases linearly with the d -axis grid current. The f_{sw} becomes greater with the negative reactive power compared to the positive reactive power. Without the weight factor λ_{swc} , the switching frequency is found to vary in a range of 1800-900 Hz as shown in Fig. 5.9(a). To overcome this issue, weighting factors are designed as shown in Fig. 5.9(c). The knowledge for the design has been obtained from the Fig. 5.9(a) and guidelines given in [247]. Observation demonstrates that these values hold a linear relation to the active and reactive powers. These values are stored in a lookup table, for online use, and as a result the switching frequency has been maintained within the 750-850 Hz range, during all the operating conditions, as shown in Fig. 5.9(b). It should be noted that the previously discussed steady-state results are obtained by including this online look-up table, and thus the switching frequency is maintained in the range of 750-850 Hz during all operating conditions as summarized in Table 5.3.

The %THD performance of a four-level inverter with respect to the switching frequency for the proposed grid-tied and resistive load [281] cases are investigated and presented in Fig. 5.10. The case-A1 is considered for grid-tied application. For a resistive load, the controller is implemented in a stationary reference frame ($\alpha\beta$) with the parameters as provided in Table 5.2. The load resistance value is set as a base impedance (Z_{bg}) of the system. For the grid-tied case, the weighting factor λ_{swc} is changed from 0-20000 and the switching frequency is reduced from 1338 to 105 Hz and the THD is increased from 2.27 % to 14 %. For the resistive load case, the λ_{swc} is changed from 0-10000. The f_{sw} is reduced from 1333 to 102 Hz with the increase in THD from 2.18 % to 14 %. The difference between both cases is found to be small during the entire switching frequency range. It should be noted, for both the cases, that a significant reduction in switching frequency from 1330 to 600 Hz has been achieved, with a slight increase in THD from 2.2 % to 4.1 %.

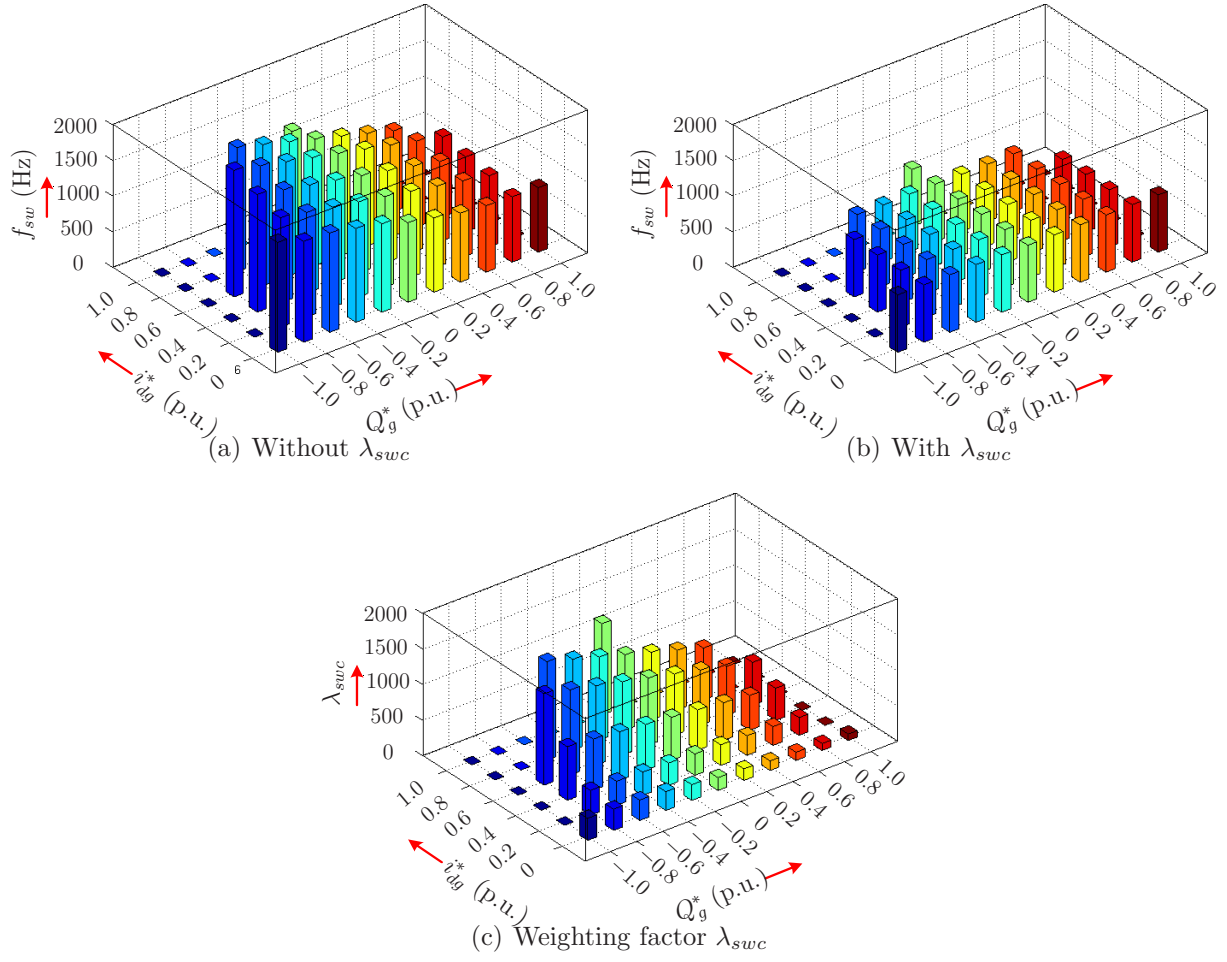


Figure 5.9: Simulation results for switching frequency variation with respect to i_{dg}^* and Q_g^* .

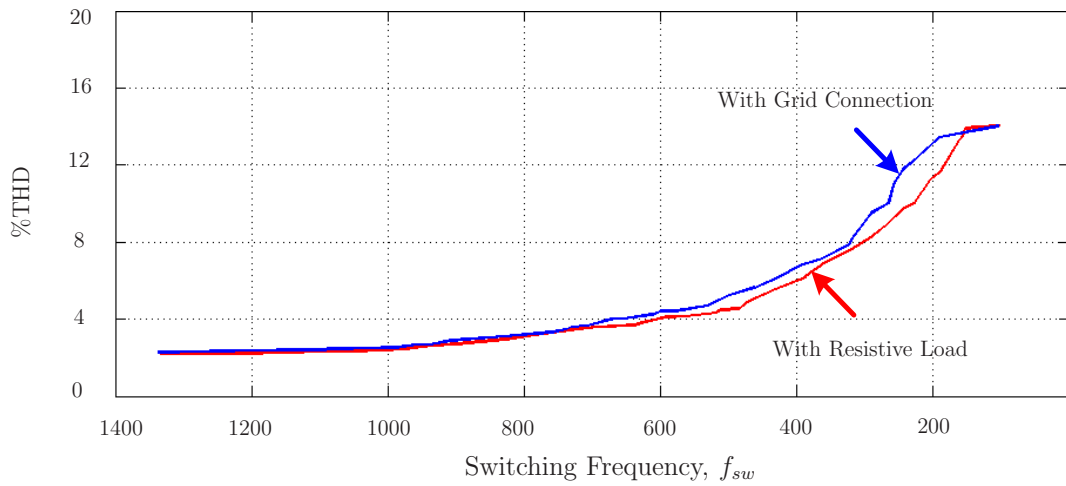


Figure 5.10: Comparison of %THD for 4L-inverter with grid-tied and resistive load cases.

5.5 Experimental Implementation and Validation

5.5.1 Experimental Setup

The experimental setup for the grid-tied four-level inverter is shown in Fig. 5.11 with the parameters as indicated in Table 5.2. The control algorithm has been implemented using a host PC running with MATLAB-Simulink 2006a software through Real-Time Interface (RTI). The dSPACE DS1103 controller is used to handle the control processes such as grid current prediction, dc-link capacitor voltages balancing and cost function minimization. The grid currents and dc-link voltages are measured by LEM LA55-P and LV25-P transducers, respectively. Feedback from the sensors has been sent to the controller through the CP1103 I/O connector. The prototype has been built by Semikron SKM75GB123D dual-pack IGBT modules. The IGBT gate drivers are based on four SKHI22B dual cores which are powered with a 0/15 V supply. An interface board with MC14504BCP and TLP521-4 is used between the dSPACE and SKHI22B gate drivers for TTL to CMOS logic conversion and signal isolation, respectively. The dc power supply (E) has been obtained by Xantrex XDC-600-20. The inverter is connected to the grid through an isolation transformer and its impedance is added to the filter values.

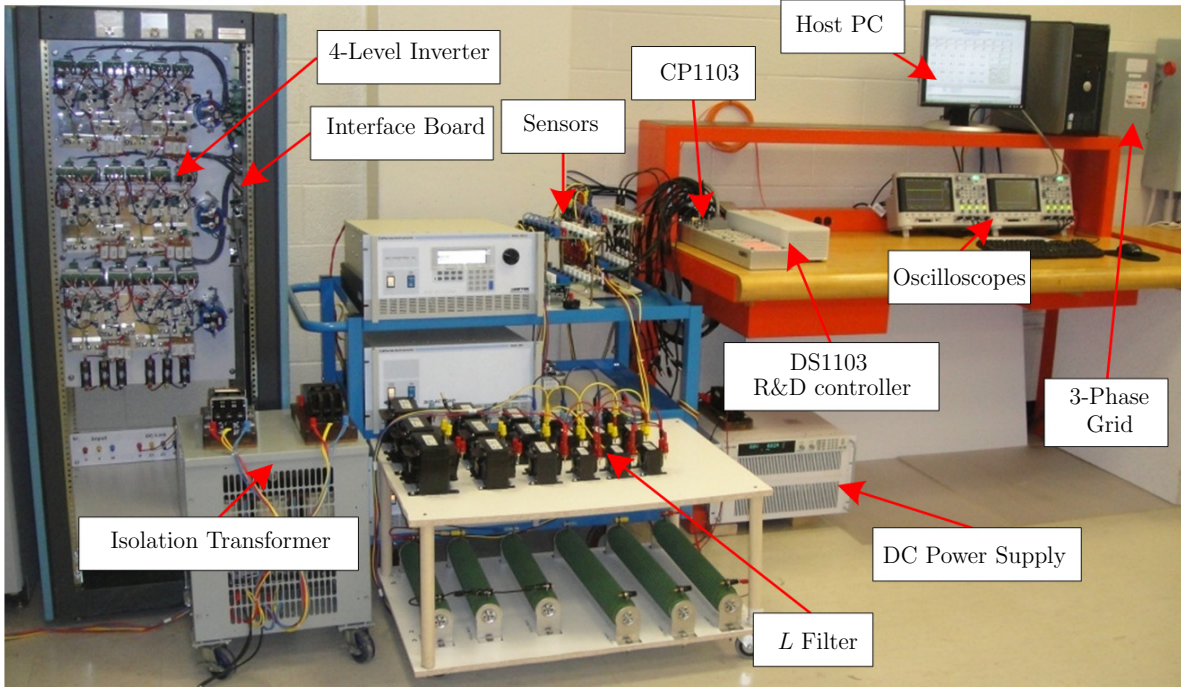


Figure 5.11: Photograph of experimental setup.

5.5.2 Delay Compensation

To verify the predictive control algorithm through MATLAB simulations [281], one-step prediction can be used as shown in Fig. 5.12(a). This is ideal case where the delay is zero between the instant measurements are made and the instant new switching state is applied [77]. The switching state which minimizes the error at $(k+1)$ instant is selected and applied at (k) instant. In the experimental verification, the delay provided by the digital signal processor, gate drivers, and switching devices is inevitable. The computational delay provided by the digital signal processor is most significant, and this must be compensated for. This delay can easily be compensated for by calculating the cost function with a modified one-step prediction [248,249] as shown in Fig. 5.12(b). The optimal switching state from the previous iteration is used to “estimate” the variables at $(k+1)$ instant and all the possible switching states are used to “predict” the variables at $(k+2)$ instant. The switching state which minimizes the error at the $(k+2)$ instant is selected and applied at sampling instant $(k+1)$. With this approach, one sampling period will be available for calculations.

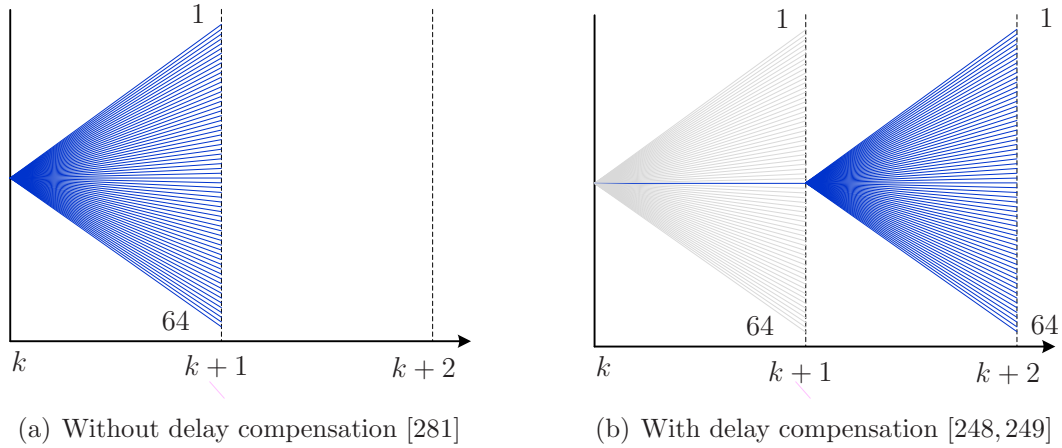


Figure 5.12: Prediction of four-level inverter control variables.

The control algorithm with this approach of control delay compensation is shown in Fig. 5.13. The measured grid and dc-link signals, along with the optimal gating signals, are used by the predictive controller. The variables at $(k+1)$ instant are estimated using the optimal values obtained from the previous iteration. This is demonstrated as follows:

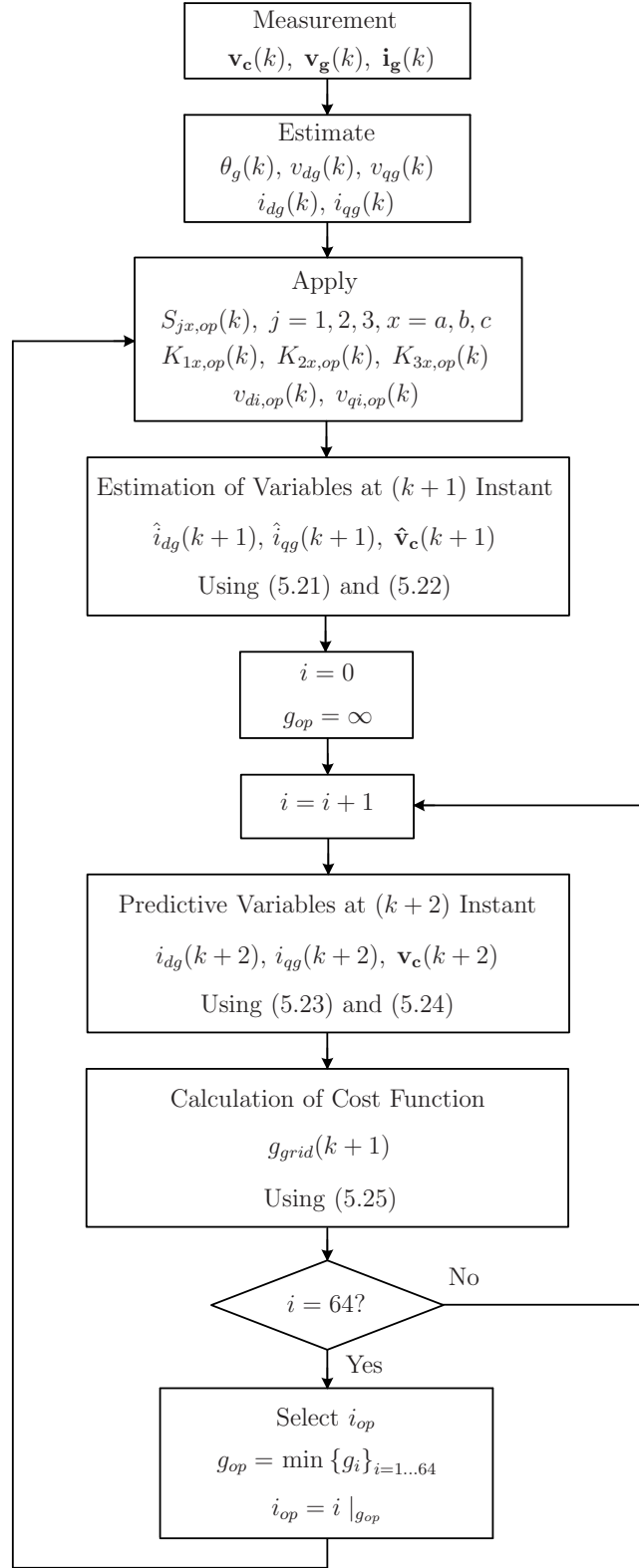


Figure 5.13: Predictive current control and dc-link capacitor voltages balancing algorithm with delay compensation.

$$\begin{bmatrix} \hat{i}_{dg}(k+1) \\ \hat{i}_{qg}(k+1) \end{bmatrix} = \Phi \begin{bmatrix} i_{dg}(k) \\ i_{qg}(k) \end{bmatrix} + \Gamma_i \begin{bmatrix} v_{di,op}(k) \\ v_{qi,op}(k) \end{bmatrix} + \Gamma_g \begin{bmatrix} v_{dg}(k) \\ v_{qg}(k) \end{bmatrix} \quad (5.21)$$

$$\hat{v}_{cj}(k+1) = v_{cj}(k) + \frac{T_s}{C_{dcj}} \sum_{x=a,b,c} K_{jx,op} i_{xg}. \quad (5.22)$$

The algorithm is initialized by setting the switching state number i to 0 and optimal g value to ∞ . The algorithm then enters the loop. The predictive variables at $(k+2)$ instant are calculated as follows:

$$\begin{bmatrix} i_{dg}(k+2) \\ i_{qg}(k+2) \end{bmatrix} = \Phi \begin{bmatrix} \hat{i}_{dg}(k+1) \\ \hat{i}_{qg}(k+1) \end{bmatrix} + \Gamma_i \begin{bmatrix} v_{di}(k+1) \\ v_{qi}(k+1) \end{bmatrix} + \Gamma_g \begin{bmatrix} v_{dg}(k+1) \\ v_{qg}(k+1) \end{bmatrix} \quad (5.23)$$

$$v_{cj}(k+2) = \hat{v}_{cj}(k+1) + \frac{T_s}{C_{dcj}} \sum_{x=a,b,c} K_{jx} i_{xg}. \quad (5.24)$$

In (5.23), $v_{dg}(k+1)$ and $v_{qg}(k+1)$ are extrapolated grid voltages and they can be obtained similar to (5.17). For stiff-grid, $v_{dg}(k) = v_{dg}(k+1)$ and $v_{qg}(k) = v_{qg}(k+1)$ and thus no extrapolation is needed. The predicted variables at $(k+2)$ instant are evaluated 64 times by a cost function $g_{grid}(k+1)$. The switching state, which produces a minimal value of g_{op} , is chosen and applied to the inverter directly. The cost function $g_{grid}(k+1)$ can be calculated by shifting the variable in (5.19) one-step forward as follows:

$$\begin{aligned} g_{grid}(k+1) = & (i_{dg}^*(k+2) - i_{dg}(k+2))^2 \\ & + (i_{qg}^*(k+2) - i_{qg}(k+2))^2 \\ & + \lambda_{dc} * [v_{c1}(k+2) - v_{c2}(k+2)]^2 \\ & + \lambda_{dc} * [v_{c2}(k+2) - v_{c3}(k+2)]^2 \\ & + \lambda_{dc} * [v_{c1}(k+2) - v_{c3}(k+2)]^2 \\ & + \lambda_{swc} * \sum_{x=a,b,c} swc_x. \end{aligned} \quad (5.25)$$

The reference currents at $(k+2)$ instant can be obtained by the Lagrange extrapolation as follows [259]:

$$\begin{aligned} i_{dg}^*(k+2) = & 10 i_{dg}^*(k) - 20 i_{dg}^*(k-1) + 15 i_{dg}^*(k-2) - 4 i_{dg}^*(k-3) \\ i_{qg}^*(k+2) = & 10 i_{qg}^*(k) - 20 i_{qg}^*(k-1) + 15 i_{qg}^*(k-2) - 4 i_{qg}^*(k-3). \end{aligned} \quad (5.26)$$

5.5.3 Selection of Sampling Time

For a four-level inverter, 64 switching states are available and the proposed predictive control method incurs a large number of calculations to predict the future behavior of grid currents and dc-link capacitor voltages. The execution times for a two-level inverter with 8 switching states [262] and three-level inverter with 27 switching states [279] are reported as $7\mu s$ and $52\mu s$, respectively. The minimum execution time of $63\mu s$ is achieved for the proposed control system. It is observed that the predictive control algorithm as shown in Fig. 5.13 took $31\mu s$ only. The tasks such as measurement of signals, grid voltage orientation, detection of grid voltage angle, online estimation of weighting factors, calculation of reference currents, and online performance assessment took $32\mu s$. The authors in [294] suggested that the weighting factor-based switching frequency reduction is more efficient compared to the selection of higher sampling times. With this recommendation, and considering a high power application, the sampling time (T_s) of $90\mu s$ or 11.11 kHz sampling frequency is selected.

5.5.4 Experimental Results

The experimental results are obtained with the modified one-step prediction [Fig. 5.12(b)]. Since the predictive controller uses the SI parameters, the weighting factors used in the experiments are different from the simulations, but their impact on the controller remains the same. The steady-state analysis has been carried out similar to the simulations and summarized in Table. 5.4.

Table 5.4: Summary of experimental steady-state analysis

Case	i_{dg}^* (p.u.)	Q_g^* (p.u.)	$\%e_{ig}$	$\%THD$	$\%e_{vc}$	f_{sw} (Hz)
A1	1.0	0	4.83	4.16	0.58	804
A2	0.8	-0.6	4.55	4.41	0.71	796
A3	0.8	0.6	3.76	3.74	0.59	811
A4	0	0	—	—	0.13	800
A5	0	-1	3.35	3.58	0.29	808
A6	0	1	4.97	4.03	0.79	807

Due to the modified one-step prediction, the number of calculations are increased, and as a result, the switching frequency is increased in all the cases [248]. For instance, for Case A1 with $\lambda_{swc} = 0$, the f_{sw} through simulation studies is 1338 Hz and in the experimental

implementation it is found to be 1736 Hz. By using $\lambda_{swc} = 1.9$ (obtained through the look-up table) in experiments, the switching frequency is reduced to 804 Hz. The higher current tracking error in experiments can be attributed to the delay provided by the sensors and IGBT gate drivers and losses in the system. The experimental results presented in Figs. 5.14(a), 5.14(b), and 5.15 are similar to the simulation results with the perfect regulation of the dc-link voltages and grid currents.

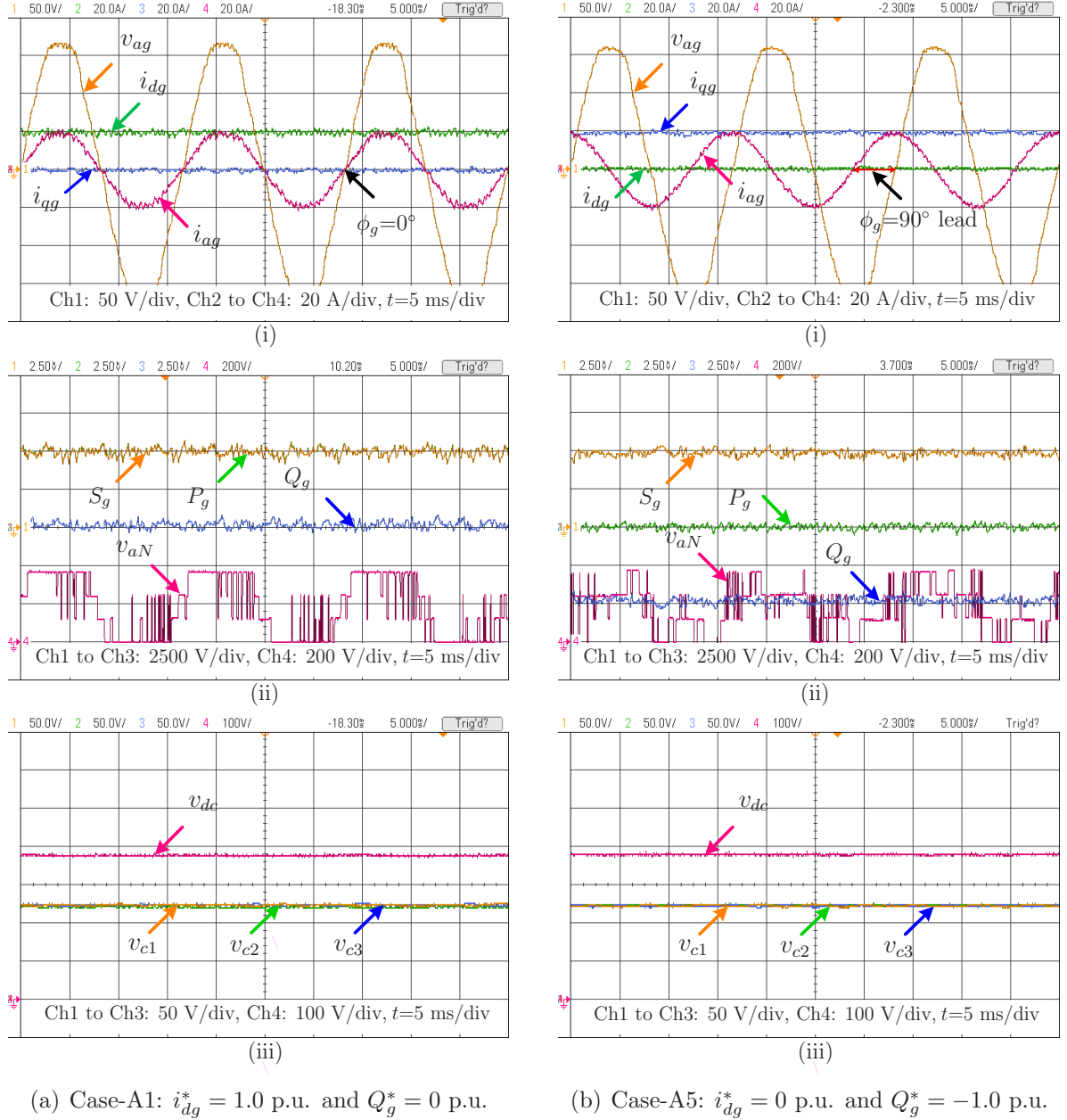


Figure 5.14: Experimental results during steady-state operation.

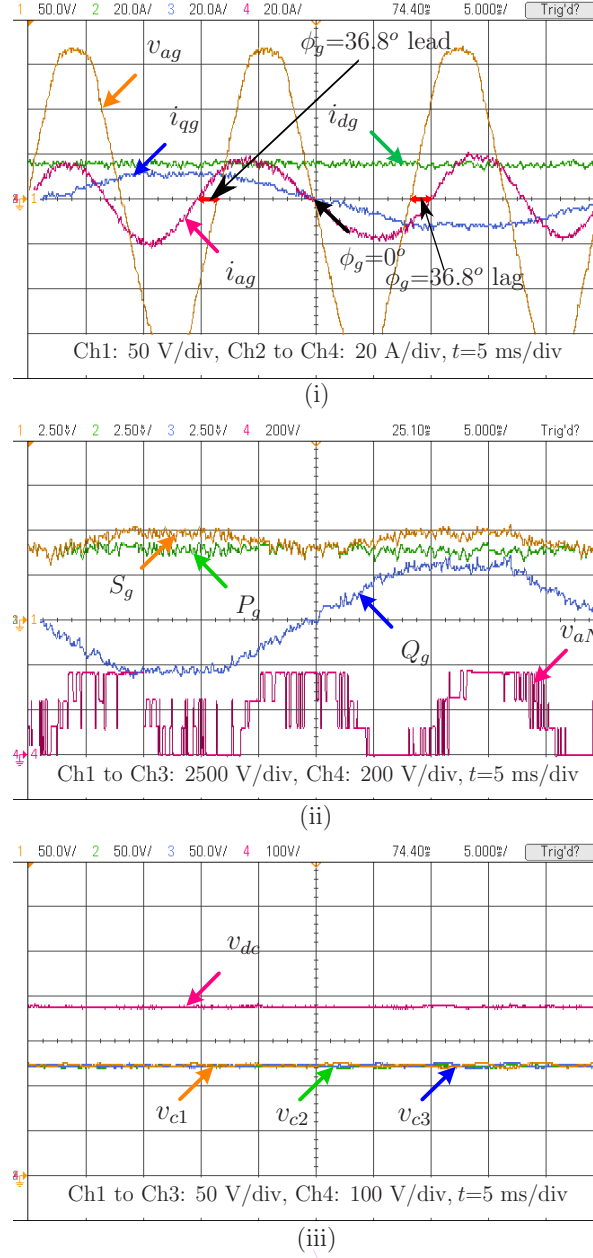


Figure 5.15: Experimental results during transient operation.

The dc-link dynamics, with the external resistor R_x across C_{dc1} , is shown in Fig. 5.16(a). Similar to the simulations, the balancing of the dc-link capacitor voltages have been maintained even with the step-connection of the resistor. During the step change, transients can be noticed by looking into the current waveform i_{Rx} . The dc-link voltage drops slightly and recovers back to normal within 1 ms. Similar to the simulations, the current i_{Rx} is found to be 11.33 % of the base current.

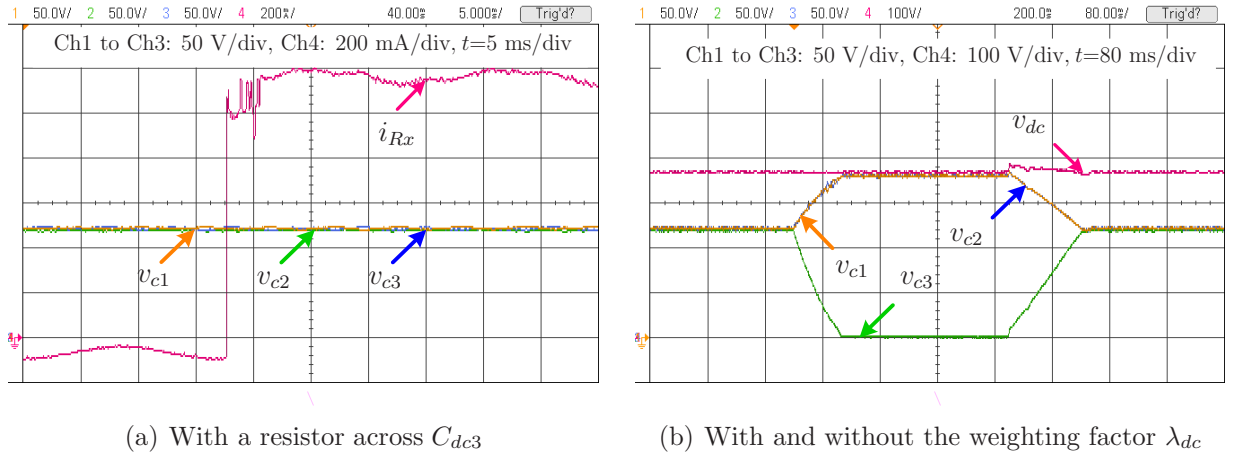


Figure 5.16: Experimental results for dc-link capacitor voltages balancing.

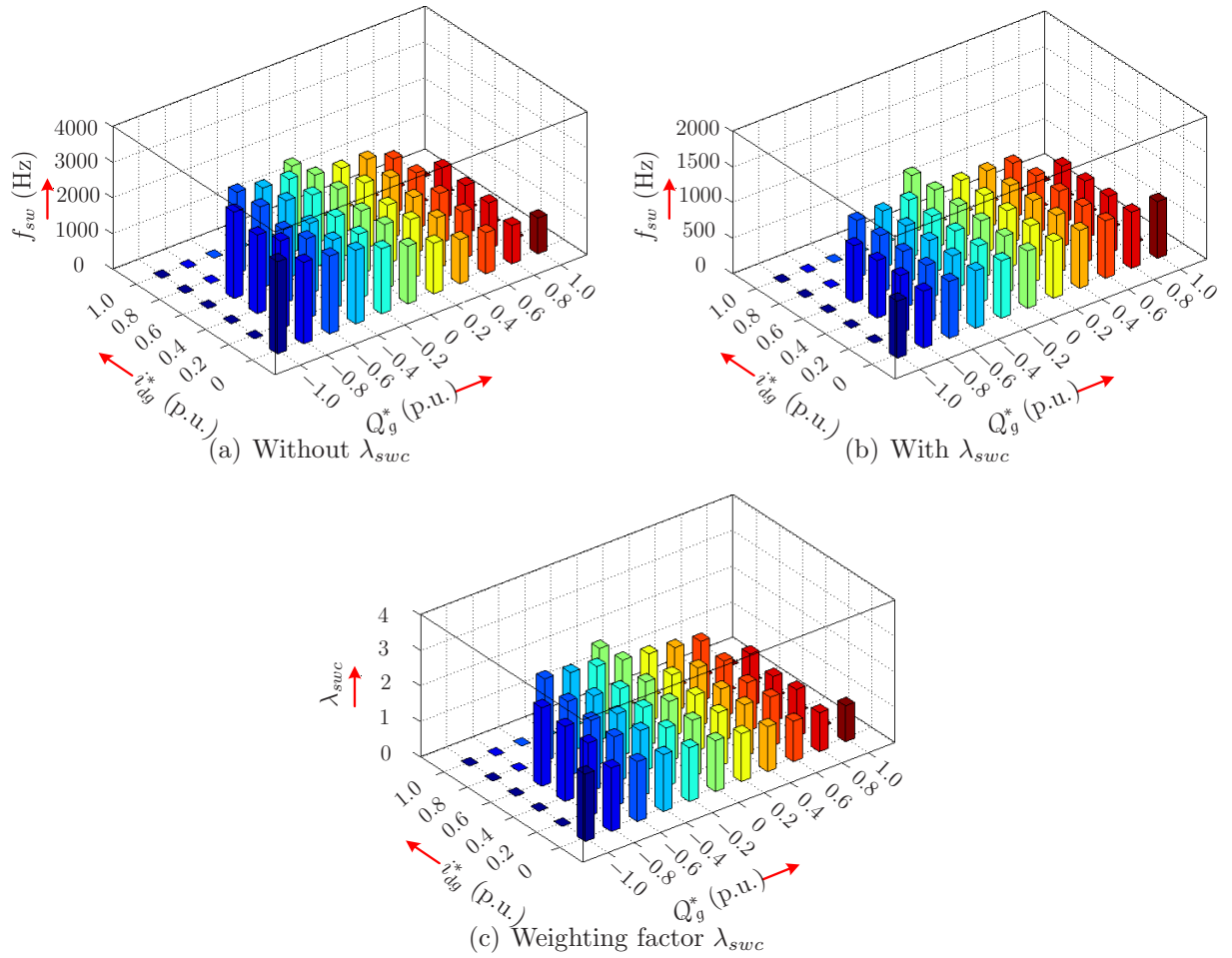


Figure 5.17: Experimental results for switching frequency variation with respect to i_{dg}^* and Q_g^* .

The relation between the λ_{dc} and the capacitors balancing have been verified experimentally and presented in Fig. 5.16(b). The divergence and convergence of capacitor voltages are similar to the simulation results. The settling time of capacitor voltages is found to be the same as those of the simulations.

The switching frequency variation with respect to the i_{dg}^* and Q_g^* is presented in Fig. 5.17(a) and it is noticed to vary in the range of 1000-2580 Hz. To deal with the lower power prototype, a scaling has been done to evaluate the weighting factor λ_{swc} as presented in Fig. 5.17(c). Similar to the simulations, the switching frequency is maintained in the range of 750-850 Hz as shown in Fig. 5.17(b).

5.6 Conclusion

In this chapter, a voltage-oriented FCS-MPC strategy is proposed for the grid-tied 4L-inverter for use in high power WECS. The proposed methodology can be simply extended for any level grid-tied inverter. The future behavior of the control variables for each of the 64 possible switching states has been predicted. The switching state which minimizes the cost function is selected and then applied directly to the inverter gating terminals. The simulation and experimental results are in a close relationship and thus validate the proposed methodology. The major contributions of this work are summarized as follows:

- The d and q -axis grid currents are tightly regulated during different active and reactive power conditions using an intuitive approach. The internal current PI controllers and modulation stage are eliminated and as a result, a good dynamic response has been achieved.
- An intuitive modeling and control for the dc-link capacitor voltages balancing is presented and verified.
- A lookup table based weighting factor design is proposed by which the switching frequency is regulated between 750 and 850 Hz during different active and reactive power references, and this has been achieved without any software or hardware reconfiguration.

Chapter 6

Model Predictive Decoupled Active and Reactive Power Control for Grid-Tied Diode-Clamped Inverters

In the Chapter 5, the predictive current control of grid-tied diode-clamped inverters (DCIs) was presented. In this chapter, another approach is proposed to directly control the grid active and reactive powers, assuming that the generator-side converter regulates the net dc-bus voltage. A 4L-DCI is considered to present the analysis and results, and the proposed concept can easily be extended to any-level DCI using the guidelines given in Chapter 4. To predict the future behavior of active and reactive grid powers, dc-link capacitor voltages, and number of switch changes, a discrete-time model of the inverter is developed in synchronous reference frame (SRF). The controller uses all the possible switching states of the inverter for the prediction and evaluates them using a cost function.

During a step change in reference control variables, the vector angle extrapolation method [261] exhibits better performance than the Lagrange extrapolation method [221]. However it is not suitable for the SRF references. In this chapter, a novel extrapolation method is presented to deal with the extrapolation of SRF references. This method is analyzed during step-changes in grid active and reactive power references. The performance of the proposed method is investigated with the perturbations in the grid-side filter and dc-link parameters. The feasibility of the proposed method is verified through simulation and experimental results showing good dynamic and steady-state performance.

6.1 Proposed Control Strategy

The proposed model predictive decoupled active and reactive power control scheme is shown in Fig. 6.1. The wind turbine, generator, and rectifier with the net dc-bus voltage control are represented by a constant dc-voltage source (battery). A diode is inserted between the battery and dc-link to perform isolation and unidirectional power flow. In commercial wind turbines, there is no need to incorporate the diode in the circuit. The top capacitor voltage corresponds to v_{c1} which is a different notation from the works presented in the Chapters 4 and 5. The reference reactive power command (Q_g^*) is provided by the grid operator, and the active power reference (P_g^*) is obtained by the maximum power point tracking (MPPT) algorithm. In commercial wind turbines, the MPPT is performed using the wind turbine characteristics and measured (using Anemometer) wind speed.

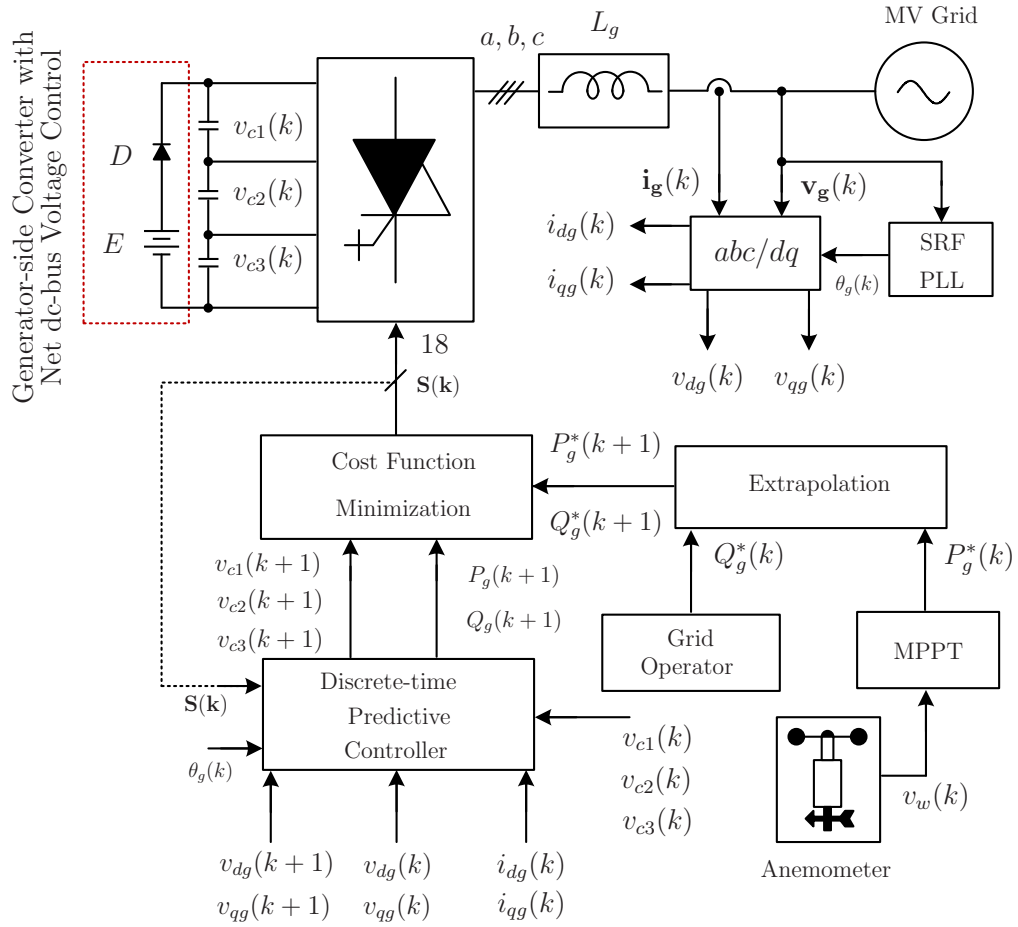


Figure 6.1: Proposed decoupled active and reactive power control with dc-link capacitor voltages balancing for a grid-tied 4L-DCI.

To simplify the analysis, the per-unit (p.u.) P_g^* is considered to be a cubic of per-unit wind speed [2]:

$$\text{p.u. } P_g^*(k) \propto \text{p.u. } v_w^3(k). \quad (6.1)$$

From the continuous time models given for the grid active and reactive powers in eq.(5.3), the discrete-time models can be derived for a one-step horizon time $(k+1)$ as demonstrated below:

$$\begin{aligned} P_g(k+1) &= \frac{3}{2}[v_{dg}(k+1) i_{dg}(k+1)] \\ Q_g(k+1) &= \frac{3}{2}[v_{dg}(k+1) i_{qg}(k+1)] \end{aligned} \quad (6.2)$$

where $v_{dg}(k+1)$ and $v_{qg}(k+1)$ are the extrapolated grid voltages. For a stiff grid, $v_{dg}(k+1) = v_{dg}(k)$ and $v_{qg}(k+1) = v_{qg}(k)$, and thus no extrapolation is needed. For weak grids the fourth-order Lagrange extrapolation method given in eq.(5.17) can be used. $i_{dg}(k+1)$ and $i_{qg}(k+1)$ are the predicted dq -axis grid currents:

$$\begin{bmatrix} i_{dg}(k+1) \\ i_{qg}(k+1) \end{bmatrix} = \mathbf{\Phi} \begin{bmatrix} i_{dg}(k) \\ i_{qg}(k) \end{bmatrix} + \mathbf{\Gamma}_i \begin{bmatrix} v_{di}(k+1) \\ v_{qi}(k+1) \end{bmatrix} + \mathbf{\Gamma}_g \begin{bmatrix} v_{dg}(k) \\ v_{qg}(k) \end{bmatrix} \quad (6.3)$$

where $v_{di}(k+1)$ and $v_{qi}(k+1)$ are the predicted inverter voltages in $(k+1)$ state using the 64 possible switching states. The $\mathbf{\Phi}$, $\mathbf{\Gamma}_i$ and $\mathbf{\Gamma}_g$ are discrete-time parameter matrices which can be computed off-line as given in (5.11). The calculation of three-phase inverter voltages is presented below for the capacitor voltages notation used in this work:

$$\begin{aligned} v_{aN} &= v_{c1}S_{1a} + v_{c2}S_{2a} + v_{c3}S_{3a} \\ v_{bN} &= v_{c1}S_{1b} + v_{c2}S_{2b} + v_{c3}S_{3b} \\ v_{cN} &= v_{c1}S_{1c} + v_{c2}S_{2c} + v_{c3}S_{3c}. \end{aligned} \quad (6.4)$$

The above natural frame (abc) inverter voltages can be converted to synchronous frame (dq) using the transformation matrix given in Appendix B.2.

The discrete-time model for dc-link voltages is given as follows:

$$\begin{aligned} v_{c1}(k+1) &= v_{c1}(k) + \frac{T_s}{C_{dc1}} i_{c1}(k+1) \\ v_{c2}(k+1) &= v_{c2}(k) + \frac{T_s}{C_{dc2}} i_{c2}(k+1) \\ v_{c3}(k+1) &= v_{c3}(k) + \frac{T_s}{C_{dc3}} i_{c3}(k+1) \end{aligned} \quad (6.5)$$

where $i_{c1}(k+1)$, $i_{c2}(k+1)$, and $i_{c3}(k+1)$ are predicted dc-link currents which can be calculated as follows:

$$\begin{aligned} i_{c1} &= K_{1d} i_{dg} + K_{1q} i_{qg} \\ i_{c2} &= K_{2d} i_{dg} + K_{2q} i_{qg} \\ i_{c3} &= K_{3d} i_{dg} + K_{3q} i_{qg} \end{aligned} \tag{6.6}$$

where K_{1d} , K_{1q} , K_{2d} , K_{2q} , K_{3d} , and K_{3q} are variables in SRF and they can be obtained from natural frame gains and grid voltage angle, θ_g . It should be noted that the capacitor currents are mean values. The natural frame gains can be expressed in terms of switching states as follows:

$$\begin{aligned} K_{1x} &= \text{sgn}(3 - S_x) \\ K_{2x} &= \text{sgn}(2 - S_x) \\ K_{3x} &= \text{sgn}(1 - S_x) \end{aligned} \tag{6.7}$$

where $x = a, b, c$. K_{1x} , K_{2x} , $K_{3x} \in \{-1, 0, 1\}$ and sgn is a Signum function. The modeling of dc-link voltages in SRF gives flexibility in digital implementation. This will be further discussed in Section 6.3.

The control objectives, such as regulation of active and reactive powers, dc-link capacitor voltages balancing and switching frequency minimization are included in a cost function as follows:

$$\begin{aligned} g_{grid}(k+1) &= ||P_g^*(k+1) - P_g^p(k+1)|| \\ &+ ||Q_g^*(k+1) - Q_g^p(k+1)|| \\ &+ \lambda_{dc} * ([v_{c1}^p(k+1) - v_{c2}^p(k+1)]^2 \\ &\quad + [v_{c2}^p(k+1) - v_{c3}^p(k+1)]^2 \\ &\quad + [v_{c3}^p(k+1) - v_{c1}^p(k+1)]^2) \\ &+ \lambda_{swc} * (swc_a + swc_b + swc_c) \end{aligned} \tag{6.8}$$

where λ_{dc} and λ_{swc} are weighting factors for the capacitor voltages balancing and switching frequency reduction, respectively. The swc_x is the number of semiconductor commutations involved in phase- x , which can be calculated as given in Table. 4.4.

The cost function requires reference powers in the $(k+1)$ state. When the sampling time T_s is sufficiently small ($< 20 \mu s$), no extrapolation is required. In this work, a sampling time of $100 \mu s$ is used to deal with the 64 switching states. At this higher sampling time, the

reference powers should be extrapolated to the $(k + 1)$ state for high performance control. During the steady-state operation, no extrapolation is required, as the reference powers are dc quantities. In practical WECS, the wind speed, and thus the active power reference, changes dynamically and as a result an extrapolation method should be used.

The Lagrange extrapolation [221, 257] can be used. However, this method produces unnecessary spikes during the step changes [77]. The vector angle extrapolation [261] method overcomes this issue [77]. But this method is based on real and imaginary (stationary frame, α, β) quantities. To use vector angle extrapolation to manage active and reactive powers, the following procedure should be used:

- Estimate $i_{dg}^*(k)$ and $i_{qg}^*(k)$ from $P_g^*(k)$ and $Q_g^*(k)$ using (5.3)
- Estimate $i_{\alpha g}^*(k)$ and $i_{\beta g}^*(k)$ from $i_{dg}^*(k)$ and $i_{qg}^*(k)$
- Extrapolate $i_{\alpha g}^*(k)$ and $i_{\beta g}^*(k)$ to $i_{\alpha g}^*(k + 1)$ and $i_{\beta g}^*(k + 1)$ using vector angle method
- Estimate $i_{dg}^*(k + 1)$ and $i_{qg}^*(k + 1)$ from $i_{\alpha g}^*(k + 1)$ and $i_{\beta g}^*(k + 1)$, and
- Estimate $P_g^*(k + 1)$ and $Q_g^*(k + 1)$ from $i_{dg}^*(k + 1)$ and $i_{qg}^*(k + 1)$ using (5.3)

As shown in the above example, this is a complex approach and increases the computational burden. To overcome this issue, a simplified extrapolation method is proposed. Since the reference active and reactive powers are of dc quantities, they can be simply extrapolated to the $(k + 1)$ state as follows:

$$\begin{aligned} P_g^*(k + 1) &= P_g^*(k - 1) \\ Q_g^*(k + 1) &= Q_g^*(k - 1) \end{aligned} \tag{6.9}$$

Comparing the proposed approach with the Lagrange extrapolation given in (5.17), this uses only one a past value, which can be simply implemented using the “Variable Time Delay” block in the MATLAB/Simulink environment. This approach gives the same result as the vector angle extrapolation, but with a lower computational burden, especially in SRF.

6.2 Simulation Results

To validate the proposed control scheme, simulations are carried out using MATLAB/-Simulink software with the parameters as indicated in Table 6.1. The dc-link diode (D) is assumed to be ideal with the zero forward voltage drop. Unless otherwise stated, the cost function includes all four variables as mentioned in (6.8).

Table 6.1: Grid-tied four-level inverter parameters

Variable	Description	Simulation		Experimental	
		SI	p.u.	SI	p.u.
S_g	Apparent Power (kVA)	4000	1.0	5	1.0
v_g	Grid L-L <i>rms</i> Voltage (V)	4000	–	208	–
i_g	Grid <i>rms</i> Current (A)	577.35	1.0	13.88	1.0
f_g	Grid Frequency (Hz)	60	1.0	60	1.0
R_g	Filter Resistance (Ω)	0.042	0.0105	0.091	0.0105
L_g	Filter Inductance (mH)	2.1	0.2	4.6	0.2
C_{dc}	DC-link Capacitance (μ F)	10200	15.33	4700	15.33
v_{dc}^*	Ref dc-link Voltage (V)	7071	3.062	367	3.062
E	Battery Voltage (V)	7071	3.062	373	3.108
R_x	External Resistance (Ω)	46.24	11.56	100	11.56
C_x	External Capacitance (μ F)	10200	15.33	4700	15.33
λ_{dc}	Weight Factor	500	–	150	–
λ_{swc}	Weight Factor	30000	–	5	–
T_s	Sampling Time (s)	100 μ	–	100 μ	–
Base Values					
v_{bg}	Base <i>rms</i> Voltage (V)	2309.4	1.0	120	1.0
Z_{bg}	Base Impedance (Ω)	4.0	1.0	8.6528	1.0
L_{bg}	Base Inductance (mH)	10.6	1.0	23.0	1.0
C_{bg}	Base Capacitance (μ F)	663.15	1.0	306.56	1.0

6.2.1 Transient Analysis

The simulation results with different active and reactive power references are shown in Fig. 6.2. The wind speed (v_w) profile is shown in Fig. 6.2(a), and it increases linearly from a cut-in wind speed of 3 m/s (0.25 p.u.) and reaches the rated value of 12 m/s (1 p.u.) at $t = 0.6$ s. A step change in wind speed from 12 to 10.12 m/s (0.8434 p.u.) is applied at $t = 0.8$ s.

The reference active power P_g^* and measured active power P_g are shown in Fig. 6.2(b). The P_g^* is proportional to the wind speed and changes from 4 MW (1 p.u.) to 2.4 MW (0.6 p.u.) at $t = 0.8$ s. The active power tracks to its reference very well during the transient and steady-state conditions. The reference and grid reactive powers are depicted in Fig. 6.2(c). A step change in Q_g^* from 0 to 1.2 MVAR (0.3 p.u.) is applied at $t = 1.0$ s. At $t = 1.5$ s, another step change in Q_g^* is applied from 0 to -2.8 MVAR (-0.7 p.u.). During the time intervals, (1 to 1.3s) and (1.5 to 1.8s), the grid apparent power, S_g is found to be 2.6833 MVA (0.671 p.u.) and 3.6878 MVA (0.922 p.u.), respectively. The phase-*a* grid current, i_{ag} magnitude is proportional to the S_g as shown in Fig. 6.2(d).

The net dc-bus voltage, v_{dc} is maintained at its reference value by the battery supply as shown in Fig. 6.2(e). The balancing of capacitor voltages has been achieved during different active and reactive power references as demonstrated in Fig. 6.2(f). From these results, it can be established that the grid active and reactive powers can be controlled in a decoupled manner, similar to the classical control schemes, but with a simpler approach.

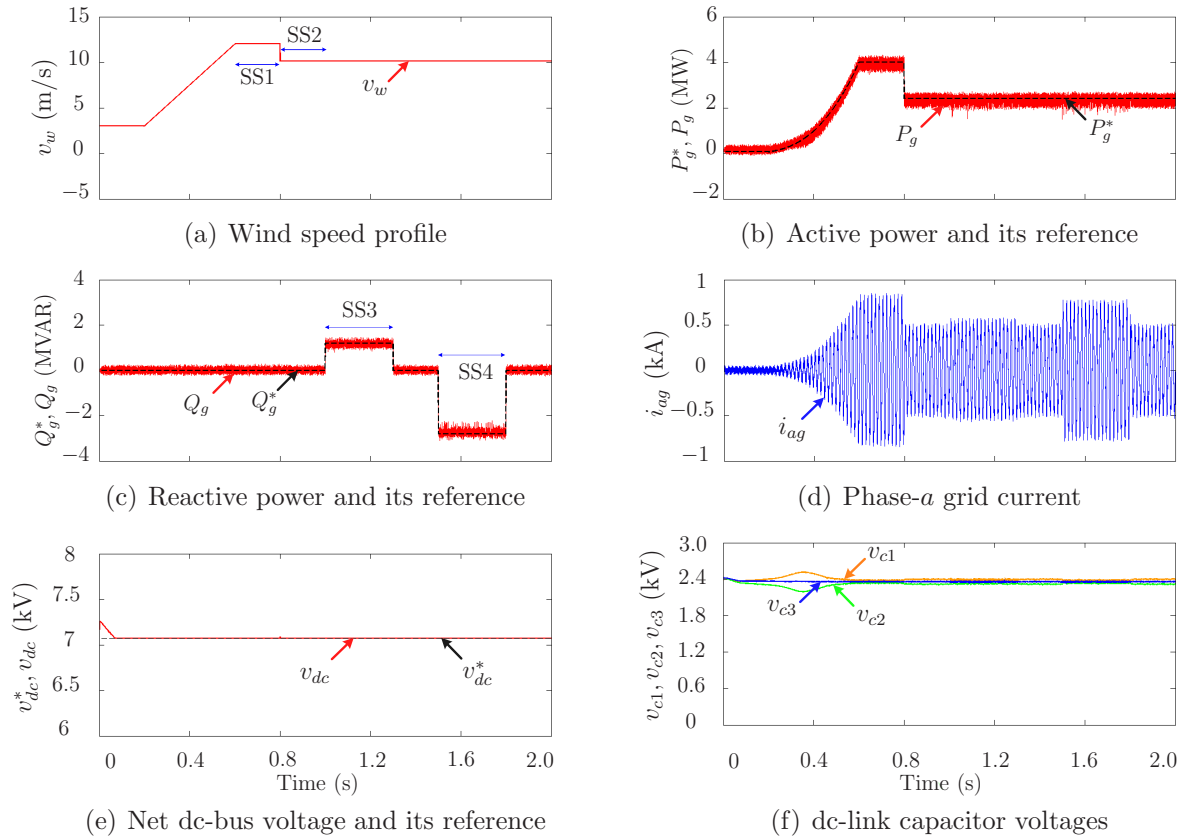


Figure 6.2: Simulation results with dynamic active and reactive power references.

6.2.2 Steady-state Analysis

The performance of the proposed controller during four steady-state operating conditions (denoted as SS1-SS4 in Fig. 6.2) is summarized in Table 6.2. The performance assessment parameters are defined in Appendix C. The reference tracking errors, e_{pg} and e_{qg} are maintained below 5 %, and thus they validate the proposed control scheme. The capacitor voltages are well balanced with an error magnitude of less than 1 %. This facilitates the reduced voltage stress on the semiconductor switches. The THD is maintained below 5 % except for SS3, where the switching frequency is much lower (776 Hz) than the other operating conditions. The switching frequency is maintained below 1 kHz and this enhances the reliability of the switches.

Table 6.2: Steady-state analysis with simulation results

Case	P_g^* (p.u.)	Q_g^* (p.u.)	% e_{pg}	% e_{qg}	% e_{vc}	%THD	f_{sw} (Hz)
SS1	1.0	0	4.90	1.63	0.45	3.41	854
SS2	0.6	0	3.91	1.37	0.75	4.80	886
SS3	0.6	0.3	4.85	2.98	0.66	5.36	776
SS4	0.6	-0.7	3.45	3.20	0.38	3.29	991

6.2.3 Comparison to Classical VOC

The proposed predictive control method is compared with the classical decoupled voltage oriented control [2, 144] in steady-state and the results are presented in Figs. 6.3 to 6.8. The active and reactive power references are considered to be 1.0 p.u. (4 MW) and 0 p.u., respectively (case SS1). The dc-link capacitor voltages are assumed to be balanced and thus the weighting factor λ_{dc} is set to zero. With this assumption, the number of calculations for the predictive control decreased and as a result, the device switching frequency f_{sw} is decreased from 854 to 680 Hz. In addition, no weighting factor is used for the switching frequency minimization. The in-phase disposition (IPD) modulation, which gives the best harmonic profile [84] is used in the decoupled voltage-oriented control. In order to make the device switching frequency the same as the predictive control, the carrier frequency is set to 2040 Hz ($= 680 \text{ Hz} \times 3$).

The comparison between the classical and proposed method in terms of reference tracking is presented in Figs. 6.3 and 6.4. The proposed method exhibits better performance compared to the classical method. The e_{pg} and e_{qg} for the classical method are 1.1 %, and 0.8 %, whereas, for the proposed method they are 0.98 %, and 0.75 %, respectively.

The inverter line-line voltage, v_{iab} and its Fast Fourier Transform (FFT) with the classical and proposed method are shown in Figs. 6.5 and 6.6. The classical method produces harmonics around the carrier frequency and its multiples, whereas the proposed method produces harmonics spread over the whole FFT window. But, the magnitude of harmonics with the proposed method is less compared to the classical, and as a result less THD is observed.

The phase- a grid current, i_{ag} and its FFT are depicted in Figs. 6.7 and 6.8, where the THD is found to be lower for the proposed method in contrast to the classical controller. Despite the lower switching frequency compared to the operating condition SS1 depicted in Table 6.2, the THD is lower, because the cost function includes only reference tracking.

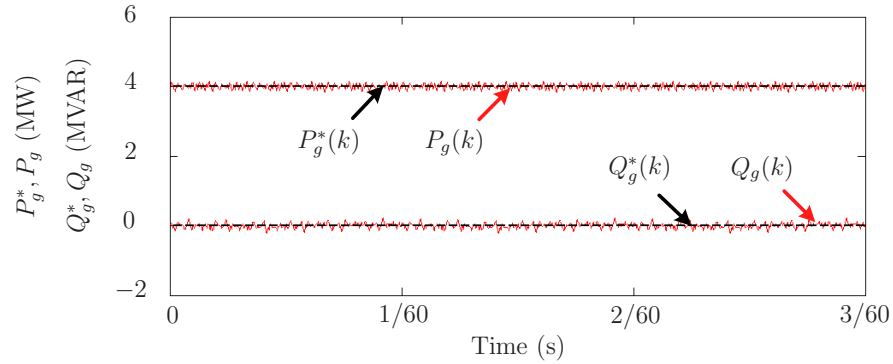


Figure 6.3: Simulation results for active and reactive powers tracking with classical VOC.

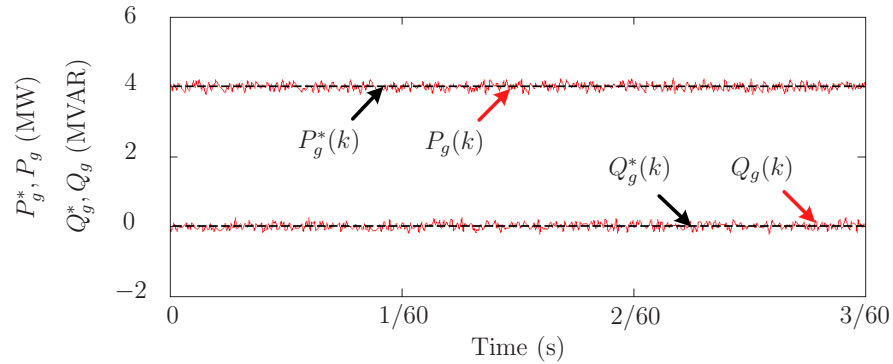


Figure 6.4: Simulation results for active and reactive powers tracking with predictive control.

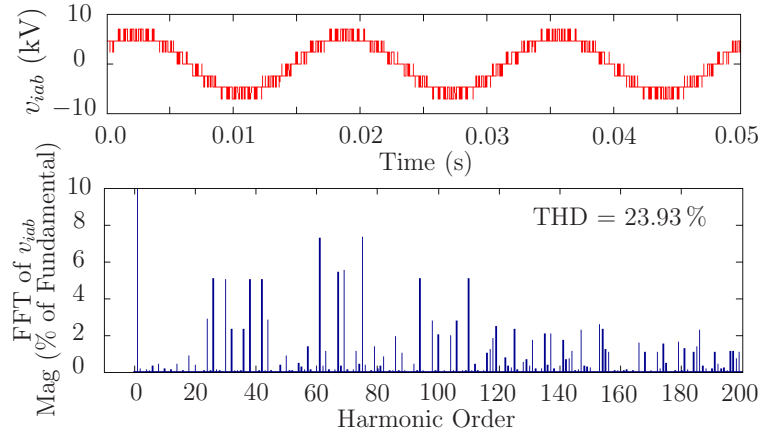


Figure 6.5: Simulation results for inverter line-line voltage and its FFT with the classical decoupled voltage-oriented control.

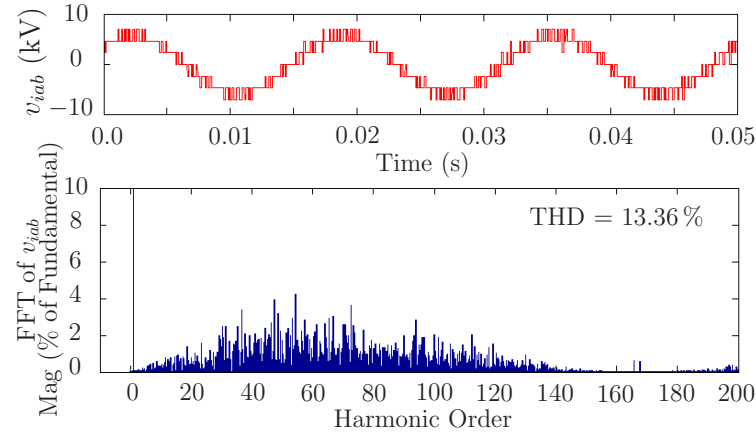


Figure 6.6: Simulation results for inverter line-line voltage and its FFT with the proposed predictive control.

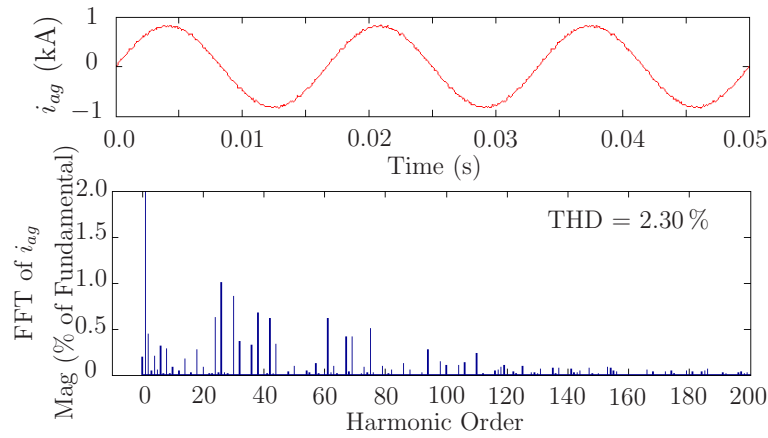


Figure 6.7: Simulation results for phase-a grid current, and its FFT with the classical decoupled voltage-oriented control.

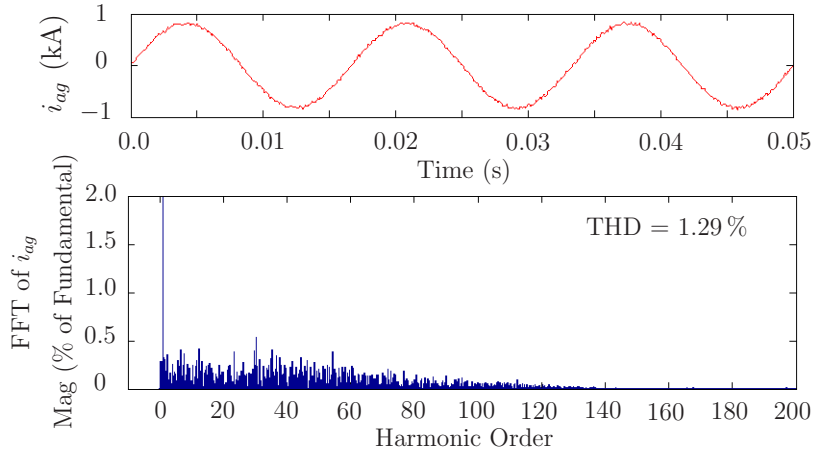


Figure 6.8: Simulation results for phase-*a* grid current, and its FFT with the proposed predictive control.

6.2.4 Comparison to Lagrange Extrapolation

The performance of the Lagrange and the proposed extrapolation methods are analyzed and compared as shown in Figs. 6.9 and 6.10. With a step change in the reference active power from 0.2 to 0.4 p.u., the Lagrange extrapolation method produces a dip in the active power, which in turn produces a spike in the inverter output line-line voltage as shown in Fig. 6.9. This voltage spike is undesirable because it will damage the semiconductor switches. It is important to note that the voltage spike is produced due to the oscillations in the extrapolated reference active power, $P_g^*(k+1)$, which is shown in the box of Fig. 6.9. The Lagrange method uses three present and past values for the calculation of future value [refer to (5.17)] and this leads to oscillations in the extrapolated reference power. The extrapolated grid voltage $[v_{dg}^e(k+1)]$ and predicted grid currents $[i_{dg}^p(k+1), i_{qg}^p(k+1)]$ do not contribute to this voltage spike [refer to (6.2)].

The voltage spike occurs even for a small step change in reference active and reactive powers and thus it is not advisable to use Lagrange extrapolation method. This problem has been rectified with the proposed extrapolation method, as shown in Fig. 6.10, and thus it guarantees safe operation of the semiconductor devices. The proposed method uses only one past value and eliminates the oscillations in $P_g^*(k+1)$ as shown in the box in Fig. 6.10. Similar performance can be observed for a step change in the reference reactive power.

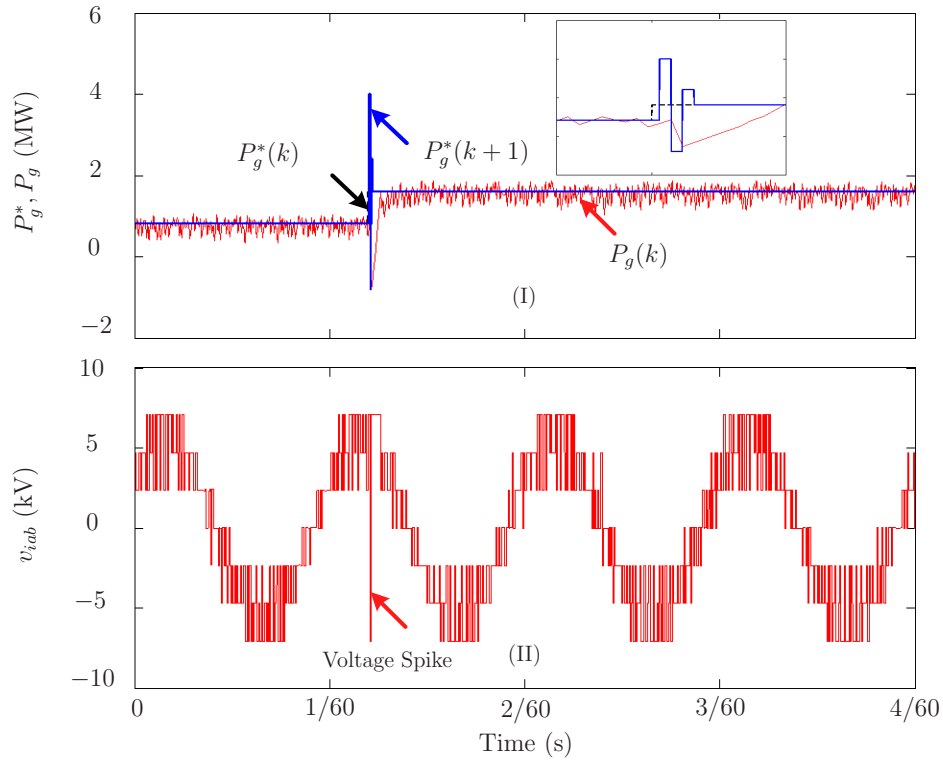


Figure 6.9: Simulation results for step-change in active power with Lagrange extrapolation.

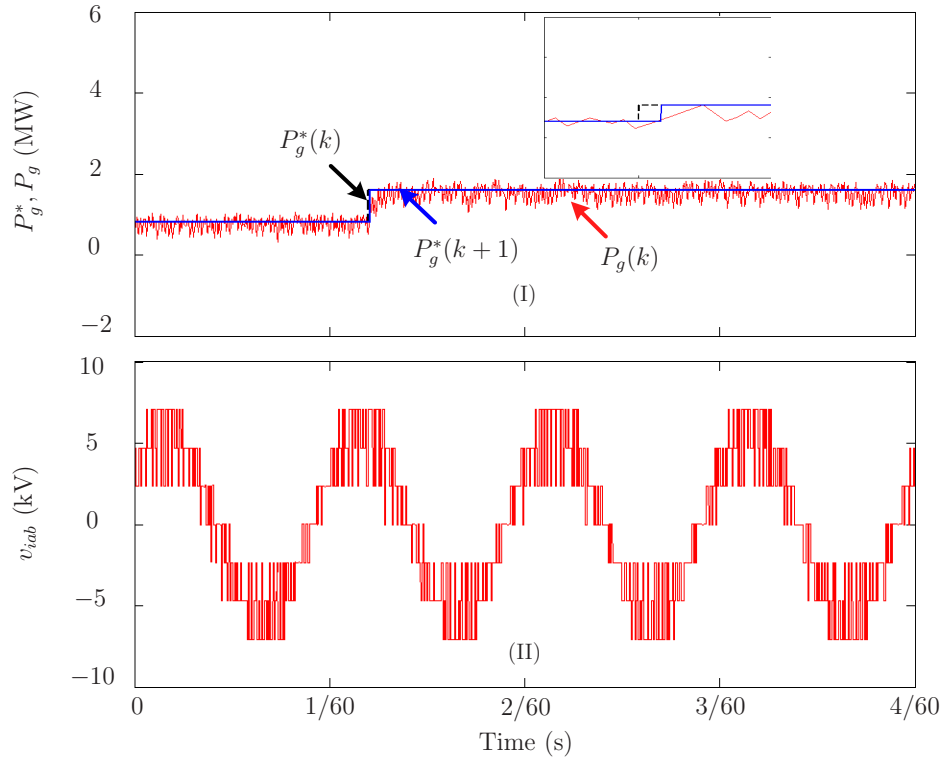


Figure 6.10: Simulation results for step-change in active power with proposed extrapolation.

6.2.5 Capacitor Voltages Balancing

In order to verify the proposed dc-link balancing algorithm, two cases are considered by connecting an external resistor R_x (11.46 p.u.) and capacitor C_x (15.33 p.u.) across the dc-link capacitor C_{dc2} at a time of $t = 0.7$ s. Even with the step-connection of the resistor, the controller takes action in a few sampling instants, and thus the capacitor voltages continue to be balanced as shown in Fig. 6.11(a). With the step connection of C_x , the capacitor voltages diverge as shown in Fig. 6.11(b), but the controller forces the capacitor voltages to be balanced, while maintaining the grid powers at their reference values (of SS1). As a consequence, the capacitor voltages become balanced, with a recovery time of 0.4 s. This case may happen when any of the dc-link capacitors are damaged while they are in the parallel connection. The currents through R_x and C_x are also shown in Figs. 6.11(a) and 6.11(b), respectively. These results validate that the proposed controller can work very well even with the dc-link parameter variations.

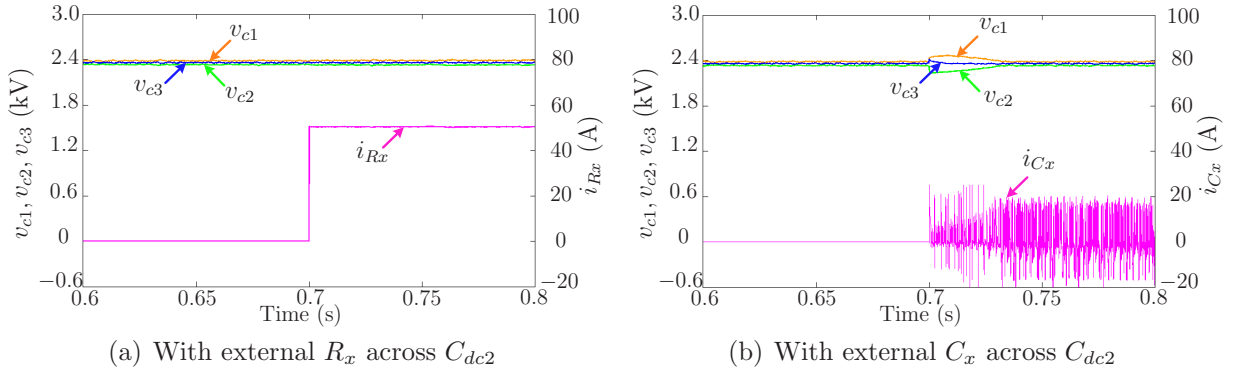
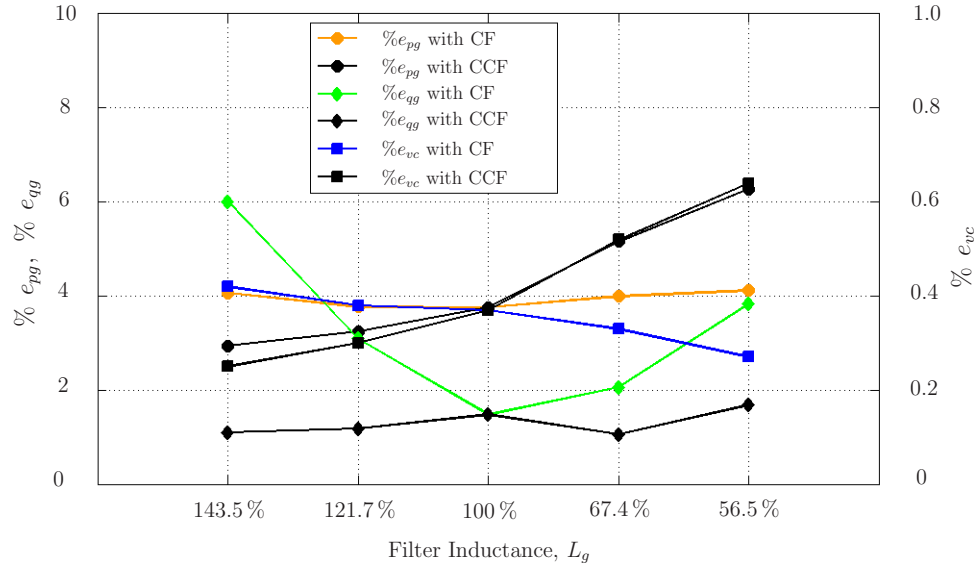


Figure 6.11: Simulation results for dc-link capacitor voltages balancing with perturbations to the system model.

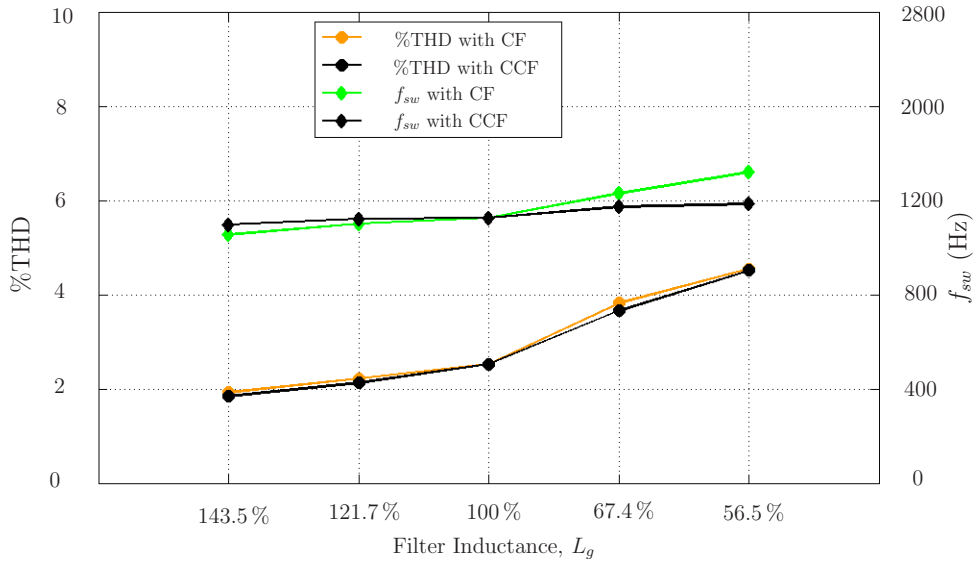
6.2.6 Robustness Analysis

To demonstrate the robustness of predictive control with the filter parameter variations, two cases are considered: in the first case (CF: changes to the filter), the filter inductance is considered to change from 143.5 % to 56.5 %, but this information is not provided to the controller. The control algorithm uses a rated filter inductance value of 100 % (0.2 p.u.=2.1 mH). This is the typical case in a grid-tied system, where the power system impedance changes randomly, and as a consequence, the equivalent filter value changes.

In the second case (CCF: changes to the controller and filter), the correct values of the filter are given to the controller for the purpose of comparison. To simplify the analysis, the switching frequency minimization is not considered, and thus $\lambda_{swc} = 0$. Even though the filter parameters change, the controller chooses a switching state that produces the minimal error in the reference tracking and capacitor voltages balancing. As shown in Figs. 6.12(a) and 6.12(b), the difference between the CF and CCF conditions is found to be very small, in the L_g variation range of 130 % to 70 %.



(a) Comparison of % e_{pg} , % e_{qg} and % e_{vc}



(b) Comparison of %THD and f_{sw} (Hz)

Figure 6.12: Simulation results with grid filter parameter variations (CF: changes to filter, and CCF: changes to controller and filter.)

6.3 Experimental Results

In order to verify the performance of the proposed control strategy, experimental results are presented using a 5 kVA/208 V 4L-DCC prototype and dSPACE DS1003 control platform. More details about the experimental set-up can be found in the Section 5.5.1. The inverter and controller parameters are listed in Table 6.1.

To compensate for the computational delay, the cost function is calculated using the guidelines given in Chapter 5.5.2. The control algorithm with delay compensation is shown in Fig. 6.13. Because of the SRF modeling of dc-link voltages, the $i_{dg}(k+1)$ and $i_{qg}(k+1)$ can be used directly in the prediction of $i_{c1}(k+2)$, $i_{c2}(k+2)$ and $i_{c3}(k+2)$ [refer to (6.6)]. If the modeling of capacitor voltages is done in a natural frame, then the $i_{dg}(k+1)$ and $i_{qg}(k+1)$ should be converted to $i_{ag}(k+1)$, $i_{bg}(k+1)$, and $i_{cg}(k+1)$ during each sampling interval, and this will increase the computational burden. Due to the $(k+2)$ predictions, and the SI parameter values, the weighting factors obtained in the experiments are different from the simulations, but their impact on the controller remains the same.

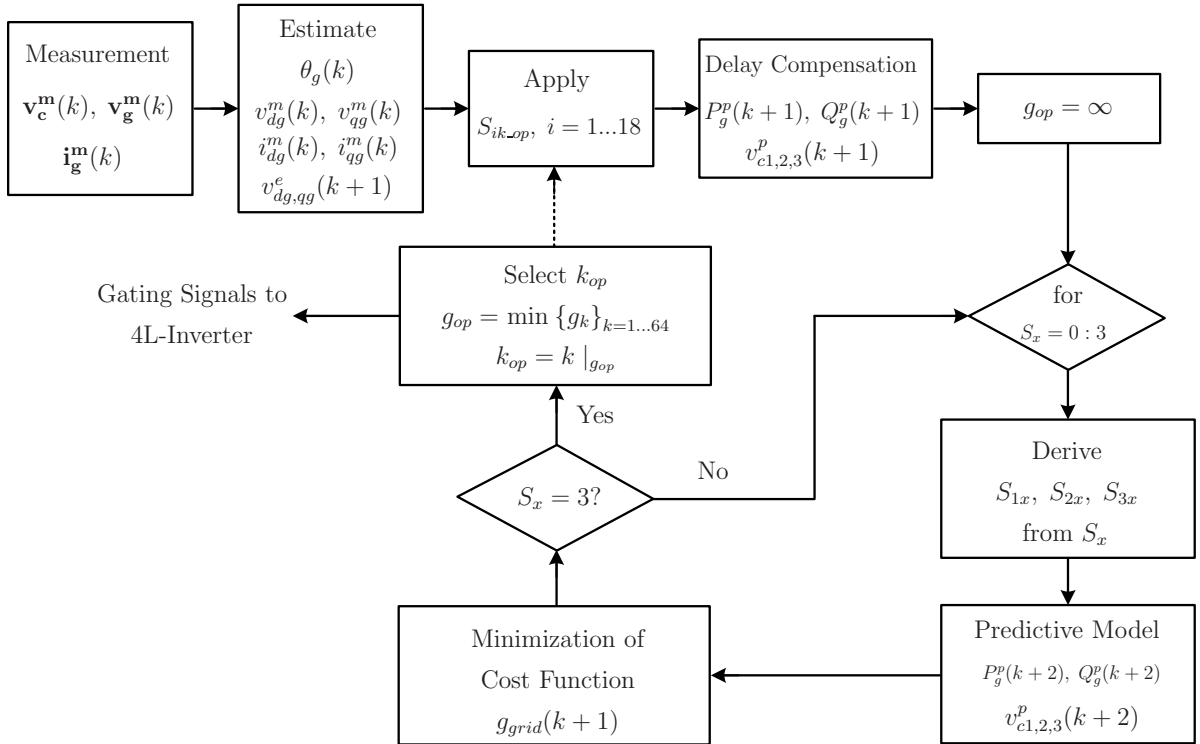


Figure 6.13: Proposed predictive power control algorithm with delay compensation.

The experimental results with the different active and reactive power references are shown in Fig. 6.14. Similar to the simulations, the decoupled control of active and reactive powers is achieved with a good dynamic response and less steady-state error. The dc-link capacitor voltages are balanced during all the operating conditions. The steady-state analysis has been carried out and summarized in Table. 6.3. The higher tracking errors in experiments can be attributed to the delay provided by the sensors and the IGBT gate drivers. Since the predictions are in $(k + 2)$, the e_{vc} is found to be smaller than in simulations.

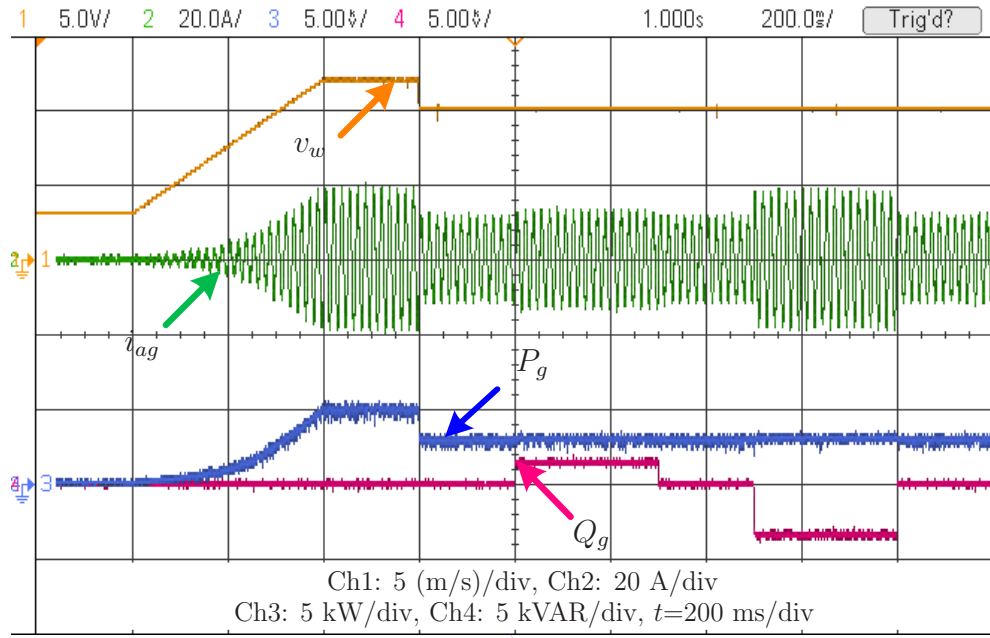
Table 6.3: Steady-state analysis with experimental results

Case	$P_g^*(\text{p.u.})$	$Q_g^*(\text{p.u.})$	$\%e_{pg}$	$\%e_{qg}$	$\%e_{vc}$	$\%\text{THD}$	$f_{sw}(\text{Hz})$
SS1	1.0	0	5.08	2.59	0.39	3.82	845
SS2	0.6	0	4.05	2.34	0.63	5.23	900
SS3	0.6	0.3	4.56	3.25	0.51	4.88	731
SS4	0.6	-0.7	3.87	3.89	0.29	3.70	998

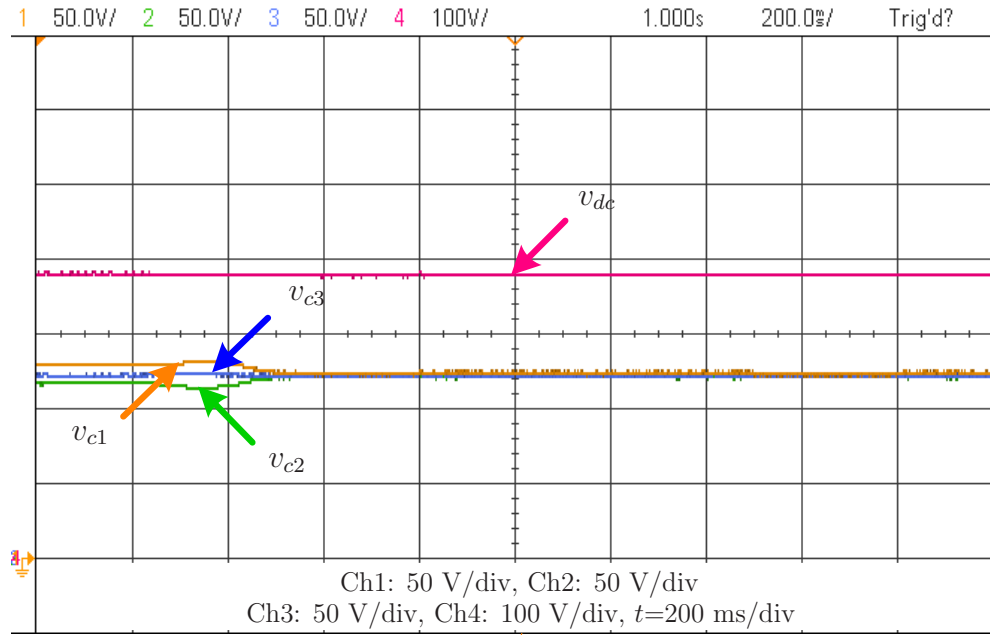
The Lagrange and proposed extrapolation methods are experimentally analyzed and compared as shown in Fig. 6.15. As confirmed by the simulations, the Lagrange extrapolation method produces a dip in the active power and a spike in the inverter output voltage as shown in Fig. 6.15(a). The oscillations in the extrapolated reference active power $P_g^*(k + 2)$ are also shown in Fig. 6.15(a). The proposed extrapolation method eliminates the voltage spike as shown in Fig. 6.15(b) and protects the semiconductor switches.

The dc-link dynamics with the external resistor R_x and capacitor C_x across C_{dc2} , are given in Figs. 6.16(a) and 6.16(b), respectively. Similar to the simulations, the balancing of the dc-link capacitor voltages have been maintained even with the step-connection of R_x and C_x . The recovery time is found to be 1.3 s with C_x , which is higher compared to the simulations. This difference is established due to the different weighting factors and SI values of the grid current and the dc-link capacitor used in the prototype.

The effect of the filter parameter variations on the proposed controller is experimentally analyzed and presented in Figs. 6.17(a) and 6.17(b). Only a small difference is observed between the CF and CCF cases which are similar to the simulation results, when the L_g variation is in a range of 130 % to 70 %. These results validate the robustness of the proposed controller.

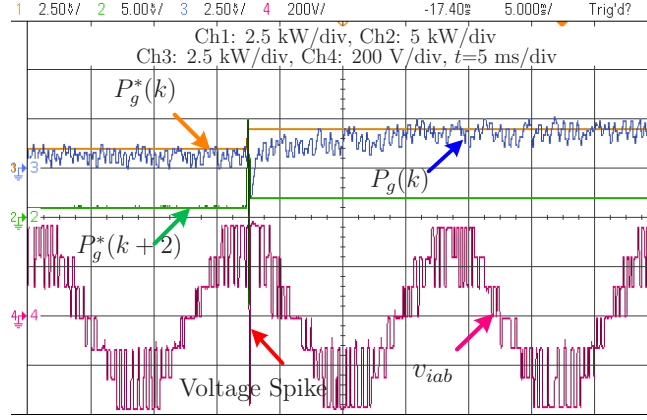


(a)

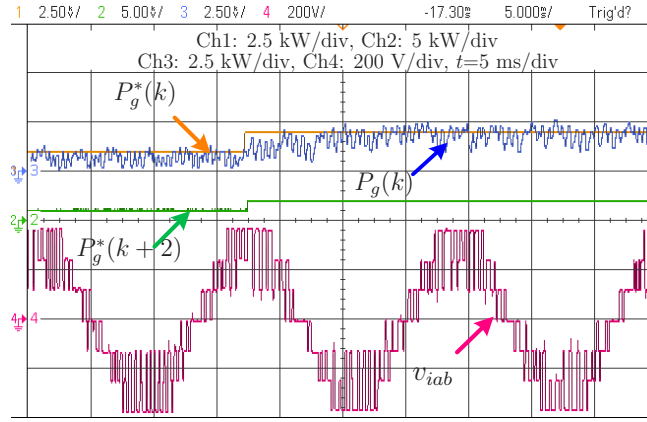


(b)

Figure 6.14: Experimental results with dynamic active and reactive power references.

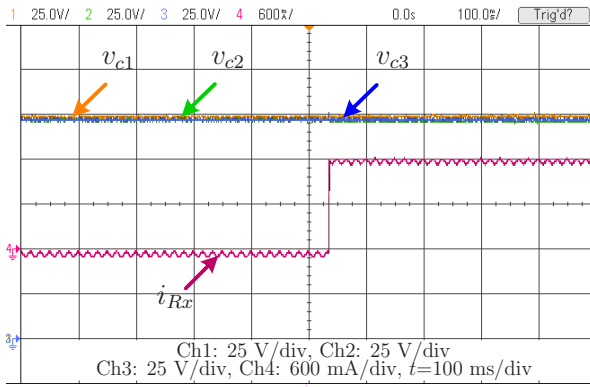


(a) With Lagrange extrapolation

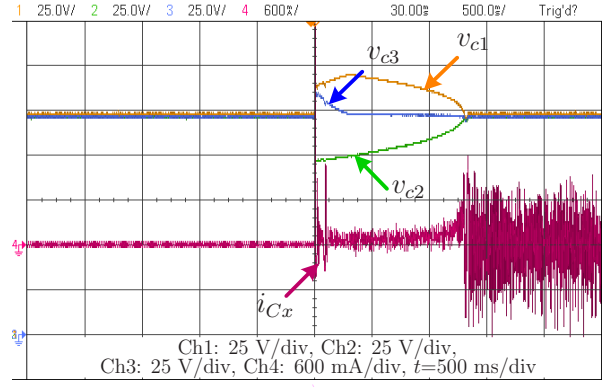


(b) With the proposed extrapolation

Figure 6.15: Experimental results during the step change in active power reference.

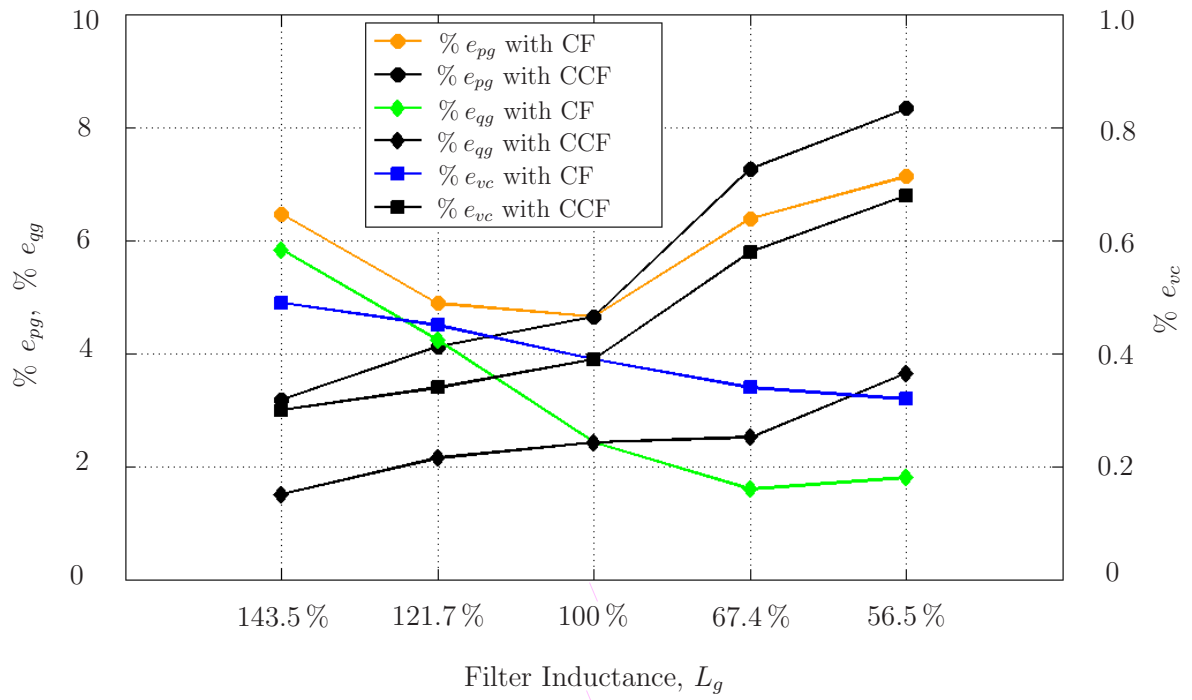


(a) External R_x across C_{dc2}

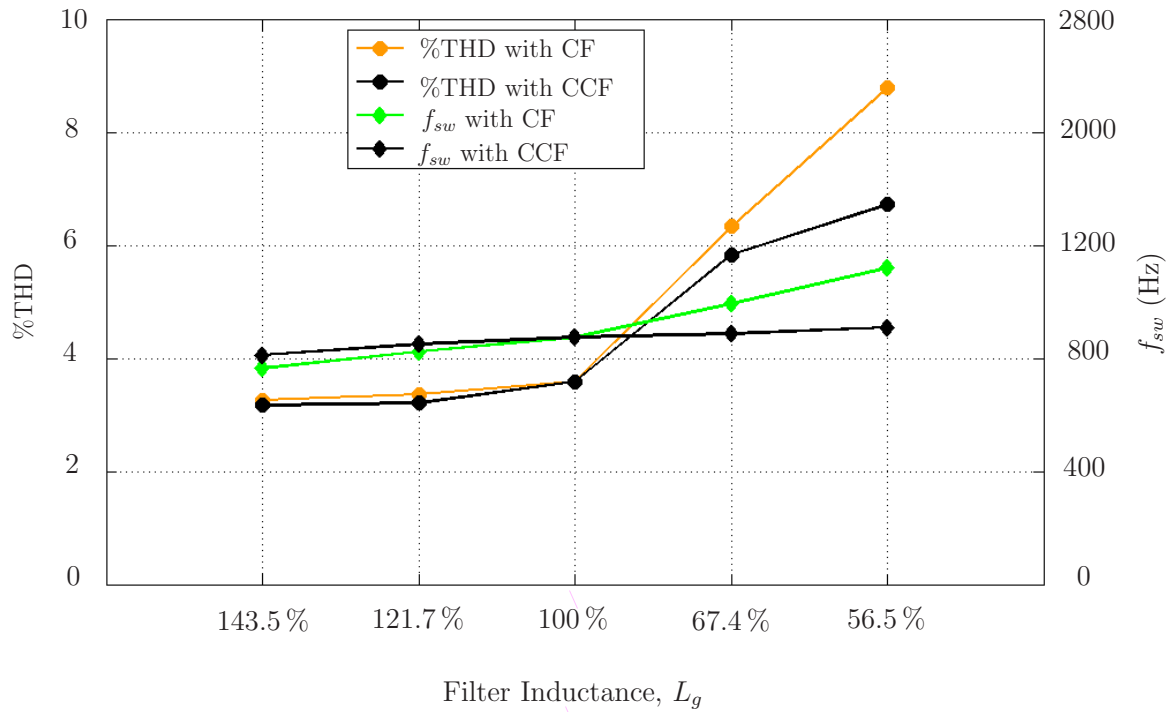


(b) External C_x across C_{dc2}

Figure 6.16: Experimental results for dc-link capacitor voltages balancing with the perturbations in system model.



(a) Comparison of % e_{pg} , % e_{qg} and % e_{vc}



(b) Comparison of %THD and f_{sw} (Hz)

Figure 6.17: Experimental analysis with grid filter parameter variations (CF: changes to filter, and CCF: changes to controller and filter).

6.4 Conclusion

In this chapter, an intuitive approach using model predictive control is presented in a synchronous reference frame for the decoupled active and reactive power regulation of a grid-tied 4L-DCC. The major contributions of the work presented in this chapter are summarized as follows:

- The decoupled active and reactive power control, along with the dc-link capacitor voltages balancing, have been achieved during all operating conditions. The proposed methodology can be easily extended to other level DCCs.
- The dynamic response has been improved by eliminating the internal current control loops and modulators. Compared with the classical decoupled voltage-oriented control, a better reference tracking and grid current waveforms have been achieved.
- The switching loss of the semiconductor devices is minimized by maintaining the switching frequency below 1 kHz.
- The proposed extrapolation method can extrapolate SRF references to future state without any oscillations (in reference control variables) during the transient conditions. Moreover, this method is computationally inexpensive compared to Lagrange extrapolation as it uses only one past sample value for the extrapolation.
- The control scheme can compensate for perturbations in the dc-link and grid filter parameter changes, while the grid active and reactive powers continue to effectively track their references.

Chapter 7

Predictive Control of Three-Level Boost and NPC Converters Based PMSG-WECS

In this chapter, a novel medium voltage (MV) converter using a diode rectifier, three-level boost (TLB) converter and neutral-point-clamped (NPC) inverter is proposed for a high power permanent magnet synchronous generator (PMSG) based wind energy conversion system (WECS). A model predictive strategy is introduced to control the complete WECS. The major tasks being carried out in this chapter are summarized as follows:

- Continuous- and discrete-time modeling of the complete WECS including TLB and NPC converters is presented;
- Independent control loops are presented for the TLB and NPC converters. The strategy presented here for the grid-tied converter control is different from the one discussed in Chapters 5 and 6.
- The average semiconductor device switching frequencies are minimized and maintained below 1.5 kHz and 1 kHz, respectively for the TLB and NPC converters.
- Effectiveness of the boost converter in controlling the neutral-point voltage with the perturbations in the dc-link is investigated.
- Feasibility of the proposed converter and control scheme is verified through MATLAB simulations on 3 MW/3000 V/577 A system and dSPACE DS1103-based experiments on a 3.6 kW/208 V/10 A prototype.

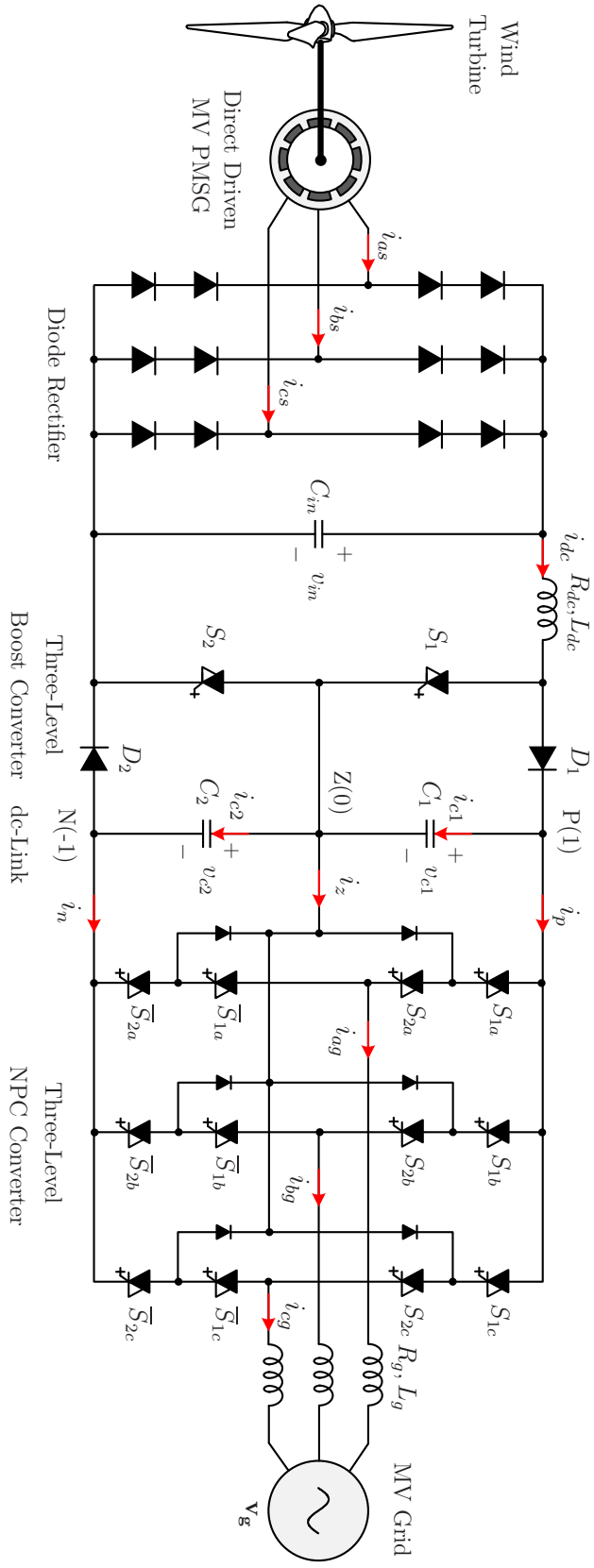


Figure 7.1: Configuration of TLB-NPC converters based medium voltage PMSG-WECS.

7.1 Modeling of Complete WECS

The power conversion system for the direct-driven PMSG-based WECS is shown in Fig. 7.1. It consists of three stages: ac/dc, dc/dc and dc/ac, and these are implemented using a diode rectifier, TLB converter and NPC inverter, respectively. The diode rectifier limits the direction of power flow, and only the generating mode is possible which is the typical requirement in a WECS. The diode rectifier features series connected diodes due to the MV generator. The output of the diode rectifier, v_{in} remains unregulated but is limited by the rated speed of the turbine, which defines the voltage rating of the capacitor. The TLB converter enables MV operation for the dc-dc stage. The WECS can be operated efficiently in the complete wind speed range by controlling the gating signals for the TLB converter [115]. The output of the TLB directly fits the two dc-link capacitors of the grid-tied NPC inverter. This second dc-link provides decoupling for the generator- and grid-side converters and thus individual control loops can be developed. The inverter is composed of 12 active switches and 6 clamping diodes. The dc-link consists of two capacitors, and ideally they will share equal voltages ($v_{c1} = v_{c2} = v_c$). The NPC inverter is connected to the MV grid through an L filter. The NPC multilevel and medium voltage operation at grid-side improves the power quality and efficiency of the system compared to the two-level converters [2, 3, 14]. It is important to note that both the generator and grid are rated for MV operation.

In the proposed megawatt-level WECS, the following four variables need to be regulated:

- Maximum power point tracking (MPPT) during all wind speed conditions to improve wind energy conversion efficiency
- Balancing of the dc-link capacitor voltages in order to reduce the device voltage stress and improve power quality
- Net dc-bus voltage control to ensure proper operation for the grid-tied inverter
- Reactive power generation to meet the grid codes

The first two variables are regulated by the TLB converter, and the last two variables are handled by the NPC inverter. In this section, the modeling is presented to demonstrate that the proposed power converters accomplish the above-mentioned control requirements.

7.1.1 Grid-Tied NPC Inverter Model

The mathematical modeling of the NPC inverter was previously analyzed in [279]. In this chapter, a simplified modeling is achieved owing to the fact that the NPC inverter need not control the dc capacitor voltages. The grid-tied inverter control was proposed in synchronous reference frame in Chapters 5 and 6. In this chapter, the model is presented in a stationary frame to reduce the number of online calculations incurred in the discrete-time predictive controller. The switching states and the corresponding inverter voltages are shown in Table 7.1, where, it can be noted that: (a) only two switches conduct at any time, (b) switch pairs (S_{1x}, \bar{S}_{1x}) , and (S_{2x}, \bar{S}_{2x}) operate in a complementary manner, and (c) a total of 19 voltage vectors with 27 (3^3) switching combinations are available [84].

Table 7.1: Switching states and NPC inverter terminal voltages ($x = a, b, c$)

S_x	S_{1x}	S_{2x}	\bar{S}_{1x}	\bar{S}_{2x}	v_{xN}
1	1	1	0	0	$v_{c1} + v_{c2}$
0	0	1	1	0	v_{c2}
-1	0	0	1	1	0

The inverter ac-side voltages (with respect to the negative dc-rail, N) can be expressed in terms of switching signals and dc-side voltages as follows:

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = v_{c1} \begin{bmatrix} S_{1a} \\ S_{1b} \\ S_{1c} \end{bmatrix} + v_{c2} \begin{bmatrix} S_{2a} \\ S_{2b} \\ S_{2c} \end{bmatrix} \quad (7.1)$$

where v_{c1} and v_{c2} are dc-link capacitor voltages. S_{1a} , S_{2a} , S_{1b} , S_{2b} , S_{1c} , and S_{2c} are the switching signals.

The grid current dynamics can be expressed in terms of inverter voltages, grid voltages and filter inductance as, in the following:

$$\frac{d\mathbf{i}_g}{dt} = \frac{1}{L_g} [\mathbf{v}_i - \mathbf{v}_g - R_g \mathbf{i}_g] \quad (7.2)$$

where L_g is the grid filter inductance and R_g is the internal resistance of the inductor.

The current and voltage vectors are defined as:

$$\begin{aligned}\mathbf{i}_g &= [i_{\alpha g} \ i_{\beta g}]^T = [K_{abc \rightarrow \alpha\beta}] [i_{ag} \ i_{bg} \ i_{cg}]^T \\ \mathbf{v}_i &= [v_{\alpha i} \ v_{\beta i}]^T = [K_{abc \rightarrow \alpha\beta}] [v_{aN} \ v_{bN} \ v_{cN}]^T \\ \mathbf{v}_g &= [v_{\alpha g} \ v_{\beta g}]^T = [K_{abc \rightarrow \alpha\beta}] [v_{ag} \ v_{bg} \ v_{cg}]^T\end{aligned}$$

where $[K_{abc \rightarrow \alpha\beta}]$ is the transformation matrix [refer to (B.1)].

The discrete-time model for grid currents can be obtained from (7.2) for one-step prediction as follows [refer to (4.8)] [258, 259]:

$$\mathbf{i}_g(k+1) = C_v [\mathbf{v}_i(k+1) + \mathbf{v}_g(k)] + C_i \mathbf{i}_g(k) \quad (7.3)$$

where C_v and C_i are constants as defined by,

$$C_v = \frac{T_s}{L_g + R_g T_s}, \quad C_i = \frac{L_g}{L_g + R_g T_s} \quad (7.4)$$

where T_s is the sampling time. The prediction of inverter voltage uses the 27 possible switching states and the measured dc-link capacitor voltages, as demonstrated in (7.1). From (7.1) and (7.3), it can be understood that the future behavior of the grid currents can be controlled by properly choosing an optimal one among the 27 switching states.

7.1.2 Three-Level Boost Converter Model

The discrete-time modeling and control of a standard 2L-boost converter was analyzed in [295]. In this paper, a similar approach is used for the modeling and control of the TLB converter. A simplified WECS as shown in Fig. 7.2 is derived to facilitate the modeling of the TLB converter [72]. The PMSG, along with the diode rectifier and capacitive filter, C_{in} can be represented as a variable dc voltage source, v_{in} , and the grid-tied inverter can be represented by two variable resistive loads (R_1 and R_2) as shown in Fig. 7.3. The R_{dc} represents the internal resistance of the inductor L_{dc} . In a 2L-boost converter only one active switch is used, and this leads to 2 ($2^{\text{number of active switches}} = 2^1$) operating modes (0 or 1). In the TLB converter, two active switches (S_1 and S_2) are used as shown in Figs. 7.1 to 7.3 and consequently 4 ($2^{\text{number of active switches}} = 2^2$) modes are available (00, 01, 10, 11) [118, 296–298]. The increase in the operating modes and thus switching states will lead to an additional control freedom to charge and discharge the dc-link capacitors independently.

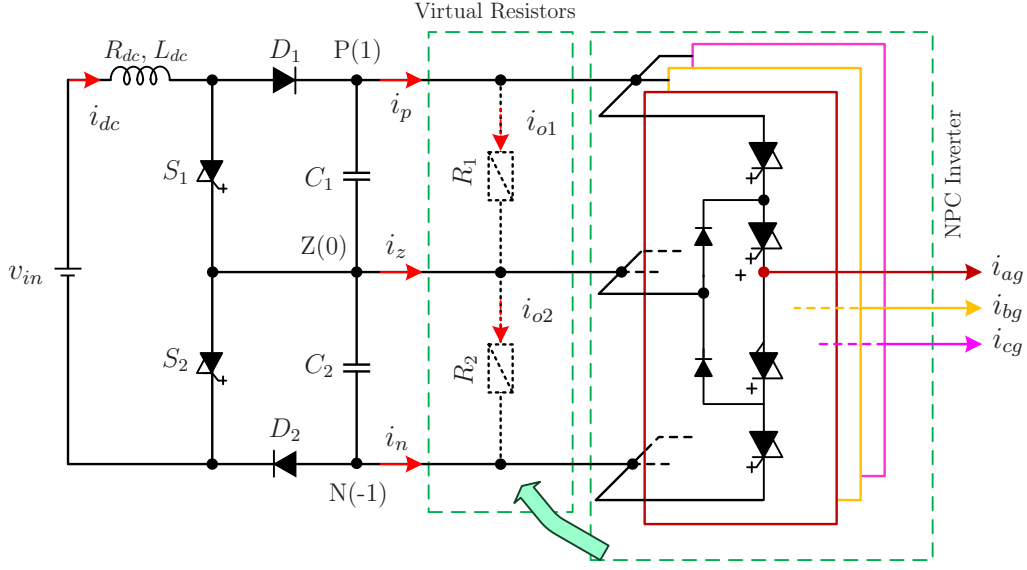


Figure 7.2: Simplified power circuit of the dc-dc TLB converter stage.

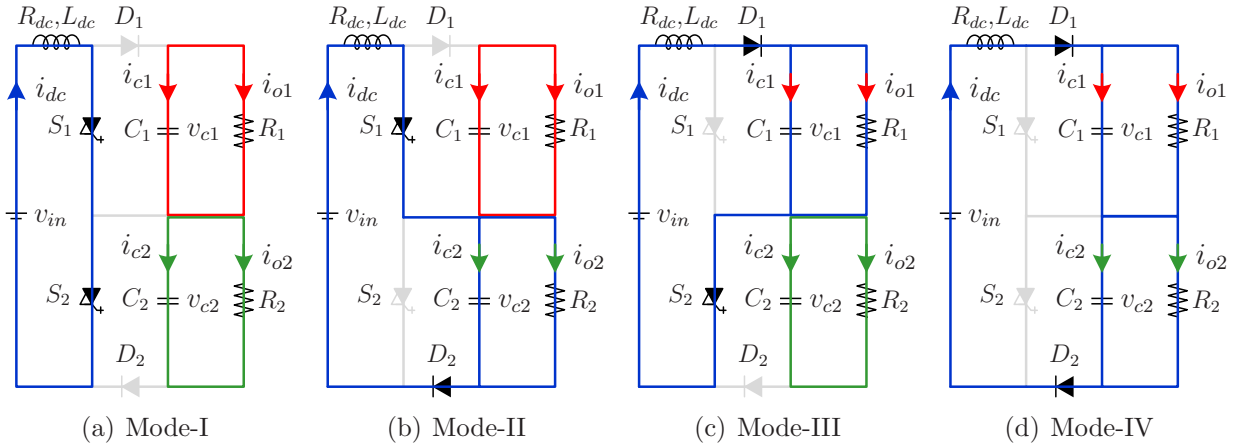


Figure 7.3: Modes of operation for three-level boost converter.

- Mode-I: [Fig. 7.3(a)] The S_1, S_2 are ON and D_1, D_2 are OFF. The dc-current, i_{dc} flows through the L_{dc} , S_1 and S_2 and thus energy is stored in the inductor only and the dc-link capacitors are not charged. The energy which is already stored in the capacitors C_1 and C_2 is discharged to the virtual loads R_1 and R_2 , respectively. The output currents through these loads can be represented as i_{o1} and i_{o2} . During this mode, the inductor current and dc-link voltages can be represented as follows:

$$\frac{di_{dc}}{dt} = \frac{v_{in} - R_{dc}i_{dc}}{L_{dc}}, \quad \frac{dv_{c1}}{dt} = -\frac{i_{o1}}{C_1}, \quad \frac{dv_{c2}}{dt} = -\frac{i_{o2}}{C_2}. \quad (7.5)$$

- Mode-II: [Fig. 7.3(b)] The S_1, D_2 are ON and S_2, D_1 are OFF. The dc-current flows through the L_{dc}, S_1, C_2, R_2 and D_2 and thus stored inductor energy is transferred to the C_2 and R_2 . The energy in capacitor C_1 is discharged to the load R_1 . The resulting equations can be given as:

$$\frac{d i_{dc}}{dt} = \frac{v_{in} - R_{dc} i_{dc} - v_{c2}}{L_{dc}}, \quad \frac{d v_{c1}}{dt} = -\frac{i_{o1}}{C_1}, \quad \frac{d v_{c2}}{dt} = \frac{i_{dc}}{C_2} - \frac{i_{o2}}{C_2}. \quad (7.6)$$

- Mode-III: [Fig. 7.3(c)] The S_2, D_1 are ON and S_1, D_2 are OFF. The dc-current flows through the L_{dc}, D_1, C_1, R_1 and S_2 and thus stored inductor energy is transferred to C_1 and R_1 . The energy in capacitor C_2 is discharged to the load R_2 . The subsequent equations are:

$$\frac{d i_{dc}}{dt} = \frac{v_{in} - R_{dc} i_{dc} - v_{c1}}{L_{dc}}, \quad \frac{d v_{c1}}{dt} = \frac{i_{dc}}{C_1} - \frac{i_{o1}}{C_1}, \quad \frac{d v_{c2}}{dt} = -\frac{i_{o2}}{C_2}. \quad (7.7)$$

- Mode-IV: [Fig. 7.3(d)] The D_1, D_2 are ON and S_1, S_2 are OFF. The dc-current flows through the $L_{dc}, D_1, C_1, R_1, C_2, R_2$ and D_2 and thus inductor energy is transferred to the capacitors C_1, C_2 and loads R_1, R_2 . The dynamic system is as follows:

$$\frac{d i_{dc}}{dt} = \frac{v_{in} - R_{dc} i_{dc} - v_{c1} - v_{c2}}{L_{dc}}, \quad \frac{d v_{c1}}{dt} = \frac{i_{dc}}{C_1} - \frac{i_{o1}}{C_1}, \quad \frac{d v_{c2}}{dt} = \frac{i_{dc}}{C_2} - \frac{i_{o2}}{C_2}. \quad (7.8)$$

By combining the dynamic equations in (7.5)-(7.8), the continuous-time system describing inductor current and dc-link capacitor voltages can be obtained as:

$$\frac{d}{dt} \begin{bmatrix} i_{dc} \\ v_{c1} \\ v_{c2} \end{bmatrix} = \begin{bmatrix} -\frac{R_{dc}}{L_{dc}} & -\frac{(1-S_{1t})}{L_{dc}} & -\frac{(1-S_{2t})}{L_{dc}} \\ \frac{(1-S_{1t})}{C_1} & 0 & 0 \\ \frac{(1-S_{2t})}{C_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{dc} \\ v_{c1} \\ v_{c2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{dc}} & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ 0 & 0 & -\frac{1}{C_2} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{o1} \\ i_{o2} \end{bmatrix} \quad (7.9)$$

where S_{1t} and S_{2t} are the switching signals applied to the switches S_1 and S_2 respectively.

It is important to note that there is no need to measure the output currents, i_{o1} and i_{o2} of the three-level boost converter. They can be calculated using the three-phase grid currents and switching states of the NPC inverter (refer to Table 7.1). This is demonstrated as follows:

$$\begin{aligned} i_{o1} = i_p &= S_{1a}S_{2a} \cdot i_{ag} + S_{1b}S_{2b} \cdot i_{bg} + S_{1c}S_{2c} \cdot i_{cg} \\ i_{o2} = i_p + i_z &= S_{1a}S_{2a} \cdot i_{ag} + S_{1b}S_{2b} \cdot i_{bg} + S_{1c}S_{2c} \cdot i_{cg} \\ &\quad + \bar{S}_{1a}S_{2a} \cdot i_{ag} + \bar{S}_{1b}S_{2b} \cdot i_{bg} + \bar{S}_{1c}S_{2c} \cdot i_{cg}. \end{aligned} \quad (7.10)$$

The currents i_p and i_z are shown in Fig. 7.2. From the continuous-time system described in (7.9), the discrete-time model for the three-level boost converter can be derived as:

$$\begin{aligned} \begin{bmatrix} i_{dc}(k+1) \\ v_{c1}(k+1) \\ v_{c2}(k+1) \end{bmatrix} &= \begin{bmatrix} \phi_{11} & \phi_{12}(1-S_{1t}) & \phi_{13}(1-S_{2t}) \\ \phi_{21}(1-S_{1t}) & \phi_{22} & \phi_{23} \\ \phi_{31}(1-S_{2t}) & \phi_{32} & \phi_{33} \end{bmatrix} \begin{bmatrix} i_{dc}(k) \\ v_{c1}(k) \\ v_{c2}(k) \end{bmatrix} \\ &+ \begin{bmatrix} \gamma_{11} & \gamma_{12} & \gamma_{13} \\ \gamma_{21} & \gamma_{22} & \gamma_{23} \\ \gamma_{31} & \gamma_{32} & \gamma_{33} \end{bmatrix} \begin{bmatrix} v_{in}(k) \\ i_{o1}(k) \\ i_{o2}(k) \end{bmatrix}. \end{aligned} \quad (7.11)$$

Since the continuous-time parameter matrix \mathbf{A} contains the switching signals of the boost converter, the discrete-time conversion is not straight forward. The gating signals S_{1t} and S_{2t} are set to zero during the process of discrete-time conversion.

$$\begin{aligned} \begin{bmatrix} \phi_{11} & \phi_{12} & \phi_{13} \\ \phi_{21} & \phi_{22} & \phi_{23} \\ \phi_{31} & \phi_{32} & \phi_{33} \end{bmatrix} &= e^{\tilde{\mathbf{A}}T_s} \\ \begin{bmatrix} \gamma_{11} & \gamma_{12} & \gamma_{13} \\ \gamma_{21} & \gamma_{22} & \gamma_{23} \\ \gamma_{31} & \gamma_{32} & \gamma_{33} \end{bmatrix} &= \tilde{\mathbf{A}}^{-1}(e^{\tilde{\mathbf{A}}T_s} - \mathbf{I}_{3 \times 3})\mathbf{B} \end{aligned} \quad (7.12)$$

where

$$\tilde{\mathbf{A}} = \begin{bmatrix} -\frac{R_{dc}}{L_{dc}} & -\frac{1}{L_{dc}} & -\frac{1}{L_{dc}} \\ \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 \end{bmatrix}. \quad (7.13)$$

From (7.11), it can be established that using the measured and estimated quantities in k^{th} instant $[i_{dc}(k), v_{c1}(k), v_{c2}(k), v_{in}(k), i_{o1}(k), i_{o2}(k)]$ and 4 possible switching states, the future behavior of the dc inductor current $[i_{dc}(k+1)]$ and dc-link capacitor voltages $[v_{c1}(k+1), v_{c2}(k+1)]$ can be obtained. In contrast to the NPC rectifier, with the proposed configuration, the number of switching states are decreased from 27 to 4, leading to a lower computational burden. Moreover, the proposed approach does not require the model of PMSG and wind turbine, and thus the complexity of modeling and control is greatly simplified compared to the BTB NPC converters.

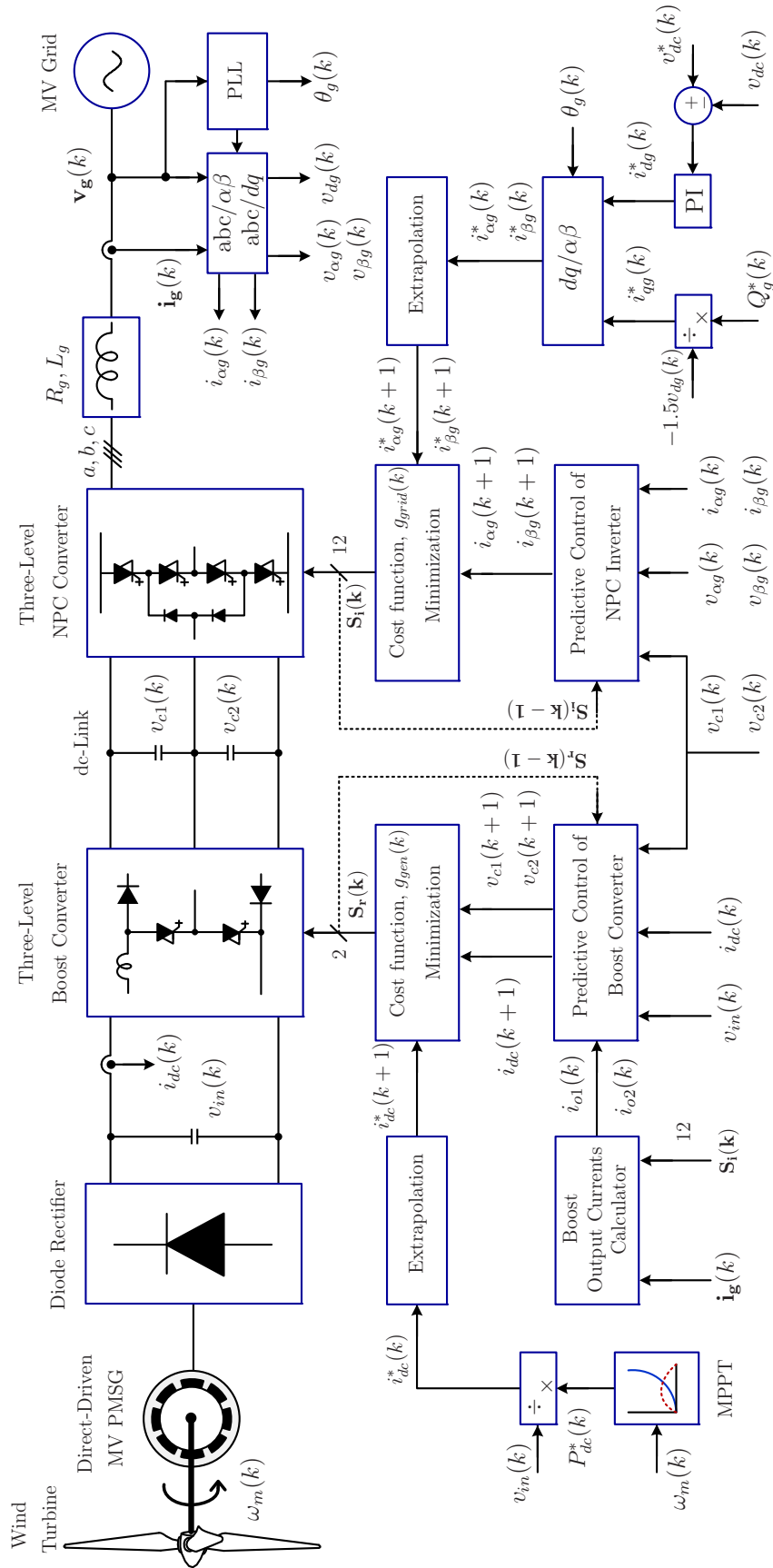


Figure 7.4: Proposed model predictive control scheme for three-level boost and NPC converter based PMSG-WECS.

7.2 Control System for Proposed PMSG-WECS

The complete control system for the proposed PMSG-WECS is shown in Fig. 7.4. Two individual control loops are developed due to the decoupled nature of the TLB converter and the NPC inverter.

7.2.1 Predictive Control of Three-Level Boost Converter

From the TLB converter perspective, the dc-link is treated as a constant voltage source, as the net dc-bus voltage is well controlled by the grid-tied NPC inverter. With this condition, the PMSG stator current, and thus the electromagnetic torque, can be regulated by controlling the gating signals for the TLB converter. A step-by-step procedure for the generation of TLB gating signals is given as follows:

- The first step in the implementation of a control system for the TLB converter is to develop the MPPT algorithm. To enable the variable speed operation of WECS, MPPT algorithm is used. In this paper, an optimum power control MPPT algorithm [47] is employed. The advanced, efficient and sophisticated MPPT algorithms proposed in literature can be readily applied to this TLB converter to increase the WECS efficiency.
- Develop a look-up table containing the generator mechanical speed (ω_m) versus output power reference ($P_{dc}^* \propto \omega_m^3$) using the rated turbine parameters.
- Measure $\omega_m(k)$ with the help of shaft encoders and compute $P_{dc}^*(k)$ using the look-up table designed in the previous step.
- The input power to the TLB converter is a product of the input dc voltage and dc-inductor current ($P_{dc} = v_{in} \cdot i_{dc}$). By dividing the input power reference [$P_{dc}^*(k)$] with the measured input voltage [$v_{in}(k)$], the reference dc-inductor current can be obtained [$i_{dc}^*(k) = P_{dc}^*(k)/v_{in}(k)$]. With the varying wind speed conditions, this reference current changes, and the MPPT operation can be achieved by tracking to this quantity.
- Estimate the future value of the reference dc current, $i_{dc}^*(k+1)$ using the fourth-order Lagrange extrapolation induced in Section 3.3.4.

$$i_{dc}^*(k+1) = 4i_{dc}^*(k) - 6i_{dc}^*(k-1) + 4i_{dc}^*(k-2) - i_{dc}^*(k-3). \quad (7.14)$$

- Develop an initialization file containing the parameter matrices Φ and Γ .
- Measure the three-phase grid currents and NPC inverter gating signals during the k^{th} sampling instant. Estimate $i_{o1}(k)$ and $i_{o2}(k)$ using (7.10).
- Measure $i_{dc}(k)$, $v_{c1}(k)$, $v_{c2}(k)$ and $v_{in}(k)$. By using (7.11), obtain the future behavior of the inductor current $[i_{dc}(k+1)]$ and dc-link capacitor voltages $[v_{c1}(k+1)$ and $v_{c2}(k+1)]$.
- Define a cost function for the TLB converter as follows by incorporating its control objectives:

$$\begin{aligned}
g_{gen}(k) = & [i_{dc}^*(k+1) - i_{dc}(k+1)]^2 \\
& + \lambda_{dc,b} * [v_{c1}(k+1) - v_{c2}(k+1)]^2 \\
& + \lambda_{swc,b} * \sum_{j=1,2} |S_{jt}(k) - S_{jt,op}(k)|
\end{aligned} \tag{7.15}$$

where $\lambda_{dc,b}$ and $\lambda_{swc,b}$ are weighting factors for the dc-link capacitor voltages balancing and switching frequency reduction, respectively. $S_{1t}(k)$ and $S_{2t}(k)$ are the predicted gating signals. $S_{1t,op}(k) = S_{1t}(k-1)$ and $S_{2t,op}(k) = S_{2t}(k-1)$ are the optimal gating signals in the previous sample.

- During each sampling instant, the switching signals $S_{1t}(k)$ and $S_{2t}(k)$, which minimize the cost function (7.15), are chosen and applied to the TLB converter directly. It should be noted that the linear regulators and PWM modulator are eliminated with the proposed approach.

In (7.15), the primary control goal is to force the inductor current to follow its reference, and thus the weighting factor associated with this term is 1. The secondary goal is to balance the dc-link capacitor voltages. A weighting factor $\lambda_{dc,b}$ is defined such that the importance for the secondary goal can be adjusted according to the desired performance. When $\lambda_{dc,b} = 1$, the secondary goal will be given equal importance compared to the primary goal, and thus a very good balancing of the dc-link capacitor voltages can be obtained, but at the expense of a higher inductor current tracking error. When $\lambda_{dc,b} = 0$, the dc-link capacitor voltages are not controlled, but the inductor current shows excellent reference tracking. Unfortunately, in the state-of-the-art predictive control, no analytical or numerical methods are available for the calculation of weighting factor values, but the guidelines given in [247] can be used.

The best approach is to select $\lambda_{dc,b} = 1$ in the initial trial, and reduce this value in small steps until the drift in capacitor voltages reach 2% of its nominal dc-link voltage.

Another secondary goal is switching frequency minimization. Its importance can be altered by changing the $\lambda_{swc,b}$ value. When $\lambda_{swc,b} > 0$, the switching frequency reduction can be obtained, but at the expense of a higher inductor current tracking error and drift in capacitor voltages. The cost function in (7.15) includes more than one control goal, and under such conditions the quadratic cost function gives better performance than the absolute cost function [77].

7.2.2 Predictive Control of NPC Inverter

From the NPC inverter perspective, the dc-link is treated as a variable dc current source whose magnitude is proportional to the active power extracted from the wind. Under these conditions, the net dc-bus voltage and reactive power to the grid can be regulated by properly generating the gating signals for the grid-tied NPC inverter [81]. The control system implementation procedure is as follows:

- Measure the grid voltages, currents and dc-link capacitor voltages, and estimate the grid voltage angle, θ_g using a SRF phase-locked loop (SRF-PLL) using guidelines given in Appendix B.4.
- Convert measured grid voltages and currents to $\alpha\beta$ and dq frames.
- Generate i_{dg}^* and i_{qg}^* from v_{dc}^* and Q_g^* loops, respectively. More details about the definition of grid-side reference control variables can be found in Chapter 5.
- Convert the SRF references (i_{dg}^* and i_{qg}^*) to stationary frame ($i_{\alpha g}^*$ and $i_{\beta g}^*$) using the grid voltage angle θ_g .
- Estimate the future value ($k+1$) of reference grid currents as shown below. The vector angle extrapolation introduced in the Chapter 3 is used here.

$$\begin{bmatrix} i_{\alpha g}^*(k+1) \\ i_{\beta g}^*(k+1) \end{bmatrix} = e^{j\omega_g T_s} \begin{bmatrix} i_{\alpha g}^*(k) \\ i_{\beta g}^*(k) \end{bmatrix} \quad (7.16)$$

where ω_g is grid angular frequency.

- Using the measured quantities and off-line computed C_v and C_i values, predict the future behavior of $\alpha\beta$ grid currents during each iteration according to (7.3).
- The grid-side cost function, developed so that control goals could be met, is defined as follows:

$$g_{grid}(k) = [i_{\alpha g}^*(k+1) - i_{\alpha g}(k+1)]^2 + [i_{\beta g}^*(k+1) - i_{\beta g}(k+1)]^2 + \lambda_{swc,i} * \sum_{j=1, 2} \sum_{x=a,b,c} |S_{jx}(k) - S_{jx,op}(k)| \quad (7.17)$$

where $\lambda_{swc,i}$ is the weighting factor for switching frequency reduction of the NPC inverter.

- During each iteration, the predicted variables are compared with the extrapolated references. The switching state (among 27) which minimizes the cost function is chosen and applied to the NPC inverter gating terminals during the next sampling interval.

The selection of the weighting factor and cost function type for the NPC inverter is similar to the TLB converter presented earlier. Compared to the works in [80, 81, 279, 280, 299], the grid-side cost function here deals with one primary objective (reference tracking of grid currents) and one secondary objective (switching frequency minimization) only. The dc-link capacitor voltages are not considered in the inverter cost function. Since the cost function has fewer numbers of objectives, the computational burden becomes lower. The selection of the best switching state (among 27) becomes easier and more straightforward (without any weighting factor designs for the dc-link capacitor voltages unlike in [80, 81, 279, 280, 299]). The quality of the primary control goal (reference tracking) greatly improves as the number of secondary control goals is reduced.

The analysis presented here is also applicable for the classical control techniques which utilize space vector modulation (SVM). The selection of the closest vector in the SVM method is decided according to the minimal value of the cost function [183]. Since the dc-link capacitor voltages do not need to be controlled by the SVM, the output power quality of the NPC inverter can be greatly enhanced. Instead of SVM, a simplified pulse width modulation can also be employed for the NPC inverter. The performance comparison of the proposed predictive controller with the simplified SVM and PWM methods will be considered as part of future work.

7.3 Simulation Results

The power converter topology and control scheme given in Figs. 7.1 and 7.4 are simulated in MATLAB/Simulink environment with the 3 MW/3000 V/577 A WECS parameters as indicated in Table 7.2. The PMSG is assumed to have surface mount magnets by which $L_d = L_q$. A one-step prediction horizon is considered in all the simulation tests.

Table 7.2: Parameters of the proposed wind energy conversion system

Variable	Description	Simulation		Experimental	
		SI	p.u.	SI	p.u.
Permanent Magnet Synchronous Generator Parameters					
P_m	Rated Mechanical Power (kW)	3000		3.6	
v_{sl}	Rated Line-Line Voltage (V)	3000		208	
v_s	Rated Phase Voltage (V)	1732.2	1.0	120.1	1.0
i_s	Rated Stator Current (A)	582	1.0	10	1.0
f_s	Rated Stator Frequency (Hz)	9.75	1.0	20	1.0
PF_s	Rated Power Factor	0.98		0.98	
n_m	Rated Rotor Speed (rpm)	22.5	1.0	150	1.0
PP	Number of Pole Pairs	26		8	
T_m	Rated Mechanical Torque (kN.m)	1273.24	1.0	0.2292	1.0
λ_r	Rated rms Rotor Flux Linkage (Wb)	28.059	1.0	0.956	1.0
R_s	Stator Winding Resistance (m Ω)	37.521	0.013	245	0.021
L_d	d -axis Synchronous Inductance (mH)	9.75	0.2	19.1	0.2
L_q	q -axis Synchronous Inductance (mH)	9.75	0.2	19.1	0.2
Medium Voltage Grid Parameters					
S_g	Rated Apparent Power (kVA)	3000	1.0	3.6	1.0
v_{gl}	Rated Line-Line Voltage (V)	3000		208	
v_g	Rated Phase Voltage (V)	1732.2	1.0	120.1	1.0
i_g	Rated Stator Current (A)	577.35	1.0	10	1.0
f_g	Rated Stator Frequency (Hz)	60	1.0	60	1.0
Z_{bg}	Base Impedance (Ω)	3	1.0	12.018	1.0
L_{bg}	Base Inductance (mH)	7.96	1.0	31.88	1.0
C_{bg}	Base Capacitance (μ F)	884.19	1.0	220.72	1.0
Rectifier and Inverter Parameters					
C_{in}	Input dc-link Capacitance (μ F)	38937	7.40	4700	7.40
C_{dc}	Output dc-link Capacitance (μ F)	4006	4.53	1000	4.53
R_{dc}	Boost Filter Leakage Resistance (Ω)	0.3	0.01	0.12	0.01
L_{dc}	Boost Filter Inductance (mH)	7.5	0.94	30	0.94
R_g	Grid-side Filter Resistance (Ω)	0.027	0.009	0.108	0.009
L_g	Grid-side Filter Inductance (mH)	1.65	0.207	6.6	0.207
Controller Parameters					
T_s	Sampling Time (s)	100 μ		100 μ	
$\lambda_{dc,b}$	Weighting Factor	0.1		0.1	
$\lambda_{sw,b}$	Weighting Factor	100		1.5	
$\lambda_{sw,i}$	Weighting Factor	100		0.05	
v_{dc}^*	Reference dc-bus Voltage (V)	5304	3.062	367	3.062
$k_{P,dc}$	DC-link Controller Proportional Gain	1		1	
$k_{I,dc}$	DC-link Controller Integral Gain	200		200	

Figs. 7.5 and 7.6 shows the simulation waveforms with different wind speeds and reactive power references. Initially the wind speed is considered to be 12 m/s (1 p.u.) and the generator operates at its rated speed. The PMSG stator voltage and current waveforms are distorted due to the natural commutation of the diodes. The fundamental components of the stator voltage and current are in-phase (not shown in figure), and thus a unity power factor operation is achieved for the PMSG. The electromagnetic torque, T_e contains ripples due to the harmonics in the generator three-phase currents. The dc-link current, i_{dc} is maintained at its reference value by the boost converter, while the net dc-bus voltage and reactive power are regulated at their reference values by the grid-side inverter. The grid current is noted to be 560 A with a total harmonic distortion (THD) of 2.76 % and the phase angle between the grid voltage and current is zero (not shown in figure) due to the zero reactive power reference. The active power and apparent powers are noted 2.91 MW and 2.91 MVAR, respectively. It is important to note that the rated output of the generator is lower than the mechanical input power (3 MW). During this operating condition, the switching frequencies of the boost converter and NPC inverters are found to be 1400 and 900 Hz, respectively.

At $t = 0.5$ s, a gradual change in wind speed is applied from 12 m/s (1 p.u.) to 10.8 m/s (0.9 p.u.), and the generator speed, generator current, electromagnetic torque and boost converter input voltage settled to a new operating point after short transients. With the changes in the generator speed, the MPPT algorithm generated a new reference for the dc-link current, and the controller forced the dc-link current to track to its reference, meaning that MPPT is obtained with varying wind speed conditions. The grid currents magnitude (409 A with 3.61 % THD) and thus active power (2.13 MW) delivered to the grid are changed according to the reduced wind speed condition. The switching frequencies are 1022 Hz and 890 Hz respectively for the boost converter and NPC inverter.

At $t = 0.7$ s, a step change in Q_g^* is applied from 0 to -2.055 MVAR (-0.685 p.u.). A good transient response is achieved as demonstrated through the grid current and reactive power waveforms. The grid current magnitude, grid current THD, grid power factor and inverter switching frequency are found to be 567 A, 2.67 %, 0.73 leading, and 840 Hz, respectively. The boost converter switching frequency is unchanged (1022 Hz). The grid current leads the grid voltage by 43.22° . The grid apparent power ($S_g = \sqrt{P_g^2 + Q_g^2}$) is noted to be 2.96 MVA.

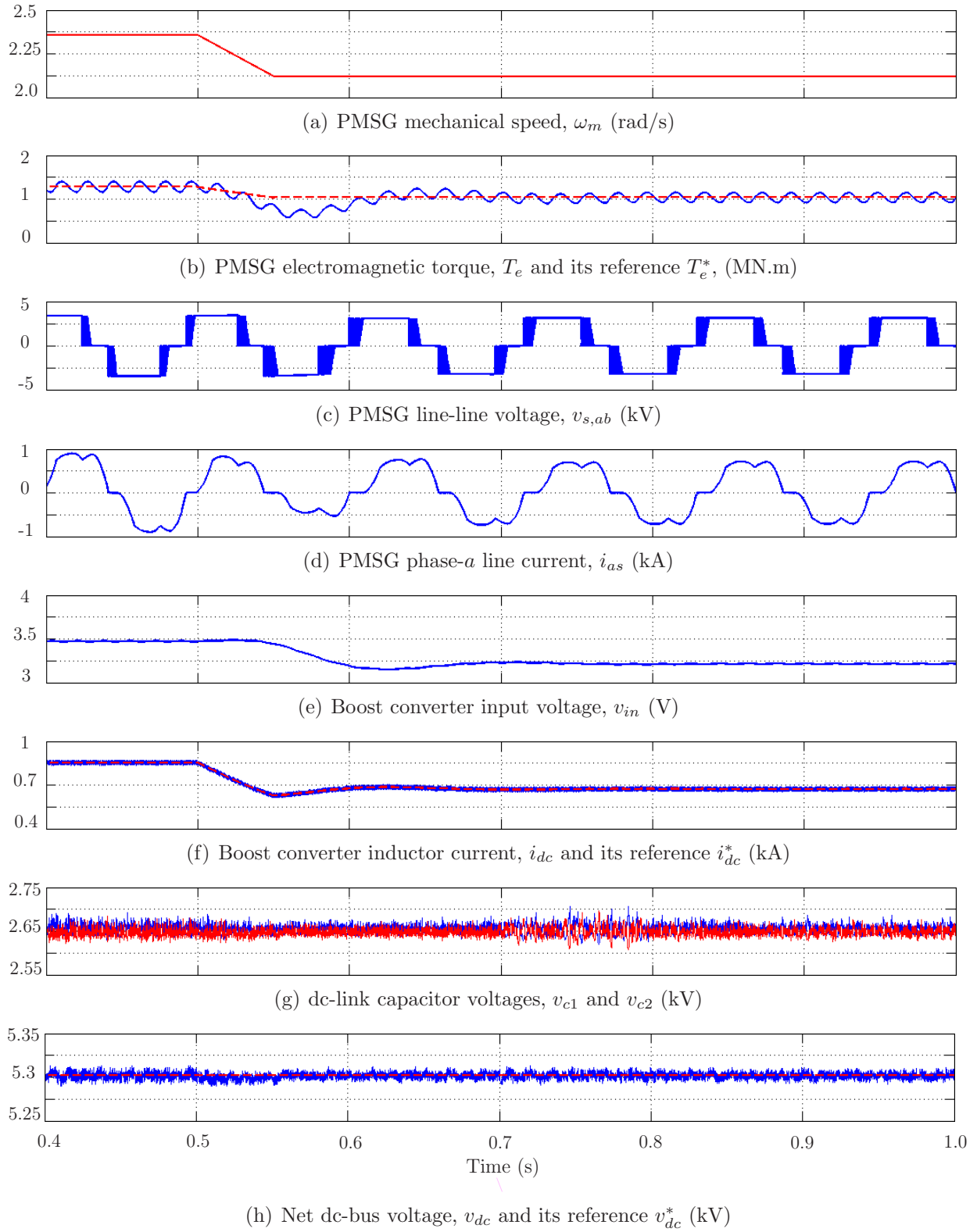


Figure 7.5: Simulation results with step change in wind speed and programmed changes in reactive power reference (first part of figure).

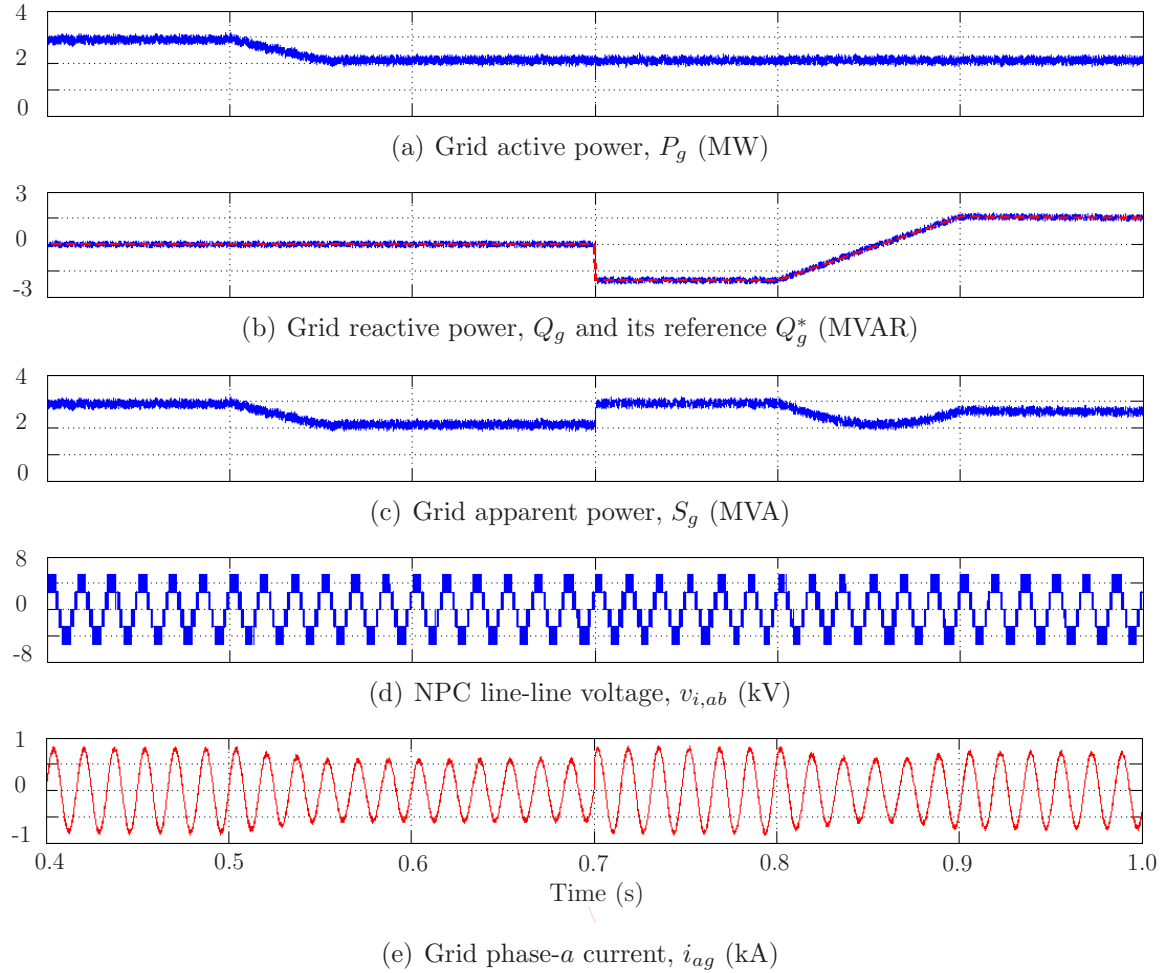


Figure 7.6: Simulation results with step change in wind speed and programmed changes in reactive power reference (second part of figure).

From 0.8 to 0.9 s, the Q_g^* value is changed linearly from -2.055 MVAR (-0.685 p.u.) to 1.584 MVAR (0.528 p.u.), and during this interval the net dc-bus voltage and reactive power are regulated at their reference values, and this operation demonstrates an excellent transient response of the proposed predictive controller. From $t = 0.9$ s onwards, the Q_g^* value is maintained at 1.584 MVAR (0.528 p.u.). The grid current magnitude, grid current THD, grid power factor, inverter switching frequency and grid apparent power are found to be 511 A, 3.25 %, 0.81 lagging, 784 Hz, and 2.65 MVA, respectively.

During all the operating conditions including transient conditions: (a) the dc-link current tracks to its reference, (b) the dc-link capacitor voltages are very well-balanced, (c) the net dc-bus is maintained at its reference value, and (d) reactive power is supplied as requested by the grid operator.

The capability of the boost converter in balancing the dc-link capacitor voltages is demonstrated in Fig. 7.7. The rated wind speed condition is used. A resistor, R_x (8.32 p.u.) is connected on purpose across the dc-link capacitor C_1 at time $t = 1/40$ s. The dc-link capacitor voltages are shown in Fig. 7.7(a) and perfect balancing is noticed even with the perturbations in the dc-link. The predictive controller operates with a sampling time of $100 \mu\text{s}$ and the control action has been taken in a few sampling instants. With the proposed controller, no transients are noticed. The current through the parallel resistor is shown in Fig. 7.7(b), and its value is noted as 106 A (0.184 p.u.). As shown in Fig. 7.7(c), the three-phase grid currents continue to track to their references even with the parallel resistor. Due to the power dissipated in the resistor R_x (282 kW), the magnitude of the current delivered to the grid is decreased. This test verifies that the proposed three-level boost converter performs very well in controlling the neutral-point voltage.

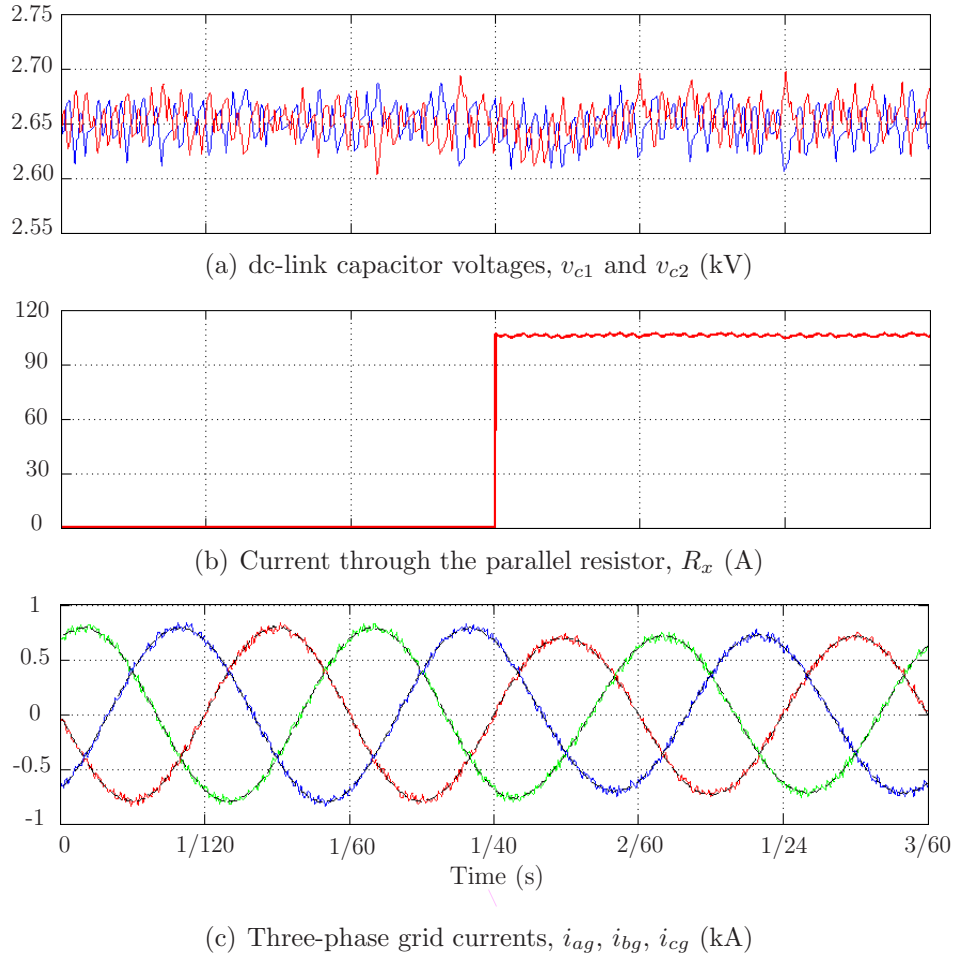


Figure 7.7: Simulation results for capacitor voltages balancing with a resistor across C_{dc1} .

The comparison between the proposed topology and back-to-back (BTB) connected NPC converters topology equivalent during inverter switching frequency minimization is presented in Figs. 7.8 and 7.9. For these topologies, rated wind speed and zero reactive power condition is considered. The simulation results, with the BTB NPC topology, is presented in Fig. 7.8. In the BTB NPC topology, the grid-tied NPC inverter performs three jobs: (a) control of the net dc-bus voltage, (b) balancing of dc-link capacitors, and (c) reactive power regulation. To derive an equivalent topology for the BTB NPC converters, the control algorithm given in Fig. 7.4 is modified in such a way that the balancing of the dc-link capacitor voltages is achieved by the grid-tied NPC inverter (in addition to the reference current tracking and switching frequency minimization), and the weighting factor $\lambda_{dc,b}$ is set to zero. This is also the case with the standard two-level boost converter + NPC inverter based WECS [125,300]. For the balancing of the dc-link capacitor voltages with the help of the NPC inverter, the methodology presented in [279] is used.

At time $t = 2/60$ s, the weighting factor for switching frequency minimization, $\lambda_{sw,i}$ is changed from 0 to 5500, and with this the f_{sw} is changed from 1190 to 385 Hz. This can be noticed by looking into the number of switch changes in the inverter line-line voltage waveform [Fig. 7.8(ii)]. With the introduction of switching frequency minimization terms to the cost function, two other variables (balancing of dc-link capacitor voltages and reference tracking) are affected, as seen in Figs. 7.8(i) and (iii). The grid current THD with $\lambda_{sw,i} = 0$ and $\lambda_{sw,i} = 5500$ are 3.16 % and 6.64 %, respectively. The fast Fourier transform (FFT) of phase-*a* grid current is shown in Fig. 7.8(iv). The harmonics are spread over the whole FFT window with a peak magnitude of 2.5 % of the fundamental component.

The simulation results with the proposed topology are shown in Fig. 7.9, where perfect balancing of the dc-link capacitor voltages is achieved, irrespective of the NPC inverter switching frequency minimization. With the change in the weighting factor $\lambda_{sw,i}$ from 0 to 5000, the NPC inverter switching frequency is decreased from 1169 to 385 Hz and the grid current THD is increased from 2.63 % to 4.82 %. These values are lower compared to the one obtained by the BTB NPC topology. The peak magnitude of the harmonics is also lower compared to the BTB NPC topology, as shown in Fig. 7.9(iv). The cost function for the NPC inverter of the proposed topology includes only the reference tracking and switching frequency minimization, and thus better performance is achieved in terms of dc-link capacitor voltages balancing and grid current quality.

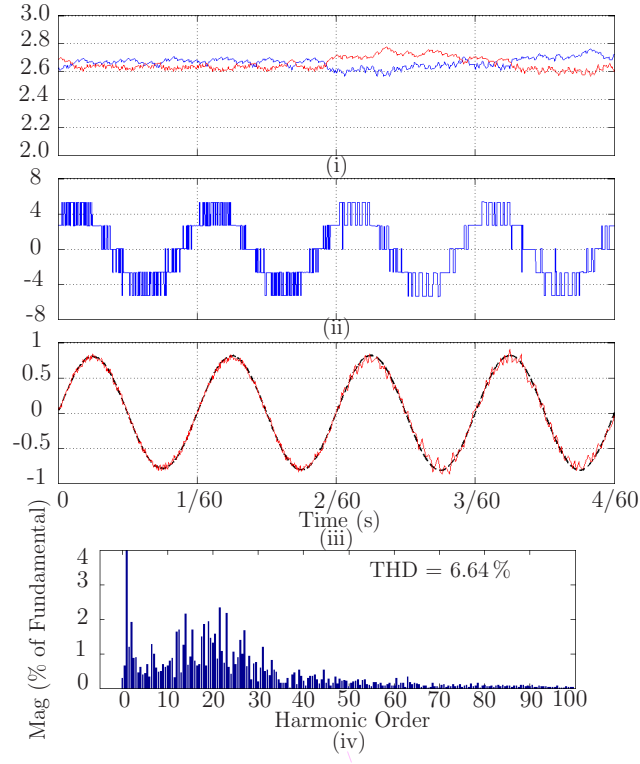


Figure 7.8: Simulation results for NPC f_{sw} minimization with BTB NPC converters.

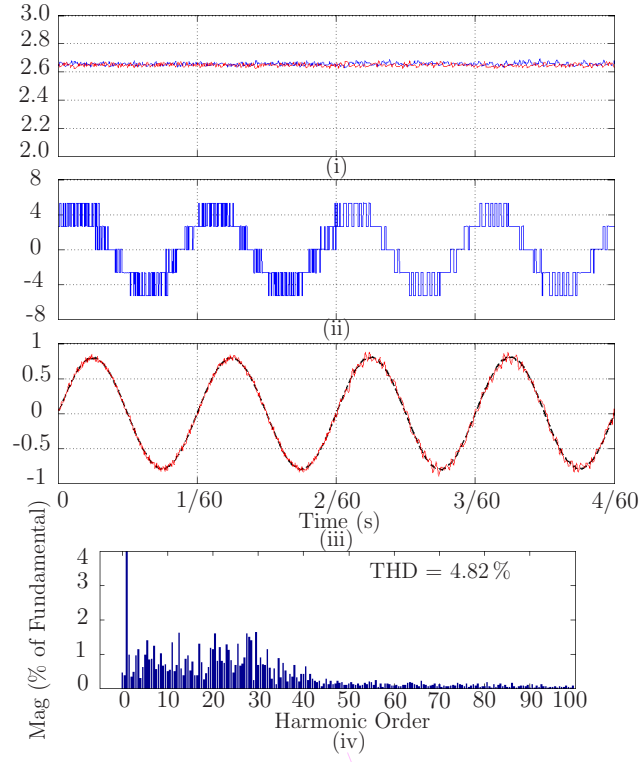
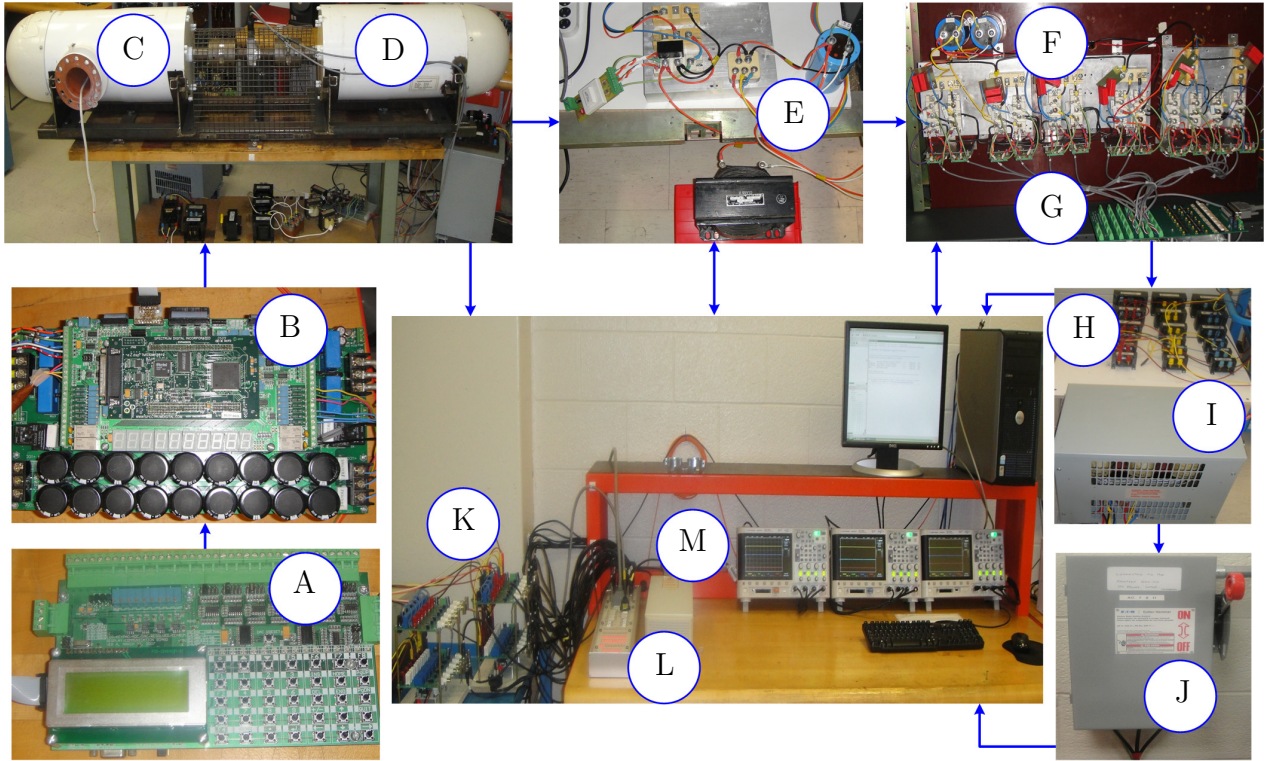


Figure 7.9: Simulation results for NPC f_{sw} minimization with proposed topology.

7.4 Experimental Implementation and Validation

As shown in Fig. 7.10, a low power prototype of PMSG-WECS using the proposed power converters has been developed. The complete system parameters are indicated in Table 7.2 which are the same simulation parameters except for the generator frequency and stator winding resistance. Two mechanically coupled PMSGs are used. The first PMSG along with the DSP/FPGA controller is used as a prime mover to provide the required speed to the second PMSG. The TLB converter and NPC inverter are controlled by a dSPACE DS1003 rapid prototyping board. The MATLAB/Simulink, Real-Time Workshop and dSPACE Control Desk are used together to handle the control algorithm. The prototype has been built by Semikron SKM75GB123D dual-pack IGBT modules, SKKD75F12 dual-pack diode modules and SKHI22B dual core gate drivers. The inverter is connected to the grid through an isolation transformer and its impedance is added to the filter values.



(A) keyboard, (B) DSP/FPGA based wind turbine simulator, (C) prime mover, (D) direct-driven PMSG, (E) diode rectifier and three-level boost converter, (F) NPC inverter, (G) interface board, (H) L filter, (I) isolation transformer, (J) three-phase grid, (K) voltage and current sensors, (L) DS1103 R&D controller and CP1103 connector, and (M) Oscilloscopes.

Figure 7.10: Block diagram of the experimental setup.

In the experimental verification, the computational delay caused by the digital signal processor is compensated for by calculating the cost functions at $(k + 2)$ instant. The switching states which minimize the cost functions at $(k + 2)$ instant are selected and applied at sampling instant $(k + 1)$. With this approach, one sampling period will be available for calculations. The control algorithms with this approach using delay compensation are shown in Fig. 7.11.

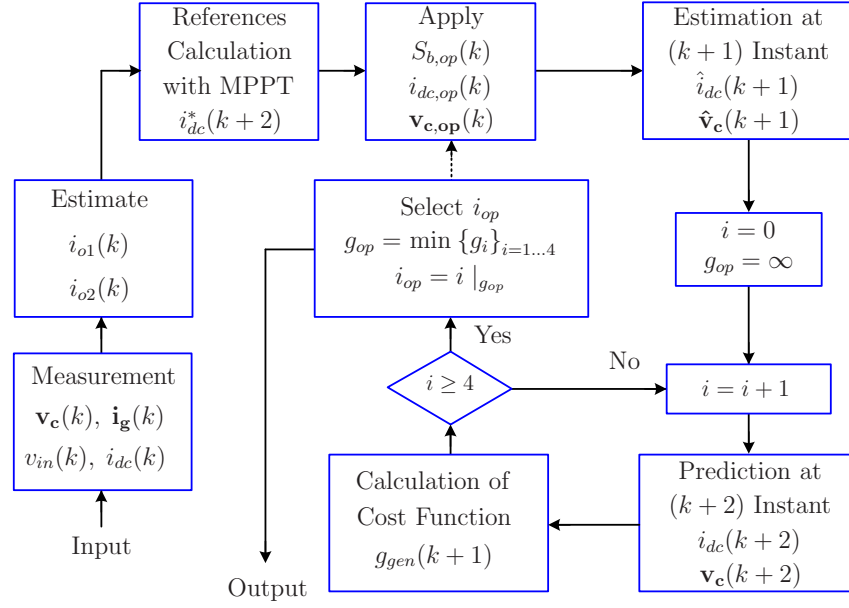
The experimental results with the variation in generator speed from 1 to 0.9 p.u. are presented in Fig. 7.12(a), where the response of the system is noted to be similar to the simulation results presented in Figs. 7.5 and 7.6. The grid current, its THD, f_{sw} of boost converter and inverter during (1 p.u.) and (0.9 p.u.) wind speeds are: (9.0 A, 3.84 %, 1550 Hz, 995 Hz) and (6.6 A, 4.73 %, 1150 Hz, 953 Hz), respectively. The f_{sw} is higher than in simulations due to the delay compensation method employed [81, 248].

The reactive power reference tracking capability and good transient response of the proposed controller is demonstrated in Fig. 7.12(b). The grid current, its THD, power factor, f_{sw} of inverter during (-0.685 p.u.) and (0.528 p.u.) Q_g^* are noted as: (9.1 A, 3.38 %, 0.73 leading, 910 Hz) and (8.3 A, 4.52 %, 0.81 lagging, 790 Hz), respectively. The capacitor voltages are well balanced during all the operating conditions in addition to the reference tracking.

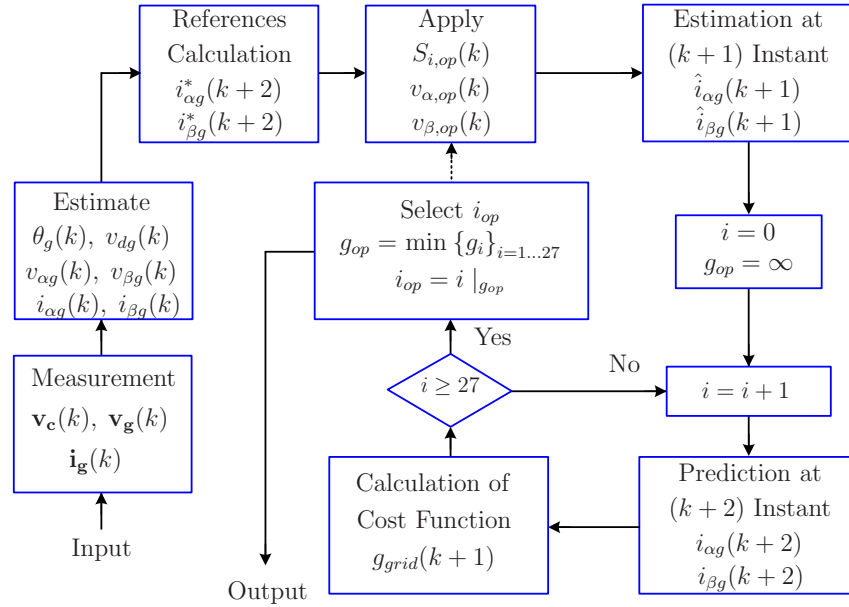
The effect of the dc-link perturbations on the performance of a three-level boost converter is investigated experimentally and presented in Fig. 7.13. The dc-link capacitor voltages are well balanced by the three-level boost converter, irrespective of the step-connection of 100 Ω resistor (8.32 p.u.). The transient duration is noted to be 5 ms only. The grid currents magnitude is decreased, but they continue to track to their references.

The inverter switching frequency minimization and its impact on the dc-link capacitor voltages is experimentally verified with the proposed topology and presented in Fig. 7.14. The experimental weighting factor $\lambda_{sw,i}$ is changed from 0 to 1.2, and the (f_{sw}) and (THD of grid currents) is changed to (1055 Hz to 394 Hz) and (3.11 % to 5.45 %), respectively. As shown in Fig. 7.14, the dc-link capacitor voltages, which are controlled by the boost converter, are not affected by the inverter switching frequency reduction algorithm.

The NPC inverter line-line voltage waveform, as demonstrated in Figs. 7.12(a), 7.12(b) and 7.14 contain five levels, whereas a 2L inverter (Fig. 2.4) produces three-levels [84]. The increase in the number of output voltage levels from 3 to 5 leads to smaller voltage



(a)

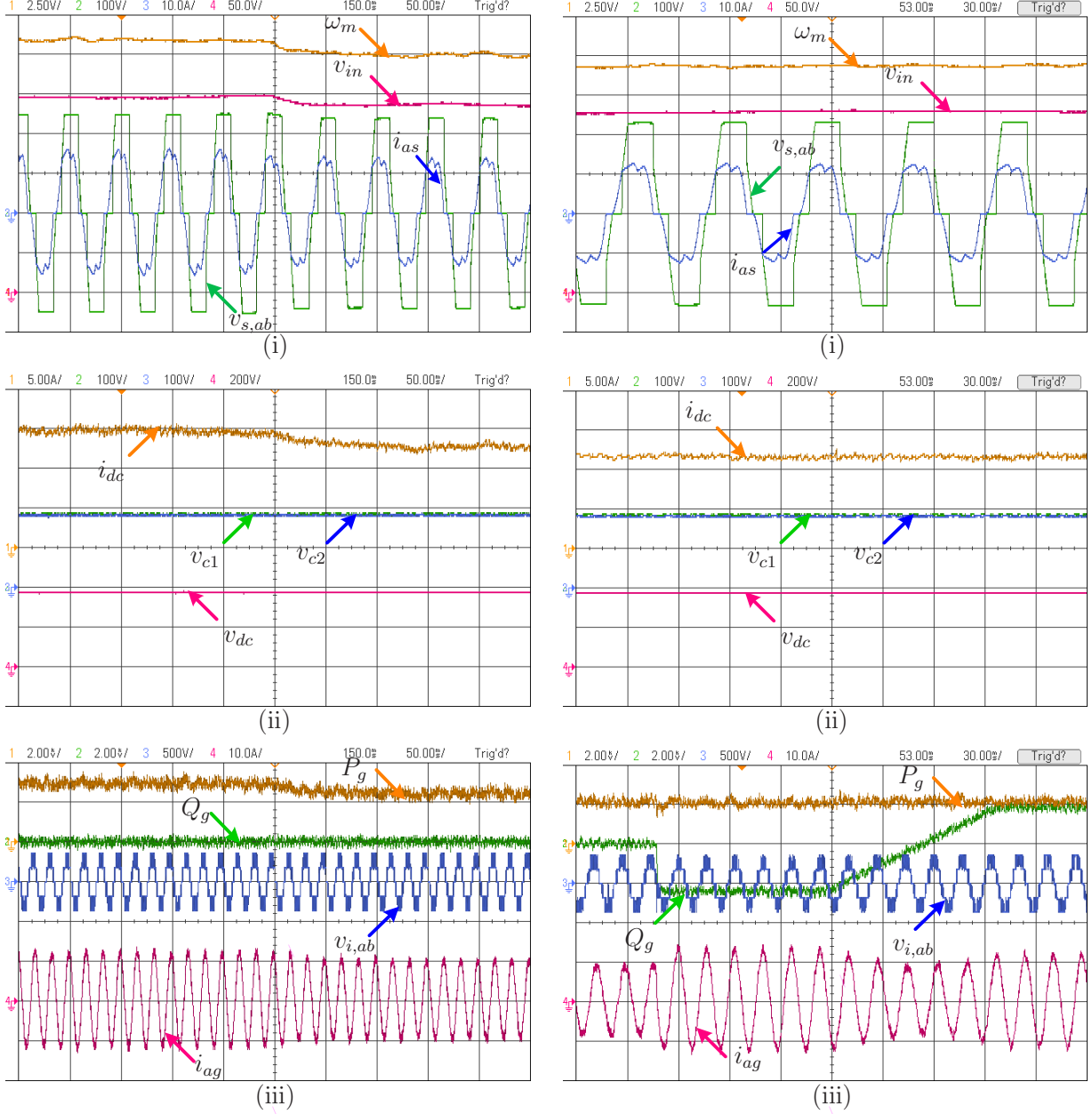


(b)

Figure 7.11: Proposed predictive control algorithm with delay compensation for: (a) TLB converter, and (b) NPC inverter.

steps and thus lower dv/dt . Moreover, with the NPC inverter, the output current ripple becomes 4 times lower compared to the 2L-inverter for the same device-switching frequency [62]. For a given value of the grid-side filter, this reduction in the current ripple leads to very good power quality. In other words, the 2L inverter requires a large, grid-side filter to achieve a power quality which is comparable to the NPC inverter. Many scholarly works

have been presented in recent years focusing on the multilevel operation of the grid-side inverter [60, 80, 81, 123, 128]. A different inverter configuration was proposed such as 5L, 7L and 9L ANPC [60, 123], and 5L H-bridge (HB) inverter [128] to achieve smaller voltage steps in the output voltage waveform. Reduction in the grid-side filter size, while improving the grid power quality, represents a common interest in all these works.



(a) Programmed change in ω_m from 1.0 to 0.9 p.u.

(b) Programmed change in Q_g^*

Figure 7.12: Experimental results for programmed changes in ω_m and Q_g^* .

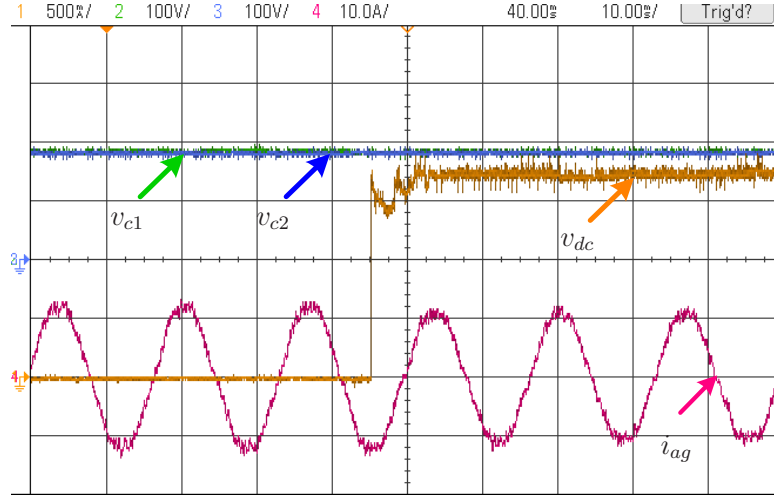


Figure 7.13: Experimental results for capacitor voltages balancing with a resistor across C_{dc1} .

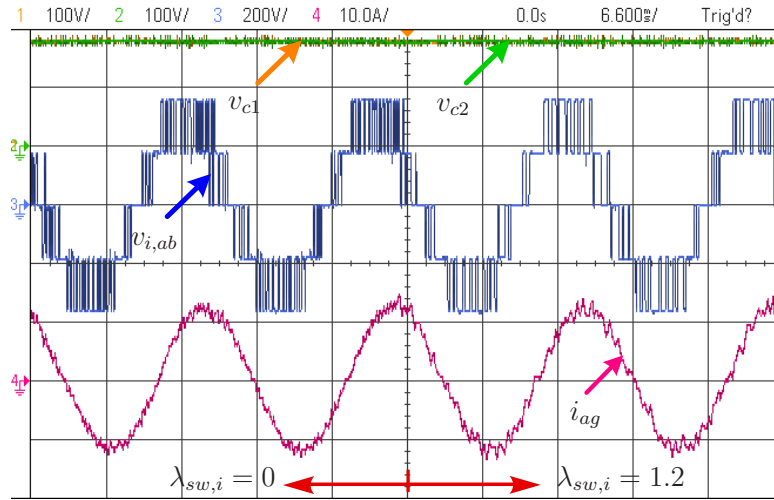


Figure 7.14: Experimental results for inverter switching frequency minimization.

The proposed TLB converter has many potential applications and possible extensions to use in MV-WECS. Since the output of the TLB converter directly fits the dc-link capacitors, different inverter configurations can be developed on the grid-side with reduced control complexity. The 5L to 9L ANPCs introduced in [60, 123] have two split dc-link capacitors similar to the NPC inverter. By using these ANPCs in conjunction with the TLB converter, the grid current quality can be improved further (this is true with the predictive control or classical control based on SVM/PWM).

7.5 Conclusion

A novel medium voltage power converter topology, consisting of a diode rectifier, three-level boost converter and neutral-point-clamped inverter is proposed for high power PMSG-WECS. The proposed configuration combines the advantages of passive generator-side converters and grid-side multilevel operation. Compared to the BTB-NPC converters, the proposed configuration uses less number of active switches and thus the overall cost and control system complexity is lower. The added benefit of this configuration is that the dc-link capacitor voltages are balanced during all operating conditions by the TLB converter, and thus there is no need to develop a complex control system for the NPC inverter to handle the dc-link capacitor voltages balancing task.

A model predictive control strategy is proposed to control the complete wind energy system. Compared to the BTB-NPC converters, with the proposed topology, the number of switching states is decreased from 54 to 31, and thus a lower computational burden has been accomplished. Using the discrete-time model of the system, two individual control loops are developed, and they generate the gating signals to the TLB converter and NPC inverter based on minimization of cost functions. The use of linear controllers and modulation stage are eliminated with the proposed FCS-MPC strategy, and as a result, good dynamic response has been obtained. The MPPT and neutral point voltage are effectively controlled by the TLB converter, while net dc-bus voltage and reactive power are regulated by the NPC inverter. Because of the control freedom for the NPC inverter, a significant improvement in the grid power quality has been achieved. Through the simulation and experimental results, it has been demonstrated that the FCS-MPC strategy performs very well in achieving the control goals for the complete wind energy system.

Chapter 8

Predictive Control of Four-Level Converters Based PMSG-WECS

Considering the state-of-the-art wind energy market and its trend towards medium voltage (MV) technology, the initiative of this work is to combine passive generator-side converters with the grid-side multilevel inverters. To meet the future generation of 1-10 kV class (as defined in [82]) PMSG wind turbines, a four-level diode-clamped inverter (4L-DCI) is proposed at the grid-side. Compared with the 3L-DCI, the 4L-DCI offers many benefits as discussed in Chapters 2, 4 and 5. However, the balancing of dc-link capacitor voltages with the 4L-DCI is much more difficult and complicated compared to the 3L-DCI [83, 84]. To overcome this problem, a four-level boost converter (4L-BC) is proposed, with which the balancing of the dc-link capacitor voltages can be achieved during all the operating conditions.

In this research, the continuous- and discrete-time modeling of the proposed power conversion system is analyzed. To achieve an optimal control performance, a modified two-step model predictive strategy is proposed. The high power wind turbine requirements, such as maximum energy harvesting, balancing of dc-link capacitor voltages, net dc-bus voltage control, regulation of grid reactive power, and minimization of switching frequency and common-mode voltage are expressed as cost functions. Best switching states are chosen and applied to the power converters during each sampling interval based on the minimization of cost functions. The feasibility of the proposed configuration and control scheme are verified through MATLAB/Simulink tests on a high power (5 MVA/4160 V/694A) system and dSPACE experiments on a low power (3.6 kVA/208 V/10 A) prototype.

8.1 Configuration and Modeling of Proposed WECS

The configuration of the proposed variable-speed WECS is shown in Fig. 8.1. The proposed configuration consists of MV-PMSG connected to a low cost three-phase diode bridge rectifier, a dc-dc 4L-boost converter as an intermediate stage, and a 4L-DCI at the grid-side. The output voltage of the diode rectifier changes with respect to the varying wind speed conditions and this represents an unregulated dc-link. A regulated dc-link is used at the inverter terminals to ensure proper operation of the system. The 4L-BC is composed of three active switches and four diodes. The voltage rating of these devices is one third of those used in the standard boost converter, and thus the cost of this 4L-BC is approximately the same as that of a standard boost converter [119]. The 4L-DCI uses 18 active switches and 18 clamping diodes. The active switches can be realized using the MV-IGBT or IGCT. Three capacitors are used in the regulated dc-link, and the total dc-link voltage is divided among these capacitors ($v_{c1} = v_{c2} = v_{c3} = \frac{v_{dc}}{3}$). The regulated dc-link isolates the 4L-BC and 4L-DCI, and thus the operation of one converter does not affect the other. As shall be shown in the following subsections, this feature facilitates easier modeling and control.

8.1.1 Continuous-Time Modeling of Four-Level Inverter

The four-level diode-clamped inverter as grid-interfacing unit needs to control the net dc-bus voltage and reactive power requested by the grid operator. From the detailed modeling presented for the grid-tied inverter in Chapter 5, the synchronous reference frame (SRF) grid currents are expressed in state-space form as follows:

$$\frac{d}{dt} \begin{bmatrix} i_{dg} \\ i_{qg} \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{-R_g}{L_g} & \omega_g \\ -\omega_g & \frac{-R_g}{L_g} \end{bmatrix}}_{\mathbf{P}_i} \begin{bmatrix} i_{dg} \\ i_{qg} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_g} & 0 \\ 0 & \frac{1}{L_g} \end{bmatrix}}_{\mathbf{Q}_i} \begin{bmatrix} v_{di} \\ v_{qi} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{-1}{L_g} & 0 \\ 0 & \frac{-1}{L_g} \end{bmatrix}}_{\mathbf{R}_i} \begin{bmatrix} v_{dg} \\ v_{qg} \end{bmatrix} \quad (8.1)$$

where v_{di} and v_{qi} are SRF inverter voltages and they can be calculated from the three-phase inverter voltages given below:

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = v_{c1} \begin{bmatrix} S_{1a} \\ S_{1b} \\ S_{1c} \end{bmatrix} + v_{c2} \begin{bmatrix} S_{2a} \\ S_{2b} \\ S_{2c} \end{bmatrix} + v_{c3} \begin{bmatrix} S_{3a} \\ S_{3b} \\ S_{3c} \end{bmatrix} \quad (8.2)$$

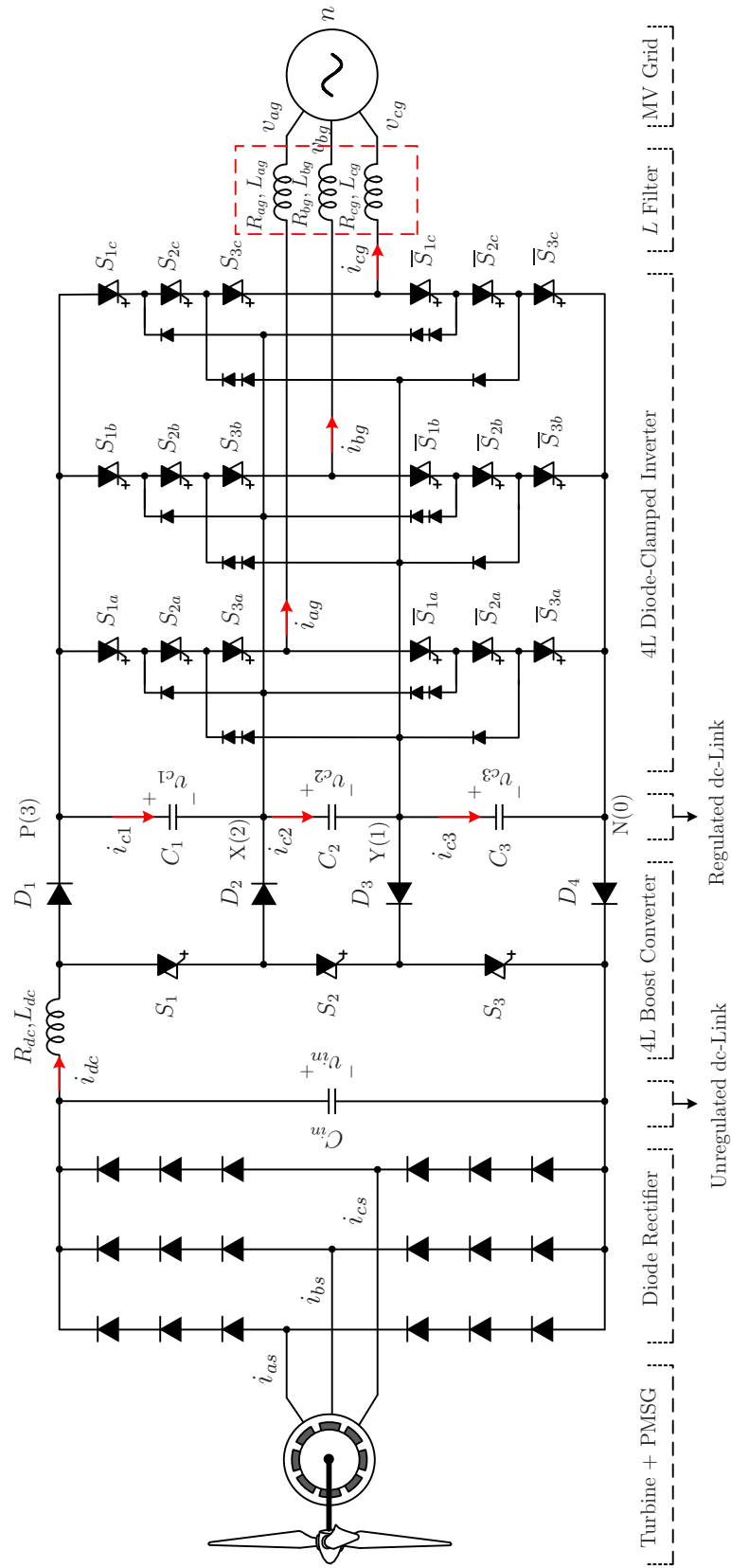


Figure 8.1: Configuration of proposed high power PMSG wind energy system.

where v_{c1} , v_{c2} and v_{c3} are dc-link capacitor voltages. S_{1a} , S_{2a} , S_{3a} , S_{1b} , S_{2b} , S_{3b} , S_{1c} , S_{2c} , and S_{3c} are the switching signals of 4L-DCI.

The common-mode voltage (CMV) can be represented as the voltage between the neutral-point of the grid (n) and the negative dc-rail (N) [276, 301]:

$$v_{nN} = v_{cm} = \frac{v_{aN} + v_{bN} + v_{cN}}{3}. \quad (8.3)$$

The systems in (8.1), (8.2) and (8.3) depict a situation wherein the grid currents and CMV are related to the switching signals. By properly selecting a switching state among 64, the grid currents can be controlled while minimizing the CMV.

8.1.2 Continuous-Time Modeling of Four-Level Boost Converter

The MPPT can be effectively achieved by controlling the inductor current of the four-level boost converter. The dc-link capacitor voltages can also be balanced by the 4L-BC with the proper selection of switching states. To facilitate the controller design, modeling of inductor current and dc-link capacitor voltages is performed in this section.

The model of a standard boost converter is presented in [295] for a single-phase power factor correction application. Similar modeling is performed for the 4L-BC, treating an unregulated dc-link as the input voltage source and the four-level inverter as three virtual resistive loads. As demonstrated in Fig. 8.2, the boost converter operates in five modes [119]. In comparison to the standard boost converter, which operates in mode I and V only, the additional modes help in the charging and discharging of each capacitor. The 4L-BC switching states and the corresponding status of active switches, diodes and capacitors are summarized in Table 8.1. The R_{dc} represents the internal resistance of the inductor L_{dc} .

Table 8.1: Summary of four-level boost converter switching states

Mode	S_1	S_2	S_3	D_1	D_2	D_3	D_4	C_1	C_2	C_3
I	ON	ON	ON	OFF	OFF	OFF	OFF	Discharge	Discharge	Discharge
II	ON	OFF	ON	OFF	ON	ON	OFF	Discharge	Charge	Discharge
III	ON	OFF	OFF	OFF	ON	OFF	ON	Discharge	Charge	Charge
IV	OFF	OFF	ON	ON	OFF	ON	OFF	Charge	Charge	Discharge
V	OFF	OFF	OFF	ON	OFF	OFF	ON	Charge	Charge	Charge

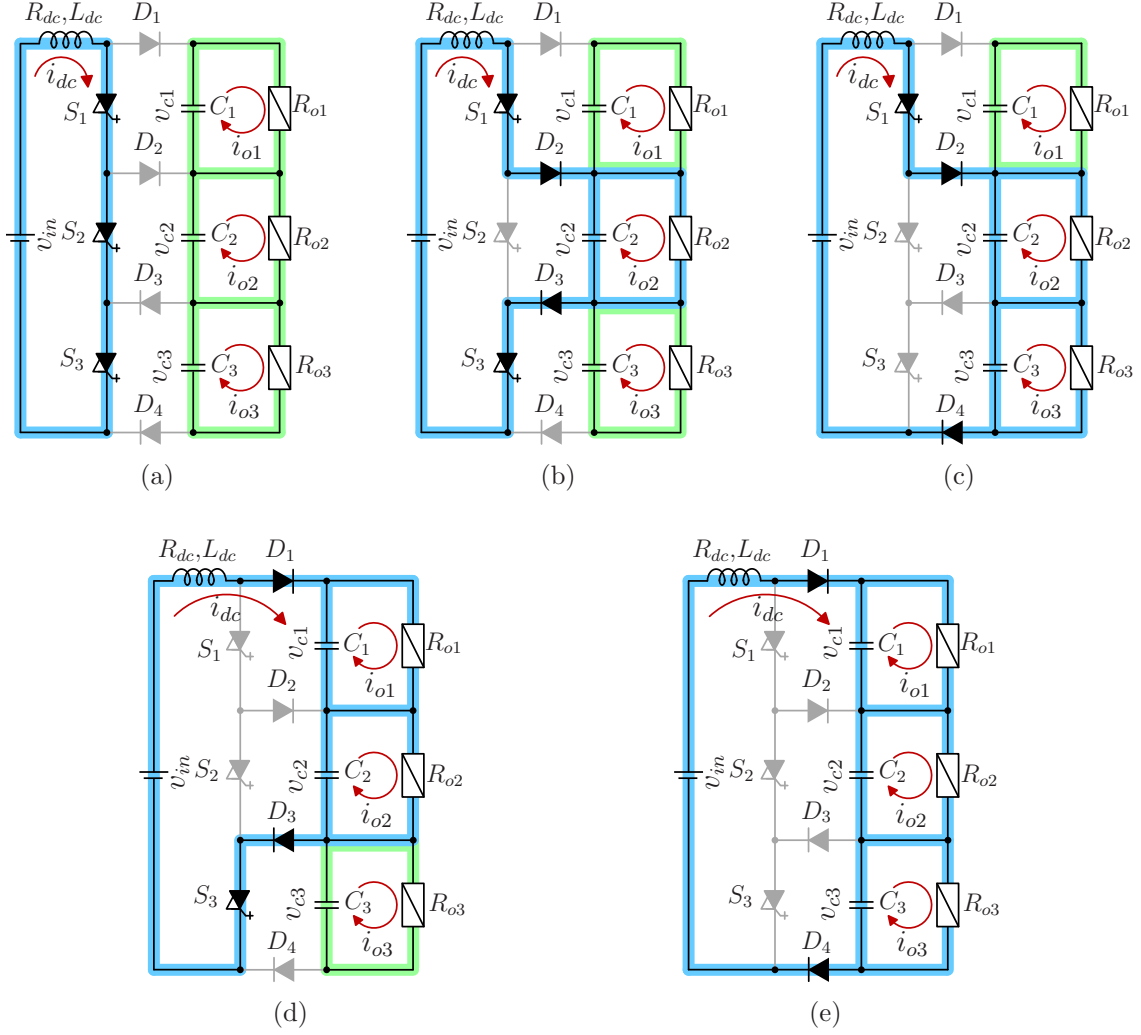


Figure 8.2: Operating modes for the four-level boost converter: (a) mode-I, (b) mode-II, (c) mode-III, (d) mode-IV, and (e) mode-V.

The operating modes presented in the Fig. 8.2 can be analyzed with Kirchhoff's law and the dynamic equations for the inductor current i_{dc} can be represented as:

$$\begin{aligned}
 \text{Mode-I : } \quad \frac{d i_{dc}}{dt} &= \frac{v_{in} - R_{dc} i_{dc}}{L_{dc}} \\
 \text{Mode-II : } \quad \frac{d i_{dc}}{dt} &= \frac{v_{in} - R_{dc} i_{dc} - v_{c2}}{L_{dc}} \\
 \text{Mode-III : } \quad \frac{d i_{dc}}{dt} &= \frac{v_{in} - R_{dc} i_{dc} - v_{c2} - v_{c3}}{L_{dc}} \\
 \text{Mode-IV : } \quad \frac{d i_{dc}}{dt} &= \frac{v_{in} - R_{dc} i_{dc} - v_{c1} - v_{c2}}{L_{dc}} \\
 \text{Mode-V : } \quad \frac{d i_{dc}}{dt} &= \frac{v_{in} - R_{dc} i_{dc} - v_{c1} - v_{c2} - v_{c3}}{L_{dc}}.
 \end{aligned} \tag{8.4}$$

Similarly, the dc-link capacitor voltage dynamics can be obtained as:

$$\begin{aligned}
\text{Mode-I : } & \frac{dv_{c1}}{dt} = \frac{0 - i_{o1}}{C_1}, \quad \frac{dv_{c2}}{dt} = \frac{0 - i_{o2}}{C_2}, \quad \frac{dv_{c3}}{dt} = \frac{0 - i_{o3}}{C_3}, \\
\text{Mode-II : } & \frac{dv_{c1}}{dt} = \frac{0 - i_{o1}}{C_1}, \quad \frac{dv_{c2}}{dt} = \frac{i_{dc} - i_{o2}}{C_2}, \quad \frac{dv_{c3}}{dt} = \frac{0 - i_{o3}}{C_3}, \\
\text{Mode-III : } & \frac{dv_{c1}}{dt} = \frac{0 - i_{o1}}{C_1}, \quad \frac{dv_{c2}}{dt} = \frac{i_{dc} - i_{o2}}{C_2}, \quad \frac{dv_{c3}}{dt} = \frac{i_{dc} - i_{o3}}{C_3}, \\
\text{Mode-IV : } & \frac{dv_{c1}}{dt} = \frac{i_{dc} - i_{o1}}{C_1}, \quad \frac{dv_{c2}}{dt} = \frac{i_{dc} - i_{o2}}{C_2}, \quad \frac{dv_{c3}}{dt} = \frac{0 - i_{o3}}{C_3}, \\
\text{Mode-V : } & \frac{dv_{c1}}{dt} = \frac{i_{dc} - i_{o1}}{C_1}, \quad \frac{dv_{c2}}{dt} = \frac{i_{dc} - i_{o2}}{C_2}, \quad \frac{dv_{c3}}{dt} = \frac{i_{dc} - i_{o3}}{C_3}.
\end{aligned} \tag{8.5}$$

By combining the dynamic equations in (8.4) and (8.5), the continuous-time system describing the inductor current and dc-link capacitor voltages can be obtained as:

$$\begin{aligned}
\frac{d}{dt} \begin{bmatrix} i_{dc} \\ v_{c1} \\ v_{c2} \\ v_{c3} \end{bmatrix} &= \underbrace{\begin{bmatrix} -\frac{R_{dc}}{L_{dc}} & -\frac{(1-S_{1f})}{L_{dc}} & -\frac{(1-S_{2f})}{L_{dc}} & -\frac{(1-S_{3f})}{L_{dc}} \\ \frac{(1-S_{1f})}{C_1} & 0 & 0 & 0 \\ \frac{(1-S_{2f})}{C_2} & 0 & 0 & 0 \\ \frac{(1-S_{3f})}{C_3} & 0 & 0 & 0 \end{bmatrix}}_{\mathbf{P}_b} \begin{bmatrix} i_{dc} \\ v_{c1} \\ v_{c2} \\ v_{c3} \end{bmatrix} \\
&+ \underbrace{\begin{bmatrix} \frac{1}{L_{dc}} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_3} \end{bmatrix}}_{\mathbf{Q}_b} \begin{bmatrix} v_{in} \\ i_{o1} \\ i_{o2} \\ i_{o2} \end{bmatrix}
\end{aligned} \tag{8.6}$$

where S_{1f} , S_{2f} and S_{3f} are the switching signals applied to the 4L-BC active switches S_1 , S_2 and S_3 , respectively.

In deriving the above dynamic system, the inverter is replaced by three virtual resistive loads as shown in the Fig. 8.3. The measurement of output currents, i_{o1} , i_{o2} and i_{o3} is not recommended as it increases the complexity as well as the cost. Rather these variables can be estimated using the measured grid currents and 4L-DCI switching signals. The relation between the output currents and inverter branch currents can be demonstrated as follows with the help of Fig. 8.3:

$$\begin{aligned}
i_{o1} &= i_p \\
i_{o2} &= i_{o1} + i_x = i_p + i_x \\
i_{o3} &= i_{o2} + i_y = i_p + i_x + i_y.
\end{aligned} \tag{8.7}$$

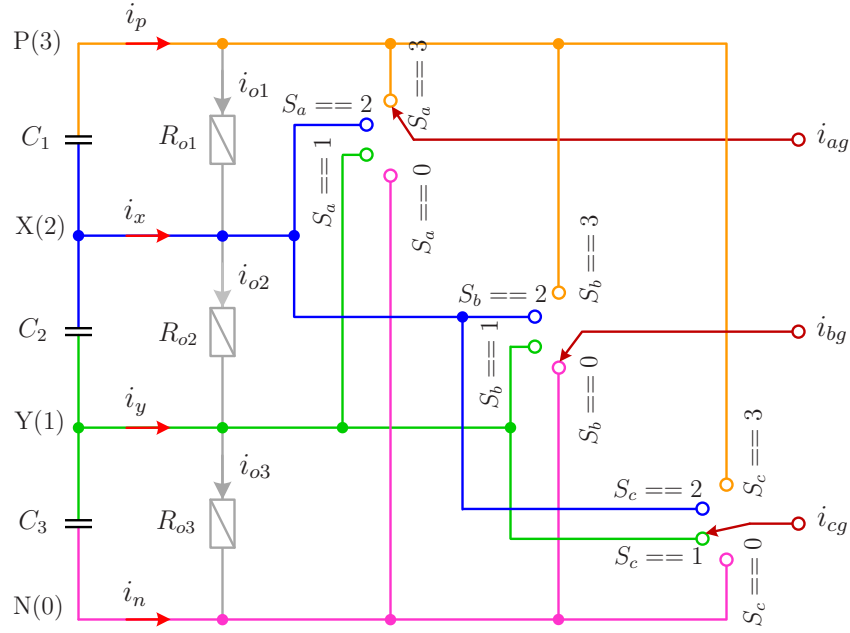


Figure 8.3: Representation of virtual resistors and the inverter.

The inverter branch currents i_p , i_x and i_y can be estimated based on inverter voltage vector levels S_a , S_b and S_c , and measured grid currents as [108, 281, 302]:

$$\begin{bmatrix} i_p \\ i_x \\ i_y \end{bmatrix} = \begin{bmatrix} S_a == 3 \\ S_a == 2 \\ S_a == 1 \end{bmatrix} i_{ag} + \begin{bmatrix} S_b == 3 \\ S_b == 2 \\ S_b == 1 \end{bmatrix} i_{bg} + \begin{bmatrix} S_c == 3 \\ S_c == 2 \\ S_c == 1 \end{bmatrix} i_{cg}. \quad (8.8)$$

By substituting the S_a , S_b and S_c values given in Table. 5.1, the above expression can be described in terms of 4L-DCI switching signals. This is shown as follows:

$$\begin{bmatrix} i_p \\ i_x \\ i_y \end{bmatrix} = \begin{bmatrix} S_{1a}S_{2a}S_{3a} \\ \bar{S}_{1a}S_{2a}S_{3a} \\ \bar{S}_{1a}\bar{S}_{2a}S_{3a} \end{bmatrix} i_{ag} + \begin{bmatrix} S_{1b}S_{2b}S_{3b} \\ \bar{S}_{1b}S_{2b}S_{3b} \\ \bar{S}_{1b}\bar{S}_{2b}S_{3b} \end{bmatrix} i_{bg} + \begin{bmatrix} S_{1c}S_{2c}S_{3c} \\ \bar{S}_{1c}S_{2c}S_{3c} \\ \bar{S}_{1c}\bar{S}_{2c}S_{3c} \end{bmatrix} i_{cg}. \quad (8.9)$$

As demonstrated in this section, the proposed approach does not require the dynamic model and parameters of the PMSG. Moreover, the PMSG rotor position is also not required. This greatly simplifies the complexity of the control system. From (8.7), it can be understood that the inductor current and dc-link capacitor voltages can be effectively controlled by the optimal selection of switching signals.

8.2 Discrete-Time Modeling and Two-Step Prediction

The discrete-time dynamic system for SRF grid currents can be obtained from (8.1) as follows:

$$\begin{bmatrix} i_{dg}(k+h) \\ i_{qg}(k+h) \end{bmatrix} = \Xi \begin{bmatrix} i_{dg}(k+h-1) \\ i_{qg}(k+h-1) \end{bmatrix} + \Upsilon \begin{bmatrix} v_{di}(k+h-1) \\ v_{qi}(k+h-1) \end{bmatrix} + \Psi \begin{bmatrix} v_{dg}(k+h-1) \\ v_{qg}(k+h-1) \end{bmatrix} \quad (8.10)$$

where

$$\Xi = e^{\mathbf{P}_i T_s}, \quad \Upsilon = \mathbf{P}_i^{-1}(\Xi - \mathbf{I}_{2 \times 2})\mathbf{Q}_i, \quad \Psi = \mathbf{P}_i^{-1}(\Xi - \mathbf{I}_{2 \times 2})\mathbf{R}_i. \quad (8.11)$$

In the above systems, h is the prediction horizon and T_s is the controller sampling time. The continuous-time system for the boost converter which is described in (8.6) can also be converted to a discrete-time domain as:

$$\begin{bmatrix} i_{dc}(k+h) \\ v_{c1}(k+h) \\ v_{c2}(k+h) \\ v_{c3}(k+h) \end{bmatrix} = \Phi \begin{bmatrix} i_{dc}(k+h-1) \\ v_{c1}(k+h-1) \\ v_{c2}(k+h-1) \\ v_{c3}(k+h-1) \end{bmatrix} + \Gamma \begin{bmatrix} v_{in}(k+h-1) \\ i_{o1}(k+h-1) \\ i_{o2}(k+h-1) \\ i_{o3}(k+h-1) \end{bmatrix} \quad (8.12)$$

where

$$\Phi = e^{\mathbf{P}_b T_s}, \quad \Gamma = \mathbf{P}_b^{-1}(\Phi - \mathbf{I}_{4 \times 4})\mathbf{Q}_b. \quad (8.13)$$

The parameter matrix, \mathbf{P}_b contains gating signals S_{1f} , S_{2f} and S_{3f} . These signals are set to zero during the off-line discrete-time conversion.

As shown in Figs. 8.4(a) and 8.4(b), the prediction of control variables at $(k+1)$ uses 5 and 64 switching states for the 4L-BC and 4L-DCI, respectively. This is essentially called one-step prediction ($h=1$) and this methodology is used in many works [79, 281, 295] to simplify the analysis and digital implementation computations. The works in [253–255] suggest the use of a two-step prediction ($h=2$) for an optimal performance. But this leads to a higher computational burden for 4L-BC and 4L-DCI caused by 25 (5^2) and 4096 (64^2) predictions, respectively. To reduce the number of calculations while achieving better performance compared to the one-step prediction, a modified two-step prediction is previously analyzed in [303]. But its feasibility has not been tested by digital implementation. In this paper, the modified two-step prediction is extended for the control of proposed power converters and this concept is shown in Figs. 8.5(a) and 8.5(b). Similar to one-step prediction,

this approach uses 5 and 64 switching states for 4L-BC and 4L-DCI, respectively. But the predictions are projected to $(k+2)$ sampling instant, and with this approach the advantages of lower computations of one-step prediction and optimal performance of two-step prediction can be combined.

The discrete-time model for the two-step prediction of grid currents is as follows:

$$\begin{bmatrix} i_{dg}(k+2) \\ i_{qg}(k+2) \end{bmatrix} = \Xi \begin{bmatrix} i_{dg}(k+1) \\ i_{qg}(k+1) \end{bmatrix} + \Upsilon \begin{bmatrix} v_{di}(k) \\ v_{qi}(k) \end{bmatrix} + \Psi \begin{bmatrix} v_{dg}(k+1) \\ v_{qg}(k+1) \end{bmatrix} \quad (8.14)$$

where $v_{dg}(k+1)$ and $v_{qg}(k+1)$ are extrapolated [77,258,259] grid voltages. The $i_{dg}(k+1)$ and $i_{qg}(k+1)$ are predicted grid currents in $(k+1)$ sampling instant, and they can be obtained as:

$$\begin{bmatrix} i_{dg}(k+1) \\ i_{qg}(k+1) \end{bmatrix} = \Xi \begin{bmatrix} i_{dg}(k) \\ i_{qg}(k) \end{bmatrix} + \Upsilon \begin{bmatrix} v_{di}(k) \\ v_{qi}(k) \end{bmatrix} + \Psi \begin{bmatrix} v_{dg}(k) \\ v_{qg}(k) \end{bmatrix} \quad (8.15)$$

where $v_{dg}(k)$ and $v_{qg}(k)$ are measured grid voltages. $i_{dg}(k)$ and $i_{qg}(k)$ are measured grid currents. By observing (8.14) and (8.15), it can be noticed that the same inverter voltages $[v_{di}(k), v_{qi}(k)]$ are used in $(k+1)$ and $(k+2)$ prediction of grid currents. Compared to one-step prediction, the number of calculations are higher, but significantly lower compared to the standard two-step prediction.

Similarly, the two-step prediction model for the 4L-boost converter can be obtained as:

$$\begin{bmatrix} i_{dc}(k+2) \\ v_{c1}(k+2) \\ v_{c2}(k+2) \\ v_{c3}(k+2) \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12}[1 - S_{1f}(k)] & \phi_{13}[1 - S_{2f}(k)] & \phi_{14}[1 - S_{3f}(k)] \\ \phi_{21}[1 - S_{1f}(k)] & \phi_{22} & \phi_{23} & \phi_{24} \\ \phi_{31}[1 - S_{2f}(k)] & \phi_{32} & \phi_{33} & \phi_{34} \\ \phi_{41}[1 - S_{3f}(k)] & \phi_{42} & \phi_{43} & \phi_{44} \end{bmatrix} \quad (8.16)$$

$$\begin{bmatrix} i_{dc}(k+1) \\ v_{c1}(k+1) \\ v_{c2}(k+1) \\ v_{c3}(k+1) \end{bmatrix} + \mathbf{\Gamma} \begin{bmatrix} v_{in}(k+1) \\ i_{o1}(k+1) \\ i_{o2}(k+1) \\ i_{o3}(k+1) \end{bmatrix}$$

where $v_{in}(k+1)$, $i_{o1}(k+1)$, $i_{o2}(k+1)$ and $i_{o3}(k+1)$ are extrapolated quantities. ϕ_{ij} with $i = 1, 2, 3, 4$ and $j = 1, 2, 3, 4$ are the elements of the matrix Φ defined in (8.13). $i_{dc}(k+1)$, $v_{c1}(k+1)$, $v_{c2}(k+1)$, and $v_{c3}(k+1)$ are predicted quantities during $(k+1)$ sampling instant

as:

$$\begin{bmatrix} i_{dc}(k+1) \\ v_{c1}(k+1) \\ v_{c2}(k+1) \\ v_{c3}(k+1) \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12}[1 - S_{1f}(k)] & \phi_{13}[1 - S_{2f}(k)] & \phi_{14}[1 - S_{3f}(k)] \\ \phi_{21}[1 - S_{1f}(k)] & \phi_{22} & \phi_{23} & \phi_{24} \\ \phi_{31}[1 - S_{2f}(k)] & \phi_{32} & \phi_{33} & \phi_{34} \\ \phi_{41}[1 - S_{3f}(k)] & \phi_{42} & \phi_{43} & \phi_{44} \end{bmatrix} \quad (8.17)$$

$$\begin{bmatrix} i_{dc}(k) \\ v_{c1}(k) \\ v_{c2}(k) \\ v_{c3}(k) \end{bmatrix} + \mathbf{\Gamma} \begin{bmatrix} v_{in}(k) \\ i_{o1}(k) \\ i_{o2}(k) \\ i_{o3}(k) \end{bmatrix}$$

where $v_{in}(k)$, $i_{dc}(k)$, $v_{c1}(k)$, $v_{c2}(k)$, and $v_{c3}(k)$ are measured variables and $i_{o1}(k)$, $i_{o2}(k)$, and $i_{o3}(k)$ are calculated in terms of grid currents and 4L-DCI gating signals [refer to (8.9)]. Similar to the two-step prediction of 4L-DCI, the $(k+1)$ and $(k+2)$ predictions are carried out using the same 4L-BC switching signals $[S_{1f}(k), S_{2f}(k), \text{ and } S_{3f}(k)]$.

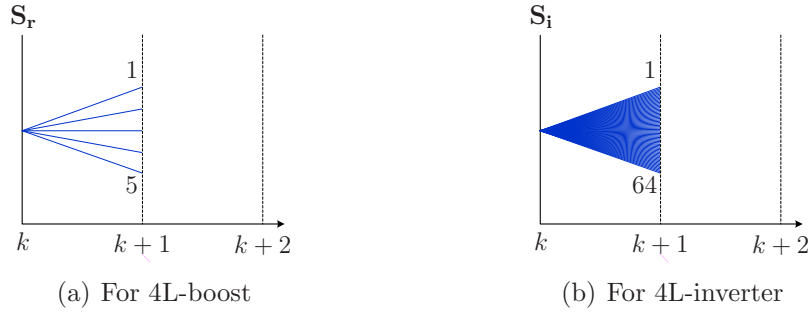


Figure 8.4: Prediction of control variables using one-step prediction.

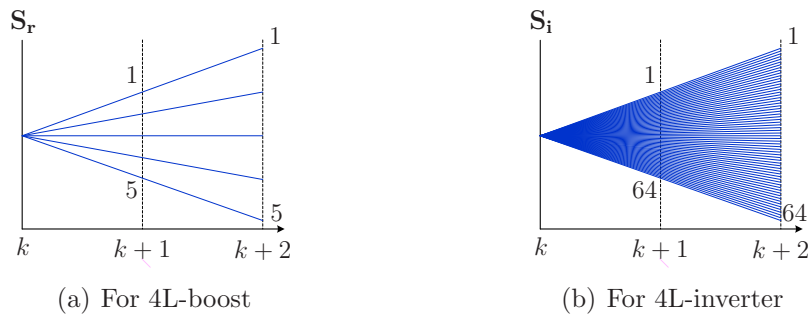


Figure 8.5: Prediction of control variables using modified two-step prediction .

8.3 Proposed Model Predictive Control Strategy

The proposed control scheme using two-step prediction is shown in Fig. 8.6. As shown in Fig. 8.6, independent control loops are developed for 4L-BC and 4L-DCI and the control objectives are set for both of them. This is further clarified in the following subsections:

8.3.1 Control System for Four-Level Boost Converter

The control system for 4L-BC is depicted in Fig. 8.7(a). The MPPT algorithm provides reference speed to the generator based on varying wind speed conditions. A PI controller generates the input active power reference, P_{in}^* as follows:

$$P_{in}^*(k) = (K_p + K_i/S) [\omega_m^*(k) - \omega_m(k)] \quad (8.18)$$

where K_p and K_i are the PI controller proportional and integral gains. By tracking to this reference variable, the MPPT can be achieved in such a way that the generator speed, current and electromagnetic torque can be regulated. This control objective is expressed as the following cost function:

$$g_{track,b}(k) = [P_{in}^*(k+2) - P_{in}(k+2)]^2 \quad (8.19)$$

where $P_{in}^*(k+2)$ is the extrapolated reference variable.

The two-step prediction for the input active power is obtained using extrapolated input voltage, $v_{in}(k+2)$ and a predicted dc-link current, $i_{dc}(k+2)$ (according to [8.16]). This is depicted as follows:

$$P_{in}(k+2) = v_{in}(k+2) \cdot i_{dc}(k+2). \quad (8.20)$$

Another important control objective is to balance the dc-link capacitor voltages. This is expressed as follows:

$$\begin{aligned} g_{dc,b}(k) = & \lambda_{dc,b} * [v_{c1}(k+2) - v_{c2}(k+2)]^2 \\ & + \lambda_{dc,b} * [v_{c2}(k+2) - v_{c3}(k+2)]^2 \\ & + \lambda_{dc,b} * [v_{c1}(k+2) - v_{c3}(k+2)]^2 \end{aligned} \quad (8.21)$$

where $\lambda_{dc,b}$ is the weighting factor used for the capacitor voltages balancing task.

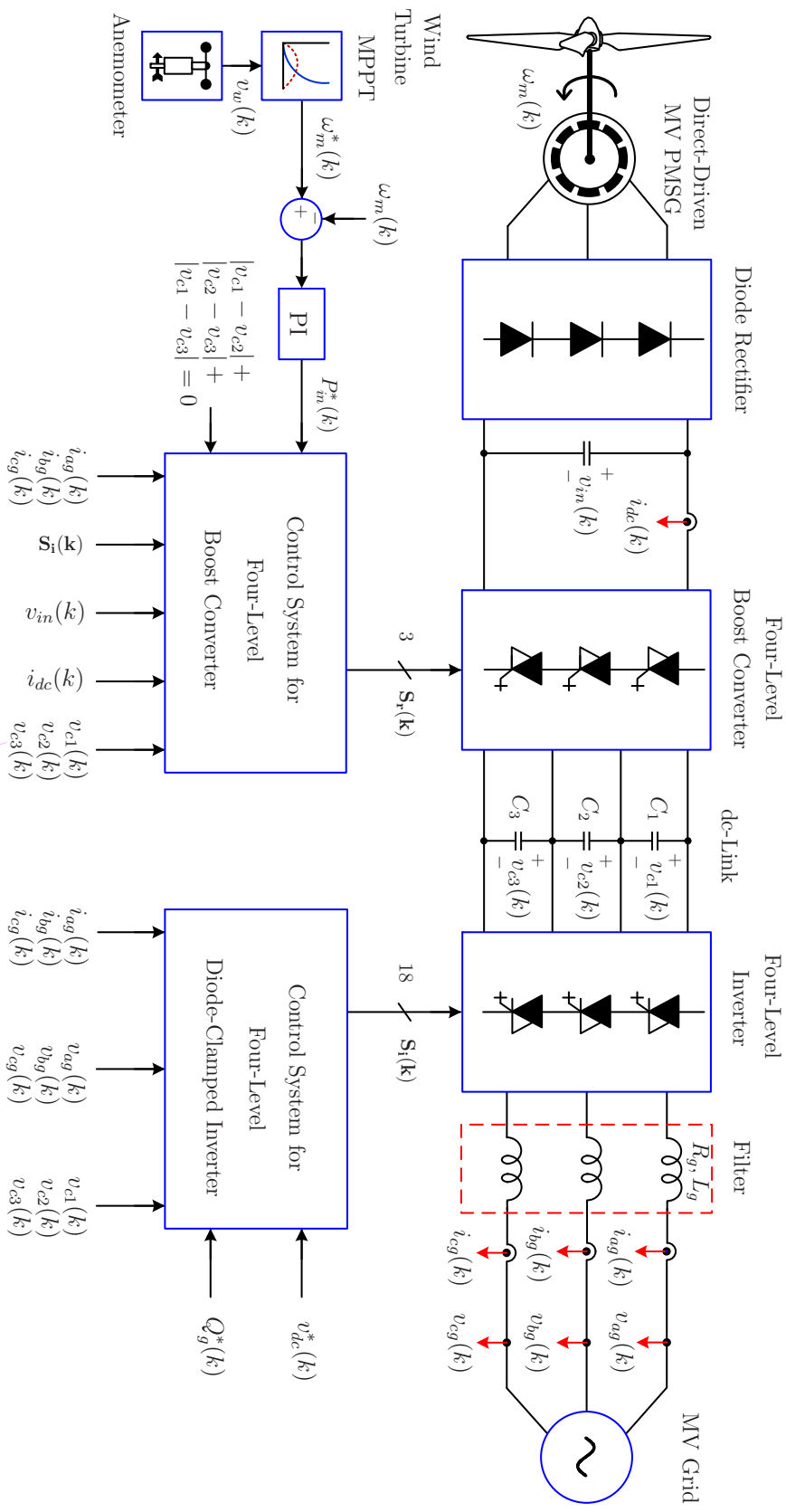


Figure 8.6: Block diagram of the complete control system.

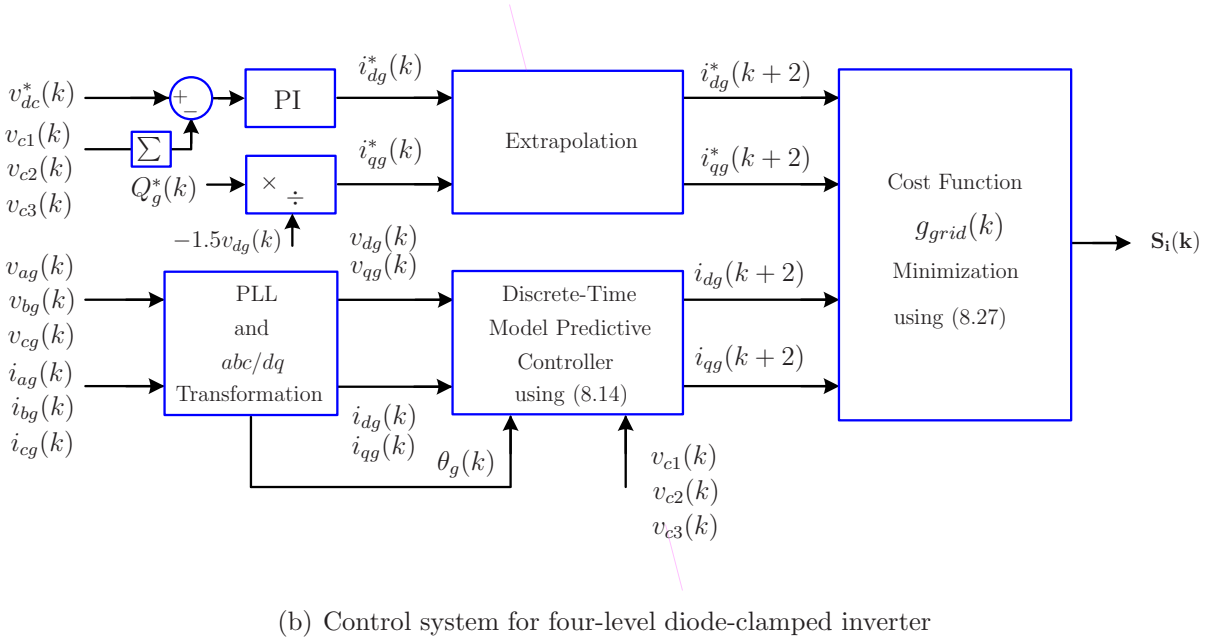
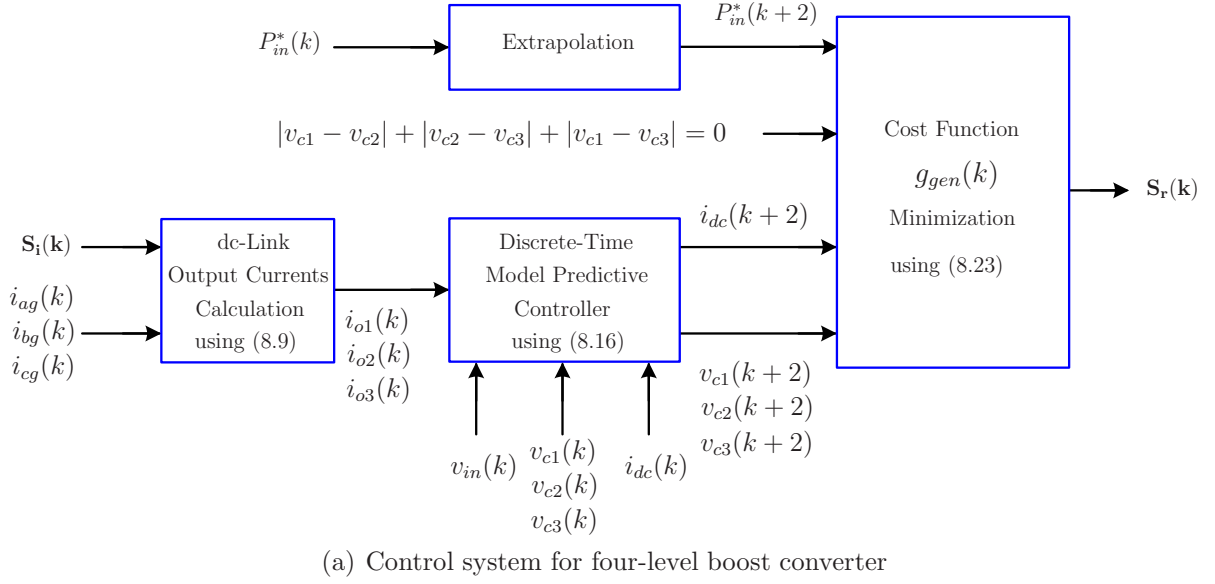


Figure 8.7: Proposed predictive control scheme for 4L-converter based PMSG-WECS.

The device switching frequency reduction is penalized in the cost function, $g_{swc,b}$:

$$g_{swc,b}(k) = \lambda_{swc,b} * \sum_{x=1,2,3} |S_{xf}(k) - S_{xf,op}(k)| \quad (8.22)$$

where $\lambda_{swc,b}$ is the corresponding weighting factor. $S_{xf,op}(k)$ is the optimal 4L-BC switching signal in the previous iteration. This switching frequency minimization algorithm anticipates and minimizes the number of switch changes compared to the previous sampling instant.

All these control objectives for the 4L-BC are merged into a cost function as:

$$g_{gen}(k) = g_{track,b}(k) + g_{dc,b}(k) + g_{swc,b}(k). \quad (8.23)$$

The control algorithm for the digital implementation two-step prediction for the 4L-BC is shown in Fig. 8.8(a). The algorithm is initialized by setting the switching state number i to 0 and optimal g value to ∞ . At this point, the algorithm enters the loop. The measured quantities and 5 switching states are used in the prediction of $(k+1)$ instant variables. The predicted variables at $(k+1)$ instant and the extrapolated quantities are used in the prediction of $(k+2)$ variables. It is important to note that the number of predictions at $(k+1)$ and $(k+2)$ instants are 5 only. The cost function minimization is based on the $(k+2)$ variables only. The switching state, which produces minimal value of g_{op} is chosen and applied to the 4L-BC gating terminals directly. The current regulators and modulation are eliminated with the proposed approach.

8.3.2 Control System for Four-Level Inverter

The 4L-DCI control system is shown in the Fig. 8.7(b). The two control objectives can be met by forcing the grid currents to track to their references. This is defined as:

$$g_{track,i}(k) = [i_{dg}^*(k+2) - i_{dg}(k+2)]^2 + [i_{qg}^*(k+2) - i_{qg}(k+2)]^2 \quad (8.24)$$

where $i_{dg}^*(k+2)$ and $i_{qg}^*(k+2)$ are the extrapolated reference currents. The two-step prediction for the grid currents are obtained according to (8.14).

The switching frequency reduction objective is expressed as:

$$g_{swc,i}(k) = \lambda_{swc,i} * \sum_{x=1, 2, 3} \sum_{j=a,b,c} |S_{xj}(k) - S_{xj,op}(k)| \quad (8.25)$$

where $\lambda_{swc,i}$ is a weighting factor. $S_{xj,op}(k)$ is the optimal 4L-DCI switching signal in the previous sampling instant.

The common-mode voltage can be minimized by penalizing the following cost function:

$$g_{cmv,i}(k) = \lambda_{cmv,i} * |v_{cm}(k)| \quad (8.26)$$

where $\lambda_{cmv,i}$ is the weighting factor for CMV minimization.

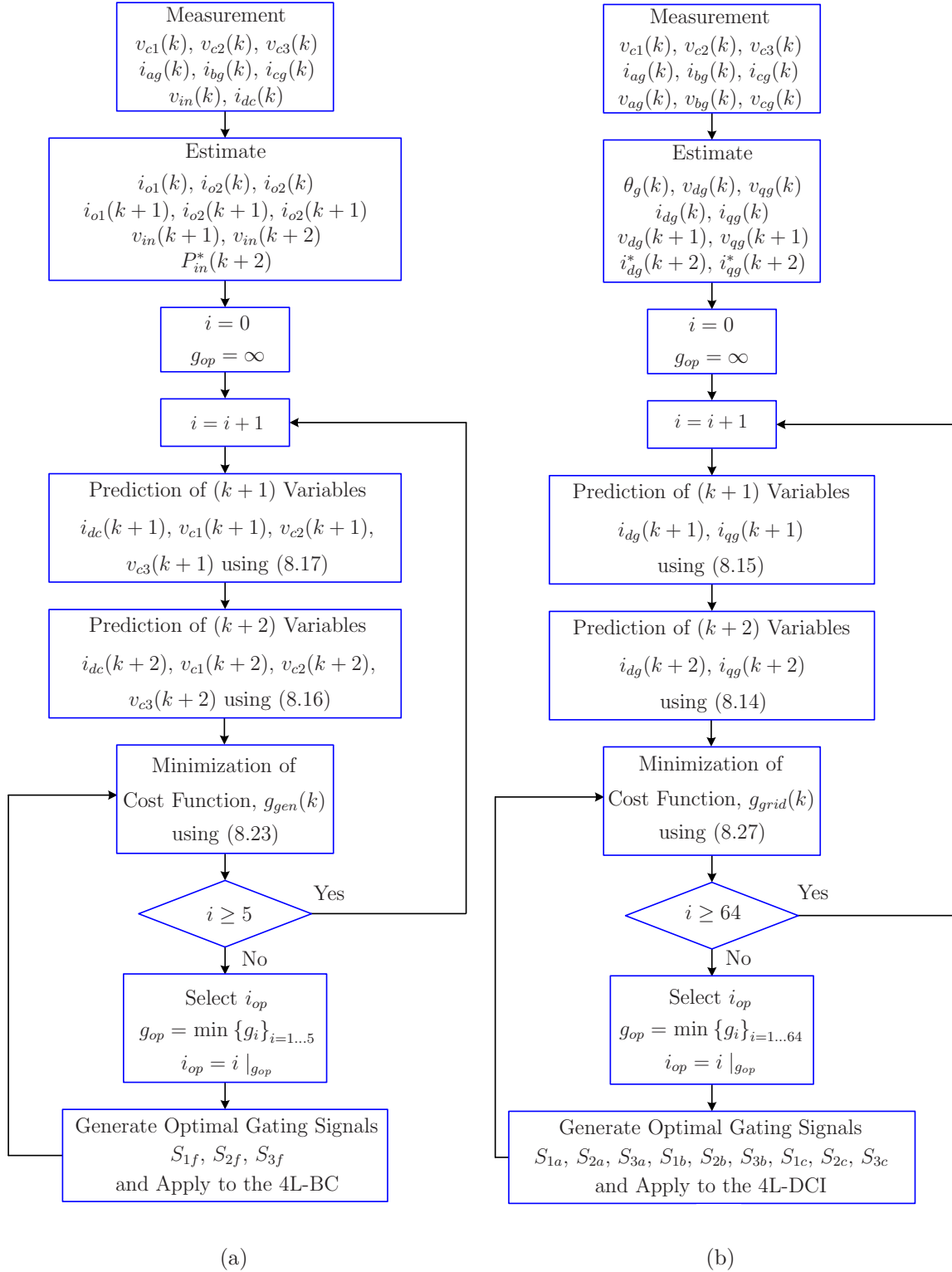


Figure 8.8: Proposed two-step predictive control algorithm for: (a) four-level boost converter, and (b) four-level diode-clamped inverter.

The final cost function for the 4L-DCI is defined as:

$$g_{grid}(k) = g_{track,i}(k) + g_{swc,i}(k) + g_{cmv,i}(k). \quad (8.27)$$

The control algorithm for the 4L-DCI is shown in Fig. 8.8(b) and it is similar to the boost converter's algorithm in terms of the implementation. During each iteration, the future behavior of the control variables are predicted using the 64 switching states. The switching state (among 64) which minimizes the cost function $g_{grid}(k)$ is chosen and applied to the 4L-DCI. The linear regulators (PI) are eliminated in the internal current control loops and there is no need to design the pulse width or space vector modulation.

Table 8.2: Parameters of the proposed power conversion system

Variable	Description	Simulation		Experimental	
		SI	p.u.	SI	p.u.
P_T	Rated Power (kW)	5000	1.0	3.6	1.0
T_T	Rated Torque (kN.m)	318.31	1.0	0.2292	1.0
N_T	Rated Speed (rpm)	150	1.0	150	1.0
R_{gb}	Gear Ratio	1		1	
r_T	Rotor Radius (m)	55.97		–	
ρ	Air Density (kg.m ²)	1.225		–	
$C_{p,op}$	Optimal Power Coefficient	0.48		–	
$\lambda_{T,op}$	Optimal Tip Speed Ratio	73.267		–	
Permanent Magnet Synchronous Generator Parameters					
P_m	Rated Mechanical Power (kW)	5000		3.6	
v_{sl}	Rated Line-Line Voltage (V)	4160		208	
v_s	Rated Phase Voltage (V)	2402	1.0	120	1.0
i_s	Rated Stator Current (A)	700	1.0	10	1.0
f_s	Rated Stator Frequency (Hz)	20	1.0	20	1.0
PF_s	Rated Power Factor	0.98		0.98	
n_m	Rated Rotor Speed (rpm)	150	1.0	150	1.0
PP	Number of Pole Pairs	8		8	
T_m	Rated Mechanical Torque (kN.m)	318.31	1.0	0.2292	1.0
λ_r	Rated rms Rotor Flux Linkage (Wb)	18.92	1.0	0.956	1.0
R_s	Stator Winding Resistance (m Ω)	34.4	0.013	245	0.021
L_d	d -axis Synchronous Inductance (mH)	5.475	0.2	19.1	0.2
L_q	q -axis Synchronous Inductance (mH)	5.475	0.2	19.1	0.2
J	Moment of Inertia (kg.m ²)	237.93			
Medium Voltage Grid Parameters					
S_g	Rated Apparent Power (kVA)	5000	1.0	3.6	1.0
v_{gl}	Rated Line-Line Voltage (V)	4160		208	
v_g	Rated Phase Voltage (V)	2402	1.0	120	1.0
i_g	Rated Stator Current (A)	694	1.0	10	1.0
f_g	Rated Stator Frequency (Hz)	60	1.0	60	1.0
Z_{bg}	Base Impedance (Ω)	3.46	1.0	12.018	1.0
L_{bg}	Base Inductance (mH)	9.18	1.0	31.88	1.0
C_{bg}	Base Capacitance (μ F)	766.39	1.0	220.72	1.0
Power Electronic Converter Parameters					
C_{in}	Input Capacitance (μ F)	8300	10.87	2400	10.87
C_{dc}	Output dc-link Capacitance (μ F)	3500	4.53	1000	4.53
R_{dc}	Boost Filter Leakage Resistance (Ω)	0.04	0.01	0.12	0.01
L_{dc}	Boost Filter Inductance (mH)	2.9	0.314	10	0.314
R_g	Grid-side Filter Resistance (Ω)	0.031	0.009	0.108	0.009
L_g	Grid-side Filter Inductance (mH)	1.9	0.207	6.6	0.207
Controller Parameters					
T_s	Sampling Time (s)	100 μ		100 μ	
$\lambda_{dc,b}$	Weighting Factor	100		2	
v_{dc}^*	Reference dc-link Voltage (V)	7354	3.062	367	3.062

8.4 Simulation Results

Various tests were carried out using MATLAB/Simulink software to effectively demonstrate the advantages of proposed topology and control strategy. The parameters of the high power (5 MW/4160 V/694 A) PMSG power conversion system are shown in Table 8.2. The one-step prediction strategy is shown in Fig. 8.4 and it implies the ideal case where the time taken for the computations is zero. This means that the switching state, which minimizes the error at the $(k + 1)$ instant, is selected and applied at the k^{th} instant. But in the real-systems, zero computation time can never be achieved. All the digital signal processor platforms require some computational time. To effectively compare the one-step and two-step methods, treat real-time scenario, and better correlate the simulation and experimental results, the digital signal processor control delay is included in the simulation models. The computational delay is set to one sampling period T_s .

8.4.1 Steady-state Analysis

The steady-state analysis is carried out at rated wind speed condition, $v_w = 12$ m/s, and presented in Fig. 8.9. Without the control delay, using one-step prediction, the 4L-BC and 4L-DCI switching frequencies are found to be 806 and 910 Hz, respectively. The grid current reference tracking error, e_{ig} and total harmonic distortion (THD) are found to be 1.1 % and 1.95 %, respectively. The f_{sw} , e_{ig} and THD are calculated according to the guidelines given in Appendix C.

In the presence of the control delay, the performance of the one-step predictive control algorithm deteriorates. To overcome this challenge, a modified one-step prediction is developed using the guidelines given in [248, 249]. With this approach, the best switching state in the previous iteration is used to estimate the control variables at $(k + 1)$ instant. The prediction of $(k + 2)$ variables is carried out using all the switching states of power converters. The switching state, which minimizes the error at $(k + 2)$ instant, is selected and applied.

The simulation results with the modified one-step prediction and proposed method are presented in Figs. 8.9(a) and 8.9(b), respectively and they can compensate the control delay. With one-step prediction, the number of calculations are increased due to the estimation (not prediction) of $(k + 1)$ variables. For this reason, the f_{sw} for 4L-BC and 4L-DCI are increased to 980 and 1350 Hz, respectively. To make a fair comparison with the proposed method,

the f_{sw} for 4L-BC and 4L-DCI are decreased to 420 and 580 Hz by using weighting factors $\lambda_{swc,b} = 3$ and $\lambda_{swc,i} = 20$, respectively. As shown in Fig. 8.9(a), the boost converter input power P_{in} contains a large ripple mainly caused by the inductor current. This high ripple is not a problem because the inductor current is filtered by the dc-link capacitors. The dc-link capacitor voltages are balanced, but present a higher steady-state error. The inverter line-line voltage waveform contains high dv/dt 's and this is reflected to grid currents as higher tracking error and THD.

The simulation results with the modified two-step prediction are presented in Fig. 8.9(b). The f_{sw} and CMV minimization is not considered in the two-step prediction test and thus $\lambda_{swc,b} = \lambda_{swc,i} = \lambda_{cmv,i} = 0$. Even without employing any switching frequency reduction algorithm, the f_{sw} is noted as 408 and 565 Hz for 4L-BC and 4L-DCI, respectively. It is important to note that no delay compensation is needed with the proposed modified two-step prediction. As shown in Fig. 8.9(b) (i), the P_{in} contains less ripple and this indicates the use of a lower rated dc-link capacitive filter compared to the modified one-step prediction. The dc-link capacitor voltages are perfectly balanced and this improves the reliability of the semiconductor switches. The inverter voltage waveform contains less dv/dt 's. The grid currents track to their references with a lower steady-state error of 1.8 % in comparison to the 2.95 % for modified one-step prediction. The grid current THD is found to be 3.29 % which is lower compared to the modified one-step prediction value of 5.05 %. These results validate that by using the proposed strategy, an optimal control performance can be obtained in the complex systems which involve a large number of computations.

8.4.2 Harmonic Analysis

The harmonic analysis and comparison between the modified one-step and proposed method is presented in Fig. 8.10. The fast fourier transform (FFT) of inverter line-line voltage ($v_{i,ab}$) and phase- a grid current are analyzed. In comparison to the PWM and SVM methods, which produce harmonics around the carrier frequency and its multiples, the predictive control method produces harmonics spread over the whole FFT window [262,279]. The proposed method produces low THD values for $v_{i,ab}$ and i_{ag} in comparison to the one-step prediction. The reason is that the peak amplitude of the harmonics is lower compared to the one-step prediction. The results validate that the proposed method is most suitable for high power applications, where power quality is a major concern.

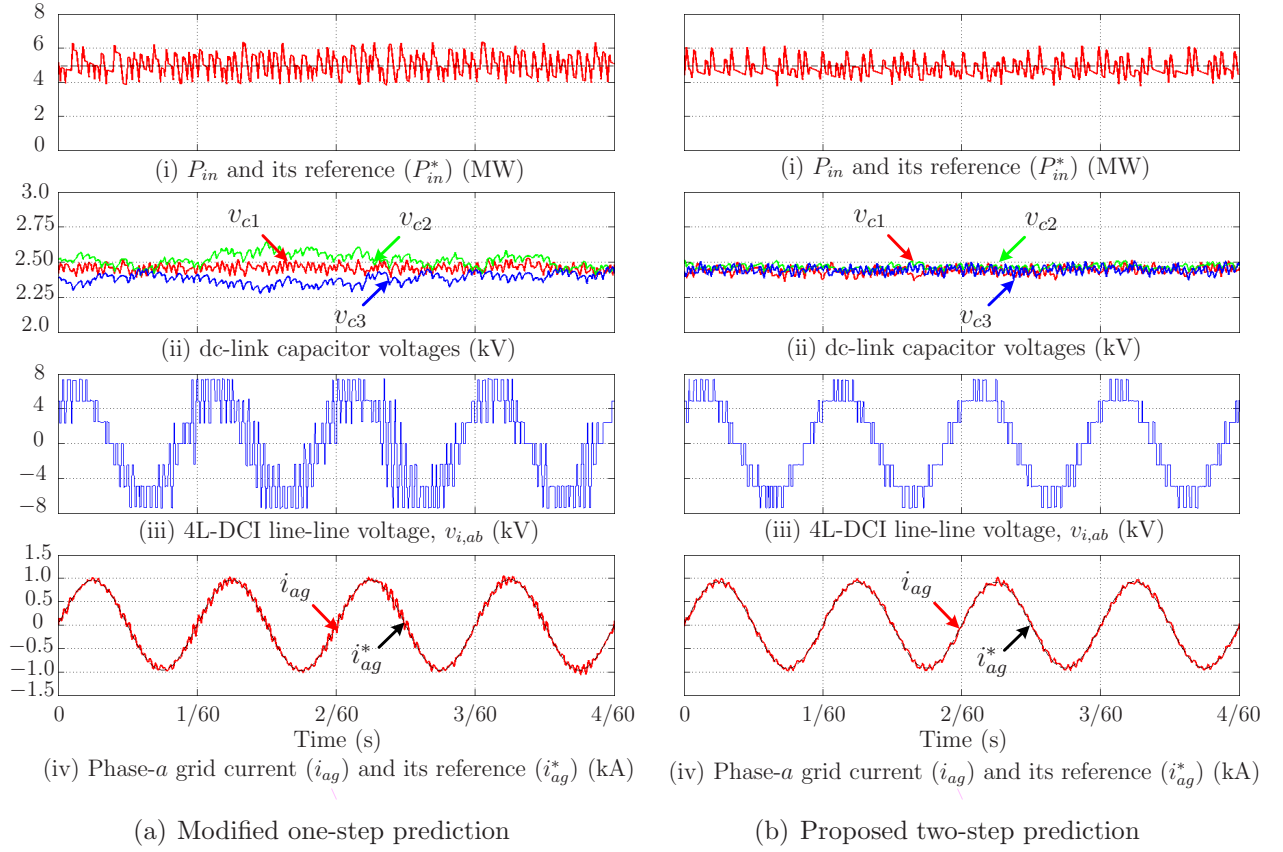


Figure 8.9: Comparison of simulation results during rated wind speed condition using two different prediction methods.

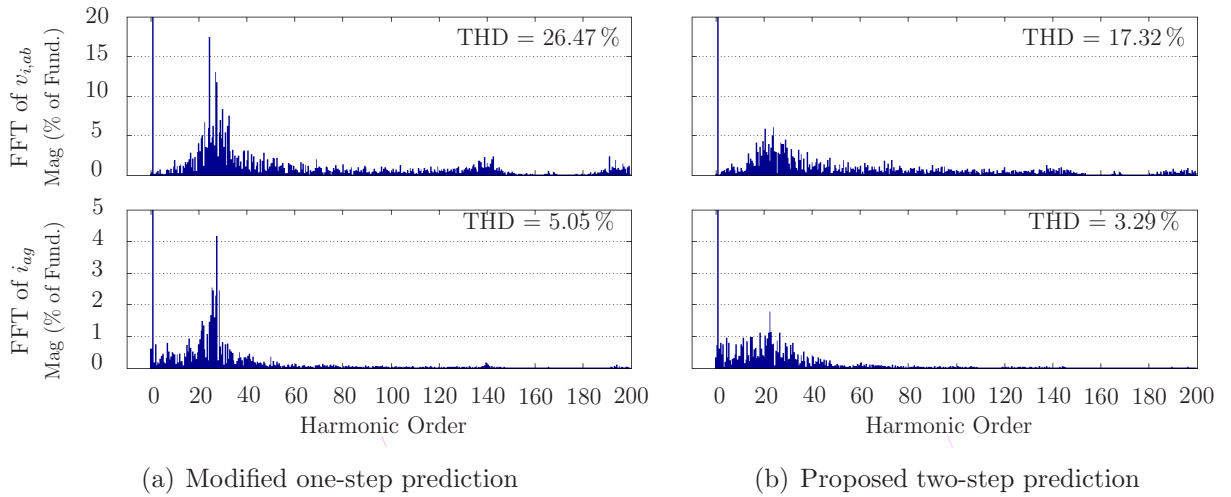


Figure 8.10: Simulation FFT analysis of inverter line-line voltage and grid currents using two different prediction methods.

8.4.3 Switching Frequency Minimization

The simulation results for the f_{sw} minimization of 4L-DCI and its impact on the grid current quality and capacitor voltages is analyzed and presented in Fig. 8.11. From $t = 0$ to $2/60$ s, no penalty is applied for the switching frequency reduction and thus $\lambda_{swc,i} = 0$. During this condition, the f_{sw} , grid current reference tracking error e_{ig} , and grid current THD are 565 Hz, 1.8 % and 3.29 %, respectively. The capacitor voltages are well balanced by the 4L-BC. At $t = 2/60$ s, the weighting factor, $\lambda_{swc,i}$ is changed to 50, and the f_{sw} is decreased to 364 Hz, but with an increase in the reference tracking error (2.4 %) and current THD (4.55 %). The inverter phase voltage waveform v_{aN} clearly shows the reduced number of switch changes. The $\lambda_{swc,i}$ is changed to 4000 at $t = 4/60$ s, and the switching frequency is further minimized to 161 Hz. The e_{ig} , and THD are 3.1 % and 5.83 %, respectively. Even though the f_{sw} is significantly decreased from 565 to 161 Hz, the grid current THD is marginally increased. The reason is that the 4L-DCI does not control the capacitor voltages, and thus it has a control freedom in choosing the best switching state which will generate lower current tracking error and switching frequency. This is one of the best features of the proposed power conversion system.

The 4L-BC switching frequency can also be minimized by including $\lambda_{swc,b}$ in the cost function, g_{gen} . By increasing $\lambda_{swc,b}$ from 0 to 5, the boost converter switching frequency is minimized from 408 to 360 Hz, but with a slight increase in the P_{in} tracking error and capacitor voltages balancing error.

8.4.4 Common-Mode Voltage Minimization

The CMV can be minimized by imposing a weighting factor $\lambda_{cmv,i}$ to the cost function g_{grid} and this is demonstrated in Fig. 8.12. The rated wind speed condition is considered in this test. The $\lambda_{swc,i}$ is set to zero to clearly show the effectiveness of the CMV minimization algorithm. At $t = 3/60$ s, the $\lambda_{cmv,i}$ is changed from 0 to 10 and the CMV is dramatically decreased as shown in Fig. 8.12(a). But, the grid current tracking error increases from 1.8 % to 3.2 %, and also the THD increases from 3.29 % to 4.89 %. The capacitor voltages are well balanced by the 4L-BC, but they contain a higher ripple to the increased grid current THD. This test verifies that CMV in 4L-DCI can be minimized to a certain level without using any additional hardware circuitry such as common-mode choke.

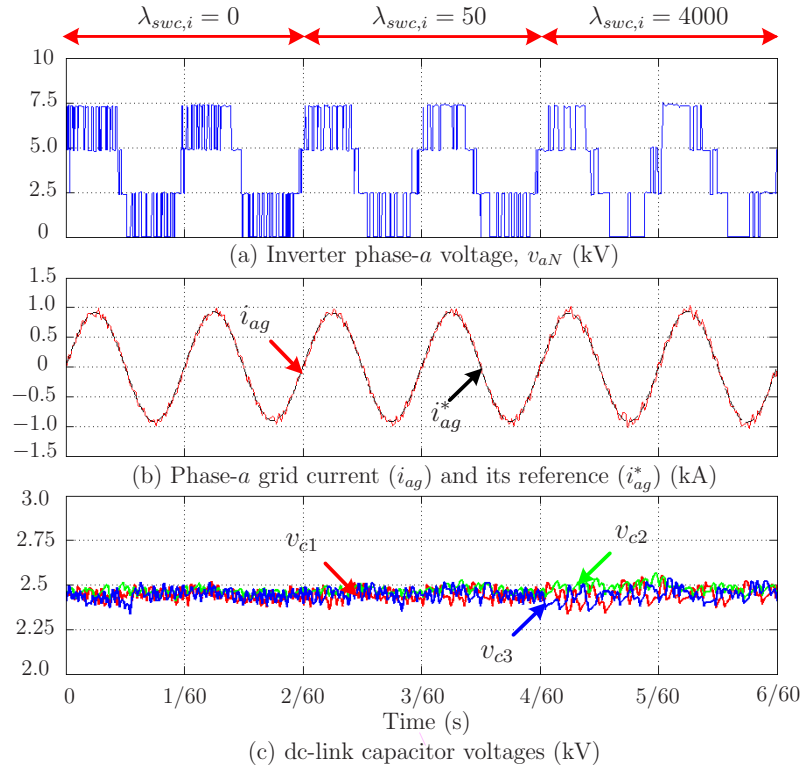


Figure 8.11: Simulation results for grid-tied inverter switching frequency minimization.

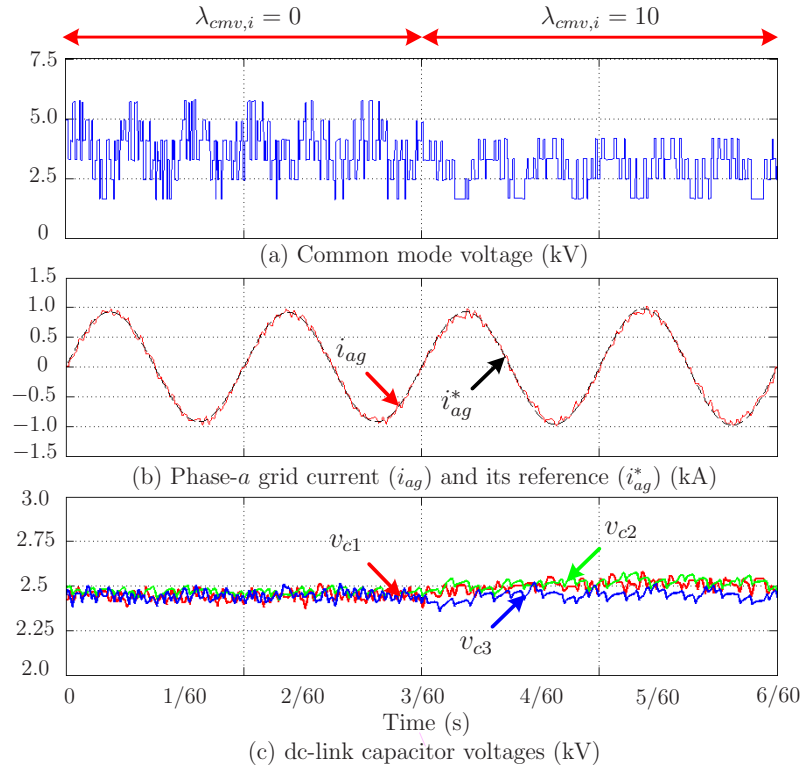


Figure 8.12: Simulation results for grid-tied inverter common-mode voltage minimization.

8.4.5 DC-link Perturbations

The effectiveness of the four-level boost converter and predictive control algorithm are analyzed in this section. Rated wind speed condition is considered in this test. The switching frequency and CMV minimization are not considered to clearly describe the dc-link capacitor voltages balancing. A perturbation is created on purpose by connecting an external capacitor C_{ext} across the dc-link capacitor—2. In real systems, in order to achieve rated capacitance and voltage rating, the dc-link capacitors are connected as series-parallel strings. The perturbation assumed here resembles the faulty condition in one of the dc-link parallel strings. The simulation results with such faulty condition are shown in Fig. 8.13. The C_{ext} rating is assumed to be same as of C_{dc} (4.53 p.u.).

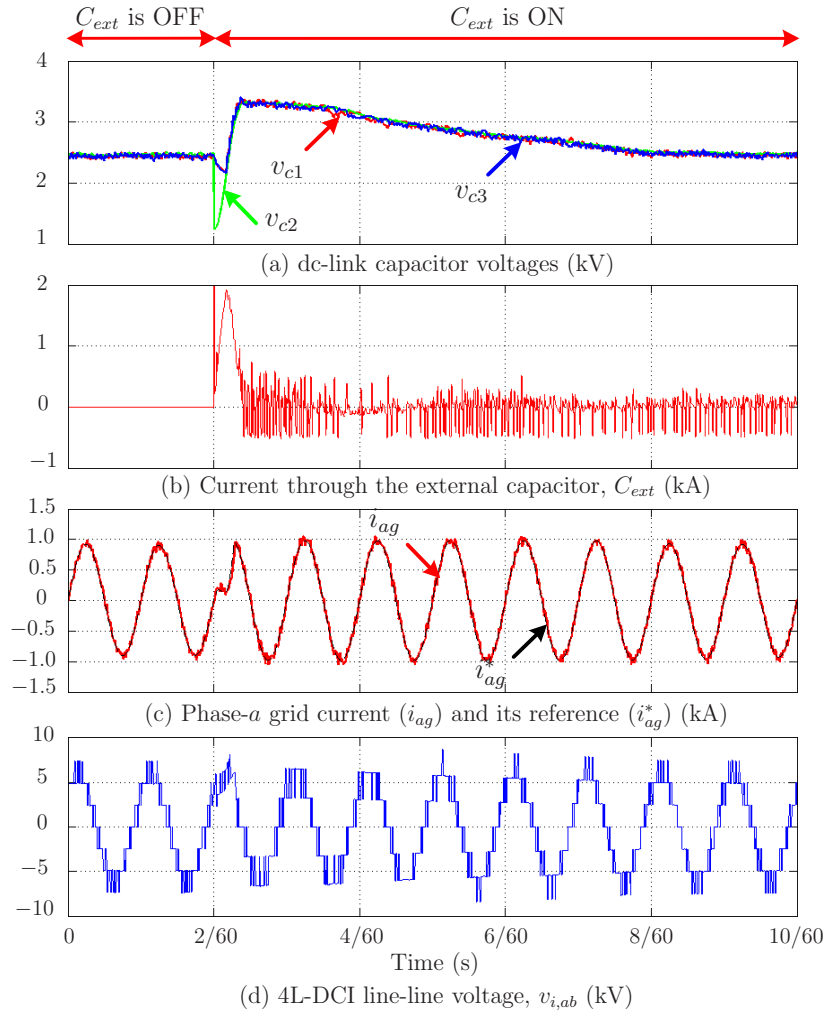


Figure 8.13: Simulation results with step-connection of capacitor C_{ext} across C_{dc2} .

With the step-connection of C_{ext} at $t = 2/60$ s, the v_{c2} suddenly drops due to the large current flowing through the C_{ext} [Fig. 8.13(b)]. But the predictive control algorithm selects appropriate switching states to make the capacitor voltages balanced, and as a consequence the v_{c2} reaches the voltage level of v_{c1} and v_{c3} in a quarter of a fundamental cycle.

The net dc-bus voltage v_{dc} deviates from its reference v_{dc}^* due to the faulty condition and also due to an imbalance in the capacitor voltages. At $t = 8/60$ s, the v_{dc} recovers back to its reference value with the help of a dc-link PI controller. The capacitor voltages are maintained as balanced even during this transient period (2/60 to 8/60 s). From this operating condition, it can be concluded that the proposed control strategy is robust, and can mitigate the perturbations in the dc-link. Moreover, the reference tracking algorithm is not affected by this faulty condition. The grid currents continue to track to their references as shown in Fig. 8.13(c). As demonstrated in Fig. 8.13(d), during a transient condition, a three-level waveform is noticed due to the divergence of v_{dc} from its reference. But at $t = 8/60$ s, normal operation is restored.

8.4.6 Step-Change in Wind Speed Condition

The dynamic response of the system to a step-change in wind speed is investigated in this section. It is assumed that the system is operating at rated condition until $t = 1.0$ s. The f_{sw} and CMV minimization terms are not included in the cost functions. As shown in Fig. 8.14, until $t = 1.0$ s, the system operates in steady-state, and rated power is delivered to the grid. All the control variables are maintained at the reference values. The mechanical system of the wind turbine is much slower compared to the electrical system, and to better represent the results, a very low moment of inertia ($J = 16.381$ kg.m² which is 14.5 times lower than the original value) is used in the simulations, but this will not affect the system performance [2].

At $t = 1.25$ s, a step change in wind speed is applied from 12 m/s (1.0 p.u.) to 9.6 m/s (0.8 p.u.). Due to the sudden decrease in the wind speed, the MPPT algorithm produces a new speed reference ($\omega_m^* = \frac{\lambda_{T,op}}{r_T} \cdot v_w$) of 12.57 rad/s. This step change in wind speed sets a new electromagnetic torque reference, T_e^* , but the T_e is maintained at its current value to allow the PMSG to decelerate. When the PMSG speed ω_m reaches its reference value, the T_e starts to build up and reaches its new reference value. The electromagnetic torque contains higher torque ripple due to the significant 5th and 7th harmonics in the PMSG currents.

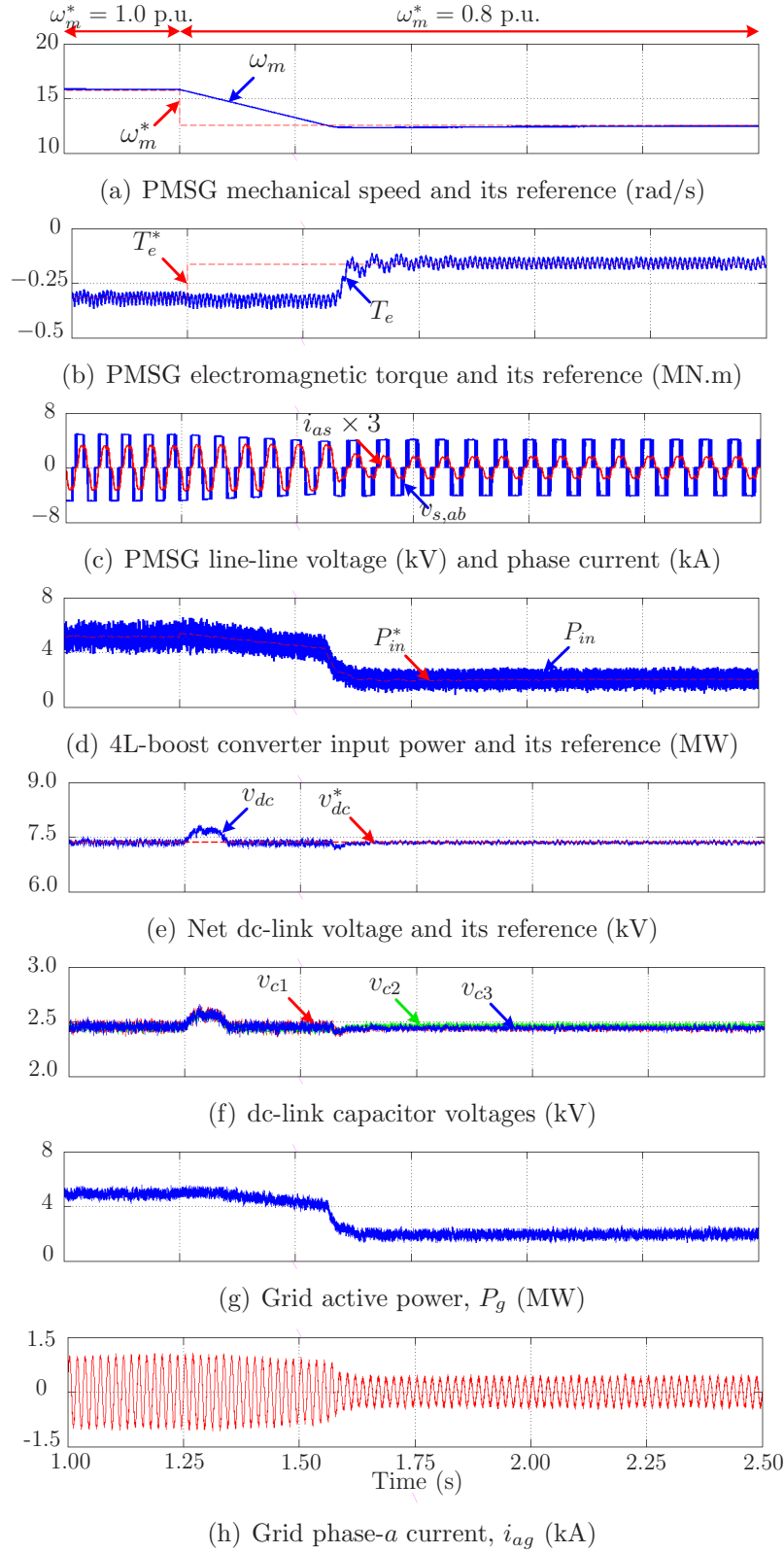


Figure 8.14: Simulation results with step change in wind speed from 12 m/s to 9.6 m/s.

These higher harmonics are caused by the diode-bridge rectifier. This is the only disadvantage of using diode-rectifiers for the PMSG turbines. Due to the decoupled nature of the power converters, these harmonics are not reflected to the grid and thus they do not cause any conflict to the grid codes.

During the time interval 1.25-1.6 s, where the PMSG decelerates to a new reference value, the PMSG line current i_{as} , line-line voltage $v_{s,ab}$, boost converter input power P_{in} , grid power P_g and grid currents decrease at a slow rate. When the PMSG speed reaches new reference value, the P_{in} and P_g settle to a new steady-state value. During this interval, the net dc-bus voltage deviates from its reference value, but the dc-link capacitor voltages are well balanced by the boost converter. The system reaches a new steady-state at $t = 2.25$ s and all the control variables are maintained at the new steady-state operating condition.

8.4.7 Step-Changes in Grid Reactive Power Reference

The grid codes [17] indicate that the wind turbine system should support the grid reactive power when ever requested by the grid operator. The ability of the proposed system to supply unity power factor (UPF), leading power factor and lagging power factor is studied in this section. The simulation results with the step change in grid reactive power reference is shown in Fig. 8.15. The wind speed is considered to be 9.6 m/s (0.8 p.u.), and the active power generated is approximately 2.56 MW (0.8³ p.u.). The f_{sw} and CMV minimization is not considered. A step change in Q_g^* is applied from 0 to -3.075 MVAR (-0.615 p.u.) at $t = 1/60$ s changing the grid power factor from UPF to leading. The grid current leads the grid voltage as shown in Fig. 8.15(b). At $t = 3/60$ s, another step change in Q_g^* is applied from -3.075 MVAR (-0.615 p.u.) to 3.075 MVAR (0.615 p.u.). The grid power is changed from leading to the lagging and the grid current lags the grid voltage [Fig. 8.15(b)]. An excellent dynamic response is noticed for the grid reactive power and currents tracking. During all the operating conditions, the capacitor voltages are well balanced by the boost converter.

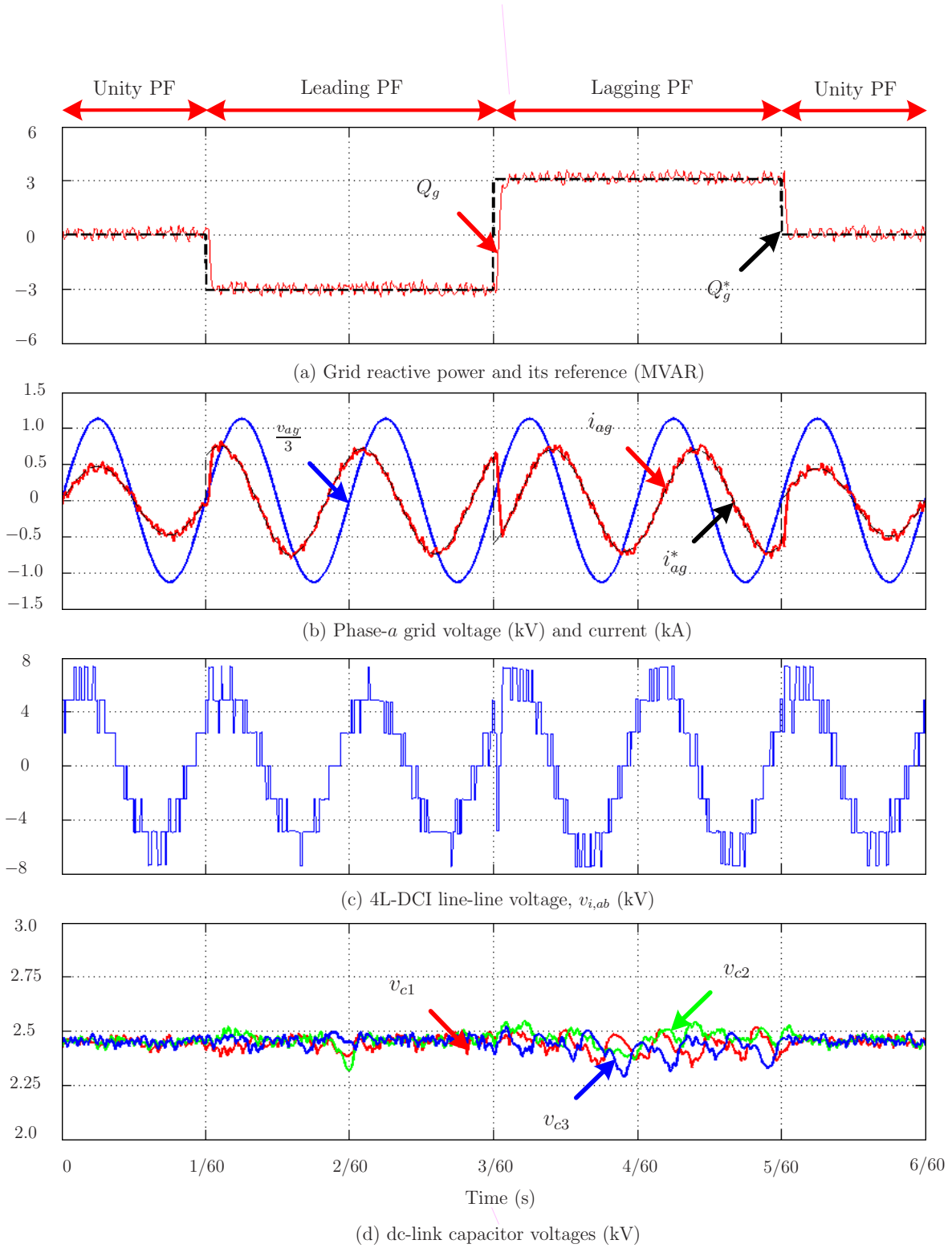


Figure 8.15: Simulation results with step-changes in grid reactive power reference.

8.5 Experimental Implementation

8.5.1 Experimental Platform

As shown in Fig. 8.16, a low power (3.6 kW/208 V/10 A) prototype of PMSG-WECS using the proposed power conversion system is developed. The parameters of the system are given in Table 8.2. Two mechanically coupled PMSGs are used, where initially the PMSG, along with the DSP/FPGA controller, is used as a prime mover to provide the required torque to the second PMSG.

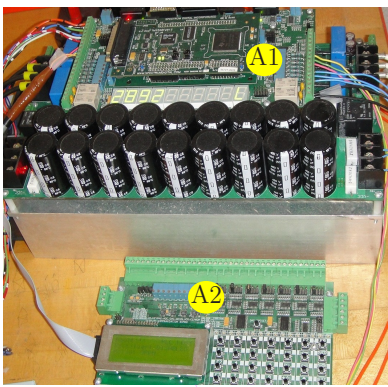
The 4L-BC and 4L-DCI are controlled by a dSPACE DS1003 R&D controller. The control algorithm has been implemented using a host PC running with MATLAB-Simulink software through Real-Time Interface (RTI). The required current and voltage measurements are made by LEM LA55-P and LV25-P sensors, respectively, and sent to the controller through a CP1103 I/O connector. The prototype has been built by Semikron SKM75GB123D dual-pack IGBT modules, SKKD75F12 dual-pack diode modules and SKHI22B dual core gate drivers. The inverter is connected to the grid through an isolation transformer and its impedance is added to the filter values.

8.5.2 Experimental Results

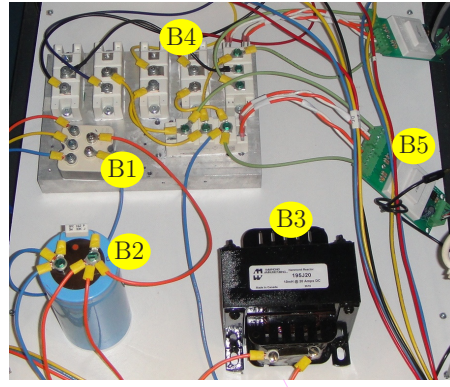
The experimental comparison between one-step prediction and proposed method is presented in Fig. 8.17. With a one-step prediction, and without any f_{sw} minimization algorithm, the switching frequencies for 4L-BC and 4L-DCI are found to 993 and 1380 Hz, respectively. By using a weighting factor of $\lambda_{swc,b} = 0.5$, the f_{sw} for the 4L-boost converter is decreased to 465 Hz. The f_{sw} of 4L-DCI is decreased to 595 Hz by using a $\lambda_{swc,i} = 1.2$. The switching frequencies with the proposed method are noted as 482 and 583 Hz for the 4L-BC and 4L-DCI, respectively.

Similar to the simulation results, the proposed method clearly shows better performance compared to the modified one-step prediction. The P_{in} contains lower ripple, the capacitor voltages are well balanced, and lower dv/dt 's are obtained in the inverter waveform compared to the one-step prediction. The peak magnitude of the harmonics is also lower with the proposed method. The e_{ig} and THD with the one-step prediction are: 3.8% and 6.2%, where, for the proposed method they represent: 2.9% and 4.35%, respectively. The tracking

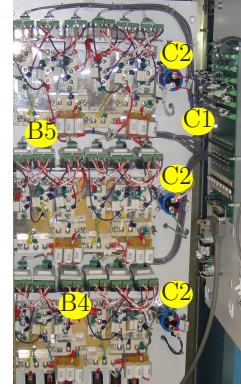
error and THD with the proposed method are higher compared to the simulations due to the delay offered by the current and voltage transducers, dead-time of gate drivers, and losses in the system. These results confirm that the proposed method gives an optimal performance compared to the one-step prediction. Through these results, it has been demonstrated that the current digital platforms can handle the computational capacity of the proposed method. Having the one-step predictive model of the system, the proposed method can be easily extended to any complex system to achieve optimal performance with good quality of the control variables.



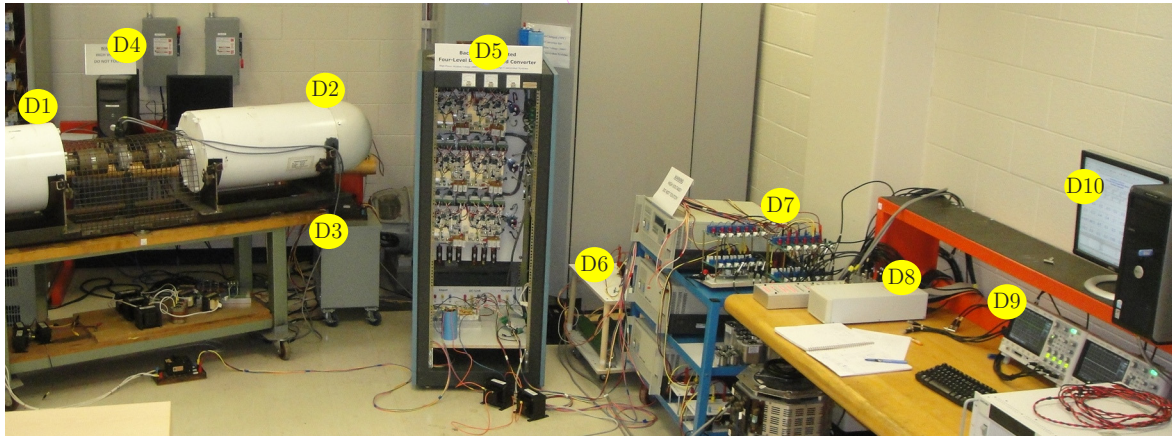
(a) Wind Turbine Simulator



(b) Four-Level Boost Converter



(c) 4L-Inverter



(A1) DSP/FPGA controller, (A2) key board, (B1) three-phase diode-rectifier, (B2) input capacitor, (B3) dc inductor, (B4) semiconductor switches, (B5) IGBT gate drivers, (C1) interface board, (C2) dc-link capacitors, (D1) prime mover, (D2) non-salient pole PMSG, (D3) isolation transformer, (D4) three-phase grid, (D5) power converters, (D6) grid-side filters, (D7) voltage and current transducers, (D8) DS1103 R&D controller, (D9) measurement system, and (D10) MATLAB/Simulink and control desk.

(d) Complete Experimental Platform

Figure 8.16: Photographs of the experimental setup.

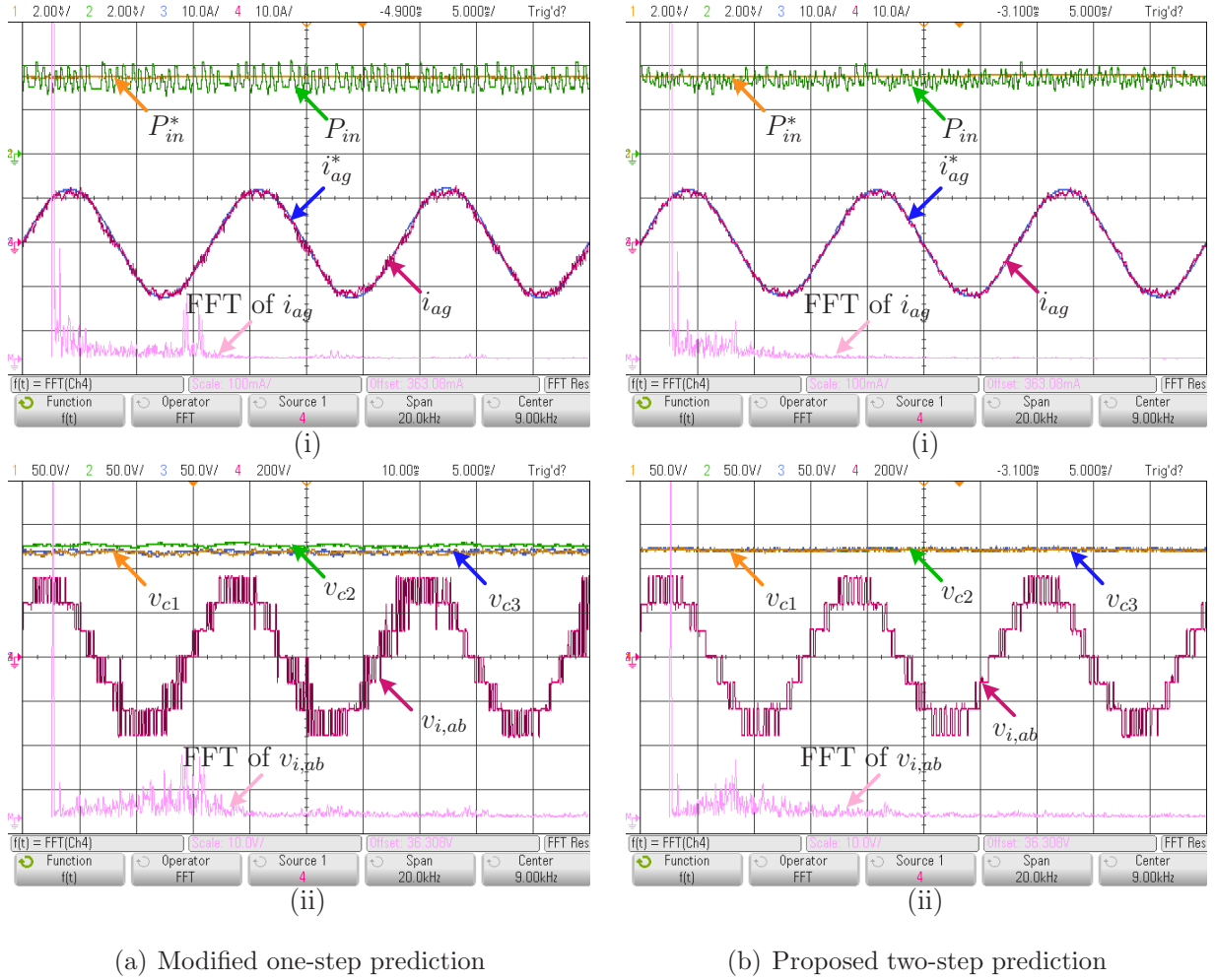


Figure 8.17: Comparison of experimental results during rated wind speed condition.

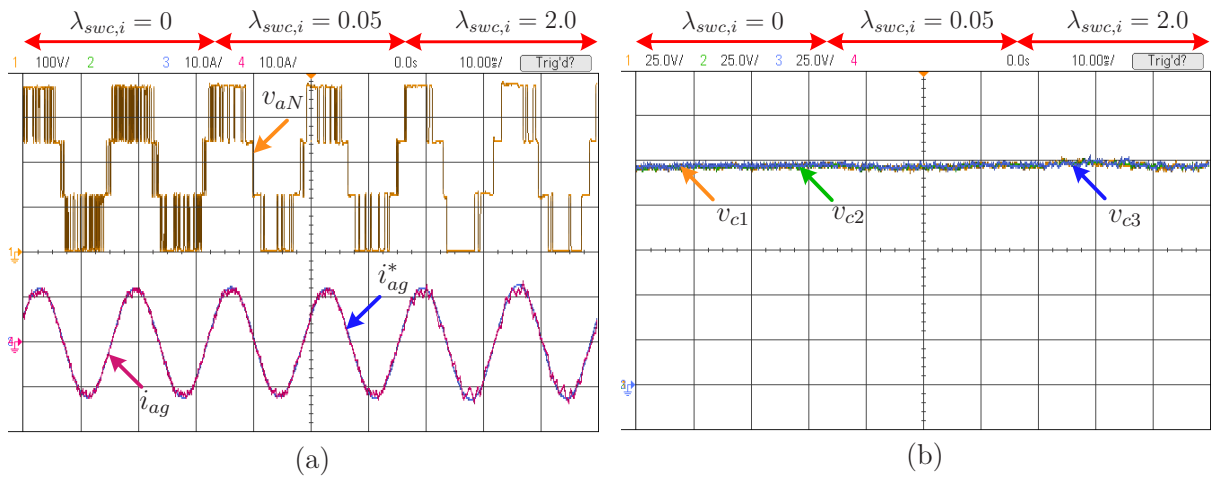


Figure 8.18: Experimental results for grid-tied inverter switching frequency minimization.

The switching frequency minimization algorithm is experimentally tested and presented in Fig. 8.18. The weighting factor $\lambda_{suc,i}$ is changed in the order of: 0, 0.05 and 2. The switching frequencies are minimized in the order of: 583, 375, 146 Hz; e_{ig} is increased in the order of: 2.9 %, 3.7 %, 4.8 %; and THD is increased in the order of: 4.35 %, 5.86 %, 6.72 %. This switching frequency minimization is achieved without any software or hardware reconfiguration. As explained in the simulation results section, the dc-link capacitor voltages are not balanced by the 4L-DCI. This gives fewer numbers of restrictions in the selection of the best switching state. As a result, the power quality is maintained at an acceptable level while minimizing the device switching frequency. This test clearly exhibits that the proposed power conversion system and control strategy is most suitable for megawatt-level applications, where a lower switching frequency operation and high power quality are mandatory.

The CMV minimization is experimentally evaluated and its impact on the grid currents is studied. As shown in Fig. 8.19, with the increase of weighting factor $\lambda_{cmv,i}$ from 0 to 0.0008, the CMV is drastically decreased, but, with little increase in the grid currents reference tracking error (2.9 % to 4.3 %) and THD (4.35 % to 5.63 %). The capacitor voltages are not affected by this CMV minimization algorithm. These experimental results validate the proposed CMV minimization algorithm. This test verifies that the CMV can be minimized to a certain level with the penalization of cost function. This leads to the lower rating and thus lower cost for the external hardware used for the CMV minimization.

The experimental study of the dc-link capacitor voltages balancing algorithm with the faulty dc-link is carried out as shown in Fig. 8.20. The external capacitor C_{ext} is deliberately connected across the dc-link capacitor-2 to resemble the faulty condition. The C_{ext} value is the same as that of C_{dc} . The voltage v_{c2} dropped with the step connection, and recovers back to the voltage level of v_{c1} and v_{c3} . This operation is similar to the simulation results presented in Fig. 8.13. A fast recovery time of 12 ms is noticed. Even during the transient period, where the net dc-bus voltage recovers back to its reference value, the dc-link capacitor voltages are well balanced. Similar to the simulations, the grid currents effectively track to their references even with the faulty dc-link. A robust performance is obtained for the capacitor voltages balancing, and this test validates the simulation results.

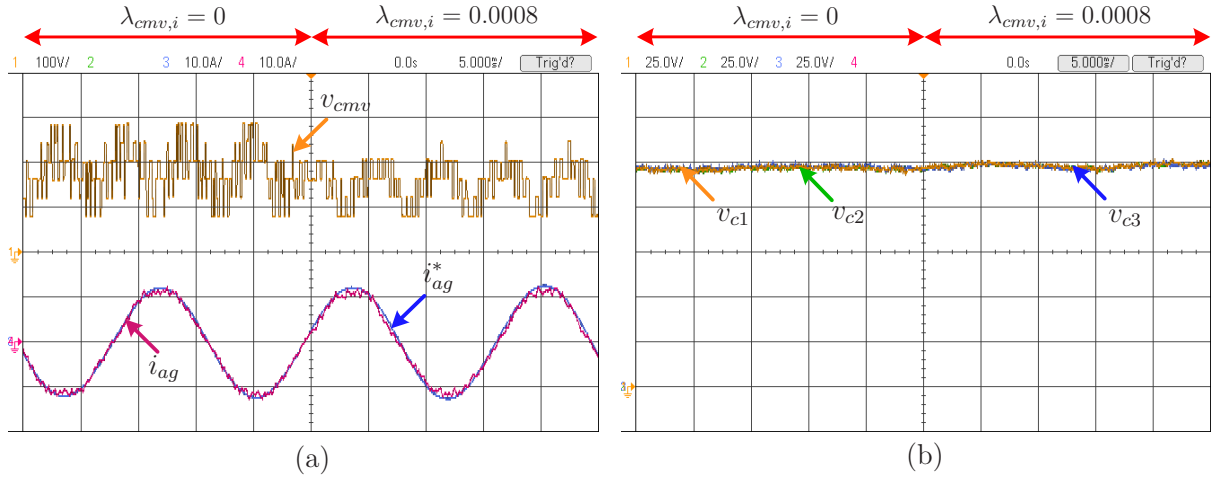


Figure 8.19: Experimental results for grid-tied inverter common-mode voltage minimization.

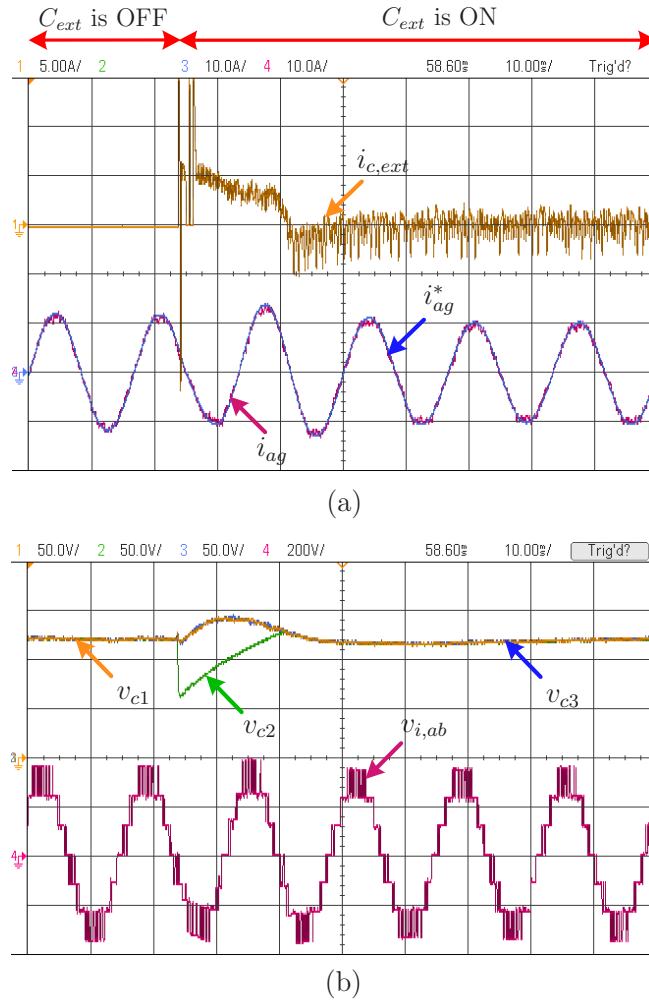


Figure 8.20: Experimental results with step-connection of capacitor C_{ext} across C_{dc2} .

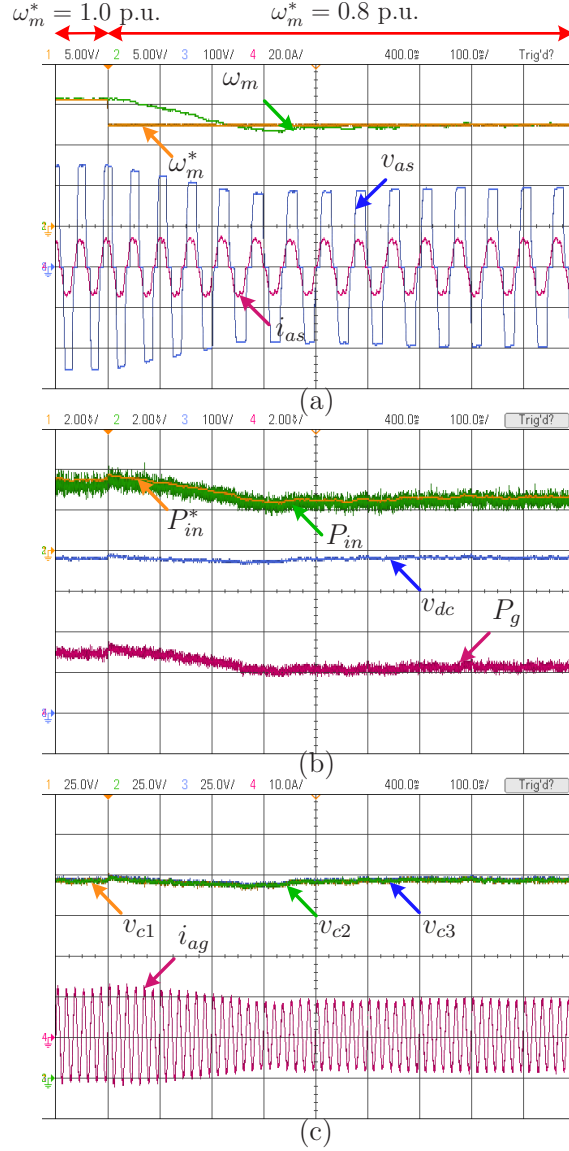


Figure 8.21: Experimental results with step change in ω_m^* from 1.0 to 0.8 p.u..

The experimental dynamic response of the system for a step-change in PMSG speed reference is investigated and presented in Fig. 8.21. The moment of inertia for the PMSG used in the experimental tests is very low compared to the simulations. Due to this, the transient duration is lower compared to the simulations. The time duration of the simulation and experimental tests is 1.5 and 1.0 s, respectively. The reference speed command is directly given by the user. A step change in the speed reference from 1.0 to 0.8 p.u. is provided from the control desk. A similar dynamic response is observed in the experimental test. The control variables shifted their steady-state operation from 1.0 to 0.8 p.u.. The dc-link capacitor voltages are well balanced even during the transient condition.

The experimental results with the step changes in the Q_g^* is presented in Fig. 8.22. The f_{sw} and CMV minimization is not considered. The mechanical speed of the PMSG is maintained at 0.8 p.u. which produces 0.512 p.u. active power. The Q_g^* pattern is similar to the simulation results presented in Fig. 8.15. Also similar to the simulation results, the grid reactive power and currents are tracked to their reference with an excellent dynamic response and no overshoots. The capacitor voltages are well-balanced by the boost converter during all the reactive power conditions. A slight error between the Q_g^* and Q_g results because of the losses in the system. This test verifies that the proposed power converters and control scheme can be used in high power wind turbines to meet the grid code requirements.

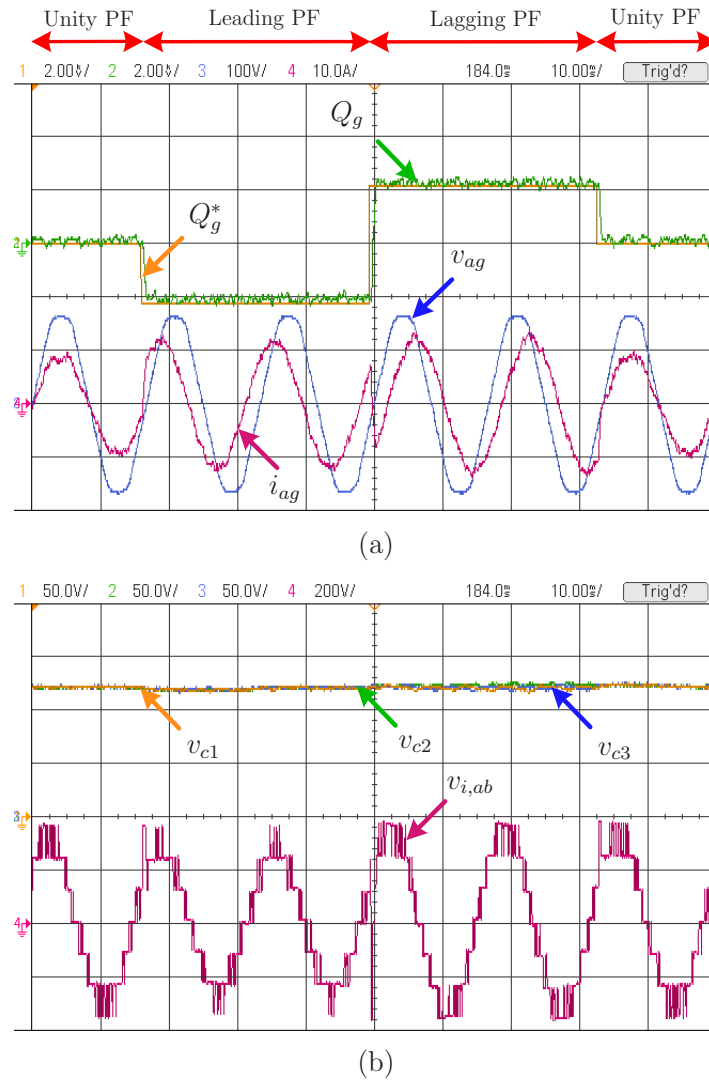


Figure 8.22: Experimental results with step-changes in grid reactive power reference.

8.6 Conclusion

In this chapter, a novel medium voltage power conversion system consisting of diode rectifier, four-level boost converter and four-level diode-clamped inverter is proposed for megawatt-level PMSG wind turbines. The proposed topology combines the advantages of low cost passive generator-side converters and efficient grid-side multilevel operation. The four-level boost converter ensures the balancing of the dc-link capacitor voltages during all the operating conditions. Since the capacitor voltages are balanced by the boost converter, the grid-tied four-level inverter has a control freedom in choosing a best switching state. With this feature, a significant improvement in the grid power quality has been achieved, even with the lower switching frequency operation.

The proposed algorithm can also mitigate the perturbations in the dc-link. A good dynamic and robust response is achieved for capacitor voltages balancing during all operating conditions. A two-step model predictive strategy is proposed and an optimal performance is obtained compared to the one-step prediction. The results also indicate that the current digital signal processors can handle the computational requirement of the proposed two-step prediction. All the control goals are well achieved by minimizing the cost functions during each sampling interval. The proposed methodology appears as a promising tool to control high power converters where the power quality is a major concern. In order to comply with the high power application, the device switching frequencies and common-mode voltages are minimized without involving any external hardware.

Chapter 9

Predictive Control for Low Voltage Ride-Through Enhancement of Three-Level Converter Based WECS

As discussed in Chapter 1, among all the grid codes, the low voltage ride-through (LVRT), also called as fault ride-through, is the major concern for the wind turbine/power converter manufacturers [12–14]. According to LVRT requirements, during grid faults, the wind energy conversion system (WECS) should remain connected to the grid regardless of the turbine/generator/converter configuration being used, and must supply reactive power to help the grid to recover from the voltage dip.

In this chapter, a predictive control scheme is proposed for the LVRT enhancement of direct-driven permanent magnet synchronous generator (PMSG)-based megawatt-level wind turbine. The proposed method uses the turbine-generator rotor inertia to store the surplus energy during the grid voltage dips. The power conversion system is realized using the three-level configuration introduced in Chapter 7. The wind turbine requirements, such as maximum power point tracking, net dc-bus voltage control, balancing of the dc-link capacitor voltages, and reactive power generation, are modeled as the reference control variables. During each sampling interval, these control goals are achieved based on the minimization of generator- and grid-side cost functions. The coordination of generator- and grid-side converters and the exchange of references during normal and LVRT operation is formulated such that the net dc-bus voltage is maintained constant (so as to protect the power converters) while meeting the grid code requirements. Simulation and experimental results are presented to validate the proposed strategy.

9.1 State-of-the-art LVRT Enhancement Methods

Many methods are proposed in literature for the LVRT enhancement of PMSG wind turbines such as [18, 304]: pitch control system, over sizing of dc-link capacitors, dissipation of surplus energy in dc-link crowbar (resistor), storage of surplus energy in the battery banks and fly-wheel systems, use of power quality conditioning devices, and relevant control of power electronic converters. The latter concept has found increased acceptance by industry and academia [52, 67, 293]. Owing to the large moment of inertia, the mechanical system response of the MW direct-driven wind turbines is much slower compared to the electrical system response [2]. Using this feature, the surplus energy can be stored in the mechanical system inertia during the grid voltage dips [67, 293, 305, 306]. This attractive solution, combined with the converter control, is previously analyzed using back-to-back (BTB) connected NPC converters [67] and current source converters [293, 305]. The same concept is studied in [306] for a standard boost converter-based WECS. However, its feasibility is not proved experimentally.

The previously analyzed converter control solutions [67, 72, 293, 305, 306] are based on the classical approach of using cascaded linear regulators and pulse width/ space vector modulation. The predictive control approach for the LVRT enhancement of the grid-tied NPC inverter was previously studied in [299, 307] through simulations. However, the generator-side control and complete WECS response during the grid voltage dips is not analyzed.

In this work, the three-level boost (TLB)-NPC converters are used to realize the power conversion system for PMSG-WECS. The turbine-generator inertia, along with the converter control-based system on predictive control is used to enhance the LVRT capability. The continuous- and discrete-time models of the power converters are presented. The generation of reference control variables and the coordination between the TLB and NPC converters during the normal and LVRT operation is presented. The control objectives for the TLB converter are expressed as generator-side cost function, while the grid-side cost function deals with the NPC inverter control requirements. During each sampling interval, these cost functions are minimized using the actual measurements and predicted quantities (using switching states of the converters). The switching states which minimize these cost functions have been chosen and applied to the TLB and NPC converters directly. To achieve an optimal control performance, as suggested by [303], a two-step predictive model is utilized.

9.2 Configuration of the PMSG-WECS

The power conversion system for the direct-driven PMSG based WECS is shown in Fig. 9.1. More details about the converters are given in Chapter 7.

The pitch control system regulates the output power of the turbine when the wind speed is above its rated value. The magnitude, phase and frequency of the grid voltages are monitored by the grid integration supervisory system. It sends appropriate control signals to the references generation system in the event of grid faults [293]. During the normal and LVRT operation, with the help of the reference generation system, the reference inductor current is generated for the TLB converter, while the reference dq -axis currents are generated for the NPC inverter.

The control objectives for the power converters include:

- TLB Converter:
 - regulation of inductor current, i_{dc}
 - * to achieve maximum power point tracking (MPPT) during normal operation
 - * to store the surplus energy in the turbine-generator rotor inertia during LVRT operation
 - balancing of dc capacitor voltages during all operating conditions to maintain semiconductor device voltage stress within safe limits
- NPC Inverter:
 - regulation of d -axis grid current
 - * to maintain net dc-bus voltage, v_{dc} at its reference value during normal operation
 - * to limit the active power output, P_g during LVRT operation
 - regulation of q -axis grid current to generate reactive power to the grid
 - grid synchronization

The generator- and grid-side controllers take appropriate switching actions in order for the above-mentioned control objectives to be met during normal and LVRT operation. The grid synchronization is carried out as per the guidelines given in [14].

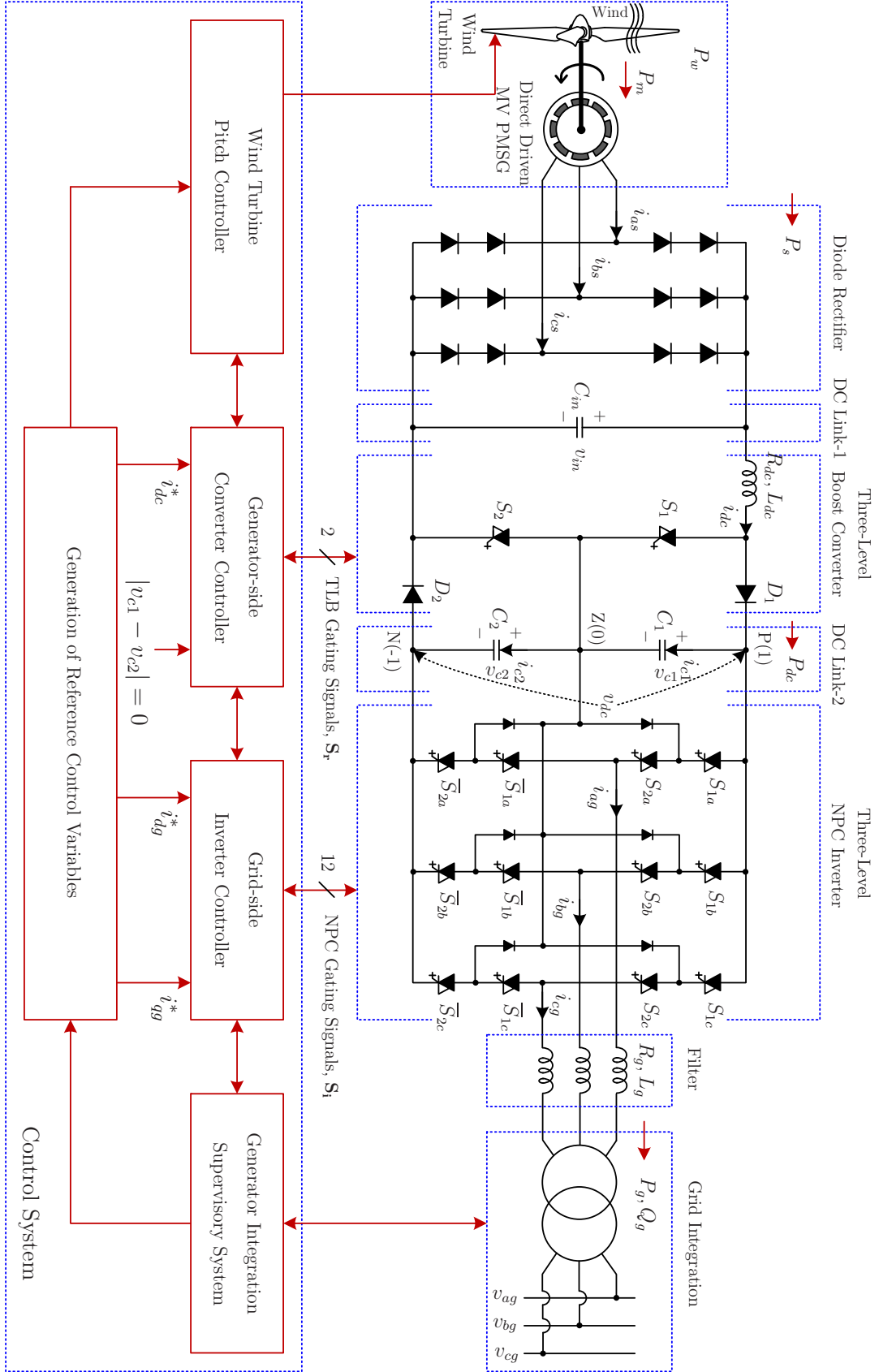


Figure 9.1: Configuration of three-level boost converter and NPC inverter based MW-MV PMSG-WECS.

9.3 Storage of Surplus Energy in Turbine-Generator Rotor Inertia

As discussed in the previous sections, during grid faults the active power injected to the grid is zero ($P_g = 0$). The surplus energy must be managed by the wind turbine system and power converters. By referring to Fig. 9.1, the following analysis can be made:

$$P_w - P_s = P_m = \omega_m J \frac{d\omega_m}{dt} \quad (9.1)$$

where P_w is power captured from the wind, P_m is mechanical input power to the electric generator, P_s is active power output of the generator, J is turbine-generator moment of inertia, and ω_m is mechanical shaft speed. If P_s is decreased without altering the power captured from the wind (P_w), then the mechanical power ($P_m = P_w - P_s$) increases, and this scenario leads to an increase in the turbine-generator shaft-speed from $\omega_{m,R}$ to $\omega_{m,max}$ [67]:

$$\int P_m dt = \frac{1}{2} J (\omega_{m,max}^2 - \omega_{m,R}^2) \quad (9.2)$$

where $\omega_{m,max}$ is the maximum value of shaft speed during grid fault, and $\omega_{m,R}$ is rated shaft speed.

The relation between maximum shaft-speed $\omega_{m,max}$ and fault duration ($dt = t_f$) can be obtained from (9.2) as follows:

$$\omega_{m,max} = \sqrt{\frac{2 P_m t_f}{J} + \omega_{m,R}^2}. \quad (9.3)$$

In the practical MW direct-driven wind turbines, the value of inertia constant H ($= \frac{J\omega_{m,R}^2}{2P_m}$) is in the range of 5-6 seconds [2, 67, 293, 305], and it will maintain the shaft speed to a safe limit.

9.4 Control System for the PMSG-WECS

The control systems for the generator- and grid-side converters are presented here. They force the converters to track to the references during normal and LVRT operation.

9.4.1 Generator-side Converter Controller

The proposed control system for the generator-side converter control is shown in Fig. 9.2. The control objectives for the TLB converter are included in the generator-side cost function as follows:

$$g_{gen}(k) = [i_{dc}^*(k+2) - i_{dc}(k+2)]^2 + \lambda_{dc} * [v_{c1}(k+2) - v_{c2}(k+2)]^2 \quad (9.4)$$

where $i_{dc}^*(k+2)$ is the extrapolated reference inductor current, $i_{dc}(k+2)$ is the predicted inductor current, $v_{c1}(k+2)$ and $v_{c2}(k+2)$ are the predicted dc-link capacitor voltages, and λ_{dc} is the weighting factor for the balancing of capacitor voltages. The weighting factor λ_{dc} substantiates the importance of the secondary objective (balancing of dc-link capacitor voltages) over the primary control requirement (regulation of i_{dc}). Equal importance will be given to primary and secondary objectives when $\lambda_{dc} = 1$, but this scenario leads to a poor performance for the primary goal. By setting $\lambda_{dc} = 0$, a very good response can be obtained for the primary objective, but the dc-link capacitor voltages cannot be regulated. In this work, the value for λ_{dc} is chosen as 0.1 to ensure acceptable balancing for the dc-link capacitor voltages and good reference tracking for i_{dc} .

Predictions for the future behavior of the inductor current and dc capacitor voltages can be obtained as follows:

$$\begin{bmatrix} i_{dc}(k+h) \\ v_{c1}(k+h) \\ v_{c2}(k+h) \end{bmatrix} = \Phi_{\mathbf{b}} \begin{bmatrix} i_{dc}(k+h-1) \\ v_{c1}(k+h-1) \\ v_{c2}(k+h-1) \end{bmatrix} + \Gamma_{\mathbf{b}} \begin{bmatrix} v_{in}(k+h-1) \\ i_{o1}(k+h-1) \\ i_{o2}(k+h-1) \end{bmatrix} \quad (9.5)$$

where h is the prediction horizon length. Φ_b and Γ_b are given in (7.11).

The dynamic systems in (9.5) suggests that the generator-side control variables (i_{dc} , v_{c1} and v_{c2}) do not require the model of the PMSG and the wind turbine. This feature greatly simplifies the complexity of the control system compared to the one used with the BTB-NPC

converters. The current state (k) measurements and the four switching states are used in the prediction of future behavior of the control variables. With the optimal selection of switching signals, the control variables can be effectively controlled.

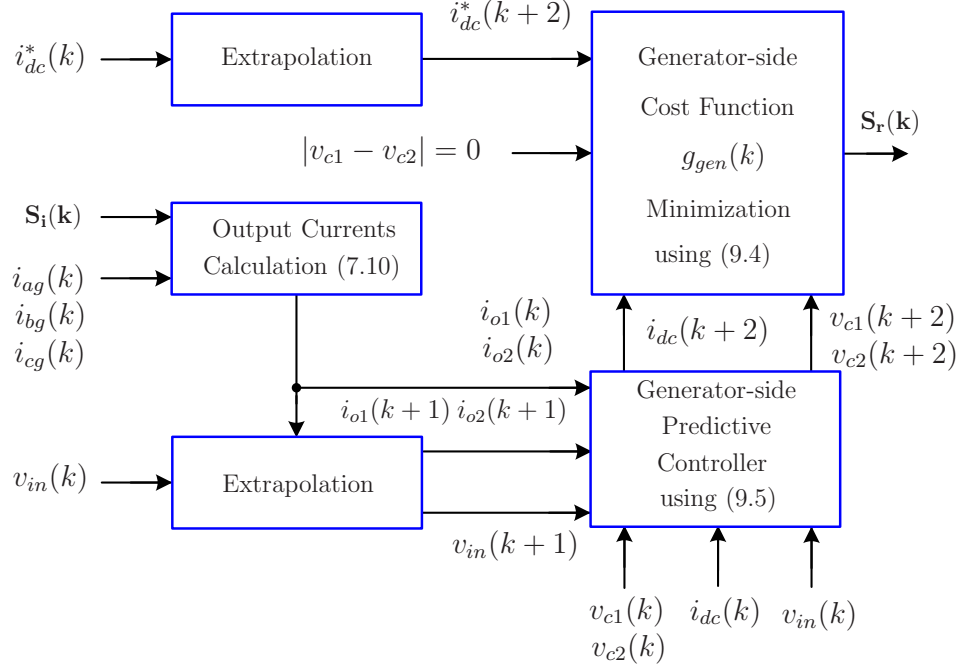


Figure 9.2: Proposed model predictive controller for the generator-side converter.

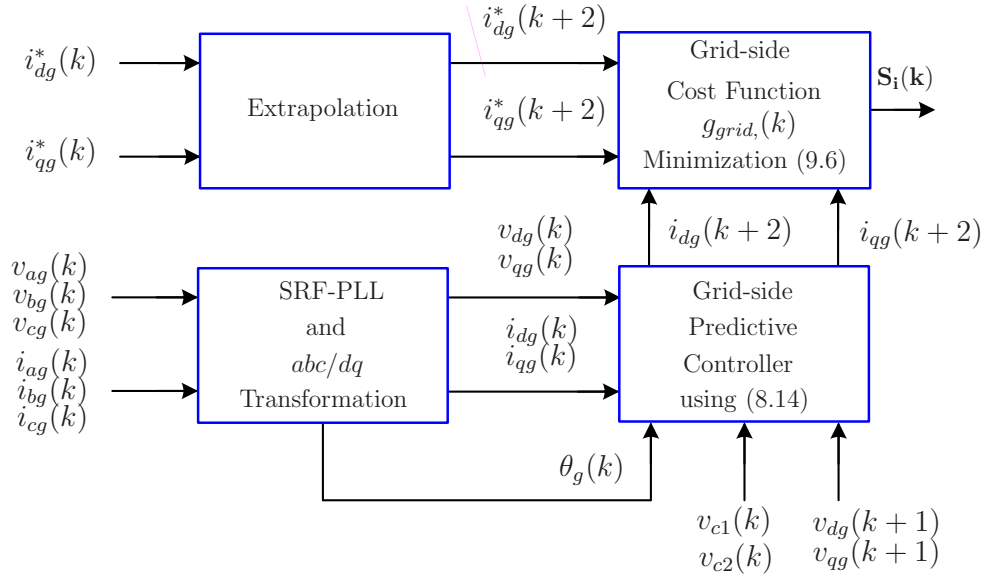


Figure 9.3: Proposed model predictive controller for grid-side inverter.

9.4.2 Grid-side Inverter Controller

The proposed grid-side inverter controller is shown in Fig. 9.3. The grid-side inverter is used to control the d - and q -axis currents. This control objective is expressed as a grid-side cost function:

$$g_{grid}(k) = [i_{dg}^*(k+2) - i_{dg}(k+2)]^2 + [i_{qg}^*(k+2) - i_{qg}(k+2)]^2 \quad (9.6)$$

where $i_{dg}^*(k+2)$ and $i_{qg}^*(k+2)$ are the extrapolated reference currents, and $i_{dg}(k+2)$ and $i_{qg}(k+2)$ are the predicted dq -axis currents. The prediction for dq -axis grid currents is obtained according to the models given in Chapter 8.

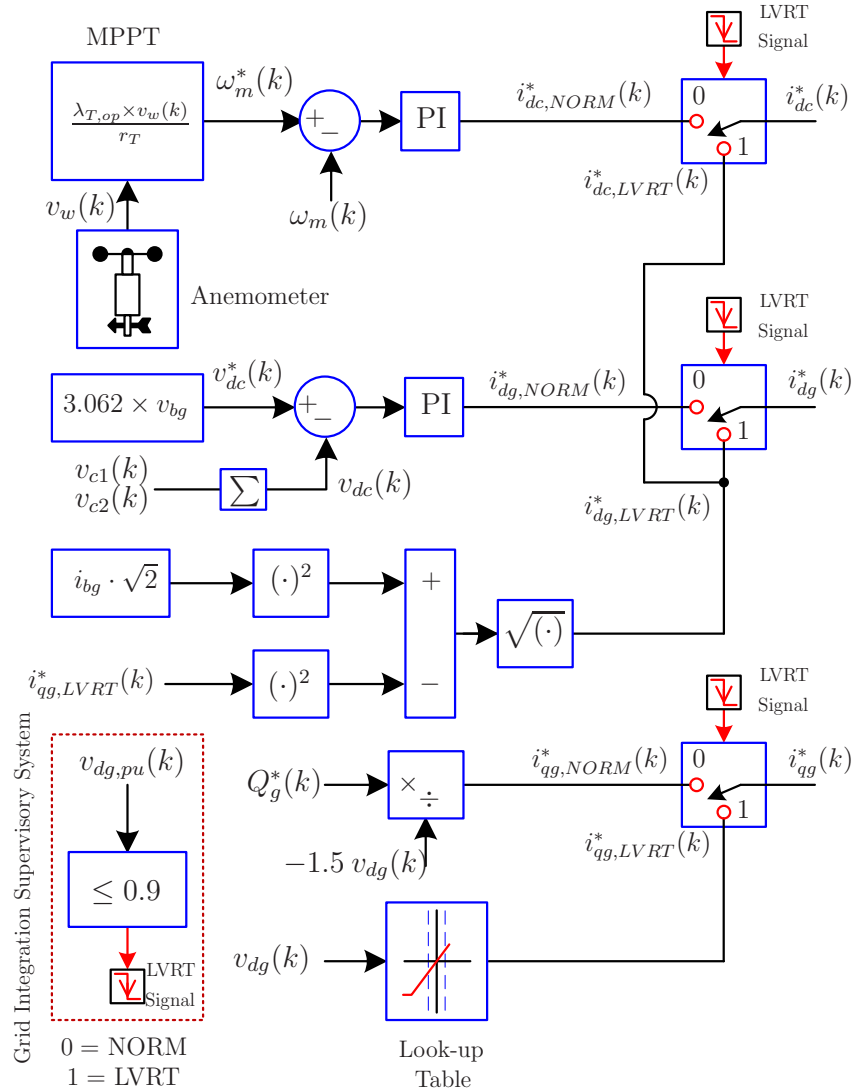


Figure 9.4: Generation of reference control variables during normal and LVRT operation.

9.5 Generation of Reference Control Variables

In the previous section, the generator- and grid-side cost functions are designed based on the assumption that the references are readily available. The generation of such references is very important in order to allow for the safe operation of power converters and wind turbines, and also to meet the grid codes. The block diagram of the references generation system is shown in Fig. 9.4.

9.5.1 Normal Operation

The maximum power point tracking (MPPT) is an important issue in variable speed WECS. In this research an optimal tip-speed-ratio (OTSR) MPPT algorithm [51] is used. This algorithm provides reference speed based on the measured wind speed. As shown in Fig. 9.4, a speed regulator (PI) generates the corresponding inductor current reference. The PMSG speed, current and electromagnetic torque can be regulated by tracking this reference. The dq -axis grid current references are generated by a method similar to the classical voltage oriented control [2]. Through the PI controller-based regulation of net dc-bus voltage, the d -axis reference current is generated. With the Q_g^* command provided by the grid operator, the q -axis reference current is obtained.

9.5.2 LVRT Operation

The TSOs and DSOs of diverse countries issue different LVRT profiles [13] based on the experience acquired through the operation of their power systems. The LVRT profiles can be broadly classified into six different categories as shown in Fig. 1.5. Despite their different shapes, they all share a common purpose and background, i.e., to keep the electric power system stable and secure during the grid fault conditions.

Among all the LVRT profiles, the German Transmission and Distribution Utility (E.ON) regulation [17] is likely to set the standard. According to this grid code, the LVRT function should start when the grid voltage falls below 90 % of its nominal value. For the grid voltages in the range of 50 – 90 %, the generation system should provide 2 % reactive current for each 1 % voltage dip, and when the grid voltage falls below 50 %, the system should provide 100 % reactive current. In this work, the dq -axis reference grid currents are produced according to the E.ON grid code and shown in Fig. 9.4.

9.6 Simulation Results

To validate the proposed converter and control scheme during grid voltage dips, simulation results are presented using MATLAB/Simulink. The parameters of the PMSG-WECS are shown in Table 9.1. To better compare the simulation and experimental results, the computational delay caused by the real-time digital signal processor is considered in the simulation tests, and this value is set to one sampling period, T_s . Two-step predictive models are used in all the tests. To reduce simulation run time, the original moment of inertia is reduced to 14.5 %. The PMSG-WECS is assumed to be operating at the rated wind speed condition. The average switching frequencies for the TLB and NPC converters are noted as: 253 and 740 Hz, respectively. The average switching frequencies can be minimized to lower values by including extra constraint in the cost functions $g_{gen}(k)$ and $g_{grid}(k)$. The grid current THD is found to be 4.41 %.

9.6.1 Analysis with Generator-side LVRT Controller Disabled

In the first test, as demonstrated in Figs. 9.5 and 9.6, the generator-side LVRT controller is disabled meaning that $i_{dc}^*(k) = i_{dc,NORM}^*(k)$, and the grid-side LVRT controller is enabled ($[i_{dg}^*(k) = i_{dg,LVRT}^*(k) \text{ and } i_{qg}^*(k) = i_{qg,LVRT}^*(k)]$ (refer to Fig. 9.4). As shown in Fig. 9.5(a), a dip in the grid voltage is applied from 100 % to 10 % at $t = 2.0$ s, with a duration of 150 ms.

Since the generator-side references correspond to the MPPT operation, the PMSG shaft speed (ω_m), electromagnetic torque (T_e), stator voltage ($v_{s,ab}$), stator current (i_{as}) and input dc voltage (v_{in}) do not respond to the LVRT operation as depicted in Fig. 9.6. The PMSG currents contain significant 5th and 7th harmonics (mainly caused by the diode-bridge rectifier) which leads to higher ripple in T_e . The use of diode rectifier also leads to the clipping of the generator terminal voltage. The shape of the generator voltage changes according to the configuration of the diode rectifier, C_{in} value and the operating condition [68]. This is the only disadvantage of using diode-rectifiers for the PMSG turbines. Due to the decoupled nature of the power converters, these harmonics are not reflected to the grid, and thus they do not cause any conflict to the grid codes.

During the voltage dip, the active power injected to the grid is zero [$i_{dg}^*(k) = 0$] [Fig. 9.5(b)], but, the PMSG injects rated power into the dc-link. According to the power balance

Table 9.1: Parameters of the proposed PMSG-WECS

		Simulation		Experimental	
Variable	Description	SI	p.u.	SI	p.u.
Wind Turbine Parameters					
P_M	Rated Power (kW)	3000	1.0	3.6	1.0
T_M	Rated Torque (kN.m)	1273.3	1.0	0.2292	1.0
N_M	Rated Speed (rpm)	22.5	1.0	150	1.0
R_{gb}	Gear Ratio	1		1	
r_T	Rotor Radius (m)	43.3553		–	
ρ	Air Density (kg.m ²)	1.225		–	
$C_{p,op}$	Optimal Power Coefficient	0.48		–	
$\lambda_{T,op}$	Optimal Tip Speed Ratio	8.5128		–	
Permanent Magnet Synchronous Generator Parameters					
P_m	Rated Mechanical Power (kW)	3000		3.6	
P_s	Rated Output Active Power (kW)	2962		3.527	
v_{sl}	Rated Line-Line Voltage (V)	3000		208	
v_s	Rated Phase Voltage (V)	1732.2	1.0	120	1.0
i_s	Rated Stator Current (A)	582	1.0	10	1.0
f_s	Rated Stator Frequency (Hz)	9.75	1.0	20	1.0
PF_s	Rated Power Factor	0.98		0.98	
$n_{m,R}$	Rated Rotor Speed (rpm)	22.5	1.0	150	1.0
PP	Number of Pole Pairs	26		8	
$T_{m,R}$	Rated Mechanical Torque (kN.m)	1273.24	1.0	0.2292	1.0
λ_r	Rated rms Rotor Flux Linkage (Wb)	28.059	1.0	0.956	1.0
R_s	Stator Winding Resistance (mΩ)	37.521	0.013	245	0.021
L_d	d -axis Synchronous Inductance (mH)	9.75	0.2	19.1	0.2
L_q	q -axis Synchronous Inductance (mH)	9.75	0.2	19.1	0.2
J	Moment of Inertia (kg.m ²)	6327			
H	Inertia Time Constant (s)	5.81			
Λ_{bs}	Base Flux Linkage (Wb)	28.059	1.0	0.956	1.0
Z_{bs}	Base Impedance (Ω)	2.978	1.0	12.024	1.0
L_{bs}	Base Inductance (mH)	48.606	1.0	95.683	1.0
C_{bs}	Base Capacitance (μF)	5481.9	1.0	661.83	1.0
$v_{bs,peak}$	Peak Base Voltage (V)	2449.7	1.414	169.9	1.414
$i_{bs,peak}$	Peak Base Current (A)	823.1	1.414	14.14	1.414
Medium Voltage Grid Parameters					
S_g	Rated Apparent Power (kVA)	3000	1.0	3.6	1.0
v_{gl}	Rated Line-Line Voltage (V)	3000		208	
v_g	Rated Phase Voltage (V)	1732.2	1.0	120	1.0
i_g	Rated Stator Current (A)	577.35	1.0	10	1.0
f_g	Rated Stator Frequency (Hz)	60	1.0	60	1.0
Z_{bg}	Base Impedance (Ω)	3	1.0	12.018	1.0
L_{bg}	Base Inductance (mH)	7.96	1.0	31.88	1.0
C_{bg}	Base Capacitance (μF)	884.19	1.0	220.72	1.0
$v_{bg,peak}$	Peak Base Voltage (V)	2449.7	1.414	169.9	1.414
$i_{bg,peak}$	Peak Base Current (A)	816.5	1.414	14.14	1.414
Rectifier and Inverter Parameters					
C_{in}	Input Capacitance (base: C_{bs}) (μF)	18828	3.43	4700	3.43
C_{dc}	Output dc-link Capacitance (μF)	4006	4.53	1000	4.53
R_{dc}	Boost Filter Leakage Resistance (Ω)	0.3	0.01	0.12	0.01
L_{dc}	Boost Filter Inductance (mH)	2.5	0.31	10	0.31
R_g	Grid-side Filter Resistance (Ω)	0.027	0.009	0.108	0.009
L_g	Grid-side Filter Inductance (mH)	1.65	0.207	6.6	0.207
Controller Parameters					
h	Prediction horizon length	2		2	
T_s	Sampling Time (s)	100 μ		100 μ	
λ_{dc}	Weighting Factor	0.1		0.1	
v_{dc}^*	Reference dc-link Voltage (V)	5304	3.062	367	3.062

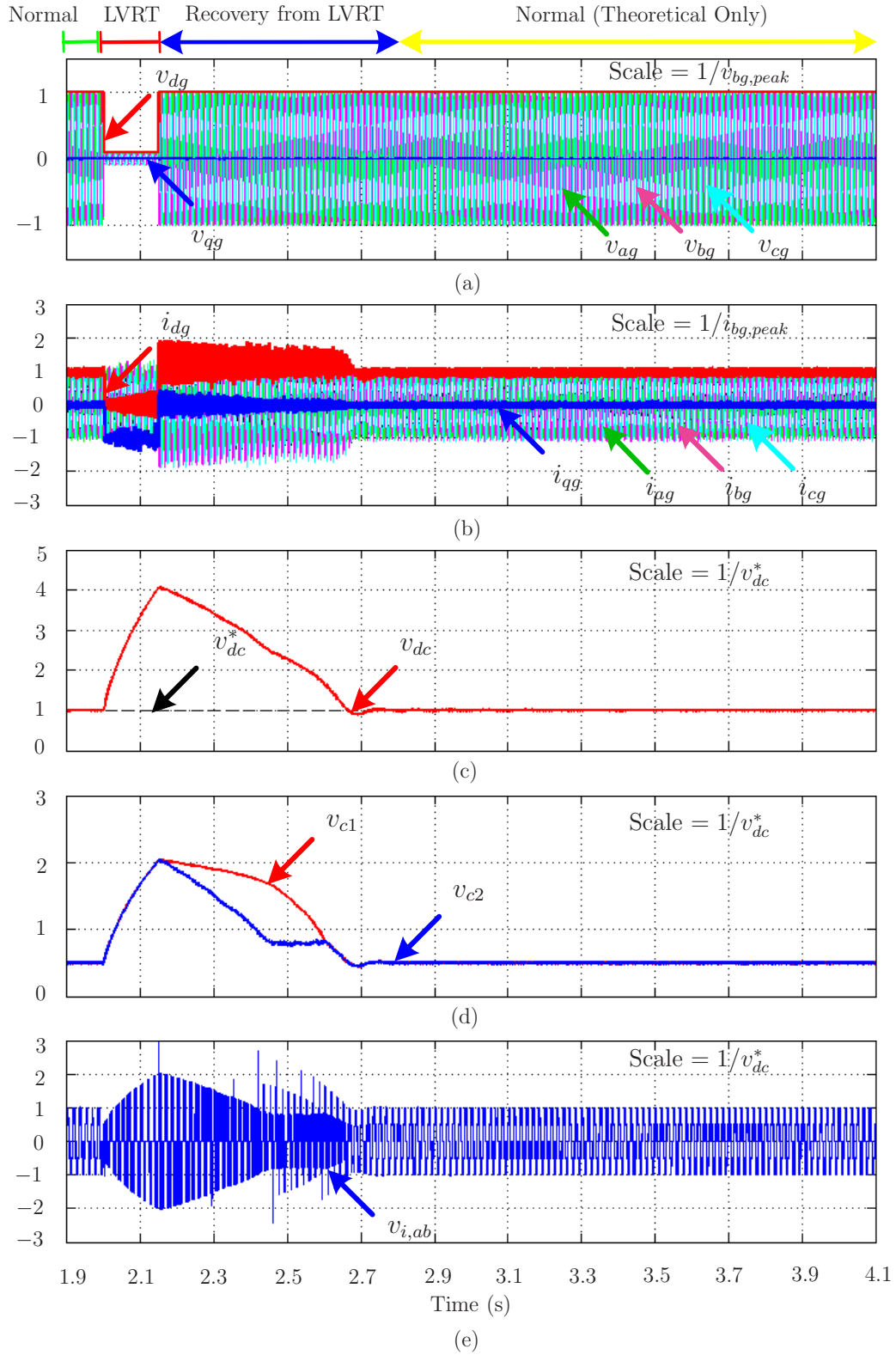


Figure 9.5: Simulation results during three-phase grid voltage dip with the generator-side LVRT controller disabled (Part-I).

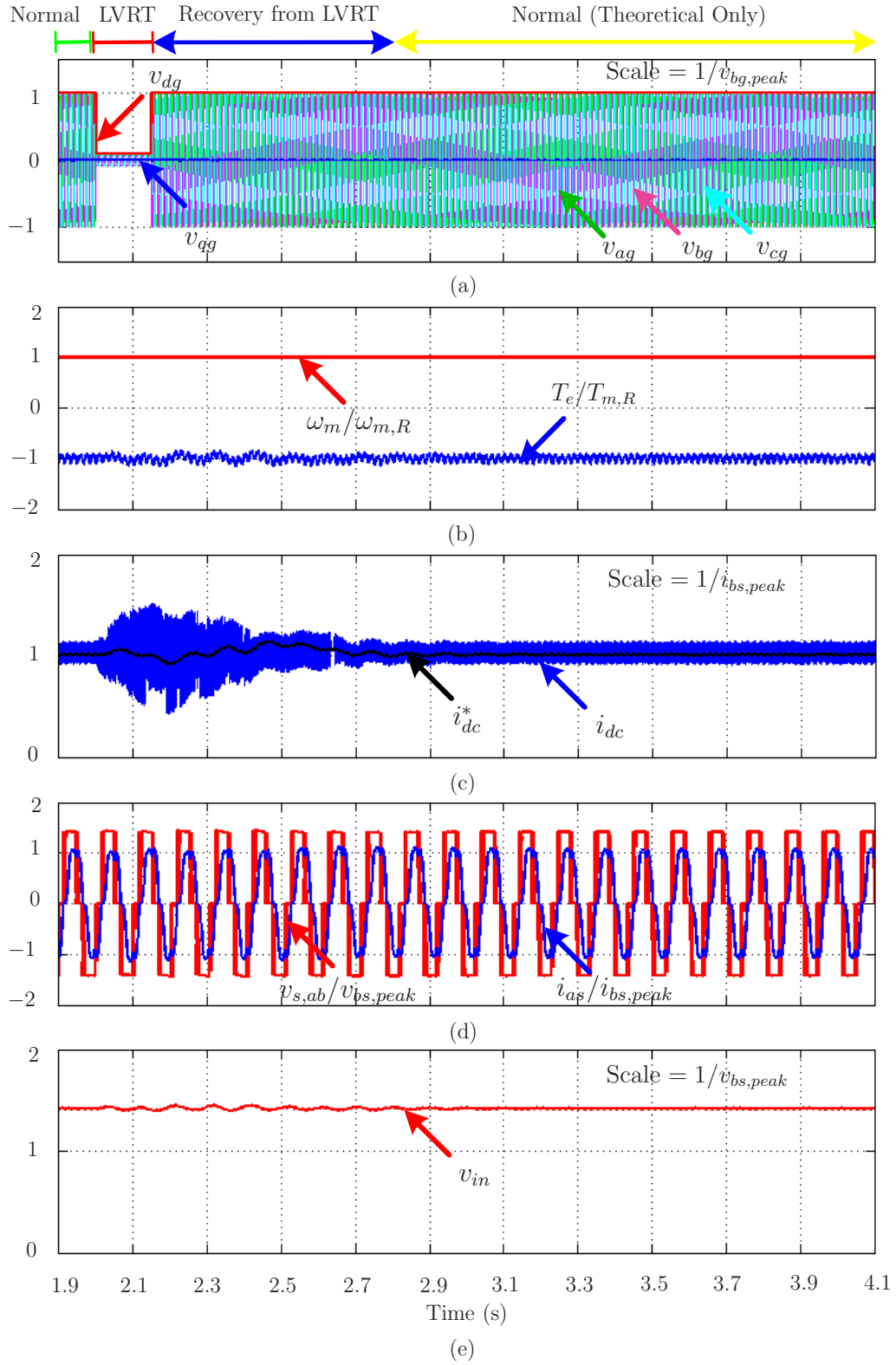


Figure 9.6: Simulation results during three-phase grid voltage dip with the generator-side LVRT controller disabled (Part-II).

theorem, the surplus energy should be stored in the dc-bus. As a consequence, the net dc-bus voltage is increased to 4 times its rated value [Fig. 9.5(c)], and in real systems, this will destroy both the TLB and NPC converters. For this reason, some works proposed to dissipate this surplus energy using a resistor in the dc-link (crowbar), and some other works proposed to store this energy in the battery banks [18, 304].

As shown in Fig. 9.5(d), the v_{c1} and v_{c2} are balanced by the TLB converter even during the divergence period ($t = 2.0$ to 2.15 s). Due to the significant increase in v_{c1} and v_{c2} , the inverter voltage magnitude [refer to Eq. (7.1)], the ripple in inductor current [Eq. (9.5)], and the ripple in dq -axis grid currents [Eq. (8.14)] increases. This scenario leads to non-compliance of grid codes, in addition to the failure of power converters.

At $t = 2.15$ s, the grid voltages recover back to its normal operating condition. The saturation limits of the dc-bus PI controller is set to 1.5 times $i_{bg,peak}$. This helps to quickly discharge the capacitor voltages by injecting more active power to the grid. In theory, the system returns back to its normal operation at $t = 2.8$ s (only if the power converters do not fail during the LVRT operation).

9.6.2 Analysis with Generator-side LVRT Controller Enabled

The simulation results using the generator-side LVRT controller are presented in Figs. 9.7 and 9.8. The reference control variables are: $i_{dc}^*(k) = i_{dc,LVRT}^*(k)$, $i_{dg}^*(k) = i_{dg,LVRT}^*(k)$ and $i_{qg}^*(k) = i_{qg,LVRT}^*(k)$. The profile of grid voltage is similar to the previous case. Since the PMSG speed control loop is disabled, the surplus energy is stored in the inertia of turbine and generator. As shown in Fig. 9.8(b), with the reduced inertia constant $H = 0.4$, the PMSG speed increases to 17 % above its rated value. This can be theoretically conformed as:

$$\begin{aligned}\omega_{m,R} &= \frac{n_{m,R} \times 2 \times \pi}{60} = 2.3562 \text{ rad/s} \\ J &= \frac{H \times 2 \times P_m}{\omega_{m,R}^2} = 432.3 \text{ kg.m}^2 \\ \omega_{m,max} &= \sqrt{\frac{2 P_m 150 \times 10^{-3}}{J} + \omega_{m,R}^2} = 2.7629 \text{ rad/s} \\ \frac{\omega_{m,max} - \omega_{m,R}}{\omega_{m,R}} \times 100 &= 17.3 \text{ \%}.\end{aligned}$$

By using the original value of $H = 5$ [2, 67, 293, 305], the percentage increase in ω_m can be obtained as 1.48 % and 6.02 % for the fault durations of 150 ms and 625 ms, respectively.

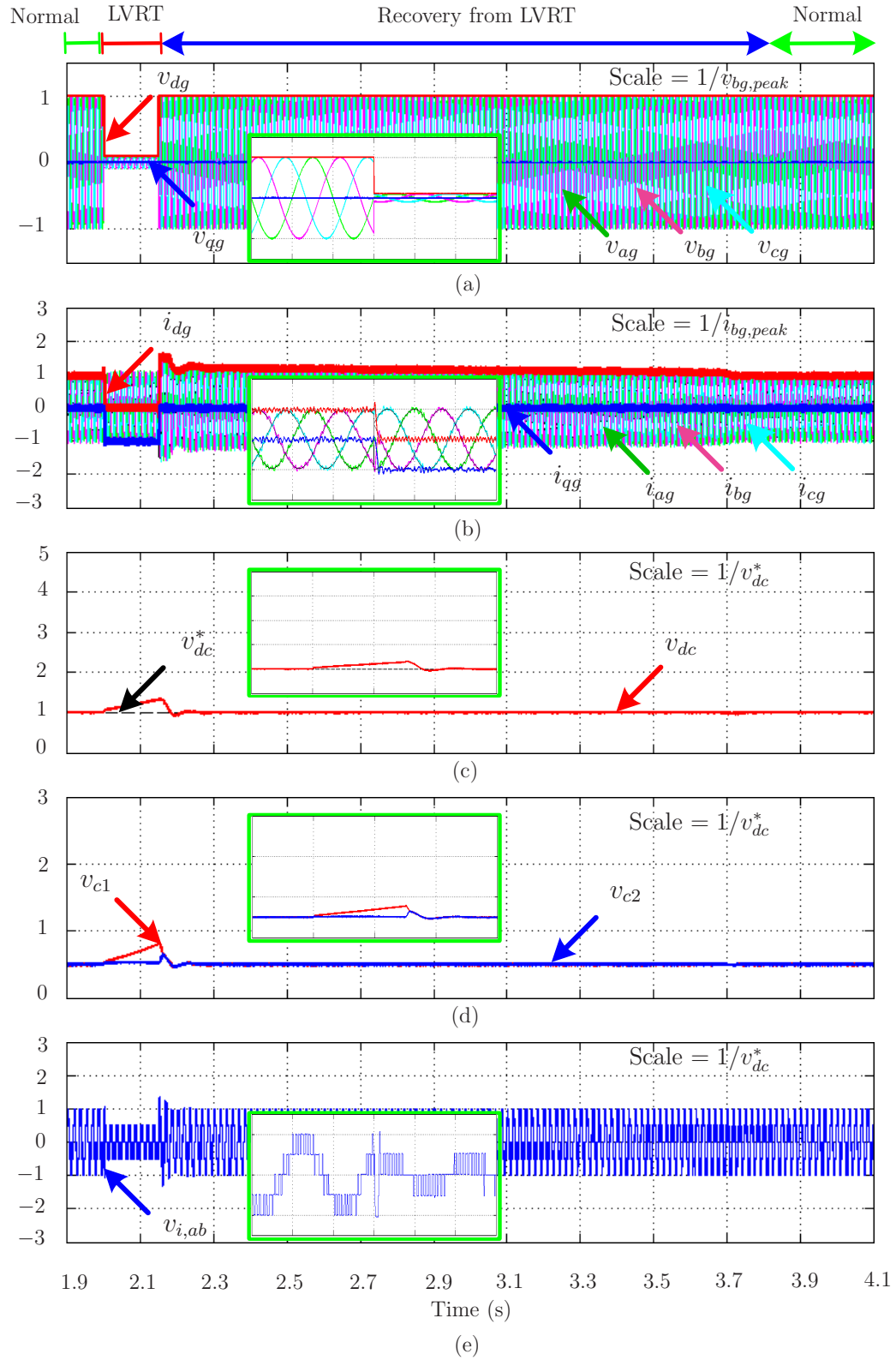


Figure 9.7: Simulation results during three-phase grid voltage dip with the generator-side LVRT controller enabled (Part-I).

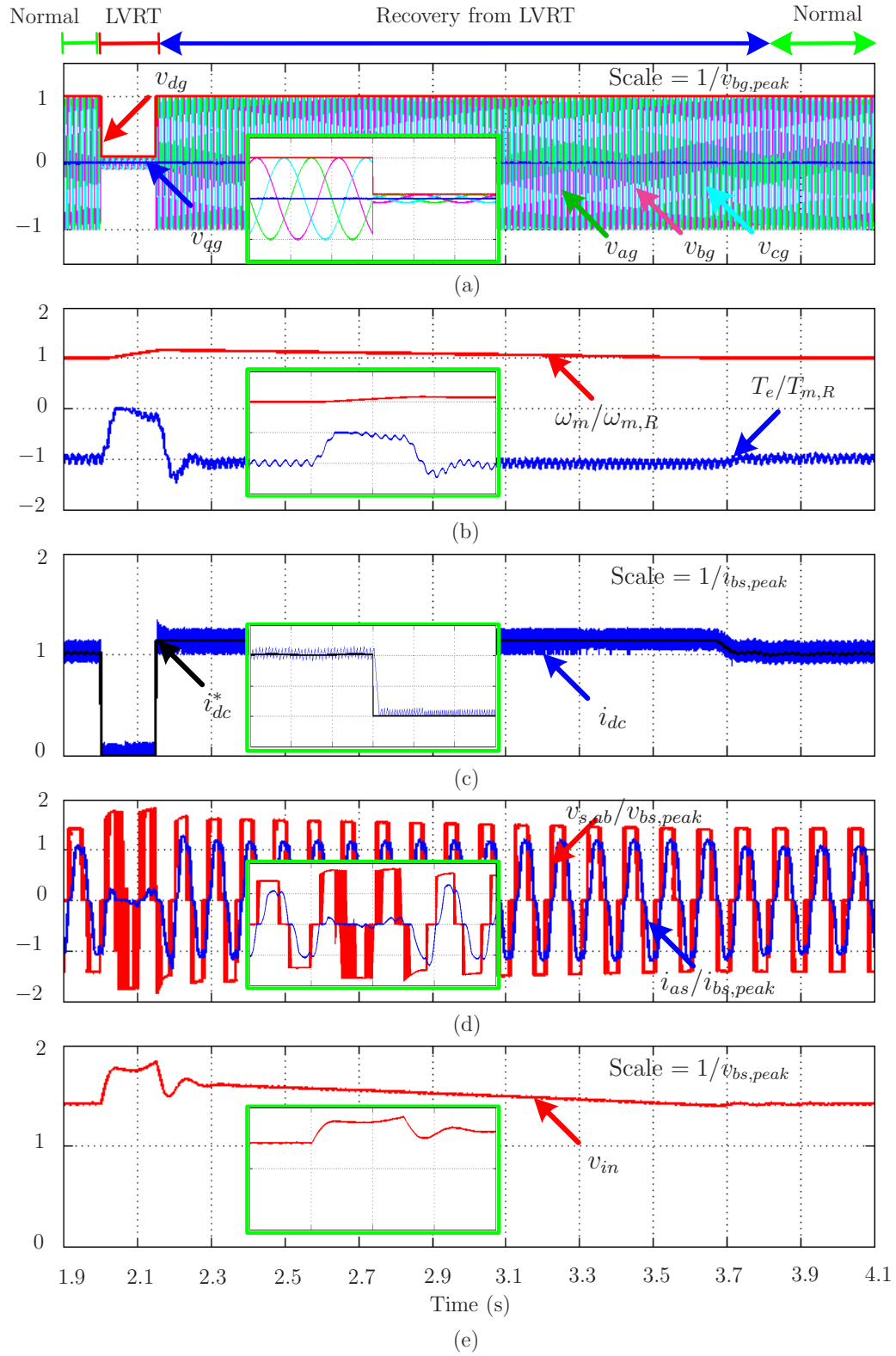


Figure 9.8: Simulation results during three-phase grid voltage dip with the generator-side LVRT controller enabled (Part-II).

This analysis conforms that the turbine-side mechanical system response is much slower compared to the grid-side electrical system response.

During the LVRT interval, $t = 2.0$ to 2.15 s, the electromagnetic torque is maintained at zero to allow the PMSG to accelerate as shown in Fig. 9.8(b). The active power generated by the PMSG is zero, and this can be understood from the zero values of PMSG and inductor currents [Fig. 9.8(d)]. The magnitude of the net dc-bus voltage is maintained within safe limits, and the dq -axis grid currents track to their reference values with minimal ripple. During the step-change in references at $t = 2.0$ s, the inductor and grid currents follow their references accurately (shown in box). The input dc voltage magnitude increases with respect to the generator speed, but, this increase is in the acceptable limits. During the recovery from the LVRT operation ($t = 2.15$ s onwards), the inductor current reference is maintained at its higher saturation level to help the PMSG to decelerate rapidly. At $t = 3.8$ s, the system recovers back to normal operation without causing any failures to the power electronic converters.

These results confirm that the proposed converters and predictive control can be used efficiently in the MW PMSG-WECS. For the compliance with new grid code requirements, the rather old concept of storing energy in the inertia of rotating masses is applied to wind energy system, and this approach eliminates the cost and complexity associated with the conventional approach of dc-link crowbar. This method is more efficient because no energy is dissipated in the crowbar. Moreover, the proposed approach is safe because most of the commercial wind turbines are equipped with the over-speed capability. For example, the Yaskawa[®] is offering a MV DD-PMSGs (Enewin-Generators) for wind turbines in the power ratings of 2–5 MW@3000 V. These generators have over-speed capability of 130 % for 2 minutes.

When the fault duration is too long, the generator may cross the threshold level of over-speed capability, and the output voltage of diode-rectifier v_{in} ($\approx 1.35 \times v_{sl}$) may exceed its threshold limit. When this scenario happens, which ever is first, the pitch mechanism and brake enter into action to trip the turbine. It should be noted that the v_{in} does not increase significantly compared to the v_{dc} . As shown in the summary of the state-of-the-art national grid codes in Table 1.3, the maximum grid voltage sag duration, without allowing wind turbine tripping is 625 ms. The previous analysis indicates that the increase in v_{in} for the maximum fault duration is 6.02 % only. Therefore, according to Table 1.3, beyond 625 ms

the turbine is allowed to be disconnected from the point of view of grid-connected WECS.

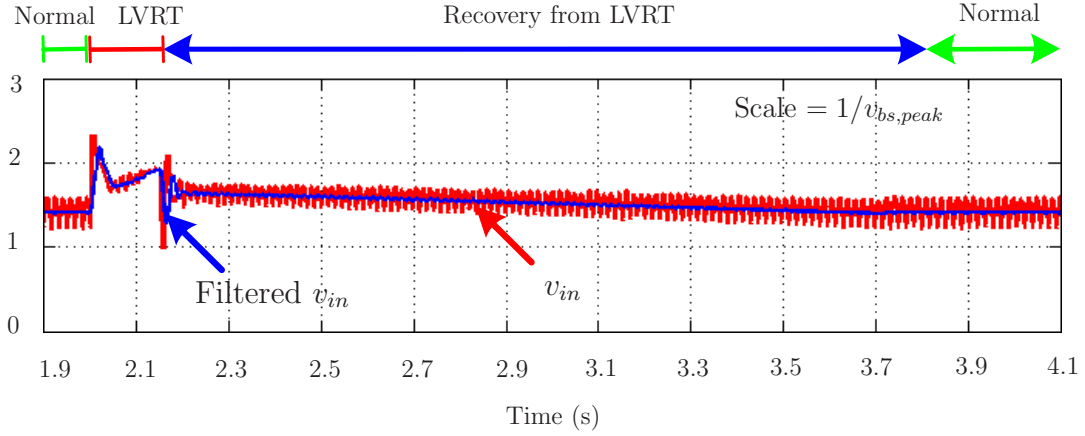
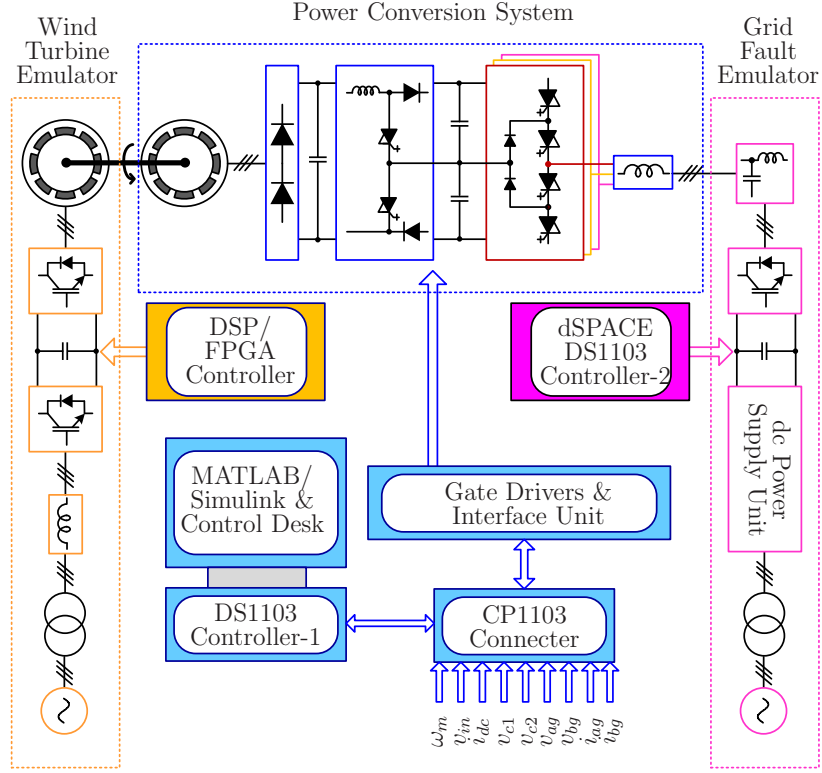


Figure 9.9: Simulation result for input dc voltage v_{in} during three-phase grid voltage dip with the generator-side LVRT controller enabled and $C_{in} = 820 \mu\text{F}$.

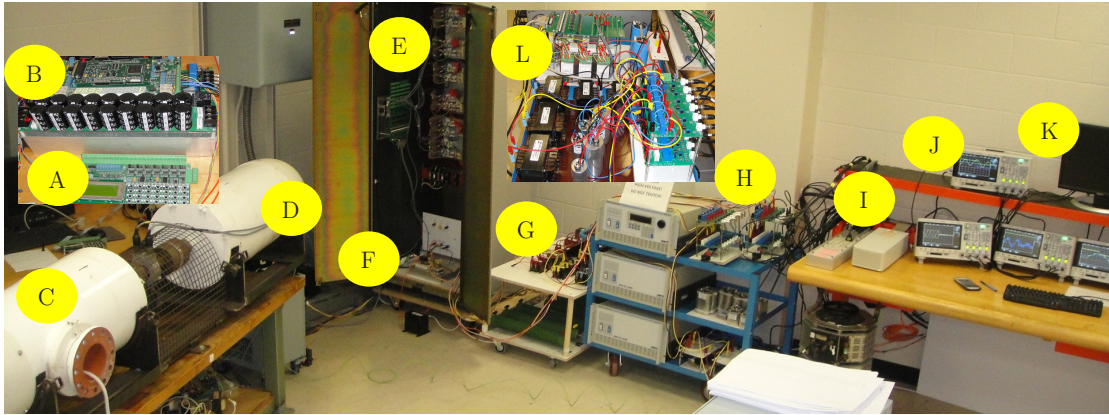
For the simulation results presented in Figs. 9.5, 9.6, 9.7 and 9.8, the value of C_{in} is chosen as 3.43 p.u.. The generator-side base capacitance C_{bs} is much larger compared to the grid-side base capacitance C_{bg} due to the lower fundamental frequency of PMSG (refer to Table 9.1). Due to this reason, the C_{in} value is much larger compared to C_{dc} . The C_{in} has less impact on the system performance, and thus its value can be decreased significantly to further reduce the cost and size of overall power converter. The simulation results shown in Figs. 9.7 and 9.8 are repeated with $C_{in} = 820 \mu\text{F}$ (0.15 p.u.) and the waveform for v_{in} is presented in Fig. 9.9. Due to lower value of C_{in} , the ripple in v_{in} increases, but by using filtered v_{in} in the control scheme (refer to Fig. 9.2) the system response during normal and LVRT operation becomes similar to Figs. 9.7 and 9.8. The voltage rating for the C_{in} is decided according to the maximum rise in the mechanical shaft speed $\omega_{m,max}$. To fulfill the state-of-the-art LVRT requirements with the maximum fault duration of 625 ms, the voltage rating of C_{in} becomes approximately 4293 V ($=1.35 \times 3000 \times 1.06$) [84]. To realize input dc-link, 10 units of 8200 μF , 450 V capacitors can be connected in series. It should be noted that the cost of input dc-link is very low (\$470) compared to the cost of one 6.6 kV, 1200 A IGCT (\$1800) [11]. The work in [113] demonstrated that the power conversion system can also work without employing C_{in} . The elimination of C_{in} , and the analysis of its impact on torque ripple, grid-side converter control and LVRT operation is considered as future work.

9.7 Experimental Results

A low power prototype model is developed as shown in Fig. 9.10.



(a) Block diagram



(A) key board, (B) DSP/FPGA controller, (C) prime mover, (D) non-salient pole PMSG, (E) NPC inverter, (F) three-level boost converter, (G) grid-side filter, (H) voltage and current transducers, (I) DS1103 R&D controller, (J) measurement system, (K) control desk, and (L) three-phase grid fault simulator.

(b) Photograph of complete setup

Figure 9.10: Experimental setup.

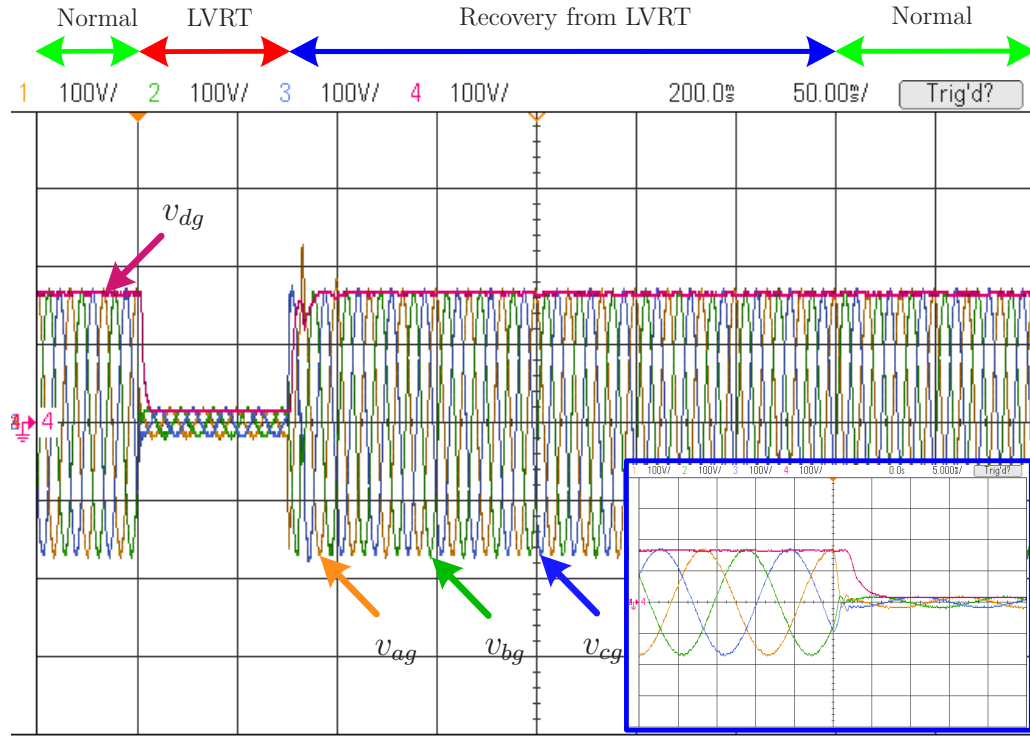
Two mechanically coupled PMSGs are used. The first PMSG, along with a DSP/FPGA controller, is used as a prime mover to provide the required mechanical torque emulating the wind for the second PMSG. These machines have been obtained from a real wind farm, and they feature over-speed capability similar to the MW-DD generators. The TLB and NPC converters are controlled by a dSPACE DS1003 rapid prototyping board. The grid fault emulator is developed based on a two-level inverter with an output LC filter, which is controlled using another DS1103 platform. More details about the experimental setup can be found in Section 7.4.

It should be noted that slower switching times of the IGBTs does not affect the predictive control strategy. In the predictive control approach, sampling time (T_s) is selected based on the minimum execution time required to perform the optimization algorithm during each sampling interval [81, 279]. Unlike in the classical modulation-based control techniques [67], the selection of T_s is not related to the switching frequency [81, 279]. In other words, for a given value of T_s , the predictive controller can operate with a wide range of switching frequencies by just including a constraint in the cost function. In the present experimental tests, the dSPACE controller can handle all the calculations and two-step predictions related to the proposed method within $100\ \mu\text{s}$.

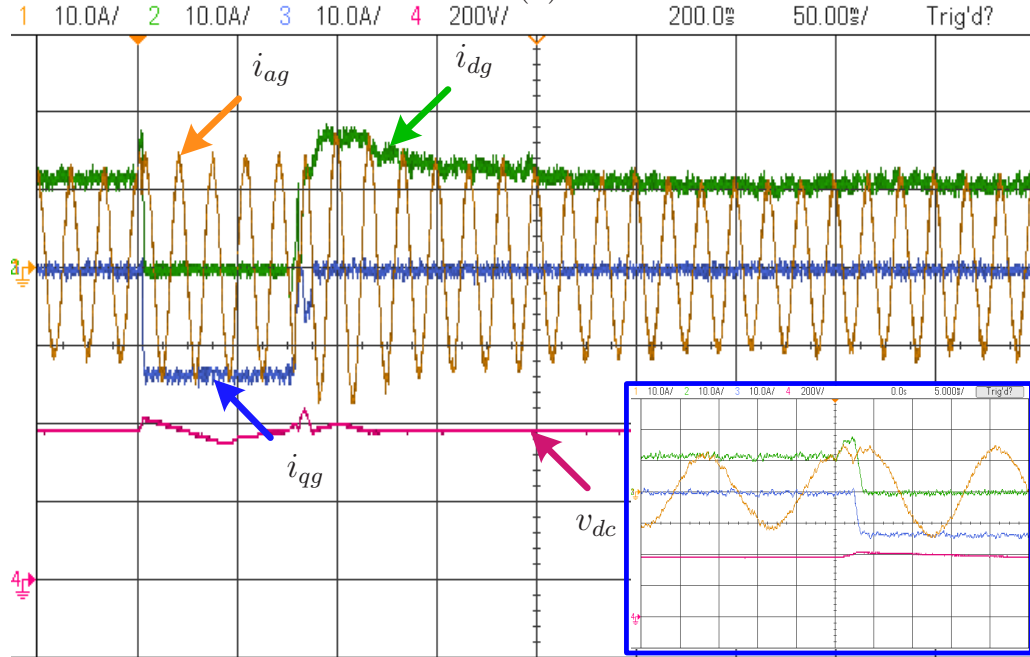
The moment of inertia of the PMSG used in the experimental set-up is very low, which means that, during grid fault condition, it reaches the over-speed threshold quickly compared to the PMSG used in simulation analysis. To avoid an unexpected increase in speed, the fault duration is reduced from 150 to 75 ms, but the depth of the voltage dip is same as of simulations. Even though the duration of grid fault is different in the simulations and experiment, the operating principle remains same. Due to hardware restrictions, the saturation limit of the dc-bus PI controller is set to 1.2 times $i_{bg,peak}$.

The experimental results with the proposed strategy are presented in Figs. 9.11 and 9.12. The PMSG operates at rated condition and the average switching frequencies for the TLB and NPC are noted as 280 and 760 Hz, respectively. The THD of the grid currents is measured as 5.2%. The transient responses during the grid voltage dip from 100% to 10% are shown in boxes. The voltages generated by the grid fault simulator contain less THD. But it has been demonstrated in Chapters 5 to 8 that the predictive control technique is robust against grid voltage harmonics and also grid-side filter parameter variations.

During the LVRT interval, the generator shaft speed and input dc voltage are increased



(a)



(b)

Figure 9.11: Experimental results during three-phase grid voltage dip with the generator-side LVRT controller enabled (Part-I).

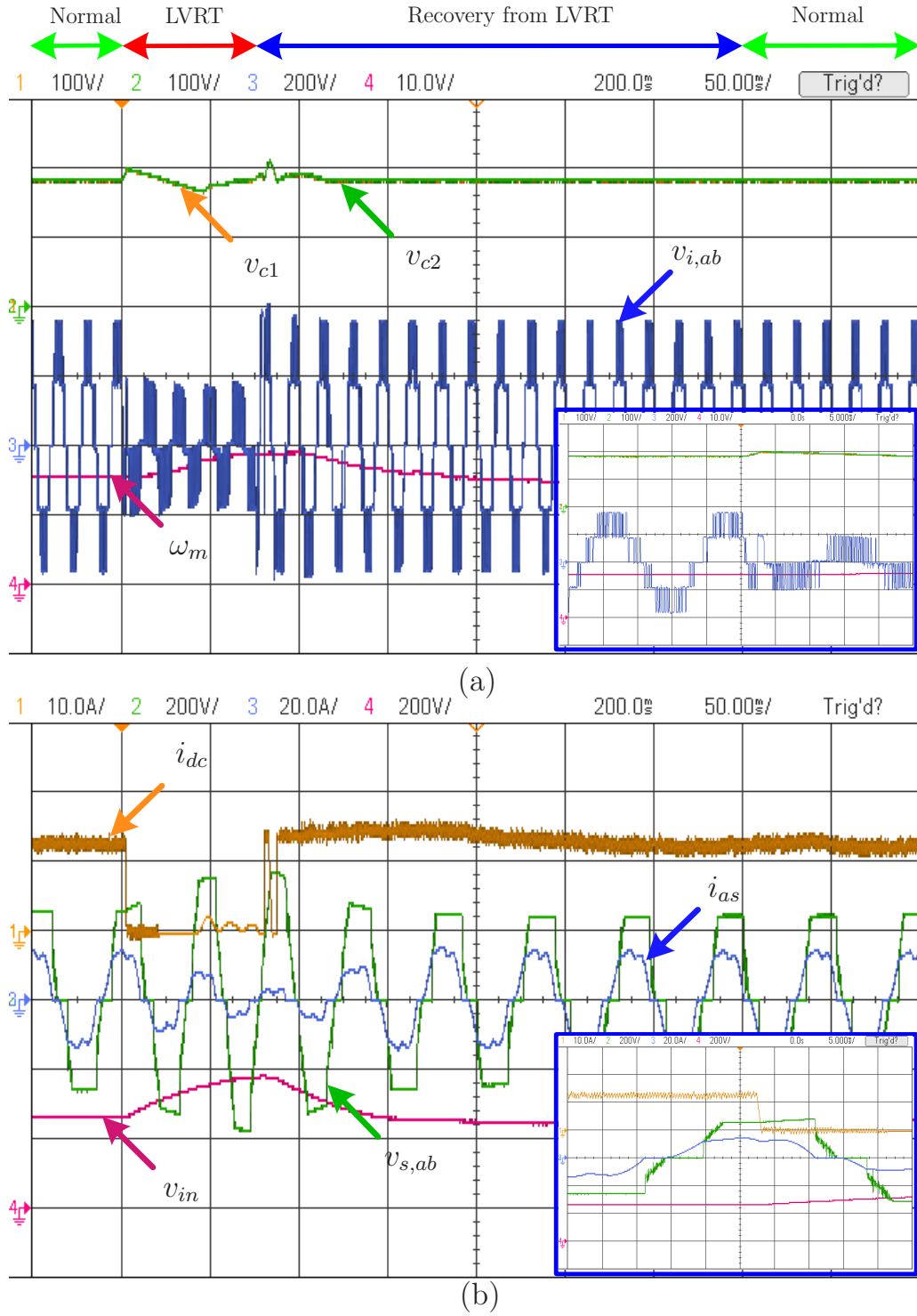


Figure 9.12: Experimental results during three-phase grid voltage dip with the generator-side LVRT controller enabled (Part-II).

similar to the simulation results. Due to the low moment of inertia, the percentage of speed increase is high compared to the simulation. This would not be the case with MW turbines. During this time frame, the inductor current and stator currents are maintained at zero value. The grid currents corresponding to the active and reactive power are maintained at their reference values during normal and LVRT operation. The net dc bus voltage is maintained within safe limits and the dc-link capacitor voltages are well balanced during all the operating conditions.

A delay time of 3 ms is noticed from the instant the grid voltages become zero and the reactive current becomes 100 %. This is mainly due to the dead-time caused by the voltage and current sensors, gate drivers and controller. The E.ON grid codes indicate that the control actions should be taken within 20 ms if the grid voltage drops below 90 %. The response time of 3 ms provides excellent compliance with the grid codes. Similar to the simulations, the grid and inductor currents track their references accurately (shown in box). This is made possible due to the elimination of the linear regulators and modulation stage in the controller design. The experimental results presented here confirm that the LVRT compliance can be enhanced efficiently using the proposed power converters and control scheme. This analysis considers symmetrical grid fault conditions, but it is also possible to include unsymmetrical grid faults as outlined in [299]. The system analysis with unsymmetrical grid faults is considered as a possibility for future work.

9.8 Conclusion

A model predictive control scheme is proposed for the LVRT enhancement of megawatt direct-driven PMSG wind turbines. The proposed approach is based on the storage of surplus energy in the turbine-generator shaft inertia during the grid faults. The reference control variables are exchanged during the LVRT operation to protect the power converters (by limiting the dc-bus voltage to safe limits), while meeting the grid code requirements. This method is most favorable for megawatt direct-driven wind turbines which possess extensive moment of inertia. The proposed solution is verified for a medium voltage PMSG-WECS based on a three-level boost and NPC converters. The experimental results indicate that during the grid faults the proposed predictive control provides smooth transition between normal and LVRT operation with a response time of 3 ms.

Chapter 10

Conclusions

The present wind energy industry indicates a trend towards the research and development of megawatt-level wind turbines. The major interests of the current wind turbine manufacturers include: variable-speed (Type-4) technology, direct-driven (DD) permanent magnet synchronous generator (PMSG), medium voltage (MV) operation and development of sophisticated control systems to increase the wind energy conversion efficiency and to meet stringent grid codes. In this work, by incorporating the aforementioned wind industry interests as basic components, two novel power converter configurations, and various model predictive control schemes, have been developed and validated aimed at next generation 3–15 MW wind turbines.

The outcome of the research work presented in this dissertation has brought several major innovations in the development of next generation converter configurations and control schemes for the megawatt wind energy systems. The proposed configurations are very promising for the future development as they have been designed by combining the best features of the existing commercial wind turbine solutions. The research results presented here also promote the predictive control strategy as a simple, efficient and high performance control tool for megawatt power converters which operate at a very low (< 1 kHz) switching frequency. Various control objectives such as grid/inductor currents, dc-link capacitor voltages, switch changes, common-mode voltage, net dc-bus voltage, grid active power and grid reactive power are included in the design and operation of the predictive controller. The modeling and analysis presented in this work can be used in other power electronics and energy system applications.

10.1 Summary of Major Contributions

The major contributions and conclusions of this research work are summarized as follows.

1) A review of the wind energy industry, full-scale power converters and digital control schemes is presented

- An extensive survey on the past, present and future trends of the wind energy market is presented to fill gaps in the existing literature,
- A review of practical and emerging full-scale power converters is presented. Various technical issues, features and drawbacks are analyzed, and important survey results are summarized by tables, and
- Various classical and advanced control techniques are discussed and compared based on an intuitive example of load current control.

2) Novel three-level converters are proposed for 3–4 kV WECS

In this dissertation, a novel power converter topology using a diode rectifier, three-level boost converter and neutral-point-clamped (NPC) inverter is proposed for the next-generation DD-PMSG based 3–4 kV class WECS. Compared to the commercially available back-to-back (BTB) connected NPC converter, the proposed configuration uses less number of active switches and thus it is less expensive and reliable. The dc-link capacitor voltages are balanced during all operating conditions by the boost converter. Because of the control freedom for the NPC inverter, the grid current harmonic distortion is noted to be lower compared to the BTB-NPC converters.

3) Four-level converters are proposed for 4–10 kV WECS

A new power conversion system based on four-level converters is explored aimed at the next generation 4–10 kV class WECS. The grid current quality has been increased significantly compared to the three-level converters. To solve the problem of the dc-link capacitor voltages balancing, which is more complicated compared to the three-level converters, a four-level boost converter is proposed as an intermediate stage. Despite the large number of active switches and clamping diodes used in the four-level inverter, the cost of this configuration is approximately the same as that of the BTB-NPC converter.

4) Continuous- and discrete-time models are presented

In this work, the continuous-time model of the variables to be controlled is presented in terms of power converter switching states. Several variables, such as load/grid/inductor currents, dc-link capacitor voltages, switching frequency, common-mode voltage, net dc-bus voltage, active power and reactive power, are incorporated in the design of the system model. All the continuous-time models have been converted to discrete-time so as to incorporate the control delay and prediction horizon.

5) A generalized method is proposed to control the multilevel diode-clamped converters (MLDCCs)

In this dissertation, similar to those in the classical control methods, a generalized approach based on FCS-MPC strategy is presented for the load/motor/grid current control, dc-link capacitor voltages balancing, switching frequency reduction and common-mode voltage mitigation in MLDCCs. The proposed method shows a promising solution to controlling the converters with diverse control objectives and constraints.

6) Two advanced techniques are proposed to control the grid-tied converters

The grid-tied multilevel converters are crucial to the dispatch of generated power and also in meeting the grid codes. In this dissertation, two advanced control schemes based on FCS-MPC are proposed:

- In the first control strategy, the net dc-bus voltage and grid reactive power are controlled, assuming that the generator-side converter performs MPPT;
- In the second strategy, the grid active and reactive powers are controlled with an assumption that the generator-side converter regulates the net-dc bus voltage;
- In both methods, the voltage stress and switching losses of the semiconductor switches are reduced by balancing the dc-link capacitor voltages and by minimizing the switching frequency below 1 kHz, respectively;
- An excellent dynamic response has been achieved by eliminating the internal current control loops and modulators; and
- Compared with the classical decoupled voltage-oriented control, a better reference tracking and power quality has been achieved.

7) Complete control systems have been built for the 3L and 4L converters based WECS

A step-by-step procedure for the design of a complete control system for the proposed 3L and 4L converters based MW-MV-DD-PMSG-WECS is presented. The objectives such as MPPT, dc-link capacitor voltages balancing, regulation of net dc-bus voltage, reactive power generation, lower switching frequency operation, and common-mode voltage minimization are considered in the design of generator- and grid-side cost functions. The proposed solutions can be easily extended to other WECS configurations and motor drive applications.

8) FCS-MPC strategy is proposed for the low voltage ride-through (LVRT) enhancement of PMSG wind turbines

A predictive control scheme is proposed for the LVRT enhancement of DD-PMSG wind turbines. The proposed approach is based on the storage of surplus energy in the turbine-generator shaft inertia during the grid faults, and thus no additional dc-link crowbar (resistor) is required. The exchange of reference control variables between normal and LVRT operation is suggested to protect the power converters (by limiting the dc-bus voltage to safe limits), while meeting the grid code requirements. The proposed method is most favorable for the high power wind turbines which possess large moment of inertia. The E.ON grid code indicates that the control actions should be taken within 20 ms if the grid voltage drops below 90 %. In this work, a response time of 3 ms is achieved to switch from the normal to LVRT operation mode.

9) Various challenges related to the FCS-MPC strategy are addressed

- In order to solve the variable switching frequency nature of the predictive control strategy, a look-up table based on weighting factor selection is proposed and verified. This approach guarantees the regulation of switching frequency within the set boundary limits (for example 750-850 Hz);
- A detailed empirical procedure for the selection of weighting factors is presented to fill the gap in literature;
- A novel extrapolation method is proposed to estimate the future values of the synchronous reference frame variables. The proposed method eliminates the os-

cillations in the reference active and reactive powers (which are control variables for the case study considered), and the spike in the inverter line-line voltage. This method leads to safe and reliable operation for the semiconductor devices during step-changes in the reference control variables;

- A simplified two-step predictive control strategy is proposed to improve the performance and also to reduce the computational burden involved in the real-time implementation. The proposed solution offers accurate tracking to the reference control variable, lower dv/dt in the output voltage waveform and lower switching frequency compared to the standard one-step and two-step prediction methods;
- A novel delay compensation technique is introduced for the FCS-MPC. Compared to the state-of-the-art works which compensate the control delay at the expense of higher switching frequency, the proposed technique shows a better solution without increasing the converter switching frequency. The proposed solution is promising for high power applications where lower switching frequency operation is mandatory; and
- Performance of the proposed predictive control techniques are investigated with the perturbations in the grid-side filter and dc-link parameters. The results indicate that the proposed controllers are robust and can compensate for the system perturbations, while the control variables continue to effectively track to their references.

10) Simulation and experimental studies are conducted to verify the system operations

All the simulation studies are carried out using MATLAB/Simulink software. The predictive control algorithms are developed using MATLAB S-Builder function for an easy transfer of code to real-time implementation.

Several low power prototype converters have been built such as BTB 2L-, 3L- and 4L-VSCs; and 2L-, 3L- and 4L-boost converters. All the theory, control system design and simulation results are validated through the experimental tests. A dSPACE DS1103 rapid prototyping controller based test platform has been developed. A grid-fault simulator based on 2L-4Leg-VSC is developed which can generate different symmetrical and unsymmetrical output voltage waveforms.

10.2 Future Works

The following future research works are suggested as an extension to the knowledge presented in this dissertation.

1) Comparison of proposed controllers with the classical control techniques

To contribute to the ongoing research on predictive control, and to clearly distinguish this method from classical control techniques, comparison studies can be carried out.

2) Active damping of the *LCL* filters employed in the grid-connection

The variable switching frequency operation with the FCS-MPC method causes grid current harmonics to spread over the whole spectrum. These harmonics cause more challenges for the operation of grid-connected converter even during normal operation. The proper design of predictive controller with *LCL* filters should be studied.

3) Investigation of other multilevel converters for wind energy

Since the dc-link capacitor voltages are controlled by the intermediate dc-dc converter, other multilevel converter configurations can be used to reduce or completely eliminate the grid-side filter.

4) Operation of the proposed WECS under unbalanced grid voltage dips

Investigation of PMSG-WECS behavior under unbalanced grid fault conditions and development of new control systems represent a very good research direction to meet the emerging grid code requirements.

5) Study of stability issues with the predictive control

The stability issues with the FCS-MPC strategy should be studied by employing different discretization methods and prediction horizons.

6) Application of proposed control philosophies to other power electronic converters

The generalized modeling and control approach presented in this dissertation can be extended to flying capacitor, active NPC and novel power electronic converters.

Appendix A

List of Commercial Wind Turbines

The megawatt-level projects based on SCIG/PMSG/WRSG/HTS-SG which are in the development stage are summarized in Table. A.1.

Table A.1: Future development of full-scale converters based MW wind turbines

Manufacturer	Model	Gear and Generator	Rating	Rotor (m)	Release By
China Energine	CE2 MW	Direct Drive PMSG	2.0 MW	93	2014
United Power	UP100 – 3000	Direct Drive PMSG	3.0 MW, 690 V	101	–
Marvento	M3.6 – 118	Direct Drive PMSG	3.6 MW, 3900 V	118	2014
Envision Energy	E128 – 3.6 MW	Dual Drive PMSG	1.9 MW \times 2, 730 V	128	2014
Siemens	SWT4.0 – 130	Geared SCIG	4.0 MW	130	2015
XEMC-Darwind	XE/DD115	PMSG	5.0 MW, 3000 V	115	2014
CSIC	CSIC5 MW	PMSG	5.0 MW	154	–
Goldwind	GW5 MW	Direct Drive PMSG	5.0 MW	–	2014
Hyosung	Hyosung5 MW	PMSG	5.0 MW	136	–
Gamesa	G128 – 5.0 MW	Medium Speed PMSG	5.0 MW	128	2014
AMSC-Hyundai	HQ5500/140	PMSG	5.5 MW	140	2014
Goldwind	GW6 MW	Direct Drive PMSG	6.0 MW	–	2014
Siemens	SWT6.0 – 154	Direct Drive PMSG	6.0 MW, 690 V	154	2014
Alstom Power	Haliade150 – 6 MW	Direct Drive PMSG	6.0 MW, 900 V	150	2014
Nordex	N150/6000	Direct Drive PMSG	6.0 MW, 3300 V	150	2015
MingYang	SCD6.5	PMSG	6.5 MW	140	2014
Condor Ltd.	Condor6	Geared MV SCIG	6.6 MW, 3300 V	125	2015
Bard GmbH	BARD6.5	Dual Drive MV PMSG	3.4 MW \times 2	122	2014
Daewoo Ltd.	DSME7.0	PMSG	7.0 MW	160	2014
Mitsubishi	SeaAngel 7.0 MW	Dual Drive Brushless SG	3.5 MW \times 2	165	2015
Siemens	SWT7.0 – 171	PMSG	7.0 MW, 3300V	171	2014
Vestas	V164 – 8.0 MW	Medium Speed PMSG	8.0 MW	164	2016
Clipper	Britannia	Quantum Drive PMSG	2.6 MW \times 4, 3600 V	150	2015
Sway Turbine AS	ST10	Axial Flux PMSG	10 MW, 3500 V	164	2015
AMSC	SeaTitan	Direct Drive HTS	10 MW, 690 V	190	2015
GE Energy	GE15 MW	Direct Drive HTS	15 MW	180	2016

The summary of few commercial wind turbines which use SCIG/PMSG/WRSG and full-scale power converters is given in Table A.2.

Table A.2: List of commercial wind turbines using full-scale converters

Manufacturer Country	Model	Generator (Supplier)	Power (MW) Voltage (V)	Gear Steps Gear Ratio	Height (m) Dia (m)	Rotor Speed (rpm)	Converter (Supplier)	Figure	Other Models
AREVA Wind Germany	M5000	PMSG (ABB)	5.0 3300	1 1 : 10	90 116	4.5 – 14.8	ABB PCS 6000	Fig. 2.5	M5000-135
Enercon GmbH Germany	E126/7580	WRSG	7.5 690	DD 1 : 1	135 127	5 – 11.7	2L-VSC	Fig. 2.4	E126/7500, 7000,6000
	E101/3000	WRSG	3.0 690	DD 1 : 1	99/135/ 149; 101	4 – 14.5	2L-VSC	Fig. 2.4	E82/3000
	E82/2000	WRSG	2.0 400	DD 1 : 1	75/85/98/ 108/138; 82	6 – 18	2L-VSC	Fig. 2.4	E66/2000 E70/2000
WinWinD Ltd. Finland	WWD-1-D60	PMSG (ABB)	1.0 690	1 —	56/66/70 60	8 – 26	2L-VSC	Fig. 2.4	D56
	WWD-3-D90	PMSG (ABB)	3.0 690	2 1 : 26.66	80/88/90/ 100; 90	5 – 18	2L-VSC	Fig. 2.4	D100, D103 D109, D120
Vensys AG Germany	Vensys70	PMSG	1.5 690	DD 1 : 1	65/85 70	9 – 19	Boost+ 2L-VSC	Fig. 2.11	77/82/87
	Vensys100	PMSG	2.5 690	DD 1 : 1	100 100	6.5 – 14.5	2L-VSC	Fig. 2.4	109/112
	Vensys120	PMSG	3.0 690	DD 1 : 1	90/140 120	6.5 – 12.8	2L-VSC	Fig. 2.4	112– 3000
Gamesa Spain	G128	PMSG	4.5 690	2 1 : 37.88	81/120/140 128	448	2L-VSC	Fig. 2.4	G136
	G128 – 5.0	PMSG	5.0 690	2 1 : 41.405	80/94 128	490	2L-VSC	Fig. 2.4	G11X/5000
Avantis China	AV928	PMSG	2.5 690	DD 1 : 1	80/100 93.2	16	ABB ACS 800	Fig. 2.4	

Appendix B

System Modeling

In this Appendix, a brief description about various system models and notation employed in this dissertation is presented.

B.1 Notation of Per-Unit Values

The following notation is employed in representing per-unit (p.u.) values. The rated values of wind turbine or power converter are selected as base values.

- Base apparent power S_B represents the rated power of generator or power converter
- Base active power P_B represents the rated generator mechanical input power or rated converter output power
- Base voltage V_B represents the phase voltage of generator or grid
- Base frequency $\omega_B = 2\pi f$ represents the rated frequency of generator or grid.
- Base current $I_B = \frac{S_B}{3 \times V_B}$
- Base impedance $Z_B = \frac{V_B}{I_B}$
- Base inductance $L_B = \frac{Z_B}{\omega_B}$
- Base capacitance $C_B = \frac{1}{\omega_B \times Z_B}$
- Base flux-linkage $\Lambda_B = \frac{V_B}{\omega_B}$
- Base torque $T_B = \frac{P_B}{\omega_B}$

B.2 Reference Frame Transformation

The reference frame theory helps to simplify the modeling, analysis, simulation and digital implementation of control schemes employed in the WECS. In this dissertation, the following three reference frames were used:

- Natural reference frame (abc)
- Stationary reference frame ($\alpha\beta$)
- Synchronous reference frame (dq)

The transformation of variables between these reference frames is presented below. The variable x represents either voltage, current or flux linkage.

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (\text{B.1})$$

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \quad (\text{B.2})$$

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta - \frac{4\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{4\pi}{3}) \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (\text{B.3})$$

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta - \frac{4\pi}{3}) & -\sin(\theta - \frac{4\pi}{3}) \end{bmatrix} \cdot \begin{bmatrix} x_d \\ x_q \end{bmatrix} \quad (\text{B.4})$$

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} x_d \\ x_q \end{bmatrix} \quad (\text{B.5})$$

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \quad (\text{B.6})$$

B.3 Wind Turbine Model

The model of the wind turbine is important for the study of the WECS response during dynamic changes in wind speed and also during grid faults. The model of the wind turbine also helps to effectively design MPPT algorithms. In this subsection, the model of the wind turbine is given with additional details about MATLAB/Simulink implementation.

The mechanical output power of a wind turbine can be given as:

$$P_M = \frac{1}{2} \rho A v_w^3 C_p \quad (\text{B.7})$$

where ρ is air density (typical value is 1.225 kg/m³), A is rotor swept area, and v_w is wind speed velocity. C_p represents the power coefficient of a blade and it has a theoretical maximum value of 0.59 according to Betz limit. The C_p value varies between 0.2 and 0.5 for most of the MW-level commercial wind turbines.

The C_p can be defined in terms of turbine coefficients C_1 to C_7 as:

$$C_p = C_1 \left(\frac{C_2}{\lambda_i} - C_3\beta - C_4\beta^2 - C_5 \right) e^{-\frac{C_6}{\lambda_i}} + C_7\lambda_T \quad (\text{B.8})$$

where β is the pitch angle which is adjusted by the pitch control system according to the wind speed. The β value is zero when wind speed is below its rated value. λ_T corresponds to optimal tip-speed-ratio (TSR) as defined below:

$$\lambda_T = \lambda_{T,op} = \frac{n_{M,R} \times \frac{2\pi}{60} \times r_T}{v_{w,R}} \quad (\text{B.9})$$

where r_T is radius of turbine, $n_{M,R}$ is rated speed of turbine, and $v_{w,R}$ is rated wind speed. The wind turbine operates at its optimal TSR ($\lambda_{T,op}$) during all the wind speed conditions.

In (B.8), λ_i is intermittent TSR and it is related to λ_T and β as demonstrated below:

$$\frac{1}{\lambda_i} = \frac{1}{\lambda_T + 0.08\beta} - \frac{0.035}{\beta^3 - 1}. \quad (\text{B.10})$$

The turbine output torque can be estimated as:

$$T_M = \frac{P_M}{\omega_M} \quad (\text{B.11})$$

where ω_M is turbine shaft speed which can be estimated as follows:

$$\omega_M = \frac{\omega_m}{r_{gb}} \quad (\text{B.12})$$

where ω_m is measured generator speed and r_{gb} is gearbox ratio.

The MATLAB/Simulink model of a wind turbine is shown in Fig. B.1, where the inputs are wind speed velocity v_w , pitch angle β and generator speed ω_m , while the output is mechanical torque. The model given here can be used for SCIG, PMSG or WRSG.

Fig. B.2 depicts the MATLAB/Simulink model of the pitch control system. This system maintains generator active power output at its rated value by producing suitable β value. Based on the measured generator output voltages and currents, the active power output is computed and its value is compared to the reference active power which is always 1.0 p.u.. The error is processed by a PI controller whose output value is β which is applied gradually (through a rate limiter) to the turbine. It is important to recall that the β value becomes more than 0 only when the generator output power exceeds its rated value.

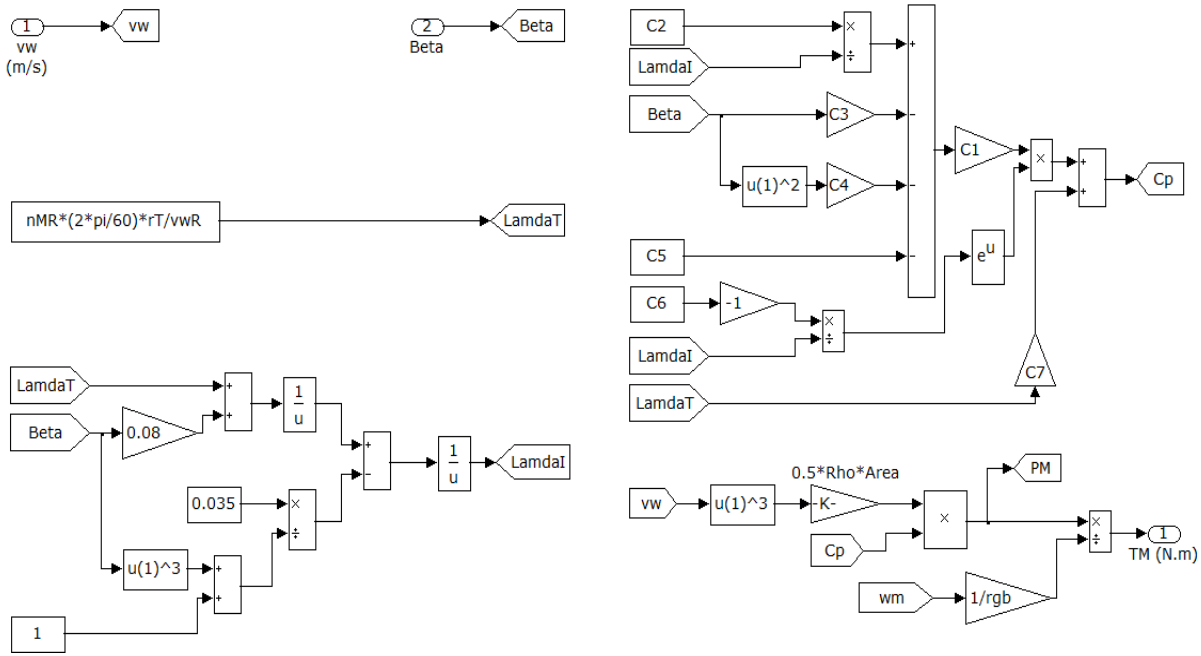


Figure B.1: MATLAB/Simulink model of wind turbine.

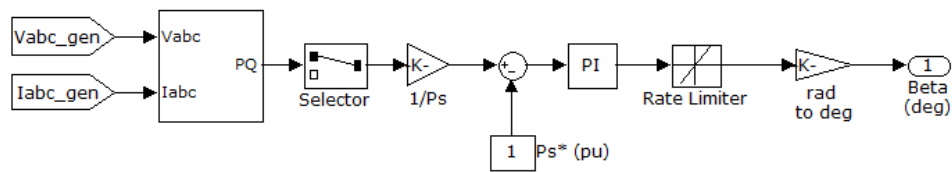


Figure B.2: MATLAB/Simulink model of pitch control system.

B.4 Phase-Locked Loop (PLL) Model

The grid synchronization is one of the most important issues in WECS in order to allow the grid and grid-tied inverter to work in unison. PLL is a widely accepted method to generate the reference variable (grid voltage angle θ_g) for the grid synchronization. In this dissertation, three-phase symmetrical grid voltages are considered ($v_{ag} + v_{bg} + v_{cg} = 0$). The grid voltage angle θ_g is also crucial in the transformation of variables between abc and dq frames, and in the operation of grid-side control system.

For an ideal grid (used in the MATLAB simulations), the following method can be used to estimate θ_g :

$$\theta_g = \tan^{-1} \frac{v_\beta}{v_\alpha} \quad (\text{B.13})$$

where v_α and v_β are stationary frame grid voltages, and they can be estimated from the three-phase grid voltages using (B.1).

A simplified model for the system is shown in Fig. B.3. In real-time, the grid voltages contain harmonics and they are distorted. In such cases, SRF-PLL can be used as shown in Fig. B.4. This method uses a PI controller to force the q -axis grid voltage v_{qg} to zero value. A feed-forward frequency term ω_g ($= 2\pi f_g$) is added to the output of the PI controller to improve initial dynamic performance. An integrator is then employed to convert ω_g to θ_g . To ensure that the θ_g changes between 0 and 2π , a modulus function is used.

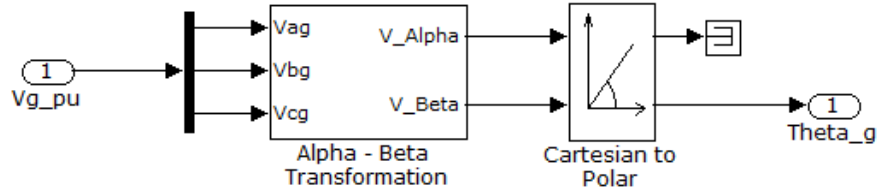


Figure B.3: Simplified model for grid voltage angle estimation.

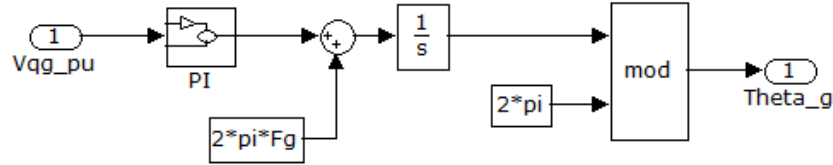


Figure B.4: Standard SRF-PLL model for grid voltage angle estimation.

Appendix C

Performance Assessment

In order to assess the performance of FCS-MPC scheme, various parameters are defined in this appendix.

The percentage mean absolute current reference tracking error $\%e_{ig}$ is defined as the absolute difference between the reference and load/grid currents with respect to the *rms* value of load/grid current:

$$\%e_{ig} = \frac{\frac{1}{m} \sum_{k=0}^m |i_g^*(k) - i_g(k)|}{\text{rms}(i_g(k))} \times 100 \quad (\text{C.1})$$

where m represents number of samples. In the simulation and experimental tests, 25000 samples are considered, which corresponds to 15 fundamental cycles.

Similarly, the active and reactive power tracking errors are defined with respect to the base apparent power S_g as:

$$\%e_{pg} = \frac{\frac{1}{m} \sum_{k=0}^m |P_g^*(k) - P_g(k)|}{S_g} \times 100 \quad (\text{C.2})$$

$$\%e_{qg} = \frac{\frac{1}{m} \sum_{k=0}^m |Q_g^*(k) - Q_g(k)|}{S_g} \times 100. \quad (\text{C.3})$$

The percentage mean absolute dc-link capacitor voltages deviation $\%e_{vc}$ is formulated for 3L converter as:

$$\%e_{vc} = \frac{\frac{1}{m} \sum_{k=0}^m |v_{c1}(k) - v_{c2}(k)|}{v_{dc}^*} \times 100. \quad (\text{C.4})$$

For a 4L-converter, the $\%e_{vc}$ is determined as follows:

$$\%e_{vc} = \frac{\frac{1}{m} \sum_{k=0}^m \sum_{i=1,2,3, j=2,3,1} |v_{ci}(k) - v_{cj}(k)|}{3 \times v_{dc}^*} \times 100. \quad (\text{C.5})$$

A similar approach can be used to calculate capacitor voltages deviations in other multilevel converters.

The percentage of total harmonic distortion (THD) is described as follows:

$$\% \text{ THD} = \sum_{x=a,b,c} \frac{1}{3} \cdot \frac{\sqrt{i_{2,x}^2 + i_{3,x}^2 + \dots + i_{n,x}^2}}{i_{1,x}} \times 100 \quad (\text{C.6})$$

where $i_{n,x}$ and $i_{1,x}$ are n^{th} order harmonic and fundamental components of phase- x load/grid currents, respectively.

The average device switching frequency of a 3L-converter is calculated below:

$$f_{sw} = \sum_{x=a,b,c} \frac{f_{sw,1x} + f_{sw,2x}}{6}. \quad (\text{C.7})$$

The switching frequency of each upper switch is calculated by measuring the number of switching changes in the gating signals for 15 fundamental cycles. Similarly, for a 4L-converter, the average switching frequency is calculated as:

$$f_{sw} = \sum_{x=a,b,c} \frac{f_{sw,1x} + f_{sw,2x} + f_{sw,3x}}{9}. \quad (\text{C.8})$$

The switching frequencies of other multilevel converters can be calculated in a similar manner.

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