SWITCH-LEVEL DYNAMIC FAULT MODELING FOR RESISTIVE SHORT AND OPEN FAULTS IN NANOMETRE TECHNOLOGIES

by

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ABSTRACT

Thesis Title:

Switch-level Dynamic Fault Modeling for

Resistive Short and Open Faults in Nanometre Technologies

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Modeling the dynamic behaviour of resistive shorts and opens at switch-level dictates the characterization of enhanced delay attributable to these faults with reference to the input combinations, fault sites, defect resistance and CMOS technology variation. Resistive physical failures make the output voltage fluctuate between intermediate ranges by disturbing the propagation time of the logic, without adversely changing the functional output. To determine the impact of logic propagation delay (t_P) on the output voltage (V_{OUT}) of a gate, a switch-level fault analysis on CMOS primitive gates is executed for CMOS technologies 350 nm, 180 nm, and 90 nm in comparison with nanometre technologies 45 nm and 32 nm. To understand the nature and effect of actual resistive faults in silicon, static faults in static primitive gates are reviewed after altering the defect resistance. Delay and output voltage changes induced by these variations are determined for CMOS 32 nm technology.

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I am indebted to my parents for their constant love and support for me. Their patience and sacrifices in life have made me the person, I am today.

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Nomenclature

I_i	i^{th} input of a gate		
I_{iN}	Input of i^{th} NMOS transistor		
I_{iP}	Input of i^{th} PMOS transistor		
D_i	Drain of i^{th} CMOS transistor		
S_i	Source of i^{th} CMOS transistor		
V_{DD}	Operating voltage		
W/L	Aspect ratio		
$K`$	Transconductance parameter of a MOSFET		
V_{TH}	Threshold voltage		
t_P	Total propagation delay		
t_{PHL}	High-to-low propagation time		
t_{PLH}	Low-to-high propagation time		
R_{ON}	Transistor on-resistance		
R_N	NMOS Transistor on-resistance		
R_P	PMOS Transistor on-resistance		
R'_N	Equivalent switching resistance in the NMOS network		
R'_P	Equivalent switching resistance in the PMOS network		
R'	Equivalent circuit resistance including resistive elements from NMOS and PMOS sides respectively		
n	Identical number of transistors for all low input case		
	For mixed input case,	n_N	Number of active or ON NMOS
		n_P	Number of active or ON PMOS
C_{MOSFET}	Parasitic capacitive load of a MOSFET		
C_{OXIDE}	Oxide related capacitance of a MOSFET		
$C_{JUNCTION}$	Junction related capacitance of a MOSFET		
C_{Ni}	C_{MOSFET} for NMOS transistor network of a gate		
C_{Pi}	C_{MOSFET} for PMOS transistor network of a gate		
C_{LOAD}	Load capacitance of a gate resulting from the combination of C_{Ni} and C_{Pi}		

CHAPTER 1

INTRODUCTION

1.1 Overview

A key goal in manufacturing test is to maximize the quality of parts delivered to customers while reducing the cost of testing those parts. But arrival of deep-submicron (DSM) designs with latest nanometre technologies demonstrated that defect sizes are not proportionately scaled to the feature sizes. Overlooking testability issues arising out of these designs would result in degraded performance, because the faults are located predominantly in routing. Detailed models which can more explicitly model the behaviour of faulty DSM chips are required. Failure analysis conducted by major silicon manufacturers reveals that a majority of the failures are timing related, and delay is the prevalent culprit. As a result, manufacturers are demanding dynamic defect models that are more sophisticated than the traditional static stuck-at fault model. Transition and path-delay models satisfy this demand, aiding the identification of various manufacturing defects, including in-line resistances as well as opens on single and pairs of transistors. Modern VLSI (Very Large Scale Integration) chips clocking at higher frequencies

tend to have performance violations due to timing related fault mechanisms. A timing error prevents a circuit from functioning at its desired clock rate, functionally slower or faster than designed output delay. The delay of paths in a circuit becomes larger than expected resulting in the output of a chip to be deviant from the expected behaviour, in spite of the chip being functionally correct. The fault models associated with these timing-related defects are called delay fault models.

Complex circuitries make it nearly impossible to guarantee the perfect functioning of each and every manufactured part and more over they account for physical failures or spot defects occurring in silicon [10]. High quality test generation requires an improved knowledge of defect behaviour. Growing contact parasitic in deep sub-micron assemblies has been one of the main reasons for the rise of dynamic logical faults. Recent studies [5] on dynamic faults confirm that static and dynamic behaviour of the defective interconnects can be electrically classified, taking into account the fault location as well as the defect resistance value. Many defective IC's with excessive propagation delay are missed by a 100 % SSF (Single Stuck-at Fault) coverage test set. In reality, fault modeling needs to move from the discrete to the continuous area [20], [21], and [22]. The low-K dielectric copper metal layers in DSM assemblies are now made using the dual Damascene process. Resistive physical defects, including those caused by contamination or voids in via, are among the more common defects observed in DSM technologies [4].

Dynamic effects of physical failures like shorts and opens are yet to be fully understood. As their name suggests, 'RESISTIVE' faults are characterized by the resistance of their connection. A short between any two circuit nodes should have zero-resistance value and a break in a line

has infinite resistance. Both these categories of faults, behave otherwise when the faulty connection has substantial amount of resistance on it. Not all defects permanently alter circuit behaviour the way the stuck-at fault model requires. Instead, some change the timing of the circuit, causing incorrect operation only at certain frequencies. This time disturbance causes the voltage associated with the logic to change as well. After certain stages, as the logic propagates in a bigger circuit through various other circuit elements, the flaws in the gate output voltage are fixed. This prevents the faulty voltage information from being retained at the circuit output along with the faulty delay details. Estimating the voltage change at the gate output in which the resistive faults has been introduced, and propagating the delay logic through a robust path sensitization will solve the above mentioned problem to a certain extent.

1.2 Prior Work

It is assumed that a substantial fraction of short defects have non-zero resistance [32]. The vast majority of the bridging fault models [38], [34], [31], [29], [28], and [15] which describe shorts between logical nodes assume a short resistance of zero Ohm. Also the stuck-at fault model, which can be seen as one describing short defects between a logical node and V_{DD} (stuck-at-1) or ground (stuck-at-0), does not consider resistive connections. Many studies have been published regarding the delay defect synthesis with respect to reducing transistor sizes. Most deal with gate–level fault modeling [37] and others with fault diagnosis [7]. Generally, the voltage degradation caused by resistive physical defects, is accounted for as intermediate

node voltage or voltage at the node where a faulty connection is present [14], [26]. However, few studies have dealt with the propagation of the voltage change that occurs at the gate output to the circuit output along with the induced delay. A comparative study involving different submicron and deep submicron technologies (350 nm, 180nm, 90nm, 45nm and 32nm) is executed. The delay calculations are provided in detail for the nanometre technology of 32 nm. The delay behaviours in terms of time and voltage as opposed to reducing transistor dimensions are investigated, considering a well-defined range of defect resistance and for fault sites, both derived and discussed in [1]. The output voltage is estimated corresponding to the delay calculated for a particular combination of parameters discussed above.

1.3 Summary of Contributions

The objective of the thesis report is to model the dynamic behaviour of resistive physical failures in silicon and the effect of this behaviour on the timing of the logic propagation at the outputs of an integrated circuit. The overall research contributions are summarised as follows:

- A complete dynamic fault list for primary gates (NOR, NAND, AND, OR and INVERTER)
- Switch – level representation of primitive gates, by replacing transistors with a voltage controlled resistance switch and replacing static physical faulty connections (shorts and opens) with a resistor at each fault site.

- Estimate propagation delay at the output of a primitive gate for single physical failures, based on the equivalent resistance of the whole circuit.
- Extract a general formula for calculating the propagation delay caused at the gate output depending on factors like the input combinations applied to the gate, type of fault, fault location and the defective resistance value.
- Derive a mathematical relation between the propagation delay at the gate output and the gate output voltage based on negative or positive delay effect on the gate.
- Present a delay pattern based on the propagation delay and output voltage variation recorded for transistor sizes featuring from submicron to deep submicron CMOS technologies
- Degraded timing effect of resistive fault on the gate output and eventually on the primary circuit outputs is analyzed for the latest available CMOS technology spice models for feature size of 32 nm.

1.4 Organization of Thesis

Remaining chapters are organized as follows: Chapter 2 provides an inside view of CMOS physical failures and their fault modeling platform. Chapter 3 describes the switch-level fault model for a MOSFET used in latter part of the thesis to derive the delay calculation and output voltage calculation formulas. Chapter 4 discusses the transistor-level to gate-level mapping of resistive faults for all the primitive gates. Chapter 5 presents the propagation delay and output

voltage derivation. Numerical calculations for delay and voltage in a faulty and fault-free NOR gate, are presented in Chapter 6. Graphical representation of the delay pattern and effect of propagation delay caused by resistive faults on the output voltage of a gate are provided in Chapter 7. Concluding remarks and future prospects of this research study are discussed in Chapter 8, followed by a list of cited references and publications.

CHAPTER 2

MODELING PHYSICAL DEFECTS

In order to calculate a quality measurement, a measurement criteria or model has to exist. Fault is a model of the failure mode of the defect that relates the defect to the circuit behaviour. A fault model can be defined as the translation of physical defects to a mathematical construct, which can be operated upon algorithmically and understood by software simulation for providing quality measurement. It bridges the gap between physical authenticity and mathematical perception [18]. Before discussing the modeling process, the nature and type of physical defects are considered.

2.1 Nature and Effect of Physical Defects

Defective behaviour in microchips is caused by errors in processes like design, fabrication and manufacturing, or physical malfunctions. Design errors can be identified and corrected in

the design simulation process. Fabrication and manufacturing errors can be taken care of during the manufacturing process. Physical defects occur during lifetime of a system due to component attrition and probable environmental effects [36]. A physical fault present in a system may or may not cause a system failure. Modeling physical failures can be distinguished between logical faults, parametric faults and delay faults that affect the operating speed of the system [40].

- **Logical fault:** A fault type that causes the logic functions of a circuit element to be changed to some other function
- **Parametric fault:** A fault type that alters the magnitude of a circuit parameter, causing a change in some factor such as resistance, capacitance, current, or voltage
- **Delay fault:** A fault type that is related to circuit delays which usually affects the timing of the circuit, causing hazards, critical races, or performance degradation

The duration of physical defects on a circuit or system may vary depending of the modeling or nature of the fault. Based on their impact on the circuit, physical faults are classified as permanent fault, temporary faults and intermittent faults.

- **Permanent fault:** A lasting fault that is continuous and stable, whose nature does not change before, during, and after testing (e.g. a broken wire, an incorrect bonding, a design fault, etc.) and the presence of this fault affects the functional behaviour of the system permanently
- **Temporary fault:** A fault that is present temporarily, occurs anytime and affects the system for finite, but unknown time intervals (caused by environmental conditions, e.g.,

cosmic rays, foreign particles, temperature, pressure, vibrations, power supply fluctuations, electromagnetic interference, static electric discharge, etc.) and doesn't cause any permanent damage to the logic of the system

- **Intermittent fault:** A fault that is caused by non-environmental conditions, such as minor values of component parameters, wear-out or critical timings (hazards, races, clock skews, etc.), loose or weak solder connections

Permanent faults are easily localized and have well-defined fault models (like stuck-at-0, stuck-at-1, bridging, stuck-open, stuck-on etc.). Intermittent faults can use traditional fault models with repetitive stress tests. But temporary faults do not have precise fault modeling techniques for all fault characteristics.

2.2 Static and Dynamic Physical Defects

Most physical failures (up to 75%) in CMOS circuits stem from short and open faults while the remainder can be declared unobservable or insignificant and hence remain undetected. In other words, the fault effect cannot be propagated to an observable point. Physical defects in can normally be divided into two classes: inter-gate shorts or shorts between logic gates and intra-gate shorts or shorts within a logic gate. In this research, the effects of resistive shorts and resistive opens present within logic gates in CMOS circuits are studied.

2.2.1 Static Fault Library

This analysis is based on a static CMOS library applied to a primary gate circuit with two groups of faults (short and open) [27]. The basic static fault library was reorganized pertaining to the resistive defect requirements [1]. The synthesis procedure or logic design begins with the specification for the desired terminal behaviour of a gate network. To synthesize a fault, a fault-free gate in the circuit is replaced using the previously generated library based faulty gate. The circuit behaviour is observed in the presence of this fault.

2.2.1.1 Shorts

Shorts are unintentional connections between otherwise non-connected circuit leads, and have been identified as an important type of IC defect. Shorts can be caused during an IC's manufacture, or during normal life of a microchip.

Previous studies [35] confirmed that shorts within CMOS gates are not fully modeled by gate level logic faults. The voltage levels and logic values of the shorted circuit leads depend on the transistor strengths in the affected gates. Intermediate voltage levels at shorted nodes are common consequences. In order to model shorts accurately and realistically, the resistance value of shorts should be considered. It is found that circuit behaviour can change drastically for even

slight variations in the resistance value of a bridge connection. This makes a circuit very vulnerable to circuit degradation over time.

2.2.1.2 Opens

Generally, a missing contact, thinner metal connection, higher number of via, poly breaks, scaling of the devices and the increase in complexity of the fabrication processes lead to open defects in CMOS technology. A high proportion of customer returns are due to open and resistive open defects, and thus leading to the conclusion that the test coverage is poorer for open defects than for bridges, which causes higher escape rate [24]. The probability of open defects highly increases as we are moving from aluminium to copper in more advanced technology (from CMOS 0.13μm and below).

2.2.2 Dynamic Fault Library

Resistive open and resistive bridging faults create additional positive or negative difference in the system clock speed. This makes the fault dynamic in nature, as it doesn't produce a static or fixed effect on the potential difference between any two circuit nodes where a fault has occurred. Instead, a timing error is generated. For modeling dynamic behaviours of shorts and opens, physical wire connection of a static defect in a circuit (shorts or opens) is replaced by a

resistor and a simple electrical analysis of the circuit is performed to obtain the timing variations which occurred during propagation of a logic value from gate inputs to gate output. All primitive gates are subjected to all combinations of input vectors and exhaustive fault list is exercised on every fault location. Detailed fault locations for all gates are emphasized in Chapter 4

2.3 Logical Fault Model

A logical fault provides a suitable representation for effect of physical failures on the operation of a modeled system. A logical fault model makes the fault analysis problem a logical problem, rather than a physical one. Different physical faults can be modeled by the same logical faults and hence the complexity will be greatly reduced. Tests derived for logical faults can be useful for analysing and understanding those physical faults whose effect on the circuit behaviour is too complex and can not be justified [18]. The static behaviour of commonly observed physical faults such as shorts and opens produces logical failures, with large delay values. However, when a physical defect leads to excessive delays on signal paths instead of altering the logic function of the circuit; it is no longer a static defect. Such unknown and unpredictable defect behaviours make it very difficult to analyze a fault.Those physical defects which have an inexplicable effect on the logic output of a system can be modeled as dynamically behaving static (logical) faults.

2.4 Levels of Logical Fault Models

Modeling faults is based on modeling of the circuit. A logical fault can modeled in different levels of circuit design hierarchy, which are referred as levels of abstraction [18], [36].

- Behavioural level (High level) circuit description is based on a HDL (Hardware Description Language) approach. This level has fewer implementation details and is not exactly correlated to manufacturing defects
- At the register-transfer level (RTL or logic level), stuck-at faults are the most accepted fault models in digital testing. This level contains registers, modules, net list of gates (AND, OR, NOT, NAND, NOR, XOR) and interconnect structures. This level consists of all gate-level faults, bridging faults and delay faults
- Transistor-level or Switch-level (low level) fault, models consist of stuck-open type of faults, which are also known to be technology-dependent faults. This level establishes transistor-level details in a circuit and provides the basis of CMOS networks.

Dynamic effect of physical failures on a digital system can be further investigated by altering the electrical parameters like resistance or voltage in a faulty circuit injected with a static short or open defect. Modeling the dynamic nature of bridging and open defects would be more precise for a transistor-level CMOS circuit.

CHAPTER 3

SWITCH-LEVEL MOSFET MODEL

Switch-level representation of a transistor or a MOSFET can be defined as "an electronic device that acts like an electrically activated switch but has no moving parts, so it can switch millions of times per second."

The representation of a MOSFET as a switch provides an opportunity to utilize the resistance parameter of the circuit. By symbolizing the connection between drain and source of a MOSFET as a transistor resistance, the effect of the resistive faults subjected to the circuit can be calculated in the form of equivalent circuit resistance. The switch consists of two fixed terminals corresponding to the ***S*** and ***D*** terminals of the transistor. In addition, there is a movable contact that, depending on its position, determines whether the switch is open or closed. The position of the contact is controlled by the voltage applied to the gate terminal ***G***.

3.1 Transistor-level Fault Model

Classical stuck-at-fault models do not correspond to some significant failure modes, especially in the case of lower level circuit abstractions. In complex gates, the physical nodes do not directly match up to nodes in a comparable gate level network. Hence, many physical opens and shorts cannot be satisfactorily represented at the gate level. Modeling physical defects at lower abstraction levels can make the process more accurate and actual physical defects can be closely examined. Considerations of failure modes at the switch level or circuit level are alternatives to gate level modeling.

3.1.1 Transistor as a Resistor

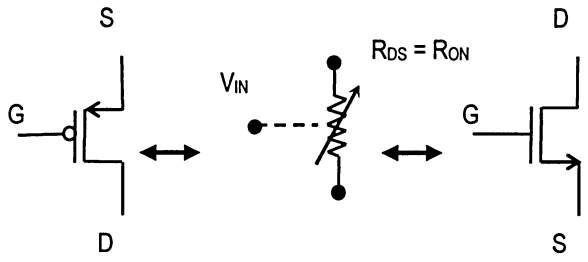
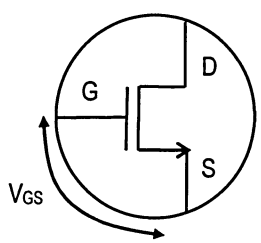


Figure 1 MOSFET as a voltage-controlled resistance

A transistor is an active component of an electronic circuit consisting of a small block of semi-conducting material to which at least three electrical contacts are made. A transistor is also

known as a MOSFET (*metal-oxide semiconductor field-effect transistor*) or a MOS transistor. One of the three terminals can be used to control the flow of current through the other two terminals. A MOSFET can be modeled as a 3-terminal device that acts as a voltage controlled resistance (Figure 1). In digital logic applications a MOS transistor is operated in a way that its resistance is either always high (off transistor) or very low (on transistor). A transistor can be used as an amplifier, detector, or switch.

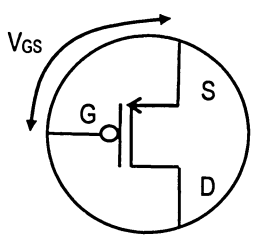
3.1.2 Switch Models for CMOS Transistors



Logic 1 turns the switch on

Logic 0 turns the switch off

(a) n-channel MOSFET or NMOS



Logic 0 turns the switch off

Logic 1 turns the switch on

(b) p-channel MOSFET or PMOS

Figure 2 Logic operation of a MOSFET

CMOS technology utilizes two types of transistor: ***n***-channel and ***p***-channel; depending on the type of semiconductor material used for the resistance controlled terminals. The two differ in

the mechanism governing the conduction of a current through them and in the characteristics of the semiconductor materials used in their implementation. However, the most important thing is the behavioural difference in the two types of transistor. This behaviour is modeled using switches controlled by voltages corresponding to logic 0 and logic 1.

The symbol for an ***n***-channel transistor is shown in Figure 2(a) and a symbol for a ***p***-channel transistor is shown in Figure 2(b). The transistor has three terminals: the gate (***G***), the source (***S***), and the drain (***D***). The voltage applied between ***G*** and ***S*** determines whether a path for current to flow exists between ***D*** and ***S*** (for NMOS) or between ***S*** and ***D*** (for PMOS). If a path exists, it is said that the transistor is ON, and if a path does not exist, the transistor is OFF. For a NMOS device (Figure 2(a)), the voltage between gate and source (V_{GS}) of the transistor is normally zero or positive i.e. when $V_{GS} = V_{DD}$, the transistor is ON and if $V_{GS} = 0$ Volts, the transistor is OFF. On the other hand a PMOS transistor, behaves in a complementary manner. It is ON when $V_{GS} =$ 0 Volts and is OFF for $V_{GS} = V_{DD}$. An n-channel MOSFET when OFF ($V_{GS} = 0$ Volts), the resistance between its drain and source (R_{DS}) or the transistor on-resistance (R_{ON}) is very high and it is inversely proportional to the voltage at the transistor gate (V_{GS}). For a PMOS device, the operation is similar to that of NMOS, except the fact that source is at a higher voltage than drain, and V_{GS} is negative or zero. R_{ON} has a very high value for $V_{GS} = 0$ Volts and unlike NMOS, it decreases with an algebraic fall in the V_{GS} value.

3.1.3 Dynamic Behaviour of a MOSFET

Dynamic as well as static properties of short and open faults are analyzed as a function of the defect resistance in static primitive gate circuits. Mathematical formulas are derived for calculating increased propagation delay at the output of a gate. The variable quantities throughout are n (number of gate inputs), equivalent circuit resistance, input combinations and the fault locations. Nominal resistive short resistance values (R_{SH}) and nominal resistive open resistance value (R_O) are used to formulate a fault pattern showing changing delay value at the functional output.

A CMOS primitive gate consists of serial/parallel PMOS/NMOS combined with parallel/serial NMOS/PMOS network. According to the structure of any logic gate, equivalent digital models can be derived by solving the parameters resulting from these serial/parallel connections. Considering the circuit utilities such as resistance, capacitance and number of MOSFET's involved, the resistive effect of a physical circuit change can be expressed in the form of total logic propagation delay at the output. This delay is associated with the serial and parallel connections of n MOSFETs due to the propagation of a correct or faulty logic value through a particular circuit path to its output. In order to make the RC equivalent network, every transistor in the circuit is replaced with the switch-level MOSFET model as shown in Figure 1 and using the theory explained in this chapter.

3.1.4 Average MOSFET Switching Resistance (R_{ON})

Consider a NMOS circuit in the Figure 3. The transistor is off initially, $V_{GS} = 0$ and the drain is at V_{DD}. If the gate voltage of the MOSFET is varied from zero to V_{DD}, a current is given by the Eqn: 3.1 and Eqn: 3.2, flows through the transistor initially [3].

$$I_D = \frac{K_N' W}{2L}(V_{DD} - V_{THN})^2 \qquad \text{(Eqn: 3.1)}$$

$$I_D = \frac{\beta}{2}(V_{DD} - V_{THN})^2 \qquad \text{(Eqn: 3.2)}$$

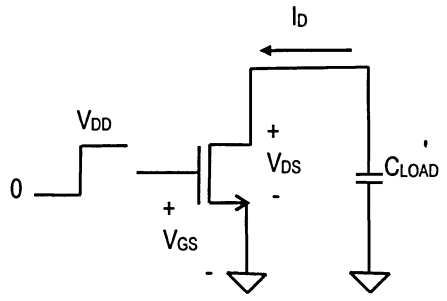


Figure 3 ***n*-channel MOSFET switching circuit**

Point A in the Figure 4 shows the operating point of the MOSFET prior to switching the voltage to $V_{DD} = 3.3$V. After switching occurs, the operating point moves to point B and follows the curve $V_{GS} = V_{DD}$ until $I_D = 0$ and $V_{DS} = 0$, point C. At this point, the NMOS is ON.

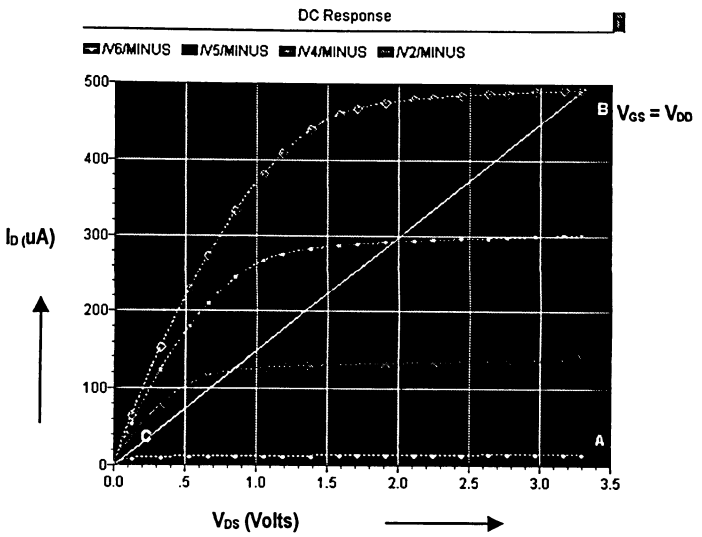


Figure 4 IV plot for 0.35 μm NMOS transistor to estimate average switching resistance

An estimate of the resistance between the drain and source (R_{ON}) for a NMOS (R_N) is given by the reciprocal slope of the line BC in Figure 4, or can be expressed as shown in Eqn: 3.3 [3],

$$R_N = \frac{V_{DD}}{\frac{K_N' W}{2L}(V_{DD} - V_{THN})^2} \qquad \text{(Eqn: 3.3)}$$

Where,

V_{DD} = Operating voltage

W/L = Aspect ratio

K' = Transconductance parameter of a MOSFET

V_{TH} = Threshold voltage.

Assumptions for switch-level fault analysis:

- A MOSFET can be modeled as a 3-terminal device that acts as a voltage controlled resistance, R_{ON} (Figure 1) [30]
- In digital logic applications a MOS transistor is operated in a way that its resistance is either always high (OFF transistor) or very low (ON transistor)
- MOSFET is operating in triode region

3.2 Average MOSFET Load Capacitance (C_{MOSFET})

The switching characteristics of digital integrated circuits essentially state the overall operating speed of digital systems. The dynamic performance requirements of a digital system are usually among the most important design specifications that must be met by the circuit designer. Therefore, the switching speed of the circuits must be approximated and optimized very early in the design phase. The conventional approach for determining the switching speed of a digital system is based on the assumption that the loads are mainly capacitive and lumped. The dynamic behaviour of the circuit can be estimated easily once the load is determined. The standard delay estimation approaches seek to classify three main components of the gate load, all of which are assumed to be purely capacitive.

- Intrinsic parasitic capacitances of the transistors
- Interconnect (line) capacitances

- Input capacitances of the fan-out gates

For a transistor-level fault analysis, the first component of capacitive parasitic is of prime importance. These parasitic components are mainly responsible for the intrinsic delay of logic gates, and they can be modeled with reasonably high accuracy for gate delay estimation. The extraction of transistor parasitic from physical structure is fairly a trivial task. The parasitic capacitances associated with a MOSFET symbol are shown in Figure 5 as lumped elements between the device terminals ***G***-gate, ***S***-source, ***D***-drain and ***B***-bulk.

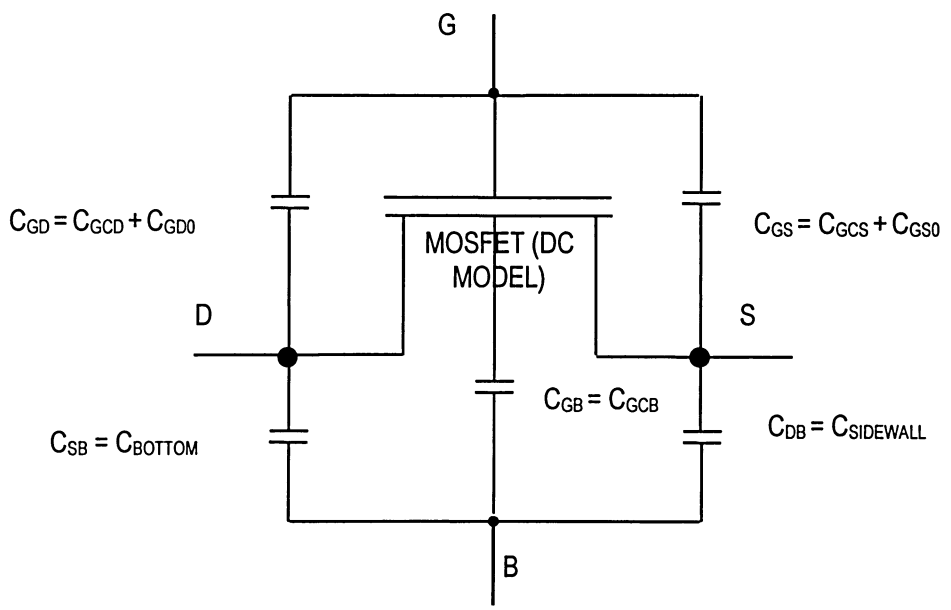


Figure 5 Lumped representation of parasitic MOSFET capacitances

Based on the physical design [9], the parasitic capacitive load (C_{MOSFET}) of a MOSFET device can be divided into two major categories:

- Oxide-related capacitance (C_{OXIDE})
- The depletion regions for reverse-biased pn-junction of the drain and source– Diffusion/Junction capacitances ($C_{JUNCTION}$)

3.2.1 Oxide-related Capacitances

Structurally, the gate of a MOS transistor is detached from the channel by the gate oxide which leads to the gate capacitance, C_{GATE} and can be decomposed as follows

$$C_{GATE} = C_{OX}\,WL \text{ and } C_{OX} = \varepsilon_{OX}/T_{OX}$$

This capacitance contributes to the parasitics developed due to channel charge and the MOS composition. Looking at a cross-sectional view and the top view of a typical n-channel MOSFET (Figure 6), it is seen that the gate electrode overlaps both the source region and the drain region at the edges. One of the main contributions of MOSFET structure into the intrinsic parasitic is due to the channel overlap. The source and drain of a MOSFET diffuse laterally under the oxide layer by an amount X_D. The expansion relates the effective channel length (L) of a MOSFET to the drawn length by the following expression (as seen from Figure 5).

$$L_D = L - 2*X_D$$

This also gives rise to a linear, fixed capacitance called overlap capacitance. Since X_D is technology dependent, it is usually combined with C_{OX}. The overlap capacitances arising due to this physical attribute are gate-source overlap capacitance, C_{GS0}; gate-drain overlap capacitance, C_{GD0} and gate-bulk overlap capacitance, C_{GB0}. All the overlap capacitances are voltage–independent, i.e. they do not depend on the bias conditions. Assuming that both the source and the drain diffusion regions have the same width W, the overlap capacitances can be formulated as:

$$C_{GS0} = C_{GD0} = C_{OX}XDW = \tfrac{1}{2}C_{OX}W\,(L-L_D)$$

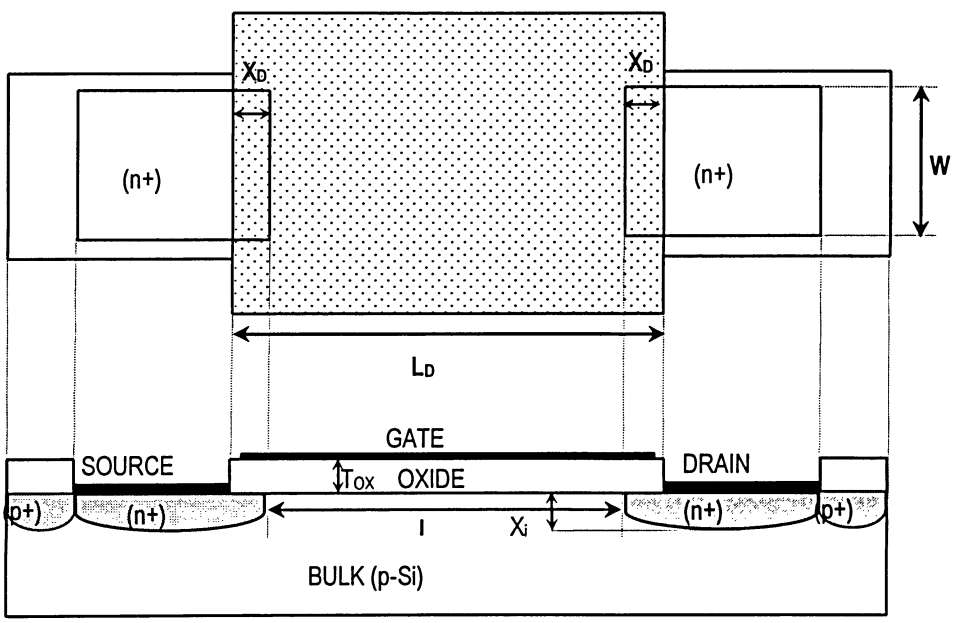


Figure 6 Cross-sectional view and the top view of a typical *n*-channel MOSFET

Given that, the channel region is connected to the source, the drain as well as the substrate, we can categorize three capacitances between gate and the other three regions, namely C_{GCS}, C_{GCD} and C_{GCB}, respectively. These capacitances result from the interaction between the gate voltage and the channel charge and can sum up to be known as gate-to-channel capacitance ($C_{CHANNEL}$). In reality, the gate-to-channel capacitance is non-linear and voltage dependent. The distributed C_{GS0}, C_{GD0} and C_{GB0} values combined with the relevant overlap capacitance values gives the total oxide capacitance (C_{OXIDE}) between the external terminals.

For calculation purpose, the required overlap capacitance values are obtained from the spice model of an *n*-channel or *p*-channel MOSFET. The total oxide capacitance for a MOSFET can be calculated using the following expression:

$C_{OXIDE} = (C_{GD}/C_{GS}/C_{GB})$ TOTAL; Where, $C_{GS} = C_{GCS} + C_{GS0}$

$$C_{GD} = C_{GCD} + C_{GD0}$$

$$C_{GB} = C_{GCB}$$

The total gate oxide capacitance is mainly determined by the parallel-plate capacitance between the poly-silicon gate and the underlying structures (C_{GD}, C_{GS} and C_{GB}). Hence, the total gate capacitance decreases with decreasing device dimensions (W and L), and increases with decreasing gate oxide thickness. Consequently, MOSFET transistors fabricated using sub-micron technologies have smaller gate capacitances. The fact that they are in direct proportion to each other makes them non-negligible for propagation delay computation. Table 1 presents the oxide related capacitance (C_{OXIDE}) of a MOSFET under three different operating regions.

Table 1 Oxide related capacitance (C_{OXIDE}) of a MOSFET

Capacitance	Cut-off	Linear	Saturation
C_{GB}	$C_{OX}WL$	0	0
C_{GD}	$C_{OX}WX_D$	$\frac{1}{2}(C_{OX}WL)$ + $C_{OX}WX_D$	$\frac{2}{3}C_{OX}WL$ + $C_{OX}WX_D$
C_{GS}	$C_{OX}WX_D$	$\frac{1}{2}(C_{OX}WL)$ + $C_{OX}WX_D$	$\frac{2}{3}C_{OX}WL$ + $C_{OX}WX_D$
C_{OXIDE}	$C_{OX}W(L + 2X_D)$	$C_{OX}W(L + 2X_D)$	$C_{OX}W(\frac{2}{3}L$ + $2X_D)$

3.2.2 Junction Capacitances

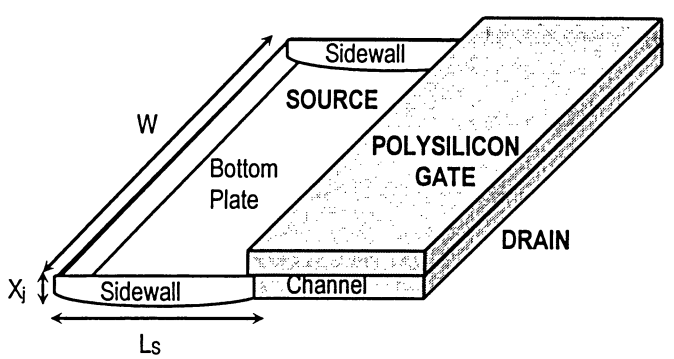


Figure 7 Detailed view of the source junction in a MOSFET

The other half contributing to the internal MOSFET parasitic are the junction capacitances, which further categorize as the voltage-dependent source-bulk and drain-bulk capacitances, C_{SB}

and C_{DB}, respectively. Both of these are caused due to depletion charge surrounding the respective source or drain diffusion regions set in the substrate. The source-bulk and drain-bulk junctions are reverse-biased under normal operating conditions of the MOSFET and the amount of capacitance at these junctions is a function of applied terminal voltages. It is non-linear and decreases with the rise in reverse-bias.

As understood from the Figure 7, capacitance in the bottom plate junction can expressed as:

$$C_{SB} = C_{BOTTOM} = C_j W L_S$$

Here $L_D = L_S$

Capacitance in the sidewall junction can be expressed as:

$$C_{DB} = C_{SIDEWALL} = C_{jsw}(2L_S + W)$$

Therefore, total junction capacitance ($C_{JUNCTION}$) is:

$$C_{JUNCTION} = C_{BOTTOM} + C_{SIDEWALL}$$

$$\begin{aligned} & C_{JUNCTION} \\ & = C_{SB} + C_{DB} \\ & = C_j W L_S + C_{jsw}(2L_S + W) \\ & = C_j * Area + C_{jsw} * Perimeter \end{aligned}$$

Therefore, total parasitic capacitive load (C_{MOSFET}) is:

$$C_{MOSFET} = C_{JUNCTION} + C_{OXIDE}$$

Where, L_S = Sidewall length

C_{OX} = Gate oxide capacitance per area

C_j = Zero-bias bottom depletion capacitance

C_{jsw} = Zero-bias sidewall depletion capacitance

ε_{OX} = Electric field of the gate oxide

T_{OX} = Gate oxide thickness

W = Drawn channel width

L = Drawn channel length

L_D = Effective channel length

X_D = Lateral diffusion length.

$L_D = L - 2 * X_D$

CHAPTER 4

TRANSISTOR-LEVEL TO GATE-LEVEL RESISTIVE FAULT MODEL MAPPING

As CMOS has emerged as an important technology for VLSI, testing of large CMOS networks has become a crucial issue. The classical stuck-at fault model assumptions are not sufficient for modeling certain faults that are specific to a CMOS-based VLSI technology. This applies particularly when systems with a high reliability or high availability such as space applications are considered. Depending on the technology, typical physical defects such as CMOS dynamic faults may not be covered by stuck-at fault models. Therefore, new fault models have been introduced at different description levels to increase the accuracy of fault modeling.

Transistor-level fault model is more accurate than gate-level fault model. However, its fault simulation, fault emulation, and test pattern generation are degraded in comparison to teat of gate-level. In order to maintain the efficiency resulting from gate-level modeling while the

accuracy of the fault model is increased, transistor-level to gate-level fault mapping is required. The following chapter is dedicated to mapping of dynamic transistor-level faults to the gate-level for the primitive gates NOR, OR, NAND, AND, INVERTER.

4.1 NOR*n* and OR*n* Fault List

It is known that accuracy of internal node values cannot be reached just by assuming a circuit at the gate-level. Figure 8(a) shows a gate-level NOR circuit. Figure 8(b) shows the transistor-level circuit NOR circuit. At the gate-level, faults can only be injected or diagnosed on input and output pins. Injecting a fault in a circuit may result in different output values according to different input combinations.

By symbolizing the connection between drain and source of a MOSFET as a transistor resistance (as seen in Figure 8(c)), the effect of the resistive faults subjected to the circuit can be calculated in the form of equivalent circuit resistance. Figure 8(b) shows a transistor-level CMOS NOR gate with 3 inputs, where $n = 3$. n is an integer ($n \geq 2$) and it not only symbolizes the total number of inputs of a gate, but also the i^{th} ($1 \geq i \geq n$) input of a gate. I_{iN} is the i^{th} NMOS input and I_{iP} is the i^{th} PMOS input, which are both branches of I_i. In case of NOR gate, I_i, I_{iP}, and I_{iN} function as the same node for short faults but are act as separate nodes for open faults.

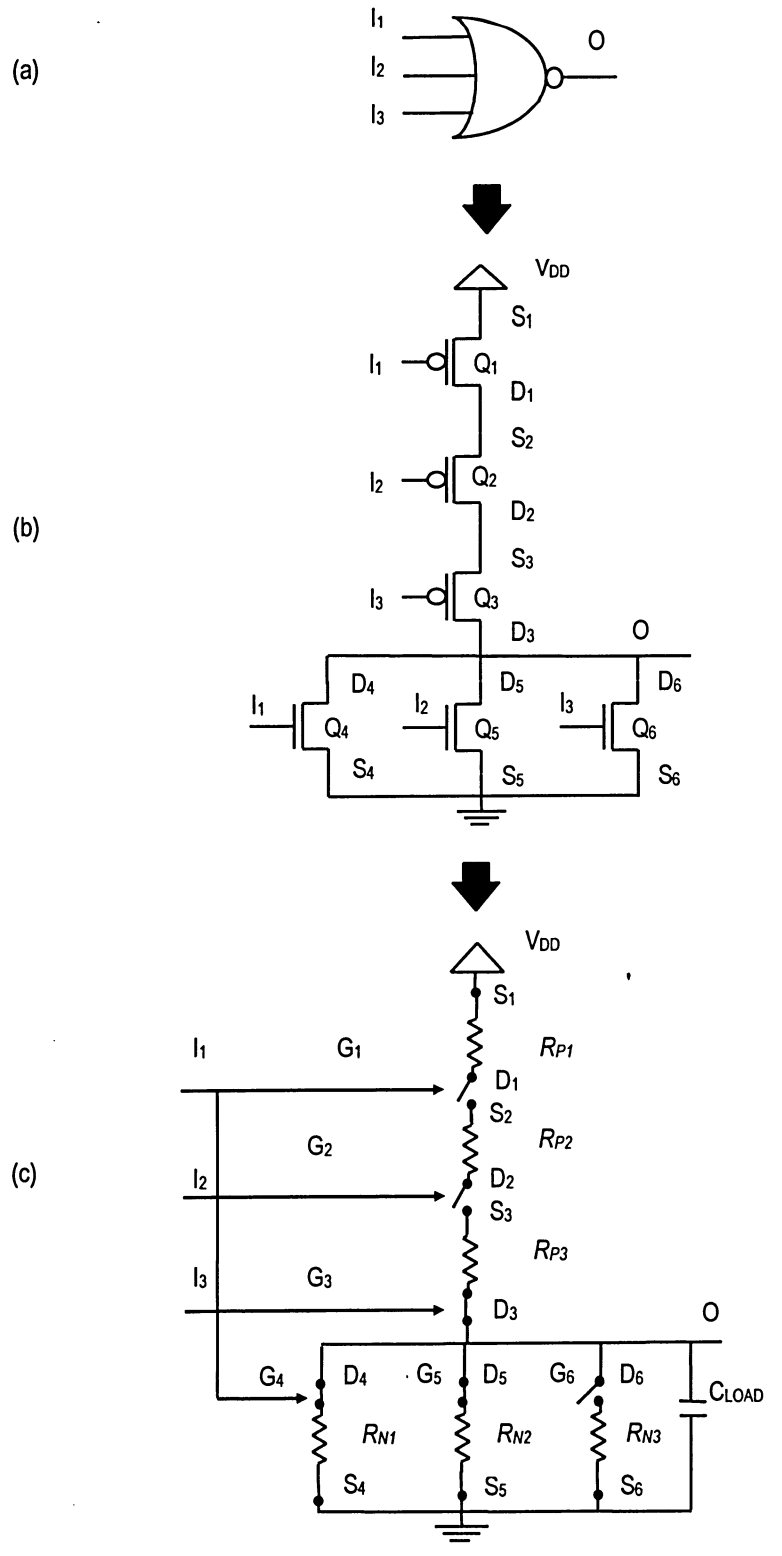


Figure 8 (a) Gate-level, (b) Transistor-level and (c) Switch-level representation for a 3-input NOR Gate

Figure 8(c) shows the switch-level structure for the 2-input NOR gate, which has a serial connection in PMOS network and a parallel connection in the NMOS. Parallel and serial connections of identical MOSFETs play an important role in the delay calculations [3]. The transistors on the PMOS side of the circuit shown in Figure 8(c) are represented by their ON-resistances. For instance, PMOS1 transistor is R_{P1}, PMOS2 is R_{P2}, NMOS1 is R_{N1} and NMOS2 is R_{N2}. Further conventions for transistor resistances are done in the same manner.

4.1.1 NOR*n* and OR*n* Short Faults

For a NOR gate, all faults are subjected to the PMOS network. The list of short faults for an n-input NOR gate and n-input OR gate can be categorized as follows:

- Short between D_{iP} and power, $(1 \leq i \leq n)$
- Short between D_{iP} and ground, $(1 \leq i \leq n - 1)$
- Short between I_i and D_{kP}, $(1 \leq i \leq n; k \leq i \leq n - 1)$
- Short between D_{iP} and D_{kP}, $(1 \leq k \leq n - 1 ; 1 \leq i \leq n - 1$ and $k \neq i)$
- For OR gate, Short between O and ground and between O and power, where $O = D_n)$
- For OR gate, Short between O and O'

Some faults are redundant and are not expressed separately when they are assumed to be resistive shorts. For instance, a short between I_1 and D_1 or I_2 and D_1 or I_3 and D_1 or I_n and D_1 will

have the same delay results. Where I_i symbolizes one of the NOR i^{th} input where ($1 \leq i \leq n$). Similar is the case for the connections; I_i *to* D_2, I_i *to* D_3, and *Ii to* D_4... I_i *to* D_n and I_i *to* O. An illustration for the representation of logic short as a resistive short is shown in Figure 9. Figure 9(a) shows a logic short between the nodes, PMOS input I_{2P} and PMOS drain D_3 and the same fault is converted to a resistive short with a defect resistor R_{SH} replacing the short connection.

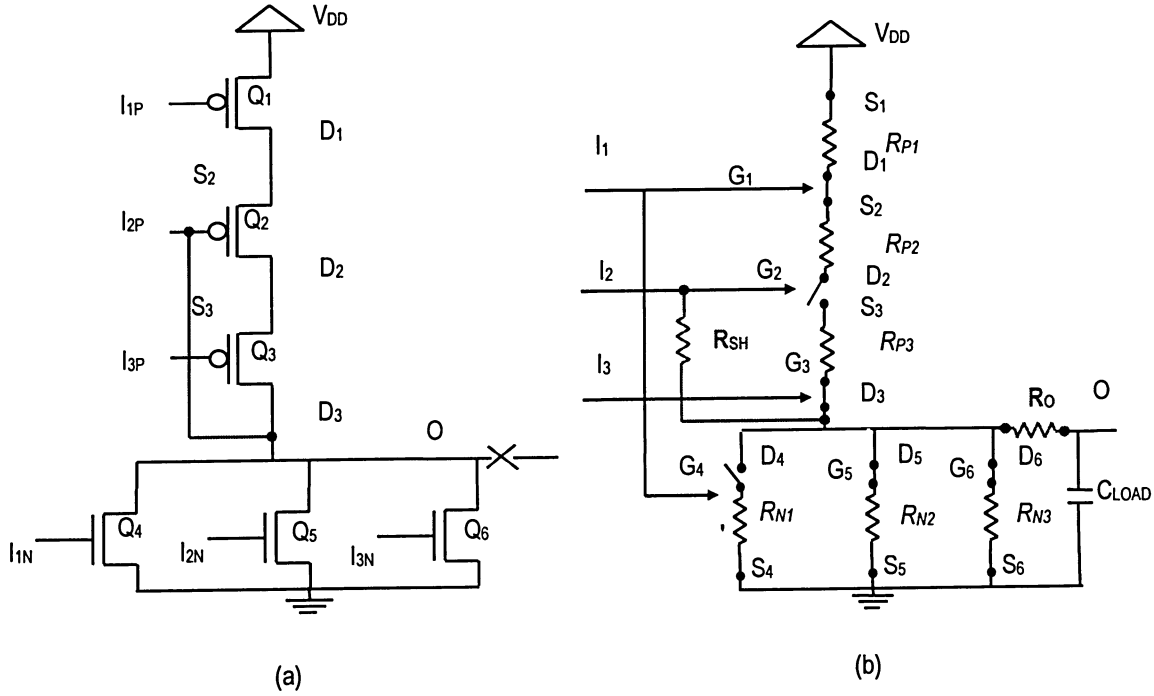


Figure 9 3-input NOR Gate injected with (a) Logic short fault between PMOS input I_{2P} and PMOS drain D_3 ; Logic open fault at the output, O (b) Resistive short between PMOS input I_{2P} and PMOS drain D_3 ; Resistive open at the output, O

Also, D_n and O is a common node (i = 1 to n). Hence, it is not necessary to analyze the fault caused by D_n connections to ground due to similarities in results. D_1 and S_2 are the same nodes; thus, only D_1 is analyzed. Comparing the CMOS circuit diagram for a NOR gate in Figure 8 to

that of an OR gate (NOR + INVERTER = OR) in Figure 10 it can be assumed that the short and open fault list for NOR gate can be applied to an OR gate too.

A logic open at the output of the gate-level representation of 3-input NOR gate in Figure 9(a), is shown with a resistive open having defect resistance of R_O Ω at the same fault location in Figure 9(b). An open connection at the output ***O'*** of the OR gate would have a different logic or delay result as compared to the open fault at output ***O*** of the NOR gate.

4.1.2 NOR*n* and OR*n* Open Faults

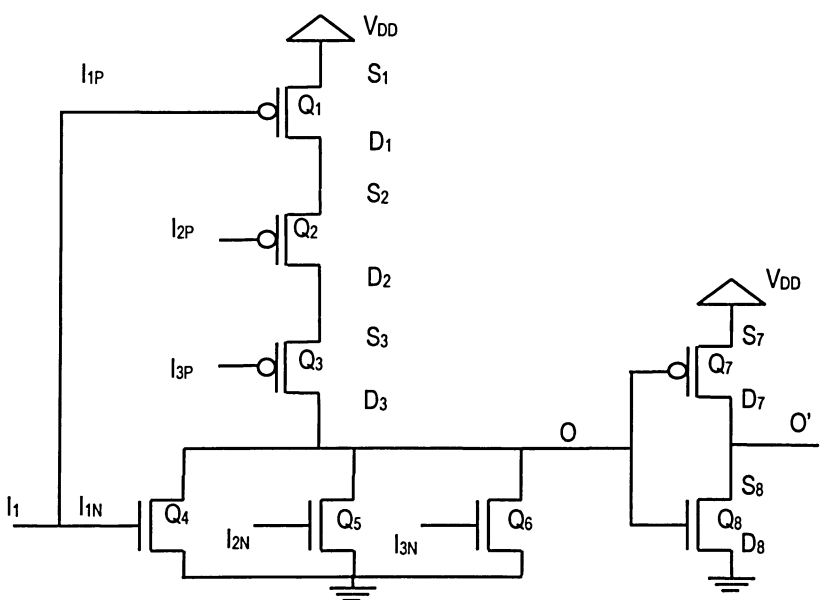


Figure 10 3-input OR Gate

The second group consists of open faults in the NMOS and the PMOS network accordingly. For an n-input NOR gate and n-input OR gate, resistive open faults can be finalized as:

- For all low input, D_{iP} is open
- For all high input D_{iN} is open
- For all low input, S_{iP} is open
- For all high input S_{iN} is open
- O is open
- For OR gate, O' is open

D_i represents a drain belonging to NMOS or PMOS. When ($1 \leq i \leq n$), D_i is a PMOS drain (D_{iP}). D_i is a NMOS drain (D_{iN}) if ($n+1 \leq i \leq 2n$). Similar illustration for the representation of logic open as a resistive open is shown in Figure 9.

4.2 NAND*n* and AND*n* Fault List

Figure 11 presents the gate-level and switch-level representation of a 3-input NAND gate. Unlike NOR gate, all short faults in a NAND gate are subjected to NMOS network of the gate. A complete list of static bridging faults occurring in NAND*n* gate and AND*n* gate are as follows:

4.2.1 NAND*n* and AND*n* Short Faults

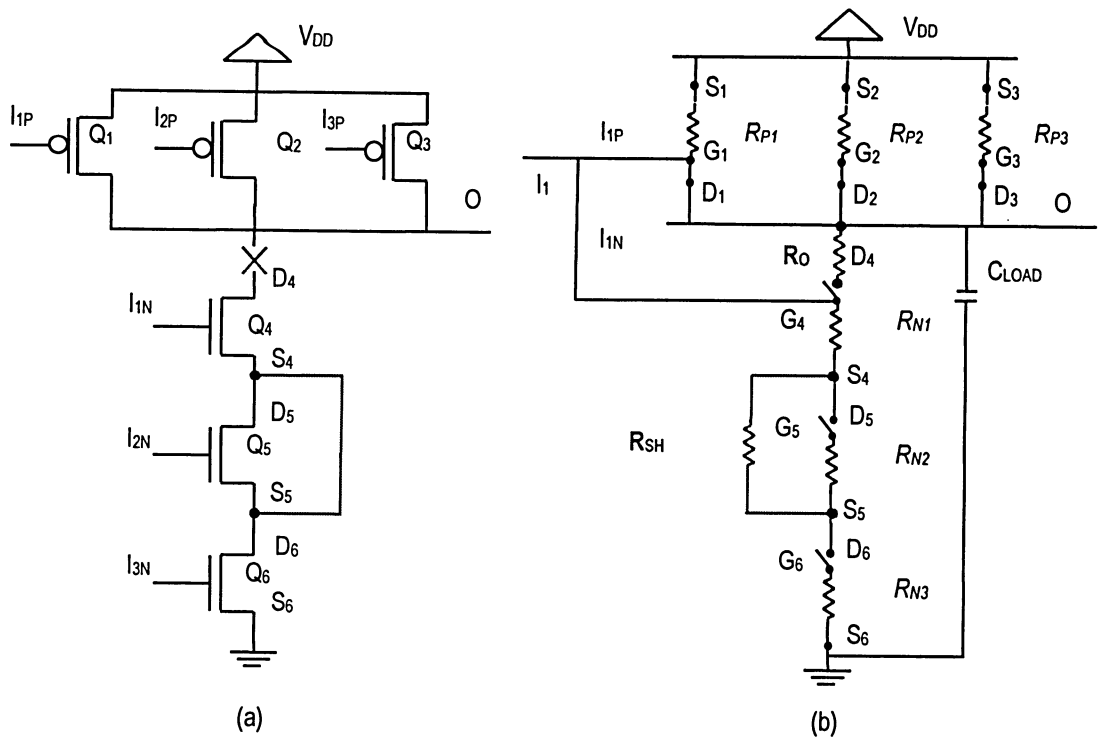


Figure 11 3-input NAND Gate injected with (a) Logic short fault between NMOS sources S_4 and S_5; Logic open at NMOS drain D_4 (b) Resistive short between NMOS sources S_4 and S_5; Resistive open at NMOS drain D_4

- Short between S_i and power, $(1 \leq i \leq n - 1)$
- Short between S_i and ground, $(1 \leq i \leq n - 1)$
- Short between I_i and S_{kn}, $(1 \leq i \leq n;\ n+1 \leq k \leq 2n)$
- Short between S_{in} and S_{kn}, $(n + 1 \leq k \leq 2n - 1\ ;\ n + 1 \leq i \leq 2n - 1$ and $k \neq i)$

- Short between I_i and O, $(1 \leq i \leq n)$
- For AND gate, Short between O and ground and between O and power, where $O = D_n$)
- For AND gate, Short between O and O'

Figure 11a) and Figure 11(b) show a 3-input NAND gate with a short connection between NMOS sources S_4 and S_5 respectively and a open on the NMOS drain D_4.

4.2.2 NAND*n* and AND*n* Open Faults

The open fault category for NAND gate is analogous to the open fault group of NOR gate. Both NMOS and PMOS network can be actively targeted with open faults for a NAND gate. For an n-input NOR gate, resistive open faults can be finalized as:

- For all low input, S_{iN} is open
- For all high input S_{iP} is open
- For all low input, D_{iN} is open
- For all high input D_{iP} is open
- O is open
- For AND gate, O' is open

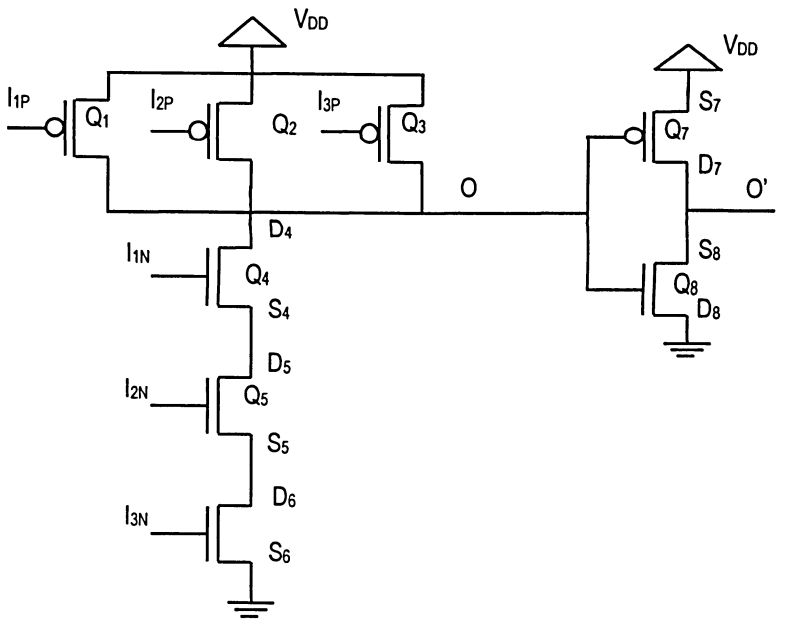


Figure 12 3-input AND Gate

A resistive open at the output ***O'*** of an AND gate shown in Figure 12 will have an added propagation delay as compared to the delay caused due to an open node at output ***O***.

4.3 INVERTER Fault List

The most basic representation of CMOS logic, is provided by a NOT gate or an INVERTER. Its circuit consists of one ***n***-channel transistor and one ***p***-channel transistor as shown by the gate-level and switch-level representations shown in Figure 13, parts (a) and (b) respectively. . A CMOS Inverter has a limited number of shorts and opens possible. The only short fault possible

according to the fault list required for this research is a short between input and output of the gate. And opens or breaks can materialize in the circuit at the source nodes S_1 and S_2 and drain nodes D_1 and D_2 respectively.

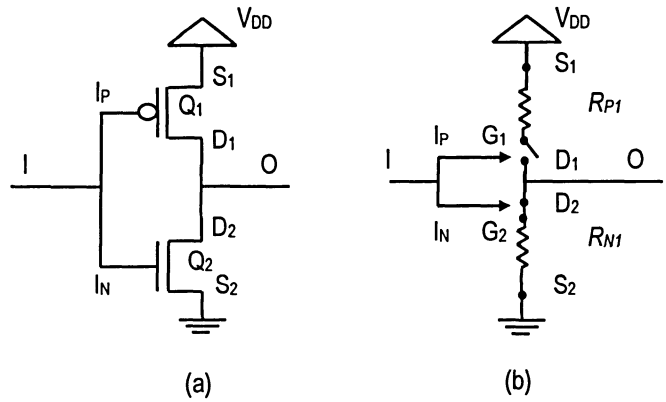


Figure 13 CMOS Inverter (a) Gate-level, (b) Switch-level

CHAPTER 5

PROPAGATION DELAY AND OUTPUT VOLTAGE

Referring to Section 3.1.4, Eqn: 5.1 and Eqn: 5.2 show the NMOS-on-resistance and PMOS-on-resistance respectively

$$R_{ON} = R_N = \frac{V_{DD}}{\frac{K_N' W}{2L}(V_{DD} - V_{THN})^2} \qquad \text{(Eqn: 5.1)}$$

$$R_{ON} = R_P = \frac{V_{DD}}{\frac{K_P' W}{2L}(V_{DD} - V_{THP})^2} \qquad \text{(Eqn: 5.2)}$$

5.1 All High Input Case

For the all high input case (for example, $I_1I_2I_3$ = 111), NMOS transistors are on and PMOS are off. Generalizing the NMOS structure for all primitive gates, both the parallel and the serial connections of NMOS are discussed. For n number of NMOS transistors in a logic gate,

The high-to-low propagation delay-time (t_{PHL}) for this gate is,

Serial NMOS connection:

$$t_{PHL} = 0.7R_N^{'}nC_{LOAD} \qquad \text{(Eqn: 5.3)}$$

Parallel NMOS connection:

$$t_{PHL} = 0.7\{R_N^{'}/n\}C_{LOAD} \qquad \text{(Eqn: 5.4)}$$

Considering Eqn: 5.3

$$\frac{1}{R_N^{'}} = \frac{0.7C_{LOAD}}{t_{PHL}} * n \qquad \text{(Eqn: 5.5)}$$

Considering Eqn: 5.4

$$\frac{1}{R_N^{'}} = \frac{0.7C_{LOAD}}{t_{PHL}} * \frac{1}{n} \qquad \text{(Eqn: 5.6)}$$

Substituting the value for $R^{'}_N$, from Eqn: 5.1 and Eqn: 5.2

$$\frac{\frac{K_N^{'}W}{2L}(V_{OUT} - V_{THN})^2}{V_{OUT}} = \frac{0.7nC_{LOAD}}{t_{PHL}} \qquad \text{(Eqn: 5.7)}$$

$$\frac{(V_{OUT} - V_{THN})^2}{V_{OUT}} = \frac{0.7nC_{LOAD} * 2L}{t_{PHL}K_N^{'}W} \qquad \text{(Eqn: 5.8)}$$

$$V_{OUT} - 2V_{THN} + \frac{V_{THN}^2}{V_{OUT}} = nX_N \qquad \text{(Eqn: 5.9)}$$

Where,

$$X_N = \frac{0.7C_{LOAD} * 2L}{t_{PHL}K_N^{'}W} \qquad \text{(Eqn: 5.10)}$$

Therefore, for serial NMOS combination

$$V_{OUT} + \frac{V_{THN}^2}{V_{OUT}} = nX_N + 2V_{THN} \qquad \text{(Eqn: 5.11)}$$

And for parallel NMOS connection,

$$V_{OUT} + \frac{V_{THN}^2}{V_{OUT}} = \frac{X_N}{n} + 2V_{THN} \qquad \text{(Eqn: 5.12)}$$

Rearranging Eqn: 5.11 makes it fit the quadratic equation format that can have two roots as shown below:

$$V_{OUT}^2 - (nX_N + 2V_{THN})V_{OUT} + V_{THN}^2 = 0 \qquad \text{(Eqn: 5.13)}$$

And re-organizing Eqn: 5.12, makes it a quadratic equation format, as shown below:

$$V_{OUT}^2 - (\frac{X_N}{n} + 2V_{THN})V_{OUT} + V_{THN}^2 = 0 \qquad \text{(Eqn: 5.14)}$$

Replacing X_N, n and V_{THN} with numerical values in Eqn: 5.13 and Eqn: 5.14, the voltage level at the output (V_{OUT}) of a gate is obtained using quadratic formula [42].

5.2 All Low Input Case

On the contrary, the V_{OUT} value for all low input case will be completely influenced by the PMOS transistors, unlike the all high input case. For the all low input case (for example, $I_1I_2I_3$ = 000), PMOS transistors are on and NMOS are off.

The low-to-high propagation delay-time (t_{PLH}) for this gate is,

Serial PMOS connection:

$$t_{PLH} = 0.7R_P^{'}nC_{LOAD} \qquad \text{(Eqn: 5.15)}$$

Parallel PMOS connection:

$$t_{PLH} = 0.7\{R_P^{'} / n\}C_{LOAD} \qquad \text{(Eqn: 5.16)}$$

Correlating Eqn: 5.2 and Eqn: 5.15;

$$\frac{1}{R_P^{'}} = \frac{0.7C_{LOAD}}{t_{PLH}} * n \qquad \text{(Eqn: 5.17)}$$

And similarly, correlating Eqn: 5.2 and Eqn: 5.16;

$$\frac{1}{R_P^{'}} = \frac{0.7C_{LOAD}}{t_{PLH}} * \frac{1}{n} \qquad \text{(Eqn: 5.18)}$$

The output voltage values for serial PMOS connection,

$$V_{OUT}^2 - (nX_P + 2V_{THP})V_{OUT} + V_{THP}^2 = 0 \qquad \text{(Eqn: 5.19)}$$

And correspondingly, for parallel PMOS connection,

$$V_{OUT}^2 - \{(X_P/n) + 2V_{THP}\}V_{OUT} + V_{THP}^2 = 0 \qquad \text{(Eqn: 5.20)}$$

X_P value is calculated analogous to method with used for calculating X_N in Eqn: 5.10, and is shown below:

$$X_P = \frac{0.7C_{LOAD} * 2L}{t_{PLH}K_P^{'}W} \qquad \text{(Eqn: 5.21)}$$

Replacing X_N, n and V_{THN} with numerical values in Eqn: 5.19 and Eqn: 5.20, the voltage level at the output (V_{OUT}) of a gate is obtained using quadratic formula [42].

5.3 Mixed Input Case

A mixed input case (for example, $I_1I_2I_3$ = 001,010,100,110,101 etc.), is a combination of NMOS and PMOS transistors that are on and the rest are off. For this particular category, the numbers of on PMOS and on NMOS transistors affect the combined delay at the gate output. Hence, the propagation delay consequential from activities of MOSFETs both on PMOS and

NMOS sides is presented correspondingly. The variable n has different values for PMOS and NMOS in this case. The identical number of active PMOS is termed by n_P and the identical number of active NMOS is n_N. For instance, when the primitive gate consists of serially linked PMOS and a parallel formation of NMOS, then the total propagation delay at the output of that gate, can be represented as,

$$t_P = 0.7R^{'}C_{LOAD} \qquad \text{(Eqn: 5.22)}$$

$$t_P = 0.7\{n_P R_P^{'} + R_N^{'} / n_N\}C_{LOAD} \qquad \text{(Eqn: 5.23)}$$

And alternatively, a parallel PMOS connection with serial NMOS connection is regarded in the following equations,

$$t_P = 0.7R^{'}C_{LOAD} \qquad \text{(Eqn: 5.24)}$$

$$t_P = 0.7\{n_N R_N^{'} + R_P^{'} / n_P\}C_{LOAD} \qquad \text{(Eqn: 5.25)}$$

Thus, the output voltage due to the mixed effect of NMOS and PMOS networks can be derived as following:

Referring to Eqn: 5.22,

$$\frac{1}{R'} = \frac{0.7C_{LOAD}}{t_P} \qquad \text{(Eqn: 5.26)}$$

$$R' = n_P R'_P + R'_N / n_N \qquad \text{(Eqn: 5.27)}$$

$$R' = n_P \{\frac{2LV_{OUT}}{K'_P W (V_{OUT} - V_{THP})^2}\} + \frac{1}{n_N} \{\frac{2LV_{OUT}}{K'_N W (V_{OUT} - V_{THN})^2}\} \qquad \text{(Eqn: 5.28)}$$

Since both PMOS and NMOS networks respectively have substantial contributions in deteriorating the clock speed, an average of all their respective parameters is applied to Eqn: 5.27.

$$R' = \{n_P + \frac{1}{n_N}\} \{\frac{2LV_{OUT}}{K'_{PN} W (V_{OUT} - V_{THPN})^2}\} \qquad \text{(Eqn: 5.29)}$$

Where,

K'_{PN} = Average Transconductance value of the CMOS gate.

V_{THPN} = Average threshold voltage value of the CMOS gate.

Correlating Eqn: 5.26 and Eqn: 5.27, a quadratic equation is formed:

$$V_{OUT}^2 - \{n_P + \frac{1}{n_N}\} X_{PN} V_{OUT} + V_{THPN}^2 = 0 \qquad \text{(Eqn: 5.30)}$$

Where,

$$X_{PN} = \frac{0.7C_{LOAD} * 2L}{t_P K'_{PN} W} \qquad \text{(Eqn: 5.31)}$$

Substituting numerical values for all the parameters into Eqn: 5.30, V_{OUT} value is obtained [42].

For Eqn: 5.3 to Eqn: 5.31, variables are listed as follows,

t_P = Total propagation delay

t_{PHL} = High-to-low propagation time

t_{PLH} = Low-to-high propagation time

R'_N = Equivalent switching resistance in the NMOS network

R'_P = Equivalent switching resistance in the PMOS network

R' = Equivalent circuit resistance including resistive elements from NMOS and PMOS sides respectively

n = Identical number of PMOS transistors for all low input case

= Identical number of NMOS transistors for all high input case

For mixed input case,

n_P = Number of active or ON PMOS

n_N = Number of active or ON NMOS.

CHAPTER 6

NOR GATE : PROPAGATION DELAY AND OUTPUT VOLTAGE CALCULATION

A faulty or fault-free NOR gate propagation delay computation requires replacement of the electrical parameters with their respective numerical values in the delay equation derived in Chapter 5. For instance, estimation of NMOS transistor on-resistance (R_N) in Eqn: 5.1 or PMOS transistor on-resistance (R_N) in Eqn: 5.2 would require the nominal values of transistor parameters: V_{DD} , W/L, $K`$, and V_{TH}. It is a known fact that [21][20][19][13][6] resistive physical failures have a devastating effect on the timing of the circuits as the CMOS technology narrows down. Similarly, considering Eqn: 5.3 or Eqn: 5.4 it is evident that to calculate the propagation delay value at the output of any primitive gate, variables like n, equivalent circuit resistance and equivalent circuit capacitance (C_{LOAD}) are required.

To complement the theory described in Chapter 5, delay calculations for two different input combinations in a NOR gate are considered. All low input vector ($I_1I_2I_3$ = 000) symbolizing a serial connection of three PMOS transistors and a mixed input vector like $I_1I_2I_3$ = 010, which denotes a combination of serial/parallel connection of PMOS/NMOS or vice versa. The experimental results are based on the assumption that the clock speed is below 1 MHz. Short and open connections, resistive in nature, are introduced into the circuit.

6.1 Transistor Parameters

Table 2 R_{ON} values for 32nm, PMOS and NMOS transistors respectively.

R_{ON} ()		V_{DD} (volts)	W/L	$K`_n$ (A/V^2)	V_{TH} (volts)
R_N	1556.70	0.6	50/2	9.8E-04	0.42
R_P	2550.53	0.6	100/2	2.7E-04	0.41

The gate output voltage values are derived through the delay results. For this example, transistor channel length of 32nm is considered and the BPTM SPICE model parameters [39] are obtained. The operating voltage is 0.6 V. Simulations are performed for a single fault at a time replaced by a resistor of each defect resistance value (mentioned in Table 5) individually.

Table 3 Transistor parameters for various CMOS technologies

CMOS (nm)	R_{ON} (Ω)		V_{DD} (volts)	W (m)	L (m)
32	R_N	1556.70	0.6	8.00E-07	3.2E-08
	R_P	2550.53	0.6	1.60E-06	3.2E-08
45	R_N	302.68	0.7	1.13E-06	4.5E-08
	R_P	510.62	0.7	2.25E-06	4.5E-08
90	R_N	429.43	1.2	2.25E-06	9E-08
	R_P	771.75	1.2	4.50E-06	9E-08
180	R_N	238.97	1.8	4.50E-06	1.8E-07
	R_P	564.96	1.8	9.00E-06	1.8E-07
350	R_N	196.51	3.3	8.75E-06	3.5E-07
	R_P	403.87	3.3	1.75E-05	3.5E-07

For 32nm technology, the NMOS and PMOS on- resistance values are calculated using the Eqn: 3.3 and are presented in Table 2. The aspect ratio adopted from [3] has been used for all CMOS technologies presented in this paper. The transistor resistance values with the respective operating voltage values for all CMOS technologies investigated are also shown in Table 3.

6.2 Load Capacitance

The load capacitance value for a MOSFET can be calculated by combining the oxide and junction capacitance values for each transistor in a gate circuit. The C_{MOSFET} for PMOS transistor is symbolized as C_{Pi} and the C_{MOSFET} for NMOS is symbolized as C_{Ni} ($1 \leq i \leq n$). Equivalent capacitance value for a serial and parallel connected capacitance network can be calculated using the formulas shown in Table 4. Also, the load capacitance (C_{LOAD}) value for a 32nm technology is calculated based on the theory described above and MOSFET capacitance values for an n-input NOR gate are shown in Table 4 [9].

Table 4 C_{LOAD} value for 32 nm PMOS and NMOS transistors for a NOR Gate

LOAD CAPACITANCE (C_{LOAD}) IN FARAD (F)		
C_P (SERIAL connection):	C_{P1}	2.1E-10
$\frac{1}{C_{SERIES}} = \frac{1}{C_1} + \frac{1}{C_2} + \ldots + \frac{1}{C_n}$	C_{Pi} ($2 \leq i \leq$ n)	4.2E-10
C_N (PARALLEL connection):	C_{Ni} ($1 \leq i \leq$ n)	2.1E-10
$C_{PARALLEL} = C_1 + C_2 + \ldots + C_n$		

6.3 Defect Resistance

Actual or static bridging faults have a nominal resistance value mainly in the range of 0 to 500Ω. This problem has been previously analyzed by choosing a fixed resistance value or by applying a locally exhaustive test set at the bridge location [6]. Transistor-level bridging faults can occur internally (intra-gate) or externally (integrate). This paper focuses on the intra-gate bridging faults, which occur inside the transistor level circuit of a primitive gate.

Table 5 Defect Resistance Range

RESISTIVE DEFECT	RESISTANCE VALUE	EFFECT
Short (R_{SH})	$500\Omega \leq R_{SH} \leq 50\ K\Omega$	Increased delay or speed failure
Open (R_O)	$5K\Omega \leq R_O \leq 500K\Omega$	

Opens can be classified as strong opens (>10MΩ) and weak opens (≤10MΩ) [12]. Strong open defects can cause a circuit to malfunction and even weak open defects can cause it to function poorly with degraded speed at the output. The timing failures produced by these defects make them dynamic faults. Considering the delay inducing property of these faults, they have been addressed as delay faults for the discussion in this paper. After surveying previous studies [25], [23], [16], [12], [10], the defect resistance values for the resistive failures were finalized and are presented in Table 5.

6.4 Resistive Short

A 3-input NOR gate shown in Figure 14 demonstrates how a single short or a single open fault can be injected at the locations provided by the static fault list. The short is then replaced by a defect resistor R_{SH} for a short and R_O for open fault. The resistive short fault is computed first in order to analyze single physical failures. Figure 15 provides a switch-level representation of the (resistive) short shown in Figure 14.

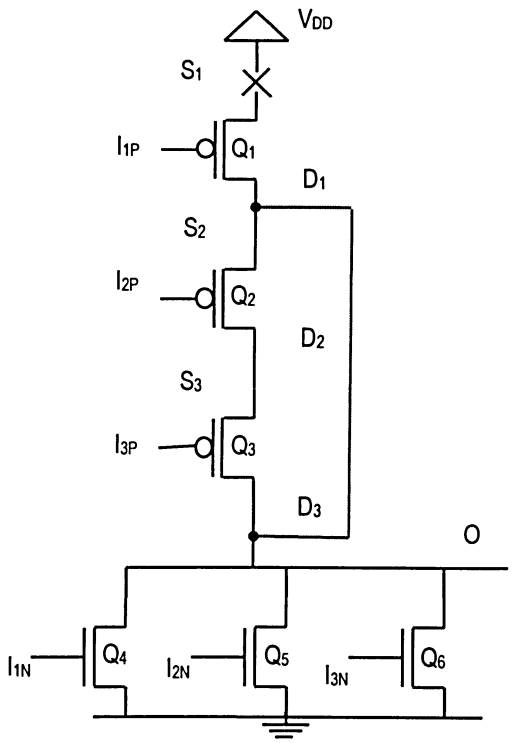


Figure 14 Faulty 3-input NOR gate

6.4.1 All Low Input Combination $I_1I_2I_3 = 000$

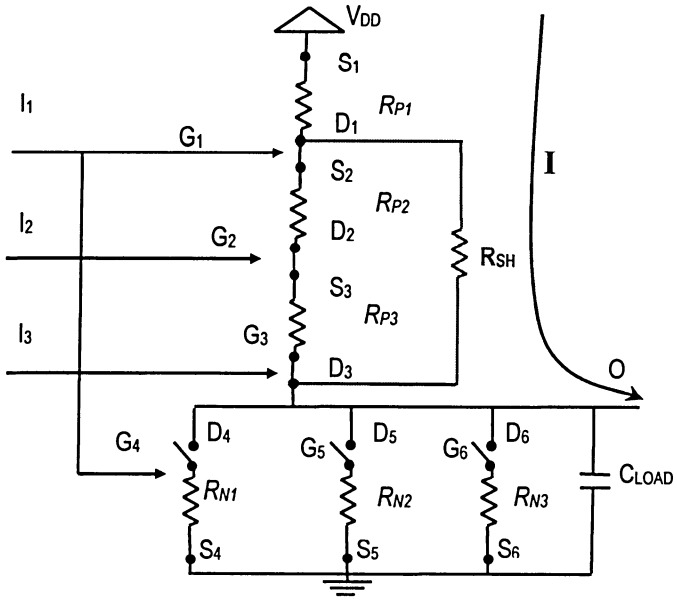


Figure 15 Switch-level 3-input NOR gate; $I_1I_2I_3 = 000$ showing a resistive short fault between PMOS drains D_1 and D_3 respectively

Figure 15 shows a 3-input NOR gate injected with a resistive short fault between D_1 to D_3 (O) on the PMOS side of the gate and an input of $I_1I_2I_3 = 000$ is applied to it. All low input implies that all PMOS transistors are on. Only the PMOS transistors will be responsible for any delay change at the output in this case. Two current paths are formed, one is through the nodes V_{DD}, R_{P1}, R_{P2}, R_{P3} and the output, O; and other one is through the nodes V_{DD}, R_{P1}, R_{SH} and the output, O. All PMOS resistances are in series and their resulting equivalent resistance is in parallel connection to the defect resistance R_{SH}. According to the data summarized in Table 5, initial R_{SH} value is assumed to be 5000Ω. Applying the laws of electric circuit analysis, R'_P or

equivalent PMOS resistance can be determined. The ultimate current path can be symbolised by current, ***I*** shown in Figure 15.

For a serial PMOS network, the low-to-high propagation delay value can be estimated using Eqn: 5.15, as shown earlier in Section 5.1:

$$t_{PLH} = 0.7 R_P' n C_{LOAD}$$

Both PMOS resistances R_{P2} and R_{P3} are in parallel with R_{SH}. And the result of this parallel combination is in series with R_{P1}.

Referring to Table 2, equivalent PMOS resistance is;

$$R_{P1} = R_{P2} = R_{P3} = 2550.53\ \Omega$$

$$R_{SH} = 5000\ \Omega$$

$$R_P' = \{1/(1/(R_{P2} + R_{P3}) + 1/R_{SH})\} + R_{P1}$$

$$R_P' = 5075.55\ \Omega$$

Similarly load capacitance value for the serial connection of three PMOS transistors according to Table 4 is given by;

$$C_{LOAD} = 1/\{(1/C_{P1} + 1/C_{P2} + 1/C_{P3})\} \qquad \text{(Eqn: 6.1)}$$

$$C_{LOAD} = 1.05\text{E-}10\ \text{F}$$

The value of n, in this case $n_P = 3$ is valid. Substituting these parameter values into the delay formula, the propagation delay at the output of the 3-input NOR gate can be obtained.

$t_{PLH} = 0.7 * 5075.55 * 3 * 1.05E\text{-}10$

$t_{PLH} = 1.12E\text{-}06$ seconds

For a low input combination for 3-input NOR gate, Eqn: 5.19 is required to calculate the gate output voltage.

$$V_{OUT}^2 - (nX_P + 2V_{THP})V_{OUT} + V_{THP}^2 = 0$$

Referring to Eqn: 5.21, X_P is given as;

$$X_P = \frac{0.7C_{LOAD} * 2L}{t_{PLH}K_P'W}$$

$$X_P = \frac{0.7*1.05E-10*2*3.2E-08}{1.12E\text{-}06*2.7E\text{-}04*1.6E\text{-}06}$$

$X_P = 0.01$

Hence V_{OUT} can be calculated by replacing X_P, n_P and V_{THP} (Referring to Table 2) with numerical values in Eqn: 5.19 and applying the quadratic formula [42].

$$V_{OUT} = \frac{-(nX_P + 2V_{THP}) \pm \sqrt{(nX_P + 2V_{THP})^2 - 4V_{THP}^2}}{2}$$

$$V_{OUT} = \frac{-(3*0.01 + 2*0.41) \pm \sqrt{(3*0.01 + 2*0.41)^2 - 4*(0.41)^2}}{2}$$

V_{OUT} = 0.095 Volts, 0.313 Volts

The first root for V_{OUT} is accepted.

6.4.2 Mixed Input Combination $I_1I_2I_3 = 010$

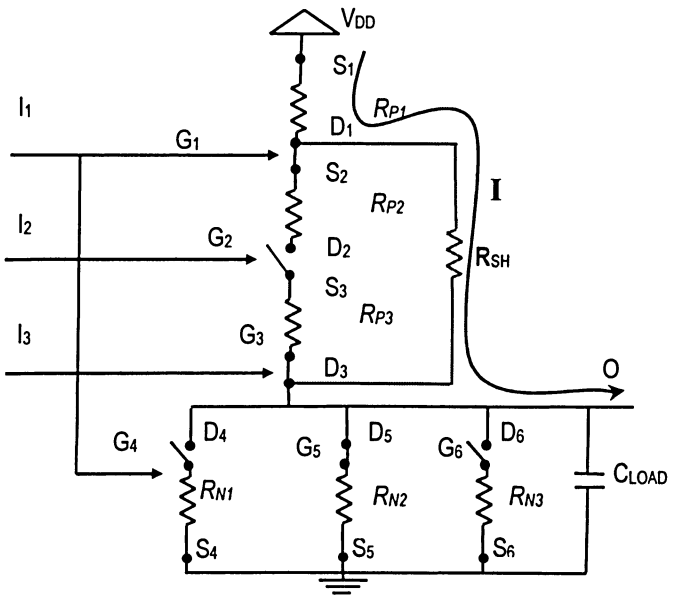


Figure 16 Switch-level 3-input NOR gate; $I_1I_2I_3 = 010$ showing a resistive short fault between PMOS drains D_1 and D_3 respectively

When the same faults in the same gate are subjected to a mixed input vector results differ. For example, in mixed logic input both PMOS and NMOS networks will be accountable for delay variation as seen in Figure 16. The flow of current in the circuit changes to the current path, I shown in the Figure 16.

The total propagation delay due to mixed activities of both CMOS sides is calculated using Eqn: 5.22 and Eqn: 5.23,

$$t_P = 0.7R^{'}C_{LOAD}$$
$$t_P = 0.7\{n_P R_P^{'} + R_N^{'} / n_N\}C_{LOAD}$$

Total PMOS resistance is as a result of a serial connection between $\boldsymbol{R_{PI}}$ and $\boldsymbol{R_{SH}}$, since transistor PMOS2 is OFF and hence PMOS 3 is not directly connected to power source.

Referring to Table 2, equivalent PMOS resistance is;

$R_{SH} = 5000\ \Omega$

$R_{PI} = 2550.53\ \Omega$

$R_P^{'} = R_{P1} + R_{SH}$

$R^{'}_P = 7550.53\ \Omega$

Since $\boldsymbol{R_{PI}}$ is the only active PMOS transistor, the PMOS load capacitance according to Table 4 is;

$C_P = C_{PI}$

$C_P = 2.1\text{E-}10\text{F}$

Referring to Table 2, equivalent NMOS resistance is;

$R'_N = R_{N2}$

$R'_N = 1556.7\ \Omega$

NMOS load capacitance referring to Table 4 is;

$C_N = C_{N2}$

$C_N = 2.1\text{E-}10\ \text{F}$

Number of active PMOS, $\boldsymbol{n_P} = 1$

Number of active NMOS, $\boldsymbol{n_N} = 1$

Total Capacitive load;

$C_{LOAD} = C_P + C_N$

$C_{LOAD} = 4.2\text{E-}10\ \text{F}$

Therefore, the total propagation delay at NOR gate output will be:

$t_P = 0.7\{n_P R_P^{'} + R_N^{'} / n_N\} C_{LOAD}$

$t_P = 0.7 * \{1 * 7550.53 + 1556.7/1\}$ 4.2E-10

$t_P = 2.68$E-06 seconds

For a 3-input NOR gate subjected with a mixed input vector, Eqn: 5.30 is required to calculate the gate output voltage.

$$V_{OUT}^2 - \{n_P + \frac{1}{n_N}\} X_{PN} V_{OUT} + V_{THPN}^2 = 0$$

Where,

$$X_{PN} = \frac{0.7 C_{LOAD} * 2L}{t_P K_{PN}^{'} W}$$

$$X_{PN} = \frac{0.7 * 4.2E-10 * 2 * 3.2E-08}{2.68E-06 * 6.22E-04 * 1.2E-06}$$

$$X_{PN} = 0.0095$$

Hence V_{OUT} can be calculated by applying the quadratic formula to Eqn: 5.30[42].

$$V_{OUT} = \frac{-(nX_{PN} + 2V_{THPN}) \pm \sqrt{(nX_{PN} + 2V_{THPN})^2 - 4V_{THPN}^2}}{2}$$

$V_{OUT} = 0.54$ Volts, 0.32 Volts

The first root for V_{OUT} is accepted.

6.5 Resistive Open

An open fault shown at the PMOS source node, S_1 in Figure 14 can be symbolized as a resistive open defect in the switch-level NOR gate illustration Figure 17 (for all low input vector) and in Figure 18 (for mixed input vector).

6.5.1 All Low Input Combination $I_1I_2I_3 = 000$

Considering the resistive open shown in Figure 17 and assuming that an all low input vector is applied to the NOR gate, it is evident that the open fault forms a serial link with the rest of the PMOS transistors in the circuit. Referring to Table 5, the initial R_O value is assumed to be 5000 Ω.

For a serial PMOS arrangement, the formula from Eqn: 5.15 is again used for resistive opens for the case when all low inputs are applied to a NOR gate.

$$t_{PLH} = 0.7R_P^{'}nC_{LOAD}$$

The serial PMOS combination consists of R_O added to the three PMOS on-resistances R_{P1}, R_{P2}, and R_{P3} respectively. Referring to Table 2 equivalent PMOS resistance is obtained.

$R_{P1} = R_{P2} = R_{P3} = 2550.53\ \Omega$

$R_O = 5000\ \Omega$

$R_P^{'} = R_{SH} + R_{P1} + R_{P2} + R_{P3}$

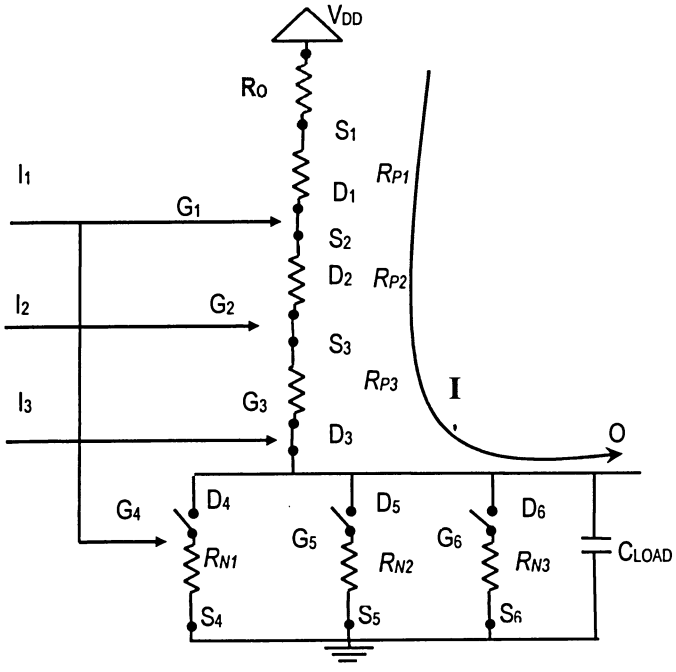


Figure 17 Switch-level 3-input NOR gate; $I_1I_2I_3$ =000, showing a resistive open fault at the output, O

$R_P^{'}$=12651.59 Ω

Number of active PMOS, n_P= 3

Load capacitance value for serial connection of three PMOS transistors and a resistive open defect resistor is similar to Eqn: 6.1 (Referring to Table 4);

$$C_{LOAD} = 1/\{(1/C_{P1} + 1/C_{P2} + 1/C_{P3})\}$$

$$C_{LOAD} = 1.05\text{E-}10 \text{ F}$$

The low-to-high propagation delay for an open fault at the node S_1 of a 3-input NOR gate is shown below:

$$t_{PLH} = 0.7 * 12651.59 * 3 * 1.05\text{E-}10$$

$$t_{PLH} = 2.8\text{E -}06 \text{ SEC}$$

Applying a low input combination to 3-input NOR gate, Eqn: 5.19 is required to calculate the gate output voltage.

$$V_{OUT}^2 - (nX_P + 2V_{THP})V_{OUT} + V_{THP}^2 = 0$$

Referring to Eqn: 5.21, X_P is given as;

$$X_P = \frac{0.7 * 1.05E\text{-}10 * 2 * 3.2E\text{-}08}{2.8E\text{-}06 * 2.7E - 04 * 1.6E\text{-}06}$$

$$X_P = 3.9E{-}03$$

Hence V_{OUT} can be calculated by replacing X_P, n_P and V_{THP} (Referring to Table 2) with numerical values in Eqn: 5.19 and applying the quadratic formula [42].

$$V_{OUT} = \frac{-(nX_P + 2V_{THP}) \pm \sqrt{(nX_P + 2V_{THP})^2 - 4V_{THP}^2}}{2}$$

$$V_{OUT} = 0.5 \text{ Volts}, 0.355 \text{ Volts}$$

The first root for V_{OUT} is accepted.

6.5.2 Mixed Input Combination $I_1I_2I_3 = 110$

For a mixed input vector, a resistive open fault is shown at S_4 instead of S_1, as the PMOS side is totally disconnected from the output of the gate as seen in Figure 18. The NMOS side is responsible for the delay, since there is no physical connection between the power source, V_{DD} and Out (O) as seen in Figure 18. The three NMOS transistors are parallel to each other and the resultant resistance value is serially coupled to the defect resistor. Also the resistive open, forms a serial connection with the NMOS transistor (R_{N1}) in the circuit.

For a parallel NMOS array, the formula in Eqn: 5.4 used for resistive shorts in case of all low inputs can be applied.

$$t_{PHL} = 0.7\{R_N^{'} / n\}C_{LOAD}$$

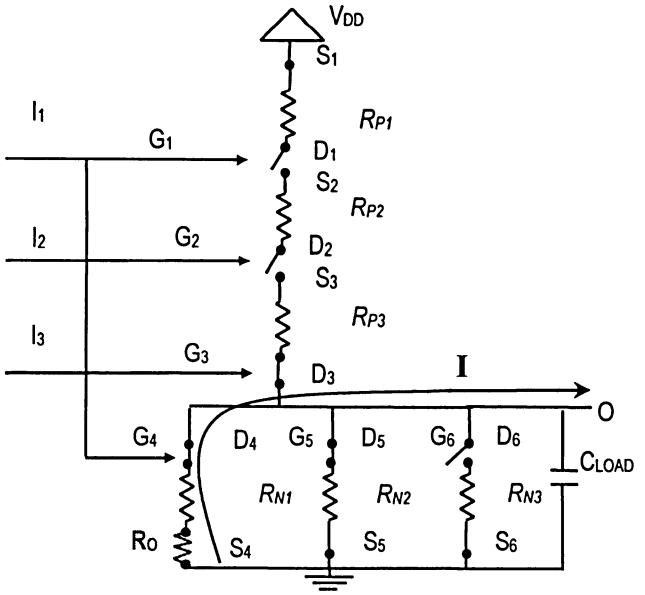


Figure 18 Switch-level 3-input NOR gate; $I_1I_2I_3 = 110$, showing a resistive open fault at NMOS source, S_4

The parallel NMOS combination consists of NMOS on-resistances R_{N1} and R_{N2}. This combination is serial to R_O. Referring to Table 2 equivalent NMOS resistance is obtained.

$R_{N1} = R_{N2} = 1556.7\ \Omega$

$R_O = 5000\ \Omega$

$$R'_N = \frac{1}{\{\frac{1}{R_{N1}} + \frac{1}{R_{N2}}\}} + R_O$$

$R'_N = 5778.35\ \Omega$

Number of active NMOS, $n_N = 2$

Referring to Table 4, load capacitance value for serial connection of three NMOS transistors and a resistive open defect resistor;

$$C_{LOAD} = C_{N1} + C_{N2}$$

$$C_{LOAD} = 4.2\text{E-}10 \text{ F}$$

The low-to-high propagation delay for an open fault at the NMOS node S_4 of a 3-input NOR gate is shown below:

$$t_{PLH} = 0.7 * (5778.35/2) * 4.2\text{E-}10$$

$$t_{PLH} = 8.49\text{E-}07 \text{ seconds}$$

Applying a low input combination to a 3-input NOR gate, Eqn: 5.14 is required to calculate the gate output voltage.

$$V_{OUT}^2 - (\frac{X_N}{n} + 2V_{THN})V_{OUT} + V_{THN}^2 = 0$$

Referring to Eqn: 5.10, X_N is given as;

$$X_N = \frac{0.7 * 4.2E-10 * 2 * 3.2E-08}{8.49E-07 * 6.22E-04 * 1.2E-06}$$

$$X_N = 0.03$$

Hence V_{OUT} can be calculated by replacing X_P, n_P and V_{THP} in Eqn: 5.14 (Referring to Table 2) with numerical values and applying the quadratic formula [42].

$$V_{OUT} = \frac{-(\frac{X_N}{n} + 2V_{THN}) \pm \sqrt{(\frac{X_N}{n} + 2V_{THN})^2 - 4V_{THN}^2}}{2}$$

V_{OUT} = 0.49Volts, 0.36 Volts

First root value for $V_{OUT,}$ is accepted. An output voltage pattern is proposed, based on the propagation delay calculation at various fault sites and for all input combinations in ***n***-input primitive gates. Also, the circuit features to be changed involve channel length or technology specification and of course defect resistance values.

CHAPTER 7

EXPERIMENTAL RESULTS : PROPAGATION DELAY AND OUTPUT VOLTAGE

The three most important variables required for calculating change in propagation delay and output voltage of a gate, injected with resistive faults are: R_{SH} or R_O; t_{PLH} or t_{PHL} or t_P; V_{OUT}. Initially, the strength of the resistive opens and shorts is made variable within a realistic range of resistances starting from nearly strong open/weak bridge (very high resistive) to a weak open/strong bridge (low resistive). Propagation delay and output voltage are calculated for each resistive short and open fault with variable defect resistance as exemplified in Sections 6.4 and 6.5, correspondingly. The nature of the output voltage as opposed to propagation delay is expressed in graphical formats. The delay value is expressed in μseconds and the voltage value in volts. The experimental results for both resistive short and open faults are based on the theory

described in Chapter 5. Spice model parameters for deep sub-micron technologies such as 32 nm, 45 nm, and 90nm are extracted from the Berkeley Predictive Technology Model (BPTM) [39], whereas for sub-micron technologies 350 nm and 180 nm, SPICE model parameters are exercised from (BPTM) [39] and TSMC [41] respectively

7.1 Technology Scaling

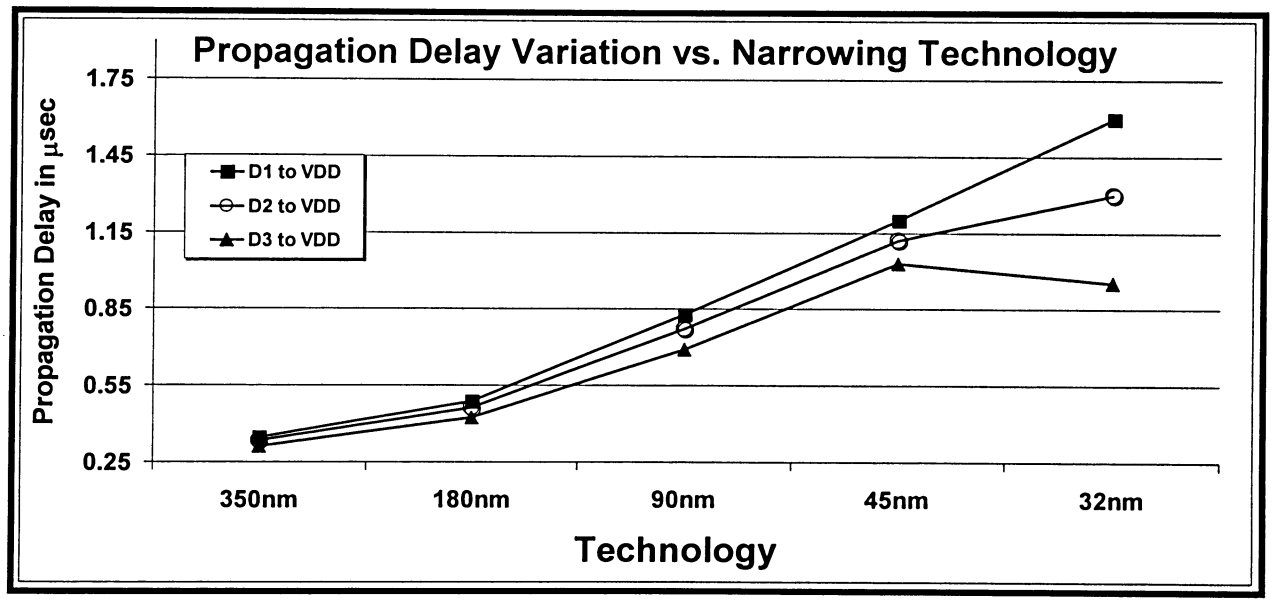


Figure 19 Propagation Delay vs. DSM Technologies

Narrowing technology gives rise to more and more timing issues. This fact can be reinforced by evaluating the comparison of transistor sizes vs. the delay they induce for a certain defect resistance value e.g. 10Kohms for the resistive shorts. Figure 19 shows an illustration for a 3-

input NOR gate again, applied with an all low input vector. The propagation delay value at gate output is evidently rising with the advance of nanometre technology, supporting the fact that physical defects like resistive faults can be disastrous in terms of disturbing the system clock speed. The next subsection demonstrates that delay grows more with rising defect resistance values. Based on this proof, further examination regarding the influence of propagation delay on interruption of logic propagation is carried out in view of Figure 19. An example of 32 nm CMOS technology is used to verify the calculations in Sections 6.4 and 6.5. Section 7.2 presents propagation delay produced by a resistive short fault in a 3-nput NOR Gate for all low input combination, whereas, section 7.4 presents the results of propagation delay induced by a resistive open in the same gate. Sections 7.3 and 7.5 illustrate the effect of propagation delay on the output voltage of a gate for resistive shorts and resistive opens respectively.

7.2 Excess Delay (t) : Resistive Shorts

The fault list for resistive shorts, as explained in Section 4.1.1 can further be scrutinized based on the delay produced due to each type of fault and its different fault locations. A 3-input NOR gate in 32 nm technology is subjected to an input vector $I_1I_2I_3$ = 000. The fault list shown in Figure 20 is deduced from the theory described in section 4.1.1.

Considering the fault locations D_1 *to* V_{DD} and D_2 *to* D_3:

$$R_P^{'}(D_1 toV_{DD}) = (R_{SH}\, parallel R_{P1}) + R_{P2} + R_{P3}$$

$$R_P^{'}(D_2 toD_3) = (R_{SH}\, parallel R_{P2}) + R_{P1} + R_{P3}$$

It is known that, $R_{P1} = R_{P2} = R_{P3} = \ldots\ldots\ldots = R_{Pn}$. Thus, the equivalent resistance ($R^{'}_P$) for both these faults and all others with the same delay are equal. Likewise, D_2 *to* V_{DD} and D_3 *to* V_{DD} represent a delay fault category for all low input combination. An important observation made at this stage is that the delay fault type can be predicted by recording the delay induced by any physical fault in the circuit. These are of course dynamic in nature and can be verified within the three categories shown in Figure 20. Similar predictions can be made for other input combinations, other primitive gates and when applying any other DSM technology. A selected list of faults is discussed in the three graphical comparisons to follow this subsection.

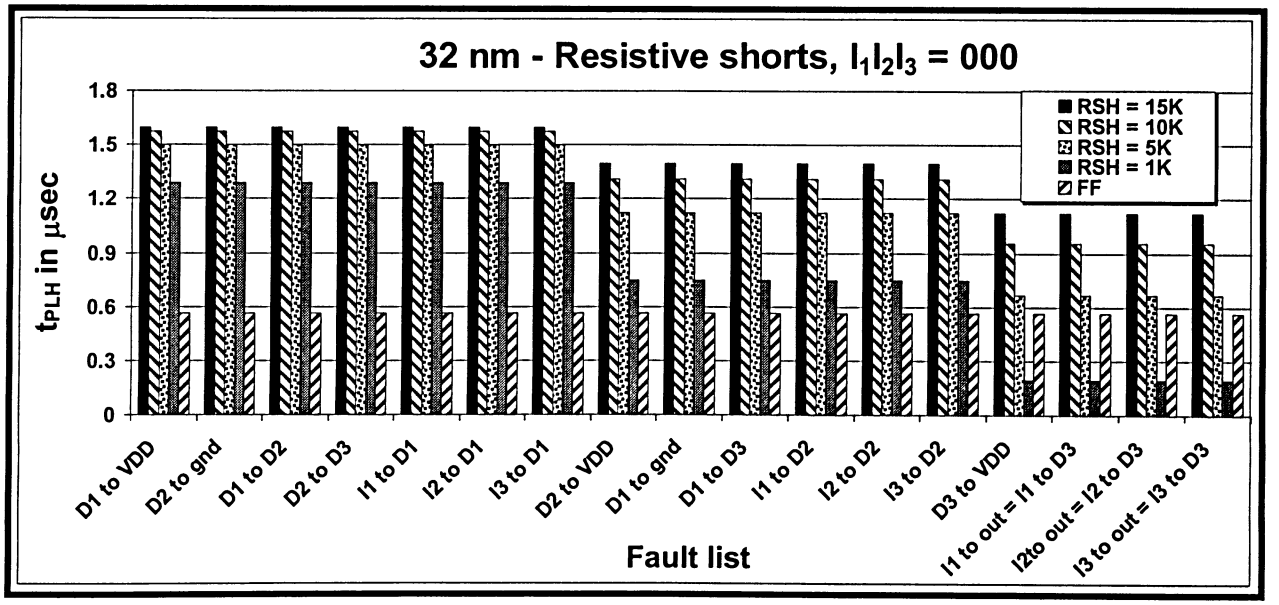


Figure 20 32 nm – t_{PLH} for Resistive Shorts; $I_1I_2I_3 = 000$

Resistive shorts show a distinct delay pattern with significant delay values. The variable resistances used for this type of shorts are FF, 1 KΩ, 5 KΩ, 10 KΩ and 15 KΩ. FF implies a fault-free condition, and more importantly, represents the designed gate delay obtained when there is no fault (static or dynamic) in the circuit However, every circuit tends to have some delay due to the manufacturing processes. The purpose for including reference level (FF) is to get an idea how the circuit degraded in terms of timing due to a resistive short as compared to a totally fault free gate. It also acts as a reference value for showing a positive or negative delay difference (Δt). The results seen in the figures to follow reinforce the fact that resistive failures lead to serious timing issues in a circuit and making it either too fast or too slow.

It is clear that propagation delay rises as the index i ascends from 1 to n, (here, n = 3) in addition to the defect resistance rising from 1KΩ to 15KΩ, for all possible faults in an all low input category. For the fault types D_i to V_{DD}, D_i to ***gnd*** and D_i to D_k (for i = 1 to n, k = 1 to n and $i \neq k$). As explained in Section 3, for the fault types I_i to D_k and I_i to (D_n ***or Out***) the delay remains the same for I_i ranging from i = 1 to n. But, the delay value falls for D_k varying from k =1 to $k = n$.

The delay difference (Δt) between a circuit with resistive defects and a circuit that is (static or dynamic) fault-free,

$\Delta t = t_{PLH} - t_{FF}$; *For all low input case*

$\Delta t = t_{PHL} - t_{FF}$; *For all high input case*

$\Delta t = t_{P} - t_{FF}$; *For a mixed input case*

Where

Δt = delay difference

t_{FF} = fault-free propagation delay of a gate.

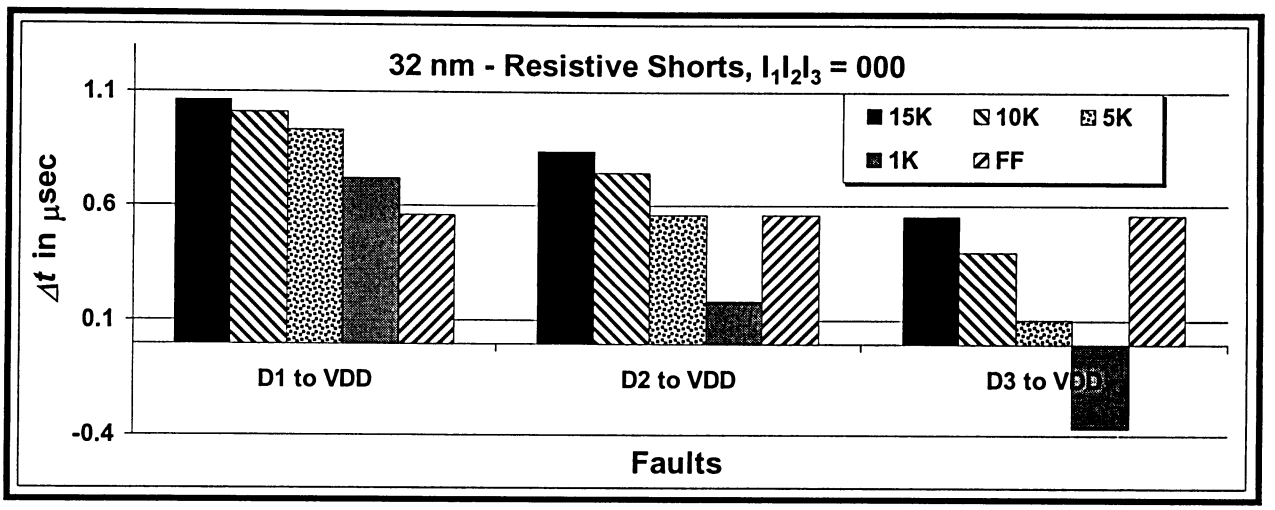


Figure 21 Δt for 32nm-Resistive Shorts; $I_1I_2I_3$ = 000

Figure 21 shows three types of faults injected into a 3-input 32 nm CMOS NOR gate one at a time and the gate is subjected to an all zero input vector. X-axis represents the fault and Y-axis depicts delay difference, Δt in μsec and the legend shows the types of defect resistance in ohms (Ω). The resistive short fault between PMOS drain, D_3 and power has lower delay value for 1KΩ defect resistance as compared to the same configuration for D_2 to power. Similarly, delay due to 1KΩ defect resistance for the fault D_1 to power is the highest among all three D_i to power faults shown in Figure 21. The fault D_1 *to* V_{DD}, makes the NOR gate circuit slower by a significant amount of time, highest being over 1 μsec for R_{SH} = 15000 Ω. Only D_2 *to* V_{DD} is the fault location, which makes the clock speed faster by 0.37 μsec for the defect resistance value, R_{SH} = 1KΩ.

7.3 Propagation Delay vs. Output Voltage : Resistive Shorts

Output voltage versus propagation delay value, for three main kinds of input combinations is provided in this section. All three comparisons have propagation delay value in μsec on the X-axis and output voltage value in volts on the Y-axis. Each fault has one trend line, and is made of four points each labelled with R_{SH} data.

Figure 22 shows three types of faults injected into a 3-input NOR gate one at a time and the gate is subjected to an all zero input vector. All three faults have different orientations for the respective data labels, to create a differentiation among fault lines. The resistive short between PMOS drain, D_3 and power has the lower delay value for 1KΩ defect resistance as compared to the same configuration for D_2 to power. Similarly, delay due to 1KΩ defect resistance for the fault D_1 to power is the highest among all three D_i to power faults which confirms the observation made in section7.2. The output voltage also shows similar behaviour but in a descending order unlike the propagation delay. V_{OUT} values for D_2 to V_{DD} are

- V_{OUT} for R_{P1} = 1K is 0.576 volts
- V_{OUT} for R_{P1} = 5 K is 0.544 volts
- V_{OUT} for R_{P1} = 10 K is 0.534 volts
- V_{OUT} for R_{P1} = 15 K is 0.530 volts

V_{OUT} value, unlike the propagation delay drops with increasing defect resistance.

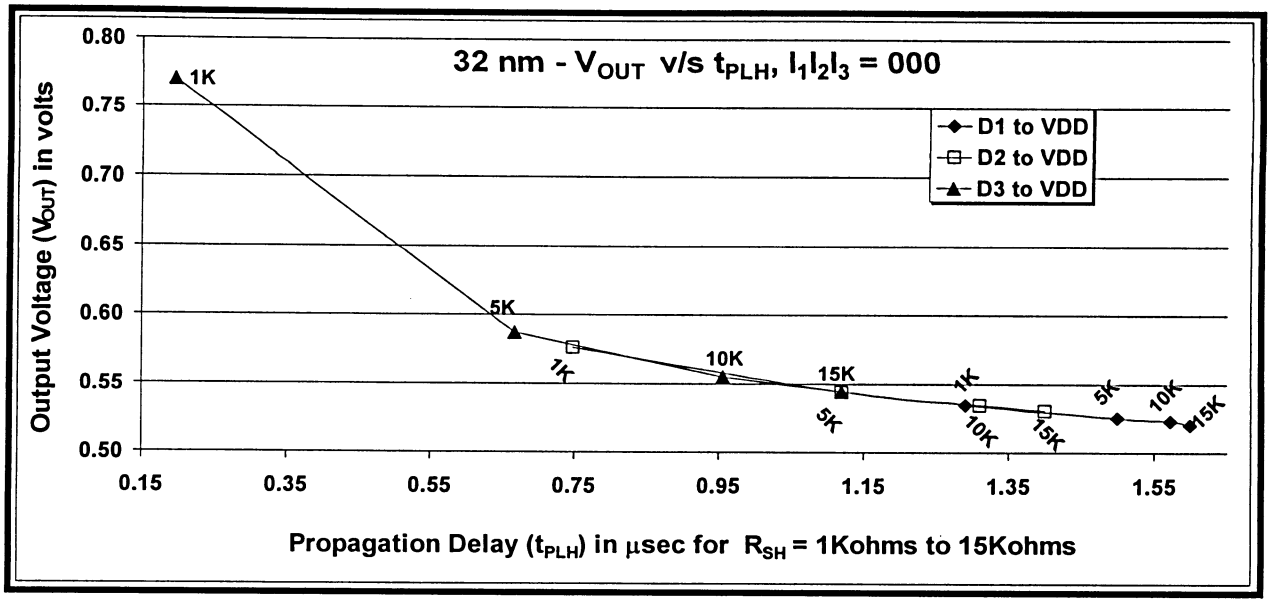


Figure 22 Output Voltage vs. Propagation Delay; Resistive Shorts for $I_1I_2I_3$ = 000

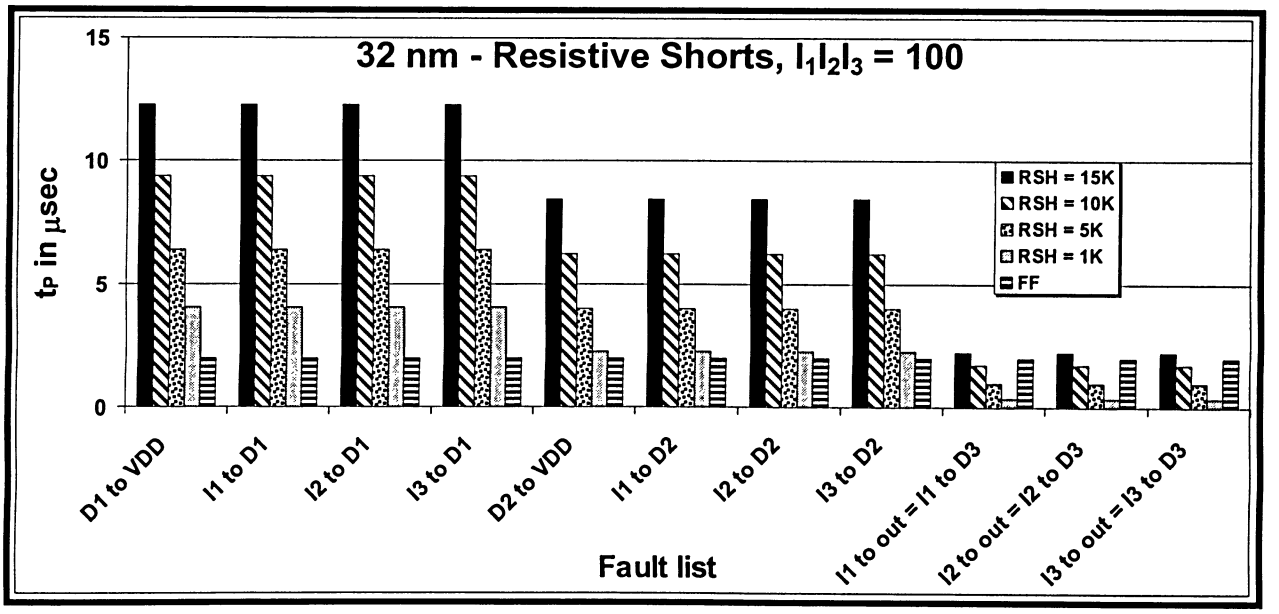


Figure 23 32 nm – t_P for Resistive Shorts; $I_1I_2I_3$ = 100

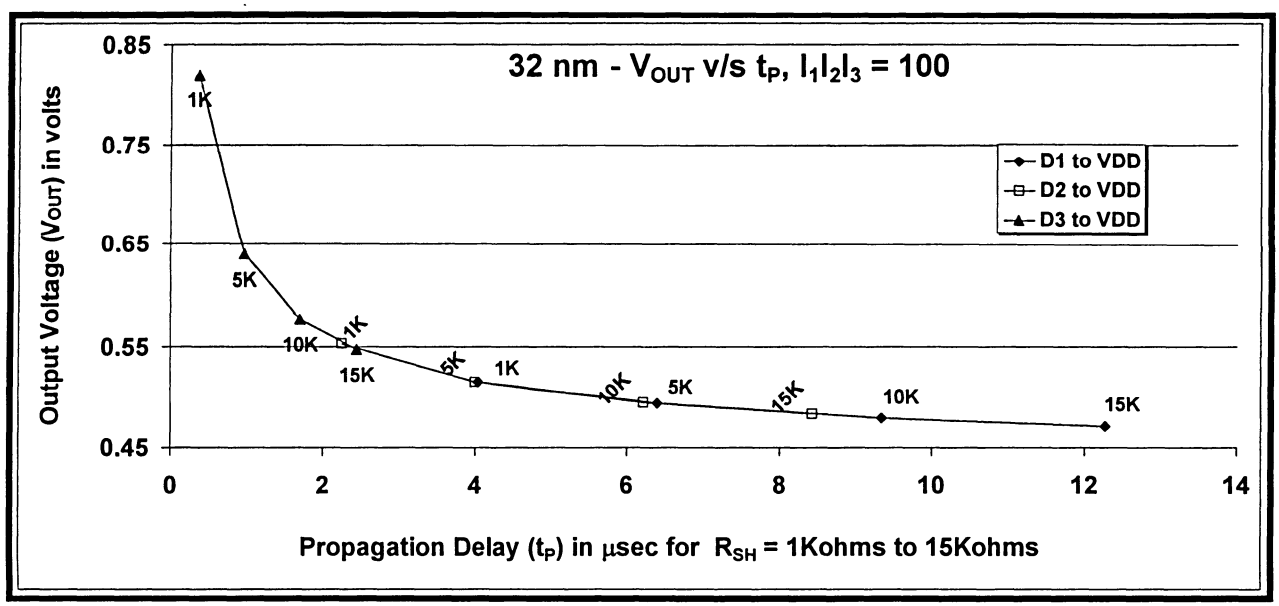


Figure 24 Output Voltage vs. Propagation Delay; Resistive Shorts for $I_1I_2I_3$ = 100

The mixed input case ($I_1I_2I_3$ = 100), has delay value reaching a high of over 12 µsec, which is an inconceivable delay considering the high frequency demands. For 1KΩ of defect resistance, D_3 to V_{DD} fault has an output voltage exceeding 0.6 Volts. Omission of fan-out capacitances leads to such absurd voltage values. The selected faults in Figure 24 stand for the delay categories shown in Figure 23 and they demonstrate the same trend as mentioned for all low input combinations. The three faults in Figure 24 show rising delay and falling voltage values for i ranging from 1 to n.

Figure 25 depicts the all high input category, which has only one delay fault type and it becomes evident that all four faults are feasible for all high input vectors, since they fall into the same delay category. Moreover, Figure 26 exemplifies that voltage and delay vary inversely with respect to the defect resistance. With rising defect resistance, voltage diminishes and delay amplifies. Figure 25 has the delay values highlighted in logarithmic scale. Resistive short at D_n

or ***O*** having defect resistance of 1 KΩ behave more like a hard short, in terms of V_{OUT} value. And in some cases like $I_1I_2I_3$ = 100 and $I_1I_2I_3$ = 000, the V_{OUT} value exceeds the operating voltage mark due to the exclusion of fan-out and interconnect capacitances.

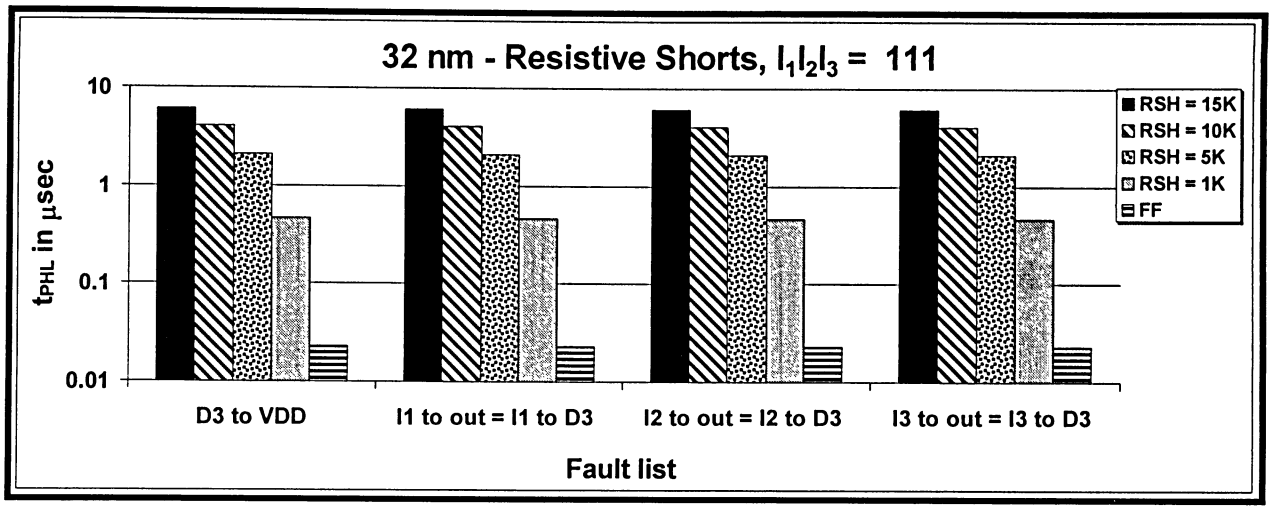


Figure 25 32 nm – t_{PHL} for Resistive Shorts, $I_1I_2I_3$ = 111

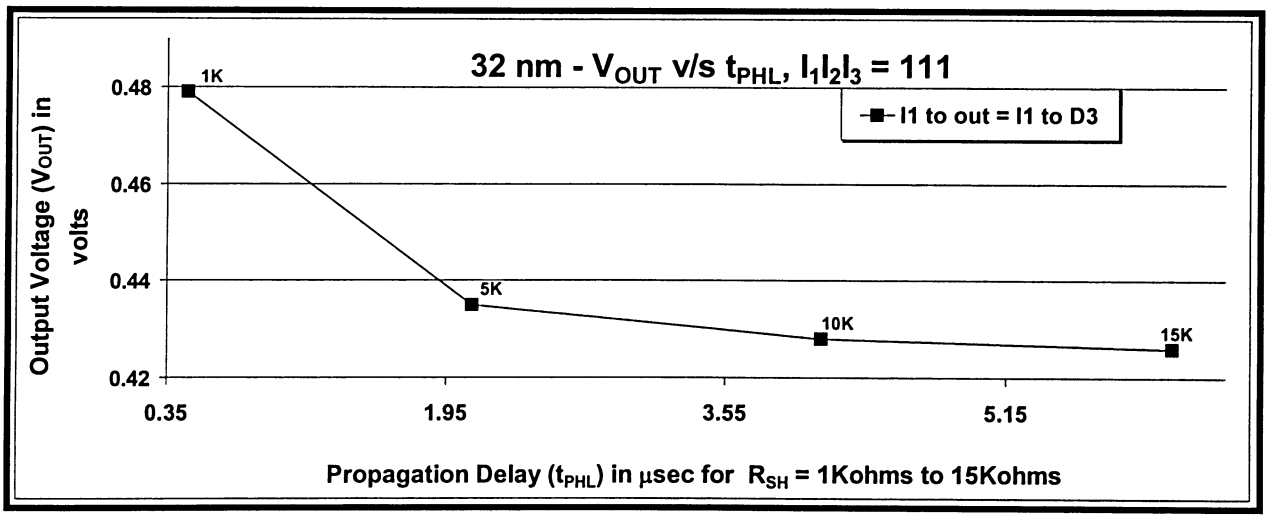


Figure 26 32nm - Output Voltage vs. Propagation Delay; Resistive Shorts for $I_1I_2I_3$ = 111

7.4 Excess Delay (Δt) : Resistive Opens

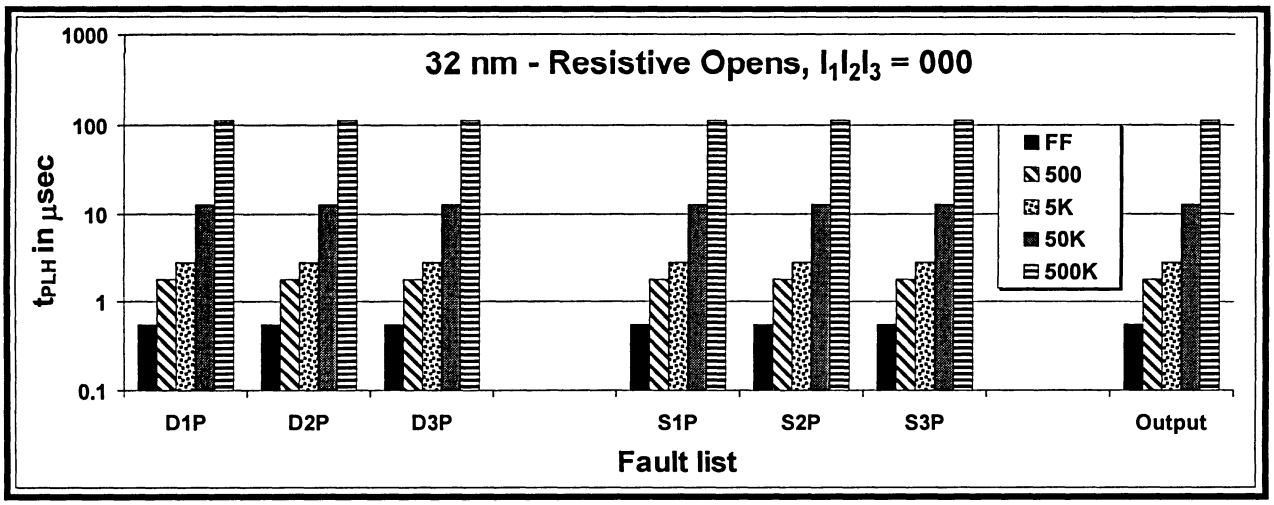


Figure 27 32 nm – t_{PLH} for Resistive Opens, $I_1I_2I_3$ = 000

The fault list for resistive opens, as explained in Section 4.1.1 can further be scrutinized based on the delay produced due to each type of fault and its different fault locations. A 3-input NOR gate in 32 nm technology is subjected to an input vector $I_1I_2I_3$ = 000. The defect resistance range applied for resistive open faults consists of FF, 500Ω, 5 KΩ, 50 KΩ and 500 KΩ. Above 500 KΩ, the defect resistance is assumed static in nature or behaves as a strong open. FF is meant to provide a reference to the faulty delay values with the nominal delay of a (static or dynamic) fault-free circuit. As mentioned before, it is used as a reference value for showing a positive or negative delay difference (Δt). Resistive opens at drain, source and output nodes are evaluated assuming the same example of a 3-input NOR gate. Due to vast delay differences caused by resistive open faults, the delay pattern is emphasized with logarithmic scales fro Figure 27 and Figure 28 respectively.

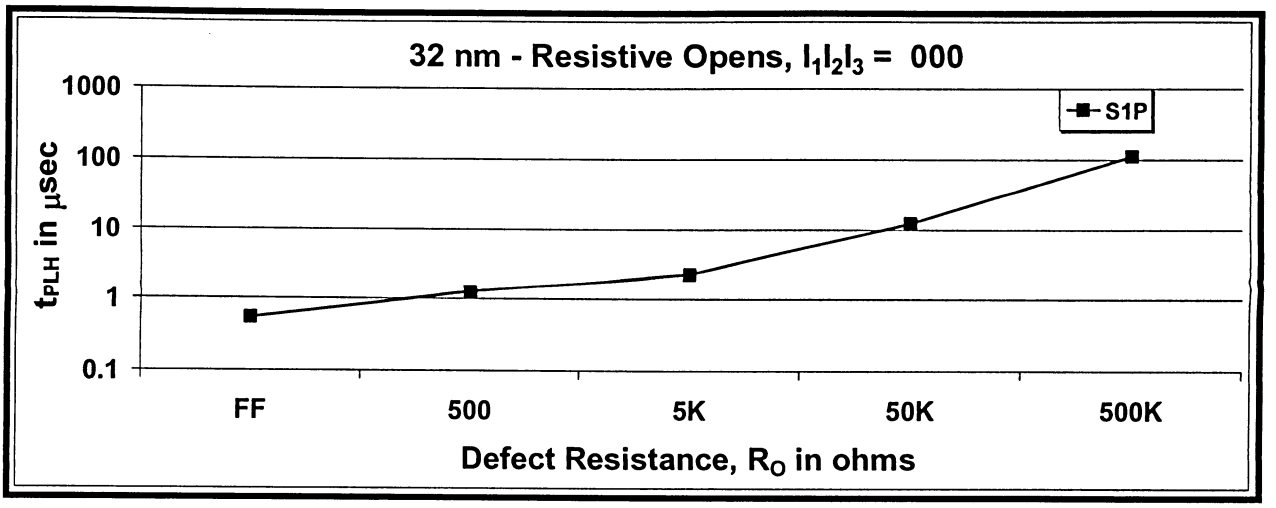


Figure 28 Δt for 32nm-Resistive Opens; $I_1I_2I_3 = 000$

Figure 27 presents the output delay changes due to different defect resistance values for the input combination, $I_1I_2I_3 = 000$ $\forall$ $i = 1$ to n for a 32 nm CMOS NOR Gate. As observed from Figure 27, the electrical analysis of resistive open faults based on the static fault list results in equal delay variations for all the probable fault sites referred to in section 4.1.1. However, taking into account the range of defect resistance, it is noticeable that the resistive effect produces substantial delays at the output. Above and beyond the value R_O = 500KΩ, a large delay (112 µsec) resembling a logic failure appears.

Figure 28 demonstrates that all faults for input vector, $I_1I_2I_3 = 000$ fall in the same delay slot and hence only the resistive open at S_{1P} is measured. The logarithmic scale on the Y-axis of the graph shows a rising pattern among all five defective resistance cases applied to open at S_{1P}.

7.5 Propagation Delay vs. Output Voltage : Resistive Opens

Output voltage versus propagation delay value, for two main kinds of input combinations is provided in this section. All comparisons have propagation delay value in μsec on the X-axis and output voltage value in volts on the Y-axis. Each fault has one trend line, and is made of four points each labelled with the corresponding R_O data. Due to vast delay differences caused by resistive open faults, the propagation delay vs. output voltage pattern is emphasized with logarithmic scale for Figure 30.

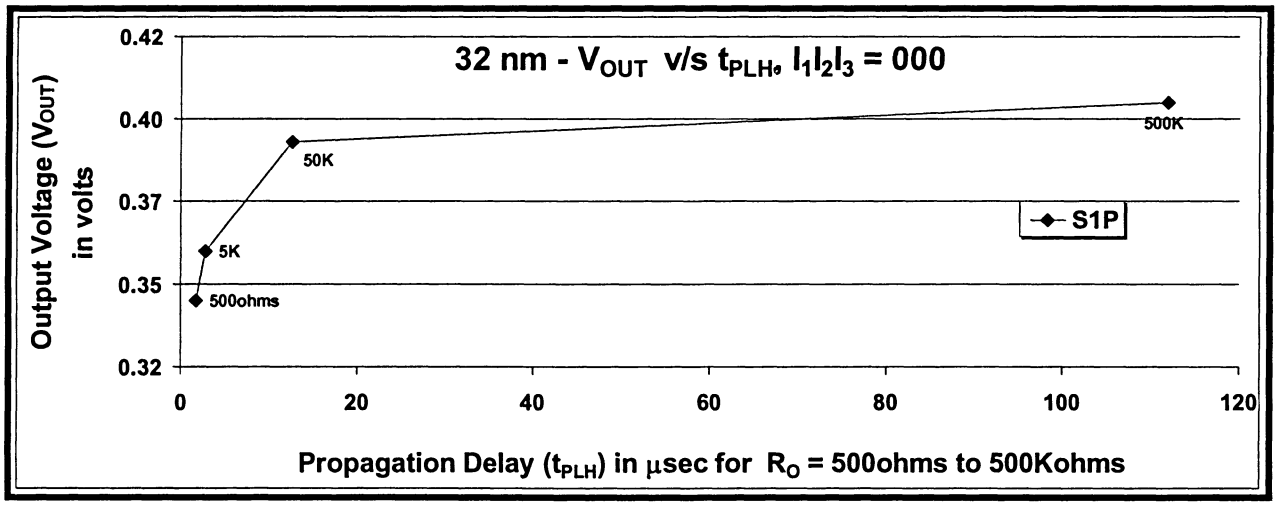


Figure 29 32nm - Output Voltage vs. Propagation Delay; Resistive Opens for $I_1I_2I_3 = 000$

Figure 29 Referring back to Figure 27 all probable faults for the $I_1I_2I_3 = 000$ category are reviewed, which all fall in the same delay slot for resistive open at S_{1P}. The delay is seen rising

with growing defect resistance. And reviewing Figure 29, it is evident that the voltage is also directly proportional to the defect resistance, R_O and the delay. But the output voltage does not change as drastically as the propagation delay value.

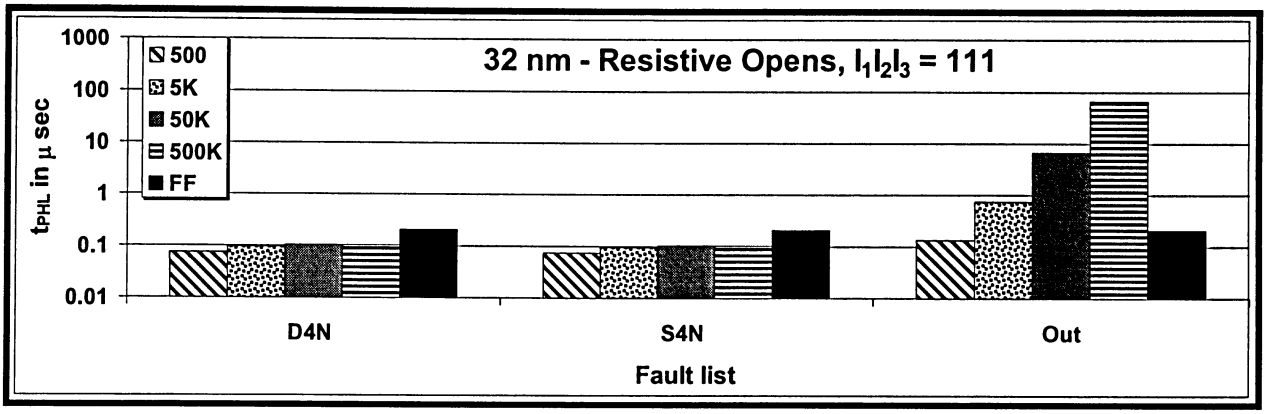


Figure 30 32 nm – t_{PHL} for Resistive Opens, $I_1I_2I_3$ = 111

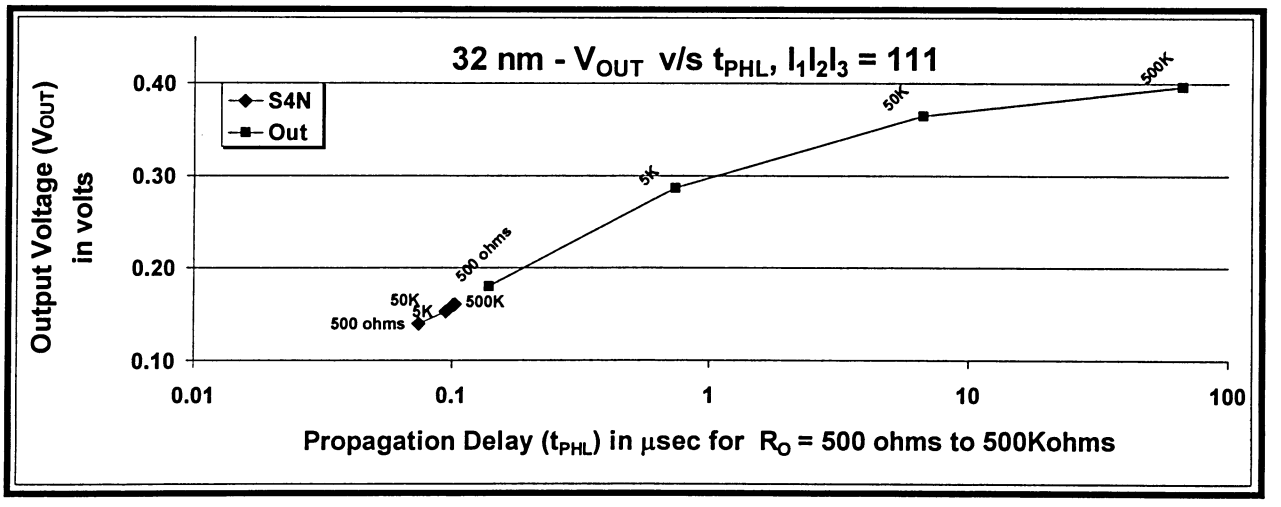


Figure 31 32nm - Output Voltage vs. Propagation Delay; Resistive Opens for $I_1I_2I_3$ = 111

As seen in Figure 30 three faults are possible in a NOR gate for all high input vectors. Of these, resistive opens at D_{4N} and S_{4N}, respectively have similar delay limits. The open fault at the gate output causes enormous delays (67 μsec) for a defect resistance of 500 KΩ, which is ultimately a logic fault. Figure 31 shows the comparative study of propagation delay versus output voltage for variable defect resistance. For delay values below 0.1 μsec, the output voltage may not prove disastrous in terms changing the functional output of the system but definitely it will affect the timing of the circuit. But as the delay reaches beyond 1 μsec, the output voltage might result in logical errors.

CHAPTER 8

CONCLUSION AND FUTURE WORK

8.1 Conclusion

This research provides some convincing results to support the prediction of an expected rise dynamic nature of the soft defects (which cause failures only under specific conditions of voltage, timing and temperature) with narrowing technology sizes [24]. Switch-level single resistive fault modeling is applied on primitive gates; propagation delay and relative output voltage is estimated for various CMOS technologies. Propagation delay at gate output determined for variable circuit parameters like defect resistance, input vectors, defect location, MOSFET resistance and MOSFET capacitance. Prediction of an expected rise in timing failures in VLSI chips with narrowing technology sizes is confirmed from experimental results. Fault simulation and fault emulation of resistive physical failure was not possible due to inability to implement the DSM technologies (45nm and 32nm) in hardware.

Graphical representation of the delay fault pattern and output voltage results for resistive shorts and opens describes the effect of variable defect resistance on physical faults in deep-submicron assemblies. The delay occurring at the output becomes the deciding factor for the dynamic nature of the physical faults considered. The characterization of the delay to voltage fault pattern is applicable for further research studies to investigate the areas of delay fault testing, detection and simulation. Resistive fault behaviour can be explored in greater depth in view of the inconsistent environmental conditions [13].

8.2 Future Work

Derivation of output voltage values sets up a platform for propagating the logic from a gate output to the circuit output. The switch-level fault modeling approach for DSM technology proposed in through this research can be useful for propagating resistive short and open faults to the circuit output by applying path delay fault propagation algorithms [2]. The detect ability of the resistive spot defects can be improved through fault injection at a variable operating voltage value as proposed with MINVDD in [17], with consideration given to the observations made in [8] regarding VLV testing [33] for resistive shorts. Characterization of the delay to voltage fault pattern is applicable for further research of delay fault propagation to circuit output. Output voltage estimated in this research can be categorised into logic voltage levels and the logic voltage along with delay information provided through this approach can be useful at gate-level for applying conventional delay fault detection algorithms.

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1. Reza Sedaghat, Mayuri Kunchwar, Raha Abedi, Reza Javaheri, "*Transistor-level to Gate-level Comprehensive Fault Synthesis for n Input Primitive Gates*" International Journal of Microelectronics Reliability, Science Direct, Elsevier, Volume 46, Issue 12, December 2006, Pages 2149-2158

2. Mayuri Kunchwar, Reza Sedaghat, "*Dynamic Behaviour of Resistive Faults in Nanometre Technology*" 1st Revision, International Journal of Microelectronics Reliability, Science Direct, Elsevier, 2006

3. M. Reza Javaheri, Reza Sedaghat, Mayuri Kunchwar, "*Delay Propagation for Resistive Faults in Deep Sub-Micron Technologies*" International Journal of Microelectronics Reliability, Science Direct, Elsevier, submitted, 2006

4. Mayuri Kunchwar, Reza Sedaghat, "*Dynamic effect of Resistive Faults on Propagation Delay and Output Voltage in Nanometre Technology*", submitted to ASPDAC conference

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