UTILIZATION OF DIFFERENTIAL PULSE POSITION MODULATION IN DESIGNING TIME-MODE SERIAL DATA LINKS

by

Taha Mehrabi Shahsavari,

Bachelor of Engineering, Ryerson, 2012

A thesis

presented to Ryerson University

in partial fulfillment of the requirements for the degree of Master of Applied Science in the Program of Electrical and Computer Engineering

Toronto, Ontario, Canada, 2014

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Utilization Of Differential Pulse Position Modulation In Designing Time-Mode Serial Data Links

Master of Applied Science 2014

Taha Mehrabi Shahsavari

Electrical and Computer Engineering

Ryerson University

A new differential time-based architecture for use in serial communication data links is presented in this thesis, the main idea of which involves transmitting the difference between the input clock signal and the data signal to the receiver. A time to digital converter (TDC) is then used to demodulate the data from the differential pulse position modulated signal.

The proposed design substantiates an improvement in the bandwidth and simplifies the circuit complexity of the currently used serializer de-serializers (SerDes). Additionally, a feature of testability that covers different stuck-at faults was proposed to be implemented in the transmitter side of the proposed architecture. The complete proposed design was tested in TSMC 65 nm CMOS technology; it achieved a data rate of 10 Gbps running at the input clock frequency of 1.25 GHz. Moreover, a complete study of different components of a time mode transceiver architecture was performed during which different design implementation of TDC and phase locked loop (PLL) were thoroughly investigated. Last but not the least, different factors that are mainly imposed by the communication channel that affect the signal integrity were studied, and various methods both from a signal and a circuit point of view were investigated.

ACKNOWLEDGEMENTS

The completion of this thesis would not have been possible without the consistent help and support of my supervisor, Dr. Kaamran Raahemifar who gave me the opportunity to serve as a research assistant under his supervision in the department of Electrical and Computer Engineering at Ryerson University. His belief in me throughout the difficult times of my research and my graduate studies is what still keeps me motivated to this day.

I would also like to thank Dr. Fei Yuan for teaching me the basics of CMOS circuits during my undergraduate program at Ryerson University. His passion for CMOS and electronic circuits and its applications in Wireless and Wire-line communication systems greatly inspired me in choosing transistor level circuits as my main field of research.

I also wish to thank all the members of Ryerson Microsystems research group for their constructive guidance and suggestions as well as their consistent encouragement. Moreover, I would like to thank the lab technicians Mr. Jim Koch and Jason Naughton for their technical support.

Last but not the least, I thank my parents for everything I have today. They made me who I am today and sacrificed many of their own dreams so that my dreams could become reality. They provided every tool that I needed to succeed, and their constant encouragement made the completion of this degree possible.

Dedicated to my parents.

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Glossary

AC	Alternating current
ADC	Analog to Digital Converter
AWGN	Additive White Gaussian Noise
BBPD	Bang Bang Phase Detector
BER	Bit Error Rate
BIST	Built In Self Test
BPF	Band Pass Filter
BW	Bandwidth
CDR	Clock and data recovery
CMOS	Complementary metal oxide semiconductor
dB	Logarithmic Ratio
DC	Direct current
DCO	Digital Controlled Oscillator
DFE	Decision Feedback Equalizer
DFF	D Flip Flop
DLL	Delay locked loop
DPLL	Digital phase locked loop
DPPM	Differential pulse position modulation
FPGA	Field-Programmable Gate Array
Gbps	Giga bit per second
ISI	Inter-Symbol Interference
LSB	Least significant bit
LPF	Low Pass Filter
MLSE	Maximum Likelihood Sequence Estimation
MSB	Most significant bit
NMOS	N-channel metal oxide semiconductor
PAM	Pulse amplitude modulation
PCB	Printed Circuit Board
PD	Phase detector
PLL	Phase locked loop
PMOS	P-channel metal oxide semiconductor
PPM	Pulse position modulation
PVT	Process Voltage Temperature
PWM	Pulse width modulation
Rx	Receiver
SerDes	Serializer/De-serializer
SOC	System On Chip
TDC	Time to Digital Converter
TMSP	Time Mode Signal Processing
Tx	Transmitter
VCO	Voltage Controlled Oscillator
Z	Impedance

Chapter 1: Introduction

At the present time serial links are the essential components in almost every electronic system. Serial links, in contrast to parallel links, are utilized in serial data communication where data is transmitted sequentially one bit at a time via a communication channel. Serial link applications are mostly observed in off chip high-speed servers, communication networks systems, serial ports (USB, Ethernet, FireWire), and data transfer between line cards through traces or cables (such as in backplane applications and system-on-chip [SOC] device communications via interconnects and metal layers). Serial links gradually became popular over the years as the high cost of cable and difficulties associated with parallel data links were making this type of communication a less viable option. Serial communications have been strongly favored over parallel communications, specifically in chip-to-chip communication, since the newer serial technologies are of high speed. Serial links have become a trustworthy alternative since they combat the common issues associated with parallel links, such as clock skew, cross talks and interconnect density. Nevertheless, the parallel link's lack of need for serializer and de-serializer (SerDes) do make it a simpler design [1-5].

The demand for multi-Gbps data communication has continually expanded the requirements for designing serial links. CMOS technology scaling, on the other hand, has not been accommodating, and it has enforced more limitations on such designs. As the CMOS technology scales down, the resultant smaller voltage headroom makes it more difficult to drive high frequency signals off-chip. Moreover, due to the increasing demand for rise of data rates to multi Gbps for both off-chip and on-chip communication, the data signal has been extensively

affected by the BW limitations. At such high data rates, combating issues such as data skew, cross talk and ISI becomes much more challenging than ever before.

Typically, as shown in Figure 1.1, to perform a serial communication specifically for chip-to-chip communication, a SerDes is used where data is multiplexed at the transmitter side and de-multiplexed at the receiver side. In order to serialize the incoming data, the transmitter entails a parallel-to-serial circuit and a phase-locked loop (PLL). The PLL is required to generate an accurate clock frequency signal in order to "line-up" the serialized bits. A driver circuit is then used to transmit the now-serialized data through the channel. On the receiver end, the reverse operation takes place. The serialized data are first passed through a signal revival stage circuit that is commonly called an equalization circuit. The signal is then split, with one line going to the serial-to-parallel circuit and the other going to the clock and data recovery (CDR) circuit. The CDR is used to recover the clock signal that will then be used to align the data signal with the generated clock signal in order to begin the data recovery process.

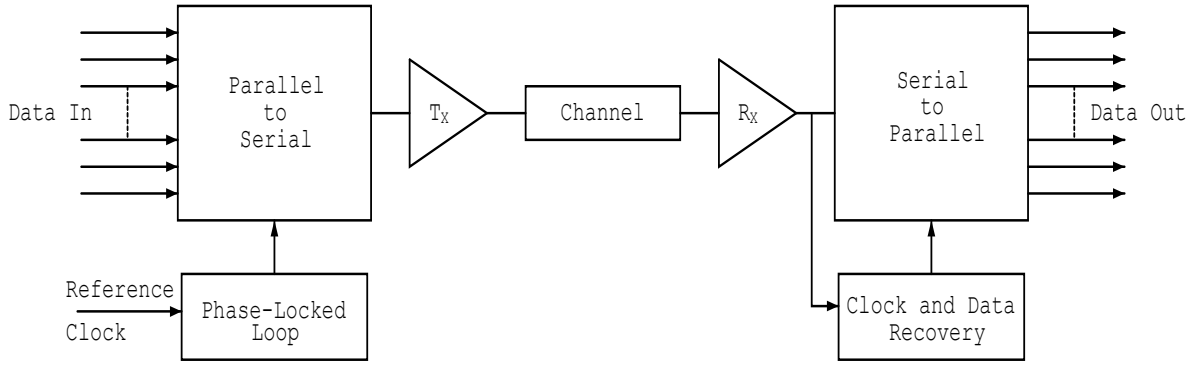

Figure 1.1 - Generic diagram of a serial link [6].

The transmitter circuit is in charge of serializing the parallel input data into a single bit-stream signal. Various methods to serialize the input bits exist that will be discussed here.

1.1. PAM Transmitters

In PAM transmitters, the following is transmitted: a sequence of continuous-time pulses of some pre-specified shape, with the sequence of pulse amplitudes carrying the information. The amplitude of the input clock signal is modulated according to the input bit combination. For instance, an 8-PAM serial link transmits 3 bits, because 3 bits give a combination of 8 cases, shown in Figure 1.2.

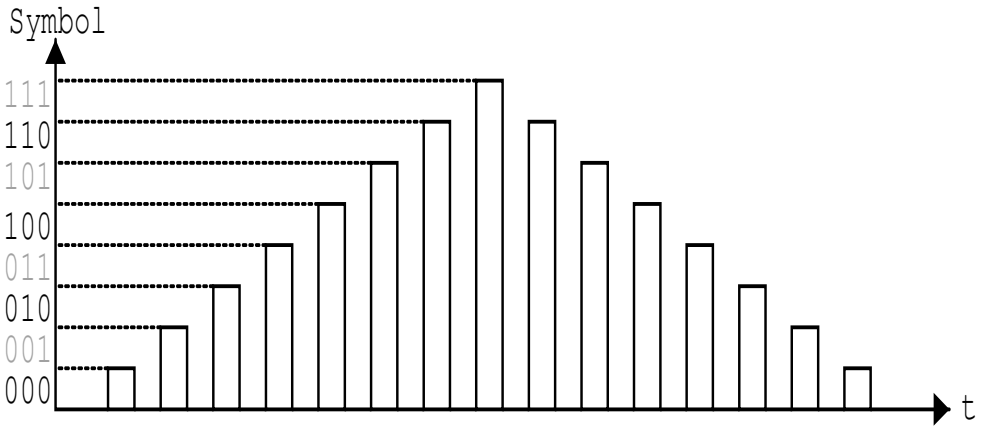

Figure 1.2 - Pulse Amplitude Modulation (PAM) [6].

Due to scaling of CMOS technology, the supply voltage and, consequently, the circuits' voltage head room have been vastly reduced. Therefore, multi-level PAM topologies now have a poor voltage resolution and do not provide enough flexibility for more bits to be added to the link. Thus, they are unappealing for high speed applications. However, the main benefit of this architecture is its requirement for the input clock frequency to equal to the input bit rate. This constraint provides a more relaxed circuit requirement at the transmitter end such that frequency synthesis is not required.

1.2. PWM Transmitters

Pulse width modulating transmitters require that the frequency and amplitude of a clock signal be kept constant, while the width is varied according to the input data bits. Three types of PWM schemes are possible: (a) the pulse center may be fixed while rising and falling edges may be moved to vary width, (b) the leading edge may be fixed and the tail edge modulated, and (c) the tail edge is fixed while the leading edge is modulated. Most CMOS communication circuits follow scheme (b), as the rising (leading) edge is quicker to detect and delay lines; or other techniques may be used to modulate the width. Unlike PAM, pulse width modulation does not have the problem of voltage resolution, so a clock signal need not be embedded with the signal because the leading edge of each data pulse specifies the clock. It does, however, suffer from poor resolution in the horizontal (time) plane rather than the vertical. Because serial links are required to operate at high frequencies, the period of the clock is therefore decreased as the frequency increases; therefore, the pulse width now has a very limited range, as shown in Figure 1.3. High-speed CMOS circuitry is therefore required with both very high sensitivity and high resolution.

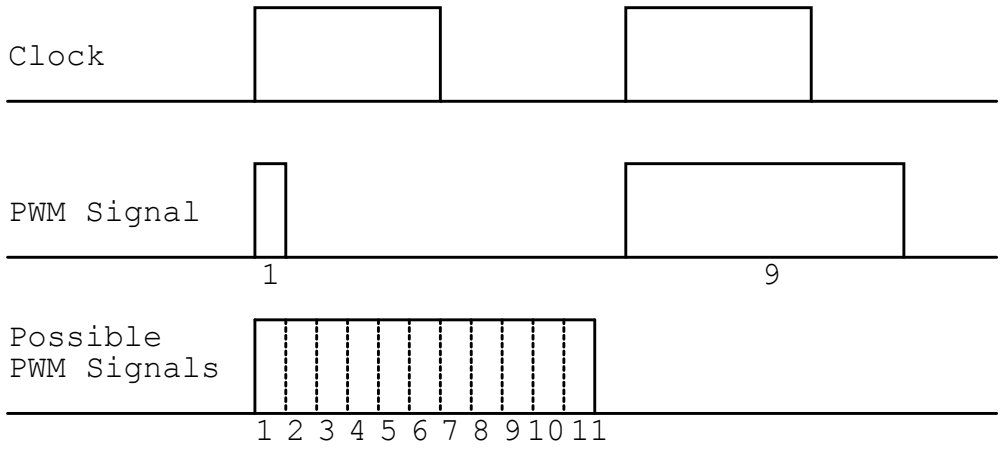

Figure 1.3 - Pulse Width Modulation (PWM) [6].

1.3. PPM Transmitters

Pulse position modulation has been used primarily in optical communication systems, where little or no multipath interference tends to exist. The basic premise of PPM requires that the circuit modulate the rising edge of a clock pulse in time according to the input data while keeping the amplitude and pulse width constant. Therefore, the position of each pulse, in relation to the position of the clock pulse, is varied by each data bit of the incoming signal, as shown in Figure 1.4.

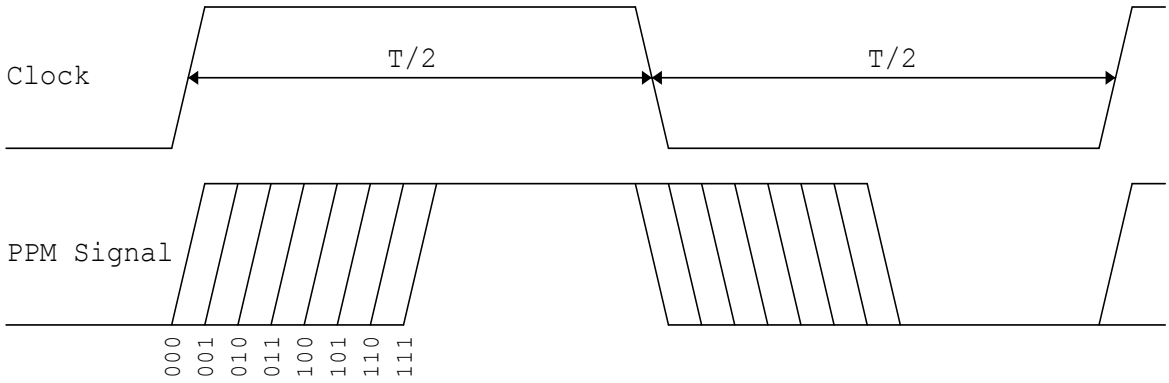

Figure 1.4 - Pulse Position Modulation (PPM) [6].

The table below summarizes the different parameters of the abovementioned data encoding types.

Table 1.1 - Comparison of PAM, PWM and PPM data encoding [7].

Parameter	PAM	PWM	PPM
Variation parameter	Amplitude	Width	Position
BW requirement	Less	High	High
Noise immunity	Low	High	High
Transmitted Power	Varies with amplitude	Varies with width	Constant
Need for pulse synchronization	No	No	Yes
Complexity	Less	More	More

1.4. Thesis Objectives and Contributions

Given the enforced limitations of CMOS technology scaling on the PAM and PWM, the main focus of this thesis will be on a time-mode design approach of a multi-Gbps SerDes through PPM and DPPM. As a result, the main objective is to utilize a different type of data encoding, namely, DPPM in designing a serial data link to better combat the BW limitations imposed by the communication channel and to further improve the circuit complexity introduced by other typical data encoding types. In achieving this objective throughout the work, a new time mode SerDes architecture that uses differential pulse position modulation technique has been proposed. Moreover, a testability feature was proposed to make this architecture a more trustworthy alternative compared to other schemes.

1.5. Thesis Layout

Chapter 2

In Chapter 2, different implementations of SerDes along with the factors affecting the signal integrity will be investigated. These factors justify the use of signal revival stages, such as pre-emphasis and equalization circuits, which will be discussed thoroughly in this chapter.

Chapter 3

This chapter will be thoroughly dedicated to time-mode SerDes and its two main components, namely, PPM module at the transmitter side and TDC module at the receiver end. Moreover, time-mode architecture's advantages, disadvantages, and common challenges will be discussed in this chapter.

Chapter 4

Chapters 4 and 5 will cover the main contributions of this work. More specifically, in Chapter 4 a new 4-bit programmable delay will be introduced to replace the conventional PPM module discussed in Chapter 3. Additionally, a new feature of testability will be submitted and investigated using the proposed circuit.

Chapter 5

In this chapter, a new DPPM-based time-mode SerDes will be proposed; an explanation will be provided regarding the way in which this proposed technique will combat certain issues associated with PPM-based SerDes (as mentioned in Chapter 3).

Chapter 6

This chapter will focus mainly on the results and observations of the proposed designs (as mentioned in Chapters 4 and 5).

Chapter 7

This chapter will present the conclusions, final thoughts and future works. Finally, the reference section will cover all the sources used in this endeavor.

Chapter 2: Different Design Implementations of SerDes

As mentioned earlier, serial links are important components in high-speed communications for both off-chip and on-chip applications. They are used in on-chip applications to reduce the number of pins used in different ICs than conventional parallel links use. Moreover, they are used in off-chip applications for high speed data transfer between line cards through cables or traces in backplane applications.

2.1. Transmitter (Tx)

The most commonly used architecture of a SerDes, as shown in Figure 2.1, is the multiplexer-based SerDes.

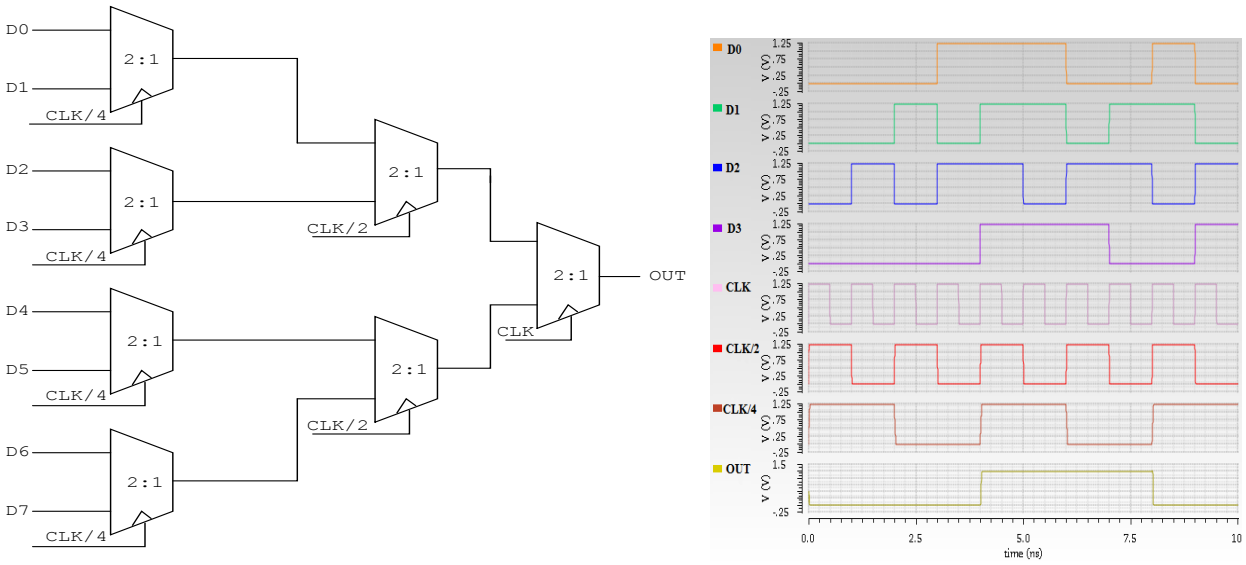

Figure 2.1 - Multi-stage multiplexing transmitter of an 8-bit conventional SerDes [8] along with its first 4 bits transient response.

In this architecture, the parallel data gets multiplexed via an array of multiplexers with a divide-by-2^N clock pulse at the transmitter side, is passed through the channel and finally de-multiplexed at the receiver side to retrieve the transmitted parallel bits. In order to achieve a relatively high data rate using this design, high-speed multiplexers need to be designed, which also have very high input clock frequency. Such architecture can be extensively observed in memory and mobile display interface applications.

In Chapter 1, it was explained how PAM and PWM modulations schemes could be used when designing the transmitter side of a SerDes. However, the challenges that designers encounter when envisioning a PAM-based transmitter are extremely difficult to cope with; that is, as the CMOS technology scales down, the voltage supply decreases and, consequently, circuits' voltage headroom decreases significantly. As a result, the designers must settle for 2-PAM modulation scheme rather than 4-PAM; in other words, it means settling for a lower data rate. Additionally, the PWM modulation scheme suffers from poor resolution in horizontal plane (time). Thus, as the data rate increases the pulses need to be narrower. Considering the signal degradation imposed by the channel, the proper demodulation process will be extremely difficult for the receiver. In another approach, as seen in [9-10], the authors have achieve a higher data rate by combining the two modulation schemes, namely, PAM and PWM. Such hybrid design implementation allows 4 bits to be transmitted, of which 2 bits are modulated using PAM and 2 bits are modulated using PWM.

2.2. Pre-emphasis Circuit

At the transmitter side, the serialized signal is passed through a simple network that increases the gain of the high frequency components or attenuates the low frequency components

to compensate for the high frequency attenuation caused by the channel, as shown in Figure 2.2. The main advantage of this circuit is that it does not amplify the noise.

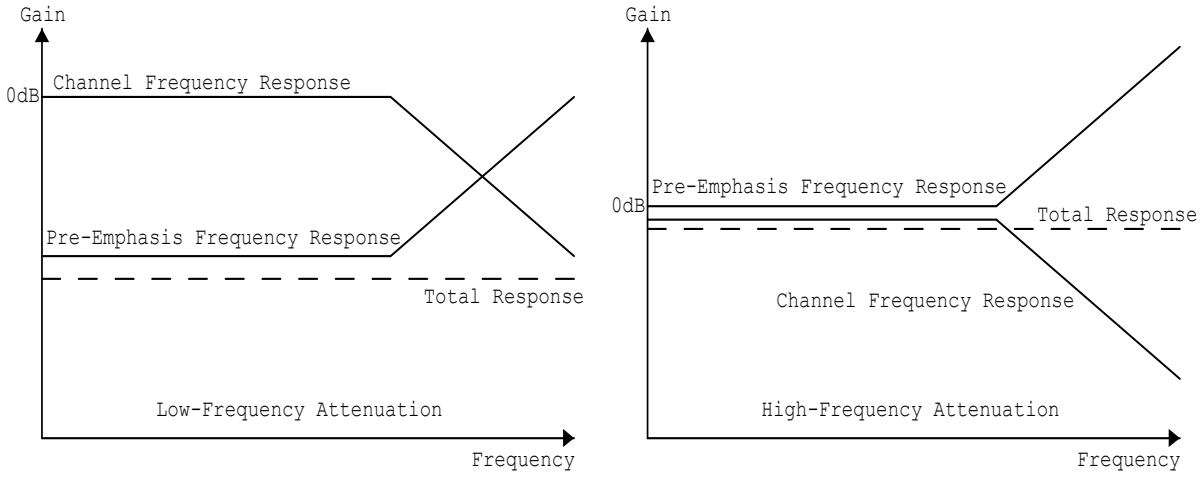

Figure 2.2 - Transfer function of pre-emphasis circuit [6].

The first stage of the pre-emphasis circuit is the main differential driver, whereas the following stages are the taps. The input to the driver stage is the serialized transmitted signal. The input to the first tap is the same signal but delayed by T. Similarly, the input to the second tap is the transmitted signal delayed by 2T. The timing diagram of the 2-tap pre-emphasis circuit is shown in Figure 2.3, where V_2 is the peak-to-peak voltage and V_1 is the static voltage.

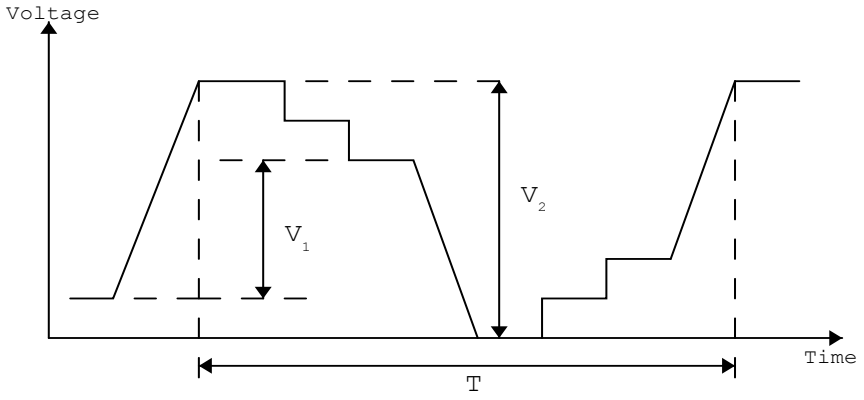

Figure 2.3 - Pre-emphasis timing diagram [11].

When using pre-emphasis circuits, due to the low frequency components being attenuated, smaller received signal amplitude is obtained following the pre-emphasis; however, a reduced inter-symbol interference (ISI) is achieved in this way. If long channels are used, pre-emphasis may not be enough. The use of an equalization circuit is then recommended. It should be noted that many serial links have been designed using pre-emphasis circuits at the transmitter side in order to achieve a successful recovery at the receiver end.

2.3. Channel

A channel is a transmission medium that is used to transfer the data signal from one point to another. Limitations caused by the channel are the main challenge imposed on high-speed data links. Issues such as attenuation and reflection are only some of the challenges that need to be tackled when designing SerDes. Moreover, a channel has a certain transmission capacity, namely, a bandwidth that limits high speed data rates. As the length of the channel increases, attenuation of the signal will more difficult to cope with. Figure 2.4 shows the eye diagram of a signal for a 25Gbps serial link with and without pre-emphasis, as investigated in [12].

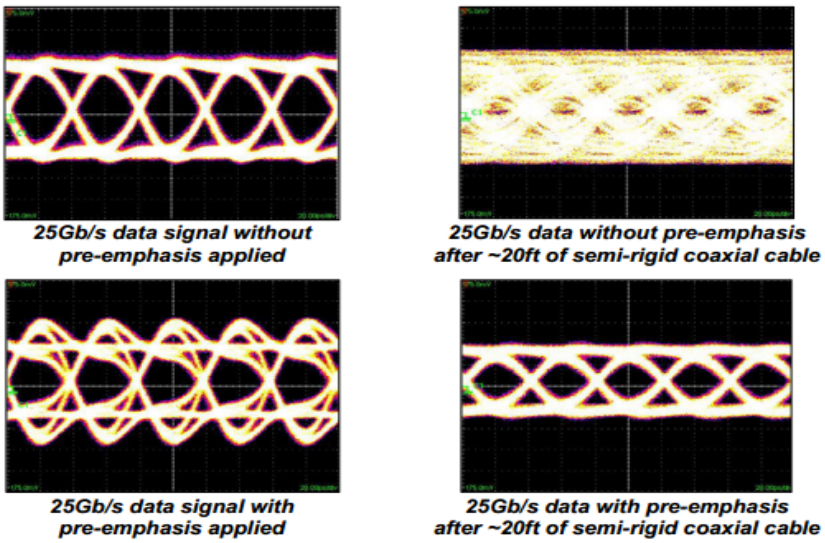

Figure 2.4 - Eye diagram of a 25Gbps signal with and without pre-emphasis [12].

FR-4 is a typical and most cost effective channel that is mainly used in commercial data communications and PCB fabrication. According to the attenuation response of 40-inch FR-4 PCB trace, the increase in frequency is aligned with an increase in transmitted signal attenuation. As a result, the signal SNR will decrease and seriously affect the BER of the serial links.

Table 2.1 - Parameter specifications of a 40-inch FR-4 PCB trace [13-15].

Parameter	Value
Specific gravity/density	1,850 kg/m^3 (3,120 lb/cu yd)
Water absorption	−0.125 in < 0.10%
Temperature index	140 °C (284 °F)
Thermal conductivity, through-plane	0.29 W/m·K, 0.343 W/m·K
Thermal conductivity, in-plane	0.81 W/m·K, 1.059 W/m·K
Rockwell hardness	110 M scale
Bond strength	> 1,000 kg (2,200 lb)
Flexural strength (A; 0.125 in) - LW	> 440 MPa (64,000 psi)
Flexural strength (A; 0.125 in) - CW	> 345 MPa (50,000 psi)
Tensile strength (0.125 in) LW	> 310 MPa (45,000 psi)
Izod impact strength - LW	> 54 J/m (10 ft·lb/in)
Izod impact strength - CW	> 44 J/m (8 ft·lb/in)
Compressive strength - flatwise	> 415 MPa (60,200 psi)
Dielectric breakdown (A)	> 50 kV
Dielectric breakdown (D48/50)	> 50 kV
Dielectric strength	20 MV/m
Relative permittivity (A)	4.8
Relative permittivity (D24/23)	4.8
Dissipation factor (A)	0.017
Dissipation factor (D24/23)	0.018
Dielectric constant permittivity	4.70 max., 4.35 @ 500 MHz, 4.34 @ 1 GHz
Glass transition temperature	Can vary, but is over 120 °C
Young's modulus - LW	3.5×10^6 psi (24 GPa)
Young's modulus - CW	3.0×10^6 psi (21 GPa)
Coefficient of thermal expansion - x-axis	1.4×10^{-5} K^{-1}
Coefficient of thermal expansion - y-axis	1.2×10^{-5} K^{-1}
Coefficient of thermal expansion - z-axis	7.0×10^{-5} K^{-1}
Poisson's ratio - LW	0.136
Poisson's ratio - CW	0.118
LW sound speed	3602m/s
SW sound speed	3369m/s
LW Acoustic impedance	6.64 MRayl

2.3.1. Channel Modeling

2.3.1.1. Continuous-time channel modeling

The transfer function of the channel can be expressed in both the continuous-time and discrete-time descriptions. The continuous-time transfer function is shown using an Nth-order transfer function, which has *N* number of poles and *M* number of zeros as seen in the equation below [6]:

$$H(s) = \frac{A_H(s - Z_1)(s - Z_2) \dots \dots \dots \dots (s - Z_M)}{(s - P_1)(s - P_2) \dots \dots \dots \dots (s - P_N)} \qquad (2.1)$$

2.3.1.2. Discrete-time channel modeling

Using the discrete channel model, the input and output of the signals are represented using discrete samples. The sampling frequency, f_s, must be high enough to avoid aliasing. The finite-impulse-response (FIR) channel model can be obtained using the equation below, where *k* is the sample number and *N* is the number of samples [6]:

$$y(k) = h(k) * u(k) = \sum_{i=0}^{N-1} h(l)u(k - l) \qquad (2.2)$$

2.3.1.3. Transmission line channel modeling

A channel can be modeled as a transmission line, as shown in Figure 2.5, where it is represented by a lumped network that consists of *R* (series resistance per unit length), *L* (self-inductance per unit length), *G* (shunt conductance per unit length) and *C* (shunt capacitance per unit length).

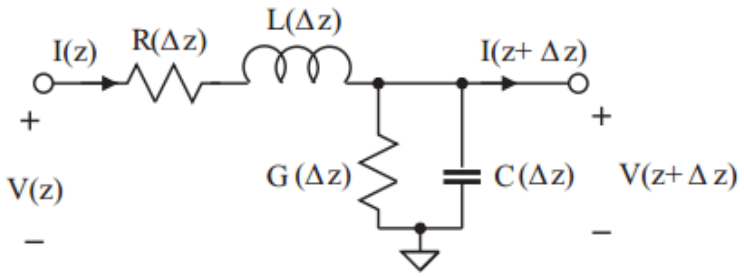

Figure 2.5 - Lumped network model of a section of transmission line [16].

A transmission line has the following equations [16]:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2.3}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{2.4}$$

where $\gamma=\sqrt{(G+j\omega C)+(R+j\omega L)} = \alpha + j\beta$ is the complex propagation constant, α is the attenuation constant which quantifies the attenuation of the voltage or current amplitude, and β is the phase constant that indicates the variation of the voltage or current phase.

The above equations are 2nd-order differential equations that have the following solutions and represent the voltage and the current of the transmission line in the frequency domain [16]:

$$V(z) = V^+e^{-\gamma z} + V^-e^{\gamma z} \tag{2.5}$$

$$I(z) = I^+e^{-\gamma z} + I^-e^{\gamma z} \tag{2.6}$$

Additionally,

$$V^+e^{-\gamma z} = V^+e^{-(\alpha+j\beta)z} = V^+e^{-\alpha z}[\cos(\beta z) - j\sin(\beta z)] \tag{2.7}$$

And,

$$V^{-}e^{\gamma z} = V^{-}e^{(\alpha+j\beta)z} = V^{-}e^{\alpha z}[\cos(\beta z) + j\sin(\beta z)]$$
$$= V^{-}e^{-\alpha(-z)}\{\cos[\beta(-z)] - jsin\left(\beta(-z)\right)]\} \quad (2.8)$$

Where α and β are the attenuation and phase constants, respectively. Also, $V^{+}e^{-\gamma z}$ is the propagation of the voltage in the z-direction, namely, incident wave, and $V^{-}e^{\gamma z}$ is the propagation of the voltage in the -z-direction, namely, reflected wave [16].

2.3.2. Skin effect

A time-varying current has a tendency to concentrate on the surfaces of conductors. When the frequency is very high, the current is practically restricted to the surfaces. This phenomenon of non-uniform distribution of current in conductors is known as the skin effect. This effect causes the signal current to conduct within a limited skin depth on the conductor surface, and it can be calculated using the following equation [17]:

$$\delta = \frac{1}{\sqrt{\frac{\pi\mu}{\rho}.f}} \quad (2.9)$$

Where ρ is the resistivity of the conductor, *f* is the frequency of the signal and μ is the permeability constant. Additionally, the effective series resistance of the cable corresponding to the skin depth increases with the square root of the frequency for a round conductor with radius *r,* as shown in the equation below [17]. At very high frequencies, the skin effect is so pronounced that as series resistance increases, the current encounters greater loss.

$$R_{skin} = \frac{\sqrt{\frac{\rho\mu}{\pi}.f}}{2r} \quad (2.10)$$

Table 2.2 - Skin depth of some materials for different frequencies [17].

Material	f **= 60 Hz**	f **= 1 KHz**	f **= 1 MHz**	f **= 1 GHz**
Copper	8.61 mm	2.1 mm	0.067 mm	2.11 μm
Iron	0.65 mm	0.16 mm	5.03 μm	0.016 μm
Sea Water	32.5 m	7.96 m	0.25 m	7.96 mm
Wet Soil	650 m	159 m	5.03 m	0.16 m

2.3.3. Dielectric loss

Dielectric loss is a quantity that expresses the dissipated electromagnetic energy of the dielectric material surrounding a transmission line. This loss increases proportionally to the frequency, according to the following equation [6]:

$$\alpha_D = \pi \frac{\sqrt{\varepsilon_r}}{c} . f . \tan(\varphi) \qquad (2.11)$$

Where α_D is the dielectric loss, $\tan(\varphi)$ is the loss tangent, c is the speed of light and ε_r is the relative permittivity.

2.3.4. Inter-Symbol-Interference (ISI)

ISI is a form of signal distortion in which a signal pulse interferes with the consecutive signal pulses. The narrower the signal pulse, the more severely it is affected by the channel. This is an unwanted outcome in which the previous signal pulses have an effect similar to noise. The main causes of the ISI are the filtering effects introduced by hardware and the multipath propagation or the inherent nonlinear frequency response of the channel causing the pulses to interleave together. Moreover, the transmission of a signal through a band-limited channel is another source of ISI. The chief issue that this phenomenon imposes is the difficulty for the

decision device at the receiver to demodulate the transmitted signal correctly. Thus, ISI is one of the most significant factors that limits the data rates in high-speed serial links [18].

Several techniques are used to mitigate the effects of ISI. One of them is applying an equalizer circuit that attempts to undo the effect of the channel by applying an inverse filter. Another option is applying a sequence detector at the receiver, which attempts to decode the sequence of the transmitted bits using *Viterbi* algorithm.

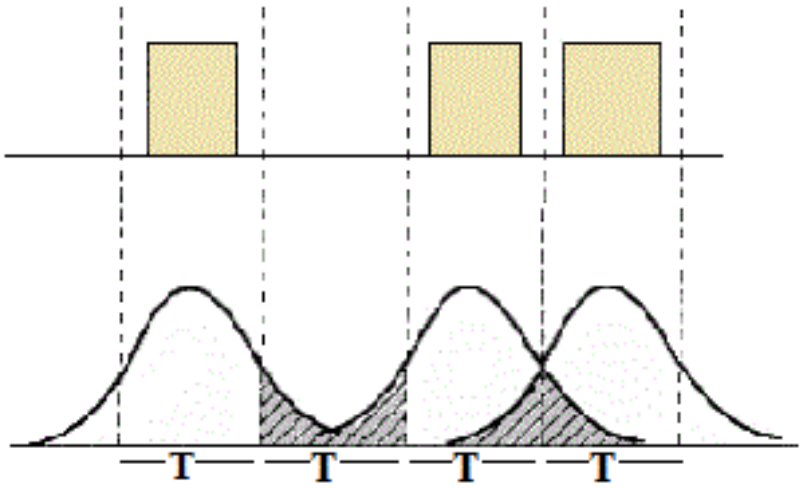

Figure 2.6 - ISI in digital transmission.

2.3.5. Reflections (Impedance Mismatch)

Another phenomenon that degrades the signal integrity is signal reflection that occurs when the signal transitions from one transmission line to another has an impedance mismatch (a difference in impedance). The reflection coefficient, or the ratio of the energy that is bounced back, depends on the impedances of the transmission lines and can be calculated using equation 2.12 [16]:

$$\Gamma = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{2.12}$$

Similarly, the above concept can be extended to a terminated line with a load for which the above equation can be rewritten as follows [16]:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{V^-}{V^+} \tag{2.13}$$

Where V^+ and V^- are the amplitude of the voltage of the incident and reflected waves, respectively.

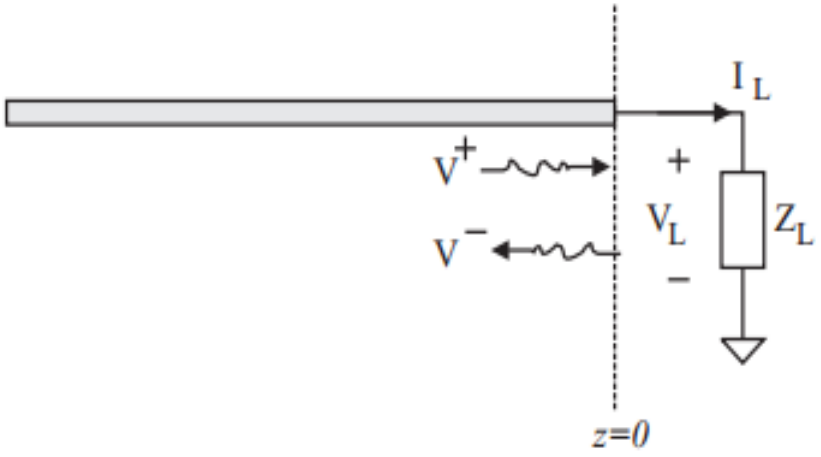

Figure 2.7 - Reflection in a terminated line [16].

2.3.6. Crosstalk

A phenomenon in which a signal is transmitted in one channel affects the integrity of the signal transmitted in another channel is called crosstalk. Crosstalk is much more visible in parallel data links and is caused mainly by the capacitive, inductive or conductive coupling of one circuit or channel to another circuit or channel.

2.3.7. Jitter

Jitter is the undesirable variation of a digital pulse at both its positive and negative edges. It mainly occurs in transmission of data, and its main source is the noise picked up by the PLL. Jitter is typically categorized into deterministic and random jitter. The deterministic jitter is attributed to the ISI introduced by the channel, while the random jitter is an electronic timing noise and typically follows Gaussian or Normal distribution. Moreover, the total jitter--a combination of the above-mentioned jitters--can be calculated using the following equation:

$$Total\ Jitter = D_{p-p\ jitter} + 2.n.R_{rms} \tag{2.14}$$

Where $D_{p-p\ jitter}$ is the peak to peak deterministic jitter, n is based on the bit error rate (BER) and R_{rms} is the rms-value of random jitter.

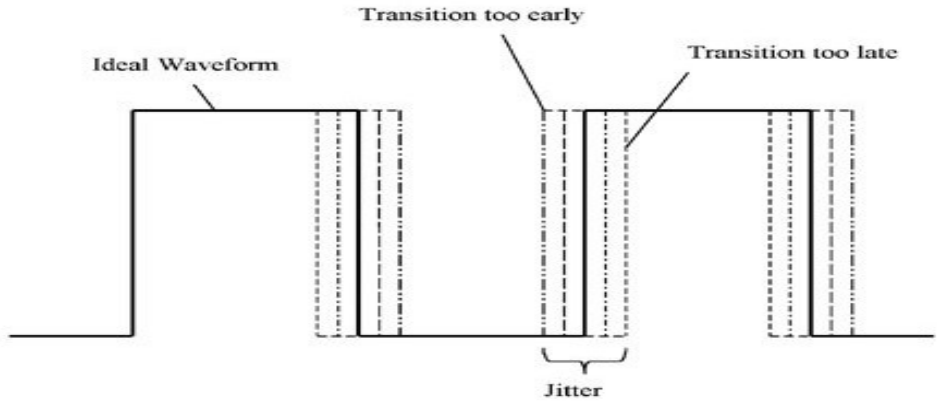

Figure 2.8 - Jitter in a signal [19].

2.4. Receiver (Rx)

The receiver circuit demodulates the transmitted data. More specifically, in a serial link the receiver is in charge of de-serializing the received signal into a number of output bits that represent the parallel input bits. Moreover, the receiver consist of a signal revival stage to

prepare the signal for the decision device so that it can properly demodulate the received signal. Another important block at the receiver side is the CDR circuit that recovers the clock that is not transmitted along with the transmitted data bits and must be generated and aligned with the data signal. There are many CDR architectures, namely, Filter-type CDR in which the clock signal is created using an edge detector followed by a band pass filter (BPF), a PLL-based CDR that can be classified into linear and non-linear architectures. Both these architectures utilize a phase detector (PD) circuit and translate the phase difference into voltage that would control a voltage controlled oscillator (VCO). Variable-interval oversampling CDR architecture that uses a VCO and delay locked loop (DLL) combination to track the data edges and put the sampling strobe in the middle of two data edges., Phase-picking or oversampling CDR architecture, whereby an odd number of samples is acquired per bit and the decision logic uses the sample closest to the eye center to recover the data. And Eye-tracking DR architecture that tracks the data eye instead of the data edges.

2.5. Equalization Circuit

Equalization circuits at the receiver end serve a purpose similar to that of the pre-emphasis on the transmitter end. The circuit is used to compensate for the attenuation caused by the channel and its signal degrading factors on the transmitted data, as mentioned earlier. The main premise of the receiver equalizer is to match the inverse of the channel magnitude response so that the cascade of the transmitter, channel, and receiver front-end yields a flat frequency response [6]. These equalization methods try to convert a band-limited channel with ISI into one that appears memory-less, in hopes of synthesizing a new AWGN-like channel at the receiver output. Equalizers are categorized into linear and non-linear types, as shown in Figure 2.9.

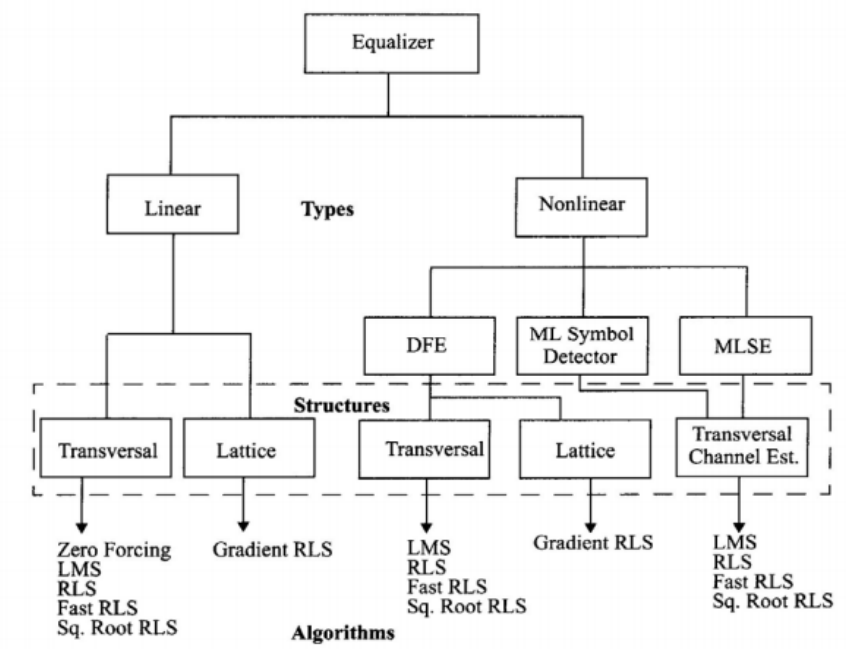

Figure 2.9 - Category of equalizers [20].

2.5.1. Maximum-Likelihood Sequence Estimation (MLSE) Equalizers

This method entails making measurements of channel impulse response and then providing a means for adjusting the receiver to the transmission environment (i.e. Viterbi method). More specifically, MLSE equalizer tests all possible data sequences and chooses the data sequence that has the maximum probability as the output. This technique is used rather than decoding each received symbol by itself [20].

2.5.2. Equalization using filters

Filters are used in this method to compensate the distorted pulses. However, this type of equalizers can be preset, assuming that the channel is time invariant; the *H(f)* of the channel will then be found and the filter will subsequently be designed. Alternatively, they can be adaptive,

which assumes that the channel is time varying and that a filter's coefficients also vary in time according to the change of channel to eliminate ISI.

2.5.3. Linear Transversal Equalizers

Linear equalizers are the most common format made up of tapped delays, as shown in Figure 2.10. Next, Figure 2.11 shows the transistor level circuit of the designed linear equalizer.

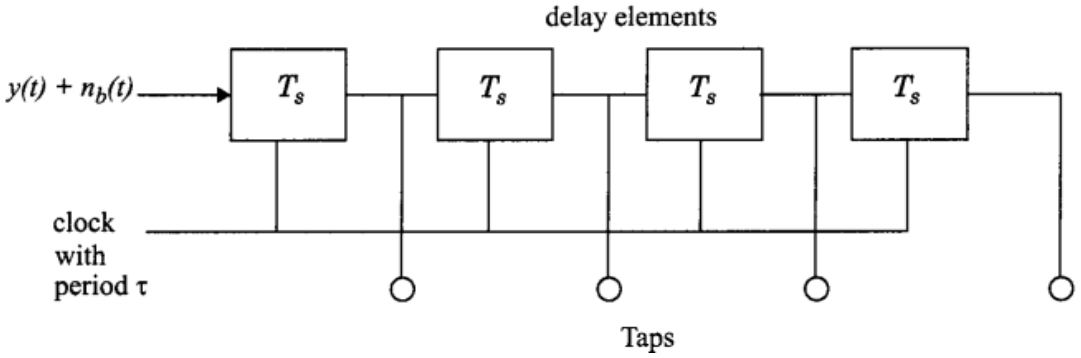

Figure 2.10 - Linear equalizer [20].

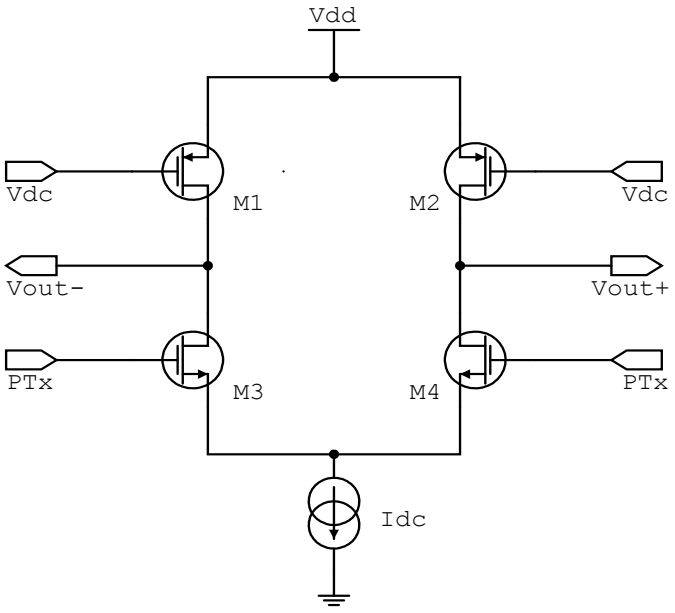

Figure 2.11 - Transistor level linear equalizer.

2.5.4. Decision Feedback Equalizers (DFE)

In this method, the detected signal is first delayed and then fed back to cancel the ISI due to the previously detected symbols. Figures 2.12 and 2.13 show the block diagram and operation of DFE circuit, respectively, where *x(t)* is the receiving signal, y*(t)* is the equalized analog signal, y*(n)* is the binary decision data and *N(t)* is the high frequency noise added to the channel and to the receiver.

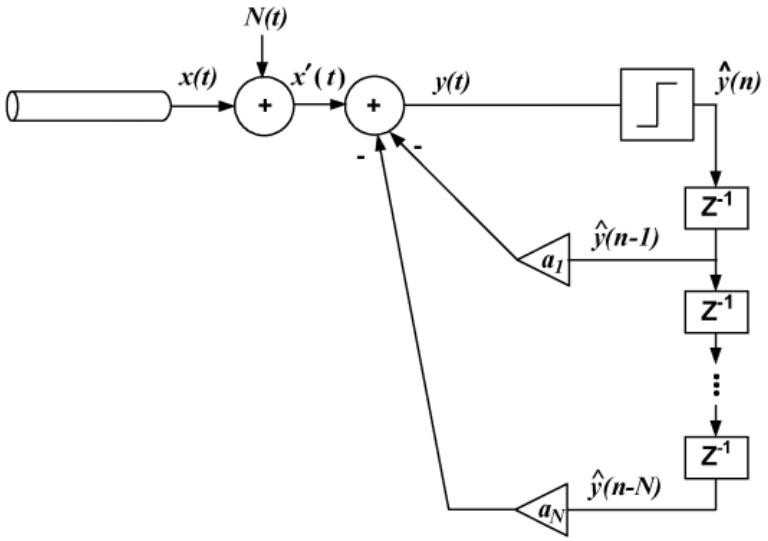

Figure 2.12 - DFE block diagram [21].

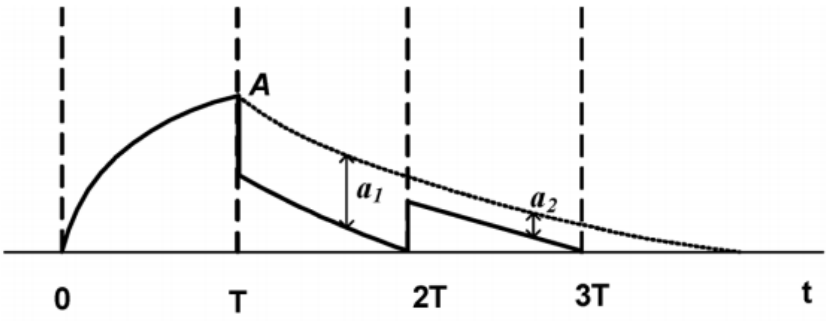

Figure 2.13 - Equalized pulse response of the DFE [21].

2.6. PLL and CDR

An integral part of communications systems, phase-locked loops (PLLs) are useful in clock and data recovery (CDR) circuits for high speed I/O and frequency synthesizers for clock signal generation. They are critical components to any digital or mixed-signal system requiring an accurate clock. In CDR circuits, the PLL can be used to recover a clock signal embedded in a serial data stream, and it optimally captures the data bits using the recovered and re-timed clock. Alternatively, if a clock signal is not embedded within the transmitted data stream, the PLL is able to capture the rising edge of progressive data bits and, through negative feedback, to generate an equivalent clock signal. Other uses of PLLs include jitter reduction, clock distribution and skew suppression.

Working on the basis of dynamic feedback systems, PLLs produce an output clock, φ_{FB}, in response to the frequency and phase of an input (reference) clock, φ_{REF}. Basically, through negative feedback, a PLL tries to maintain a phase difference of zero between the reference clock and the feedback clock. Figure 2.14 shows a typical block diagram of a phase-locked loop, encompassing a phase detector (PD), loop filter (LF), and voltage-controlled oscillator (VCO).

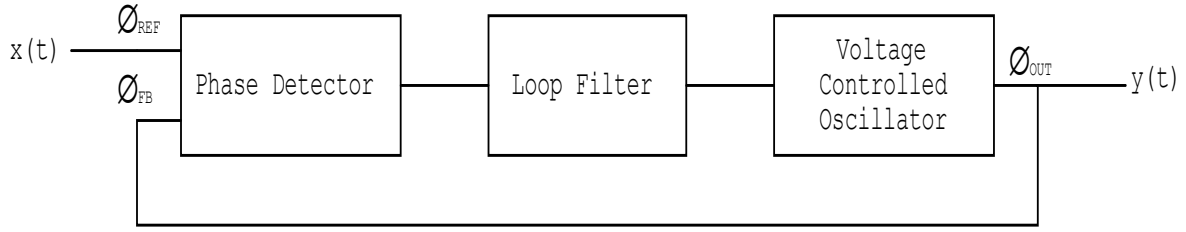

Figure 2.14 - Type I PLL Architecture [22].

The loop is considered to be in a "locked" state if the phase difference, $\Delta\varphi$, between *x(t)* and *y(t)* is constant with time, due to the phase and frequency match between *x(t)* and *y(t)*. Once the locked condition is met, all the signals in the PLL occur at a steady state, at which point the PD produces a DC value proportional to $\Delta\varphi$ [22]. The low-pass filter suppresses the high frequency components of the PD output. The VCO now oscillates at a frequency equal to the reference signal frequency with a phase error of $\Delta\varphi$.

If the phase difference changes momentarily, i.e. *y(t)* has had a slight phase shift, *x(t)* will accumulate phase faster than *y(t)* such that the phase detector will produce wider pulses. Each pulse will create an increasingly higher DC voltage at the output of the LPF, thus increasing the frequency of the VCO. As the difference between φ_{FB} and φ_{REF} decreases, the pulse width at the output of the PD will decrease, eventually returning to a value that places the PLL in a locked state. This is known as "tracking". Thus, the loop locks under only two conditions: 1) ω_{FB} is equal to ω_{REF} and 2) φ_{FB} and φ_{REF} are matching. It should be noted that this type of PLL falls under "Type I phase-locked loops" classification.

To decrease the time required to achieve a lock-state, a separate frequency detection circuit may be used. The most commonly used topology for high-speed data I/O and frequency synthesis is a "Type II" charge-pump based PLL (CPPLL). Since the development of PLLs using phase/frequency detectors and charge-pumps, the CPPLL (Figure 2.18) has been the dominant choice in high performance clock recovery and frequency synthesis applications [22].

A Type II PLL generally consists of a phase/frequency detector, charge-pump, loop filter and a VCO. The phase/frequency detector (PFD) detects the phase, frequency, difference between the reference clock (φ_{REF}), and the feedback clock (φ_{FB}), and generates UP and DN

signals. The charge-pump outputs a square wave current whose average value is proportional to the phase/frequency difference detected by the PFD (UP/DN signals) [23-24]. The loop filter then removes high frequency components from the square wave and converts the current through the low-pass filter to a voltage signal that is used to control the oscillation of the VCO. The signal is then fed back to the PFD as φ_{FB}.

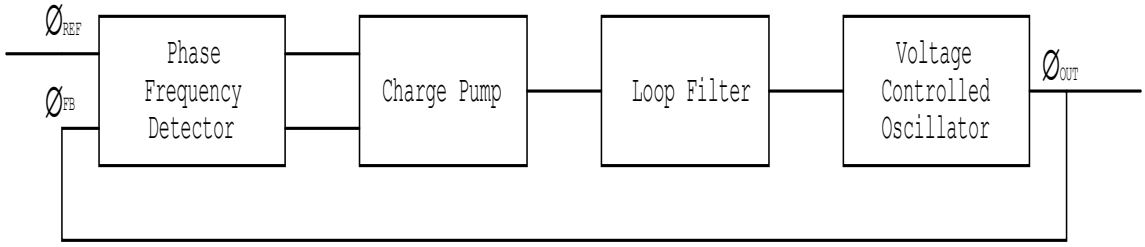

Figure 2.15 - Type II PLL Architecture [23]

2.6.1. VCO

A voltage-controlled oscillator is a very critical part of PLL. For a VCO that is to be used in a PLL, the following parameters are important:

1) Tuning range: the range between the minimum and maximum values of the VCO frequency. In this range, the variation of the output signal amplitude and jitter must be kept at a minimum. 2) If the VCO is integrated in a mixed-mode circuit, it must be highly immune to supply and substrate noise; therefore, a fully differential VCO is desirable.

3) Timing accuracy requirements place an upper bound on the VCO jitter and phase noise. For the above reasons a fully differential ring VCO is employed in the design. A differential ring VCO consists of an even number of VCO delay cells that are connected to each other in a loop.

The transistor level schematic of the VCO delay cell is shown in Figure 2.16.

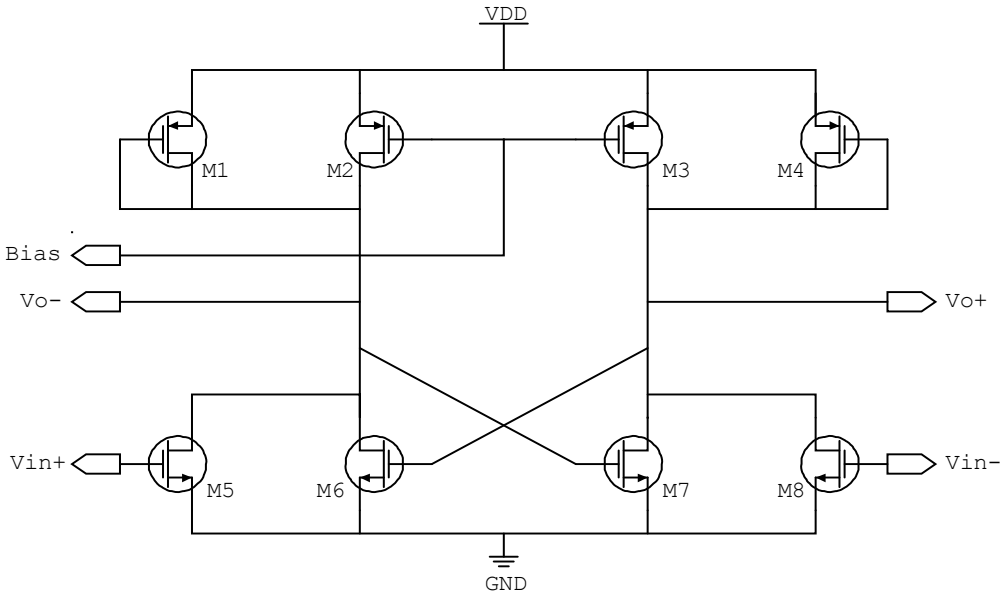

Figure 2.16 - Transistor level VCO delay cell [25].

The delay cell of the VCO is a fully differential cross-coupled cell including a positive feedback latch and symmetrical load. The symmetrical load is provided through transistors M1 and M4; furthermore, transistors M6 and M7 create the latch. The symmetrical load is placed to improve linearity of the VCO and the latch is placed to speed up the discharging process and to reduce timing jitter (phase noise) [25]. In this topology, a biasing tail current is not required and thus the flicker noise from the tail current source is eliminated. To further lower the VCO frequency, MOS-Capacitors may be added at the output of each delay cell, as shown in Figure 2.17. However, this addition would add extra capacitance load and thus increase the delay of each cell, further lowering the VCO frequency.

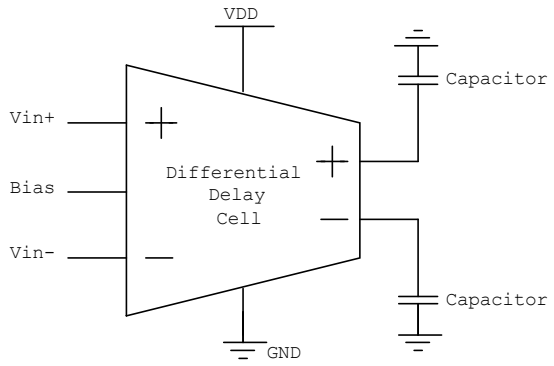

Figure 2.17 - VCO delay cell [25].

2.6.2. Phase Detector

The objective of a phase detector is to generate an output signal whose average value is linearly related to the difference between φ_{REF} and φ_{FB}, as described in the equation below [26]:

$$PD_{OUT} = Avg\ (\varphi_{REF} - \varphi_{FB}) \qquad (2.15)$$

PD_{OUT} is the average value of the output signal and can be a voltage, current, or charge depending on the particular PD implementation. Two forms of phase detection are linear and non-linear. Linear phase detectors can be implemented with standard CMOS logic gates--AND, OR, XOR--and latches to produce a pulse-width modulated signal. Figures 2.18-2.20 show the previously mentioned linear phase detectors and their transfer characteristics.

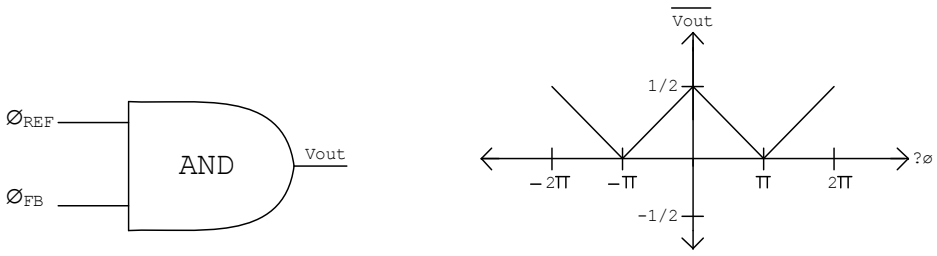

Figure 2.18 - AND PD [26].

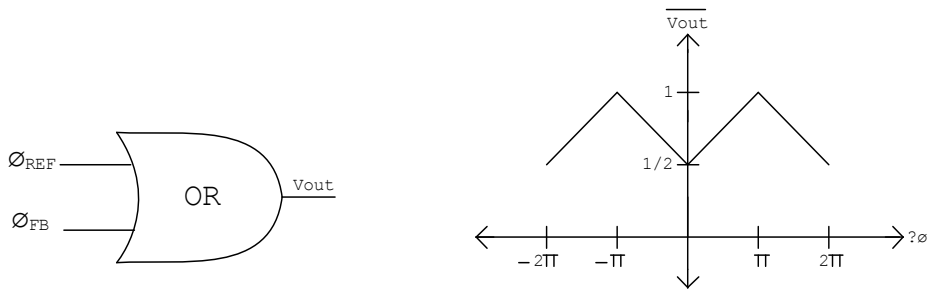

Figure 2.19 - OR PD [26].

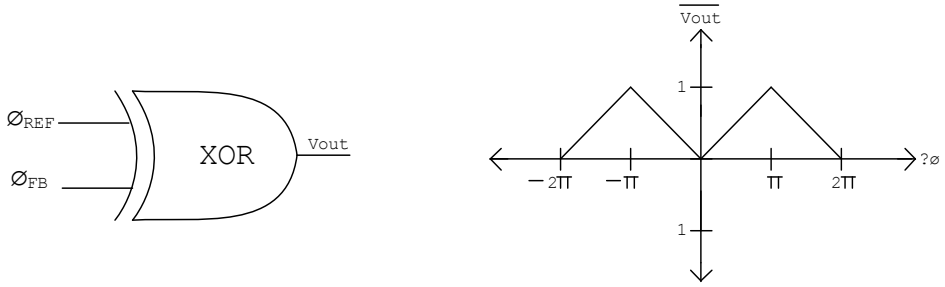

Figure 2.20 - XOR PD [26].

A downfall of these phase detectors is their duty cycle distortion sensitivity, phase and voltage offsets, and limited linear range, which necessitates additional circuitry. A frequency detector may be added to the phase detector. One advantage of the phase/frequency detector is the ability to not only detect the phase difference but also the frequency difference between φ_{REF} and φ_{FB}, thus speeding up the lock time. As well, insensitivity to duty cycle distortion, increased linear range, and zero phase and voltage offset are other key advantages of this structure [23]. Figure 2.21 shows a typical PFD and its transfer characteristics. Evidently, the DC component of the difference of the UP and DN signals is in fact linearly related to the phase and frequency difference (φ_{REF} and φ_{FB} difference).

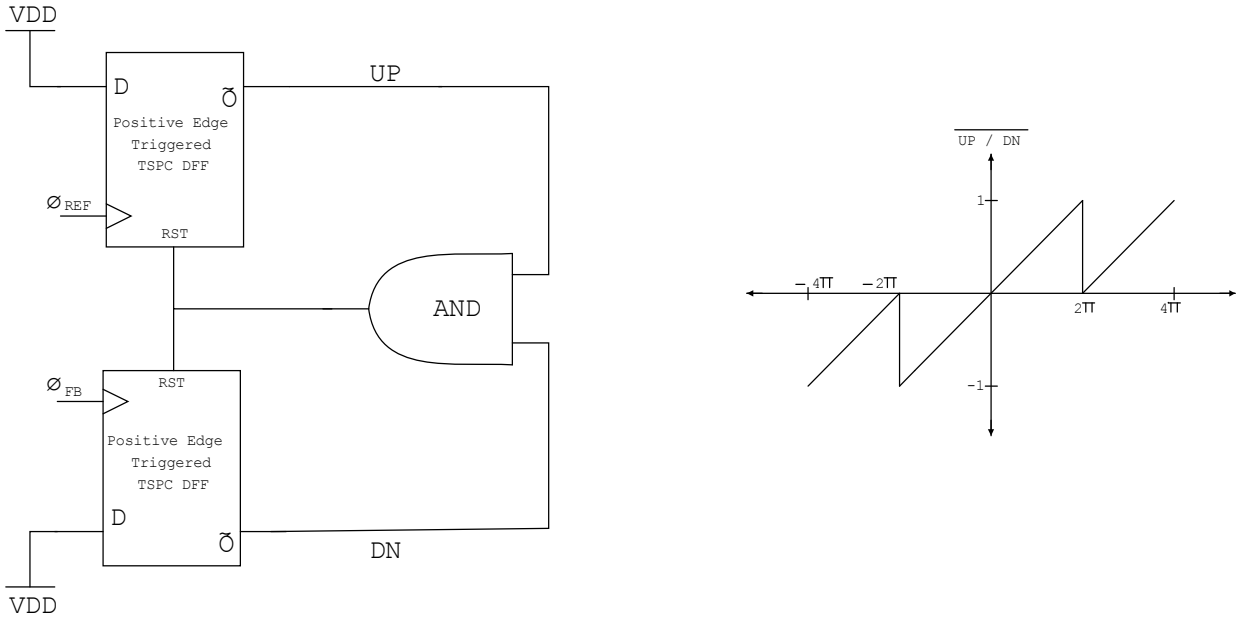

Figure 2.21 - Typical phase frequency detector [27].

One popular phase detector suitable for high speed I/O is the *lead-lag* or *bang-bang* phase detector (BBPD), shown in Figure 2.22. The simplest BBPD can be implemented using a single D flip-flop; the detector will output a digital *'1'* or *'0'* depending on whether φ_{FB} is leading or lagging with respect to φ_{REF}. An advantage of this type of phase detector is its simplicity and high-speed operation limited only by the speed of the fast flip-flop that can be designed in a given process. Because the output voltage is sensitive only to the polarity rather than the actual value of the phase difference of the inputs, a disadvantage is the high level of jitter that exists in the lock state. Suppressing high frequencies via the loop filter can alleviate this problem. As well, because a fully differential VCO is used, it has a tendency to reject high-frequency components applied to its voltage control input.

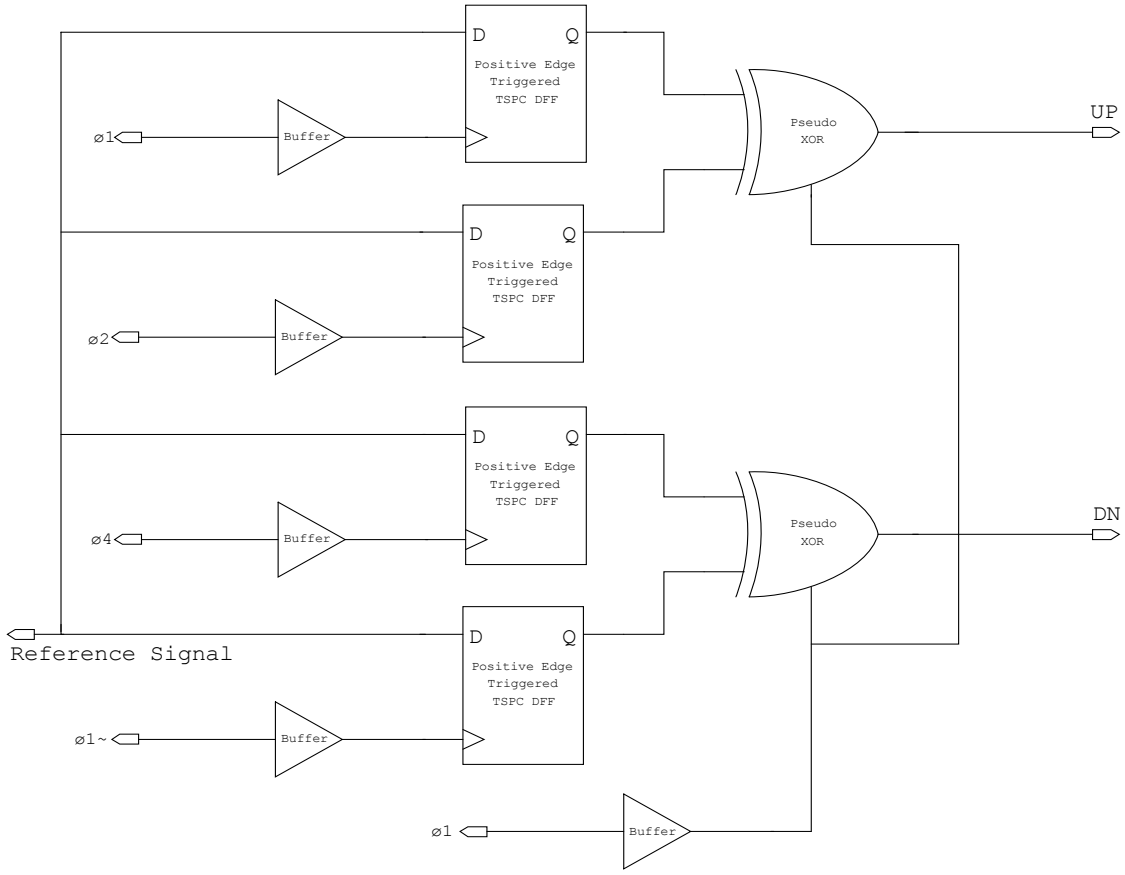

Figure 2.22 - Bang-Bang phase detector [26].

The 8-stage VCO has a total (DC) phase shift of 180^{o}, with each delay cell providing a 22.5^{o} phase shift. The bang-bang phase detector requires a $\frac{\pi}{4}$ signal spacing between each clock trigger on the TSPC DFF; thus, the clock signals for the DFF were taken from every other delay cell of the VCO. The "True-Single Phase D Flip Flop" (TSPC DFF) was used because it offers low transistor count, small chip area, fast transient response and simplicity of design.

As previously mentioned, four pairs of clock signals obtained from every other stage of the VCO are used for the bang-bang PD. The phase detection block uses these signals to generate two control signals UP and DN, according to which signals are leading or lagging the reference voltage; it then sends them downstream to the charge-pump.

2.6.3. Charge Pump and Loop Filter

A PFD is commonly used in conjunction with a charge pump and a loop filter to generate a control signal for the VCO. The charge pump converts the UP/DN signals to a current, I_{CP}. The current, which is the average value proportional to phase and frequency difference or a polarity based on lead-lag signals, is then fed to a loop filter that is typically a combination of a low-pass RC filter in parallel to another capacitor. As a rule of thumb, C_2 is typically chosen to be much smaller than C_1 (roughly 10 times smaller) and provides additional filtering at high frequencies. The series combination of C_1 and R provides a low-pass filter in order to suppress high frequency.

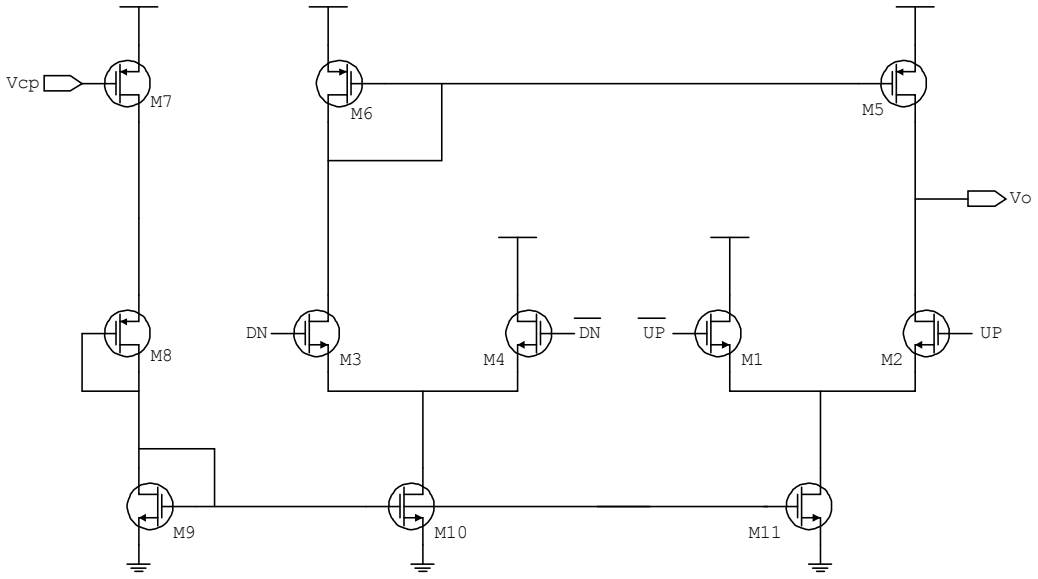

Figure 2.23 - Charge pump circuit [25].

The charge pump design, shown in Figure 2.23, is based on the improved current steering charge pump proposed in [25]. It essentially works as a digital-to-analog converter. The charge pump accepts two control signals UP and DN from the PFD and thus has three states. A charge-up state occurs when UP=1 and DN=0, where it conveys the current JUP to the load capacitor.

The charge-down state occurs when UP=0 and DN=1, and it sinks JDN from the load capacitor. Lastly, the lock state occurs when both UP and DN settings are the same in the bang-bang phase detector; this condition causes JUP=JDN so that the voltage across the capacitor remains unchanged.

2.6.4. Fractional divider

A divider block may be placed in the feedback path of the PLL, to build a PLL-based frequency synthesizer. The purpose of a frequency synthesizer is to generate a different, usually high, frequency signal than that of the reference signal. Typically, a crystal oscillator with a low frequency, roughly 10MHz ~ 100MHz, is used as a reference signal because a crystal oscillator is able to produce a pure (no jitter) signal. The simplest method to building a frequency divider is through a cascade of flip-flops, as shown in Figure 2.24, that is basically an asynchronous binary counter. However, to avoid the delay introduced by the inverter used in this circuit it is also possible to use the $\overline{Q}$ instead of inverting the Q of the DFF. Moreover, such a circuit was favored over other synchronous counters due to its simplicity. The input signal to the frequency synthesizer is the high frequency output of the VCO, while the output is a lower frequency, which is then compared with the reference signal by the PFD. If N is the divider ratio, the divider output frequency can be calculated by Equation 2.16.

$$\omega_{div} = \frac{\omega_{VCO}}{N} \tag{2.16}$$

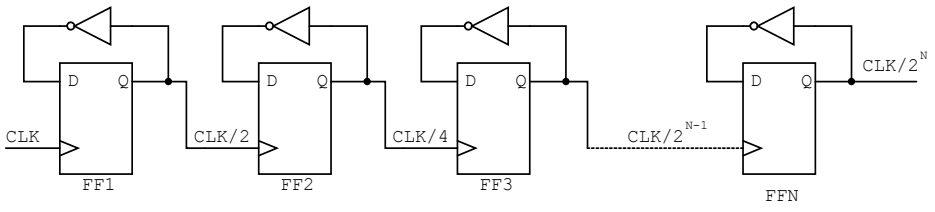

Figure 2.24 - Frequency divider.

Chapter 3: Time-mode SerDes

The rapid advance of CMOS technologies has resulted in more limitations such as loss of voltage headroom and shrinkage of voltage supply for the analog circuits that caused these circuits to deal with increasing voltage error and low signal-to-noise ratio (SNR) [28-31]. As an alternative to voltage mode circuits, current mode circuits have been widely used in many applications. However, the power consumed by these types of circuits make them appealing only for applications where power is not an issue and speed is of main importance [32]. The effect of technology scaling in the analog circuits has led to the introduction of digitally assisted circuits at the cost of increased circuit complexity and resultant higher power consumption. Technology scaling, on the other hand, has reduced the gate delay of the digital circuits, thereby improving the timing resolution of digital circuits [33]. Recently proposed designs show how useful this advantage could be, where the analog information is represented as the difference between two digital pulses. This concept has enabled analog signal processing to be performed with the help of time-mode circuits in the digital domain and thus avoiding the use of power hungry and low speed DSPs. Besides, as the CMOS technology scales down, the time-mode circuits offer higher speed and lower power consumption [31].

Time-mode signal processing (TMSP) in general is defined as the manipulation of sampled analog signal information using time-difference variables. TMSP enables the implementation of analog signal processing functions in any technology using the most basic element available, namely, propagation delay. Figure 3.1 shows the architecture of a time-mode SerDes, which consists of these two main blocks: PPM, which is in charge of data encoding and transmission, and TDC, which is in charge of the data reception and demodulation.

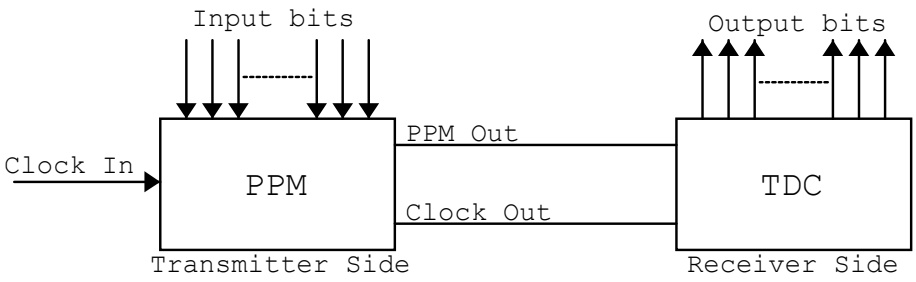

Figure 3.1 - Time-mode SerDes architecture [6].

3.1. PPM

A PPM signal uses a pulse of fixed width and amplitude that varies its position in relation to a data clock signal. The position of the pulse is determined using the value of the modulating bit word. In other words, the PPM module works as an N-bit programmable delay that, depending on the 2^N bit combinations, delays the input clock by a distinct amount.

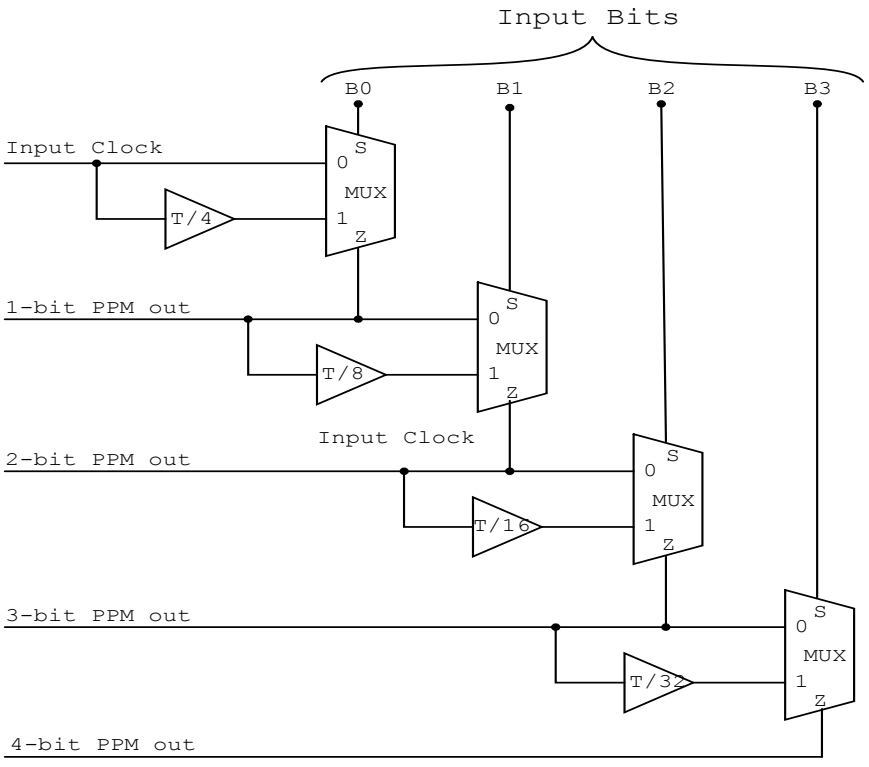

Figure 3.2 - Pulse position modulation block diagram [6].

The circuit shown in Figure 3.2 works by deciding whether or not to delay the pulse according to the appropriate value for each level of multiplexer-controlled delay, depending on the input being 1 or 0. In this case, the signal will be maximally delayed when the bit combination is 1111 and minimally delayed when the bit combination is 0000. The value of bit B0 controls the first multiplexer, which decides whether to pass the reference clock undisturbed or to delay it by T/4. Moreover, multiplexers 2 to 4 in the PPM circuit hierarchy are controlled the same way by bits B1, B2, and B3, respectively. When the output signal is read from the final stage in the hierarchy, the original reference clock signal is then delayed by a combination of the four types of delays assigned to each multiplexer. This combination of delays is read on the receiver side by the TDC circuit, which translates the delayed pulse back into the 4-bit data streams. The timing diagram for the above circuit could be observed in Figure 1.4.

To achieve an even higher data rate using the above design, another PPM module could also work parallel with the first module so that it modulates the falling edge of the signal. In other words, the first 4-bit PPM modulates the rising edge of the pulse, and the second 4-bit PPM modulates the falling edge of the pulse on the negative edge of the clock. In this way, the data rate would double. For instance, considering a clock frequency of 1.25 GHz the data rate will increase from 5 Gbps to 10 Gbps.

The description of the pulse position modulation can be characterized by the following equations [6]:

$$rising\ edge\ delay = (B3 * 2^0 + B2 * 2^1 + B1 * 2^2 + B0 * 2^3) \qquad (3.1)$$

$$falling\ edge\ delay = (B7 * 2^0 + B6 * 2^1 + B5 * 2^2 + B4 * 2^3) \qquad (3.2)$$

3.2. TDC

A time-to-digital converter (TDC) converts the time difference between two edges of two clock signals into a sequence of digital numbers. The applications of TDC initially appeared in nuclear science research, which dates back to 1970s [31]. Since then, however, TDC has been widely used in the design of all digital PLLs, sensor interface circuits, modulation and demodulation circuits, time-mode ADCs, digital storage oscillators, and many other applications [34-40]. An abundance of research regarding TDC implementation methods has been undertaken. Traditional TDC, where current or voltage is used as an intermediary stage, Counter-based TDC, where it counts the number of cycles of a reference clock fitting into the respective measurement interval [33], Vernier TDC, where the start and stop signals propagate into two different delay lines that will eventually catch up with each other [39], Time amplification TDC, which takes advantage of metastability of SR-Latch proposed in [41] are only a few of these methods. Below are more detailed and technical explanations of different TDC implementations.

3.2.1. Traditional TDC

The traditional approach to TDC is to use current or voltage as the intermediary stage, meaning that the time interval is first converted into a voltage and the voltage is then digitized by a conventional analog-to-digital converter (ADC). The start and stop signals are used to form a pulse width equal to the time duration that is being measured. An analog ADC is utilized to convert this pulse width to a voltage, which is then fed into the ADC for digitization. One of the main disadvantages of this approach is that the resolution achieved is not fine enough because the integrator block is connected to an integration capacitance with a finite output resistance (also a current source). Such resistance makes for weak linearity when short intervals are being

measured. Moreover, the finite bandwidth of the operational amplifier limits the speed, which means that resolution is significantly affected [33].

3.2.2. Counter-based TDC

One of the simplest TDC implementations is the flash or counter-based design, in which a counter is used to tally the number of clock cycles fitting into the measurement interval, as shown in Figure 3.3. Although simple, the main drawback with this approach is that, to improve the resolution or minimum measurement interval, the clock must run at a very high speed, which means more power consumption [33].

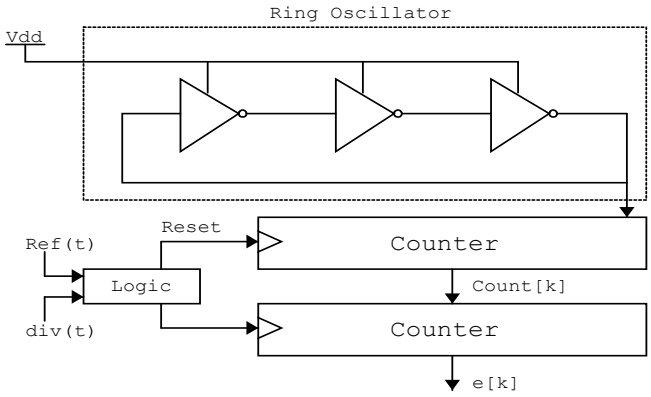

Figure 3.3 - Counter-based TDC architecture [33].

3.2.3. Single Delay Chain TDC

There are multiple approaches for designing a TDC circuit. A classic approach is the simple delay chain method in which the start signal is gradually delayed in different stages with each stage being fed as the input to a D Flip-Flop (DFF), while the stop signal is fed as the clock of the DFF simultaneously. At each stage the flip flops output a signal Q that, depending on its logical value, indicates whether the start and stop signals are synchronous or not. If both signals are synchronized, the DFF will output logic 1.

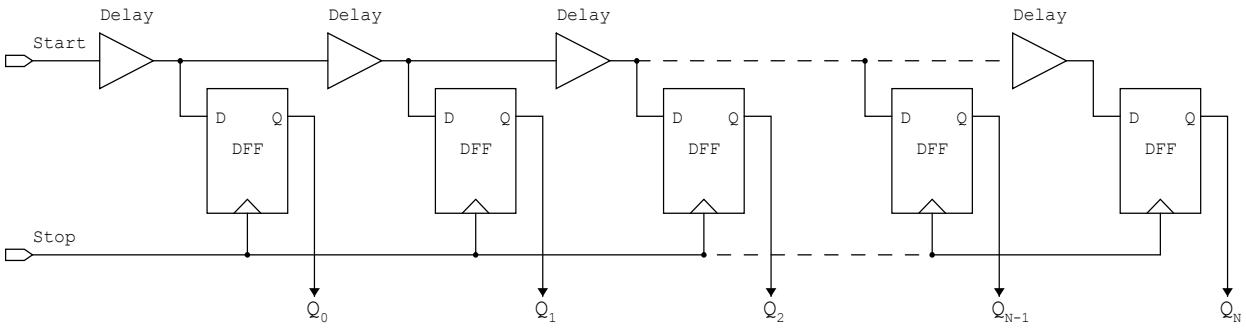

Figure 3.4 - Single delay chain TDC architecture [33].

3.2.4. Vernier TDC

The main problem with the single delay approach is the time resolution, which is set by a single delay cell. To improve the timing resolution, the delay cells must be tiny and the number of delay cells has to increase to an impractical level, since in the best case scenario the achievable time resolution would be around 10 Pico-seconds. To improve the time resolution of the above method, various authors suggest the use of a Vernier Delay TDC method in which the start is delayed by "Delay1" and is fed through the data input of the DFF. At the same time the stop signal is delayed by "Delay2"and is fed as the clock signal of the DFF. The output of the DFF at each stage becomes high once the two signals meet each other. In this way the timing resolution is improved to "Delay1 – Delay2" as compared to "Delay1" only, from the previous method. The Vernier method, however, suffers from mismatch issues that are more severe compared to a single delay chain. As well, in the Vernier approach the dynamic range of the TDC, which is the maximum time that can be measured, is limited to $DR=n*(td1-td2)$, where n is a number of delay elements of the delay line (indicative of the need for an additional circuitry). The large measurement range requires a large area on the chip. Figure 3.5 shows the architecture of the Vernier method [33, 42].

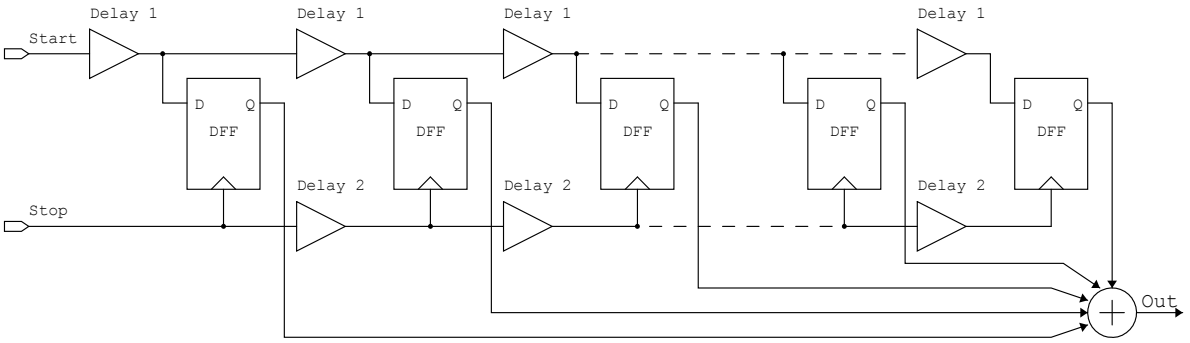

Figure 3.5 - Vernier TDC architecture [33].

3.2.5. Inverter Delay Line TDC

An inverter delay line based TDC was initially utilized in the implementation of a DPLL for a blue-tooth radio application in [37]. Figure 3.6 shows the circuit of inverter delay line TDC. Its time resolution is the propagation delay of an individual inverter, while its detectable range is proportional to the number of delay stages used. Its measured time interval can be expressed as $N*T_D$, where T_D is the time resolution of the TDC. Achieving a fine resolution contradicts the goal of achieving a large detectable range, since a TDC with finer resolution would require more delay cells in order to achieve the same detectable range. Additionally, both the time resolution and the detectable range of this type of TDC are very sensitive to PVT variations [34].

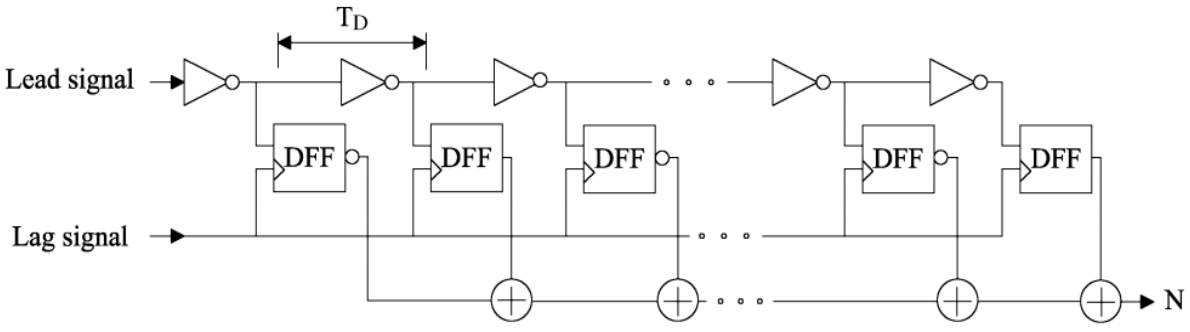

Figure 3.6 - Inverter delay line TDC architecture [34].

3.2.6. Vernier-Inverter delay line TDC

This type of TDC uses two delay lines instead of one as seen previously. The respective inverter delays are T_1 and T_2; thus, the effective time resolution will now be the delay difference T_2 - T_1, assuming $T_2 > T_1$. Moreover, the delay difference is now first-order tolerant of PVT variations if the two lines are well matched [34]. On the other hand, since the time resolution is now determined by a much smaller delay difference, an extensive number of inverter stages is required to cover a large detection range [43].

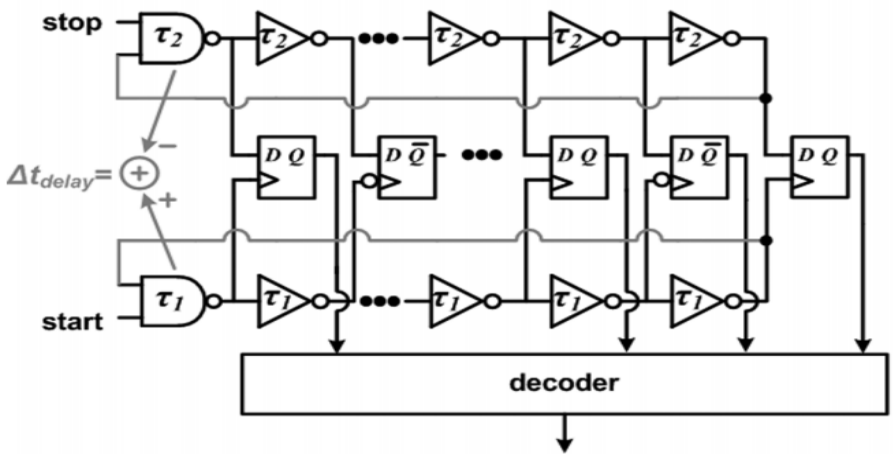

Figure 3.7 - Vernier-inverter delay line TDC architecture [43].

3.2.7. Two-Dimensional TDC

As mentioned earlier, more stages are used when attempting to improve the resolution of a TDC. This means that for measuring large intervals the length of the delay line must significantly increase. As the number of stages grow, jitter and sensitivity to mismatches escalate. In the linear Vernier, the time quantization is realized by taking the time differences only between taps located in the same position of the two delay lines. If all possible differences between the taps are used, the Vernier plane (of time references) can be built, where the number

of quantization levels is given by the product of the elements of two delay lines, as shown in Figure 3.8. An immediate consequence of this 2-D solution is a potential improvement of the TDC range, since the uniform quantization provided by the linear Vernier (from Δ to 5Δ) is extended to the range (from -3Δ to 9Δ) [44].

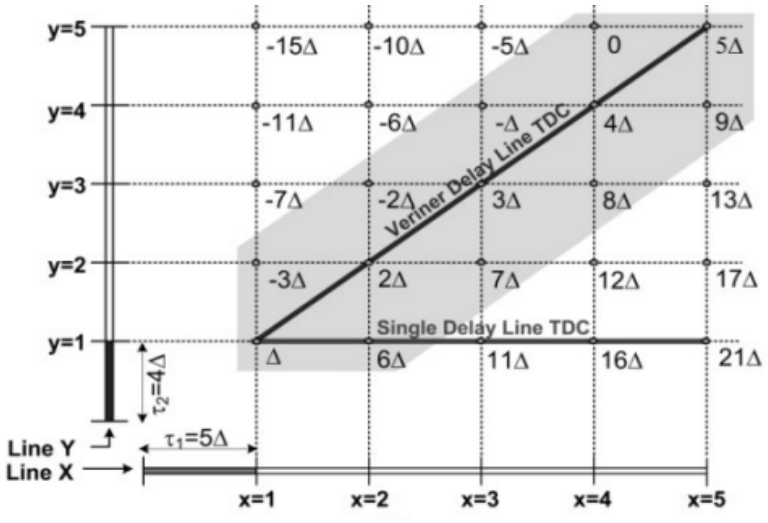

Figure 3.8 - Time quantization of 2-D Vernier TDC [44].

Figure 3.9 shows a 7-bit 2-D TDC that was designed and implemented in [44]. To provide a better symmetry, the delay lines were realized by non-inverting delay stages in order to perform the digital conversion only on rising edges.

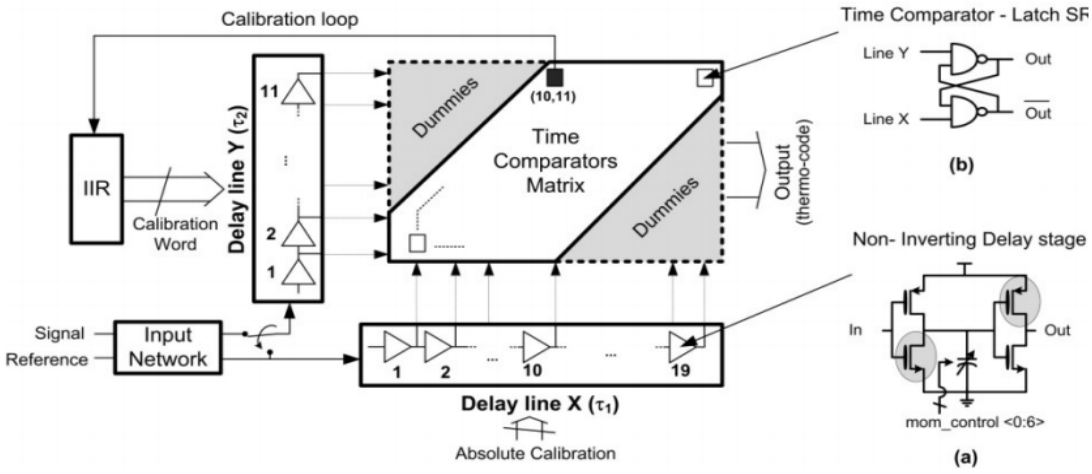

Figure 3.9 - 2-D Vernier implementation [44].

3.2.8. Hybrid TDC

To reduce the area used by Vernier TDC, a two-step TDC architecture has been proposed in [45]. In this approach the first stage uses a single delay chain to produce a coarse measurement. At the second step, using the Vernier method, a fine measurement signal is produced. This approach is shown in Figure 3.10.

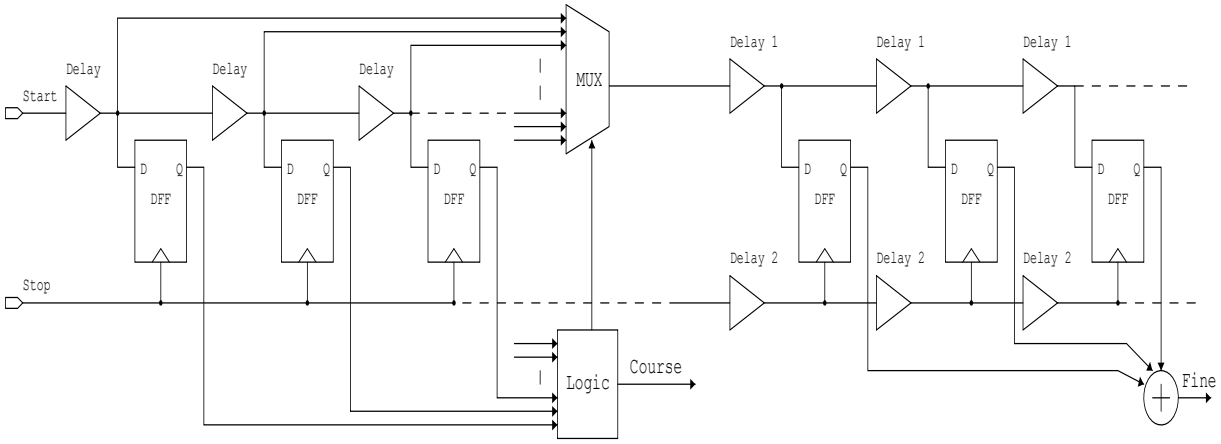

Figure 3.10 - Hybrid TDC architecture [45]

3.2.9. Time Amplifier (TA)

In an approach similar to hybrid TDC proposed in [42], a single delay chain is used at the first step, and the remaining residue is amplified through the utilization of a time amplifier (TA). Finally, another step of single delay chain is used to obtain a fine resolution. The idea of using time amplifiers suggests taking advantage of the metastability of an SR latch to amplify the time difference of the input at the output. In other words, metastability leads to progressively slower output transitions as setup time on the latch is encroached upon. Figure 3.11 shows leveraging metastability to create time amplification.

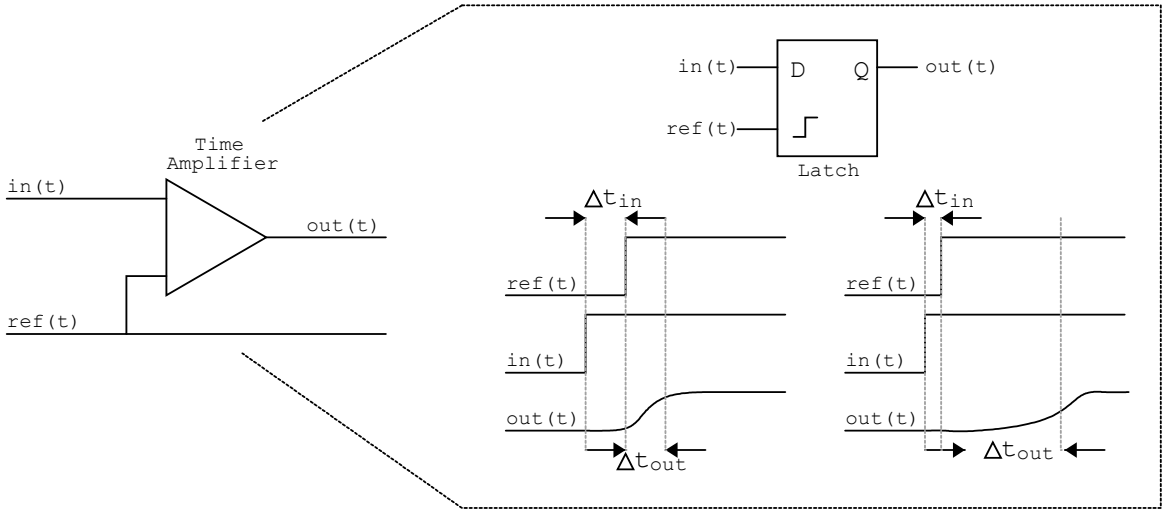

Figure 3.11 - Time amplification using an SR latch [42].

3.2.10. Gated Ring Oscillator (GRO) based TDC

Another well-known approach for implementing a TDC circuit is the Gated Ring Oscillator (GRO) method, which applies the same idea as in the oscillator-based TDC. However, the ring oscillator is applied only during measurement intervals, and the state of the oscillator is held between measurements. In this way the quantization error becomes shaped by first order noise [46]. Figure 3.12 shows how the GRO method can improve the quantization noise.

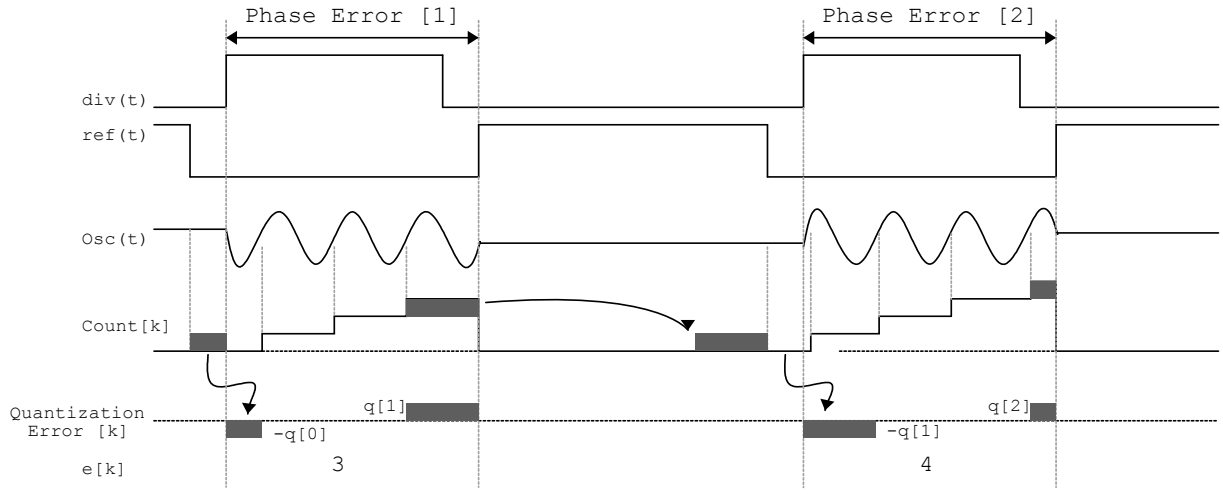

Figure 3.12 - First-order quantization noise [46].

Moreover, the resolution could be further improved as proposed in [47], where all phases of the ring oscillator have been used. Figure 3.13 shows the improved GRO approach.

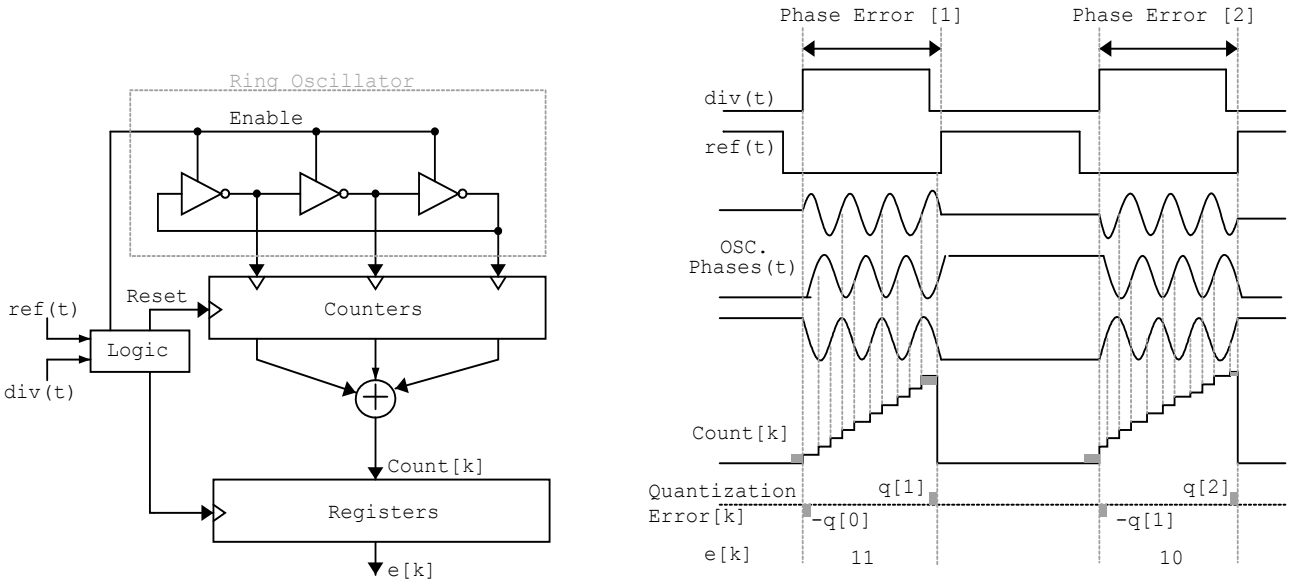

Figure 3.13 - GRO TDC with the use of ring oscillator phases [47].

3.2.11. Interpolating TDC

Another commonly used TDC is known as the interpolating TDC proposed in [36], in which fine resolution is achieved through interpolation between the edges.

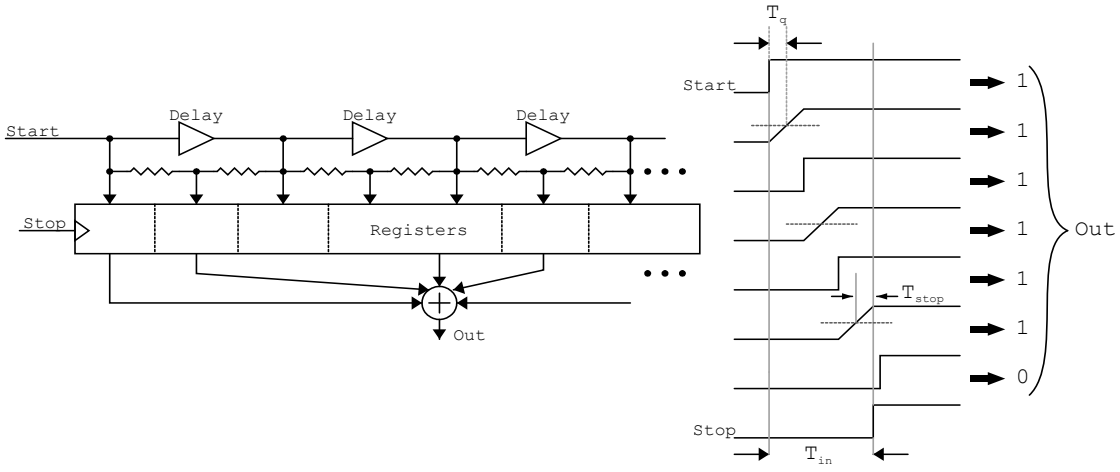

Figure 3.14 - Interpolating TDC operation [36].

Figure 3.14 and Figure 3.15 show the operation of the interpolating TDC and its possible implementation, respectively.

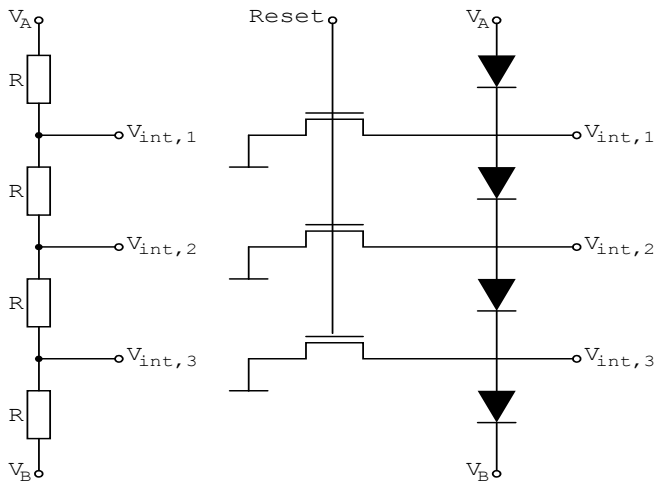

Figure 3.15 - Implementation of interpolation circuit using resistor or diode [36].

3.2.12. Cyclic Vernier TDC

The quantization noise from the TDC impacts in-band phase noise of the receiver; thus, a high resolution TDC is desirable. In [48] an improved version of the oscillator-based (Cyclic) TDC is proposed that consists of two DCOs running at different speeds. The goal of the TDC is to measure the time difference between the rising edges of the "Start" and "Stop" signals (F_{ref} *and* F_{div}) in the ADPLL, respectively. When the "Start" is asserted, the slow DCO starts to oscillate with a period of T_s, and the coarse counter counts the number of oscillations. After an input delay of T_{input}, it activates the "Stop" signal, which triggers the faster DCO to oscillate with a period of T_f. At this time, the coarse counter is disabled, and the output of the counter represents a coarse measurement of the time between "Start" and "Stop" rising-edges (T_{course}). To improve the measurement accuracy, the residue of the input delay, T_{fine}, is measured by the Vernier structure. When T_f is slightly smaller than T_s, the time difference between rising edges of

the two oscillations is reduced every cycle by the difference in periods (T_f- T_s) so that the edge of the fast DCO eventually catches up to the slow DCO. T_{fine} is measured by counting the number of cycles it takes for the fast DCO to catch up with the slow DCO. Then the overall measurement of T_{input} can be determined according to the equation below [48]:

$$Tinput = Tstop - Tstart = Tcourse + Tfine = N_sTs + N_f(Ts - Tf) \qquad (3.3)$$

Where N_s and N_f are the number of cycles of the slow and fast oscillations, respectively, and (T_s -T_f) is programmed to be much smaller than T_s. Figure 3.16 shows the architecture and operation of this method.

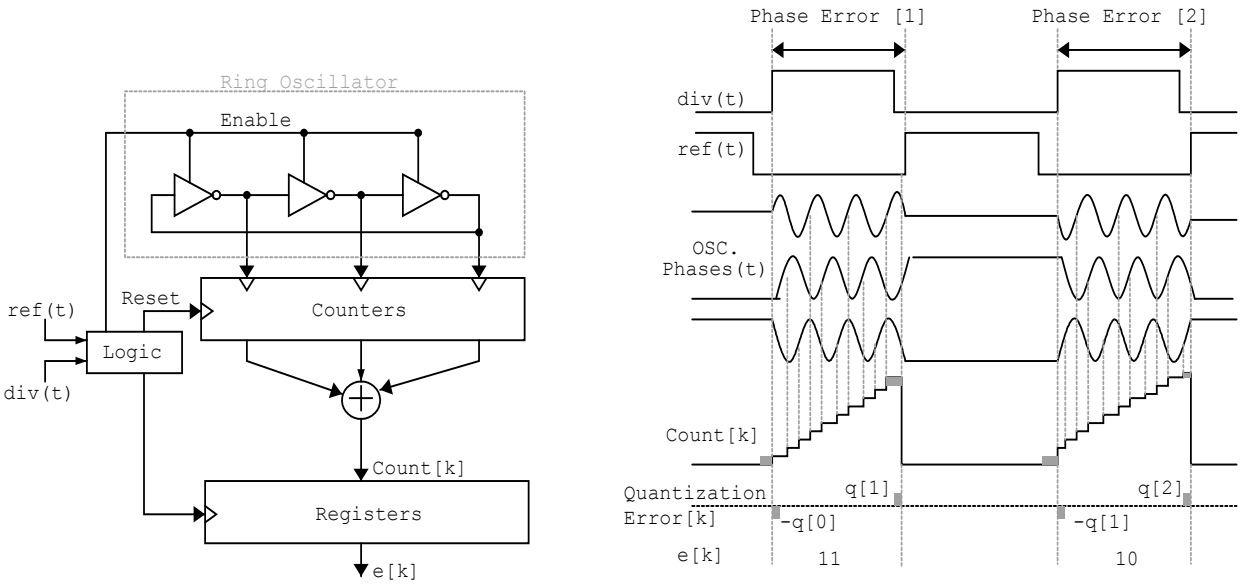

Figure 3.16 - Cyclic-based TDC with improved time resolution [48].

3.2.13. Pulse shrinking TDC

In this type of TDC, a square wave initially enters the inverter couple, as shown in Figure 3.18. Due to the first unit inverter cell and the M times load of the second unit inverter cell, the

output waveform is asymmetric. The effective pulse width compared to the initial pulse width is reduced by tPLH1–tPHL1. Similarly, this phenomenon occurs until the overall pulse width is reduced to tPHL2–tPLH2+tPLH1–tPHL1. The resultant signal will then be passed through a counter for digitization of the signal, as shown in Figure 3.17 [49].

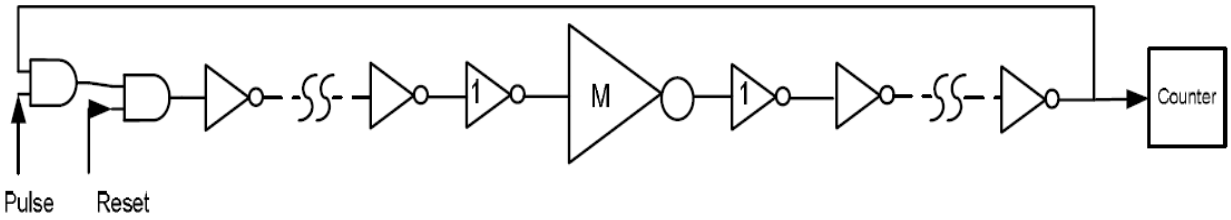

Figure 3.17 - Pulse shrinking TDC circuit diagram [49].

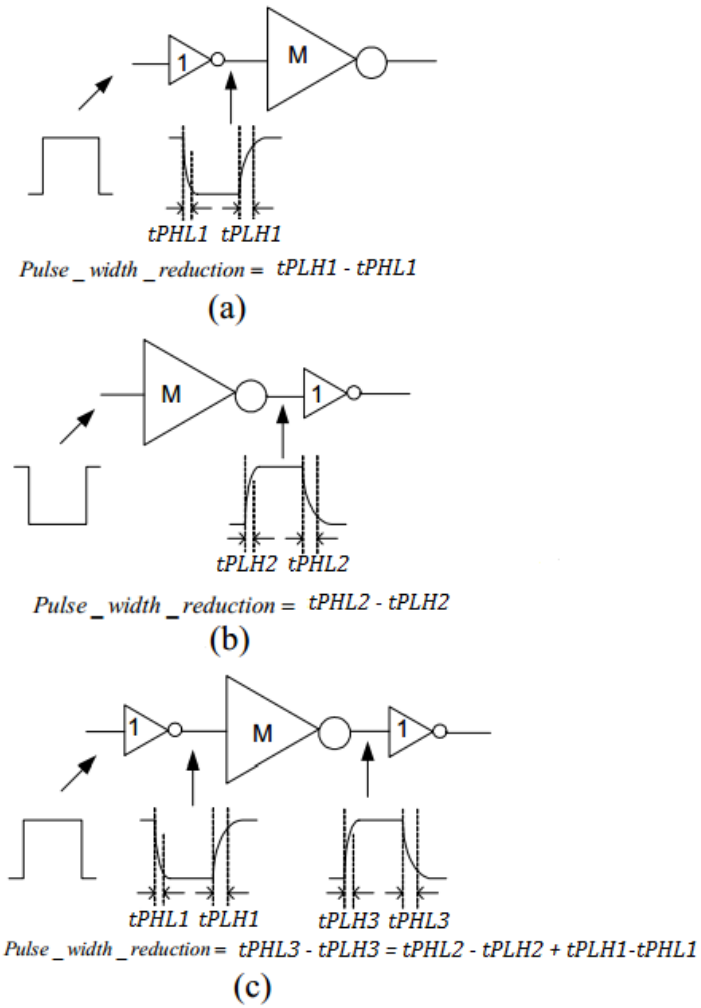

Figure 3.18 - Pulse shrinking TDC operation [49].

Chapter 4: Proposed Testability Feature of Time-mode SerDes

As seen in the previous chapter, the pulse position modulated signal is generated by utilizing a programmable delay to shift the clock signal by the parallel bits. The PPM module, investigated in [6] and shown in Figure 3.2, consists of four multiplexers and four delay elements. Although the operation seems simple, the design suffers from circuit complexity, which demands a much simpler design. Moreover, it lacks speed because each multiplexer must wait for the incoming signal from the previous multiplexer stage. In other words, when the first bit, B0, is fed in, the input clock is shifted by T/4; when the second bit, B1, is fed in, the signal has to wait for the operation of the first multiplexer to be done; and so on. Additionally, this design lacks the testability feature, meaning that if a fault is present in any of the delay elements, the input signal will be shifted by the wrong amount of delay. Therefore, the TDC will demodulate the wrong bit sequence. Due to the aforementioned issues, a simple testable 4-bit programmable delay has been proposed in this chapter to be used in the design of time-mode SerDes, more specifically at the transmitter side.

The 4-bit programmable delay, shown in Figure 4. 1, consists of a PMOS branch to create a distinct amount of current depending on the input bits. The created current is then converted to voltage using the diode connected MOSFET and is used to bias the NMOS transistor. Depending on this biasing voltage, each combination of parallel bits would shift the clock signal by a different amount since each PMOS transistor has a unique size. Hence, each unique transistor makes a distinct amount of current that results in shifting the input clock by a distinct amount. In

other words, the delay created by the combination 0011 would be different than the delay created by the combination 1100.

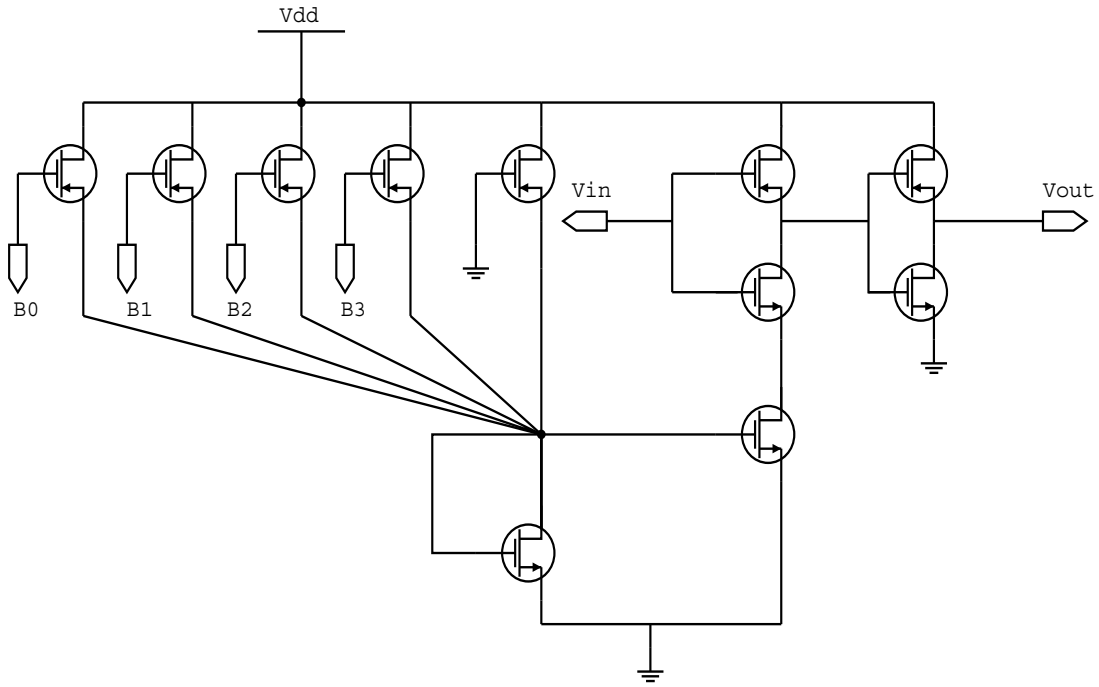

Figure 4.1 - Transistor level circuit of the proposed 4-bit programmable delay.

Figure 4.2 shows the implemented circuit of 4-bit programmable delay in Cadence environment, while Figure 4.3 shows the transient response of this circuit using a clock frequency of 1 GHz. Note that the output corresponds to a delayed input signal depending on the combination of bits B0, B1, B2 and B3. This circuit could be used as the PPM module of a time-mode SerDes architecture, as shown in Figure 3.1, where the synthesized clock is delayed according to the parallel data bits. The pulse position modulated signal along with the main clock is then transmitted through the channel, and then received and demodulated using the TDC module at the receiver end.

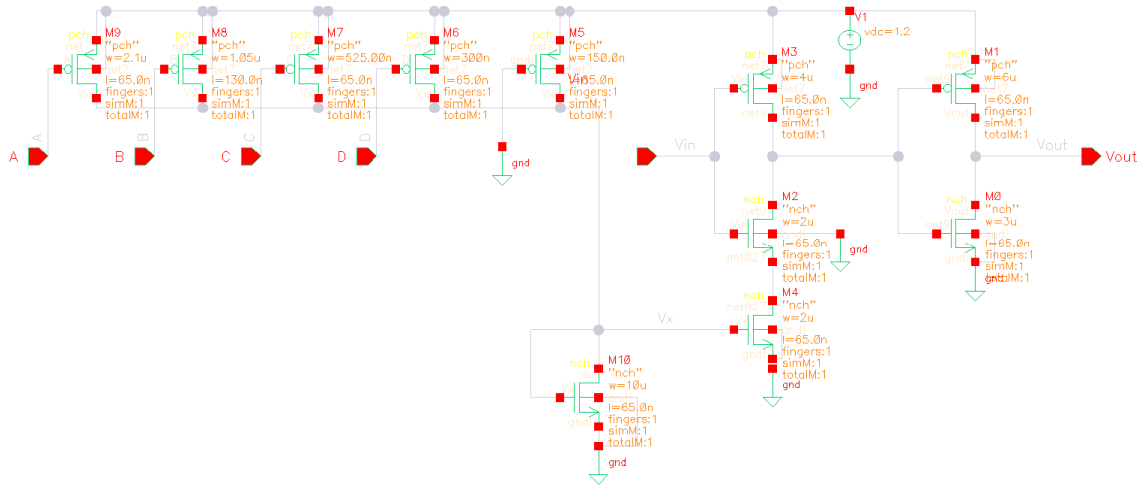

Figure 4.2 - Implemented circuit of proposed 4-bit programmable delay in Cadence environment using TSMC 65 nm technology.

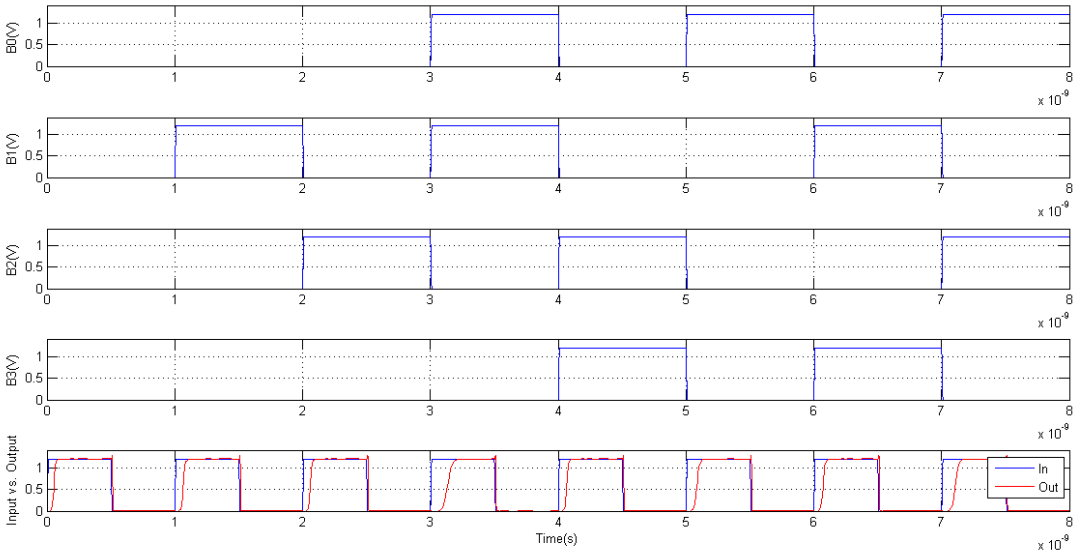

Figure 4.3 - Transient response of the proposed 4-bit programmable delay.

Table 4.1 summarizes the possible delays for all 16 combinations for an input signal of 1 GHz (4 Gbps data rate). The created delay is the difference between the positive edges of the original clock signal and the delayed clock signal. Note that the 4-bit programmable delay only delays the positive edge of the clock rather than delaying both the positive and the negative

edges of the original clock. The reason for this divergence is the fact that TDC requires only the positive edges of the signals for demodulation. However, with slight modification of the programmable delay shown in Figure 4.1, the negative edge could also be shifted if needed for different applications or if one needs to remain faithful to the concept of PPM where both amplitude and pulse width are required to remain constant.

Table 4.1 - Possible delay for the 4-bit programmable delay.

#	Bit Combination (B3 B2 B1 B0)	Delay(ps)
1	0 0 0 0	30
2	0 0 0 1	45
3	0 0 1 0	60
4	0 0 1 1	75
5	0 1 0 0	85
6	0 1 0 1	95
7	0 1 1 0	105
8	0 1 1 1	120
9	1 0 0 0	135
10	1 0 0 1	150
11	1 0 1 0	165
12	1 0 1 1	185
13	1 1 0 0	200
14	1 1 0 1	225
15	1 1 1 0	250
16	1 1 1 1	300

When observing the SerDes architecture illustrated in Figure 3.2, it is evident how important the programmable delay module is. That is, if any type of fault is present in this part of the circuit, it could result in shifting the clock signal by a wrong amount of delay and thus demodulating and parallelizing bits other than those intended for transmission. In other words, if any of the PMOS transistors in the PMOS branch of the programmable delay circuit contains even one fault, such as stuck-on or stuck-open, the overall design would be ruined.

To avoid the occurrence of the aforementioned issues, the designed 4-bit programmable delay would have a built-in-self-test (BIST) circuit checking capability. Prior to running the normal operation of the overall circuit, it would check for the presence of two potential types of faults, namely, stuck-on and stuck-open in the PMOS branch. The proposed BIST will be able to detect single or multiple stuck-at faults, and it will figure out which of the transistors located in the PMOS branch contains this type of fault. Moreover, the BIST is a confirmation of the output of the normal operation of the delay cell. In other words, if the BIST does not detect any faulty PMOS transistors, it is safe to assume that the normal operation is indeed correct; thus, the input signal will be shifted by the correct amount of delay.

The BIST circuit (see Figure 4.4) consists of a test sequence generation circuit along with a TDC module. Note that the proposed BIST circuit can be built using the standard cell components, thus minimizing the probability of containing any faults. Another main advantage of this technique is the speed and simplicity of the design. Moreover, it is believed that, with slight modifications to the proposed circuit, the idea of using TMSP (Time Mode Signal Processing) for fault detection can be extended to faults other than stuck-at faults, such as delay faults.

Note that the TDC block shown in Figure 4.4 can be any of the possible designs as thoroughly discussed in Chapter 3. Table 4.2 summarizes these possibilities along with their corresponding operations and their associated advantages and disadvantages.

Table 4.2 - Summary of different TDC designs.

TDC type	Operation	Advantages	Disadvantages
Traditional TDC	Time difference is converted to current or voltage; then ADC is	Simple to implement	Poor resolution

	used for conversion to digital bits.		
Counter-based TDC	A counter tallies the number of clock cycles fitting into measurement interval	Simple to implement	Clock must run at very high frequency for fine resolution. Consumes too much power
Single delay chain TDC	Start signal is delayed gradually until it meets stop signal. The output of the DFF at each stage is the translated bit sequence.	Simple to implement	Delay mismatch. Requires tiny delay cell for fine resolution. Highly dependent on technology scaling.
Vernier TDC	Same structure as single delay chain TDC. However, a smaller delay stage now shifts the stop signal as well.	Simple to implement Much better resolution	Delay mismatch Highly dependent on technology scaling. Requires large area for measuring long intervals.
Inverter delay line	Same structure as single delay chain TDC, where the buffer is replaced by an inverter.	Simple to implement Improved resolution	Delay mismatch Requires many delay stages for measuring long intervals. Very sensitive to PVT.
Vernier inverter delay line	Same structure as inverter delay line. However, the stop signal is delayed by a smaller inverter stage.	Improved resolution Delay difference is tolerant of first-order PVT variations.	Delay mismatch Requires extensive number of inverter stages to cover large detection range.
Two-dimensional TDC	Similar to Vernier TDC. But, all the differences between the delay taps are used.	Fine resolution	Complex circuit implementation.
Hybrid(Two step) TDC	Utilizes single delay chain TDC for coarse measurement and Vernier TDC for fine	Improved resolution. Less consumed area compared to Vernier TDC.	Contains issues associated with single delay chain TDC and Vernier

	measurement.		TDC.
Time amplifier	Uses a single delay chain TDC for coarse measurement. Then amplifies the residue using SR latch metastability for fine measurement and uses another stage of TDC to convert to digital bits	Fine resolution	Complex circuitry. Consumes too much area.
GRO-based TDC	Similar to oscillator-based TDC, but oscillator only runs only during measurement interval.	Improved quantization noise.	Oscillator must run at high frequency to achieve fine resolution.
Interpolating TDC	Fine resolution is achieved by interpolating the edges.	Improved resolution. Simple to implement.	Requires large area for long detection range.
Cyclic Vernier TDC	Consists of two DCOs running at different frequencies. Start triggers the slow DCO, and Stop triggers fast DCO. The operation ends when the two clock signals meet each other.	Fine resolution Improves quantization noise.	Consumes too much power.
Pulse shrinking TDC	The square pulse is passed through an inverter couple. Due to the unit inverter cell and the M times load of the second inverter, the pulse width shrinks. This operation is performed and then passed through a counter for digitization.	Fine resolution. Simple to implement	Extensive number of inverter stages are required. Delay mismatch may occur.

The operation of the proposed circuit shown in Figure 4.4 is as follows: Two operating modes exist for the 4-bit programmable delay, namely, normal operation mode and test mode. In normal mode the circuit operates as designed, assuming there are no faults, meaning the user

inputs the bit sequence that would control the PMOS branch to delay the input signal by a certain amount depending on the combination of bits. In test mode, on the other hand, the input signal needing to be delayed would be shifted by the amount generated via the test sequence generation circuit as part of the BIST circuit. The two sets of generated bit sequences are 0 0 0 0 and 1 1 1 1 for the purpose of detecting any stuck-at faults that might occur in any of the PMOS transistors in the PMOS branch. When the circuit runs in test mode, the test sequence generation circuit shown in Figure 4.4 would initially generate 0 0 0 0 to check if there are any stuck-open faults. This process is performed by turning all the PMOS transistors on; assuming a fault-free case, the expected delay should be the minimum possible. When the input signal is delayed, this amount is confirmed by the TDC module, which quantizes the difference between the main clock signal and the delayed input signal. If after decoding the digits generated by the TDC, bit sequence 0 0 0 0 is observed, then it is safe to assume the circuit does not contain any stuck-open faults. However, if the generated bits by the TDC are different than 0 0 0 0, for example 0 0 1 1, this indicates that the first two bits, B0 and B1, are stuck-open. However, the testing operation does not end here, as we need to ensure whether the last two bits, B2 and B3, are indeed 0 0, respectively or are stuck-on. This step is achieved by inputting the 1 1 1 1 sequence, generated by the test sequence generation circuit to the 4-bit programmable delay and later demodulating by the TDC module. The bits generated by the TDC, along with previously generated bits, can be used to determine if any stuck-at faults exist and, if so, which PMOS transistors contain these faults. In other words, the test mode consists of two steps, and a conclusion is made once these steps are both performed. If the test determines that there is no fault, the testing operation can be stopped, and normal operation will begin.

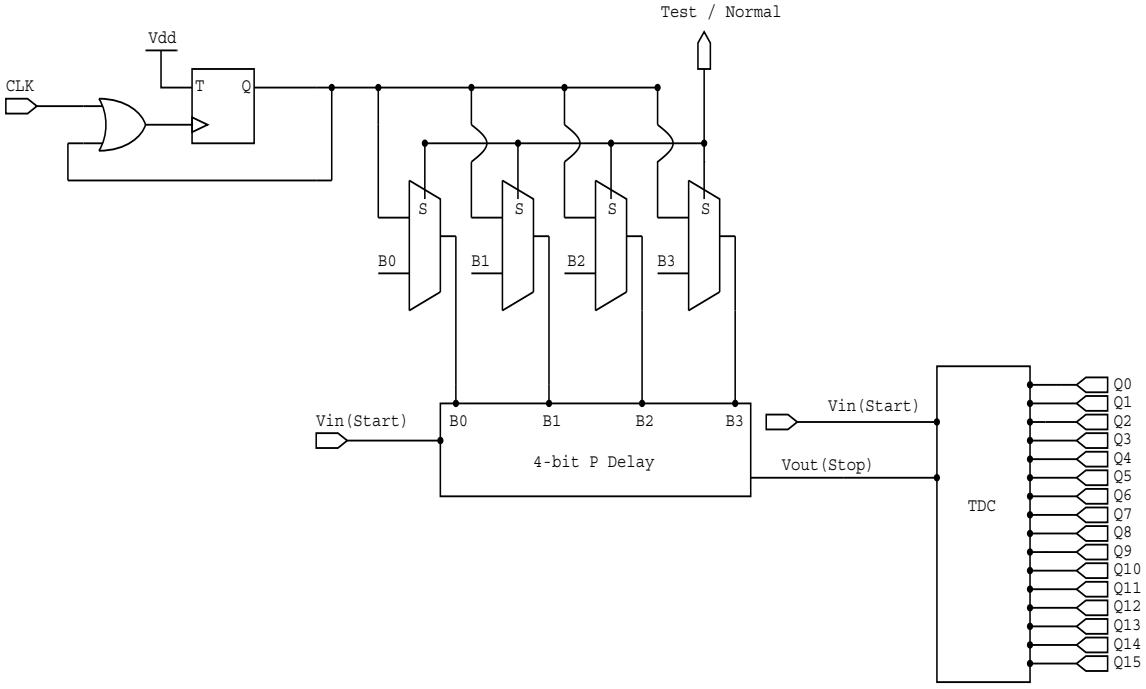

Figure 4.4 - Test mode of the proposed BIST 4-bit programmable delay.

When the test sequences 0 0 0 0 and 1 1 1 1 are generated, they are inputted into the 4-bit programmable delay, and the TDC output is checked. When the test sequence is 0 0 0 0, the difference between the main clock and the delayed clock are 30ps (minimum delay) thus TDC outputs the first 3 bits (Q0 to Q2) as 1 and the rest of the outputs as 0. When the test sequence is 1 1 1 1, maximum delay occurs. Thus, the TDC will generate all the output bits (Q0 to Q15) as 1.

Chapter 5: DPPM-based SerDes

As mentioned in Chapter 3, the main idea of PPM-based SerDes was to delay the clock signal according to the parallel input bits. Furthermore, transmitting the embedded clock and delayed clock to the receiver, after which the signals are revived through decision feedback equalization (DFE), a TDC could be used to demodulate and simultaneously make the serialized data parallel at the receiver by simply finding the difference between the positive edges of the clock signal and the shifted clock signal. The delayed clock signal is called pulse position modulated signal, also known as pulse phase modulation, in chip-to-chip communications. This signal refers to delay encoding technique, where the amplitude and width of the pulse is kept constant and the position of each pulse is varied in relation to the reference clock. The pulse position modulated signal is generated by utilizing a programmable delay to shift the clock signal by the parallel input bits. The PPM module, investigated in [6] and shown in Figure 3.2., consists of four multiplexers and four delay elements. The pulse position modulated signal corresponding to the parallel input data is serialized in this way and is sent to the receiver along with the main clock. A TDC module is then used to convert the difference between the positive edges of the clock and the delayed clock (PPMed signal) into parallel bits.

Figure 5.1 shows the implemented PPM-based transceiver design, which was implemented in Cadence environment using TSMC 6m nm technology. This design utilizes two PPM modules, where each module is in charge of transmitting 4 bits. As a result, the combination of these modules will transmit 8 bits per clock cycle. Thereby, it achieves a data rate of 10 Gbps, considering that the synthesized clock runs at 1.25 GHz.

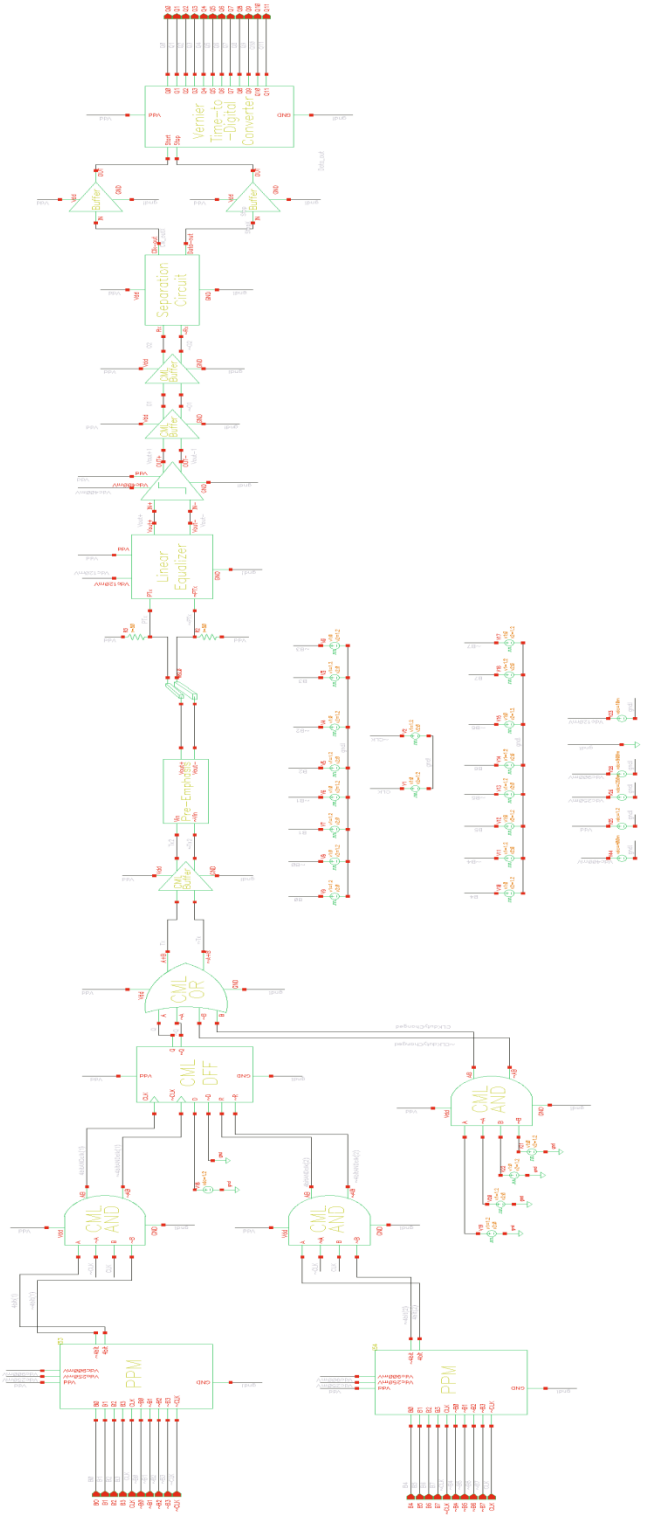

Figure 5.1 - Full PPM-based transceiver.

When both the clock and delayed clock that correspond to the parallel data are transmitted to the receiver, PPM has been used. Consequently, as proposed here, when the difference between the original clock and delayed clock corresponding to the parallel data is transferred to the receiver, DPPM is used. The applications of such data encoding are well known in optical communications systems.

The main motivation for such a proposed system is that in the PPM-based transceiver (see Figure 5.1), additional circuitry is used to embed the clock and the delayed clock together. As well, more circuitry is required to defer the delayed clock, which corresponds to the parallel data, especially so that the embedding process is performed correctly with no pulse coincidence. Moreover, PPM-based transmitters would require additional bandwidth since the data pulses (delayed clock) are supposed to fit together within a reasonable space to avoid inter-symbol interference (ISI).

In this way, by using a DPPM module only the difference between the original clock and the delay clock could be sent. That limited transmission means less circuit complexity, more bandwidth improvement and further minimization of ISI. Additionally, the abundant research in designing pre-emphasis circuits and decision feedback equalization (DFE) could be used for reviving the differential pulse position modulated signal at the transmitter and receiver sides, respectively. Figure 5.2 shows the block diagram of the proposed DPPM-based communication architecture for designing time-mode SerDes.

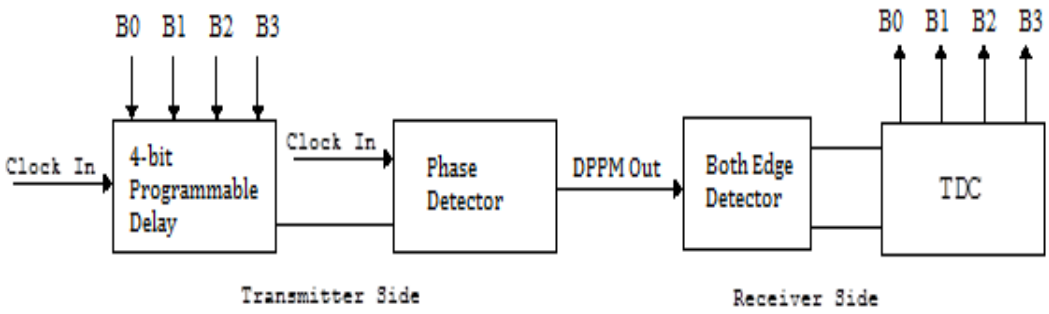

Figure 5.2 - Simplified architecture of the proposed DPPM-based time-mode SerDes.

Figure 5.2 shows that, using the programmable delay designed in Chapter 4, the input clock will be shifted according to the input data bits. Next, the phase difference between the original clock and the shifted clock generated by the 4-bit programmable delay cell will be generated using the phase detector circuit. This signal will be driven off to the receiver. At the receiver side, the positive edge of the DPPM out signal will be extracted using the positive edge detector component of the both-edge detection circuit to be the main clock and used for data recovery. The negative edge of the DPPM out signal will be extracted using the negative edge detector component of the both-edge detection circuit to represent the positive edge of the main data bits. Note that the both-edge detector shown in the proposed architecture, in fact, replaces the separation circuit that was utilized in the conventional PPM-based transceiver, as shown in Figure 5.1. Once these signals are generated, the difference can be digitized using the TDC module. At this stage a decoder needs to be used to translate the TDC output into the parallel data bits.

The complete proposed architecture will now be as shown in Figure 5.3, where the signal revival stages known as pre-emphasis and equalization circuit are also added. The proposed architecture was then implemented using TSMC 65 nm technology using Cadence environment, as shown in Figure 5.4.

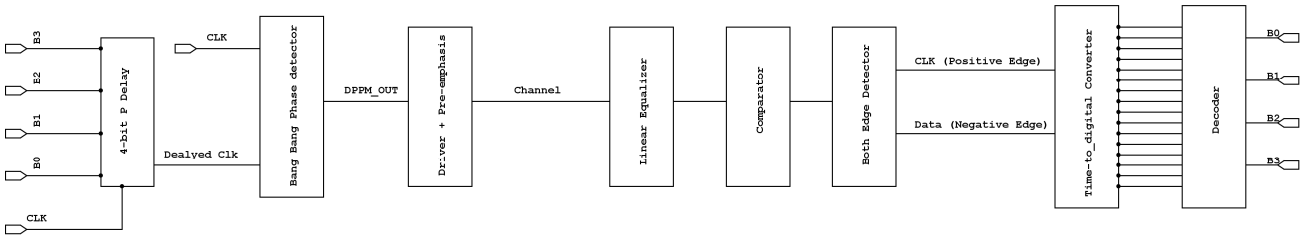

Figure 5.3 - The complete architecture of the proposed DPPM-based SerDes considering signal revival stages.

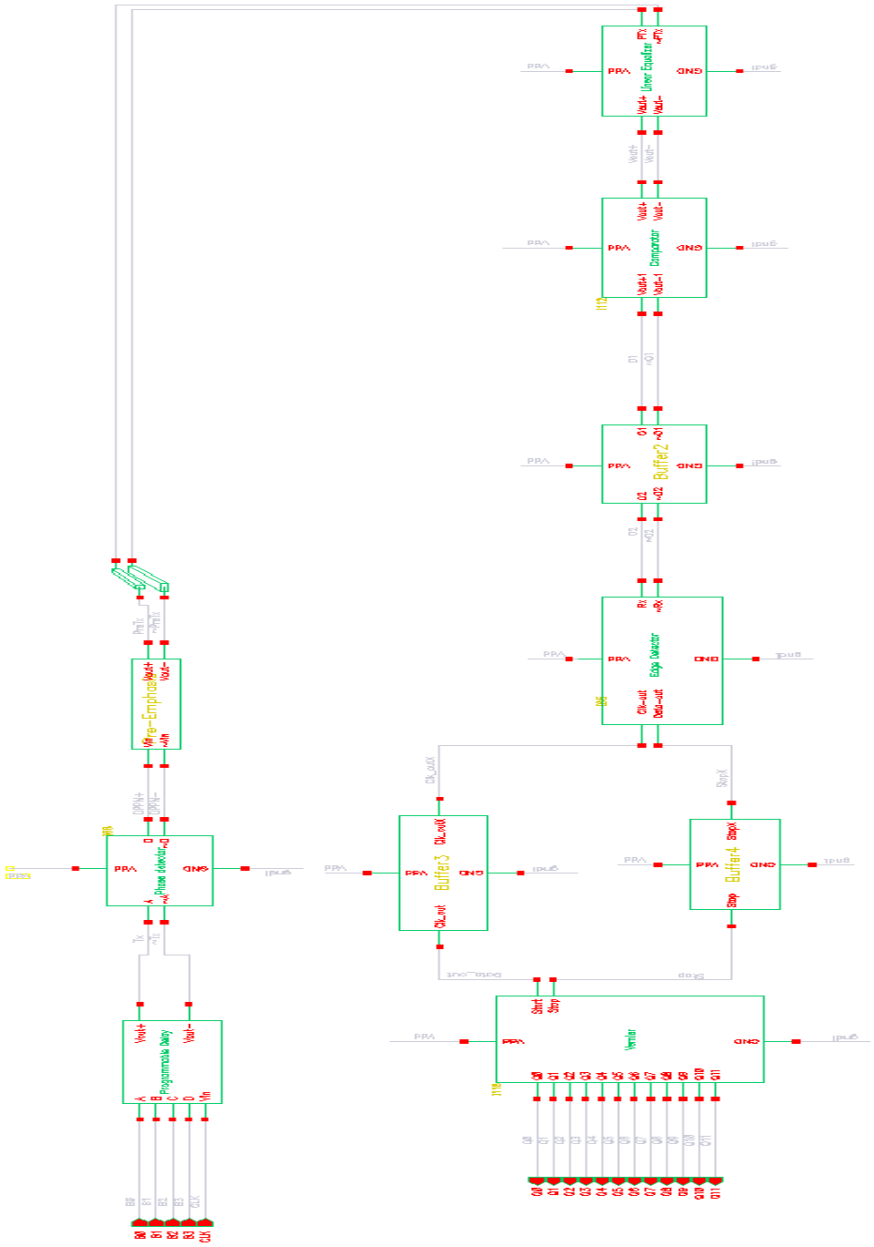

Figure 5.4 - Full DPPM-based transceiver

Figure 5.5 shows the implemented conventional phase detector module in Cadence environment using TSMC 65 nm technology. As mentioned earlier, this module generates the phase difference between the main clock and the delayed clock, which represents the data.

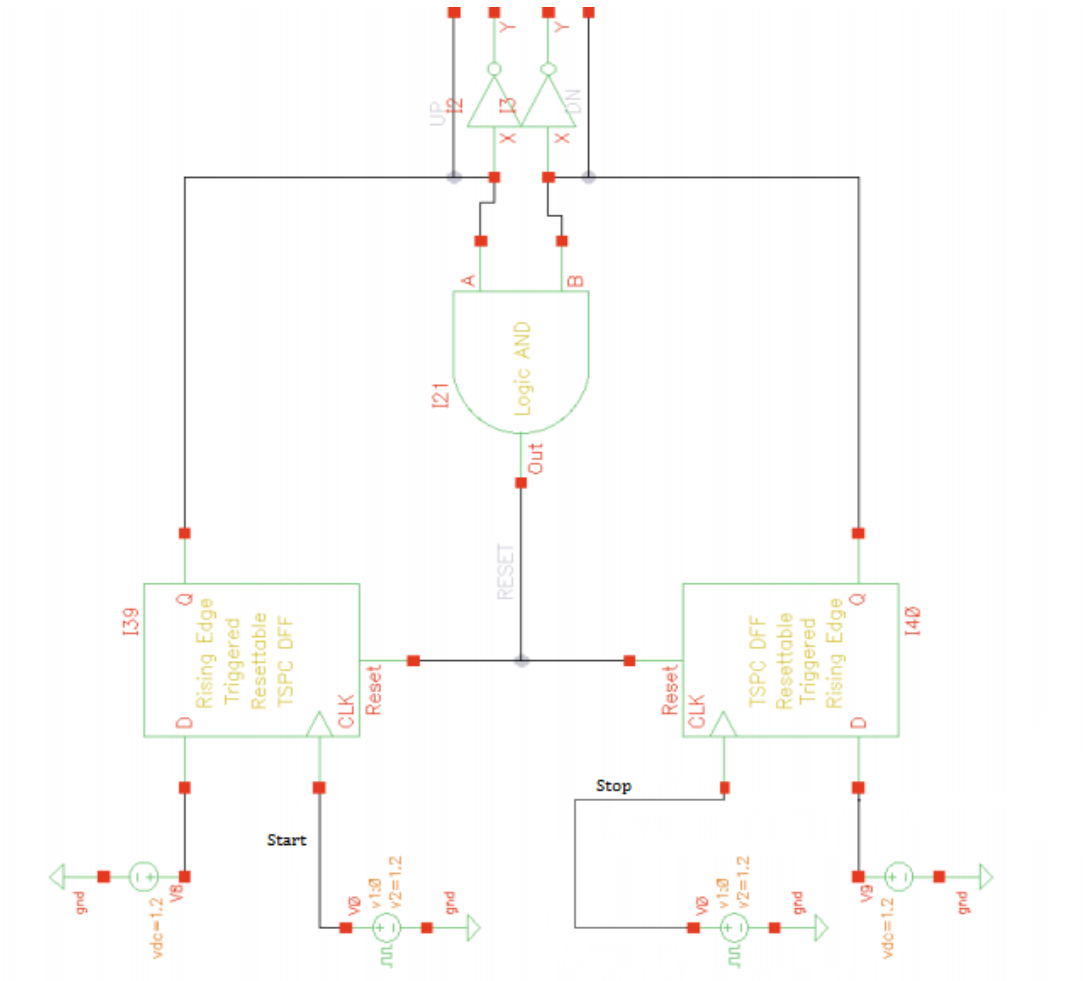

Figure 5.5 - Conventional phase detector module to be used in the time-mode SerDes.

However, we are not limited to using only this type of phase detector. In fact any of the potential phase detector designs investigated in Chapter 2, including bang-bang phase detector (see Figure 2.22), could also be used.

Figure 5.6 shows the implemented circuit of the main driver and the pre-emphasis circuit in Cadence environment. The combination of these modules is used as a signal revival stage at

the transmitter side, where the gain of high frequency components are boosted. Different taps in the design cause the amplitude of the signal to be generated in levels, as shown in Figure 2.3 and discussed in Chapter 2.

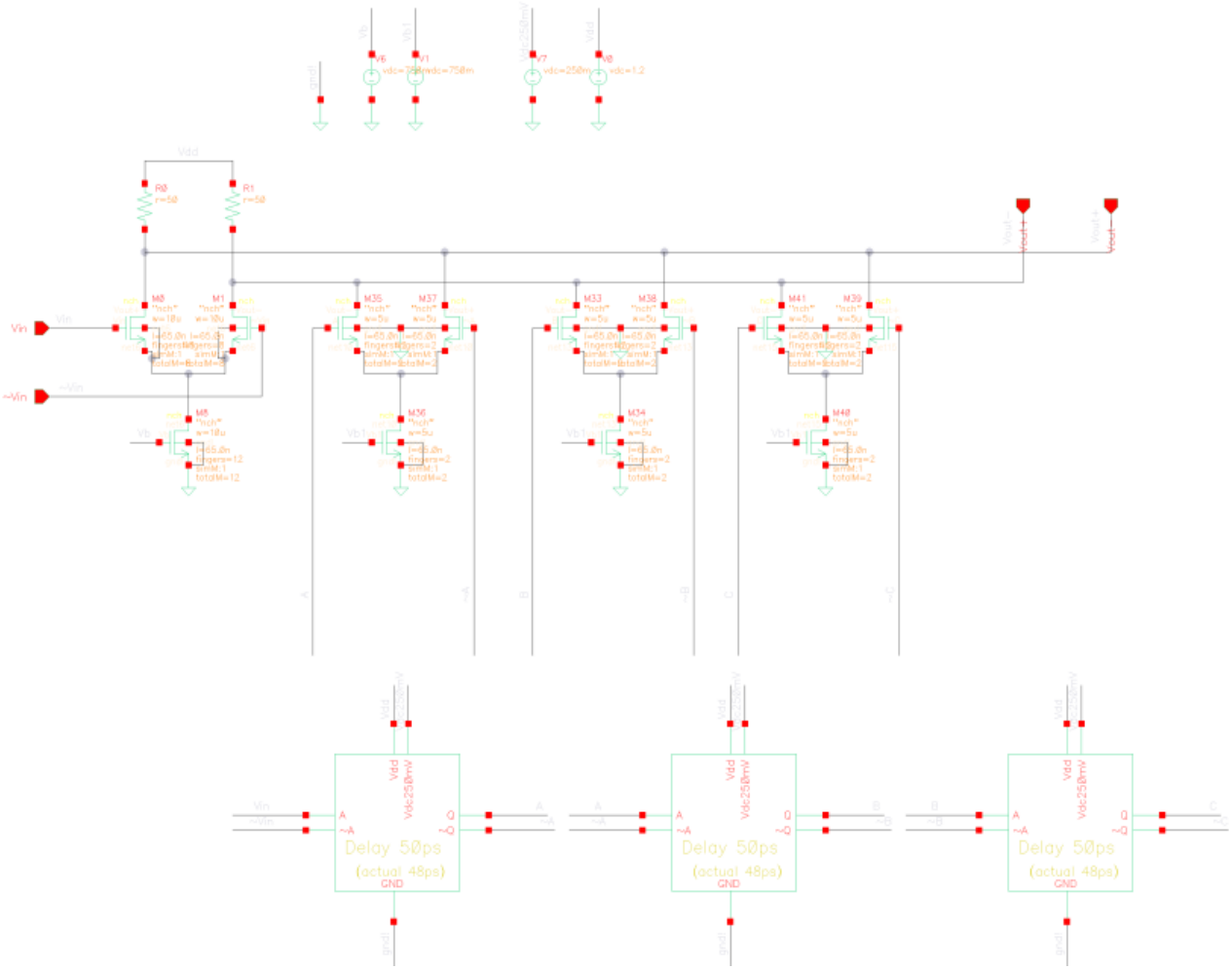

Figure 5.6 - Pre-emphasis circuit implementation.

Figure 5.7 shows the circuit diagram of the implemented 4-stage comparator. This stage is used to fix any shape degradation that may have occurred during the transmission and to ensure the signal has a full dynamic range.

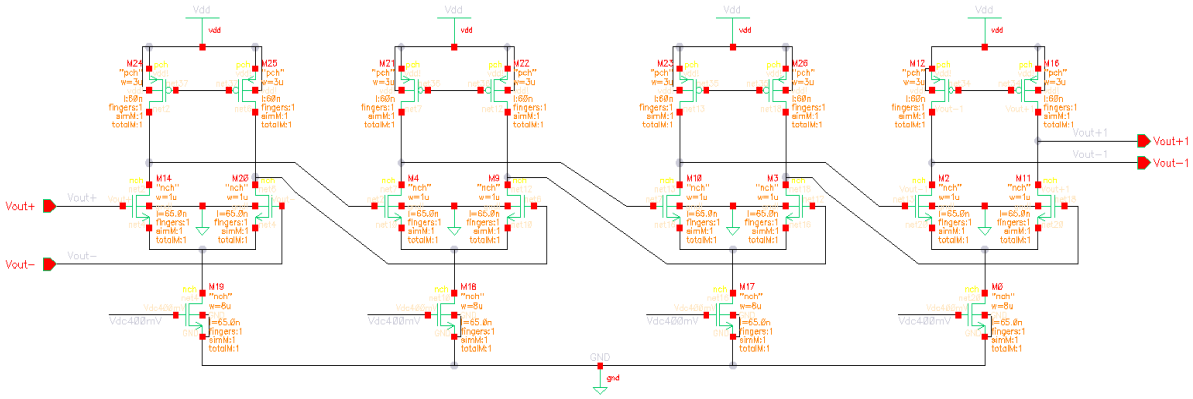

Figure 5.7 - Transistor level circuit of 4-stage comparator.

As mentioned earlier, a linear equalizer is in fact similar to a high-pass filter that amplifies the high frequency components of the signal but does not attenuate the low frequency components as opposed to a high-pass filter. Figure 2.11 shows the transistor level circuit of the utilized equalization circuit. One of the disadvantages of this circuit is that amplifying the high-frequency components of the received signal becomes an issue if the SNR is poor.

Figure 5.8 shows the circuit diagram of the both-edge detection circuit used in this work. This circuit is used to extract both positive and negative edges of the DPPM-treated signal. Figure 5.9 shows this module's operation waveform.

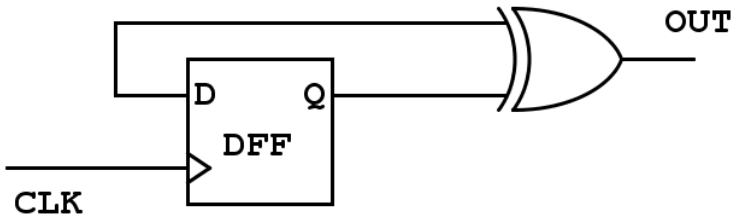

Figure 5.8 - Both-edge detector circuit diagram.

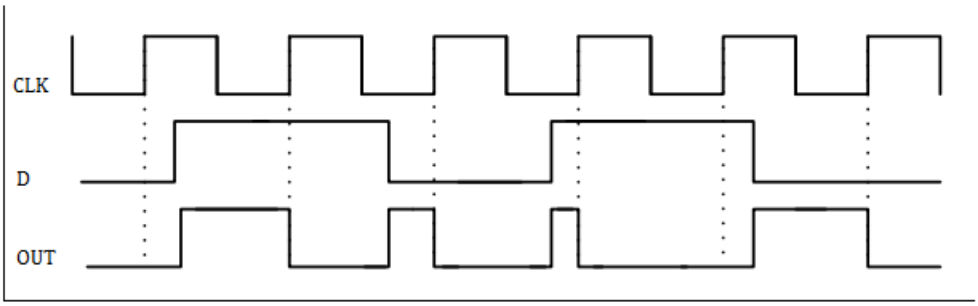

Figure 5.9 - Both-edge detector waveform.

Figure 5.10 shows the circuit diagram of the designed single delay chain TDC module, which is used at the receiver to digitize the difference between the positive edges of the clock and the delayed clock corresponding to the data. The simulation result of this circuit is shown in Figure 6.1.

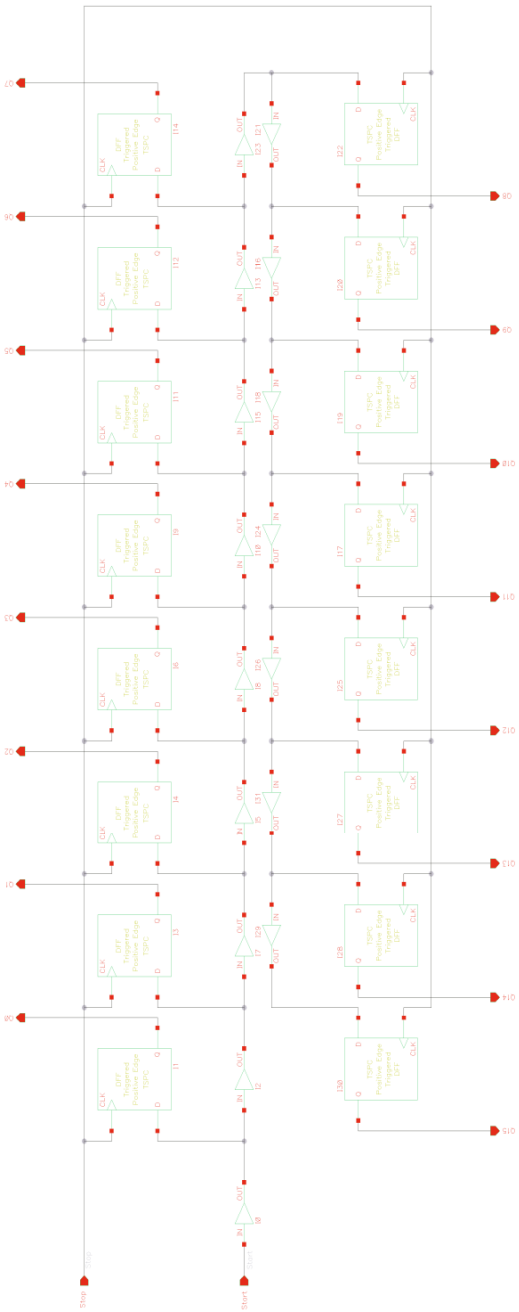

Figure 5.10- Complete circuit of TDC module.

Note that using the proposed DPPM technique will allow the design to achieve the same data rate as the PPM technique. Therefore, using a clock frequency of 1.25 GHz and a programmable delay of 4 bits will result in a 5 Gbps data rate (1.2 GHz 5 * 4 bits). Unlike the PPM-based architecture proposed in [6], there is no need to use two PPM generator modules and double the circuitry in order to increase the data rate. In fact, in the proposed architecture the 4-bit programmable delay needs to be simply replaced by an 8- bit programmable delay, for instance, to achieve a data rate of 10 Gbps (1.25 GHz * 8 bits).

Table 5.1 shows a comparison between the proposed DPPM-based serial link and other serial links in terms of the CMOS technology used, required input clock frequency and the achieved data rate.

Table 5.1 - Comparison between this work and other SerDes links.

Work description	CMOS technology	Input clock frequency	Data rate
This work: Implemented PPM-based SerDes	65 nm	1.25 GHz	10 Gbps
This work: Proposed and Implemented DPPM-based SerDes	65 nm	1.25 GHz	5 Gbps
DTS link [6]	90 nm	500 MHz	3 Gbps
1.25-3.125 Gbps [50]	180 nm	1.25-3.125 GHz	3.125 Gbps
4.8-6.4 Gbps [3]	130 nm	4.8-6.4 GHz	6.4 Gbps
4ch-10.3 Gbps [4]	90 nm	2.575 GHz	10.3 Gbps
ADC-based [51]	65 nm	2.5 GHz	5 Gbps
PAM [52]	180 nm	1.6 GHz	3.2 Gbps
PAM-PWM [9]	180 nm	250 MHz	1 Gbps

Another important concept that needs to be considered is that, in order to achieve the desired data rate as mentioned in the table above, it needs to be ensured that the main clock runs at the correct frequency. It is worth mentioning that the desired clock is not always the system's global clock. Thus, the main clock used for transmission must be synthesized using a frequency

synthesizer as discussed in Chapter 2. Figure 5.11 shows the implemented frequency synthesizer in Cadence environment that generated a clock frequency of 1.25 GHz.

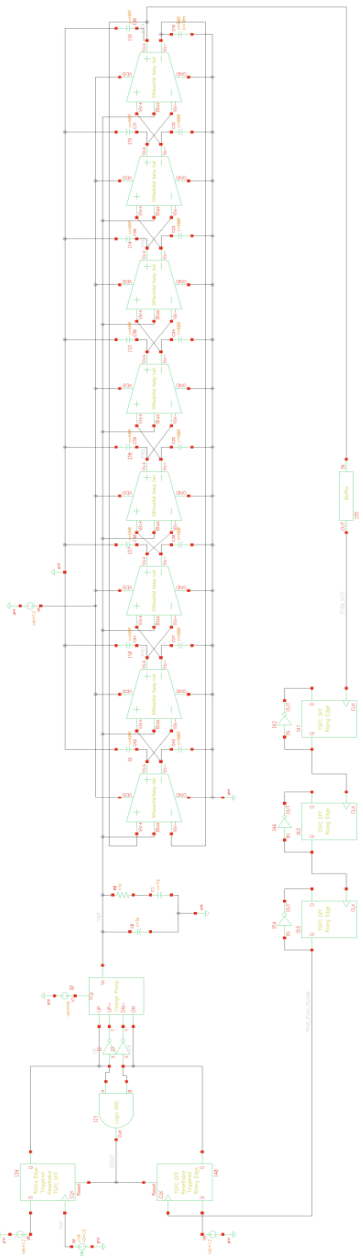

Figure 5.11 - Complete circuit of the frequency synthesizer.

The frequency synthesizer shown in Figure 5.11 and discussed in Chapter 2 consists of a phase detector (see Figure 5.5), a charge pump (see Figure 5.12), a low pass filter, a VCO (which consists of 8 differential delay stages as shown in Figure 5.13), and a frequency divider that can be seen in the feedback loop of the designed frequency synthesizer.

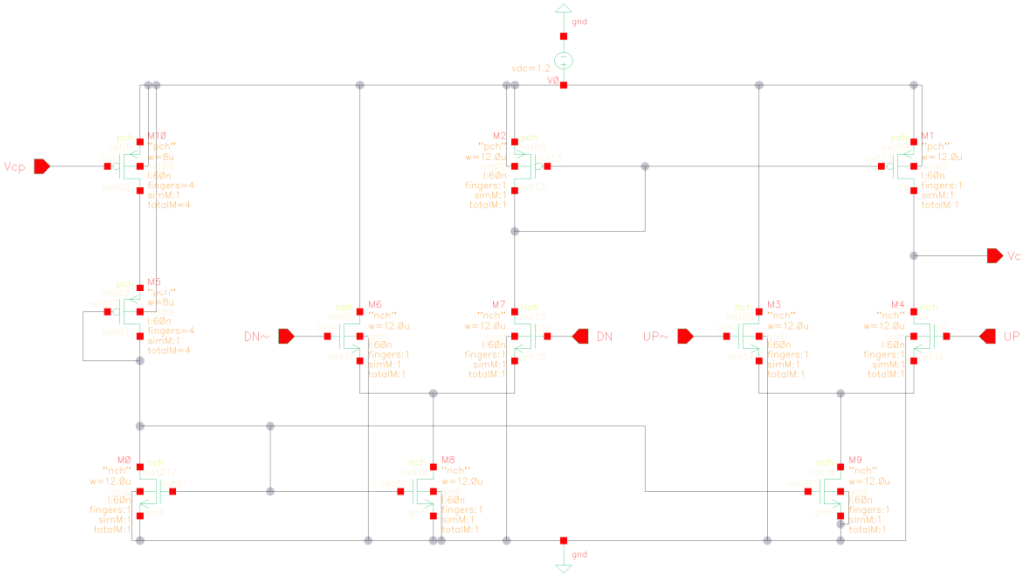

Figure 5.12 - Transistor level circuit of the charge pump circuit used in design of frequency synthesizer.

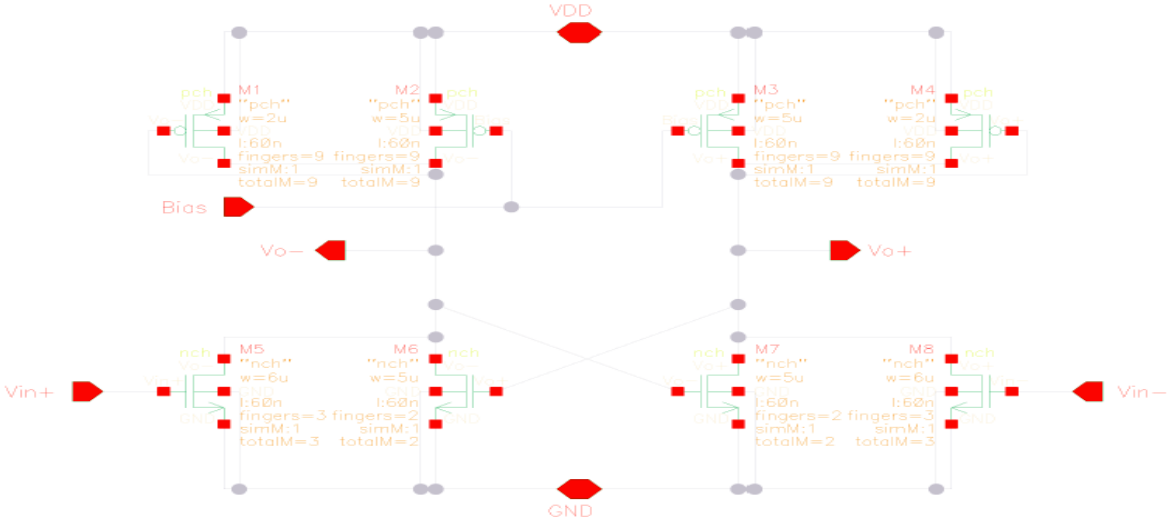

Figure 5.13 - Implemented transistor level circuit of the VCO delay cell used in design of VCO.

Chapter 6: Simulation Results and Observations

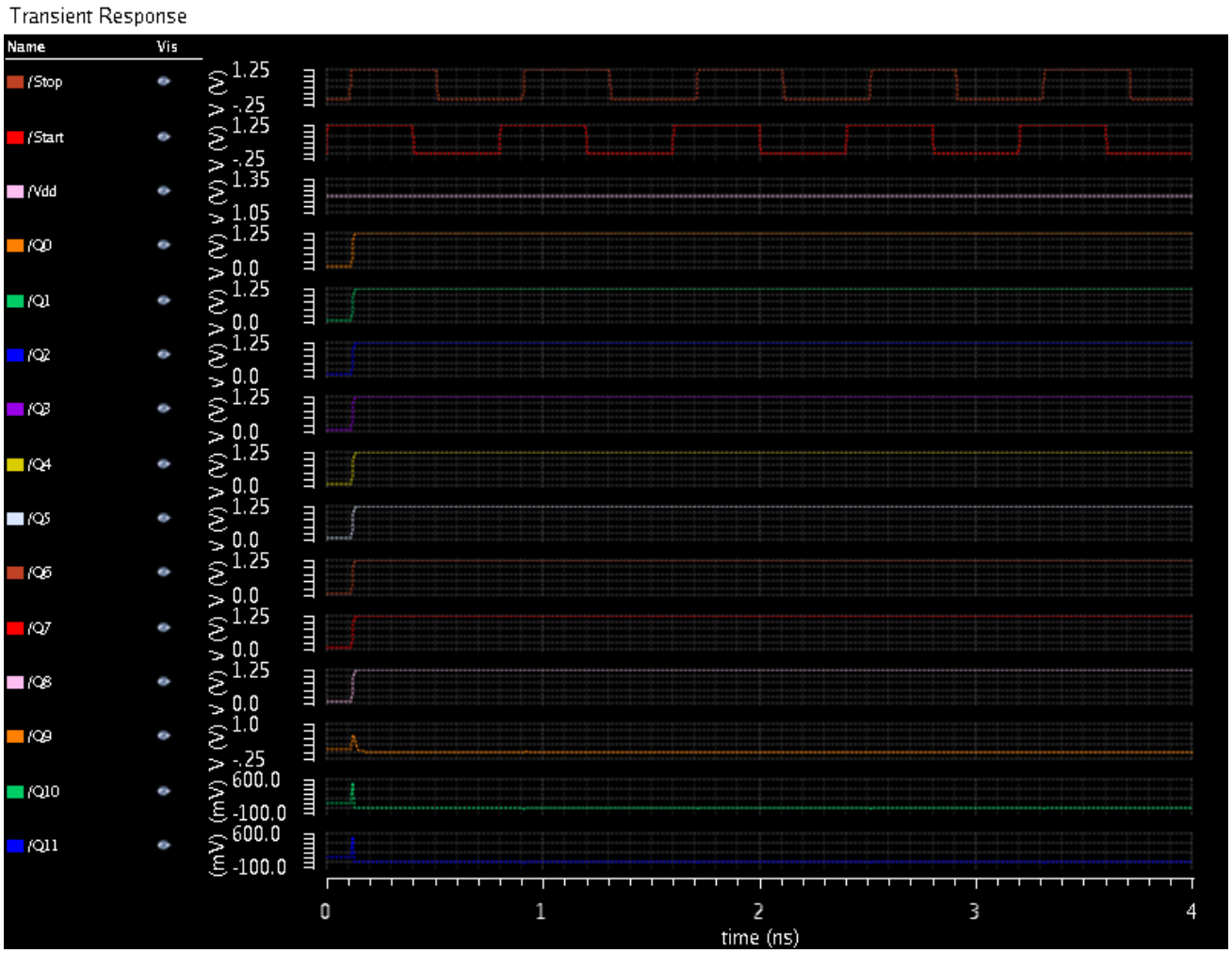

Figure 6.1 - Transient response of the designed TDC module.

Figure 6.1 shows the transient response of the designed single delay chain TDC module used in this work (see Figure 5.8); this module translates the phase difference between the start and stop signals into parallel signals. In a time-mode SerDes the start signal is the main clock

signal, and the stop signal is the signal generated using the 4-bit programmable delay (see Figure 4.2). The difference between these two signals is of interest, where the positive edge corresponds to the input clock and the negative edge corresponds to the information data.

Figure 6.2 is the transient response of the proposed BIST 4-bit programmable delay as shown in Figure 4.4 and discussed in Chapter 4. Note that the test signal corresponds to a test sequence that would check the 4-bit programmable delay. Signals Q0 to Q11 corresponds to the output bits generated by the TDC module to check whether the shifted signal has been delayed correctly or not.

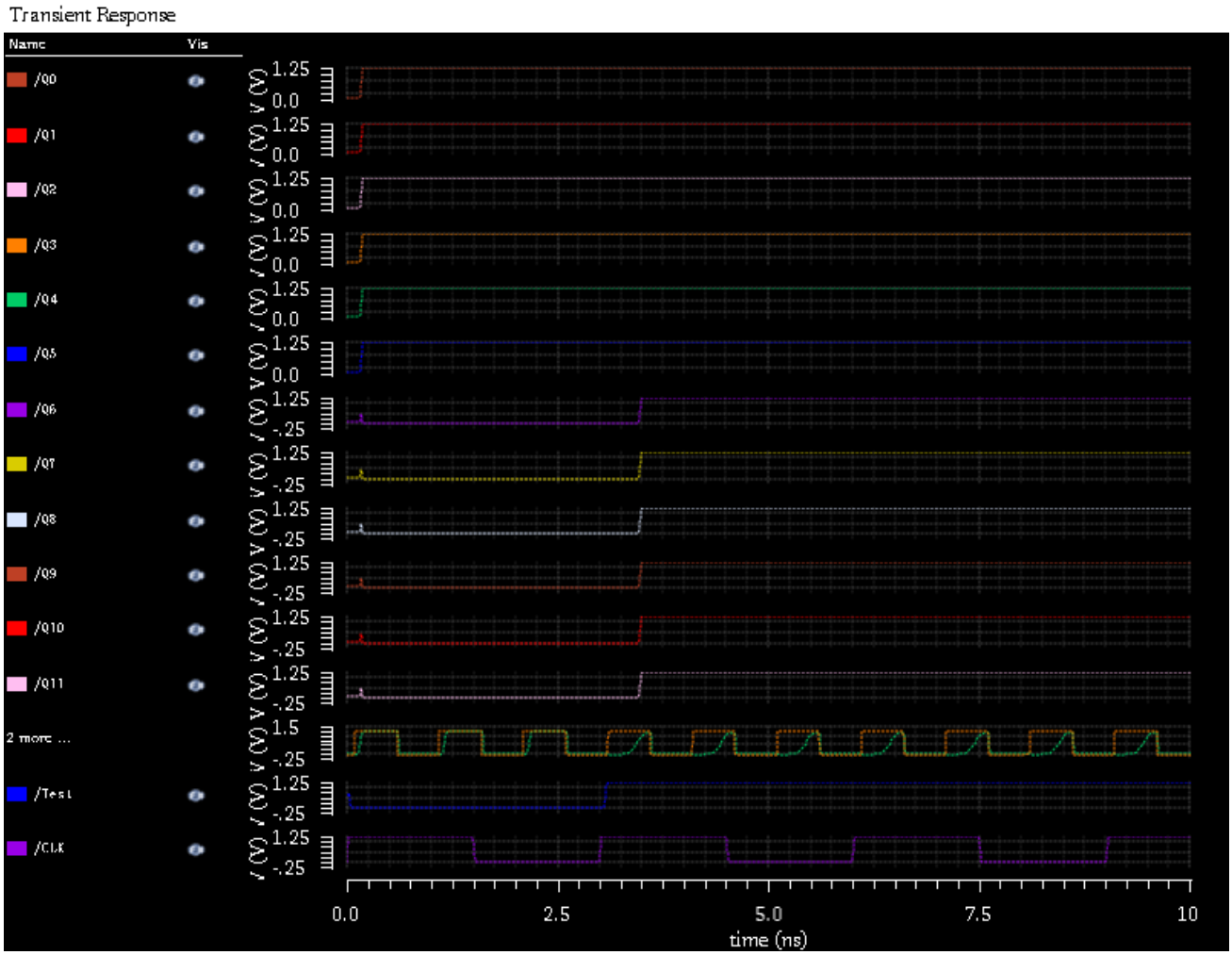

Figure 6.2 - Simulation result of a fault free programmable delay.

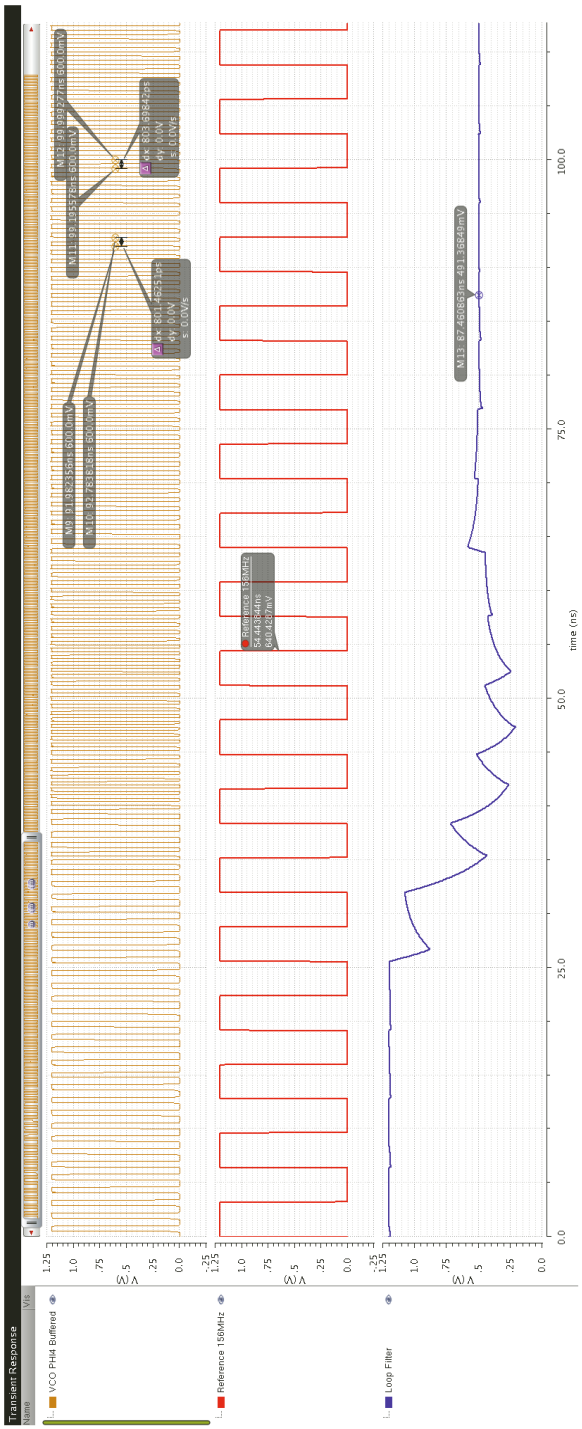

Figure 6.3 - Frequency synthesizer transient response.

As seen in the transient response of the frequency synthesizer shown in Figure 6.3, the lock state is acquired at roughly 80ns. The signal shown in this figure has a free running

frequency of 1.25 GHz, which is suitable to operate as the main clock for either PPM-based or DPPM-based transceivers.

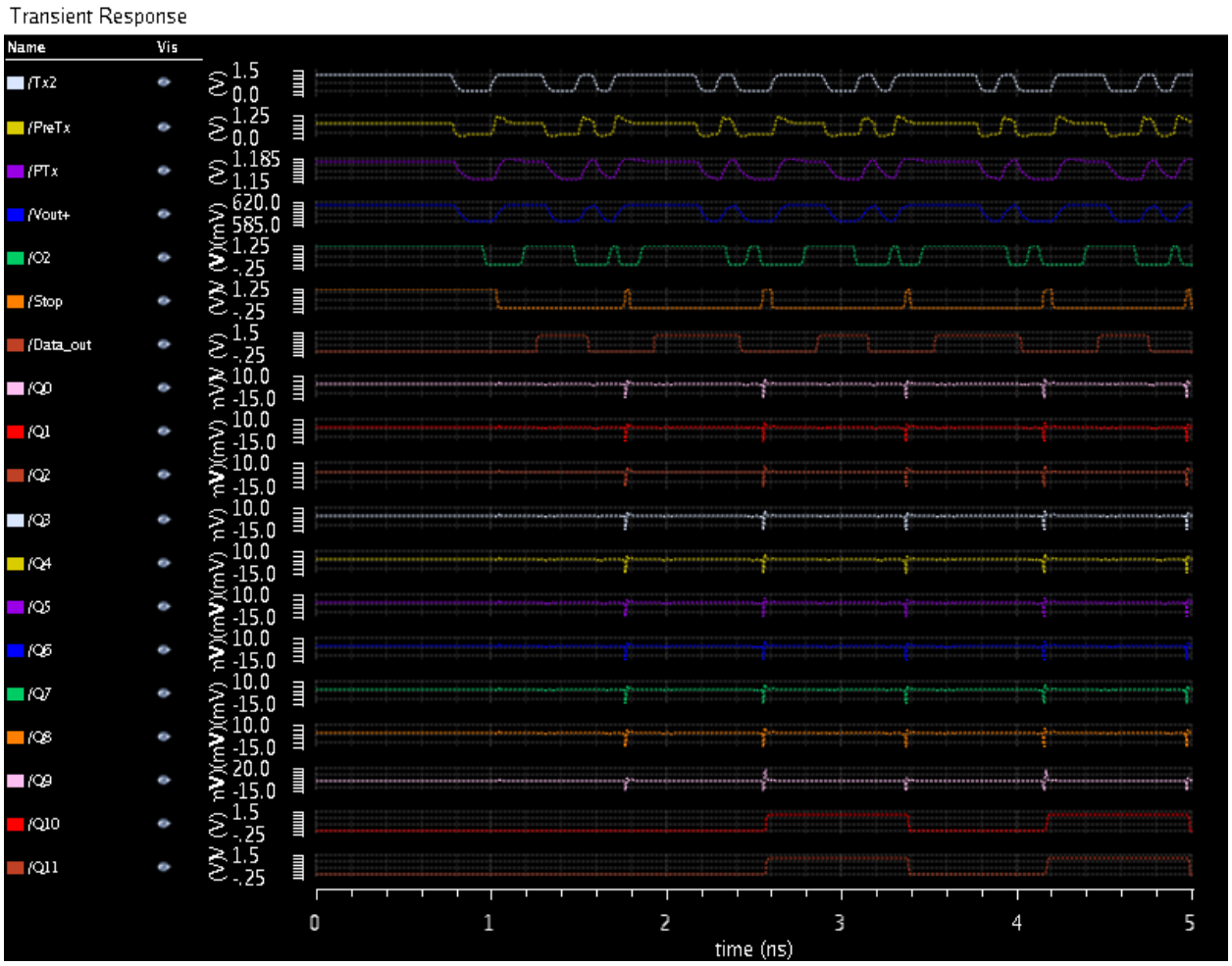

Figure 6.4 - Transient response of the PPM-based transceiver.

Figure 6.4 shows the transient response of the time-mode PPM-based SerDes. As evident from the above figure, the system achieves a data rate of 10 Gbps. The main clock frequency runs at 1.25 GHz while sampling 8 bits at each clock cycle. Tx corresponds to the transmitted signal which contains both the clock and the delayed clock (PPMed data). PreTx refers to the pre-emphasized signal before passing through the channel. PTx is the received signal after the channel. Vout signal refers to the revived signal after the equalization circuit. O2 signal refers to

the signal after the comparator circuit to ensure the signal pulse is shaped properly and reaches its full dynamic range. Stop and Data-out signal refer to the separated signals after the operation of the separation circuit. Q0 to Q11 refer to the output bits generated by the TDC that translated the difference between the stop and Data-out signal.

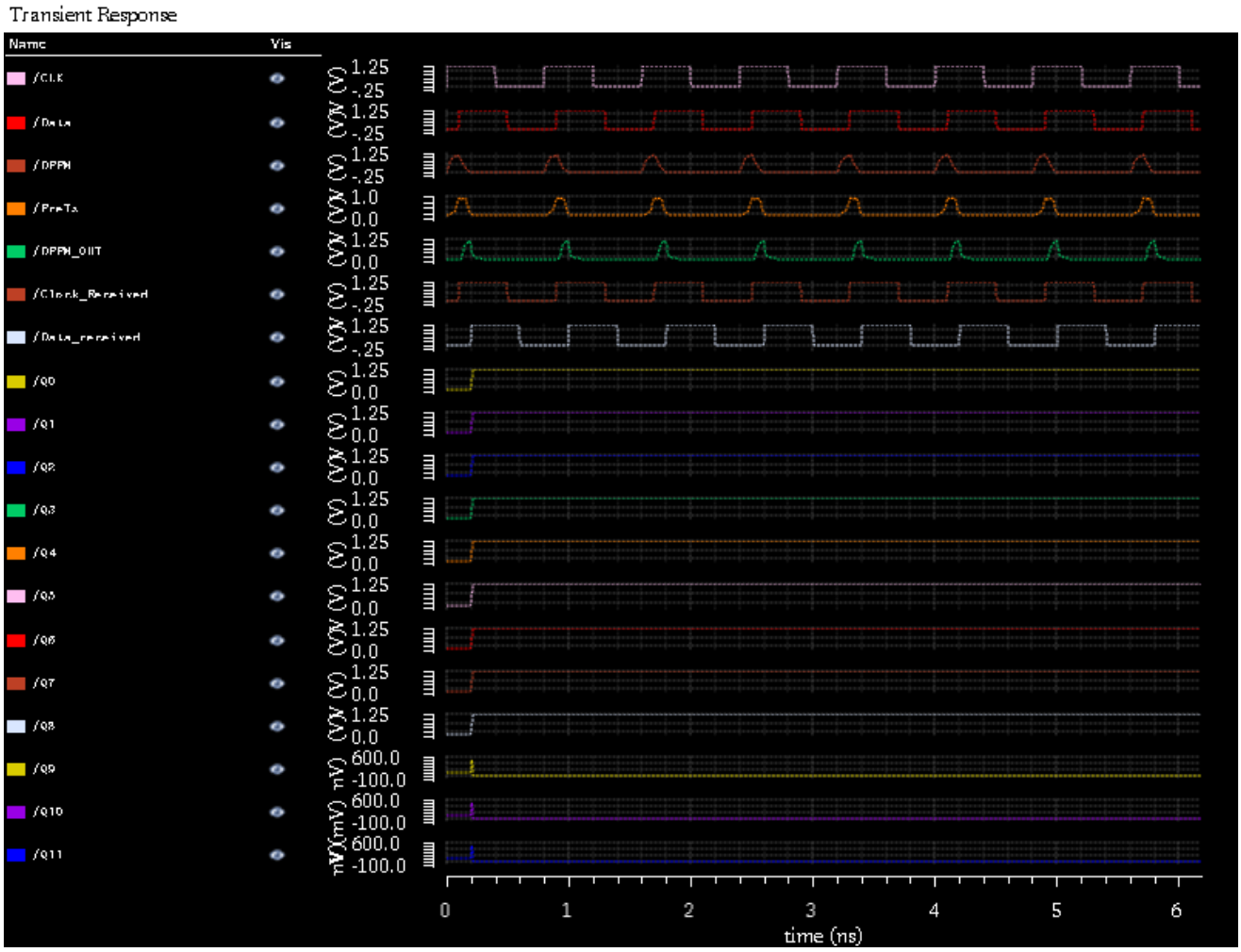

Figure 6.5 - Transient response of the DPPM-based transceiver.

Figure 6.5 shows the transient response of the proposed time-mode DPPM-based SerDes. The main clock frequency of the system runs at 1.25 GHz while sampling 4 bits at each clock cycle; thus a data rate of 5 Gbps is achieved. The data signal indicates that it has been delayed by considering 4 parallel bits. The DPPM signal corresponds to the transmitted signal; i.e. the

difference of the main clock signal and the data signal (delayed clock). PreTx refers to the pre-emphasized DPPM signal, which will be transmitted through the channel. DPPM_OUT signal, on the other hand, is the received signal after the channel; this signal has been shaped by the comparator stage to avoid erroneous demodulation. Additionally, Clock_received and Data_received signals are the extracted clock and data, respectively, generated by the edge detection circuits. Note that the duty cycles of these circuits were generated to be 50 percent. However, we are only interested in the positive edges of these signals since the difference between the positive edges of these signals are the representations of the transmitted data. Moreover, Q0 to Q11 refer to the output bits generated by the TDC that translated the difference between the Clock_received and Data_received signals.

Chapter 7: Conclusions and Future Work

7.1. Thesis Summary

In this work, a thorough study of time-mode serial data links was initially performed. Different components of such circuits were investigated, and different design implementations of such components were researched with an examination of their benefits and drawbacks. Moreover, different factors and phenomena affecting the various performance criteria, such as BER, data rate, power consumption, etc. were investigated. It was also observed how different techniques, such as DFE and pre-emphasis, can mitigate such issues imposed on the signal integrity of a typical SerDes design.

Additionally, in Chapter 4 a new 4-bit BIST programmable delay circuit architecture was proposed that has a testability feature when used in the design of time-mode SerDes. Such circuits proved to be useful for detecting different stuck-at faults as opposed to the conventional multiplexer-based pulse position modulator in a time-mode SerDes design.

Furthermore, in Chapter 5 a complete time-mode SerDes architecture utilizing differential pulse position modulation (DPPM) was proposed that was inspired by the PPM-based architecture. It was employed to tackle the issues of circuit complexity and BW limitations introduced by the conventional PPM-based SerDes architecture.

Different components of such architectures (PPM-based and DPPM-based) were built using the TSMC 65 nm Cadence tools, the results of which showed the correct operation of such circuits. The implemented PPM-based transceiver runs using an input clock of 1.25 GHz, which

achieves a data rate of 10 Gbps, while the proposed DPPM-based architecture achieves a data rate of 5 Gbps using the same clock frequency.

7.2. Summary of Contributions

- Proposed a BIST programmable delay to be used in the design of the transmitter side of a time-mode SerDes for detection of different stuck-at faults, namely, stuck-open and stuck-on.
- Implemented a PPM-based transceiver as proposed in [6] and achieved a data rate of 10 Gbps using a synthesized clock frequency of 1.25 GHz. The system was implemented in Cadence environment using TSMC 65 nm CMOS technology.
- Designed a newly proposed time-mode SerDes using the differential pulse position modulation (DPPM) data encoding technique that achieved a data rate of 5 Gbps using a synthesized clock frequency of 1.25 GHz. The system was implemented in Cadence environment using TSMC 65 nm CMOS technology.

7.3. Future Work

Although the implemented design of both proposed BIST 4-bit programmable delay cell and DPPM-based SerDes showed good results, different possibilities for equalization circuits and TDC modules were not implemented in Cadence simulation tools. In other words, the implemented TDC was chosen to be a single delay chain, while the equalization circuit was chosen to be a linear equalizer. The main reason for this choice was the simplicity of these two modules so that a better test of the proposed circuits could be performed without complicating it with more complex DFE and TDC circuit possibilities. As a result, the focus of future work will be testing the proposed SerDes architecture along with different DFE and TDC circuits for an

empirical study of how much the transceiver parameters, such as speed, data rate, BW, BER and power consumption can be further improved.

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