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Novel Anti-Islanding Detection Method And Maximum Power Tracking Algorithm For Grid Connected Photovoltaic Systems With Interleaved DC/DC Converters

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NOVEL ANTI-ISLANDING DETECTION METHOD AND MAXIMUM POWER TRACKING ALGORITHM FOR GRID CONNECTED PHOTOVOLTAIC SYSTEMS WITH INTERLEAVED DC/DC CONVERTERS

by

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A Dissertation

Presented to Ryerson University

in Partial Fulfillment of the

Requirements for the Degree of

Doctor of Philosophy

in the Program of

Electrical and Computer Engineering

Toronto, Ontario, Canada,2012

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Abstract

Photovoltaic (PV) energy, which has proven to be environmentally friendly and sustainable compared to traditional energy sources, has gained widespread attention in recent years. The grid-tied PV energy conversion system has become a preferred choice for renewable power generation since it does not need energy storage devices. In this dissertation, an advanced state-of-the-art PV energy system is developed. This includes a high-efficiency zero-voltage zero-current switching DC/DC converter with active voltage clamping for power loss minimization, a multiphase interleaved power conversion system with cascade control for power rating expansion, a modified maximum power point tracking (MPPT) scheme with improved accuracy and dynamic response, a novel active frequency drift anti-islanding detection method with grid code compliances, and a laboratory prototype PV energy system for performance evaluation and verification.

Various soft switched DC/DC converters for PV applications are investigated. A new gating scheme for the converter with active voltage clamping that results in zero-voltage and zero-current switching (ZVZCS) is proposed. The operating principles of the proposed converter are presented and its performance is investigated.

To increase the power rating of the PV converters, a multi-channel DC/DC converter system, consisting of multiple units of parallel converters and operating in an interleaved mode, is developed. A new cascade control method is proposed, where the PV array voltage is controlled by a master converter and the active current sharing is implemented by the remaining slave converters. The performance of the new control method under varying temperature and irradiance levels are analyzed and verified by simulation in the Matlab/Simulink platform.

Various MPPT algorithms are investigated and their performance with rapid changes in irradiance and temperature are compared. A detailed simulation of the algorithms is carried out, and an experimental setup is developed.

The islanding phenomenon in renewable energy systems is examined, and an improved active anti-islanding detection method that can detect islanding with less total harmonic distortion compared to the conventional methods is proposed. The rms value and the Fourier series coefficients of the current waveform of the proposed method are obtained and used to derive the operational characteristics of the method.

Acknowledgements

First, and foremost, all the praises and thanks are to Allah Almighty for his persistent bounties and blessings.

I would like to express my deep gratitude to my supervisor, Professor Bin Wu for his invaluable guidance, generous support, and consistent kindness throughout the course of the work. Without his help, this work would not have been completed.

I would like to thank all my friends in LEDAR for their friendly support, whether technical or moral. I am proud to have worked with them and grateful for the help and the company they gave me.

I would like to acknowledge the contribution of the NSERC Solar Buildings Research Network. And the financial support from Professor Bin Wu and Ryerson University are gratefully acknowledged.

Special appreciation goes to my mother for her continuous encouragement and unlimited support. Finally, I would like to thank my wife, Ghinwa, and children, Aya, Alaa, Abdullah and Adib, for their support. Their understanding enabled me to reach my potential and complete my work. My family has been an important part of this life-changing experience.

List of Publications

[1] Yafaoui, A.; Bin Wu; Kouro, S.;, "Improved Active Frequency Drift Anti-islanding Detection Method for Grid Connected Photovoltaic Systems," *Power Electronics, IEEE Transactions on* , vol.27, no.5, pp.2367-2375, May 2012

[2] A. Yafaoui, S. Kouro, and B. Wu, "An improved active frequency drift anti-islanding method with lower total harmonic distortion ," in IEEE Industrial Electronics Conference IECON, Glendale, Az Nov.07-10, 2010.

[3] A. Yafaoui, B. Wu, and R. Cheung, "Photovoltaic energy systems-An overview Part-1," IEEE Canadian review, no. 60, pp. 8-12, Spring 2009.

[4] A. Yafaoui, B. Wu, and R. Cheung, "Photovoltaic energy systems-System control technology part-2," IEEE Canadian Review, no. 61, pp. 14-17, Fall 2009

[5] A. Yafaoui, B. Wu and R. Cheung, " A Novel Method To Reduce The Non-Detection Zone Of Frequency-Drift Islanding Detections," in 3rd Canadian Solar Buildings Conference, Fredericton, 2008.

[6] A. Yafaoui and B. Wu," Review of Maximum Power Point Tracking Algorithms for photovoltaic systems" IEEE International Symposium on Power Electronics for Distributed Generation Systems Hefei, China Aug. 7- 9, 2007

[7]A. Yafaoui, B. Wu and R. Cheung, "Implementation Of Maximum Power Point Tracking Algorithm For Residential Photovoltaic Systems," in 2nd Canadian Solar Buildings Conference, Calgary, 2007,

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Chapter 1
Introduction

1.1 Introduction

The Sun generates $3.8x10^{20}$ MW of electromagnetic energy, some of which reaches us as solar energy. Solar irradiance is the solar power received per unit area; an average of $1.377kW/m^2$ can be measured outside the earth's atmosphere. On a clear sky day, 70% of it ($1kW/m^2$) reaches the earth's surface, which is defined as 1 Sun insolation. Solar energy can be utilized in two forms: thermal solar energy and photovoltaic (PV) energy. PV energy is the electrical energy obtained by converting solar radiation into electricity using photovoltaic cells. The increase in global demand for energy combined with the environmental concern about limited fossil fuels has energized the search for environmentally friendly, renewable energy resources. Photovoltaic energy, which has proven to be environmentally friendly and sustainable compared to traditional energy sources, has gained a lot of attention in recent years.

Canada installed 62MW of PV power in 2009, 197MW of PV power in 2010, and 289MW of PV power in 2011 raising the total capacity to 580MW as of the end of 2011. A major portion of the installed PV power was grid-connected applications, and the rest were off-grid applications. Eighty three percent of the grid-connected applications are large solar farms, while the rest are residential and building integrated systems [1]. Although Canada is in the north, it receives a decent amount of solar energy. The city of Regina (Saskatchewan) receives about 1361 kWh annually for every kW installed power as seen in Figure 1-1. This level of PV energy is comparable to other cities like Sydney (Australia) which receives 1343 kWh/kW and Los Angeles (USA) which receives 1485kWh/kW. This level of solar irradiance combined with a cold climate, which has a positive effect on the performance of solar panels, makes Canada an appropriate place to utilize PV energy.

The boost in demand of PV power has resulted in increases in research to enhance the performance of the PV system. The research and development of PV energy systems has mainly focused on the DC side of the PV systems, where new algorithms have been proposed to increase

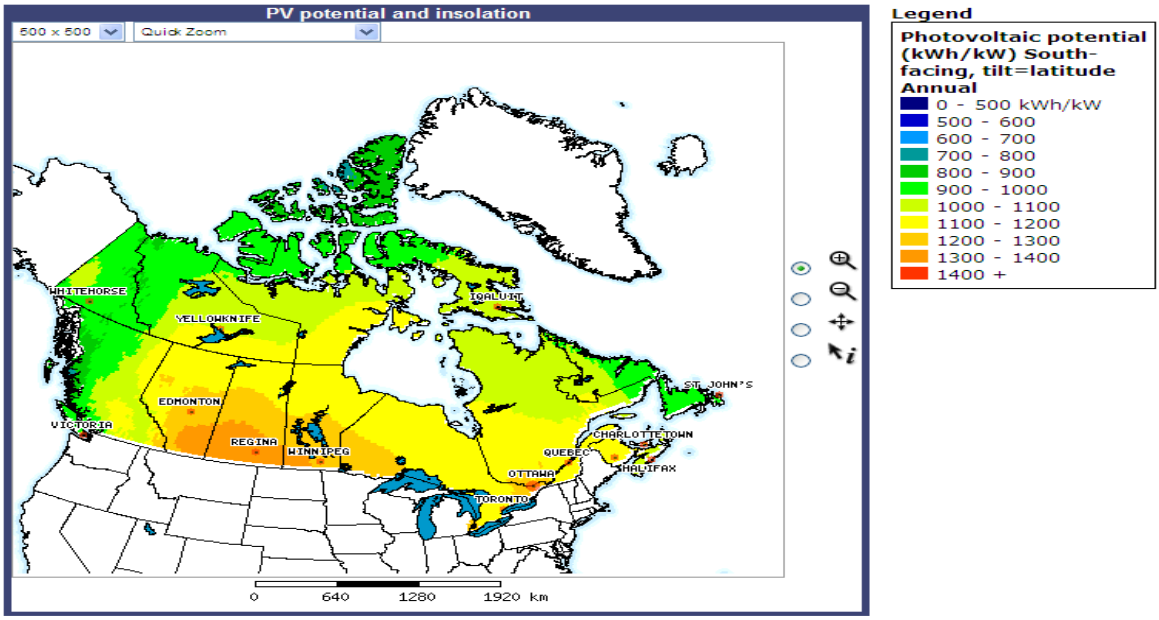

Figure 1-1 Yearly photovoltaic potential map of Canada (Natural Resources Canada).

energy yield and new topologies to increase efficiency. Another point of focus in grid-tied PV systems is the anti-islanding algorithms.

In this dissertation, an enhanced grid-tied photovoltaic energy conversion system is proposed with improved Maximum Power Point Tracking (MPPT) algorithm. A high-efficiency zero-voltage zero-current switching full-bridge DC/DC converter with active voltage clamping is designed to implement the MPPT algorithm. In addition, a novel active frequency drift anti-islanding detection method for grid connected photovoltaic systems is developed.

This chapter begins with the introduction of photovoltaic systems and its types: off-grid and grid-tied photovoltaic systems. The characteristics and electrical model of PV cells are then introduced, followed by an introduction to the types of power converters used in the grid-tied photovoltaic systems. A comprehensive review of maximum power point tracking algorithms is presented. The anti-islanding phenomenon is explained and a variety of methods for anti-islanding detection are discussed. Finally, the objectives of this dissertation are presented.

1.2 Photovoltaic Energy Systems

PV energy conversion systems use solar energy to generate electricity and they can either be off-grid (stand-alone) or grid-connected. A description of both types of PV systems follows.

1.2.1 Off-Grid PV Energy Systems

The off-grid PV systems are usually used in rural or remote areas, where the grid is not available or not accessible. The off-grid systems can be further divided into two sub-categories: domestic and non-domestic applications. In the former, the PV system is used to provide electricity for small communities, where connection to the power grid is not feasible [2]. Usually small PV systems (< 5kW) are used for household applications together with an energy storage unit and a backup system. In the latter, the PV system is used to energize a single industrial or agricultural load that is not connected to the grid, such as a water pump, traffic light, or telecommunication equipment. A battery unit is used to store energy [2, 3].

An off-grid PV energy system consists of a solar array connected to a DC/DC converter, a battery bank and an optional DC/AC inverter as shown in Figure 1-2. The DC/DC converter regulates the battery charging/discharging process and implements MPPT to ensure high efficiency of the system. An optional DC/AC inverter may be connected to the DC bus to energize AC loads, especially when used in domestic applications. The off-grid PV system can be integrated with other energy sources, like a wind energy system or diesel generator, to form a hybrid system with larger capacity and higher reliability [4].

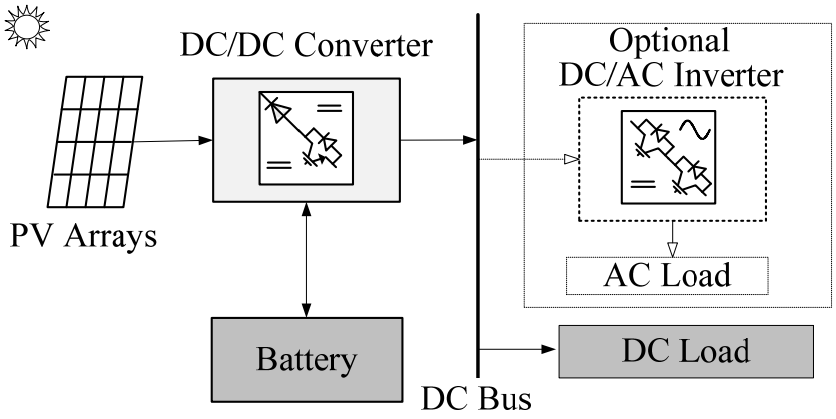

Figure 1-2 Off-grid PV energy conversion system.

1.2.2 Grid-Connected PV System

Grid-connected PV systems are usually composed of three components: a PV array, a DC/DC converter and a DC/AC inverter as illustrated in Figure 1-3. The DC/DC and DC/AC converters are normally referred to as a power converter system, which also includes a digital

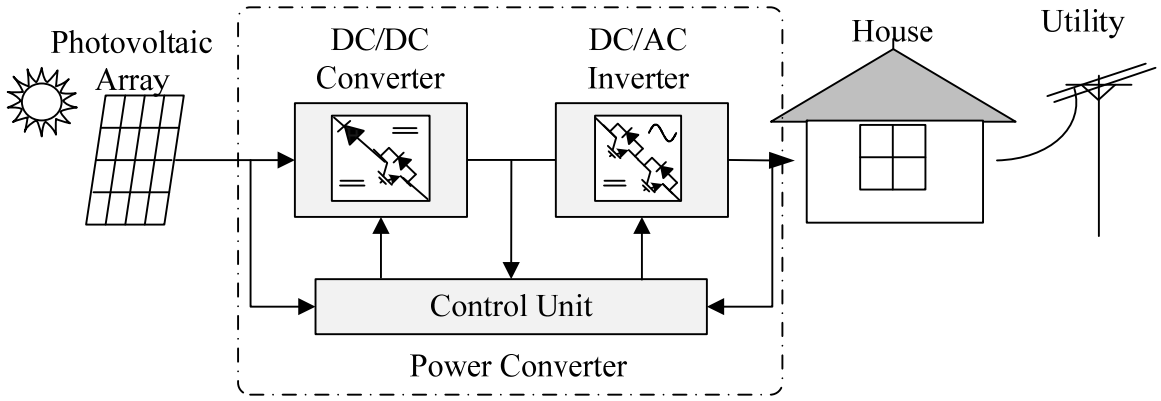

Figure 1-3 Grid-connected PV system.

controller that controls the converter operation and implements the control and protection algorithms [3].

Grid-connected PV systems are also categorized into two main groups: distributed grid-connected applications and centralized grid-connected applications. In distributed applications the PV system is mounted on the premises of a customer who is connected to the grid. The PV system can be connected to the load side of an electricity meter, and the energy generated is used by the customer load. Any energy surplus can be delivered to the grid or vice versa [2, 3]. This method is called Net Metering. Another method to consider is the PV energy system as a distributed generator (DG), which is connected directly to the grid with a separate meter. Centralized grid-connected applications are also known as solar farms, which are large PV systems that act as power stations and are connected directly to the grid [2, 3]. In this dissertation only distributed grid-tied PV energy systems will be discussed.

1.3 PV Arrays

PV arrays are the main and also the most expensive element of the PV energy conversion system. In this section, classifications and modeling of the PV cells are elaborated upon.

1.3.1 Classifications of PV Cells

The first crystalline silicon PV cell was developed at Bell Laboratories in 1954, where solar energy was converted to electricity with an energy efficiency of 6%. The physical construction of the PV cell is similar to that of a diode. When the junction absorbs light, the energy of the

photons is transferred to the material, by creating charge carriers: electrons and holes, as shown in Figure 1-4. Metallic contacts on both sides collect the charges and transfer electrical current. The top contact is made of a thin mesh to let the light pass through. The lower contact is made of a thin conducting foil. Usually the top layer is painted with an anti-reflective coat, and protected by a layer of glass. The PV cells are usually a few square inches in size, and typically produce 1W of power. PV cells are arranged in modules and arrays to generate larger currents and higher voltages. PV cells can be manufactured from different materials:

- Mono-Crystalline Silicone is the most widely available material for PV cells with an efficiency around 16-17%. The slow manufacturing process and high energy yield lead to high prices;
- Poly-Crystalline Silicone is easier to produce but with lower energy efficiency;
- A-Si thin film (Amorphous-silicon) uses much less material, and thus is much cheaper. However its low efficiency (around 6%) makes the price per watt comparable to that of mono-crystalline; and
- CdTe thin film (Cadmium-Tellurium) is the most successful type of thin film PV cells with efficiency reaching around 9%. Mass production has recently been achieved. The use of cadmium (poisonous material) in the production has caused some environmental concerns.

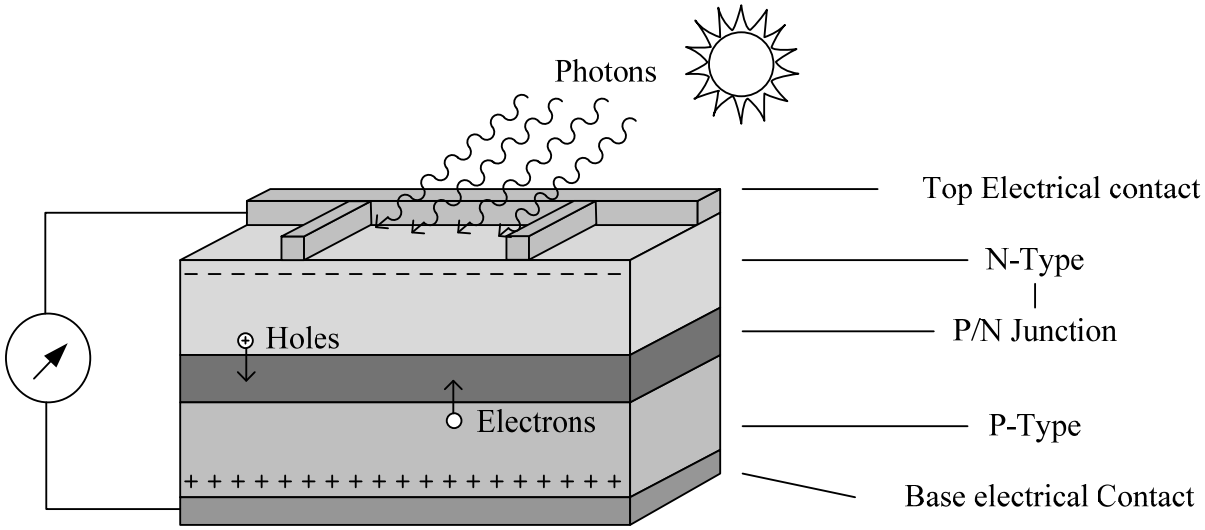

Figure 1-4 Schematic drawing of PV cell.

1.3.2 Electrical Model of PV Cell

The electrical characteristics of the PV cell are non-linear and vary with the environmental conditions. The PV cell can be electrically modeled as a current source with shunt and series resistors as shown in Figure 1-5 [5].

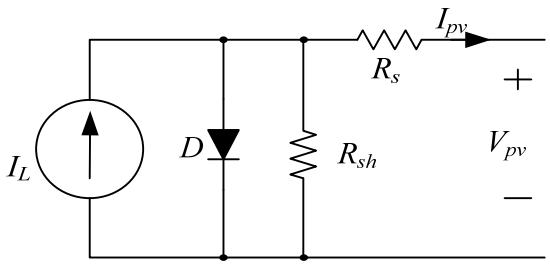

Figure 1-5 One diode PV cell electrical model.

The current-voltage relation of a PV cell can be described by:

$$I_{pv} = I_L - I_o\left[e^{\frac{q\left(V_{pv}+I_{pv}R_s\right)}{nKT}} - 1\right] - \frac{V_{pv}+I_{pv}R_s}{R_{sh}} \tag{1-1}$$

where I_{pv} is output current generated by the PV cell, which is a function of a number of variables defined in Table 1-1.

Table 1-1 PV Cell Parameters for the One Diode Model

Ipv	Cell output current
Vpv	Cell output voltage
R_S	Cell series parasitic resistance
R_{sh}	Cell shunt parasitic resistance
q	Electronic charge: 1.6 x 10^{-19} Coulombs
K	Boltzmann's constant : 1.38 x 10^{-23} J/K
T	Absolute temperature
n	Diode ideality factor : ideally n =1
I_0	Cell reverse saturation current: 10^{-12}A/cm^2
I_L	Cell photocurrent : 35 to 40 mA/cm2/Sun for Si cells

PV arrays are built from PV cells, by connecting them in series and parallel to increase the output voltage and current respectively. The output current depends mainly on the irradiance levels as shown in Figure 1-6, [6]. As the irradiance level changes, the output current of the PV array changes proportionally. The open circuit voltage (voltage at zero current) is not strongly affected by the change in irradiance level and stays relatively constant.

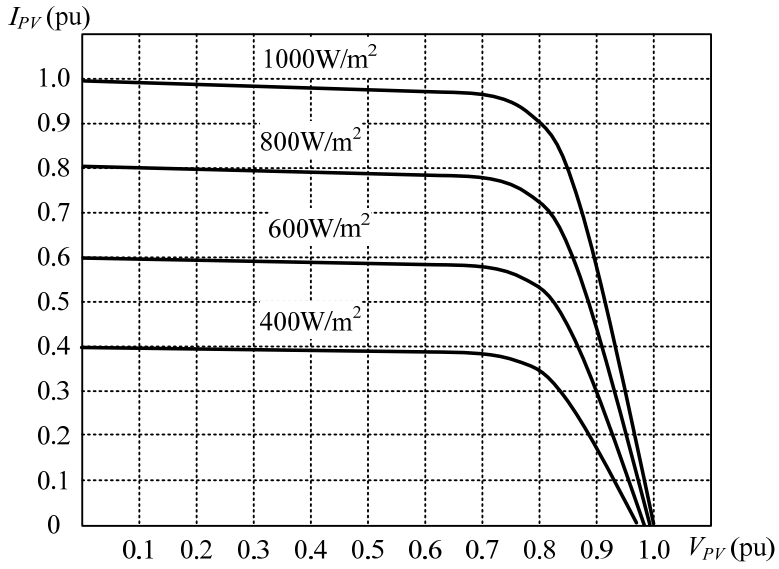

Figure 1-6 PV characteristics at different irradiance levels.

The output voltage of the PV array depends on the temperature, as illustrated in Figure 1-7. The open circuit voltage increases as the temperature decreases. However, the PV array output current remains constant as the temperature changes. At low temperatures, the out voltage increases above the nominal values, thus enhancing the efficiency of the PV array.

The PV array power characteristics are shown in Figure 1-8. These curves are also dependent on the environmental conditions and thus the output power of the PV array. The operating point changes as the PV array characteristics change due to changes in ambient conditions. It also changes as the load changes. To obtain the maximum power from the PV array, the operating point must be at the maximum power points (MPP) of the power curves. This can be achieved by using a DC/DC converter with a maximum power point tracking (MPPT) algorithm.

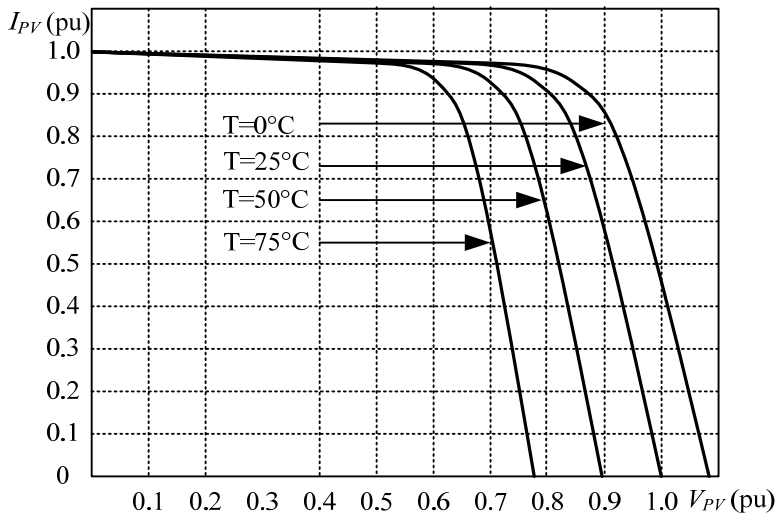

Figure 1-7 PV characteristics at different temperatures.

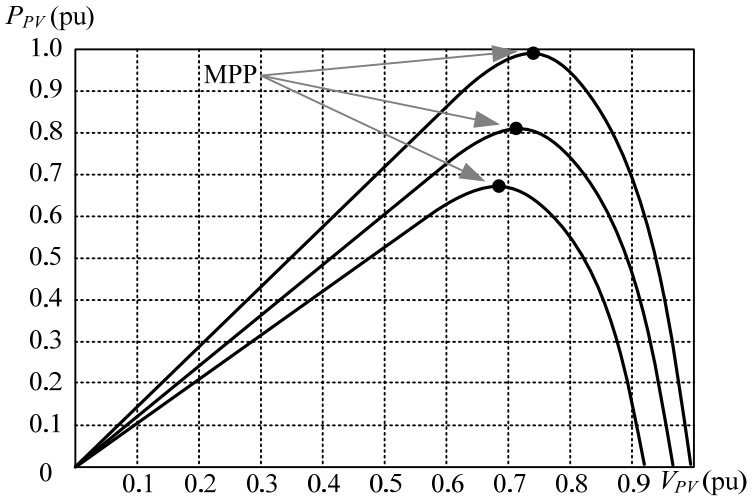

Figure 1-8 Power characteristics of PV array at different irradiances.

1.4 Power Converters

The power converter is the central part of a grid-connected PV system. The main task of the converter is to convert the DC output of the PV array to AC current. As shown in Figure 1-9, this conversion can be done in one or more power conversion stages [7, 8]. The power converter in Figure 1-9(a) is a single-stage power converter, which handles all the tasks such as MPPT, grid current control, and voltage amplification in one stage. Figure 1-9(b) illustrates a dual-stage power converter, where the DC/DC converter performs the MPPT and voltage amplification

while the DC/AC inverter feeds the grid with AC current. Figure 1-9(c) is also a dual-stage power converter but the DC/DC converters are connected to the DC link of a common DC/AC inverter. Each DC/DC converter implements voltage amplification and MPPT and the DC/AC inverter takes care of the grid current control.

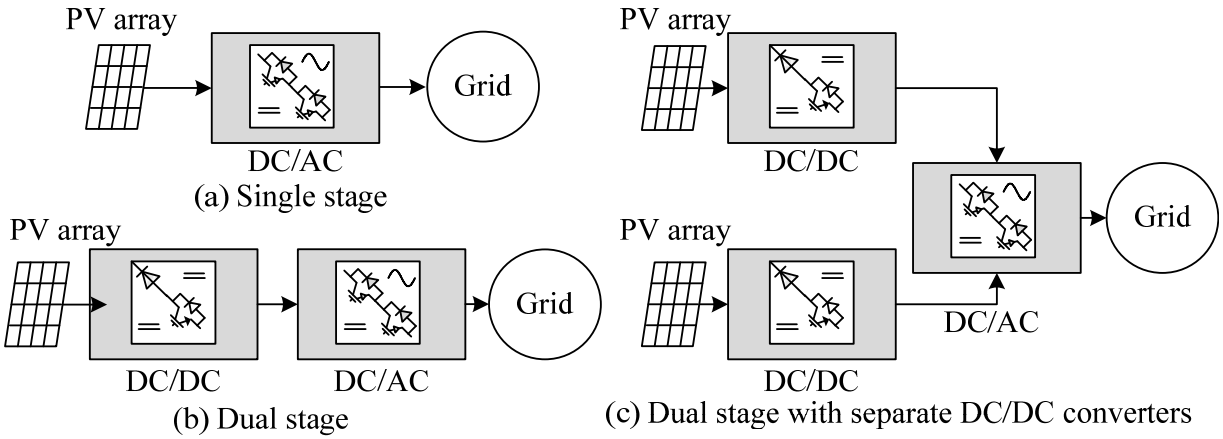

Figure 1-9 Power processing stages.

There are mainly four types of power converters for PV energy conversion: 1) central power converter, 2) string power converter, 3) multi-string power converters, and 4) module integrated or module oriented power converters [9].

1.4.1 Central Power Converters

Figure 1-10 shows a typical configuration of a grid-connected central power converter. PV modules are connected in series to form strings which are connected in parallel to a central power converter [9-11]. The PV energy systems are equipped with self-commutated IGBT technology, controlled by a digital signal processor (DSP) with space vector modulation (SVM). The large power converters can implement grid quality improvements, such as reactive power compensation [12, 13]. An example of central power converter topology is shown in Figure 1-11. The power converter is a three-phase voltage source inverter with a three-phase inductive filter *L*.

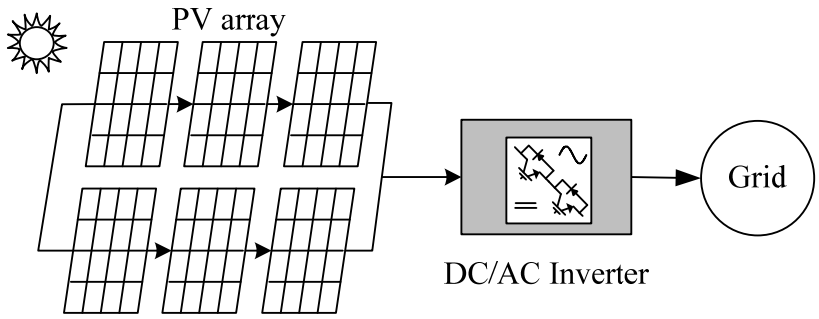

Figure 1-10 Grid-connected central power converter.

Although these power converters are robust, highly efficient and cheap, their energy yield decreases due to a module mismatch and partial shading [9, 14]. In addition, these power converters have the following drawbacks:

- High-voltage DC cables between the PV modules and the power converter;
- Power losses due to a centralized MPPT scheme and mismatch between the PV modules;
- Nonflexible design where the benefits of mass production could not be reached; and
- Limited reliability due to single power converter.

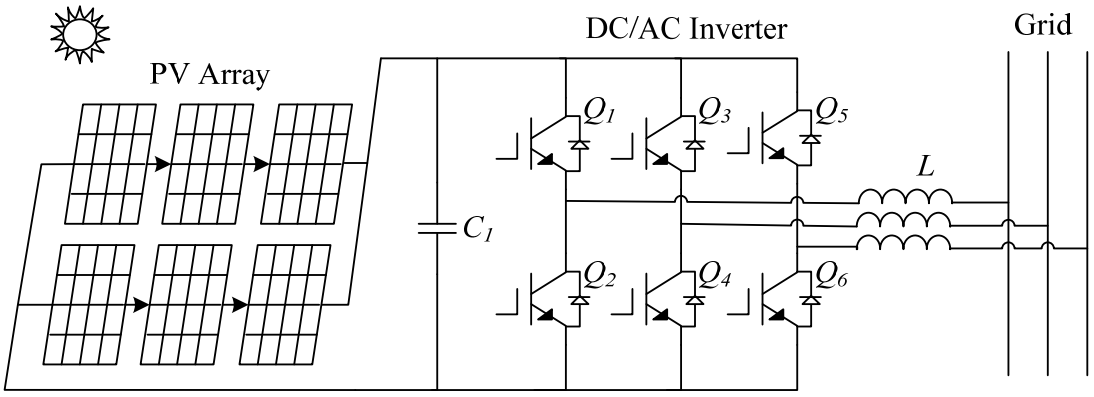

Figure 1-11 Central power converter topology.

1.4.2 String Power Converters

String power converters are reduced versions of the central power converter. In string power converters, the PV panels are divided into several parallel strings. Each of them is connected to a dedicated power converter which implements MPPT independently, as shown in Figure 1-12 [8, 9, 11-15]. This technology results in a 1% to 3% increase in energy yield compared to the central power converter due to the reduction in mismatch and partial shading losses. Eventually it became a standard in PV system technology for grid-connected applications [9, 10, 13, 14]. Figure 1-13 shows an example of a string power converter with two stage conversion. In the first stage, the DC voltage is boosted and converted to a semi-sinusoidal waveform, which is unfolded in the next converter at the line frequency.

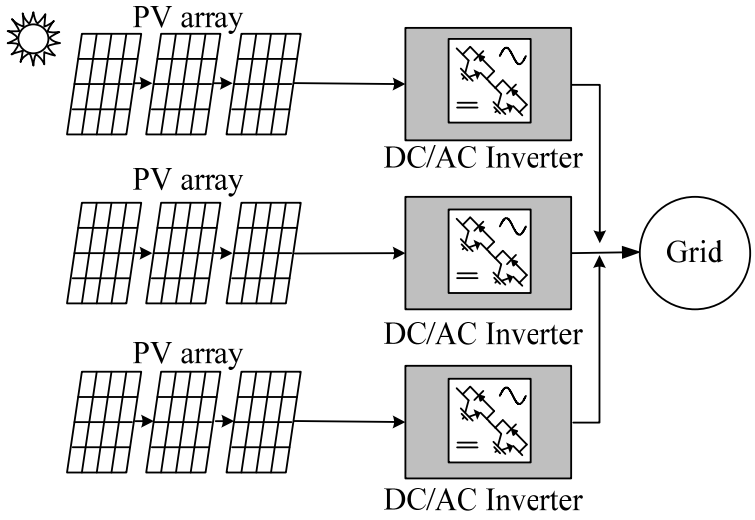

Figure 1-12 Grid-connected string power converters.

1.4.3 Multi-String Power Converters

In multi-string power converters, each PV string is connected to a separate DC/DC converter that implements its own MPPT, and the output is fed to a DC bus that feeds a central DC/AC inverter, as in the example shown in Figure 1-14. This configuration enables the use of different PV modules with different technologies (e.g., crystalline or thin film) and orientations (e.g., south, east and west) in the same PV plant [8]. This power converter combines the advantages of string power converter (high energy yield) and central power converter (low cost) [12, 14, 16-18].

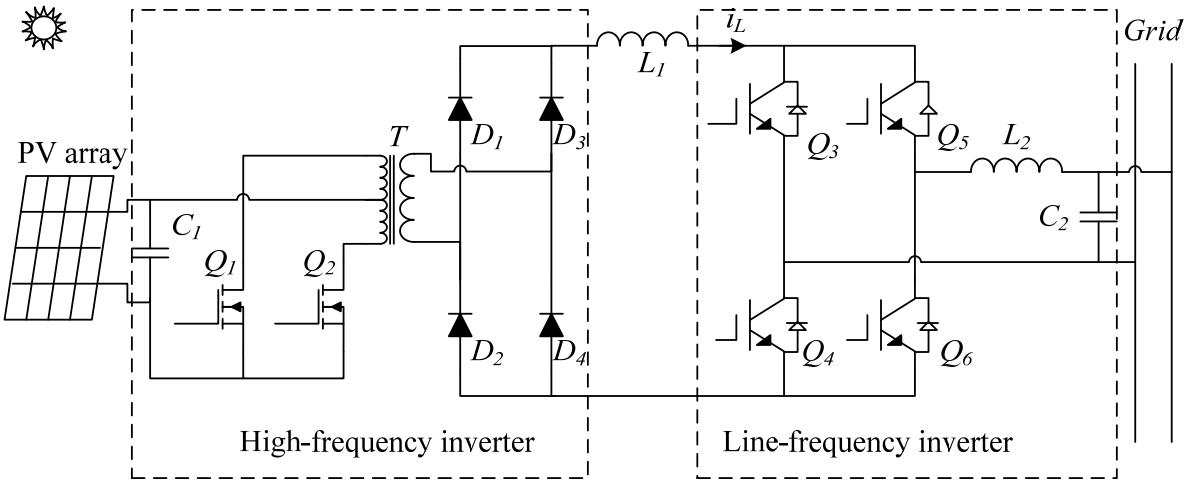

Figure 1-13 A Two-stage string power converter.

The modular nature of this power converter makes it more flexible and more robust, since the failure of one string does not affect the operation of the other converters [16]. An example of a multi-string power converter is shown in Figure 1-15, where full-bridge DC/DC converters are interfaced to a single three-phase inverter through a DC bus.

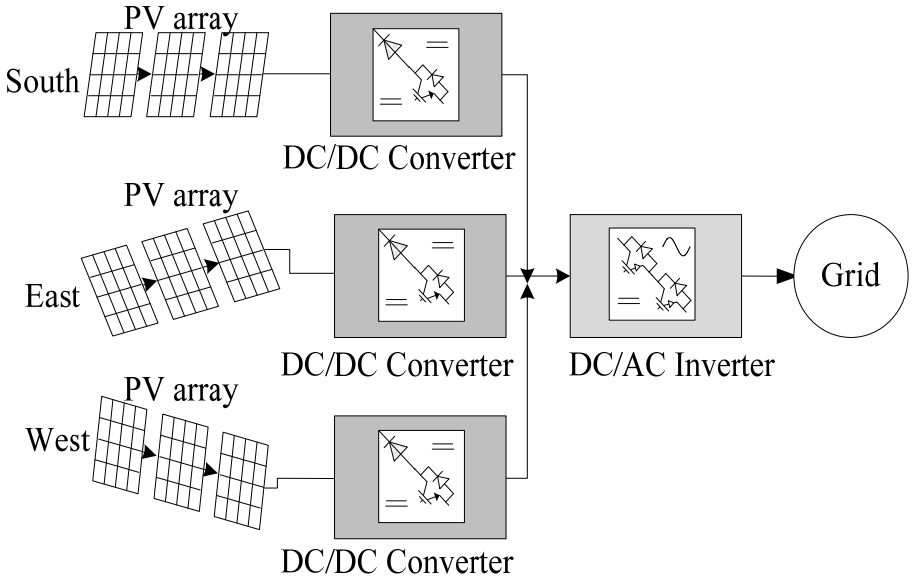

Figure 1-14 Grid-connected multi-string power converter.

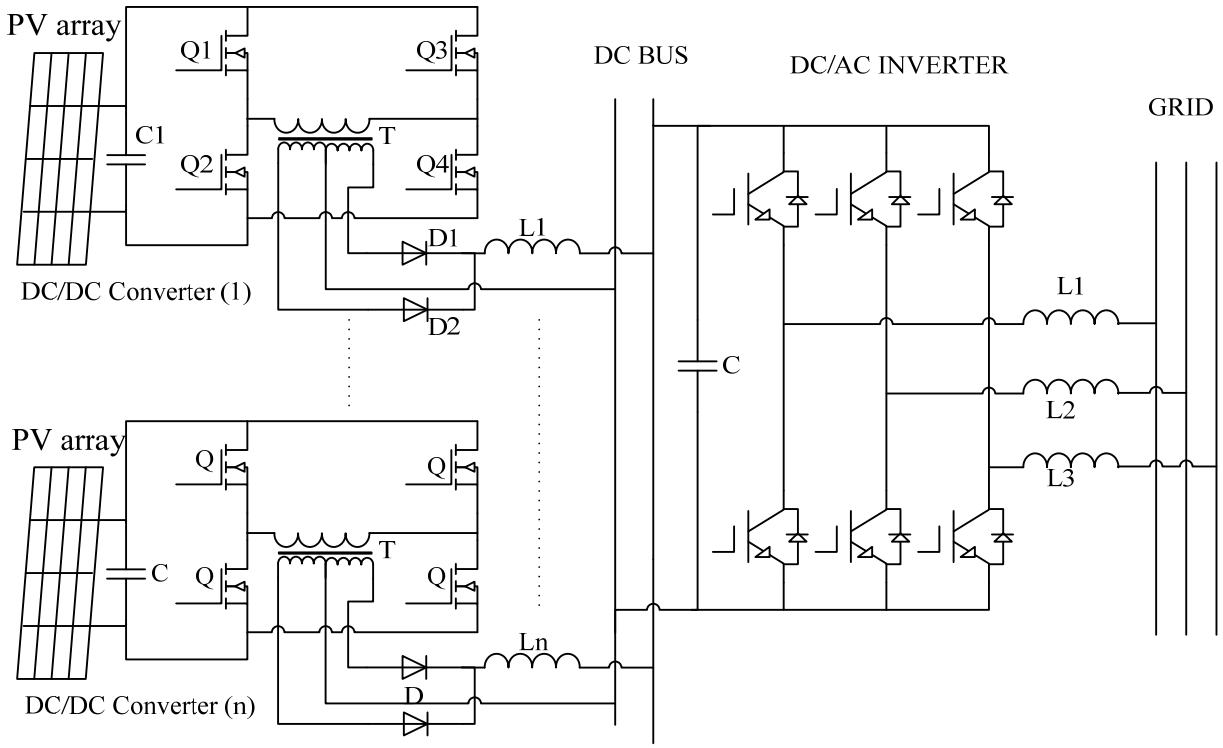

Figure 1-15 A Multi-string power converters.

1.4.4 Module Integrated Power Converters

Module integrated power converters, or AC modules, consist of a PV module connected to a power converter to form a single electrical device as illustrated in Figure 1-16 [8-10]. They are usually rated below 500W and paralleled together to form a PV plant [12, 13]. This results in the highest system flexibility and highest energy yield, since each PV module has its own MPPT and the mismatch losses are eliminated [9, 10, 14]. Although this type of power converter has some advantages, such as no DC wiring and the availability of a complete PV system at low investment cost, it has some significant drawbacks, such as low efficiency due to voltage amplification and high cost per watt [8-13]. Nevertheless, it is seen as the future trend in PV systems [19]. Another example of module integrated power converter is shown in Figure 1-17. In this system, a flyback converter generates a rectified sine wave which is unfolded in the second converter.

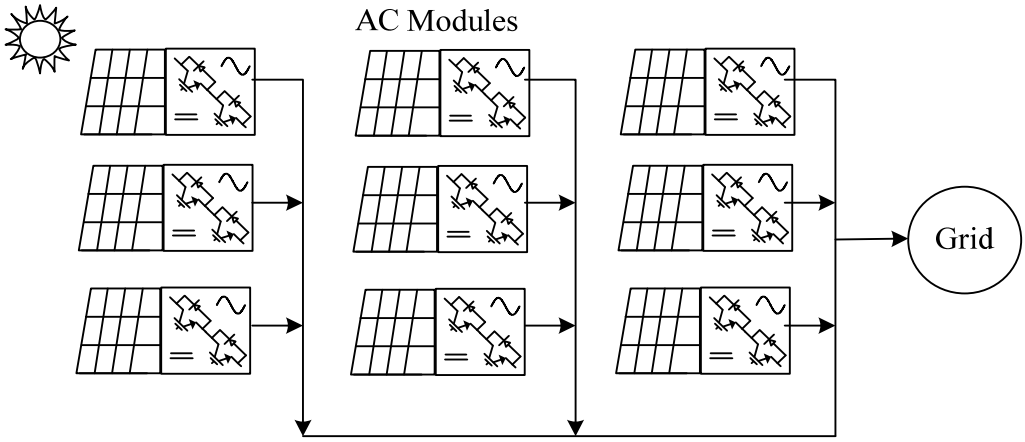

Figure 1-16 Grid-connected module integrated power converter system.

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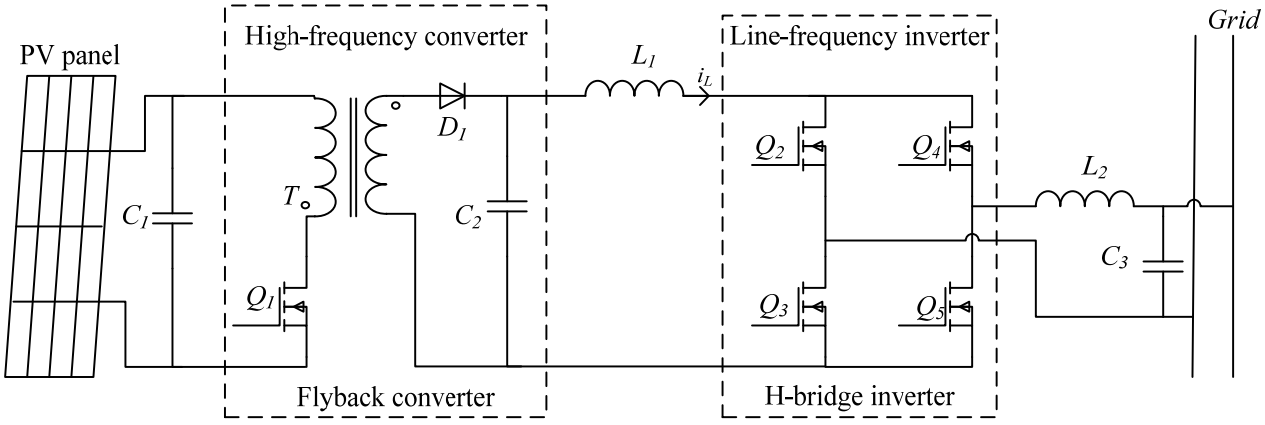


Figure 1-17 AC module in a module integrated power converter.

Table 1-2 gives a summary of the characteristics, main advantages and disadvantages of the above-mentioned power converter types. The central power converter has the lowest cost per watt but it has a poor energy yield due to a mismatch between the PV panels. The AC module power converter has the best energy yield since each PV panel has its own MPPT, but this results in the highest cost per watt. The string power converter is a compromise between these two power converters, and the multi-string is the new trend in industry for residential and small commercial applications.

Table 1-2 Summary of Power Converter Topologies

Power converter Type	Input voltage	Power range	Cost/W	advantages	Disadvantages
Central Power converter	150-750V	20kW-400kW	low	Low cost, high efficiency	Mismatch losses, low energy yield
String Power converter	150-450V	1kW-2kW	Med	Separate MPPT	NA
Multi String Power converter	125-750V	1kW-10kW	Med	Separate MPPT, high efficiency	NA
AC Module	30-150V	<500W	High	No DC wiring, high energy yield	high cost/Watt

1.5 Maximum Power Point Tracking Algorithms

The maximum power point tracking (MPPT) control of the PV system is critical for the success of a PV system since it determines the maximum amount of energy that can be delivered to the grid by the PV power converters. The MPPT algorithms range from simple hill-climbing algorithms to fuzzy logic and neural network algorithms. The most commonly used algorithms are presented in the following subsections.

1.5.1 Hill Climbing (Perturb and Observe) Algorithm

The hill climbing (perturb and observe) algorithm is the most popular method used in practice [6, 20]. Its popularity is due to the simplicity of implementation. It has been extensively studied and there are many versions with minor discrepancies [21-24]. It is an iterative process to reach the maximum power point. The operating point is perturbed and then the system response is measured to determine the direction of the next perturbation. From Figure 1-8, we can observe that increasing the PV voltage, while in the left hand side of the MPP, increases the PV output power. On the contrary, in the right hand side of the curve, decreasing the voltage increases the power. So after a perturbation, if the power increases the subsequent perturbation will continue in the same direction. If the power decreases then the direction is reversed. The hill climbing method is therefore also referred to as the Perturb and Observe (P&O) method. This algorithm is summarized in a flowchart in Figure 1-18.

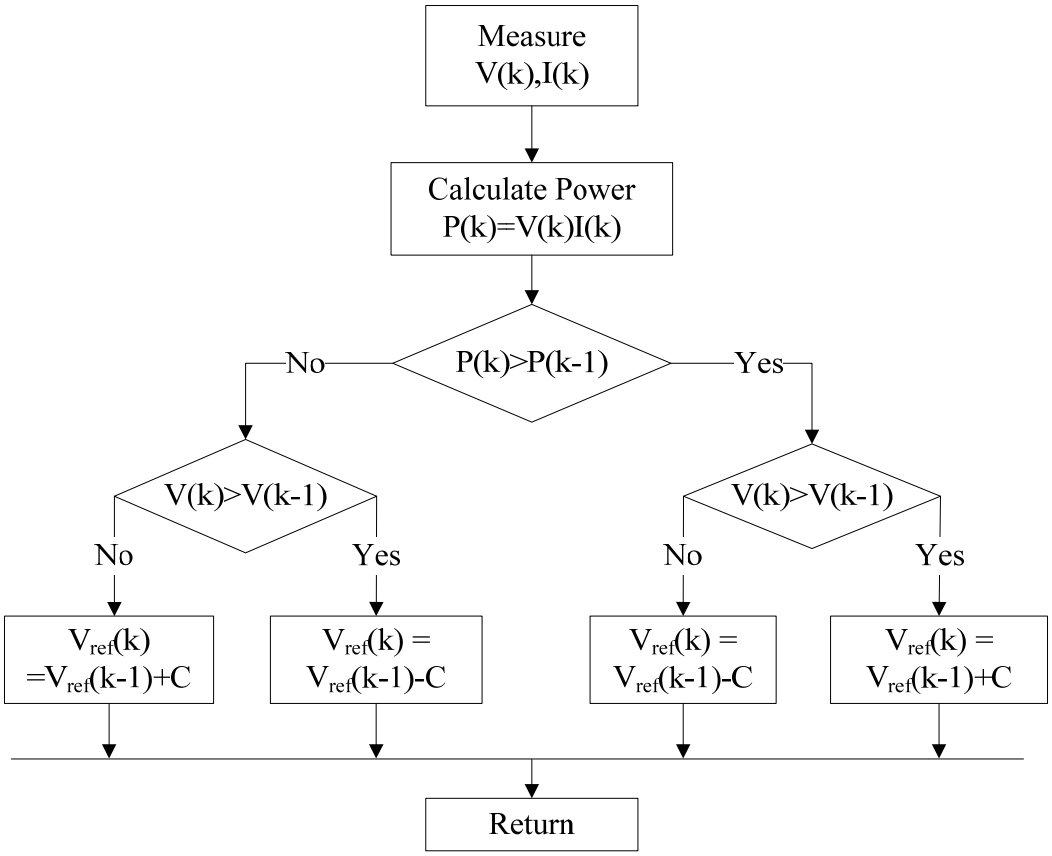


Figure 1-18 Flowchart of hill-climbing (P&O) algorithm.

The algorithm determines the reference voltage $V_{ref}(k)$ for the PV array voltage controller. The power at the current instant P(k) is calculated from the instantaneous voltage and current V(k) and I(k) respectively. Next P(k) is compared with the power of the previous instance P(k-1). If the power has increased, then the algorithm checks the last change in the PV array voltage and continues to change it in the same direction, either by adding or subtracting incremental value C to the reference voltage. However, if the power has decreased, the change to the voltage is set in the opposite direction.

This process is repeated till the system reaches MPP and then it oscillates near the MPP. The magnitude of oscillation depends on the magnitude of the perturbation and the frequency of update. The algorithm can be optimized to reduce the oscillation [22, 25]. One drawback of this method is that it fails under rapidly changing irradiance and environmental conditions [26]. This occurs when the change in power due to atmospheric conditions is larger and in the opposite direction than the changes due to perturbation caused by the algorithm, which results in the operating point shifting in the opposite direction.

1.5.2 Modified Perturb and Observe Method

As mentioned in the previous section, the P&O method has some limitations under rapidly changing atmospheric conditions [21, 24, 26-31], which may lead to incorrect or slow maximum power point tracking. To overcome this problem, a modified perturb and observe (MP&O) method was proposed, whose flowchart is shown in Figure 1-19 [23, 24]. This algorithm isolates the fluctuations caused by the perturbation process from those caused by the irradiance or weather change.

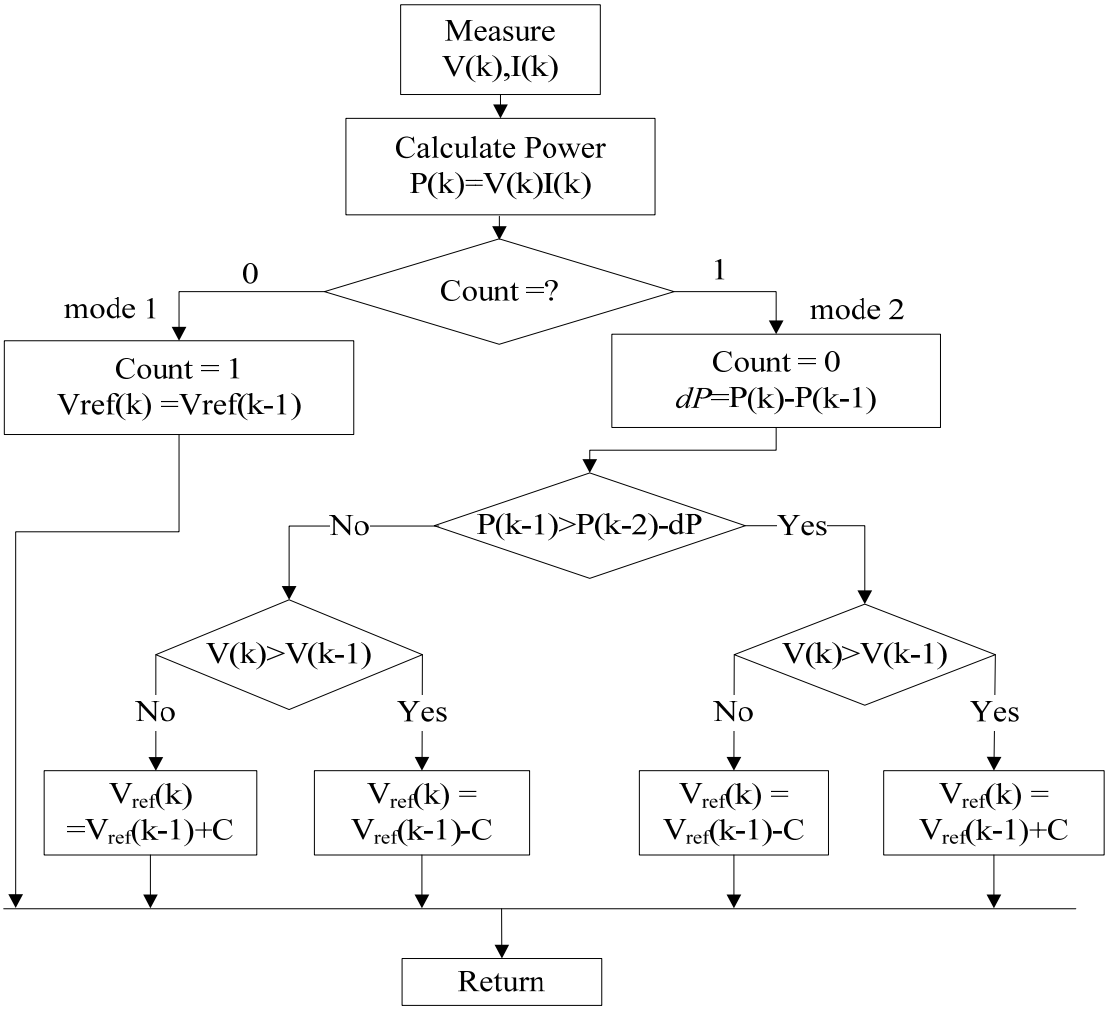


Figure 1-19 Flow chart of MP&O algorithm.

This can be achieved by executing an irradiance-changing estimate process (mode 1) before each perturbation. The amount of power change caused by the change in atmospheric condition *dP* is calculated by subtracting the previous calculated power P(k-1) from the current power

P(k) at the beginning of the perturbation (mode2). The deference *dP* is only caused by environmental changes, since the reference voltage of the PV array did not change in the previous mode. Then the change in power caused only by the perturbation is determined and the algorithm decides on the direction of the next perturbation in the same way as the P&O algorithm.

1.5.3 Open Circuit Voltage Method

The I-V characteristics of the PV array in Figures 1-6 and 1-8 suggests a linear relation between the open circuit voltage (V_{oc}) and the maximum power point voltage (V_{MPP}) at different irradiance and temperature conditions .This relation can be described as

$$V_{MPP} = k_1 V_{oc}; \quad k_1 < 1 \tag{1-2}$$

where k_1 is a constant, which depends on the characteristics of the PV array and can be determined by measuring the V_{MPP} and V_{oc} at different irradiance and temperature conditions. Although the constant k_1 differs according to the type of the PV array, it is between 0.71 and 0.8 [32]. For a given k_1, V_{MPP} can be calculated using Eq. (1-2) by turning off the DC/DC converter and measuring the open-circuit voltage of the PV array V_{oc}. This momentary but frequent shutdown of the system in order to measure V_{oc} causes some power loss, which can be avoided by using a separate PV cell to do the measurement [33].

1.5.4 Short Circuit Current Method

Similar to the previous method, the maximum power point current I_{MPP} is proportional to the short circuit current I_{SC} during different environmental conditions, as can be seen in Figures 1-6 and 1-7. This relation is defined by:

$$I_{MPP} = k_2 I_{SC}; k_2 < 1 \tag{1-3}$$

where k2 is a constant that depends on the characteristics of the PV array and is found to be between 0.78 and 0.92 [34]. Measuring the short circuit current during operation increases the complexity of the circuit and may require additional components. In addition to this drawback, the power loss associated with finding I_{SC} makes this method less popular.

1.5.5 Incremental Conductance

This method is similar to the Perturb and Observe algorithm and was proposed for rapidly changing atmospheric conditions [35, 36]. The method is derived from the graph of the power curve in Figure 1-20, where the slope of the curve is positive on the left side, negative on the right side, and zero at the maximum power point.

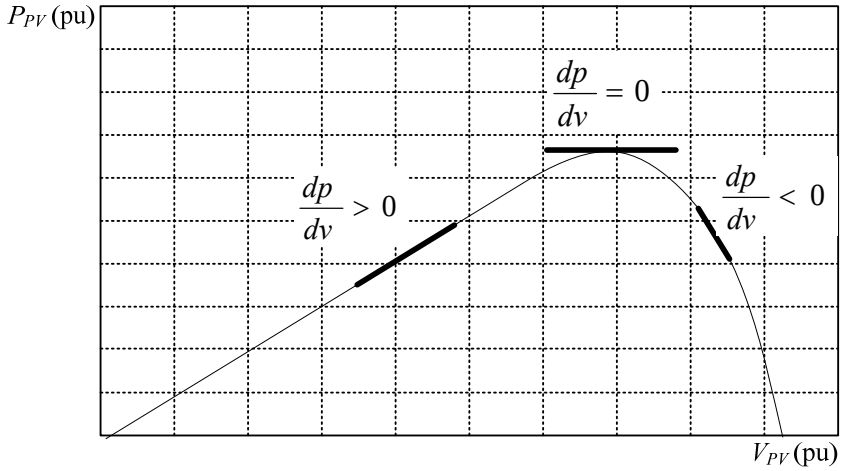


Figure 1-20 Variation of *dP/dV* in the incremental MPPT method.

The slope of the power curve can be found from

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{dI}{dV} \tag{1-4}$$

Equating the slope *dP/dV* to zero at the MPP in Eq. (1-4) yields:

$$\frac{dP}{dV} = 0 \Rightarrow \frac{dI}{dV} = -\frac{I}{V} \tag{1-5}$$

The right-hand side of Eq. (1-5) represents the negative of the conductance, while the left hand-side represents the incremental conductance. The derivative of the current and voltage can be approximated as the difference between the actual values and the values of the previous instant. Thus, by comparing the conductance I/V to the incremental conductance *dI/dV,* as shown in Figure 1-21, the algorithm can track the MPP and stay there until a change of *dI* or *dV* occurs as a result of changes in atmospheric conditions.

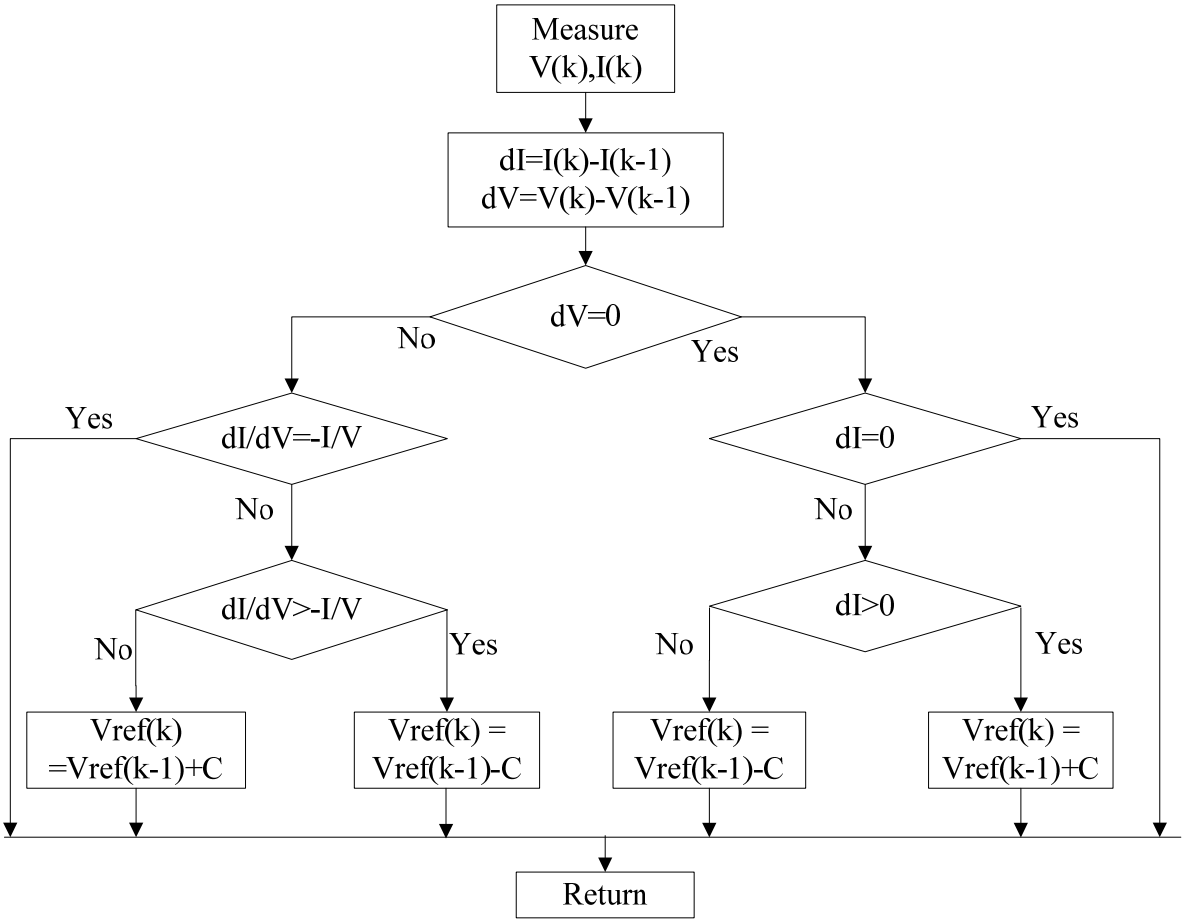


Figure 1-21 Flowchart of incremental conductance MPPT method.

1.5.6 Output Power Maximization

This method maximizes the output power of the DC/DC converter which results in maximizing the power from the PV array [37, 38]. Most of the load can be modeled as resistive load, current source, or voltage source load. Maximizing the load voltage will lead to maximizing the load power, which results in maximizing the power obtained from the PV array. Usually positive feedback from the load current is used to control the DC/DC converter [39].

1.5.7 Fuzzy Logic

Fuzzy logic control for the MPPT became popular with the development of microcontrollers and digital signal processors [40-42]. Fuzzy logic controllers have the advantage of working with imprecise inputs and therefore don't need an accurate mathematical model [43]. Since the *dP/dV*

is usually zero around the maximum power point, the error can be calculated as shown in Eq. (1-6). This error is usually used as the input to the fuzzy logic controller.

$$E(n) = \frac{P(n) - P(n-1)}{V(n) - V(n-1)} \tag{1-6}$$

During fuzzification, the error E is converted to a linguistic variable, and the output, which is usually the change in duty ratio ΔD, is determined by the rule base lookup table. The output of the fuzzy logic controller is obtained by de-fuzzification of the ΔD into a numeric variable. MPPT fuzzy logic controllers have been shown to perform well under varying atmospheric conditions. However, their effectiveness depends significantly on choosing the right error computation and the rule base table.

The simplicity of the algorithm plays an important role in implementing the MPPT algorithm. Although advanced algorithms like fuzzy logic may increase the efficiency of the MPPT algorithm, the overhead load on the processor may slow the execution of the algorithm, resulting in deterioration of the performance of the system. As mentioned earlier, the P&O method is the most used method because of its simplicity. However, its inability to track fast changes led to the development of the MP&O method. MP&O method performance is acceptable in both dynamic and static conditions. However the added wait state reduces the algorithm speed by half.

1.6 Anti-Islanding Algorithms

Islanding is a phenomenon in grid-tied PV systems, during which the inverter and some of the load are disconnected from the rest of the grid to form an island that is energized by the inverter, as shown in Figure 1-22 [44, 45]. This situation is undesirable since [44-47]:

- It imposes a dangerous situation for maintenance personnel;
- The quality of the power is no longer regulated by the grid, which may result in damage to the load; and
- Unsynchronized re-connection of the grid may cause damage to the inverter and loads.

In order to avoid islanding, grid-connected PV systems are required to implement methods to detect the formation of islanding and force the inverter to shut down.

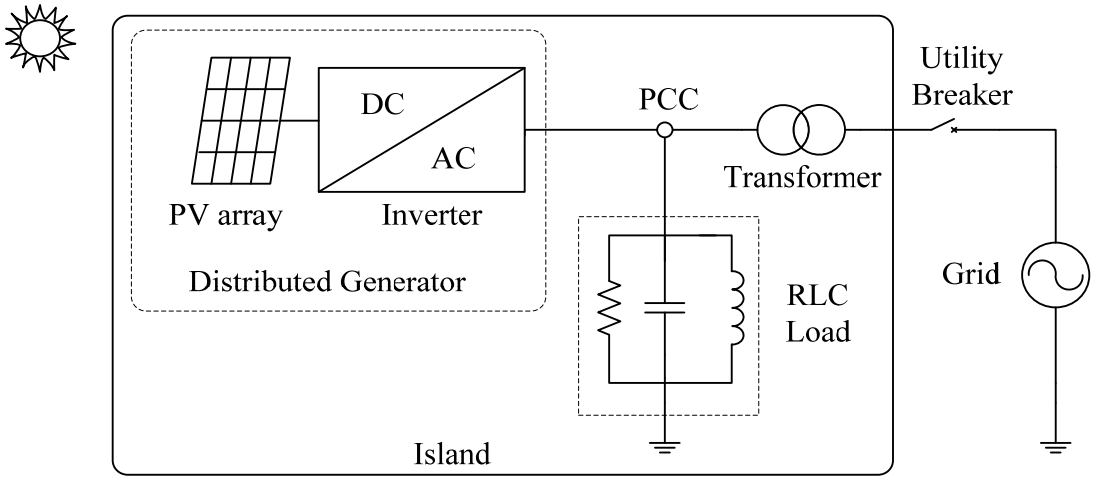


Figure 1-22 Grid-connected PV system.

The IEEE STD 929 and STD 1547 standards demand the use of an anti-islanding detection feature by the grid-connected inverter [44, 46]. These standards also suggest test procedures and set the limits for the grid parameters, as shown in Table 1-3 [44, 46, 48]. The voltage limits are divided into ranges and the trip time for each range is defined in each standard. The normal operational range for the frequency is the same in both standards, as are the current harmonic distortion limits.

Table 1-3 IEEE Std929-2000 and Std1547

Standards	IEEE Std 929		IEEE Std 1547	
Parameter	**Limits**	**Trip time limit**	**Limits**	**Trip time limit**
Grid Voltage	V < 60	6 cycles	V < 60	0.16s
	60≤V≤106	120 cycles	60≤V≤106	2.0s
	106≤V≤132	Normal operation	106≤V≤132	Normal operation
	132≤V≤165	120 cycles	132≤V≤144	1.0s
	165≤V	2 cycles	144≤V	0.16s
Grid Frequency	59.3-60.5Hz	Normal operation	59.3-60.5Hz	Normal operation
	Other wise	6 cycles	Other wise	0.16s
Current THD	< 5%	Always	< 5%	Always

Anti-islanding methods have been proposed to detect the islanding of the system and force the inverter to cease energizing the loads. These methods can be divided into three categories: 1) passive methods, 2) active methods, and 3) remote methods, as shown in Figure 1-23 [49-51].

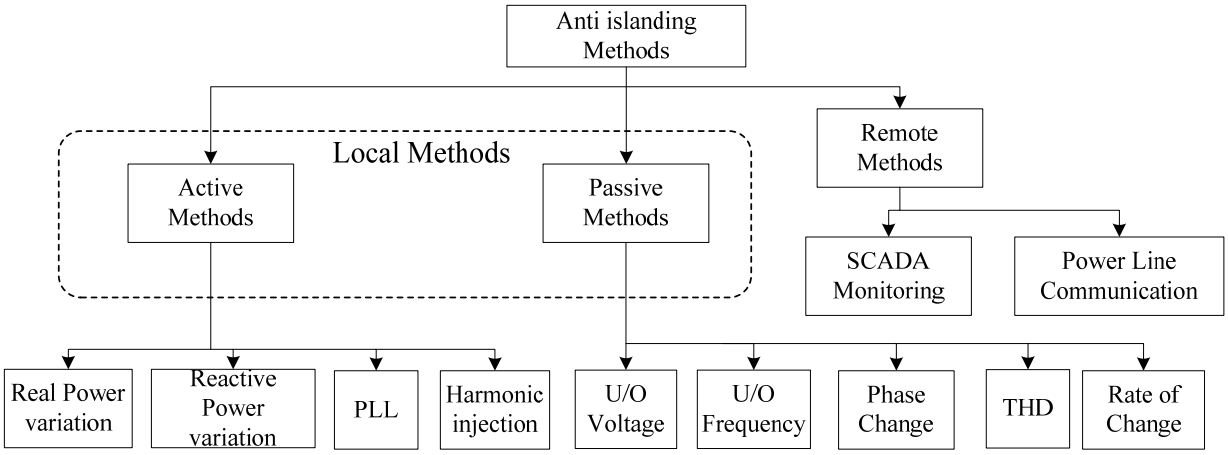


Figure 1-23 Anti-islanding method classification.

The non-detection zone (NDZ) is a defined space where the island cannot be detected. More than one space can be defined as the NDZ, such as the *RLC* space that was introduced in [52], the power mismatch space used in [53], and the load parameter space based on "quality factors" and load capacitance defined in [54]. The derivation of the NDZ in the power mismatch space is based on the real power mismatch ΔP and voltage at the island PCC given by [53]:

$$\frac{\Delta P}{P} = \left(\frac{V}{V_{island}} \right)^2 - 1 \tag{1-7}$$

where P is the active power, V_{island} the voltage of the local RLC loads of the DG system, and V is the grid voltage.

The relationship between the reactive power mismatch ΔQ and the frequency can be obtained by:

$$\frac{\Delta Q}{P} = Q_f \cdot \left[1 - \left(\frac{f}{f_{island}} \right)^2 \right] \tag{1-8}$$

where f is the grid frequency, f_{island} the resonance frequency of the local RLC loads of the DG system, and Q_f is the quality factor. The quality factor is defined as the reactive energy stored in L or C, divided by the active power consumed in R.

With the values specified in IEEE Std 929-2000 and a quality factor of Q_f =2.5, Eqs. (1-7) are in the range of

$$-17.36\% \le \frac{\Delta P}{P} \le 29.13\% \tag{1-9}$$

$$-5.95\% \le \frac{\Delta Q}{P} \le 4.11\% \tag{1-10}$$

Equations (1-9) and (1-10) show the range of change in real and reactive power with repect to the load power. If the change ratio is larger than these limits, the voltage and/or the frequency of the point of common coupling (PCC) will be driven outside the limits set by IEEE Std 929-2000. If the local loads have similar power capacity as that of the DG system, i.e., all the generated power is consumed locally, voltage and current levels at the PCC will vary only slightly when the islanding occurs, which falls in the NDZ.

1.6.1 Passive Methods

Passive methods use the grid parameters such as voltage, frequency and harmonics to detect the island formation [49-51]. Nevertheless, passive methods are conceptually simple and easy to implement, and do not introduce any impact on the power quality of the system. However, they have large NDZ since an island can only be detected if the grid parameters fall outside the limits set in Table 1-3.

a) Under/Over Voltage Methods

Under/Over-voltage (UV/OV) protection is a requirement for all grid-connected inverters, and can be used as an anti-islanding method. At the instant of island, if the real power generated by the inverter (P_{inv}) is not equivalent to the power absorbed by the load (P_{load}), the amplitude of the voltage at PCC will vary. The inverter may detect the island if the voltage is beyond the limits given in Table 1-3 [45, 50].

b) Under/Over Frequency Method

Under/Over-frequency (UF/OF) protection is another requirement for the grid-connected inverters and can also be used as an anti-islanding detection method. At the instant of islanding, if the reactive power delivered by the inverter (Q_{inv}) does not equal the reactive power demanded by the load (Q_{Load}), the current waveform at the PCC will experience a sudden jump in phase angle with respect to the inverter voltage waveform. As a consequence, the inverter control will try to minimize the error by changing the frequency until the reactive power difference (ΔQ) is zero at the resonance frequency of the load [50]. If this frequency exceeds the limit set by Table 1-3, the island is detected [44, 45, 49, 50].

c) Sudden Change in Phase Angle

A sudden change in the phase angle of the current waveform with respect to the voltage waveform can be used to detect the island formation [49, 50]. After the island formation, if the phase angle change in the current is larger than a certain predefined limit, $\theta_{threshold}$, the island is detected. This method is rarely used due to the difficulty of setting the threshold to provide reliable islanding detection, since the switching of certain loads may result in false tripping [49, 50, 53].

d) Voltage Harmonic Detection

The harmonics generated by the inverter current is limited to 5% by the standard given in Table 1-3, which will generate negligible change in the grid voltage THD when the low impedance grid is connected. However, when the grid is disconnected, the inverter current will flow through the load, which has much higher impedance than the grid, and thus the voltage harmonic distortion will be increased substantially [50]. If the measured THD of the grid voltage exceeds the predefined limits, an islanding is detected and the inverter ceases to operate [49, 51].

e) Rate of Change Methods

These methods measure the rate of change of voltage (ROCOV) [55], the rate of change of frequency (ROCOF) [55-58], the rate of change of Power (ROCOP) [59], or a combination of more than one of these methods. Eq. (1-7) shows that the mismatch in real power during islanding will result in a change in the voltage at PCC. However, if this imbalance is small, then the island is not detected, as shown in Eq. (1-9). To overcome this limitation, the rate of change

in voltage $\Delta V/\Delta t$ is used as an index of islanding [60]. The relation between the mismatch in real power ΔP and the rate of change in voltage can be expressed as [55]:

$$\frac{\Delta V}{\Delta t} = \frac{V}{2P} \times \frac{\Delta P}{\Delta t} \tag{1-11}$$

Equations (1-8) and (1-10) show that the mismatch in reactive power leads to a change in frequency. The rate of change of frequency $\Delta f/\Delta t$ can be used as an indication of islanding since it is much larger when the grid is absent. The relation between the rate of change of frequency and the mismatch in reactive power ΔQ was found in [55]:

$$\frac{\Delta f}{\Delta t} \cong K \frac{\Delta Q}{\Delta t} \quad \text{where} \quad \frac{1}{K} = -\frac{V^2}{2\pi L f^2} - 2\pi C V^2 \tag{1-12}$$

1.6.2 Active Methods

In active methods, a perturbation is injected into the current waveform, which will drive one of the system parameters out of its limits during islanding operation [61, 62]. These perturbations should be small in order to avoid degrading the power quality when the grid is connected [63]. Active methods reduce the NDZ, particularly in cases where the local loads are close in capacity to the DG system.

a) Impedance Measurement Method

The impedance measurement method uses the fact that the impedance of the grid is so small compared to the impedance of the load. So a change in the current waveform will not affect the voltage waveform in case the grid is connected. One way to do this is to change the amplitude of the current waveform so that the change in the power delivered to the load changes accordingly, which drives the PCC voltage out of its limit [49, 51]. Another method is to make a notch in the current waveform as shown in Figure 1-24 [64]. When the grid is connected, the voltage waveform is undisturbed by the current notch because the impedance of the grid is so small. In the island situation, the voltage waveform will be distorted, which enables

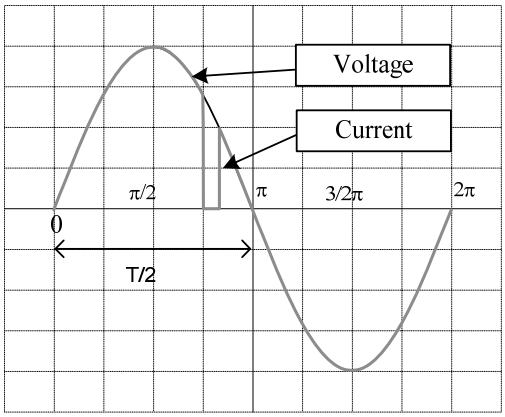


Figure 1-24 Waveforms of the impedance measurement method.

the detection of the island. However, if the time constant of the load is much larger than the time length of the notch, this method fails to detect the island [64].

b) Slip Mode Frequency Shift Method

In the slip mode frequency shift method (SMS) the phase angle of the output current of the inverter is a function of the frequency of the voltage at the PCC instead of being zero as shown in Figure 1-25 [49-51, 65]. When the grid is connected, the system works at the utility frequency, but when an island is formed, a small disturbance will force the system to work at the other intersection points, where the island can be detected. For some loads which have their phase increases faster than the inverter, this method fails [50].

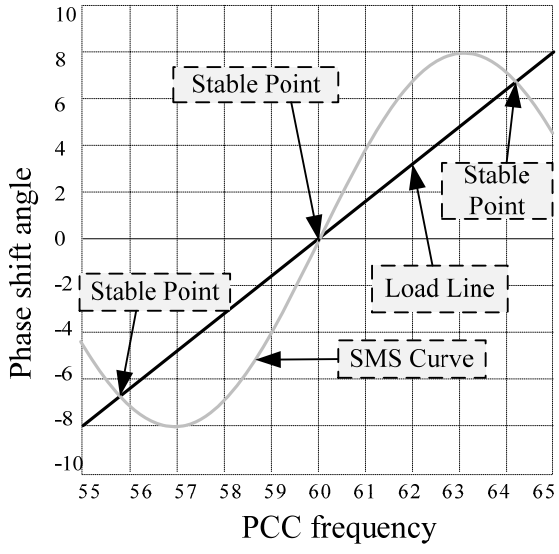


Figure 1-25 Frequency response of the slip mode frequency shift method.

c) Active Frequency Drift Method

The active frequency drift (AFD) method is based on the injection of a current waveform distortion to the original reference current of the inverter, to force a frequency drift in case of islanding operation. By introducing a zero conduction time t_z at the end of each half cycle, as shown in Figure 1-26, the phase angle of the fundamental component of the current is shifted.

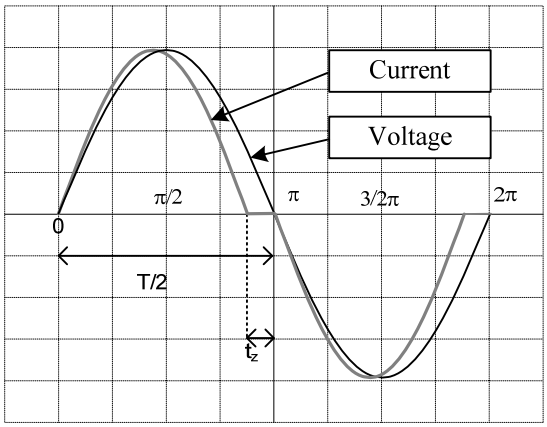


Figure 1-26 Waveforms of the active frequency drift method.

During normal grid operation, the inverter is synchronized to the grid voltage and will operate at the grid frequency. In islanding operation, the added distortion to the current will produce a permanent drift in the operating frequency towards the local load resonance frequency as the inverter attempts to maintain the unity power factor. This drift will eventually reach the frequency boundary limits set for islanding detection[49-51, 66]. The dead time t_z in which the current is forced to zero, and the period of the original signal T can be related to each other to define the chopping factor C_f used to perturb the waveform as [63, 67]:

$$C_f = \frac{2t_z}{T} \tag{1-13}$$

d) Sandia Frequency Drift Method

Sandia frequency drift, also known as active frequency drift with positive feedback, is the same as the previous method, with the chopping factor being a function of the frequency error as expressed by the following equation [49, 51, 63]:

$$C_f = C_{f0} + K(f - 60Hz) \tag{1-14}$$

When the grid is connected, the frequency error is zero; thus, the inverter works at a constant chopping factor. However when an island is formed, the frequency is changed due to the distortion in the current waveform, and the error is not zero anymore. Consequently, this leads to a larger C_f and more frequency drift until the frequency is out of limit and the island is detected [49-51]. This technique reduces the NDZ of the AFD method.

e) Phase Lock Loop Methods

A Phase lock loop (PLL) is used to synchronize the inverter output current to the Grid voltage. Usually PLLs are implemented into the control software of the inverter. The input to the PLL is the voltage signal and its output is the phase angle θ. PLL anti-island methods introduce some perturbation to the reference phase angle θ. Figure 1-27 shows the block diagram of a typical PLL. In [68, 69] a small phase deviation ε is added to the phase error such that:

$$\Delta\phi' = \Delta\phi + \varepsilon \tag{1-15}$$

During islanding $\Delta\phi \approx 0$, the modified phase error is always non-zero and this disturbs steady-state operation, causing the frequency to drift out of limit. In [70] the PI filter is designed such that the loop stability depends on the impedance seen by the converter. When the grid is connected, the loop is stable. Otherwise (during islanding) the frequency will oscillate with exponential growth until it drifts out of limit. One setback to this method is that the drift frequency and the growth speed are dependent on the load.

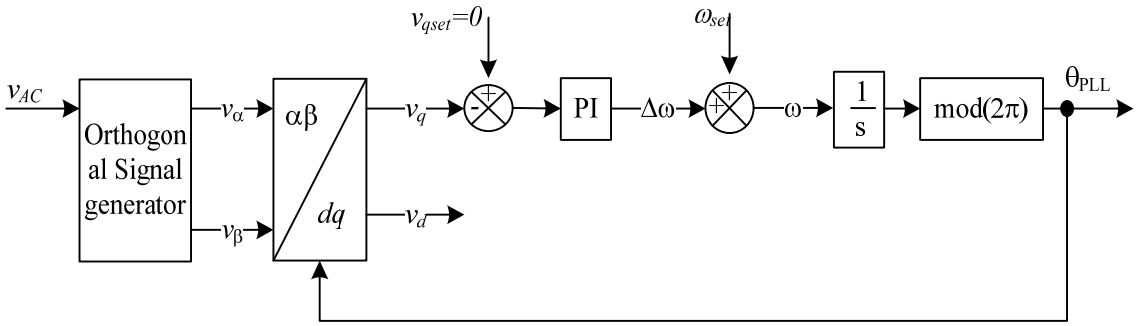


Figure 1-27 Block diagram of a PLL.

In [71-74] a perturbation is added to the output of the PLL such that:

$$\theta'_{PLL} = \theta_{PLL} + k\sin(\theta_{PLL}) \tag{1-16}$$

where k<<1 controls the amount of distortion injected.

Figure 1-28 shows the effect of this perturbation on the phase angle. Note that the zero crossing is not affected by this perturbation. This is equivalent to the addition of a second order harmonic to the original referenced waveform. Figure 1-29 shows the current waveform with the amount of distortion exaggerated to illustrate the method. The current waveform will result in a second order harmonic in the voltage at the PCC, which is in proportion to the grid impedance. Park transformation or Goertzel algorithms are used to extract the content of the voltage second order harmonic and some logic algorithms are used to determine the Islanding.

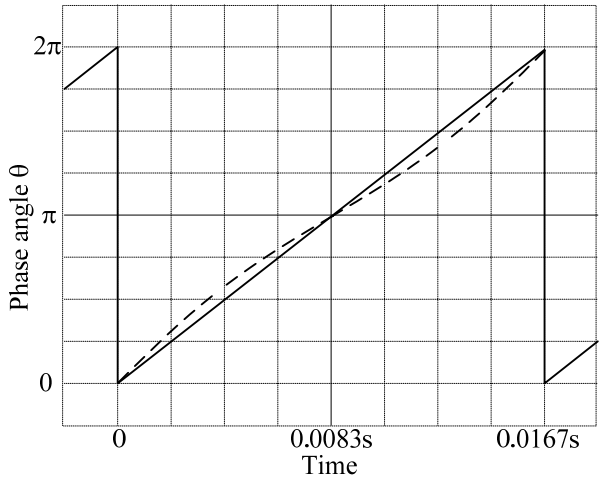


Figure 1-28 phase angle perturbation in the PLL method.

f) Harmonic injection methods

These methods inject some harmonics and measure the voltage response at that specific frequency to determine the impedance of the grid [75]. When the grid is connected, the Harmonic voltage at the PCC $V_{PCC}\ (h)$ is given by:

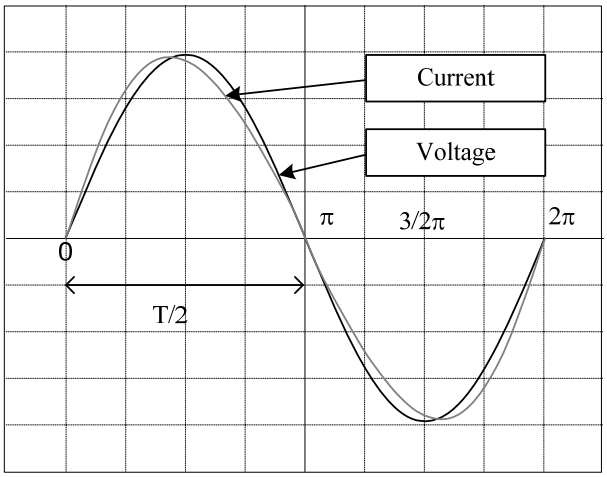


Figure 1-29 Current and voltage waveforms in the PLL method.

$$V_{PCC}(h) = \left(\frac{Z_{load} Z_{grid}}{Z_{load} + Z_{grid}} \right) I_{inv}(h) \tag{1-17}$$

where Z_{load}, Z_{grid} are the load and grid impedances respectively and $I_{inv}(h)$ is the injected harmonic current.

When the grid is disconnected during islanding the above equation becomes:

$$V_{PCC}(h) = Z_{load} I_{inv}(h) \tag{1-18}$$

In [75, 76] the 9th harmonic is added to the output current and the response at the PCC is calculated using Goertzel's algorithm. The 9th harmonic distortion factor (HD9) of voltage increases from 0.147% to 0.467% during islanding. This facilitates the detection of islanding.

Another way to address harmonic injection is to periodically use over-modulation of the PWM to inject harmonics into the grid [77]. The over-modulation injects mainly 3rd, 5th and 7th harmonics into the grid. In this method modulation index m_a is varied periodically according to the following equation:

$$m_a = \begin{cases} m_{op} & 0 \le t \le 9T \\ m_{over} & 9T \le t \le 10T \end{cases} \tag{1-19}$$

where m_{op} is the modulation index during normal operation, m_{over} is the modulation index during the harmonic injection period, and T is the time period of the grid.

During the over-modulation period, the m_a is set to 1.1 since it provides sufficient harmonic distortion to detect the grid impedance without exceeding the 5% THD limit. One advantage of this method is that the distortion is injected periodically, which reduces the overall effect on the power quality even with multiple inverters. Another advantage is that in multi-inverter operation, the inverters do not cancel the effect on each other, since they are all synchronized by the PLLs.

1.6.3 Remote Methods

Remote methods usually reside some distance away from the DG and are usually at the grid (substation) side of the network. They either use a communication means between the utility and the DG to detect and prevent islanding, or they monitor the status of the grid and send commands to the DG to seize energizing the grid in case of islanding. These methods are usually very reliable with no NDZ; but they are expensive and hard to implement thoroughly, since they need to be implemented across the whole network [51, 78].

a) Power Line Carrier Communications

The power line carrier communication (PLCC) method uses a transmitter to send low energy signals through the power line. These signals are picked up by a receiver at the inverter side. The transmitters are usually located at the substations and send the signals to all the lines fed by that station as illustrated in Figure 1-30. In case of island formation due to circuit breaker opening, the signal is lost. The receiver commands the inverter to cease energy or open a switch to isolate the inverter and the load. The signal could be a low energy signal like the one used for smart grid application [79, 80]. Moreover, the same technique could be used to achieve a safe ride-through operation during grid voltage disturbances [81]. Another way to send a signal through power lines is by the waveform distortion technique [82-84], where the voltage waveform is distorted at the zero-crossing by a transmitter at the substation, and a receiver at the DG side detects the distortion and resembles it as a signal from the transmitter.

b) Supervisory Control and Data Acquisition

The supervisory control and data acquisition (SCADA) system is widely used in the electrical power distribution system to monitor the grid parameters (voltage, frequency, etc.). They are also used to monitor the status of all circuit breakers and re-closers. This system can detect unintentional islanding after a loss of grid, and issues a transfer trip scheme to isolate the

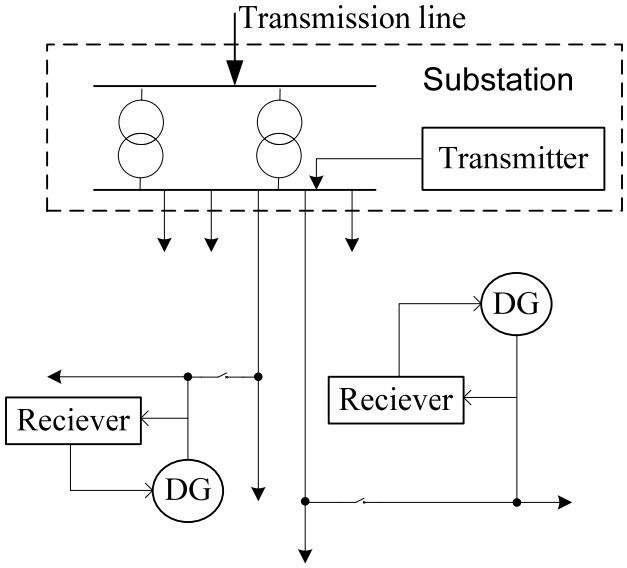


Figure 1-30 power line communication method.

inverter. This method might be very effective but is highly expensive [49, 50] since each inverter needs to be connected to the SCADA system.

1.6.4 Discussion about anti-islanding methods

Remote methods are rarely used except in high power systems which already have a communication link with the grid and they usually implement ride-through during the fault. Whereas passive methods are present in most inverters for monitoring grid parameters, and they usually trigger the island detection. By themselves passive methods are not sufficient to detect the island in a large area of the load spectrum. On the other hand, active methods insert some perturbation into the current waveform in order to alter the balance of real or active power between the load and inverter. By doing so, they also introduce harmonics. Similarly, phase lock loop methods and harmonic injection insert harmonics at different frequencies to detect the island's high impedance at these frequencies. The deterioration in power quality due to the increase in the number of PV inverters is a real concern for utility authorities.

1.7 Thesis Objectives

The grid-tied PV energy system normally consists of a DC/DC converter which is responsible for boosting the DC voltage and implementing the MPPT algorithm, and a DC/AC inverter which is connected to the grid for energy transfer and grid code compliance. As presented earlier in this chapter, many PV converter topologies, MPPT controls schemes, and anti-islanding methods have been proposed. They all have some good features, but are accompanied by certain drawbacks. This thesis focuses on a comprehensive solution for a grid-connected PV energy system, where the features of the existing power converters and control schemes are retained and their drawbacks are mitigated. In particular, the thesis research is focused on three major areas of a PV energy system: 1) development of a power converter with minimum power losses, 2) optimization of an MPPT algorithm with improved dynamic performance, and 3) development of an active anti-islanding method with reduced non-detection zone and minimal adverse impact to the grid.

The main objectives of this work are as follows:

1) Investigation and development of DC/DC converter topologies

DC/DC conversion can be achieved by different power converter topologies, among which the full-bridge converter is the most suitable one for medium power (500W to 3kW) PV systems. The classic full-bridge converter uses hard switching of the MOSFETs, hence limiting the power rating of the converter. The phase shifted full-bridge converters (PSFB) use soft switching to achieve Zero-Voltage Switching (ZVS) or Zero-Current Switching (ZCS). To minimize the power losses of the PV converters, the PSFB converter investigated in this thesis uses two different types of snubber circuits: the RCD circuit and the active clamp circuit. A new control scheme is proposed, which achieves zero voltage zero current switching (ZVZCS) for the main switches and ZVS for the active clamp switch in the phase shifted full-bridge converter.

2) Development of control scheme for parallel DC/DC converters

Parallel converters are used to achieve higher power ratings for the PV energy system. They should be able to control the PV array voltage and share the array current while working at the

maximum power point. Another advantage of parallel converters is the ability to cancel the current ripple at both the input and output by interleaving technology.

3) Investigation and evaluation of MPPT algorithms

The third objective of this thesis is to evaluate the performance of different MPPT schemes. The tracking of the maximum power point (MPP) is a challenging task since the characteristics of the PV array are nonlinear and vary with the irradiance and temperature levels. An optimal algorithm should be able to track the MPP fast and closely during rapid changes in environmental conditions.

4) Development of an anti-islanding method with small NDZ and minimal impact to the grid

One of the most challenging issues for the grid-tied PV inverter is to detect its disconnection from the grid and prevent the inverter from islanding formed by the disconnection. Many methods have been proposed. These can be classified into passive and active islanding detection methods. Passive methods use grid parameters to determine the island, while active methods inject a perturbation into the current. Active methods are more effective in detecting islands even when there is a balance between the load demand and the generated power. However the injected perturbation introduces harmonics into the grid. The last objective of this thesis is to develop an anti-islanding method which generates minimal harmonics into the grid while retaining all the attractive features of other active detection methods.

1.8 Thesis Outline

This dissertation consists of six chapters as follows:

Chapter 1 presents background information about the PV energy systems, the PV arrays and an introduction to MPPT and anti-islanding methods.

Chapter 2 investigates various soft switched DC/DC converters for PV applications. The operation principles of converters with RCD and active clamp snubbers are presented. A new gating scheme of the active clamp that results in zero voltage and zero current switching is proposed. Its operating principles are presented and its performance is investigated. The performance of the proposed converter is verified by both simulation and experiment.

Chapter 3 presents the design of a multi-channel DC/DC converter consisting of three parallel individual converters working in interleaved method. A new cascaded control method is proposed, where the PV array voltage is controlled by a master converter and the active current sharing is implemented by the remaining slave converters. The performance of the new control method under varying temperature and irradiance levels are examined by simulation in the Matlab/Simulink platform.

Chapter 4 investigates different MPPT algorithms, and compares their performance during changing in irradiance and temperature. A detailed simulation of the algorithms is carried out inMatlab, and an experimental setup with a solar array simulator is used to test the performance in realistic situations. The results verify that the Estimate Perturb Perturb (EPP) algorithm can provide accurate and reliable maximum power tracking performance even under a rapidly changing irradiance condition.

Chapter 5 examines the islanding phenomena and presents an improved active anti-islanding detection method that can detect islanding with less total harmonic distortion compared to conventional methods. The rms value and the Fourier series coefficients of the current waveform of the proposed method are obtained and used to derive analytically the operational characteristics of the method. Simulations and experiments are conducted to demonstrate the performance of the method.

Chapter 6 summarizes the main contributions and provides conclusions for the dissertation. Future research work on PV energy conversion systems is suggested.

Chapter 2
Zero-Voltage Zero-Current Switching Full-Bridge Converter with Active Clamp

2.1 Introduction

The DC/DC converter is the building block of PV energy conversion systems. DC/DC conversion can be achieved by different converter topologies, among which the Full-Bridge (FB) converter is the most suitable for medium power (500W – 3kW) PV systems [85, 86]. Classical FB converters use hard switching technology, resulting in high power losses. In order to achieve high efficiency power conversion, the switching losses of the DC/DC converter should be minimized. Soft switching resonant converters can achieve Zero-Voltage Switching (ZVS) or Zero-Current Switching (ZCS), but they have variable switching frequencies, which complicates the optimization of the design of the output filter and the control circuit. Quasi-resonant or multi-resonant converters work in a narrower frequency range, but their high component stress makes them unsuitable for high power and high voltage applications [85]. Another type of converter is the phase-shifted zero-voltage switching full-bridge converter (ZVSFB), which uses the parasitic components of the circuit to achieve ZVS.

The ZVSFB converter has several desirable features such as high power density, high efficiency and small filter components [87]. Moreover, primary switches in the converter do not need snubber circuits since they work under zero-voltage switching conditions. However, the rectifier diodes on the secondary side of the transformer usually require a snubber circuit to absorb the severe ringing during the switching transients, causing high power losses in the circuit.

This chapter starts with an introduction to the ZVSFB converter with two different types of snubber circuits: a passive RCD circuit and an active clamp circuit. A new gating scheme is proposed for the phase-shifted FB converter with active clamp circuit to achieve zero-voltage

and zero-current switching (ZVZCS) for power loss minimization. The simulation and experimental results of these three converters are presented together with a comparison of power losses and efficiencies for each converter.

2.2 Conventional Phase-Shifted Zero-Voltage Switching Full-Bridge Converter (ZVSFB)

The ZVSFB converter, shown in Figure 2-1, is widely used due to its simple circuit and zero-voltage switching without the need for additional resonant circuitry [88, 89]. The ZVSFB converter utilizes four switches to transfer energy to the output through a high-frequency transformer. The switches are controlled by phase-shifted PWM, which results in ZVS to all four switches in both legs. This is achieved through resonance between the MOSFETs parasitic capacitance C_{MOS} and the transformer leakage inductance L_{lk}. The output of the transformer is rectified using a diode bridge. Then it is smoothed by an LC filter composed of L_0 and C_0. A blocking capacitor C_b is used to block the DC current in case of volt-second unbalance in the transformer. The steady-state operation of the converter is discussed in the following section.

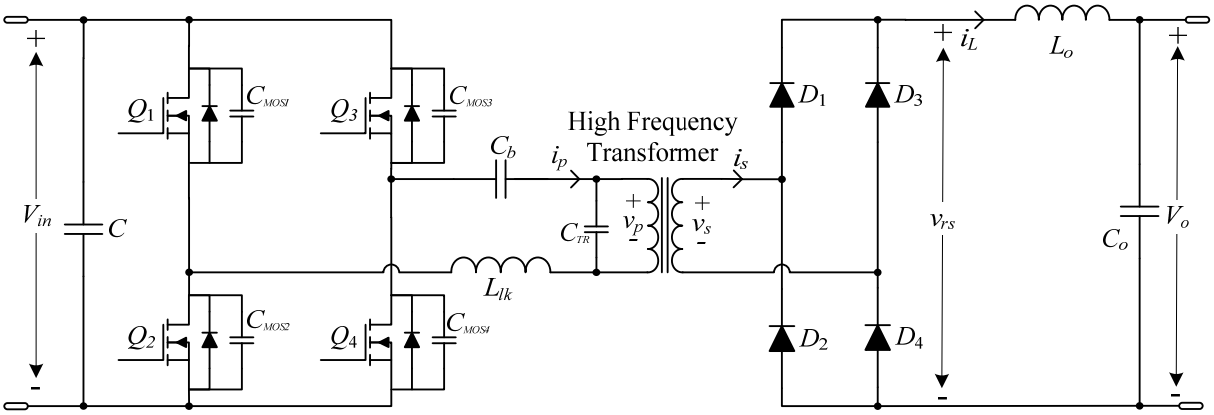


Figure 2-1 Schematic diagram of ZVS full-bridge DC/DC converter.

2.2.1 Operation Principles

Figure 2-2 shows the gating signals v_{gs}, the transformer primary voltage v_p, primary current i_p the secondary voltage v_s and the reflected inductor current ni_L, where n is the transformer ratio. The MOSFETs operate at 50% duty cycle. The converter operating duty cycle is controlled by the phase shift ϕ between the left and right legs. The energy stored in the leakage inductance L_{lk} is used to discharge the MOSFET capacitance prior to its turn on, thus achieving ZVS. To

ensure ZVS, the energy stored in the leakage inductance should be higher than that of the MOSFET's capacitance C_{MOS} and transformer winding capacitance C_{TR}, as shown in Eq. (2-1):

$$E = \frac{1}{2} L_{lk} I_{pb}^2 > \left(\frac{4}{3} C_{MOS} + \frac{1}{2} C_{TR} \right) \times V_{in}^2 \tag{2-1}$$

where I_{pb} is the primary current at the beginning of the resonance transition and V_{in} is the input voltage of the converter.

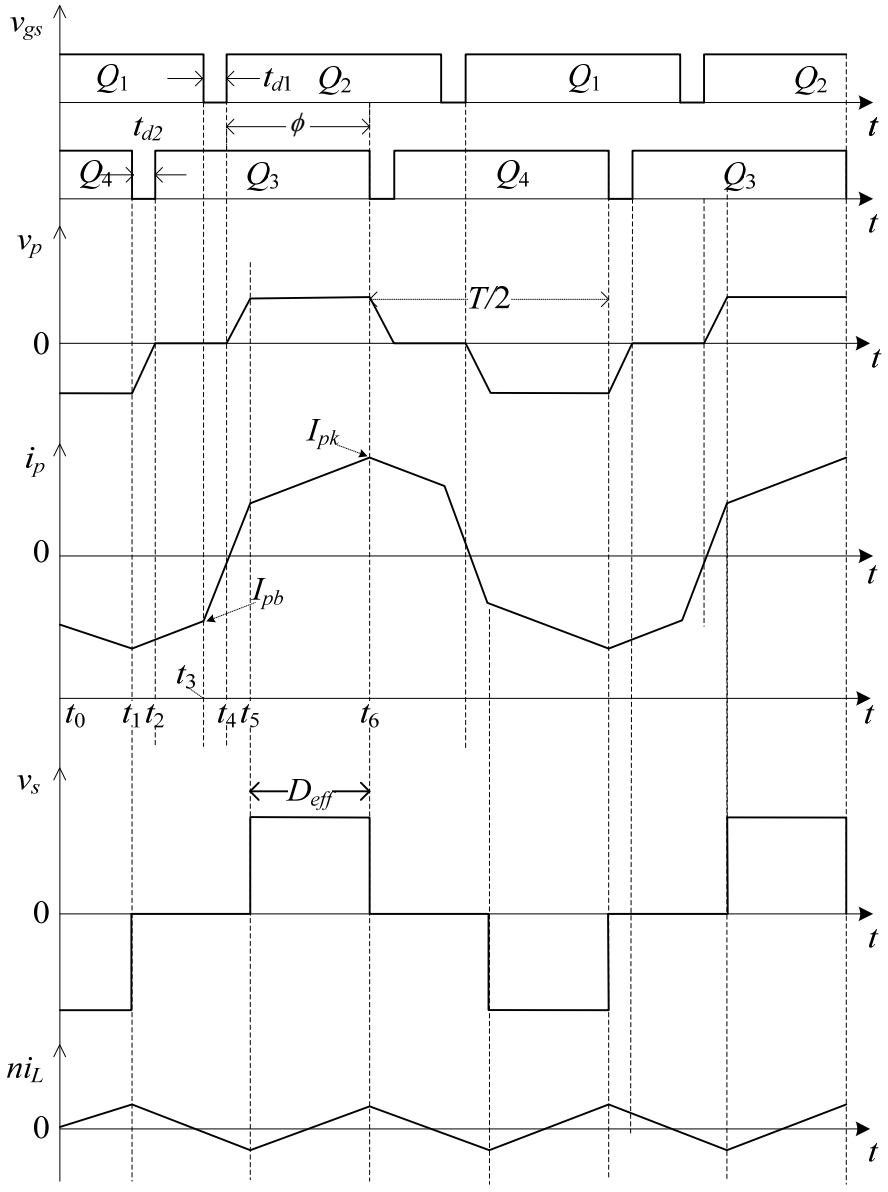


Figure 2-2 Operation waveforms of ZVS full-bridge converter.

The critical load current I_{crtk} which ensures that the inductive energy is larger than the capacitive one is given in the following equation:

$$I_{crtk} = \sqrt{\frac{2}{L_{lk}}\left(\frac{4}{3}C_{mos} + \frac{1}{2}C_{TR}\right) \times V_{in}^2} \tag{2-2}$$

The operation of the converter during each half cycle of the switching period can be divided into five operating modes:

Mode 1 t_0-t_1: Prior to t_1, Q_1 and Q_4 are on, and the power is transferred through the transformer to the load. The primary voltage v_p is equal to the negative of the input voltage, and the secondary voltage v_s is equal to the primary voltage multiplied by the turn's ratio. The primary current increases at the same rate as the inductor reflected current.

Mode 2 t_1-t_2: At t_1, the MOSFET Q_4 is turned off. The primary current i_p, which is the reflected load current ni_L, is maintained by the transformer leakage inductance L_{lk}. i_p continues to flow through the MOSFET capacitance C_{MOS4}, charging it to $+V_{in}$ and discharging C_{MOS3} (active phase). The primary voltage v_s decreases as C_{MOS4} is charged. The time needed to ensure full discharge (t_{d2}) is given by:

$$t_{d2} = \left(4C_{MOS} + C_{TR}\right)\frac{V_{in}}{i_{peak}} \tag{2-3}$$

Mode 3 t_2-t_3: At t_2, the primary current i_p flows through the body diode of Q_3, enabling zero voltage turn-on of Q_3. Until t_3, the primary current i_p freewheels through Q_1 and Q_3. At t_3, Q_1 is turned off, which makes the primary current i_p charge C_{MOS1} and discharge C_{MOS2}. The voltage across the transformer begins to increase, and this voltage is applied across the leakage inductance L_{lk} of the transformer.

Mode 4 t_3-t_4: The load current is no longer reflected on the primary side and this current freewheels through the secondary diode rectifier. The leakage inductance L_{lk} resonates with the MOSFETS output capacitors C_{MOS1} and C_{MOS2} (passive phase). This drives the primary current i_p to charge C_{MOS1} and discharge C_{MOS2}. The delay time needed for the resonance to completely discharge the capacitors is one fourth of the resonance period as defined by:

$$t_{d1\max} = \frac{\pi}{2}\sqrt{L_{LK}C_{Total}}\ ; \quad \text{where } C_{Total} = C_{MOS} + C_{TR} \tag{2-4}$$

Mode 5 t_4-t_5: At t_4, Q_2 is turned on with zero voltage across it. This places the full voltage across the leakage inductance L_{lk} since the transformer secondary winding is short circuited (v_s=0) by the freewheeling load current. The primary current i_p starts to ramp in the opposite direction until it reaches the reflected secondary current ni_L at t_5. Then the power transfer begins to the load through the transformer, and the second half of the cycle repeats again in the same manner.

The duty cycle of the converter is controlled by changing the phase angle ϕ between the two legs. Due to the leakage inductance, the effective duty cycle D_{eff}, seen at the secondary winding of the transformer, is less than the applied duty cycle, as shown in Figure 2-2. The effective duty cycle can be approximated by [85] :

$$D_{eff} = \frac{D}{\left(1 + 4\frac{L_{lk}}{R'}f_s\right)}; \tag{2-5}$$

where $R' = \frac{R_{load}}{n^2}$; $n = \frac{N_s}{N_p}$ and f_s is the switching frequency of the MOSFETs.

The output voltage is given by the following equation:

$$V_o = \left(\left(\left(V_{in} - V_{mos}\right)\times\frac{N_s}{N_p}\right) - V_{diode}\right)\times D_{eff} \tag{2-6}$$

where V_{mos} is the average voltage drop across the MOSFET during on time, and V_{diode} is the voltage drop across the rectifier diode while forward biased.

2.2.2 Passive Snubber Circuits

In the above-mentioned topology, the soft switching of the bridge MOSFETs eliminates the need for snubber circuits on the primary side of the transformer, but the resonance of the leakage inductance with the rectifier's diode capacitance and the capacitance of the windings generates ringing across the rectifier that could produce voltage spikes as high as three times the voltage applied to the secondary [85].

The frequency of the ringing is dependent on the leakage inductance of the transformer and on the combined capacitance of the transformer and output rectifiers C_e. The ringing frequency is explained in Eq. (2-7):

$$f_{ring} = \frac{1}{2\pi\sqrt{\left(\frac{N_s}{N_p}\right)^2 L_{lk} C_e}} \tag{2-7}$$

Since the leakage inductance is large (a desired feature to facilitate ZVS), the frequency is low, which makes RC snubber losses too high, especially in high voltage applications. An RCD snubber circuit, which returns some of the power to the output, can be used to reduce the ringing at the rectifier diodes, and to clamp the rectifier voltage, as shown in [90].

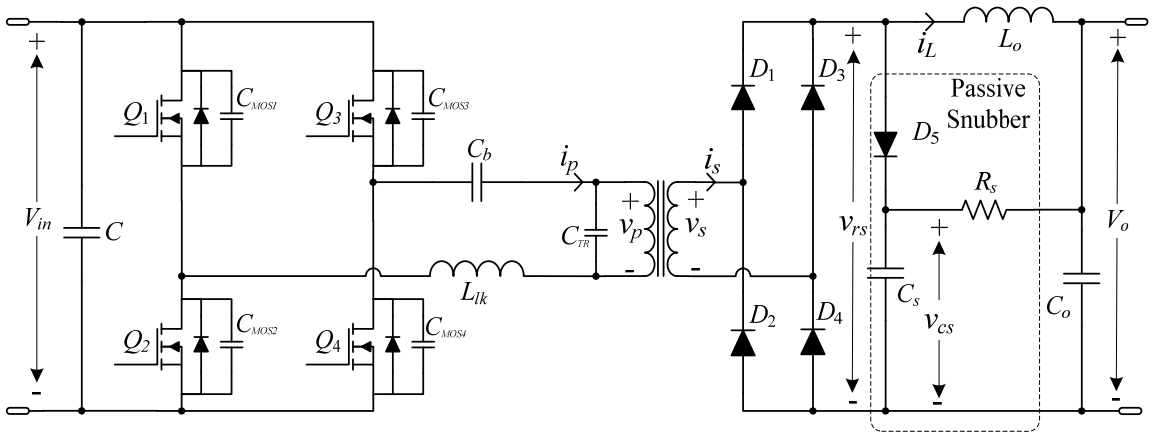


Figure 2-3 Schematic diagram of full-bridge converter with passive snubber.

In this topology, the rectifier voltage is clamped by the snubber capacitor voltage V_{cs}, and the energy recovered from the leakage inductance is then transferred to the load through the resistor R_s. The relation between the clamp voltage V_{cs} and the snubber resistor R_s is given by:

$$R_s = \frac{T(V_{CS} - V_o)(V_{CS} - V_S)}{C_S \times V_{CS}(2V_S - V_{CS})} \tag{2-8}$$

where T is the switching period, V_o is the output voltage, and V_s is the peak of the secondary voltage. The power losses in the resistor depend on the voltage differences between the clamped voltage V_{cs} and output voltage V_o,. These can be calculated by:

$$P_{loss} = \frac{(V_{CS} - V_o)^2}{R_S} \tag{2-9}$$

The power losses in the clamp circuit are the main disadvantage of this topology, and a compromise between the clamp voltage V_{cs} and the power dissipation in R_s needs to be optimized [91, 92].

2.3 Zero-Voltage Switching Full-Bridge with Active Snubber

The power losses in the snubber circuit discussed in the previous section can reach high levels, which reduce the efficiency of the converter. Hence a lossless snubber circuit shown in Figure 2-4 was proposed [93]. The snubber circuit consists of an active bi-directional switch (MOSFET) in a series with a large capacitor. When the secondary voltage v_s rises above the snubber capacitor voltage v_{cs}, the snubber MOSFET body diode is forward biased and the snubber capacitor *Cs* is placed in parallel to the rectifier. The leakage inductance and the capacitor resonate at low frequencies in comparison to the switching frequency, because of the large capacitance. This results in the rectifier voltage being clamped to the snubber capacitor voltage V_{cs}. The leakage energy stored in the snubber capacitor is then transferred to the load through the MOSFET.

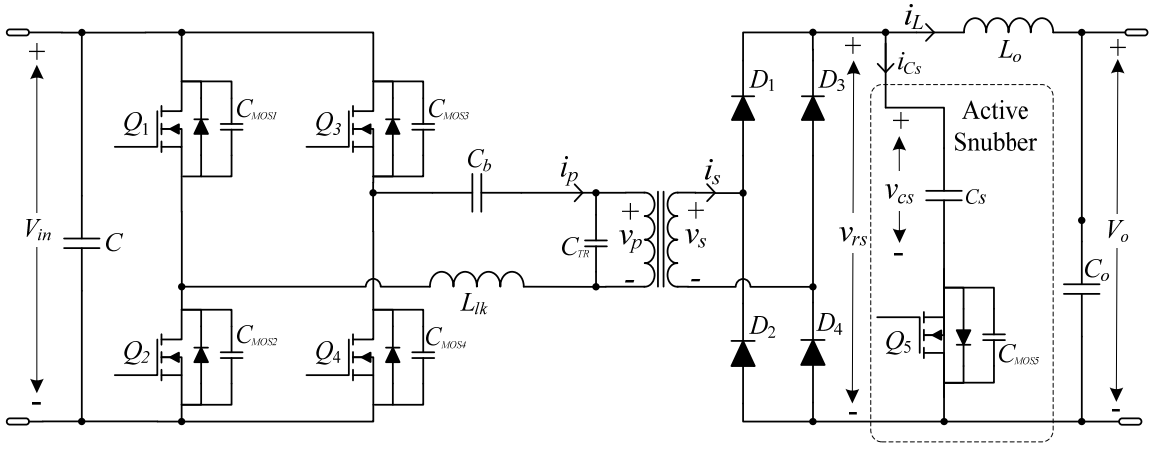


Figure 2-4 Schematic diagram of full-bridge converter with active snubber.

2.3.1 Operation Principle

The full-bridge converter operates the same way as in the conventional ZVS full-bridge converter discussed in Section 2.2. Figure 2-5 shows the typical waveforms of the converter together with the snubber circuit current i_{Cs} and gate signals.

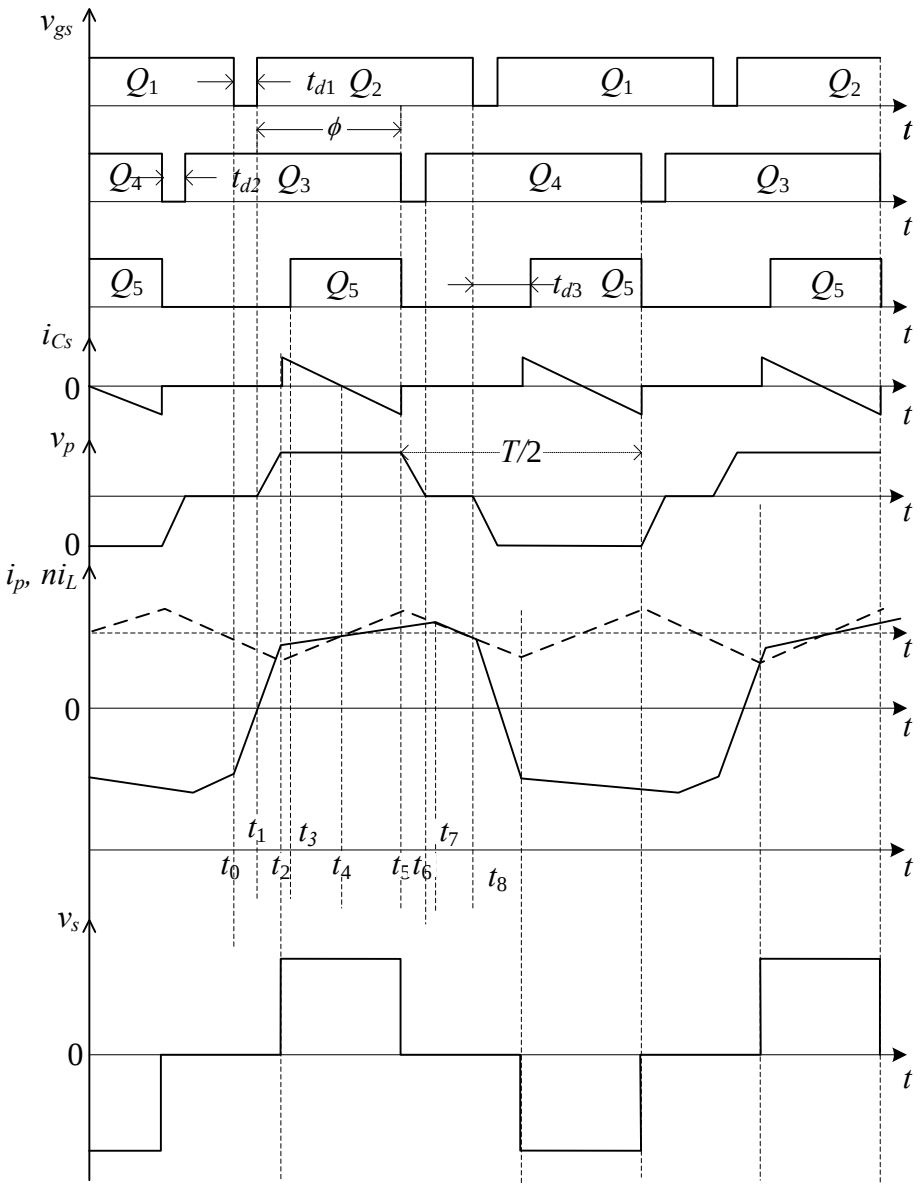


Figure 2-5 Waveforms of ZVS full-bridge converter with active clamp.

The operation of the converter during each half cycle of the switching period can be divided into the following seven modes:

Mode 1 t_0-t_1: The half cycle begins at the end of the freewheeling cycle when Q_1 is turned off at t_0. The primary current i_p, which is maintained by the leakage inductance L_{lk} during freewheeling, charges the capacitor of Q_1 and discharges the capacitor of Q_2. The primary current i_p then continues through the body diode of Q_2 and turns it on. The input voltage is now

applied across the transformer primary side, but the secondary is still shorted (v_s = 0) by the freewheeling current through the output rectifier.

Mode 2 t_1-t_2: At t_1, device Q_2 is turned on with ZVS. The primary current increases at the rate of V_{in}/L_{Lk} until it reaches the reflected output current ni_L. The freewheeling process ends at t_2 and the input voltage is applied to the transformer primary (v_p=V_{in}).

Mode 3 t_2-t_3: At t_2, the secondary winding is no longer short-circuited. The clamp MOSFET body diode becomes forward-biased and turns on. The clamp capacitor connected across the secondary acts as a constant voltage source and clamps the rectifier voltage.

Mode 4 t_3-t_4: At t_3, the clamp MOSFET is turned on with ZVS, the secondary current i_s supplies the inductor current, and charges the clamp capacitor.

Mode 5 t_4-t_5: At t_4, the inductor current i_L reaches i_s. The clamp current i_{Cs} reverses polarity and begins to supply the inductor current, thus transferring the stored energy in the snubber capacitor to the load.

Mode 6 t_5-t_6: The preset duty cycle ends at t_5, and MOSFETs Q_3 and Q_s are turned off. The primary current i_p charges Q_3 capacitor and discharges the Q_4 capacitor. Then the primary current i_p flows through the body diode of Q_4 and turns it on.

Mode 7 t_6-t_7: At t_6, Q_4 is turned on with ZVS. At t_7, the reflected inductor current reaches the primary current. This concludes the first half cycle. An identical operation occurs in the second half cycle of the switching period.

2.3.2 Effect of Snubber MOSFET Capacitance in Step-up Converters

The primary current observed in practical circuits is usually different from the theoretical one as shown in Figure 2-6. This difference is mainly due to the snubber MOSFET output capacitance C_{MOS}, which affects the shape of the current and increases the peak value of the primary current, while the average value is unchanged. Before the MOSFET body diode turns on, the MOSFET can be modeled with its output capacitor. The snubber circuit can be simplified to the equivalent capacitance of the clamp capacitor and the MOSFET output capacitor in series. The resonance of the leakage inductance and the output capacitance of the MOSFET, together with the rectifier diodes capacitance, results in the primary current increasing sharply at the beginning of the power transfer period.

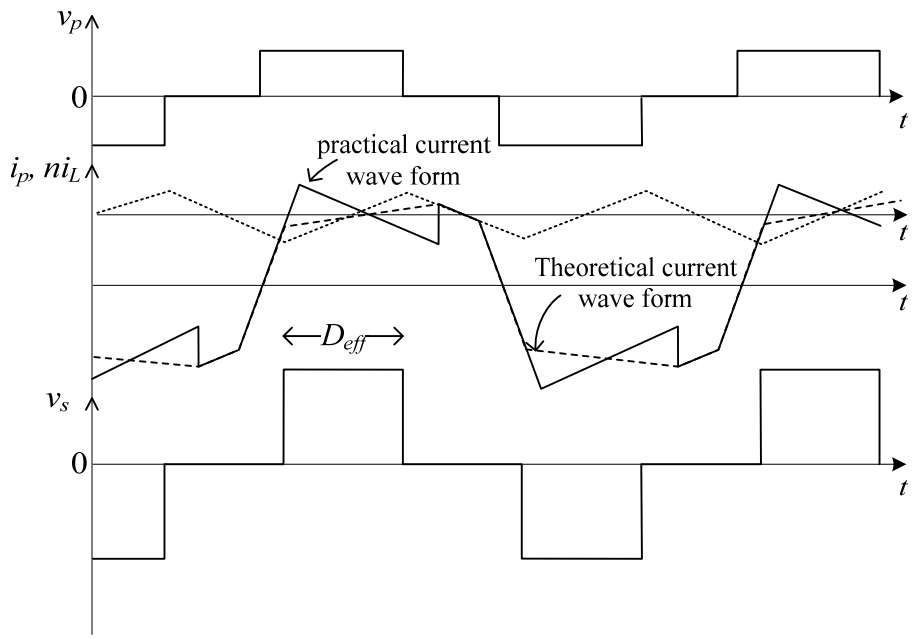


Figure 2-6 Practical waveforms of ZVS full-bridge with active clamp.

The equivalent model of the converter referred to the primary side during the power transfer period is shown in Figure 2-7. And the primary current during the on time is shown in Figure 2-8.

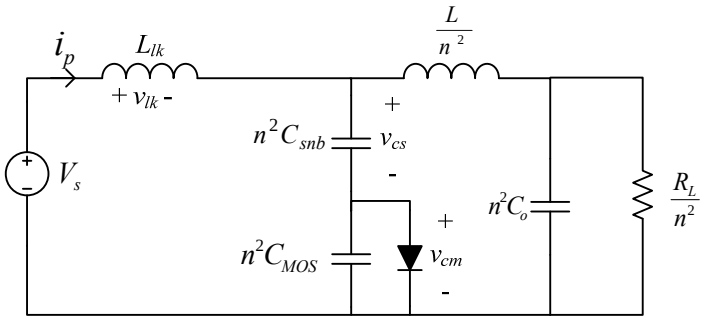


Figure 2-7 Equivalent model of the snubber circuit.

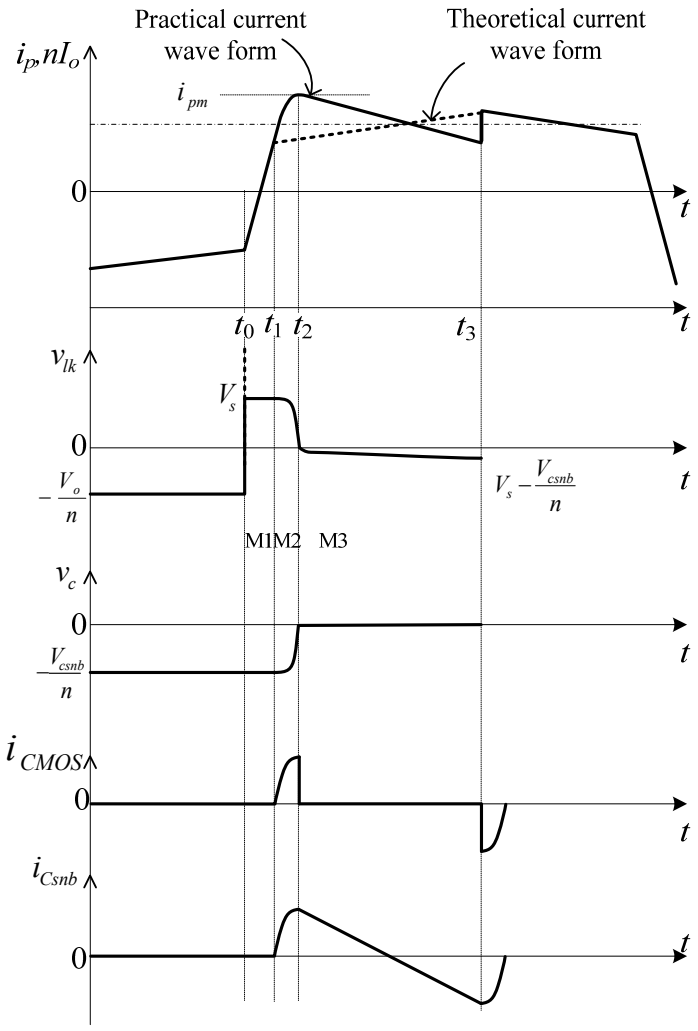


Figure 2-8 Voltage and current waveforms of the snubber circuit.

During this period, the diagonal MOSFETs are turned on, and the input voltage is applied to the transformer, which is modeled by the leakage inductance L_{Lk}. The output inductor, output capacitor and the load are referred to the primary side of the transformer. The snubber MOSFET is modeled by its output capacitance C_{MOS} and the anti-parallel diode since it is off during the beginning of the period. The snubber capacitor and the MOSFET capacitance are also referred to the primary side.

The primary current goes through three stages:

Mode 1 $t_0 - t_1$: The transformer secondary is short-circuited by the freewheeling diode and all the input voltage is applied to the leakage inductance as shown in Figure 2-9.

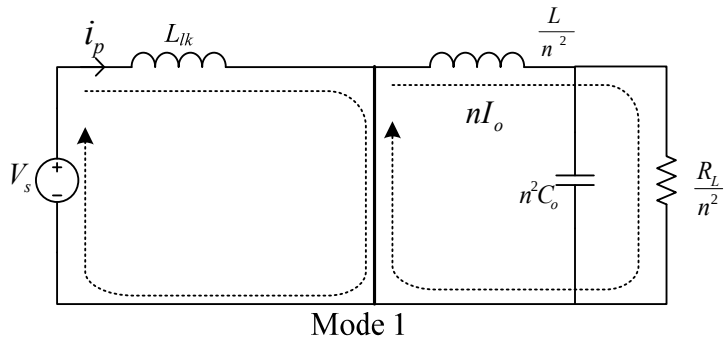


Figure 2-9 Equivalent model of the snubber circuit in Mode 1.

The primary current rises at a slope proportional to the leakage inductance, as shown in Figure 2-8 and given by

$$\Delta i_p = \frac{V_s \Delta t}{L_{lk}} \tag{2-10}$$

This mode ends when the primary current i_p reaches the reflected output current, as shown in Figure 2-10.

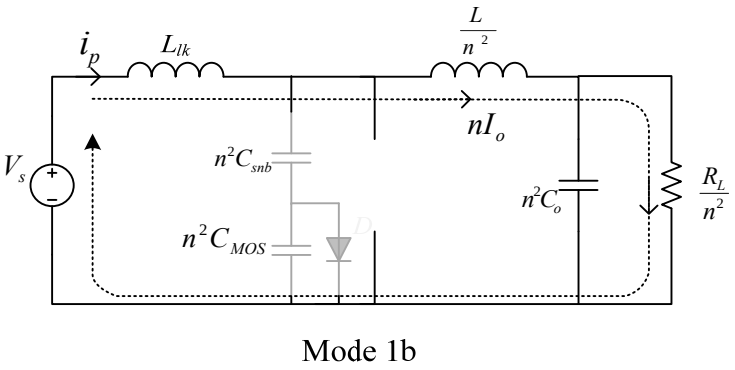


Figure 2-10 Equivalent model of the snubber circuit at the end of Mode 1.

Mode 2 t_1-t_2: After the primary current i_p reaches the reflected output current nI_o, the rectifier diodes are turned off with zero current and no reverse recovery losses occur. The short circuit on the transformer secondary is removed and the equivalent model becomes the same as that shown in Figure 2-11. Since the snubber capacitor C_{snb} is much larger than the MOSFET capacitor C_{MOS}, it can be considered a constant voltage source. The leakage inductance begins to resonate with the snubber MOSFET output capacitor. The primary current can be divided into two

components. The first component is the reflected inductor current nI_o, and the second is the resonant current i'_p of the leakage inductance and the snubber MOSFET capacitor. The equivalent circuit for the second component is shown in Figure 2-11b).

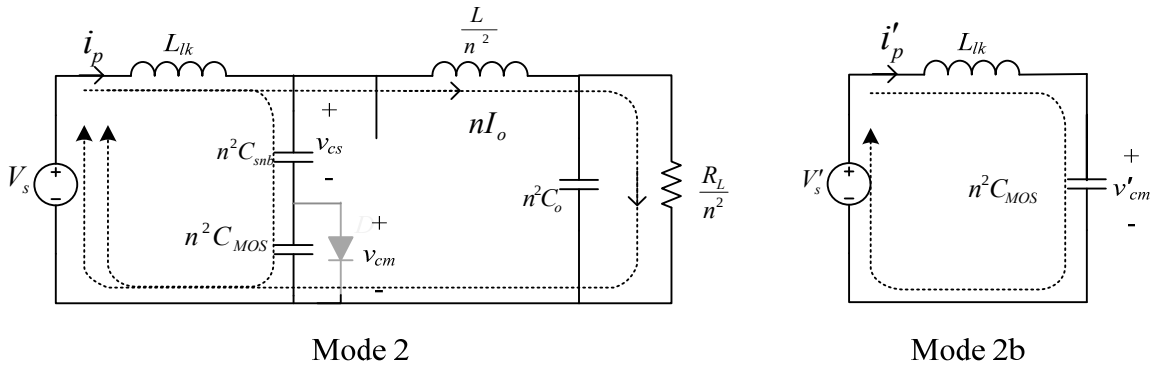


Figure 2-11 Equivalent model of the snubber circuit Mode 2 and 2b.

Applying KVL to the equivalent model, we obtain:

$$-V'_s + L_{lk}\frac{di'_p}{dt} + v'_{cm} \tag{2-11}$$

where $V'_s = V_s - V_{cs} \cong 0$

Since the snubber capacitor voltage during steady state is almost equal to the transformer secondary voltage. When it is reflected to the primary side, it will be equal to the supply voltage. The capacitor current is defined by

$$i'_p = C_{eq}\frac{dv'_{cm}}{dt} \tag{2-12}$$

where C_{eq} is the equivalent capacitance of the C_{MOS} and C_{snb} in series referred to the primary side, given by $C_{eq} = n^2\left(\frac{C_{MOS} \bullet C_{snb}}{C_{MOS} + C_{snb}}\right)$.

Substituting (2-12) into (2-11) yields

$$\frac{d^2v'_c}{dt^2} + \frac{v'_{cm}}{L_{lk}C_{eq}} = 0 \tag{2-13}$$

Solving the above differential equation with the initial condition of $v'_{cm}(0^-) = -V_{cs} \cong -V_s$, we have:

$$v'_{cm} = -V_s(1-\cos\omega t) \quad \text{where} \quad \omega = \frac{1}{\sqrt{L_{lk}C_{eq}}} \tag{2-14}$$

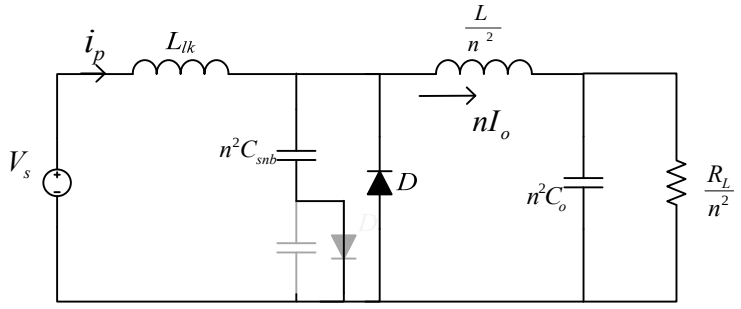
Substituting (2-13) into (2-12), the referred primary current of the transformer can be calculated by

$$i'_p = V_s\sqrt{\frac{C_{eq}}{L_{lk}}}\sin\omega t \tag{2-15}$$

The total primary current is then defined as $i_p = nI_o + i'_p$, and its maximum current is reached when the capacitor voltage v'_{cm} reaches zero at $\omega t = \frac{\pi}{2}$. The peak primary current is given by:

$$i_{pm} = nI_o + V_s\sqrt{\frac{C_{eq}}{L_{lk}}} \tag{2-16}$$

Mode 3 t_2-t_3: When the voltage across the MOSFET becomes zero, the anti-parallel diode turns on, as shown in Figure 2-12. The voltage across the leakage inductor becomes slightly negative due to the increase in snubber capacitor voltage. The primary current decreases whereas the output current increases. When the reflected load current exceeds the primary current, the current in the snubber capacitor reverses direction and begins to supply the load current together with the primary current.



Mode 3

Figure 2-12 Equivalent circuit of the converter operating in Mode 3.

This current spike is common in most full-bridge converters with an active snubber [94-96]. It is more significant in step-up converters, since the snubber switch capacitance is multiplied by the square of the turn's ratio when referred to the primary side. Special attention should be taken when considering the primary current protection, since its peak value occurs at the beginning of the power period and not at the end of it as in the conventional full-bridge converter. Thus, a primary peak current protection is not effective any more. This phenomenon is investigated and verified by simulation and the experimental results given in Section 2.5.2.

2.4 Proposed Zero-Voltage Zero-Current Switching Full-Bridge with Active Snubber

The freewheeling current mentioned in the previous section results in high conduction losses. In order to eliminate the circulating current, the primary current should be reset to zero at the end of each power delivery period, which results in the zero current turn off switching of the MOSFETs.

Many ZVZCS converters in literature require additional components to reset the freewheeling current. Usually the losses associated with these components reduce the overall efficiency of the converter. The converter in [97] uses the same active clamp mentioned in Section 2.3 to reset the primary current, but the clamp switch is operated in hard switching, which increases the losses of the clamp switch. In converter [98], the active clamp switch is turned on with ZVS, but it requires an extra auxiliary inductor and separated input source voltages.

To solve the above-mentioned problems, a novel switching scheme is proposed without any additional components to rest the primary current. This scheme achieves ZVS in the leading-leg, ZCS in the lagging leg, and ZVS in the clamp switch. The schematic of the converter is shown in Figure 2-13.

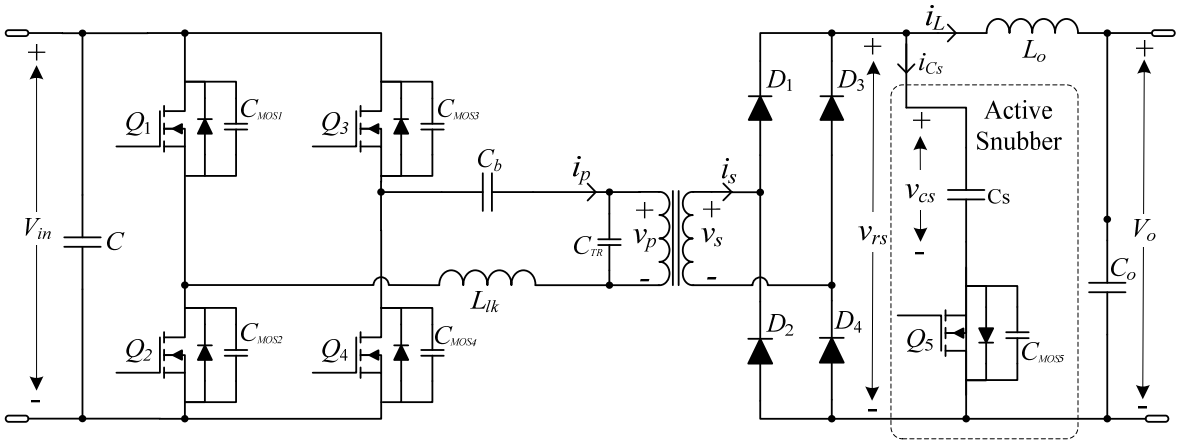


Figure 2-13 Schematic diagram of ZVSZCS full-bridge converter with active snubber.

The freewheeling current circulates in the primary circuit at the end of the power transfer cycle, and is maintained by the leakage inductance and load current. In the new switching scheme, the active clamp gate is prolonged after the power transfer period, which results in a negative voltage applied across the leakage inductance since the voltage across the primary winding is zero. This forces the primary current to sharply decrease to zero and the load current to freewheel through the diode rectifier.

The proposed soft switching technique has the following features:

- It does not require any additional circuit components;
- The clamp switch is turned on with zero voltage, reducing the power losses further;
- It resets the transformer primary current to zero, resulting in a reduction of conduction losses; and
- The prolonged duration of the clamp switch increases the effective duty cycle and can be seen as a compensation for the T_{on} loss due to the leakage inductance.

2.4.1 Operation Principle

The full-bridge converter is operated in the same way as in the conventional ZVS full-bridge converter. The energy stored in the leakage inductance is transferred to the snubber capacitance through the snubber MOSFET body diode and then transferred to the load through the MOSFET.

Figure 2-14 shows the typical waveforms of the converter. The operation during the half cycle can be divided into 7 modes:

Mode 1 t_1-t_2: At t_1, the primary current is zero and the inductor current is freewheeled through the rectifier. Q_2 is turned on, with ZCS, since the primary current cannot change instantaneously. The primary current increases at a slope defined by V_{in}/L_{Lk} until it reaches the reflected output current ni_L.

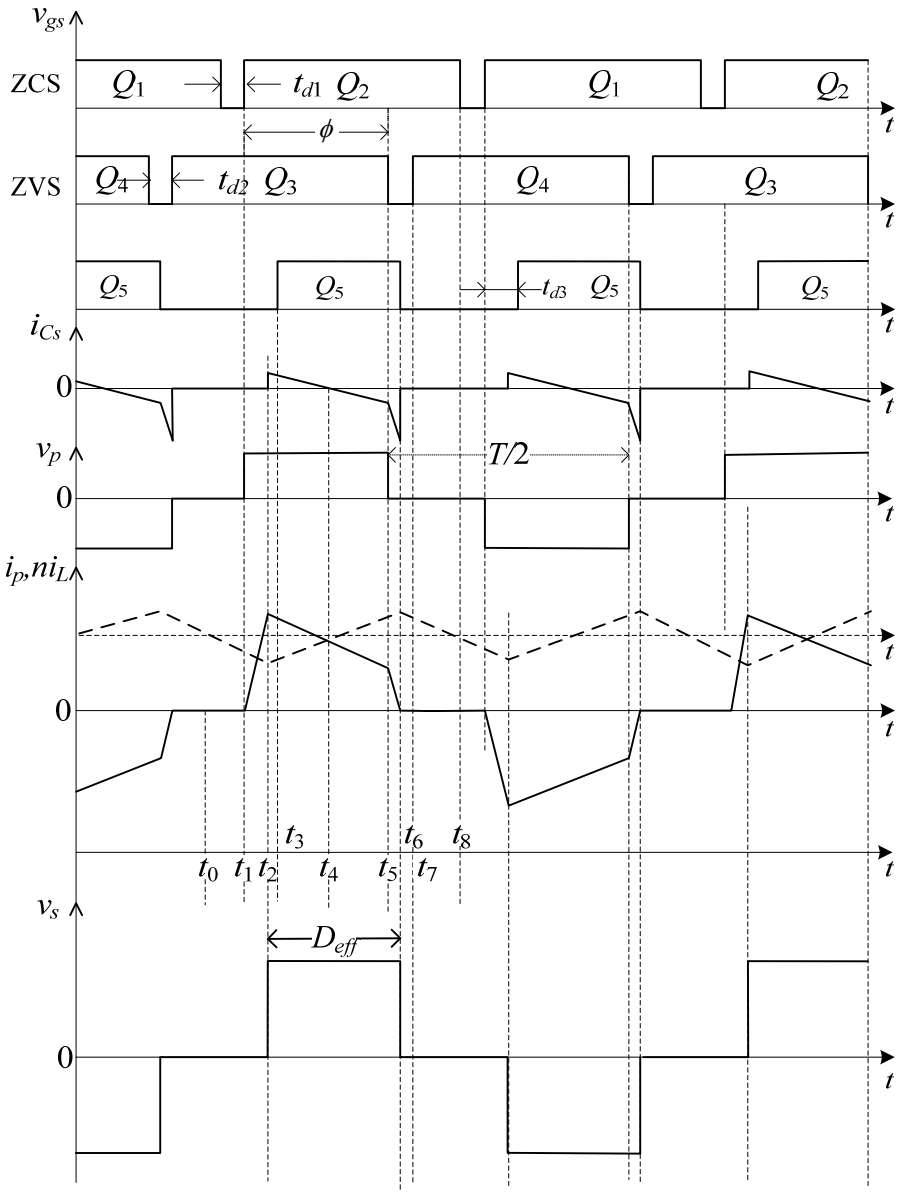


Figure 2-14 Operation waveforms of ZVZCS full bridge with active clamp.

Then, as explained in the previous section, the leakage inductance resonates with the clamp MOSFET capacitance and the current continues to increase until the clamp MOSFET output capacitor is discharged.

Mode 2 t_2-t_3: At t_2, the clamp MOSFET body diode turns on and the clamp capacitor resonates with the leakage inductance and clamps the rectifier voltage.

Mode 3 t_3-t_4: At t_3, the clamp MOSFET is turned on with ZVS. The secondary current i_s supplies the inductor current and charges the clamp capacitor. Since the reflected clamp voltage V_{cs} is higher than the input voltage, the primary current decreases at a slope given by $(V_{in}-V_{cs})/nL_{LK}$.

Mode 4 t_4-t_5: At t_4, the secondary current i_s reaches i_L, and the clamp current i_{Cs} reverses its polarity and begins to supply the inductor current. The primary current continues to decrease at the same slope.

Mode 5 t_5-t_6: The preset duty cycle ends at t_5 and MOSFET Q_3 is turned off. The energy stored in the leakage inductance charges the Q_3 capacitor and discharges the Q_4 capacitor, ensuring the ZVS turn-on for Q_4. The primary current i_p decreases as it freewheels in Q_2 and D_{Q4}. The reflected clamp capacitor voltage reduces the primary current at the rate of $-V_{cs}/nL_{LK}$ until it reaches zero.

Mode 6 t_6-t_7: After the primary current reaches zero, the clamp MOSFET Q_s can be turned off at t_6. At t_7, Q_4 is turned on with ZVS.

Mode 7 t_7-t_8: The inductor current freewheels through the rectifier diodes. This half cycle ends when Q_2 is turned off with ZCS at t_8. An identical operation occurs in the second half cycle of the switching period.

The simulation and experimental results of the proposed ZVZCS FB converter with active clamp are discussed in following section.

2.5 Simulation and Experimental Verification

To compare and verify the performance of the three converters presented in this chapter, computer simulation using Pspice is carried out. The design parameters of the converters are given in Table 2-1. These parameters are obtained from the design of a 1.8kW DC/DC converter built in the laboratory, and the result of the simulation is later compared to experimental data.

The design procedure for the converters is given in the Appendix. The MOSFET switches and the high-frequency transformer in the simulation model use non-ideal models, such that the efficiency and the power losses of these converters can be evaluated.

Table 2-1 DC Converter Parameters

Parameters	Value	Parameters	Value
Rated output power	1800W	Transformer leakage inductance L_{lk}	0.5μH
Rated input voltage	160V	Output filter inductance L_o	315μH
Rated output voltage	400V	Output filter capacitance C_o	2μF
Transformer turns ratio n	28/8	Switching frequency f_s	200kHz

2.5.1 ZVS Full-Bridge Converter with Passive Snubber

The converter shown in Figure 2-3 is simulated with snubber resistor R_s =3KΩ and capacitor C_s=1μF. Figure 2-15 shows the secondary rectified voltage, primary current and voltage of the transformer. The snubber circuit limits the secondary voltage to the snubber capacitor voltage, but cannot eliminate the ringing. As mentioned earlier, the frequency of the ringing is a function of the leakage inductance, the equivalent of the transformer capacitance, and the diode capacitance.

The power losses on the snubber resistance are estimated to be 18W at the full load, the losses in the rectifier diodes are 42.4W, and the losses of MOSFETs are 64.3W. The detailed breakdown of the losses of the main components is shown in Table 2-2 . The losses in the snubber resistor are approximately 1% of the output power. The losses in the rectifier diodes are also high due to the ringing at the rectifier output. The total efficiency of this converter can be calculated by $\eta = P_{out} / P_{in}$ = 1809W / 1972W= 91.73%

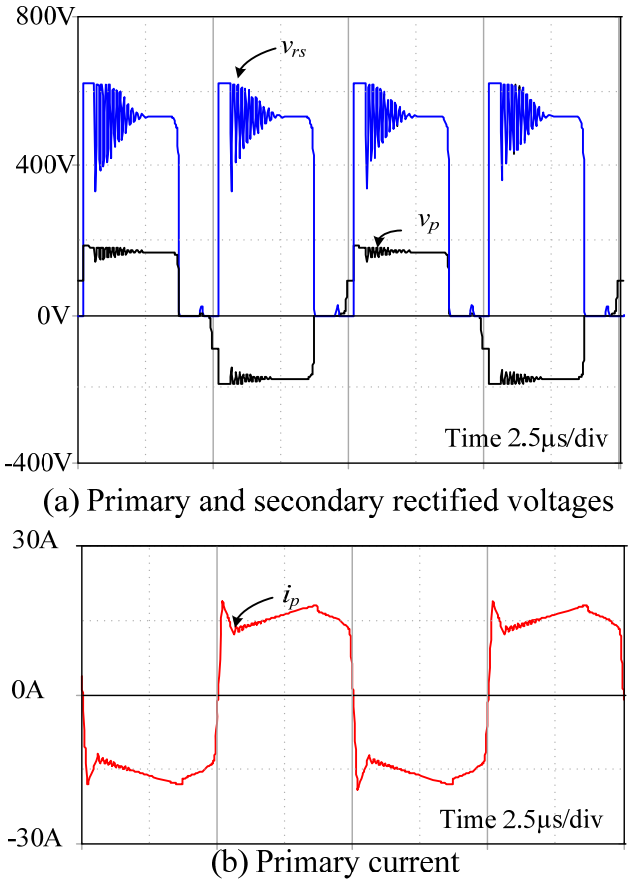


Figure 2-15 Simulation results of the ZVS full-bridge converter with an RCD snubber.

2.5.2 ZVS Full-Bridge Converter with Active Snubber

The converter with active snubber shown in Figure 2-4 is simulated, and the results are illustrated in Figure 2-16. It is obvious that the ringing of the secondary voltage is eliminated and the voltage is clamped. The power losses in the rectifier diodes are reduced by 25% (31.8W) at full load. The losses in the transformer are also reduced. However, the MOSFET losses remain the same. The snubber circuit losses are reduced to 2.36W compared to 18W in RCD circuit and the efficiency increased to 92.7%. Also the peak in the primary current due to the clamp switch capacitance (discussed in Section 2.3.2) is apparent. A detailed breakdown of losses of the main components is shown in Table 2-2 .

The experimental waveforms of the converter primary voltage, secondary voltage and primary current are shown in Figure2-17. These coincide with the theoretical ones in Figure 2-5 and the simulation results in Figure 2-16.

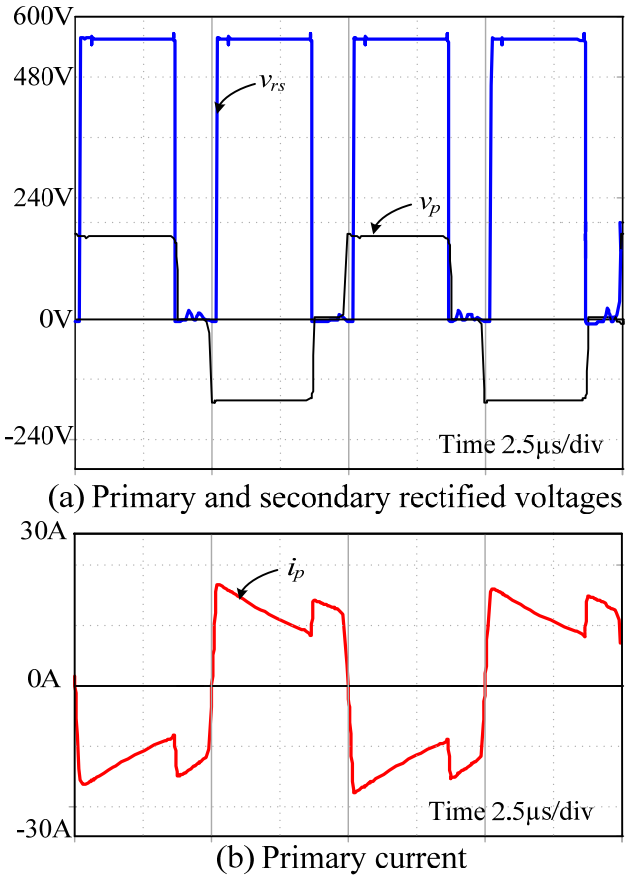


Figure 2-16 Simulation results of the ZVS full-bridge converter with an active clamp.

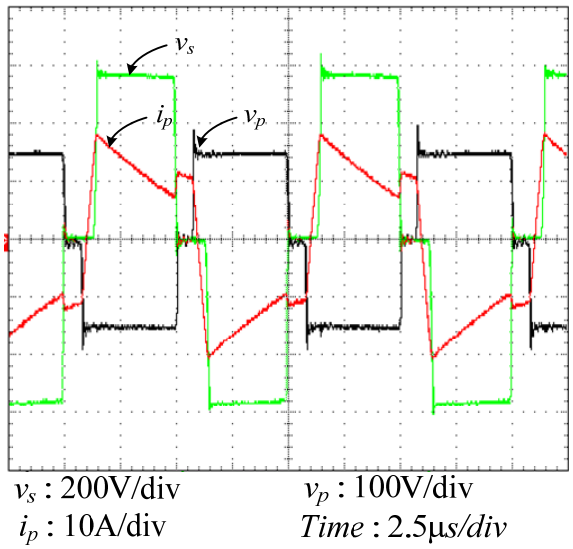


Figure 2-17 Measured waveforms of the ZVS full-bridge converter.

2.5.3 ZCZVS Full-Bridge Converter with Active Snubber

The proposed ZCZVS converter is also simulated with the gating scheme discussed in Section 2.4. The simulation results are shown in Figure 2-18. In addition to eliminating the ringing in the secondary voltage, the snubber circuit is used to rest the primary current and to achieve zero current switching. The rectifier diode losses are further reduced 12% to 28.3W and the transformer losses are reduced from 6.3W to 4.8W since the freewheeling current is no longer circulating through the transformer. The MOSFET losses dropped from 62.2W to 43.4W, and the efficiency increased to 94%.

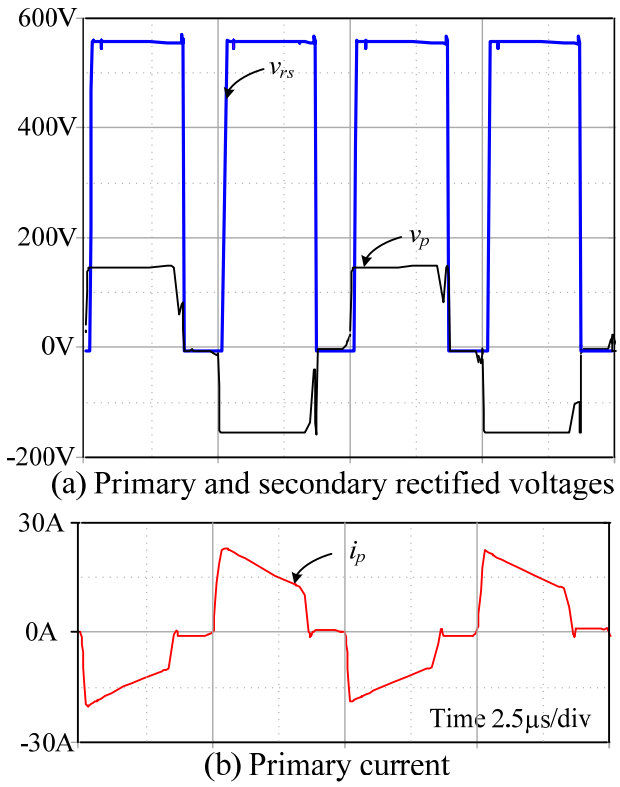


Figure 2-18 Simulation results of ZVZCS full-bridge converter with active clamp.

The experimental waveforms of the primary voltage, the current and secondary voltage are shown in Figure 2-19. The reset of the primary current is obvious and the ringing at the secondary voltage is totally eliminated.

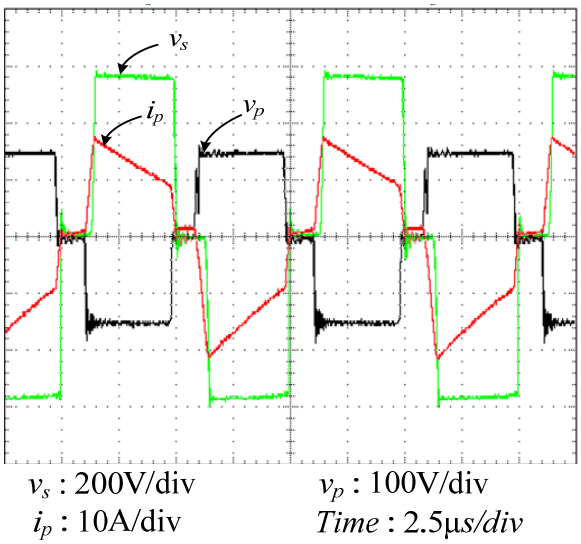


Figure 2-19 Measured waveforms of the ZVZCS full-bridge converter.

2.5.4 Efficiency Improvements

The results of the simulation of the three converters are summarized in Table 2-2.

Table 2-2 Component Power Losses

Components	Losses or RCD	Losses of ZVS	Losses of ZVZCS
Q_1	15.5W	15.23W	11.3W
Q_2	16.6W	16.3W	10.5W
Q_3	15.4W	14.5W	11.2W
Q_4	16.8W	16.2W	10.4W
Transformer	8.8W	6.3W	4.8W
Diodes D_1-D_4	42.4W	31.8W	28.3W
Snubber Resistor	18W	0	0
Snubber switch	0	2.36W	1W
Total Losses	133.5W	102.69W	77.5W
P_{out}	1806W	1842W	1845W
P_{in}	1972W	1988W	1960W
Efficiency	91.6%	92.7%	94.13%

The power losses of the MOSFET do not change substantially between the RCD converter and the ZVS converter, since the primary current wave form is the same in both cases. The MOSFET losses in the ZVZCS converter are much lower due to the elimination of the freewheeling current and the zero current turn-off of the lagging leg. The losses of the diodes are also reduced in the ZVS and ZVZCS converter due to the elimination of the ringing. Total losses in the switches and the transformer of the ZVS converter are 68.53W, while in the ZVZCS converter these losses are reduced to 48.2W. The losses in the clamp switch are also reduced in the ZVZCS converter.

Figure 2-20 shows the experimental results of the efficiency for the ZVS and ZVZCS converters at different power levels. The efficiency of the ZVZCS is always higher throughout the power range of the converters. This is due to the elimination of the freewheeling current and the reduction of the turn-off losses of the passive leg MOSFETs.

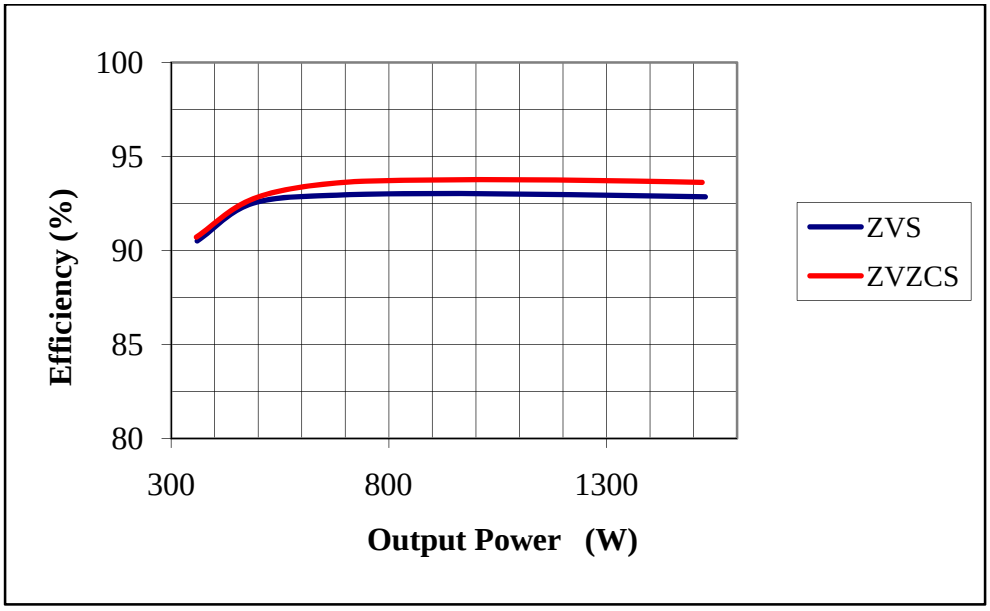


Figure 2-20 Measured efficiency of ZVS and ZVZCS full-bridge converters.

2.6 Conclusion

This chapter investigates two types of soft-switched full-bridge converters: the ZVSFB converter with RCD snubber and the ZVSFB converter with active clamp. The operating principles of these converters are explained and the effect of the clamp MOSFET capacitance is discussed. A new gating scheme for the ZVSFB converter with the active clamp, which realizes

zero-voltage and zero-current switching, is proposed. The operation principles of the proposed scheme are presented, and its performance is investigated. This new method does not require any additional hardware and yet is able to boost the duty-cycle to compensate for the duty-cycle loss while the clamp switch is turned on with ZVS. Comparison of simulation results proves that the proposed scheme reduces the power losses of the MOSFETs and the transformer by 30% at the rated output power. The close match between the experimental and simulation results show that the proposed ZVZCS full-bridge maintains better efficiency throughout the load spectrum and achieves an efficiency of 94% at full load. Both simulation and experimental results verify the operational principles of the proposed scheme and its improvement of the efficiency of the converter.

Chapter 3
Digital Control of Multiphase Interleaved DC/DC Converters

3.1 Introduction

The DC/DC power converters presented in Chapter 2 for PV energy conversion systems are in the power range of a few kilowatts, but their maximum power is limited due to the physical limitation of the magnetic components and MOSFET switches. However, a larger power rating can be achieved by paralleling converters [99, 100]. With converters in parallel, each converter processes part of the total power in order to reach a higher power level and better power quality. A parallel DC/DC conversion system is shown in Figure 3-1, where multiple units of DC/DC converters are connected in parallel to increase the power rating of the PV energy systems and a DC/AC inverter is used to deliver the PV energy to the grid.

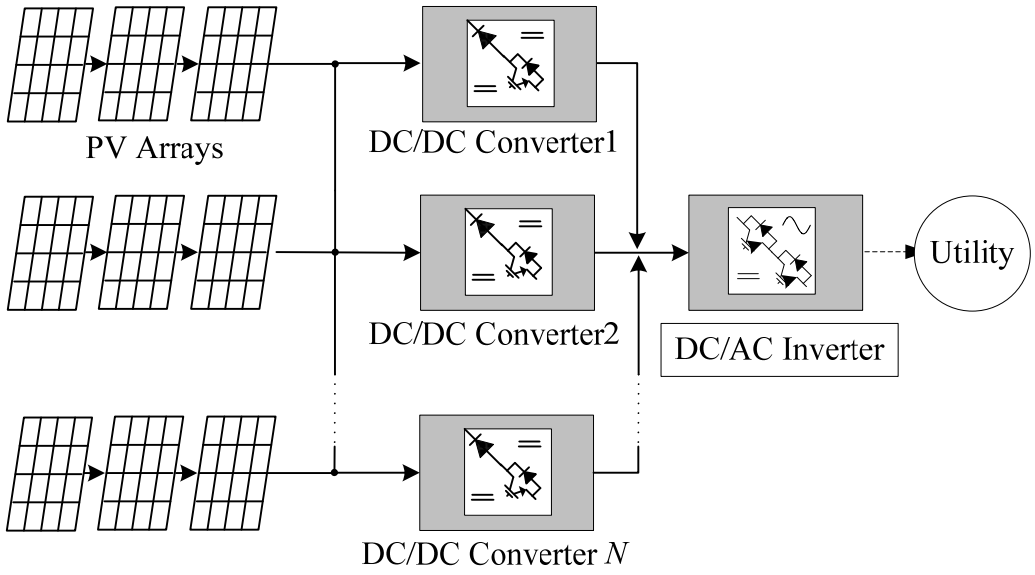


Figure 3-1 Parallel multiphase DC/DC power conversion system.

Interleaving technology is used to reduce the input and out voltage ripples in parallel connected converters. In interleaving, all the converters are operated at the same switching frequency but phase shifted among each other over the switching period. Converters working with interleaving technology are usually called multiphase converters.

In a PV energy conversion system, the input voltage ripples increase the oscillation around the maximum power point of the PV array. Consequently, multiphase converters reduce the input voltage ripple, resulting in increasing the energy yield from the PV array. Furthermore, the multiphase converters require smaller output filter components due to the reduction of the output voltage ripples.

To develop a control scheme for the multiphase converter-based PV energy system, it is necessary to: 1) control the input voltage of the converter to achieve maximum power point tracking; 2) ensure even current distribution among the parallel converters [101, 102]; and 3) limit the output voltage in case the available PV power is higher than the load demand. These requirements, combined with the non-linear characteristics of the PV arrays and converters, lead to a complex control system that is difficult to analyze and design.

This chapter describes a novel cascade control scheme to control the multiphase DC/DC converter systems. The cascade controller divides the control system into multi-loops that are simpler to analyze and design. This proposed control scheme is developed to control the PV array voltage and to enforce current sharing among the converters. In addition, the design of the control loops of the system, together with the small signal models, is presented. The performance of the system under changing irradiance and temperature is verified by simulation. Finally, a 5.4kW prototype PV conversion system with three parallel converters using the proposed control scheme is developed and tested.

3.2 Interleaved Converter System Operation

The interleaving of converters is used to enhance input and output current waveforms by reducing the ripple amplitude and increasing ripple frequency [100]. This also results in a reduction in the filter components such as capacitors and inductors. The paralleling of the converters enhances the transient response and improves dynamic performance and reliability [103, 104]. Figure 3-2 shows an interleaved system of three identical converters.

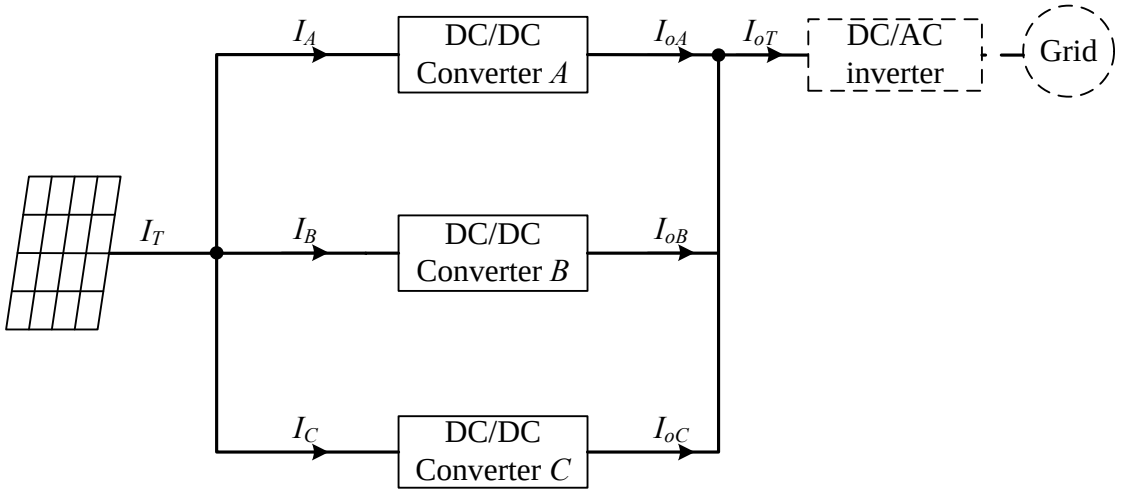


Figure 3-2 Schematic of power conversion system with three interleaved DC/DC converters.

The circuit diagram of the DC/DC power converters in Figure 3-2 is illustrated in Figure 3-3. The converter is essentially the zero-voltage zero-current switching (ZVZCS) converter discussed in Chapter 2, which is the building block for the multiphase PV system. This converter features high energy efficiency and compact physical size, and therefore is selected for use in the proposed PV energy system.

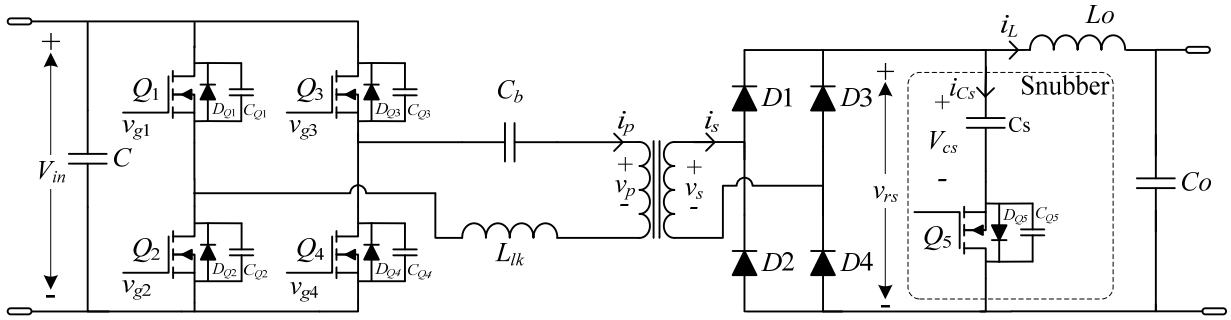


Figure 3-3 Circuit diagram of the ZVZCS DC/DC converter.

In the interleaved system, all the converters are switched at the same frequency, while a phase shift equal to T_s/N is introduced, where T_s is the switching time and N is the number of parallel converters. In the case of a full-bridge converter, the ripple frequencies at the input and output of the converter are twice the device switching frequency. Consequently, only half of the phase shift ($T_s/2N$) is needed between the converters. The converters used for this system uses

phase shift angle ϕ between the two legs of the converter to execute the duty cycle as mentioned in Section 2.4.1:

$$D = \frac{2\phi}{T_s} \quad \text{OR} \quad \phi = \frac{DT_s}{2} \tag{3-1}$$

where D is the duty cycle and ϕ is the phase angle introduced between the gates of the two legs.

In case three converters are interleaved, the MOSFET gate signals are generated according to Table 3-1 and shown in Figure 3-4.

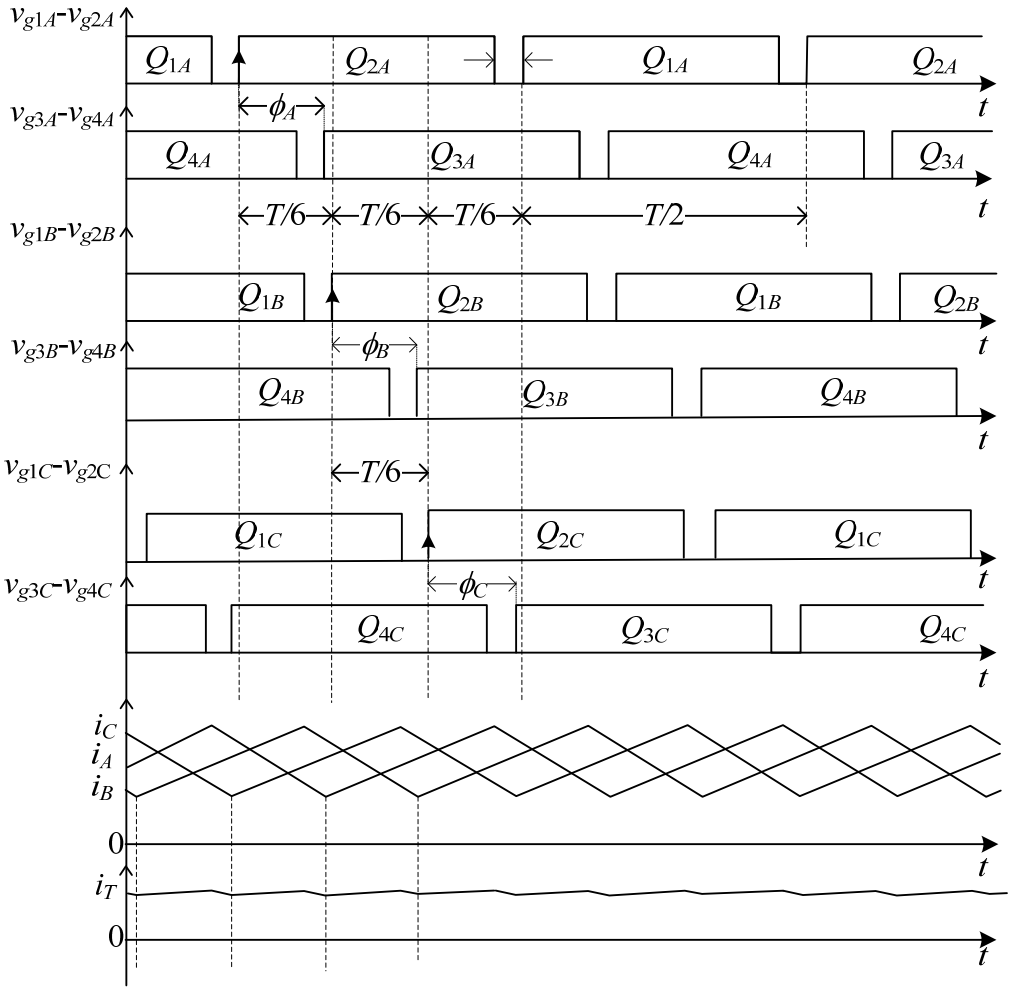


Figure 3-4 Waveforms of the interleaved DC/DC converter system.

Table 3-1 Phase Shift Angle between the Two Legs of the Converter

	Converter *A*	Converter *B*	Converter *C*
Left Leg	Reference	$T_s/6$	$T_s/3$
Right Leg	ϕ_A	$T_s/6 + \phi_B$	$T_s/3 + \phi_C$

The phase shifts of the left legs (LL) are fixed, whereas the phase shift of the right legs (RL) vary as the duty cycle of each converter changes. The LL gate signal of converter *A* is taken as reference and the LL signal of the other converters are shifted by $T_s/6$ and $T_s/3$. The RL gate signal of converter *A* is shifted ϕ_A according to the duty cycle set by the control loops. The shift in the RL gate signal of the other converters is composed from two terms. A fixed term comes from the phase shift due to interleaving of the converters and the variable term comes from the duty cycle control of the converters.

3.2.1 Investigation of the Interleaved Operation

The simulation model in Section 2.5 is used to simulate the behavior of three converters connected in an interleaved parallel. Figure 3-5 shows the gate signals of opposite MOSFTES of the three converters. Each converter signal is shifted 60° from the other converter.

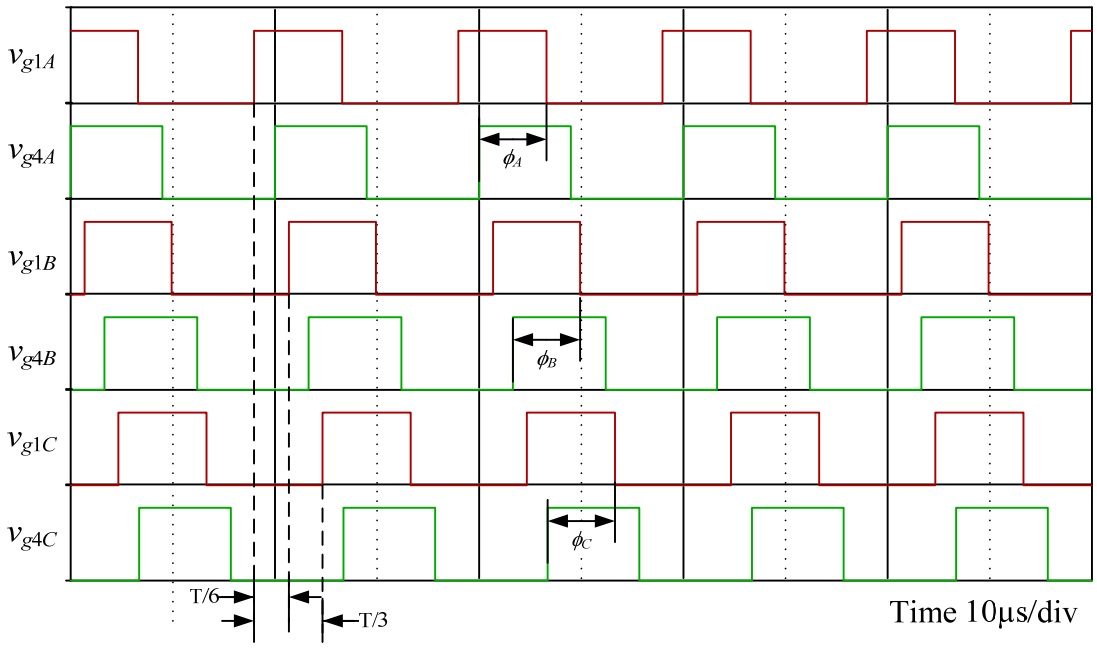


Figure 3-5 Simulated gating signals for the DC/DC conversion system with three interleaved power converters.

Figure 3-6 shows the input currents of the three converters together with the total current. Note that the ripple is canceled in the total current I_T. The cancellation of the ripple in the total current is important for the MPPT. Otherwise, this ripple forces the system to oscillate around the MPP. The ripple in the total output current is also eliminated as shown in Figure 3-7.

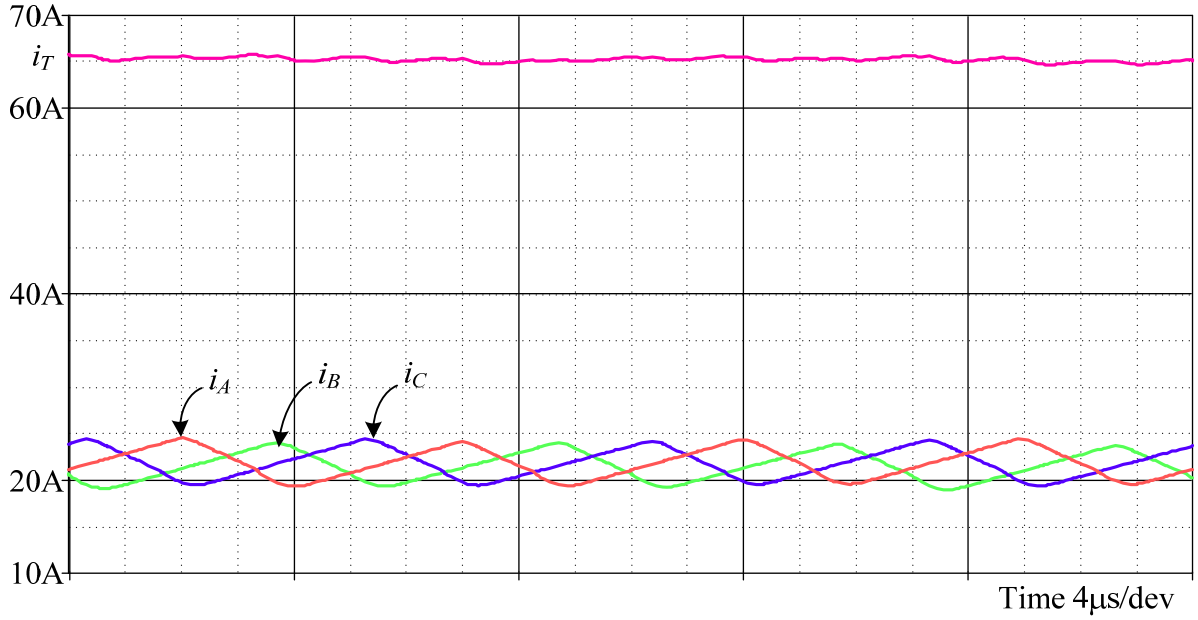


Figure 3-6 Simulated input current waveforms for the DC/DC conversion system with three interleaved power converters.

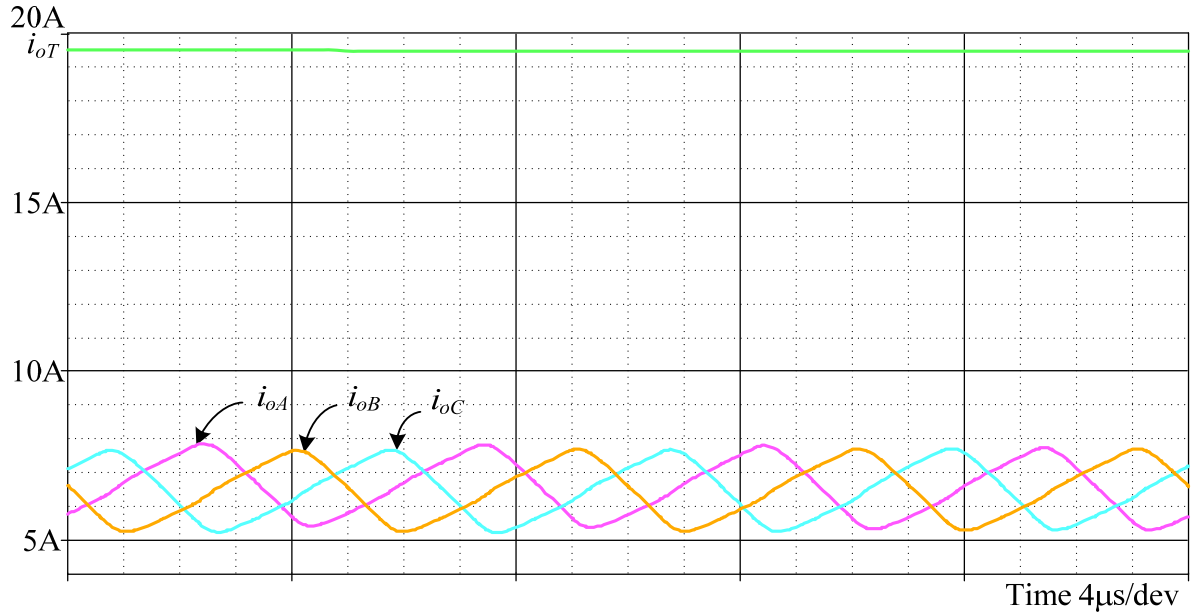


Figure 3-7 Simulated output current waveforms for the DC/DC conversion system with three interleaved power converters.

This results in reducing the filter components and especially the filter capacitor and in eliminating the need for electrolytic capacitor which has a short life span. This change results in the increasing reliability of the system.

3.3 Proposed Control Scheme

The purpose of the controller is to regulate the operation of the system at the desired set point. In the PV system, three parameters are of interest with respect to the controller – the input voltage, the input current, and the output voltage. For off-grid applications the output voltage is usually regulated during the period when load demand is lower than the available PV power. However when the load demand becomes larger, the input voltage should be regulated in order to prevent the array voltage from collapsing [105, 106]. In the case of a grid-tied application, the output voltage of the DC/DC converter is controlled by the DC/AC inverter which controls the amount of power delivered to the grid.

The input voltage is regulated according to the set point determined by the Maximum Power Point Tracking algorithm. As the environmental conditions change, the MPP changes and the MPPT algorithm changes the set point in order to force the system to track the MPP. In multiphase converters the controller should also insure power sharing among the parallel connected converters. So the main objectives of the control system are:

- Automatic and smooth switching between output and input voltage control according to the available PV power and the load power demand;
- Control of the input voltage according to the set point of the MPPT algorithm; and
- Active current sharing between the DC/DC converters.

In order to achieve the above-mentioned objectives of the controller, a multi-loop cascade Master/Slave control system is proposed, as shown in Figure 3-8, where the inner loop will regulate the output voltage while the outer loop controls the PV array voltage in the master converter and the input current in the slave converters.

3.3.1 Cascade Control

Cascade control is widely used in process control applications to divide a control process into two loops where the outer loop variable is controlled by adjusting the set point of the inner loop.

Cascade control has the following advantages:

- Improved dynamic performance of the system;
- Set limits for the inner loop variable;
- Fast recovery from disturbances on the inner loop;
- Outer loop variable are less affected by disturbances; and
- Better control of the outer loop variable.

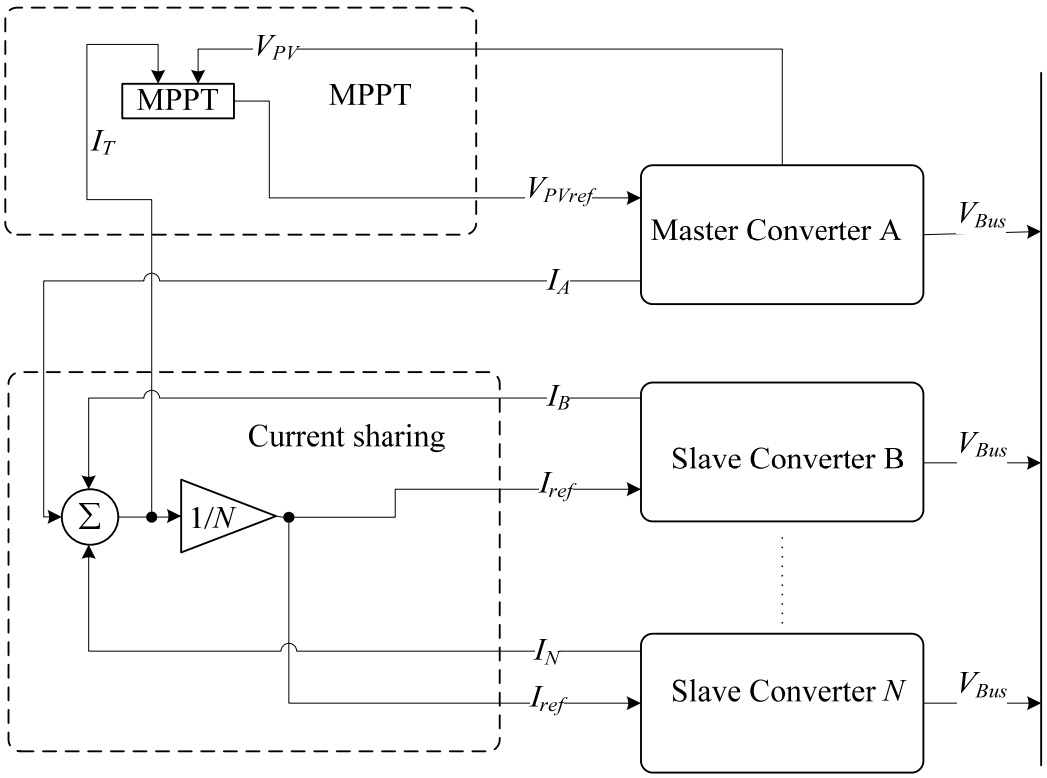


Figure 3-8 Control of the interleaved DC/DC converters.

In the PV system, cascade control will be effective since the output voltage control loop should be fast while control of the input voltage and input current are slow loops. Therefore, the output voltage control loop is set as the inner loop since it requires a fast response to the disturbance, such as a change in the load. The outer loop is designed to be slower, to control the main variables of the system, such as the input voltage in the master converter. It is also designed to offset slow disturbances like change in irradiance and temperature.

3.3.2 Output Voltage Control

The output voltage is controlled by the inner loop of the cascade controller. The set point of the loop is adjusted by the outer loop, either to regulate the input voltage or to force current sharing. In case the PV power is less than demand, the output voltage set point is regulated such that the outer loop variable is controlled either by the MPPT algorithm, in the case of the master converter, or by the current sharing controller as in the case of a slave converter. On the other hand when the PV power is more than the load demand, the outer loop will increase the set point in an attempt to increase the load until it reaches the upper limit of the maximum output voltage.

3.3.3 Input Voltage Control and MPPT

The MPPT algorithm determines the set point for the input voltage control loop for the master converter according to environmental conditions. Then the input voltage control loop will determine the set point of the output voltage control loop. The relationship between the input voltage and the output voltage is reversed. A positive increment in the output voltage will increase the load, thus decreasing the input voltage. The reversed relationship is shown by having a negative gain in the transfer function between the duty cycle variation and the input voltage. Consequently the error is reversed by subtracting the reference from the feedback signal. The reversed error will generate a positive reference for the inner output voltage loop.

3.3.4 Current Sharing

Identical parallel connected converters may not share the current automatically due to discrepancies in their input or output impedances. As a result, these systems usually have active current sharing to force them to share the current. In the proposed PV system, the input current is controlled to ensure that the system is working at the MPP. In the proposed control scheme, the total current of the converters is added and then divided by the number of converters in the system. This creates the reference current for the converters to follow, excluding the master converter which regulates the PV array voltage.

For example, if the system has three converters, one third of the total current is set as the reference for the input current control loop of the second and third converter. This mechanism will force current sharing among the three converters. Since each of the second and third converters get one third of the total current, the first converter is left with one third of the current,

although its input current is not regulated. The current sharing in the proposed scheme is implemented in a single control platform. This eliminates the need for wiring between the converters to achieve current sharing and synchronization.

The above three control tasks will be discussed separately in the following sections. The performance of the whole system will be analyzed at the end of this chapter.

3.4 Controller Design and Stability

The design of the controller to implement the control scheme proposed in the previous section is presented in this section together with the stability analysis of the designed controller. The small signal model for the DC/DC converter is derived, together with the small signal model of the PV array.

3.4.1 Small Signal Model

Small signal models are developed to linearize the system around a steady state operating point. Then the transfer function of the linear system is derived as a relation between two variants to study the effect of one on the other. The controller is designed in such a way that the response to a change in one variant remains bounded and stable.

The electrical model of the PV array was given in Figure 1-5 and the corresponding I-V relation in Eq. (1-1) is highly non-linear. To obtain the small signal model of the PV array, let us consider the I-V characteristics shown in Figure 3-9.

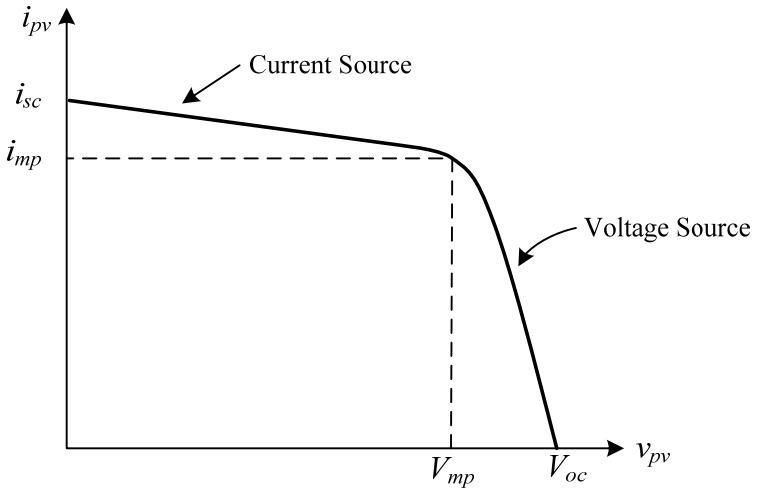


Figure 3-9 PV array I-V characteristics.

The graph can be divided into two linear parts, the horizontal part which can be modeled into a current source with a parallel shunt resistor as shown in Figure 3-10 (a), and the vertical part which can be modeled as a voltage source with series resistor as in Figure 3-10(b) [107].

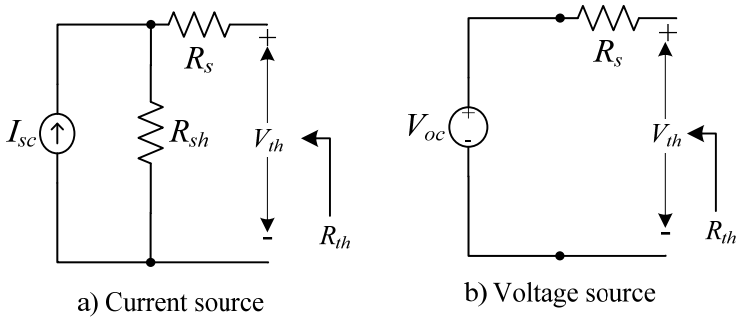


Figure 3-10 PV array equivalent model.

In order to obtain the values of R_s and $R_{sh,}$ the parameters from the datasheet of the PV array can be used as follows:

$$R_s = \frac{V_{oc} - V_{mp}}{I_{mp}} \tag{3-2}$$

$$R_{sh} + R_s = \frac{V_{mp}}{I_{sc} - I_{mp}} \tag{3-3}$$

where V_{oc} is the open circuit voltage, I_{sc} is the short circuit current, V_{mp} is the voltage at the MPP and I_{mp} is the current at MPP obtained from the datasheet of the PV array.

Each model represents a part of the graph, and cannot represent the PV array at all operation points. Thus, both models should be considered during the design of the controller. To simplify the notation, the Thevenin equivalent of the model will be used, as shown in Figure 3-11. The model for ZVZCS full-bridge DC/DC converter is also shown in Figure 3-11. The effect of leakage inductance and phase shifting is accounted for by considering the effective duty cycle $d_{eff} = D_{eff} + \hat{d}_{eff}$ [108]. The perturbation of the effective duty cycle $\hat{d}_{eff}$ is defined as the sum of perturbation due to the change in duty cycle $\hat{d}$, change in inductor current $\hat{d}_i$ and change in input voltage $\hat{d}_v$:

$$\hat{d}_{eff} = \hat{d} + \hat{d}_i + \hat{d}_v \tag{3-4}$$

where $\hat{d}_i = -\frac{R_d}{nV_p}\hat{i}_L$, $\hat{d}_v = \frac{R_d I_L}{nV_p^2}\hat{v}_p$, $R_d = 4n^2 L_{lk} f_s$, L_{lk} is the leakage inductance, V_p is the steady state input voltage and f_s is the switching frequency.

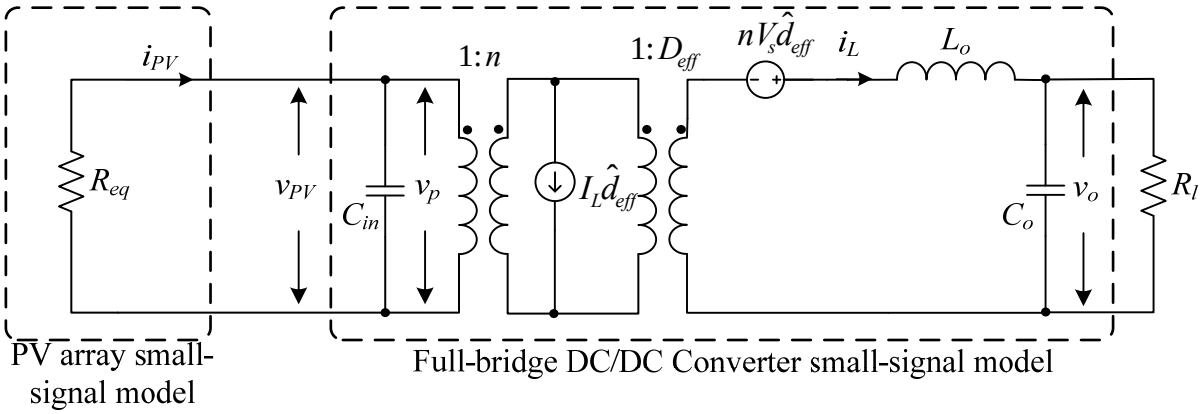


Figure 3-11 Small signal model of DC/DC converter and PV array.

3.4.2 Design of Output Voltage Control Loop

The design of the output voltage controller requires knowledge of a control-to-output voltage transfer function. To determine the transfer function, the PV array voltage is considered constant and is modeled as a constant voltage source. Then, the small signal model reduces to the model shown in Figure 3-12.

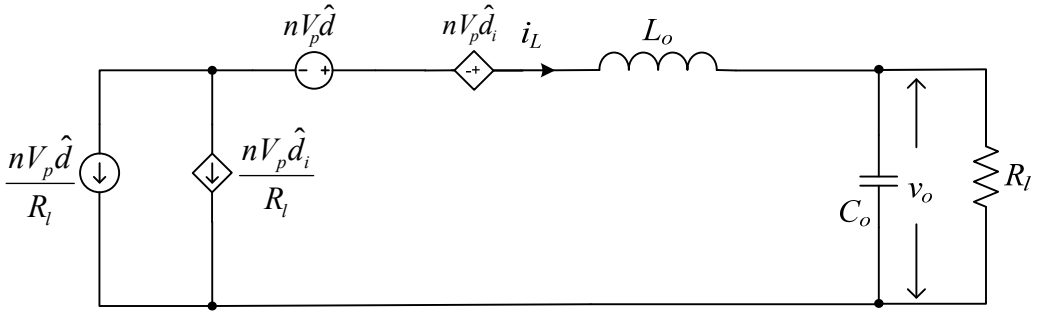


Figure 3-12 Small signal model of DC/DC converter and PV array under constant input voltage.

The above small signal model is used to determine the transfer function of the output voltage to the duty cycle variations:

$$Go_{vd} = \frac{\hat{V}_o}{\hat{d}} \cong \frac{nV_p\omega_0^2}{s^2 + s\left(\frac{1}{R_l C_o} + \frac{R_d}{L}\right) + \omega_0^2} \tag{3-5}$$

where $\omega_0 = \frac{1}{\sqrt{LC}}$.

The output voltage control loop is shown in Figure 3-13 where G_{cA} is the compensator, Go_{vd} is the plant transfer function derived above and H_A is the feedback transfer function:

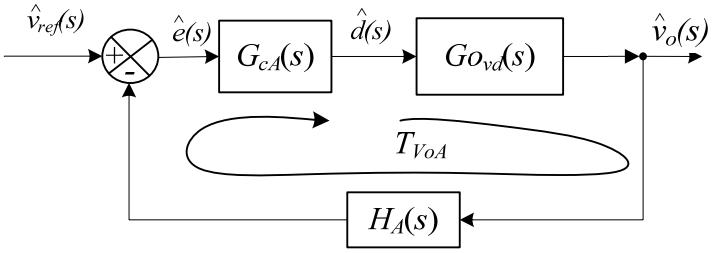


Figure 3-13 Output voltage control loop.

The open loop is given by:

$$T_{VoA}(s) = G_{cA}(s) \cdot Go_{vd}(s) \cdot H_A(s) \tag{3-6}$$

And the corresponding closed loop transfer function is,

$$\frac{\hat{v}_{ref}(s)}{\hat{v}_o(s)} = \frac{G_{cA}(s) \cdot Go_{vd}(s)}{1 + G_{cA}(s) \cdot Go_{vd}(s) \cdot H_A(s)} \tag{3-7}$$

For the closed loop to be stable, it should not contain any right half plane poles. One method to ensure this is:

- The compensator is designed such that the compensated open loop transfer function T_{voA} does not have any right half plane poles;
- The open loop transfer function T_{voA} has a positive phase margin at the cross-over frequency;

- The cross-over frequency is chosen as 1/5 of the switching frequency to ensure fast response; and
- The phase margin at the cross-over frequency is chosen to be at least 45° to limit the overshot and oscillation.

To achieve this, a two-pole two-zero compensator is used where the poles and zeros of the compensator are located as shown in Table 3-2.

Table 3-2 System Design Parameters

Parameters	Value	Parameters	Value
Output power	1600W	Leakage inductance L_{lk}	0.5μH
Input voltage	160V	Output filter inductor L_o	315μH
Output voltage	380V	Output filter capacitor C_o	2μF
Transformer turns ratio	28/8	Switching frequency	200kHz
Effective duty Cycle	68%	Load current I_L	4.21A
First compensation zero	5kHz	First compensation pole	0Hz
Second compensation zero	7kHz	Second compensation pole	100kHz
Compensator gain	20	Feedback gain H_A	0.004

Figure 3-14 shows the bode plot of the uncompensated open loop H_A*Go_{vd} , the compensator H_c and the overall gain $H_A*Go_{vd}* H_c$, using the parameters in Table 3-2. The uncompensated loop had a cross-over frequency of 10kHz and a small phase margin, which resulted in a long transient time and large oscillation, as shown in the step response in Figure 3-15.

The compensator is added to modify the open loop gain such that the cross-over frequency is higher with enough phase margin. The bode plot of the compensated loop is also shown in Figure 3-15, where it has a cross-over frequency of 20.8 kHz and a phase margin of 53.1°. The step response of the compensated loop is also shown in Figure 3-15, where the improvement in the transient time and the elimination of oscillation is obvious. Also the steady state error is eliminated due to the high gain at low frequencies.

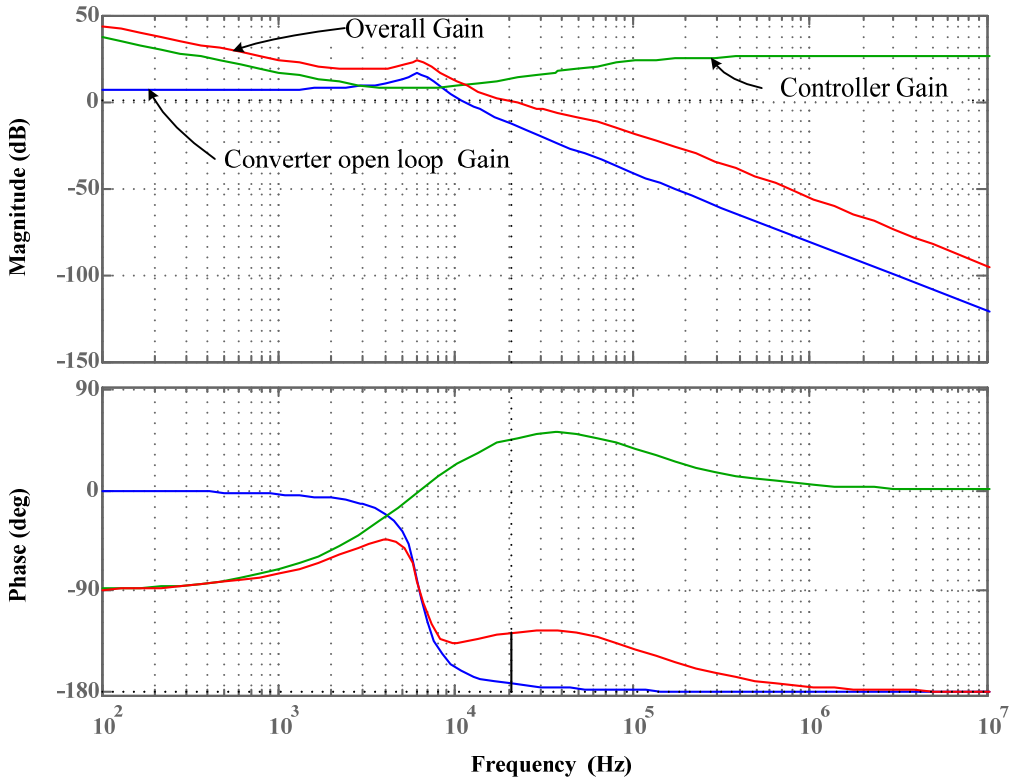


Figure 3-14 Bode plot of the controller and the converter transfer functions.

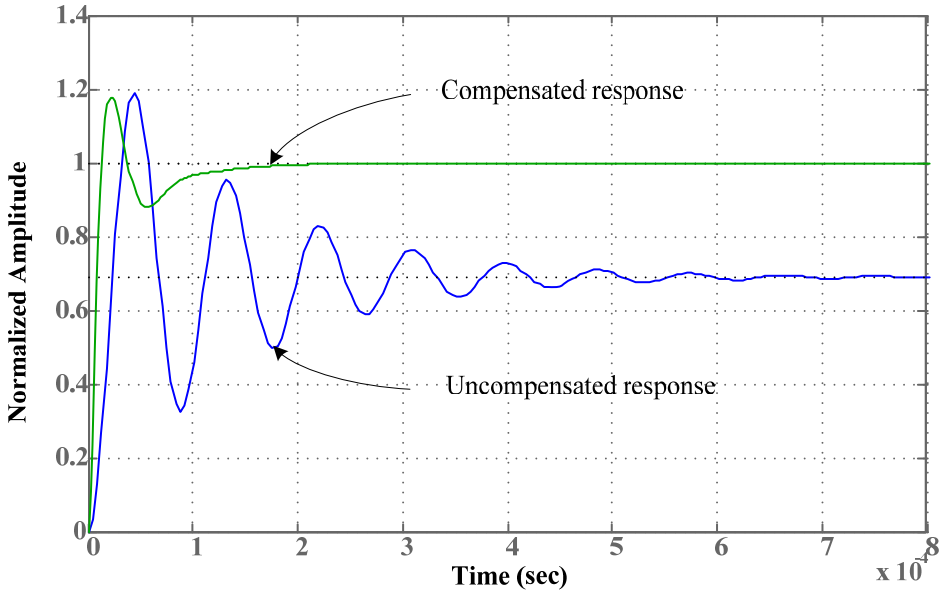


Figure 3-15 Step response of the closed loop output voltage control.

3.4.3 Design of Input Voltage Control Loop

The input voltage is controlled by the outer loop of the cascade control. Input voltage is controlled by changing the set point of the output voltage. To design the control loop compensator, the transfer function of the input voltage to the duty cycle needs to be determined. The output voltage is considered constant since it is controlled by the inner loop. The PV array is modeled by the Thevnin equivalent as discussed in Section 3.4.1. The simplified small signal model is shown in Figure 3-16.

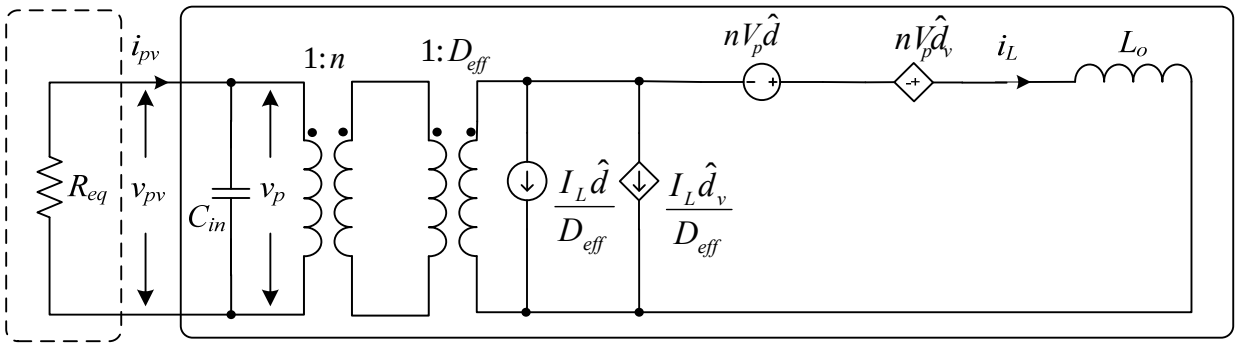


Figure 3-16 Small signal model of DC/DC converter and PV array with constant output voltage.

The transfer function for the input voltage to the duty cycle is found using the small signal model in Figure 3-16 as:

$$G_{vin}=\frac{\hat{v}_p}{\hat{d}}=-\frac{nSL_oI_L+n^2D_{eff}V_p}{S^2L_oC_{in}+SL_o(\frac{1}{-R_{eq}}+\frac{R_dI_L^2}{V_p^2})+n^2D_{eff}^2+\frac{D_{eff}R_dI_L}{V_p^2}} \tag{3-8}$$

The negative gain of the transfer function is due to the fact that the positive variation of the duty cycle will result in negative variation of the input voltage. The type of PV model considered, being a voltage source or a current source, will affect the transfer function of the system. Figure 3-17 shows the bode plot of the transfer function for both the current source PV array type and the voltage source PV array type, using the parameters shown in Table 3-3.

Table 3-3 PV Array Parameters

Parameters	Value	Parameters	Value
Peak power	2340W	Series resistor R_s	2.61Ω
Max. power Voltage V_{mp}	158V	Shunt resistor R_{sh}	134Ω
Max. Power Current	14.92A	Input capacitor C_{in}	1mf
Open circuit voltage	197V		
Short circuit Current	16.1A		

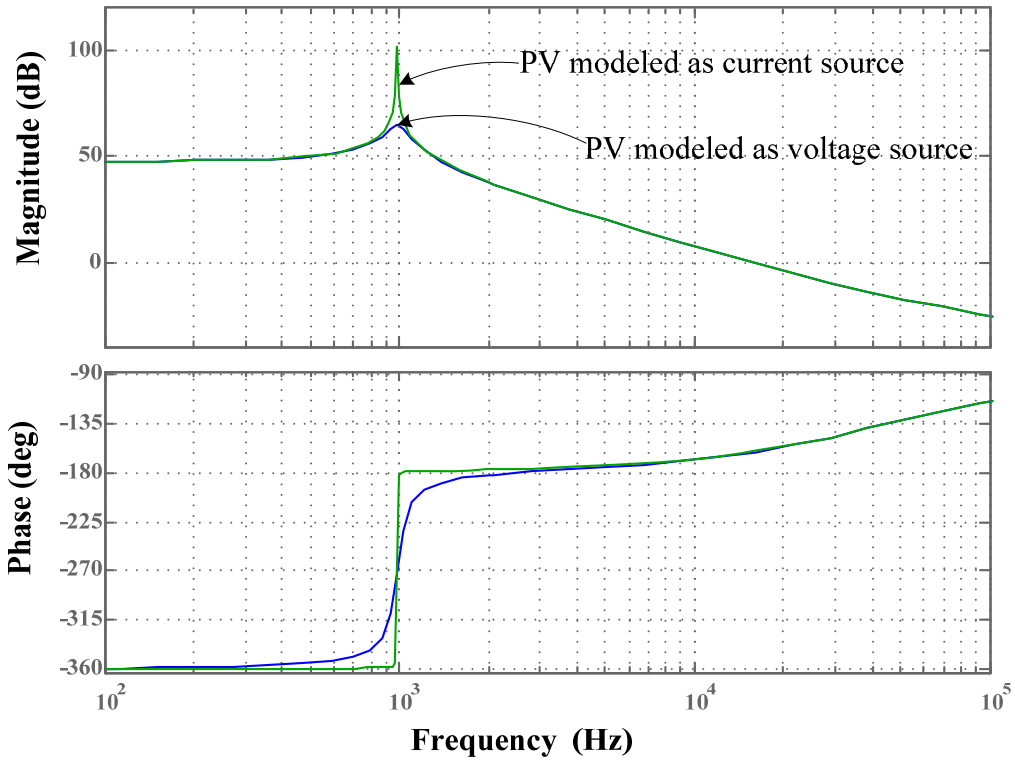


Figure 3-17 Bode plot of the transfer function G_{vin}.

It is obvious that control is harder when the PV array is modeled as a current source. Moreover, due to the cascade control method, the input voltage of the converter is only controlled when the load demand is larger than the PV array available power, which results in an operating point to the left of the MPP on the current source section. Thus only the current source

model will be considered hereafter. The cascade input voltage control loop is shown in Figure 3-18.

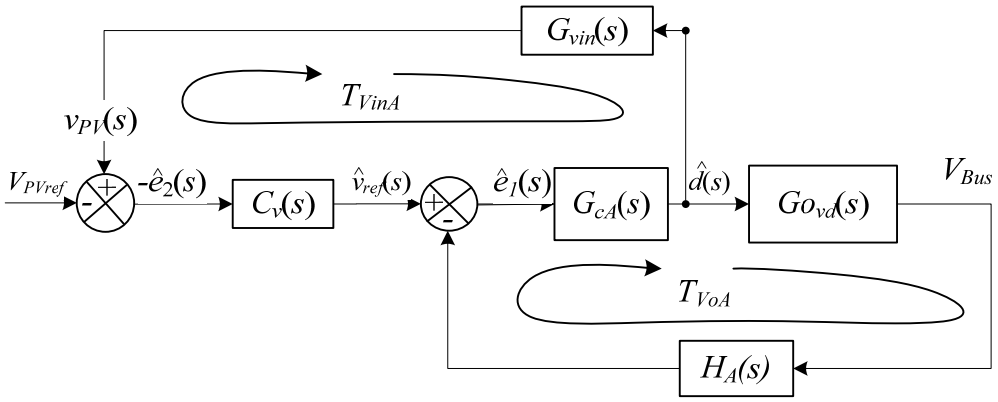


Figure 3-18 Cascade control loop of input voltage control.

The outer input voltage control loop is expressed as follows:

$$T_{VinA}(s) = \frac{C_v(s) \cdot G_{cA}(s) \cdot G_{vin}(s)}{1 + T_{VoA}(s)} \tag{3-9}$$

where C_v is the compensator of the outer loop and G_{vin} is the input voltage to duty cycle transfer function expressed in Eq.(3-8).

The step response of the uncompensated close loop of $T_{VinA}(s)$ is shown in Figure 3-19. The response is stable; however a steady state error is present. A PI compensator is designed to eliminate the steady state error. The response of the compensated closed loop is also shown in Figure 3-19. The step response of the outer loop is slow compared to the inner loop, which makes cascade control a good choice. In addition, the change in the environmental condition is a slow process.

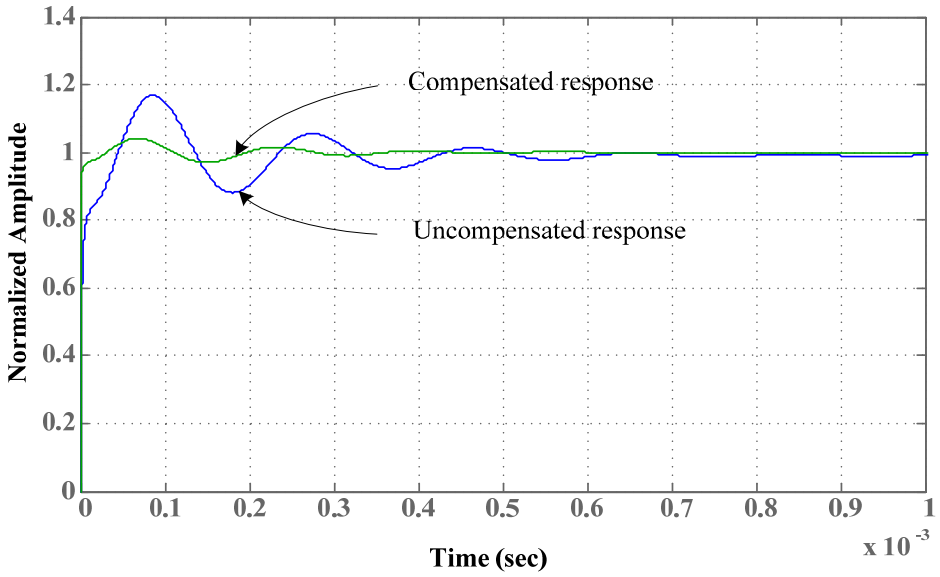


Figure 3-19 Step response of closed loop control of input voltage.

3.4.4 Design of Input Current Control Loop

The input current is controlled by the outer loop to enforce current sharing among the slave converters; this is also achieved by changing the step point of the inner loop. From Figure 3-16 the input current is related to the input voltage as follows:

$$G_{id} = \frac{\hat{i}_s}{\hat{d}} = -\frac{\hat{v}_s}{R_{eq}\hat{d}} = -\frac{G_{vd}}{R_{eq}} \tag{3-10}$$

Thus the transfer function of the input current to the duty cycle is given by:

$$G_{id} = \frac{\hat{i}_s}{\hat{d}} = \frac{\frac{1}{R_{eq}}\left(nSLI_L + n^2 D_{eff} V_s\right)}{S^2 LC + SL\left(\frac{1}{-R_{eq}} + \frac{R_d I_L^2}{V_s^2}\right) + n^2 D_{eff}^2 + \frac{D_{eff} R_d I_L}{V_s^2}} \tag{3-11}$$

The cascade input current control loop is shown in Figure 3-20.

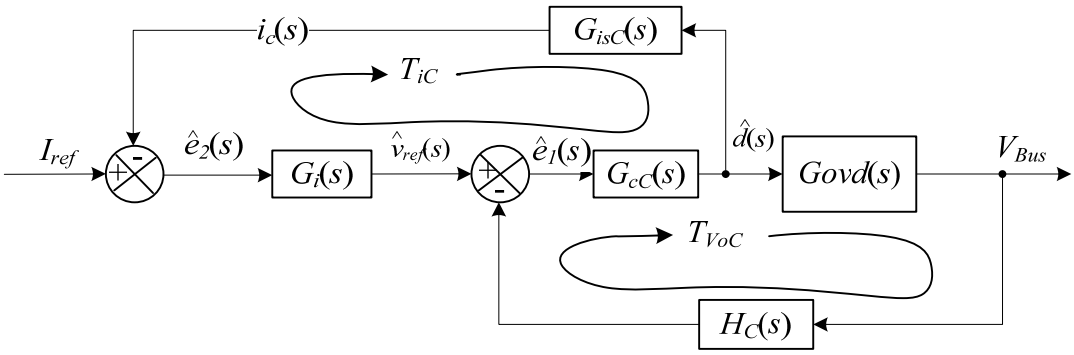


Figure 3-20 Cascade control loop of input current.

The input control loop is expressed in Eq. (3-12):

$$T_{iC} = \frac{G_i \cdot G_{cC} \cdot G_{isC}}{1 + T_{VoC}} \tag{3-12}$$

where G_i is the loop compensator and G_{isC} is the input current to duty cycle transfer function.

The step response of the input current loop is similar to the input voltage loop, as shown in Figure 3-21. The uncompensated step response suffers large oscillation and a steady state error, both of which can be eliminated by a PI compensator. The step response of the compensated loop is also shown in Figure 3-21.

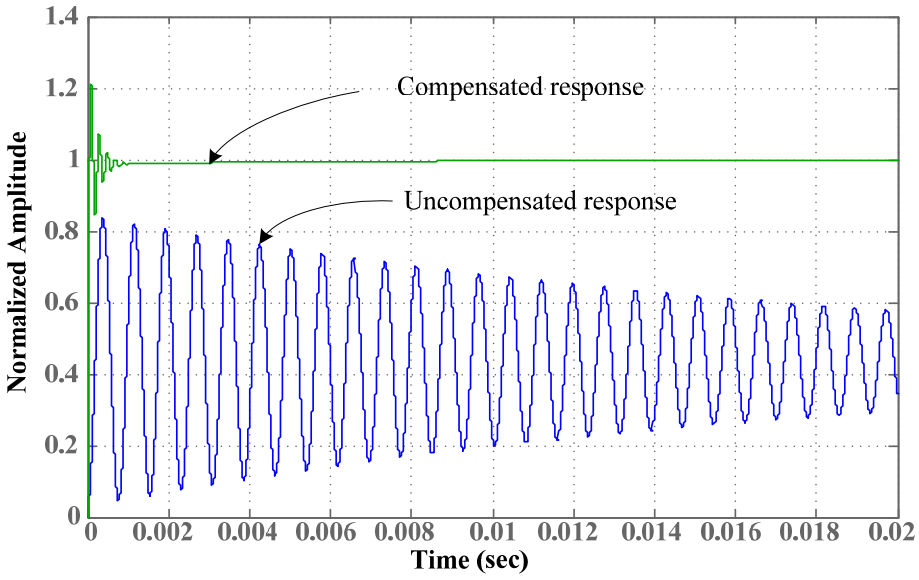


Figure 3-21 Step response of the close loop control of input current.

The control loops are implemented in the DSP platform and the discrete time domain version of the compensators are obtained by linear transformation of the Analog version using Matlab. The simulation of the proposed control scheme is presented in the following section.

3.5 Simulation Results

In order to verify the control method suggested in this chapter, a DC/DC system is simulated using a Matlab/Simulink platform, as shown in Figure 3-22. The PV array consists of 20 parallel strings each having 5 panels in series for a total of 6kW, and an open circuit voltage of 120V. An average signal model of the DC/DC converter is used in the simulation to reduce the computational load [109].

The MPPT module implements the P&O algorithm to maximize the power yield of the system. The controller discussed in Section 3.3 is implemented in Simulink to regulate the PV array Voltage and to achieve current sharing. Converter A is implemented as a master converter to control the voltage of the PV array, whereas the slave converters B&C share the input current with it. In order to simulate the impedance difference between the converters, the resistors R1 and R2 are added in a series with converter B&C. The aim of the simulation is to test the dynamic behavior of the controller as environmental conditions change. Two sets of simulations are performed, one for the change in temperature, and the other for the change in irradiance.

3.5.1 Investigation of Change in Temperature

The temperature of the PV array is changed from 0 to 52°C in a sine wave while the irradiance is constant at 1 sun as shown in Figure 3-23. Figure 3-24 shows the change in I-V and the power curve of the PV array as the temperature changes. At low temperatures the open circuit voltage of the PV array increases and the MPP voltage increases, while the current stays almost constant, which results in an increase in power. When the temperature increases the opposite happens and the power decreases. The change in the PV array voltage and current, together with the MPP voltage, and current of the PV array, are shown in Figure 3-25.

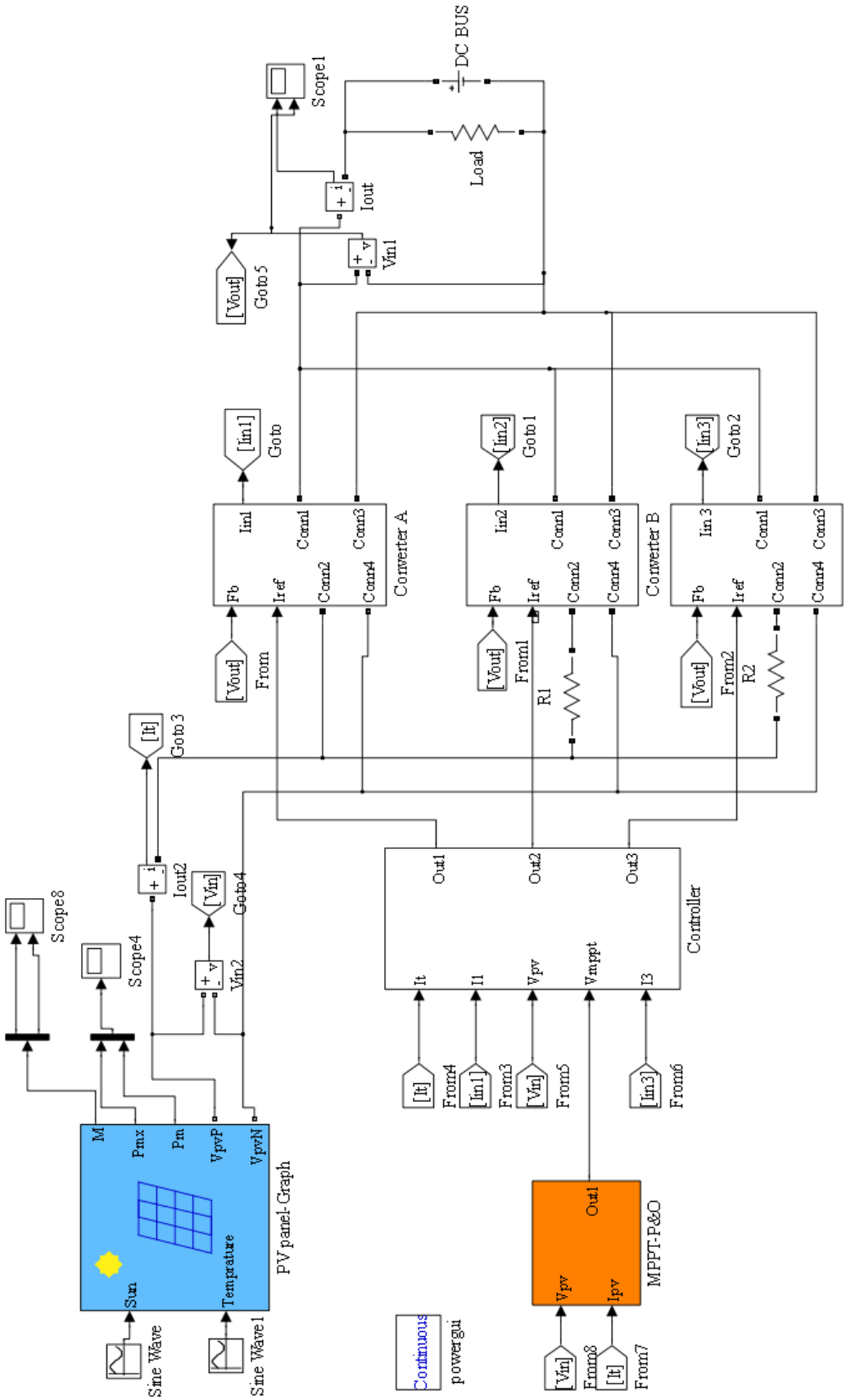


Figure 3-22 Simulink model of the interleaved system

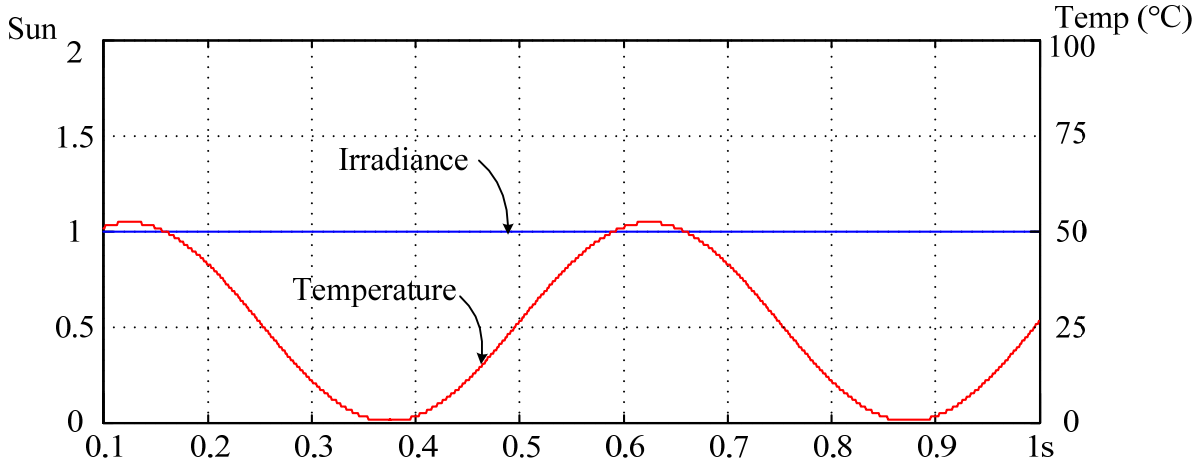


Figure 3-23 Irradiance and temperature waveforms with temperature changing.

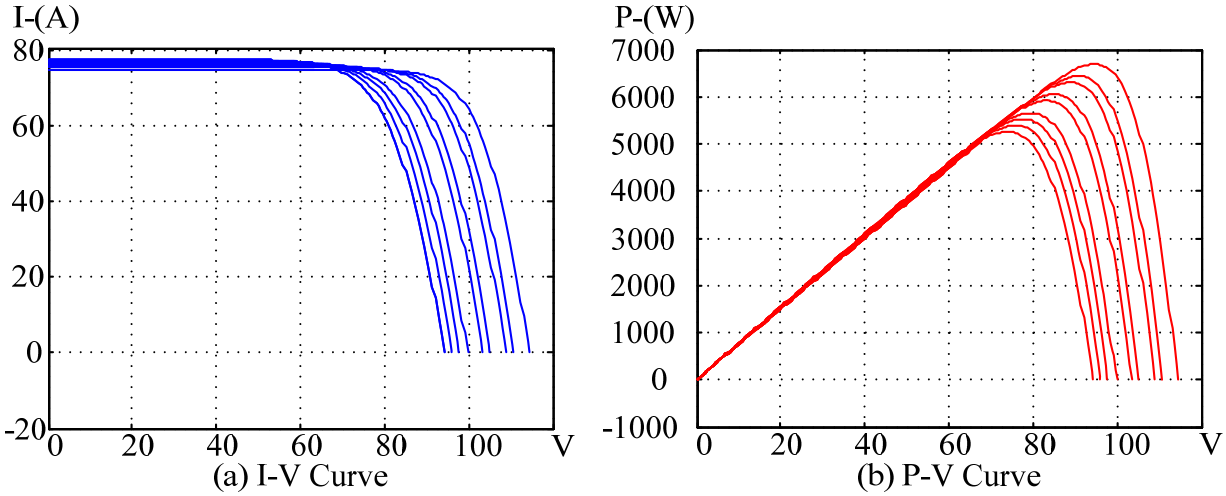


Figure 3-24 PV array characteristics with temperature changing.

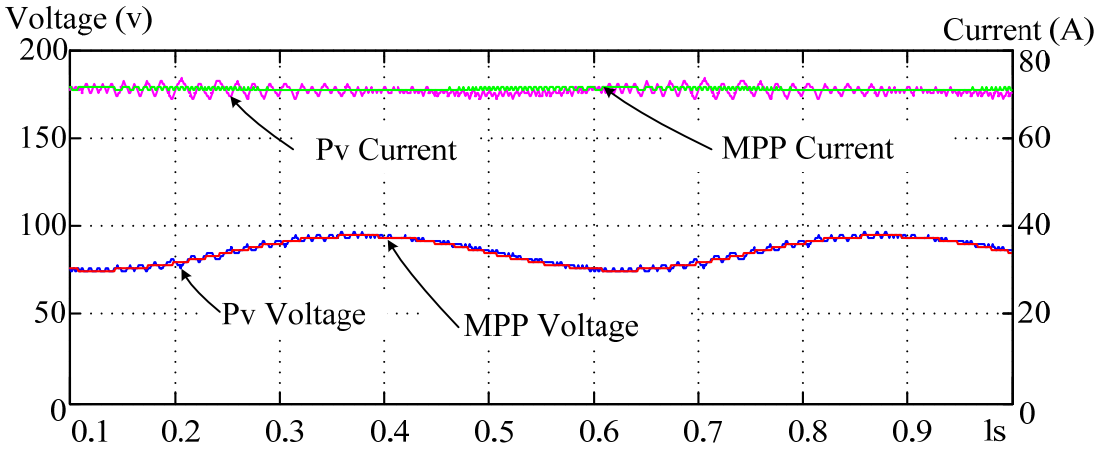


Figure 3-25 PV voltage and current waveforms with temperature changing.

The power wave form is shown in Figure 3-26, together with the maximum available power at the PV array. The P&O MPPT algorithm is used to track the MPP. It is clear that the system is able to track the PV MPP but with some errors This is an inherent problem of the P&O method as explained in Section 1.4.3. Figure 3-27 shows the currents of the three converters. The current sharing mechanism is able to force current sharing despite the difference in the impedance of each converter.

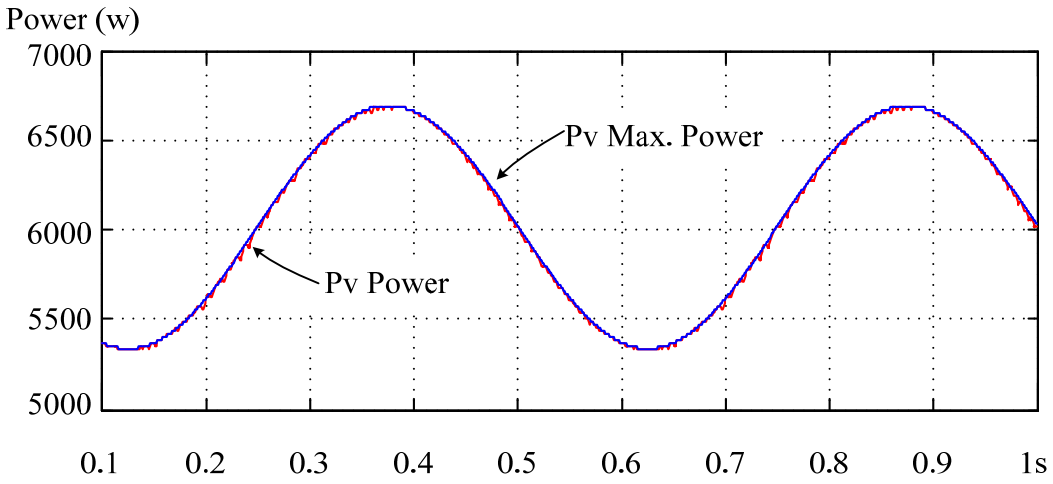


Figure 3-26 PV power waveform with temperature changing.

3.5.2 Investigation of Change in Irradiance

The change in irradiance affects the current generated by the PV array, while at the same time, the voltage stays almost constant. The irradiance waveform shown in Figure 3-28, where the irradiance changes from 0.25 suns to 1 sun in sine wave, is applied to the simulation model while the temperature is kept constant at 26°C. The change in the I-V curve and power curve is shown in Figure 3-29. The PV array voltage and current waveforms, together with the MPP voltage and current waveforms, are shown in Figure 3-30. The deviation from the MPP during the change in irradiance, which is caused by the P&O algorithm, is apparent in Figure 3-30 and Figure 3-31.

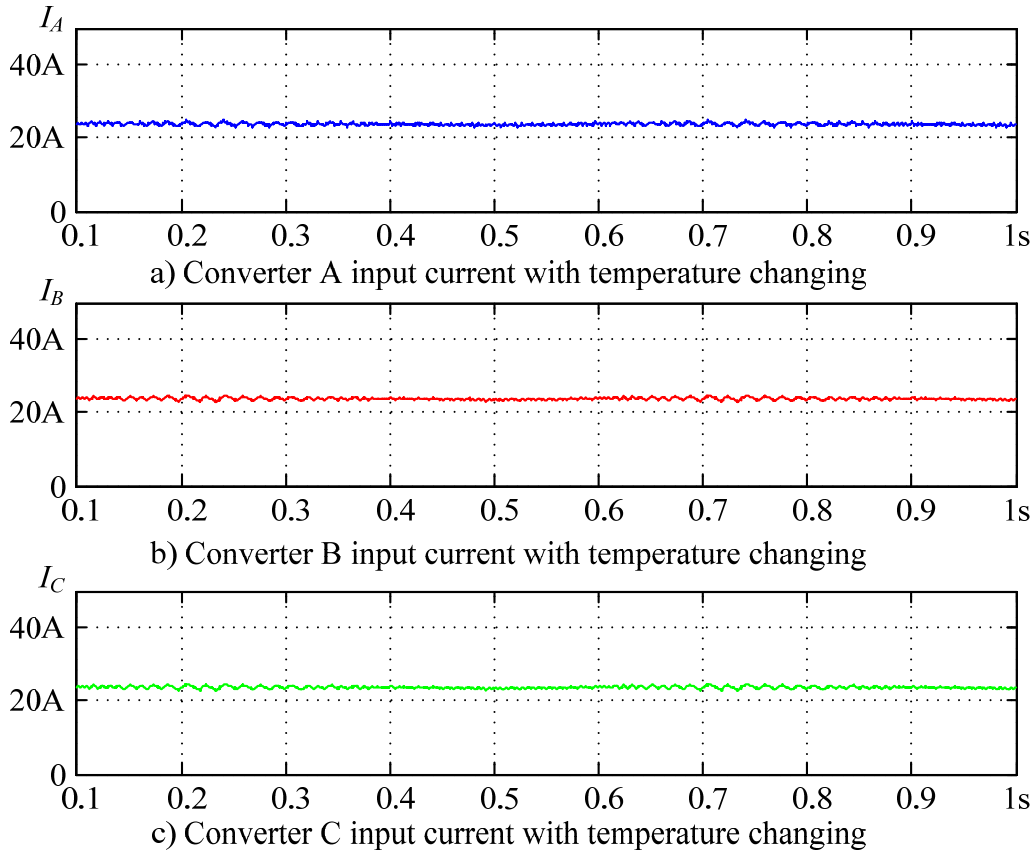


Figure 3-27 Converters input currents with temperature changing.

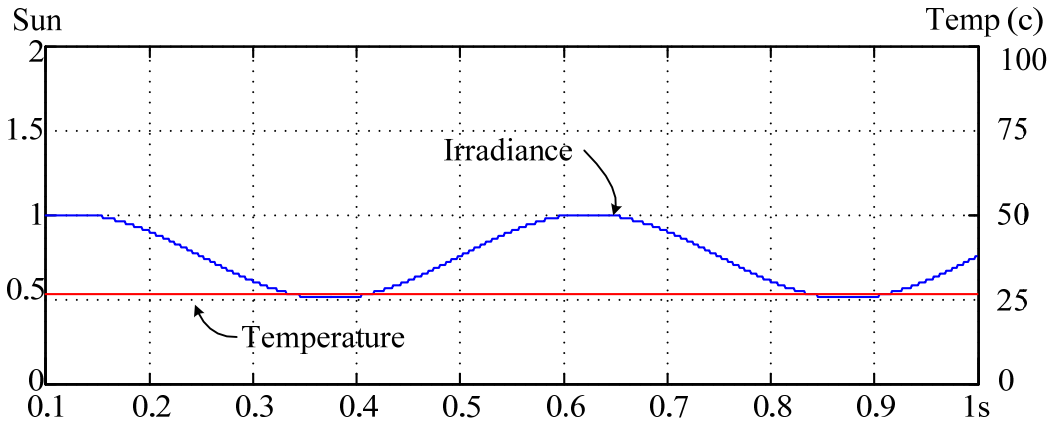


Figure 3-28 Irradiance and temperature waveforms with irradiance changing.

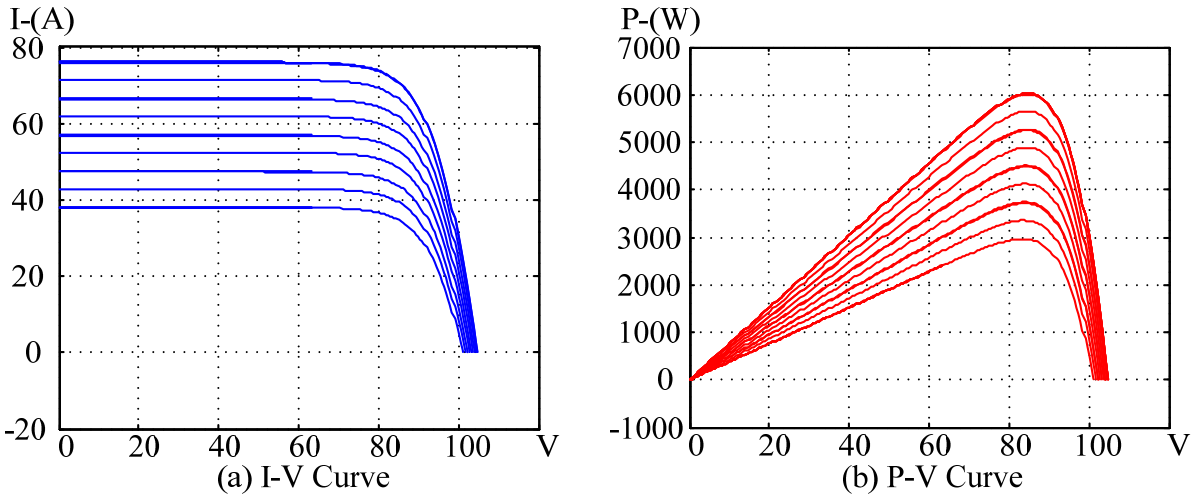


Figure 3-29 PV array characteristics with irradiance changing.

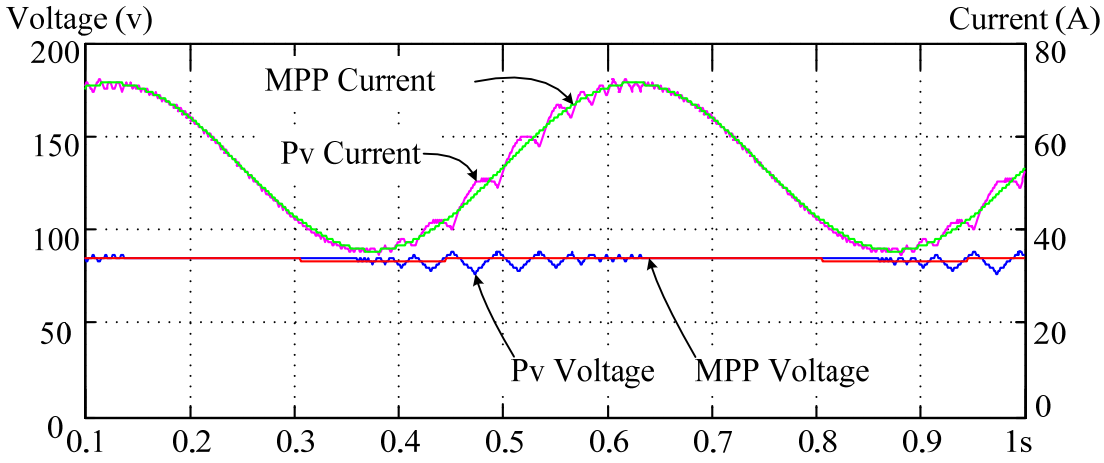


Figure 3-30 PV voltage and current waveforms with irradiance changing.

The change in irradiance causes the current of the PV array to change. However the controller is able to keep the current sharing during this change, as shown in Figure 3-32. The controller is also able to force the system to track the MPP voltage set by the MPPT controller.

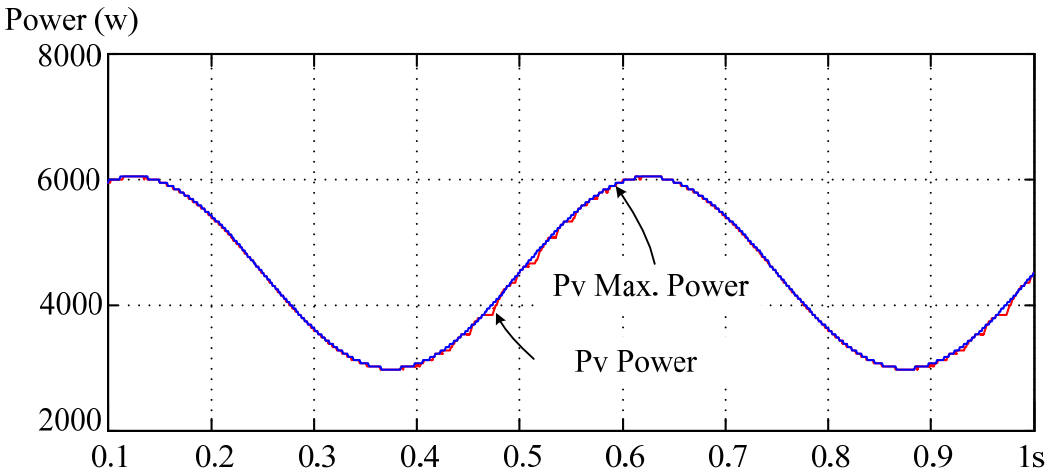


Figure 3-31 PV power waveform with irradiance changing.

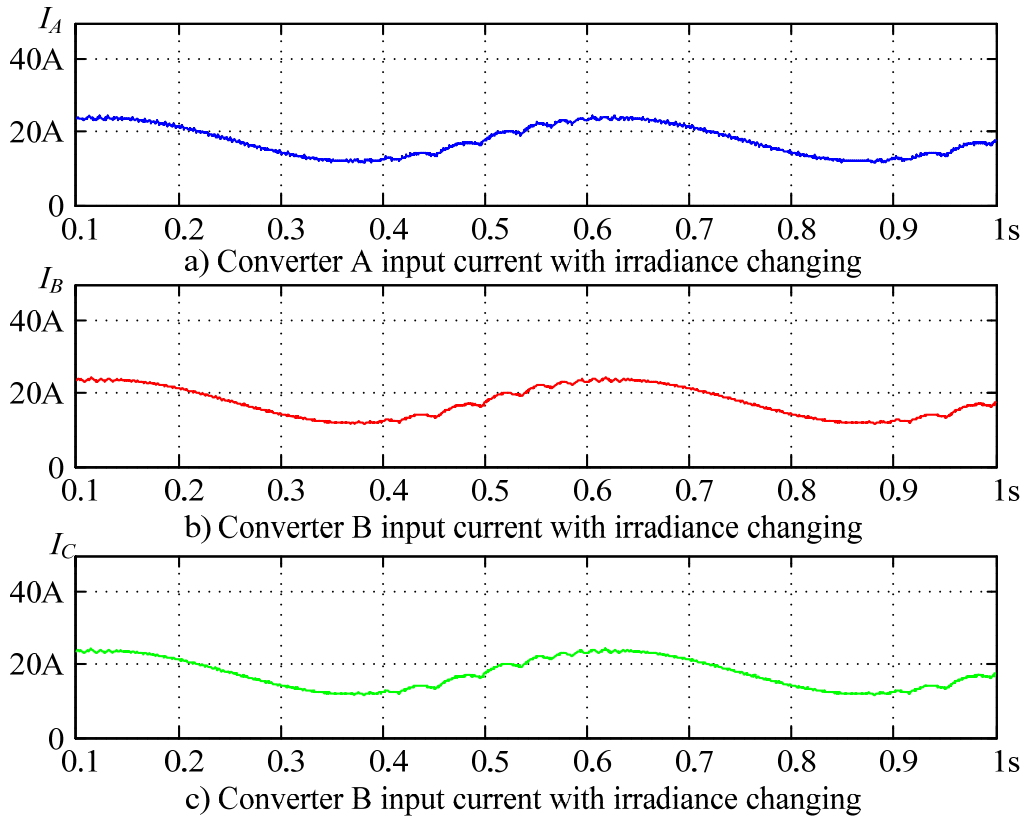


Figure 3-32 Converters input currents with irradiance changing.

3.6 Hardware Realization

A prototype was built as shown in Figures 3-33 to 3-36. This prototype consisted of three converters, each with an output power of 1.8kW, with a total output power of 5.4kW. The three

converters were controlled from a single DSP evaluation board utilizing the microcontroller TMS320F28335. The DSP generated four gate signals for each converter, and the gate signal for the active snubber of each converter. All 15 of the gate signals were synchronized and shifted according to the interleaving scheme discussed in Section 3.2. The switching frequency of each converter is 100 kHz. Thus, the ripple at the input and output of each converter is 200 kHz, and the interleaving of the total ripple at the input and output of the system is 600 kHz. This prototype is part of the NSERC Solar Building Research Network Project, and the preliminary tests of the complete system were carried out at the Laboratory for Electric Drive Research and Application (LEDAR) at Ryerson University, while the final tests of the system were carried out at Concordia University in the John Molson School of Business (JMSB) building. There, the device was connected to a PV solar array and used in their research in a grid-tied PV system.

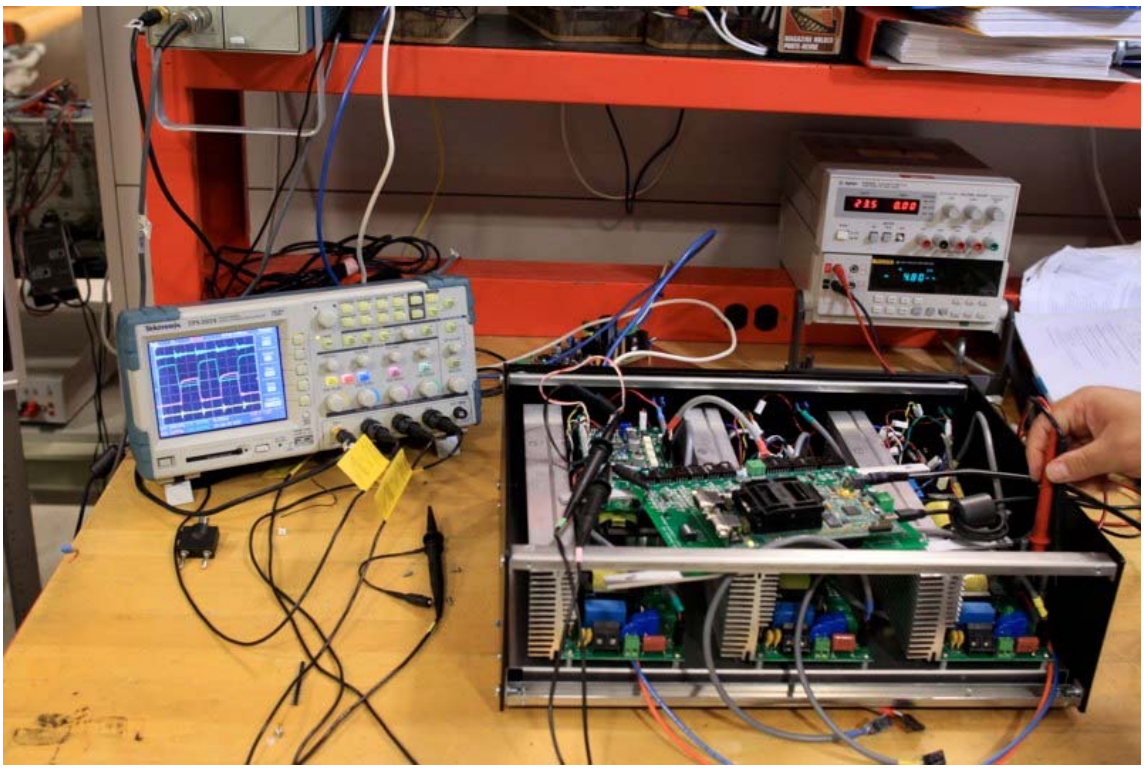


Figure 3-33 PV system during test at LEDAR Lab Ryerson University.

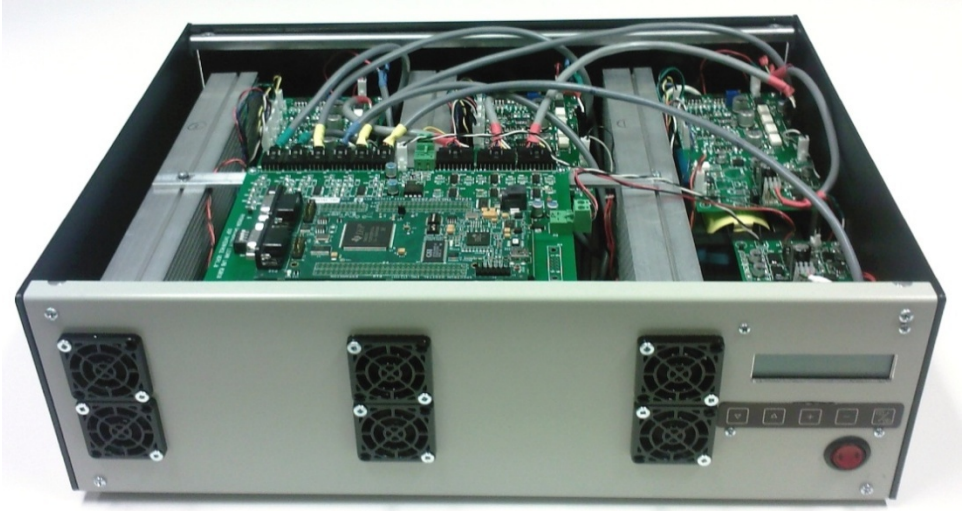


Figure 3-34 Assembled prototype of 3x1.8kW DC\DC converter.

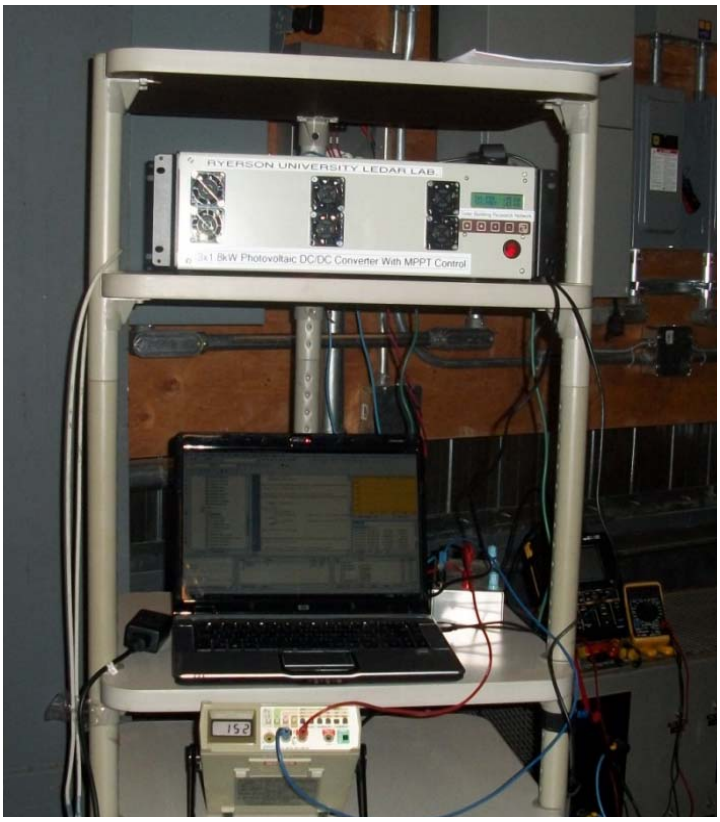


Figure 3-35 PV system during test at Concordia University JMSB.

Figure 3-36 Demonstration project at Concordia JMSB.

3.7 Conclusion

This chapter presented the design of a multiphase DC/DC power conversion system consisting of three parallel individual converters working in an interleaved method. The ripple cancellation due to interleaving was demonstrated by simulation using a PSPICE platform. A new cascade control method was proposed, where the PV array voltage for maximum power point tracking was controlled by a master converter, and the active even current sharing was implemented by the remaining slave converters. A linear model of the PV system was derived. The control loops were designed analytically and proven by simulation in Matlab. The performance of the new control method under changing temperature and irradiance was investigated by simulation in the Matlab/Simulink platform. A 5.4kW DC/DC prototype system controlled by a single DSP controller was built for a Solar Building Demonstration Site at Concordia University under the NSERC Solar Building Research Network Program.

Chapter 4
Evaluation of Maximum Power Point Tracking Algorithms

4.1 Introduction

Maximum Power Point Tracking algorithms, introduced in Section 1.4, are important for the success of PV energy conversion systems since they ensure that all the energy available at the PV array is retrieved and processed by the converter. The tracking of the maximum power point (MPP) is challenging because the characteristics of the PV array are nonlinear and change as the irradiance and temperature conditions change. An optimal algorithm should be able to track the MPP quickly as environmental conditions change. The hill climbing algorithm is widely used in practical PV systems because: 1) it is one of the simplest methods; 2) it does not require prior study or modeling of the PV array characteristics; and 3) it accounts for characteristics' drift resulting from aging, shadowing, or other operating irregularities [27, 28].

The basic hill-climbing algorithm is the Perturb and Observe (P&O) algorithm. Although the P&O algorithm works well when the irradiance changes slowly, it exhibits erratic behavior for rapidly changing irradiance levels that causes incorrect tracking. This led to the development of the Modified Perturb and Observe (MP&O) algorithm [29], which improves the P&O algorithm but at the expense of a slow response speed to the irradiance changes. An enhanced new MPPT algorithm, named the Estimate-Perturb-Perturb (EPP) algorithm, was proposed in [24]. However, its performance has neither been investigated thoroughly nor verified by experiments. A detailed analysis of the three algorithms is conducted. Their performance is investigated by simulation, and experimental verification is presented in this chapter.

4.2 Estimate-Perturb-Perturb MPPT Algorithm

During rapidly changing irradiance and environmental conditions, if the change in power due to atmospheric conditions is larger and in the opposite direction from the changes due to perturbation caused by the algorithm, the operating point is shifted in the opposite direction. This

phenomenon is explained in Section 1.4.3. To isolate the fluctuations caused by the perturbation process, as opposed to those caused by irradiance or weather changes, an irradiance-changing estimate process is implemented before each perturbation in the MP&O algorithm. This process is explained in Section 1.4.4. The estimate-perturb-perturb (EPP) algorithm uses one estimate mode between every two perturb modes, resulting in a fast response to environmental changes.

Figure 4-1 shows the time sequences for the P&O algorithm, the MP&O algorithm, and the EPP algorithm. While the P&O algorithm executes a perturbation for each time instant, the MP&O algorithm skips one time instant to estimate the change in environmental conditions before the next perturbation. Because the estimate process stops tracking the maximum power point by keeping the PV voltage constant, the tracking speed of the MP&O algorithm is only half that of the conventional P&O algorithm. The EPP algorithm improves the speed of the MP&O algorithm while keeping its main features. The execution of the perturbation is only skipped once for every three time instants.

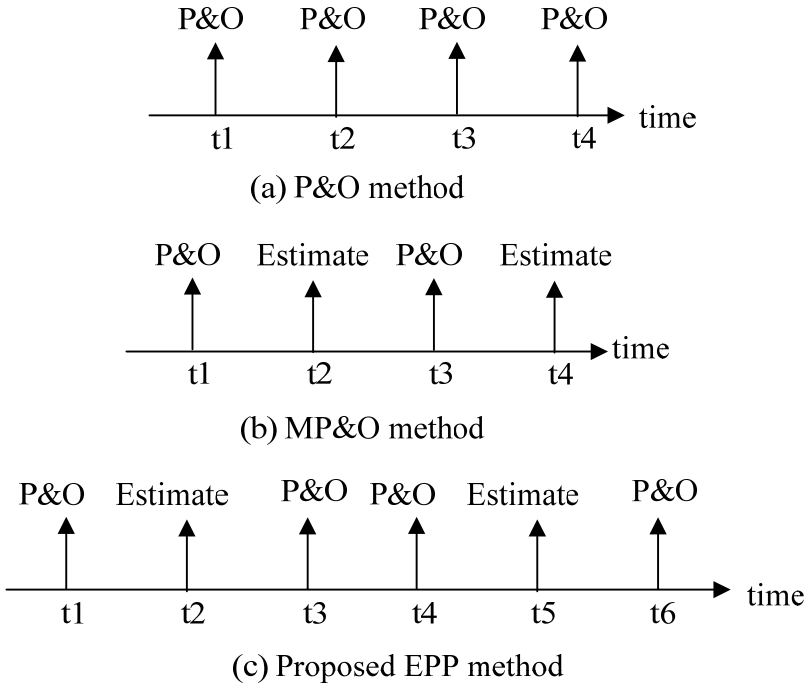


Figure 4-1 Time sequence of three P&O algorithms.

Figure 4-2 shows the flow chart for the EPP algorithm. The present power *P(k)* is calculated with the present values of PV voltage *V(k)* and current *I(k).* One of the following three modes is executed according to the "count" flag:

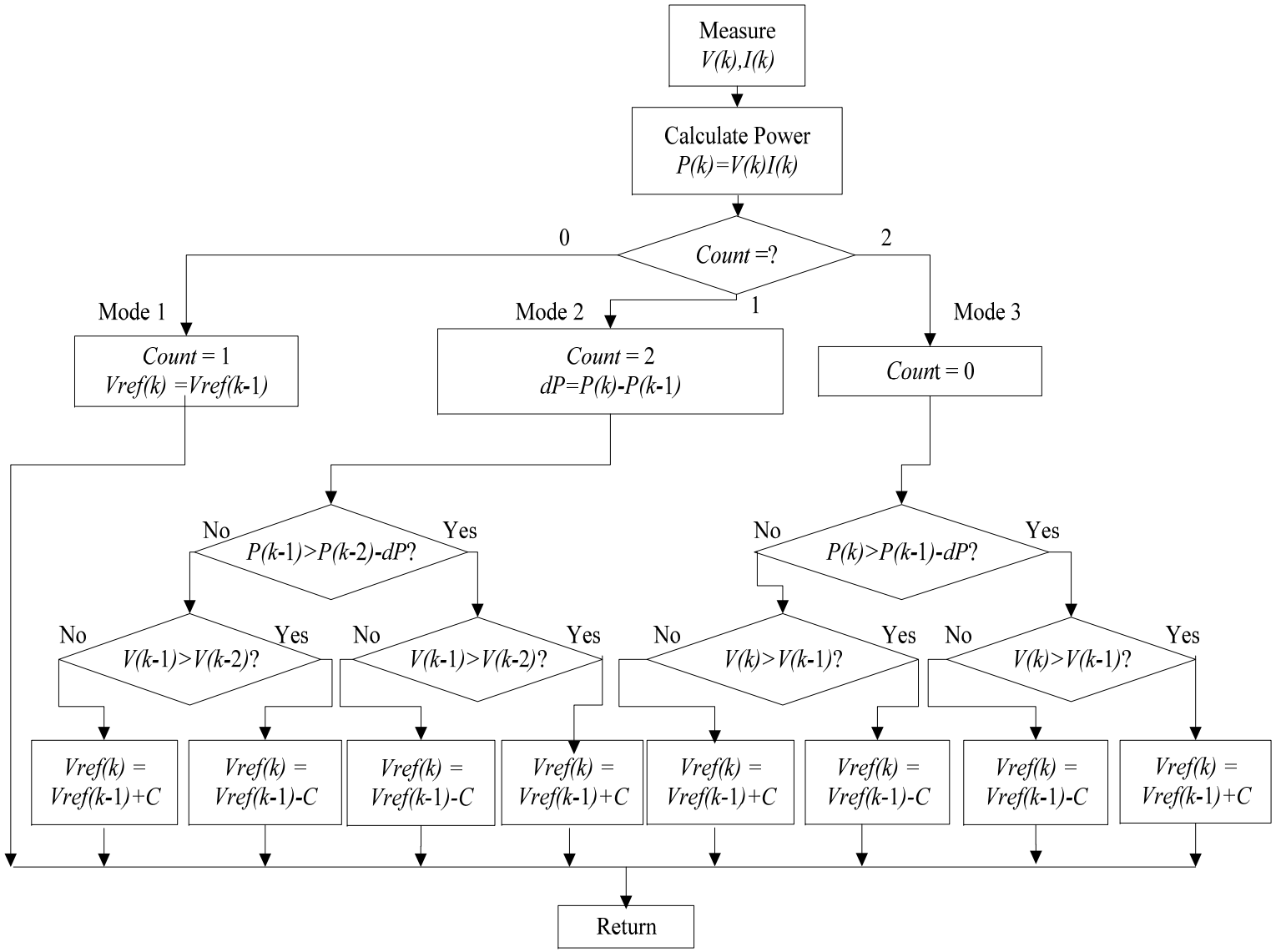


Figure 4-2 Flow chart of EPP algorithm

Mode 1 (estimate mode): The counter is advanced to indicate Mode 2 in the next run. Since there is no change to the reference in this mode, this guaranties that in the next run, when the power values $P(k\text{-}1)$ and $P(k)$ are compared, the change dP is merely due to environmental changes. If there is no change in environmental conditions, then $P(k\text{-}1) = P(k)$ and $dP=0$.

Mode 2 (1^{st} perturb mode): The counter is advanced to indicate Mode 3 in the next run. The power $P(k\text{-}1)$ is subtracted from $P(k)$ to determine the change dP. Then $P(k\text{-}1)$ is compared with the previous power $P(k\text{-}2)\text{-}dP$, which is the absolute change due to the perturbation. If the power has increased, the next voltage change is kept in the same direction as the previous change. Otherwise the voltage is changed in the opposite direction of the previous one.

Mode 3 (2^{nd} perturb mode): The counter is reset to indicate Mode 1 in the next run. $P(k\text{-}1)\text{-}dP$, which is the previous power minus the change due to environmental conditions estimated previously, is compared to the recent power $P(k)$. If the absolute power change has increased, the next voltage change is in the same direction as the previous change; otherwise, the voltage is changed in the opposite direction of the previous one. In this mode, the change in power due to environmental conditions is assumed constant during the period between Modes 2 and 3, which is justifiable since the algorithm execution is much faster than the changes in environmental conditions.

When compared with the P&O algorithm, the EPP algorithm has an additional estimate mode, which considers the effect of the change in irradiance upon the tracking algorithm. This significantly improves the MPPT performance. However, when compared with the MP&O algorithm, the EPP algorithm uses one estimate mode for every two perturb modes, which significantly increases the tracking speed of the MPPT control, without reducing tracking accuracy.

4.3 Simulation of MPPT Algorithms under Different Conditions

The three MPPT algorithms are simulated and analysed in Matlab/Simulink for different atmospheric conditions in order to investigate their performance. A simplified model of the PV array is used, where the shunt resistance is ignored and the electrical model reduces to that shown in Figure 4-3:

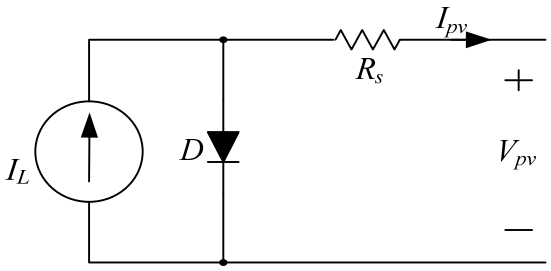


Figure 4-3 Simplified PV array electrical model.

The current-voltage relation Eq. 1-1 given in Section 1.2.2 then becomes:

$$I_{pv} = I_L - I_o \left[e^{\frac{q\left(V_{pv}+I_{pv}R_s\right)}{nKT}} - 1 \right] \tag{4-1}$$

The parameters defined in Table 1-1 and Eq. (4-1) are used to develop the Simulink model of the PV array [110, 111]. The PV array used in the simulation is 20 sets of Solarex MSX60 60W panels connected in a 5×4 matrix. The open-circuit voltage of the PV array is 105V, and the short-circuit current is 14.8A. The maximum power point of the PV array is at 85.5V, 14A, and 1198 W under 1000W/m^2 insolation at 25ºC. Figure 4-4 shows the simulation model of the PV system, where the DC/DC converter is a boost converter with resistive load. The simulation is conducted under different environmental conditions. The performance of the three algorithms is presented in the following sub-sections.

4.3.1 Rapid Change in Irradiance Conditions

The fast change in irradiance conditions usually results in a decrease of the power retrieved from the PV array because MPPT algorithms fail to track the MPP during these changes. In this simulation, the irradiance is varied from 330W/m^2 to 1000W/m^2 with a period of 2 sec in a sinusoidal waveform. Figure 4-5 shows the PV output power, voltage and current using the P&O algorithm. Figure 4-5 (a) shows the maximum available PV power P_{pvmax}, the actual PV output power P_{pv} and tracking error $\Delta P = P_{pvmax} - P_{pv}$. The initial tracking error is reduced to zero in 0.15s by the P&O algorithm. When the irradiance decreases, the P&O algorithm tracks the maximum power point well and the tracking error is nearly zero. However, when the irradiance increases, the P&O algorithm fails to track the maximum power point and the maximum tracking error is nearly 100W. This represents around 8% of the full power.

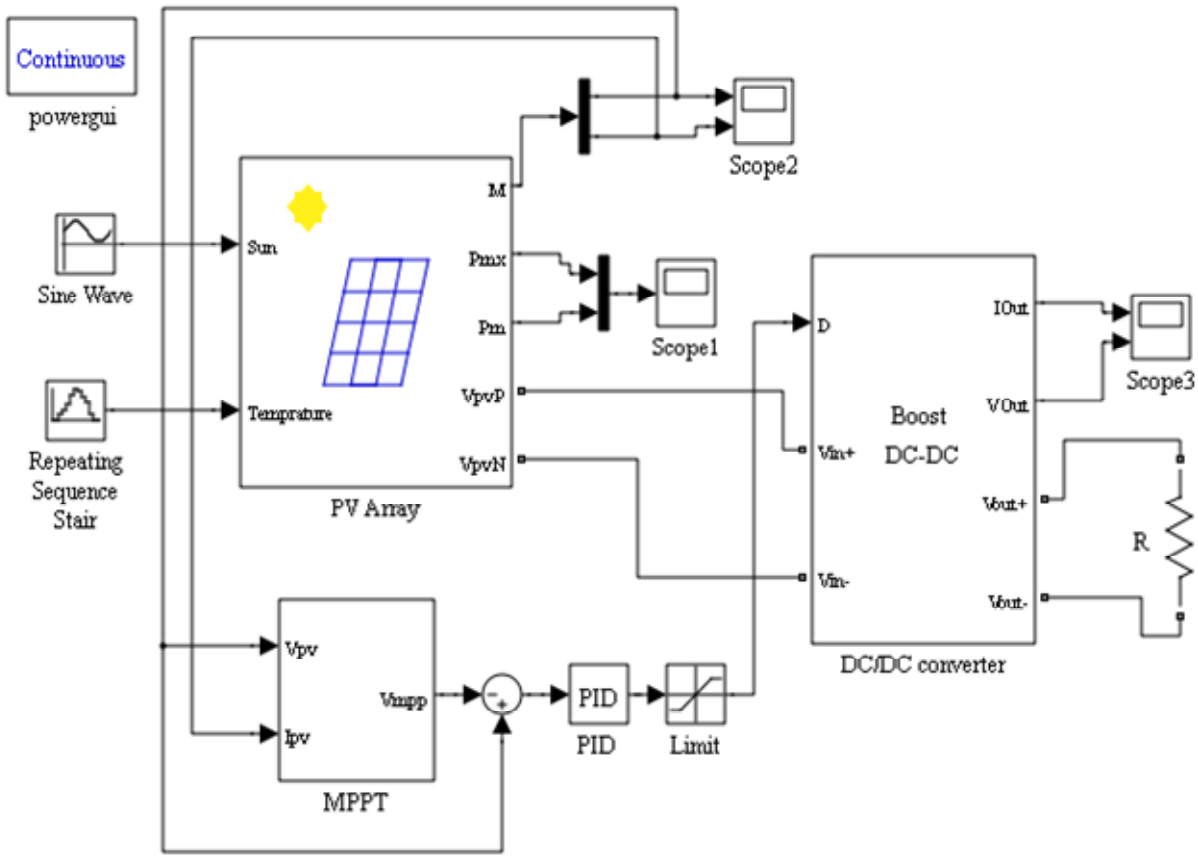


Figure 4-4 Simulink model of the PV system.

Figure 4-5(b) shows the unpredictable behaviour of PV voltage due to the algorithm changing the PV voltage setting in the opposite direction during the change of irradiance.

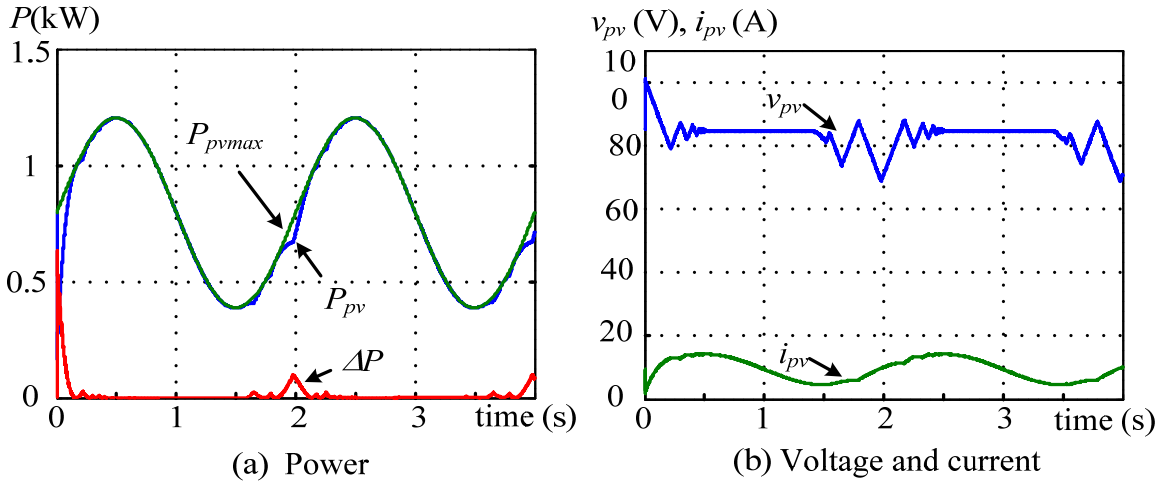


Figure 4-5 P&O algorithm under sinusoidal changing irradiance.

Figure 4-6 shows the PV output power, voltage and current for the MP&O algorithm. This algorithm tracks the maximum power point very well, with a steady tracking error of less than 1W. It is obvious that the initial time to track the MPP is double that of the P&O algorithm.

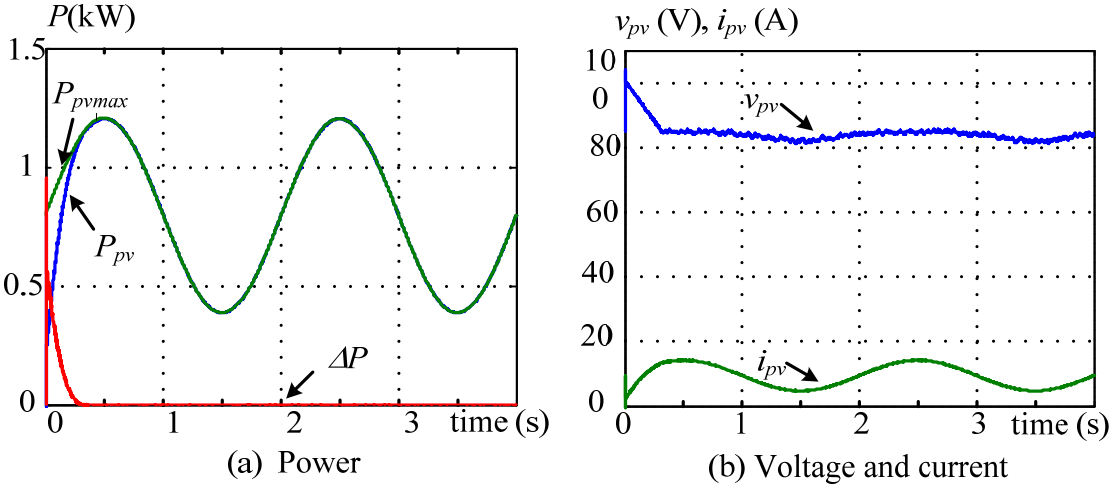


Figure 4-6 MP&O algorithm under sinusoidal changing irradiance.

Figure 4-7 shows the PV output power, voltage and current for the EPP algorithm. The EPP algorithm has a maximum power tracking performance similar to that of MP&O algorithm, both with a steady state tracking error of less than 1W, while the initial tracking time of EPP is less than that of MP&O.

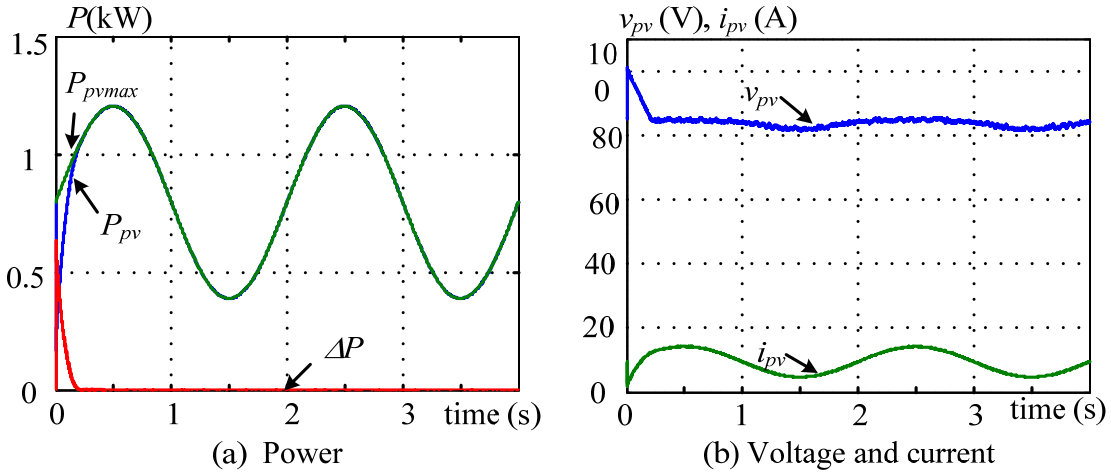


Figure 4-7 EPP algorithm under sinusoidal changing irradiance.

4.3.2 Rapid Changes in Temperature Conditions

The simulation is also carried for temperature variations between 10°C and 50°C with a period of 1 sec. Figure 4-8 shows the simulation results for the P&O algorithm. As the temperature increases, the voltage decreases; hence the power decreases. During this period, the algorithm fails to track the changing MPP with a large error of approximately 200W. Note that the error is larger since the change in the environmental conditions are faster. During the decrease of temperature, the algorithm tracks the MPP with a small error. Figure 4-8(b) shows the change in voltage and current. Since the temperature is changing, the PV voltage changes in sinusoidal-like waveform, while the current, which is irradiance dependent, is almost constant. Also the PV voltage changes in an irregular way due to the fact that the P&O algorithm perturbs the setting into the opposite direction.

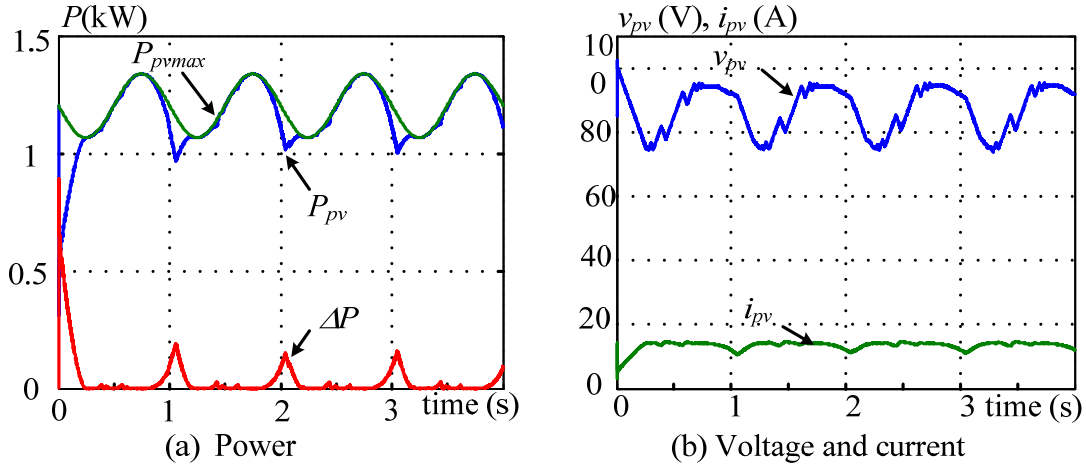


Figure 4-8 P&O algorithm under sinusoidal changing temperature.

The simulation of the MP&O algorithm is shown in Figure 4-9. During the increase of temperature, the algorithm tracks the MPP with a small error of about 20W. The EPP algorithm tracks the MPP during temperature changes of the same conditions with approximately zero error, as shown in Figure 4-10.

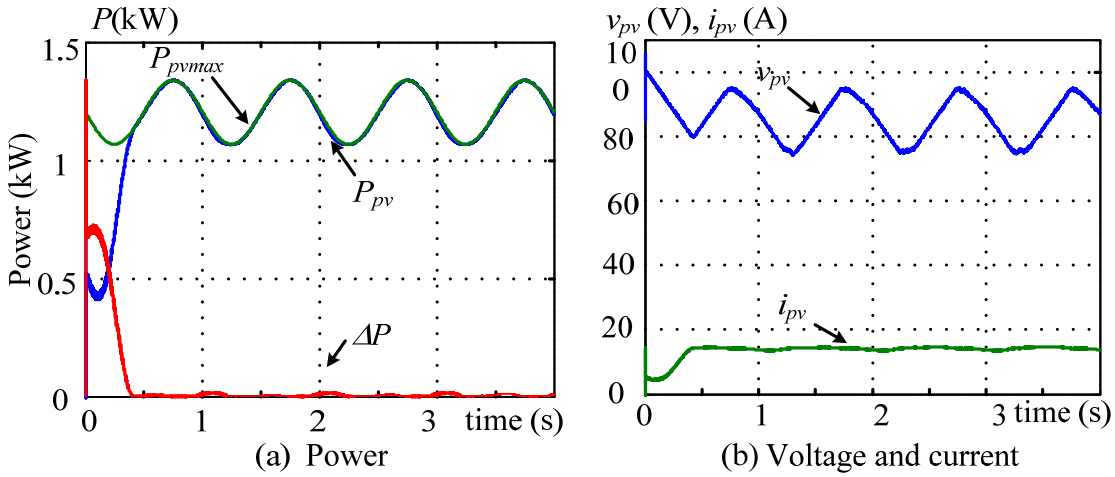


Figure 4-9 MP&O algorithm under sinusoidal changing temperature.

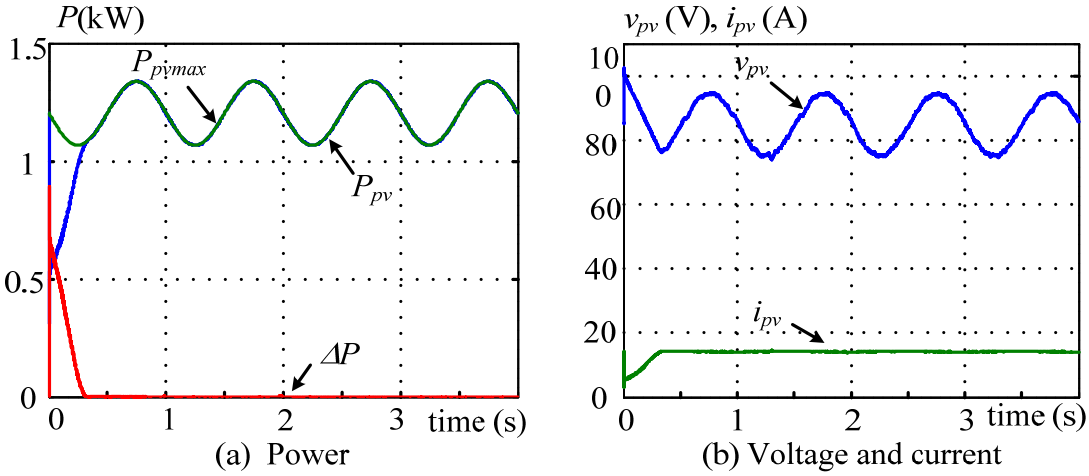


Figure 4-10 EPP algorithm under sinusoidal changing temperature.

The response time of the maximum PV power tracking due to a step irradiance input reflects the tracking speed of the MPPT algorithm. Figure 4-11 shows the PV power tracking waveforms for three MPPT algorithms. Curve (i) is the maximum PV internal power, curves (ii), (iii), and (iv) represent actual PV power under the P&O algorithm, the MP&O algorithm, and the EPP algorithm, respectively. Among these three algorithms, the P&O algorithm is the quickest one, with a tracking time of only 0.15s. The MP&O algorithm is the slowest one that needs doubled tracking time of 0.3s. The EPP algorithm needs 0.2s tracking time, quicker than the MP&O algorithm but slower than the P&O algorithm.

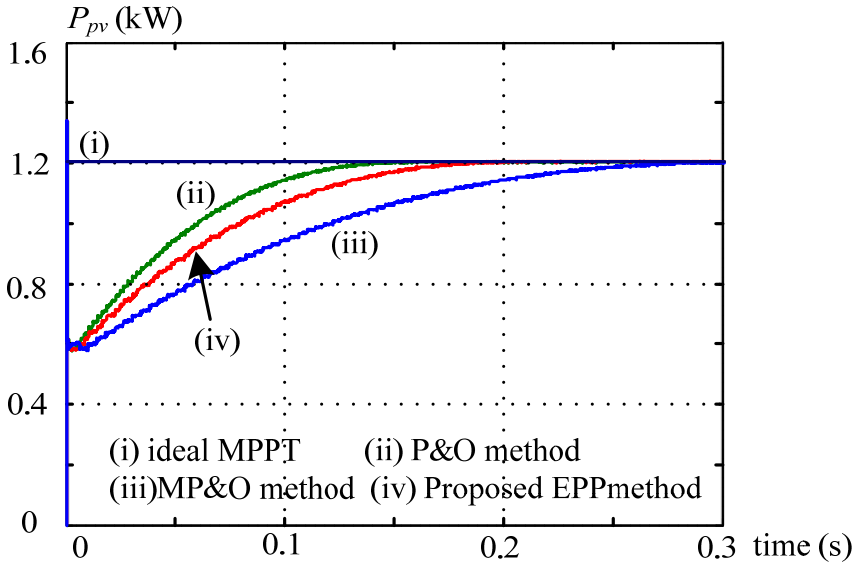


Figure 4-11 The PV power of P&O, MP&O, EPP and ideal MPPT under step changing irradiance.

4.4 Experimental Verification

The setup shown in Figure 4-12 is implemented to test the performance of these MPPT algorithms. The setup consists of: 1) a DC/DC converter, 2) a solar array simulator, 3) a DSP control board, and 4) a digital real time oscilloscope and a PC. The varying irradiance conditions are simulated using the Solar Array Simulator (SAS) E4351B. The current and voltage characteristics of five BPSX60 multi-crystalline PV modules connected in a series are fed to the simulator. The simulated PV arrays have a short-circuit current I_{sc} = 3.87A , a maximum power point current I_{mp} = 3.56A, open circuit voltage of V_{oc} = 105V and a maximum power point voltage of V_{mp} = 84V. A Visual Basic software application is implemented to facilitate the change of the output power as a sine function of the irradiance and temperature. The simulator is connected to the PC using a USB/GPIB interface. The power settings generated by the software application are also fed to the DSP module though the UART port. The calculated power, together with the power values fed from the software application, is provided to the D/A module in order to compare and analyze the MPPT algorithms.

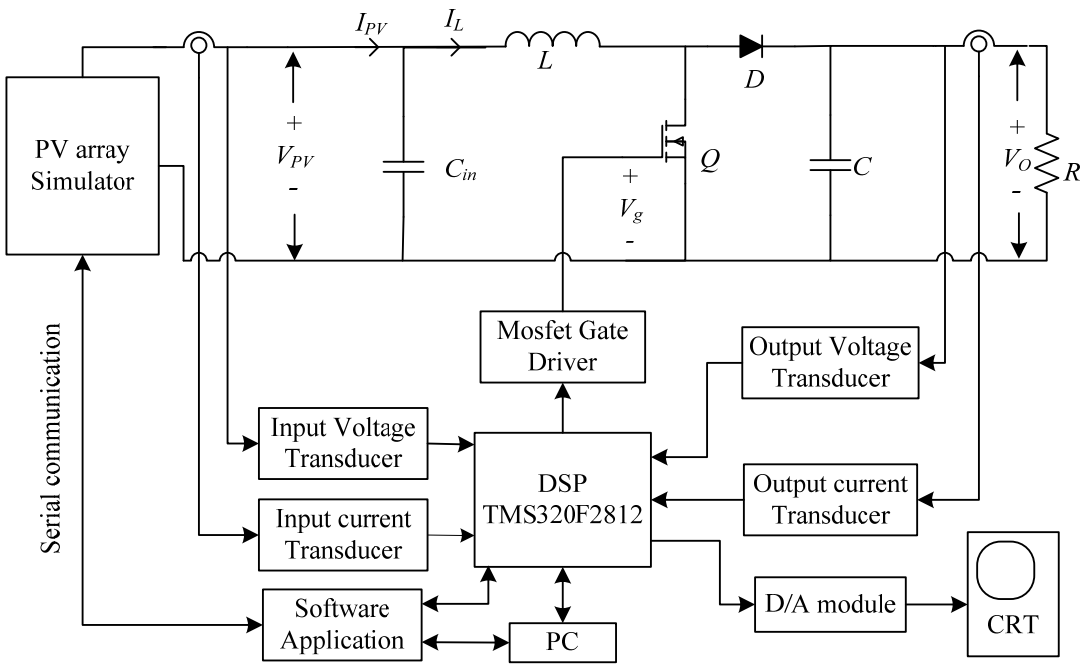


Figure 4-12 Block diagram of the experimental PV system with MPPT control.

The DC/DC converter is a 1KW boost converter working at a switching frequency of 100 kHz. The parameters of the converter are given in Table 4-1. The MPPT algorithm and the control of the DC/DC converter are implemented on TI TMS320F2812 DSP. The DSP measured the input current and input voltage though the A/D module and calculated the power obtained from the SAS. The duty cycle is used as the control variable in order to simplify the control structure of the system [21]. The D/A module is implemented as a pulse-width-modulated (PWM) signal and a two-stage low-pass filter. The update rate of the MPPT algorithms is set to 25msec. The prototype implemented for the experiment is shown in Figure 4-13.

Table 4-1 DC/DC Converter Parameters

Parameter	Value
Inductance *L*	265μH
Capacitor *C*	1.36mF
MOSFET switch *Q*	36A 500V
Diode *D*	60A 600V
Switching frequency	100 kHz
MPPT update rate	25msec

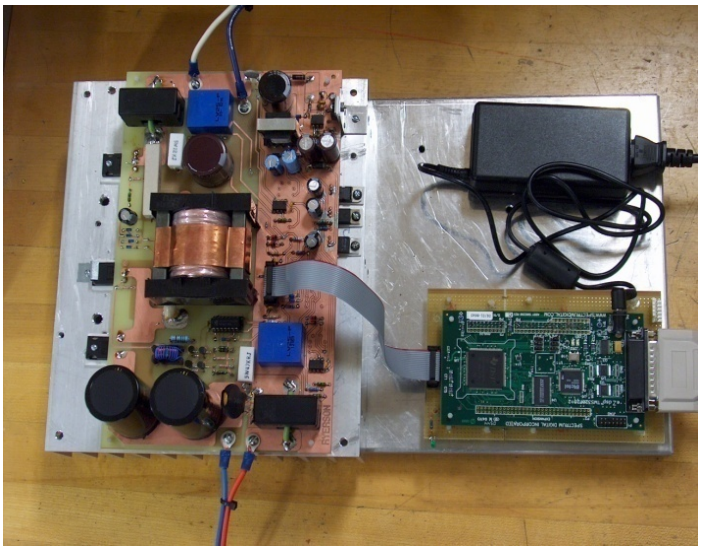


Figure 4-13 1kW experimental prototype.

4.4.1 Results under Constant Environment Conditions

At constant irradiance and temperature, the P&O algorithm oscillates around the maximum power point. This can easily be seen from the oscillation of the PV array current i_{pv} and voltage v_{pv} waveforms in Figure 4-14.

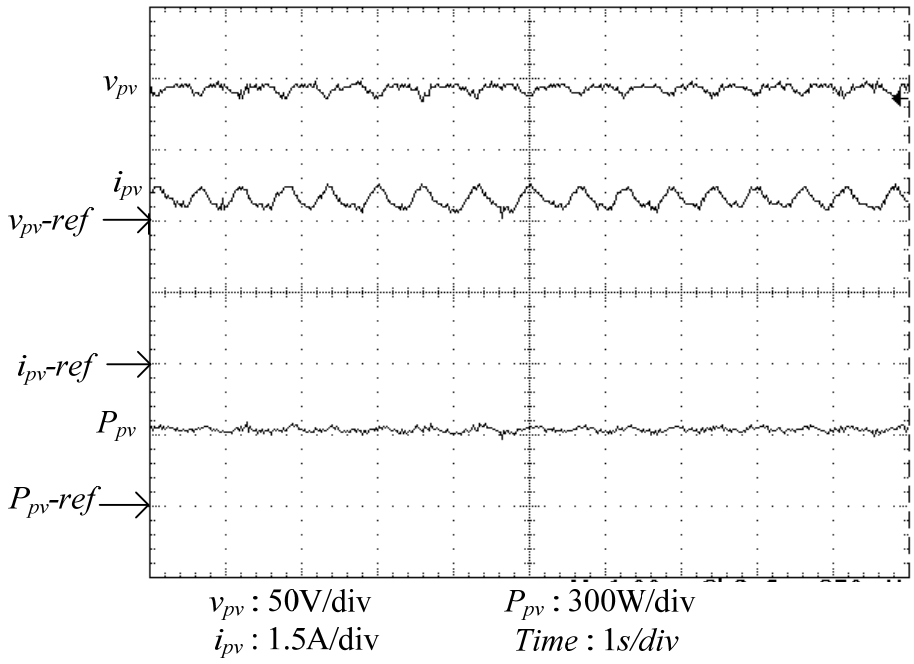


Figure 4-14 Measured performance of P&O algorithm during constant conditions.

The PV array current i_{pv} and voltage v_{pv} waveforms with MP&O algorithms are shown in Figure 4-15. They have much less oscillation since the estimate mode reduces the speed of the algorithm.

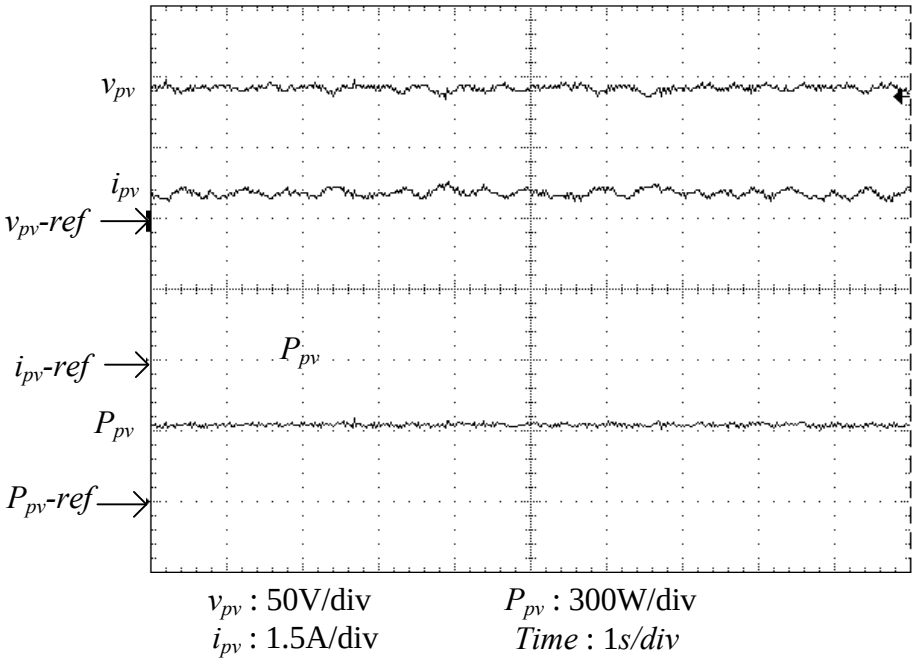


Figure 4-15 Measured performance of MP&O algorithm during constant conditions.

The performance of the EPP algorithm is identical to the MP&O under constant environmental conditions. Figure 4-16 shows the PV array current i_{pv} and voltage v_{pv} waveforms with the EPP algorithm. They are almost identical to the ones shown in Figure 4-15 for the MP&O. Next, the three algorithms are tested with different environmental conditions simulated by the SAS.

4.4.2 Results under Irradiance Change

The change of irradiance results in vertical shifting of the I/V curve of the PV array as shown in Figure 1-6. This change can be implemented as the shifting of the maximum operating current and the short-circuited current values. In this experiment, the irradiance is changed from 1KW/m^2 to 600W/m^2 following a sine function with a period of 5sec. Figure 4-17, Figure 4-18 and Figure 4-19 show the responses of the P&O, MP&O and EPP algorithms respectively, where P_{max} is the reference maximum power set by the software application, P_{pv} is the power obtained from the solar array and ΔP is the difference between them.

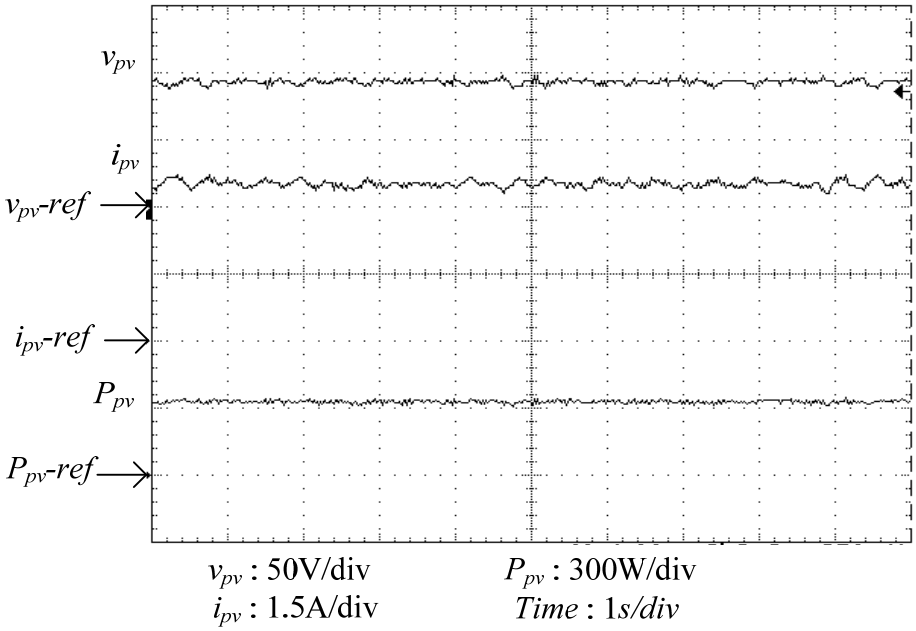


Figure 4-16 Measured performance of EPP algorithm during constant conditions.

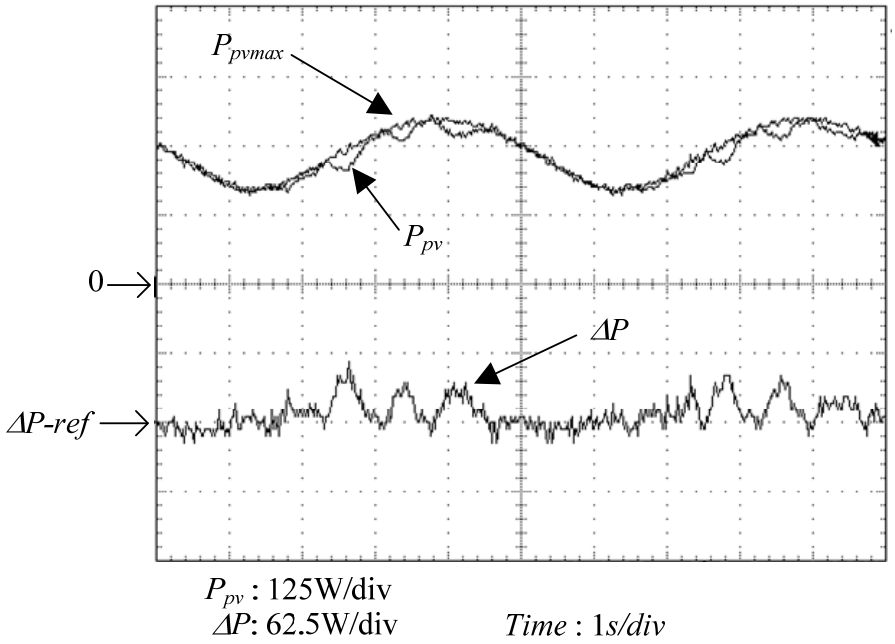


Figure 4-17 Measured performance of P&O algorithm under sinusoidal changing irradiance.

The erratic behavior of the P&O algorithm under fast-changing irradiance is obvious from waveforms of Figure 4-17. The same power profile is applied to the MP&O algorithm as seen in

Figure 4-18. The MP&O algorithm is capable of tracking the MPP accurately during the change in irradiance. The EPP algorithm also tracks the MPP accurately and its performance is similar to the MP&O algorithm as shown in Figure 4-19.

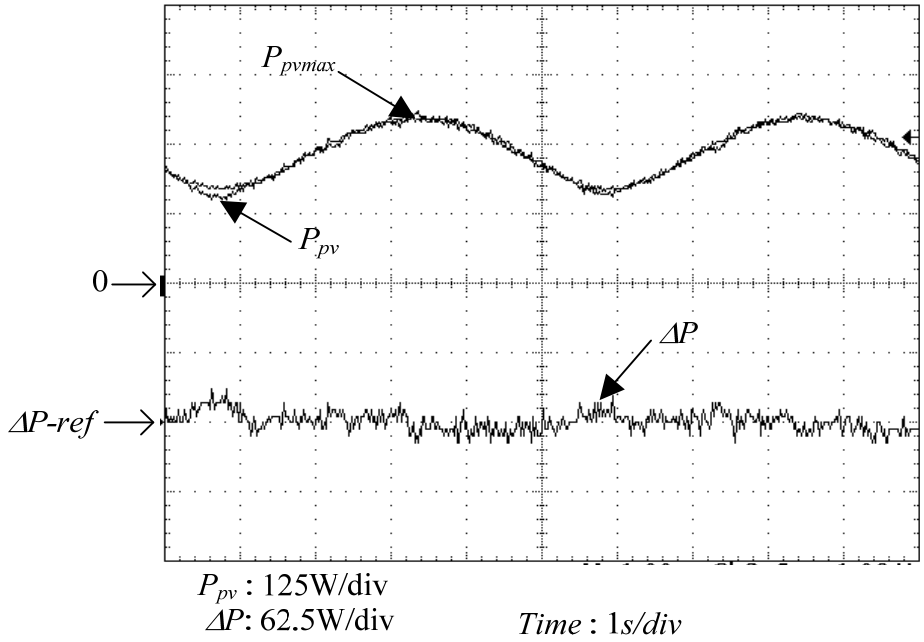


Figure 4-18 Measured performance of MP&O algorithm under sinusoidal changing irradiance.

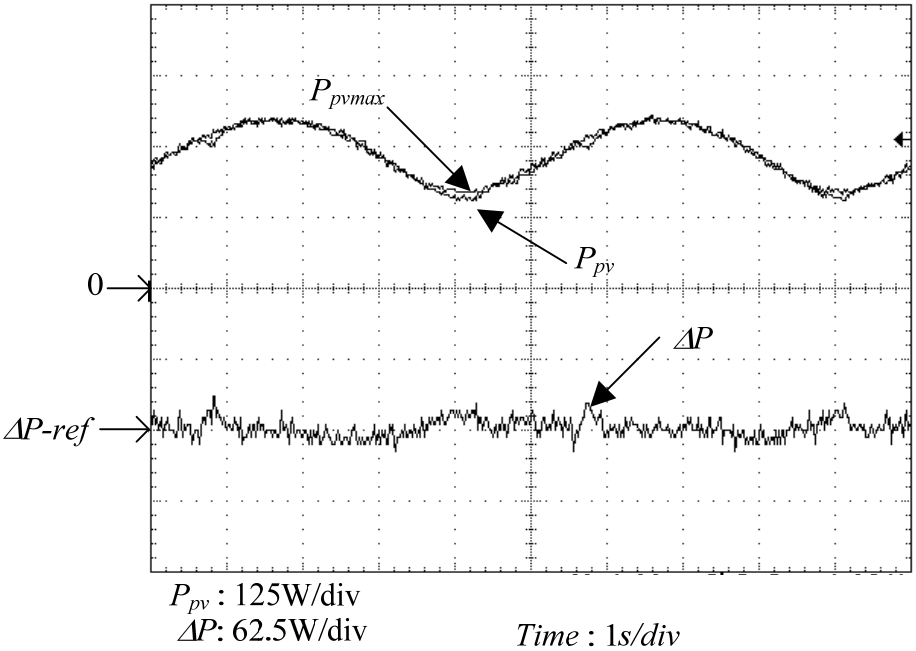


Figure 4-19 Measured performance of EPP algorithm under sinusoidal changing irradiance.

4.4.3 Results under Temperature Change

Although the change in temperature of the PV array is a slow process in residential type applications, it might be much faster and wider in other PV array application. For an inclusive evaluation of the algorithms, the change in temperature from -25°C to 75°C is considered. The change results in shifting the IV curve horizontally, as in Figure 1-7, and is implemented as a function of sine with a period of 6 sec. Figures 4-20, 4-21 and 4-22 show the performance of the PV system under the P&O, MP&O and EPP algorithms.

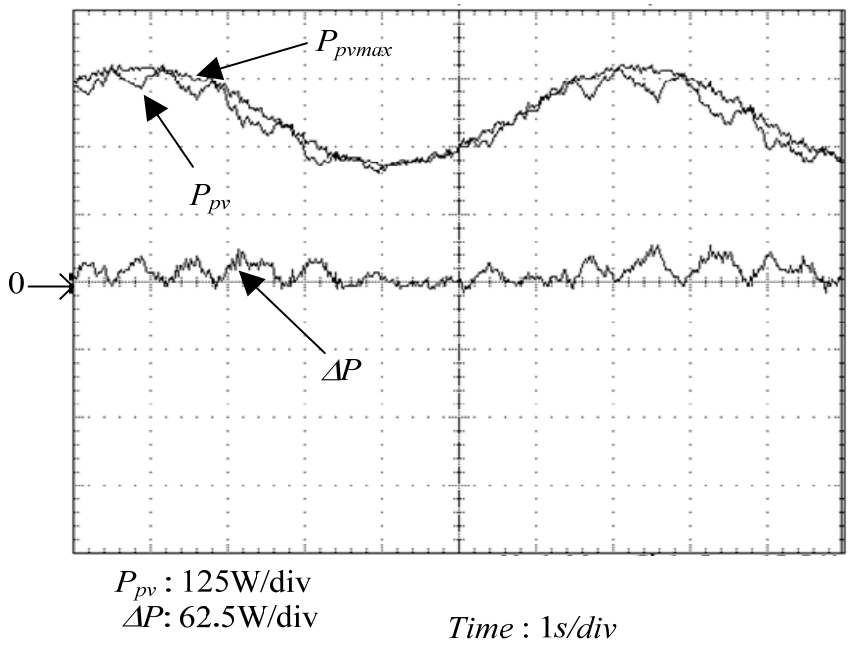


Figure 4-20 Measured performance of P&O algorithm under sinusoidal changing temperature.

Also during a temperature change the P&O algorithm experiences irregular behavior as shown in Figure 4-20. On the other hand, Figures 4-21 and 4-22 show the performance of the MP&O and EPP algorithms, which is more consistent and stable than the P&O algorithm.

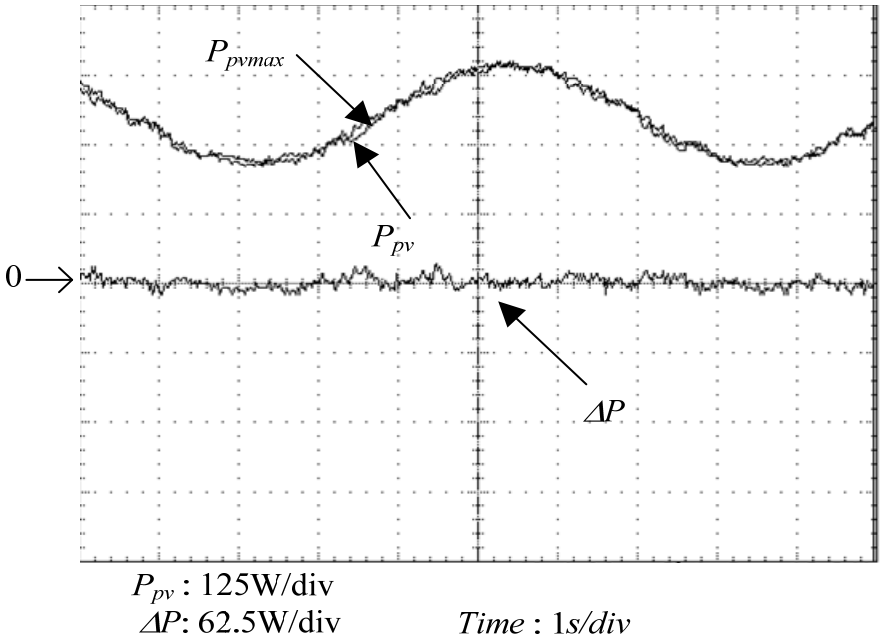


Figure 4-21 Measured performance of MP&O algorithm under sinusoidal changing temperature.

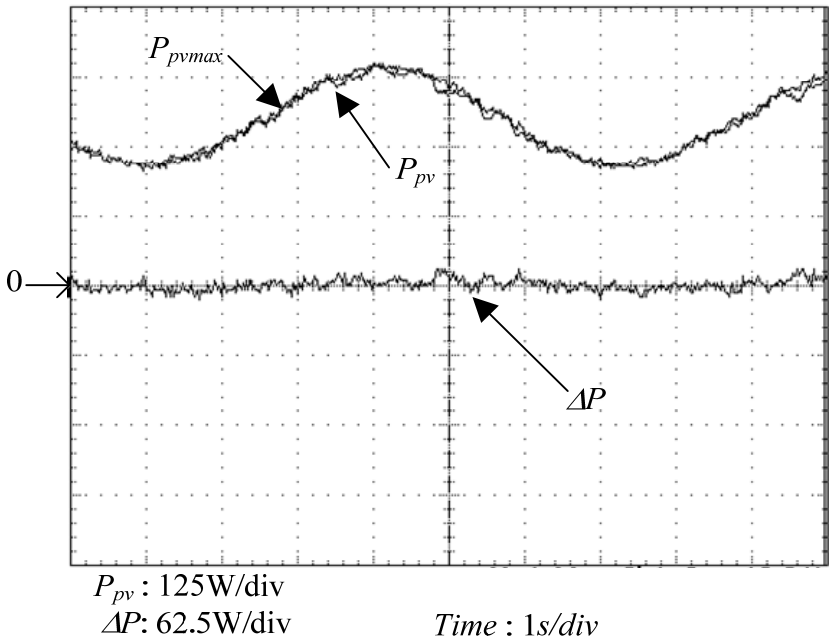


Figure 4-22 Measured performance of EPP algorithm under sinusoidal changing temperature.

4.4.4 Results under Step Change in Irradiance

Step change response is one of the most important parameters of MPPT algorithms since it is a measure of the speed of the algorithms. Figures 4-23, 4-24 and 4-25 show the response of the P&O, MP&O and EPP algorithms under a step change of irradiance from 700W/m^2 to 1kW/m^2. As shown in the three graphs, there is a 100msec delay in the response. This is mainly due to the delay in the response of the solar array simulator to the commands of software applications. As expected, the P&O algorithm has the fastest response with 300msec rise-time. The EPP algorithm has the next fastest response with 400ms rise-time, while the slowest response is the MP&O with 600ms rise-time.

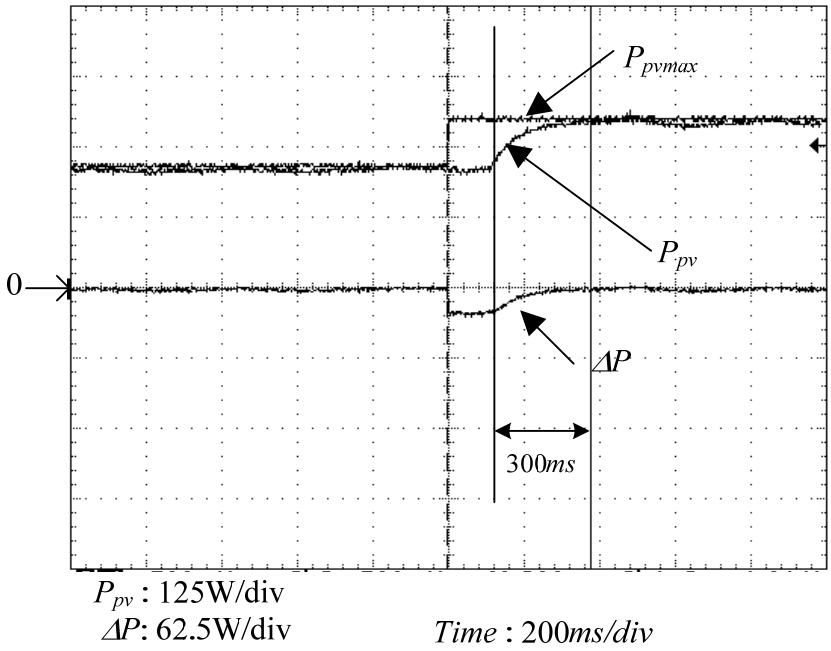


Figure 4-23 Measured performance of P&O algorithm under step changing irradiance.

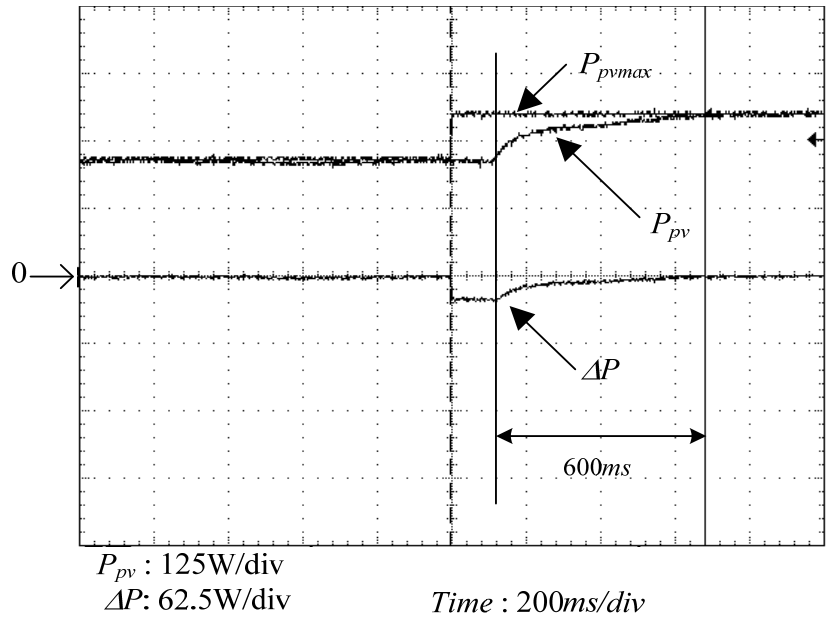


Figure 4-24 Measured performance of MP&O algorithm under step changing irradiance.

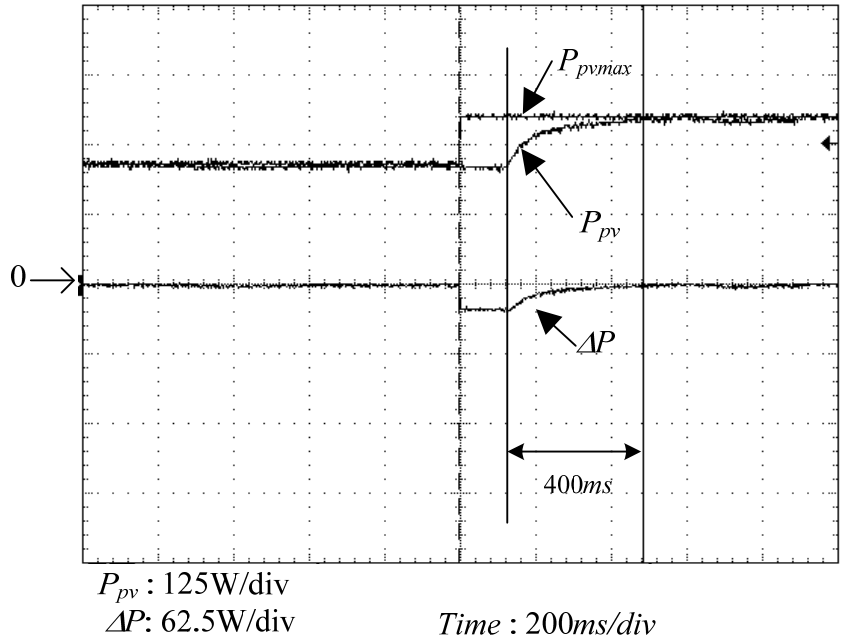


Figure 4-25 Measured performance of EPP algorithm under step changing irradiance.

4.5 Conclusion

Three MPPT algorithms are investigated in this chapter, including the P&O, MP&O and EPP algorithm. The P&O algorithm experiences difficulties in tracking the MPP during a rapid change in environmental conditions. The MP&O algorithm has a slower speed than the P&O, but is able to track the MPP during the change in environmental conditions. The EPP algorithm, is a

compromise in the realm of speed between both algorithms. Nonetheless it operates with the same performance as the MP&O algorithm.

It is verified by simulation that the EPP algorithm can provide accurate and reliable maximum power tracking performance even under a rapidly changing irradiance condition. In addition, the tracking speed of the EPP algorithm is significantly improved compared to the modified MP&O algorithm. A DSP-controlled PV energy conversion system was used to evaluate the performance of the MPPT algorithms experimentally. The EPP algorithm was tested versus the P&O algorithm and its modified version, the MP&O. The algorithms were tested against fast change in irradiance, fast change in temperature and step change in irradiance. The experimental results are in accordance with the simulation: the EPP algorithm has achieved the same accuracy as the MP&O with a speed comparable to the P&O speed, and therefore is recommended for use in practical PV energy conversion systems.

Chapter 5

Anti-Islanding Method with Reduced THD Injection and Fast Dynamic Response

5.1 Introduction

Section 1.5 described the islanding phenomenon and discussed different methods used to detect its formation. Passive methods alone are not sufficient to detect islands when the load consumption is close to the generated power, which results in a large non-detection zone (NDZ). Active methods are used in conjunction with passive ones to reduce the NDZ, but they usually result in degrading the power quality of the grid. Among the active methods, the active frequency drift (AFD) method has drawn increased attention in literature because of its ability to effectively detect islanding with a smaller NDZ [63, 112-115]. In the AFD method, a perturbation is normally injected to the current waveform that causes the inverter output frequency to drift in the case of islanding operations, which does not happen when the grid is available. The frequency drift can then be easily detected with the boundary limits.

Unfortunately, the smaller NDZ obtained with the AFD method compared to the passive methods comes at the expense of increased line current THD, which degrades the power quality provided by the grid-tied converter [74]. The loss in power quality is inherent to the AFD method due to the distortion injected into the current waveform. In order to minimize the impact on power quality, several variations of the AFD methods have been proposed in the literature, such as the AFD with pulsation of chopping fraction [116]. However, these methods introduce a design compromise or tradeoff between the amount of distortion added to the system and the reduction of the NDZ.

In this chapter, a new distortion injection to the current waveform is presented and analyzed. The proposed perturbation introduces lower THD to the current waveform, while improving the NDZ compared to the AFD method. The performance of the proposed method is derived analytically and investigated by simulation using MATLAB. Validation of the analysis and simulation is obtained experimentally using a prototype setup. The prototype is essentially a

single phase, grid-tied photovoltaic distributed generation system with local *RLC* loads, which is developed according to the IEEE Standard 929 and IEEE Standard 1547.1.

5.2 Active Frequency Drift Method Overview

An AFD method proposed in the literature and introduced in Section 1.5.3 is analyzed in this section. This analysis is also necessary for comparison purposes in later sections of this chapter. The AFD method is based on the injection of a zero conduction time t_z to the current waveform of the original reference current of the inverter, to force a frequency drift in case of islanding operation, as shown in Figure 5-1. This distortion will result in the shift of the phase angle of the fundamental component of the current.

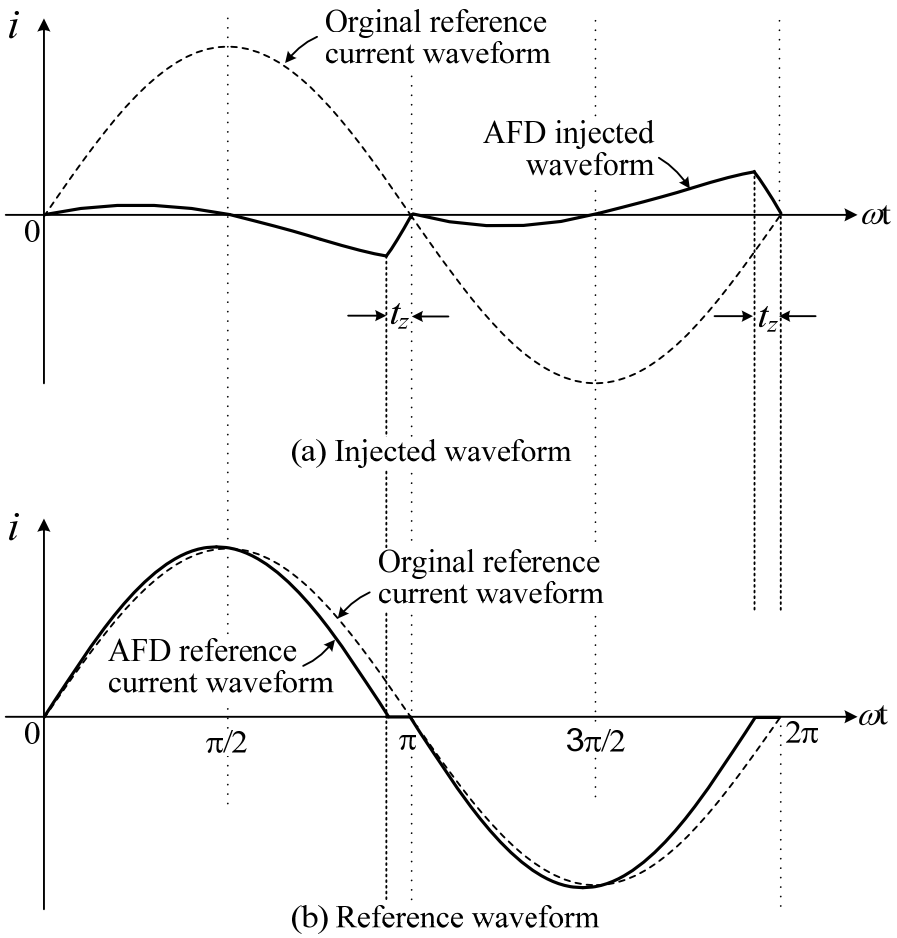


Figure 5-1 AFD method: a) Original reference current and injected current waveforms b) Original reference current and AFD reference current waveforms.

The AFD reference current waveform shown in Figure 5-1 can be defined as:

$$i_{AFD}(t) = \begin{cases} I\sin(2\pi f' t) & \rightarrow 0 \le \omega t < \pi - t_z \\ 0 & \rightarrow \pi - t_z \le \omega t < \pi \\ I\sin(2\pi f' t) & \rightarrow \pi \le \omega t < 2\pi - t_z \\ 0 & \rightarrow 2\pi - t_z \le \omega t \le 2\pi \end{cases} \tag{5-1}$$

where $f' = f\left(\frac{1}{1-C_f}\right)$.

The relation between the dead time t_z and the chopping factor C_f was given in Eq. (1-13) and repeated here:

$$C_f = \frac{2t_z}{T} \tag{5-2}$$

Basically, the chopping factor defines the amount of drift introduced to the frequency *f*. Note that since the current waveform has a different frequency *f′*, the vertical axis is shifted to facilitate the zero current period t_z. The distortion introduced by t_z ,which defines the amount of drift introduced to the frequency *f*, can be deducted from the original reference current as shown in Figure 5-1(a). According to Eq. (5-2), the greater the t_z, the greater the chopping factor. Hence the larger perturbation is introduced to the current. In contrast, if $t_z = 0$, from Eq. (5-2), C_f is also zero, then according to Eq. (5-1) the AFD reference current waveform is equal to the original reference current waveform ($i_{AFD}(t) = I\sin(2\pi f t)$).

When this modified waveform is applied to an isolated DG system with an *RLC* load, the frequency of the load will change such that the phase angle of the *RLC* load will satisfy the following equation [54, 117, 118].

$$\phi_L = \tan^{-1}\left[R^{-1} + (j\omega L)^{-1} + j\omega C\right]^{-1} = 0.5\pi C_f \tag{5-3}$$

where ϕ_L is the phase angle of the load.

This method is effective for resistive loads but has a larger NDZ for some RLC load combinations. To overcome this problem, positive feedback AFD methods have been proposed [66]. These improve the NDZ for different load types, but still affect the power quality by introducing a higher THD into the system.

5.2.1 Islanding Detection Analysis

Undetected islanding can happen when there is a balance between the power (both active and reactive) delivered by the inverters and consumed by the local loads of the DG system. A mismatch would lead to a change in the amplitude, frequency or both, of the load voltage, consequently resulting in islanding detection. This mismatch can be forced by injecting reactive power to the system by introducing a distortion to the current waveform. In order to drive the load frequency out of limit faster and with a smaller NDZ, a larger amount of reactive power ($\Delta Q/P$) is needed, as can be seen from Eq. (1-10). This is shown again by Eq. (5-4):

$$-5.95\% \leq \frac{\Delta Q}{P} \leq 4.11\% \tag{5-4}$$

For non-sinusoidal waveforms the active power is defined in IEEE Std 1459-2010 [119] as:

$$P = V \cdot I_1 \cdot \cos(\phi_1), \tag{5-5}$$

where I_1 and ϕ_1 are the rms value and the phase angle of the fundamental waveform respectively. On the other hand the reactive power is defined as:

$$Q = V \cdot I_1 \cdot \sin(\phi_1), \tag{5-6}$$

from which

$$\frac{Q}{P} = \tan(\phi_1). \tag{5-7}$$

Equation (5-7) shows the relationship between the reactive power generated by the distortion of the current waveform and the phase angle of the fundamental waveform. In the AFD method, a distortion is added to the current, which forces the fundamental component of the current to shift by angle ϕ_1. It is known from [63] that $Q/P = THD$ for the AFD method. Consequently increasing the reactive power injected into the load to reduce the NDZ will increase the THD of the current wave form.

5.2.2 THD Problem in AFD Method

For the AFD method to be effective, the chopping factor C_f needs to be fairly large, which directly affects the THD of the current waveform [61, 66]. The relationship between THD and C_f has been reported to be linear [63, 66]. The maximum allowable C_f is limited by the maximum THD ($< 5\%$ according to Table 1-3). It is mentioned that a C_f of 0.046 results in a THD of 4.88% [114]. Hence, like most of the active methods, the AFD reduces the quality of the power delivered to the grid. Generally speaking, the larger the chopping factor, the smaller the NDZ and the higher the THD for AFD-based methods.

The injected current waveform used in AFD, as shown in Figure 5-1a, introduces high-low order frequency harmonics to the original current waveform. This can be seen from the fact that the injected current waveform changes slowly over the half cycle of the original reference current. In other words, the phase shift of the fundamental component (ϕ_1) is achieved gradually over a half cycle, which in consequence translates to high-low order harmonics.

5.3 Improved AFD Anti-Islanding Method

Instead of introducing a gradual change in the current waveform over half cycle, a sudden change can also introduce the necessary phase shift of the fundamental component (ϕ_1) while introducing less THD. The following section describes the proposed waveform, which is analyzed analytically and compared to classic AFD.

5.3.1 Proposed Current Waveform Distortion

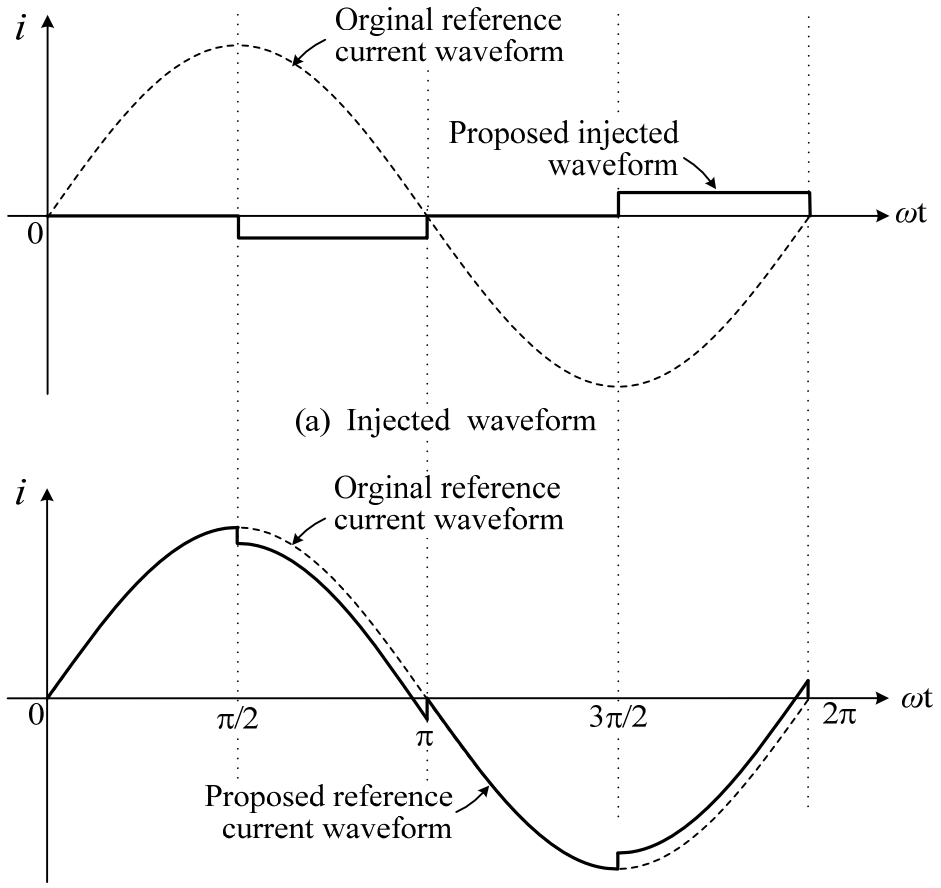
An effective way to shift the fundamental component phase angle of a sine wave is by introducing a step change in the amplitude in the 1st and 3rd or 2nd and 4th quarters of the waveform. This perturbation injection and the resulting reference waveform are illustrated in Figure5-2a and b respectively. In these cases, the 2nd and 4th quarters are considered. The resulting reference current waveform is defined by:

$$i(t) = \begin{cases} I\sin(\omega t) & \rightarrow 0 \le \omega t < \pi/2 \\ I\sin(\omega t) - KI & \rightarrow \pi/2 \le \omega t < \pi \\ I\sin(\omega t) & \rightarrow \pi \le \omega t < 3\pi/2 \\ I\sin(\omega t) + KI & \rightarrow 3\pi/2 \le \omega t \le 2\pi \end{cases} \tag{5-8}$$

where I is the current amplitude, ω is the grid frequency and K is the distortion factor.

In order to analyze the harmonic contents and the phase angle of the proposed current waveform, the Fourier series coefficients of the fundamental components are found:

$$F(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}[a_n \cos(\omega_n t) + b_n \sin(\omega_n t)] \tag{5-9}$$



(b) Current reference waveform

Figure 5-2 Proposed AFD method: a) Original reference current and proposed injected current waveforms, b) Original reference current and proposed reference current waveforms.

where $$a_1 = \frac{2KI}{\pi}$$ (5-10)

and $$b_1 = I\left(1 - \frac{2K}{\pi}\right)$$ (5-11)

The fundamental rms current of the proposed method is:

$$I_1 = I\sqrt{1 + \frac{8K^2}{\pi^2} - \frac{4K}{\pi}}$$ (5-12)

and the displacement angle is:

$$\phi_1 = \tan^{-1}\left(\frac{a_1}{b_1}\right) = \tan^{-1}\left(\frac{2K}{\pi - 2K}\right)$$ (5-13)

The rms value of the current waveform is defined as:

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2(t)dt},$$ (5-14)

Then the rms value for the proposed current waveform can be obtained replacing Eq. (5-8) in Eq. (5-14), which yields:

$$I_{rms} = I \cdot \sqrt{\frac{1}{2} - \frac{2K}{\pi} + \frac{K^2}{2}}.$$ (5-15)

In addition, the THD of the current waveform is defined as:

$$\text{THD} = \frac{\sqrt{I_{rms}^2 - I_{1rms}^2}}{I_{1rms}}$$, with $I_{1rms} = \frac{I_1}{\sqrt{2}}$. (5-16)

Substituting Eq. (5-15) and Eq. (5-12) into Eq. (5-16) yields:

$$\text{THD} = \sqrt{\frac{K^2\left(\pi^2 - 8\right)}{\pi^2 - 4\pi K + 8K^2}},$$ (5-17)

In addition, by replacing in Eq. (5-7) the terms in Eq. (5-10), Eq. (5-11) and Eq. (5-13), the Q/P ratio of the proposed waveform can be computed as:

$$\frac{Q}{P} = \frac{2K}{\pi - 2K}. \tag{5-18}$$

Using Eq. (5-17) and Eq. (5-18), the THD and the Q/P ratio can be calculated for different distortion factors (K). For example, with a distortion factor of K=0.075 the THD of the current waveform is 3.42% with a Q/P ratio of 5%. When compared with traditional AFD, in order to generate the same Q/P ratio of 5%, the THD of the AFD current waveform increases to 5% (more than 30% increase in distortion). Figure 5-3 shows the THD versus Q/P curve for both methods at different values of their respective distortion factors K and C_f. It is obvious that the proposed method always generates less harmonic distortion at any given Q/P value.

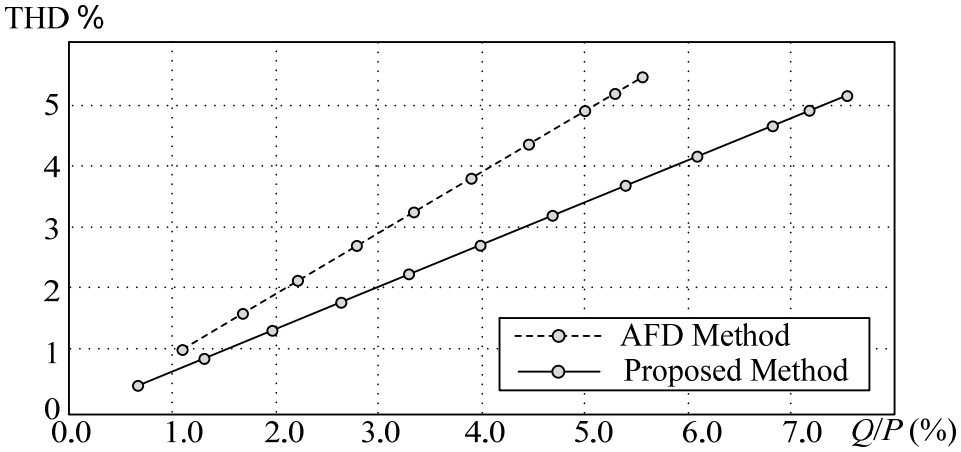


Figure 5-3 THD versus Q/P for the conventional AFD and proposed methods.

Based on the above analysis, it can be concluded that:

- The proposed method can achieve the same results as the conventional AFD method with about a 30% reduction in THD; and
- The proposed method can generate approximately 50% more reactive power to the grid than the conventional AFD method, resulting in better islanding detection. Considering the maximum allowed THD of 5%, the proposed method generates a Q/P of 7.4% whereas the conventional AFD method can only produce a Q/P of 4.8% as shown in Figure 5-3.

5.3.2 Implemented Waveform

The proposed current waveform illustrated in Figure 5-2 has one drawback, the current spikes when crossing zero are difficult to implement in practice. The current controller is not able to follow this sudden change in reference accurately. Therefore a slight modification is introduced to the proposed waveform which eliminates the current spike at zero crossing. The proposed practical current injection and the resulting reference current waveform are shown in Figure 5-4, (a) and (b) respectively. Note that the original motivation, which is to concentrate the perturbation in the 2nd and 4th quarter of the waveform, still holds.

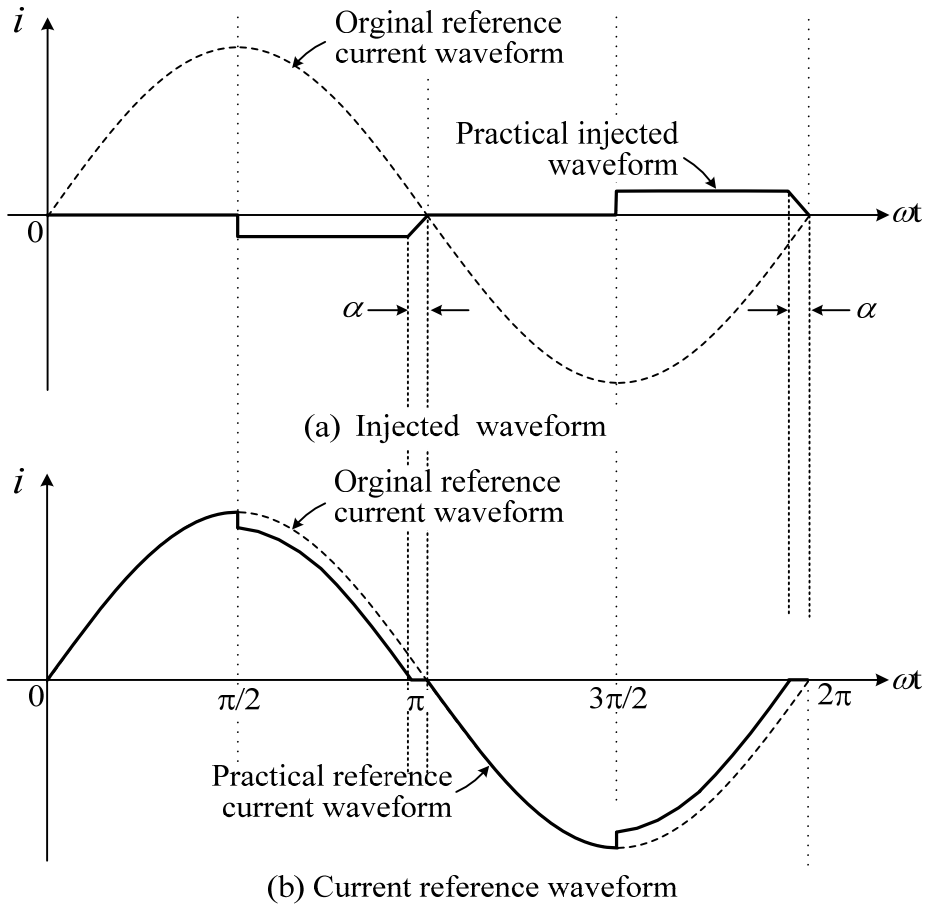


Figure 5-4 Practical proposed improved AFD method: a) Original reference current and practical injected current waveform, b) Original reference current and practical reference current waveform.

The resulting waveform can be defined by:

$$i'(t) = \begin{cases} I\sin(\omega t) & \rightarrow 0 \le \omega t < \pi/2 \\ I\sin(\omega t) - KI & \rightarrow \pi/2 \le \omega t < \pi - \alpha \\ 0 & \rightarrow \pi - \alpha \le \omega t < \pi \\ I\sin(\omega t) & \rightarrow \pi \le \omega t < 3\pi/2 \\ I\sin(\omega t) + KI & \rightarrow 3\pi/2 \le \omega t < 2\pi - \alpha \\ 0 & \rightarrow 2\pi - \alpha \le \omega t \le 2\pi \end{cases} \tag{5-19}$$

where $\alpha = \arcsin(K)$.

For this new current waveform, the Fourier coefficients and the rms value can be computed following the same steps as for the previous waveform, which yields:

$$a_1' = \frac{2KI}{\pi} - \frac{K^2 I}{\pi} \tag{5-20}$$

$$b_1' = I\left(1 - \frac{K\sqrt{1-K^2}}{\pi} - \frac{\arcsin(K)}{\pi}\right) \tag{5-21}$$

The fundamental rms current of the practical method is:

$$I'_{rms} = I \cdot \sqrt{\frac{1}{2} + \frac{K^2}{2} - \frac{3K\sqrt{1-K^2}}{2\pi} - \frac{\arcsin(K)\cdot(1+2K^2)}{2\pi}}. \tag{5-22}$$

Since the values for the distortion factor are small ($K \le 0.1$), the quadratic terms $K^2 << 1$ can be neglected. In addition, for small values of K the following holds: $\arcsin(K) \cong K$. Replacing both approximations in Eq. (5-20), Eq. (5-21) and Eq. (5-22) yields the same results obtained for the originally proposed waveform from Eq. (5-10) to (5-18). In summary, the small modification introduced to eliminate the current spike at zero crossing and make the proposed waveform practical, does not affect the THD and NDZ achieved with the originally proposed waveform.

5.4 Simulation Results

In order to verify the proposed method, a single phase photovoltaic distributed generation system with a local RLC load has been considered. The power circuit of the system is shown in Figure 5-5. The system parameters are listed in Table 5-1. The simulations for both AFD and the

proposed method were implemented in a Matlab/Simulink platform together with Over/Under voltage and Over/Under Frequency relays.

The active frequency drift method was simulated with a chopping factor C_f of 0.046. The resulting current waveform is shown in Figure 5-6(a). The simulation of the proposed method was performed considering a distortion factor *K* of 0.08. These values were chosen since they generate the same Q/P as shown before. The resulting current waveforms for both the original and practical cases are shown in Figure 5-6 b and c respectively.

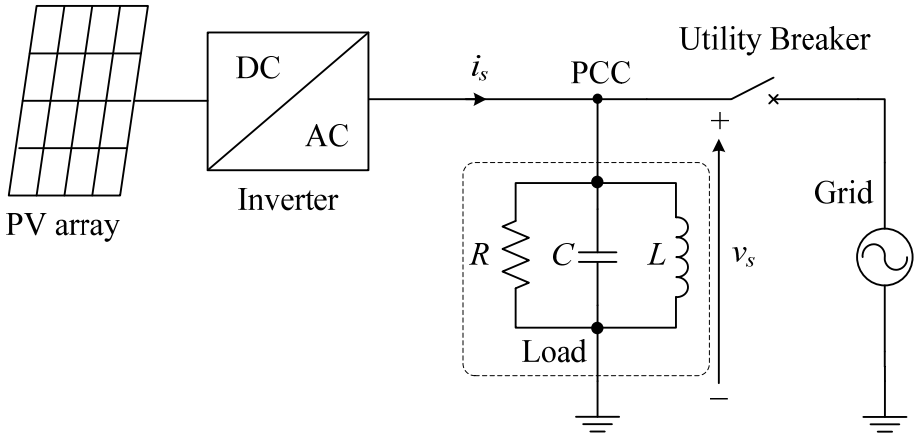


Figure 5-5 DG photovoltaic grid-connected system with local RLC load.

Table 5-1 DG Circuit Parameters

Parameter	**Value**
Power	300W
Voltage	120V
Grid frequency	60Hz
Load resistance	48 Ω
Load capacitance (750VAR)	139.2 μ F
Load inductance (750VAR)	50mH
Normalized Capacitance C_{norm}	1.01
Load Quality Factor Q_f	2.5

The spectra of the three current waveforms are compared in Figure 5-7 along with their THD values. The THD value obtained for the classic AFD current waveform is found to be 4.90% which coincides with the data given in [63] and discussed in the above analysis. The proposed

methods resulted in current waveforms with a THD of 3.65% and 3.64% respectively, around 30% lower than with the classic AFD. Again, these results are consistent with the ones obtained analytically in the previous section, thus verifying the validity of the equations Eq. (5-9) - Eq. (5-22). This also confirms that the approximation introduced by the practical implementation waveform of the proposed method does not affect the power quality. This is therefore a valid approach to overcome the drawback of the original current injection waveform.

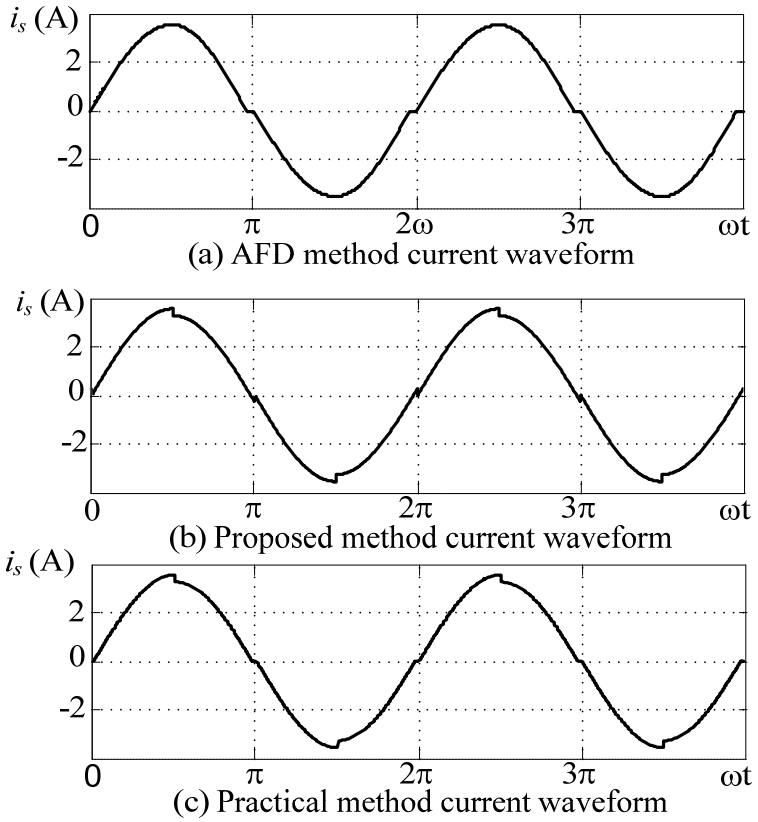


Figure 5-6 Inverter current: a) for AFD with C_f =0.046, b) for original proposed method with K = 0.08c) for practical proposed method with K = 0.08.

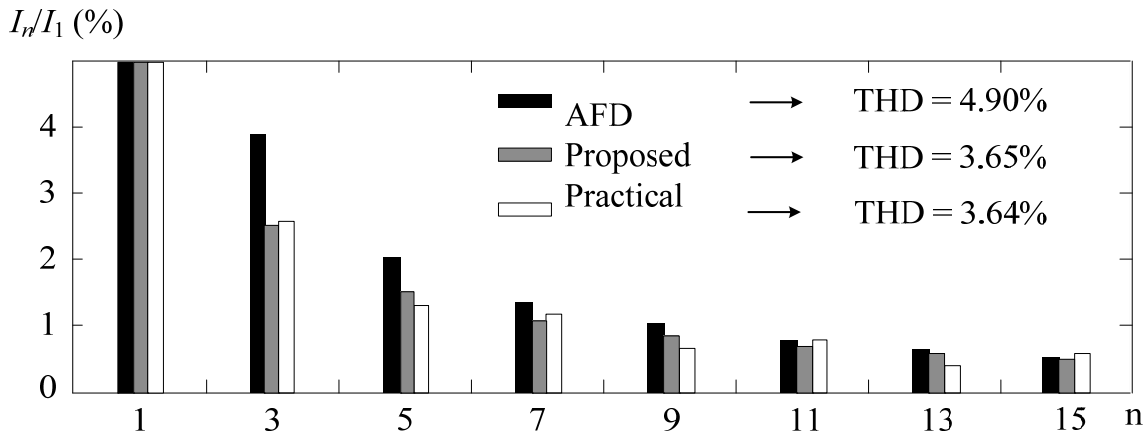


Figure 5-7 Inverter current spectrum: for AFD with C_f =0.046, for original proposed method with K=0.08 for practical proposed method with $K = 0.08$.

When the proposed waveform is applied to an RLC load, the frequency at the PCC will change during islanding until the load phase angle is equal to the displacement angle of the fundamental waveform ϕ_1 given in Eq. (5-13) as shown below:

$$\phi_L = \tan^{-1}\left[R^{-1} + (j\omega L)^{-1} + j\omega C\right] = \tan^{-1}\left(\frac{2K}{\pi - 2K}\right) \tag{5-23}$$

The NDZ of the proposed method can be obtained using Eq. (5-23). Figure 5-8 shows the NDZ of both the AFD and the proposed method mapped into the load space characterized by the quality factor Q_f and the normalized load capacitance C_{norm}. This mapping method relates the NDZ to the IEEE Std 929-2000 requirements in an efficient way [54]. This graph is obtained for the AFD method with a chopping factor $C_f = 0.046$ and the proposed method with a distortion factor $K = 0.105$ which both generate the same $THD = 4.9\%$. Although both methods have the same NDZ shape in relation to the quality factor, the proposed method has a higher NDZ, making the islanding formation in the vicinity of a balanced load more unlikely. This holds true particularly for $Q_f < 5$, which is the usual case in practical applications.

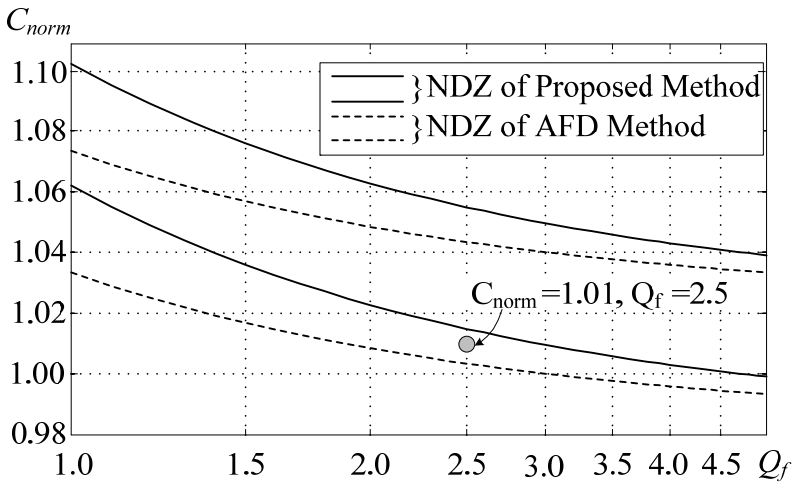


Figure 5-8 NDZ of both ADF and proposed methods for different C_{norm}.

The simulation of the islanding phenomena is performed with load capacitor C=139.2 μ F whose normalized capacitance is C_{norm}=1.01, and a quality factor Q_f=2.5, which is one of the load combinations required by IEEE Std 929-2000 to test against islanding. This load combination is a point shown in Figure 5-8 that lies inside the NDZ of the AFD but outside the NDZ of the proposed method. Here also the AFD method with a chopping factor C_f of 0.046 and the proposed method with a distortion factor K of 0.105 were used. The utility breaker was opened after 4 cycles to simulate the grid disconnection. As expected, the AFD method fails to detect the islanding, and the inverter continues to energize the load beyond the 2-second limit as shown in Figure 5-9. The proposed method forces the frequency of the PCC to increase above the limit in 9 cycles, which triggers the over-frequency relay and causes the islanding operation to be detected, as shown in Figure 5-10.

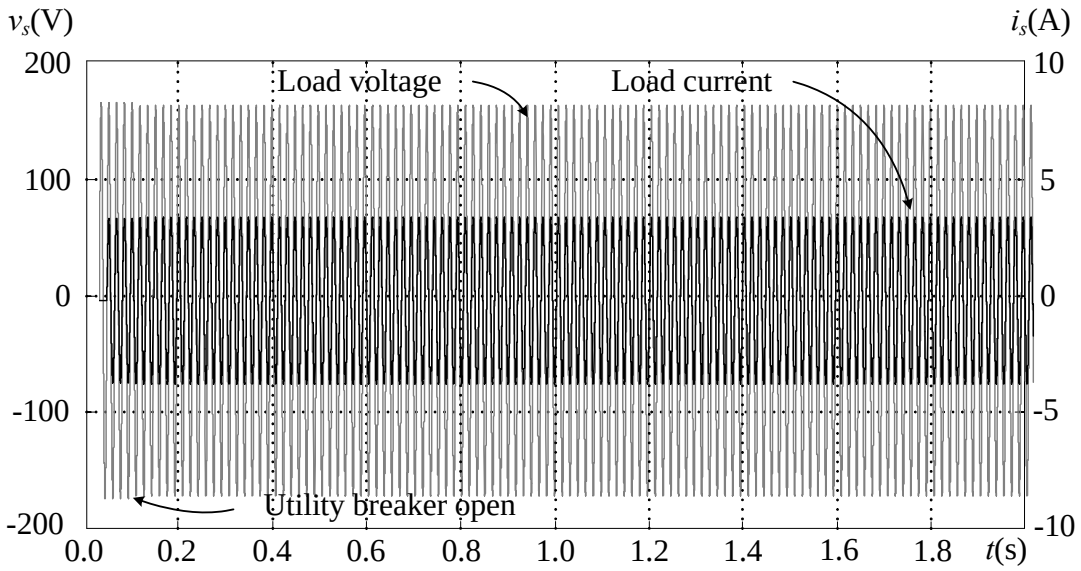


Figure 5-9 Voltage and current at PCC for AFD with C_f =0.046

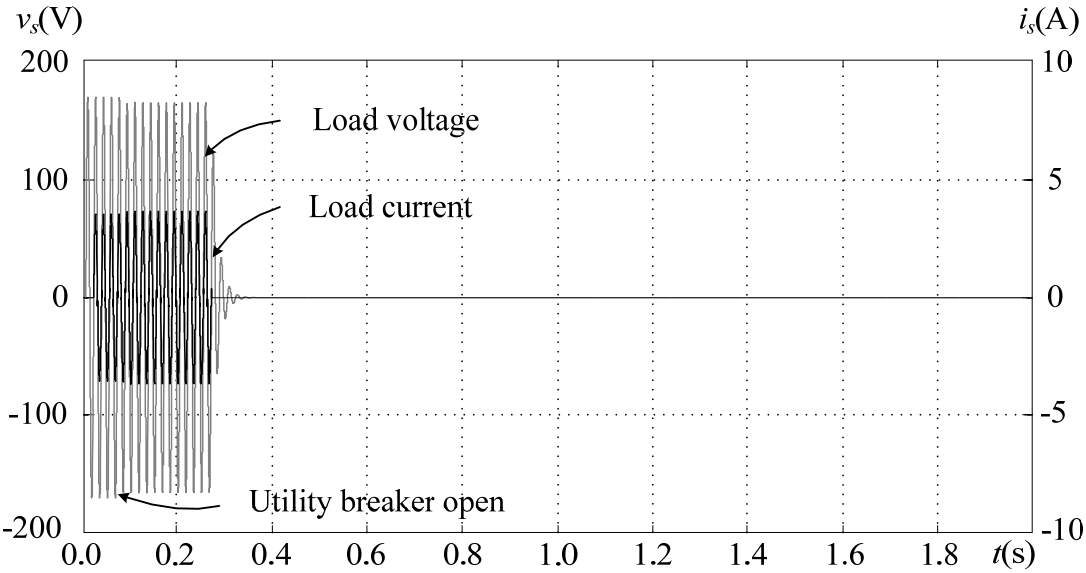


Figure 5-10 Voltage and current at PCC: for proposed method with distortion factor K =0.105.

This effect can be more clearly appreciated in the evolution of the frequency of the system for both methods, shown together for comparison in Figure 5-11.

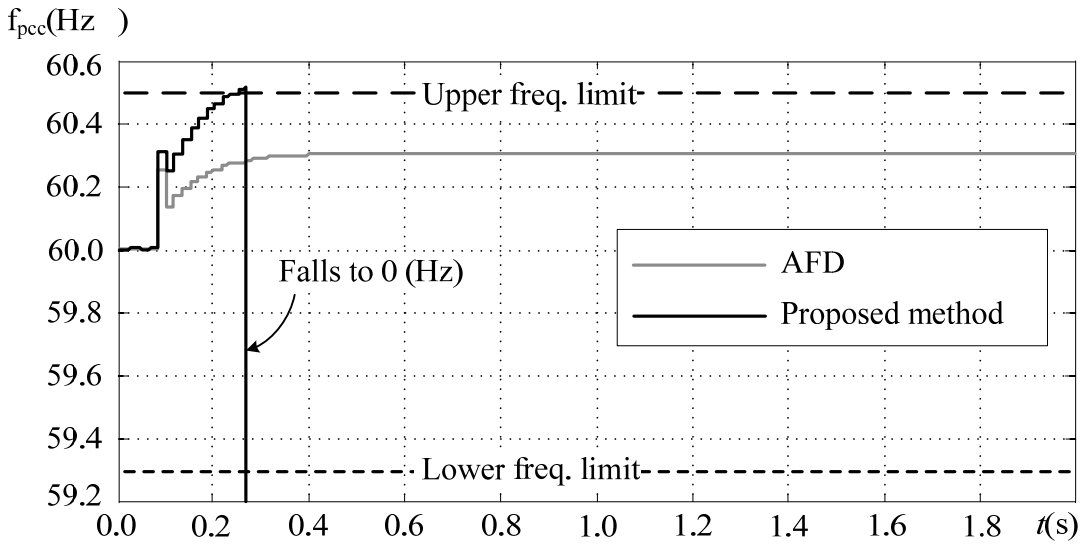


Figure 5-11 System frequency evolution for AFD with chopping factor C_f =0.046 and proposed method with distortion factor K =0.105.

5.5 Experimental Verification

An experimental prototype has been built in order to test the proposed method. The corresponding power circuit of the setup is shown in Figure 5-12. The grid-tied inverter shown in Figure 5-13, is constructed as a MOSFET H-bridge followed by an LC filter (L =1.3mH and C =3 μ F), and connected to a RLC load. The setup uses the same parameters as the ones used for simulation and listed in Table 5-1. A Digital Signal Processor board (TMS320F2812) is used to generate a 20kHz unipolar PWM gate signals and to implement a Proportional Resonant current controller, which is a typical controller for the single phase AC systems to ensure zero steady state error [120, 121].

Figure 5-14 shows the voltage and current waveform of the AFD method with a chopping factor of C_f =0.046, the THD in the current was measured using the power analyzer YOKOGAWA PZ4000 to be 5.16%. The measured active and reactive powers were 334W and 17.4VAR respectively.

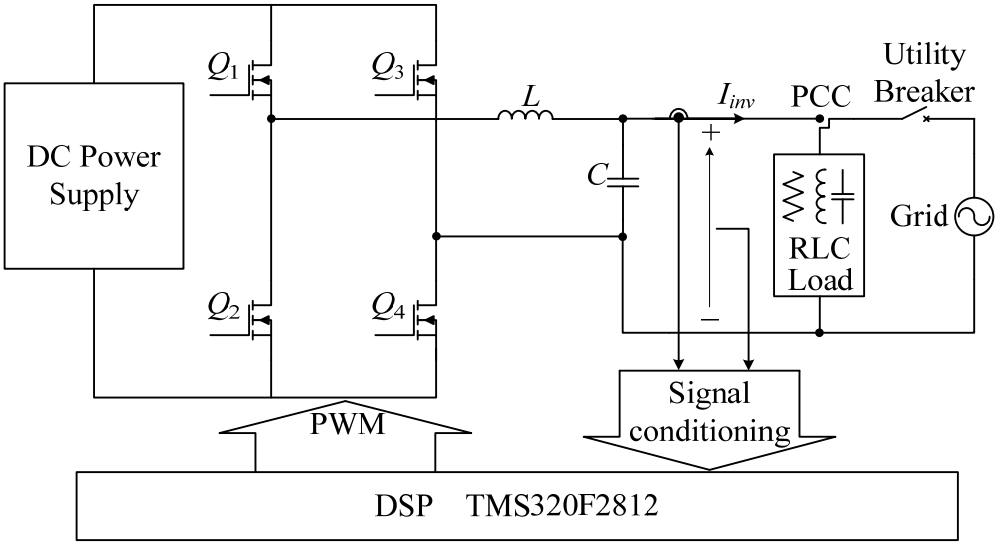


Figure 5-12 Experimental setup power circuit diagram.

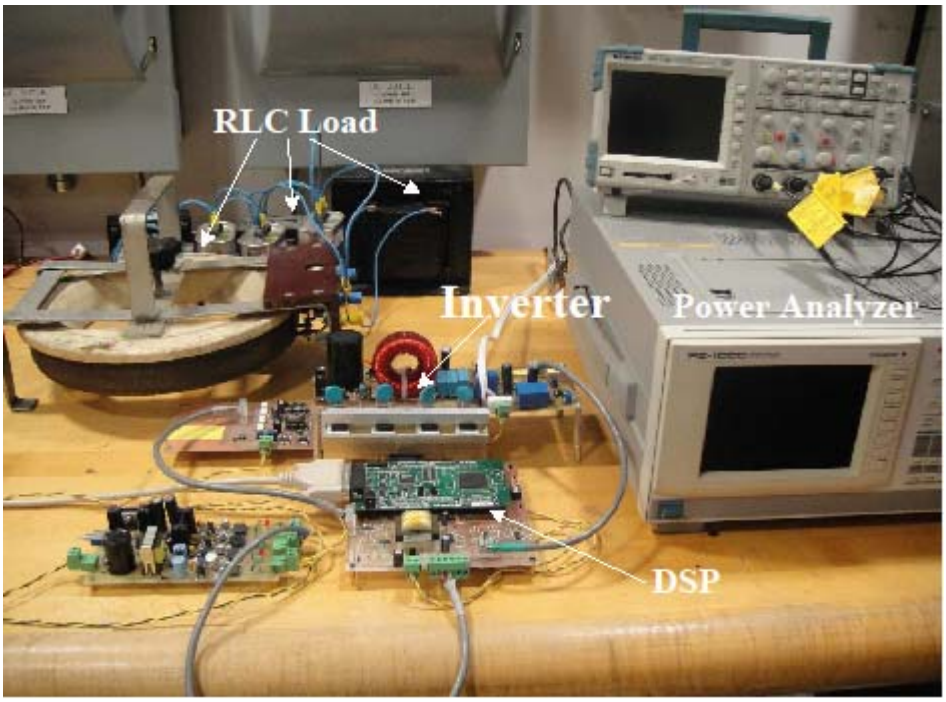


Figure 5-13 Experimental setup.

Also the frequency spectrum of the current waveform is shown, the 3rd and 5th harmonics are the dominant harmonics in accordance with the simulation results shown in Figure 5-8.

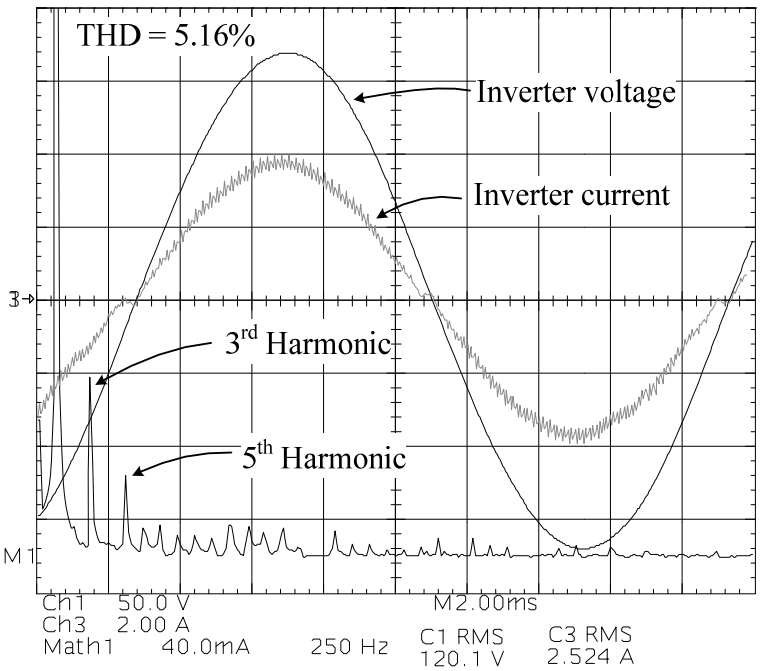


Figure 5-14 Experimental voltage and current waveforms for the AFD method with chopping factor C_f of 0.046.

Figure 5-15 shows the voltage and current waveform of the proposed method with a distortion factor K of 0.08. The THD of the current was measured as 3.91%. The measured active and reactive powers were 335W and 18.2VAR respectively. The experimental results shown in Figure 5-14 and Figure 5-15 match the simulated results of Figure 5-7 and Figure 5-8 for the AFD and the proposed method respectively.

Note that when both methods generate the same amount of reactive power to shift the frequency in case of islanding, the proposed method features a lower THD than the AFD method, as demonstrated analytically and the frequency spectrum of the current waveform of the proposed method has lower 3rd and 5th harmonics as has been shown previously in the simulation results presented in Figure 5-8.

The Islanding detection test is carried out first in accordance with the IEEE 929-2000 standard with a load quality factor Q_f set to 2.5 and with the same parameters as the ones used for simulation as listed in Table 5-1. The AFD method chopping factor is C_f of 0.046 . As can be seen from Figure 5-16, the inverter fails to detect the islanding after the grid is disconnected and continues to energize the load beyond the 2-second limit.

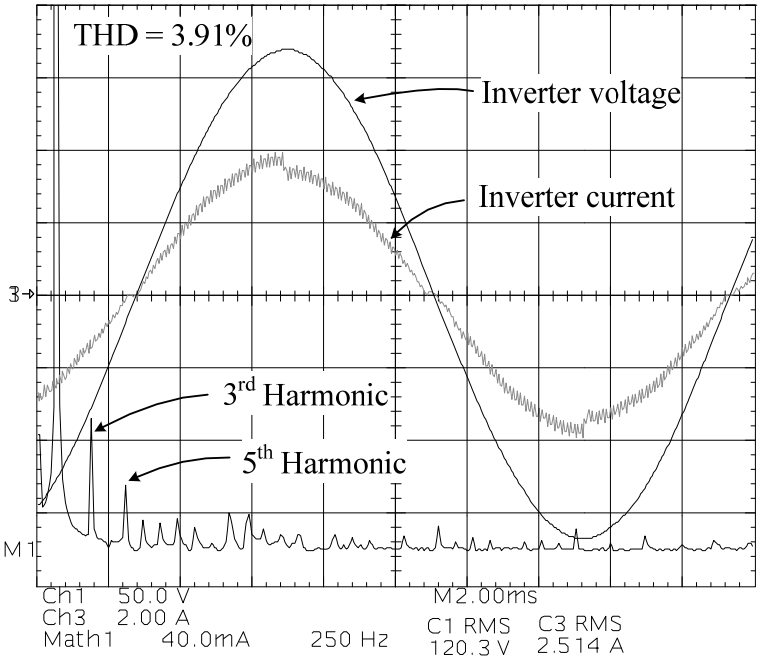


Figure 5-15 Experimental voltage and current waveforms for the proposed method with distortion factor K of 0.08.

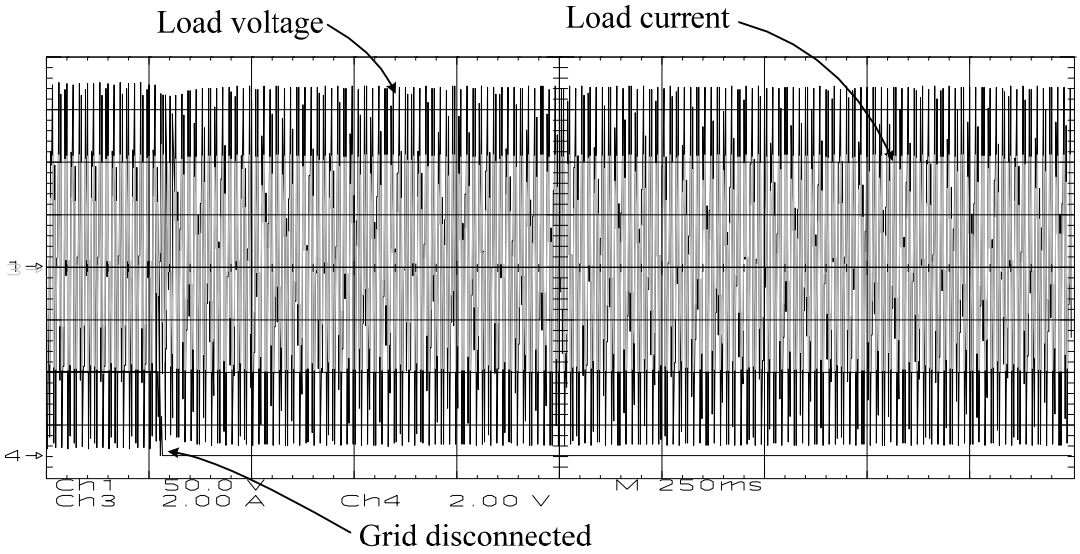


Figure 5-16 Islanding test result for the AFD method with C_f =0.046.

The same test is repeated with the proposed method and distortion factor set to K =0.105, which results in the same amount of harmonic distortion as the AFD method with C_f =0.046. The inverter detects islanding operation as the load frequency increases beyond the limit (60.5Hz) and discontinues energizing the load after 4 cycles, as can be seen from Figure 5-17. Note that it takes 3 cycles for the phase lock loop of the inverter to adjust the load frequency.

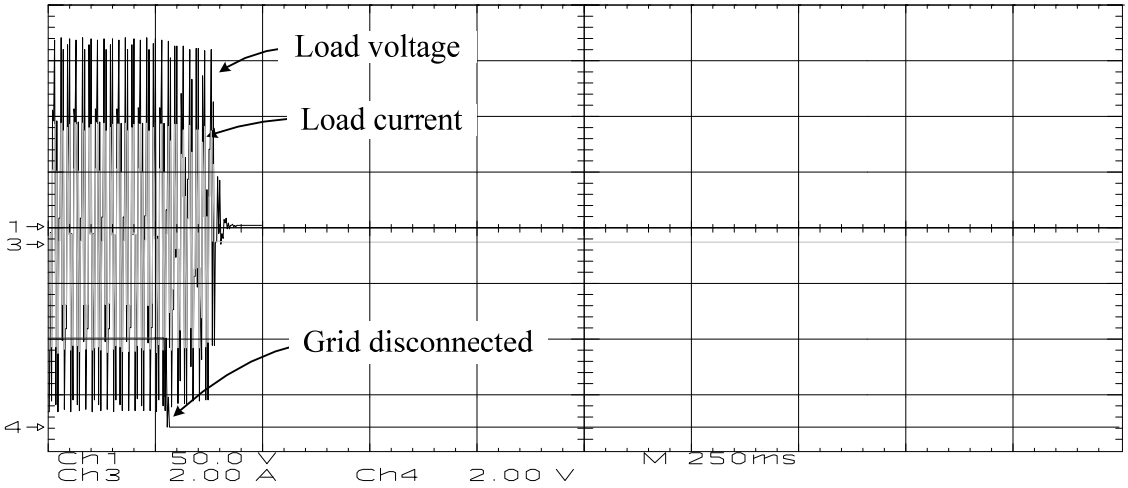


Figure 5-17 Islanding test result for the proposed method with distortion factor K =0.105.

The second Islanding test is carried out with the load quality factor Q_f set to 1.0 and C_{norm}=1.02, as required by the IEEE 1547.1 standard. Note that this operating point is outside the NDZ of both methods as can be seen from Figure 5-8. The AFD method chopping factor is set to C_f = 0:046 and the proposed method distortion factor is set to K=0.105. It is clear from Figure 5-18 and Figure 5-19 that the proposed method is faster in detecting the islanding due to the extra reactive power injected into the load during islanding. The detection time is reduced from 100ms to 33ms. Note that there is a three cycle delay after the frequency reaches the limit before the inverter stops, which is necessary to eliminate false tripping.

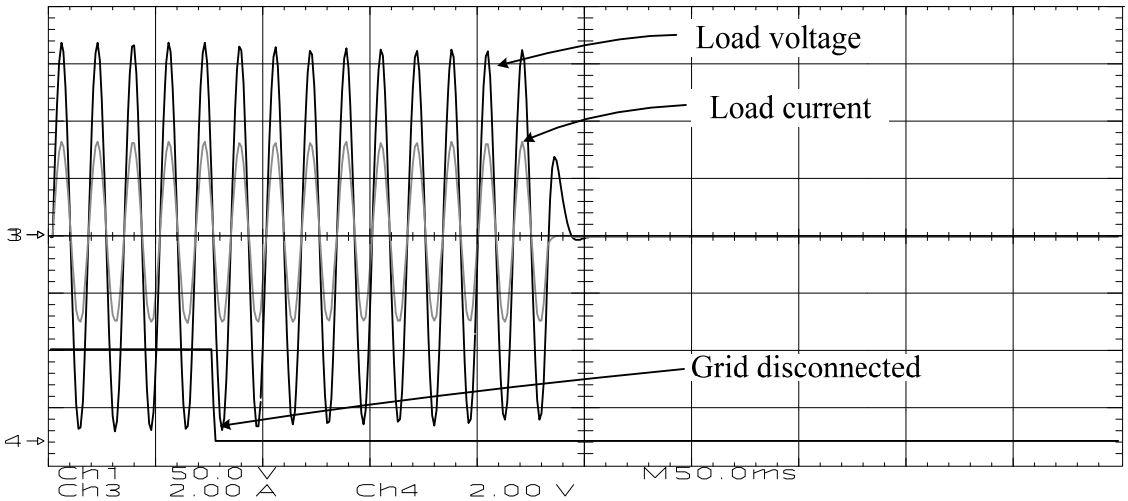


Figure 5-18 Islanding test result for the AFD method with chopping factor C_f= 0.046 and quality factor Q_f = 1.

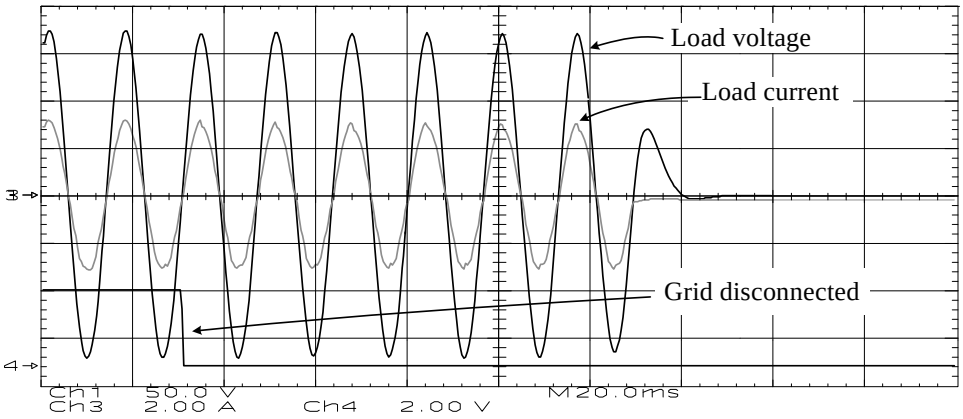


Figure 5-19 Islanding test result for the proposed method with a distortion factor K=0.105 and quality factor Q_f =1.

5.6 Conclusion

This chapter proposed an improved active anti-islanding detection method with a new AFD reference current waveform. The proposed method has a number of features over the conventional AFD method: 1) it can detect islanding with 30% less total harmonic detection, which improves the power quality of the grid, 2) it can generate more reactive power into the grid, which leads to faster anti-islanding detection, and 3) it has a better NDZ, since the islanding formation in the vicinity of balanced load is more unlikely. The rms value and the Fourier series coefficients of the current waveform of the proposed method are obtained and used to derive analytically the operational characteristics of the method. The performance of the proposed method is investigated by simulation and further verified by experiments through a laboratory prototype.

Chapter 6
Conclusion

The environmental and economic demand for renewable energies is resulting in the widespread adaptation of distributed power generation. The use of distributed generation (DG) has numerous advantages, such as generation of electricity at the point of load, reduction in the losses of transportation, and more reliable electrical systems. One of the most important DG systems is the grid-tied photovoltaic (PV) energy system.

In this dissertation, the main issues related to the research and development of an efficient and reliable grid-tied PV system is investigated. To minimize the power losses, a novel DC/DC converter with zero-voltage zero-current switching (ZVZCS) is proposed. To efficiently harvest the maximum power available from PV arrays, an enhanced maximum power point tracking (MPPT) algorithm is analyzed. To minimize the impact of islanding detection methods on the grid, a new anti-islanding algorithm is proposed.

6.1 Conclusions

The main contributions and conclusions of this research work are summarized as follows.

1) **Development of a novel efficient zero-voltage zero-current switching phase-shifted full-bridge DC/DC converter with active clamp.**

The operating principles of soft-switched full-bridge converters with passive RCD snubber and active clamp circuit were studied. The effect of the clamp MOSFET capacitance was investigated. A novel gating scheme for zero-voltage zero-current full-bridge converter with active clamp was proposed. The proposed method requires no extra components and is capable of resting the primary current during freewheeling, thus reducing the conduction losses. The power losses of the main components of each converter were evaluated by computer simulation. The proposed ZVZCS full-bridge converter operated with the new gating scheme has better efficiency than the conventional zero-voltage switching full-bridge converter throughout the load spectrum, and an efficiency of 94% is achieved under the full load conditions.

2) Development of an effective current sharing algorithm and MPPT control scheme for multiphase interleaved DC/DC converter.

A new current sharing scheme with MPPT control was proposed to control multiphase interleaved parallel connected DC/DC converters. Multiphase DC/DC converters have the advantage of reducing input and output ripples and better dynamic response. In the proposed cascade control scheme, one converter regulates the PV array voltage according to the MPPT algorithm and the remaining converters ensure equal current sharing among all the parallel converters. The performance of the controller was proven by simulation under changing temperature and irradiance conditions. A 5.4kW DC/DC PV energy prototyping system with three interleaved power converters controlled by a single DSP was designed and developed based on the proposed control algorithm. This unit was tested and delivered to Concordia University for use in the Demonstration Site of the NSERC Solar Building Research Network Program.

3) Evaluation and optimization of maximum power point tracking algorithms.

Three MPPT algorithms were evaluated and compared: the Perturb and Observe method (P&O), the Modified Perturb and Observe method (MP&O), and the Estimate Perturb-Perturb method (EPP). The P&O method is used in practice because of its simplicity, but it may fail to track the maximum power point under fast-changing environmental conditions. To enhance the performance of the P&O, the MP&O was developed. However, it reduces the speed of the maximum power tracking to half that of P&O. The EPP method is a compromise of the P&O and MP&O methods. A Matlab/Simulink model was developed to evaluate these methods. A DSP-controlled PV system, together with a solar array simulator, were used to evaluate the performance of the MPPT algorithms experimentally. The algorithms were tested against fast change in irradiance and temperature. The EPP algorithm is considered an optimized scheme since it achieves the same accuracy as the MP&O method with a speed comparable to the P&O method, and therefore is recommended for use in practical PV energy conversion systems.

4) Development of a novel anti-islanding method with lower current THD.

An improved active anti-islanding detection method that can detect islanding with less total harmonic distortion compared to the conventional active frequency drift (AFD) method was

proposed. The proposed method can detect islanding with 30% less total harmonic detection, which improves the power quality of the grid. The proposed method can generate more reactive power into the grid, which leads to faster anti-islanding detection, and better non-detection zone (NDZ). The operational characteristics of the proposed method, including the rms value and the Fourier series coefficients of the current waveform, were derived analytically. The performance of the proposed method is investigated by simulation and further verified by experiments through a laboratory prototype.

6.2 Future work

The following work is suggested for future research.

1) **Effect of the partial shading on the MPPT algorithm.**

Under partial shading conditions, the PV array's power characteristics experience multiple maxima, while conventional MPPT methods may be trapped on a local maxima, which is away from the absolute maximum power point. Developing an algorithm that can effectively detect the absolute maximum power point under partial shading conditions should be studied to increase the overall efficiency of a PV energy system.

2) **Performance of the new AFD method under nonlinear load conditions**.

The anti-islanding method proposed in this thesis was tested with an RLC load according to the recommendations of IEEE standards. However, different types of loads with non-linear characteristics may exist in practice, such as motor drives and uninterruptible power supplies. The performance of the proposed method under such conditions should be evaluated.

Appendix A

Design of the 1.8kW DC/DC Converter

The DC/DC converter is designed according to the specification of the PV array found at Concordia University. The solar arrays consist of 9 panels connected in a series. Each panel is 18 cells. The datasheet of a 36 cells panel of the same manufacturer is given in Appendix B. In order to raise the voltage, two strings will be connected in a series to form an array of 18 panels in series. At 0°C, the maximum cell voltage is 0.667V. Then the maximum panel voltage is 12V. Finally, each string is 108V and the array maximum voltage is 216≅ 220Vdc. The Isc is given as 8A ,Imp is given as 7.5, V_{mp} is given as 158V and V_{oc}=197 from the datasheet at 25°C:

A-1 Operating Condition of the Converter

Maximum input voltage (Vin_{max}): the maximum input voltage occurs at no load with cold temperature conditions. From the datasheets of the solar panels Voc can reach up to 12V at 0°C. Since 18 panels are connected in series Vin_{max} will be 216V and Vmp_{max}=0.8x216=172.

Minimum input voltage (Vin_{min}): the output voltage of the panel does not depend much on the irradiance level but depends on the temperature of the array. From the datasheet of the panels we can see that the Voc drops to 8.75V at 75°C. Assuming Vmp=0.8Voc, then at this temperature the maximum power point occurs at a panel voltage of Vmp =7V . The minimum array voltage is Vin_{min}=126V.

Maximum input current (Iin): From the data sheet, we can see that the maximum current the solar panel can achieve is 8.5A at 75°C.

Output voltage: Since the converter will supply a 3phase inverter, its out voltage must be sufficient to generate these voltages. At a modulation index ma=1 V_{LL}=0.612Vdc then Vdc=1.64VLL =1.64x208=341V. This is the minimum output voltage. Leaving sufficient margin for the voltage ripple and regulation, $Vout$ is set at 400V.

A-2 Topology Selection and Design of the Converter

Considering the power rating of the converter I_{mp}xV_{mp} = 8.5x172=1462W, A Full-Bridge converter shown in Figure A-1 is chosen since it has the best utilization of magnetic and semi-conductor components.

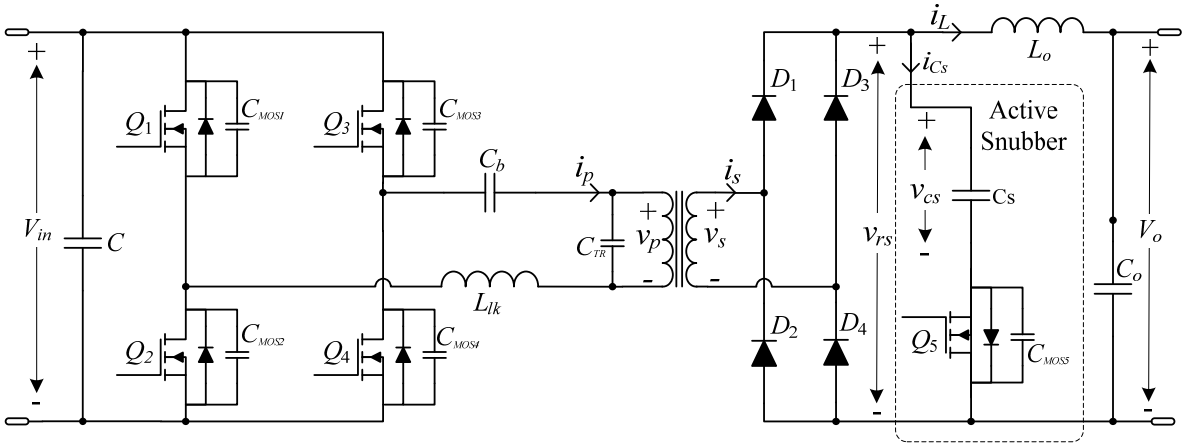


Figure A-1 Schematic diagram of DC/DC converter.

Frequency Selection: The frequency selection is a compromise between the switching losses and the volume of magnetic components. F_s is selected to be 200KHz; the transformer frequency is half the switching frequency; in Full-bridge then F_T=100KHz.

The maximum duty cycle can be between 0.8-0.9, considering both limits:

Maximum duty cycle is set at D_{max}=0.8.

Maximum duty cycle is set at $D1_{max}$=0.9.

Transformer ratio: n= $N_s/N_p = V_{out}/(Vin_{mim}xD_{max})=400/(126x0.8)=3.97\cong 4$

Transformer ratio: n= $N_s/N_p = V_{out}/(Vin_{mim}xD1_{max})=400/(126x0.9)=3.53$

Therefore a transformer turns ratio of 4 is chosen.

Choosing transformer core material: The core material is chosen according to the transformer frequency and the core losses per volume at a given flux density. Ferrite N97 from Epcos is chosen. It has 300Kw/m^3 at 100Khz and 200mT.

The transformer is chosen either by Area to power relation or by using tables prepared by the manufacturer. ETD49 core from Epcos was chosen with Ae=2.11cm^2 Aw=2.69cm^2. Or ETD59 core Epcos with Ae=3.68cm2 and Aw=3.66cm2

The Thermal resistance is very difficult to derive from the geometry of the core but a rule of thumb' related Re to the winding area Aw of a transformer:

Re=36/Aw =36/2.69=13.4 °C/Watt for ETD49 and for ETD59 Re=9.1 °C/Watt

Temperature rise is set as 40°C

Then the total power loss d in the transformer is obtained from Figure A-2 for material N97, at the specified flux density the losses are 40/13.4≅3Watt for ETD49 and for ETD59= 40/9.1=4.4Watt Dividing the losses between core losses and winding losses equally results in *Pcore*=1.5W for ETD49. If the temperature rise is kept the same then *Pcore* =2.2W for etd59 the power loss density is 43Kw/m^3 and this correspond to B=100mT.

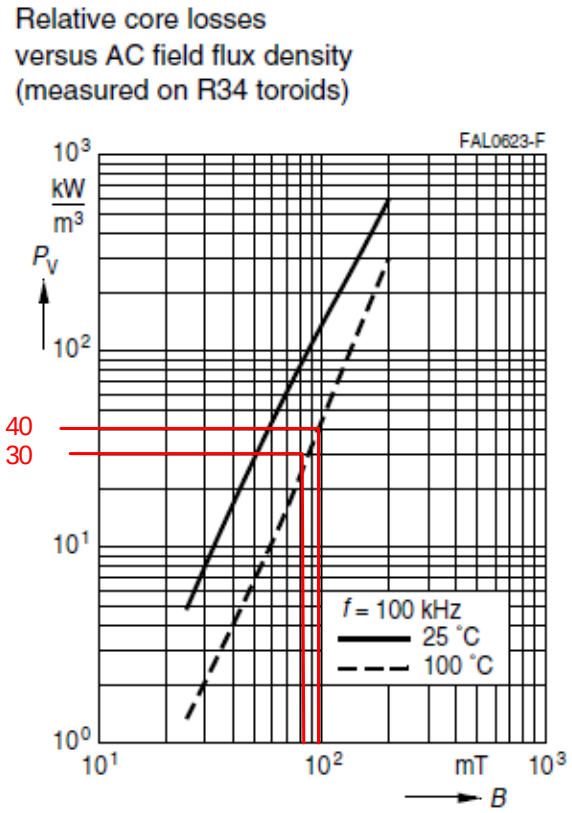


Figure A-2 Relative core losses Vs. Ac Flux density for the chosen material.

The volume of the core is *Ve*=2.41x$10^{-5}$$m^3$ for ETD 49 and *Ve*=5.12x$10^{-5}$$m^3$ for ETD59,

then the maximum power loss density is 60Kw/m^3 for ETD 49 and from the datasheet this corresponds to flux density *B*=150mT. For ETD59 power loss density is 30Kw/m^3 and this corresponds to B=80mT.

The primary turns ratio can be calculated from: $Np=(Vin_{min}\ xD_{max}x10^4\ )/(2xF_txA_exA\Delta B)$ which result in Np=8 turns for ETD59 ΔB=170mT then Ns=32 turns (n= 4) .

if Dmax =0.9 Np=9 for ETD59 ΔB=170mT then Ns=32 turns (n= 3.55) .

if Dmax =0.9 and N=8 then ΔB=190mT

Litz wire design: Available litz wire are : 5x3x44/42 or 52x36

Using 5x3x44/42 wire, the cross-section is considered to be equivalent to a wire of diameter 1.6mm (0.064"); then the area is 2mm^2. The current density is assumed as 4A/mm^2. The current capacity is 8A. Two strands are needed for the primary and one strand for the secondary.

Output filter: The output inductor is selected such that the converter works in continuous current mode at low load as shown in Figure A-3. The minimum load current can be set to 10% then during off time *Toff* the current should decrease to zero.

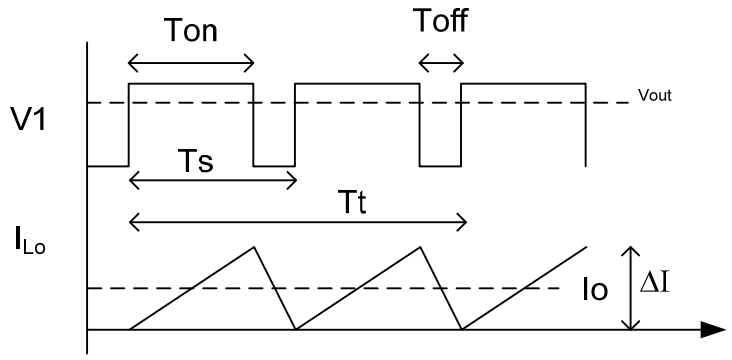


Figure A-3 Typical voltage and current waveforms of the output inductor.

$Vout=LxdI/dt$ then $L=(V1xdt)/dI$

$dI=\Delta I=2xIo_{min}=2x0.2xIo=0.4Io$

Minimum Io current is set as 20% of nominal current that is because the output current in this case is set as buy the irradiance, the 20% means the convertor will stay in CCM until 20% of full irradiance.

$dt=Toff=0.2xTs=1x10^{-6}$;$Ton=0.8Ts=4x10^{-6}$ or $Toff=0.1xTt$;$Ton=0.4Tt$

$L=(0.5xVoutxTs)/Io$ or $L=(0.25xVoutxTt)/Io$

$Io=Iin/(n\ x\ Dmax)=8.5/(0.8x4)=2.65A$

$L=(0.5x400x5x10^{-6})/2.65=377\ \mu H$

Output capacitor : The output capacitor is chosen to limit the voltage ripple due to the current ripple as shown in Figure A-4. The current through the capacitor is shown below:

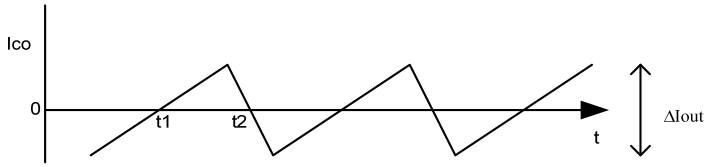


Figure A-4 Typical current waveforms of the output capacitor.

The ripple voltage (Vrc) due to current ripple is equal to:

$$V_{rc} = \frac{1}{C_o}\int_{t1}^{t2} I_{co}\,dt$$

$$V_{rc} = \frac{\Delta I_{out}}{8 f_s C_o}$$

Let total voltage ripple Vr=0.5%Vout =2V, and assume 25% of it is due to current ripple and the rest is due to the equivalent series resistor (ESR) of the capacitor.

Vrc=0.5V

Then Co=(0.4x2.65)/(8x200x10^3x0.5)=1.325μF Use Co=2μF

Blocking Capacitor Cb: is used to avoid flux unbalance in the transformer. Its value is calculated according to the acceptable voltage drop across it. Limiting this drop to 10% of the input voltage:

Cb= (Iin_{peak} xTon)/0.1Vinmin = 3.6 μF but as the capacitor must also withstand the maximum current at the switching frequency a 15μF 300V capacitor is chosen.

The voltage across the mosfet is the same as the input voltage and since zvs operation then no ringing appears at the mosfet. The maximum voltage Vinmax=216Vdc then a mosfet with Vds=300 will be enough. The input current is limited by the PV array but a higher mosfet current means a lower Ron but it may increase the output capacitance of the mosfet. Preliminary we set Imosfet to 1800W/Vinmin =1800/126=15A then the peak current can be 1.5x15=22A

Digikey has in this range: STW75NF30 with 37mohm 300V,60A,Coss=837pf Ciss=6nf 7.14$

Irfp260n with 40mohm, 200V, 50A, Coss=603pf Ciss= 4nf 8.13$

IXFH 40N30Q 80mohm, 300V, 40A, Coss=650pf Ciss=3nf 11.2$

STP30NM30N 90mohm, 300V,30A,Coss=500pf Ciss=2.5nf To220 7.6$

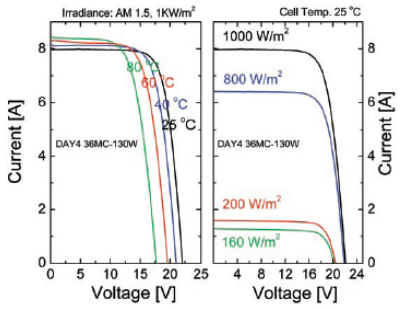
Choose STW75N30 from unitrode excel sheet the total mosfet loss is 37w and with leakage inductance 0.5μH , zvs will happen at 50%.

Output diode: since the max non-load input voltage is 220 then the diode will have a maximum voltage stress of 4x220= 880. We may use the HFA08tb120 which is 8A 1200v since we have an active snubber then the safety margin is enough. The output current is around 5A, then 8 A diode is chosen

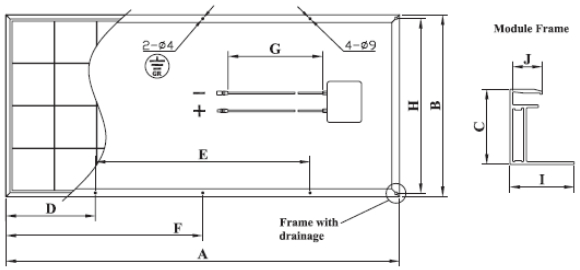
The active clamp switch is stw13nk100z which is 13A 1000v is o chosen for the application.

Appendix B

Day4 Energy Solar Panel Datasheet

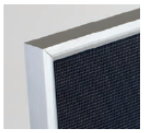


MODULE DIAGRAM



Qualification Test Parameters:

Temperature cycling range:	-40°C to +90°C (-40°F to 194°F)
Humidity freeze:	85% rH, -40°C to +85°C (-40°F to 185°F)
Static load front and back:	UL 2155 pa (45 psf)
Front loading (e.g. snow):	
Fire Class:	C
Corrosive atmosphere test:	pass
Protection Classification:	IP 65



Day4™ Anodized Aluminum Frame:
The unique design features: water drainage holes to reduce frame breakage due to freezing temperatures; multiple grounding holes for ease of installation; top frame surface has a beveled profile to reduce dirt and water trapping; deep glass frame slot increases strength and durability.

Mechanical Specifications:
GLASS: Solar glass (tempered)
JUNCTION BOX: Tyco Solarlok Interconnection,
output cables, male and female locking cable couplers
CELLS: 36 cells Multi Crystalline Silicon 156 mm square (6+ inches)
BACK SHEET: Multi-layer water resistant compound

Physical Specifications:

	METRIC	IMPERIAL	
A	1,465.5 mm	57.697 in.	
B	675.5 mm	26.594 in.	
C	35 mm	1.378 in.	
D	482.25 mm	18.986 in.	
E	501 mm	19.724 in.	
F	732.75 mm	28.848 in.	(Grounding holes on each side)
G	925 mm (±10mm)	36.417 in.	(± 0.393 in.)
H	631.5 mm	24.862 in.	
I	30 mm	1.181 in.	
J	13 mm	0.512 in.	
WEIGHT:	12.9 kg approx.	28.44 lbs approx.	

2-ø4 denotes 2 holes (grounding holes) with a diameter of 4 mm
Grounding Hole
4-ø9 denotes 4 holes (mounting holes) with a diameter of 9 mm
NOTE: All dimensions are accurate within +/-1.5 mm tolerance unless otherwise stated. Product dimensions in imperial inches (conversion of 1 mm equals 0.03937 inches, 1 kg equals 2.2 lbs) are provided for information purposes only.

Typical Electrical Performance at STC (1000 W/m², AM 1.5 Spectrum, cell temperature 25°C)

Peak Power (Wp)	Watts	115	120	125	130	135	140	145
Max. Power Voltage (Vmp)	Volts	16.80	16.95	17.21	17.55	17.78	17.98	18.24
Max. Power Current (Imp)	Amps	6.89	7.08	7.30	7.46	7.60	7.79	7.95
Open Circuit Voltage (Voc)	Volts	20.98	21.23	21.52	21.90	22.05	22.28	22.57
Short Circuit Current (Isc)	Amps	7.60	7.70	7.90	8.05	8.10	8.20	8.30
Short Circuit Temp. Coefficient	mA/K	7.80	7.80	7.80	7.80	7.80	7.80	7.80
Open Circuit Temp. Coefficient	V/K	-0.11	-0.11	-0.11	-0.11	-0.11	-0.11	-0.11
Max. Power Temp. Coefficient	%/K	-0.48	-0.48	-0.48	-0.48	-0.48	-0.48	-0.48

Module power tolerance:	+/- 3.5%
Module Maximum Fuse Series Amps:	15 A
Reduction of efficiency (from 1000W/m² to 200 W/m²):	< 4%
Normal Operating Cell Temperature (NOCT):	46ºC
Maximum System Voltage:	600V (US)

Performance Warranty:
5 years limited warranty on material and workmanship
10 years limited warranty on 90 % power output
25 years limited warranty on 80 % power output

Specifications and design are subject to change without notice. The features, functions and appearance of Day4 36MC may differ from details given due to continual product development.

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Document: Day4_PM_S_005 Revision 1.0 June 2007

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