

DEVELOPMENT OF AN ELECTROTHERMAL SIMULATION TOOL FOR INTEGRATED CIRCUITS

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by

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Abstract

Sara Sharifian Attar

Development of an Electrothermal Simulation Tool for Integrated Circuits

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The goal of this research was to develop a capability for the electrothermal modeling of electronic circuits. The objective of the thermal modeling process was to create a model that represents the thermal behavior of the physical system. The project focuses on electrothermal analysis at devices and chip level. A novel method to perform electrothermal analysis of integrated circuits based on the relaxation approach is proposed in this research. An interface program couples a circuit simulator and a thermal simulator. The developed simulator is capable of performing both steady state and transient analysis at devices and chip level.

The proposed method was applied to perform electrothermal analysis of Silicon Bipolar Junction Transistor (BJT) to predict the temperature distribution and the device performance in a circuit. Thermal nonlinearity due to temperature-dependent material parameters in the context of thermal modeling of the device and circuit has also been considered. The DC characteristics of the device were investigated. The obtained results indicate that the operating point of the device varies while the device reaches its junction temperature.

The accuracy of the electrothermal simulator has been evaluated for steady state analysis. The experimental results of a BJT amplifier were compared to the simulator results of the similar circuit. The electrothermal simulation results of BJT amplifier circuit indicate a good agreement with the available experimental results in terms of power dissipation, collector current and base-emitter voltage.

The performance of the electrothermal simulator has been evaluated for transient analysis. A current mirror circuit using Si NPN BJTs was simulated. According to the electrical simulator, the output current follows the reference current immediately. Nonetheless, the electrothermal simulator results depict that the load current has delay to reach a constant value which is not the same as the reference current, due to the influence of thermal coupling and self heating. The obtained results are in agreement with the available results in literature.

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In closing, I thank God. For only through God's grace and blessings has this pursuit been possible.

Dedication

*To my dear husband, Farhad, for his encouragement, support,
patience and model of perseverance,
without whom this would have never been possible.*

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Chapter 1

1. Introduction

Shrinking device sizes and higher integration densities are giving rise to numbers of new challenges in designing the next generation of integrated electronic circuits. Many roadmaps now recognize advanced electrothermal analysis as one of the major challenges in electronic product innovation. The reasons are due to ongoing push of technology towards higher speed and device density and/or higher power and increased complexity. The compounding effects of size reduction and increased power lead invariably to higher heat generation per unit area. Without accurate prediction of the temperature profile, it is impossible to determine properly the electrical characteristics of devices and therefore these devices may be at risk of overheating thus causing early device failure. When a device operates at high power dissipation, self heating and thermal coupling are the main issues in its performance and reliability [1]. Device temperature enhancement affects its electrical properties such as carrier mobility, electron saturation velocity, ionization rate, thermal conductivity, operating frequency, and power dissipation [2].

BJTs are commonly utilized in high power applications due to their high voltage/current characteristics. High power applications evidently cause increase in temperature. Temperature enhancement causes thermal runaway in bipolar transistors in contrary to field effect transistors. BJTs have positive temperature coefficient on collector current. Increase of temperature causes increase of current gain, which determines the value of the collector current. The more the current flows into the device, the higher its temperature rises. Increase of temperature results in increase of current gain and consequently an increase in current.

The positive loop continues until the device fails due to thermal runaway [3]. Therefore, it is critical to perform electrothermal analysis on BJTs.

Electrothermal simulation of VLSI circuits prior to the manufacturing enhances the estimation accuracy of the circuit performance at the operating temperature. With increasing concerns for on-chip power dissipation due to high packing density and high-frequency operation, electrothermal analysis has become critically important for accurate assessment of thermally activated device and circuit failures, and for timing analysis.

There are mainly two methods for electrothermal analysis: *Direct method and Relaxation method*. In direct or simultaneous iteration method [4] the thermal system is represented by an electrical model network, which has common nodes with the electrical only network, the so-called thermal nodes. In relaxation method an interface program couples two powerful electrical and thermal simulators. One simulator uses the updated results of the other simulator in the iterative process.

1.1 Thesis Objectives

The goal of this research was to develop a capability for the electrothermal modeling of electronic circuits. The objective of the thermal modeling process was to create a model that represents the thermal behavior of the physical system. This research project aimed to create simulation method to enable rapid assessment of thermal parameters affecting performance in electronic equipment. The project was focus on electrothermal analysis at devices and chip level.

Using relaxation method, an algorithm was developed in MATLAB [5] to create an interface between PSpice [6], as the electrical simulator, and COMSOL [7] as the thermal simulator. Applying this algorithm, an electrothermal simulator to analyze different electronic circuits and devices was obtained. The implementation of the electrothermal simulator requires: a) Communication between two simulators to receive and to send calculated parameters to another simulator. b) Time step to reach steady state values of parameters in that particular time step in a transient simulation. c) Convergence test. The developed algorithm in MATLAB controls these requirements. The developed simulator is capable of performing both steady state and transient analysis at devices and chip level.

The electrothermal simulator was employed to investigate the thermal effects in an active BJT, operational amplifier circuit and current mirror circuit. The results obtained from simulation were compared to the available experimental results to validate the accuracy of the electrothermal models. In addition, the performance of the electrothermal simulator has been evaluated through steady state and transient analysis of operational amplifier circuit and current mirror circuit.

1.2 Thesis Outline

In this research we have attempted to provide coverage of important subjects required for electrothermal analysis of device and circuits.

The first four chapters are designed to present the fundamental building blocks in an electrothermal simulation. Chapter 2 discusses an general introduction to heat transfer. The available methodologies to solve the heat transfer governing equations are elaborated in chapter 3. In chapter 4, SPICE electrical simulator is briefly introduced and BJT SPICE modeling and its temperature dependency is discussed. The deficiency of SPICE simulator in considering device temperature is also investigated. Chapter 5 focuses on the framework of an electrothermal simulator. The results of chapter 3 and 4 are combined to study several techniques of electrothermal analyses. Literature review on these techniques is also included in this chapter.

Chapter 6 concentrates on the proposed method and developed algorithm for electrothermal simulation. The developed algorithm is first presented. An incremental simulation strategy used in simulation efforts is illustrated in this chapter.

Chapter 7 addresses three important applications of the electrothermal analysis, based on the building blocks discussed in previous chapters. The impact of the thermal effect on the circuit performance is examined. Finally, the conclusions and suggested future works are summarized in chapter 8.

Chapter 2

To be able to perform thermal analysis on a circuit we need to know the basics of heat transfer. This chapter is an introduction to the fundamentals of heat transfer and thermal equations. Heat transfer mechanisms are examined and the governing heat transfer equation is introduced. The boundary conditions and initial condition that can be applied to a thermal model are explained for different environments.

2. Heat Transfer

In general, Heat Transfer or *Heat* is defined as “the energy in transit due to a temperature difference” [9].

There are two major mechanisms of heat transfer, *Conduction* and *Radiation*, which occur in solids and fluids. However if heat transfers from a solid surface to a moving fluid by conduction, it is known as *Convection* [10].

2.1 Heat Conduction

When heat is transferred within a material due to the molecular agitation, it is called *Conduction*. For instance, heat is transferred into a metal rod from one end to the other due to the temperature difference.

2.1.1 Fourier's Law

According to *Fourier's law*, the amount of heat being transferred by conduction in a one-dimensional plane per unit time can be expressed as equation (2.1), where k (W/mK) is the thermal conductivity and T is temperature in K [10].

$$q_x = -k \frac{dT}{dx} = -k \nabla T \quad (2.1)$$

The negative sign indicates that heat is transferred in the direction of decreasing temperature.

Figure 2.1 shows that plate surface temperatures are T_1 and T_2 ; assuming T_1 is greater than T_2 . In this example heat is transferred only by conduction in x direction. Temperature differences in y and z directions are assumed to be zero.

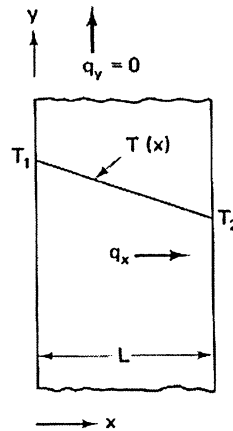


Figure 2.1: 1D conduction heat transfer in a plate with $T_1 > T_2$; $q_y = 0$ and $q_z = 0$ [10].

2.1.2 Thermal Conductivity

Thermal conductivity, k , is a thermo-physical property of materials. It represents the rate of conduction heat transfer per unit area for a temperature gradient of $1^\circ\text{C}/\text{m}$. It has SI units of $\text{W}/\text{m}^\circ\text{C}$ [10].

Most materials have a thermal conductivity that varies with temperature. Figure (2.2) shows thermal conductivity of different materials versus temperature variations.

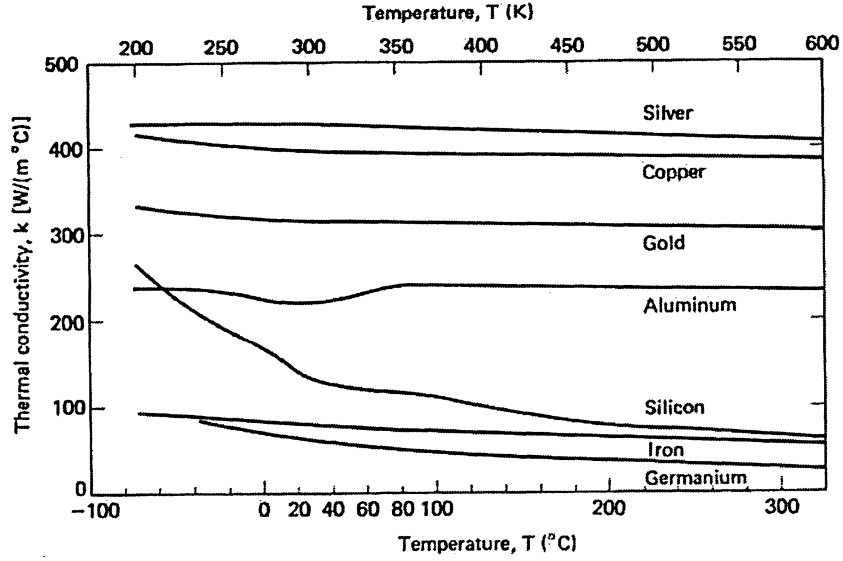


Figure 2.2: Thermal conductivity of different materials versus temperature [10].

A constant thermal conductivity can be assumed for a substance if its temperature variations are small.

In case of semiconductors, a nonlinear thermal conductivity variable with temperature is considered, equation (2.2).

$$k(T) = k(T_0) \left[\frac{T}{T_0} \right]^n \quad (2.2)$$

Where $n = -1.25$ for Silicon [11].

2.1.3 Heat Capacity

Heat Capacity, c , is the quantity that represents the amount of heat required to change one unit of mass of a substance by one degree. The SI units of heat capacity are J/kg°K [10].

$$Q = mc\Delta T \quad (2.3)$$

where Q is the heat energy received or given out by the substance, m is the mass of the substance, and ΔT is the change in temperature.

Heat capacity is often expressed in a constant volume, C_v , or a constant pressure, C_p .

A heat source can be either internal or external in a heat transfer system. Transistors, resistors and semiconductor chips are good examples of internal heat sources. Examples of external heat sources are different types of cooling systems such as fans and fins in power devices.

Considering heat is transferred only by conduction, heat sources are all internal and thermal conductivity is temperature dependent, by applying Fourier's law, time dependent heat transfer equation is defined as follows:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = Q \quad (2.4)$$

Where T (°K) is temperature, t (s) is time, ρ (kg/m³) is density, and C_p (J/kg°K) is specific heat capacity. Q (W/m³) is the heat source or heat sink density; depending on the heating or cooling behavior, it is positive or negative respectively.

2.2 Heat Radiation

Heat Radiation is an exchange of temperature between two surfaces with different temperature via electromagnetic waves [10]. Figure (2.3) illustrates electromagnetic spectrum for thermal radiation wavelength band.

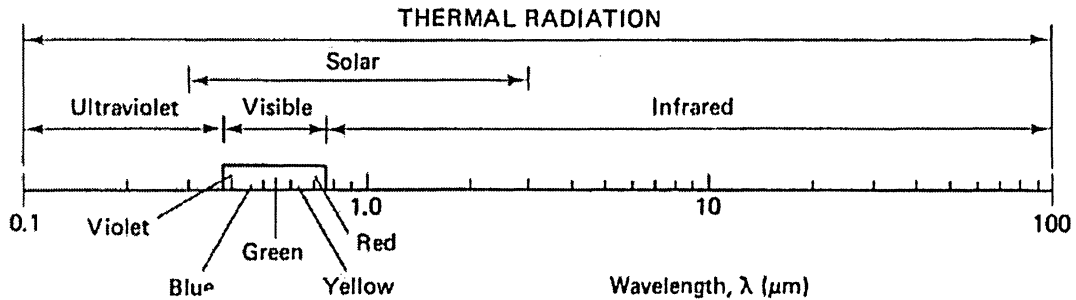


Figure 2.3: Electromagnetic spectrum for thermal radiation wavelength band [10].

The medium through which thermal radiation passes can be a vacuum or a transparent gas, liquid or solid. Objects within the path of heat radiation *absorb*, *reflect* and in case of transparent materials, *transmit* these electromagnetic waves. Absorptivity α , reflectivity ρ ,

and transmissivity τ , of a body represent how much a body absorb, reflect and transmit in the presence of thermal radiation. These parameters (α , ρ , and τ) depend on the material of the body and the temperature of the emitting source [10].

$$\alpha + \rho + \tau = 1 \quad (2.5)$$

2.2.1 Stefan-Boltzmann Law

According to Stefan-Boltzmann law, the total emissive power, E_b , for a blackbody is the total rate of thermal radiation emitted by a perfect radiator per unit surface area [10].

$$E_b = \sigma T_s^4 \quad (2.6)$$

A blackbody is an object that absorbs all the radiant energy reaching its surface, $\alpha = 1$. Where σ is Stefan-Boltzmann constant and T_s is the absolute surface temperature.

For non-blackbody surfaces the total emissive power is generally given in the following form:

$$E = \varepsilon E_b = \varepsilon \sigma T_s^4 \quad (2.7)$$

Where the emissivity (ε) can have a value between zero and one.

The total radiative heat flux that arrives at a body is called *irradiation*, G . The thermal irradiation received by a surface is distributed as follows (see Figure 2.4):

Thermal radiation flux absorbed = αG

Thermal radiation flux reflected = ρG

Thermal radiation flux transmitted = τG

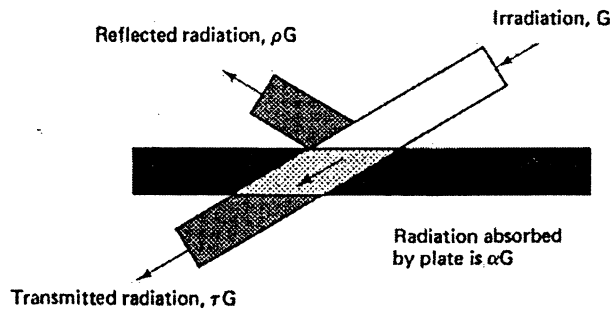


Figure 2.4: Absorption, reflection and transmission of thermal radiation incident on a surface [10].

Considering an opaque surface, the total radiative heat flux that leaves the body is called *radiosity*, J [9].

$$J = \rho G + \varepsilon \sigma T^4 \quad (2.8)$$

Therefore the net radiative heat flux into the body is obtained according to equation (2.9).

$$q = G - J \rightarrow q = (1 - \rho)G - \varepsilon \sigma T^4 \quad (2.9)$$

If the surface is diffusive-gray (gray body is a surface whose emissivity is independent of the electromagnetic wavelength) and opaque then the net radiative heat flux into a boundary is:

$$\rho = \varepsilon \rightarrow q = \varepsilon(G - \sigma T^4) \quad (2.10)$$

Consequently, heat transfer equation is defined as in equation (2.11), when heat is transferred by conduction and radiation.

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = \dot{Q} + \varepsilon(G - \sigma T^4) \quad (2.11)$$

2.3 Heat Convection

When a fluid flows over a solid, with different temperature than the solid, the process of heat transfer is called *Convection*. Heat convection is generally the conduction mechanism of heat transfer when the heat source is external; therefore, heat conduction has primary roll in heat convection.

2.3.1 Newton's Law of Viscosity

Newton's Law of Viscosity describes the velocity of a flowing liquid. Newton viewed laminar flow as the behavior of a liquid separating two solid parallel plates [9] as

$$\mu = \frac{Fy}{Au} \quad (2.12)$$

where μ is the viscosity (kg.ms), F is the shear force (kg.m/s²), y is the distance between the plates (m), A is the area of each plate (m²), and u is the fluid velocity, (m/s).

Therefore, the shear stress is defined as:

$$\tau = \frac{dF}{dA} = \mu \frac{\partial u}{\partial y} \quad (2.13)$$

2.3.2 Newton's Law of Cooling

Newton's law of cooling states that the rate of cooling of an object is proportional to the temperature difference between the object and its surroundings [9].

$$\frac{dT}{dt} = -k(T - T_a) \quad (2.14)$$

In equation (2.14), T_a is the ambient temperature, T is the temperature of the solid and k is a positive constant.

Applying Newton's law, the local convection heat flux of a fluid passing over a surface is expressed as:

$$q'' = h(T_s - T) \quad (2.15)$$

Where T_s is the surface temperature and h is the local convection coefficient.

Since the heat convection coefficient and local heat flux vary by the flow conditions, the total heat flux rate is defined as follows:

$$q = \int_{A_s} q'' dA_s \quad (2.16)$$

This leads to another way of expressing total heat flux, equation (2.17).

$$q = \bar{h}(T_s - T) \quad (2.17)$$

Where \bar{h} is the *mean coefficient of heat transfer*. It has SI units of (W/(m²°K)). It depends on flow regimes, fluids and thermodynamic conditions.

Therefore, heat transfer equation is defined as follow (considering heat is transferred by all types of the above mechanisms) [12]:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = Q + \varepsilon(G - \sigma T^4) + \bar{h}(T_s - T) \quad (2.18)$$

where $\rho C_p \frac{\partial T}{\partial t}$ represents the rate of energy increase in the solids, $-k \nabla T$ is the heat conduction term, and the right side of the equation represents the heat generation amount in the system.

For most electronic component, heat conduction is the most important heat transfer phenomenon; therefore most researchers consider a component that has thermal conduction as its only mode of internal heat transfer. Therefore equation (2.18) can be expressed as:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = Q \quad (2.19)$$

2.4 Boundary and Initial Conditions

A boundary condition is a mathematical concept relevant to the dependent variable, which in this case is temperature, T . Defining boundary conditions are necessary to solve any differential equation. Number of required boundary conditions for an ordinary differential equation is equal to the highest-order derivative of the equation.

If the heat transfer is unsteady, there must be an initial condition or initial spatial distribution known for temperature at $t = 0$.

The heat conduction equation given in (2.19) is subjected to the general boundary condition:

$$k \frac{\partial T}{\partial n} + hT = F \quad (2.20)$$

and the initial temperature condition:

$$T(t = 0) = G \quad (2.21)$$

F and G are the arbitrary functions, and n is the outward direction normal to the surface.

The following three types of thermal boundary conditions are the most common boundaries which can be applied to the electronics' object boundaries, depending on the packaging materials and the surrounding environment.

$$\text{Isothermal (Dirichlet): } T = F(x, y, z, t) \quad (2.22)$$

$$\text{Insulated (Neumann): } \frac{\partial T}{\partial n} = 0 \quad (2.23)$$

$$\text{Convective (Robin): } k \frac{\partial T}{\partial n} = h(T - T_{\text{ambient}}) \quad (2.24)$$

Where T_{ambient} is the ambient temperature.

To solve the boundary value problem of heat conduction, many existing analytical or numerical approaches are available. This will be addressed in the next chapter.

2.5 Summary

Heat transfer mechanisms (Conduction, Convection, and Radiation) and governing equations are introduced. For most electronic component, heat conduction is the most important heat transfer phenomenon; therefore most researchers consider a component that has thermal conduction as its only mode of internal heat transfer.

The thermal boundary conditions and the initial temperature condition are given. The three thermal boundary conditions are: Isothermal, Insulated and Convective.

Chapter 3

This chapter is an introduction to different types of analysis for the heat transfer equation obtained in chapter 2. Numerical and analytical approaches are briefly introduced in this part.

3. Thermal Analysis

In this research we performed the thermal analysis on integrated circuits without forced heat convection for the cooling system and heat was mainly transferred by conduction; hence, for the thermal analysis, the other two mechanisms of heat transfer are neglected. Consequently, the main focus is on the procedures that are developed to analyze conduction-heat-transfer systems.

There are different methods to solve heat conduction equations such as, Fourier series, Finite element method (FEM), Finite difference method (FDM), Boundary element method (BEM), Analytical approaches, Thermal network and Extraction approximation approaches. Figure (3.1) shows different approaches for thermal analysis.

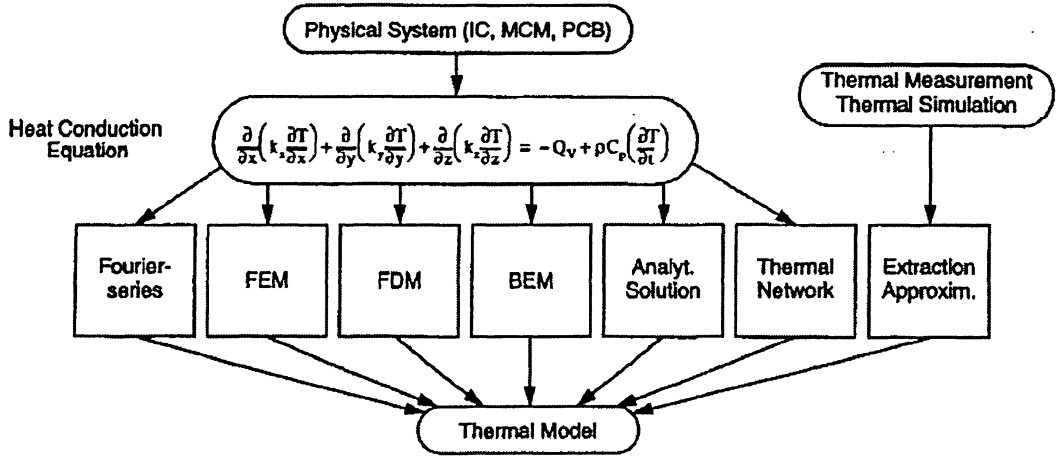


Figure 3.1: Thermal modeling approach [8].

3.1 Fourier Series

One of the primary methods to solve heat transfer equation is Fourier series. Considering Figure (3.2) as the thermal structure of an IC and its packaging, it has four layers of different types of materials with different thermal conductivities.

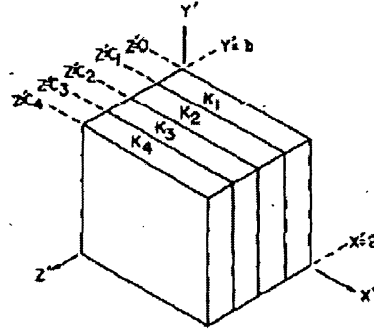


Figure 3.2: Thermal model of an IC and its packaging [13].

The only heat source is located at the $z = 0$ coordinate. It can be expanded for more than one heat source employing superposition. Considering the steady state heat transfer equation with uniform thermal conductivity (k):

$$\nabla^2 T = - \left(\frac{1}{k} \right) Q \quad (3.1)$$

The boundary conditions are defined according to boundaries of layers. Both temperature at field point r' and the source heat dissipation per unit volume parameters are expanded in a double Fourier cosine series to obtain:

$$Q(r') = \sum_{\alpha} \sum_{\beta} \varepsilon_{\alpha} \varepsilon_{\beta} \phi_{\alpha\beta}(z') \cos \alpha x' \cos \beta y' \quad (3.2)$$

$$T(r') = \sum_{\alpha} \sum_{\beta} \varepsilon_{\alpha} \varepsilon_{\beta} \psi_{\alpha\beta}(z') \cos \alpha x' \cos \beta y' \quad (3.3)$$

$$\text{where } \alpha = \frac{l\pi}{a}, \beta = \frac{m\pi}{b}, m, l = 0, 1, 2, 3, \dots \text{ and } \varepsilon_{\alpha} = \begin{cases} \frac{1}{2}, & \alpha = 0 \\ 1, & \alpha \neq 0 \end{cases}, \varepsilon_{\beta} = \begin{cases} \frac{1}{2}, & \beta = 0 \\ 1, & \beta \neq 0 \end{cases}$$

where a and b are the package dimensions at the x and y directions of a three dimensional coordinate system respectively. The Fourier coefficients $\phi_{\alpha\beta}$ are given by:

$$\phi_{\alpha\beta}(z') = \left(\frac{4}{ab} \right) \int_{x'=0}^a \int_{y'=0}^b Q(r') \cos \alpha x' \cos \beta y' dx' dy' \quad (3.4)$$

The surface source $Q(r')$ at $z = 0$ is:

$$Q(z') = q(x'y') \delta(z') \quad (3.5)$$

$q(x'y')$ is source heat dissipation per unit area and $\delta(z')$ is the Dirac delta function.

In all the above equations, the Fourier coefficients $\psi_{\alpha\beta}$ are unknown and are not simply computed. They are calculated by means of Green's function which has been elaborated in [13].

This method is computationally very complex when temperature variations with time and thermal conductivity variations with temperature are considered. It becomes more complex when additional layers and heat sources are added to the thermal structure.

3.2 Finite Element Method

Finite element method (FEM) was first developed for problems in stress analysis of solids and structural systems. However, its power and wide applicability can be fully recognized when it is applied on nonstructural problems: heat transfer and fluid flow [14].

FEM is a *discretization* method. It is a subdivision of a mathematical model into non-overlapping components of simple geometry. The response of each element is characterized by the finite number of degrees of freedoms (DOFs) [14].

Considering a system that has finite number of DOFs. DOFs are collected in a column vector u , also called state vector. For a set of DOFs there is a set of conjugate quantities called *forces* which are the factors of change. They are also collected in a column vector f . The relation between u and f is assumed linear and homogenous. If u vanishes so does f . Equation (3.6) shows the relation between f and u .

$$K \times u = f \quad (3.6)$$

K is called the *stiffness matrix*. The physical meaning of u and f varies according to the modeled application. In case of heat transfer modeling, u represents temperature and f represents heat flux.

In direct stiffness method elements are disconnected from their neighbors by disconnecting the nodes; then, each element is modeled by a generic element. Figure (3.3) illustrates some typical generic elements for 1D, 2D and 3D geometries.

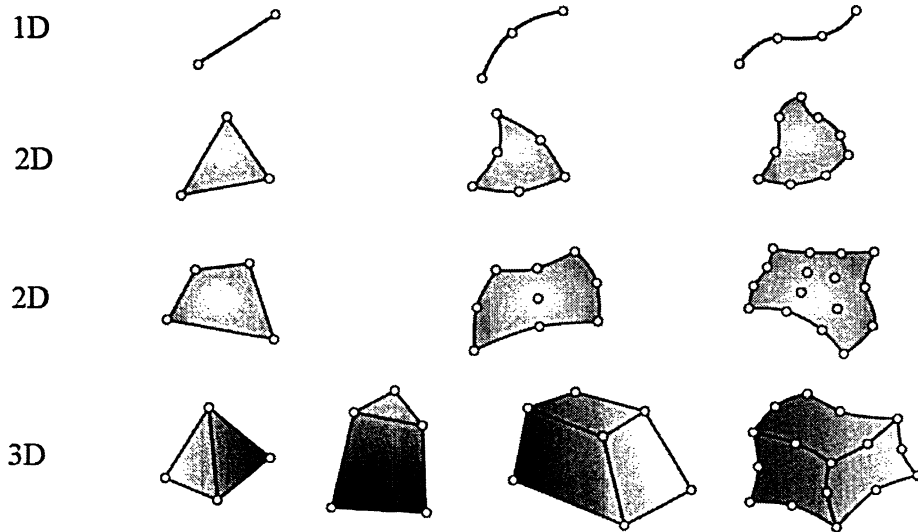


Figure 3.3: Some typical generic elements for 1D, 2D and 3D mesh geometries [15].

To analyze a discrete system the following steps are required [14]:

1. System Idealization, in which the actual system is idealized as an assemblage of elements.

2. Element Equilibrium, in which the equilibrium requirements of each element are recognized by state variables.

3. Element Assemblage, in which the element interconnection requirements are applied to recognize the set of simultaneous equations for the unknown state variables.

4. Solution of Response, in which the simultaneous equations are solved for the state variables and using the element requirements the response of each element can be calculated.

To develop a finite element solution scheme on heat transfer equation, we consider the heat conduction equation in electronic components (see section 2.3, equation (2.19)), given by

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = Q(T) \quad (3.7)$$

A discretization based on variation Galerkin procedures gives, after integration by parts of the $(-k \nabla T)$ term, the problem

$$\delta \Pi = \int_{\Omega} \delta T \rho C_p \frac{\partial T}{\partial t} d\Omega + \int_{\Omega} (\nabla \delta T) \cdot (-k \nabla T) d\Omega - \int_{\Omega} \delta T Q(T) d\Omega - \int_{\Gamma} \delta T \cdot (-k \nabla T)_n d\Gamma = 0 \quad (3.8)$$

Where δ denotes “variation in”.

This variation (weak) formulation is still valid even if the term $(-k \nabla T)$ and/or Q (indeed the boundary conditions) are dependent on T or its derivatives. Introducing the interpolations

$T = N\bar{T}$ and $\delta T = N\delta\bar{T}$, a discretized form of (3.8) is given as:

$$f(\bar{T}) - C(\dot{\bar{T}}) - P(\bar{T}) = 0 \quad (3.9)$$

Where

$$f = \int_{\Omega} N^T Q(T) d\Omega - \int_{\Gamma} N^T \cdot (-k \nabla T)_n d\Gamma$$

$$C = \int_{\Omega} N^T \rho C_p N d\Omega$$

$$P = \int_{\Omega} N^T \cdot (-k \nabla T) d\Omega$$

For steady state heat analysis the equation (3.9) can be written as: $P(\bar{T}) = f(\bar{T})$.

Equation (3.9) states the equilibrium of heat flow at all time. To discretize this equation, we consider the first step of Newton-Raphson iteration for the heat flow equilibrium in which:

$${}^{i+\Delta t}T^{(i)} = {}^{i+\Delta t}T^{(i-1)} + \Delta T^{(i)} \quad (3.10)$$

where i is the number of iteration.

Therefore, at time $t+\Delta t$ and for element m :

$${}^{t+\Delta t}T^{(m)} = H^m {}^{t+\Delta t}T \quad (3.11)$$

$${}^{t+\Delta t}T^{(m)} = B^m {}^{t+\Delta t}T \quad (3.12)$$

Hence, ${}^{t+\Delta t}T$ a vector of all nodal point temperatures at time $t + \Delta t$ is defined as:

$${}^{t+\Delta t}T^T = \left[{}^{t+\Delta t}T_1 \quad {}^{t+\Delta t}T_2 \quad \dots \quad {}^{t+\Delta t}T_n \right] \quad (3.13)$$

H^m is the element temperature matrix and B^m is the temperature gradient interpolation matrix [14].

3.3 Finite Difference Method

The basic concept of the finite difference approach is to approximate the partial derivative of a given point by a derivative taken over a finite interval across that point. Let $f(x)$ be a function which is finite, continuous and single valued. The derivative of $f(x)$ at point x_i can be approximated by the following difference equation:

$$\left. \frac{df(x)}{dx} \right|_{x_i} = \frac{f(x_i + \Delta x) - f(x_i - \Delta x)}{2\Delta x} \quad (3.14)$$

Where $(x_i + \Delta x)$ and $(x_i - \Delta x)$ are the two neighboring points. The central finite difference approximation of the second derivative of $f(x)$ can be written as:

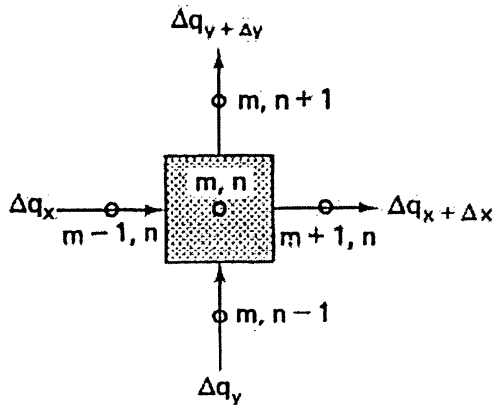
$$\left. \frac{d^2 f(x)}{dx^2} \right|_{x_i} = \frac{f(x_i + \Delta x) + f(x_i - \Delta x) - 2f(x_i)}{\Delta x^2} \quad (3.15)$$

The finite difference expression of (3.14) and (3.15) can be applied to equation (2.19) with respect to the time domain and the space domain. The object under simulation is first discretized into many space grid point x_i , and the algebraic difference equations are obtained for each x_i . The resulting set of equations that represent all grid points can be solved for the successive time points provided that temperature distribution at $t = 0$ is known.

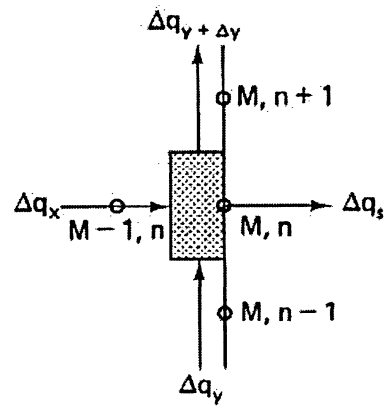
Here, we explained this method for 2D system. It can be expanded for 3D analysis.

For 2D analysis the dimensions of each subvolume is $\Delta x \Delta y \delta$ where δ is the thickness of the plate, as shown in Figure (3.4). To provide such a network the horizontal and vertical

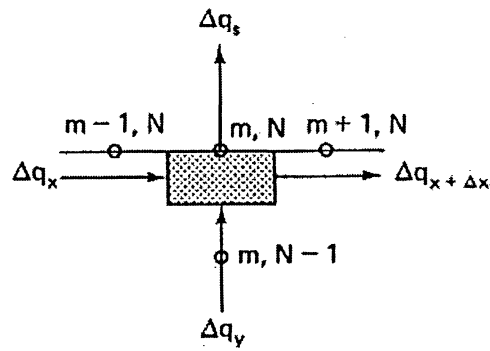
The resulting network is represented by nodes. The nodes are located at the intersections of construction lines. Each subvolume is treated as a lumped subsystem. The mass of each subvolume is considered to be located at the node and the temperature of the node represents the mean temperature of the subvolume. The distance between two adjacent nodes is Δx and Δy . The coordinates x, y of each node are equal to $(m-1).\Delta x$ and $(n-1).\Delta y$, respectively, where m is an integer value in the range of $[1, M]$ and n is an integer value in the range of $[1, N]$. M and N are the total number of nodes in x and y directions, correspondingly.



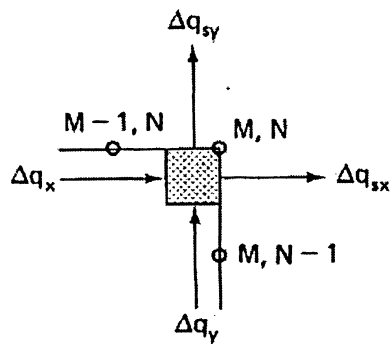
(a)



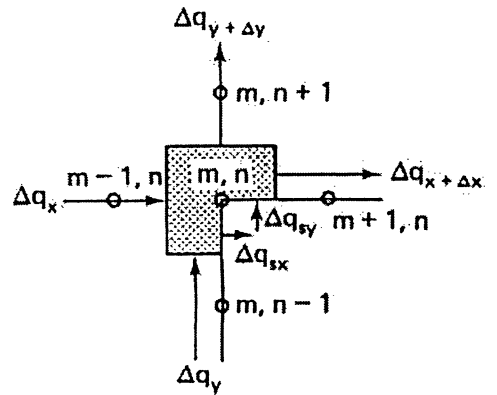
(b)



(c)



(d)



(e)

Figure 3.5: a) Interior node. b) Regular exterior node c) Regular exterior node. d) Outer corner node. e) Inner corner node [10].

To solve the heat conduction differential equation, first law of thermodynamics needs to be applied on each node. For instance, for Figure (3.5a) it is written as:

$$\Delta q_x + \Delta q_y + q' \Delta V = \Delta q_{x+\nabla x} + \Delta q_{y+\nabla y} + \frac{\Delta E_s}{\Delta t} \quad (3.16)$$

where q' is the internal energy of the subvolume. In case of steady conduction heat transfer, $\frac{\Delta E_s}{\Delta t} = 0$.

Applying simple difference approximations for the Fourier's law, the equation can be simplified into an algebraic equation:

$$\frac{(T_{m-l,n} + T_{m+l,n} - 2T_{m,n})}{\Delta x^2} + \frac{(T_{m,n-l} + T_{m,n+l} - 2T_{m,n})}{\Delta y^2} + \frac{q'}{k} = 0 \quad (3.17)$$

where $T_{m,n}$ is the temperature of the node located at x, y .

3.4 Boundary Element Method

Boundary element method is a numerical technique which solves boundary integral equations. This method is very similar to FEM. It is a *discretization* method, which enforces boundary elements along the material interfaces and obtains a set of boundary integral equations [16]. By dicritizing the boundaries into boundary elements a set of linear equations are obtained. Variables at any point of space may be attained by performing integration associated with the equivalent sources at the boundaries.

3.5 Analytical Solution

In analytical solution or differential formulation the heat conduction equation is solved directly. There are three steps to solve the equation.

Considering T_i as the initial temperature and q' as the internal energy generated per unit volume, according to the *first law of thermodynamics* we obtain:

$$dq_x + dq_y + dq_z + q' dV = dq_{x+dx} + dq_{y+dy} + dq_{z+dz} + \frac{\partial(\rho dV C_v T)}{\partial t} \quad (3.18)$$

First law of thermodynamics (conservation of energy) expresses that the change in internal energy of a system is equal to the heat added to the system minus the work done by the system [10].

Utilizing the definition of partial derivative the following replacement is applied:

$$dq_{x+dx} = dq_x + \frac{\partial(dq_x)}{\partial x} dx \quad (3.19)$$

Similarly, equations for dq_{y+dy}, dq_{z+dz} are obtained.

Therefore, equation (3.18) changes to:

$$q'dV = \frac{\partial(dq_x)}{\partial x} dx + \frac{\partial(dq_y)}{\partial y} dy + \frac{\partial(dq_z)}{\partial z} dz + \frac{\partial(\rho dV C_v T)}{\partial t} \quad (3.20)$$

Implementing Fourier's law of conduction and dividing through by differential volumes, it revised to:

$$\frac{\partial}{\partial x} \left(\frac{k \partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left(\frac{k \partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left(\frac{k \partial T}{\partial z} \right) + q'dV = \frac{\partial(\rho C_v T)}{\partial t} \quad (3.21)$$

Equation (3.21) can be further simplified if k, ρ, C_v are considered constant values.

3.6 Thermal Network

Since there are analogies between heat transfer and flow of electric current, FDM concept is put into the form of a RC network. Table 3.1 explains this analogy [10].

Table 3.1: Electrical Analogy.

Electrical	Thermal
E_e : Voltage (V)	T: Temperature (°C)
I_e : Current (A)	q: Rate of Heat Transfer (W)
R_e : Resistance (Ω)	R: Thermal Resistance (°C/W)
C_e : Capacitance (F)	C: Thermal Capacitance (J/ °C)

In addition, comparing Fourier equation to the differential equation for voltage distribution in an electrically conducting multidimensional system shows that an electrical

field set up within an electrical conductor corresponds to the thermal field in the modeled heat transfer problem.

Considering Figure (3.6), which is a subvolume of a 2D finite difference model with interior node, an energy balance on this node is developed as follows:

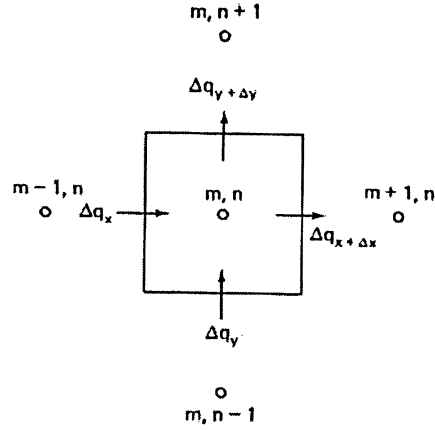


Figure 3.6: Interior finite-difference subvolume [10].

$$q'\Delta V + \Delta q_x + \Delta q_y - \Delta q_{x+\Delta x} - \Delta q_{y+\Delta y} = \frac{\Delta E_s}{\Delta t} \quad (3.22)$$

Applying Fourier's law of conduction we obtain:

$$\Delta q_x = -k\delta\Delta y \frac{T_{m,n}^r - T_{m-1,n}^r}{\Delta x} = \frac{T_{m-1,n}^r - T_{m,n}^r}{l/(\delta k)} \quad (3.23)$$

$$\Delta q_{x+\Delta x} = \frac{T_{m,n}^r - T_{m+1,n}^r}{l/(\delta k)} \quad (3.24)$$

$$\Delta q_y = \frac{T_{m,n-1}^r - T_{m,n}^r}{l/(\delta k)} \quad (3.25)$$

$$\Delta q_{y+\Delta y} = \frac{T_{m,n}^r - T_{m,n+1}^r}{l/(\delta k)} \quad (3.26)$$

Considering $R = l/(\delta k)$ and $C = \rho C_v \nabla V$ equation (3.22) is revised to:

$$q'\Delta V + \sum \frac{T_i^r - T_{m,n}^r}{R_i} = C_i \frac{T_{m,n}^{r+1} - T_{m,n}^r}{\Delta t} \quad (3.27)$$

The above equation shows that the summation of the currents flowing into the node (m, n) from the surroundings is equal to the flow of current into the capacitor. In a steady state

situation no current flows into the capacitor and the summation of the currents is zero, since $T_{m,n}^{\tau+1} = T_{m,n}^{\tau}$.

Note that equation (3.27) must assure stability requirements that restrict Δt . In case of severe restrictions, equation (3.27) can be written as:

$$q' \Delta V + \sum \frac{T_i^{\tau} - T_{m,n}^{\tau}}{R_i} = C_i \frac{T_{m,n}^{\tau} - T_{m,n}^{\tau-1}}{\Delta t} \quad (3.28)$$

Figure (3.7), illustrates the equivalent thermal network of Figure (3.6).

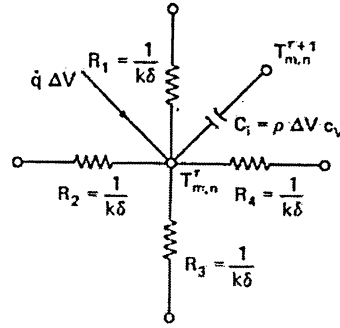


Figure 3.7: Equivalent thermal network for interior subvolume [10].

Applying similar calculations, RC network can be developed for subvolumes with exterior nodes, which is shown in Figure (3.8b).

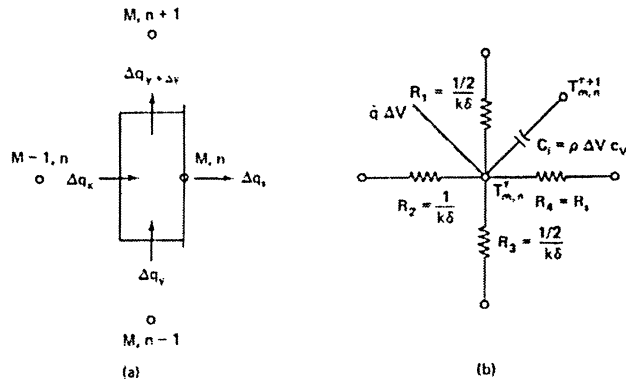


Figure 3.8: a) Exterior finite-difference subvolume. b) Equivalent thermal network for exterior subvolume [10].

3.7 Summary

So far different thermal analysis methods have been reviewed. In general, the numerical method is more powerful and can be more easily applied to various kinds of heat conduction problems (e.g. linear, non-linear, homogeneous, non-homogeneous). The analytical method, on the other hand, is more restrictive in solving complex problems. For instance, if the thermal conductivity (k) is temperature dependent, some variable transformation technique may need to be used to simplify the original problem.

Finite element method (FEM) is chosen in this research as the numerical thermal simulation method. This is one of the most popular numerical methods used by design engineers in today's product design process in industry. The great advantage of FEM programs is their generality since they can simulate structures with arbitrarily complex geometries. In case of thermal analysis on VLSI circuits, FEM simulators are more accurate especially when the packaging of the IC is also considered. FEM is computationally less complex compare to methods such as Fourier series, FDM and thermal network.

Chapter 4

In this chapter SPICE electrical simulator is briefly explained. SPICE is the implemented electrical simulator in our research work to perform electrical analysis. SPICE model of a bipolar junction transistor is also expanded, since our major focus is on BJT circuits.

To illustrate the temperature dependency of BJT parameters, their variations with temperature, which are obtained by experiments, are presented. The deficiency of SPICE simulators to consider temperature in simulations is also discussed.

The importance of power dissipation of VLSI circuits is also presented and the effects of power dissipation on circuit performance and junction temperature are briefly investigated.

4. Electrical Analysis

To perform an electrical analysis on an integrated circuit an electrical circuit simulator is needed. Every circuit simulator has a library which includes model definitions for each element type. In these models a set of equations are defined to specify the characteristics of the element.

One of the primary circuit simulators is called SPICE (Simulation Program with Integrated Circuits Emphasis) which was originally developed at the electronic research laboratory of the University of California, Berkeley in 1975. There are different versions of SPICE such as PSpice which is a PC version of SPICE and HSpice which runs on UNIX workstations and large computers. HSpice is the fast version of SPICE and is normally used. In this research we used PSpice as the electrical simulator [6].

4.1 BJT SPICE Model

Bipolar Junction Transistor was the first solid state amplifier, which revolutionized the solid state electronics. BJT has many advantages over other types of transistors in terms of speed, current drive, transconductance and noise figure. These advantages make BJT suitable in applications for ultra high speed discrete logic circuits such as emitter coupled logic (ECL), power switching applications and in microwave power amplifiers. They are also used in electrical circuits where current needs to be controlled. Some of the areas are: switching elements to control DC power to a load, amplifiers for analog signals, and 3-phase AC motors [17].

All the above applications of a BJT are directly dependent on its operating point and therefore its power dissipation. Since BJT is very sensitive to temperature variations, any changes in the device junction temperature or the temperature of the surrounding environment can cause changes in the device operating point and power dissipation. Temperature variations may also cause device failure; hence, failure of the entire circuit.

There are two main models for a BJT: Eber-Molls model and Gummel-Poon model. In today's SPICE simulators the latter is employed, since it considers the second order effect, therefore, it is more accurate in high and low current levels [18]. Figure (4.1) shows PSpice model of a BJT.

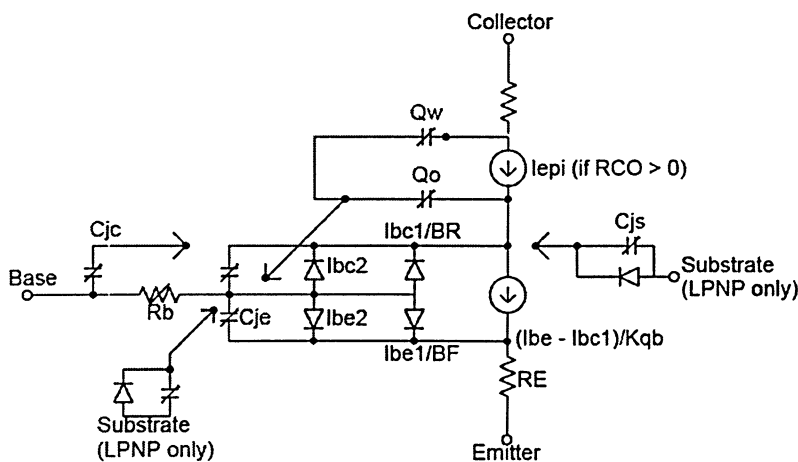


Figure 4.1: BJT SPICE model [19].

For DC current, the bipolar equation system is defined as follows:

$$I_b = \frac{I_{be1}}{\beta_F} + I_{be2} + \frac{I_{bc1}}{\beta_R} + I_{bc2} \quad (4.1)$$

$$I_c = \frac{I_{be1}}{K_{qb}} - \frac{I_{bc1}}{K_{qb}} - \frac{I_{bc1}}{\beta_R} - I_{bc2} \quad (4.2)$$

$$I_{be1} = I_S \cdot (e^{V_{be}/(N_F \cdot V_t)} - 1) \quad (4.3)$$

$$I_{be2} = I_{SE} \cdot (e^{V_{be}/(N_E \cdot V_t)} - 1) \quad (4.4)$$

$$I_{bc1} = I_S \cdot (e^{V_{bc}/(N_C \cdot V_t)} - 1) \quad (4.5)$$

$$I_{bc2} = I_{SC} \cdot (e^{V_{bc}/(N_C \cdot V_t)} - 1) \quad (4.6)$$

$$K_{qb} = K_{q1} \cdot (1 + (1 + 4K_{q2})^{N_K}) / 2 \quad (4.7)$$

$$K_{q1} = \frac{1}{1 - V_{bc} / V_{AF} - V_{be} / V_{AR}} \quad (4.8)$$

$$K_{q2} = \frac{I_{be1}}{I_{KF}} - \frac{I_{bc1}}{I_{KR}} \quad (4.9)$$

$$V_t = \frac{K \cdot T}{q} \quad (4.10)$$

All the parameters are defined in Table 4.2.

Similar to other transistors, BJTs are utilized for applications such as current sources, amplifiers and switches. Reliable BJT current sources, amplifiers and switches need to have stable collector current, stable forward current gain and stable base-emitter voltage, respectively. Nonetheless, all these parameters are temperature variables and strongly depend on device temperature. Table (4.1) indicates an example of these variations [20].

Table 4.1: Some BJT parameters variations with temperature.

T (°C)	-65	25	175
I _{SC} (nA)	1.9e-3	1.0	33000
β _F	25	55	100
V _{BE} (V)	0.78	0.60	0.225

The following represents temperature dependent equations for some parameters that significantly affect the behavior of a BJT in DC applications.

$$I_S(T) = I_S \cdot e^{(T/T_{nom}-1) \cdot (E_g/N \cdot V_t)} \cdot \left(\frac{T}{T_{nom}}\right)^{XTI/N} \quad (4.11)$$

$$I_{SE}(T) = (I_{SE} / \left(\frac{T}{T_{nom}}\right)^{XTB}) \cdot e^{(T/T_{nom}-1) \cdot (E_g/N_E \cdot V_t)} \cdot \left(\frac{T}{T_{nom}}\right)^{XTI/N_E} \quad (4.12)$$

$$I_{SC}(T) = (I_{SC} / \left(\frac{T}{T_{nom}}\right)^{XTB}) \cdot e^{(T/T_{nom}-1) \cdot (E_g/N_C \cdot V_t)} \cdot \left(\frac{T}{T_{nom}}\right)^{XTI/N_C} \quad (4.13)$$

$$I_{SS}(T) = (I_{SS} / \left(\frac{T}{T_{nom}}\right)^{XTB}) \cdot e^{(T/T_{nom}-1) \cdot (E_g/N_S \cdot V_t)} \cdot \left(\frac{T}{T_{nom}}\right)^{XTI/N_S} \quad (4.14)$$

$$\beta_F(T) = \beta_F \cdot \left(\frac{T}{T_{nom}}\right)^{XTB} \quad (4.15)$$

$$\beta_R(T) = \beta_R \cdot \left(\frac{T}{T_{nom}}\right)^{XTB} \quad (4.16)$$

Table 4.2: Parameters definitions.

β_F	Ideal Maximum Forward Beta
β_R	Ideal Maximum Reverse Beta
E_g	Energy Bandgap
I_{KF}	Corner for Forward-Beta High-Current Roll-Off
I_{KR}	Corner for Reverse-Beta High-Current Roll-Off
I_b	Base Current
I_c	Collector Current
I_{be1}	Forward Diffusion Current
I_{be2}	Non-ideal Base-Emitter Current
I_{bc1}	Reverse Diffusion Current
I_{bc2}	Non-ideal Base-Collector Current
I_S	Transport Saturation Current
I_{SC}	Base-Collector Leakage Saturation Current
I_{SE}	Base-Emitter Leakage Saturation Current
I_{SS}	Substrate p-n Saturation Current

k	Boltzman's Constant
q	Electron Charge
K_{qb}	Base Charge Factor
N_F	Forward Current Emission Coefficient
N_E	Base-Emitter Leakage Current Coefficient
N_C	Base-Collector Leakage Current Coefficient
N_R	Reverse Current Emission Coefficient
N_K	High-Current Roll-Off Coefficient
N_S	Substrate p-n Emission Coefficient
V_{be}	Built-in Base-Emitter Voltage
V_{bc}	Built-in Base-Collector Voltage
V_{AF}	Forward Early Voltage
V_{AR}	Reverse Early Voltage
T_{nom}	Reference Temperature
X_{TI}	Temperature Effect Exponent
X_{TB}	Forward and Reverse Beta Temperature Coefficient

The equations show that temperature variations can significantly affect the operation of a bipolar transistor, especially the scaling of transistor geometries that increase current density and thermal spreading impedances [21].

4.2 Temperature Effects on BJT Parameters

In this part we will review some experimental results regarding BJT parameter variations with temperature.

Fundamentals of a BJT operation are based on carrier mobility which is a temperature dependent factor. Figure (4.2) and Figure (4.3) indicate temperature reliance of electron and hole mobility for different doping concentration obtained by experiments [22].

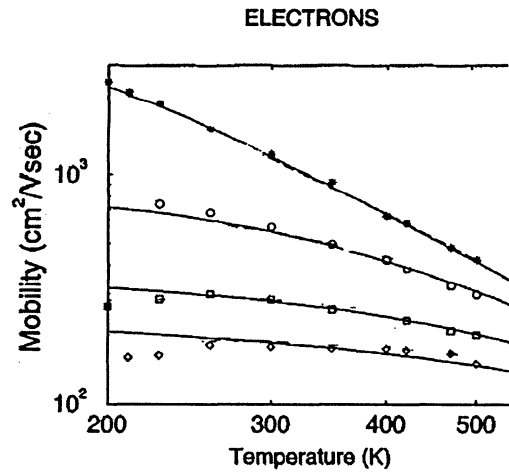


Figure 4.2: Electron mobility variations vs. temperature [22].

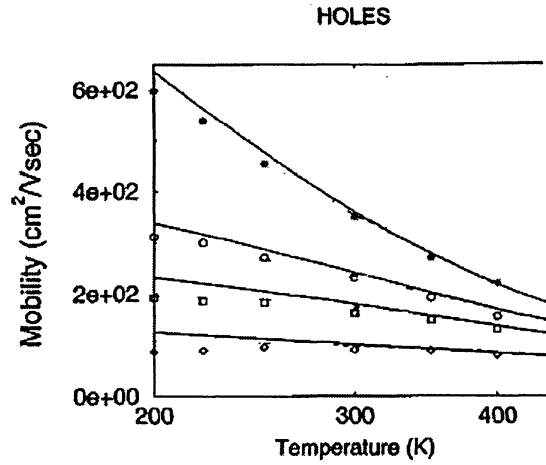


Figure 4.3: Hole mobility variations vs. temperature [22].

These curves show that electron and hole mobility decreases with increase in temperature. In case of an NPN BJT, it results in reduction of base and collector transient time.

Variations of Base transient time, τ_{BT} , Collector transient time and charging time, τ_{CT} and τ_C , and Emitter charging time, τ_E , are obtained according to Figure (4.4) for an NPN BJT [23].

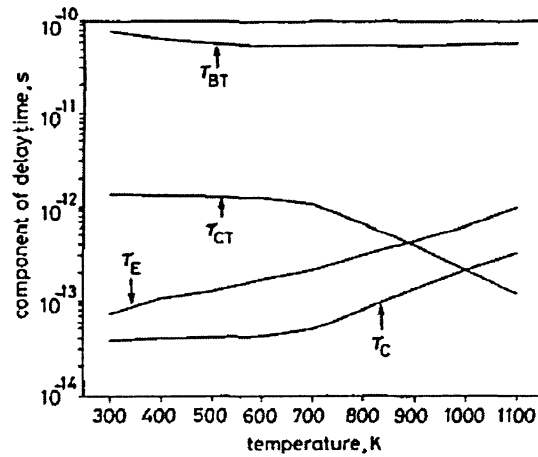


Figure 4.4: Collector, Emitter and Base transient and charging time variations with temperature [23].

Decrease in the base and collector transient time while increase in emitter and collector charging time reduces the device switching speed and cut-off frequency.

Figure (4.5) indicates the variations of cut-off frequency, f_T , versus temperature attained by observation [23]. Reduction of f_T influences the current gain and device efficiency.

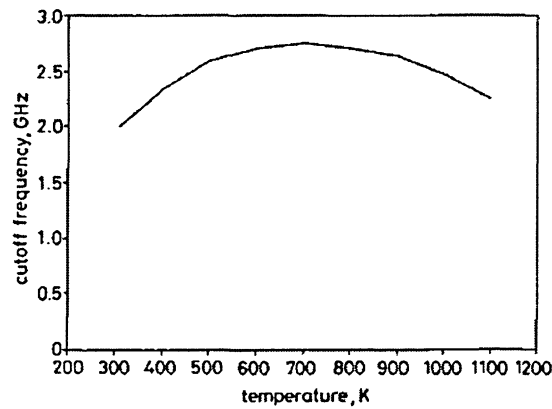


Figure 4.5: BJT cut-off frequency variations with temperature [23].

Figure (4.6) shows variations of collector saturation current versus temperature, when the device works at high temperatures. It shows that as temperature increases the saturation current increases accordingly. Variations in I_{co} cause variations of the device collector current. This is very critical mainly if the device is operating as a current source, as it needs a constant collector current [24].

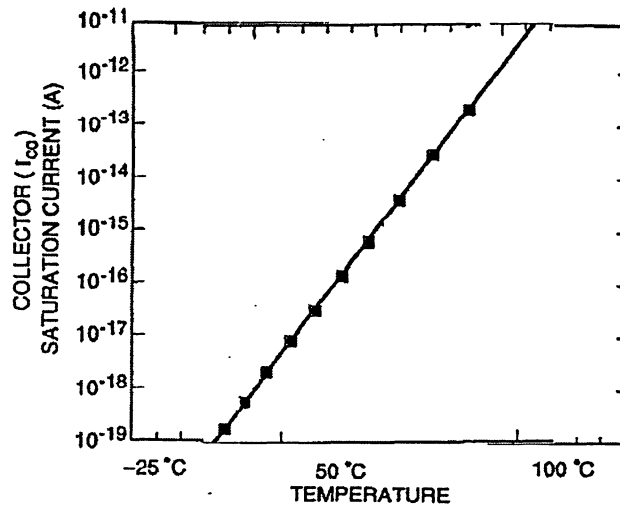


Figure 4.6: Collector saturation current variations with temperature [24].

Figure (4.7) illustrates the Base-Emitter voltage, V_{BE} , variations with temperature. It shows that V_{BE} decreases with temperature increase. V_{BE} is a very important parameter in a BJT performance. It indicates the region of the device operation. For instance, variations in V_{BE} may change BJT operating as a current source into a resistor [23].

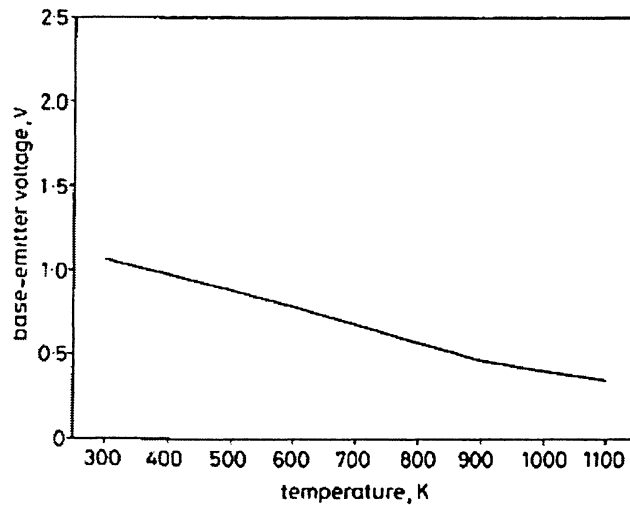


Figure 4.7: Base-Emitter voltage variations versus temperature [23].

Figure (4.8) shows variations of BJT current gain versus temperature. Since BJTs are recognized by their high current gain, it is very critical to be able to determine the current gain accurately [23].

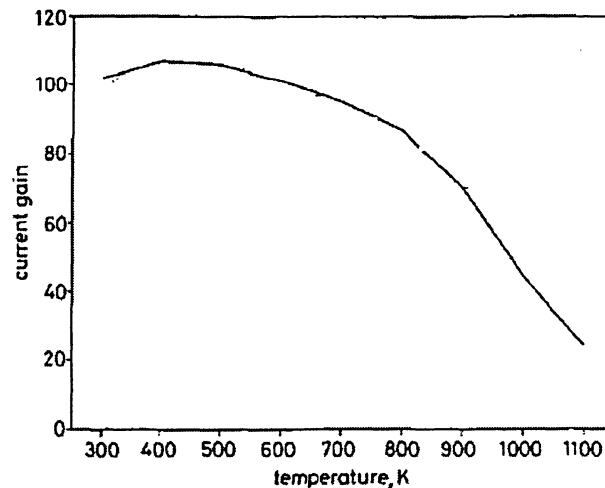


Figure 4.8: Current gain variations with temperature [23].

The above graphs confirm that device temperature variations result in changes of the device operating point. Figure (4.9) shows the DC characteristics of an NPN Si BJT for different V_{BE} as operating time increases. It shows that at a constant V_{BE} and V_{CE} , I_c increases by time since device junction temperature increases. This data obtained by experiment for a common emitter circuit [25]. The value of I_c converges to a constant value when device reaches its steady state junction temperature.

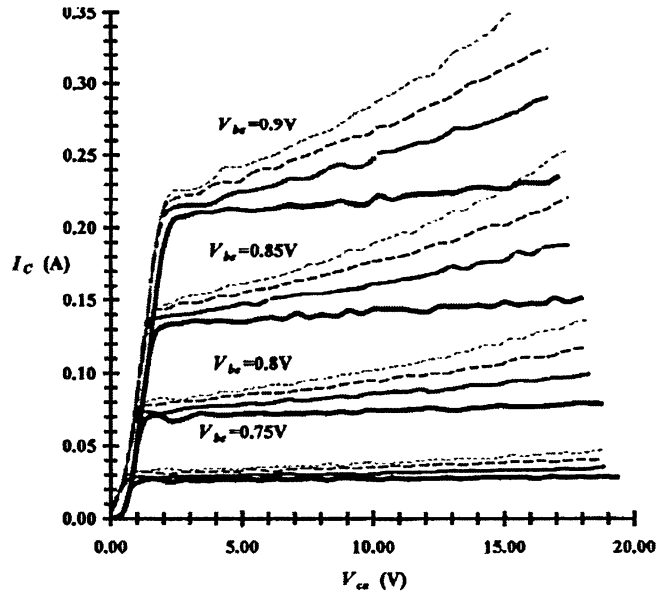


Figure 4.9: I-V characteristics of common emitter Si BJT . Data was taken at $4\mu\text{s}$ (solid line), $40\mu\text{s}$ (semi-dashed line), $100\mu\text{s}$ (dashed line) and $200\mu\text{s}$ (dotted line) [25].

Figure (4.10) shows power dissipation and efficiency of a Si BJT. It shows that the power dissipation increases by increase of device temperature; therefore, the efficiency decreases [26]. This defect is more significant in high power applications which produce high temperature.

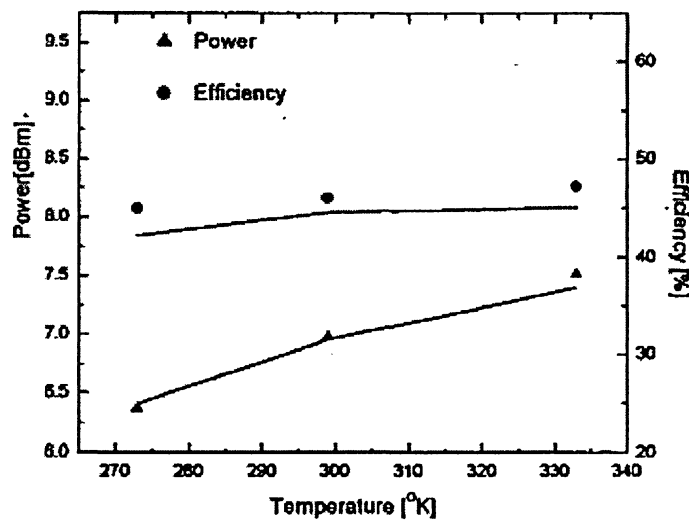


Figure 4.10: BJT power and efficiency variations with temperature [26].

4.3 Power Dissipation and Temperature Effects on Integrated Circuits

In 1965 Gordon Moore observed that the total number of devices on a chip doubled every 1.5 year. Today's low cost, high speed electronic devices consisted of multimillion gate ICs prove the validation of Moore's Law [27].

Technology shrinkage culminates in some difficulties; one of them is IC power consumption. Even though many efforts have been performed to reduce IC power supply voltages, the number of devices per chip and their operating frequencies enhance faster than their reduction of power consumption. Figure (4.11) shows power dissipation drifts with technology [27]. It indicates that by decreasing device size its power density increases in contrary. In Figure (4.11), LKg Pwr denotes device Leakage power; it is proportional to the current leakage of the device through its substrate. Active Pwr denotes device Active power. It is the device power dissipation when it is working in its active region.

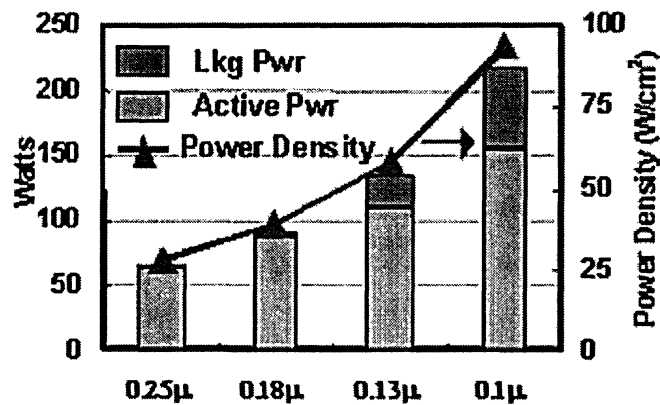


Figure 4.11: Power density trends [27].

ITRS (International Technology Roadmap for Semiconductors) assigned a maximum allowable power for three of the primary types of electronic products; they are shown in Table (4.3). It shows improvements on the power limitations of ICs over 5 years.

Table 4.3: Improvement trends for ICs enabled by feature scaling [27].

Allowable Max Power (W)	2002	2003	2004	2005	2006	2007
High-Performance	140	150	160	170	180	190
Cost-Performance	75	81	85	92	98	104
Hand-Held	2.6	2.8	3.2	3.2	3.5	3.5

There are two main sources of power dissipation in a chip, dynamic power dissipation and static power dissipation. Dynamic power is due to charge and discharge of node capacitances of gates and interconnects. It increases as the chip operating frequency rises. Static power is due to leakage current that flows at the silicon substrate. It intensifies by downscaling of the technology.

The electrical power dissipated in devices causes the increase of the inside temperature above the ambient one, as a result of non-ideal conditions of the heat abstraction. Therefore, the mutual interactions between the electrical and the thermal phenomena both in devices and between them exist.

Another important heat generator in an IC is device self heating. Current flowing through a device substrate or chip interconnects creates heat due to their electrical resistance.

Temperature distribution along a chip influences the IC performance. Even if the maximum temperature has not reached, the IC may malfunction due to non-uniform distribution of power consumption along the chip.

Because power consumption and power management of ICs are critical, power analysis become indispensable for IC design and is one of the fields which is currently under extensive investigation. IC power analysis becomes more critical and more important as the number of gates increase. A common goal of power analysis is to accurately calculate the power consumption of the system under analysis.

The SPICE-like simulators are usually the analysis engine to perform power analysis. However, SPICE simulators are not able to model all thermal effects (see section 5.1) on a device. In 1995 a new model for bipolar transistors was proposed. It was called VBIC, Vertical Bipolar Intercompany Model. It improved some deficiencies of BJT GP model including self heating effect. Figure (4.12) shows the equivalent schematic of VBIC model. It shows that a simple thermal network has been used for the model. Such a simple thermal

circuit is not able to perform accurate thermal analysis and present temperature distribution across the IC. Also, it is not able to consider temperature dependency of thermal conductivity of semiconductors. In case of complex circuits the model is incapable of performing thermal coupling.

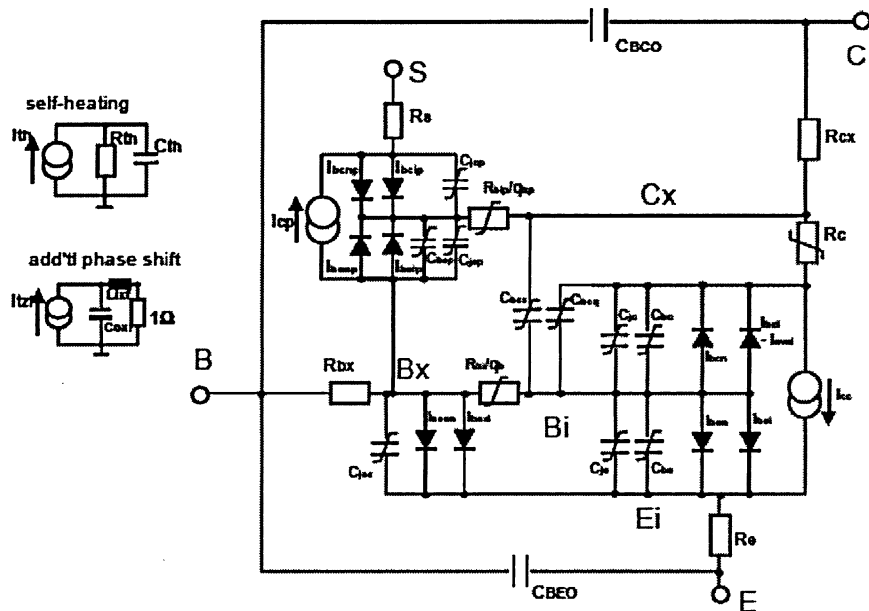


Figure 4.12: Equivalent Schematic of VBIC model. [28]

To present an example of limitations of circuit simulators the results of the electrothermal simulation of Op-Amp 741 obtained in [29] is presented. Figure (4.13) shows the DC transfer characteristic of the operational amplifier attained by experiment and computer prediction. It shows a seriously distorted DC transfer curve when the output load resistance, R_L , is 1 k Ω . The load results in power dissipation in the output transistors; Hence, increasing their temperature. The heat dissipated at the output transistors propagates inside the chip toward the input transistors; while the input stage of an Op-Amp is very temperature sensitive. This thermal feedback results in a distorted transfer curve [29, 30].

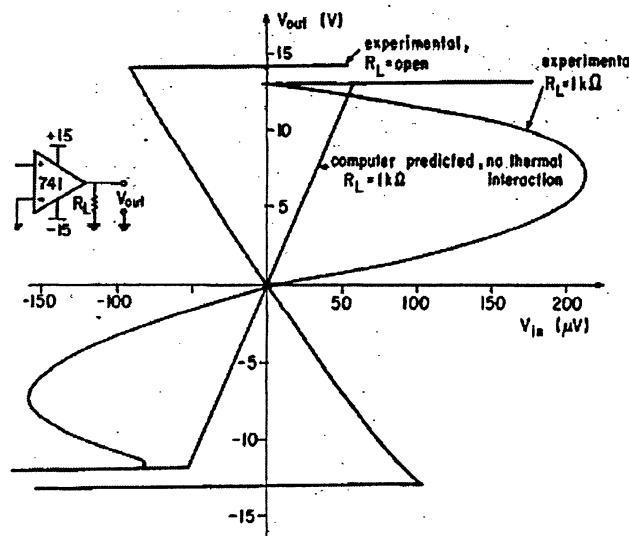


Figure 4.13: DC transfer curve of Op-Amp 741[29].

Even though thermal feedback can be reduced by applying special rules to the layout of analog or mixed signal circuits, the need to apply electrothermal analysis on VLSI circuits is still vital.

As discussed above electrical and thermal characteristics of an IC are strongly subjected to each other; therefore, to obtain an accurate estimation of power dissipation and temperature distribution in a chip, electrical and thermal analyses need to be performed simultaneously.

4.4 Summary

In this chapter we introduced SPICE electrical simulator, which is the applied electrical simulator in the developed electrothermal simulator. The deficiency of SPICE in regards to device temperature variations was discussed. Since the main focus of this research is on BJTs, BJT SPICE model and its parameters variations with temperature were presented. To confirm the parameters variations with temperature some experimental results were also illustrated.

The effects of increase of power dissipation on VLSI circuits and its consequence on the circuit temperature were discussed.

Chapter 5

In this chapter two numerical methods that are implemented to design an electrothermal simulator are introduced. The first one is called the *direct* method. The second method was called the *relaxation* method. For each of these methods the available electrothermal simulators in literatures are described. However, the attention is on the simulators with BJT circuit's application.

5. Electrothermal Analysis

As it has been discussed earlier in two previous chapters (chapter 2 and chapter 4), the performance and characteristics of semiconductor components in electronic circuits can be considerably affected by temperature variations. Therefore, accurate circuit simulation requires that the dynamic temperature effects induced by the heat dissipated in the circuit be taken into account. Modeling electrothermal interactions in integrated circuits has been addressed in a variety of ways [31]. Based on the literature and available researches, existing methods can be broadly classified into two major methods: *direct* method and *relaxation* method. In this chapter different techniques that have been designed to perform an electrothermal analysis are examined.

5.1 Direct Method

One way of incorporating thermal effects in a circuit simulator is to make the thermal model look like an electrical circuit. The thermal and electrical problems are then solved simultaneously as if they were one large electrical problem. This strategy is based on

transforming the thermal problem into an equivalent electrical problem (see also section 3.6). The iterative solution takes place simultaneously for the electrical and thermal sub-networks. This electrical modeling of thermal characteristics is possible thanks to the similarities that exist between some fundamental electrical and thermal behaviors of solids. Electrical potential difference between two points of a conductor causes electrical charge movements inside it and temperature gradient between two points of a conductor causes heat flows through it. This means different locations within a component and their corresponding temperatures can be modeled by nodes of an electrical network and their corresponding voltages. Amount of heat transferred between two locations and its rate on the other hand can be represented by electric charge and its rate which is electrical current.

Assuming that:

Ω_i : A physical location inside a component, of node i of electrical model.

T_i : Temperature of Ω_i .

V_i : Voltage of node i .

ΔQ_{th} : Heat flow from one location to another location.

ΔQ_e : Electrical charge moving from one node to another node.

q : Heat transfer rate from one location to another location.

I : Charge transfer rate or electrical current from one node to another node.

The relation between voltage difference and current of an electric conductor is called *Ohm's law*. The relation between temperature gradient and heat transfer rate is called *Fourier's law* (see also section 2.1.1).

Ohm's law: $I = \Delta V / R$, where R is electrical resistance.

Fourier's law: $q = \Delta T / R_{th}$, where R_{th} is thermal resistance.

Electrical resistance and thermal resistance are dependent to both physical characteristics and physical dimensions of a material.

Electrical resistance: $R = \frac{l}{\sigma} \times \frac{L}{A}$

Thermal resistance: $R_{th} = \frac{l}{k} \times \frac{L}{A}$

Where σ represents electrical conductivity of material and k represents thermal conductivity of material. A is the cross section and L is the length of the component.

Thermal capacitance is a characteristic of material. It shows how much heat must be transferred inside a unit size of that material such that its temperature increases one degree of centigrade and can be modeled by an electrical capacitance.

C_{th} : represents thermal capacitance, and C represents electrical capacitance

These dualities allow us to model thermal characteristic of component by an electrical network consisting of resistors, capacitors and current sources.

Node voltages of this model then will be calculated and represent the temperature of different locations within the component.

To be able to perform an accurate simulation many details need to be considered, which make the thermal network very complex, such as die, header and packaging of the IC and their boundary conditions, 3D property of temperature and temperature-dependent thermal conductivity of semiconductors. Each of the above conditions increases the system complexity.

Performing electrothermal analysis using direct method usually needs to change the equation systems of devices or to define a new model for the particular device. Hence, a new model definition is required for each device type.

5.1.1 Literature Review on Direct Method

One of the earliest researches implementing direct method was performed by Munro et. al [8, 32] in 1991. Figure (5.1) shows the electrical analog circuit between the electrical nodes and the thermal nodes. B, C and E are the electrical nodes whereas J and A are the thermal nodes.

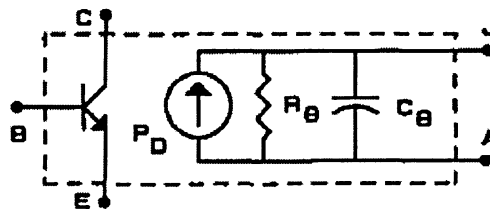


Figure 5.1: The BJT CAD model showing the electrical analog circuit between nodes J and A which models thermal effects [32].

Node J stands for Junction and node A stands for Ambient; therefore, T_{JA} represents device junction to ambient temperature. BJT equation is the standard Gummel-Poon (GP) model. The electrical simulator WATAND [33, 34] has been used. Basically any simulator that provides access to the device equations and has the ability to analyze a user defined model is applicable [8].

In the simulation, the device temperature is estimated from the voltage drops between nodes J and A. Equation (5.1) is solved by the CAD simulator to obtain V_{JA} , which is equivalent to the device junction to ambient temperature.

$$P_D = \frac{V_{JA}}{R_\theta} + C_\theta \frac{dV_{JA}}{dt} \quad (5.1)$$

$$V_{JA} \equiv T_{JA} = T_J - T_A \quad (5.2)$$

where P_D is device power dissipation and R_θ and C_θ are device junction to ambient thermal resistance and capacitance, respectively.

In [32] Munro et. al applied the method on a simple BJT amplifier as shown in Figure (5.2). Some measurements on a similar circuit have been also conducted.

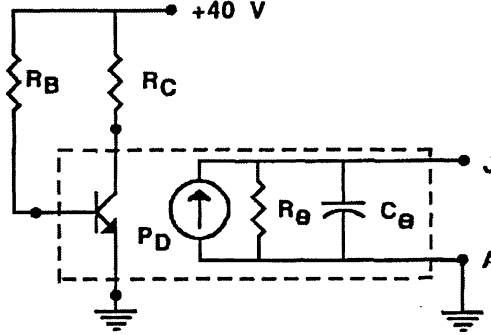


Figure 5.2: The BJT circuit and its electrical analog thermal circuit [32].

In this experiment, the collector current has been kept constant and equal to 10mA by changing R_B . R_C was varied to provide power dissipation ranges between 50mW and 340mW. Comparison between simulation results and experimental results indicated that the electrical-only simulation had error ranges from -22% to +28% while the electrothermal simulation results had the maximum error of 2.3%.

In [8] Munro et. al applied the same method on a current mirror circuit. Figure (5.3) illustrates the implemented electrothermal circuit. J_1 and A_1 are the thermal nodes of Q_1 whereas; J_2 and A_2 are the thermal nodes of Q_2 .

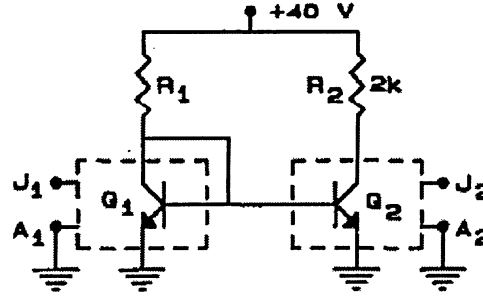


Figure 5.3: The current mirror circuit and the thermal nodes of the BJTs [8].

Experimental measurements have also been performed on the same circuit. In the experiment efforts, R_1 was varied in a range between $2K\Omega$ to $20K\Omega$ and provided a reference current value between 19.6mA to 2mA .

Comparison between the simulation results and the experimental results confirmed the advantages of performing an electrothermal analysis. The results indicated that the standard GP model had a maximum error of 84% while the error of the new method was 6.1%. The results of electrothermal analysis showed that the load current did not appropriately follow the reference current.

This method has also been applied to analyze a current mirror IC where the devices were thermally coupled and had the same junction temperature, nodes J_1 and J_2 were connected together to model thermal coupling. The results were similar to the CAD standard, where devices were assumed to have the same junction temperature.

A similar work was performed by Shelar et. al [9] in 2004. They also used the analogy of electrical and thermal equations, using HSpice as the electrical simulator. This technique models the thermal behavior of a chip by assigning the heat conduction equations in terms of electrical equations. Since heat conduction problems can be solved numerically by using finite difference approach, the heat diffusion equation (see section 3.3) was transformed to equation (5.3). In finite difference approach the partial derivative at a given point is

approximated by a derivative taken over a finite interval across that point as discussed in section 3.3.

$$\begin{aligned}
 & k(h_{y^+} + h_{y^-})(h_{z^+} + h_{z^-}) \left[\frac{T_{i+1,j,k}^n - T_{i,j,k}^n}{2h_{x^+}} + \frac{T_{i-1,j,k}^n - T_{i,j,k}^n}{2h_{x^-}} \right] + \\
 & k(h_{x^+} + h_{x^-})(h_{z^+} + h_{z^-}) \left[\frac{T_{i,j,k+1}^n - T_{i,j,k}^n}{2h_{y^+}} + \frac{T_{i,j,k-1}^n - T_{i,j,k}^n}{2h_{y^-}} \right] + \\
 & k(h_{x^+} + h_{x^-})(h_{y^+} + h_{y^-}) \left[\frac{T_{i,j,k+1}^n - T_{i,j,k}^n}{2h_{z^+}} + \frac{T_{i,j,k-1}^n - T_{i,j,k}^n}{2h_{z^-}} \right] = \\
 & k(h_{x^+} + h_{x^-})(h_{y^+} + h_{y^-})(h_{z^+} + h_{z^-}) \rho C_p \frac{T_{i,j,k}^{n+1} - T_{i,j,k}^n}{\Delta t}
 \end{aligned} \tag{5.3}$$

where $h_{x^+}, h_{x^-}, h_{y^+}, h_{y^-}, h_{z^+}$ and h_{z^-} are halves of the distances from grid (i, j, k) to grids $(i+1, j, k)$, $(i-1, j, k)$, $(i, j+1, k)$, $(i, j-1, k)$, $(i, j, k+1)$ and $(i, j, k-1)$, respectively [35]. This is also shown in Figure (5.4).

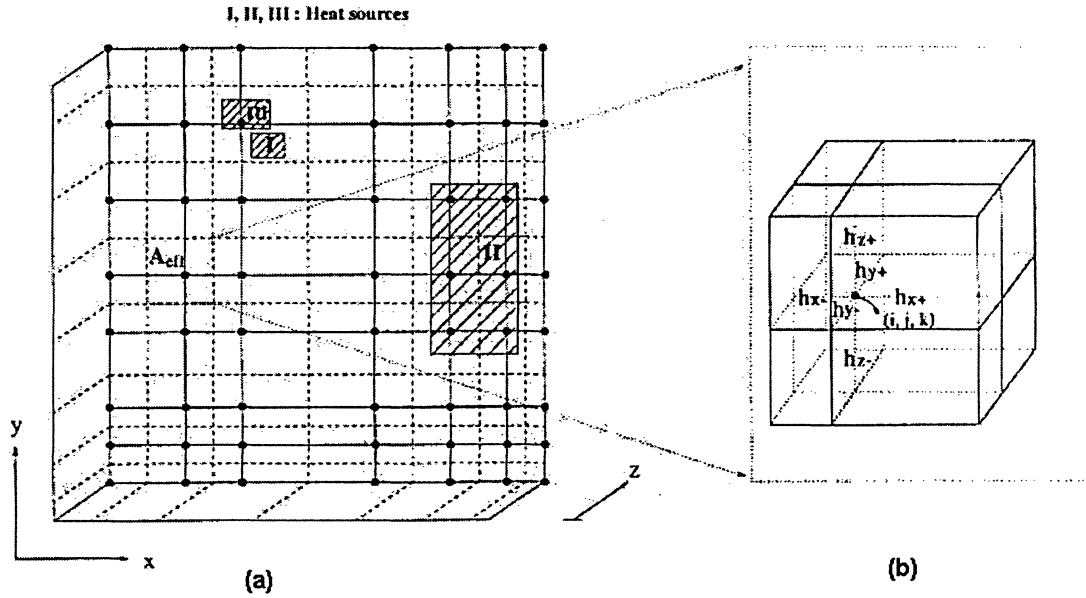


Figure 5.4: (a) Top view of the solid containing heat sources, and (b) 3-D view of grid point (i, j, k) [35].

Figure (5.5) shows the implemented RC network when self heating, thermal coupling and global heating were considered. As shown in the figure, device power dissipation is modeled by a current source, self heating and global heating are modeled by sets of parallel resistors and capacitors. The entire RC network is eventually evaluated by a thermal resistor, R_{th} , in parallel with a thermal capacitor, C_{th} .

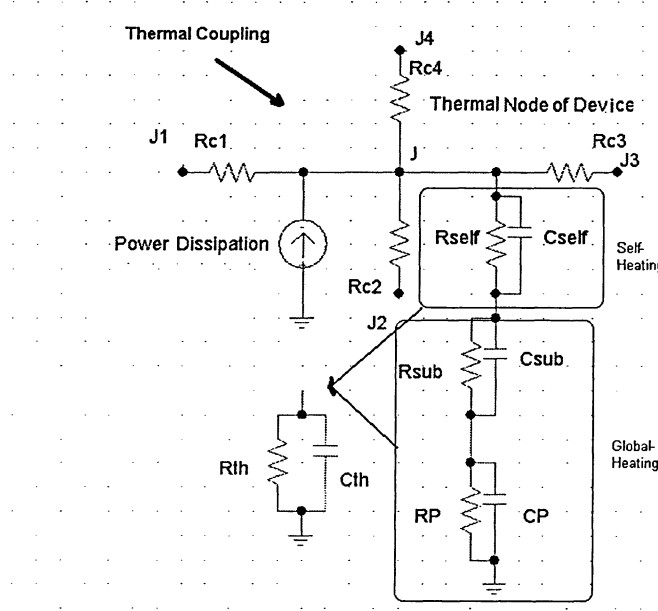


Figure 5.5: Thermal model of Shelar et. al [21].

Thermal components were defined by equations (5.4) and (5.5).

$$C = (h_{x^+} + h_{x^-}).(h_{y^+} + h_{y^-}).(h_{z^+} + h_{z^-})\rho C_p \quad (5.4)$$

$$G = \frac{k(h_{y^+} + h_{y^-}).(h_{z^+} + h_{z^-})}{2h_{x^+}} \quad (5.5)$$

In case of a BJT, temperature dependent BJT parameters are modeled as controlled sources. Considering BJT is working in the active region, Figure (5.6) shows forward diffusion current, V_F , non-ideal base emitter current, I_{NB} , and forward current gain, B_F , as a combined controlled source.

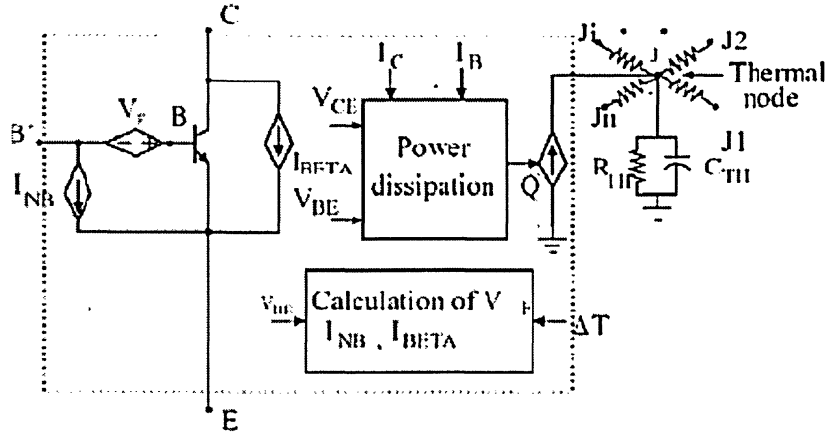


Figure 5.6: BJT thermal model of Shelar et. al simulator [21].

Shelar et.al [21] applied their method on a current mirror similar to Munro et. al [8]. The results were not improved compare to Munro et.al [8]; Nonetheless, the advantage is that, in Shelar et.al method there is no need to access device model equations to include thermal effects in electrical analysis. Another advantage is that in Munro et.al's work [8] the temperature dependent BJT parameters have to be calculated first, to obtain the operating point. This method adjusted the problem by modeling temperature dependent parameters as a combined controlled source. Therefore, the simulator performance is less time consuming for smaller circuits.

Shelar et.al [21] employed the electrothermal simulator on HFA3046B, which is an ultra high frequency transistor array integrated circuit. It included five dielectrically isolated NPN BJTs as shown in Figure (5.7).

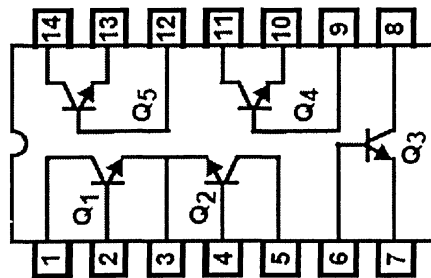


Figure 5.7: Pin diagram of HFA3046B [21].

An electrothermal simulation was performed on a current mirror circuit employing Q_1 and Q_2 . The results expressed very good agreements among the electrical simulation, the electrothermal simulation and the measurements, since the transistors were thermally coupled in the IC and had identical temperatures.

Another electrothermal analysis was carried out on a similar current mirror utilizing Q_1 and Q_4 . This time, the outcomes of the electrical simulator did not coordinate with the measurements and the electrothermal simulator. This is due to the fact that the transistors were thermally isolated but HSpice considered similar junction temperatures for them.

Figure (5.8) shows the circuit implemented in the electrothermal simulation. R_{th1} and R_{th2} represent devices self heating and R_{C12} characterizes thermal coupling.

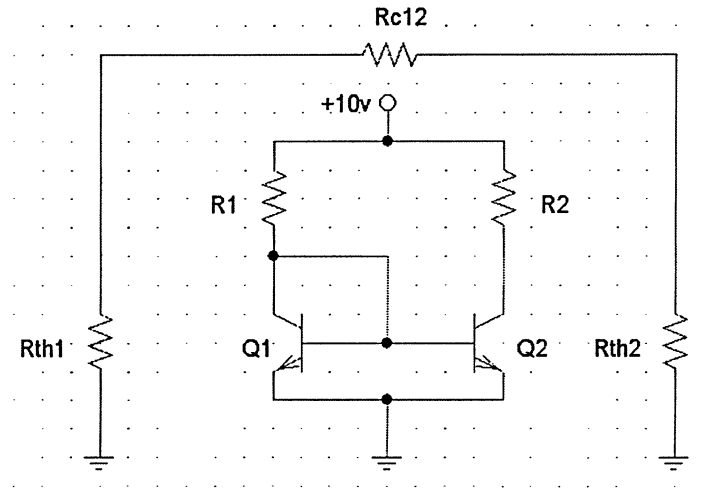


Figure 5.8: Circuit diagram of the current mirror using HFA3046B [21].

The results depicted a maximum error of 23% in HSpice while the designed simulator had an error of 7%.

Although, this method is an improvement over Munro et.al [8] model in case of device equation systems, there are still some imperfections. The method needs to define a new set of equations for every transistor type such as MOSFETs, BJTs and BiCMOS [21]. The system complexity increases when considering three dimensional heat transfer equation, different working regions of the device and thermal structure of die, header and packaging. This technique is unable to model temperature dependent thermal conductivity of semiconductors.

The direct method is accurate enough for a rough estimation of the circuit performance compared to an electrical-only simulator. However, it has some shortcomings. A newly defined set of equations has to be determined for each device in the circuit so that the electrothermal simulator can specify the device junction temperature. The method is exact only for simple circuits. In case of a composite circuit, numbers of thermal nodes increase and the simulator has to consider self heating for each device and thermal coupling among all devices. The method becomes very complex if performs 3D analysis of temperature, which significantly decreases its precision. It is also incapable of considering temperature dependency of thermal conductivity of materials. The direct method may not be able to handle nonlinearities of the system.

5.2 Relaxation Method

This method divides the original problem into electrical and thermal systems. They are solved separately and the solutions were obtained by applying successive relaxation between the two systems.

Contrary to direct method, in relaxation method two powerful electrical and thermal simulators are coupled together. Since each simulator is designed to analyze the particular electrical or thermal problem, the electrical analysis is perfectly executed by the electrical simulator and the thermal analysis is performed accurately by the thermal simulator. This method offers the advantage of using an accurate 3D thermal simulator to handle non-linear heat equation, governing on the electrical systems.

Almost all the commercial thermal simulators are able to perform 3D analysis and to consider material nonlinearities.

The only challenges in relaxation method is that how to make the simulators to communicate to each other in a synchronized manner and how to determine a consistence constraint for convergence test.

5.2.1 Literature Review on Relaxation Method

An electrothermal simulator based on relaxation method was designed by Lee et. al [36] in 1993.

A new thermal simulator was designed particularly for this simulator to perform thermal analysis. The thermal simulator performed based on the thermal network approach. The RC elements were extracted from the circuit layout. Figure (5.9) shows the implemented thermal model.

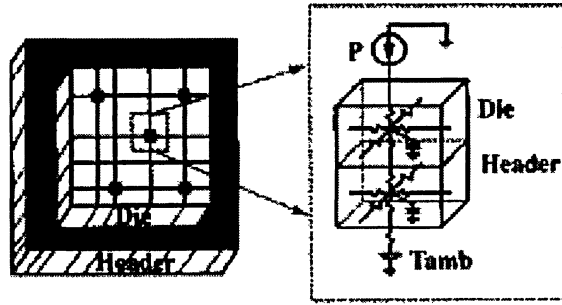


Figure 5.9: Lumped RC thermal model for the die/header structure [36].

For dc and steady state simulation the Choleski conjugate gradient method (ICCG) was applied. ICCG is a combination of incomplete Choleski decomposition and conjugate gradient optimization [36]. This method was implemented to solve three dimensional heat transfer equation faster than directly solving the equation.

For the transient analysis, first the transfer function of the RC thermal model was extracted then asymptotic waveform evaluation method (AWE) was applied. AWE determines circuit behavior by its dominant poles and residues obtained from transfer function which is expanded as a Taylor series [36]. Considering $H(s)$ in equation (5.8) as the s-domain transfer function, equation (5.10) shows expanded $H(s)$ as a Taylor series about $s = 0$. m_i represents the i^{th} moment of a circuit.

$$H(s) = C(sI - A)^{-1}B \quad (5.8)$$

$$H(s) = -\sum_{i=0}^{\infty} CA^{-(i+1)}Bs \quad (5.9)$$

$$H(s) = \sum_{i=0}^{\infty} m_i s^i \quad (5.10)$$

Where A is a $n \times n$ matrix, B is an n -dimensional vector and I is the identity matrix [36].

The designed thermal simulator was coupled to SPICE3 as the electrical simulator to compose an electrothermal simulator.

The thermal simulator programming format was readable for SPICE so the electrical simulator could communicate to the thermal simulator.

This technique was able to consider temperature dependency of semiconductor thermal conductivity.

The reprehensive results of the electrothermal simulator for a current mirror circuit are shown in Figure (5.10). In this example two types of BJT structures were considered, the conventional structure and SOI (Silicon on Insulator) structure. As expected, the electrical simulator results indicated a good mirroring between the reference current and the output current however, the electrothermal simulation results contravene it.

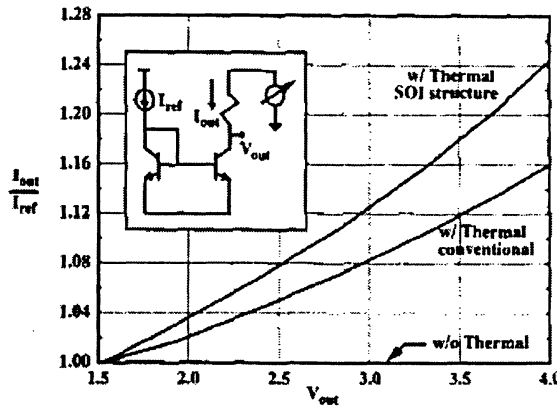


Figure 5.10: DC gain versus output voltage of a current mirror using SOI and trench isolated BJT devices, with and without thermal effects [36].

Clearly, this technique is significantly improved compared to the models applying direct method. Since thermal equation is solved by a distinct thermal simulator, there is no need to define new device equations. The extracted thermal network is more comprehensive. It is able to consider thermal conductivity temperature dependency of materials. It is also capable to perform 3D thermal simulation.

There are a few drawbacks in this technique. Multilayer structures complicate consideration of temperature-dependent thermal conductivity. The system was not able to present a 3D temperature profile of the applied circuit. There are many commercially available thermal simulators that could perform more accurately than the designed one.

There is no data available to estimate the accuracy of the model in comparison to experimental results.

A new electrothermal simulator, called ETS, was designed by Petegem et. al in 1994 [37]. The electrical circuit simulator was ANASIM and was based on SPICE model. The thermal simulator was SYSTUS and was based on finite element approach. Figure (5.11) shows a one layer thermal model implemented in SYSTUS when heat conduction was the only heat transfer method.

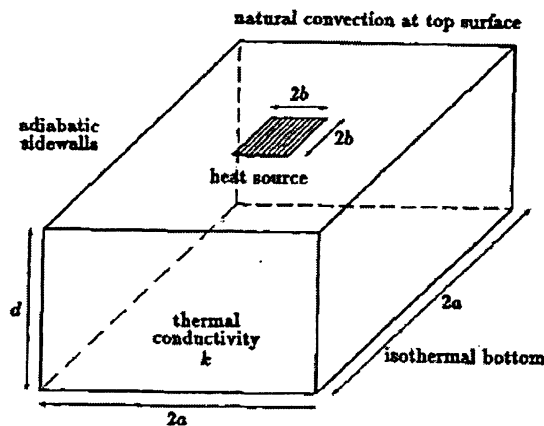


Figure 5.11: One layer model for a typical heat conduction problem [37].

Both transient and steady state thermal analysis can be performed in SYSTUS. In a transient analysis, for each critical time interval, mean temperature of each component was calculated by thermal simulator and the electrical model was updated according to that. The new voltage and current were calculated by the electrical simulator then by translating voltage and current into dissipation, thermal transient simulation was performed again in SYSTUS. If only small variations of temperature were attained at this stage the next time interval was selected, otherwise the loop continued until the convergence was achieved.

The steady state analysis was the same as the transient, except that no time interval was required.

ETS is able to consider system nonlinearities since it is implementing two powerful simulators. Nonetheless, there are some deficiencies in the simulator. ANASIM, according to the literature, is not able to specify an exclusive temperature for each device in the circuit; therefore, a model has to be defined for each semiconductor device and all temperature dependent parameters have to be modeled according to their specified temperature. SYSTUS, on the other hand, is a time consuming simulator when more layer is added to the thermal model. It is also not capable of considering more than one dissipating element at the same time; therefore, superposition needs to be applied.

No resources were found to explain how ANASIM and SYSTUS communicated in Petegem et. al work.

One of the most improved electrothermal simulators was designed by Wunsche et. al [38] in 1997. For the electrical simulator they used SABER, which is a multiphysics domain that supports a hardware description language, and ANSYS was used as a thermal simulator, which is a FEM based program.

The electrical circuit model has to be implemented by MAST, which is a behavioral description language.

To transfer data between the simulators they used parallel virtual machine, PVM. A program was written in C for SABER and a program was written in FORTRAN for ANSYS to perform the data transfer process. In case of transient analysis, to control the time interval a control routine was written in MAST. For the convergence test the calculated and extrapolated power from SABER was compared in a program also written in MAST. Since MAST was unable to repeat a calculated time step in SABER, a time step control algorithm was developed in MAST. Selected time step depended on the convergence behavior. If the convergence is smaller than a predefined error Δ_1 time step increased otherwise it decreased.

A transient electrothermal analysis applied on a current mirror circuit, Figure (5.12), similar to the work of Munro et. al [8], to estimate the simulator performance. In SABER the BJT model was extended to an electrothermal model. The analog behavioral language MAST was used to implement the model.

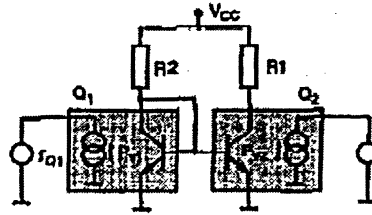


Figure 5.12: Current mirror circuit implemented in SABER [38].

The 3D thermal FEM model was composed of 608 finite elements using a simplified model of the real system. It consisted die, die attach and header as shown in Figure (5.13).

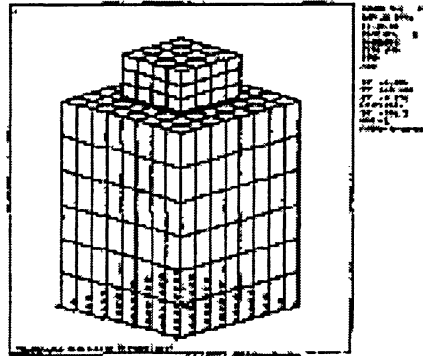


Figure 5.13: Thermal model of the device [38].

The transient results are illustrated in Figure (5.14). Figure (5.14) shows that the reference current, I_{R2} , reached its finite value immediately while the output current, I_{R1} , had delay until it reached a steady state value; nonetheless, it did not mirror the reference current.

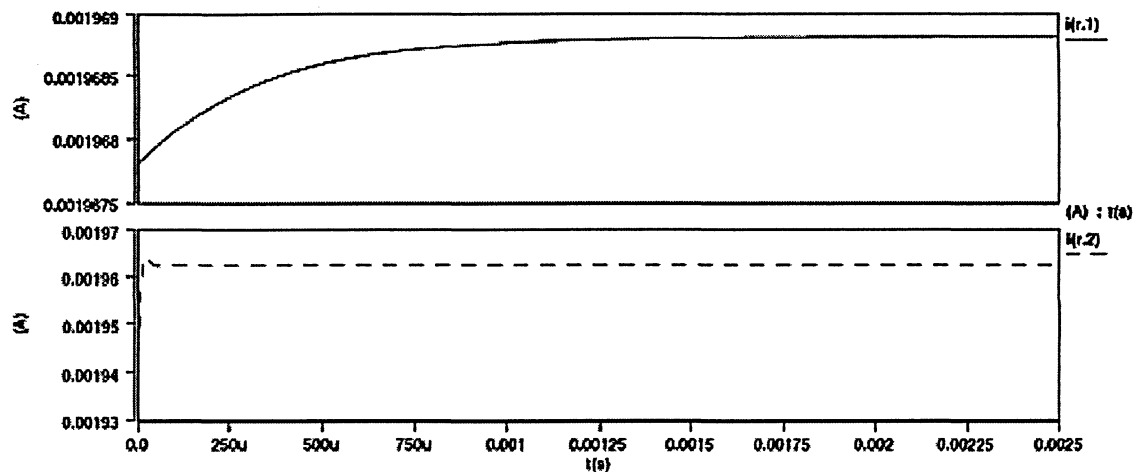


Figure 5.14: Simulation results of Wunsche et. al simulator [38].

According to the references of this method, it is more accurate than the previously explained techniques. Nonetheless, it still has some weaknesses. The simulator coupling is very complicated. The user needs to be familiar with three major programming languages to be able to couple the two simulators. The error control for each time step is not always sufficient. The simulation is very time consuming; for instance, it took four hours to simulate the current mirror circuit.

5.3 Summary

So far different methodologies (Direct method and Relaxation method) to perform electrothermal analysis on a VLSI system were introduced. Then, we went through the advantages and disadvantages of each method by presenting different electrothermal simulators that were available in literatures.

Relaxation method was implemented in the developed electrothermal simulators due to its advantages compare to Direct method, especially when system nonlinearities increase and when different parts of a chip such as its packaging and cooling system are considered. In addition, detailed three-dimensional thermal analysis of the internal structure of the device and the inclusion of circuit metal interconnects of devices can be performed.

Chapter 6

In this chapter we will elaborate our method to design a new electrothermal simulator. This method is based on the relaxation approach. A circuit simulator and a finite element thermal simulator are coupled through an application program interface that transfers information between two simulators. The methodology of coupling simulators and implemented technique and algorithm will be reviewed.

6. Implemented Methodology

An electrothermal simulator should have certain features in order to be widely useful as a design tool. These specifications include, capability of performing DC, AC and transient analysis, easily obtaining the required parameters for thermal simulation, accurately modeling of temperature dependency of electrical circuit, capability of simulating different aspects of electronic circuit behavior and capability of simulating different parts of a chip structure such as die-attach and flip chip attach bonding [29]. The proposed method contains all the above features.

6.1 Methodology of Simulators Coupling

An electrothermal simulator based on the relaxation method has been developed. As mentioned in chapter 5.2 the relaxation method requires an electrical simulator to perform circuit analysis and a thermal simulator to perform thermal analysis. These simulators should

have some typical properties. The simulators must be able to receive and to send calculated values (i.e. power dissipation and temperature distribution) to another simulator. In addition, a time incremental approach is required during the simulation efforts. The circuit simulator PSpice [6] and the finite element analysis tool COMSOL [7] possess these properties. PSpice, which is a very powerful circuit simulator for PCs, was selected as the electrical simulator. It is based on SPICE modeling of the device. COMSOL was selected as the thermal simulator. This simulator is based on finite element method. It is able to perform 3D transient and steady state thermal analyses and post process the output data, such as temperature distribution, in a 3D domain.

MATLAB was chosen as the environment to synchronize the transfer of information between these two simulators.

6.1.1 Implemented Algorithm

The flow chart of the developed algorithm is shown in Figure (6.1). The procedure begins by computing power dissipation in PSpice at the given time step. The initial device junction temperature, T_J , is defined according to the ambient temperature. The power dissipation is imported to COMSOL as the heat source of the thermal model, through MATLAB program. The three-dimensional finite element model generated by COMSOL is used to obtain temperature distribution in the thermal model according to the defined heat source. Time dependent thermal conduction equation (see section 2.1) is solved in COMSOL at a given time step to extract the junction temperature, and temperature profile. The new junction temperature is imported to PSpice and the power dissipation is updated, by taking the new temperature profile into account. PSpice is run from MATLAB and new power dissipation is computed [39]. Every time that COMSOL computes new junction temperature according to the new heat source, a convergence test is executed. The selected convergence parameter depends on the simulation. It can be device temperature, power, current etc. The parameter should be the one that the user has a good knowledge of its variation or the one that is more critical in the simulation. The convergence parameter is compared to the previously calculated one.

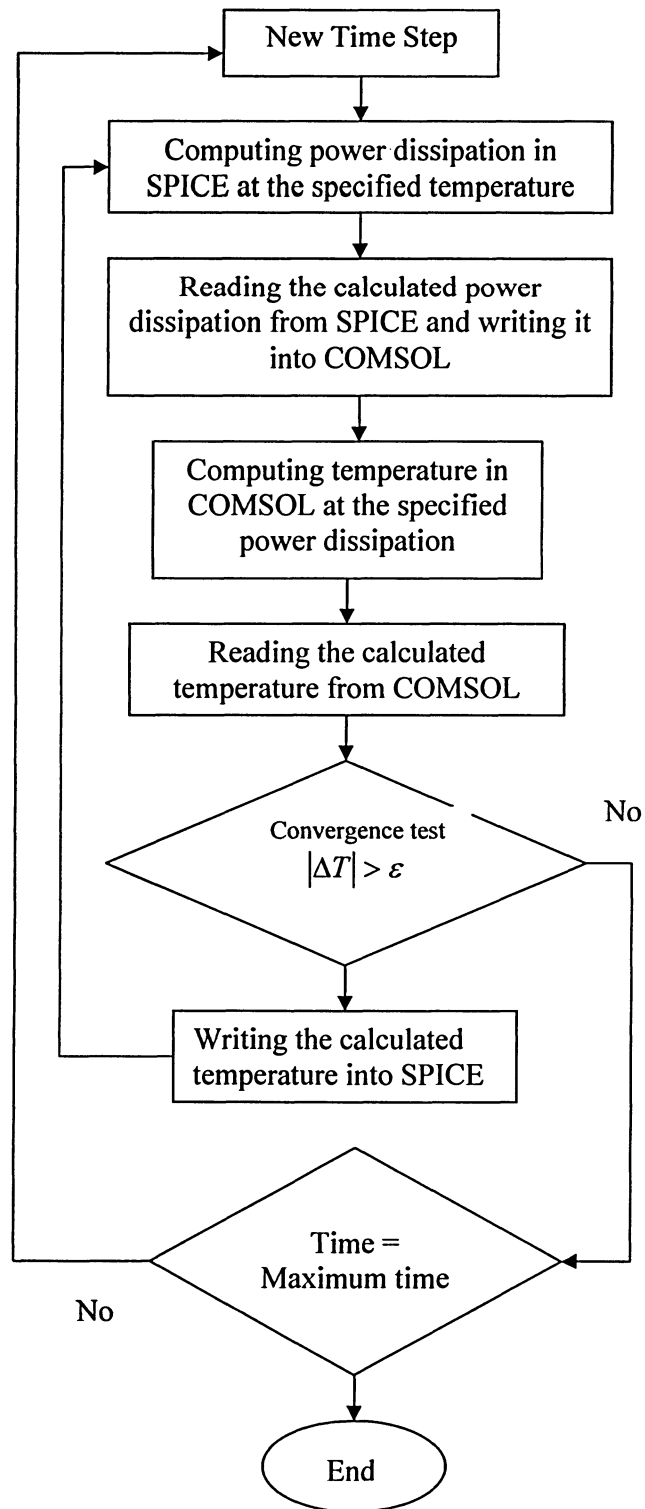


Figure 6.1: Flow chart of the electrothermal simulator.

In figure (6.1) the convergence factor is considered device temperature. The loop should be continued until the difference is smaller than the specified error, ε . If the convergence is achieved, the next time step will begin.

Based on the analysis type (DC, AC, and Transient) a default value of ε can be extracted for a given circuit. ε should be small enough so that increase of temperature (or another selected parameter) does not affect the electrical behavior of the circuit at the specified time step.

The termination of the iteration in the algorithm is determined by convergence criterion. The convergence behavior of the simulator is affected by the choice of proper initial conditions for the first time interval. Each time interval applies the results of the previous time step as its initial condition. Selecting an appropriate time step depends on the convergence behavior of the system. If variations of the convergence factor are large, time step should be small so the changes can be modeled properly. In addition, if the parameter variations are small, time step may be selected large enough to accurately model the changes and to reduce the simulation time. In case of a steady state simulation no time step is required.

The procedure of the simulator has been elaborated in more details in the following sections.

6.1.2 Coupling COMSOL and MATLAB

COMSOL Multiphysics is an interactive environment for modeling scientific and engineering applications based on partial differential equations [7]. It is fully compatible with MATLAB. By developing an FE model in COMSOL using COMSOL Scripts, user can easily switch between MATLAB commands and COMSOL codes. In fact COMSOL codes are similar to MATLAB codes; however, in case of FEM it is more user friendly than MATLAB. COMSOL codes can be compiled in MATLAB.

For this research heat transfer equation was modeled by COMSOL scripts. Heat sources, start time, stop time and time step were considered as variables; therefore, they were simply modified during the electrothermal simulation according to the newly calculated data.

6.1.3 Coupling PSpice and MATLAB

To consider device junction temperature (T_J) in PSpice, the device model was modified to include T_J . The general format for modeling a bipolar transistor in PSpice is [40].

QNAME NC NB NE MODEL_NAME
.MODEL MODEL_NAME TRANSISTOR_TYPE
MODEL_PARAMETERS

NC, NB, NE are the node numbers for the collector, base and emitter, respectively.

MODEL_NAME is a name for the particular model.

TRANSISTOR_TYPE can be either NPN or PNP.

MODEL_PARAMETERS are the parameters that model the BJT characteristics. Device junction temperature is included in these parameters [40].

If more than one device is integrated in the simulation, a junction temperature should be specified for each device.

By analyzing a circuit in PSpice, the simulator creates several data files such as, *Circuit* files, *NET* files, *Output* files, *CSDF* files etc. Each of these files contains specific information regarding the circuit and its simulation results.

Circuit files in PSpice control all the specifications of the circuit under simulation. Device models, voltage and current sources are included in them. Types of analysis such as, transient, DC and AC are also integrated in the *Circuit* files. For instance, *.TRAN* control statement is used in a *Circuit* file to perform transient analysis on a circuit. The general format of this statement is

.TRAN TSTEP TSTOP

TSTEP is the printing or plotting increment.

TSTOP is the final time of the transient analysis.

Similar to the transient analysis, the control statement for a DC analysis is

.DC SOURCE_NAME START_VALUE STOP_VALUE INCREMENT_VALUE

SOURCE_NAME is the name of an independent voltage or current source.

START_VALUE, STOP_VALUE and INCREMENT_VALUE represent the starting, ending and increment values of the source, respectively.

NET files contain all the elements of the circuit with their values and circuit wiring.

Output files include a summary of all the data files as well as results of a steady state simulation. In case of an error in analyses, it is specified in this file.

CSDf files contain all the simulation results by default; such as, all the currents, voltages, power dissipations and noise. In case of a transient analysis *CSDf* files include the simulation results of each time step.

To be able to write a new T_j into the device model and to introduce a new time step to PSpice in case of a transient analysis, a subroutine was developed in MATLAB. This program, called “*Writing*”, writes a new *Circuit* file and inserts the new values of the time step and the junction temperature. Therefore, PSpice performs the electrical analysis according to the modified model and the new time step. In case of steady state simulation, no time step is required.

To read the calculated power dissipation, P_D , a program was developed in MATLAB. This function, called “*Reading*”, reads the required parameter values from PSpice *CSDf* file. However, in case of a steady state analysis, the power dissipation can be obtained from the *Output* file, too. *Reading* function reads the required data from the *CSDf* or the *Output* file.

Writing and *Reading* functions are the main interfaces between PSpice and COMSOL.

6.2 Summary

The methodology and implementation of the developed electrothermal simulator has been reviewed. Applying relaxation method, commercially available thermal simulation tool, COMSOL finite element software, and SPICE electrical simulator were coupled to each other using an interface program developed in MATLAB.

All the detailed regarding the performance of each simulator were elaborated in this chapter, and the coupling procedure of the two simulators through MATLAB was also explained in details.

Chapter 7

7. Electrothermal Investigation of Si BJT Circuits

To examine the performance of the electrothermal simulator we performed both DC and transient analysis on different Si BJT circuits. Electrothermal analysis was performed on an active BJT implementing a simple thermal model. The results were satisfactory and very close to what was obtained in theory. A DC analysis was performed on a Si BJT amplifier and the results of the circuit parameters were compared to the available experimental data. The results were in good agreement to the experimental data. Transient analysis was also performed on a Si BJT current mirror to estimate the ability of the simulator in the presence of thermal coupling. The obtained results were very encouraging. The following sections are the elaborations of these analyses.

7.1 Active BJT

A bipolar junction transistor has four distinct regions of operations, forward active, reverse active, saturation and cutoff. Figure (7.1) shows BJT regions of operation.

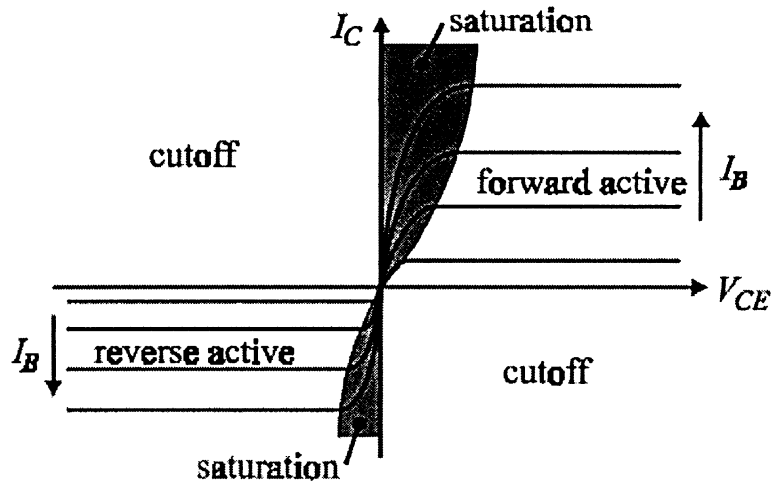


Figure 7.1: BJT regions of operation [3].

BJT is called active when it is biased in its forward active region of operation. BJT operates in its forward active region when the base-emitter junction is forward biased and the base-collector junction is reversed biased.

As expanded in chapter 4, BJT parameters are temperature dependent. We showed on chapter 4 how BJT parameters and its operating point change by temperature. In this section we would like to illustrate some of these variations implementing our electrothermal simulator.

7.1.1 Electrical Model

Figure (7.2) represents the electrical circuit of active 2N3904 NPN BJT. The device junction temperature was added to the transistor model.

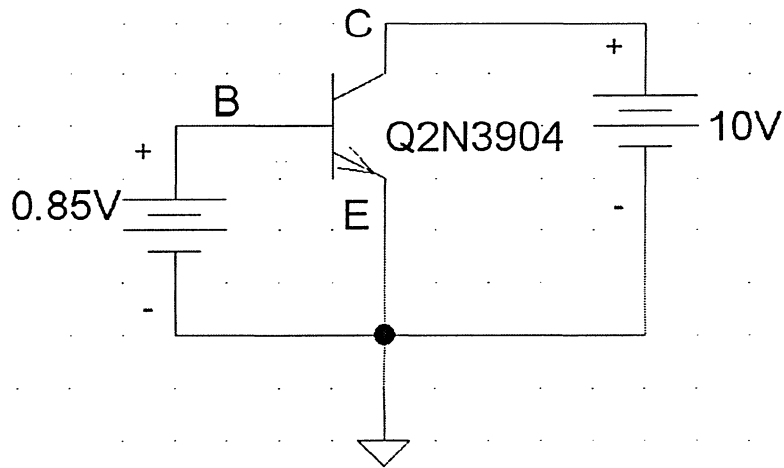


Figure 7.2: Circuit of the active BJT.

The BJT was biased in a moderate operating point. The collector-emitter voltage, V_{CE} , was 10V and the collector current, I_C , was 182.37mA. Figure (7.3) shows the graph of I_C versus V_{CE} at ambient temperature (27°C). When input voltage of base-emitter, V_{be} , was 0.85 VDC, the power dissipation was computed 1.83 Watts at the ambient temperature.

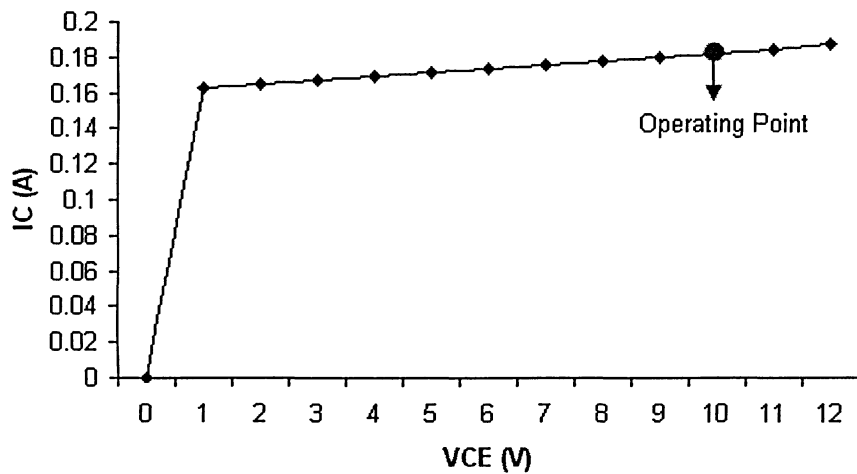


Figure 7.3: BJT DC characteristics.

7.1.2 Thermal Model

The thermal model was consisted of 8×8 devices with the size of $400\mu m \times 300\mu m \times 10\mu m$, located on a chip area of $1cm \times 1cm \times 0.035cm$. The substrate was made of Silicon. Only one device was considered active in the simulation.

The three-dimensional finite element model shown in Figure (7.4) was developed to simulate the thermal behavior of the system. The chip and the active device were modeled using approximately 11000 solid elements as shown in Figure (7.4). Only active device and the substrate are considered in the thermal model at this stage. Other parts such as die-attach and header were neglected. However, their effects are taken into account by a thermal resistance at the backside of the thermal model.

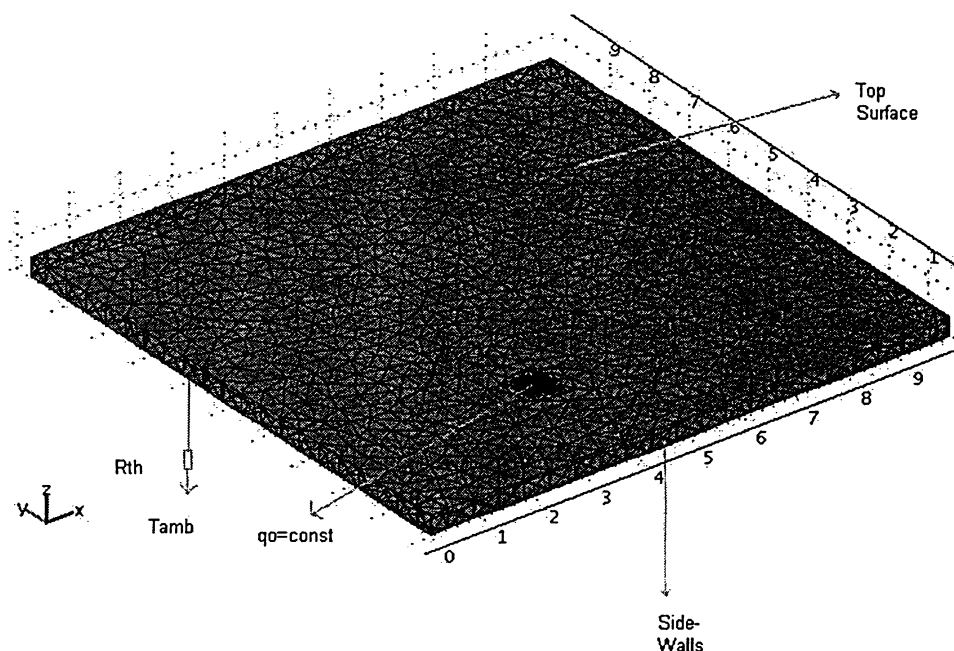


Figure 7.4: Finite element model and boundary condition.

As shown in Figure (7.4) the active device is considered as the only heat source of the thermal model.

The following boundary conditions were applied:

The top surface and the sidewalls were considered adiabatic. Therefore, Neumann boundary condition is assigned.

$$-k(\nabla T) = 0 \quad (7.1)$$

A thermal resistance was considered at the backside of the substrate to model the effects of die-attach, header, and other parts of the packaging and the surrounding environment; Therefore, the Robins boundary condition was defined at the backside.

$$-k(\nabla T) = q \quad (7.2)$$

where

$$q = \left(\frac{1}{r_{th,b}} \right) \times (T_{amb} - T) \quad (7.3)$$

and

$$r_{th,b} = R_{th,b} \times A_b \quad (7.4)$$

A_b is the backside area. $R_{th,b}$ was obtained by measurements in [2] equal to 16 K/W.

Si thermal characteristics are listed in Table (7.1).

Table 7.1: Silicon thermal characteristics.

ρ (kg/m ³)	2330
C_p (J/kg°K)	703
k_0 (W/m°K)	163
k (W/m°K)	$k_0 \times 163 \times \left(\frac{T}{300} \right)^{\left(\frac{-4}{3} \right)}$

As shown in the Table (7.1), a temperature dependent thermal conductivity was considered for Si.

7.1.3 Simulation Results

Before applying the electrothermal simulator, a steady state thermal simulation was performed on the thermal model in COMSOL to approximate the junction temperature and temperature distribution. Figure (7.5) shows the temperature contour obtained from the FEM simulation while power dissipation was considered a constant value equal to 1.83 W.

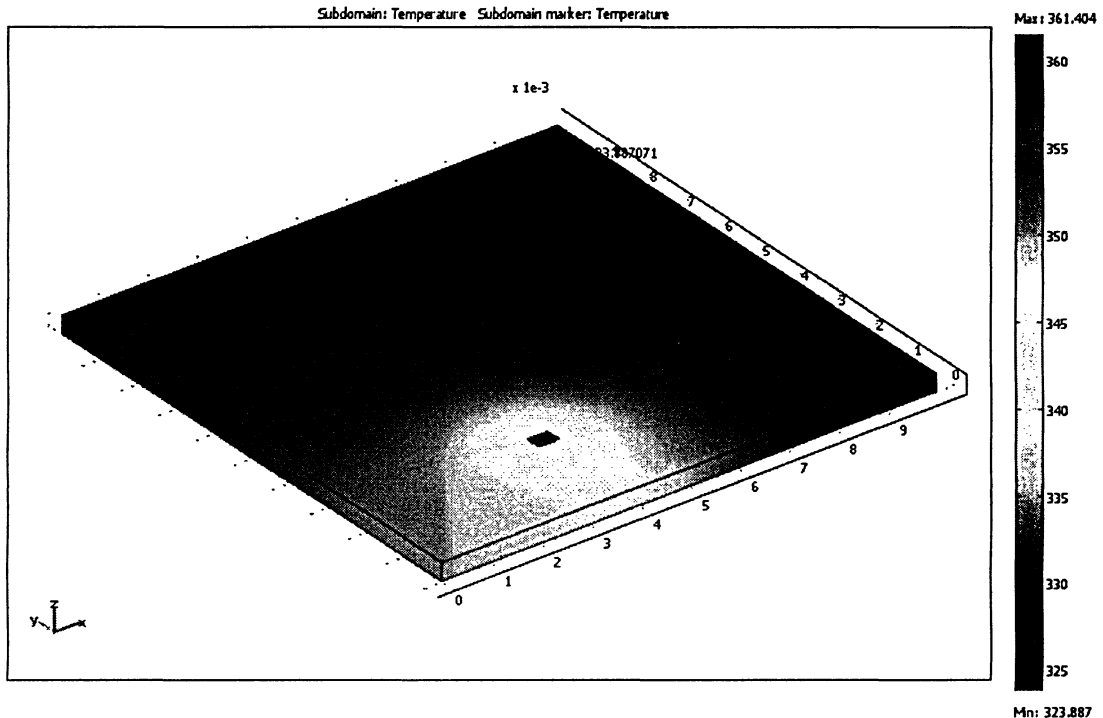


Figure 7.5: 3D temperature distribution at a power dissipation of 1.83W.

As shown in Figure (7.5), the maximum temperature was 88.4°C. It can be observed that the maximum temperature occurred at the device junction.

During coupled simulation PSpice sent the power dissipation of the transistor and received the temperature T_j of the device from COMSOL. A constant time step equal to 0.1s was considered. Since simulation time in COMSOL took approximately 4s for the device to reach its steady state junction temperature, 0.1s time step was a reasonable value to demonstrate the variations. In all the time steps, the stop time was equal to the start time plus the time step and the start time was equal to the stop time of the previous time step. The initial start time

was set at zero second. The initial temperature of the system was the same as the ambient temperature, 27°C. The active BJT junction temperature was considered as the convergence parameter. PSpice showed that only temperature increase greater than 0.1° affects the electrical simulation results; therefore, ϵ was selected 0.01 for a good convergence. The entire simulation took approximately 8 minutes on a Pentium 4 CPU, 2.80 GHz, 512 MB of RAM . Since the thermal model was very simple in this experiment, only one iteration was required in each time step to achieve the convergence criterion.

The junction temperature and power dissipation versus numbers of iterations are depicted in Figures (7.6) and Figure (7.7), respectively.

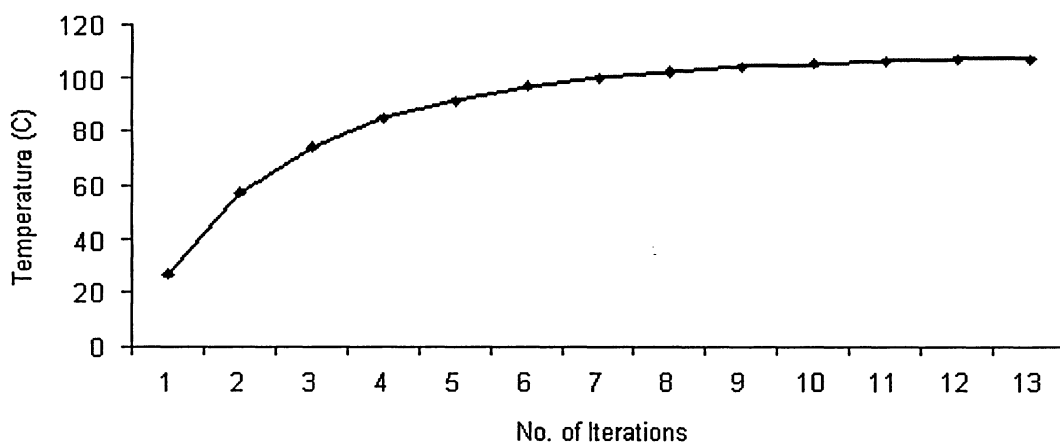


Figure 7.6: Device temperature variations versus numbers of iterations.

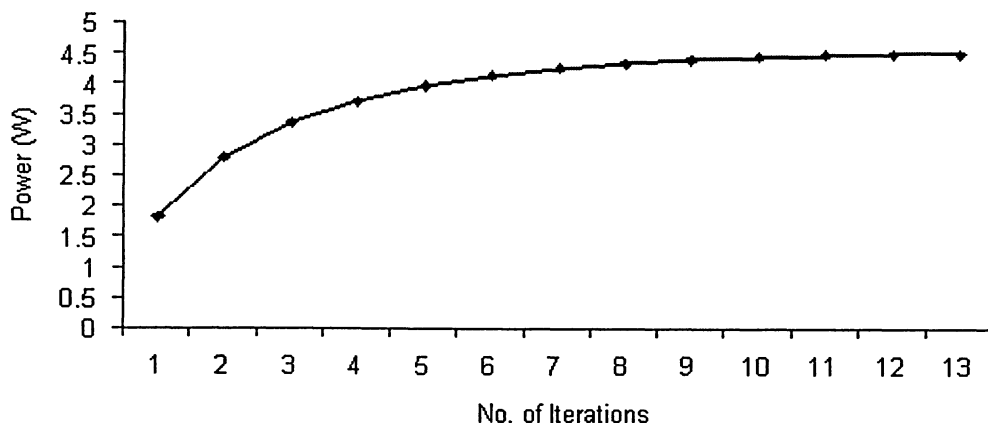


Figure 7.7: Device power variations versus numbers of iterations.

Figure (7.6) shows that the device junction temperature increased significantly in the first five iterations and it continued until it converged at the 13th iteration to the value of 107.2°C. Since each time step was 0.1s, it took 1.3s for convergence accomplishment. This figure also shows that the device junction temperature is greater than the value attained in the thermal analysis; this is due to the fact that the value of the heat source increased for all iterations which results in increase of the junction temperature.

Figure (7.7) shows that the device power dissipation started at 1.83W and increased until it converged to the value of 4.5W at 13th iteration. It shows that the device power dissipation expanded more than 2.5W.

These results confirm temperature effects on the circuit performance.

The power dissipation-temperature curve is also shown in Figure (7.8). It indicates that the converged temperature is 107.2°C. Power dissipation increased from 1.83W to 4.5W at T_j , which verifies the importance of an electrothermal simulation.

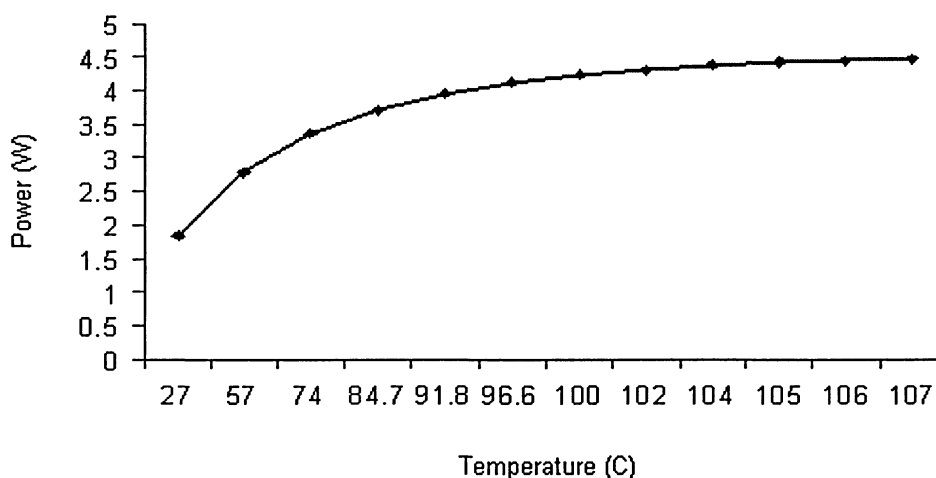


Figure 7.8: Device power variations versus its temperature.

To estimate the variations in the device DC characteristics, the collector current versus collector-emitter voltage curve was plotted while the temperature rose. Figure (7.9) indicates these variations for four given temperature at 27°C, 74°C, 96.5°C and 107.2 °C.

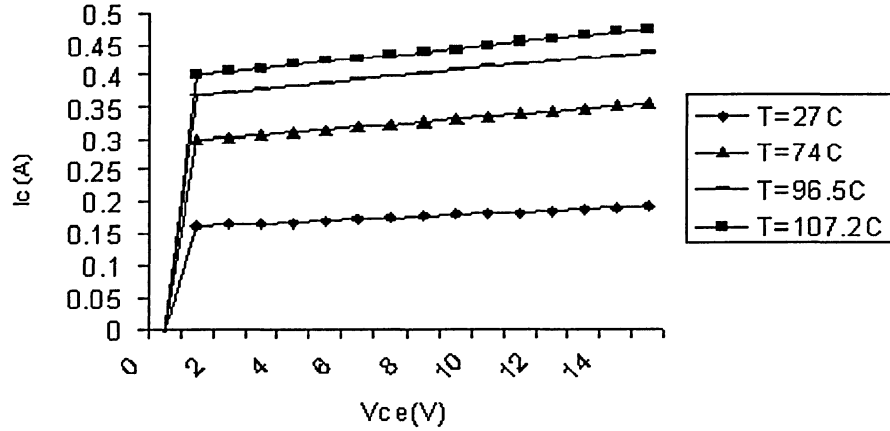


Figure 7.9: I_C versus V_{CE} while device reaches its junction temperature.

The operating point was initially located at the $I_C=0.183A$ and $V_{ce}=10V$ at the ambient temperature (see Figure (7.3)). Considering a constant V_{ce} , the value of I_C varies by increasing the temperature, for example at $T_J = 74^\circ C$, I_C is $0.334A$, at $T_J = 96.5^\circ C$, I_C is $0.411A$ and at $T_J = 107.2^\circ C$, I_C is $0.450A$. The results show changes in the device operating point. Clearly, operating points of transistors are the fundamentals of any design. Variations of operating points have severe consequences on the circuit behavior.

Note that the results may not be exactly analogous to reality. The errors may be due to the fact that the layout and dimensions of 2N3904 NPN BJT in thermal modeling had some simplification and assumption associated with its structure. This affects the dimensions of the thermal model and the backside thermal resistance; therefore, affects the values of power dissipation, collector current and number of iterations.

7.2 BJT Amplifier

In this section the electrothermal behavior of a BJT amplifier circuit is investigated. A thermal gradient on chip is generated due to the power dissipation of the BJT. The simulation results were compared to the experimental results in [32], to verify the performance of the electrothermal simulator and the accuracy of the thermal model.

7.2.1 Electrical Model

A DC analysis was performed on a BJT amplifier shown in Figure (7.10). 2N2222 Si BJT from the PSpice library was implemented during the simulation efforts. However, some parameters were changed to provide a good model for the BJT used in the experiment. GP saturation current was set to 0.03pA, the composite forward and inverse low saturation currents were set to 0A. Base, emitter and collector ohmic resistance were set to 15 Ω , 0.1 Ω and 1 Ω , respectively [32]. The forward Beta value was selected 110 [32].

The following is the BJT model in PSpice.

```
.model QMOD1 NPN(Is=30f Xti=3 Eg=1.11 Vaf=370 Bf=110 Ne=1.307
+ Ise=14.34f Ikf=0 Xtb=1.5 Br=6.092 Nc=2 Isc=0 Ikr=0 Rc=1
+ Cjc=7.306p Mjc=.3416 Vjc=.75 Fc=.5 Cje=22.01p Mje=.377 Vje=.75
+ Tr=46.91n Tf=411.1p Itf=.6 Vtf=1.7 Xtf=3 Rb=15 Re=0.1 T_ABS=Tj)
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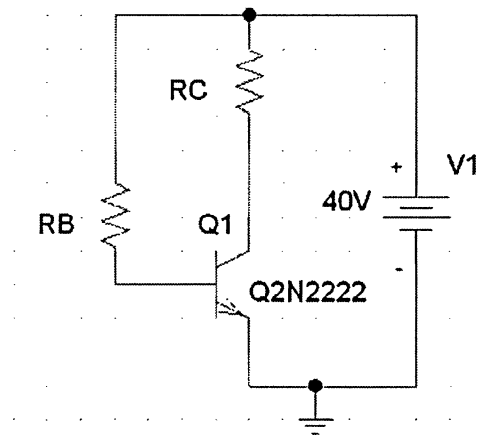


Figure 7.10: BJT amplifier circuit.

The collector current was set to 10 mA, by adjusting R_B . The power dissipation varied from 50mW to 340mW, by changing R_C [32].

7.2.2 Thermal Model

IC thermal modeling is very important in developing a useful electrothermal simulation program. The thermal model should be satisfactory enough to be able to accurately model the die and the packaging structure of the IC without significantly increasing the simulation time [29]. Figure (7.11) illustrates the actual die and header structure of an IC and its simplified physical model.

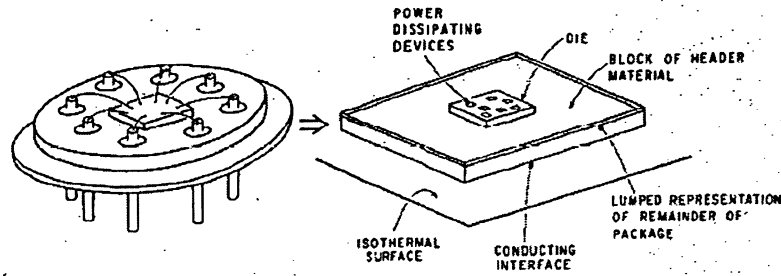


Figure 7.11: Die and header of an IC and its simplified physical model [29].

Considering only die, die-attach and header of the IC structure create a reliable thermal model. The dimensions of the die and die-attach are selected according to the device die datasheet [35]. Bearing in mind the thermal resistance of the die and die-attach, the thickness of the header is calculated in such a way to provide the remaining required junction to case thermal resistance, R_{JC} [29, 36, 38, 42].

To take into account the effect of heat convection, a thermal resistance needs to be defined at the backside equal to the device case to ambient thermal resistance, R_{CA} .

$$R_{JC} = R_{th_Die} + R_{th_Die_Attach} + R_{th_Header} \quad (7.5)$$

$$R_{CA} = R_{JA} - R_{JC} = R_{th_backside} \quad (7.6)$$

The three-dimensional finite element model developed to study the thermal properties of the transistor and its packaging is shown in Figure (7.12). The thermal model consists of approximately 8200 solid elements. As mentioned above this model was divided into three major parts: die, die-attach and the header.

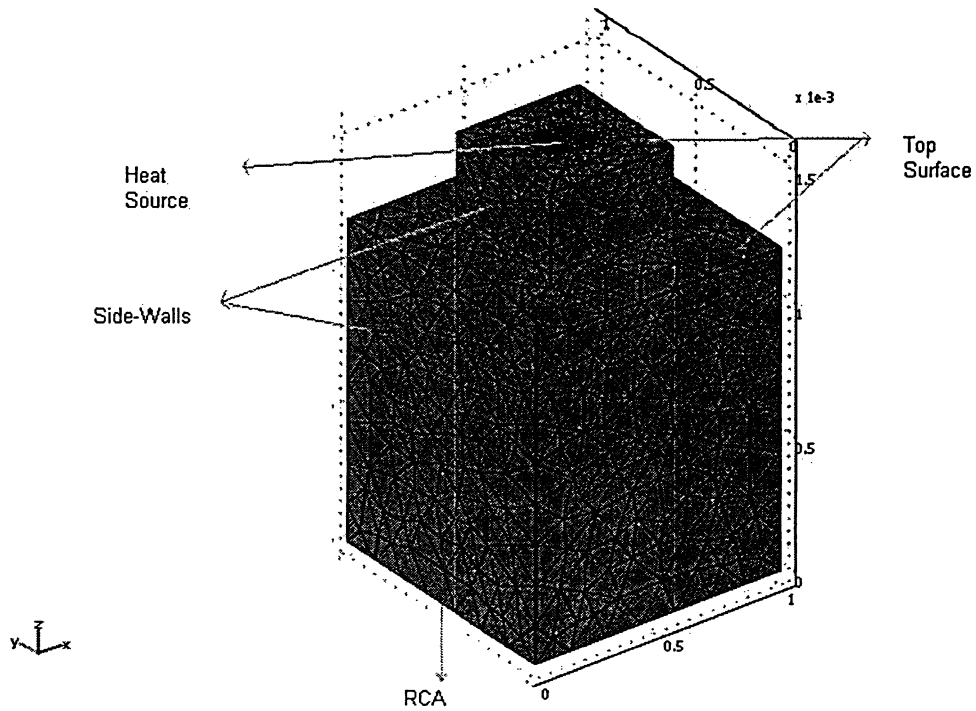


Figure 7.12: Finite element model of BJT amplifier.

Table (7.2) shows material property, dimensions and calculated thermal resistance of each layer.

Table 7.2: Material properties and dimensions of layers of the thermal model.

Layer	Material	ρ (kg/m ³)	C_p (J/kg°K)	k (W/m°K)	L (mm)	A (mm ²)	R_{th} (°K/W)
Die	Silicon	2330	703	$k_o \times 163 \times \left(\frac{T}{300} \right)^{\left(\frac{-4}{3} \right)}$	0.3	0.25	7.36
Die-Attach	97%A-3% Si	15400	169	31.46	0.05	0.25	6.35
Header	Kovar	8359	430	17.3	1.2	1	69.36

TO-18 is the predefined packaging of 2N2222 in PSpice. According to the BJT datasheet [41], the junction to case thermal resistance, R_{JC} , for TO-18 is 83K/W and the junction to ambient thermal resistance, R_{JA} , is 300K/W; Therefore, R_{CA} is 217K/W.

The only heat source in the thermal model is the active BJT with the dimensions of $100\mu m \times 100\mu m \times 10\mu m$.

The followings are the specified boundary conditions:

The top surface and the sidewalls were considered adiabatic, therefore:

$$-k(\nabla T) = 0 \quad (7.7)$$

A thermal resistance was considered at the backside with a value equals to the case to ambient thermal resistance, R_{CA} , the result is:

$$-k(\nabla T) = q = \frac{(T_{amb} - T)}{R_{CA} \times A_b} \quad (7.8)$$

7.2.3 Simulation Results

The temperature distribution across the thermal model, for a power dissipation of 246mW is shown in Figure (7.13). As it is expected the hot spot is in the location of the active device. The junction temperature was computed 112°C in COMSOL, while power dissipation was considered constant.

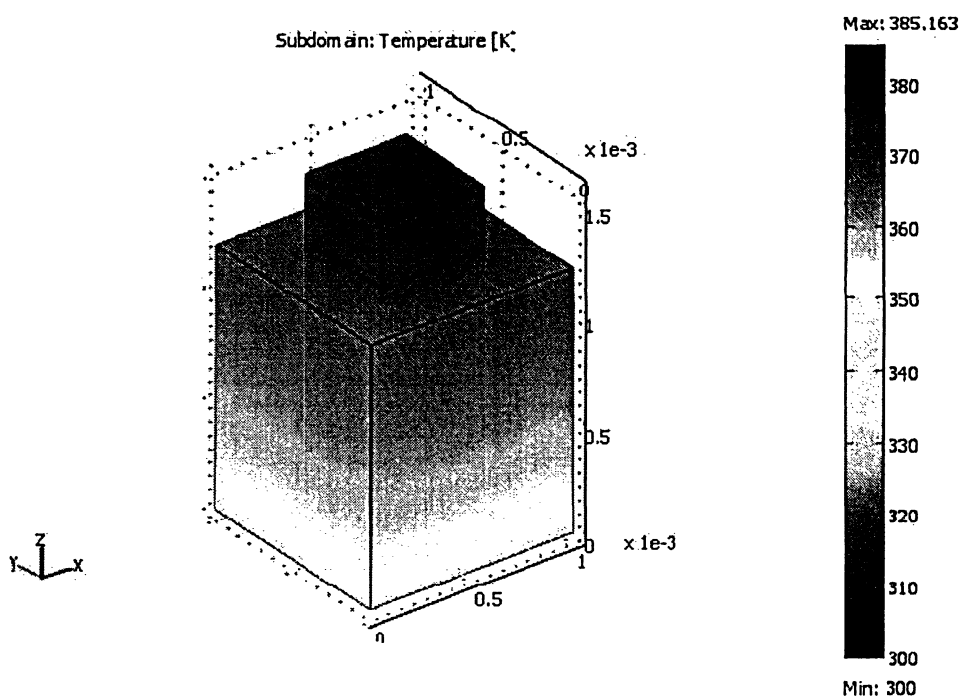


Figure 7.13: 3D temperature distribution across the amplifier thermal model.

Tables (7.3) to (7.6) show the results of steady state electrothermal simulation. Table (7.3) indicates the electrical simulator had the error ranges from -27% to 58% when computing the power dissipation. The maximum error of the electrothermal simulator was about -4% . During the measurement, R_B was changed in a way to provide a constant collector current of 10mA . The maximum error of -31.5% was calculated for PSpice simulation results of the collector current as reported in Table (7.4). The results of the electrothermal simulator are in good agreement with the experimental results, and the maximum error was about 5% . The base-emitter voltage and the forward current gain obtained from experimental and simulation results are compared in Tables (7.5) and (7.6). These results indicate very good agreements between the experimental results and the results obtained from the electrothermal simulator. The maximum error for the base-emitter voltage, V_{BE} , and the forward current gain, β_F , in PSpice were 14.7% and -31.2% while it was only -8.1% and 5.3% in the electrothermal simulator, respectively [42, 43, 44].

Table 7.3: Comparison results of the power dissipation.

R_B (kΩ)	R_C (kΩ)	P_D(mW) Experimental	P_D(mW) PSpice	Error(%)	P_D(mW) Electrothermal	Error(%)
620	0.6	340	246	-27.6	340	0.0
599	0.8	320	242	-24.3	324	1.2
581	1	300	237	-21.0	308	2.6
550	1.5	250	217	-13.2	254	1.6
522	2	200	191	-4.5	200	0.0
492	2.5	150	160	6.6	144	-4.0
474	3	100	123	23.0	96	-4.0
450	3.5	50	79	58.0	51	2.0

Table 7.4: Comparison results of the collector current.

R_B (kΩ)	R_C (kΩ)	I_c(mA) Experimental	I_c(mA) PSpice	Error(%)	I_c(mA) Electrothermal	Error(%)
620	0.6	10.00	6.85	-31.5	10.00	0.0
599	0.8	10.00	7.07	-29.3	10.20	2.0
581	1	10.00	7.26	-27.4	10.40	4.0
550	1.5	10.00	7.60	-24.0	10.50	5.0
522	2	10.00	7.93	-20.7	10.50	5.0
492	2.5	10.00	8.32	-16.8	10.50	5.0
474	3	10.00	8.54	-14.6	10.20	2.0
450	3.5	10.00	8.88	-11.2	9.95	-0.5

Table 7.5: Comparison results of the Base-Emitter voltage.

R_B (k Ω)	R_C (k Ω)	$V_{BE}(V)$ Experimental	$V_{BE}(V)$ PSpice	Error(%)	$V_{BE}(V)$ Electrothermal	Error(%)
620	0.6	0.589	0.676	14.7	0.542	-7.9
599	0.8	0.593	0.677	14.1	0.546	-7.9
581	1	0.599	0.678	13.1	0.550	-8.1
550	1.5	0.614	0.679	10.5	0.564	-8.1
522	2	0.629	0.681	8.2	0.582	-7.4
492	2.5	0.646	0.682	5.5	0.601	-6.9
474	3	0.660	0.683	3.4	0.623	-5.6
450	3.5	0.677	0.685	1.1	0.646	-4.5

Table 7.6: Comparison results of the current gain.

R_B (k Ω)	R_C (k Ω)	β_F Experimental	β_F PSpice	Error(%)	β_F Electrothermal	Error(%)
620	0.6	157	108	-31.2	157	0.0
599	0.8	152	108	-28.9	155	1.9
581	1	147	107	-27.2	153	4.0
550	1.5	140	106	-24.2	147	5.0
522	2	132	105	-20.4	139	5.3
492	2.5	125	104	-16.8	131	4.8
474	3	120	103	-14.1	123	2.5
450	3.5	114	102	-10.5	114	0.0

To evaluate the simulation performance we compared the results of the experiments, the proposed electrothermal simulator and PSpice. Figures (7.14), (7.15) and (7.16) show this comparison for the power dissipation, current gain and the base emitter voltage. As expected PSpice has the maximum error. The results of the proposed electrothermal simulator are much improved with regard to PSpice. The results of the new method could be more

improved if the layout and die datasheet of 2N2222 was available for the thermal model. Types of materials used in 2N2222 transistors implemented in the experiment and the exact SPICE model of the BJT were also not available.

In case of a precise set of data, there is no doubt that the simulator is very exact since both PSpice and COMSOL are reliable and accurate.

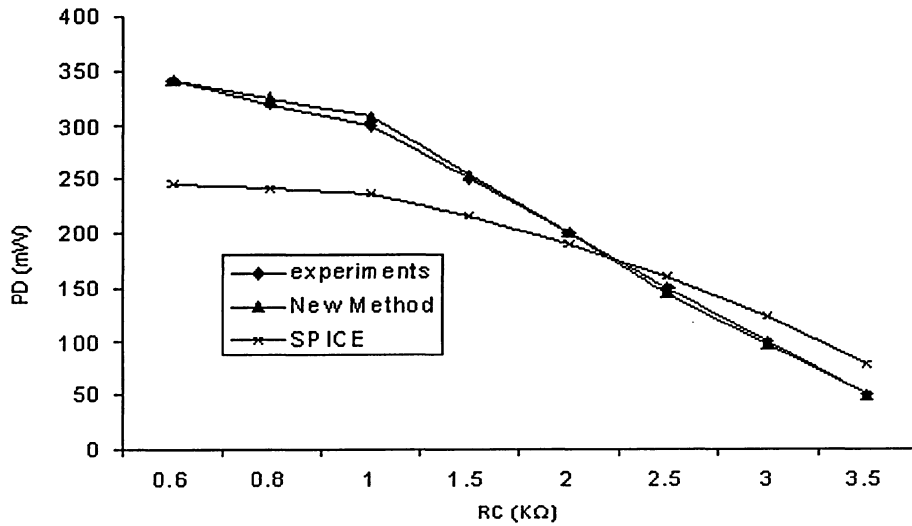


Figure 7.14: Power dissipation variations of the compared methods versus variations of R_C .

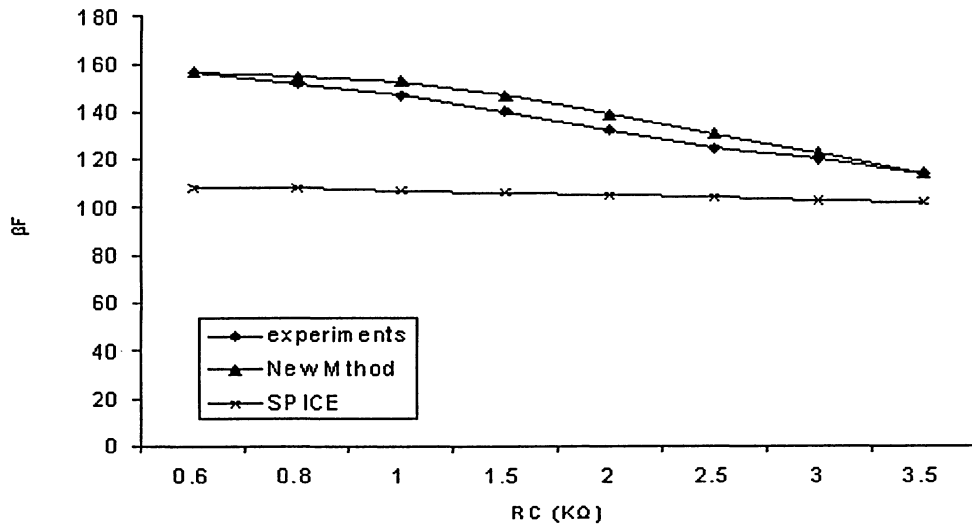


Figure 7.15: Current gain variations of the compared methods versus variations of R_C .

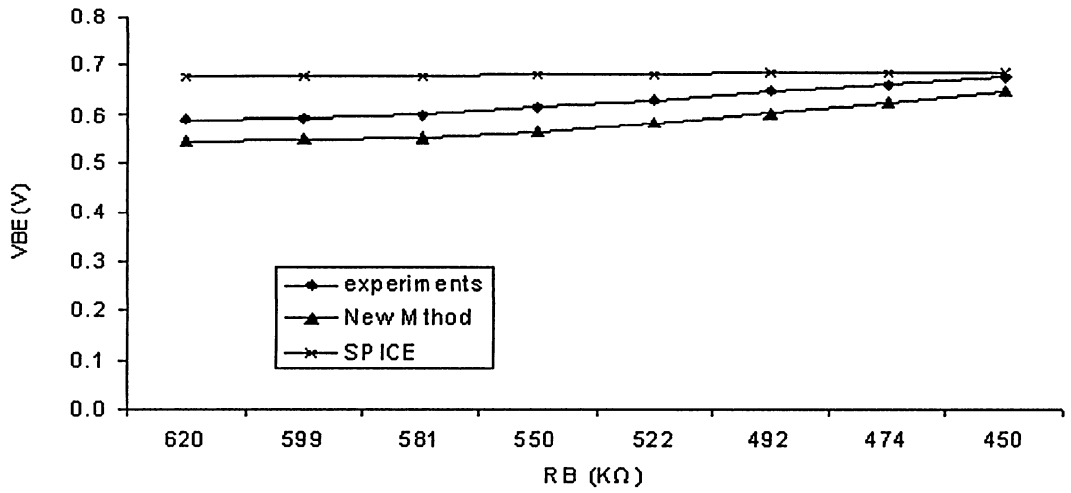


Figure 7.16: Base-Emitter voltage variations of the compared methods versus variations of R_C .

There are many advantages in the new method. 3D thermal simulation is performed in this method. It is able to consider temperature dependency of semiconductor thermal conductivity. Temperature distribution along the thermal model is presented.

7.3 BJT Current Mirror

To evaluate the transient performance of the proposed simulator in the presence of thermal coupling, a current mirror circuit was designed implementing NPN BJTs. This chapter will go through the results of this simulation.

7.3.1 Electrical Model

A current mirror circuit was developed in PSpice according to the circuit applied in [38]. Two 2N2222 Si BJTs from the PSpice library were implemented. BJT parameters were changed similar to section 7.2.1; therefore, GP saturation current was set to 0.03PA, the composite forward and inverse low saturation current were set to 0A. Base, Emitter and Collector ohmic resistance were set to 15Ω, 0.1Ω and 1Ω, respectively [32]. The forward

Beta value was selected 110 [32]. R_1 and R_2 were both equal to $2K\Omega$. The electrical model of the current mirror circuit is shown in Figure (7.17).

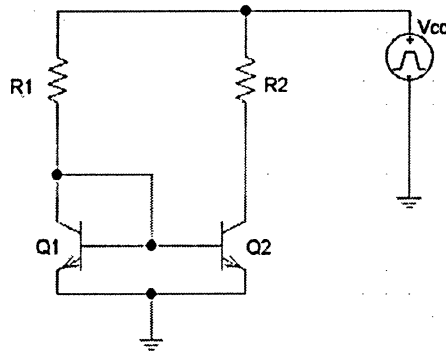


Figure 7.17: Implemented current mirror.

V_{cc} was switched from 0V to 40V at time $t = 0$ to be able to observe the step response of the system.

Numerical calculations showed that current flow in R_1 was 19.65mA and R_2 immediately followed the reference current with equal value.

7.3.2 Thermal Model

As explained in section 7.2.2 thermal model was consisted of die, die-attach and header. Two devices were located on a single die to model thermal coupling. Dimensions of die and die attach should be calculated according to the IC die datasheet. Dimensions of the header were estimated according to the device junction to case thermal resistance. TO-18 [41] was considered as the packaging of the device.

Thermal model is included 13300 solid elements, as shown in Figure (7.18).

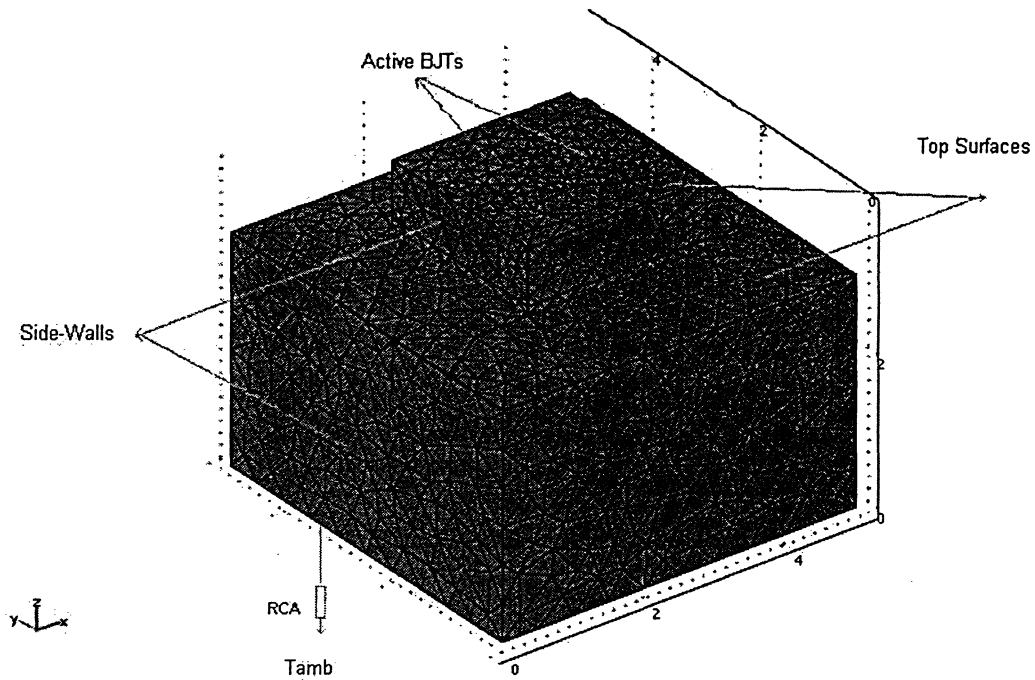


Figure 7.18: Finite element model of the current mirror.

Two active devices located on the die with dimensions of $60\mu m \times 60\mu m \times 10\mu m$ were the only heat sources in the model.

Table (7.7) illustrates the dimensions and the material properties of the thermal model.

Table 7.7: Material properties and dimensions of layers of the thermal model.

Layer	Material	ρ kg/m ³	Cp J/kgK	k W/mK	L (mm)	A (mm ²)	R _{th} K/W
Die	Silicon	2330	703	$ko \times \left(\frac{T}{300} \right)^{\left(\frac{-1}{3} \right)}$	0.75	0.0625	7.36
Die-Attach	97%Au-3% Si	15400	169	31.46	0.0125	0.0625	6.35
Header	Kovar	8359	430	17.3	0.3	0.25	69.36

The followings are the specified boundary conditions:

The top surface and the sidewalls were considered adiabatic, therefore:

$$-k(\nabla T) = 0 \quad (7.9)$$

A thermal resistance was considered at the backside with a value equals to the case to ambient thermal resistance, R_{CA} .

$$-k(\nabla T) = q = \frac{(T_{amb} - T)}{R_{CA} \times A_b} \quad (7.10)$$

7.3.3 Transient Simulation Specifications

There are two major factors that are very critical in a transient electrothermal simulation, the value of each time step and the convergence criterion.

Considering an electrical circuit, the time constant of the electrical network is smaller than 1 μ s while the thermal network time constant is greater than 100 μ s [45]. For the transient analysis of the current mirror, the time step was selected 100 μ s. It was a reasonable value since in each time step a steady state temperature was achieved for the particular steady state power dissipation.

Several numbers of iterations may need to be performed in each time step to achieve the convergence. For the current mirror transient electrothermal analysis, only two iterations were required to be executed in each time step to attain convergence. Nonetheless, in cases that there was no variation in the results of two consecutive iterations the time step was doubled. Increasing the time step indicated that variation of temperature and its effect on the electrical network was not significant anymore; therefore, time had to be increased. Enlarging the time step also reduced the simulation time.

As illustrated in Figure (6.1), a convergence test should be performed after each iteration. In this algorithm, the output current, I_{R2} , was selected as the convergence parameter, since the current values and its variations could be more accurately expected prior to the simulation than the other parameters. Therefore, the convergence criterion would be more reliable. The convergence condition was achieved when the newly calculated output current was smaller or equal to the current computed in the previous iteration or in case of the first iteration, the previous time step.

The maximum time was reached when the temperature variations of Q_2 was smaller than $1e-4$. This is due to the fact that the variations of T_{Q2} smaller than 0.01 had very small effect on the electrical performance of the circuit; therefore $1e-4$ was selected to be more conservative.

The initial start time was set to zero second. The start time of each time step was equal to the stop time of the previous time step. The stop time of each time step was equal to the start time of the particular time step plus the time step.

The initial temperature of the devices for the first time step was similar to the ambient temperature, 27°C . The initial temperatures of the devices after the first time step was set analogous to the previous time step.

7.3.4 Simulation Results

To have a general idea of the temperature distribution along the IC, a steady state thermal simulation was performed using COMSOL finite element solver. Device junction temperature was considered equal to the ambient; the power dissipation of each device was computed by PSpice. P_{Q1} and P_{Q2} were computed 13.77mW and 27.21mW, respectively.

The simulation results indicate that the maximum temperature is located at the junction of the device with the most power dissipation. Maximum junction temperature obtained 47°C and 48°C for Q_1 and Q_2 , correspondingly, as shown in Figure (7.19).

The results of the electrothermal simulator are illustrated in Table (7.8). The table indicates the variations of currents, temperatures and power dissipations of the devices in each time step. Eight time steps were totally executed to reach the circuit steady state.

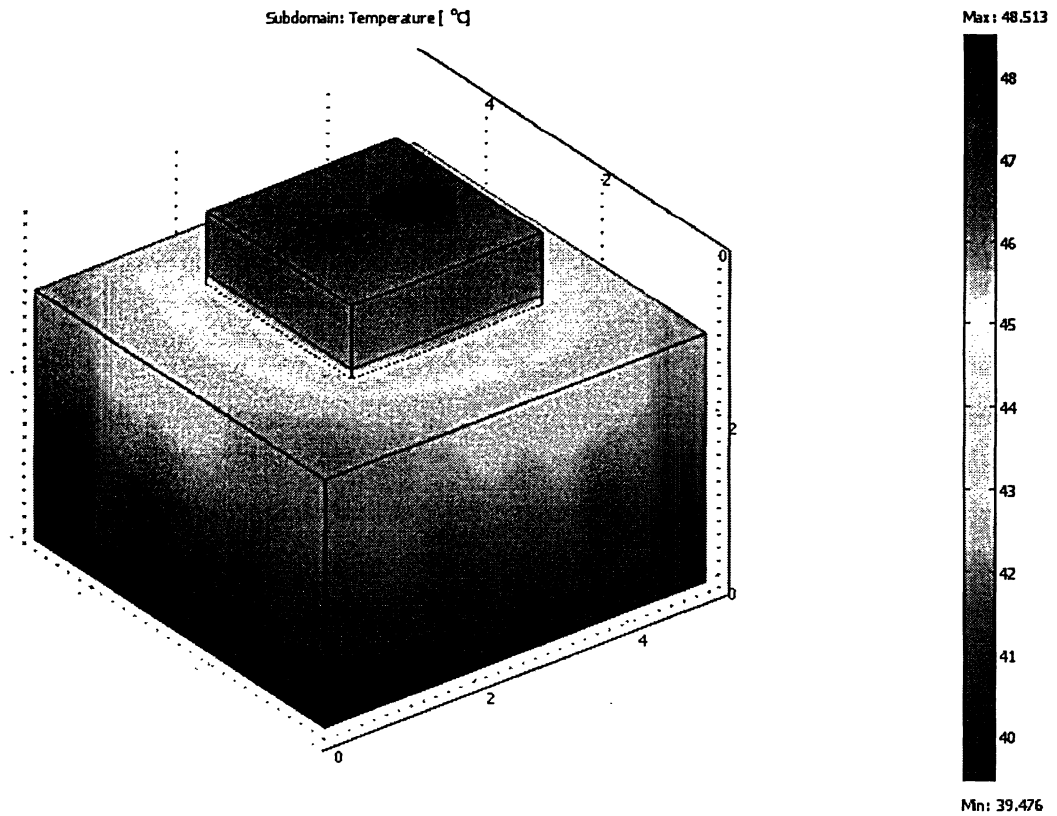


Figure 7.19: 3D temperature distribution across the current mirror thermal model.

Table 7.8: Results of the transient simulation of the current mirror.

No. of Time Steps	<u>0</u>	<u>1</u>	<u>2</u>	<u>3</u>	<u>4</u>	<u>5</u>	<u>6</u>	<u>7</u>	<u>8</u>
Time(s)	0	0.0001	0.0002	0.0003	0.0004	0.0005	0.0015	0.0137	0.4103
$I_{R1}(A)$	0.01965	0.01965	0.01965	0.01965	0.01965	0.01965	0.01965	0.01965	0.01965
$I_{R2}(A)$	0.01930	0.01938	0.01942	0.01944	0.01945	0.01946	0.01947	0.01948	0.01949
$T_{Q1}(C)$	27	28.147	28.643	29.01	29.301	29.539	29.993	32.998	43.31
$T_{Q2}(C)$	27	28.235	28.774	29.162	29.462	29.706	30.168	33.174	43.518
$P_{Q1}(W)$	0.01377	0.01374	0.01372	0.01371	0.01371	0.01370	0.01368	0.01359	0.01327
$P_{Q2}(W)$	0.02721	0.02404	0.02253	0.02177	0.02138	0.02116	0.02087	0.02058	0.01986

Table (7.8) illustrates that temperature and as its results the output current varies considerably in the first five time steps; however, after the 5th time step time increments are not equal. This indicates that time step doubling was occurred during the simulation due to small temperature variations. The electrothermal simulator recorded the required parameters each time temperature variations changed the electrical parameters; therefore, there was no more data available among the last three time steps. Even though it seems that temperature raised suddenly among the last three time steps, its variations by time was much smaller than the first five time steps. For instance, in case of T_{Q2} , temperature increased 2.7 °C in the first 0.0005s while it increased only 0.46 °C between 0.0005s and 0.0015s; consequently temperature variations decreased considerably after the first 0.0005s. Since variations of the temperatures decreased after the 5th time step, their effects on the electrical parameters of the circuit also decreased; until the circuit reached its steady state. As illustrated in the Table (7.8), variations of the other parameters also decreased after the fifth iteration.

The simulation took 40 minutes to accomplish using a Pentium 4 CPU, 2.80GHz, and 512 MB of RAM.

The variation of the devices temperature, current and power dissipations are shown in figures (7.20), (7.21), (7.22) and (7.23) for the first 500 μ s. The temperatures-time curves of the active BJTs are shown in Figure (7.20). It can be observed that the two devices had similar temperature during the simulation due to thermal coupling between them.

Figure (7.21) depicts variations of I_{R1} with time. It shows that the reference current was constant during the simulation. This is due to the fact that the transistors were thermally coupled and the collector of Q_1 was also electrically connected to the base of Q_2 ; therefore, the collector current of Q_1 depended on the temperature difference between Q_1 and Q_2 , which is almost zero according to Figure (7.20) [21].

Figure (7.22) indicates the variations of the output current with time. In contrary to theory, I_{R2} followed I_{R1} with delay and the final value was not mirroring the reference current. The variations of I_{R2} were very similar to the temperature variations, since the collector current of Q_2 depended on the changes of the device junction temperature [21, 38].

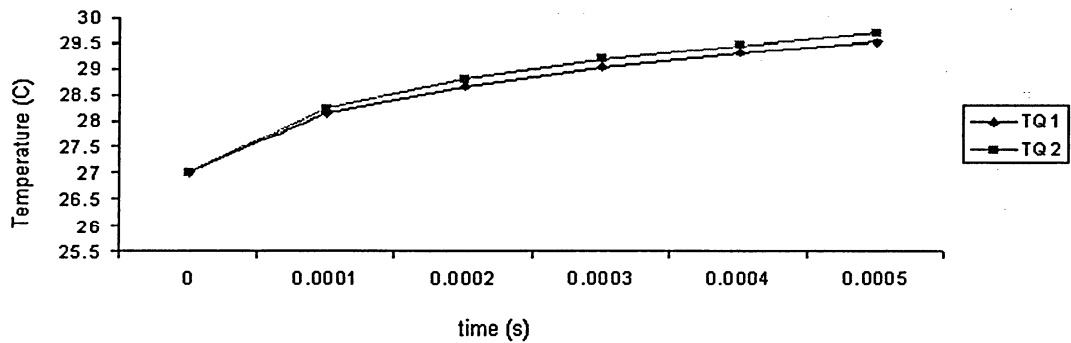


Figure 7.20: Temperature variations of the active devices over time.

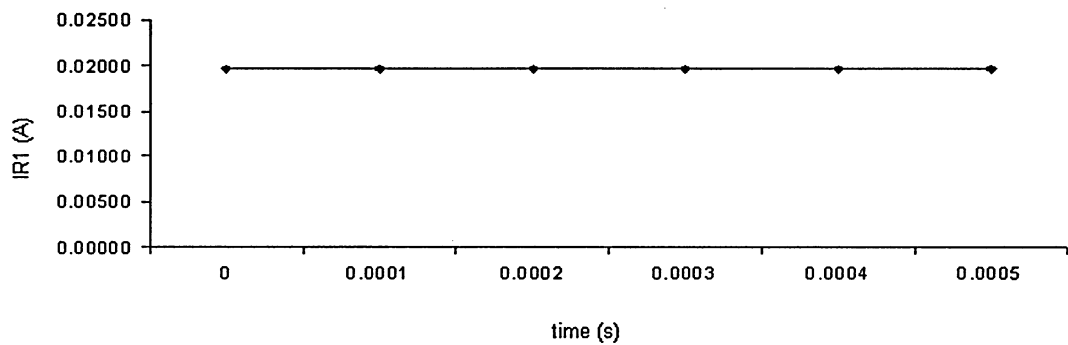


Figure 7.21: Variations of the reference current over time.

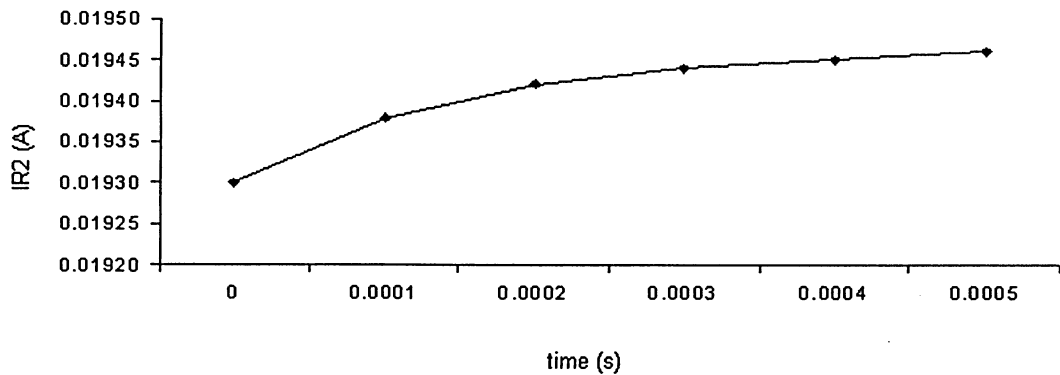


Figure 7.22: Variations of the output current over time.

Figure (7.23) shows the power variations over time. In contrary to the active BJT in section 7.1, power dissipation of Q_1 and Q_2 did not increase by temperature. This is due to the fact that the power dissipations were very small, in the range of mW, which resulted in

very small temperature variations. For instance, the power dissipation of the active BJT was in the range of 2W to 4W and its junction temperature varied in the range of 27°C to 107°C, while in case of Q_2 , it had the maximum power dissipation of only 27mW and the maximum junction temperature was only reached to 43°C. Clearly, temperature increase in the active BJT is much larger than the current mirror. Therefore, in the current mirror temperature increase was not the primary factor to determine P_{Q1} and P_{Q2} . In fact the resistors were the main elements that determined the power dissipations. In case of Q_1 , since there was no current variation, P_{Q1} was constant. P_{Q2} decreased because R_2 was constant and it was the major factor of establishing the power dissipation. As I_{R2} increased, since R_2 was constant, the collector voltage of Q_2 (V_{C2}) decreased. Since reduction of V_{C2} was greater than increase of I_{R2} , P_{Q2} decreased. For example, in the first time step when I_{R2} changed from 0.0193A to 0.01938A, V_{C2} changed from 1.4V to 1.24V, hence P_{Q2} was reduced from 27.02mW to 24.031mW, neglecting base power dissipation.

Despite the fact that temperature variations were small with time, the time duration of the temperature to reach its steady state value affected the transient performance of the electrical parameters.

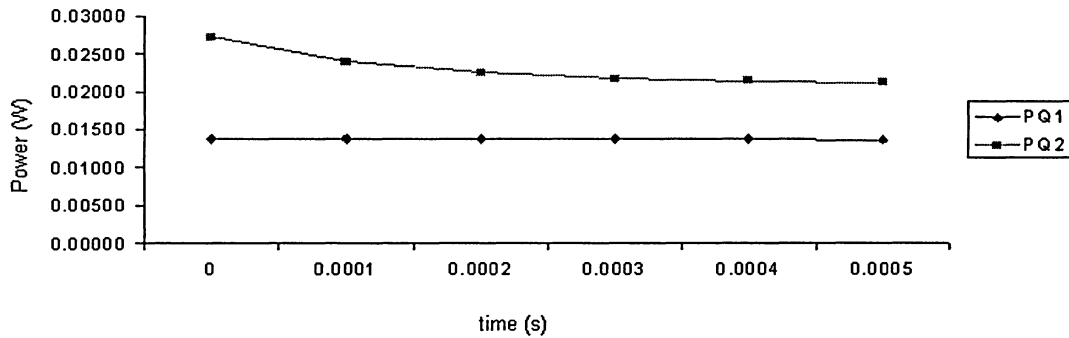


Figure 7.23: Variations of the power dissipations of the active devices by time.

7.3.5 Constant Time Step Effect

As demonstrated above, variations of the Q_1 parameters are very small and negligible; so our main focus is on Q_2 .

To be able to demonstrate the exact behavior of the Q_2 parameters all time steps must be equal, which means that we should not double the time steps even if there is no variation or there is small variations in the junction temperature. Selecting equal time steps highly increases the simulation time. Such a simulation was performed considering all time steps equal to $100\mu\text{s}$. The simulation took 14 hours to accomplish using the same machine as described earlier. Most of the time was consumed by COMSOL to solve the FE thermal model.

Even though more data was obtained this time, similar outcomes were resulted. Figure (7.24) illustrates the variations of temperature over time while time steps were equal. As expected, major variations were in the first $500\mu\text{s}$. Although temperature varied after $500\mu\text{s}$, the variations were very smooth and did not significantly affect the electrical performance.

Figure (7.25) depicts the output current variations over time obtained from the similar simulation. Similar to temperature the output current varied significantly until $500\mu\text{s}$; however, it remained constant for more than 0.012s . This is due to the fact that temperature variations were not large enough to influence the electrical performance of the circuit. After 0.0132s a small variation was occurred, and the current became constant again. There was another change at 0.0241s , after which the current reached its steady state. If the time step was doubled, the data repetition would be prevented and simulation time would be reduced considerably.

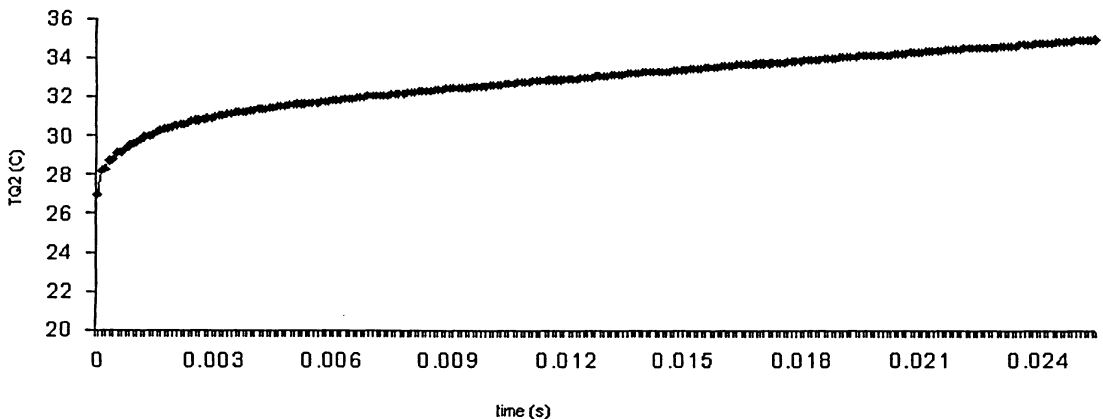


Figure 7.24: Variations of TQ_2 versus time while time steps were equal.

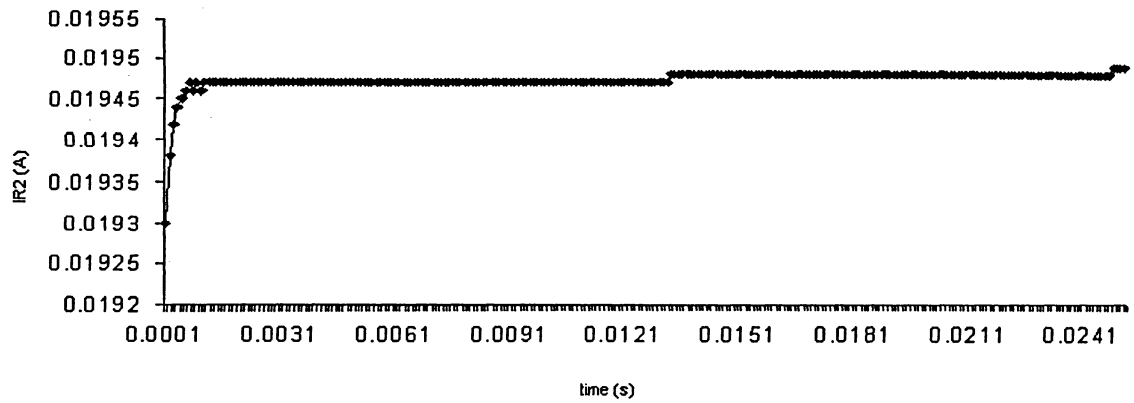


Figure 7.25: Variations of I_{R2} versus time while time steps were equal.

As shown in the figures (7.24) and (7.25), the variations of the output current and the temperature are very small as time increases.

To be able to show similar results implementing the time efficient version of the electrothermal simulator, the variations of T_{Q2} and I_{R2} over the variations of time, $\Delta I_{R2}/\Delta t$ and $\Delta T_{Q2}/\Delta t$, are represented in Figure (7.26) and Figure (7.27), respectively. These figures confirm that temperature and current variations became smooth as time increased. In both curves the variations of T_{Q2} and I_{R2} were significant in the first 500 μ s; nevertheless, it decreased notably after the 5th time step.

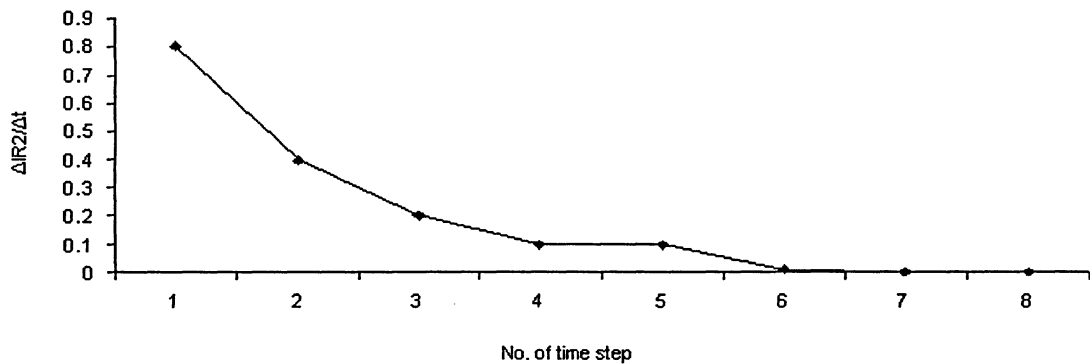


Figure 7.26: Variations of the output current over variations of time versus No. Of time step .

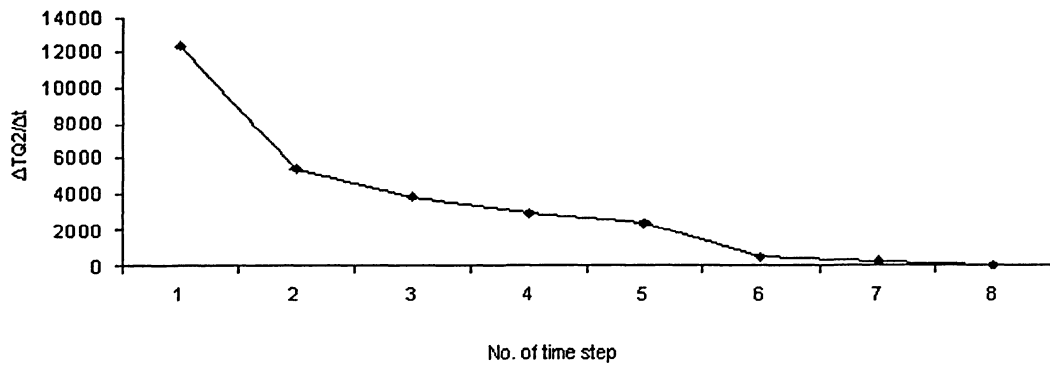


Figure 7.27: Variations of the T_{Q2} over variations of time versus No. of time step.

7.3.6 Validation of Electrothermal Simulator

The simulation results were compared to the results obtained by the electrothermal simulators designed by Shelar et. al [21] and Wunsche et. al [38].

Shelar et. al performed a DC analysis on a similar current mirror and compared the results to the results obtained by measurement as reported in Table (7.9). In case of $R_1 = 2K\Omega$ the reference current was obtained 19.6mA and the output current was obtained 19.4mA, by experiment. The steady state values of I_{R1} and I_{R2} obtained from the developed simulator were computed 19.65mA and 19.49mA, respectively. This indicates a better agreement between the developed simulator and experimental results.

Table 7.9: Experimental results, and Munro et. al and Shelar et. al's results of the current mirror.

$R_1=2 K\Omega$	I_{R1} (mA)	I_{R2} (mA)
Experiment	19.6	19.4
Shelar et. al's simulation	19.6	19.6
Developed simulator	19.65	19.49

Wunsche et. al [38] performed a transient simulation on the current mirror, the results of which are presented in Figure (7.28a-c). The comparison shows very similar behavior between the results of the two simulators. Similar to the obtained results from our simulation,

Figure (7.28a) shows equal temperature for both transistors during the simulation. It illustrates that temperature increased significantly for 500 μ s and reached its steady state after 750 μ s. The trends of the temperature variations are very close to our results. Figure (7.28b) shows that the reference current immediately reached its steady state value. Figure (7.28c) shows that the maximum variations of the output current occurred in the first 500 μ s and flattened after that until it reached its steady state value. Nevertheless, the current values demonstrated on both Figure (7.28b) and Figure (7.28c) do not show the correct amount. The reference current is close to 1.96mA and the output current steady value is close to 1.969mA. This may be due to typing problems. However, even if it is typing difficulties, our results are more improved than Wunsche et. al's results according to Table (7.9).

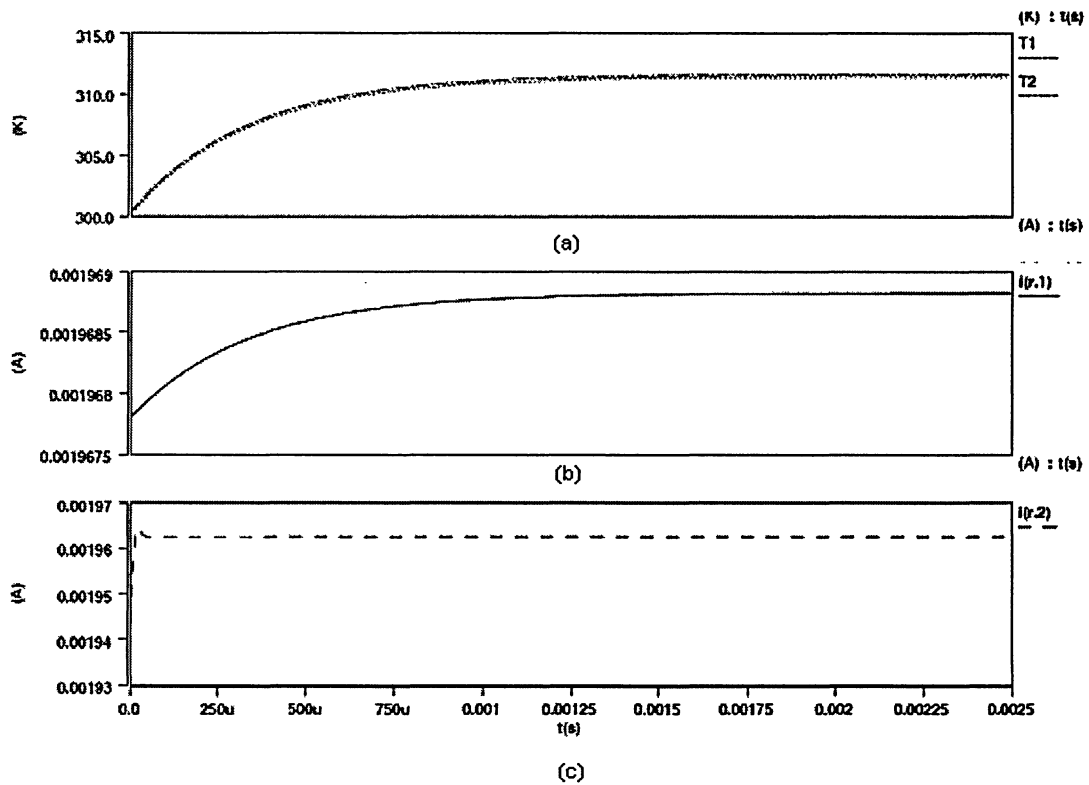


Figure 7.28: Wunsche et al's a)Temperature, b)Output current and c) Reference current simulation results [38].

A disadvantage of Wunsche et.al's method according to [38] is that a MAST model could not initiate a previously calculated time step therefore, only one iteration was performed in

each time step. Even though it is an advantage that only one iteration is performed, the important disadvantage is that another error control should be applied which reduced the simulator accuracy. As a result, the simulator might not be able to recognize the small variations occurred after $750\mu\text{s}$ so the total calculation time was reduced when no variation could be detected. The computation time in Wunsche et. al's work was 2.5ms while it reached to 0.4s in our simulation.

Another disadvantage of Wunsche et. al's work is that it took four hours to attain the total calculation time of 2.5ms, while the proposed method accomplished the same calculation time of 2.5ms in a matter of few minutes. This is more essential when we know that the number of finite elements in the proposed method was approximately 13300 while [38] contained only 600 finite elements. The higher is the number of elements, the more accurate is the thermal simulation.

Another disadvantage of [38] is that its simulator structure is very complex compare to our simulator. In our simulator the user needs to be familiar with MATLAB coding and some knowledge of PSpice and COMSOL, while [38] not only required expertise with SABER and ANSYS, but also the user should know three major programming languages, FORTRAN, C and MAST.

By and large, the proposed method is more time efficient, more accurate and more user friendly than Wunsche et. al's work.

7.4 Summary

The electrothermal simulator was employed to investigate the thermal effects in an active BJT, operational amplifier circuit and current mirror circuit. The results obtained from simulation were compared to the available experimental results to validate the accuracy of the electrothermal models.

First the simulator was applied on a simple BJT biasing circuit. A thermal model has been developed to study the thermal behavior of the device. The simulation results were obtained as it was expected from theory. According to the results the device power dissipation

increased as the device junction temperature increased until they converged to some steady state values.

The second simulation was performed on a BJT amplifier. Several DC electrothermal simulations were executed on the amplifier, implementing different values for the collector and base resistors. Results from the electrothermal model of the circuit provided data on the several variables such as power dissipation, collector current, Base-Emitter voltage and current gain that compared very well to experimental data. The results showed that the PSpice simulation results had the maximum error of 58% in case of device power dissipation while the electrothermal simulation results had the maximum error of only 4%.

Finally, a transient electrothermal simulation was applied on a current mirror circuit. The model was more complex than the previous simulations since thermal coupling was added to the self heating and global heating. There were good agreements among simulation results, literature results and experimental results. The results showed that the output current reached its steady state value with delay and it did not mirror the reference current. Evaluation of the model showed that it was computationally stable, reliable and repeatable.

Chapter 8

Conclusion and Future Work

In this thesis a new electrothermal simulator has been introduced. The simulator is based on the relaxation method. COMSOL, which is based on finite element method (FEM), has been applied as the thermal simulator. It has the ability to manage material nonlinearity of semiconductors and complex geometries. PSpice has been selected as the electrical simulator, which is based on the SPICE model of devices. These simulators have been coupled using an interface program developed in MATLAB. Two functions named *Reading* and *Writing* have been developed in MATLAB to read the power dissipation from PSpice and to write the calculated temperature by COMSOL into PSpice. The electrothermal simulator is capable of performing DC, AC and transient analyses. To evaluate the simulator, transient analyses was performed on an active BJT and a current mirror and a DC analysis was applied on a BJT amplifier.

The electrothermal analysis on an active BJT was implemented while only self heating and global heating was considered. Since only one BJT was active during the simulation, no thermal coupling was considered. The results indicated that the device junction temperature increased in each time step until it reached its steady state value. The power dissipation of the BJT had similar behavior as the temperature. It increased with temperature and gained a constant value when temperature reached its steady state. The results showed that temperature increased from 27°C to 107°C and the power dissipation was raised from 1.83W to 4.5W. Increase of the junction temperature affected the device operating point, as well. Considering a constant collector-emitter voltage, the collector current varied from 183mA to 450mA.

A DC analysis was performed on a BJT amplifier. The steady state values of the power dissipation, collector current, base-emitter voltage and current gain were computed for different base and collector resistances and were compared to the experimental measurements and PSpice-only simulation. The results indicated good agreements between the simulation and the experiment. The simulation results were significantly improved compare to PSpice results. The maximum error obtained by the electrothermal simulator was 4% while it was 58% in PSpice for the power dissipation. The collector current value had the maximum error of 5% and 31.5% obtained by the electrothermal simulator and PSpice, respectively. Same improvement was attained for the base emitter voltage and the current gain. The maximum errors for the base emitter voltage and the current gain were calculated 8.1% and 5.3% correspondingly by the electrothermal simulator, while they were 14.7% and 31.2% likewise in PSpice.

Transient analysis was performed on a current mirror considering thermal coupling in addition to the self heating and global heating. Transient performance of the temperatures and the power dissipations of the BJTs and the reference and the output currents were investigated. The electrothermal simulation results indicated that temperatures increased by time and the devices had similar temperatures during the simulation. The temperatures varied significantly for the first 500 μ s and flattened after that until it reached to a steady state value by 0.4s. The investigation showed that the reference current reached its steady state value from the beginning nonetheless, the output current reached steady state value with delay and the final value was not mirroring the reference current. These variations were also increased considerably for the first 500 μ s. The power dissipation of the reference transistor was constant similar to its current whereas the power dissipation of the output transistor decreased by time. The steady state values of the currents were compared to the experimental results and a good accordance was among them. The transient behavior of the parameters was also compared to some other results obtained from literature and similar performance was observed. Evaluation of the models showed that they were computationally stable, reliable and repeatable.

In general, by this work we would like to emphasize on the importance of performing electrothermal simulation on VLSI circuits. It has been shown that thermal issues are critical and must be considered during their early design phase. They indicate that considering self

heating, global heating and thermal coupling can dramatically change the circuit performance. The simulation results indicate that the electrothermal simulator can quickly find the temperature profile of the chip.

Although the simulation time to perform an electrothermal analysis is greater than an electrical-only analysis, much more accurate evaluation of the circuit performance can be obtained at the end.

Hopefully in the future applying the electrothermal simulator, we would like to perform more evaluation on the simulator by comparing its results to more experimental results and improve its efficiency. We would also like to present more detail analyses of internal structure of the semiconductor devices by including the circuit metal interconnects and analyze the temperature distribution along them. We are also interested in performing electrothermal simulation on bipolar transistors, BJTs and HBTs (Heterojunction Bipolar Transistors) by applying different types of semiconductors such as Silicon Carbide (SiC) and Gallium Arsenide (GaAs), which have different thermal conductivities, and evaluate their performances.

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