TIME-INTERLEAVED PULSE-SHRINKING AND ALL-DIGITAL $\Delta\Sigma$ TIME-TO-DIGITAL CONVERTERS

by

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ABSTRACT

Young Jun Park
Time-Interleaved Pulse-Shrinking and All-Digital $\Delta\Sigma$ Time-To-Digital Coverters
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This dissertation deals with the design of sub-per-stage-delay time-to-digital converters (TDCs). Two classes of TDCs namely pulse-shrinking TDCs and $\Delta\Sigma$ TDCs are investigated.

In pulse-shrinking TDCs, a two-step pulse-shrinking TDC consisting of a set of coarse and fine pulse-shrinking TDCs is proposed to increase a dynamic range without employing a large number of pulse-shrinking stages. A residual time extraction scheme capable of extracting the residual time of the coarse TDC is developed. The simulation / measurement results of the TDC implemented in an IBM 130 nm 1.2 V CMOS technology show that the TDC offers 1.4 ns conversion time, 1 LSB DNL and INL, and consumes 0.163 pJ/step. To further improve the conversion time, a time-interleaved scheme is developed to extract the residual time of the coarse TDC and utilized in design of a two-step pulse-shrinking TDC. Residual time extraction is carried out in parallel with digitization to minimize latency. The simulation and measurement results of the TDC show that it offers 0.85 ns conversion time, 0.285 LSB DNL, and 0.78 LSB.

In $\Delta\Sigma$ TDCs, a 1-1 multi-stage noise shaping (MASH) $\Delta\Sigma$ TDC with a new differential cascode time integrator is proposed to suppress even-order harmonic tones and current mismatch-induced timing errors. Simulation results show that the proposed TDC offers 1.9 ps time resolution over 48-415 kHz signal band while consuming 502 μW. Finally, an all-digital first-order $\Delta\Sigma$ TDC utilizing a bi-directional gated delay line integrator is developed. Time integration is obtained via the accumulation of charge of the load capacitor of gated delay stages and the logic state of gated delay stages. The elimination of analog components

allows the TDC to benefit fully from technology scaling. Simulation results show that the TDC offers first-order noise-shaping, 10.8 ps time resolution while consuming 46 μW.

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List of Symbols and Abbreviations

$\Delta\Sigma$	Delta-sigma
ADC	Analog-to-digital converter
$ADPLL$	All-digital phase-locked loop
$BSIM$	Berkeley Short-channel IGFET Model
CDR	Clock and data recovery
$CMOS$	Complementary Metal-Oxide Semiconductor
DAA	Digitally assisted analog
dB	Decibel
DCO	Digitally controlled oscillator
DFF	D-type flip-flop
DNL	Differential nonlinearity
DR	Dynamic range
DTC	Digital-to-time converter
$ENOB$	Effective number of bits
FFT	Fast Fourier transform
FoM	Figure-of-merit
GDC	Gated delay cell
GDL	Gated delay line

GRO	Gated ring oscillator
Hz	Hertz
INL	Integral nonlinearity
KHz	KiloHertz
LSB	Least significant bit
$MASH$	Multi-stage noise-shaping
MHz	MegaHertz
MIM	Metal-insulator-metal
MSB	Most significant bit
MUX	Multiplexer
$NMOS$	n-type metal oxide semiconductor
NTF	Noise transfer function
$OPAMP$	Operational amplifier
OSR	Oversampling ratio
OTA	Operational transconductance amplifier
PFD	Phase frequency detector
PLL	Phase-locked loop
$PMOS$	p-type metal oxide semiconductor
PSD	Power spectral density
PVT	process, voltage, and temperature
SNR	Signal-to-noise ratio
$SNDR$	Signal-to-noise-plus-distortion ratio
$SPICE$	Simulation program with integrated circuit emphasis

SRO	Switched ring oscillator
STF	Signal transfer function
TDC	Time-to-digital converter
$VCDU$	Voltage controlled delay unit
VTO	Voltage controlled oscillator
VTC	Voltage-to-time converter

Chapter 1

Introduction of Time-Mode Signal Processing

The rapid scaling of CMOS technology has resulted in the sharp increase of time resolution and the continuous decrease of voltage headroom. As a result, time-mode circuits where information is represented by the time difference between two rising edges of pulses rather than the nodal voltages or branch currents of electric networks offer a viable and technology friendly means to combat scaling-induced difficulties encountered in design of mixed-mode systems. A time variable possesses a unique duality characteristic. Specifically, it is an analog signal as the continuous amplitude of the analog signal is represented by the difference between two rising edges of the pulses and it is also a digital signal as it only has two largely distinct values. The duality of time variables enables them to conduct analog signal processing in a digital environment. This unique characteristic is not possessed by neither analog nor digital variables. Since information to be processed by time-mode circuits is represented by the time difference of digital signals, these circuits are essentially digital systems and perform mixed-mode signal processing in digital domain without using power-greedy digital signal processing (DSP) blocks. This chapter examines the fundamentals of time-mode circuits. The intrinsic advantages of time-mode signal processing are examined in Section 1.1. The challenges encountered in time-mode signal processing are examined in Section 1.2. Section 1.3 provides an overview of time-to-digital converters (TDCs), the most important building block of time-mode systems. Section 1.4 presents the motivation of this dissertation. Primary contributions of this dissertation is in Section 1.5. Dissertation organization is detailed in Section 1.6. Finally, the chapter is concluded in Section 1.7.

1.1 Why Time-Mode?

The performance of analog circuit continues to fall behind the rapid scaling of CMOS technologies mainly optimized for digital circuits. Digitally assisted analog (DAA) circuits have been used to leverage digital circuits to improve the performance of analog circuits by adjusting the parameters of analog circuits so as to meet design specifications. The addition of DAA circuits, however, has a detrimental impact on the performance of analog circuits such as increasing the capacitance of the critical nodes through which high-frequency signals propagate. The intrinsic gate delay of digital circuits, on the other hand, has been the primary beneficiary of technology scaling. The improved switching characteristics of MOS transistors offer an excellent timing accuracy such that the time resolution of digital circuits has well surpassed the voltage resolution of analog circuits implemented in nano-scale CMOS technologies. Since time-mode circuits perform analog signal processing in the digital domain, not only the performance of these circuits scales well with technology, time-mode circuits also offer a number of attractive characteristics including full programmability, the ease of portability, and high-speed operation. As information to be processed by time-mode circuits is represented by the time difference between the occurrence of digital events, time-mode circuits are essentially digital circuits. The detrimental effect of technology scaling on the performance of voltage-mode or current-mode analog signal processing vanishes in time-mode circuits. The full programmability of time-mode circuits, attribute to their digital realization, allows them to be deployed in a broad spectrum of applications where tunable characteristics are mandatory. In addition to programmability, portability is of a critical importance in order to minimize design turn-around time. The digital nature of time-mode circuits allows them to be migrated from one generation of technology to another with the minimum design time subsequently the lowest cost. As the intrinsic gate delay of digital circuits benefits the most from technology scaling, time-mode circuits are capable of carrying out rapid signal processing.

1.2 Challenges in Time-Mode Signal Processing

Although it is evident from the preceding investigation that time-mode signal processing possesses many desirable characteristics such as excellent scalability with technology, full programmability, the ease of portability, and high-speed operation, a number of challenges are yet to be overcome in order for time-mode circuits to be deployed in a broad range of applications. One of the most challenges in time-mode signal processing is the design of time-mode arithmetic units, especially time integrators. The integration of a variable in the voltage domain can be conveniently realized by representing the variable as a current and integrating the current onto a capacitor. Withholding or storing a time variable, however, is difficult due to the irretrievable nature of time. To implement time integrators, time-mode arithmetic units such as time adders and time registers are critically needed in time-mode signal processing.

1.3 An Overview of TDCs

TDCs that map a time variable to a digital code are the most important building block of time-mode systems. Although the applications of TDCs in high-energy physics for time-of-flight measurement in nuclear science dates back to 1970s [12], the deployment of TDCs in analog-to-digital converters (ADCs) [13, 14, 15, 8, 16] and all-digital phase-locked loops (ADPLLs) [17, 18] emerged recently. TDCs can be loosely classified into sampling TDCs and noise-shaping TDCs. A sampling TDC digitizes a time variable using either a high-frequency low-jitter reference clock and counting the number of the cycles of the clock within the duration of the time variable or a delay line to count the number of the stages of the delay line that the front edge of the time variable propagates before the arrival of the rear edge of the time variable directly. Sampling TDCs include delay-line TDCs, vernier delay-line TDCs, and pulse-shrinking TDCs, to name a few. A one-to-one mapping between a time input variable and a corresponding output digital code exists in sampling TDCs since for each time variable, there is a corresponding digital code generated by sampling TDCs. The resolution of these TDCs is bound by quantization noise.

Noise-shaping TDCs, on the other hand, suppress the quantization noise of TDCs using system-level techniques such as $\Delta\Sigma$ operations that are capable of moving most of in-band quantization noise to higher frequencies outside the signal band so that the displaced excessive quantization noise can be removed effectively using a decimation low-pass filter in a post-processing step, thereby achieving a large signal-to-noise ratio. As compared with sampling TDCs, noise-shaping TDCs offer the key advantage of a better signal-to-noise ratio (SNR). An example of noise-shaping TDCs is gated ring oscillator (GRO) TDCs that possess first-order noise-shaping obtained by freezing the residual phase of one sampling phase and ported it over to the next phase [13]. Although the in-band noise of noise-shaping TDCs is lower than quantization noise, one-to-one mapping between input time variables and their digital output codes is lost since the average of the output represents the input in $\Delta\Sigma$ operations.

1.3.1 Delay-line TDCs

Delay-line TDCs quantize a time variable using a delay line. The simplified schematic of delay line TDCs is shown in Fig 1.1. The signal, *Start*, is applied to the first delay cell and delayed through the buffer delay chains. Each buffer considered as a reference time difference ladder analogous to the reference resistor ladder in a flash ADC is comprised of two inverters which have the minimum propagation delay in a circuit usually. Each buffer chain is tapped to D input of each D-flip flop (DFF) which is used as a time comparator. The signal, *Stop*, is fed to the clock pins of all DFFs. Finally, the thermometric outputs of the DFFs are fed to a thermometer to binary decoder, not shown in the figure, generating digital codes. The conversion time of a TDC is the amount of the time that the TDC needs to complete the digitization of a time variable. The conversion time of the delay-line TDC is $T_{in}+\tau_{DFF}$ where τ_{DFF} is the clock-to-Q propagation delay of the DFFs. One of the main disadvantages of this architecture is that the time resolution is lower bound by per-stage propagation delay.

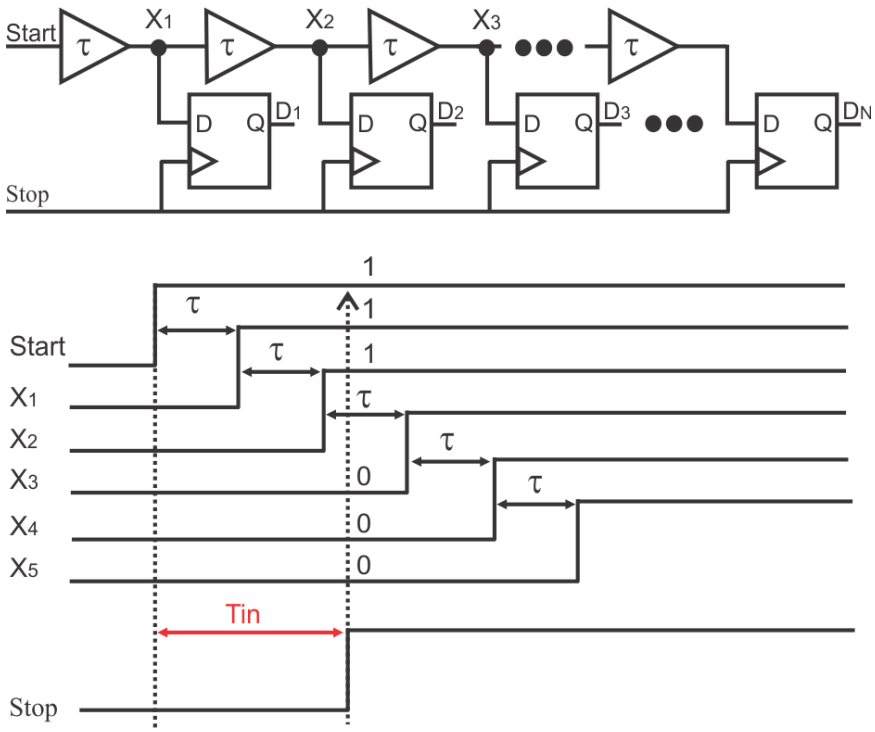

Figure 1.1: Delay-line TDCs [1], [2], [3].

1.3.2 Vernier delay-line TDCs

Vernier delay-line TDCs shown in Fig 1.2 are one of the older techniques that provide time resolution below per-stage delay. A vernier delay-line TDC adds an additional buffer delay chain having a different delay in the *Stop* path. In this case, the effective time resolution is the difference of the two propagation delays, $\tau_1 - \tau_2$, where τ_1 and τ_2 represent the propagation delay of the buffers in *Start* path and the one of the buffer in *Stop* path, respectively. Since τ_1 is designed to have larger delay then τ_2, *Stop* signal will catch up *Start* signal even though it is launched late. Because the difference between two delay lines is the effective time resolution, vernier delay-line TDC can have a much higher resolution than that of the basic delay-line TDCs shown in Fig 1.1. The time instant at which a catch-up takes place is determined from $T_{catch} = \mathrm{N}\tau_1 = \mathrm{N}\tau_2 + T_{in}$, where N is the number of the stages that *Stop* signal propagates though before the catch-up takes place. For a given T_{in}, we have $\mathrm{N} = \frac{T_{in}}{(\tau_1 - \tau_2)}$. Since $\tau_1 - \tau_2$ is very small, T_{in} must be small in order to have a manageable value of N. The dynamic range of vernier delay line TDCs is upper-bound by

N($\tau_1 - \tau_2$) and lower-bound by $\tau_1 - \tau_2$ theoretically. Improving time resolution is one of the biggest advantages of this architecture. Long conversion time is one of the disadvantages since the final thermometer output codes will be generated after *Stop* catches up *Start*. To increase a dynamic range, it requires many stages at the cost of increased silicon and power consumption.

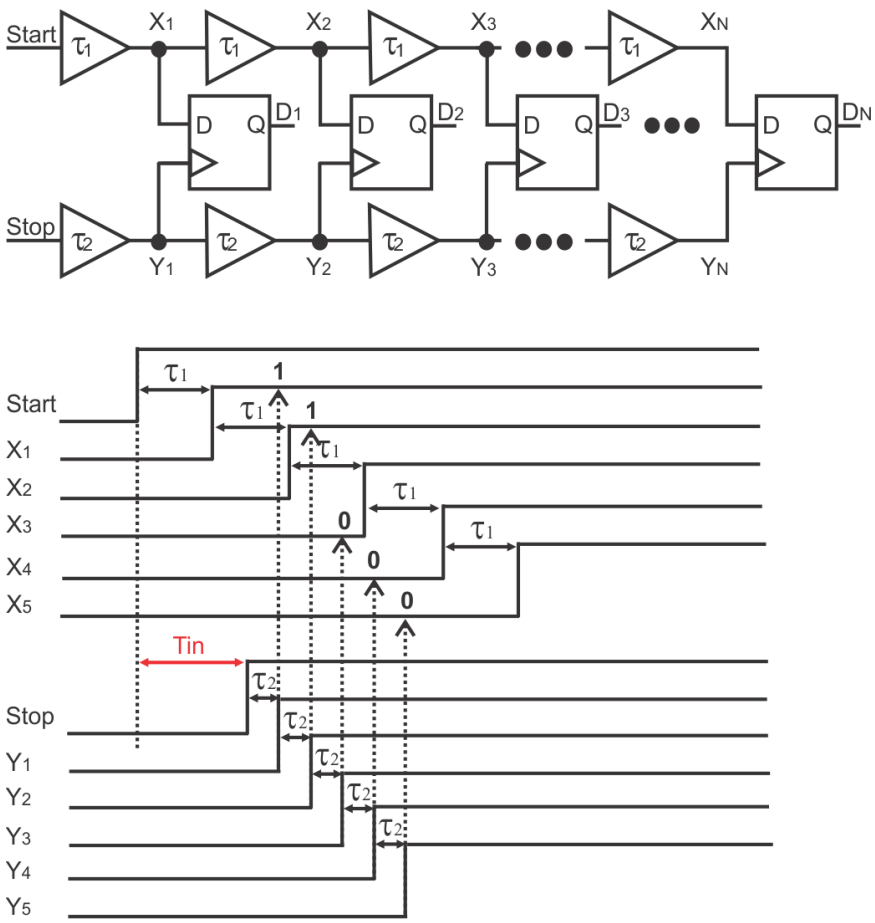

Figure 1.2: Vernier delay-line TDCs [4].

1.3.3 Hierarchical vernier delay-line TDCs

The conversion time of vernier delay-line TDCs can be reduced while preserving the resolution by using the 2-level hierarchical configuration shown in Fig.1.3[5]. Hierarchical

vernier delay-line TDC consists of a coarse vernier delay-line TDC with a total of N stages and N fine vernier delay-line TDCs. If τ_c and τ_f shown in Fig.1.3 represent the propagation delay of the buffers in coarse delay-line and the one of the buffer in fine delay-line, respectively, the conversion time of the coarse vernier delay-lines is Nτ_c. Since the digitization undertaken by the fine vernier delay-line TDCs is carried out in parallel with that by the coarse vernier delay-line TDC, the total conversion time of the hierarchical vernier delay-line TDC is the same as that of the coarse vernier delay-lines, i.e., Nτ_c. If we assume that τ_c can be resolved by the fine vernier delay-line TDCs with a total of M stages, τ_c= Mτ_f will hold. It should be noted that the price paid for reducing conversion time is the increased silicon area.

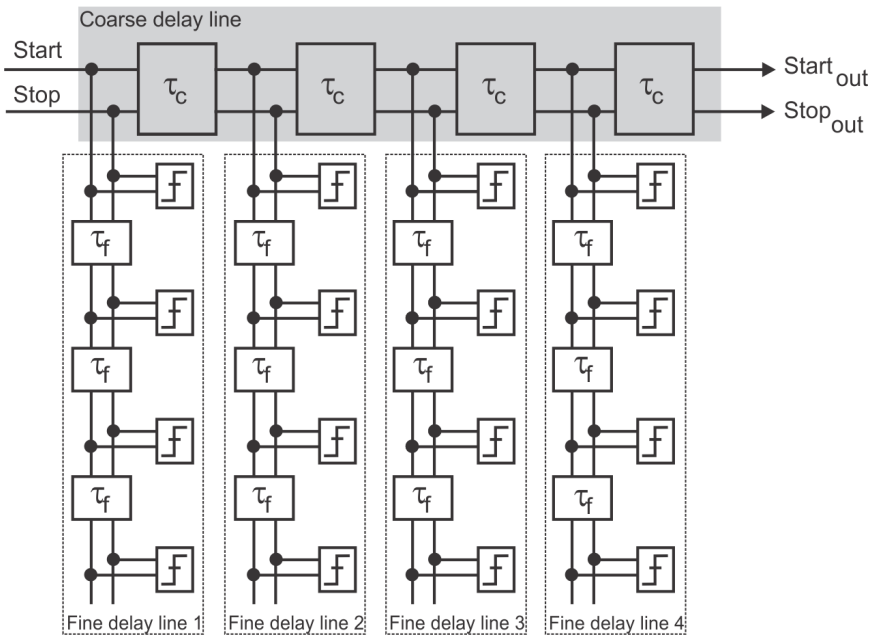

Figure 1.3: Hierarchical vernier delay-line TDC [5].

1.3.4 Pulse-shrinking TDCs

Resolution finer than per-stage delay can also be achieved using pulse-shrinking TDCs shown in Fig.1.4 [6, 7]. To set the resolution, V_c is set to V_{DD} and per-stage shrinkage is at the minimum. T_{cal} is then asserted. The width of T_{cal} is reduced stage-wise uniformly by ΔT.

ΔT is adjusted by V_c adjusting the discharge current J of the pulse-shrinking stages until the pulse at the output of the last stage just disappears ($D_M = 0$). Once this occurs, the resolution of the TDC becomes $\Delta T = T_{cal}/M$. M is the number of the pulse-shrinking stages. Clearly if M is sufficiently large, T_{cal}/M can be made arbitrarily small. By adjusting time resolution, calibration is also achieved. Increasing the number of pulse-shrinking stages, though improving resolution, is at the cost of increased silicon and power consumption. The detrimental effect of mismatches between pulse-shrinking stages deteriorates with the increase in the number of pulse-shrinking stages. The conversion range of the pulse-shrinking TDC is given by $\Delta T \leq T_{in} \leq \mathrm{N}\Delta T$ or $\Delta T \leq T_{in} \leq T_{cal}$. Although a large N is preferred from a better resolution point of view, the effect of jitter and mismatch intensifies with the increase in the number of the stages of pulse-shrinking TDCs, deteriorating the linearity of pulse-shrinking TDCs in a similar way as that in delay line TDCs.

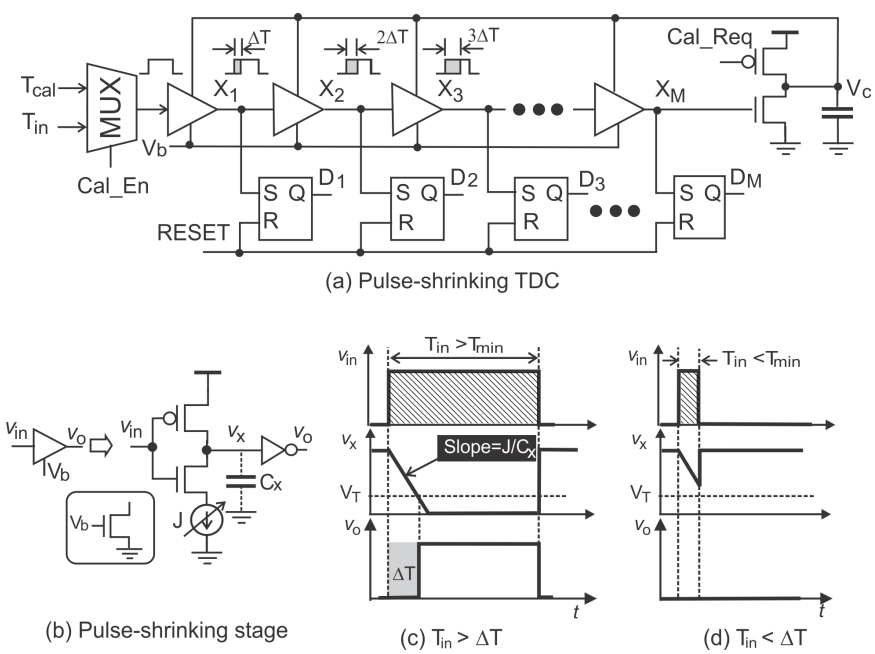

Figure 1.4: Pulse-shrinking TDCs [6, 7].

To improve the resolution of pulse-shrinking TDCs without employing a large number of pulse-shrinking stages, cyclic pulse-shrinking TDCs were proposed, as shown in Fig.1.5

[19]. A cyclic pulse-shrinking TDC consists of a delay line with stages $1, 2, ..., i-1, i+1, ...$ having the same dimension (homogeneous stages) and stage i having different dimensions (inhomogeneous stage), a control logic block, and a counter. The control logic is designed in such a way that when T_{in} is applied to the loop, the pulse will continue to circulate the loop until its width reduces to zero. The inhomogeneity of ith delay stage gives rise to a reduction in the width of the propagating pulse every time it completes a round trip. A counter is used to record the number of the round trips that the pulse completes before it diminishes. Since the number of the round trips that the pulse completes is directly proportional to T_{in}, the content of the counter when the pulse vanishes yields the digital representation of T_{in}. Cyclic pulse-shrinking TDCs exhibit a perfect linearity as the amount of cycle-to-cycle pulse shrinkage remains unchanged. In addition, they do not need to be calibrated periodically as the amount of pulse shrinkage is only set by the physical dimensions of the delay stages. One drawback of cyclic pulse-shrinking delay line TDCs is that an input pulse can be applied only after the previous one has vanished completely, resulting in a long conversion time.

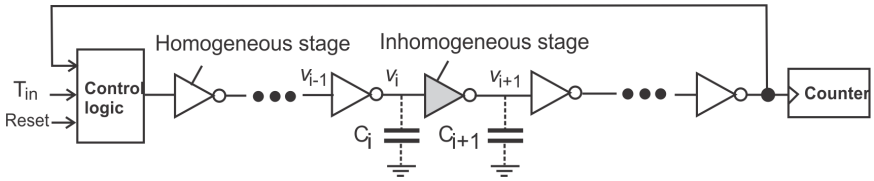

Figure 1.5: Cyclic pulse-shrinking TDCs.

1.3.5 Gated ring oscillator TDCs

GRO TDCs are one of popular noise-shaping TDCs. The TDC shown in Fig.1.6 (A) digitises time input T_{in} generated from two input signal, *Start* and *Stop*, by using a gated rign oscillator (GRO) [8]. The operation of GRO is depicted as follows: A GRO is similar to an ring oscillator (RO) except its delay stage has two additional transistors compared to the normal inverter. One is transistor between PMOS transistor and the positive power supply and the other is between NMOS transistor and the negative power supply. They act

like switches. Oscillation is enabled only when $T_{in} = 1$ and disabled when $T_{in} = 0$. The beauty of this structure is that when $T_{in} = 0$, the switch transistors are open. Oscillation is suspended and the phase of the oscillator remains unchanged until next T_{in}. The residue phase is transferred to the next T_{in}, i.e. $e_i[k] = e_f[k-1]$, where e_f[k] is a residue phase information in kT_s, and e_f[k-1] is a residue phase information in (k-1)T_s. Fig.1.6 (B) shows a waveform based on the basic operation of GRO. The quantization error can be calculated for a given measurement interval between kT_s and (k-1)T_s, T_{error} is given by

$$T_{error}[k] = e_f[k] - e_f[k-1]. \tag{1.1}$$

The first-order noise shaping of quantization noise is evident in (1.1). In addition to the first-order noise shaping of quantization noise, the effect of delay element mismatch is also first-order shaped. The randomness of the initial phase of each sampling period also effectively scrambles quantization error across different sampling periods so that it can be first-order shaped. The resolution of GRO TDCs is lower bound by the oscillation frequency of the ring oscillator of the TDCs, which is inversely proportional to the number of the delay stages of the oscillator. The quantization error of GRO TDCs given by π/N where N is the number of the stages of the oscillator is also inversely proportional to the number of the delay stages of the oscillator. The larger the number of the stages of the oscillator, the lower the quantization noise and the worse the resolution.

GRO TDCs suffer from missing count caused by the early reset of the counter at the end of T_{in} while the edge-detection and transition detection are still in action [20]. They also exhibit dead-zone behaviour if the period of the gating signal T_{in} is in the vicinity of an integer multiple of the period of the oscillator [21].

1.3.6 $\Delta\Sigma$ TDCs

It is well understood that $\Delta\Sigma$ operation offers noise-shaping. However, the realization of $\Delta\Sigma$ configurations in time-mode is rather difficult because of the lack of time-mode integra-

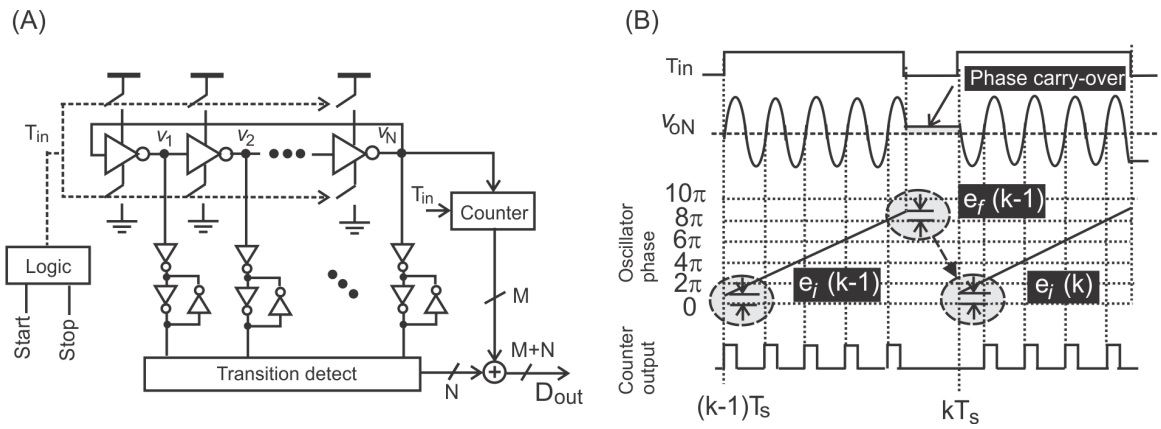

Figure 1.6: GRO TDCs [8]. (A) Block diagram. (B) Waveform.

tors needed to achieve high-order $\Delta\Sigma$ modulators. As a result, $\Delta\Sigma$ TDCs are often realized using a partial time-mode partial voltage-mode approach, more specifically, integrators using OTAs are voltage-mode while quantizers are voltage-controlled oscillator (VCO)-quantizers. Taillefer and Roberts proposed a ring oscillator voltage-to-time integrator consisting of two voltage-controlled delay units [22]. Implementing high-order integrators using this approach is rather difficult.

Fig.1.7(C) shows $\Delta\Sigma$ TDC using the time accumulator in [10]. Time accumulator is evolved from the time adder proposed in [9] shown in Fig.1.7 (A). The core of time accumulator is a time register using gated-delay cell (GDC) shown in Fig.1.7 (B) that holds an input time variable and releases the held time variable on the arrival of a triggering a signal, AWK. Time adder shown in Fig.1.7 (A) consists of two time-registers. The operation of the time register can be briefly depicted as follows: assume C_{L1} is fully charged initially, when IN_1 arrives, V_{mid1} starts to drop. When HLD_1 arrives, the gated delay cell enters its hold stage and V_{mid1} remains unchanged. When AWK is asserted, the gated delay cell is re-activated and V_{mid1} starts to drop again. If there is another time register whose HLD input and AWK are connected, the output of this time register can be a reference. Therefore, if we compare the time difference between two time registers' outputs, it should be the same as the time input variable. The preceding time register can be utilized to construct a time adder shown in Fig.1.7 (A). It should be noted that the second gated delay cell has a reversing the order of the input data because of $T_{OUT1} = T_d$-T_{in1} and $T_{OUT2} = T_d$-T_{in2} leading to

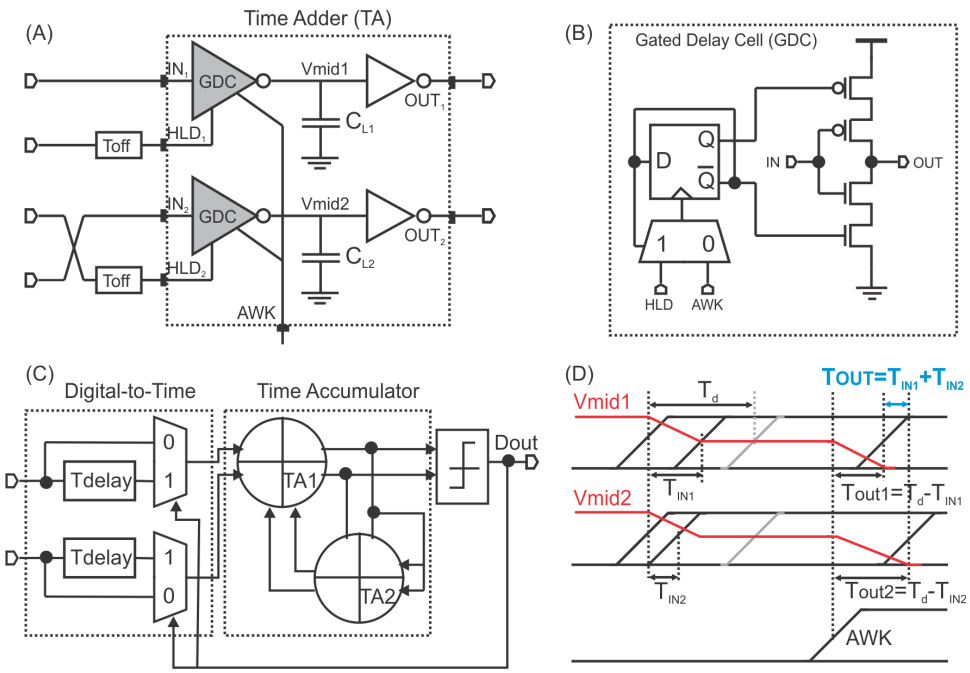

Figure 1.7: (A) Time adder [9]. (B) Gated delay cell [9]. (C) $\Delta\Sigma$ TDC [10]. (D) Waveform of time adder.

T_{OUT}=T_{OUT1}-T_{OUT2}=T_{in1}-T_{in2} instead of T_{in1}+T_{in2}. To deal with this, the order of the input is reversed as shown in Fig.1.7(A). Fig.1.7(D) shows a timing diagram of the time adder. T_d is a normal propagation delay of the GDC. The time accumulator consists of two back-to-back connected time adders. Fig.1.7(C) shows the schematic of the time accumulator in [10]. In the time accumulator, one of time adders functions like a time register since the inputs of the second time adder are tied together such that T_{in2} becomes 0. Therefore, $T_{in1} + 0 = T_{in1}$, which is identical to z^{-1} function in discrete-time domain. The operation of the time adder and time register performs $y[n] = \sum_{k=0}^{n} T_{in}[\mathrm{k}]$.

1.4 Motivation

TDCs with a sub-per-stage-delay resolution and a short conversion time are critical to a number of applications. For applications such as $\Delta\Sigma$ modulators, conversion time directly affects the oversampling ratio subsequently the performance of the modulators. Conversion time is also of a great importance for phase-locked loops (PLLs) with a TDC phase detector.

This is because conversion time in this case directly affects the speed of the TDC phase detector subsequently the loop dynamics of the PLLs. Also resolution affects the phase noise of PLLs. Vernier delay-line TDCs and hierarchical vernier delay-line TDCs are not attractive for these applications due to their long conversion time and high power and silicon consumption. Pulse-shrinking that also offer sub-per-stage delay are good candidates for these application. To improve resolution, a large number of pulse-shrinking stages are needed. Reducing the number of pulse-shrinking stages is highly desirable in minimizing nonlinearities arising from stage mismatch. To reduce the number of stages without sacrificing resolution, a two-step architecture is explored in this dissertation. A drawback of the two-step architecture is long conversion time since it needs to extract the residue information then apply to the fine stage. To combat this, a time-interleaved pulse-shrinking TDC is proposed in this dissertation.

$\Delta\Sigma$ modulation is an effective means to improve time resolution below per-stage delay. $\Delta\Sigma$ TDCs can be used along with a voltage-to-time converter to perform analog-to-digital conversion. Currently analog-to-digital conversion utilizing time-mode techniques is most realized using a voltage-controlled oscillator (VCO)-based quantizers. VCO-based quantizers offer a number of attractive intrinsic advantages including built-in first-order noise-shaping, inherent multi-bit quantization with a good linearity, fast quantization subsequently a large over-sampling ratio, and full scalability with technology. To have a better signal-to-noise-plus-distortion ratio (SNDR), a high-order OTAs based voltage-mode integrator is required in the forward path in order to have an adequate loop gain to suppress the effect of the nonlinearities and quantization noise as shown in Fig.1.8. These ADCs are therefore not all-digital. As a result, their performance does not scale naturally with technology. As the performance of voltage-mode integrators scales poorly with technology, time integrators with a large in-band gain are critically needed for all-digital $\Delta\Sigma$ TDC.

Efforts have been made to replace OTA filters with time-mode filters such that entire modulators can be realized digitally. Taillefer and Roberts proposed a ring oscillator voltage-to-time integrator consisting of two voltage-controlled delay units (VCDUs) and a static inverter [22]. Implementing high-order integrators using this approach is rather difficult.

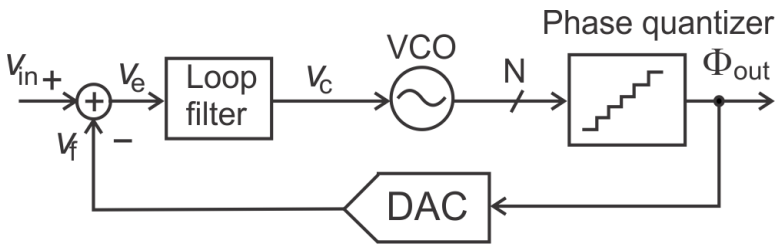

Figure 1.8: $\Delta\Sigma$ TDCs [6, 7].

The time accumulator proposed by Hong *et al.* consists of two back-to-back connected time adders realized using four GDCs [10]. The core of the time accumulator is a time register proposed capable of storing a time variable and reading out the stored variable [9]. Kim *et al.* showed that a gated delay line (GDL) functions as a time register with the gating signal consisting of the time variable to be stored and a trigger signal [23, 24]. A time adder is realized using two GDCs, each has a large capacitor. The need for two GDCs, however, increases power and silicon consumption. To minimize power and silicon consumption, a new time integrator is proposed consisting of two new time adders using only one capacitor in each time adder. In this dissertation, two time integrators realized using digital circuits are proposed and are used to implement all-digital $\Delta\Sigma$ modulators.

1.5 Contributions

1) A silicon and power-efficient two-step pulse-shrinking TDC was proposed. The TDC consists of a coarse TDC and a fine TDC with an efficient residual time extraction technique. The proposed TDC in [25] and [26] allows rapid digitization of a time input with the minimum silicon and power consumption without sacrificing time resolution.

2) A time-interleaved pulse-shrinking TDC was proposed to overcome the conversion time inefficiency of the two-step pulse-shrinking TDC also developed in this study. Similar to the preceding two-step pulse-shrinking TDC, the time-interleaved TDC in [27] and [28] is composed of a coarse TDC but a pair of fine TDCs that operate in a time-interleaved manner such that time synchronization logic and associated time latency existing in the preceding two-step pulse-shrinking TDC are removed.

3) A new all-digital time integrator consisting of a cascode time adder with a raised threshold voltage and a time register is proposed. The developed time integrator is utilized in the development of an all-digital 1-1 MASH $\Delta\Sigma$ modulator to realized an all-digital second-order $\Delta\Sigma$ modulator. To the best of the knowledge of the author, this is the first all-digital 1-1 MASH $\Delta\Sigma$ modulator ever reported in [29], [30] and [31].

4) A novel power efficient time integrator utilizing a bi-directional gated delay line was proposed. The open-loop characteristics of the proposed time integrator enables the rapid integration of time variables without stability constraints and power consumption penalty. The time integrator is utilized in the development of an all-digital first-order $\Delta\Sigma$ modulator in [32]. The large loop bandwidth of the modulator benefited from the rapid integration capability of the time integrator enables the modulator to digitize large bandwidth signals.

1.6 Dissertation Organization

This dissertation comprises of 5 chapters. Chapter 2 presents a time-interleaved pulse-shrinking TDC consisting of a 16-stage coarse pulse-shrinking TDC and a pair of 16-stage fine pulse-shrinking TDCs to overcome the conversion time issue present in two-step pulse-shrinking TDC.

Chapter 3 deals with a 1-1 MASH $\Delta\Sigma$ TDC by using time integrator. It shows a differential cascode time integrator. The differential cascode time integrator suppresses second-order harmonic tone present in single-ended time integrators. The effect of the non-idealities of the TDC, in particular, the delay uncertainty of the digital-to-time converter functioning as a time summer and jitter due to device current noise and current mismatch between the discharge paths of the time adder, are examined in detail.

The chapter 4 presents a low-power time integrator and its applications in an all-digital first-order $\Delta\Sigma$ TDC. The time integrator is realized using a bi-directional gated delay line with time variable to be integrated as the gating signal. The accumulation of the time variable is obtained via the accumulation of the charge of the load capacitor and logic state

of gated delay stages. Issues affecting the performance of the time integrator and TDC are examined.

Finally, conclusions drawn from this study and further research that can be built upon this dissertation are provided in Chapter 5.

1.7 Chapter Summary

In this chapter, we briefly examined technology scaling-induced challenges encountered in design of mixed-mode systems. We showed that although technology scaling results in a reduced voltage accuracy, it sharply improves the switching accuracy of digital circuits at the same time. As a result, analog signal processing can be performed using time-mode approaches while taking the full advantages of technology scaling. The challenges encountered in design of time-mode circuits were explored. An overview of TDCs including sampling TDCs such as delay-line TDCs, vernier delay-line TDCs, hierarchical vernier delay-line TDCs, pulse-shrinking TDCs, and noise-shaping TDCs such as GRO TDCs and $\Delta\Sigma$ TDCs, were briefly explored. The motivation and primary contributions of this dissertation were discussed. Finally, the organization of the dissertation was outlined.

Chapter 2

Time-Interleaved Pulse-Shrinking TDC

This chapter presents an area efficient time-interleaved pulse-shrinking TDC with minimal conversion time. The TDC consists of a 16-stage coarse pulse-shrinking TDC with per-stage shrinkage 4.8 ns and a pair of 16-stage fine pulse-shrinking TDCs with per-stage shrinkage 296 ps. The fine TDCs are operated in a time-interleaved manner in parallel with the coarse TDC so as to minimize conversion time. The remainder of the chapter is organized as follows : Section 2.1 presents the architecture of a two-step pulse-shrinking TDC that can be thought as a conventional approach to minimize the delay stages. The characteristics of the TDC including mismatch and noise-induced timing errors, the timing error of delay stages, conversion time, power, and silicon consumption are investigated in detail in Section 2.2. Section 2.3 presents the architecture of a time-interleaved pulse-shrinking TDC that minimizes conversion time. The characteristics of the TDC including silicon consumption, power consumption, mismatch-induced error, conversion time, and timing errors are investigated in detail in Section 2.4. Section 2.5 presents the simulation and measurement results of the two-step pulse-shrinking TDC and time-interleaved pulse-shrinking TDC implemented in an IBM 130 nm 1.2 V CMOS technology. The chapter is concluded in Section 2.6.

2.1 Two-Step Pulse-Shrinking TDC

The two-step pulse-shrinking TDC shown in Fig.2.1 uses a coarse TDC with M identical pulse-shrinking stages of per-stage shrinkage ΔT_1 to quantize an input time variable

T_{in} bound by $\Delta T_2 \leq T_{in} \leq M\Delta T_1$ and a fine TDC with N identical pulse-shrinking stages of per-stage shrinkage $\Delta T_2 = \Delta T_1/N$ to quantize the residual pulse of the coarse pulse-shrinking TDC. The outputs of both the coarse and fine TDCs are read using D flipflops (DFFs) implemented using TSPC (true-single-phase-clock) logic. A residual pulse extraction block extracts the residual pulse of the coarse TDC and conveys it to the fine TDC. Fig.2.2 shows the residual pulse of a 4-stage pulse-shrinking TDC. It is seen that the residual pulse T_{res} becomes available only at the falling edge of T_{in}. Also, the residual pulse is bound by $0 < T_{res} < \Delta T_1$. If the residual phase is at the output of m stage, we will have $X_m = 1$ and $X_{m+1} = 0$ where X_m and X_{m+1} are the output of mth and $(m+1)$th stages, respectively. Clearly $X_m \oplus X_{m+1}$ can be used to determine the location of the residual pulse, specifically, if $X_m \oplus X_{m+1} = 1$, the residual pulse will exist at the output of mth stage. Otherwise, no residual pulse will be present at the output of mth stage.

Fig.2.3 shows the simplified schematic of residual pulse extraction block. To illustrate its operation, consider a time variable T_{in} that satisfies $\Delta T_1 < T_{in} < 2\Delta T_1$, as shown in Fig.2.3(c). Since $X_{c,1} = 1$ and $X_{c,2-4} = 0$, the residual pulse is located at $X_{c,1}$ as $T_{in} \oplus X_{c,1} = 1$, $X_{c,1} \oplus X_{c,2} = 1$, $X_{c,2} \oplus X_{c,3} = 0$, and $X_{c,3} \oplus X_{c,4} = 0$. Note that since $X_{c,j}$ subsequently $Q_{c,j}$, $j = 1, 2, 3, 4$ assume their value at different times, in order for the multiplexer to select the correct residual pulse using only one selection signal, $X_{c,j}$ needs to be delayed by ΔT_1 prior to multiplexing. It is seen from Fig.2.3 that the residual pulse extraction block is capable of extracting the residual pulse of the coarse TDC regardless of the value of T_{in}.

Similar to one-step pulse-shrinking TDCs, the two-step pulse-shrinking TDC needs to be calibrated prior to measurement. To calibrate the TDC, a known time variable T_{cal}, typically a reference clock of known period, is applied to the TDC. The pulse propagates through the pulse-shrinking stages of the coarse TDC. The per-stage shrinkage is adjusted by varying V_{b1} until the pulse just disappears at the output of the last stage of the coarse TDC. This process can be automated using a delay-locked loop, similar to that used in [6, 7]. Once this is done, the calibration of the coarse TDC is completed and the resolution of the calibrated coarse TDC is given by $\Delta T_1 = T_{cal}/M$. Once the coarse TDC is calibrated, the

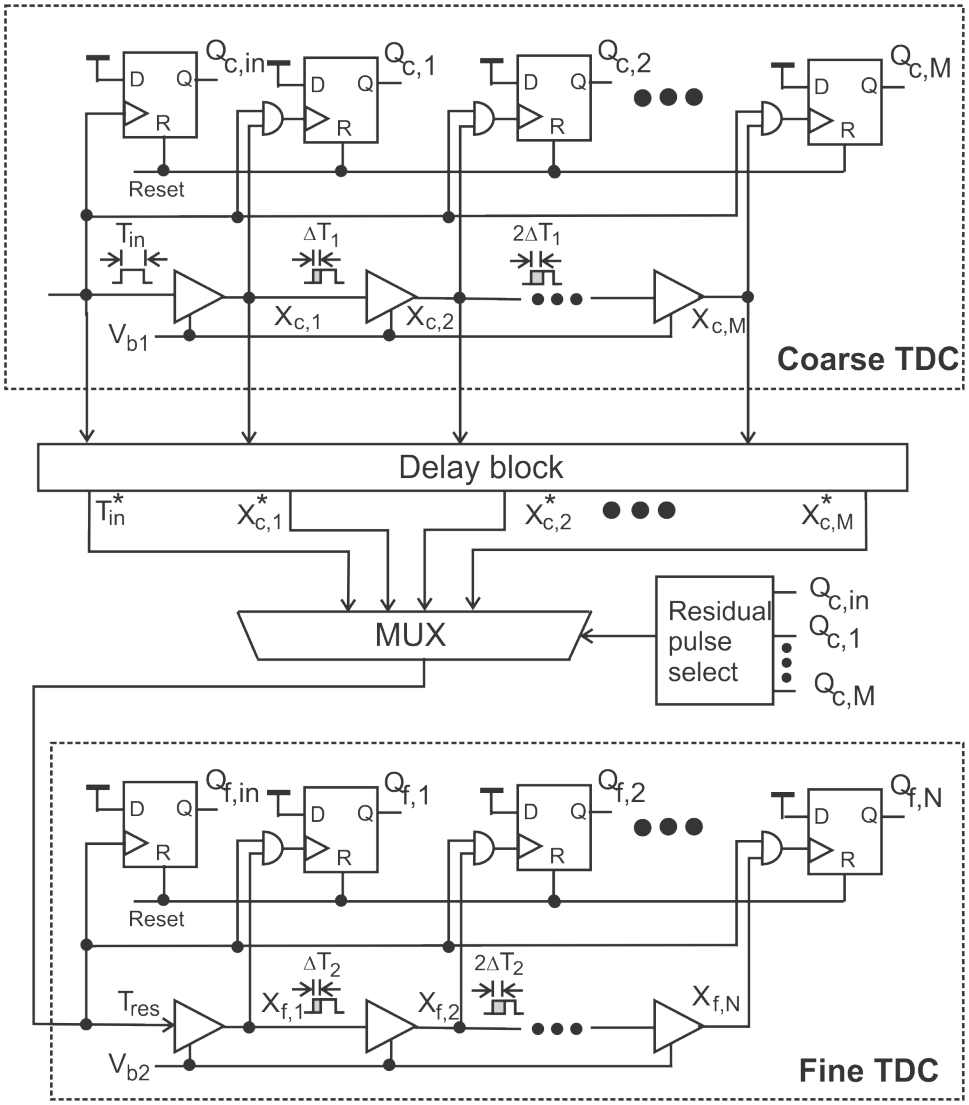

Figure 2.1: Simplified schematic of two-step pulse-shrinking delay-line TDC. All D flipflops (DFFs) are positive edge triggered.

width of the pulse at the input of the last stage is exactly ΔT_1. This pulse is then fed to the fine TDC. The per-stage shrinkage of the fine TDC is adjusted by varying V_{b2} until the pulse propagating in the fine TDC just disappears at the output of the last stage of the fine TDC. Once this occurs, the calibration of the fine TDC is completed and its resolution of the calibrated fine TDC is given by $\Delta T_2 = \Delta T_1/M = T_{cal}/(MN)$.

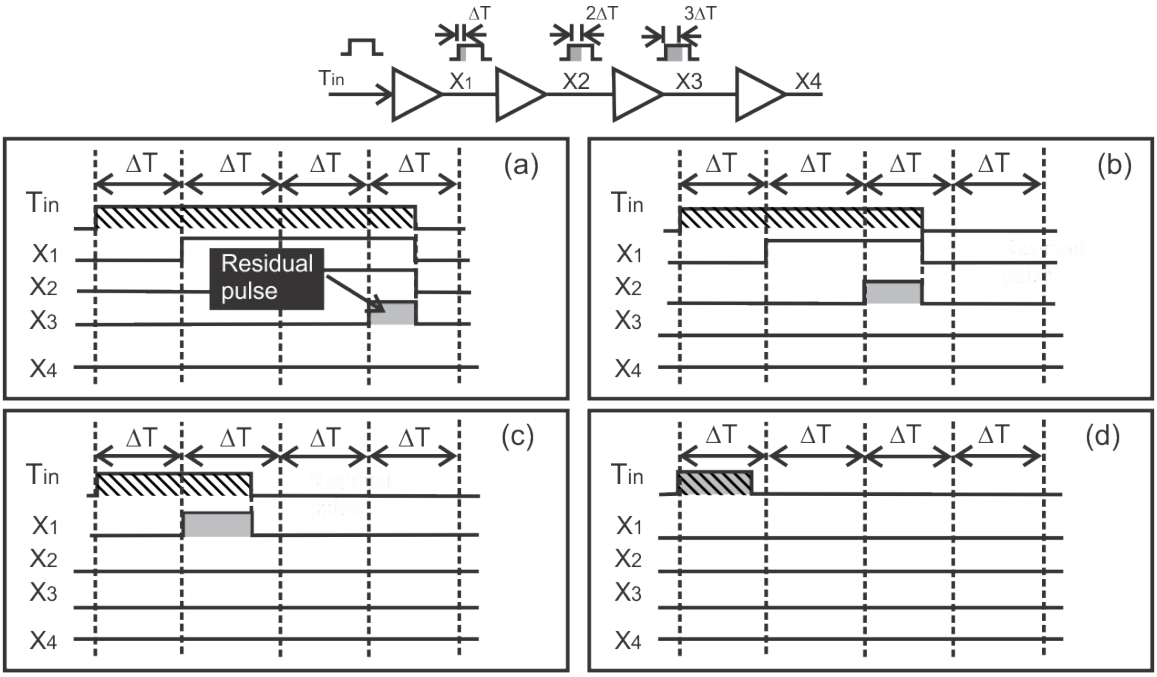

Figure 2.2: Extraction of the residual pulse of coarse TDC. (a) $3\Delta T < T_{in} < 4\Delta T$. (b) $2\Delta T < T_{in} < 3\Delta T$. (c) $\Delta T < T_{in} < 2\Delta T$. (d) $0 < T_{in} < \Delta T$.

2.2 Characteristics of Two-Step Pulse-Shrinking TDC

This section examines the characteristics of the two-step pulse-shrinking TDC. For the purpose of comparison, a single-step pulse-shrinking TDC that provides the same resolution and dynamic range as those of the TDC is utilized.

2.2.1 Mismatch-induced timing errors

Although ideally the resolution of a pulse-shrinking TDC is set by the per-stage shrinkage ΔT and ΔT can be made sufficiently small if the number of the pulse-shrinking stages is large enough, in reality, the lower bound of the resolution of pulse-shrinking TDCs is set by the timing errors caused by mismatch between pulse-shrinking stages and the noise of the TDC. To simplify analysis, we assume that mismatch between pulse-shrinking stages is dominated by the mismatch of the discharge of the load capacitor. Since capacitance ratio in standard CMOS technologies can be made accurately, the mismatch of the discharge of the load capacitor is dictated by the mismatch of the discharge current. Let the mismatch

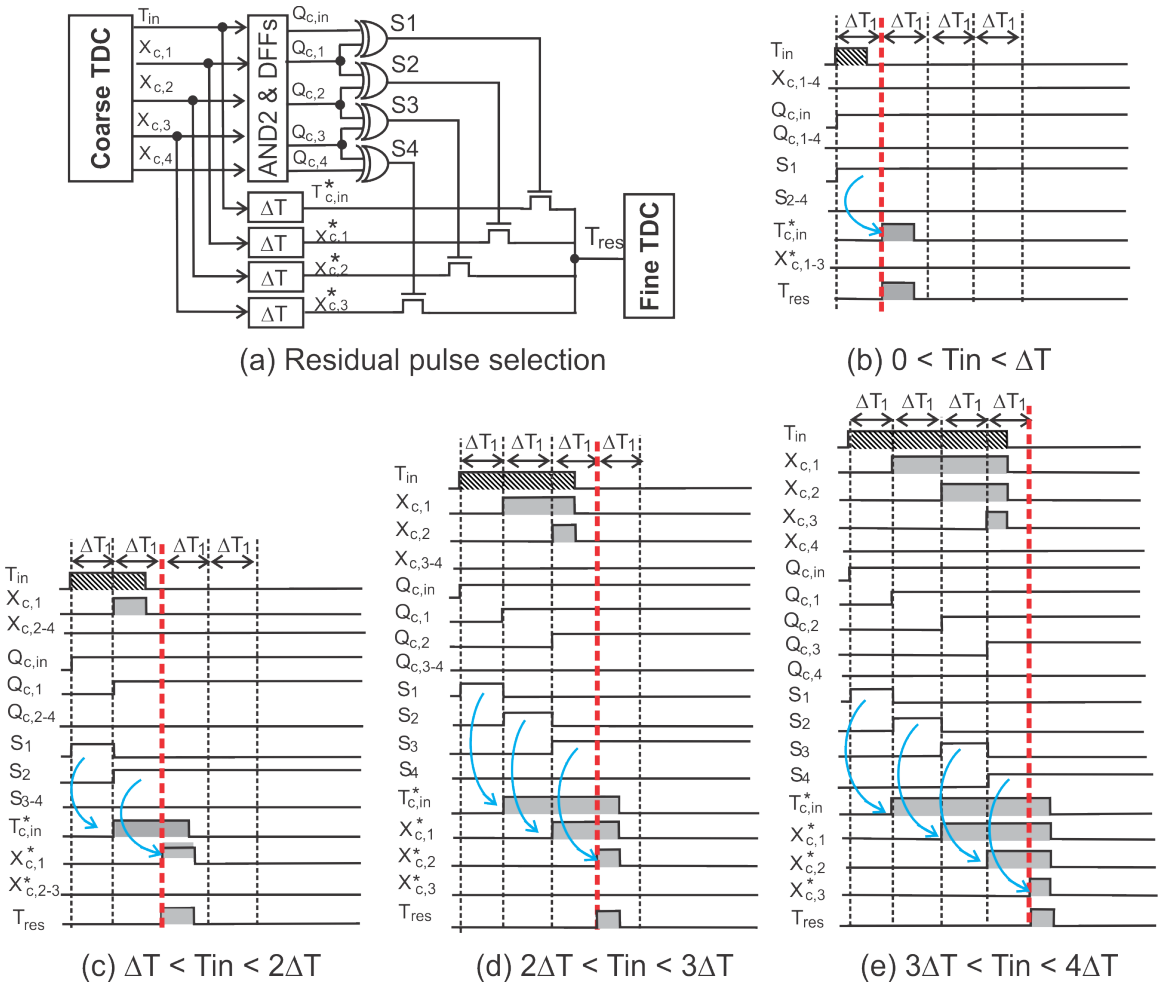

Figure 2.3: Simplified schematic of residual pulse selection and waveform. (a) Simplified schematic. (b) $0 < T_{in} < \Delta T$. (c) $\Delta T < T_{in} < 2\Delta T$. (d) $2\Delta T < T_{in} < 3\Delta T$. (e) $3\Delta T < T_{in} < 4\Delta T$.

between the discharge current of pulse-shrinking stages be ΔJ. Assume that ΔJ is normally distributed with a zero mean $\mu_J = 0$ and a non-zero standard deviation σ_J. If J is generated by a nMOS transistor in saturation, the current of the transistor with the presence of a dimension mismatch $\Delta(W/L)$ and a threshold voltage mismatch ΔV_T is determined from

$$J = \frac{1}{2}\mu_n C_{ox}\left[\frac{W}{L} + \Delta\left(\frac{W}{L}\right)\right](V_b - V_T - \Delta V_T)^2. \tag{2.1}$$

Note that we have neglected the effect of channel length modulation and high-order effects. Neglecting high-order terms, we obtain mismatch-induced current error ΔJ_m

$$J \approx J_o \left(1 + \frac{\Delta(W/L)}{W/L} - \frac{2\Delta V_T}{V_b - V_T}\right), \tag{2.2}$$

where $J_o = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_b - V_T)^2$ is the current without mismatch. Since $\Delta(W/L)$ and ΔV_T are uncorrelated, we have power of mismatch-induced current : $\sigma^2_{\Delta J_m} = \sigma^2_{\Delta J_{W/L}} + \sigma^2_{\Delta J_{V_T}}$ where $\sigma^2_{\Delta J_{W/L}} \approx \left(\frac{J_o}{W/L}\right)^2 \sigma^2_{\Delta(W/L)}$ and $\sigma^2_{\Delta J_{V_T}} \approx \left(\frac{2J_o}{V_b - V_T}\right)^2 \sigma^2_{\Delta V_T}$. Let us now calculate the timing error $\Delta\tau_m$ caused by the mismatch-induced current error ΔJ_m. When ΔJ_m is present, we have

$$v_x = V_{DD} - \frac{J + \Delta J_m}{C_x} t. \tag{2.3}$$

At the threshold-crossing, $v_x = V_T$, we have

$$\Delta T + \Delta\tau_m = \frac{(V_{DD} - V_T)C_x}{J} \frac{1}{1 + \Delta J_m/J}. \tag{2.4}$$

Making use of $\frac{1}{1+\frac{\Delta J_m}{J}} \approx 1 - \frac{\Delta J_m}{J}$, we have $\Delta T + \Delta\tau_m \approx \Delta T\left(1 - \frac{\Delta J_m}{J}\right)$ where $\Delta T = \frac{(V_{DD} - V_T)C_x}{J}$. It becomes evident that the mismatch-induced timing error is given by

$$\Delta\tau_m \approx -\left(\frac{\Delta T}{J}\right)\Delta J_m \tag{2.5}$$

with its power $\sigma^2_{\Delta\tau_m} = \left(\frac{\Delta T}{J}\right)^2 \sigma^2_{\Delta J_m}$. It is seen from (2.5) that mismatch-induced timing error per pulse-shrinking stage $\Delta\tau_m$ is directly proportional to per-stage shrinkage ΔT and mismatch-induced current error ΔJ_m, and inversely proportional to the discharge current J.

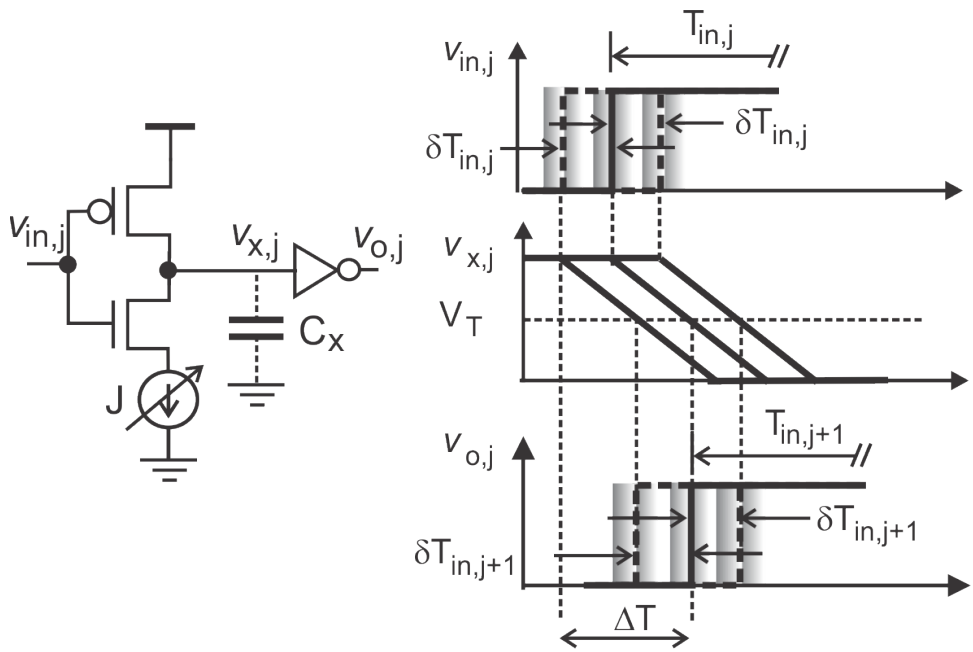

Figure 2.4: Mismatch-induced timing error in pulse-shrinking stage. The timing error at the output of a pulse-shrinking stage contains the timing error present at the input and that induced by the mismatch of the pulse-shrinking stage.

Having derived the mismatch-induced timing error per pulse-shrinking stage, let us now examine the propagation of mismatch-induced per-stage timing error in a pulse-shrinking TDC. Refer to Fig.2.4. The input of the second pulse-shrinking stage, denoted by $T_{in,2}$, is given by $T_{in,2} = T_{in} - (\Delta T + \Delta\tau_{m,1})$ where $\Delta\tau_{m,1}$ denotes the timing error caused by the mismatch of stage 1. $T_{in,2}$ is fed to the second pulse-shrinking stage that also has a mismatch discharge current ΔJ_m. The timing error of the output of the 2nd stage and the input of the 3rd pulse-shrinking stage, denoted by $T_{in,3}$, contains the timing error transmitted from that of the input of the 2nd stage and the timing error induced by the mismatch of the 2nd stage, and is given by $T_{in,3} = T_{in,2} - (\Delta T + \Delta\tau_{m,2}) = T_{in} - 2\Delta T - (\Delta\tau_{m,1} + \Delta\tau_{m,2})$. Similarly, one can show that the input of $(k+1)$th pulse-shrinking stage is given by $T_{in,k+1} = T_{in} - k\Delta T - \sum_{j=1}^{k} \Delta\tau_{m,j}$. Since $\Delta\tau_{m,j}$, $j = 1, 2, ...$, are uncorrelated, the power of the timing error at the input of $(k+1)$th stage is obtained

$$\sigma^2_{\Delta\tau_{m,k+1}} = \sum_{j=1}^{k} \sigma^2_{\Delta\tau_{m,j}}. \tag{2.6}$$

If we further assume $\Delta\tau_{m,1}$, $\Delta\tau_{m,2}$, ... have an identical distribution profile, i.e., $\mu_{\Delta\tau_{m,1}} = \mu_{\Delta\tau_{m,2}} = ... = 0$ and $\sigma^2_{\Delta\tau_{m,1}} = \sigma^2_{\Delta\tau_{m,2}} = ... = \sigma^2_{\Delta\tau_m}$, it follows from (2.6) that

$$\sigma^2_{\Delta\tau_{m,k+1}} = k\sigma^2_{\Delta\tau_m}. \tag{2.7}$$

It is important to note that $T_{in,k+1}$ decreases linearly with the increase in the number of pulse-shrinking stages while $\sigma^2_{\Delta\tau_{m,k+1}}$ increases linearly with the number of pulse-shrinking stages. The mismatch-induced timing error has the worst impact on the LSB of pulse-shrinking TDCs.

For a single-step pulse-shrinking TDC with M stages, the worst-case output time variable is given by $T_{in,M} = T_{in} - (M-1)\Delta T - (M-1)\Delta\tau_m$. In order for the readout DFFs to capture the output of the last pulse-shrinking stage without entering a meta-stable state, $T_{in,M} \geq \tau_{\text{setup}} + \tau_{\text{hold}}$, where τ_{setup} and τ_{hold} are the set time and hold time of DFFs respectively is required. For a given pulse-shrinking TDC, if we neglect mismatch-induced timing error, we will have

$$\Delta T \leq \frac{T_{in} - (\tau_{\text{setup}} + \tau_{\text{hold}})}{M-1}. \tag{2.8}$$

Eq.(2.8) gives the maximum per-stage shrinkage of the pulse-shrinking TDC for a given T_{in}. If the mismatch-induced timing error is included, we will have

$$\Delta T \leq \frac{T_{in} - (\tau_{\text{setup}} + \tau_{\text{hold}})}{M-1} + \Delta\tau_m. \tag{2.9}$$

Since $\Delta\tau_m$ is random, ΔT with mismatch is smaller as compared with that without mismatch.

2.2.2 Thermal noise-induced timing errors

Mismatch-induced timing error is static while noise-induced timing error is dynamic. Noise-induced timing error arises from device noise such as thermal noise and switching noise with the former affecting individual stage and the latter impacting all stages. Let us first consider the timing error caused by thermal noise. Refer to Fig.2.5, let v_n denote the thermal noise present at the voltage of the load capacitor with its power given by $\overline{v_n^2} = kT/C_x$ where k is Boltzmann constant and T is temperature in degrees kelvin [33]. It can be shown that the power of noise-induced timing error $\Delta\tau_n$, denoted by $\sigma^2_{\Delta\tau_n}$ with the subscript n signifies noise, is obtained from

$$\sigma^2_{\Delta\tau_n} = \frac{(\Delta T_x)^2}{V_{DD}^2}\overline{v_n^2} = \frac{kT}{C_x}\frac{(\Delta T_x)^2}{V_{DD}^2}. \tag{2.10}$$

Since $T_x = \frac{C_x V_{DD}}{J}$, we have

$$\sigma^2_{\Delta\tau_n} = \frac{kT}{V_{DD}}\frac{\Delta T_x}{J}. \tag{2.11}$$

The TDC has both coarse pulse-shrinking stages and fine pulse-shrinking stages with $\Delta T_1 = N\Delta T_2$, we have $\Delta T_{x1} = N\Delta T_{x2}$. Since both have the same discharge current in order to minimize power consumption, from (2.11), we have $\sigma^2_{\Delta\tau_{n,c}} = N\sigma^2_{\Delta\tau_{n,f}}$, where $\sigma^2_{\Delta\tau_{n,c}}$ and $\sigma^2_{\Delta\tau_{n,f}}$ are the power of the noise-induced timing jitter of the coarse and fine pulse-shrinking

stages, respectively. Utilizing (2.7) and noting that noise-induced timing error in each pulse-shrinking stage is uncorrelated, we obtain the overall jitter of the one step pulse-shrinking TDC

$$\sigma^2_{\text{1-step}} = (MN)\sigma^2_{\Delta\tau_{n,f}}. \tag{2.12}$$

Similarly, the overall jitter of the TDC is given by

$$\sigma^2_{\text{proposed}} = M\sigma^2_{\Delta\tau_{n,c}} + N\sigma^2_{\Delta\tau_{n,f}}. \tag{2.13}$$

We therefore arrive at

$$\sigma^2_{\text{proposed}} = (M+1)N\sigma^2_{\Delta\tau_{n,f}} \tag{2.14}$$

A comparison of (2.12) with (2.14) reveals that the jitter of the TDC is comparable to that of the 1-step pulse-shrinking TDC.

2.2.3 Switching noise-induced timing error

Switching noise is caused by the voltage drop across the bond wires of supply and ground rails. It gives rise to on-chip supply voltage fluctuation and ground bouncing and is the main source of the jitter of pulse-shrinking TDCs. The jitter of pulse-shrinking TDCs caused by device noise such as thermal and flicker noise is uncorrelated while that induced by switching noise is correlated. Since the rising edge of the output voltage of pulse-shrinking stages governed by time constant R_pC_x where R_p is the ON-resistance of the PMOS transistor and C_x is the load capacitance is much sharper as compared with its falling edge controlled

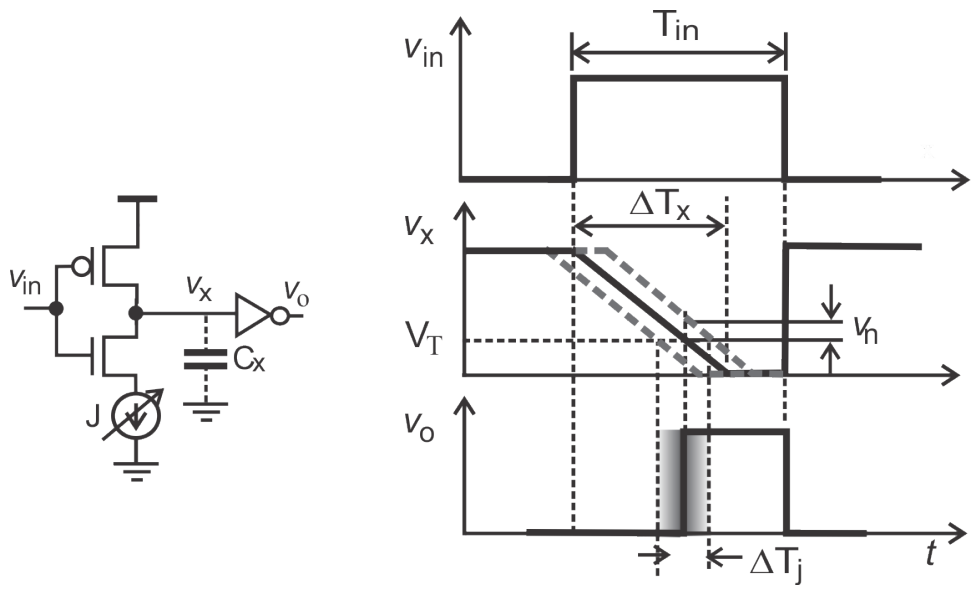

Figure 2.5: Jitter of pulse-shrinking stages.

by the current source J, the jitter of the output of the pulse-shrinking stage is mainly due to ground bounce-induced switching noise occurring during the discharge of the load capacitor.

Let the ground bouncing of the pulse-shrinking stage be represented by v_{sn}. The discharge current of the load capacitor is given by $J \approx J_o \left(1 - \frac{2v_{sn}}{V_b - V_T}\right)$ from which we obtain ground bouncing induced current error ΔJ_{sn}

$$\Delta J_{sn} = -\left(\frac{2J_o}{V_b - V_T}\right) v_{sn}. \tag{2.15}$$

Utilizing (2.5), we obtain the per-stage ground bouncing induced timing error denoted by $\Delta\tau_{sn}$

$$\Delta\tau_{sn} = \left(\frac{\Delta T}{J}\right) \Delta J_{sn}. \tag{2.16}$$

It follows that

$$\sigma^2_{\Delta\tau_{sn}} = \left(\frac{\Delta T}{J}\right)^2 \sigma^2_{\Delta J_{sn}}. \tag{2.17}$$

Following the similar approach as that for computing the propagation of mismatch-induced timing error in a pulse-shrinking TDC, we obtain the input of $(k+1)$th pulse-shrinking stage with ground bouncing considered only

$$T_{in,k+1} = T_{in} - k\Delta T - \sum_{j=1}^{k} \Delta\tau_{sn,j}. \tag{2.18}$$

The jitter of each pulse-shrinking stage caused by ground bouncing is completely correlated and therefore has the same distribution profile, i.e., $\sigma_{\Delta\tau_{sn,1}} = \sigma_{\Delta\tau_{sn,2}} = ... = \sigma_{\Delta\tau_{sn}}$. Eq.(2.18) can be written as

$$T_{in,k+1} = T_{in} - k\Delta T - k\Delta\tau_{sn}. \tag{2.19}$$

It follows that

$$\sigma^2_{\Delta\tau_{sn,k+1}} = k^2\sigma^2_{\Delta\tau_{sn}}. \tag{2.20}$$

The difference between (2.20) and (2.7) is apparent.

The power of the timing error caused by the thermal noise of devices increases linearly with the number of the pulse-shrinkage stages while that caused by switching noise arises quadratically with the number of the pulse-shrinkage stages. Since $\Delta\tau_m$, $\Delta\tau_n$, and $\Delta\tau_{sn}$ are uncorrelated, the total timing error $\Delta\tau$ is obtained from

$$\Delta\tau = \sqrt{(\Delta\tau_m)^2 + (\Delta\tau_n)^2 + (\Delta\tau_{sn})^2}. \tag{2.21}$$

and its power is given by $\sigma^2_{\Delta\tau} = \sigma^2_{\Delta\tau_m} + \sigma^2_{\Delta\tau_n} + \sigma^2_{\Delta\tau_{sn}}$. If we assume that an input sinusoid signal with an amplitude A, SNR (Signal-to-Noise) becomes

$$SNR = \frac{A^2/2}{\sigma^2_{\Delta\tau}}. \tag{2.22}$$

2.2.4 Timing error of delay stages

It was shown that for a pulse-shrinking TDC with M stages, a total of M delay stages are needed to delay $X_{c,j}, j = 1, 2, ..., M$ by ΔT_1 prior to multiplexing. In this work, each delay stage was implemented using a pair static inverters with a large capacitor load, as shown in Fig.2.6. Although simple, this delay cell suffers from a high level of power consumption. This is because the slowly rising and falling transients of the capacitor voltage due to the large load capacitance give rise to a large time interval in which the short-circuit current of the load inverter exists. To investigate the effect of the timing error of these delay cells on the performance of the TDC, we assume that the delay error of the delay cell that provides time delay ΔT_1 be $\Delta\tau_1$. Since the selection signal of the multiplexer does not go through the delay cells, it is not affected by the delay error of the delay cells. Further, since $\Delta\tau \ll \Delta T_1$ while the space between the assertion of $S_4 = 1$ and $X^*_{c,3} = 1$ is ΔT_1, the slight variation of the delay provided by the delay cells, which only affects the assertion of $X^*_{c,3} = 1$ has no effect on the extraction of the residual pulse, as evident in Fig.2.6.

2.2.5 Conversion time

If a single-stage pulse-shrinking TDC is used, since digitization starts at the rising edge of T_{in} and completes at the falling edge of T_{in}, the conversion time measured from the

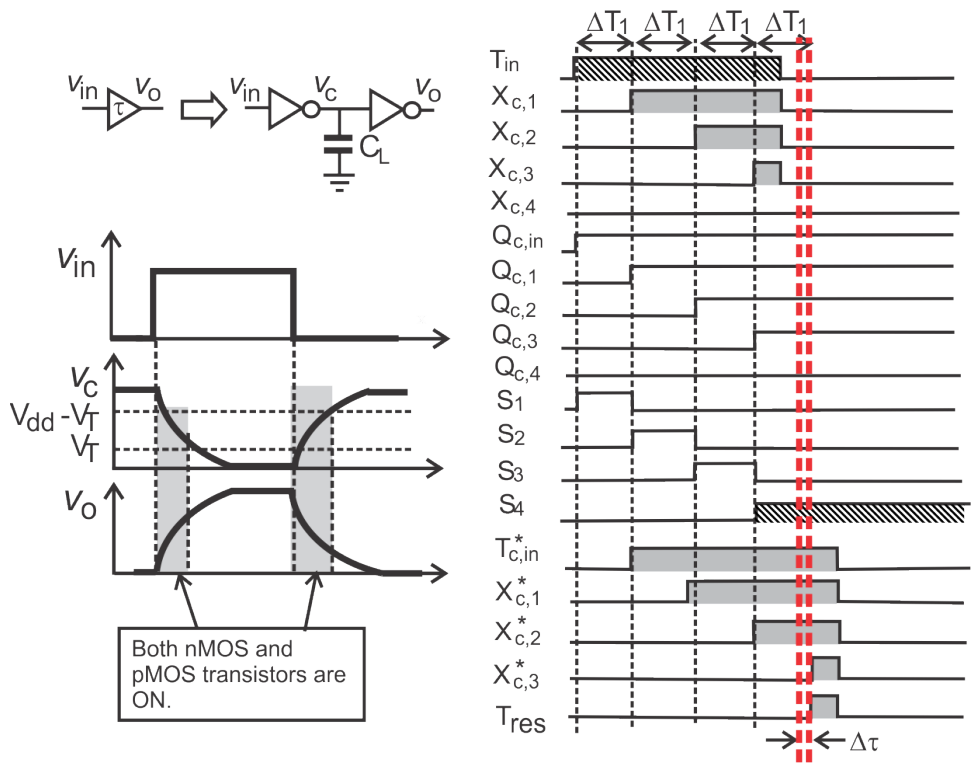

Figure 2.6: The effect of the delay error of delay stages on the TDC.

availability of the input data, which is the falling edge of T_{in}, to the availability of the digital output is given by $\tau_{\text{1-step}} = \tau_{DFF}$, where τ_{DFF} is the delay of DFFs. For the TDC it is seen from Fig.2.3 that the worst-case conversion time is given by $\tau_{\text{proposed}} = \tau_{MUX} + \Delta T_1 + \tau_{DFF}$, where τ_{MUX} is the delay of the multiplexer. The conversion time of the TDC is therefore slightly longer as compared with that of single-step pulse-shrinking TDCs. This result is expected as the residual pulse of the coarse TDC will become available only at the falling edge of T_{in}. The conversion time of the fine TDC is the duration of the residual pulse of the coarse TDC with its worst value ΔT_1.

2.2.6 Power consumption

The total power consumption of the pulse-shrinking stage in cycle is the sum of the power consumption for charging C_x by V_{DD} via the pMOS transistor, discharging C_x by the current source, and charging and discharging C_o. Since the average dynamic power

consumption of an static inverter in an input period is given by $P = C_L V_{DD}^2 f$ where C_L is the load capacitance of the inverter and f is the frequency of the input of the inverter, we obtain the power for charging C_x : $C_x V_{DD}^2 f/2$ and that for charging and discharging C_o: $C_o V_{DD}^2 f$. To calculate the power for discharging C_x, since

$$v_x = V_{DD} - \left(\frac{V_{DD}}{\Delta T_x}\right) t, \quad 0 \leq t \leq \Delta T_x, \tag{2.23}$$

utilizing $\Delta T_x = \left(\frac{V_{DD}}{V_T}\right) \Delta T$, we have the instantaneous power for discharging C_x

$$p_x = J v_x = J \left(V_{DD} - \frac{V_{DD}}{\Delta T_x} t\right). \tag{2.24}$$

The average power consumption for discharging C_x is obtained from

$$P_x = \frac{1}{\Delta T_x} \int_0^{\Delta T_x} p_x(t) dt = \frac{1}{2} J V_{DD}. \tag{2.25}$$

The total power consumption of the pulse-shrinking stage is therefore given by

$$P_s = (C_o V_{DD}^2 + \frac{1}{2} C_x V_{DD}^2 + \frac{1}{2} J V_{DD}) f. \tag{2.26}$$

Because $\frac{J_1}{C_{x1}} = \frac{V_{DD} - V_T}{\Delta T_1}$ and $\frac{J_2}{C_{x2}} = \frac{V_{DD} - V_T}{\Delta T_2}$, we arrive at $\frac{\Delta T_1}{\Delta T_2} = \frac{C_{x1}}{C_{x2}} \frac{J_2}{J_1} = N$. To minimize power consumption, we choose $J_1 = J_2 = J$ and $C_{x1} = N C_{x2} = N C_x$. The total power consumption of the single-step pulse-shrinking TDC is obtained from

$$P_{\text{1-step}} = \left[\left(C_o + \frac{C_x}{2}\right) V_{DD}^2 + \frac{1}{2} J V_{DD}\right] f(MN) \tag{2.27}$$

The total power consumption of the TDC is obtained from

$$\begin{aligned} P_{\text{proposed}} &= \left[\left(C_o + \frac{NC_x}{2}\right) V_{DD}^2 + \frac{1}{2} J V_{DD}\right] fM \\ &+ \left[\left(C_o + \frac{C_x}{2}\right) V_{DD}^2 + \frac{1}{2} J V_{DD}\right] fN \end{aligned} \tag{2.28}$$

It is evident from (2.27) and (2.28) that the TDC consumes significantly less power as compared with the single-stage TDC of the same dynamic range and resolution. It should be noted that the power consumption of the residual pulse extraction block including the delay blocks is not included in the preceding analysis. In our design, a set of simple delay blocks were used in order to extract the correct residual pulse of the coarse TDC. The simply configuration of these delay blocks is at the cost of power consumption, as to be seen later.

2.2.7 Silicon area consumption

If a single-step pulse-shrinking TDC is used to achieve the same resolution and dynamic range as those of the TDC, a total of MN pulse-shrinking stages with per-stage shrinkage ΔT_2 will be needed. The TDC, on the other hand, only needs $M + N$ pulse-shrinking stages. Note that $\Delta T_1 = N\Delta T_2$ is realized using $J_2 = J_1$ and $C_{x1} = NC_{x2}$. Let the silicon consumption of the load capacitor of the coarse and fine pulse-shrinking stages be A_{x1} and A_{x2}, respectively. Further, let the silicon consumption of readout DFFs be A_{DFF}. Neglect the silicon consumption of other logic gates for simplicity. Since $A_{x1} = NA_{x2}$, we have the total silicon consumption of the 1-step TDC

$$A_{\text{1-step}} = (A_{x2} + A_{DFF})MN. \tag{2.29}$$

The total silicon consumption of the TDC is given by

$$
\begin{aligned}
A_{\text{proposed}} &= (NA_{x2} + A_{DFF})M + (A_{x2} + A_{DFF})N \\
&= (M+1)NA_{x2} + (M+N)A_{DFF}. \qquad (2.30)
\end{aligned}
$$

It is seen that if A_{DFF} is smaller as compared with A_{x2}, then the TDC will consume comparable silicon as the 1-step TDC does. If A_{DFF} is large, the TDC will consume less silicon. It should be noted that if we choose $C_{x1} = C_{x2}$ and $J_f = NJ_c$, $\Delta T_{x1} = N\Delta T_{x2}$ will also hold. In this case, the silicon consumption of the TDC will be much lower as compared with that of the single-stage TDC.

2.2.8 Gain mismatch

The TDC uses a 2-step approach to achieve an improved resolution while minimizing silicon consumption. Similar to other TDCs, the TDC is subject to the gain error caused by the mismatch of per-stage shrinkage. Since the fine TDC digitizes the residue of the coarse TDC, the gain error of the coarse TDC will be reflected in the residue of the coarse TDC, specifically, the input of the fine TDC contains both a normal residue and a residue caused by the gain error of the coarse TDC. Clearly the latter will also be digitized by the fine TDC. The gain error of the fine TDC will directly affect the output of the fine TDC. Ideally the gain of the coarse TDC and that of the fine TDC should be identical. Any mismatch between them will introduce an error. Since the gain error of the TDC is due to the mismatch of per-stage shrinkage, minimizing the number of stage stages will reduce the gain error. Increasing transistor size of pulse-shrinking stages will also lower the gain error. To further minimize gain mismatch, the coarse and fine TDCs are calibrated separately to achieve $\Delta T_1 = N\Delta T_2$ where ΔT_1 and ΔT_2 are the resolution of the coarse TDC and that of the fine TDC, respectively, and N is the number of the stages of the fine TDC.

2.3 Time-Interleaved Pulse-Shrinking TDC

Two-step pulse-shrinking TDC is good for silicon and power consumption compared to the one-step pulse-shrinking TDC. However, it has a disadvantage in the conversion time explained in subsection 2.2.5. To improve the conversion time, a time-interleaved scheme is developed. The TDC uses a coarse pulse-shrinking TDC with a total of M stages of per-stage shrinkage ΔT_1 to quantize input time variable T_{in} and a fine pulse-shrinking TDC with a total of N stages of per-stage shrinkage ΔT_2 with $\Delta T_1 = N\Delta T_2$ to quantize the residual pulse of the coarse pulse-shrinking TDC. The residual pulse of the coarse TDC will only become available at the falling edge of T_{in}, as shown in Fig.2.7. The location and width of the residual pulse T_{res} constrained by $0 \leq T_{res} \leq \Delta T_1$ are therefore T_{in}-dependent.

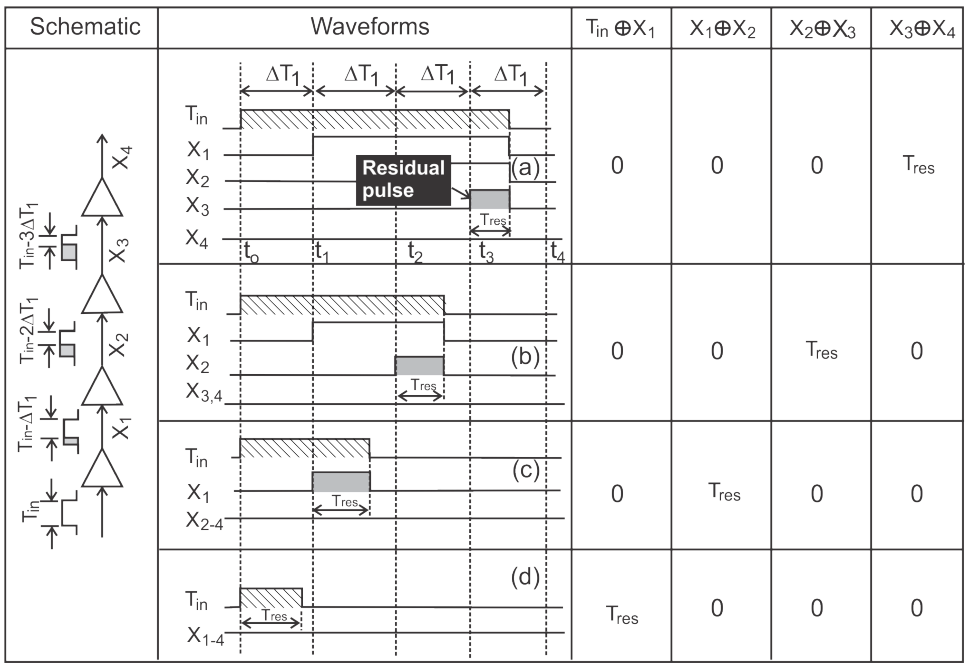

Figure 2.7: Residual pulse of coarse TDC. The location and width of the residual pulse T_{res} of the coarse TDC are determined by T_{in} and the residual pulse is only available at the falling edge of T_{in}.

For an input $\Delta T_2 < T_{in} < 4\Delta T_1$ in Fig.2.7, the pulse might vanish at the output of any of the delay stages of the TDC. If we assume that the pulse disappears at the output

of $(m+1)^{th}$ stage, we will have $X_m = 1$ and $X_{m+1} = 0$ where X_m and X_{m+1} are the output of mth and $(m+1)$th stages, respectively. A residual pulse will exist at X_m and become available at the falling edge of T_{in}. This residue pulse needs to be extracted and fed to the fine TDC for further digitization.

The simplified schematic of the time-interleaved pulse-shrinking TDC is shown in Fig.2.8 (A) with the schematic of the generic pulse-shrinking TDC shown in Fig.2.8 (B). The extraction of the residual pulse of the coarse pulse-shrinking TDC is performed by the residual pulse extraction logic. To demonstrate the operation of the residual pulse extraction, consider Fig.2.7(c) where the output of XOR gate with inputs X_1 and X_2 is 1 and others are 0. We have $T_{in,f1} = T_{in} \oplus X_1 + X_2 \oplus X_3 = 0$ and $T_{in,f2} = X_1 \oplus X_2 + X_3 \oplus X_4 = 1$ where $\oplus$ is the exclusive-OR operator. $T_{in,f1}$ and $T_{in,f2}$ are time inputs for a fine TDC1 and fine TDC2, respectively. For simplicity, we treat the data of T_{in} as a digital data although it is a time domain variable. Similarly, one can show in other cases of Fig.2.7, $T_{in,f1}$ and $T_{in,f2}$ are non-overlapping. Fig.2.9 plots the waveform of $T_{in,f1}$ and $T_{in,f2}$ for $T_{in} = 45$ ns.

In order to route the output of the chosen fine TDC to the DFFs using OR2 gates, the output of the other fine TDC needs to be set 0. This is achieved using the reset signal generation logic that consists of a pair of inverters and 2-to-1 multiplexers with selection signal T_{in}. When T_{in} is absent, both multiplexers select 0. Otherwise, MUX-1 selects $T_{in,f1}$ while MUX-2 selects $T_{in,f2}$. The output of the fine pulse-shrinking TDC is sampled by the DFFs at the rising edge of strobe signal $T_{strobe,f}$. Since the residual pulse of the coarse TDC is only available at its falling edge of T_{in}, a minimum time interval from the falling edge of T_{in} to the assertion of $T_{strobe,f}$ in order for the fine TDC to complete the digitization of the residual pulse of the coarse TDC is required to ensure that the output of the fine TDC is stable when $T_{strobe,f}$ is asserted.

The coarse and fine pulse-shrinking TDCs have 16 stages with $\Delta T_1 = 4.8$ ns and $\Delta T_2 = 296$ ps. To calibrate the TDC, a calibrating pulse of width 4.8 ns $\times$ 16=76.8 ns is fed to the coarse pulse-shrinking TDC. $V_{bias,c}$ is adjusted until a pulse width generated by XORing the output of the first pulse-shrinking stage and that of 15th pulse-shrinking delay stage becomes 72 ns. At this point, the coarse pulse-shrinking TDC is calibrated. With

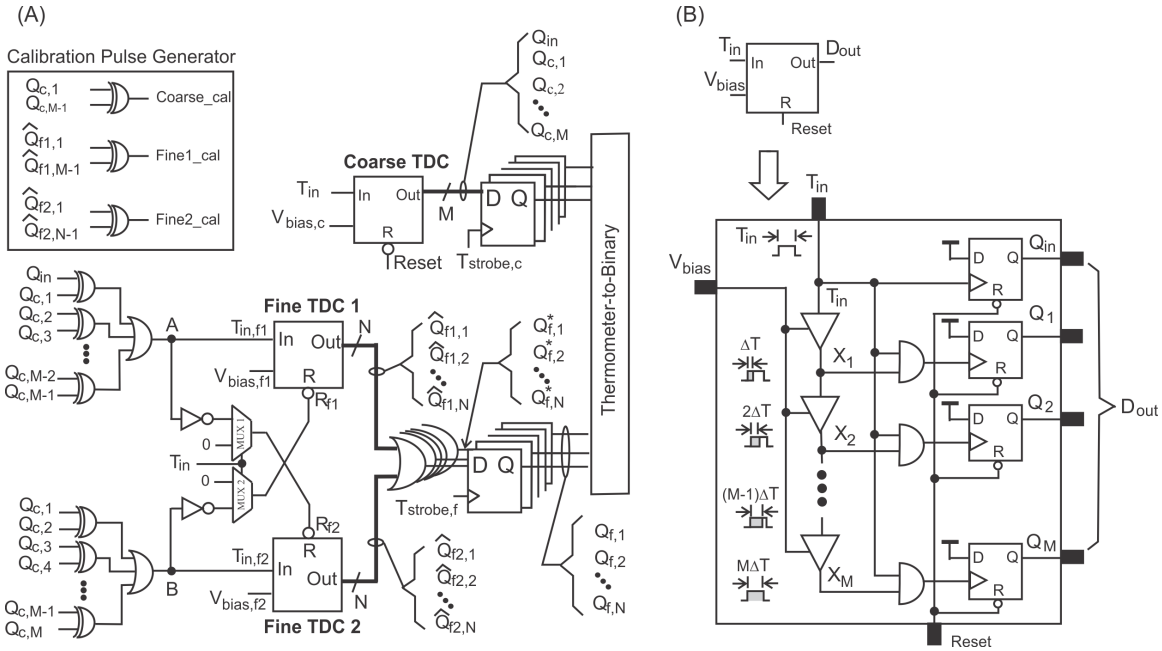

Figure 2.8: (A) Time-interleaved pulse-shrinking TDC. The pulse-shrinking stages of the coarse and fine TDCs have the same transistor dimensions but distinct capacitor loads. The load capacitance of the pulse-shrinking stages of the fine TDCs are from devices while that of the coarse TDC is an external 402 fF MiM capacitor. (B) Configuration of pulse-shrinking TDCs. The outputs of the coarse TDC are $Q_{c,1}$, $Q_{c,2}$, ..., $Q_{c,M}$ with the first subscript identifying the coarse TDC and the second subscript identifying the delay stage of the TDC. Q_{in} is the input of the coarse TDC. The outputs of the fine TDC are $Q_{f,1}$, $Q_{f,2}$, ..., $Q_{f,N}$ with the first subscript identifying the fine TDC and the second subscript identifying the delay stage of the TDC.

$V_{bias,c}$ kept unchanged, the fine pulse-shrinking TDCs are adjusted by varying $V_{bias,f1}$ and $V_{bias,f2}$ until both pulse widths generated from the calibration block becomes 4.5 ns. This process can be automated using a delay-locked loop, similar to that used in [6, 7].

2.4 Characteristics of Time-Interleaved Pulse-Shrinking TDC

In this section we examine the characteristics of the TDC. To provide a quantitative comparison, a single-step pulse-shrinking TDC that provides the same resolution and dynamic range, is utilized.

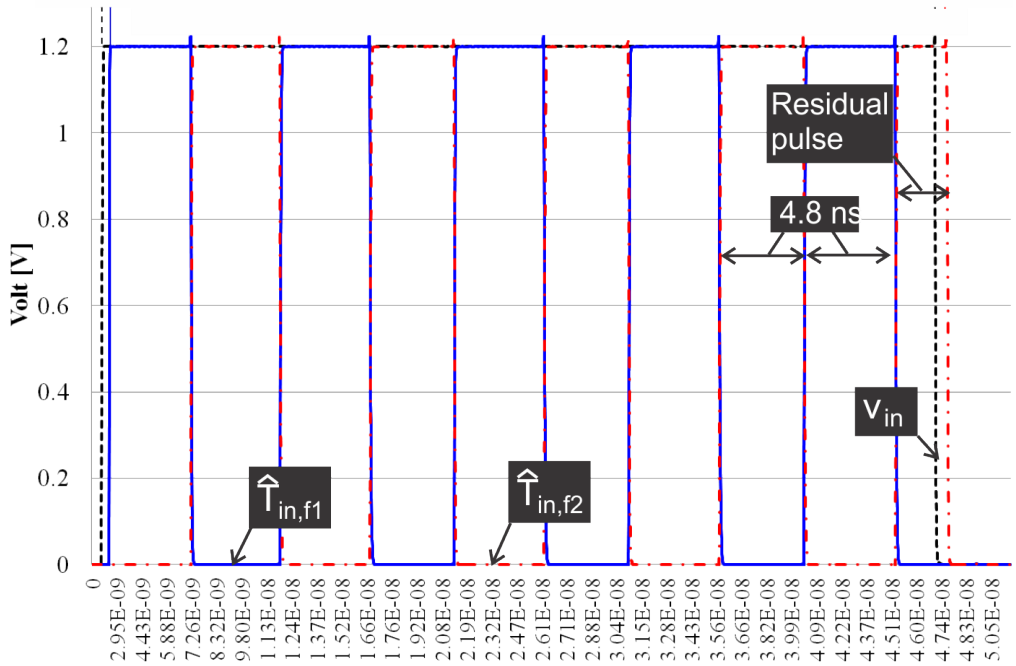

Figure 2.9: Non-overlapping waveforms of $T_{in,f1}$ and $T_{in,f2}$ for T_{in}=45 ns.

2.4.1 Silicon area consumption

We first examine the silicon consumption of the TDC. If a single-step pulse-shrinking TDC is used to achieve the same resolution and dynamic range, a total of MN pulse-shrinking stages with per-stage shrinkage ΔT_2 will be needed. The TDC, on the other hand, only needs $M + 2N$ pulse-shrinking stages, a significant reduction in silicon consumption is obtained especially when the number of the pulse-shrinking stages is large. In addition to fewer pulse-shrinking stages, fewer DFFs for readout are needed in the TDC. A total of MN readout DFFs will be needed for the single-step pulse-shrinking TDC. The number of DFFs needed for the TDC is only $M + 3N$. In the design presented in this work, $M = N = 16$. A total of 256 pulse-shrinking stages and 256 DFFs will be needed with an single-step pulse-shrinking TDC while only 48 pulse-shrinking stages and 64 DFFs are needed with the TDC.

2.4.2 Power consumption

For the purpose of simplicity, we neglect the effect of short circuit current that flows between pMOS and nMOS transistors as the input signal changes and leakage current. We will consider only one largest T_{in} case which is 76ns in this work. Therefore, we can assume the dynamic power is dominant. The average dynamic power consumption of an static inverter in an input period is given by $P = \alpha C_L V_{DD}^2 f$ where α is the activity factor, C_L is the load capacitance of the inverter and f is the frequency of the input of the inverter. In this analysis, α is average number per clock cycle when the clock goes one from zero. Therefore, α is 1 in the analysis. The time-interleaved pulse-shrinking TDC, especially fine TDC, will be activated always when each pulse-shrinking stage in the coarse TDC is activated. This is one of main differences compared to the conventional 2-step pulse-shrinking TDC explained in the previous chapter [**?**] which generates the residual pulse after the falling edge of T_{in}. Therefore, we can easily assume that this will consume more power than 2-step pulse-shrinking TDC since it is unknown when T_{in} will end, the two fine TDCs should be operated always. The total power consumption will be sum of the power consumption in the coarse TDC and the one in the fine TDC times the number of pulse-shrinking stage in the coarse TDC since the fine TDC is activated always.

$$P_{\text{proposedc}} = \alpha_c C_c V_{DD}^2 f. \tag{2.31}$$

$$P_{\text{proposedf}} = \alpha_f C_f V_{DD}^2 f(M). \tag{2.32}$$

$P_{proposedc}$ and $P_{proposedf}$ are the total power consumption in the coarse and fine TDC respectively given in the largest T_{in}. C_c and C_f are the capacitance used in the coarse and fine TDC respectively. M and N are the total number of pulse-shrinking delay cells used in the coarse and fine TDC respectively. α_c will be M and α_f will be N since α is an activity factor transitioning from zero to one in one period. M is the number of pulse-shrinking stage in the coarse TDC. Therefore, the total power consumption in the architecture is

$$P_{\text{proposed}} = (M)C_c V_{DD}^2 f + (N)C_f V_{DD}^2 f(M). \tag{2.33}$$

In the single-stage TDC, the total dynamic power consumption is

$$P_{\text{1-step}} = \alpha_1 C_f V_{DD}^2 f. \tag{2.34}$$

α_1 will be MN. If we design $C_f = C_c$, then the singe-stage TDC will be (MN)C_f V_{DD}^2 f and the TDC will be (M+MN)C_f V_{DD}^2 f. Therefore, the TDC will consume M times more. If we design C_c = NC_f, then the TDC will be 2MNC_f V_{DD}^2 f. However, in this case, the short circuit current in the coarse TDC will be higher than the fine TDC since the input signal's slope applied to the coarse TDC will be lower causing longer transition time compared to the fine TDC. Therefore, it will consume more power in either cases. This is the price pay for the faster conversion time compared to the single-stage TDC.

2.4.3 Mismatch-induced timing error

Similar to delay line TDCs, the resolution of pulse-shrinking TDCs is affected by the mismatch between pulse-shrinking stages. To simplify analysis, we assume that mismatches between pulse-shrinking stages is dominated by that of the discharge of the load capacitor. Since capacitance ratio in standard CMOS technologies can be made quite accurate, it is reasonable to assume that the mismatches of the discharge of the load capacitor are dominated by that the mismatch of the discharge current. With this in mind, let the mismatch between the discharge currents of pulse-shrinking stages be ΔI with $\Delta I \ll I$. Further let ΔI be normally distributed with a zero mean $\mu_I = 0$ and a non-zero standard deviation σ_I. In this case $v_x = V_{DD} - \frac{I+\Delta I}{C_x} t$. At $v_x = V_T$, making use of $1/(1+x) \approx 1 - x$ for $|x| \ll 1$, we

have

$$\Delta T + \delta T \approx \Delta T \left(1 - \frac{\Delta I}{I}\right) \tag{2.35}$$

where $\Delta T = \frac{(V_{DD}-V_T)C_x}{I}$. It becomes evident that mismatch-induced time error $\delta T \approx \Delta T \left(\frac{\Delta I}{I}\right)$ is directly proportional to ΔI and inversely proportional to I. If I is generated by a nMOS transistor biased in saturation, the current error due to W/L and V_{th} mismatches can be obtained as follows [34]

$$I = \frac{1}{2}\mu_n C_{ox} \left[\frac{W}{L} + \Delta\left(\frac{W}{L}\right)\right] (v_{GS} - V_{th} - \Delta V_{th})^2 \tag{2.36}$$

where $\Delta(W/L)$ and ΔV_{th} are dimension mismatch and threshold mismatch, respectively. Note that $\Delta(W/L) \ll W/L$, $\Delta V_{th} \ll V_{th}$, and $\Delta(W/L)$ and ΔV_{th} are assumed to be normally distributed with zero means and non-zero variances. Neglecting high-order terms, we arrive from (2.36)

$$I \approx \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right) (v_{GS} - V_{th})^2 \left(1 + \frac{\Delta(W/L)}{W/L} - \frac{2\Delta V_{th}}{v_{GS} - V_{th}}\right)$$

We thus have $\Delta I_{W/L} = I\left(\frac{\Delta(W/L)}{W/L}\right)$ and $\Delta I_{V_{th}} = -I\left(\frac{2\Delta V_{th}}{v_{GS}-V_{th}}\right)$ where $I = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_{th})^2$, $\Delta I_{W/L}$ and $\Delta I_{V_{th}}$ denote the current error due to W/L-mismatch and V_{th}-mismatch, respectively. The current error due to mismatches is given by

$$\Delta I = \sqrt{(\Delta I_{W/L})^2 + (\Delta_{V_{th}})^2} \tag{2.37}$$

To minimize ΔI, a large nMOS transistor with a large overdrive voltage should be used to generate the discharge current I.

Let us now consider a pulse-shrinking delay line with an input T_{in}. Let the mismatch of the discharge current of each pulse-shrinking stage be ΔI that is normally distributed with mean $\mu_I = 0$ and standard deviation σ_I. The mean of δT is given by $\mu_T = 0$. The

variance of δ_T is given by $\sigma_T^2 = (\Delta T)^2 \frac{\sigma_I^2}{I^2}$. The input of the second pulse-shrinking stage, denoted by $T_{in,2}$, is given by $T_{in,2} = T_{in} - (\Delta T + \delta T_1)$ where δT_1 denotes the time error caused by the current mismatch of stage 1. $T_{in,2}$ is fed to the second pulse-shrinking stage that also has a mismatch discharge current ΔI. It can be shown that the output of the second pulse-shrinking stage or the input of the 3rd pulse-shrinking stage, denoted by $T_{in,3}$, is given by $T_{in,3} = T_{in2} - (\Delta T + \delta T_2) = T_{in} - 2\Delta T - (\delta T_1 + \delta T_2)$. Note δT_1 and δT_2 are independent of each other. Continuing this process, one can show that the input of $(m+1)^{th}$ pulse-shrinking stage, denoted by $T_{in,m+1}$, is given by $T_{in,m+1} = T_{in} - m\Delta T - \Delta_{m+1}$ where $\Delta_{m+1} = \delta T_1 + \delta T_2 + ... + \delta T_m$. Since δT_j, $j = 1, 2, ...$, are independent of each other, we have the mean of Δ_{m+1} given by : $\mu_{\Delta_{m+1}} = 0$ and the variance of Δ_{m+1} given by :

$$\sigma_{\Delta_{m+1}}^2 = \sigma_{T_1}^2 + \sigma_{T_2}^2 + ... + \sigma_{T_m}^2 \tag{2.38}$$

If we further assume δT_1, δT_2, ... have the identical distribution profile, i.e., $\sigma_{T_1} = \sigma_{T_2} = ... = \sigma_{T_m} = \sigma_T$, it follows that $\sigma_{\Delta_{m+1}} = (\sqrt{m})\,\sigma_T$. The above results are similar to the jitter of ring oscillators given in [35, 36]. It is important to note $T_{in,m+1}$ decreases with the increase in the number of pulse-shrinking stages while $\sigma_{\Delta_{m+1}}$ increases with the number of pulse-shrinking stages. As a result, stage-wise measurement accuracy drops. This is illustrated graphically in Fig.2.10. The worst case is when all M stages of the coarse TDC and all N stages of the fine TDC are used. In this case, $\sigma_{\Delta_{M+N}} = \left(\sqrt{M+N-1}\right)\sigma_T$. In order to minimize mismatch-induced timing error, the number of pulse-shrinking stages should be kept at the minimum.

2.4.4 Conversion time

Conversion time is the time between the end of the input time interval and the moment when the measurement result is available at the TDC interface. If a single-stage pulse-shrinking TDC is used and the average propagation delay per stage is τ, the worst-case conversion time will be $\tau_{\text{1-step}} = \tau_{DFF}$ where τ_{DFF} is the delay of the DFF readout circuitry. For the TDC, the residual pulse extraction logic operates in synchronization with the coarse TDC, specifically immediately after the assertion of the rising edge of T_{in}, the rising edge of

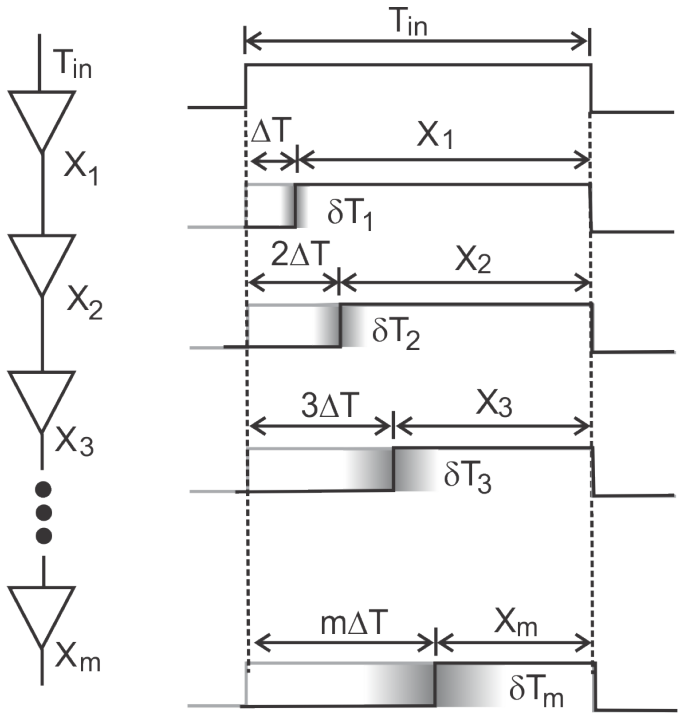

Figure 2.10: Mismatch-induced time error in pulse-shrinking TDCs.

$X_{c,j}$, $j = 1, 2, ..., M$ becomes available along with the propagation of the rising edge of T_{in} in the pulse-shrinking stages of the coarse TDC. As a result, the rising edges of $T_{in,f1}$ and $T_{in,f2}$ also become available and the fine TDC is activated. The preceding analysis shows that both the coarse and fine TDCs carry out the digitization of T_{in} simultaneously. This differs fundamentally from 2-step TDCs such as the one explained in the previous chapter in [**?**] where the residual pulse of the coarse TDC will only become available at the falling edge of T_{in} then it needs to be fed to the fine TDC. The worst-case conversion time of the TDC is therefore given by $\tau_{\text{proposed}} = \max\{M\tau_c, N\tau_f\} + 2\tau_{DFF}$ where τ_c and τ_f are the per-stage propagation delay of the coarse and fine TDCs, respectively. Note that we have neglected the delay of logic gates for extracting $T_{in,f1}$ and $T_{in,f2}$. Clearly, the conversion time of the TDC is a little bit bigger as compared with that of the single-stage TDC especially since it should consider DFF reset time and it has one more DFF groups. However, it is much smaller as compared with that of 2-step TDCs explained in the previous chapter [**?**].

2.4.5 Timing analysis

$T_{in,f1}$ and $T_{in,f2}$ in Fig.2.8 are the inputs of the fine TDCs. They should be non-overlapping ideally as shown in Fig.2.11. Strobing signal $T_{\text{strobe,f1}}$ and $T_{\text{strobe,f2}}$ that read the output of fine TDCs 1 and 2 should be asserted close to the falling edge of $T_{in,f1}$ and $T_{in,f2}$ respectively. In Fig.2.11(a), $Q_{f1,1-3} = 1$ and $Q_{f1,4-16} = 0$ when $T_{\text{strobe,f}}$ is properly asserted. If $T_{\text{strobe,f1}}$ is asserted earlier (Fig.2.11b), $Q_{f1,1-2} = 1$ and $Q_{f1,3-16} = 0$. As the output of the fine TDC is a thermometer code, $Q_{f1} = \underbrace{0...0}_{13}111$ (no early strobing) and $Q_{f1} = \underbrace{0...0\mathbf{0}}_{14}11$ (early strobing). The locations and number of erroneous bits are therefore set by the time displacement of the strobing signal.

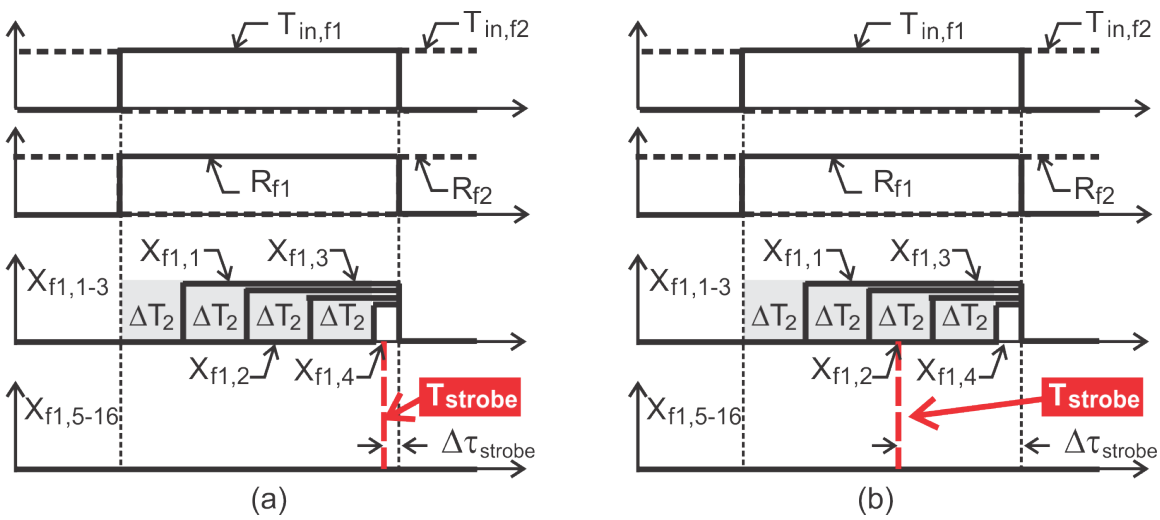

Figure 2.11: Strobing the output of fine TDC1. (a) Proper strobing. (b) Early strobing.

Mismatches between the propagation delay of the logic generating $T_{in,f1}$ and $T_{in,f2}$ and the pulse shrinking stages of the coarse TDC give rise to overlapping between $T_{in,f1}$ and $T_{in,f2}$. Consider the two cases shown in Fig.2.12 where $T_{strobe,f2}$ is asserted at the same time instant. It is seen in Fig.2.12(a) that $Q_{f1,1-2} = 1$ and $Q_{f1,3-16} = 0$ where in Fig.2.12(b), $Q_{f1,1-4} = 1$ and $Q_{f1,5-16} = 0$.

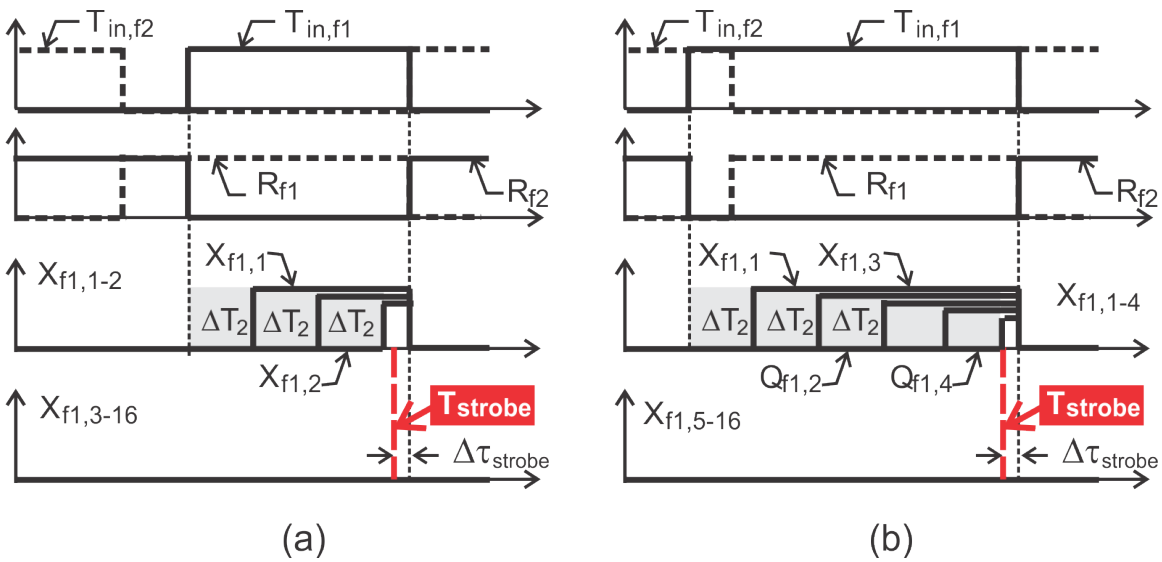

Figure 2.12: Strobing the output of fine TDC1 with T_{in} mismatch. (a) $T_{in,f1}$ has a mismatch-induced delay. (b) $T_{in,f2}$ has a mismatch-induced lead.

Mismatch between the reset paths of the fine TDCs also introduces errors. Consider Fig.2.13(a) where R_{f2} has a mismatch-induced delay. Although R_{f2} only affects the reset of fine TDC 2, the delayed reset of fine TDC 2 might affect the overall output of the fine TDCs. This is because $Q_f^* = \hat{Q}_{f1} + \hat{Q}_{f2}$. In Fig.2.13(b) where R_{f1} has a mismatch-induced delay. It is seen that R_{f1} affects the reset of fine TDC 1. The output in this case is $Q_{f1,1-2} = 1$ and $Q_{f1,3-16} = 0$ rather than the correct $Q_{f1,1-3} = 1$ and $Q_{f1,4-16} = 0$.

2.4.6 Jitter

To estimate the jitter of the output of a pulse-shrinking delay cell, we follow the approach for the jitter analysis of ring oscillators presented in [33]. Refer to Fig.2.14, let v_n denote the noise stored in C_x driven by the previous stage of the pulse-shrinking stage. For the purpose of simplicity, we neglect the effect of switching noise. The power of v_n denoted by $\overline{v_n^2}$ is given by $\overline{v_n^2} = kT/C_x$ where k is Boltzmann constant and T is temperature in degrees kelvin. It can be shown that the jitter of v_o or the variance of ΔT_j, denoted by σ_j^2, is obtained from

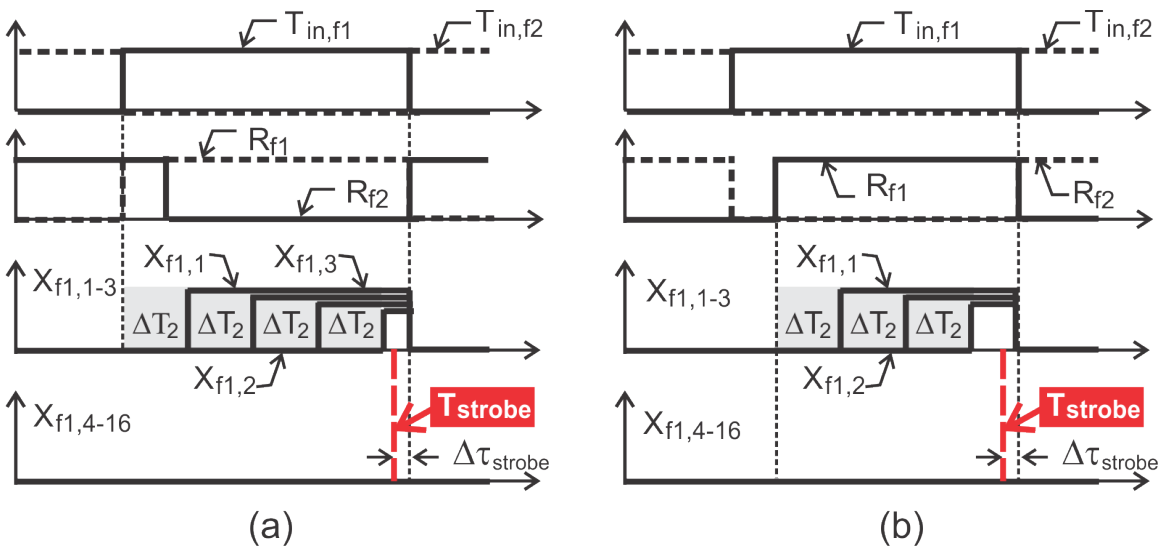

Figure 2.13: Strobing the output of fine TDC1 with reset mismatch. (a) R_{f1} has a mismatch-induced delay. (b) R_{f2} has a mismatch-induced delay.

$$\sigma_j^2 = \frac{(\Delta T_x)^2}{V_{DD}^2}\overline{v_n^2} = \frac{kT}{C_x}\frac{(\Delta T_x)^2}{V_{DD}^2} \tag{2.39}$$

Since $\Delta T_x = (C_x/I)V_{DD}$, we have

$$\sigma_j^2 = \frac{kT}{V_{DD}}\frac{\Delta T_x}{I} \tag{2.40}$$

It is seen from (2.40) that σ_j is directly proportional to discharge time ΔT_x and inversely proportional to discharge current I. ΔT_x of the coarse pulse-shrinking stage is larger than that of the fine pulse-shrinking stage. Note that both have the same discharge current in order to minimize power consumption. As a result, the jitter of the coarse TDC will be larger as compared with that of the fine TDCs. If we assume that the jitter of pulse-shrinking stages is uncorrelated and it contributes equally to the output jitter, the overall jitter of the one step pulse-shrinking TDC that has a total of MN pulse-shrinking stages of per-stage shrinkage ΔT_2 is obtained from $\sigma_{\text{1-step}}^2 = (MN)\sigma_f^2$. Similarly, the overall jitter of the TDC is given by $\sigma_{\text{proposed}}^2 = M\sigma_c^2 + N\sigma_f^2$ where σ_c^2 and σ_f^2 are the power of the jitter of the coarse pulse-shrinking stage and fine pulse-shrinking stage, respectively. Since the discharge

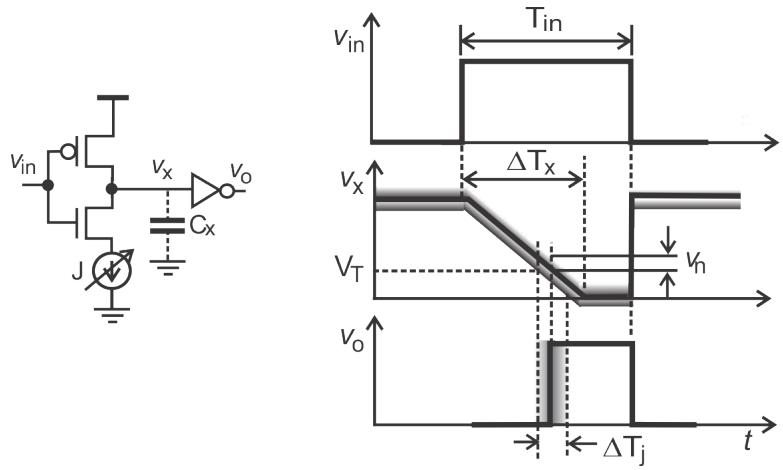

Figure 2.14: Jitter of pulse-shrinking stages.

time in the coarse pulse-shrinking stage is N times that of the fine pulse-shrinking stage, $\sigma_c^2 = N\sigma_f^2$ follows. We therefore have $\sigma^2_{\text{proposed}} = (M+1)N\sigma_f^2$. For the TDC presented in this work, $M = N = 16$, we have $\sigma^2_{\text{proposed}} = 272\sigma_f^2$ and $\sigma^2_{\text{1-step}} = 256\sigma_f^2 = 0.94\sigma^2_{\text{proposed}}$. The preceding results reveal that the jitter of the TDC is comparable to that of the 1-step pulse-shrinking TDC.

2.5 Simulation and Measurement Results

A 4-bit two-step TDC consisting of a 4-stage coarse TDC with per-stage shrinkage 1 ns and a 4-stage fine TDC with per-stage shrinkage 250 ps and a 8-bit time-interleaved pulse-shrinking delay-line TDC consisting of a 16-stage coarse pulse-shrinking TDC of per-stage shrinkage 4.8 ns and two 16-stage fine pulse-shrinking TDCs of per-stage shrinkage 0.3 ns were designed in an IBM 130 nm 1.2 V CMOS technology. The chip photo of both pulse-shrinking delay-line TDCs are shown in Fig. 2.15. A total of 18 and 20 bonding pads were used in the two-step TDC and the time-interleaved TDC, respectively. The total silicon area including the bonding pads is 1 mm $\times$ 1 mm both. The filling metals for satisfying density design rules were configured in such a way that they formed a large decoupling capacitor between V_{DD} and V_{SS} rails. MiM decoupling capacitors were also used between V_{DD} and V_{SS} rails to minimize the effect of switching noise.

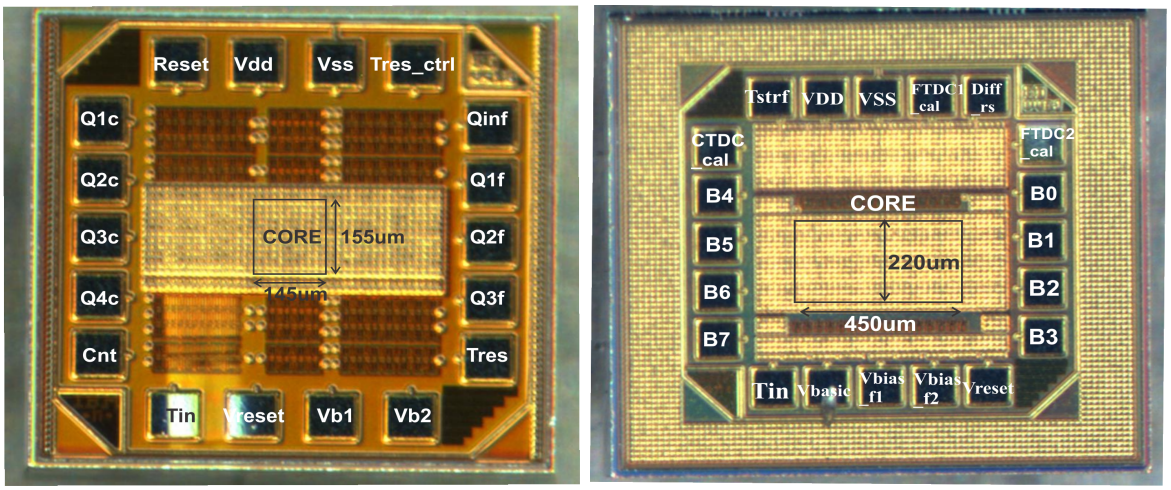

Figure 2.15: Die micrograph of the 4 bit two-step pulse-shrinking TDC (left) and that of the 8 bit time-interleaved pulse-shrinking TDC including a thermometer-to-binary encoder (Right). The core area of the two-step TDC : 145 μm x 155 μm. The core area of the time-interleaved TDC : 450 μm x 220 μm.

2.5.1 Simulation results of two-step pulse-shrinking TDC

The simulated differential nonlinearity (DNL) of the two-step TDC in the nominal process condition is shown in Fig.2.16(top). It is seen that in the normal process conditions, the DNL is approximately 0.5 LSB. The DNL of the TDC at SS and FF process corners is shown in Fig.2.16(bottom). It is seen that there is a missing code in SS corner. This is because of a negative gain error in the coarse TDC. The resolution becomes larger than the target resolution in SS corner. In this case, $T_{residue}$ can not be extracted properly due to the fixed delay line between the coarse and fine TDC. For example, if the target ΔT_1 is 1 ns and the measured coarse TDC resolution is 1.2 ns, the transmission gate at the extraction logic will be turned off 1.2 ns later. However, since the delay of the delay line is 1 ns, 0.2 ns time information can go to the fine TDC. If this is greater than the resolution of the fine TDC, it will generate one LSB and cause a DNL error. The simulated integral nonlinearity (INL) of the TDC in the nominal process condition and at SS and FF process corners are shown in Fig.2.17. It is seen that in the normal process conditions, the INL is approximately 0.5 LSB. At the process corners, the INL drops to approximately 1 LSB. Fig.2.18 shows the spectrum of the TDC. To simulate it, we designed a voltage-to-time converter by using a

current-starved inverter [22] with input range 90 ps to 4 ns. The simulation results show that ENOB is 3.16 bits. Fig.2.19 shows the results of Monte Carlo simulation with T_{in} set to 2.2 ns.

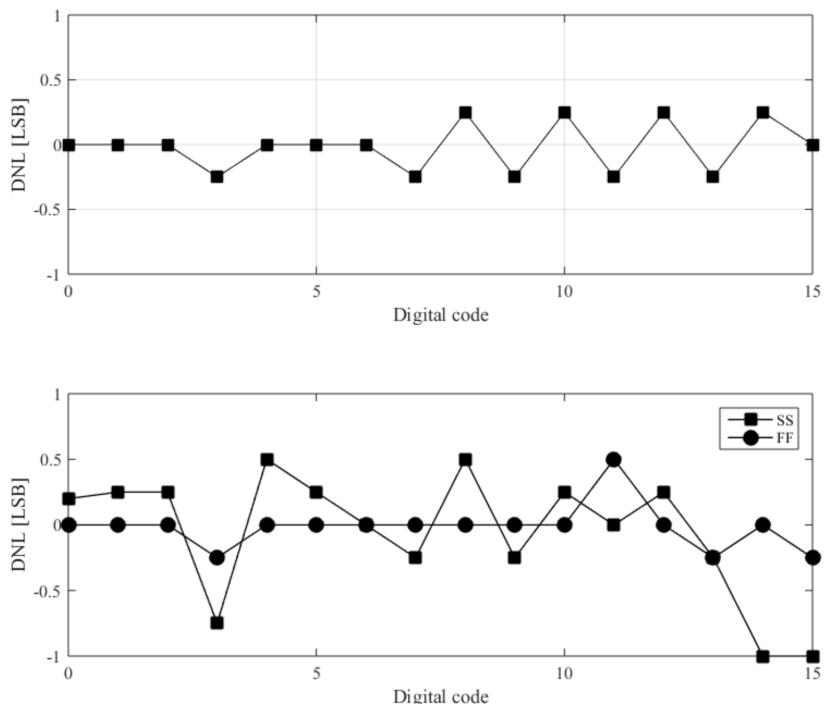

Figure 2.16: Simulated DNL of the TDC (post-layout). Top - Normal process condition. Bottom - SS and FF process corners.

The breakdown of the power consumption of the blocks of the TDC is : Delay block : 105 μW. Fine pulse-shrinking stages : 17.9 μW. Coarse pulse-shrinking stages : 9.5 μW. DFFs and reset : 29.8 μW. Residue pulse extraction : 20.2 μW. It is seen that a significant portion of the power consumption of the TDC comes from the delay block. The reason for the high level of power consumption of the delay block was explained earlier. Clearly a better residual pulse extraction method that consumes less power needs to be developed should power consumption is of a critical concern. The simulated conversion time is 1.4 ns. The conversion time of the TDC consists of three components : the delay of the 4-to-1 multiplexer τ_{MUX}, the delay of the DFFs τ_{DFFs}, and the maximum range of the input time variable of the fine TDC $\Delta T_1 = N\Delta T_2$. Since ΔT_1=1 ns, $\tau_{MUX} + \tau_{DFF} \approx 0.4$ ns.

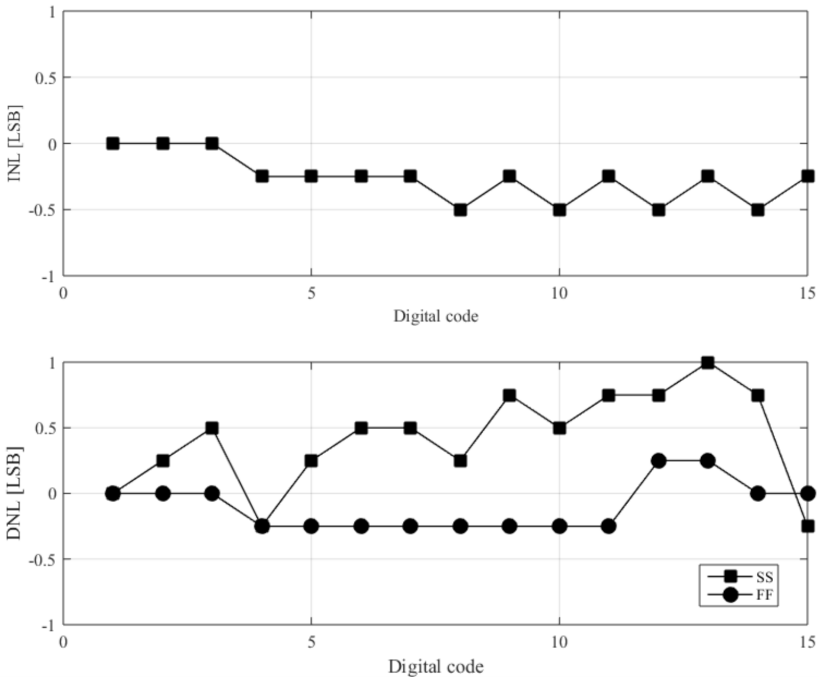

Figure 2.17: Simulated INL of the TDC (post-layout). Top - Normal process condition. Bottom - SS and FF process corners.

2.5.2 Measurement results of two-step pulse-shrinking TDC

The designed chip was fabricated and packaged with surface-mount, 20 gull-wing leads from Spectrum Semiconductor Materials Inc. The fabricated was mounted on a FR4 printed circuit board. The test setup is shown in Fig.2.20. An Agilent B1130A pattern generator was used to provide T_{in}. An Agilent 16851A logic analyzer was used to capture the digital output of the TDC. The single-ended flying leads of the logic analyzer were connected to the output of the TDC directly. DC voltages including supply voltage and tuning voltages of the coarse TDC and that of the fine TDC were from a BK 9130 multi-channel DC power supply. An Agilent 33250A arbitrary waveform generator was used to provide the reset signal for all DFFs. Ideally the reset signal should be generated on chip directly with its source from the pattern generator so as to avoid timing difficulty.

The TDC was calibrated manually. A known time variable from a precision pulse generator was applied to the TDC. The difference between Q_{1c} and Q_{3c} of the coarse TDC was measured using a logic analyzer. This value should be $2\Delta T_1$ ideally. If a difference was

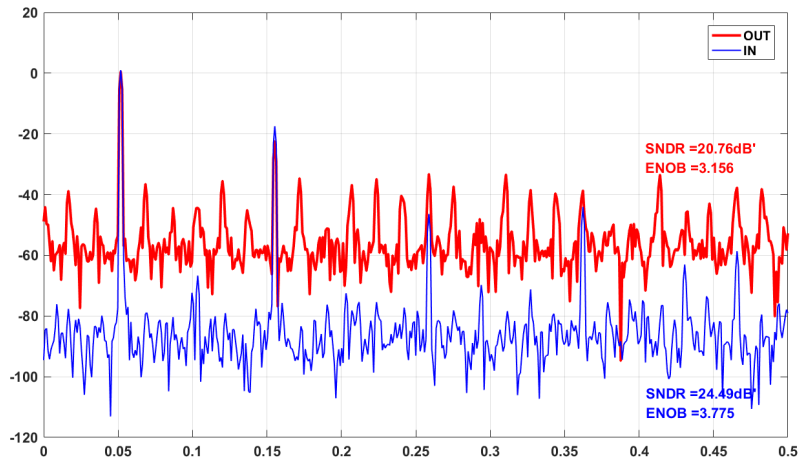

Figure 2.18: Simulated spectrum the TDC (post-layout). Input : Sinusoid of 5.176 MHz @f_s = 100 MHz.

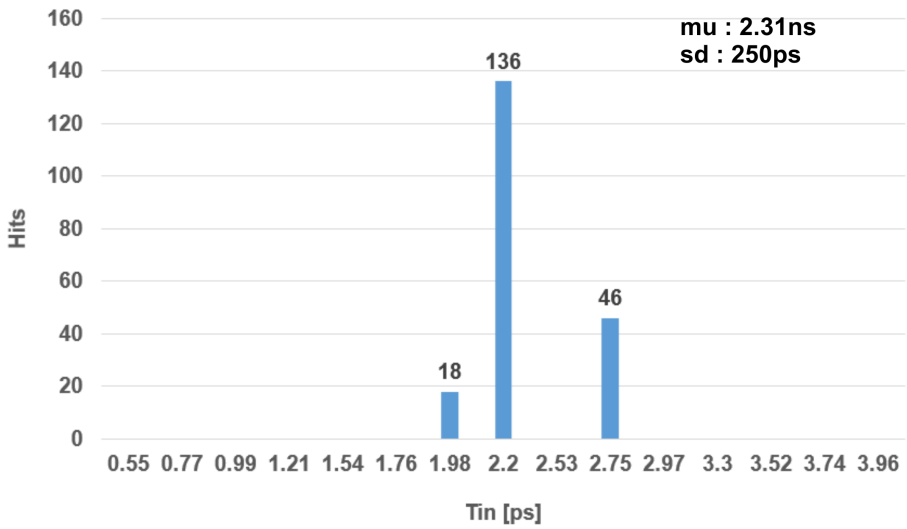

Figure 2.19: Monte Carlo simulation results when T_{in} = 2.2 ns (200 samples).

observed, the per-stage time shrinkage of the coarse TDC was tuned by varying its biasing voltage. Similarly, for the fine TDC, we measured the difference between Q_{1f} and Q_{3f}. This value should be $2\Delta T_2$ ideally. If a difference was observed, the per-stage time shrinkage of the fine TDC was tuned by varying its biasing voltage. Only when both the coarse and fine TDCs were calibrated, the calibration of the TDC was completed.

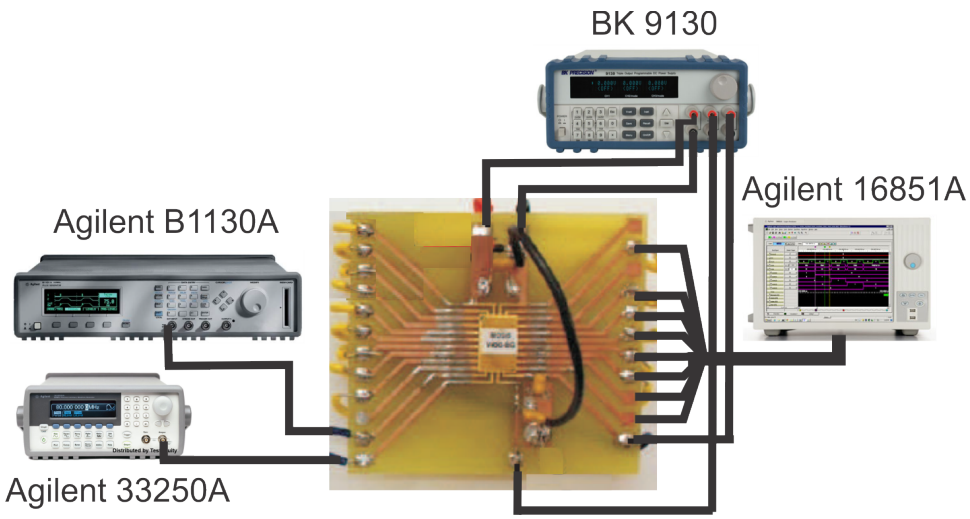

Figure 2.20: Test setup of the two-step pulse-shrinking TDC (PCB with SMA connectors for connecting to test equipment not shown).

The measured pulse shrinkage of the coarse pulse-shrinking stage of the TDC on its biasing voltage V_{b2} is shown in Fig.2.21(top). It is seen that the influence of V_{b2} on the amount of pulse shrinkage diminishes when V_{b2} exceeds 0.8V. This is because when $V_{b2} > 0.8$V, the nMOS transistor enters the triode mode of operation while when $V_{b2} < 0.8$V, it is in saturation. It is also seen that the minimum amount of pulse shrinkage is approximately 4.5 ns, well above 1 ns, the per-stage pulse shrinkage of the coarse TDC, indicating that a static time offset of 4.5 ns exists. The static time offset is caused by the delay of the output buffer for reading the output of the coarse TDC and associated PCB that connects the output buffer to the test equipment. This static timing error can be removed via calibration. For example, if we introduce a timing offset of 4.5 ns, the dependence of the pulse shrinkage of the coarse pulse-shrinking stage on bias voltage is shown in Fig.2.21(bottom). It is evident from Fig.2.21 that the per-stage shrinkage of the coarse TDC can now be tuned between 0 and 1 ns. Also observed is that the hyperbolic profile of the measured dependence of the pulse shrinkage of the coarse pulse-shrinking stage on bias voltage. Due to the process defects of the fabricated chip, especially in the delay line, we were unable to measure the dependence of the pulse shrinkage of the fine pulse-shrinking stage on bias voltage. To have an accurate delay line for accuracy, we can use a delay-locked loop (DLL) since it is good for skew control. However, in this case, we need to consider increasing silicon and power

consumption since DLL needs a reference clock signal and control logic to control enable / disable DLL block.

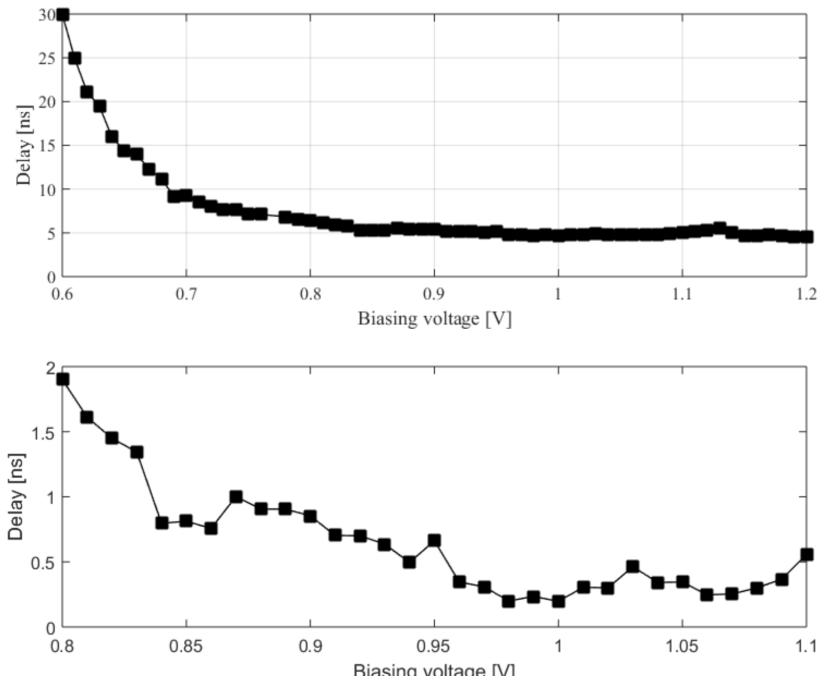

Figure 2.21: Measured dependence of the pulse shrinkage of the coarse pulse-shrinking stage on bias voltage. Top - Without offset calibration. Bottom - With 5ns offset calibration.

2.5.3 Simulation results of time-interleaved pulse-shrinking TDC

The simulated DNL and INL of the TDC in the nominal process condition are shown in Fig.2.22 (A) and (B). The largest DNL and INL are found to be ±0.285 LSB and 0.785 LSB, respectively. Fig.2.22 (C) shows the results of Monte Carlo simulation with T_{in} set to 15 ns.

2.5.4 Measurement results of time-interleaved pulse-shrinking TDC

The designed chip was fabricated and was mounted on a FR4 printed circuit board. The test setup is shown in Fig.2.23.

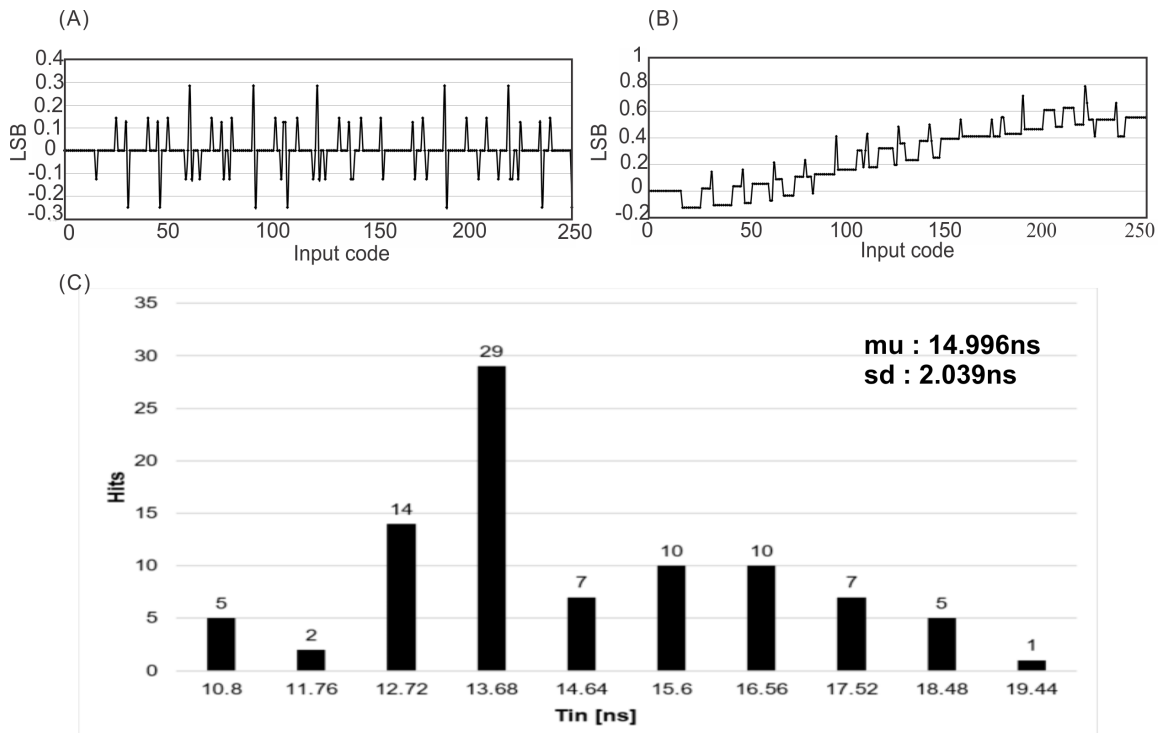

Figure 2.22: (A) Simulated DNL (post-layout), (B) Simulated INL (post-layout), (C) Monte Carlo simulation results when T_{in} = 15 ns (90 samples).

The measured transfer characteristics of the TDC over the input range 0-70 ns is shown in Fig.2.24, along with the ideal transfer characteristic for reference. It is seen that the measurement result of the output of the TDC generally agree with the desired characteristics of the TDC. Two periodic abnormal increases, one by 16 and the other by 10 approximately, exist in the measured output of the TDC. Both have a period of 9.6 ns approximately. The increase of 10 occurs approximately at the mid-point between two increases of 16. These irregularities are caused by the timing mismatches between $T_{in,f1}$ and $T_{in,f2}$ and that between R_{f1} and R_{f2}. We notice that the per-stage pulse-shrinkage of the coarse TDC is 4.8 ns and the coarse TDC has 16 pulse-shrinking stages. The outputs of the residual extraction logic blocks $T_{in,f1}$ and $T_{in,f2}$ are a total of eight 50% duty cycle non-overlapping pulses with period 9.6 ns if T_{in} takes the full-range value of the input of the TDC (76.8 ns). The overlapping of $T_{in,f1}$ with $T_{in,f2}$ and that of R_{f1} with R_{f2} will cause $T_{in,f1}$ and $T_{in,f2}$ to deviate from their nominal values at their rising or falling edges, 4.8 ns apart in the nominal condition. The variation of $T_{in,f1}$ with $T_{in,f2}$ are digitized by the fine TDCs, resulting in the periodic irregularities in

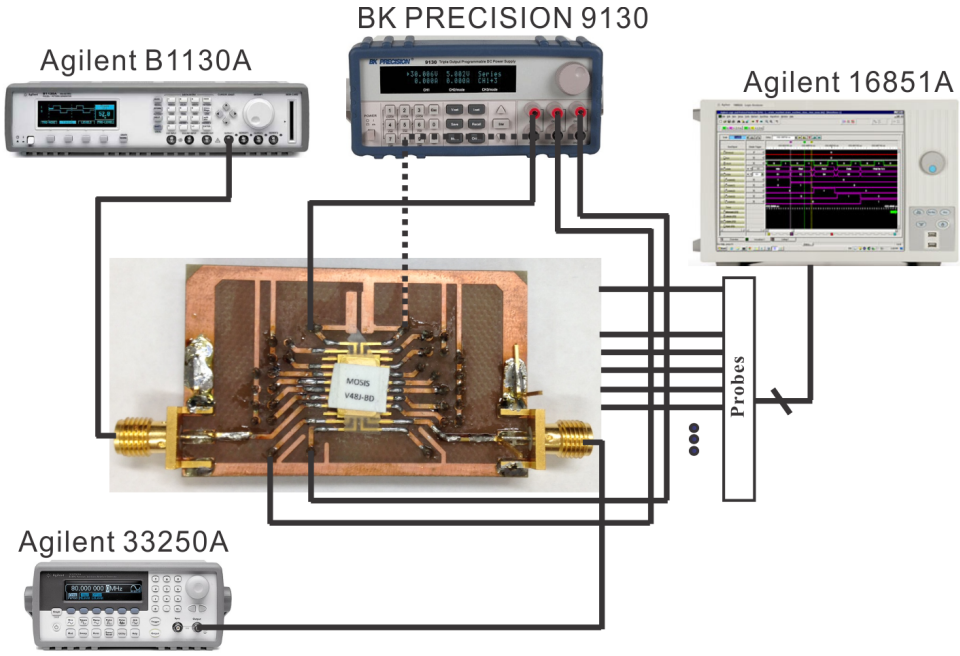

Figure 2.23: Test setup of the time-interleaved pulse-shrinking TDC. An Agilent B1130A pattern generator was used to generate T_{in} and an Agilent 16851A logic analyzer was used to capture the digital output of the TDC. Three DC voltages, namely $V_{\text{bias,c}}$, $V_{\text{bias,f1}}$, and $V_{\text{bias,f2}}$ for tuning the discharge current of the coarse and fine TDCs so as to obtain the desired per-stage pulse shrinkage are from a BK 9130 multi-channel DC power supply.

the transfer characteristics of the TDC. The overlaps of $T_{in,f1}$ with $T_{in,f2}$ and R_{f1} with R_{f2} are observed in Fig.2.25 (A) where the screen shot of the output of the logic analyzer that captures the digital outputs of the TDC for $T_{in} = 70$ ns is shown. Since only one buffer was designed and implemented for probing $T_{in,f1}$, only $T_{in,f1}$ is captured and shown in the figure. The waveform of $T_{in,f1}$ has 8 pulses spaced by 9.6 ns approximately, indicating that the even pulse-shrinking stages of the coarse TDC are also activated. The detrimental effect caused by the overlapping of $T_{in,f1}$ and $T_{in,f2}$, and that of R_{f1} and R_{f2} reveals the importance that any overlapping between $T_{in,f1}$ and $T_{in,f2}$, that between R_{f1} with R_{f2} should be removed. This can be achieved using cross-coupled OR2 gates, i.e., a RS-latch whose outputs are Q and $\overline{Q}$ and are non-overlapping. This non-overlapping prevention scheme, unfortunately, was not implemented in our design. As a result, mismatch-induced errors exist in the output of the TDC. Fig.2.25(B) shows the result of the multiple shots with oscilloscope's infinite persistence mode on.

The pulse width of $T_{in,f1}$, fine1$_{cal}$, and fine2$_{cal}$ in Fig.2.8 were measured using the logic analyzer and the results are shown in Fig. 2.27. Signal A ($T_{in,f1}$) shows the pulse width of the coarse TDC. $fine1_{cal}$ and $fine2_{cal}$ show the pulse width of the fine TDC1 and fine TDC2 including 15 stages, respectively. We also measured a pulse width in the coarse TDC by increasing T_{in} by 200 ps and measured the pulse width change of signal A, as shown in Fig. 2.27. The results show that there is a systematic error caused by a voltage drop due to the resistance of V_{ss} line. Fig. 2.28 shows the mechanism of this systematic error. Since each pulse-shrinking delay element is activated sequentially and the spacing between pulse-shrinking delay elements is 30 um, the voltage drop due to the resistance of the V_{ss} line is not negligible. As a result, per-stage pulse shrinkage is not constant.

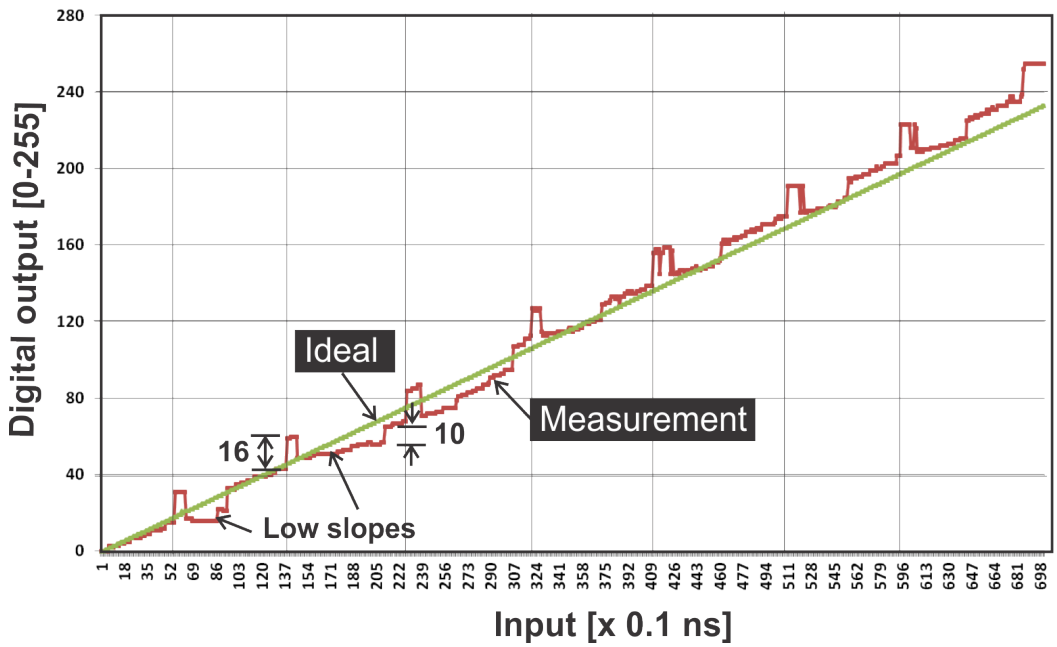

Figure 2.24: Measured transfer characteristics of TDC.

Major error sources are shown in Fig. 2.26. Error source [a] is a signal path mismatch of generating signals A and B. In this test chip, tdA is greater than tdB. This error causes non-uniform pulse-shrinkage in the coarse TDC shown in Fig. 2.27 (B) and MSB part error that is related to the increase of output code by 16 shown in Fig.2.24. Error source [b] is

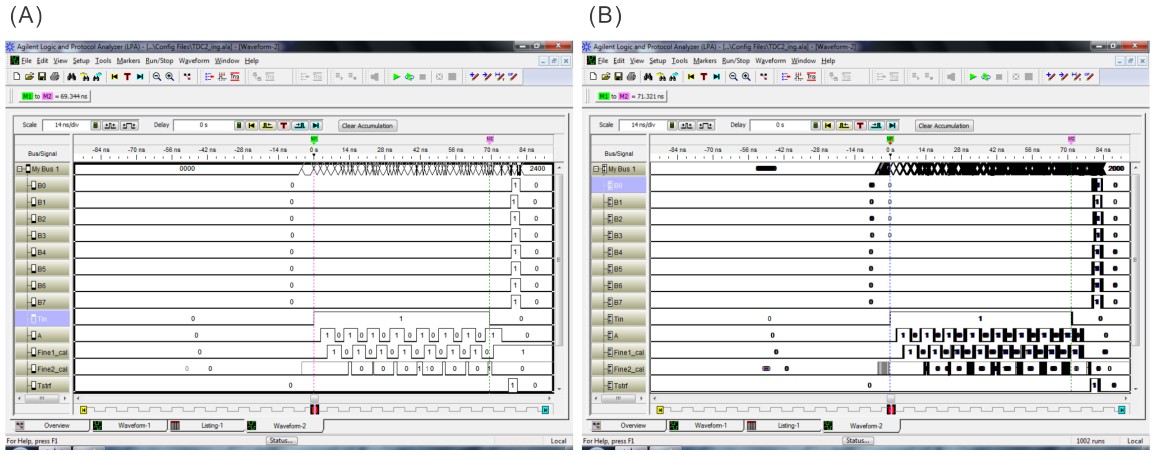

Figure 2.25: Screen shot of logic analyzer with T_{in} = 70ns. (A) Single shot, (B) Multiple shots with infinite persistence mode on.

a reset time mismatch between two fine TDCs. In this test chip, trst1 is larger than trst2. This error combining with error source [c] which is $T_{strobe,f}$ timing error causes LSB part error that is related to the increase of output code by 10 shown Fig. 2.24. Error source [3] is a $T_{strobe,f}$ timing error. Error source [d] is a propagation delay mismatch error for the residual signal fed to fine TDC1 or fine TDC2. Fig. 2.26 shows the output code when MSB error and LSB error occurs.

The following Figure-of-Merit (FoM)

$$\text{FoM} \quad = \quad \frac{P}{2^{\text{N}} \times f_s}. \tag{2.41}$$

where N = Bits - $\log_2$(INL + 1) is the effective number of linear bits, P is the power consumption, and f_s is the conversion rate is used to quantify the performance of the TDC on the basis of the amount of power consumption per conversion step [24]. Table 2.1 compares the performance of the TDC with that of some reported pulse-shrinking TDCs.

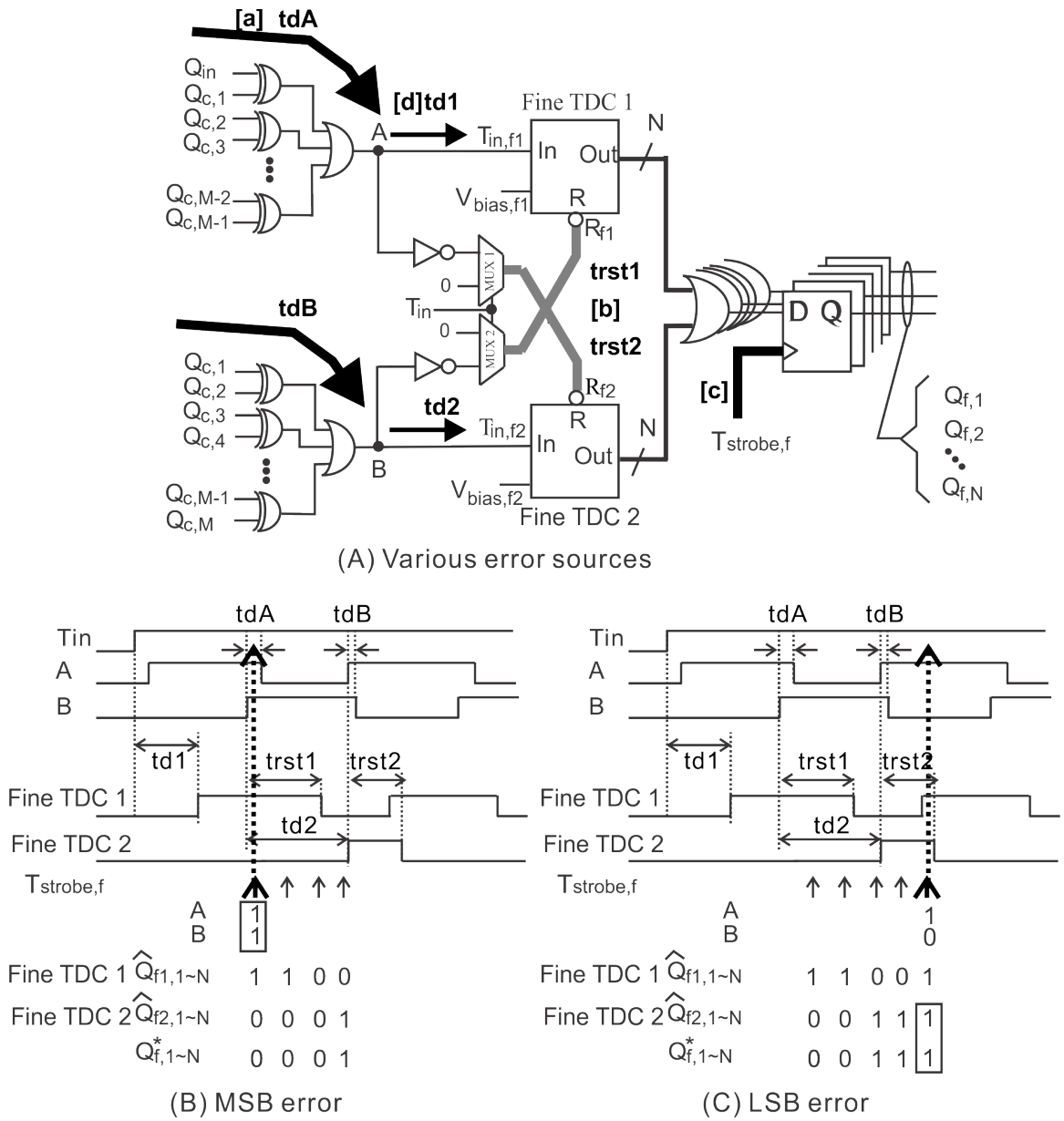

Figure 2.26: (A) Major error sources in the test chip. [a] Signal path mismatch. [b] Reset time mismatch. [c] $T_{strobe,f}$ timing error. [d] Propagation delay mismatch between two fine TDCs' input. (B) MSB error. (C) LSB error.

2.6 Chapter Summary

An area-efficient time-interleaved pulse-shrinking TDC with minimal conversion time was presented. The TDC consists of a 16-stage coarse pulse-shrinking TDC with per-stage shrinkage 4.8 ns and a pair of 16-stage fine pulse-shrinking TDCs with per-stage shrinkage 296

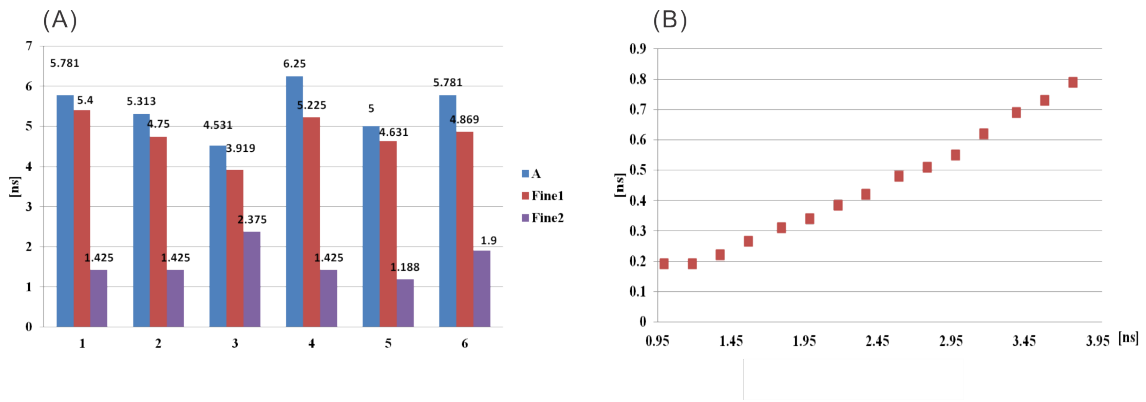

Figure 2.27: (A) Pulse width comparison. (B) Coarse TDC pulse shrinkage.

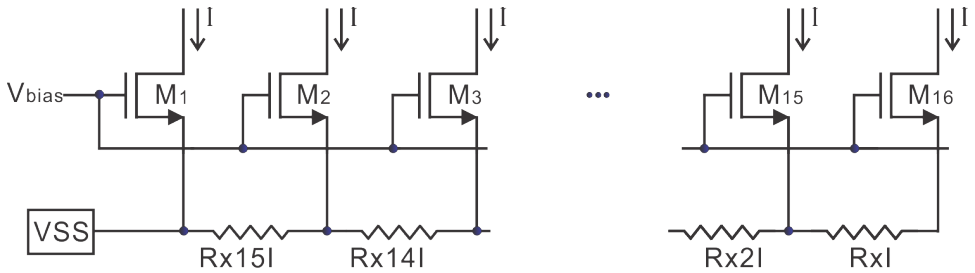

Figure 2.28: V_{ss} line resistance.

ps. The fine TDCs digitize the residual time of the coarse TDC and are operated in a time-interleaved manner. The analysis and design of a two-step pulse-shrinking TDC consisting of a 4-stage coarse pulse-shrinking TDC with per-stage shrinkage 1 ns and a 4-stage fine pulse-shrinking TDC with per-stage shrinkage 250 ps was also presented. The characteristics of the both TDCs including mismatch and noise-induced timing errors, timing errors of delay blocks, conversion time, power consumption, and silicon consumption were investigated in detail. The TDC was implemented in an IBM 130 nm 1.2 V CMOS technology. Simulation results show that the TDC offers 0.296-76.8 ns dynamic range, 850 ps conversion time, 0.285 LSB differential nonlinearity, and 0.78 LSB integral nonlinearity while consuming 7 mW including output buffers. A distinct characteristic of the TDC is that both the coarse and fine TDCs carry out the digitization of input time variables immediately from the arrival of the rising edge of input time variables. This differs fundamentally from the two-step TDCs where the residual pulse of the coarse TDC, i.e, the input of the fine TDC, will only become

Table 2.1: Performance comparison of pulse-shrinking TDCs.

Parameters	[7]	[23]	[37]	[38]	[39]	This
Tech.	1.2 μm	0.065 μm	0.35 μm	0.065 μm	0.09 μm	0.13 μm
V_{DD}	5 V	1.2 V	3.3 V	1.2 V	1.2 V	1.2 V
Conversion rate	10 KHz	200 MHz	10 Hz	250 MHz	180 MHz	12.88 MHz
Resolution	780 ps	3.75 ps	40 ps	1.12 ps	4.7 ps	296 ps (*)
Linearity	50 ps	2.3 LSB	0.6 LSB	1.7 LSB	1.2 LSB	0.78 LSB (*)
Bits	6	7	10(**)	9	7	8
Power	15 mW	3.6 mW	1.65 μW	15.4 mW	3 mW	7 mW (*)
FoM (pJ/conv.step)	249	0.463	258	0.325	0.287	3.79
Chip size (mm^2)	7.25	0.02	0.025	0.14	0.02	0.099

* Resolution and Linearity results are coming from the simulation results. Power is the test chip measurement result including output buffers.
** Bits are calculated from the input range and the resolution.

available at the falling edge of input time variables at which the digitization carried out by the coarse TDC has already completed. The digitization of input time variables by the coarse TDC and the residual pulse of the coarse TDC by the fine TDCs are carried out simultaneously.

Chapter 3

1-1 MASH $\Delta\Sigma$ TDC

This chapter presents a differential cascode time integrator and its application in a 1-1 MASH $\Delta\Sigma$ TDC. The detrimental effect of the nonidealities of the modulator on its timing accuracy is analyzed. The remainder of the chapter is organized as follows : Section 3.1 introduces the proposed time integrator. Both single-ended and differential time integrators are presented. Section 3.2 presents the design of a 1-1 MASH $\Delta\Sigma$ modulator utilizing the proposed time integrator. In Section 3.3, the imperfections of the modulators and their detrimental effects are examined in detail. Issues critical to the operation of the proposed modulator are investigated in Section 3.4. The simulation results of a 1-1 MASH $\Delta\Sigma$ modulator realized in IBM 130 nm 1.2 V CMOS technology are presented in Section 3.5. The performance of the TDC is compared with that of recently published TDCs. Finally, the chapter is concluded in Section 3.6.

3.1 Time Integrator

3.1.1 Time adder

Time integration is realized using a pair of time adders that recursively accumulate the time variable to be integrated over a time interval. Fig.3.1 shows the schematic of the time adder [29]. The DFFs are reset when RST is asserted to ensure that the integration capacitor is fully charged at the beginning of an addition operation. When STR_1, STR_2, or both arrive, M2, M4, or both will operate in the saturation region and function as current

source(s) due to a large v_{DS}[1]. STP_1 and STP_2 whose value is set to 0 initially by RST are selected by the multiplexers. The discharge of the integration capacitor is halted once $\mathrm{STP}_{1,2} = 1$ are asserted. The two time inputs of the time adder T_{in1} and T_{in2} are the time duration from the rising edge of $\mathrm{STR}_{1,2}$ to that of $\mathrm{STP}_{1,2}$, respectively, as shown in Fig.3.2.

Consider the case where T_{in1} arrives first in $[t_1, t_2]$. It is followed by $[t_2, t_3]$ where an overlap between T_{in1} and T_{in2} exists and $[t_3, t_4]$ where T_{in1} ends while T_{in2} continues. When STR_1 arrives, the integration capacitor will start to discharge via M1-M2 path in $[t_1, t_2]$. If channel modulation is not accounted for, the discharge current will be constant and v_c will drop at constant rate $k = I/C$ where I is the discharge current when only one of the two identical discharge paths is activated. When STR_2 arrives in $[t_2, t_3]$, the integration capacitor will discharge via both M1-M2 and M3-M4 paths and v_c will drop at rate $2k$. At t_3 where $\mathrm{STP}_1 = 1$, discharge path formed by M1 and M2 will be disabled while that formed by M3 and M4 will remain active. v_c in this case will drop at rate k in $[t_3, t_4]$. Finally, when $\mathrm{STP}_2 = 1$ is asserted at t_4, $\overline{Q}_2 = 0$ will be set, eliminating discharge path M3-M4. As a result, v_c will remain unchanged. Discharge will resume once $\mathrm{ACK}_1 = 1$ is asserted at t_5. When v_c drops below $V_{DD}/2$, the threshold voltage of the load inverter, $v_{inv} = 1$ is set, marking the completion of one discharge cycle of the integration capacitor.

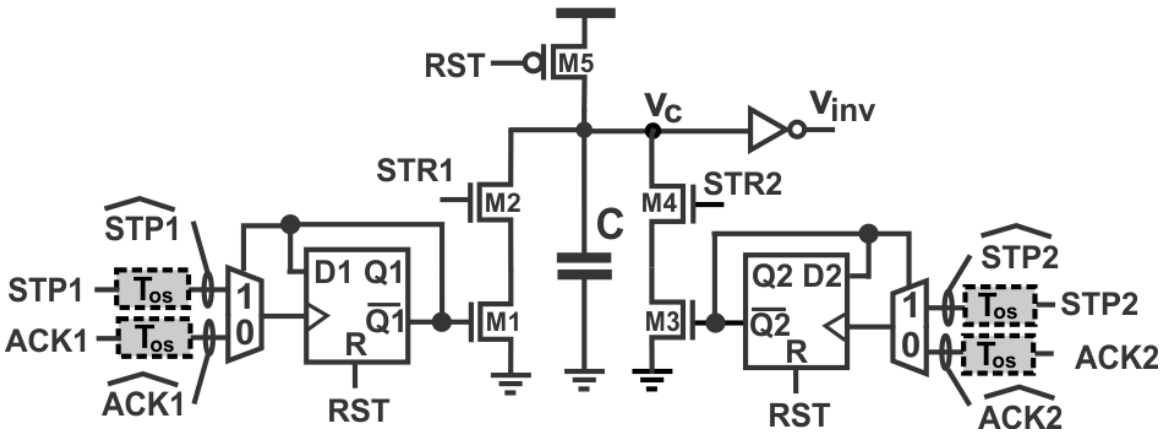

Figure 3.1: Time adder.

[1] v_{DS} at the onset of the discharge of integration capacitor is V_{DD} and that at the threshold crossing of the load inverter is $V_{DD}/2$.

To assist analysis, let T_{FS} be the time for v_c to drop from V_{DD} to $V_{DD}/2$ when only one of the two discharge paths is activated. In this work, T_{FS} is set to 1/2 of the duration of STR_1, denoted by T_s. Let T_{inv} be the time duration from the assertion of ACK_1 to the time instant at which $v_{inv} = 1$. Since $v_1 = V_{DD} - k\tau_{21}$ and $v_2 = v_1 - 2k\tau_{32}$ where τ_{ij} denotes the duration of time interval $[t_i, t_j]$, we have

$$v_3 = v_2 - k\tau_{43} = V_{DD} - k\left(T_{in1} + T_{in2}\right). \tag{3.1}$$

It follows that

$$T_{in1} + T_{in2} = \frac{1}{k}\left(V_{DD} - V_3\right). \tag{3.2}$$

$T_{in1} + T_{in2}$ is thus the amount of the time for v_c to drop from V_{DD} to v_3 with only one discharge path activated, as shown graphically in Fig.3.2. It is straightforward to show that

$$T_{in1} + T_{in2} = T_{FS} - T_{inv}. \tag{3.3}$$

$T_{in1} + T_{in2}$ is marked by the rising edge of v_{inv} and the falling edge of ACK_1. Since the rising edge of ACK_1 lags that of STR_1 by T_{FS}, $T_{in1} + T_{in2}$ is also marked by the rising edge of v_{inv} and that of $\overline{\mathrm{STR}}_1$.

It should be noted that the rising edge of STR should lead that of STP, corresponding to $T_{in} > 0$, in order for the time adder to function properly. If $T_{in} < 0$, a delay stage with delay $T_{os} > T_{in}$ needs to be employed to delay STP such that STR will lead $\widehat{\mathrm{STP}}$, the delayed version of STP, as shown in Fig.3.3. The value of T_{os} should be set in such a way that $\hat{T}_{in}[n] = T_{in}[n] + T_{os} > 0, \forall n$ holds.

3.1.2 Time register

The preceding time adder can be utilized to construct a time register that stores the input and exports the stored input upon a readout request. Specifically, if we ground one of the two inputs of the time adder while routing the time input to the other input of the time

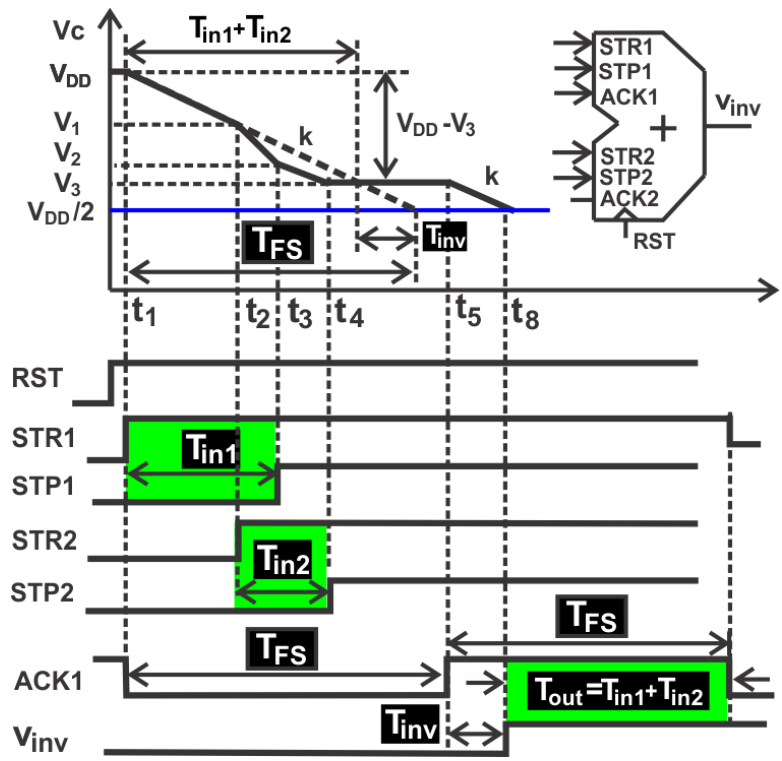

Figure 3.2: Timing diagram of time adder.

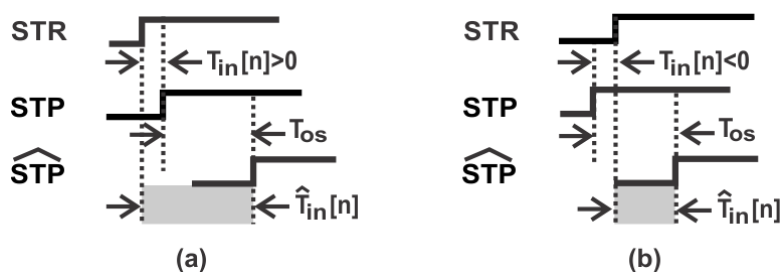

Figure 3.3: Polarity of time variables. (a) $T_{in}[n] > 0$. (b) $T_{in}[n] < 0$. $\hat{T}_{in}$ is measured from the rising edge of STR to that of $\widehat{\text{STP}}$.

adder, as shown in Fig.3.4, the time adder will function as a time register with the stored time variable marked from the rising edge of v_{inv} to that of $\overline{\text{STR}}_1$. The time register realizes $T_{in1} + T_{in2} = T_{in1} + 0 = T_{in1}$.

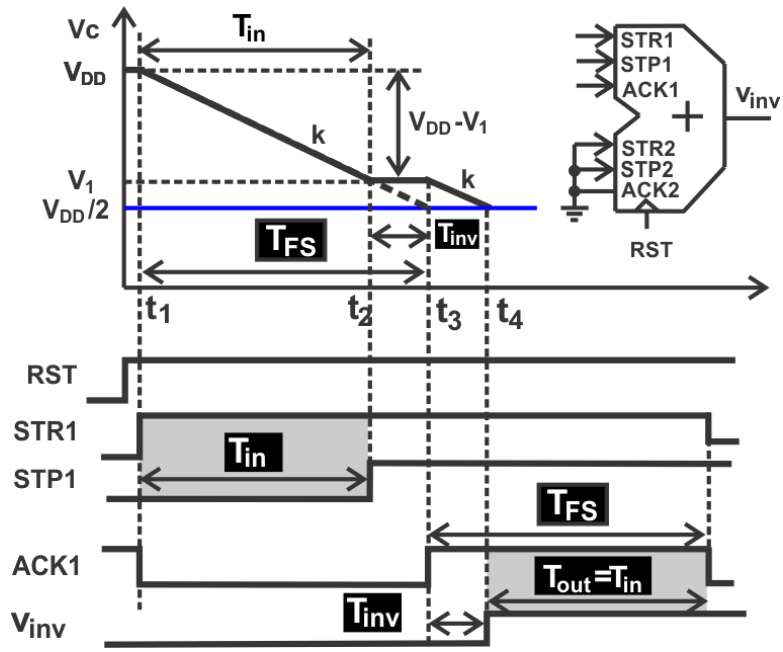

Figure 3.4: Time register.

3.1.3 Single-ended time integrator

Integration of time variable T_{in} over K clock cycles performs $\sum_{k=1}^{K} T_{in}[k]$. Each integration operation consists of a time addition operation that performs $\sum_{k=1}^{j} T_{in}[k] = T_{in}[j] + \sum_{k=1}^{j-1} T_{in}[k]$ and a time registration operation that stores $\sum_{k=1}^{K} T_{in}[k]$. Fig.3.5 shows the schematic of the time integrator. Time addition is performed at the rising edge of STR_a and time registration is conducted at the falling edge of STR_a. ACK_a is a periodic pulse with pulse width T_{FS} and arising edge ahead of the falling edge of STR_a by T_{FS}. The duration of $\mathrm{ACK}_a = 1$ is set to T_{FS} that is sufficiently long such that the integration capacitor will discharge to $V_{DD}/2$ after $\mathrm{ACK}_a = 1$ is asserted. The integration capacitor of the time register starts to discharge when $\overline{\mathrm{STR}}_a$ is asserted. Since the rising edge of $\overline{\mathrm{STR}}_a$ might lag that of STP_r, i.e., $T_{in}[n] < 0$ while the operation of the time adder requires a positive time variable, an auxiliary delay cell with delay $T_{os} > \max\{\sum_{k=1}^{n} T_{in}[k]\}$ is employed to delay STP_a such that $\widehat{\mathrm{STP}}_a$ always lags $\overline{\mathrm{STR}}_a$[2]. ACK_a is also delayed by T_{os} in order to accommodate $\overline{\mathrm{STR}}_a$. Since the duration from the rising edge of $v_{inv,a}$ to the falling edge of $\widehat{\mathrm{ACK}}_a$ is $T_{os} + T_{in}[n]$

[2]When the time integrator is used in a $\Delta\Sigma$ modulator, the error signal $T_{err}[n] = T_{in}[n] - T_{FB}[n]$ to be integrated can be either positive or negative.

while the falling edge of ACK_a is aligned with that of STR_a, the duration between the rising edge of $v_{inv,a}$ and that of $\overline{\mathrm{STR}}_a$ is $T_{in}[n]$. In the second half of STR_a where $\mathrm{STR}_a = 0$, since $\overline{\mathrm{STR}}_a$ lags $v_{inv,a}$, $v_{inv,a}$ is delayed by T_{os} so that $\overline{\mathrm{STR}}_a$ leads $\widehat{\mathrm{STP}}_r$, enabling the register to function properly. The input of the time register is from the rising edge of $\overline{\mathrm{STR}}_a$ to that of $\widehat{\mathrm{STP}}_r$, which is $T_{os} - T_{in}[n]$. ACK_r is also delayed by T_{os} accordingly. Since the falling edge of ACK_r is aligned with that of $\overline{\mathrm{STR}}_a$ while the rising edge leads the falling edge of $\widehat{\mathrm{ACK}}_r$ by the input of the register, i.e., $T_{os} - T_{in}[n]$, the time difference between the rising edge of STR_a and that of $v_{inv,r}$ is $T_{in}[n]$. The preceding analysis shows that at the end of nth cycle of STR_a, $T_{in}[n]$ is stored and is ready to be added to the next input $T_{in}[n+1]$ in $(n+1)$th cycle of STR_a. Since the result of addition operation is the time between the rising edge of v_{inv} and that of $\overline{\mathrm{STR}}_1$ shown in Fig.3.2, the output of the time integrator is the time bordered by the rising edge of $v_{inv,a}$ and that of $\overline{\mathrm{STR}}_a$. The time offset of ACK_a becomes $2T_{os}$ after the first cycle of the operation, due to the time duration of the time register.

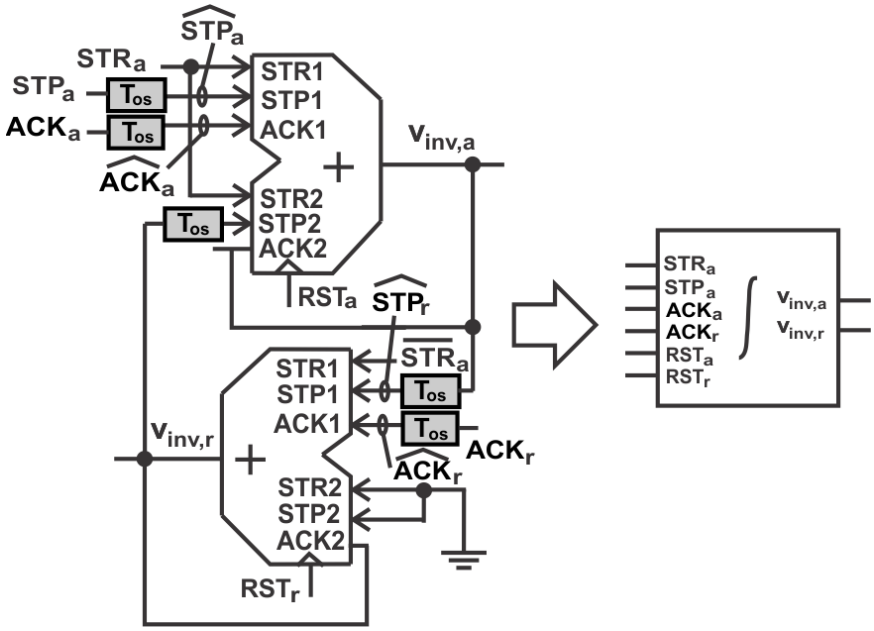

Figure 3.5: Schematic of single-ended time integrator. The output of the time integrator is the time interval bordered by the rising edge of $v_{inv,a}$ and that of $\overline{\mathrm{STR}}_a$. The time offset of ACK_a changes from T_{os} to $2T_{os}$ after the first cycle of the operation, due to the time duration of the time register.

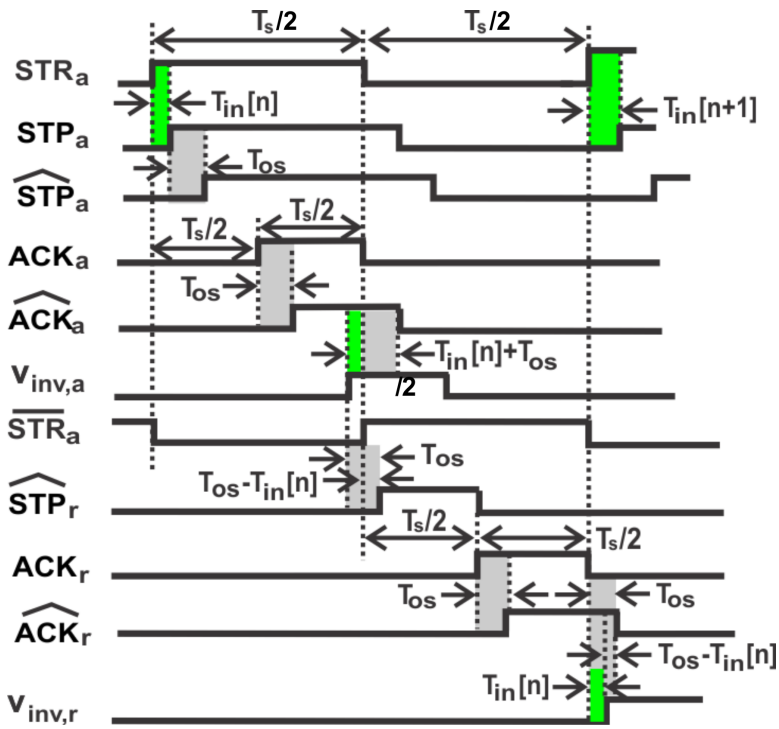

Figure 3.6: Timing diagram of single-ended time integrator. The time offset of ACK_a changes from T_{os} to $2T_{os}$ after the first cycle of the operation, due to the time duration of the time register.

3.1.4 Differential time integrator

Single-ended time integrators suffer from a large second harmonic tone arising from current mismatch of time adders. In this paper, we propose a differential time integrator shown in Fig.3.7 that consists of two single-ended time integrators. Note the polarity of the time variable to be integrated differs in the two single-ended time integrators.

Differential time input $T_{in}[n] = T_{in}^{+}[n] - T_{in}^{-}[n]$ is generated using a differential voltage-controlled delay line (VCDL) with a sinusoidal input, as shown in Fig.3.8. A differential VCDL consists of two identical single-ended VCDLs. The output of the single-ended VCDLs is the time bordered by the rising edge of CLK and that of the load inverter. Single-ended VCDLs suffer from a high degree of nonlinearity, arising from the dependence of the discharge current of the capacitor on v_{DS} of the discharge transistor. The full differential configuration suppresses even-order harmonics, as evident in Fig.3.9 where the output of single-ended and differential time integrators is shown. It is seen that the input of the time integrator

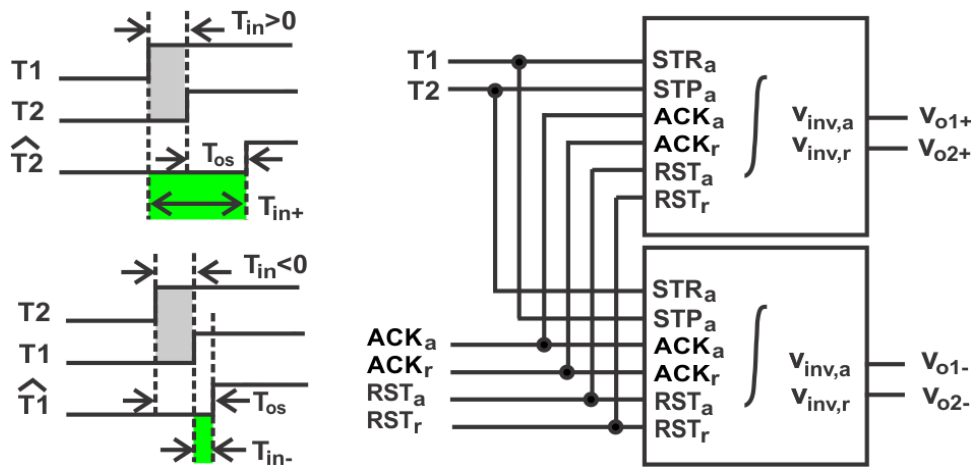

Figure 3.7: Differential time integrator.

generated using a differential VCDL does not have 2nd-order harmonic at 830 kHz. The 3rd-order harmonic tone at 1245 kHz, however, is large.

The output of the single-ended and differential time integrators is shown in Fig.3.9. It is seen that the second harmonic is reduced from 22.9 dB of the single-ended time integrator to 9.9 dB of the differential time integrator. The signal is increased by 7 dB. The differential time integrator consumes 189.2 μW while the single-ended time integrator consumes 101.6μW.

3.2 Time-Mode 1-1 MASH $\Delta\Sigma$ Modulator

The proposed time integrator is utilized to construct a 1-1 MASH $\Delta\Sigma$ TDC consisting of two $\Delta\Sigma$ TDCs called TDC1 and TDC2, as shown in Fig.3.10. Since the output of TDC1 D_{o1} determines whether feedback T_{fb1} should be added to or subtracted from the time input of TDC1. The same holds for TDC2 as well. DTC2 extracts the quantization error of TDC1. To extract the quantization error of TDC1, the output of DTC2 is subtracted from the output of the differential time integrator of TDC1. The value of T_{fb2} is determined based on the maximum output of the time integrator of TDC1.

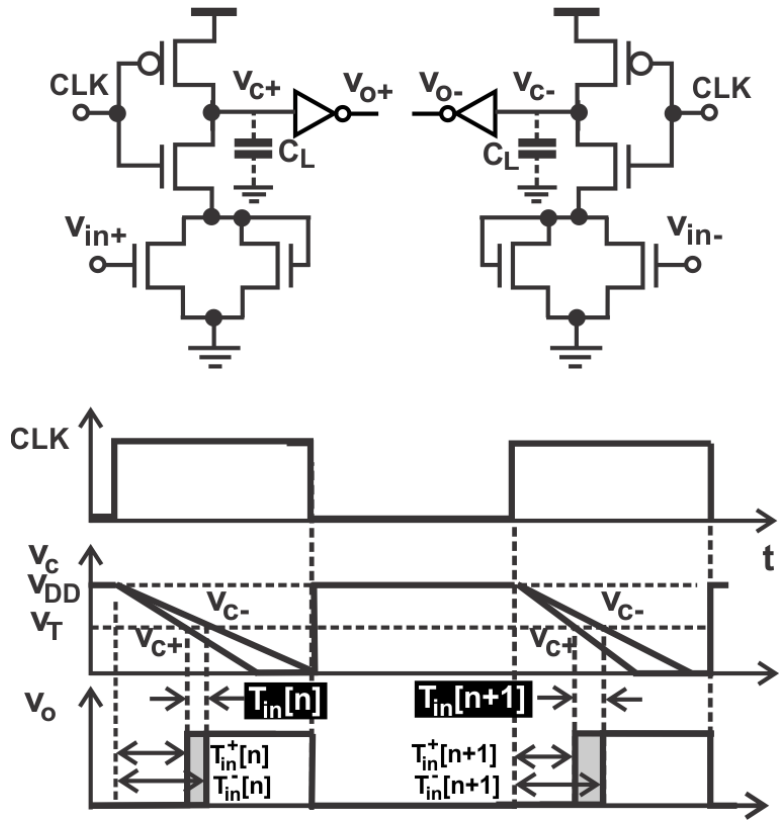

Figure 3.8: Generation of differential sinusoidal time variable.

3.3 Timing Error

The timing error of the time integrator can be classified into random timing error and deterministic timing error. The former is due to system noise such as switching noise and device noise such as thermal and flicker noise while the latter is caused by the nonidealities of the time integrator such as charge injection, clock feed-through, and current mismatch.

3.3.1 Random timing error

Device noise-induced timing error in charging phase

When RST is asserted, the integration capacitor is charged by the supply voltage via the PMOS transistor. Since the PMOS transistor operates in the triode region, it can be replaced with a resistor R_p and a thermal noise voltage source whose power is given by

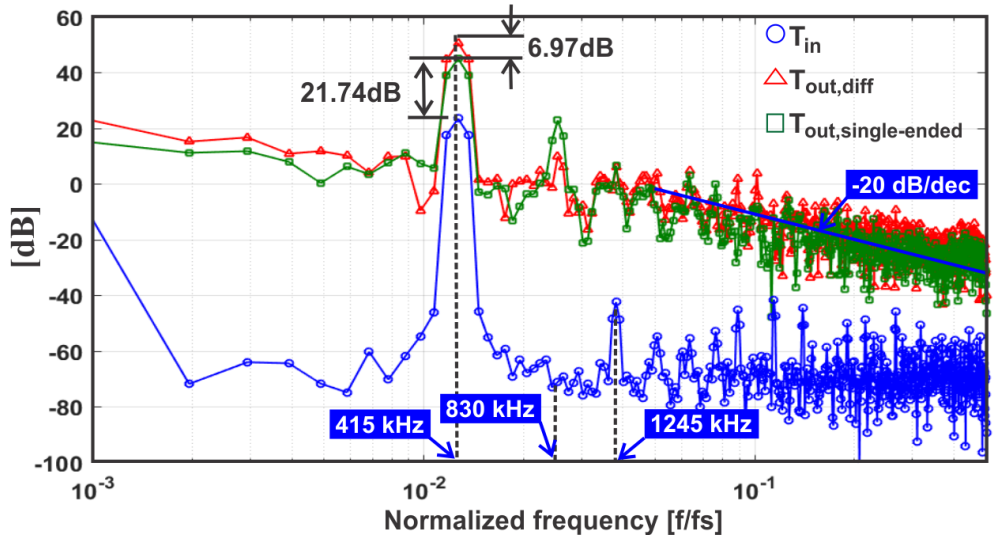

Figure 3.9: Spectrum of time integrators. Sampling frequency 25 MHz, input frequency 415 kHz, amplitude 50 ps. 1024 samples with Hanning window.

$\overline{v_{np}^2} = 4kTR_p\Delta f$ where k is Boltzmann constant, T is temperature in degrees kelvin, and Δf is the frequency range over which the power is calculated. The total noise power at the integration capacitor is given by $\overline{v_{np}^2} = \frac{kT}{C}$. The resultant jitter is obtained from

$$\overline{\tau_{PMOS}^2} = \left(\frac{2T_{FS}}{V_{DD}}\right)^2 \frac{kT}{C}. \tag{3.4}$$

Making use

$$C \approx \frac{2IT_{FS}}{V_{DD}}, \tag{3.5}$$

we have

$$\overline{\tau_{PMOS}^2} = \frac{kT}{I}\frac{2T_{FS}}{V_{DD}}. \tag{3.6}$$

Device noise-induced timing error in discharging phase

Thermal noise and flicker noise of the channel current of the transistors in the discharge paths with their power given by $\overline{i_{nt}^2} = 4kT\gamma g_m\Delta f$ and $\overline{i_{nf}^2} = \frac{K_f I}{f}\Delta f$, respectively

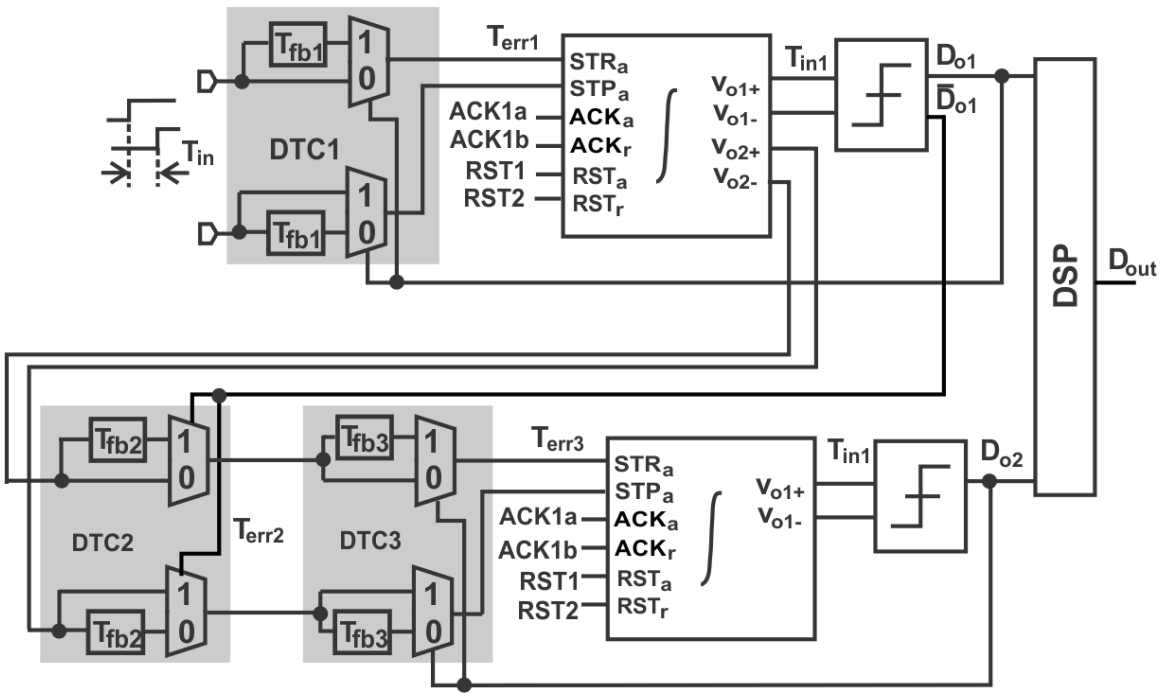

Figure 3.10: 1-1 MASH time-mode $\Delta\Sigma$ TDC.

give rise to uncertainty in the voltage of the integration capacitor, which in turn gives rise to uncertainty $\Delta\tau_n$ of the threshold-crossing time of the load inverter subsequently jitter of the output of the time adder. Since

$$I + i_{nt} + i_{nf} = C\frac{dv}{dt}, \tag{3.7}$$

with

$$\frac{dv}{dt} \approx \frac{V_{DD}/2}{T_{FS} + \tau_n}, \tag{3.8}$$

we have

$$T_{FS} + \tau_n \approx \frac{C}{I + i_{nt} + i_{nf}}\frac{V_{DD}}{2}. \tag{3.9}$$

Further making use (3.5), we arrive at

$$T_{FS} + \tau_n \approx \frac{T_{FS}}{1 + \frac{i_{nt}+i_{nf}}{I}}. \tag{3.10}$$

Since

$$1 + \frac{i_{nt} + i_{nf}}{I} \approx 1 - \frac{i_{nt} + i_{nf}}{I} \tag{3.11}$$

as $i_{nt}, i_{nf} \ll I$, we have

$$\overline{\tau_n^2} \approx \left(\frac{T_{FS}}{I}\right)^2 \left(\overline{i_{nt}^2} + \overline{i_{nf}^2}\right). \tag{3.12}$$

It is evident from (3.12) that the larger I, the smaller the timing error. This, however, is at the expense of power consumption.

Supply voltage fluctuation induced timing error

The integration capacitor is initially charged to V_{DD} prior to a discharge operation. The fluctuation of the supply voltage arising from switching noise gives rise to uncertainty in the threshold-crossing of the load inverter subsequently the timing error in the output of the time adder, as shown in Fig.3.11(a). It can be shown that

$$\overline{\Delta\tau_{V_{DD}}^2} = \left(\frac{2T_{FS}}{V_{DD}}\right)^2 \overline{\Delta V_{DD}^2}, \tag{3.13}$$

where ΔV_{DD} is the variation of the supply voltage V_{DD}. The effect of switching noise is minimized with the differential configuration of the modulator.

Threshold voltage fluctuation induced timing error

The fluctuation of the threshold voltage of the load inverter arising from switching noise, denoted by ΔV_T, gives rise to uncertainty in the threshold-crossing of the inverter subsequently the timing error in the output of the time adder, as shown in Fig.3.11(b). It

can be shown that

$$\overline{\Delta\tau_{V_T}^2} = \left(\frac{2T_{FS}}{V_{DD}}\right)^2 \overline{\Delta V_T^2}. \tag{3.14}$$

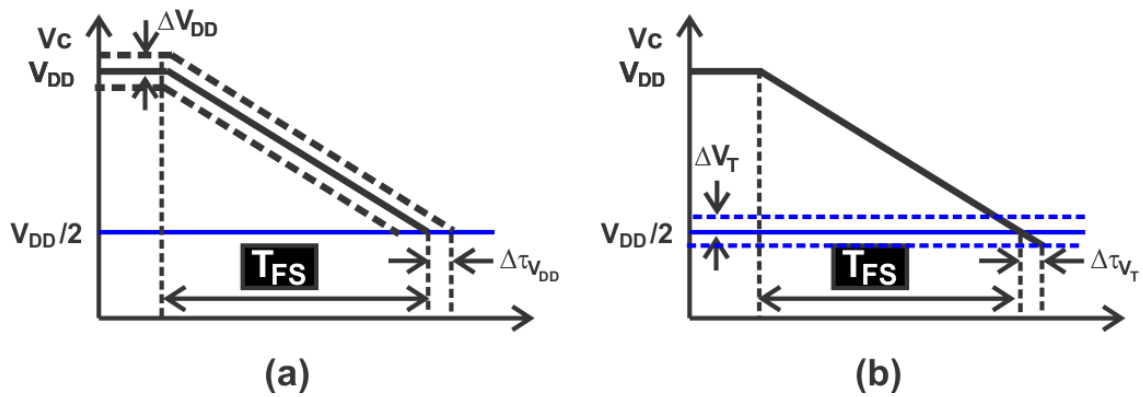

Figure 3.11: Timing error due to supply voltage fluctuation (left) and threshold voltage fluctuation of load inverter (right).

3.3.2 Deterministic timing error

Current mismatch induced timing error

Although the two discharge paths of the integration capacitor are identical, the difference between the input time variable and accumulated time variable gives rise to a current mismatch. To illustrate this, consider Fig.3.12 (ignore transistors M5 and M6 shown in light color). The amount of the charge discharged by M3 and M4 is a function of both the duration of gating signals and the drain-source voltages v_{DS3} and v_{DS4} of the transistors. Let ΔI_3 and ΔI_4 represent v_{DS}-induced currents of M3 and M4, respectively. $T_{in}[n]$ is typically much smaller as compared with $\sum_{k=1}^{n-1} T_{in}[k]$, especially when approaching the end of integration operation. As a result, $T_{in}[n]$-induced discharge process via M3 is much shorter as compared with $\sum_{k=1}^{n-1} T_{in}[k]$-induced discharge process via M4. As a result, Δv_{DS} due to $T_{in}[n]$ is much smaller as compared with that due to $\sum_{k=1}^{n-1} T_{in}[k]$. We therefore have $\Delta I_4 \gg \Delta I_3$.

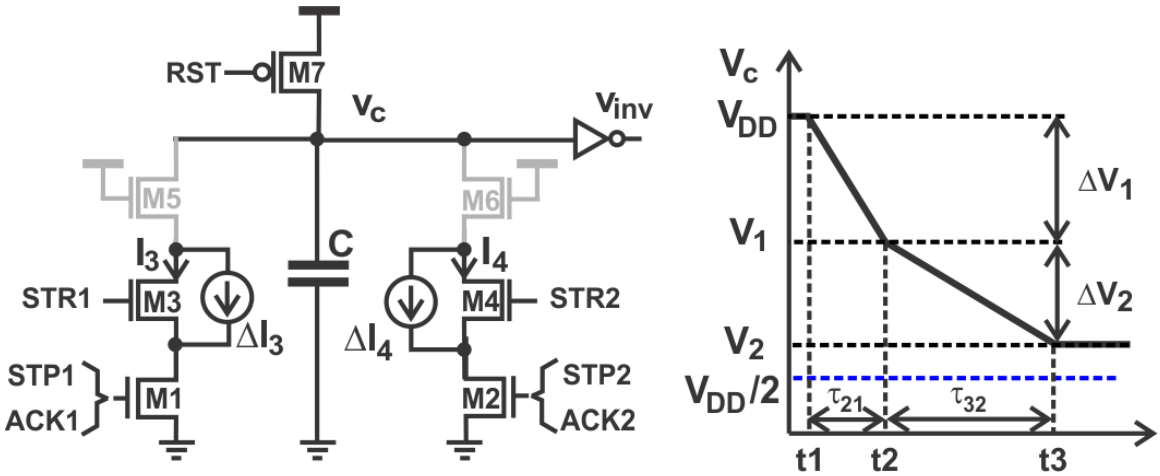

Figure 3.12: Current mismatch.

To quantify current mismatch-induced timing error, we notice

$$\tau_{21} = \frac{C\Delta V_1}{I_3 + I_4 + \Delta I_3 + \Delta I_4} \approx \frac{C\Delta V_1}{I_3 + I_4}\left(1 - \frac{\Delta I_3 + \Delta I_4}{I_3 + I_4}\right), \tag{3.15}$$

where $\Delta V_1 = V_{DD} - V_1$. Timing error due to Δv_{DS} is therefore given by

$$\Delta\tau_{21} \approx -\frac{C\Delta V_1}{(I_3 + I_4)^2}\left(\Delta I_3 + \Delta I_4\right). \tag{3.16}$$

Similarly one can show that

$$\Delta\tau_{32} \approx -\frac{C\Delta V_2}{I_4^2}\Delta I_4, \tag{3.17}$$

where $\Delta V_2 = V_1 - V_2$. Since $\Delta I_3 = v_c/r_{o3}$ and $\Delta I_4 = v_c/r_{o4}$ where r_{o3} and r_{o4} are the output resistance of M3 and M4, respectively,

$$\Delta\tau_{21} \approx -\frac{C\Delta V_1}{(I_3 + I_4)^2}\left(\frac{1}{r_{o3}} + \frac{1}{r_{o4}}\right)v_c. \tag{3.18}$$

$$\Delta\tau_{32} \approx -\frac{C\Delta V_2}{I_4^2}\frac{v_c}{r_{o4}}. \tag{3.19}$$

Since $T_{out} = \tau_{21} + \tau_{32}$, we have timing error due to current mismatch denoted by $\overline{\Delta\tau_I^2}$

$$\Delta\tau_I = \Delta\tau_{21} + \Delta\tau_{32}. \tag{3.20}$$

To minimize v_{DS} induced jitter, M5 and M6 can be added to form cascode, as shown in Fig.3.12. Since the operation range of v_c is from V_{DD} to $V_{DD}/2$, transistors M3-M6 mostly operate in saturation. The cascode configuration effectively increases the output impedance seen from the drain of M5 and M6 to $(g_{m5}r_{o5})r_{o3}$ and $(g_{m6}r_{o6})r_{o7}$, respectively. Eq.(3.18) becomes

$$\Delta\tau_{21} \approx -\frac{C\Delta V_1}{(I_3+I_4)^2}\left[\frac{1}{(g_{m5}r_{o5})r_{o3}} + \frac{1}{(g_{m6}r_{o6})r_{o4}}\right] v_c. \tag{3.21}$$

$$\Delta\tau_{32} \approx -\frac{C\Delta V_2}{I_4^2}\frac{v_c}{(g_{m6}r_{o6})r_{o4}}. \tag{3.22}$$

The effect of current mismatch is therefore reduced.

v_{DS}-induced effect can be further lowered by increasing the threshold voltage of the load inverter via proper transistor sizing such that the variation of the voltage of the integration capacitor is smaller than $V_{DD}/2$. This is equivalent to lowering ΔV_1 and ΔV_2, which will in turn lower Δ_{21} and Δ_{32}, as evident in (3.21). It should be noted that since increasing the threshold voltage also affects T_{FS} whose value is set by system specifications, the value of the integration capacitor needs to be adjusted accordingly to ensure that T_{FS} remains unchanged.

Charge Injection-induced timing error

Although the integration capacitor is initially charged to V_{DD}, the turn-off of the PMOS transistor will force the portion of the charge stored in the channel of the transistor to be injected into the integration capacitor, resulting in an additional voltage Δv_Q added to the initial voltage of the integration capacitor prior to the discharge operation. This is similar to V_{DD} fluctuation investigated earlier. If we assume that half of the channel charge is dumped to the integration capacitor, then the resultant Δv_Q is given by $\Delta v_Q = \frac{1}{2}\frac{C_g}{C}V_{DD}$

where C_g is the gate capacitance of the PMOS transistor. We therefore arrive at the timing error due to charge injection denoted by $\Delta\tau_Q$

$$\Delta\tau_Q = \left(\frac{C_g}{C}\right) T_{FS}. \tag{3.23}$$

It is seen from (3.23) that lowering C_{gs7} reduces the timing error caused by charge injection.

Clock feed-through induced timing error

In addition to charge injection from the PMOS transistor, the voltage of the integration capacitor is also affected by the effect of clock feed through via C_{gd} of discharge transistors with its amount give by $\Delta v_\phi = \frac{C_{gd}}{C_{gd}+C} V_{DD}$. The timing error due to clock feed though denoted by $\Delta\tau_\phi$ is obtained from

$$\Delta\tau_\phi = \left(\frac{2C_{gd}}{C_{gd}+C}\right) T_{FS}. \tag{3.24}$$

It is seen from (3.24) that to minimize the timing error caused by clock feed through, $C \gg C_{gd}$ is required.

3.3.3 Total timing error

The total timing error of the time integrator can be obtained by considering both the random timing error and deterministic timing error. Assume that jitter caused by the noise sources of the time integrator is uncorrelated, we have the worst-case timing error

$$\begin{aligned} \tau_{max} &= \sqrt{\overline{\tau_{PMOS}^2} + \overline{\tau_n^2} + \overline{\tau_{V_{DD}}^2} + \overline{\tau_{V_T}^2}} \\ &+ |\tau_I| + |\tau_Q| + |\tau_\phi|. \end{aligned} \tag{3.25}$$

3.3.4 Model of time integrator

Having analyzed the timing error of the time integrator, we now derive the model of the time integrator. Fig.3.13 shows the block diagram of the time integrator where e_a and e_r denote the timing error of the adder and register, respectively. Note that $e_a < e_r$ as one of the two discharge paths of the register is always disabled. Because the output of the time adder is bordered by the rising edge of $v_{inv,a}$ and that of STR_a with the former corrupted by the effect of the nonidealities of the adder investigated earlier while the latter is the input of the time integrator and is therefore assumed to be ideal, and the signal from the time adder to the time register is $v_{inv,a}$, timing error e_a exists in both the output of the time integrator and the input of the time register. Further, because the signal from the output of the time register to the time adder, $v_{inv,r}$, is also subject to the effect of the nonidealities of the time register, e_r exists at the output of the time register. It can be shown that

$$T_{out} = \frac{1}{1 - z^{-1}} \left(T_{in} + E_a + z^{-1} E_r \right) + E_a. \tag{3.26}$$

Since $sT_s \ll 1$, we have $1 - z^{-1} \approx sT_s$ and $z^{-1} \approx 1$. As a result,

$$T_{out} \approx \frac{1}{sT_s} \left(T_{in} + E_a + E_r \right) + E_a. \tag{3.27}$$

It is seen from (3.27) that the gain of the single-ended time integrator is $\frac{1}{2\pi} \frac{f_s}{f_{in}}$.

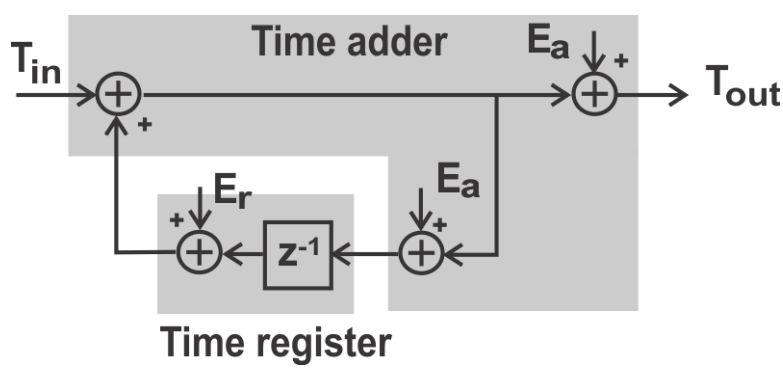

Figure 3.13: Model of time integrator. E_a outside the loop will be shaped out when the integrator is in a $\Delta\Sigma$ modulator.

3.4 Discussion

In this section, we examine factors critical to the operation of the modulator.

3.4.1 Timing signal

It is seen from the timing diagram of the single-ended time integrator given in Fig.3.6 that the key signal that controls the operation of the time integrator is STR_a. The operation of time addition takes place at the rising edge of STR_a while that of time registration occurs at the falling edge of STR_a, as shown graphically in Fig.3.14. Note that the sampling frequency of the time input is given by $f_s = 1/T_s$.

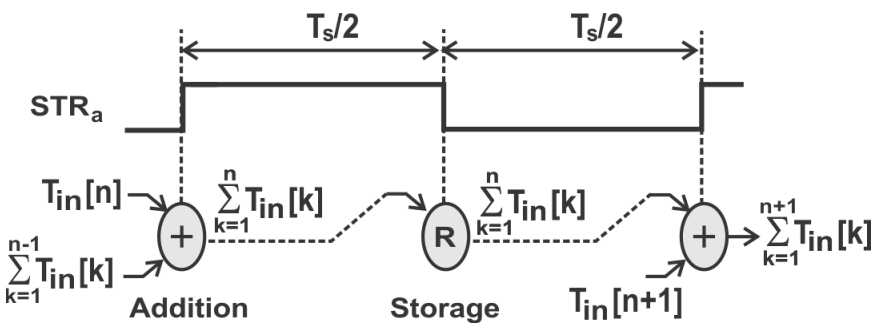

Figure 3.14: Timing of single-ended time integrator.

3.4.2 Sampling frequency

The minimum sampling period T_s is determined by the following constraints : (i) $\hat{T}_{in} = T_{os} + T_{in} > 0$ must be satisfied in order to ensure the proper operation of the time adder. Since ACK_a is asserted in the middle of STR_a, $T_{in} + T_{os} < T_s/2$ must be satisfied. (ii) The time difference between the rising edge of ACK_a and that of $v_{inv,a}$ must be smaller than $T_s/2$.

3.4.3 Offset time T_{os}

The deployment of the offset blocks with time offset T_{os} ensures the proper operation of the time adder. As the only purpose of having T_{os} is to ensure $\hat{T}_{in} > 0$ when $T_{in} < 0$, one can remove the offset blocks by employing a DFF to detect the polarity of T_{in} so as to determine whether an addition or subtraction operation should be taken. If STR and STP are routed to the data and clock inputs of the DFF, respectively, then $Q = 1$ when $T_{in} > 0$ and $Q = 0$ when $T_{in} < 0$, as shown in Fig.3.15. The time offset blocks shown in Fig.3.1 can be removed. Fig.3.16 sketches the timing diagram of the single-ended time integrator with the time offset blocks removed. It is evident that the removal of the time offset blocks will significantly simplify the timing diagram, which in turn, allowing the reduction of T_s.

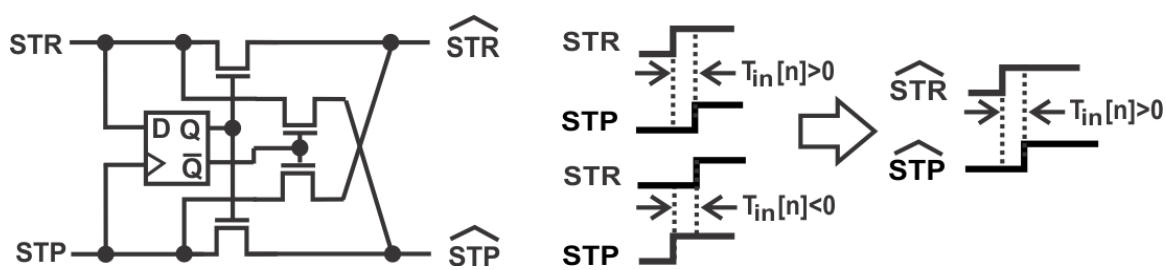

Figure 3.15: Positive time variable generation.

3.4.4 Gain of time integrator

Let the time input generated by the single-ended VCDL be $T_{in}(t) = T_m \cos(\omega_{in} t)$ where T_m and ω_{in} are the amplitude and frequency of the input, respectively. The input variable is sampled at the rising edge of STR_a with sampling frequency $f_s = 1/T_s$, the sampled time input at $t = nT_s$ can therefore be written as $T_{in}[n] = T_m \cos(2\pi f_{in} n T_s)$. The output of the time integrator is obtained from

$$\begin{aligned} T_{out}[n] &= \int_0^n T_m \cos(2\pi f_{in} k T_s) dk \\ &= \frac{T_m}{2\pi} \frac{f_s}{f_{in}} \sin\left(2\pi f_{in} n T_s\right). \end{aligned} \tag{3.28}$$

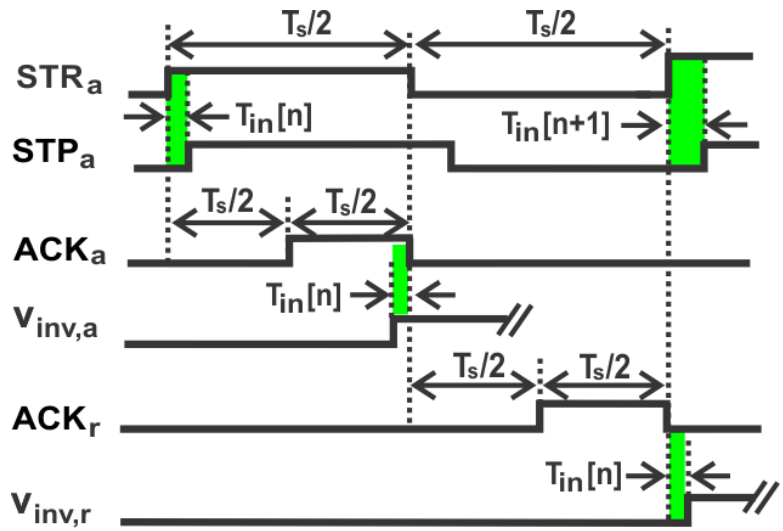

Figure 3.16: Timing diagram of single-ended time integrator with offset time blocks removed.

The gain of the time integrator is therefore obtained

$$\frac{T_{out}[n]}{T_{in}[n]} = \frac{1}{2\pi}\frac{f_s}{f_{in}} = \frac{\text{OSR}}{\pi}, \tag{3.29}$$

where ORS $= f_s/(2f_{in})$ is the oversampling ratio. Eq.(3.29), also derived earlier in (3.27), shows that the gain of the time integrator is set by the ratio of the sampling frequency f_s to the frequency of the input f_{in}. For a given input, both f_s and T_m are fixed, the gain of the time integrator can only be adjusted by varying sampling frequency. In the example presented in this paper, $f_s = 25$ MHz and $f_{in} = 317$ kHz. The calculated and simulated gain of the single-ended time integrator are 21.97 dB and 21.74 dB, respectively, as shown in Fig.3.9. Fig.3.17 shows the waveform of the input and output of the time integrator. A 90 degree phase shift between the output and input is evident.

3.5 Simulation Results

To verify whether the proposed TDC functions properly or not, a behavioral analysis was performed prior to schematic-level design. Specifically, a differential sinusoidal time input T_{in} of frequency 415 kHz and amplitude 50 ps generated from a 415 kHz sinusoidal

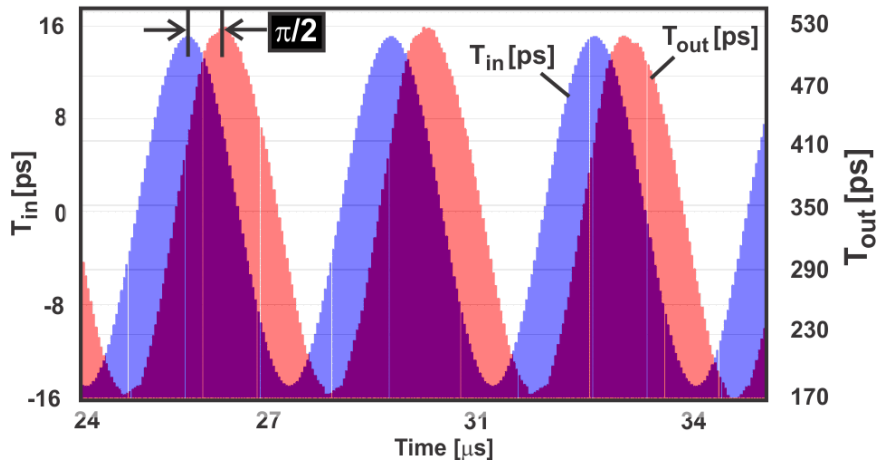

Figure 3.17: Waveforms of single-ended time integrator. Input : $T_m = 15$ ps, $f_{in} = 317$ kHz. Sampling frequency $f_s = 25$ MHz.

voltage signal of amplitude 200 mV using the differential VCDL shown in Fig. 3.8 with clock frequency $f_s = 25$ MHz was fed to the TDC. For each cycle of the operation of the TDC, T_{in} was obtained from the schematic-level simulation of the differential VCDL using Spectre from Cadence Design Systems with BSIM4 device models. The input T_{err1} and output T_{in1} of the integrator of TDC1, the input of the TDC2 T_{err2}, and the input T_{err3} and output T_{int2} of the integrator of TDC2 were calculated and the results are tabulated in Fig.3.18. The digital output of the TDC is shown in Fig.3.19. Fig.3.20 shows the spectrum of the output of the TDC calculated using the preceding behavioral analysis. The TDC exhibits 2nd-order noise-shaping outside the signal band. Also observed is the effect of the flicker noise at low frequencies, arising from the generation of T_{in} using the differential VCDL. The SNR of the TDC is 38.66 dB over 48 $\sim$ 415 kHz . The ENOB of the TDC is 6.13 and its resolution is 1.45 ps.

The preceding 1-1 MASH $\Delta\Sigma$ TDC was then designed in an IBM 130 nm 1.2 V CMOS technology. The TDC was analysed using Spectre from Cadence Design Systems with BSIM4 device models. The spectrum of the TDC is plotted in 3.19, together with that from behavioral analysis for comparison. 1024 samples with a Hanning window were used. It is seen that the TDC exhibits 2nd-order noise-shaping outside the signal band. Also observed is that the in-band noise floor of the TDC is approximately 20 dB higher as

Cycles	Tin	T_fb1	Terr1	Tint1	Do1	T_fb2	Terr2	T_fb3	Terr3	Tint2	Do2
n				0	1.2					0	1.2
1	0.00	70.00	-70.00	-70.00	0.00	-125.00	-55.00	125.00	-180.00	-180.00	0.00
2	5.48	-70.00	75.48	5.48	1.20	125.00	119.52	-125.00	244.52	64.52	1.20
3	10.85	70.00	-59.15	-53.67	0.00	-125.00	-71.33	125.00	-196.33	-131.81	0.00
4	16.12	-70.00	86.12	32.45	1.20	125.00	92.55	-125.00	217.55	85.74	1.20
5	21.23	70.00	-48.77	-16.32	0.00	-125.00	-108.68	125.00	-233.68	-147.94	0.00
6	26.10	-70.00	96.10	79.78	1.20	125.00	45.22	-125.00	170.22	22.28	1.20
7	30.88	70.00	-39.12	40.66	1.20	125.00	84.34	125.00	-40.66	-18.38	0.00
8	35.15	70.00	-34.85	5.82	1.20	125.00	119.18	-125.00	244.18	225.80	1.20
9	39.10	70.00	-30.90	-25.08	0.00	-125.00	-99.92	125.00	-224.92	0.88	1.20
10	42.58	-70.00	112.58	87.50	1.20	125.00	37.50	125.00	-87.50	-86.62	0.00
11	45.59	70.00	-24.41	63.09	1.20	125.00	61.91	-125.00	186.91	100.29	1.20
12	48.15	70.00	-21.85	41.25	1.20	125.00	83.75	125.00	-41.25	59.04	1.20
13	50.11	70.00	-19.89	21.36	1.20	125.00	103.64	125.00	-21.36	37.69	1.20

Figure 3.18: Behavioral analysis of 1-1 MASH $\Delta\Sigma$ TDC.

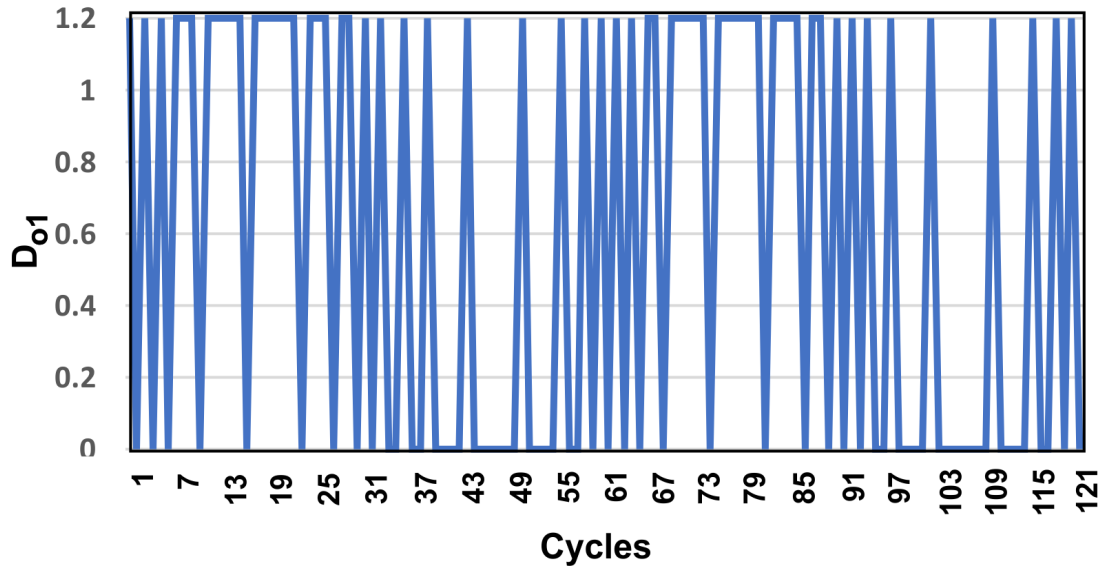

Figure 3.19: Waveform of the output of 1-1 MASH $\Delta\Sigma$ TDC from behavioral analysis.

compared with that of the ideal TDC, revealing the detrimental effect of the imperfections of the TDC examined earlier.

Fig.3.21 plots the spectrum of the TDC with the without cascode adders. It is seen that the cascode configuration of the time adder not only lowers in-band noise floor as

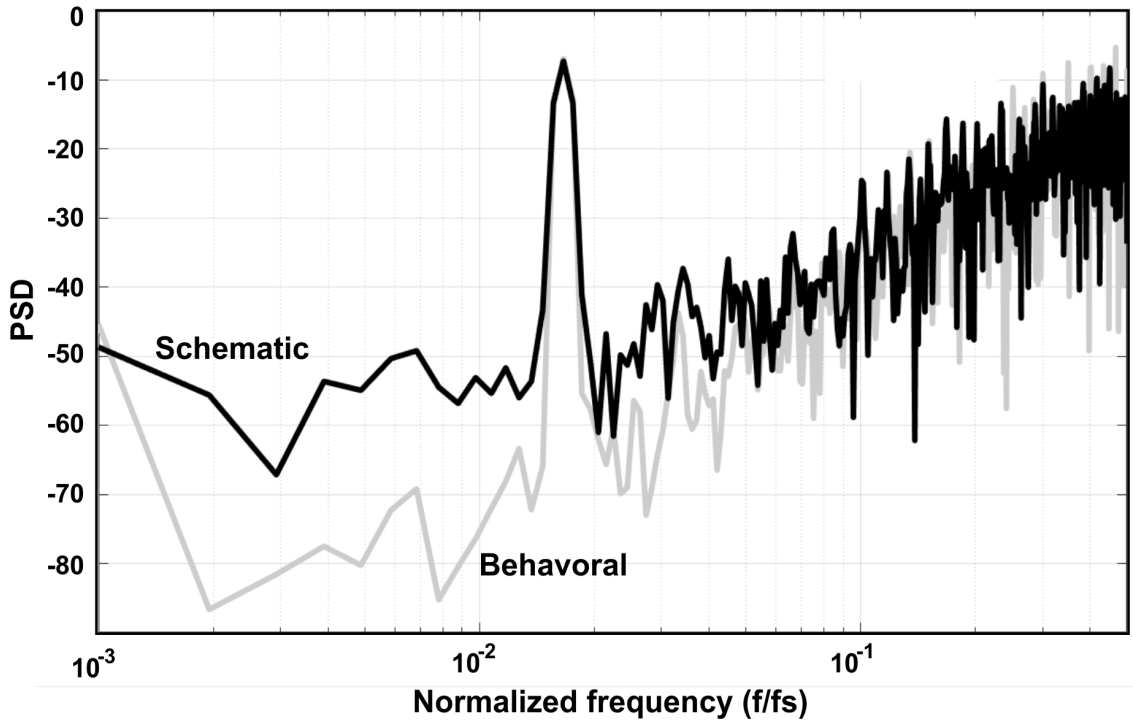

Figure 3.20: Spectrum of 1-1 MASH time-mode $\Delta\Sigma$ Modulator from both behavioral analysis and schematic-level simulation (cascode time integrators with raised threshold voltage of load inverter).

compared with that without cascode. It also improves the degree of linearity, manifested by reduced harmonic tones. Cascode also improves the noise-shaping profile of the modulator. The SNR is 36.25 dB over 48 $\sim$ 415 kHz. The ENOB of the TDC is 5.73 and its resolution is 1.96 ps.

Fig.3.22 shows the spectrum of the TDC with the threshold voltage of the load inverter raised from 0.6 V to 0.8 V. The improvement in noise-shaping profile is evident. No visible reduction in both the in-band noise floor and harmonic tones is observed.

Table 3.1 compares the performance of recently published time-mode $\Delta\Sigma$ modulators. The most relevant reference to which this work should be compared is [10] where a time adder-based time integrator was used. All other references list in Table 3.1 uses an OTA-based integrator. This work has better effective time resolution since it is the second-order $\Delta\Sigma$ modulator.

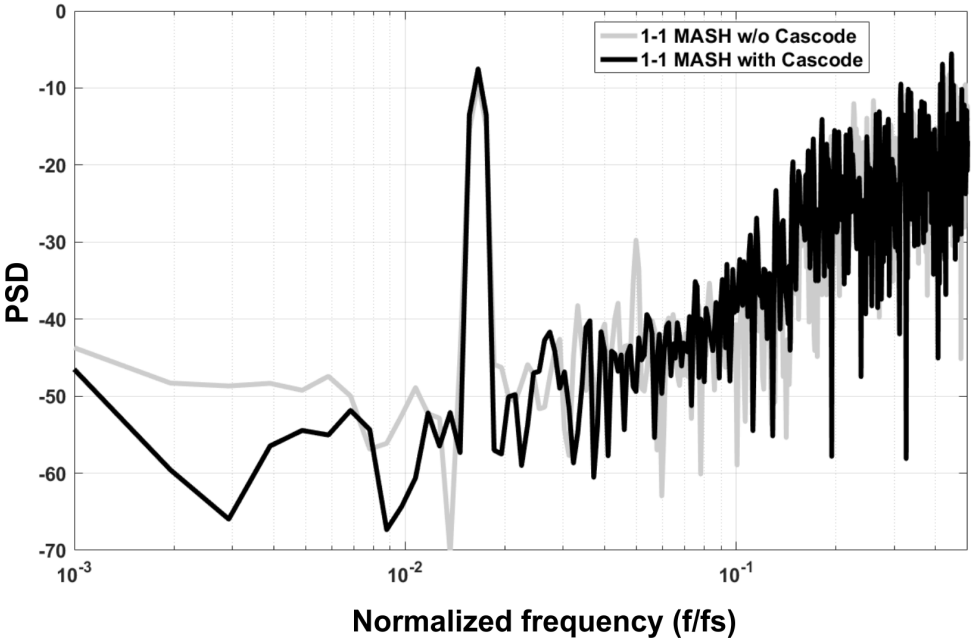

Figure 3.21: Spectrum of 1-1 MASH time-mode $\Delta\Sigma$ Modulator.

Table 3.1: Performance comparison of $\Delta\Sigma$ TDCs.

Ref.	Tech. (nm)	Supply (V)	BW (Hz)	OSR	Effective Res. (ps)	Power (mW)	Order
[40]	130	1.5	1M	25	1	2.2-21	1st
[22]	180	1.8	400k	348	8.7 (*)	0.78	1st
[41]	130	1.2	100k	250	11	1.7	3rd
[10]	32	1.0	100k	50	4.4	0.25	1st
This	130	1.2	415k	30	1.9 (**)	0.5	2nd

* ENOB. ** Ideal digital filters used.

3.6 Conclusions

An all-digital 1-1 MASH $\Delta\Sigma$ TDC utilizing a differential cascode time integrator was proposed. A cascode time adder with raised inverter threshold voltage was proposed to minimize the deterministic jitter caused by the current mismatch of the two discharge paths of the time adder. A differential time integrator consisting of a pair of identical single-ended time integrators was proposed to minimize the effect of the nonlinearities of the single-ended

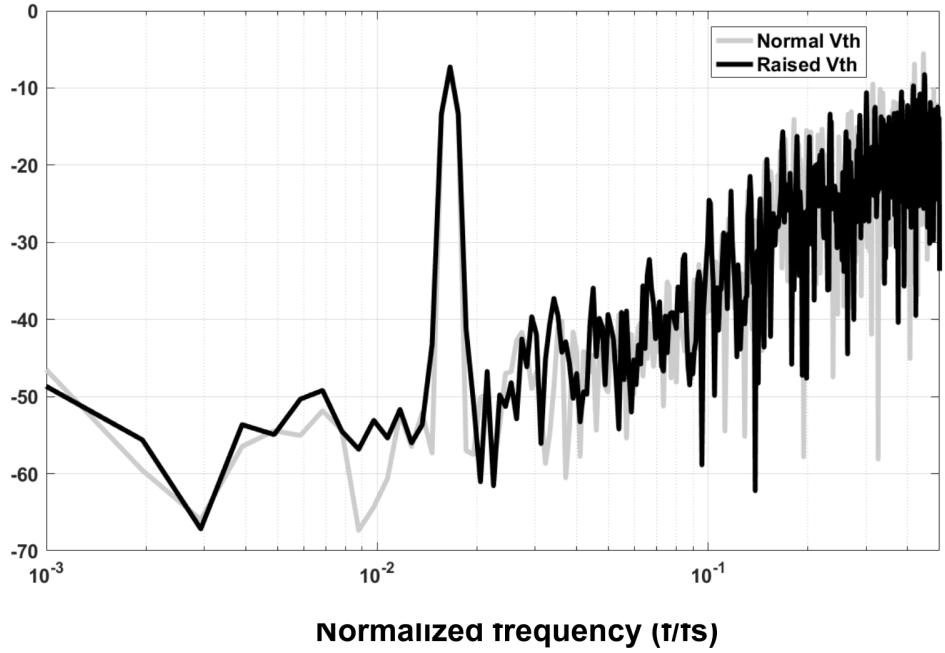

Figure 3.22: Spectrum of 1-1 MASH $\Delta\Sigma$ TDC with both differential cascode time integrator and different threshold voltage of load inverter. Blue : $V_T = 0.8$V. Red : $V_T = 0.6$V. Integration capacitor value is changed from 2.1 pF with 0.6V threshold voltage to 3.2 pF with 0.8V threshold voltage.

time integrator. The random and deterministic timing errors of the TDC were analyzed in detail. The simulation results of the proposed modulator demonstrated that the modulator exhibits 40 dB noise-shaping. The cascode-configured discharge paths and raised threshold voltage of the load inverter are effective in improving the linearity and improving noise-shaping profile of the TDC. The TDC achieves 1.9 ps time resolution over 48 $\sim$ 415 kHz signal band while consuming 502 μW.

Chapter 4

$\Delta\Sigma$ TDC with Bi-Directional Gated Delay Line Time Integrator

This chapter presents a bi-directional gated delay line time integrator and its applications in an all-digital first-order $\Delta\Sigma$ TDC. Section 4.1 presents an operation of bi-directional gated delay cell. Section 4.2 presents an operation of bi-directional gated delay line for a new low-power time-mode integrator. The time integrator consists of a bi-directional gated delay line with the time variable to be integrated as the gating signal. The accumulation of time variables is obtained via the accumulation of the charge of the load capacitor and logic state of gated delay stages. As compared with the reported time integrators, the proposed time integrator is significantly simpler. An all-digital first-order single-bit $\Delta\Sigma$ TDC is explained in detail in Section 4.3. Section 4.4 presents design considerations. Section 4.5 presents the simulation results of the proposed all-digital first-order single-bit $\Delta\Sigma$ TDC implemented in an IBM 130 nm 1.2 V CMOS technology. The chapter is concluded in Section 4.6.

4.1 Bi-Directional Gated Delay Cell

Consider the bi-directional gated delay line shown in Fig.4.1. The rising edge of a digital signal can propagate from node 1 to node 2 (forward) if the gating signal $T_{in} > 0$ or from node 2 to node 1 (reverse) if $T_{in} < 0$ in Fig.4.5 with the same per-stage delay. Consider the case where the signal propagates from node 1 to node 2. The node 1 and node 2 are initialized to V_{DD} and ground, respectively before time t_1 shown in Fig.4.1. Let the gating

signal T_{in} be a pulse bounded by $0 \sim V_{DD}$ in amplitude and $[0, t]$ in time. The gated switch is in triode region while that of the pMOS transistor of the inverter is in saturation region. When v_c increases above V_{SG}-$|V_{thp}|$, the pMOS transistor will enter triode region eventually. However, to simplify analysis, we assume that the pMOS transistor of the inverter is in saturation region until v_c arrives at $V_{DD}/2$ in the velocity saturated short channel device [42]. Therefore, in this analysis, we can ignore a nonlinear behaviour when v_c goes above $V_{DD}/2$. Then the voltage of the load capacitor at the end of the time interval is given by

$$v_c(t) = \frac{1}{C}\int_0^t I dt \approx \frac{I}{C} T_{in}, \tag{4.1}$$

Eq.(4.1) shows that the gating signal T_{in} is represented by the voltage variation of the load capacitor. We now consider the case where the gating signal T_{in} is a train of pulses in time interval $[t_{k-1}, t_k]$, $k = 1, 2, ..., K$. The pulses can be either positive ($T_{in,k} > 0$) or negative ($T_{in,k} < 0$). If a pulse is positive, the load capacitor is charged and the amount of voltage increment is given by (4.1). Similarly, if a pulse is negative, the load capacitor is discharged and the amount of voltage decrement is also quantified by (4.1). It is seen from Fig.4.1 that

$$\sum_{k=1}^{K} T_{in,k} = \frac{C}{I}\sum_{k=1}^{K} \Delta v_{c,k} \tag{4.2}$$

holds. Eq.(4.2) reveals that the bi-directional gated delay cell performs the accumulation (integration) of time variables by means of the accumulation of the voltage of the load capacitor.

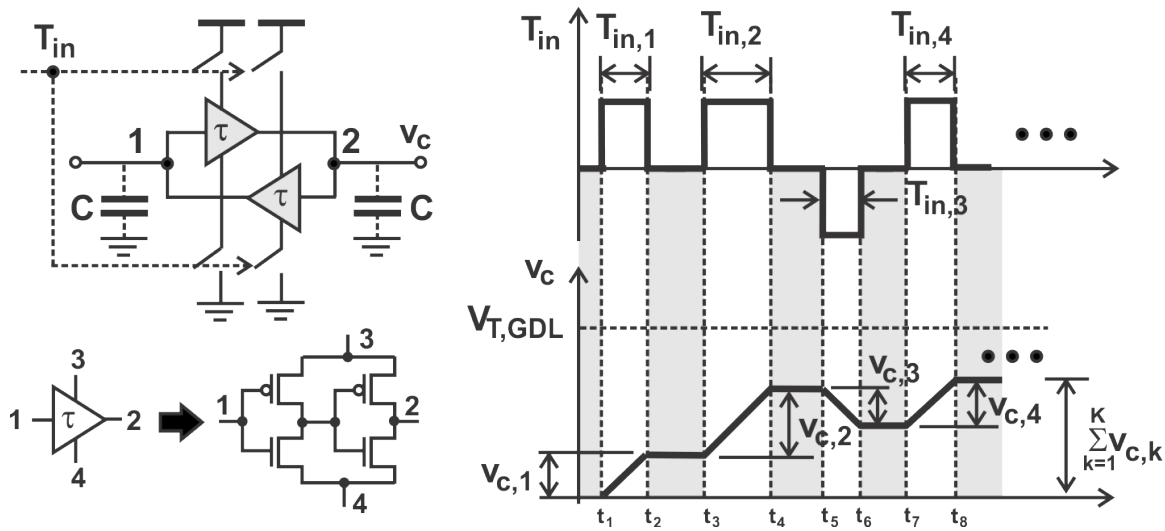

Figure 4.1: Bi-directional gated delay cell.

4.2 Bi-Directional Gated Delay Line

If the load of a bi-directional gated delay cell is another bi-directional gated delay cell whose threshold voltage is $V_{T,GDL} = V_{DD}/2$, the voltage range of the load capacitor is only $0 \sim V_{T,GDL}$, limiting the number of T_{in} pulses that can be summed. Although one can use a large load capacitor to handle a long train of positive or negative pulses, in order to quantify the voltage of the load capacitor so as to yield the output of the time integrator, a VTC is needed, contradicting our goal to perform time-mode integration in digital domain. An alternative is to cascade multiple bi-directional gated delay cells to form a bi-directional gated delay line, as shown in Fig.4.2. Load capacitance C_k is formed by device capacitances only. No explicit capacitors are needed. When the voltage of the gated delay stage exceeds $V_{T,GDL}$, the output of the driven gated delay stage will be toggled. The use of the gated delay line allow us to perform time accumulation over a large range. In order to handle both positive and negative time variables, the left-half-side nodes from node M in Fig.4.2 are initialized to V_{DD} and those in the right-half-side from node M are initialized to ground. Also, the left-most gated delay cell is connected to V_{DD} while the right-most gated delay cell is grounded to transfer charges bi-directionally. By doing this, logic-1 can be shifted to the right and logic-0 can be shifted to the left.

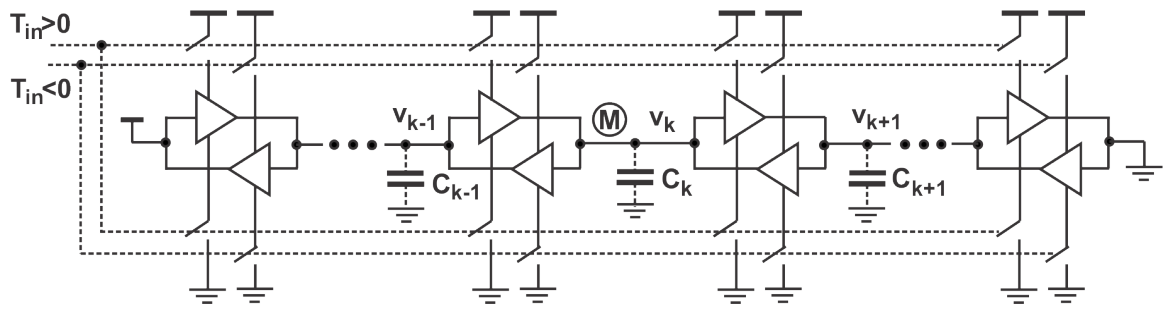

Figure 4.2: Bi-directional gated delay line. When T_{in} is positive, the forward direction is enabled, and T_{in} is negative, the reverse direction is enabled.

To demonstrate that the bi-directional gated delay line functions as a time integrator, consider a train of 5 pulses, $T_{in,k}$, $k = 1, 2, ..., 5$ with $T_{in,1} = 1.2\tau$, $T_{in,2} = 1.5\tau$, $T_{in,3} = -1.1\tau$, $T_{in,4} = 0.7\tau$, and $T_{in,5} = -2.5\tau$ where τ is the per-stage delay. Assume $V_{1n} = V_{2n} = V_M = 1$ and $V_{1p} = V_{2p} = 0$ initially. The rate of change of the output voltage of gated delay cells is $V_{T,GDL}/\tau$. With $T_{in,1} = 1.2\tau$, logic-1 at node M propagates through one stage in the forward direction and charges C_{1p} to $0.2V_{T,GDL}$. Similarly, with $T_{in,2} = 1.5\tau$, the signal continues to propagate through 2 stage and charges C_{2p} to $0.7V_{T,GDL}$. When $T_{in,3} = -1.1\tau$ arrives, the forward gated delay line is disabled while the reverse gated delay line is activated. Since $v_{3p} = 0$, the charge of C_{2p} is discharged. The same for v_{1p}. It becomes evident that the bi-directional gated delay line performs the accumulation (integration) of $T_{in,k}$. To digitize the result of the time integration, DFFs can be deployed at the output of each gated delay stage. The output of the time integrator is a thermometer code in the form 1...10...0 with the left-most 0 specifying the vanishing location of the node M.

It becomes apparent that the maximum quantization error of the time integrator, denoted by Δ_{max}, is τ. The actual quantization error, denoted by Δ_k, is preserved in the form of the voltage of the load capacitor $v_{c,k}$ of the stage whose right-adjacent stage has an output of 1. Utilizing the relation between $V_{T,GDL}$ and τ, we arrive at

$$\Delta_k = \frac{v_{c,k}}{V_{T,GDL}}\tau. \tag{4.3}$$

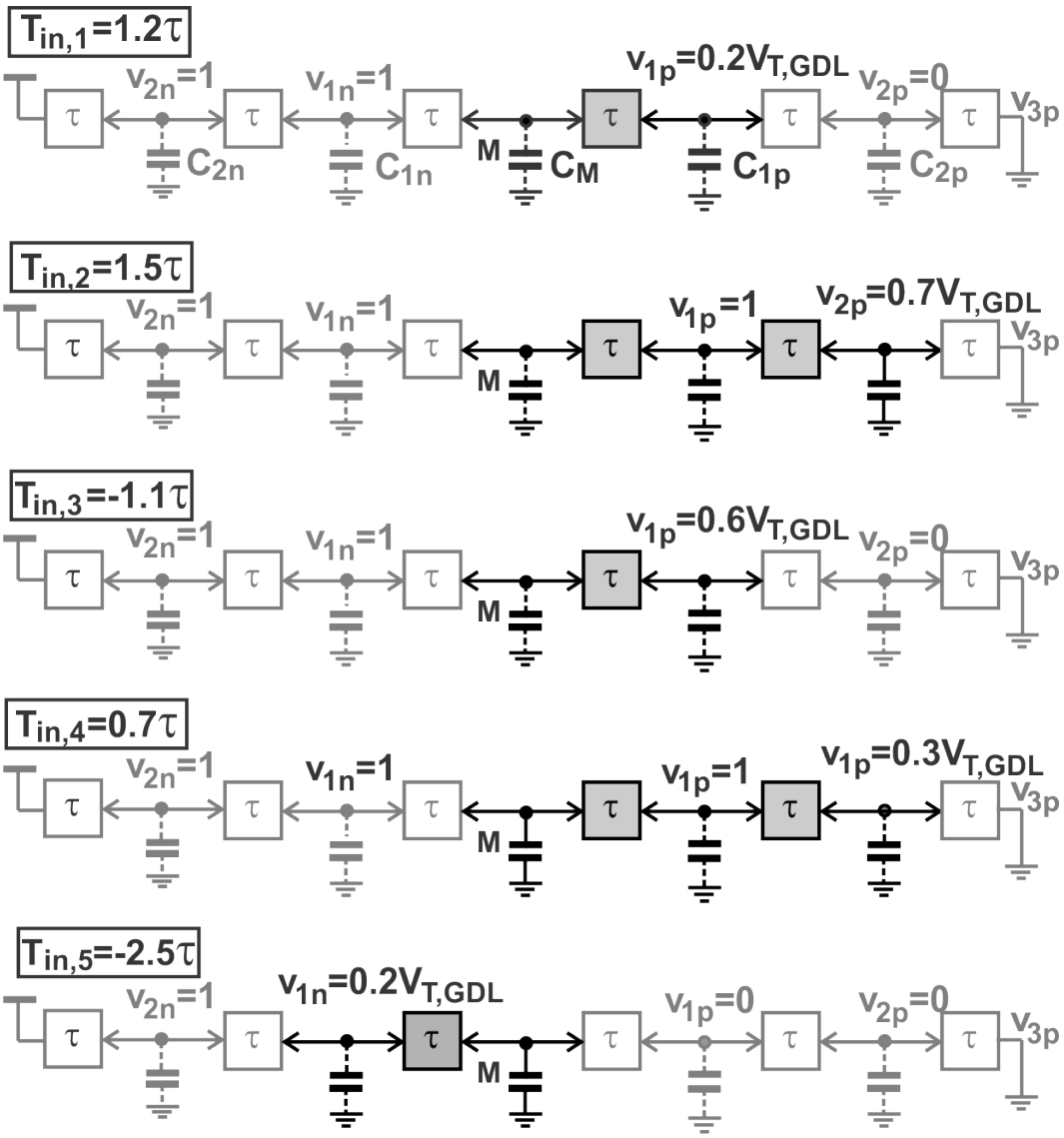

Figure 4.3: Signal propagation in bi-directional gated delay line. The bold lines highlight the path that the signal propagates. Gating signals are not shown for brevity.

4.3 All-Digital First-Order Single-Bit $\Delta\Sigma$ TDC

In this section, we utilize the preceding time integrator to construct an all-digital first-order $\Delta\Sigma$ TDC with a single-bit time quantizer. To construct the time quantizer, we notice that the output of the bi-directional gated delay line time integrator is a thermometer code. If the output of the time integrator is larger than τ, i.e., $\sum_{k=1}^{K} T_{in,k} > \tau$, v_{1p} will be set to 1. Otherwise, it will be set to 0. Note that since $\Delta_{max} = \tau$, $0 < \sum_{k=1}^{K} T_{in,k} < \tau$ cannot

be detected. This observation reveals that the output of the delay stage right-connected to node M provides the single bit quantization of the output of the integrator.

The subtraction of feedback time feedback, T_{fb}, from the input time variable T_{in} is performed using a digital-to-time converter (DTC) shown in Fig.4.4(A). The multiplexers are controlled by the output of the time comparator D_{out}. If $D_{out} > 0$, T_{fb} is subtracted from T_{in} by delaying the leading edge A by T_{fb}. Otherwise, it is added to T_{in} by delaying the leading edge B by T_{fb}. The resultant T_{err}, along with its polarity, are connected to $|T_{in}|$ block to make a negative input a positive input. 200 ps time offset T_{off} is added to generate an enable pulse applied to the bi-directional gated delay line time integrator. The polarity of T_{err} is determined using a DFF whose output is 1 if $T_{err} > 0$ and 0 otherwise.

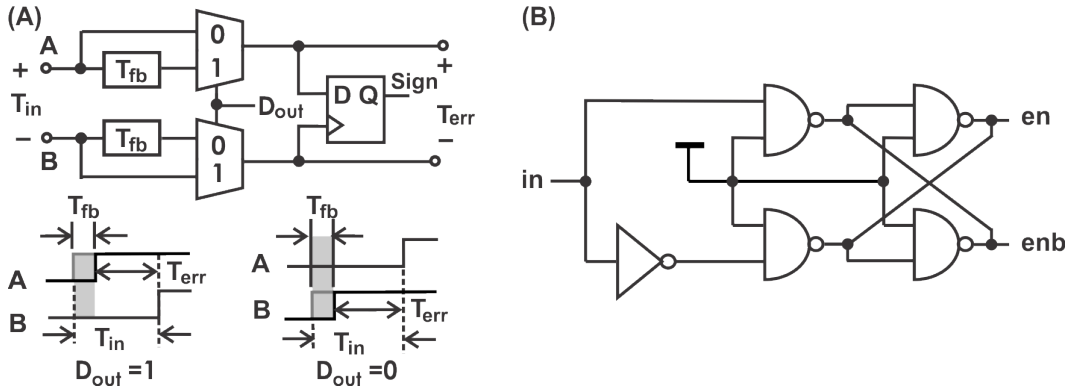

Figure 4.4: (A) Digital-to-time converter [10], (B) Edge alignment block [11].

The all-digital first-order single-bit $\Delta\Sigma$ TDC shown in Fig.4.5 consists of a DTC a 30-stage bi-directional gated delay line time integrator, and a time comparator. All blocks are realized using digital logic. To turn on/off PMOS and NMOS simultaneously for bi-directional gated delay line time integrator, we used an edge alignment block shown in Fig.4.4(B).

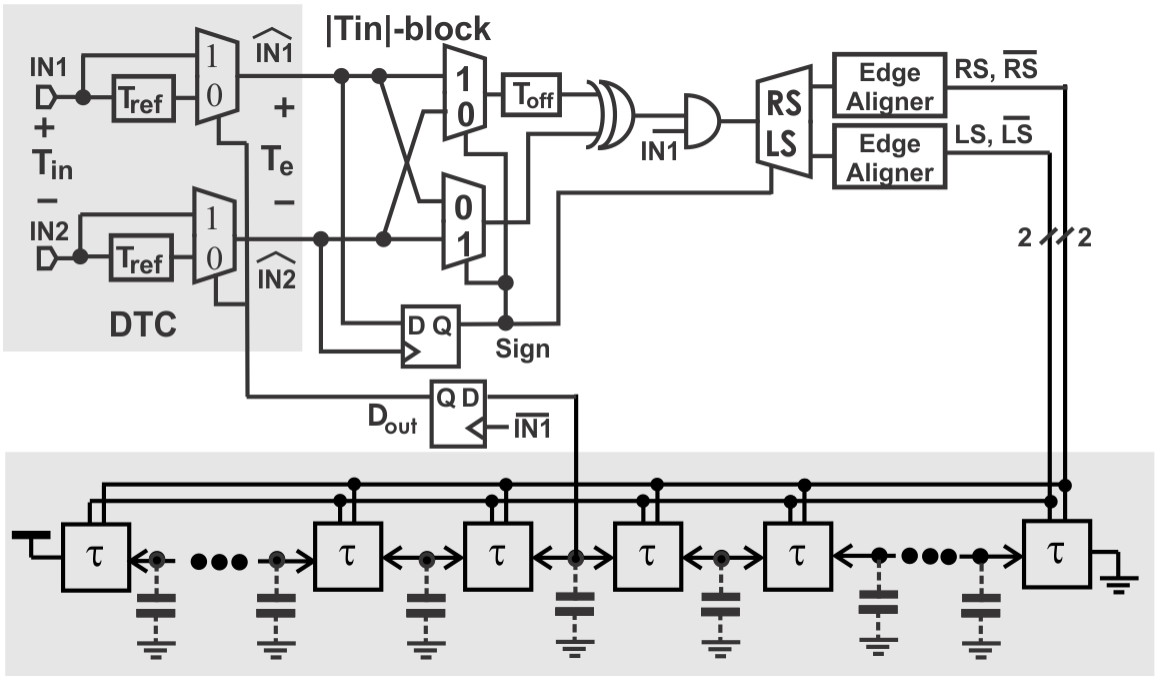

Figure 4.5: All-digital first-order ΔΣ TDC with a single-bit time quantizer.

4.4 Design Considerations

In this section, we examine issues affecting the performance of the ΔΣ TDC. (i) As the load capacitor of the gated delay stage is isolated from the gated MOS switching transistors by either a PMOS or a NMOS transistor, the effect of charge injection from the switching transistors and clock feed-through from T_{in} to the load capacitor is minimized. (ii) Gated delay cells in forward and reverse directions should be identical such that if $\sum_{k=1}^{K} T_{in,k} = 0$, $\sum_{k=1}^{K} v_{c,k} = 0$ will follow, as illustrated in Fig.4.6. Should mismatches between forward and reverse gated delay cells exist, $\sum_{k=1}^{K} v_{c,k} \neq 0$ even though $\sum_{k=1}^{K} T_{in,k} = 0$. (iii) Similar to delay-line TDCs, per-stage delay mismatch in either forward or reverse directions gives rise to the nonlinearity of the time integrator and the degree of nonlinearity deteriorates with the increase in the length of the gated delay line. (iv) The range of the output of the integrator is set by both per-stage delay and the number of delay stages. In order for the time integrator to have a large range without employing a large number of delay stages, the per-stage delay can be gradually increased when moving away from the middle node of the delay line. Since for ΔΣ TDCs, T_{err} is small in the steady state, a large per-stage delay of stages distance

away from the middle node will not affect the performance of the modulator. Since we add T_{off} shown in Fig.4.5 for XOR to make a pulse, we need to compensate it. This is simply done by obtaining the final output of the 1 bit quantizer from the shifted location based on T_{off}, not just taken from the middle location.

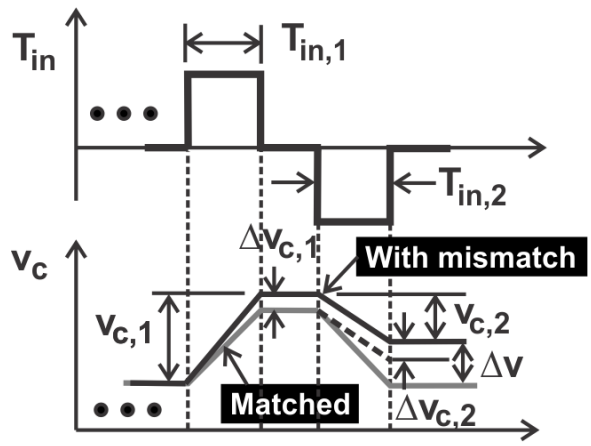

Figure 4.6: Effect of mismatch between forward and reverse gated delay cells.

4.5 Simulation Results

The all-digital first-order $\Delta\Sigma$ TDC was designed in an IBM 130 nm 1.2 V CMOS technology and analysed using Spectre from Cadence Design Systems with BSIM4 models. The bi-directional gated delay line has a total 30 stages. The outputs of the 15 stages to the left from the node M were set to 1.2V and those of the 15 stages to the right from node M were set to 0V in an initialization phase. A sinusoid time signal of frequency 232 kHz and amplitude 430 ps was digitized by the proposed $\Delta\Sigma$ TDC. Fig.4.7 shows the spectrum of the $\Delta\Sigma$ TDC obtained using FFT analysis with 2048 samples and a Hanning window. First-order noise-shaping is evident.

In Table 4.1, the performance of recently published time-mode $\Delta\Sigma$ TDCs is compared with this work. This work has advantage in terms of power consumption since it does not

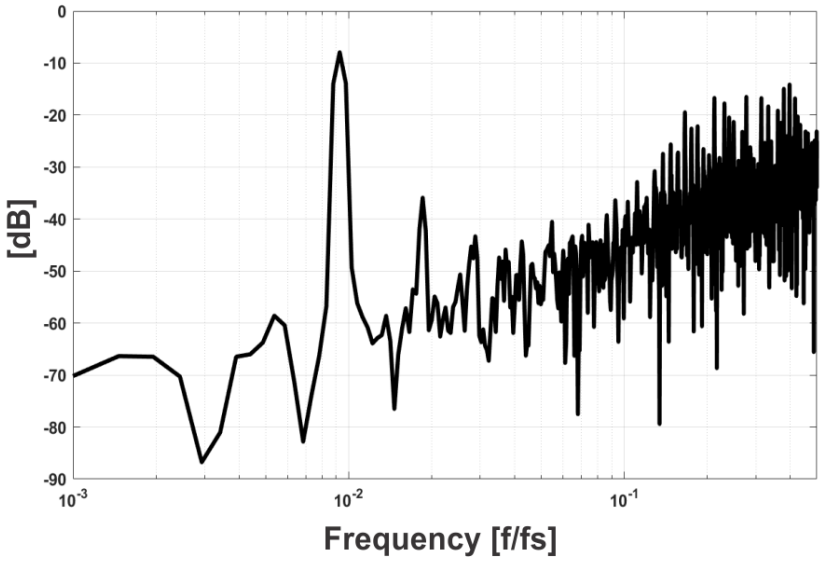

Figure 4.7: Spectrum of $\Delta\Sigma$ TDC. f_{in} = 231.93 kHz, f_s = 25 MHz. ENOB = 6.3 over frequency band 36.62∼232 kHz.

Table 4.1: Performance comparison of $\Delta\Sigma$ TDCs.

Ref.	Tech. (nm)	V_{DD} (V)	BW (Hz)	OSR	Res. (ps)	PWR (mW)	Order
[13]	130	1.5	1M	25	1	2.2-21	1st
[22]	180	1.8	400k	348	8.7 (*)	0.78	1st
[41]	130	1.2	100k	250	11	1.7	3rd
[10]	32	1.0	100k	50	4.4	0.25	1st
This	130	1.2	232k	54	10.8 (**)	0.046	1st

* This is the effective number of bits (ENOB).
** Raw resolution is 96ps.

consume any static power and spends power only during the enable time in the bi-directional gated-delay time integrator.

4.6 Chapter Summary

A bi-directional gated delay line time integrator and its applications in an all-digital first-order $\Delta\Sigma$ TDC were presented. The time integrator consists of a bi-directional gated

delay line with the time variable to be integrated as the gating signal. The accumulation of time variables is performed via the accumulation of the charge of the load capacitor and logic state of the gated delay stages. Issues critically affecting the performance of the integrator were examined. With a sinusoid time input of frequency 232 kHz with OSR 54 and amplitude 430 ps, the $\Delta\Sigma$ TDC exhibits first-order noise-shaping and provides an effective time resolution 10.8 ps which is lower than one inverter delay over frequency band 36.62$\sim$232 kHz while consuming 46 μW.

Chapter 5

Conclusions

5.1 Conclusions

This dissertation dealt with the design of sub-per-stage-delay TDCs to minimize silicon consumption without sacrificing resolution and conversion time. Two classes of TDCs namely pulse-shrinking TDCs and $\Delta\Sigma$ TDCs were studied.

In pulse-shrinking TDCs, a two-step pulse-shrinking TDC consisting of a set of coarse and fine pulse-shrinking TDCs was proposed to increase a dynamic range without employing a large number of pulse-shrinking stages. A residual time extraction scheme capable of extracting the residual time of the coarse TDC was developed. The simulation and measurement results of the TDC implemented in an IBM 130 nm 1.2 V CMOS technology shows that the TDC offers 1.4 ns conversion time, 1 LSB DNL and INL, and consumes 0.163 pJ/step. To further improve the conversion time of the 2-step pulse-shrinking TDC, a time-interleaved scheme was developed to extract the residual time of the coarse TDC. Residual time extraction is carried out in parallel with digitization so as to minimize conversion time. The simulation and measurement results of the TDC show that the TDC offers 0.85 ns conversion time, 0.285 LSB DNL, and 0.78 LSB.

In $\Delta\Sigma$ TDCs, a 1-1 MASH $\Delta\Sigma$ TDC with a new differential cascode time integrator was presented to suppress even-order harmonic tones and current mismatch-induced timing errors. Simulation results show that the TDC offers 1.9 ps time resolution over 48-415 kHz

signal band while consuming 502 μW. Finally, an all-digital first-order $\Delta\Sigma$ TDC utilizing a bi-directional gated delay line integrator was developed. Time integration is obtained via the accumulation of charge of the load capacitor of gated delay stages and the logic state of gated delay stages. The elimination of analog components allows the TDC to benefit many desirable characteristics of time-mode signal processing especially excellent scalability with technology. Simulation results show that the TDC offers first-order noise-shaping, 10.8 ps time resolution while consuming 46 μW.

5.2 Future Work

Bi-directional gated delay line integrator was proposed in this dissertation for the very first time. In order to utilize this integrator in emerging applications such as all-digital $\Delta\Sigma$ modulators and ADPLLs, more work is needed. Below are some future research topics :

- Auto calibration : The per-stage-delay of gated delay cells in forward and reverse directions should be identical such that if $\sum_{k=1}^{K} T_{in,k} = 0$, $\sum_{k=1}^{K} v_{c,k} = 0$ will follow. Should mismatches between forward and reverse gated delay cells exist, $\sum_{k=1}^{K} v_{c,k} \neq 0$ even though $\sum_{k=1}^{K} T_{in,k} = 0$. Manual calibration is done in the dissertation work. Automatic foreground calibration should be developed.

- Residue extraction : If we can extract the residue time information accurately, we can build higher-order $\Delta\Sigma$ modulators using MASH to lower in-band quantization noise. The residue time information can be extracted in a similar way as that used in [23]. However, since the bi-directional gated delay line integrator stores time information all the time, it cannot be reset. New residue extraction methods that are different from that in [23] are needed.

- Multi-bit quantization : The developed bi-directional gated delay line integrator can be used as a multi-bit quantizer naturally since it is based on the GDLs whose output constitutes a thermometer code. With multi-bit digital-to-time converters (DTCs), we

can have lower quantization noise to per-stage-delay. As a result, in-band noise can be further lowered via $\Delta\Sigma$ operation.

- Bi-directional gated delay line integrator can be used in ADPLLs to replace TDC phase detectors and loop filters since it performs both accumulation and digitization simultaneously, thereby significantly simplifying the design of ADPLLs.

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