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New bang-bang phase detectors for high-speed serial links

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NEW BANG-BANG PHASE DETECTORS FOR HIGH-SPEED SERIAL LINKS

by

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Abstract

Bang-bang phase detector studies were carried out in this thesis. Based on the comparison of linear and non-linear phase detectors, a hybrid phase detector was proposed. It possesses the characteristics of two-XOR phase detectors and improved bang-bang phase detectors. PLLs with the proposed hybrid phase detector possess low timing jitter in lock states and a fast locking process. The effectiveness of the proposed hybrid phase detector was quantified by comparing the performance of three PLLs with identical loop components but different phase detectors. A new bang-bang phase detector with regenerative DFFs was also proposed. The regenerative bang-bang phase detector ensures a fast acquisition of incoming clocks. The effectiveness of the regenerative phase detector was assessed in a 2GHz PLL. A 1X bang-bang phase detector was proposed also. Compared to a 2X bang-bang phase detector, PLLs with a 1X bang-bang phase detector offer faster locking. A DFF frequency detector and a charge-pump frequency detector were also proposed. Both effectively detect the frequency difference.

Acknowledgments

I am deeply indebted to Professor Fei Yuan for granting me the honor of being a member of his research group and for his enthusiastic support, constant guidance and inspiration throughout the course of this research. I have benefited from his vast technical expertise, insight, and his high-standards in research, teaching and publication.

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Chapter 1

Introduction

1.1 Motivation

Data and information exchange are the key features of modern communication systems. The faster data flows, the wider system bandwidth is required. Data exchange occurs between modules on a chip, chips on a board, boards in a system and systems in a network. Conventional high-speed circuits are built in either GaAs or Bipolar technologies. With the rapid down scaling of the feature size of MOS devices, reduced power consumption and high integration density, CMOS have become the dominant technologies. Traditionally, system designers have addressed the issue that increasing the number of signals of a high-speed system will lead to an increase in both the cost and complexity of the system[1]. There are two basic schemes for high-speed data communications, namely high-speed parallel links shown in Fig.1.1 and high-speed serial links shown in Fig.1.2. With parallel links plagued by a variety of problems such as cross talk, timing skews between channels and reference clock, and different noise backgrounds for signal channels and the reference clock, serial architectures are poised to take over in high-end networks and computer systems. Multiple serial links are now used to improve communication bandwidth.

As compared with parallel links, serial links offer the following advantages:

(1) Serial links use only one wire or one channel to transmit data and clock, avoiding cross talk.

(2) The clock information is embedded in data streams, avoiding timing skew.

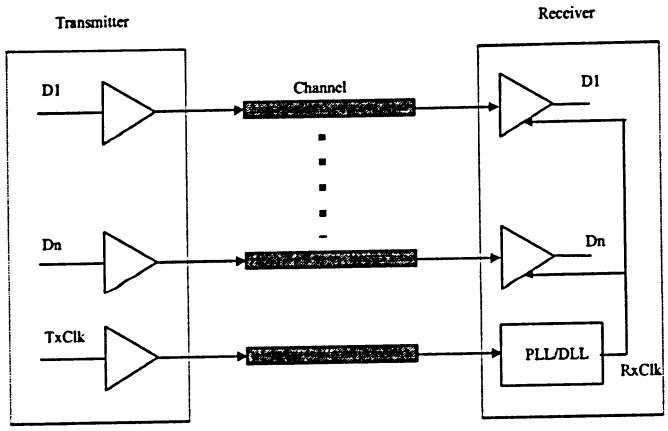

Figure 1.1: Structure of high-speed parallel links.

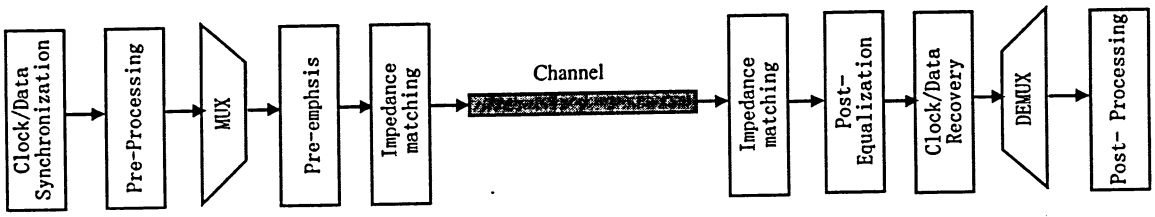

Figure 1.2: Structure of high-speed serial links.

The optical transmission system illustrated in Fig.1.3 is a typical application of serial links. Basically it composes of a transmitter, a driver, a LED or a laser diode, optical fibers and a photodiode, a pre-amplifier, and a receiver. Optical communications standard interfaces are listed in Table.1.1.

Other industrial standard high-speed interfaces are, but not limited, PCI EXPRESS, XAUI, Rapid I/O, Fiber Channel, Serial ATA, and 1000 Base-X, etc. The advanced FPGAs have even integrated Rocket I/O serial link transceivers, for instance Xilinx FPGAs. Table.1.2 shows these interfaces and their data rate. The applications of these links are diverse, from computer-to-peripheral connections, local area networks, memory-busses, and multiprocessor interconnection networks.

As depicted in Fig.1.2, high-speed serial links compose of a transmitter, a channel and a receiver. The receiver composes of a pre-amplifier, a post equalization block, a clock and data recovery (CDR) and a DEMUX. Among them, CDR is the key component.

CDR is a circuit that takes in random serial data, recovers the clock from the data, and

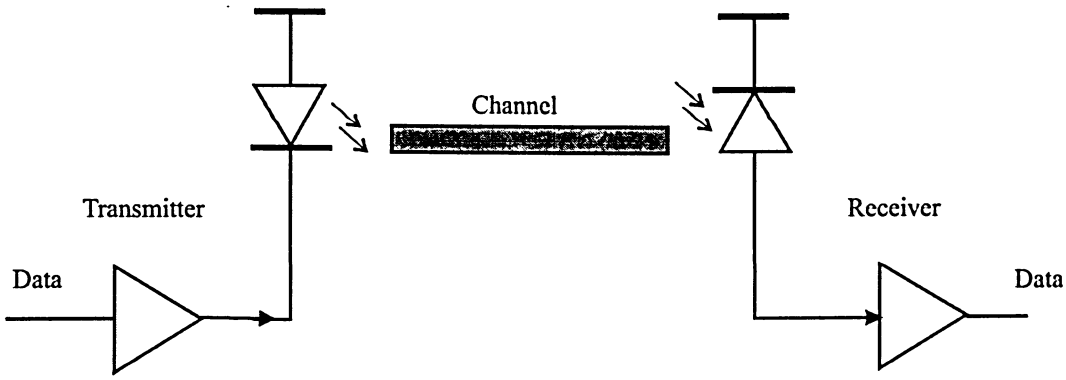

Figure 1.3: Basic configuration of optical communication links.

Table 1.1: High-speed interfaces in SONET/SDH.

SONET	SDH	Data Rate(Mb/s)
T1	E1	1.544/2.048
T3	E3	34/44.736
OC-1	—	51.84
OC-3	STM-1	155.52
OC-12	STM-4	622.08
OC-24	—	1244.16
OC-48	STM-16	2488.32
OC-96	—	4976.64
OC-192	STM-64	9953.28

Table 1.2: Applications of high-speed serial links.

Interface	Data Rate[bps]	Application
XAUI	3.125G x 4	10G Ethernet
PCI Express	2.5G	AGP bus
Radid I/O	1.25/2.5/3.125G	Processor interconnection
Fibre Channel	1.0625/2.125G	Storage area networks
Serial ATA	1.5/3.0G	Computer bus
1000 Base-X	1G	Ethernet

re-times the data by the recovered clock. Three approaches exist to design CDRs, namely phase picking, phase tracking, and current integration. In phase-picking CDR depicted in Fig.1.4, the incoming random data is sampled by a set of samplers. The recovered data and clock are selected by the data picking logic and clock picking logic by comparing the sample values to determine the data transition edge. The major drawbacks of the phase-picking CDR are the large capacitance load to the channel and the phase quantization error due to the clock-phase interval of samplers. The advantage of it is its simple open-loop structure. In Fig.1.6, a CDR using a integrating scheme is presented. This scheme is capable of filtering out transient noise presenting in the channel[16].

The phase-tracking approach has been extensively used in CDR design. Its structure is shown in Fig.1.5. In this scheme, the PLL, as a servo system, is used to align clock edges from its VCO to the input data transition edges. The phase-tracking CDR performs well in a harsh environment because it is a close-loop feedback system. The phase difference is corrected by the PLL.

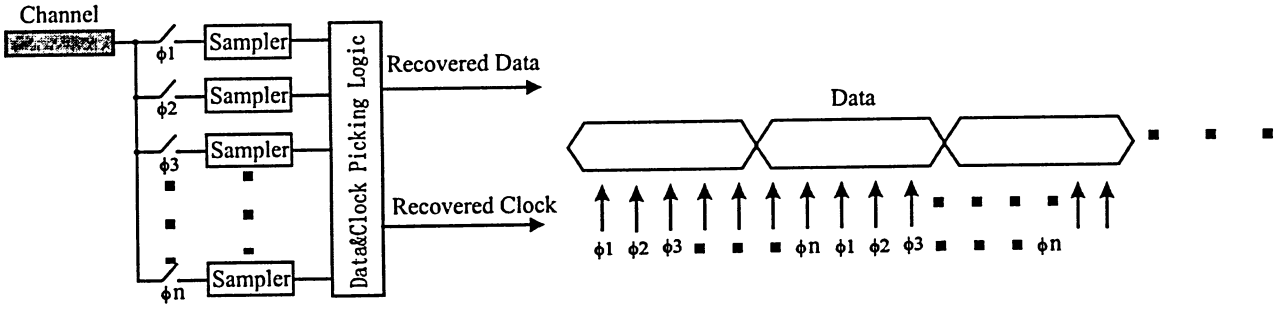

Figure 1.4: CDR using phase-picking scheme.

A PLL plays a key role in phase-tracking CDR. The property of the recovered clock and data is mostly determined by the performance of the phase detector of the PLL, which senses the phase difference between the edge of the incoming data and that of the clock output of the VCO. Although many phase detectors exist[2], not all the phase detectors are suitable for CDRs. Random data is different from clock signals, which results in random-data phase detectors are different from clock phase detectors. Gilbert cell phase detector is basically a multiplier. In theory, $sin(\omega_0 t + \theta_1) * sin(\omega_1 t + \theta_2) \simeq sin(\theta_2 - \theta_1) \approx (\theta_2 - \theta_1)$

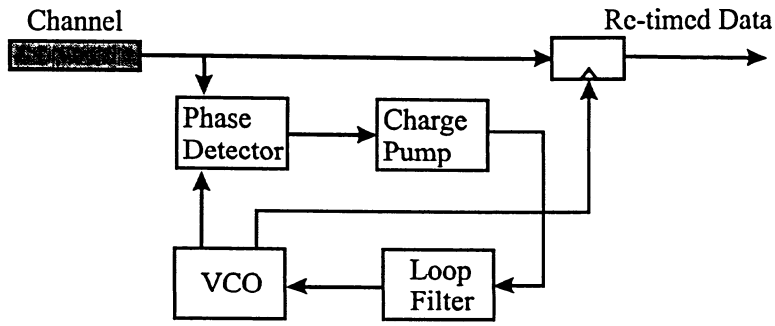

Figure 1.5: CDR using phase-tracking scheme[16].

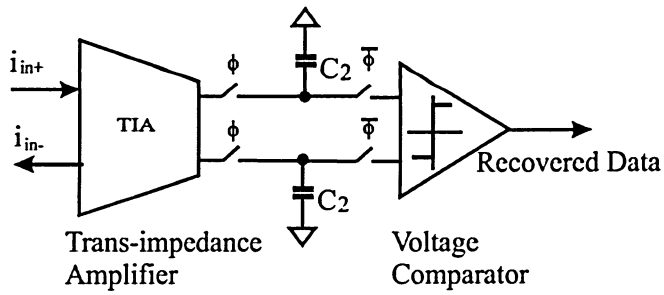

Figure 1.6: CDR using integrating scheme[16].

when $(\theta_2 - \theta_1)$ is very small, $\omega_1 + \omega_0$ and other high frequency terms are filtered out, and ω_0 is equal to ω_1. When ω_0 is not equal to ω_1, obviously Gilbert cell phase detector does not hold the phase-detection function for random data. S-R latch phase detectors and D-FF phase/frequency detectors are not random data phase detectors neither. The following phase detectors could function as random-data phase detectors: 2XOR phase detectors, bang-bang phase detectors, Hogge phase detectors, Alexander phase detectors, and half-rate phase detectors [3]. Among them, bang-bang phase detectors have been extensively employed in the industries due to its high gain and high-speed properties. Studies show that bang-bang phase detector loops have become a common design choice for CDRs[10]. Fig.1.7 surveys CDR presented at international Solid State Circuits Conferences. The figure is plotted by year against each design's ratio of the link speed to effective f_T. It shows that the higher the link speed becomes, the more frequently the bang-bang phase detector PLLs are used.

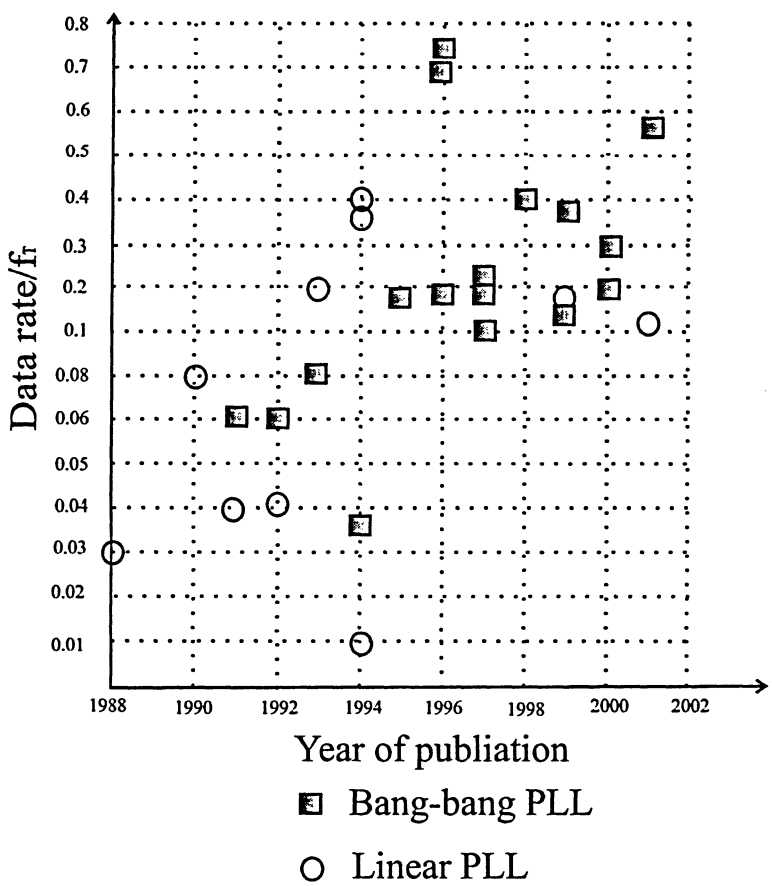

Figure 1.7: Comparison of data rate of PLLs for CDR[10].

1.2 Original Contributions

This thesis presents three new random data phase detectors,

(1) Hybrid phase detector,

(2) Bang-bang phase detector with regenerative DFFs,

(3) 1X bang-bang phase detector.

All of them have been implemented in PLLs with 0.13μm and 0.18μm technologies. The PLL locking time, clock output jitter performance and PLL output phase noise are improved by these phase detectors.

- The combination of linear and non-linear phase detectors has a high gain in the PLL locking process when the phase error is large, and a low gain when the phase error is small. With this phase detector, the PLL has a reduced locking time, and low jitter and phase noise on its clock output. The linear phase detector used in the design is a 2XOR phase detector while the non-linear one is an improved bang-bang phase detector.

- The first new bang-bang structure is based on sense amplifiers. TSPC D-flip flop is limited by its four-stage propagation in the row on speed. This aspect has been improved by the bang-bang structure with regenerative DFFs.

- The 1X bang-bang phase detector is an improved and simplified structure of the traditional bang-bang phase detectors. Compared with the conventional 2X bang-bang phase detector, the 1X bang-bang phase detector reduces circuit area by 30% approximately and extends the phase detection range.

All these phase detectors have been implemented in the same PLL structure and building blocks to compare their performance. The simulation results have shown and confirmed the properties expected in the designs.

IEEE submissions that related to this thesis are listed as follows:

- Jiwang Li and Fei Yuan "A New Hybrid Phase Detector for Reduced Lock Time and Timing Jitter of Phase-locked Loops," Analog Integrated Circuits and Signal Processing. Submitted in September 2006, revised in August 2007.

- Jiwang Li and Fei Yuan "A New 1X Bang-bang Phase Detector for Fast Locking of Phase-locked Loops," IEEE Transactions on Circuits and Systems II - Express Briefs. Submitted in June 2007.

- Jiwang Li and Fei Yuan "A New Bang-bang Phase/Frequency Detector for Fast Locking of Phase-locked Loops," IEEE Mid-West Symp. Circuits and Systems, Montreal. Accepted for publication in May 2007.

1.3 Thesis Organization

This thesis is organized as the following:

Chapter 1 presents the motivation of this research, the typical structures of high-speed serial links and high-speed parallel links, and the applications of high-speed serial links. The concept of CDR and its three implementation schemes are also described.

Chapter 2 describes the background knowledge, such as basic high-speed serial link schemes, basic PLL concept, timing jitter metrics, and data coding schemes used in high-speed serial links to ensure enough transition edges embedded in the data stream for clock recovery.

Chapter 3 investigates phase detectors, such as 2XOR phase detectors, RS phase detectors, DFF phase detectors, and existing bang-bang phase detectors, and their characteristics. A critical comparison of circuit structure, phase detection range and effect on PLLs is provided.

Chapter 4 investigates the single loop and dual loop PLL architectures and their building blocks used in this thesis. These blocks include frequency detectors, charge pumps, loop filters, VCOs and delay cells. Circuit implementations are also presented.

Chapter 5 describes the design of the hybrid phase detector that combines a linear 2XOR phase detector and a non-linear improved bang-bang phase detector. A comparison between the 2XOR phase detector, the hybrid phase detector and the improved bang-bang phase detector in the same PLL with identical charge pumps , loop filter, and VCO is provided.

Chapter 6 details the design of the bang-bang phase detector with regenerative DFFs and its implementation in a PLL. The simulation results of the timing jitter and phase noise are presented.

Chapter 7 describes the 1X bang-bang phase detector and its comparison with a conventional 2X bang-bang phase detector. The layouts of the PLLs implemented in 0.18μm, 1.8V, 8-metal CMOS technology are also presented in this chapter.

The thesis is concluded in Chapter 8.

Chapter 2

Background

This chapter gives an overview of clock and data recovery and phase-locked loops used in high-speed serial links. Basic concepts of PLLs and design challenges in serial links are investigated.

2.1 Fundamentals of High-Speed Serial Links

As depicted in Fig.1.2, there are three primary components in a data link: a transmitter, a channel, and a receiver. Registers are widely used in the data and clock synchronization in transmitters and receivers. The multiplexer is used to serialize the parallel data at the transmitter end. The de-multiplexer is employed to parallelize the serial data at the receiver end. The pre-emphasis and the post-equalization are the two techniques used to compensate for the high-frequency loss of the transmission channel at the transmitter end and the receiver end, respectively. At the receiver end, clock regeneration is the key function in order to recover the data due to the channel noise, clock jitter and ISI of the signaling. Phase picking, phase tracking and integration are the three extensively used techniques in clock and data recovery[16].

2.2 Phase-Picking CDR

Fig.2.1 gives a scheme example of phase-picking clock and data recovery. As shown, the incoming data is oversampled by a multi-phase clock. In this example, each bit of data is

sampled four times per data eye. The samples are fed to an XOR logic circuit. The clock phase that has the most Logic-1s is the one most close to the data transition edges. So this clock phase and its sample are selected as the recovered clock and data. When the data has successive '1' or '0', the CDR will keep using the most recent estimated clock as the recovered clock to retime the data. In this example, $\phi 1$ has the most '1's, and it could be selected as the clock that is approximately aligned with data transition edges and $\phi 3$ could be selected to re-time the data. Obviously, the main drawback of this scheme is the requirement of the high frequency clocks, and also high-speed XORs and counters to determine the recovered clock. Another drawback is that the long-term jitter is high since the available clocks are discrete with a large certain phase interval[16].

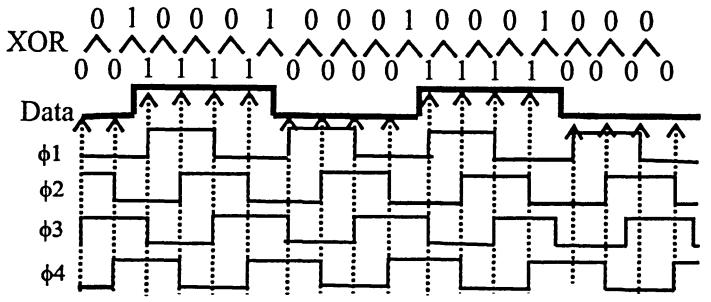

Figure 2.1: Phase-picking CDR using 4X oversampling[16].

2.3 Integrating Receiver Scheme

An integrating receiver scheme is shown in Fig.2.2. In τ period of time, the phase-picking CDR may get a false sample, while an integrating CDR could get the true value based on the area under the data waveform. The advantage of this scheme is that the sample value is determined by the area under the data voltage or current signal curve rather than a sample at a time point. This scheme shows a good immunity to noise. However design challenges exist, as shown in [16].

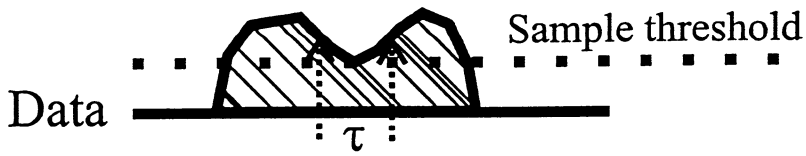

Figure 2.2: Integrating CDR scheme.

2.4 Phase-Tracking CDR

A phase-tracking CDR is built with a PLL that tracks the incoming data transition edges to regenerate the clock and further to retime the data. A typical structure is shown in Fig.2.3. The main blocks of this CDR are a phase/frequency detector(for random data), a charge pump, a loop filter, and a VCO. The PLL acts as an electronic servomechanism to suppress unwanted frequency and phase fluctuations in the incoming data. The PLL should have a fast response, and narrow bandwidth to suppress the timing fluctuations [19]. The phase difference between the data transition edges and the PLL output is measured by the phase/frequency detector in the PLL. The output of the phase/frequency detector drives the charge pump whose outputs adjust the loop filter. The loop filter is the component to establish the loop dynamics and deliver a suitable control signal, V_{ctrl}, to the VCO [16].

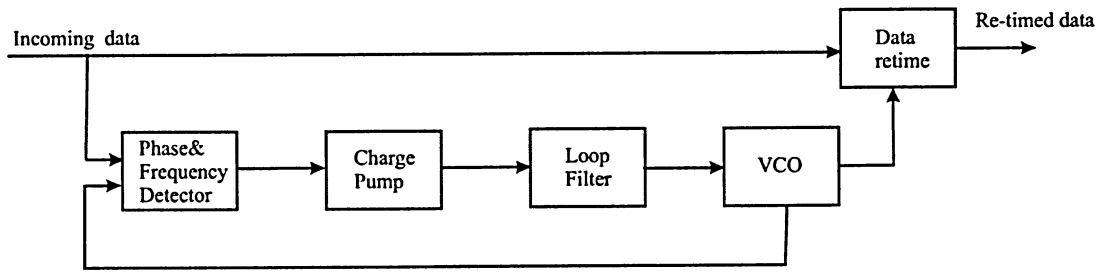

Figure 2.3: PLL-based CDR.

2.5 PLL Basics

A PLL averages the error over some length of time and the average is used to set the frequency and the phase of the VCO output. A PLL usually consists of a phase/frequency detector, a charge pump, a loop filter, and a VCO. The phase/frequency detector converts

the phase/frequency difference between the incoming data and the VCO output into a signal whose average voltage is proportional to the phase error. This signal is filtered by the loop filter to generate the control voltage, V_{ctrl}, which controls the oscillation frequency of the VCO.

As shown in Fig.2.4, an basic PLL consists of a phase detector, a loop filter, and a VCO. The phase of the input signal is denoted by $\theta_i(t)$ and the phase of the VCO output signal is denoted by $\theta_o(t)$. The phase detector output is denoted by $\nu_d(t)$.

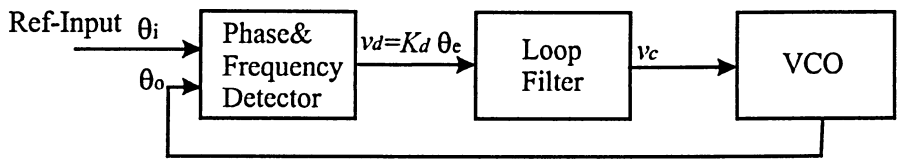

Figure 2.4: Basic PLL structure.

$$\nu_d(t) = K_d(\theta_i - \theta_o), = K_d\theta_e. \tag{2.1}$$

Where K_d is the gain factor of the phase detector.

$$\theta_e = (\theta_i - \theta_o). \tag{2.2}$$

The analytical design of PLLs is typically carried out using transfer functions. Each time domain signal can be presented by a signal in the Laplace transform domain. $\theta_i(t)$ is presented by $\theta_i(s)$, $\theta_o(t)$ is presented by $\theta_o(s)$, $\nu_d(t)$ is presented by $\nu_d(s)$, and $\nu_c(t)$ is presented by $\nu_c(s)$. The loop filter transfer function is denoted by $F(s)$.

$$\nu_c(s) = F(s)\nu_d(s). \tag{2.3}$$

The VCO is presented by

$$\theta_o(s) = \frac{K_o\nu_c(s)}{s}, \tag{2.4}$$

where K_o is the VCO gain factor and has the unit of rad/sec.V. Open loop transfer function of the PLL is given by

$$G(s) = \frac{\theta_o(s)}{\theta_e(s)} = \frac{K_d K_o F(s)}{s}. \tag{2.5}$$

The close-loop transfer function is given by

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{G(s)}{1 + G(s)}. \tag{2.6}$$

If the close-loop transfer function's denominator polynomial is of N degree, the PLL is called the N-order PLL. The term of the loop type, borrowed from the control system community, refers to the number of the integrals within the loop. In a PLL, a VCO is one integral due to

$$\frac{d\theta_o(t)}{dt} = K_{vco} V_c(t). \tag{2.7}$$

A loop filter has at least one integral capacitor.

Undamped natural frequency (ω_n) and damping factor (ξ) are important parameters for a second-order PLL. And the system transfer function can be written as

$$H(s) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}, \tag{2.8}$$

When $\xi < 1$, ω_n is the magnitude of the poles, and the $\alpha = cos^{-1}\xi$ is the clockwise angle from the negative real axis to the location of the pole in a complex plane; when $\xi = 1$, the poles are real and coincident; when $\xi > 1$, the poles are real and separate. The poles of a second-order PLL are shown in Fig.2.5. ξ is expected to be in between 0.5–2 with 0.707 as the preferred value.

The above PLL analysis is valid for linear phase-locked loops. It is not valid for nonlinear phase-locked loops.

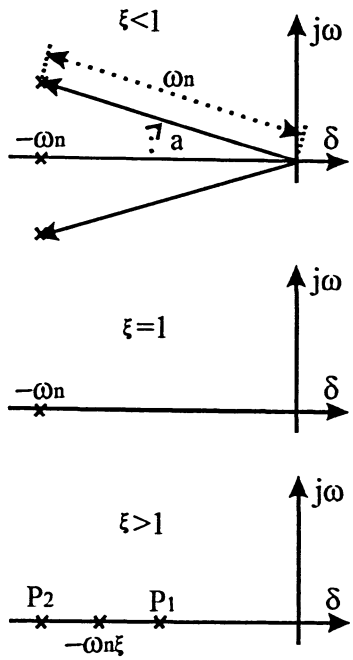

Figure 2.5: Poles of second-order PLLs, $\alpha = cos^{-1}\xi$, $P_1 = \omega_n(-\xi + \sqrt{\xi^2 - 1})$, $P_2 = \omega_n(-\xi - \sqrt{\xi^2 - 1})$.

2.6 Jitter and Phase Noise

2.6.1 Jitter metrics

Noise present in binary signals is commonly characterized in terms of jitter. Jitter is an undesired perturbation or uncertainty in the timing of events. When the clock output of a PLL is employed in digital circuits, timing jitter affects the setup-time and hold-time margins. As shown in Fig.2.6, setup time and hold time are affected by the timing jitter.

Denoted by J_{ee}, edge-to-edge jitter is the simplest metric to measure timing jitter. J_{ee} is the variation in the delay between a triggering event and the response event,

$$J_{ee}(i) = \sqrt{var(t_i)}. \tag{2.9}$$

As depicted in Fig.2.7 (a), the input signal or clock is jitter-free, and J_{ee} is measured between the edge of the input and that of the output.

Another jitter metric, called k-cycle jitter, characterizes the correlation between signal

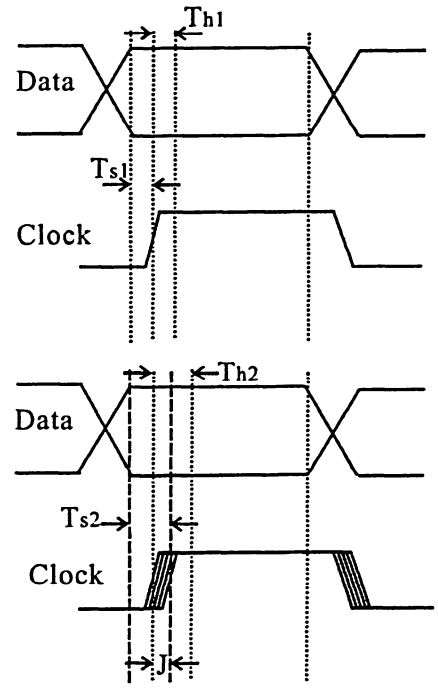

Figure 2.6: Timing jitter, T_{s2}=T_{s1}+J, T_{h2}=T_{h1}+J.

transitions as a function of how far the transitions are separated in time. Depicted in Fig.2.7 (b), k-cycle jitter is measured by the time difference between the transition t_i and t_{i+k}.

$$J_k(i) = \sqrt{var(t_{i+k} - t_i)}. \tag{2.10}$$

The third jitter metric is the cycle-to-cycle jitter shown in Fig.2.7 (c). It is measured by the difference of two adjacent cycle periods,

$$J_{cc}(i) = \sqrt{var(T_{i+1} - T_i)}. \tag{2.11}$$

The preceding jitter metrics are RMS metrics. Peak-to-peak jitter could be converted from RMS jitter [12].

2.6.2 Jitter types in PLLs

Jitter can be classified into two canonical forms in PLLs. One is called synchronous jitter when an output signal transition is a direct result of an input signal transition, and

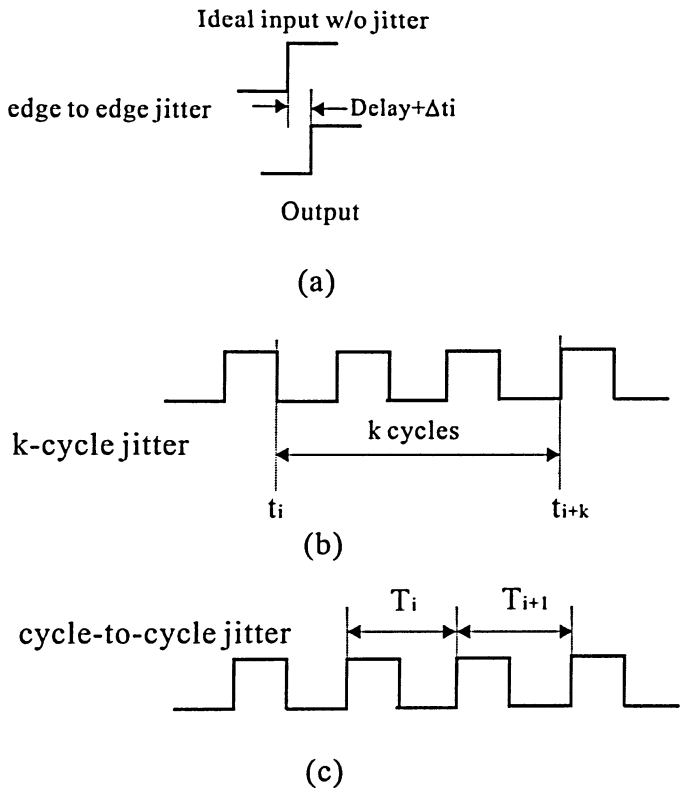

Figure 2.7: Jitter metrics.

the output transition will not go back to the input. It refers the delay variation between an input and an output through a block. Because of an interaction between noise present in the blocks and the thresholds that are inherent to logic circuits, the threshold crossing of an output signal is displaced slightly rather than precisely evenly spaced. This jitter appears as a modulation of the phase of the output signal, so it is also referred as phase modulated (PM) jitter. It is generated in phase detectors, charge pumps, and frequency dividers of PLLs and can be approximated by simple synchronous jitter J_{ee} if the flicker noise is neglected. The simple synchronous jitter is calculated from,

$$J_{ee} = \frac{\sqrt{var(n_v(t_c))}}{dv(t_c)/dt}, \tag{2.12}$$

where t_c is the threshold crossing time, $n_v(t)$ denotes the noise in the signal, $v(t)$ is the signal [12].

The other jitter form is called accumulating jitter. Accumulating jitter is exhibited in autonomous systems. It is the variation of the delay between an output transition and the subsequent output transition through feedback systems. In a PLL, an OSC and a VCO exhibit accumulating jitter, which is characterized by an undesired variation of the output transition fed back to the input to affect the next output transition. It appears as a modulation of the frequency of the output, so it is also called frequency modulation(FM) jitter. It can be approximated by simple accumulating jitter when flicker noise is neglected. The following equation is used in accumulating jitter calculation [12],

$$J_{cc} = \sqrt{2}\sqrt{var(j_{acc}(t_i + T) - j_{acc}(t_i))}. \tag{2.13}$$

The most obvious estimation or measurement of jitter is done by an eye diagram of the PLL output. In the locked state of a PLL, the output clock is folded by a certain period of time, which is closely related to the central frequency of the PLL. $\frac{3}{2}$ of the PLL period could be used as the folding time period to build the eye diagram. The bigger the eye opens, the lower the bit error rate (BER). The jitter seen in an eye diagram is long-term peak-to-peak jitter.

2.6.3 Jitter and phase noise predicting

Jitter and phase noise could also be predicted by modeling the PLL building blocks by Verilog-A[12]. The parameters to model the blocks are extracted from time-domain circuit simulation.

In a frequency divider, the output signal is sampled periodically at the threshold crossing time points to get a discrete-time random sequence. SpectreRF is used to compute the power-spectral density of the sequence, denoted by S_{n_v}. By integral of S_{n_v}, the total noise at the sample points, $var(n_v(t_c))$, is calculated. Further the J_{ee} is computed by Equation 2.12.

In a phase/frequency detector and a charge pump treated as one block, the noise of them is referred back to the input. To extract the input-referred jitter, the PFD/CP is driven by periodic signals with phase offsets to produce outputs. SpectreRF's PNoise analysis is used to compute the output noise over the total bandwidth of the phase/frequency detector and the charge pump. Then $J_{eePFD/CP}$ is computed by this equation,

$$J_{eePFD/CP} = \frac{T}{K_{det}}\sqrt{\frac{var(n)}{2}}. \tag{2.14}$$

where $var(n)$ is the integral of the noise power from 0 to infinity, K_{det} is the gain factor of PFD/CP, and T is a period of time used to scale K_{det} so that K_{det} has the units of amperes per second. To compute accumulating jitter in a VCO and an oscillator, the following equations are used,

$$J = \sqrt{cT}, \tag{2.15}$$

$$T = \frac{1}{f_o}, \tag{2.16}$$

$$c = L(\Delta f)\frac{\Delta f^2}{f_o^2}, \tag{2.17}$$

$$L(\Delta f) = log_{10}^{-1}\frac{S}{10}, \tag{2.18}$$

here S is computed by SpectreRF, Δf is the offset frequency for S, and f_o is the center frequency of the VCO or OSC.

In these PLL designs, there is no frequency divider and input oscillator, so only the phase/frequency detector and charge pump, and the VCO need to be modeled in Verilog-A. The Verilog-A modules listed in Appendix A are used to predict the phase noise of the PLLs in this thesis[12].

2.7 Serial Links and Coding

In serial data links, typical issues encountered include coding, framing, error detection, and signaling. Coding deals with the data representation. Framing focuses on the package pattern of data. Usually data frame has a certain number of bits or a certain bit range. Preamble code, frame head, address, control bits, load, cyclic redundancy check(CRC) and frame end are common segments in a data frame. Error detection monitors the quality and reliability of a data link. Signaling deals with the physical layer links. In high-speed serial links, the density of data transition edges is ensured by coding. Certain density of transition edges is required for enough clock information in order to recover the clock at the receiver end. Coding schemes critically affect the performance of serial links. In digital-to-digital coding, the following issues should be considered: signal spectrum, signal synchronization capability, signal error detecting capability, signal interference and noise immunity, cost and complexity. Among them, signal spectrum and signal synchronization capability mostly affect the design of CDR systems.

2.7.1 NRZ

None-return-to-zero coding is to use simple high/low voltage to present bits. The big problem of it is the DC component $V_{dc-avg} = \frac{V_{dd}}{2}$. It is difficult to recover the clock and data at the receiver end if successive 0's or 1's are encountered. The data bandwidth of NRZ is from zero up to half of its data rate.

2.7.2 NRZI

None-return-to-zero inverted coding generates square waves when data is '1', and keeps flat when data is '0'. With NRZI a '1' bit is represented by 0 volt or +V volt depending on the previous level. If the previous voltage is 0 volt then the '1' bit will be represented by +V volt, however if the previous voltage is +V volts then the '1' bit will be represented by 0 volts. A '0' bit is represented by whatever voltage level is used previously. This means that only a '1' bit can 'invert' the voltage. A '0' bit has no effect on the voltage, and it remains the same as the previous bit whatever that voltage was. This coding scheme reduces transitions of 0's. It is, however, lack of transition edges for clock recovery when successive 0's occur.

2.7.3 RZ

In return-to-zero coding, a '0' bit is represented by 0 volt whereas a '1' bit is represented by +V volt for half the cycle and 0 volt for the second half of the cycle. The average DC voltage is reduced to $V_{dc-avg} = \frac{V_{dd}}{4}$ plus there is an added benefit of signal transitions even if there are a series of 1's. Unfortunately, the efficiency of bandwidth usage increases when there are successive 1's and the clock recovery is difficult when there are successive 0's.

2.7.4 Manchester coding

Manchester coding, so called manchester phase encoding(MPE), uses rising edges to present 1's, falling edges to present 0's. Each bit takes the whole cycle of the clock. For '1', in the first half cycle, it is '-V' voltage and in the second half cycle, it is '+V' voltage. However for '0', in the first half cycle, it is '+V' voltage and in the second half cycle, it is '-V' voltage. When all 1's or 0's data come, the bandwidth is same as that of the system clock. Compared to NRZ and NRZI coding schemes, it doubles the bandwidth requirement, while no DC component exists in the coded signal. It also requires -V and +V voltages. The advantage is that transition edges are all ways there for clock recovery, no matter what data pattern is being sent. 802.3 Ethernet uses manchester encoding.

2.7.5 Differential manchester encoding (DME)

A '1' bit is indicated by setting the first half of the signal equal to the last half of the previous bit's signal. No transition at the start of the bit-time for a '1' bit. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal, i.e. '0' bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time, there is always a transition that ensures clock synchronization, whether from high to low, or low to high. Token ring uses DME without any preamble bits. DME is similar to MPE. They are depicted in Fig.2.8.

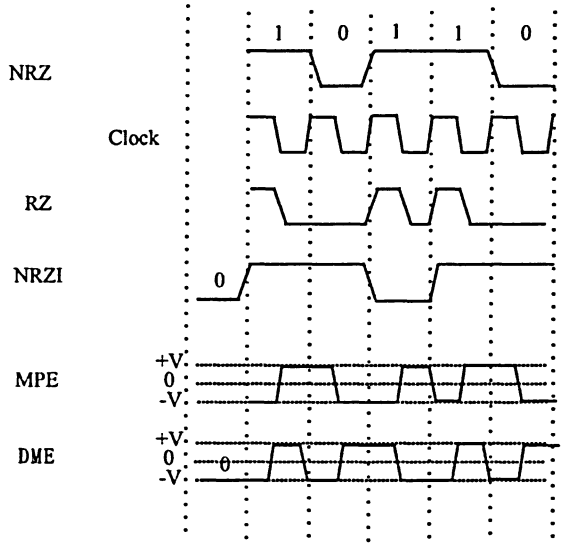

Figure 2.8: NRZ, RZ, NRZI, MPE and DME coding for 10110.

2.7.6 4B/5B coding

4B/5B encoding is sometimes called 'block coding'. Each 4-bit 'nibble' of received data has an extra 5th bit added. If input data are 4-bit nibbles, there are $2^4 = 16$ different bit patterns. With 5-bit 'packets', there are $2^5 = 32$ different bit patterns. As a result, the 5-bit patterns can always have at least two 1's and one 0 in one 'packet' even if the data is all 0's before coding. This enables clock synchronizations required for clock recovery with the cost of 1.25 times the original data rate. Table.2.1 shows the 4B/5B coding map.

Table 2.1: 4B/5B coding map.

4B	5B
0000	11110
0001	01001
0010	10100
0011	10101
0100	01010
0101	01011
0110	01110
0111	01111
1000	10010
1001	10011
1010	10110
1011	10111
1100	11010
1101	11011
1110	11100
1111	11101

2.7.7 8B/10B coding

Each octet of data is examined and assigned a 10-bit code. The data octet is split up into three most significant bits and five least significant bits. Both the two groups are mapped with its own coding mapping table. The 10-bit code groups must either contain five 1's and five 0's, or four 1's and six 0's, or six 1's and four 0's. This ensures that not too many consecutive 1's and 0's occur between code groups thereby maintaining clock synchronization. In order to maintain a DC balance, the running disparity calculation is used to keep the number of 0's transmitted the same as the number of 1's transmitted. It uses 10 bits to present each 8 bits of data, therefore drops the maximum data rate in a certain channel by $\frac{1}{5}$, the same as in 4B/5B coding.

2.7.8 PAM-5 coding

It employs multi-level amplitude signaling. To encode 8 bits, $2^8 = 256$ codes or symbols are required since there are 256 possible combinations. A five level signal (e.g. -2v, -1v, 0v,

1v and 2v) called pulse amplitude modulation 5 is used on four separate pairs. This gives us a possibility of $5^4 = 625$ codes to choose from when we use all four pairs. Actually only four levels are used for data, the fifth level (0V) is used for the 4-dimension 8-state trellis forward error correction used to recover the transmitted signal in a high noise background.

What affect CDR the most are the all 0's and all 1's. That affects CDR clock recovery capability and performance. In this design, It is assumed that the input data has been 4B/5B or 8B/10B coded without worrying about the all 1's and all 0's issues.

2.7.9 Signaling in Serial Links

Multi-level signaling is to transmit multiple bits in each transmit time. It decreases the requirement of channel bandwidth for a given bit rate. M-pulse amplitude modulation(PAM) is a multi-level signaling scheme. Fig.2.9 shows the 2-PAM and 4-PAM signalling schemes. In this thesis, 2-PAM is used.

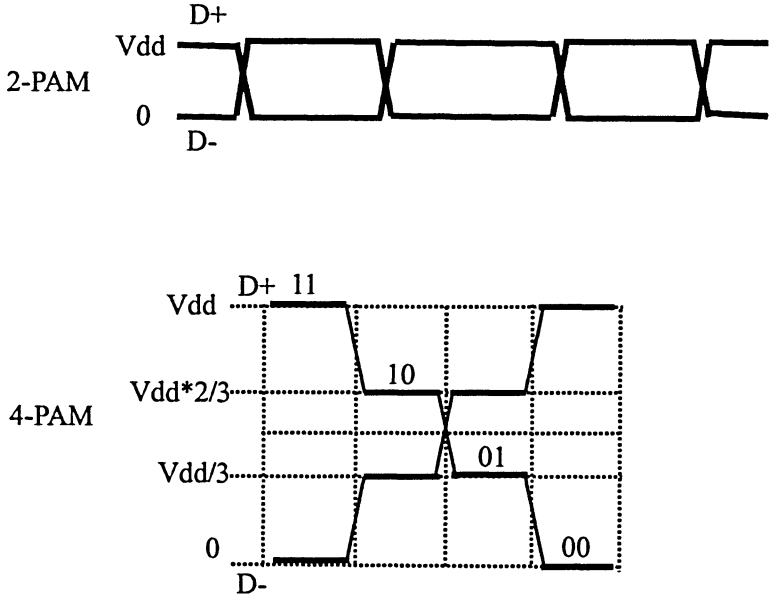

Figure 2.9: Data waveform of 2-PAM and 4-PAM signaling schemes.

Chapter 3

Bang-Bang Phase Detectors

There are a number of design specifications quantifying the performance of PLLs, among them, lock time that quantifies how fast a PLL can move to the lock state when the phase of the incoming data or that of the output of the PLL varies, and timing jitter that depicts the random characteristics of the phase of the output of the PLL in the lock state are the two most important figure-of-merits quantifying the behavior of the PLL in both the transient and lock states. Although affected by the loop dynamics of a PLL, in particular, the gain of the charge pump and the bandwidth of the loop filter, the lock time and timing jitter of a PLL are also largely affected by the characteristics of its phase detector. This is because the effectiveness of the feedback action of a PLL is ultimately determined by how fast and how accurate its phase detector can sense the phase difference between the incoming data and the output of the PLL.

Phase detectors can be briefly classified into two categories: linear phase detectors who's output is pulse-width modulated by the phase difference in a linear fashion, and non-linear phase detectors who's output is pulse-polarity modulated by the phase lead or phase lag.

3.1 Linear Phase Detectors

The widely used XOR phase detectors shown in Fig.3.1, RS phase detectors shown in Fig.3.2 , D-flip flop phase/frequency detectors shown in Fig.3.3, and two-XOR phase/frequency detectors shown in Fig.3.4 fall into the category of linear phase detectors. XOR phase de-

tectors suffer from the drawback that the output voltage varies with the duty cycle of the inputs. In the phase detector figures, V_m denotes the voltage change in one clock cycle on the VCO control line when a phase detector is given the maximum phase deference in its phase detection range.

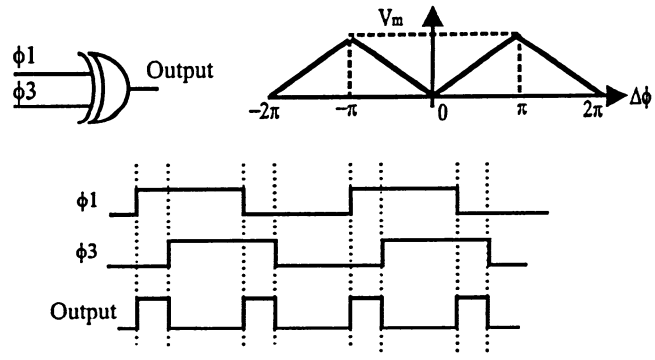

Figure 3.1: XOR phase detector[3].

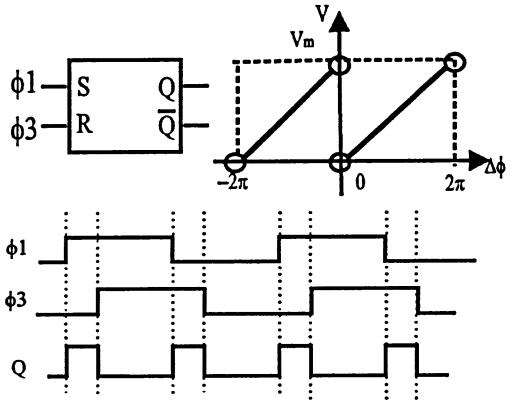

Figure 3.2: RS phase detector[3].

RS phase detectors remove this limitation by making use of the characteristics of RS-latches. The application of RS phase detectors, however, is affected by their ability to falsely lock to the harmonic of the input frequency and the jitter due to the meta-stability in the lock state.

D-flip flop phase detectors employ two positive edge-triggered D-flip flops to detect both phase and frequency differences such that a large acquisition range and a fast locking process can be achieved [18]. Two main drawbacks of these phase detectors include a phase dead

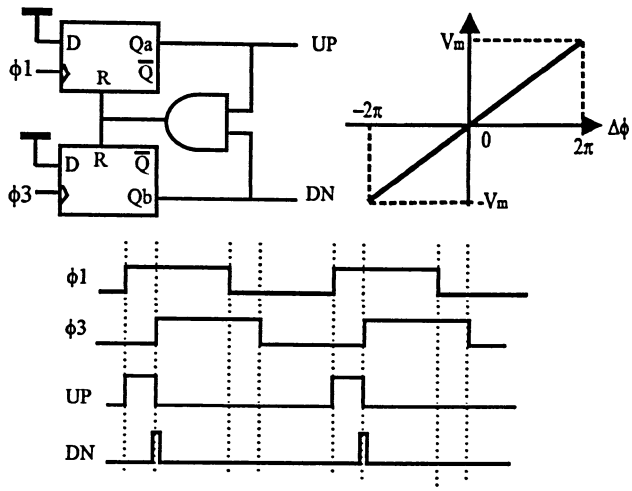

Figure 3.3: DFF phase/frequency detector.

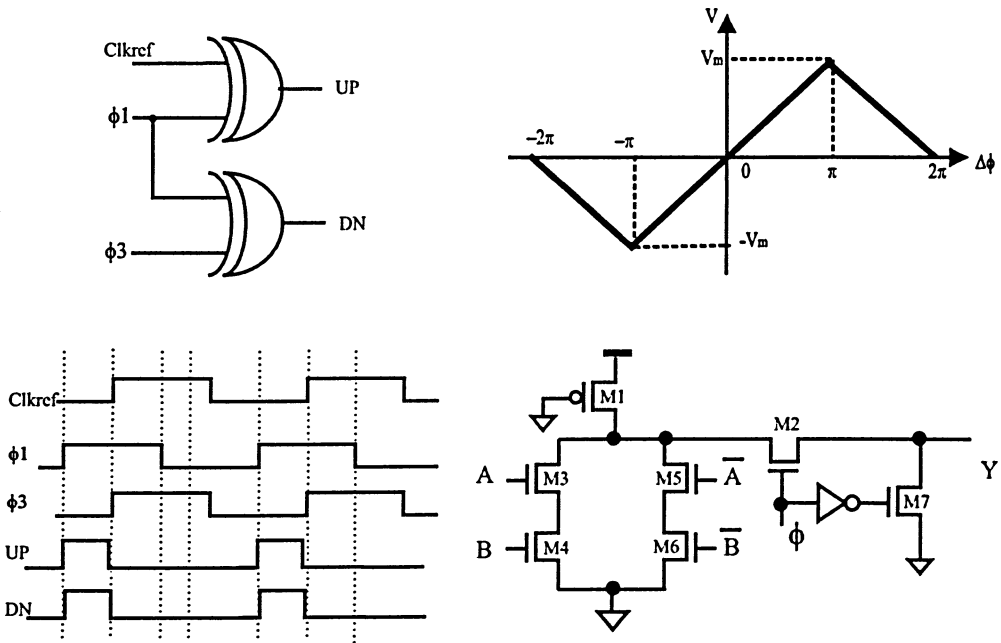

Figure 3.4: 2XOR phase/frequency detector and the schematics of XOR-2 gate[4].

zone due to the delay of the logic gates and the feedback reset operation, and a metastable stage occurring when the input phase difference becomes comparable to the delay of logic gates.

Two-XOR phase detectors require an oscillator with eight differential clock signals spaced by $\frac{\pi}{4}$ in order to function properly [4]. Because both current sources of the charge pump are ON all the time and only their non-overlapping part quantifies the duration over which the charge pump is activated, the dead zone encountered in D-flip flop phase detectors are eliminated. This, however, is at the cost of a high level of static power consumption.

3.2 Non-Linear Phase Detectors

Bang-bang phase detectors shown in Fig.3.6 and improved bang-bang phase detectors shown in Fig.3.7 are binary phase detectors. A bang-bang phase detector samples the incoming data twice per data eye with a phase quantization error of $\frac{\pi}{2}$. The phase detection range is given by $-\frac{\pi}{2} < \Delta\phi < \frac{\pi}{2}$ with a discontinuity at $\Delta\phi = 0$. Because the output voltage is only sensitive to the polarity rather than the actual value of the phase difference of the inputs, a high level of timing jitter exists in the lock state. The jitter can be lowered effectively by introducing an additional set of control signals with reduced amplitude. This phase detector is known as the improved bang-bang phase detector [5, 6]. The input data are sampled five times per data eye, lowering the phase quantization error to $\frac{\pi}{4}$. The phase detector generates two coarse control signals when $\frac{\pi}{4} < |\Delta\phi| < \frac{\pi}{2}$, and two fine control signals when $0 < |\Delta\phi| < \frac{\pi}{4}$. The amplitude of the current sources controlled by the coarse control signals is larger than that controlled by the fine control signals such that a fast locking process and lower timing jitter in the lock state can be achieved. Typically, the D-flip flop could be implemented by TSPC DFF circuit, shown in Fig.3.5 [13].

An other bang-bang phase detector used extensively is Alexander's phase detector shown in Fig.3.8 [10, 3]. The operation of Alexander's phase detector is illustrated in Table.3.1.

The different characteristics of the linear and non-linear phase detectors give rise to the distinct behavior of PLLs in both the transient and lock states. PLLs with a linear phase

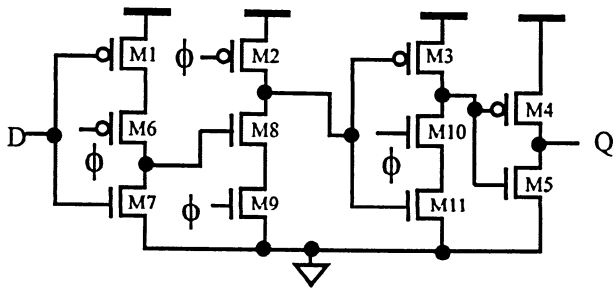

Figure 3.5: TSPC D-flip flop[13].

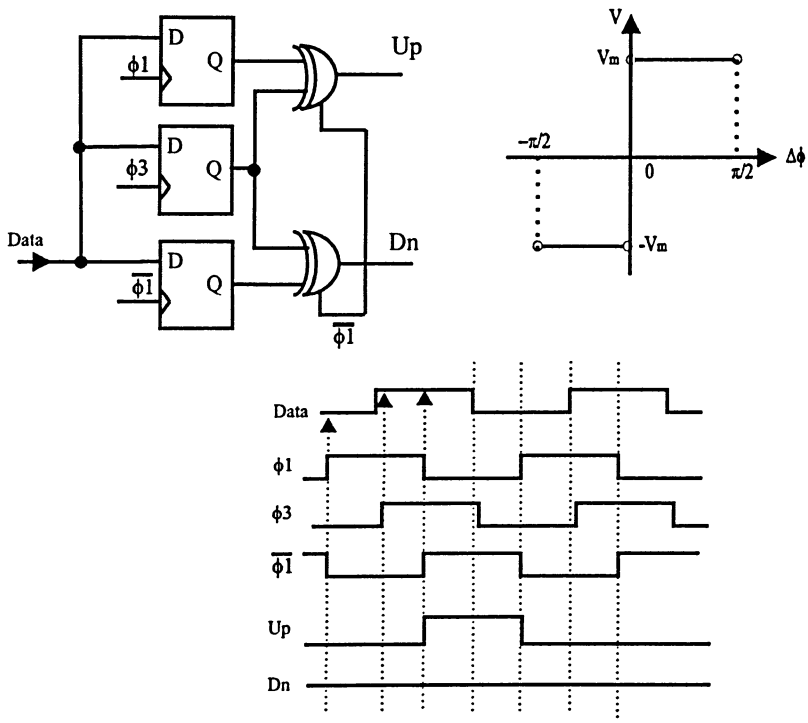

Figure 3.6: Bang-bang phase detector[5].

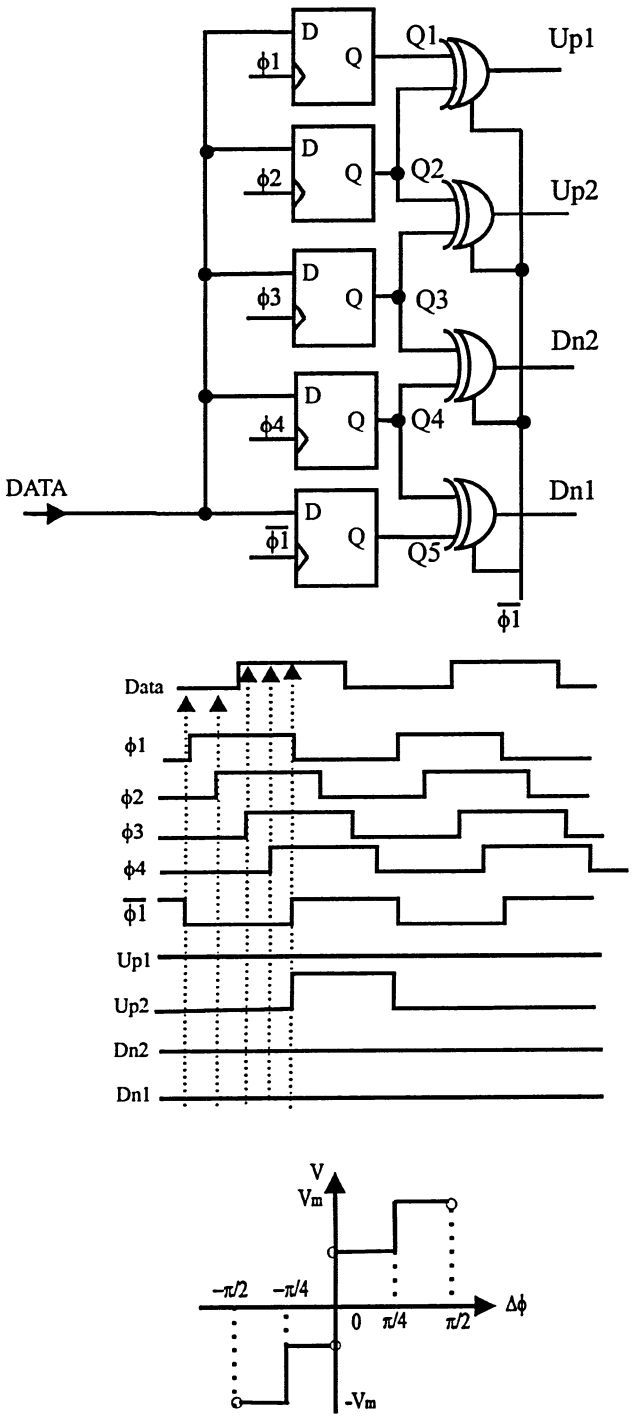

Figure 3.7: Improved bang-bang phase detector[5].

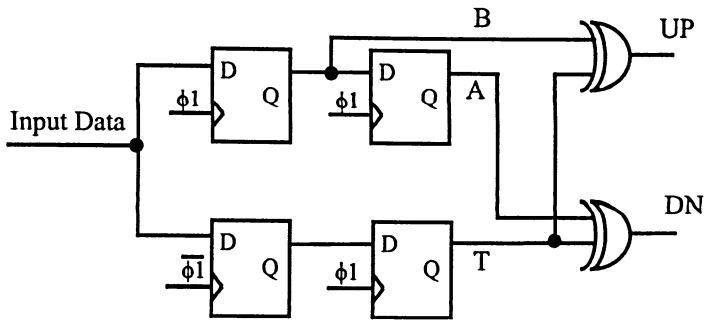

Figure 3.8: Alexander's bang-bang phase detector[3].

Table 3.1: The truth table of Alexander's bang-bang phase detector[3].

State	A	T	B	UP	DN	Meaning
0	0	0	0	0	0	hold
1	0	0	1	0	1	early
2	0	1	0	1	1	hold(not exist)
3	0	1	1	1	0	late
4	1	0	0	1	0	late
5	1	0	1	1	1	hold(not exist)
6	1	1	0	0	1	early
7	1	1	1	0	0	hold

detector have the advantage of low timing jitter in the lock state but suffer from a long locking process whereas PLLs with a binary phase detector enjoy a fast locking process, however, at the cost of large timing jitter in the lock state.

Chapter 4

PLL Architectures and Building Blocks

Two PLL architectures have been proposed in this thesis. One is depicted in Fig.4.1. It is a single loop architecture. The other is shown in Fig.4.2 and is a dual loop architecture. Separating of the phase correction loop and the frequency correction loop makes the PLL possess fast locking property and less difficulty to lock because this dual-loop technique decouples the lock range from jitter tolerance and jitter generation, and gives more design freedom.

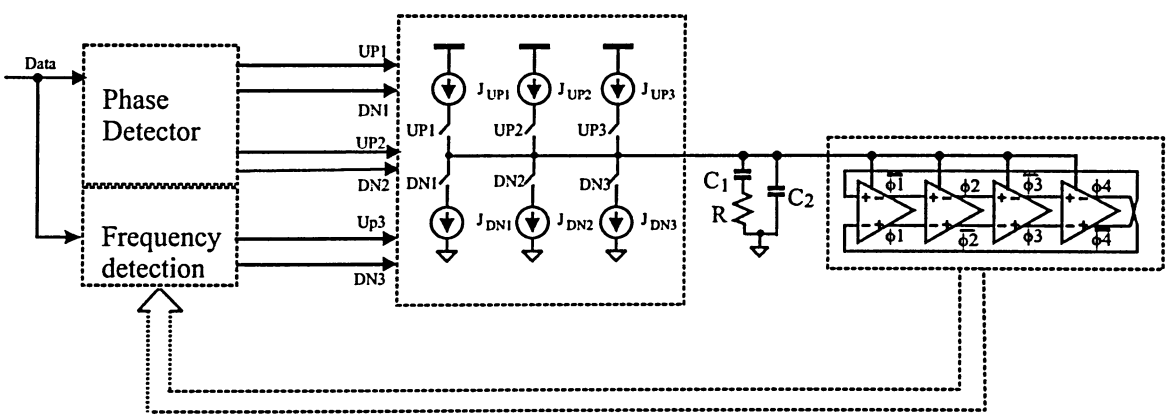

Figure 4.1: Single-loop PLL architecture.

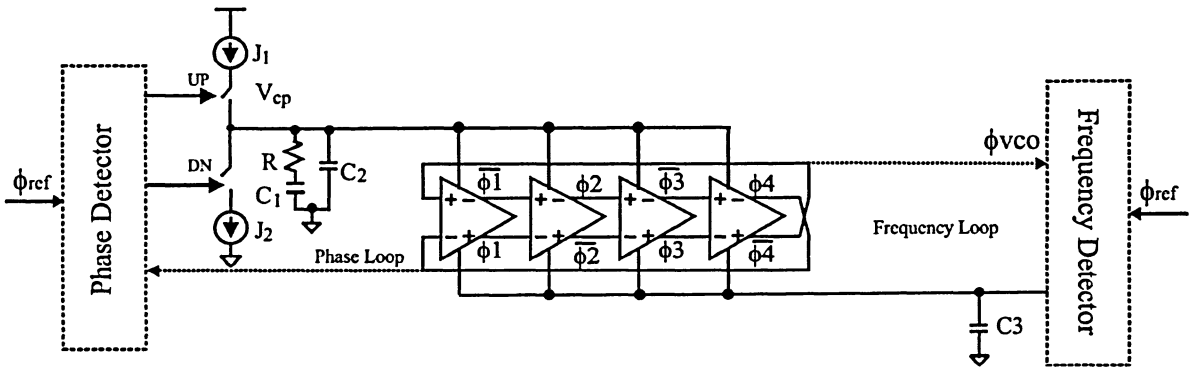

Figure 4.2: Dual-loop PLL architecture.

4.1 Frequency Detectors

Due to the phase-detection property of the bang-bang phase detector, PLL frequency has to be detected and held to that of the reference clock by a frequency detector. A frequency detection block that adjusts the frequency of the VCO prior to a phase comparison is needed to ensure the proper operation of the bang-bang phase detection block. Two frequency detectors are implemented in this design. They are depicted in Subsection.4.1.1 and Subsection.4.1.2 respectively.

4.1.1 DFF frequency detector

The schematic of the frequency detection block is shown in Fig.4.3. Three D-flip flops are used for frequency detection. DFF3 is a $\frac{1}{2}$ frequency divider. DFF1 latches the first rising edge of ϕ_1 in one cycle of ϕ_2. DFF2 latches the next rising edge of ϕ_1 in the same cycle of ϕ_2 as long as the RESET signal of DFF1 is kept at Logic-0. If the output is Logic-1, it is determined that ϕ_1 is faster than ϕ_2 because two rising edges have appeared in one cycle of ϕ_2. Another set frequency detection circuit is required to detect if ϕ_2 is faster than ϕ_1.

4.1.2 Charge-pump frequency detector

As mentioned earlier that a frequency detector is required to ensure the lock of PLLs with a binary phase detector. A charge-pump frequency detector is also proposed and used

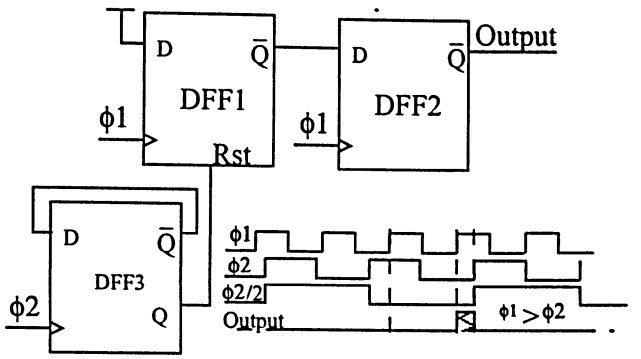

Figure 4.3: A DFF frequency detector.

together with the proposed bang-bang phase detector to ensure a fast lock. In this design, the reference clock and one of the VCO outputs are used to drive a charge pump in the second loop whose output is used to control the frequency of the VCO. Note that the frequency difference between the reference clock and the VCO output is proportional to the pulse width difference between them, as illustrated graphically in Fig.4.4. The operation of the frequency detector is briefly depicted below :

(i) When $T_r = T_v$, $V_{cf,avg}$ remains unchanged.

(ii) When $T_r > T_v$, $V_{cf,avg}$ increases.

(iii) When $T_r < T_v$, $V_{cf,avg}$ decreases.

This charge-pump frequency detector performs much faster than the DFF frequency detector does.

4.2 Charge Pumps

Charge pumps are controlled by phase/frequency detectors, dispense charges into the loop filter. The current flow time or current value is proportional to the input voltage. Typically a charge pump consists of two current switches, denoted UP and DN and a pair of current sources. Current mismatch, charge injection, clock feed-through and charge sharing need to be considered in the design of charge pumps [16, 19].

The charge pump shown in Fig.4.5 is the improved current-steering charge pump proposed

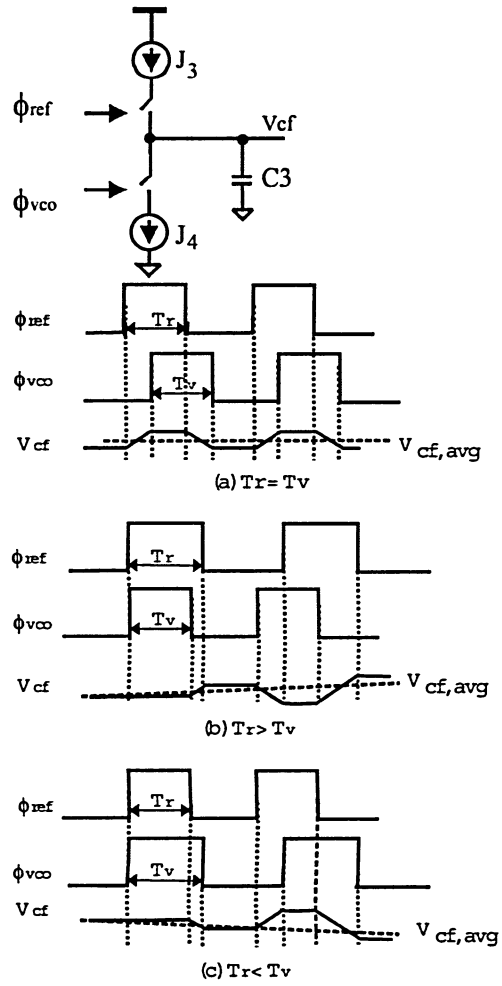

Figure 4.4: Operation of charge-pump frequency detector.

in [11].

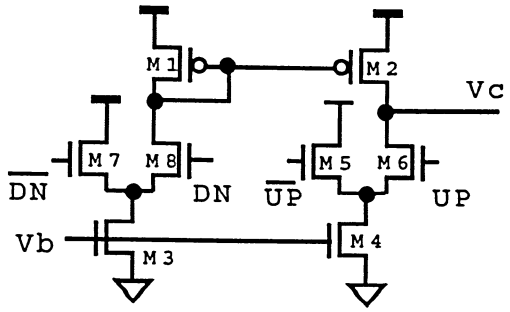

Figure 4.5: Schematic of the charge pump.

4.3 Loop Filters

A loop filter can be either a passive filter or an active filter. A passive loop filter is shown in Fig.4.6. Shown in Fig.4.7 is an example of active loop filters. Charge pumps often work with passive loop filters[19]. A passive loop filter is employed in this design. In the dual loop design, a single capacitor seen in Fig.4.2 is employed as a loop filter in the frequency-correction loop.

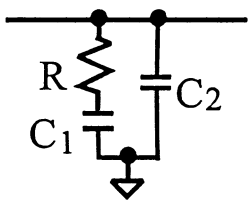

Figure 4.6: Passive loop filter.

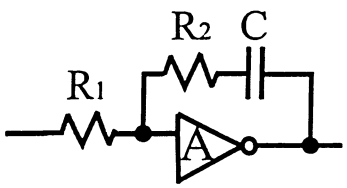

Figure 4.7: Active loop filter.

4.4 VCOs and Delay Cells

A fully differential ring VCO in Fig.4.8 is employed in this design. It has a large frequency tuning range and multiphase outputs. Also it has been chosen by its low power consumption, full swing and low area advantages. Two delay cells for the VCOs are designed to build the single and dual loop architectures shown in Fig.4.1 and Fig.4.2 respectively.

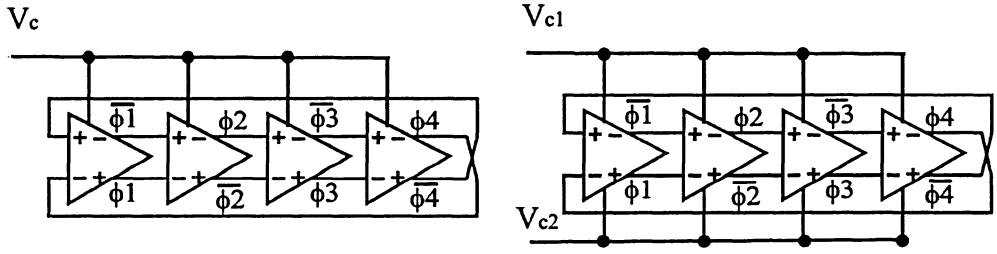

Figure 4.8: Fully differential VCOs, Left: Single voltage-controlled VCO, Right: Dual voltage-controlled VCO.

4.4.1 Single voltage-controlled delay cells

The delay cell of the VCO in the single loop structure is the fully differential cross-coupled cell proposed in [8, 9]. In this structure, the biasing tail current source is not required, so the up-conversion of the flicker noise from the tail current source is eliminated. The cross-coupled VCO delay cell operates in a full swing mode. The nMOS-latch with smaller width is chosen to speed up the transition of the output signals since the larger the transition slope, the smaller the output jitter. Its schematics implementation is shown in Fig.4.9 with one control voltage input.

4.4.2 Dual voltage-controlled delay cells

In the dual-loop PLL architecture, the cross-coupled delay cell is modified to have two control voltage inputs shown in Fig.4.10. Two control voltage inputs, one for the phase correction loop and the other for the frequency correction loop, control the pull-up pMOS transistors, as shown in Fig.4.10. It possesses all the features of the single voltage-controlled delay cell shown in Fig.4.9.

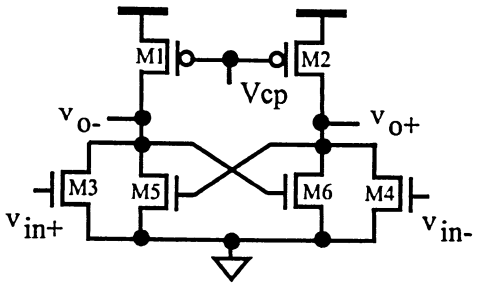

Figure 4.9: Delay cell of VCO in single-loop PLL.

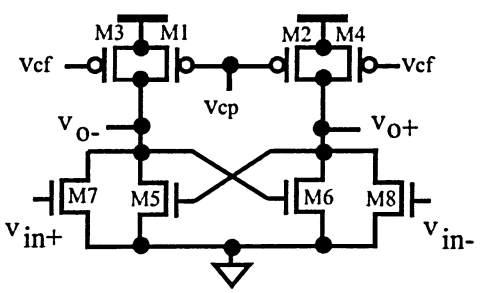

Figure 4.10: Delay cell of VCO in dual-loop PLL.

Chapter 5

Hybrid Phase Detector

PLLs with a phase detector that possesses the characteristics of linear phase detectors when the phase difference is small and that of binary phase detectors when the phase difference is large offer both fast locking and low timing jitter in the lock state. Such a phase detector in this thesis is termed as the hybrid phase detector. The fact that a 4-stage fully differential VCO is required for the operation of both the two-XOR and improved bang-bang phase detectors suggests that a possible implementation of such a phase detector could come from the combination of a two-XOR phase detector and an improved bang-bang phase detector. In this chapter, the implementation of the hybrid phase detector is detailed. The effectiveness of the proposed hybrid phase detector is assessed using three PLLs with identical loop filters, charge pumps, and VCOs but distinct phase detectors.

5.1 Hybrid Phase Detector

A hybrid phase detector consists of a two-XOR phase detection block, a bang-bang phase detection block, and a control logic block. A frequency detection block that adjusts the frequency of the VCO prior to the phase comparison is needed to ensure the proper operation of the bang-bang phase detection block. The schematics of the frequency detection block is shown in Fig.4.3 and Fig.4.4. The improved bang-bang phase detector is reduced since the third sampler in Fig.3.7 is unused. DFF here is implemented by TSPC DFF shown in Fig.3.5, and the transistors are sized by Table.5.1. The XOR gate in Fig.3.4 is sized by

Table 5.1: Transistor size of TSPC DFF for the hybrid phase detector(L=0.13μm).

Transistor	Width(μm)
M1	4
M2	4
M3	4
M4	4
M5	2
M6	4
M7	2
M8	2
M9	2
M10	2
M11	2

Table 5.2: Transistor size of XOR gate transistor for the hybrid phase detector(L=0.13μm).

Transistor	Width(μm)
M1	2
M2	8
M3	3.5
M4	3.5
M5	3.5
M6	3.5
M7	1

Table.5.2. VCO delay cells in Fig.4.9 are sized by Table.5.3.

Once the frequency of the incoming signal and the output of the VCO are identical, the frequency detection block is disabled. The phase difference, defined as the phase difference between the rising/falling edges of the waveforms of the incoming data and the rising edge of ϕ_3 of the VCO, is sensed by both the two-XOR and bang-bang phase detection blocks simultaneously. The following conventions are adopted,

$$\Delta\phi \begin{cases} > 0, & \text{if the rising/falling edges of the incoming data lead the rising edge of } \phi_3, \\ < 0, & \text{otherwise.} \end{cases}$$

The outputs of the bang-bang phase detection block are selected when the phase difference $\Delta\phi$ satisfies $|\Delta\phi| > \frac{\pi}{4}$. Otherwise, the outputs of the two-XOR phase detection block are selected.

Table 5.3: Transistor size of VCO delay cell for the hybrid phase detector PLL(L=0.13μm).

Transistor	Width(μm)
M1	13
M2	13
M3	2
M4	2
M5	1
M6	1

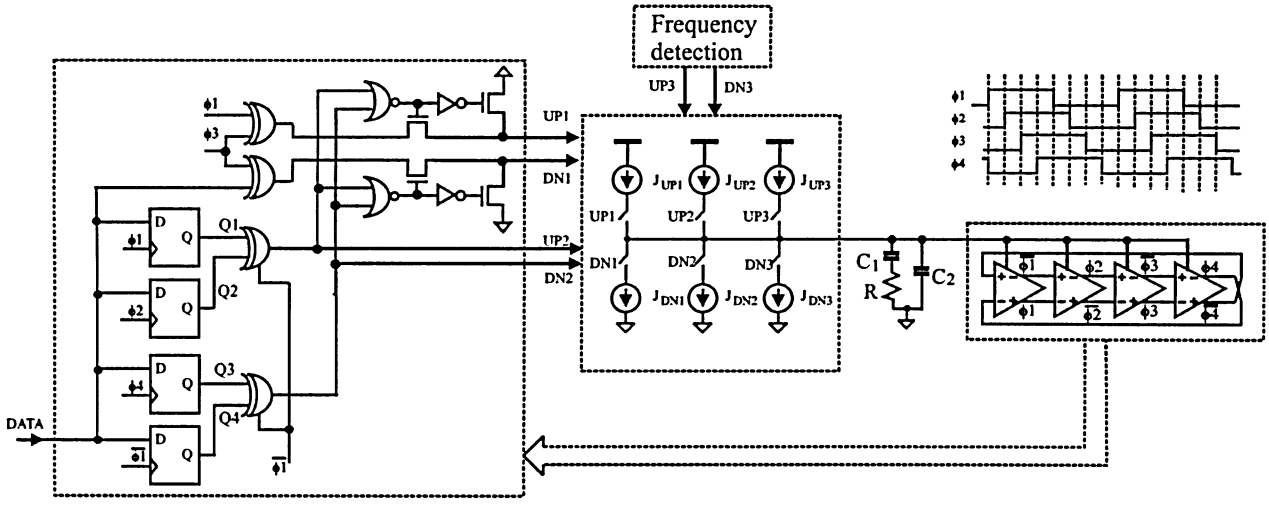

Figure 5.1: PLL with a hybrid phase detector.

Four pairs of clock signals $\phi_1, \overline{\phi}_1 \sim \phi_4, \overline{\phi}_4$, phase-spaced by $\frac{\pi}{4}$, are obtained from a four-stage differential ring VCO. The bang-bang phase detection block generates two control signals UP_2 and DN_2 when the phase difference falls into the range $\frac{\pi}{4} < |\Delta\phi| < \frac{\pi}{2}$ in accordance with,

$$\mathrm{UP}_2 = Q_1 \oplus Q_2,$$
$$\mathrm{DN}_2 = Q_3 \oplus Q_4.$$

To illustrate how the bang-bang phase detection block works, consider the rising edge of the incoming data shown in Fig.5.2(a). Two cases exist,

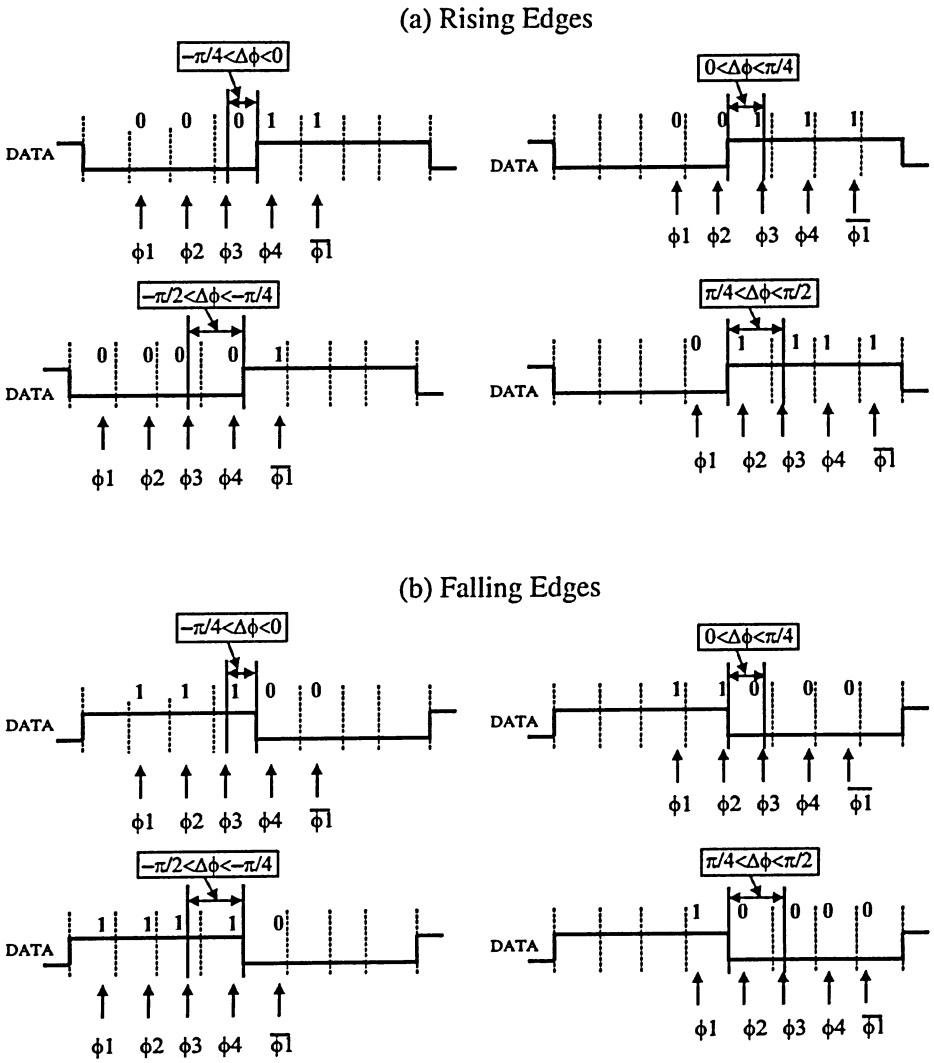

Figure 5.2: Operation of the bang-bang phase detection block.

- $|\Delta\phi| < \frac{\pi}{4}$: There are two scenarios in this case : (i) $0 < \Delta\phi < \frac{\pi}{4}$ and (ii) $-\frac{\pi}{4} < \Delta\phi < 0$. In the first case where $0 < \Delta\phi < \frac{\pi}{4}$, $Q_1 = Q_2 = 1$ and $Q_3 = Q_4 = 0$, we have $\mathrm{UP}_2 = 0$ and $\mathrm{DN}_2 = 0$. In the second case where $-\frac{\pi}{4} < \Delta\phi < 0$, $Q_1 = Q_2 = 0$ and $Q_3 = Q_4 = 1$, we have $\mathrm{UP}_2 = 0$ and $\mathrm{DN}_2 = 0$.

- $|\Delta\phi| > \frac{\pi}{2}$: Two scenarios exist : (i) $\frac{\pi}{4} < \Delta\phi < \frac{\pi}{2}$ and (ii) $-\frac{\pi}{2} < \Delta\phi < -\frac{\pi}{2}$. In the first case where $\frac{\pi}{4} < \Delta\phi < \frac{\pi}{2}$, $Q_1 = 0$, $Q_2 = 1$, $Q_3 = 1$, and $Q_4 = 1$. We have $\mathrm{UP}_2 = 1$ and $\mathrm{DN}_2 = 0$. In the second case where $-\frac{\pi}{2} < \Delta\phi < -\frac{\pi}{2}$, $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 0$, and $Q_4 = 1$, we have $\mathrm{UP}_2 = 0$ and $\mathrm{DN}_2 = 1$.

The preceding analysis shows that UP_2 or DN_2 are set to Logic-1 when $\frac{\pi}{4} < |\Delta\phi| < \frac{\pi}{2}$ and both UP_2 and DN_2 are set to Logic-0 when $|\Delta\phi| < \frac{\pi}{4}$. As a result, $\mathrm{UP}_2 \oplus \mathrm{DN}_2 = 1$ if $|\Delta\phi| > \frac{\pi}{4}$ and 0 otherwise. The same conclusion holds for the falling edge case as well, as shown in Fig.5.2(b). $\mathrm{UP}_2 \oplus \mathrm{DN}_2$ can be used to select the two-XOR and bang-bang phase detection blocks, as shown in Fig.5.1. When $\frac{\pi}{4} < |\Delta\phi| < \frac{\pi}{2}$, the nMOS transistors in series with the outputs of the two-XOR phase detection block turn off and the outputs of the bang-bang phase detection block are routed to the downstream charge pump. When $|\Delta\phi| < \frac{\pi}{4}$, the shunt transistors controlled by the outputs of the bang-bang phase detection block are off and the outputs of the two-XOR phase detection block are conveyed to the downstream charge pump.

The phase transfer characteristics of the proposed hybrid phase detector are shown in Fig.5.3, together with that of two-XOR and improved bang-bang phase detectors for the purpose of comparison. It is seen that the hybrid phase detector behaves as a two-XOR phase detector when $|\Delta\phi| < \frac{\pi}{4}$, and an improved bang-bang phase detector when $\frac{\pi}{4} < |\Delta\phi| < \frac{\pi}{2}$.

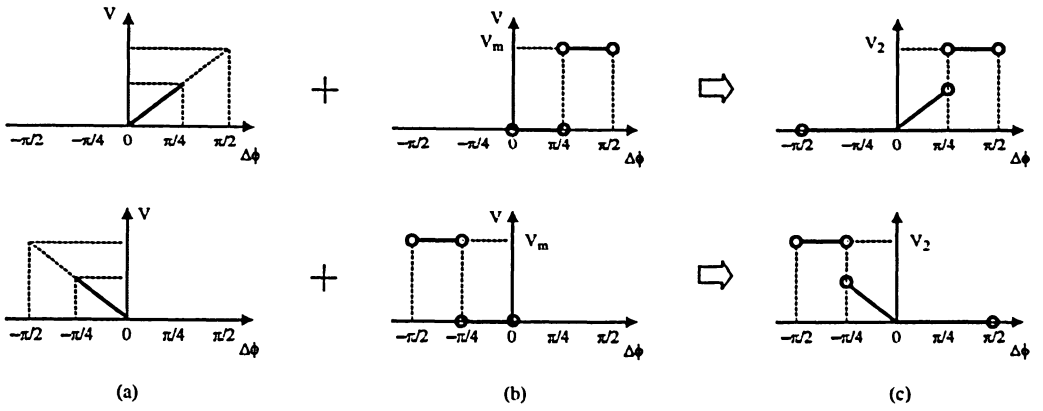

Figure 5.3: Transfer characteristics from the phase difference $\Delta\phi$ to the average output voltage of phase detectors. (a) Two-XOR phase detection block; (b) Bang-bang phase detection block; (c) Hybrid phase detector.

5.2 Simulation Results

To quantify the effectiveness of the proposed hybrid phase-frequency detector, three PLLs with identical loop filters, charge pumps, and VCOs but three distinct phase detectors, namely, a two-XOR phase detector shown in Fig.3.4, an improved bang-bang phase detector shown in Fig.3.7, and a hybrid phase detector shown in Fig.5.1, are implemented in UMC-0.13μm 1.2V CMOS technology and analyzed using Spectre from Cadence Design Systems with BSIM3v3 device models that account for both the parasitics and high-order effects of MOS devices. The frequency detector used in this design is shown in Fig.4.3. The schematics of XOR2 gates with reset, D-flip flops, the delay cells of the VCO, and the charge pump are shown in Fig.3.4, Fig.3.5, Fig.4.9 and Fig.4.5 respectively. The D-flip flops are realized by TSPC logic gates [7, 13]. The size of the transistors is tabulated in Table 5.1, Table 5.2, Table 5.3, and Table 5.4. In the loop filter, R is 1.1kΩ, C1 is 11.2pF, and C2 is 3.3pF.

The control voltage of the VCO of the PLLs with a two-XOR phase detector, an improved bang-bang phase detector with a frequency detector, and a hybrid phase detector is plotted in Fig.5.4, Fig.5.5, and Fig.5.6, respectively. It is observed that the PLL with the two-XOR phase detector has the longest locking transient while that with the improved bang-bang phase detector has the shortest locking process. The PLL with the improved bang-bang

Table 5.4: The charge pump transistor size(L=0.13μm).

Transistor	Width(μm)
M1	8
M2	8
M3	8
M4	8
M5	20
M6	20
M7	20
M8	20

phase detector also has the largest fluctuation in its control voltage, resulting in the worst timing jitter. These observations echo with our initial statements on the advantage and disadvantage of PLLs with the two-XOR and improved bang-bang phase detectors.

The PLL with the hybrid phase detector has approximately the same lock time as that of the PLL with an improved bang-bang phase detector. The amplitude of the fluctuation of the control voltage of the PLL with the hybrid phase detector is approximately same as that of the PLL with an improved bang-bang phase detector in the transient region and the same as that of the PLL with a two-XOR phase detector when a lock state is established. These observations confirm that PLLs with the hybrid phase detector possess the intrinsic advantage of the low timing jitter of PLLs with a two-XOR phase detector and yet enjoy the advantage of the short lock time of PLLs with an improved bang-bang phase detector.

The timing jitter of the output of the VCO in the PLLs with a two-XOR phase detector, an improved bang-bang phase detector with a frequency detector, and a hybrid phase detector is plotted in Fig.5.7, Fig.5.8, and Fig.5.9, respectively. It is observed that the PLL with the two-XOR phase detector has lower timing jitter as compared with that of the PLL with the improved bang-bang phase detector. The timing jitter of the PLL with the two-XOR phase detector is approximately the same as that of the PLL with the hybrid phase detector. These observations echo the earlier simulation results on the control voltage of these three PLLs. It should be noted that the timing jitter simulation results reported here only take into account the effect of the variation of the control voltage. The effect of switching noise

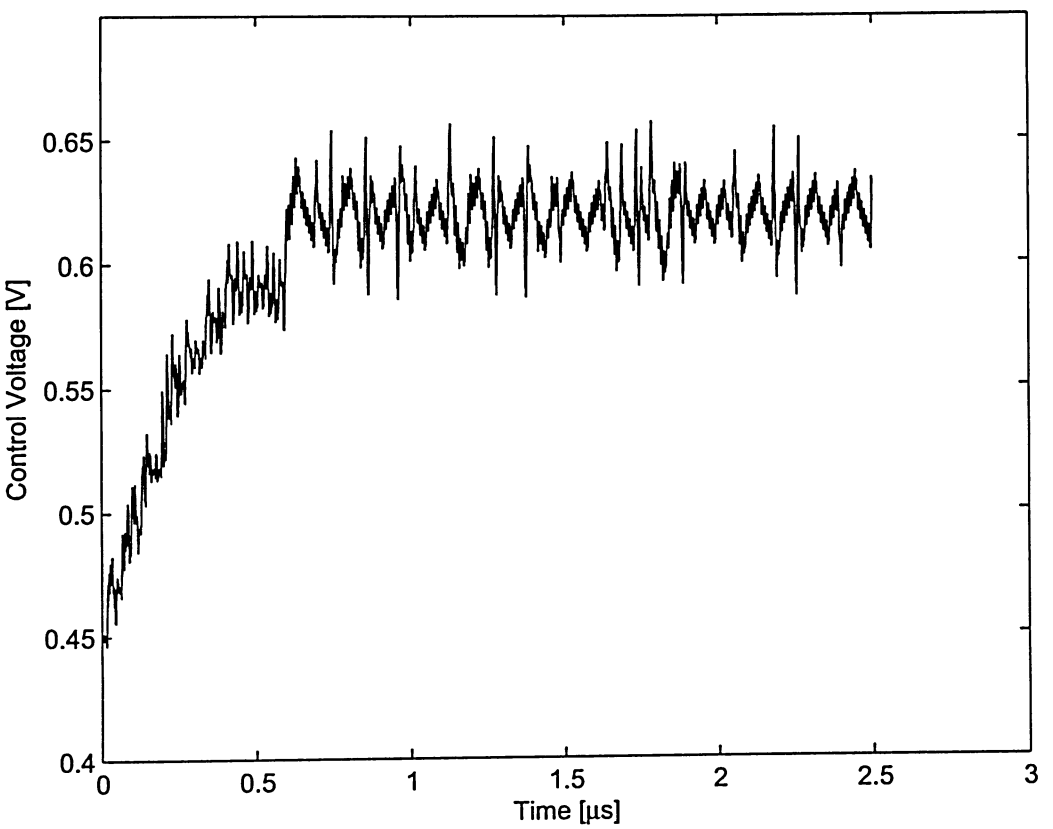

Figure 5.4: Simulated control voltage of the phase-locked loop with the improved bang-bang phase detector.

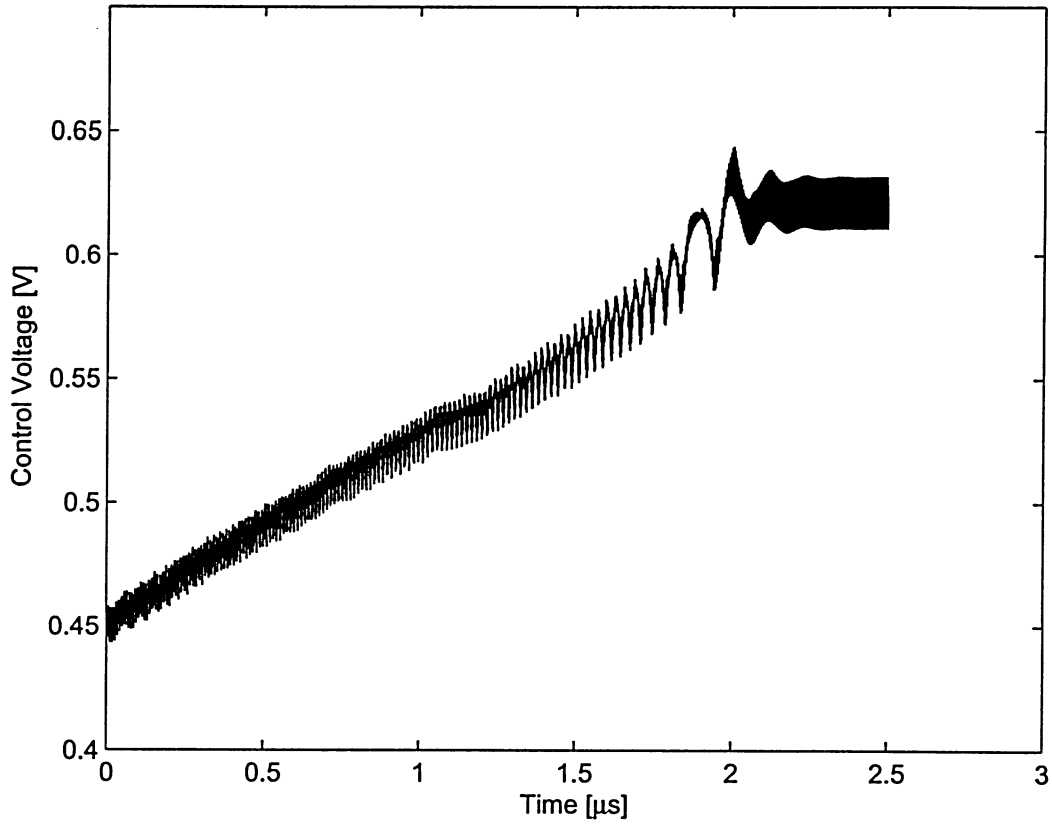

Figure 5.5: Simulated control voltage of the phase-locked loop with the two-XOR phase detector.

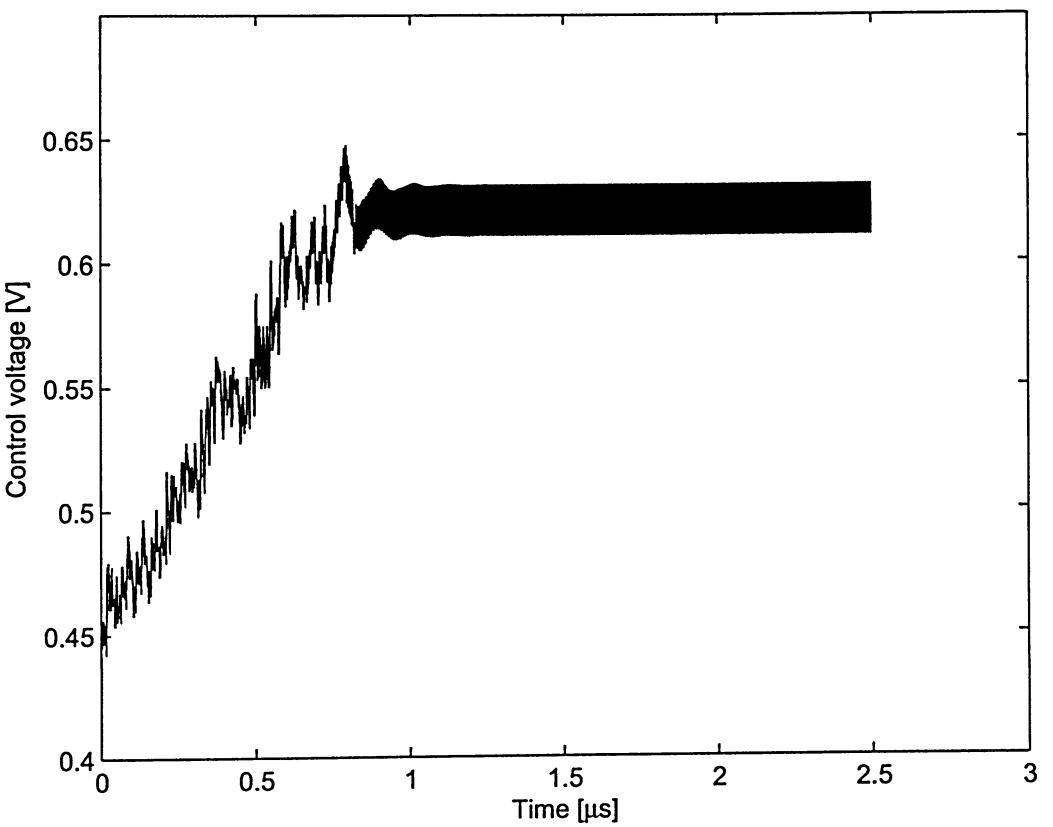

Figure 5.6: Simulated control voltage of the phase-locked loop with the proposed hybrid phase detector.

and device noise are not considered.

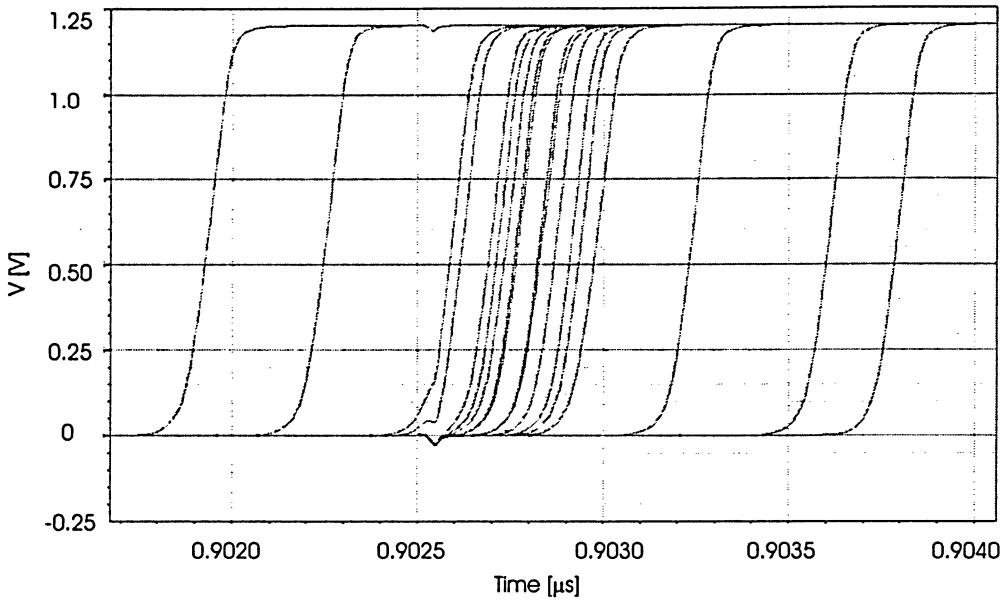

Figure 5.7: Simulated timing jitter of the phase-locked loop with the improved bang-bang phase detector.

5.3 Chapter Summary

A new hybrid phase detector that overcomes the drawback of linear and binary phase detectors has been proposed. PLLs with the proposed hybrid phase detector possess the low timing jitter of PLLs with the two-XOR phase detector in lock states and the fast locking process of PLLs with the improved bang-bang phase detector. Simulation results demonstrate that PLLs with the hybrid phase detector has approximately the same lock time as that of the PLL with the improved bang-bang phase detector. The amplitude of the fluctuation of the control voltage of the PLL with the hybrid phase detector is approximately same as that of the PLL with the improved bang-bang phase detector in the transient region and the same as that of the PLL with the two-XOR phase detector in the lock state. The timing jitter of the PLL with the hybrid phase detector is the same as that of the PLL with

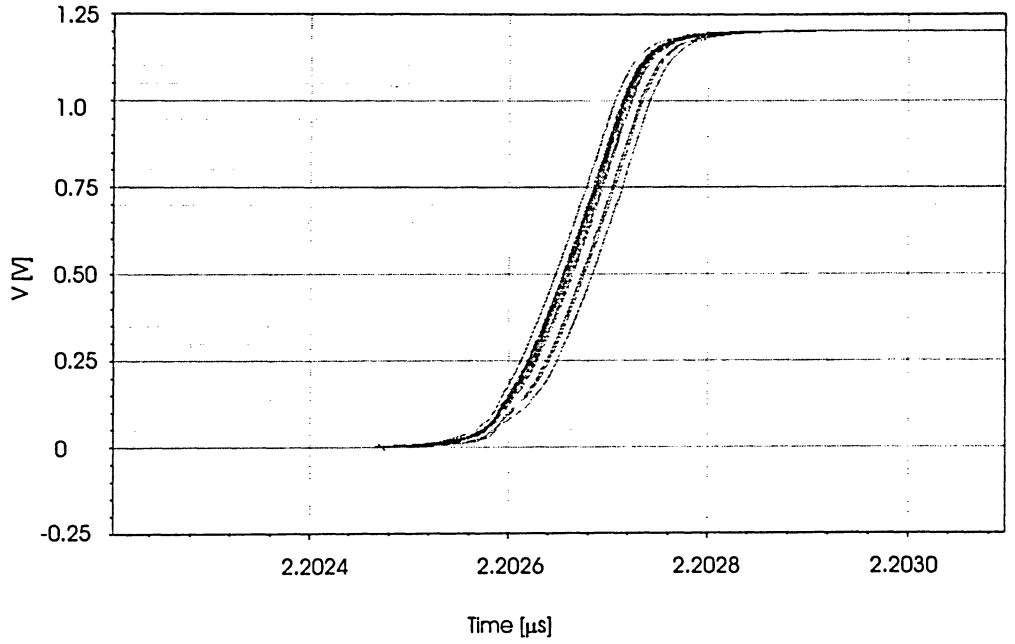

Figure 5.8: Simulated timing jitter of the phase-locked loop with the two-XOR phase detector.

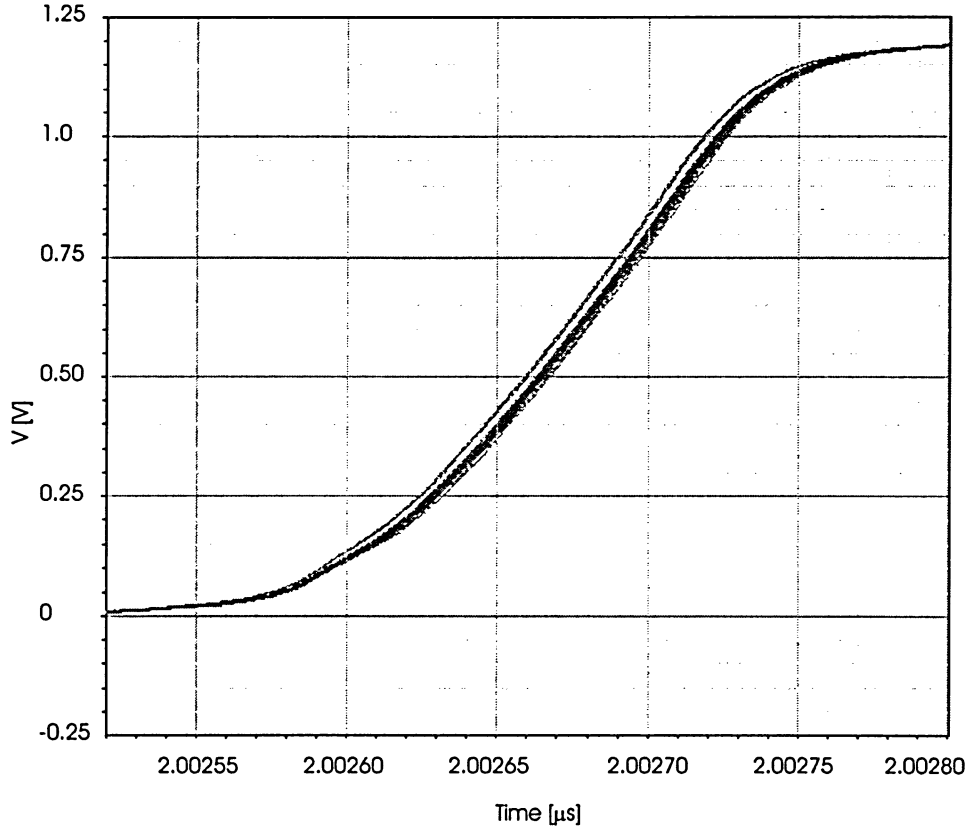

Figure 5.9: Simulated timing jitter of the phase-locked loop with the proposed hybrid phase detector.

the two-XOR phase detector and is much lower as compared with that of the PLL with the improved bang-bang phase detector.

Chapter 6

Bang-Bang Phase Detector with Regenerative DFFs

6.1 Introduction

As mentioned in Chapter3, the lock time and timing jitter of a PLL are largely affected by the characteristics of its phase/frequency detectors because the effectiveness of the feedback action of the PLL is ultimately determined by how fast and how accurate its phase/frequency detectors can sense the phase/frequency difference between the reference clock and the output of the local voltage controlled oscillator.

The performance of bang-bang phase detectors depends upon the speed of the DFF-samplers. Conventional DFFs suffer from a low speed due to their complex configuration. TSPC-based DFFs outperform others owning to their simple configuration [17]. The sampling speed of these DFFs, however, is still limited by their multi-stage configuration.

A design of a new bang-bang phase detector with regenerative samplers is presented in this chapter. The samplers of the bang-bang phase detector are evolved from the sense amplifiers widely used in memory design. Section.6.2 details the implementation of the proposed bang-bang phase detector. The effectiveness of the proposed phase/frequency detectors are assessed by incorporating them in a dual-loop phase-locked loop shown in Fig.6.3. The simulation results of the PLL are presented. This chapter concludes in Section.6.4.

6.2 Bang-Bang Phase Detectors

The bang-bang phase detector employs three D-flip flops as samplers. These DFFs are implemented using the regenerative amplifiers, as shown in Fig.6.1. The DFF consists of a re-generative stage composed of M_{1-4}, an equalization switch M_9, and four sample-and-hold switches M_{5-8}. The operation of the DFF is depicted as the following,

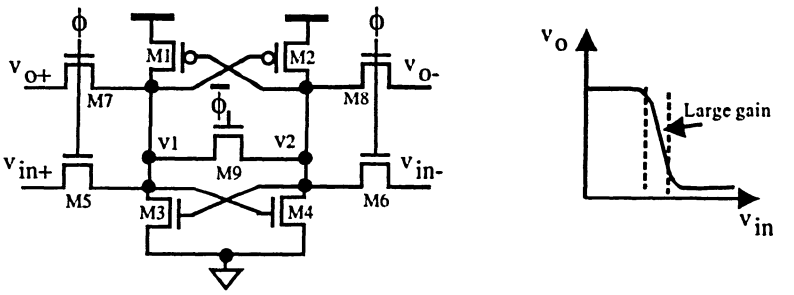

Figure 6.1: A regenerative DFF.

(1) *Equalization phase ($\phi = 0$)* - In the equalization phase, M_{5-8} are OFF and the regenerative amplifier is disconnected from the inputs. The outputs of the amplifier are held by the capacitors of M_{7-8}. The equalization switch M_9 is ON and forces $V_1 = V_2 \approx \frac{V_{dd}}{2}$. The operation point of the re-generative amplifier is set to the transition region of the cross-coupled static inverters such that a small variation of the input voltage will force the output of the amplifier to toggle from one logic state to the other.

(2) *Evaluation phase ($\phi = 1$)* - V_{in}^+ and V_{in}^- are sampled by M_5 and M_6. The outputs of the regenerative amplifier respond to the polarity of V_{in}^+ and V_{in}^- [14]. This DFF is much faster as compared with other DFFs for the following reasons : (i) The regenerative amplifier possesses a large voltage gain in the neighborhood of $V_{in} = \frac{V_{dd}}{2}$ shown in Fig.6.1. (ii) The positive feedback of the cross-coupled inverter pair ensures that even a small variation of the input voltage will result in a full-swing of the output voltage in a very short period of time, and (iii) the output voltage only needs to swing $\frac{V_{DD}}{2}$, rather than V_{DD} as other DFFs do.

The configuration of the bang-bang phase detector, shown in Fig.6.2, is similar to a conventional 2-level bang-bang phase detector, with the difference that the sampling clocks

Table 6.1: The regenerative DFF transistor size(L=0.13μm).

Transistor	Width(μm)
M1	4
M2	4
M3	4
M4	4
M5	2
M6	2
M7	2
M8	2
M9	20

are non-overlapping. Three preceding DFFs are used to sample ϕ_{ref} three time per data eye to offer $\frac{\pi}{2}$ phase quantization error and $-\frac{\pi}{2} < \phi < \frac{\pi}{2}$ phase detection range.

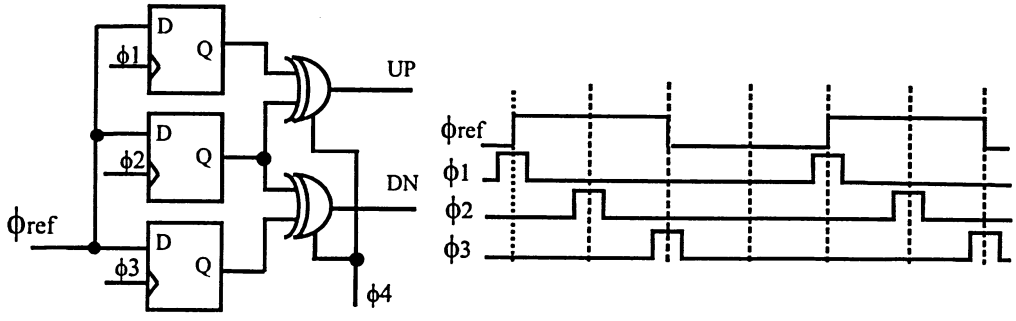

Figure 6.2: A new bang-bang phase detector with regenerative DFFs. The width of ϕ_{1-3} is $\frac{1}{3}$ of the width of the reference clock.

The dual-loop PLL shown in Fig.6.3 consists of (i) a phase correction loop and (ii) a frequency correction loop for fast lock. The charge pump is the current-steering charge pump shown in Fig.4.5. The frequency detector implemented in this design is shown in Fig.4.4. The delay cell of the VCO shown in Fig.4.10 is used in this dual loop PLL design. The schematics of resettable XOR gate is given in Fig.3.4. The transistors are sized by Table 6.1, Table 5.2, Table 5.3, and Table 5.4. In the loop filters, R is 1.1kΩ, C1 is 5.3pF, and C2 is 11.2pF, and C3 is 2pF.

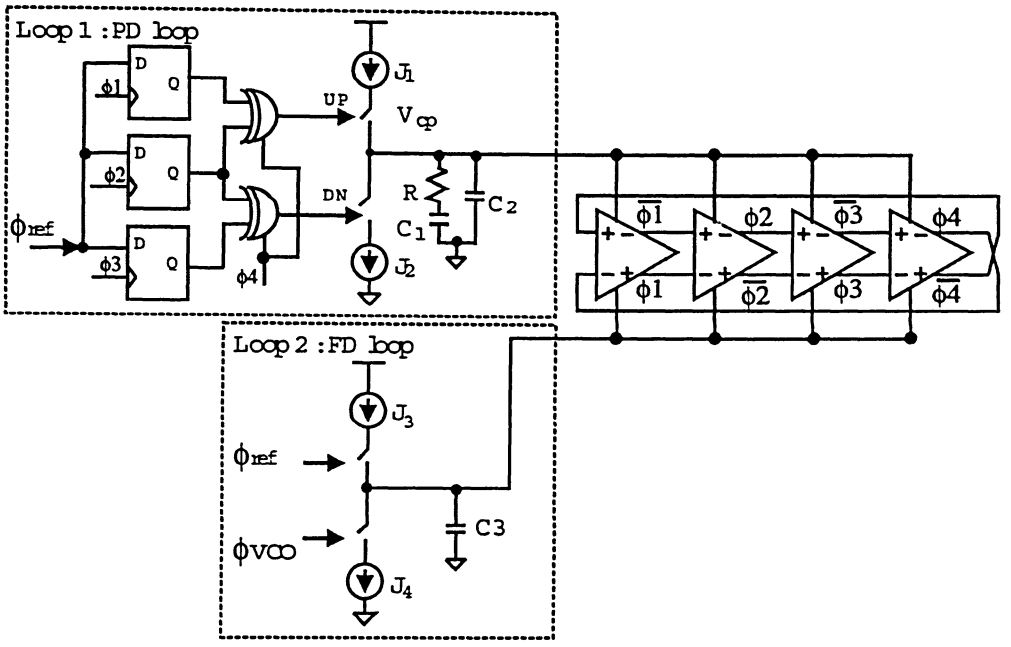

Figure 6.3: A dual-loop PLL with the new bang-bang phase detector. Circuit parameters : $C_1 = 5.3$ pF, $C_2 = 11.2$ pF, $C_3 = 2$ pF, $R = 1.1k\Omega$. $J_{1,2} = 28\mu$A, $J_{3,4} = 150\mu$A.

6.3 Simulation Results

To assess the effectiveness of the proposed bang-bang phase/frequency detector, a 2 GHz PLL has been implemented in UMC-0.13μm 1.2V CMOS technology and analyzed using Spectre from Cadence Design Systems with BSIM3v3 device models. The control voltage of the frequency correction loop of the PLL is plotted in Fig.6.4. The control voltage of the phase correction loop of the PLL is plotted in Fig.6.5. The phase noise of the output of the PLL is shown in Fig.6.6 that is computed by SpectreRF.

6.4 Chapter Summary

A new bang-bang phase detector and a charge-pump frequency detectors have been proposed and their applications in dual-loop phase-locked loops have been investigated. It was shown that the regenerative operation of the proposed bang-bang phase detector ensures a fast acquisition of incoming clocks while the charge-pump frequency detector effectively

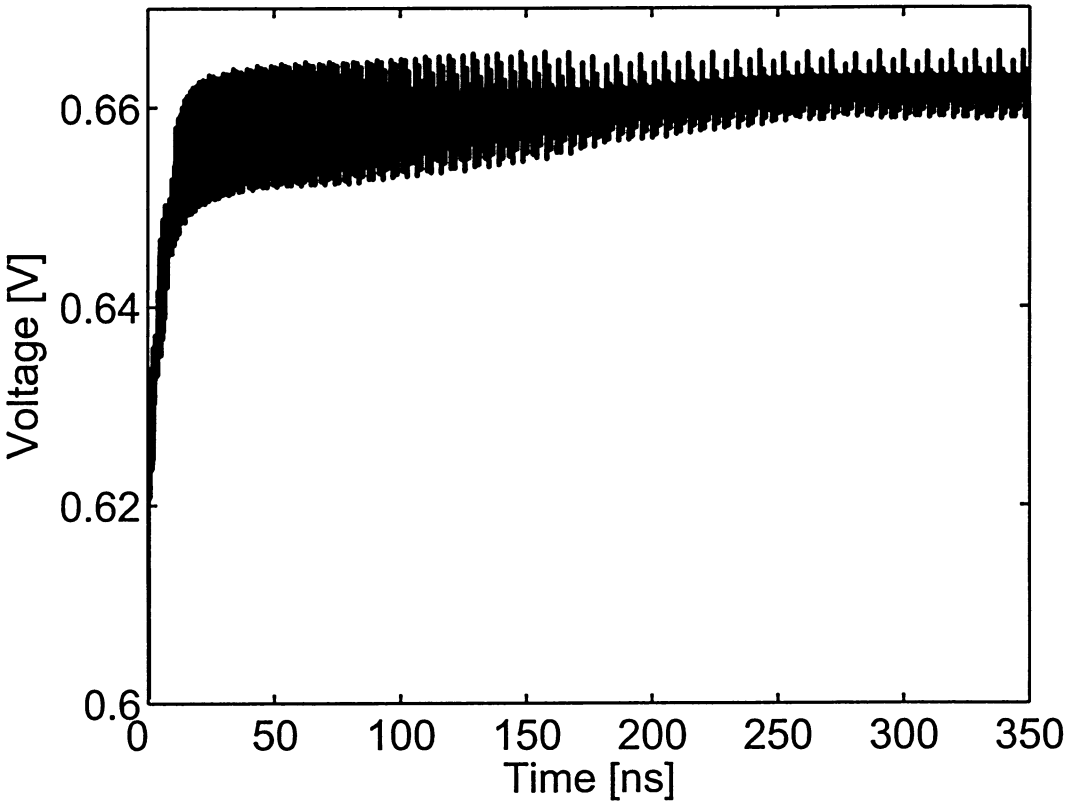

Figure 6.4: Control voltage of the frequency correction loop.

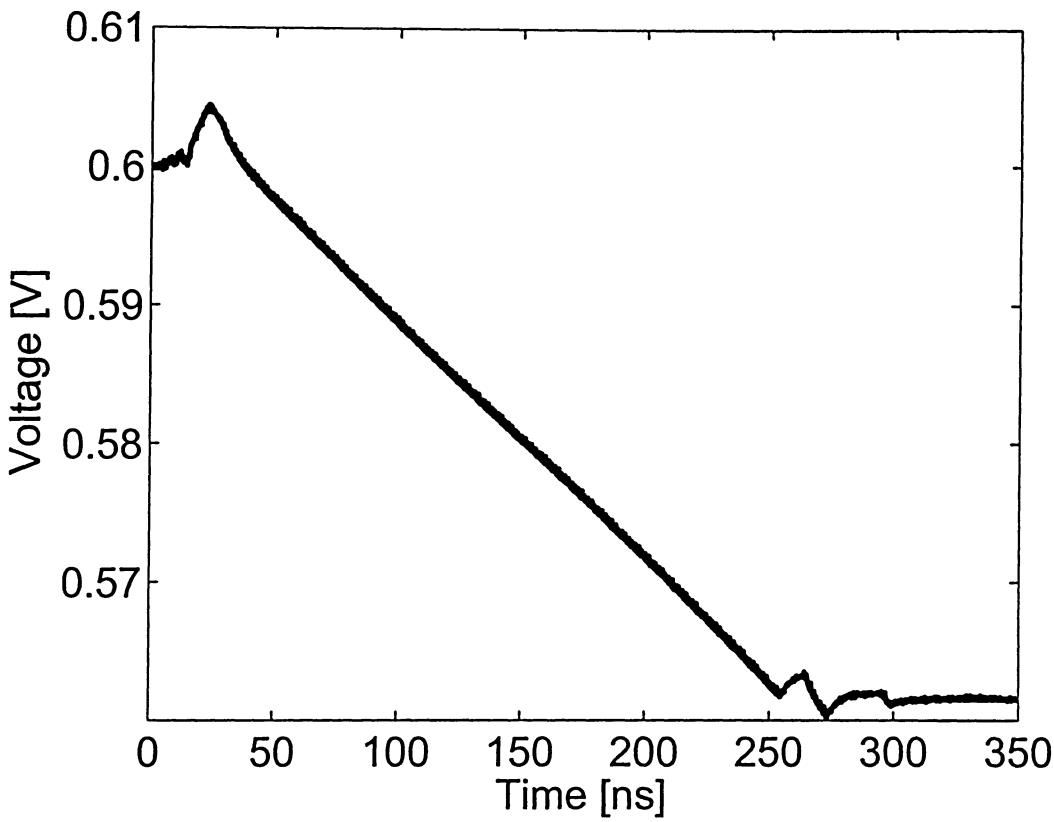

Figure 6.5: Control voltage of the phase correction loop.

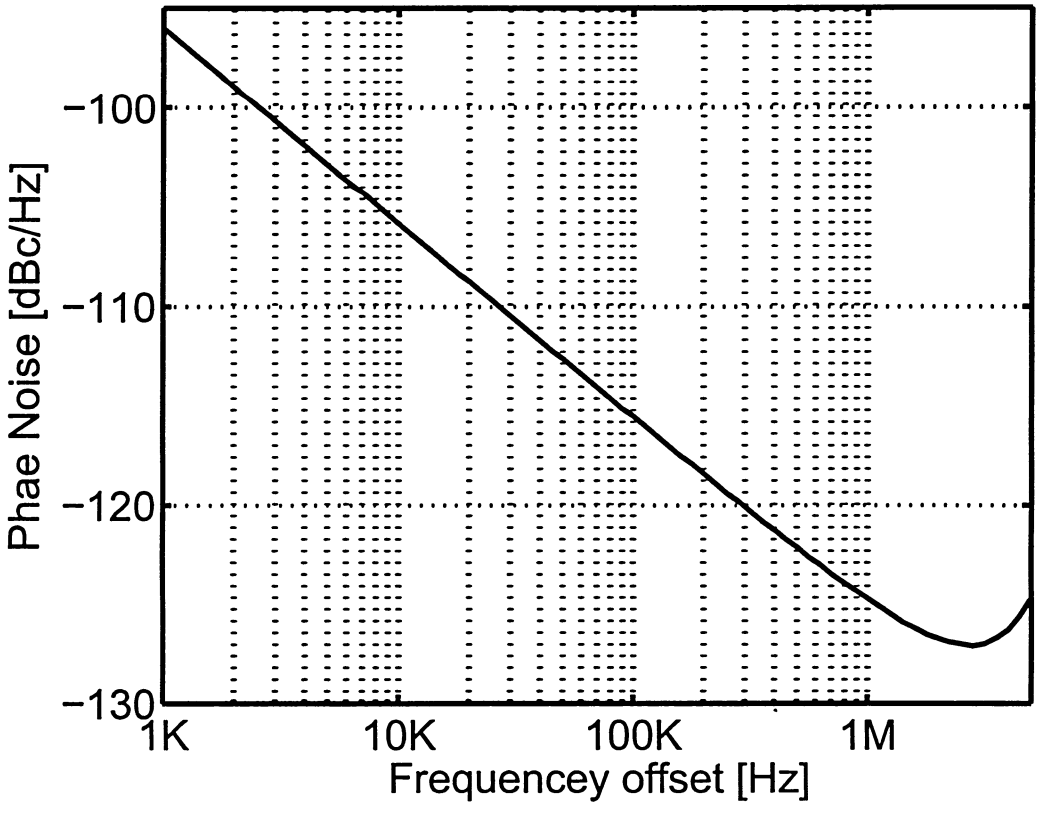

Figure 6.6: Simulated phase noise of the PLL in the locked state.

detects the frequency difference between the reference clock and local VCO output, ensuring a fast lock. The effectiveness of the proposed phase/frequency detectors has been validated by incorporated them in a 2 GHz dual-loop phase-locked loop implemented in UMC-0.13μm 1.2V CMOS technology and analyzed by Spectre with BSIM3.3v device models. Simulation results have demonstrated that the PLL reaches the lock state in 600 cycles with phase noise of -125 dBc/Hz at 1 MHz frequency offset.

Chapter 7

1X Bang-Bang Phase Detector

7.1 1X and 2X Bang-Bang Phase Detector Introduction

As mentioned in Section.3.2, bang-bang phase detectors are binary phase detectors. A traditional 2X bang-bang phase detector samples the incoming data twice per data eye using three samplers with a phase quantization error of $\frac{\pi}{2}$ [5]. The 4X bang-bang phase detector proposed in [5, 6] samples data four times per data eye and effectively lowers the phase quantization error to $\frac{\pi}{4}$, however, at the cost of five samplers. The phase detector presented in this chapter is a 1X bang-bang phase detector that samples data once per data eye. The phase detection range is extended to $-\pi < \Delta\phi < \pi$ with the lock state at $\Delta\phi = 0$. Section 7.2 details the implementation of the 1X bang-bang phase detector and the charge-pump frequency detector. The effectiveness of the proposed phase detector is assessed using a dual-loop PLL and the simulation results are compared with those of the same PLLs but with a 2X bang-bang phase detector in Section 7.3. The simulation results of the PLL are presented.

7.2 Bang-Bang Phase Detectors

7.2.1 1X bang-bang phase detector

The 1X bang-bang phase detector employs two D-flip flops as samplers. These DFFs are implemented as TSPC DFF shown in Fig.3.5.

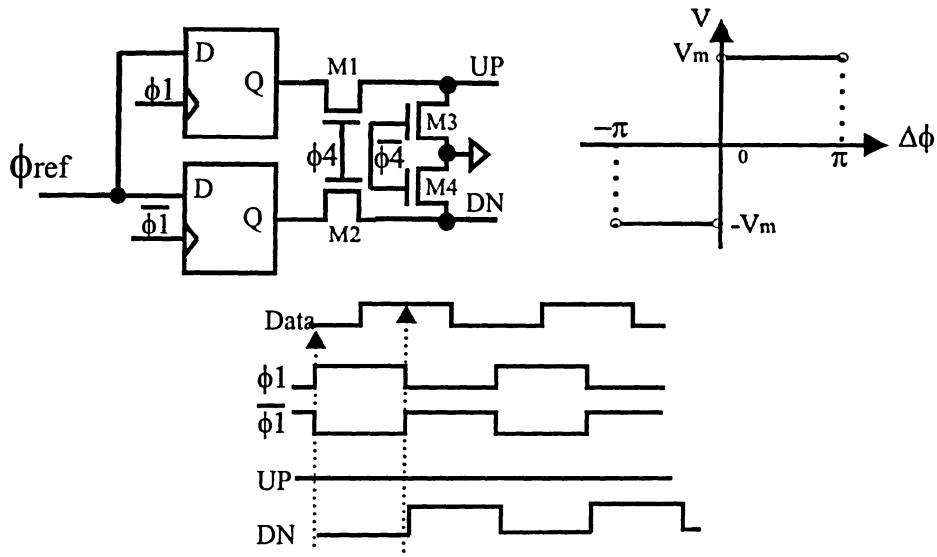

Figure 7.1: A 1X bang-bang phase detector. Circuit parameters: $W_{1-4} = 2\mu m$. $L = 0.18\mu$m.

The configuration of the 1X bang-bang phase detector is shown in Fig.7.1. Two DFFs are employed to sample data once per data eye. In the locking process, especially when the phase or frequency difference is large, 2X bang-bang phase detectors chase the rising and falling edges of the reference clock and might lock to either one of the two edges. The 1X bang-bang phase detector, however, tracks one edge only. This is explained in the next subsection.

7.2.2 Edge-chasing property of 1X and 2X bang-bang phase detector PLLs

In a PLL locking process, in case of a large phase and frequency deference, phase detcctors could not correct it in one or two cycles. In the locking process, a 2X bang-bang phase detector chases rising and falling edges, a 1X bang-bang phase detector tracks one edge only,

rising or falling edge. At a certain phase difference, the 2X bang-bang phase detector-based PLL will jump from chasing one edge to chasing the other. This property is shown in Fig.7.2 and Fig.7.3 and explained as following. Bolded waveforms are the most considered in these two figures.

Based on the PLL configuration, in both PLLs shown in Fig.7.2 and Fig.7.3 with either a 1X or a 2X phase detector, when UP='1', current source J1 charges the capacitors, Vc rises, and ϕ_3's phase from the VCO will be pulled to lead. When DN='1', J2 discharges the capacitors, Vc falls, and ϕ_3's phase from the VCO will be pushed to lag. So, that is:

(1) when UP='1' and DN='0', ϕ_3's phase is pulled to lead.

(2) when UP='0' and DN='1', it is pushed to lag.

(3) When UP=DN='1' or '0', no change.

In Fig.7.2:

CASE1: In Cycle I, UP='1', DN='0', result in that ϕ_3's raising edge is pulled towards the rising edge of ϕ_{ref}.

CASE2: In Cycle I, UP='0', DN='1', result in that ϕ_3's raising edge is pushed towards the rising edge of ϕ_{ref}.

CASE3: In Cycle I, UP='1', DN='0', result in that ϕ_3's raising edge is pulled towards the rising edge of ϕ_{ref}.

CASE4: In Cycle I, UP='0', DN='1', result in that ϕ_3's raising edge is pushed towards the rising edge of ϕ_{ref}.

In all above cases , ϕ_3's raising edge is always chasing the raising edge of ϕ_{ref}.

In Fig.7.3:

CASE1: In Cycle I, UP='1', DN='0', result in that ϕ_3's raising edge is pulled towards the rising edge of ϕ_{ref}.

CASE2: In Cycle I, UP='0', DN='1', result in that ϕ_3's raising edge is pushed towards the rising edge of ϕ_{ref}.

CASE3: In Cycle I, UP='0', DN='1', result in that ϕ_3's raising edge is pushed towards the falling edge of ϕ_{ref}.

CASE4: In Cycle I, UP='1', DN='0', result in that ϕ_3's raising edge is pulled towards the falling edge of ϕ_{ref}.

In the above first two cases, ϕ_3's raising edge is chasing the raising edge of ϕ_{ref}. In the last two cases, ϕ_3's raising edge is chasing the falling edge of ϕ_{ref}, compared to the last two cases in Fig.7.2.

Obviously, in CASE3 and CASE4 for both PLLs with the same phase difference between ϕ_3 and ϕ_{ref}, but UP and DN signals are generated differently and result in different edge chasing.

A specific phase difference point is observed when more attention is paid to the 2X bang-bang phase detector-based PLL. That is when the phase difference between ϕ_3 and ϕ_{ref} is close to $\pi/2$, any variation of ϕ_{ref} or VCO output will lead to the edge chasing jump between raising edge chasing and falling edge chasing, which is depicted in CASE5 in Fig.7.3. As a result, the 2X bang-bang phase detector tracking the rising edge of ϕ_{ref} in Cycle I, then may suddenly switch to track the falling edge in Cycle II. However, the 1X bang-bang phase detector tracks the same edge of ϕ_{ref} in both cycles and in all phase difference cases which is fixed by hardware connection of UP and DN to charge/discharge pumps. In other words, when the schematics is drawn, the lock edge is able to be predicted by the 1X bang-bang phase detector rather than the conventional bang-bang phase detector. This property secondly improves the locking speed of 1X bang-bang phase detector PLLs.

7.3 Simulation Results and Layouts

Two 2-GHz PLLs with identical second-order loop filters , charge pumps, and VCOs but a 1X bang-bang phase detector and a 2X bang-bang phase detector are implemented in TSMC-0.18μm 1.8V CMOS technology and analyzed using Spectre from Cadence Design Systems with BSIM3v3 device models that account for both the parasitics and high-order effects of MOS devices. The loop filter, charge pumps, the frequency detector and VCO delay cells are implemented as shown in Fig.4.6, Fig.4.5, Fig.4.4 and Fig.4.10. Transistors and capacitors in these figures are sized in Table.7.1, Table.7.2, Table.7.3, Table.7.4 and Table.7.5. The

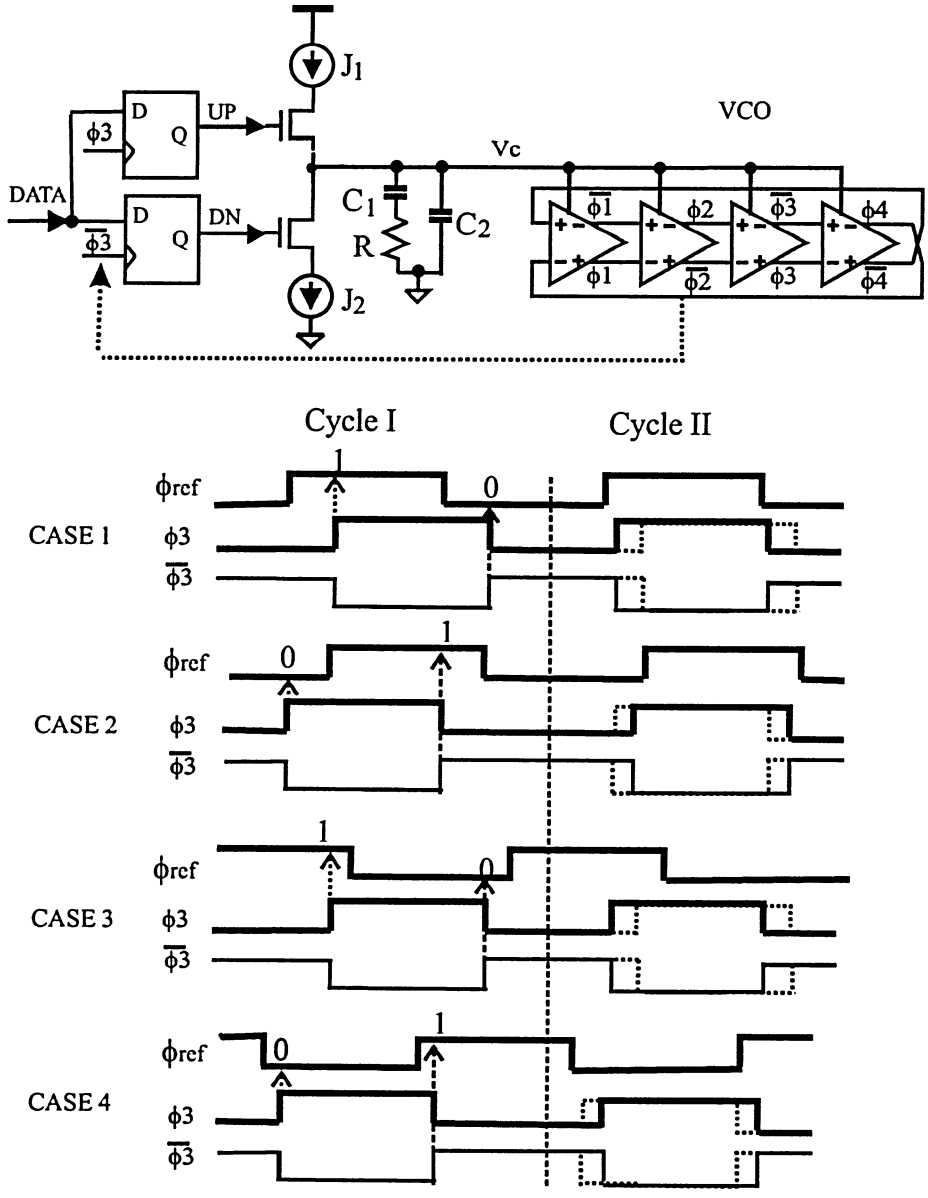

Figure 7.2: Edge chasing in the 1X bang-bang phase detector PLL.

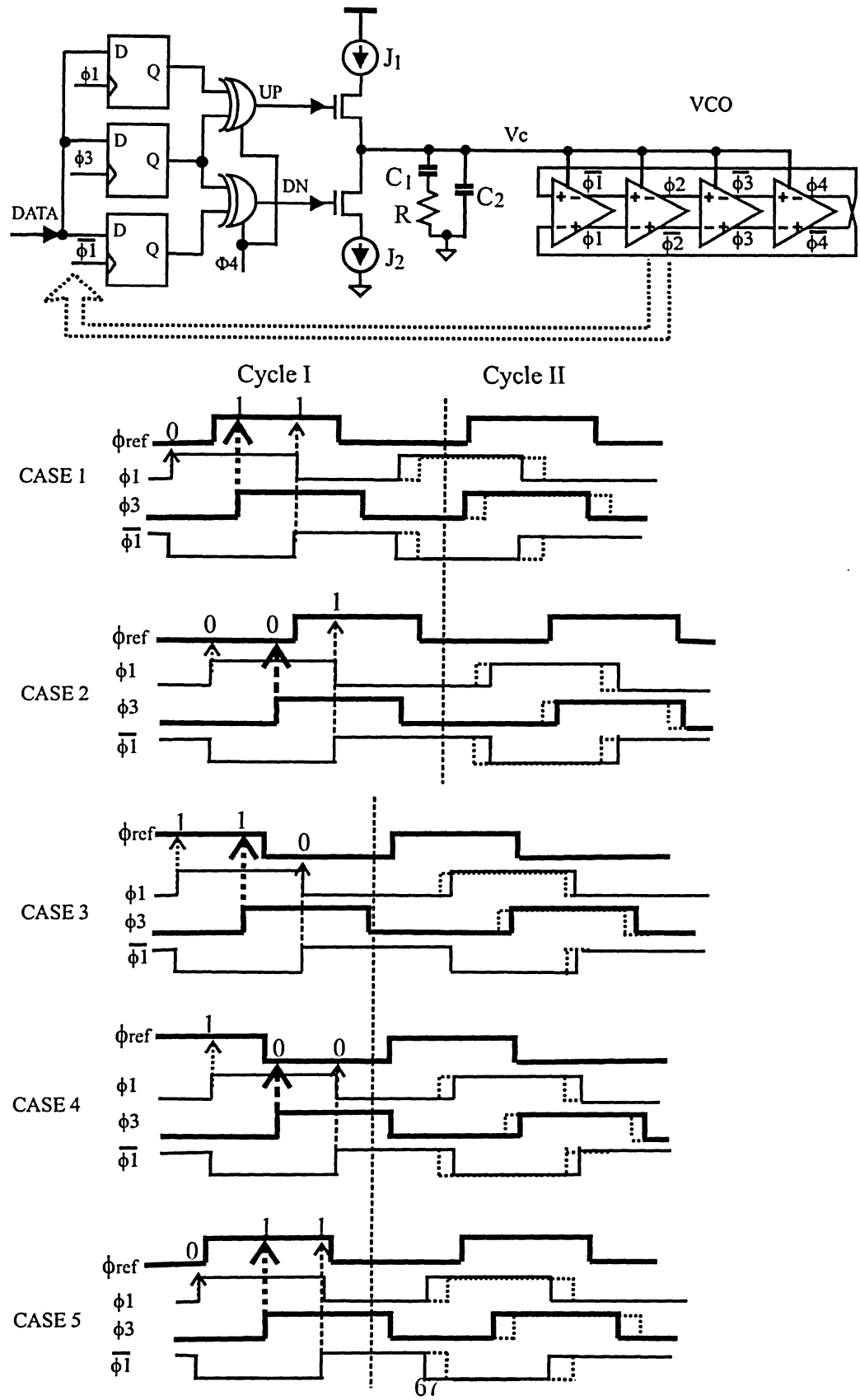

Figure 7.3: Edge chasing in the 2X bang-bang phase detector PLL.

Table 7.1: Loop filter components.

Component	Size
C1	11.2pF
C2	3.3pF
R	1.1KΩ

Table 7.2: Transistor size of charge pump for phase correction loop(L=0.18μm).

Transistor	Width(μm)
M1	20
M2	13
M3	10
M4	7
M5	10
M6	10
M7	10
M8	10

control voltages of the frequency/phase correction loops of the PLL with the 2X bang-bang phase detector are plotted in Fig.7.4. The control voltages of the frequency/phase correction loops of the PLL with the 1X bang-bang phase detector are plotted in Fig.7.5. The phase noise is shown in Fig.7.7, Fig.7.6 and Fig.7.8 predicted by Spectre and Verilog-A model. It is seen that the PLL with a 1X bang-bang phase detector has a significantly smaller lock time as compared with the PLL with a 2X bang-bang phase detector, owning to the unique locking property of the 1X bang-bang phase detector. The fluctuation of the control voltage of the frequency control loop of the two PLLs is comparable. The fluctuation of the control voltage of the phase control loop of the PLL with a 1X bang-bang phase detector, however, is visibly smaller as compared with that of the PLL with a 2X bang-bang phase detector, demonstrating that PLLs with a 1X bang-bang phase detector will have a lower phase noise. The phase noise comparison of the two PLLs will be given in the following simulation figures.

Fig.7.9 and Fig.7.10 show the layout of the 1X and 2X bang-bang phase detector PLLs. The following guidlines are used:

(1) MOSFETs with width greater than 8μm are laid out using multi-finger structures to

Table 7.3: Transistor size of charge pump for frequency correction loop(L=0.18μm).

Transistor	Width(μm)
M1	20
M2	7
M3	10
M4	4.5
M5	10
M6	10
M7	10
M8	10

Table 7.4: Transistor size of TSPC DFF for 1X and 2X bang-bang phase detectors(L=0.18μm).

Transistor	Width(μm)
M1	3
M2	4
M3	30
M4	20
M5	8
M6	3
M7	500n
M8	30
M9	30
M10	8
M11	8

Table 7.5: Transistor size of Delay cell for 1X and 2X bang-bang phase detector PLLs(L=0.18μm).

Transistor	Width(μm)
M1	800n
M2	800n
M3	12
M4	12
M5	1.5
M6	1.5
M7	2
M8	2

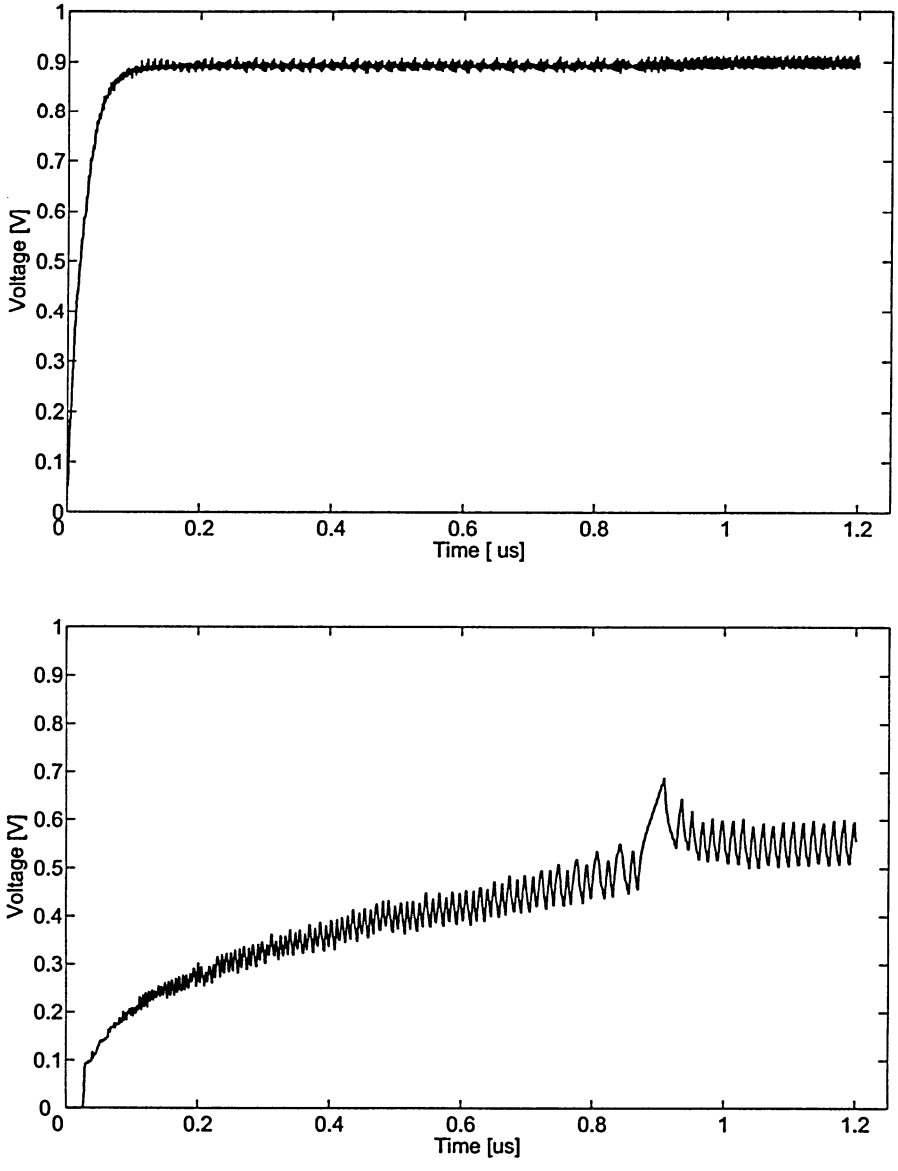

Figure 7.4: Control voltage of frequency correction loop (top) and phase correction loop of the PLL with the 2X bang-bang phase detector(bottom).

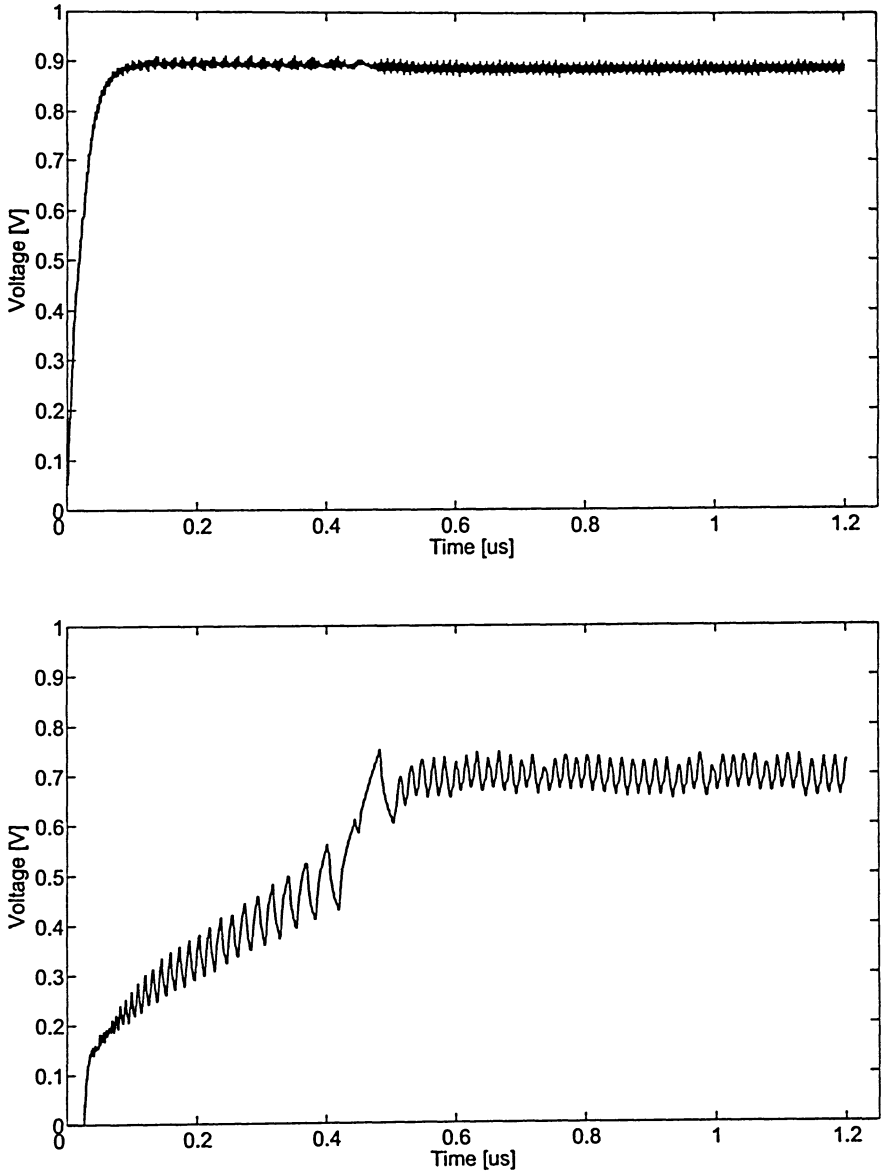

Figure 7.5: Control voltage of frequency correction loop (top) and phase correction loop of the PLL with the 1X bang-bang phase detector(bottom).

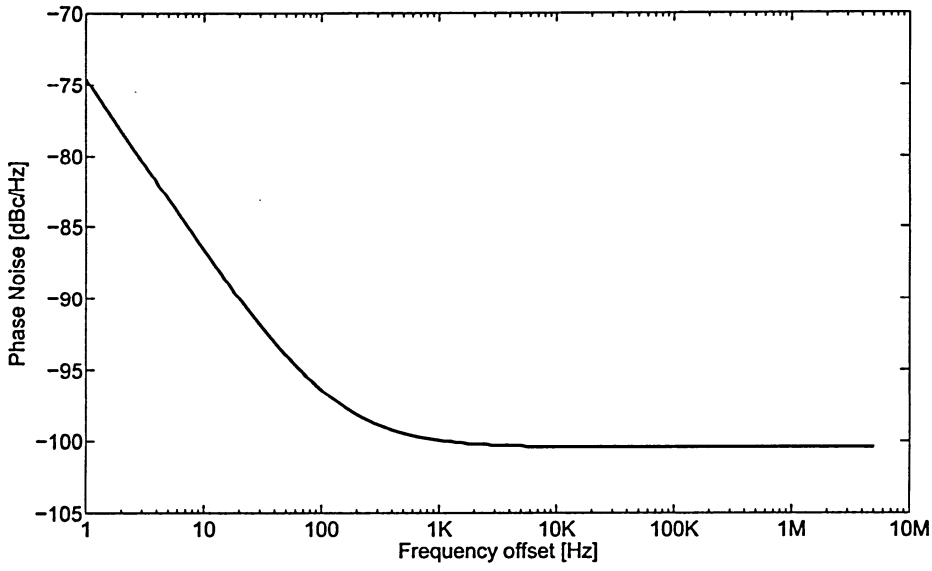

Figure 7.6: Phase noise of the 2X bang-bang phase detector PLL (SpectreRF).

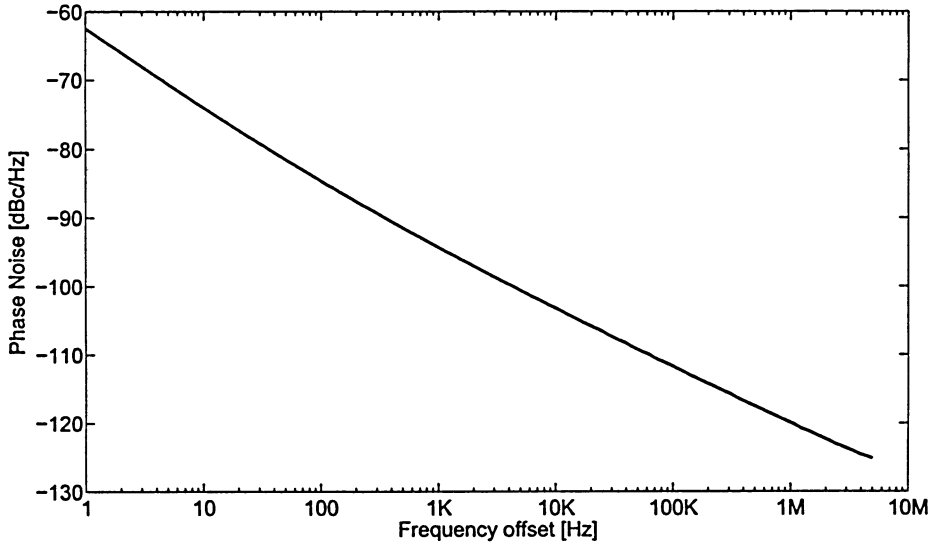

Figure 7.7: Phase noise of the 1X bang-bang phase detector PLL (SpectreRF).

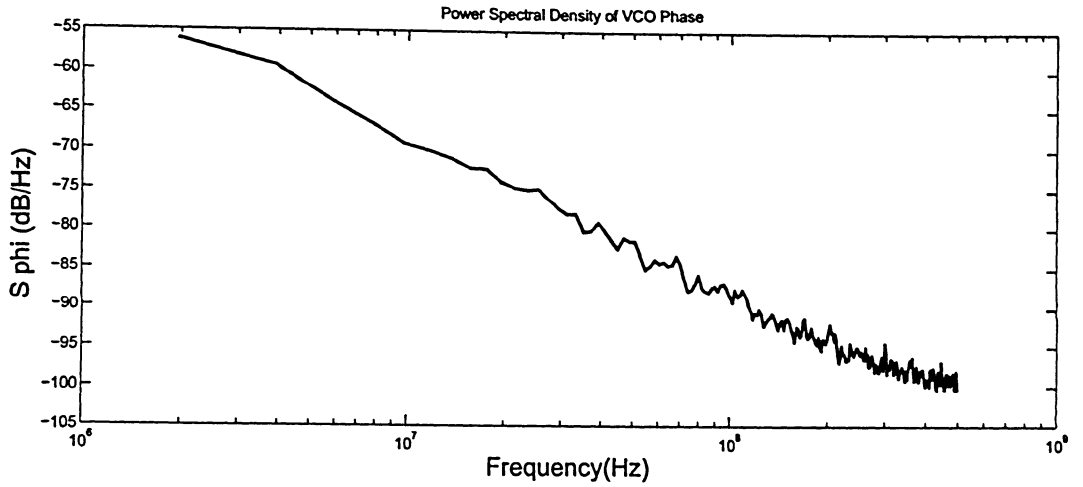

Figure 7.8: Phase noise of 1X and 2X bang-bang phase detector PLLs (Spectre and Verilog-A model).

reduce source/drain area and gate resistance.

(2) Floorplan the noise sensitive analog elements away from digital noise sources.

(3) Use dedicated analog power and ground supplies for the analog and biasing elements.

(4) Place guard rings around all sensitive circuits and noise source circuits.

Three guard rings are applied to phase detectors, charge pumps and VCOs to prevent switching noise and substrate noise coupling among these blocks.

7.4 Chapter Summary

A new 1X bang-bang phase detector has been proposed and its performance has been compared with a 2X bang-bang phase detector using dual-loop PLLs have both phase and frequency control loops. Simulation results have shown that the PLL with a 1X bang-bang phase detector has a significantly smaller lock time as compared with the PLL with a 2X bang-bang phase detector, owning to the unique locking property of the 1X bang-bang phase detector PLL. The fluctuation of the control voltage of the frequency control loop of the two PLLs is comparable. The fluctuation of the control voltage of the phase control loop of the PLL with a 1X bang-bang phase detector, however, is visibly smaller as compared with

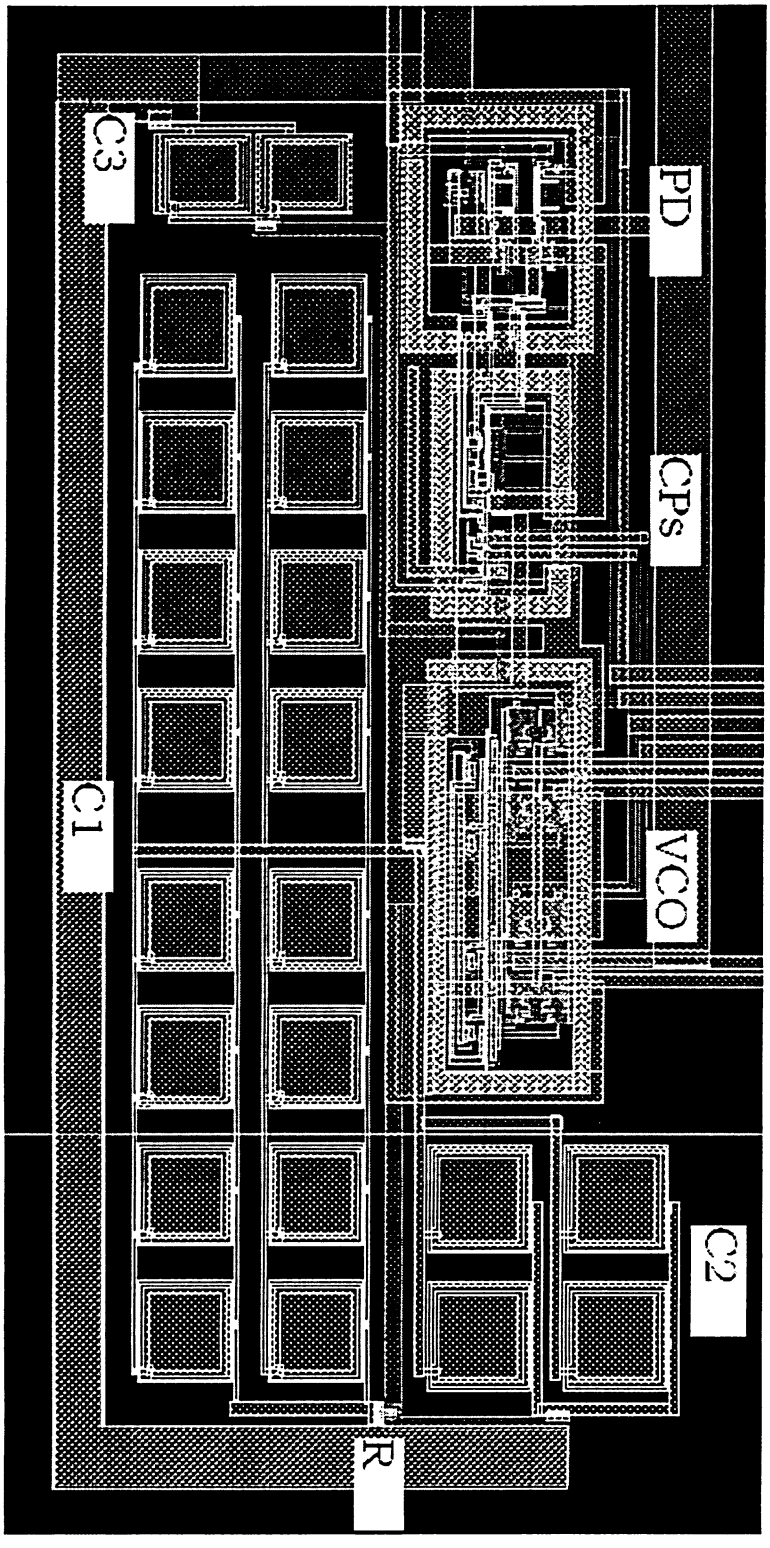

Figure 7.9: Layout of the 1X bang-bang phase detector PLL.

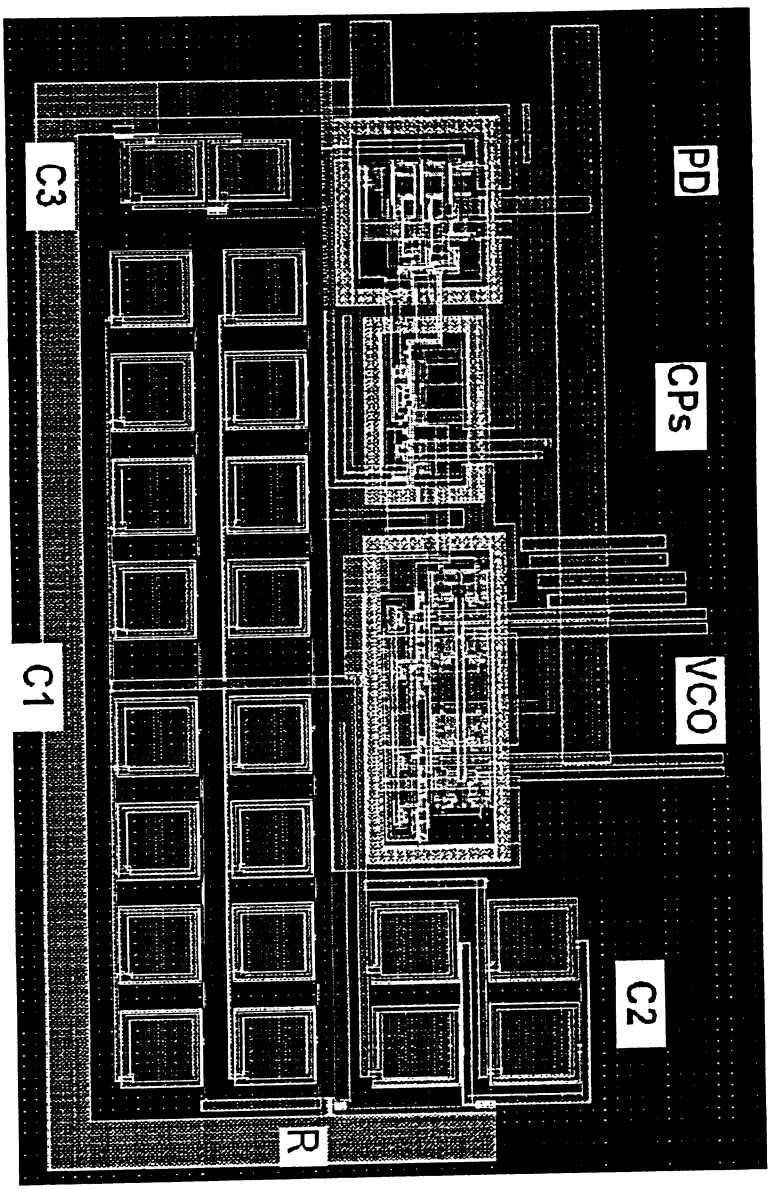

Figure 7.10: Layout of the 2X bang-bang phase detector PLL.

that of the PLL with a 2X bang-bang phase detector, demonstrating that PLLs with a 1X bang-bang phase detector has a lower phase noise.

Chapter 8

Conclusions And Future Work

In this thesis, the general high-speed serial link structure and its applications have been reviewed firstly. In a phase-tracking clock and data recovery of high-speed serial links, the phase-locked loop largely affects the system performance. Some basic phase-locked loop techniques have been reviewed. Performance of phase-locked loops is largely affected by the characteristics of that of the phase detectors.

Phase detectors and their characteristics have been discussed in this thesis. Among them, bang-bang phase detectors are extensively used in the modern high-speed serial link designs due to its high gain property, but the timing jitter is larger than that of linear phase detector PLLs. The hybrid phase detector which combines a linear phase detector, a 2XOR phase detector and a binary phase detector, a bang-bang phase detector has been presented in this thesis. A phase-locked loop with a hybrid phase detector shows a fast locking process and low timing jitter in lock state. The design of frequency detectors proposed to enhance the locking of the PLL is another important design along with a bang-bang phase detector.

Data samplers are essential components in bang-bang phase detectors. TSPC D-flip flop is used in one design of the bang-bang phase detector. In this thesis, a regenerative D-flip flop has also been proposed as a data sampler for the bang-bang phase detector. Regenerative D-flip flops possess the high-speed property as sense amplifiers do. It improves the sampler speed to sense the phase difference between two input signals.

A 2X bang-bang phase detector and a 4X bang-bang phase detector sample the incoming

data two and four times per data eye respectively. The proposed 1X bang-bang phase detector samples the incoming data only once per data eye. The simulation results show that phase-locked loops with a 1X bang-bang phase detector have the shorter locking time than that with a 2X bang-bang phase detector due to its single edge chasing characteristics. The 1X bang-bang phase detector presents phase detection range $-\pi < \Delta\phi < \pi$ with the lock state at $\Delta\phi \approx 0$ rather than $-\frac{\pi}{2} < \Delta\phi < \frac{\pi}{2}$. The simple circuit structure of 1X bang-bang phase detector improves the speed of the phase detection as well.

As examined in the preceding chapters, the proposed new bang-bang phase detectors have shown their characteristics in PLLs. It is worth taking the next step to build the receiver system and feeding the data stream in to the receiver to further exam the proposed phase detectors' performance. Connecting the receiver to a transmitter with a channel will be the further next step to build the high-speed serial link transceiver system.

Appendix A

Verilog A Code of PLL Modeling Blocks

(1) Phase/Frequency Detector and Charge Pump Module Code:

```
// VerilogA for Jitter, Jitter_PFD_CPLstg15, veriloga
include "constants.vams"
include "disciplines.vams"
module pfd_cp(out, ref, vco);
output out;
electrical out;
input ref;
electrical ref;
input vco;
electrical vco;
parameter real Iout=500u;
parameter integer dir=1 from[-1:1] exclude 0;
parameter real tt=1n from(0:inf);
parameter real ttol=1p from(0:inf);
integer state;
analog begin
@(cross(V(ref),dir,ttol)) begin
```

```
if(state>-1)state=state -1;
end
@(cross(V(vco), dir, ttol)) begin
if(state<1) state=state +1;
end
I(out)<+transition(Iout*state, 0,tt);
end
endmodule
```

(2) Oscillator Module Code:

```
// VerilogA for Jitter, OSCListing14, veriloga
include "constants.vams"
include "disciplines.vams"
module osc(out);
output out;
electrical out;
parameter real freq=25M from(0:inf);
parameter real ratio=125 from(0:inf);
parameter real Vlo=-1, Vhi=1;
parameter real tt=0.01*ratio/freq from(0:inf);
parameter real accJitter=0 from[0:0.1/freq);
parameter real syncJitter=0 from[0:0.1*ratio/freq);
integer n, accSeed, syncSeed;
real next, dT, dt, accSD, syncSD;
analog begin
@(initial_step) begin
accSeed=286;
syncSeed=-459;
accSD=accJitter*sqrt(ratio/2);
```

```
syncSD=syncJitter;
next=0.5/freq+$abstime;
end
@(timer(next+dt)) begin
n=!n;
dT=accSD*$rdist_normal(accSeed, 0, 1);
dt=syncSD*$rdist_normal(syncSeed, 0, 1);
next=next+0.5*ratio/freq +dT;
end
V(out)<+transition(n? Vhi: Vlo,0,tt);
end
endmodule
```

(3) Voltage Controlled Oscillator Module Code:

```
// VerilogA for Jitter, VCO+FDn, veriloga
include "constants.vams"
include "disciplines.vams"
module vco(out, in);
output out;
electrical out;
input in;
electrical in;
parameter real Vmin=0;
parameter real Vmax=1.2 from(Vmin:inf);
parameter real Fmin=1G from(0:inf);
parameter real Fmax=3G from (Fmin:inf);
parameter real ratio=10 from(0:inf);
parameter real Vlo=-1, Vhi=1;
parameter real tt=0.01*ratio/Fmax from(0:inf);
```

```
parameter real jitter=4.5p from(0:0.25*ratio/Fmax);
parameter real ttol=1u*ratio/Fmax from(0:ratio/Fmax);
parameter real outStart=100n from (1/Fmin:inf);
real freq, phase, dT, delta, prev, Vout;
integer n, seed, fp;
analog begin
@(initial_step) begin
seed=-561;
delta=jitter*sqrt(2*ratio);
fp=$fopen("eriods.m");
Vout=Vlo;
end
freq=(V(in)-Vmin)*(Fmax-Fmin)/(Vmax-Vmin)+Fmin;
if(freq¿Fmax)freq=Fmax;
if(freq¡Fmin)freq=Fmin;
freq=(freq/ratio)/(1+dT*freq/ratio);
phase=idtmod(freq,0.0,1.0,-0.5);
@(cross(phase-0.25, +1, ttol)) begin
dT=delta*$rdist_normal(seed,0,1);
Vout=Vhi;
end @(cross(phase+0.25, +1, ttol)) begin
dT=delta*$rdist_normal(seed,0,1);
Vout=Vlo;
if($abstime)$fstrobe(fp, "0.10e", $abstime - prev);
prev=$abstime;
end
V(out)<+ transition(Vout,0,tt);
end
```

endmodule

(4) Spectre netlist for a PLL

simulator lang=spectre

ahdl_include "osc.va"

ahdl_include "pfd_cp.va"

ahdl_include "vco.va"

Osc(in) osc freq=1294MHz ratio=1 accJitter=0 syncJitter=0

PFD(err in fb) pfd-cp Iout=150ua

C1 (err 0) capacitor c=3.3pF

R (err c) resistor r=1.1K

C2 (c 0) capacitor c=11.2pF

VCO (fb err) vco Fmin=1GHz Fmax=2.2GHz Vmin=0 Vmax=1.8 ratio=1

jitter=0.068ps outStart=1us

JitterSim tran stop=7us

(5) Matlab script file.

```
echo off;
nfft=512;
winLength=nfft;
overlap=nfft/2;
winNBW=1.5;
load periods.m
T=mean(periods);
J=std(periods);
maxdT=max(abs(periods-T))/T;
fprintf('T= .3gs, F= .3gHz, T, 1/T);
fprintf('Jabs= .3gs, Jrel=.2g, J, 100*J/T);
fprintf('max dT=.2g, 100*maxdT);
fprintf('periods=d, nfft=d', length(periods),nfft);
```

```
phases=2*pi*cumsum(periods)/T;
[Sphi,f]=psd(phases,nfft,1/T,winLength, overlap,'linear');
Sphi=winNBW*Sphi/nfft;
K=length(f);
semilogx(f(2:K),10*log10(Sphi(2:K)));
title('Power Spectral Density of VCO Phase');
xlabel('Frequency(Hz)');
ylabel('S phi (dB/Hz)');
rbw=winNBW/(T*nfft);
RBW=sprintf('', rbw, 10*log10(rbw));
imtext(0.5,0.07,RBW);
```

Appendix B

Abbreviations

ATA—Advanced Technology Attachment

BER—Bit Error Rate

CDR—Clock and Data Recovery

CP—Charge Pump

CRC—Cyclic Redundancy Check

CMOS—Complementary Metal-Oxide-Semiconductor Transistor

DEMUX—Demultiplexing

DFF—D Flip Flop

DME—Differential Manchester Encoding

FPGA—Field Programmable Gate Array

f_T—Cut off frequency

IDE—Integrated Drive Electronics

IEEE—Institution of Electrical and Electronics Engineers

LED—Light-Emitting Diode

LP—Loop Filter

MOS—Metal-Oxide-Semiconductor Transistor

MPE—Manchester Phase Encoding

NRZ—None-Return-to-Zero

NRZI—None-Return-to-Zero Inverted coding

OC——Optical Carrier

OSC——Oscillator

PFD——Phase and Frequency Detector

PAM——Pulse Amplitude Modulation

PCI——Program Controlled Interruption

PLL——Phase-Locked Loop

RZ——Return to Zero

SDH——Synchronous Digital Hierarchy

SONET—Synchronous Optical Network

STM——Synchronous Transmission Mode

TSPC—-True Single Phase Clocked

UMC——United Microelectronics Corporation

VCO——Voltage-Controlled Oscillator

XAUI—-X Attachment Unit Interface

XOR——Exclusive OR gate

Bibliography

[1] T. Wang, *A Low-Voltage CMOS Current-Mode Incremental Signaling Scheme Of High-Speed Parallel Links*, Master of Applied Science Thesis, Ryerson University, Toronto, August 2006.

[2] S. Soliman, F. Yuan and K. Raahemifar, "An overview of design techniques for CMOS phase detectors", in *Proc. IEEE Int'l Symp. Circuits and Systems*, Vol. 5, pp. 457-460, Scottsdale, Arizona, May 2002.

[3] B. Razavi, "Challenges in the design high-speed clock and data recovery circuits", *IEEE Communications Magazine*, Vol. 40, No. 8, pp. 94 - 101, Aug. 2002.

[4] J. Kang and D. Kim, "A CMOS clock and data recovery with two-XOR phase-frequency detector circuit", in *Proc. Int'l Solid-State Circuits Conf., Digest Tech. Papers*, Vol. 4, pp. 226-229, May 2001.

[5] M. Ramezani and C. Salama, "An improved bang-bang phase detector for clock and data recovery applications", in *Proc. Int'l Symp. Circuits and Systems*, Vol. 1, pp. 715-718, Sydney, June 2001.

[6] K. Lee, S. Kim, G. Ahn, and D. Jeong, "A CMOS serial link for fully duplexed data communication", *IEEE J. Solid-State Circuits*, Vol. 30, No. 4, pp. 353-364, Apr. 1995.

[7] J. Yuan and C. Svensson, "New single-clock CMOS latches and flipflops with improved speed and power savings", *IEEE J. Solid-State Circuits*, Vol. 32, No. 1, pp. 62-69, Jan. 1997.

[8] J. Lee and B. Kim, "A low-noise fast-lock phase-locked loop with adaptive bandwidth control", *IEEE J. Solid-State Circuits*, Vol. 35, No. 8, pp. 1137-1145, Aug. 2000.

[9] J. Kim, S. Lee, T. Jung, C. Kim, S. Cho, and B. Kim, "A low-jitter mixed-mode DLL for high-speed DRAM applications", *IEEE J. Solid-State Circuits*, Vol. 35, No. 10, pp. 1430-1436, Oct. 2000.

[10] R. Walker, "Designing bang-bang PLLs for clock and data recovery in serial data transmission system", In *Phase-Locking in High-Performance Systems*, IEEE Press, pp. 34-45, 2003.

[11] J. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques", *IEEE J. Solid-State Circuits*, Vol. 31, No. 11, pp. 1723-1732, Nov. 1996.

[12] K. Kundert, *Predicting The Phase Noise And Jitter Of PLL-Based Frequency Synthesizers*, Designer's guide Consulting Inc., Version 4g, August 2006.

[13] P. Huang, H. Chen and R. C. Chang, "Multiphase-output delay-locked loops", in *Proc. IEEE Asia-Pacific Conf., Advanced System Integrated Circuits*, pp. 68-71, August 2004.

[14] T. Wang and F. Yuan, "A new current-mode incremental signaling scheme with applications to Gb/s parallel links", *IEEE Trans. on Circuits and Systems I - Regular Papers.* Vol. 54, No. 2, pp. 255-167, Feb. 2007.

[15] D. Foty, *MOSFET Modeling With SPICE - Principle And Practice*, Prentice-Hall, Upper Saddle River, N.J., 1997.

[16] F. Yuan, *CMOS Current-Mode Circuits for Data Communications*, Springer, New York 2007.

[17] J. Rabaey, *Digital Integrated Circuits - A Design Perspective*, Prentice-Hall, Boston, 1st Ed., 1996.

[18] G. Bianchi, *Phase-locked loop synthesizer simulation*, McGraw-Hill, New York, 2005.

[19] F. Gardner, *Phaselock Techniques*, WILEY-INTERSCIENCE, 3rd Ed., Palo Alto, California, 2005.

[20] B. Razavi, *Design Of Analog CMOS Integrated Circuits*, McGraw Hill, Los Angeles, 2001.

[21] R. Best, *Phase-Locked Loops, Design, Simulation And Applications*, McGraw-Hill, Oberwil, Switzerland, 4th Ed., 2003.

[22] D. Banerjee, *PLL Performance, Simulation, And Design*, 3rd Ed., 2003.

[23] D. Johns, and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons Inc., Toronto, 1996.

[24] J. Lee, K. S. Kundert, and B. Razavi, "Analysis and modeling of bang-bang clock and data recovery circuits", *IEEE J. Solid State Circuits*, Vol. 39, No. 4, pp. 613-621, Apr. 2004.

[25] C-K. K. Yang, R. Farjad-Rad, and M. A. Horowitz, " A 0.5-μm CMOS 4.0-Gbit/s serial link transceiver with data recovery using over sampling", *IEEE J. Solid-State Circuits*, Vol. 33, No. 5, pp. 713-722, May 1998.

[26] M. Horowitz, C-K. K. Yang, and S. Sidiropoulos, "High-speed electrical signaling: Overview and Limitations", *IEEE Micro*, 1998, pp. 12-24.

[27] C-K. K. Yang , and M. A. Horowitz, "0.8μm CMOS 2.5Gb/s oversampled receiver for serial links", *IEEE Journal of solid State Circuits*, Vol. 31, No. 12, pp. 2010-2023, Dec. 1996.

[28] M. Ramezani, C. Andre, and C. Salama, "A 10 Gb/s CDR with a half-rate bang-bang phase detector", in *Proc. IEEE Int. Symp. Circuits and Systems*, Vol. 2, pp. 181-184, May 2003.

[29] M. Ramezani, C. Andre, and C. Salama, " Jitter analysis of a PLL-based CDR with a bang-bang phase detector", *The 2002 45th Midwest Symposium on Circuits and Systems*, Vol. 3, pp. 393-396, Aug. 2002.

[30] J. Savoj, and B. Razavi, " A 10-Gb/s CMOS clock and data recovery circuit with a half-rate binary phase/frequency detector", *IEEE Journal of Solid State Circuits*, Vol. 38, No. 1, pp. 13-21, 2003.