MAGNETICALLY COUPLED RESONANT WIRELESS POWER TRANSMISSION SYSTEM THAT MEETS THE REZENCE EFFICIENCY AND FREQUENCY SPECIFICATION

By

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Magnetically Coupled Resonant Wireless Power Transmission

System that Meets the Rezence Efficiency and Frequency Specification

Master of Applied Science, 2018

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Electrical and Computer Engineering

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Abstract

High efficiency Class-E Power Amplifiers (PA) are difficult to analytically design using the original design equations. We present a high frequency (HF) Class-E PA design methodology that simplifies design in this thesis. A high-efficiency Class-E PA was designed using a low-cost power FET by following this design-flow.

Due to their small size, it's difficult to design efficient MCR-WPT resonators for portable electronics. We propose a novel multi-layer MCR-WPT Printed Spiral Coil (PSC) design and design methodology. Two MCR-WPT PSC resonators were designed for smartphones and tablets to meet the Rezence Self-Resonant Frequency and efficiency specifications using this novel design and design methodology.

The MCR-WPT resonators power transfer efficiency is reduced when their separation distance is below the optimal Critical Coupling Distance (CCD) due to frequency splitting. We present a novel maximum-peak detection and auto-tuning circuit that automatically improves efficiency using capacitive tuning when the separation distance is below the CCD.

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Table of Contents

List of Tables

List of Figures

List of Appendices

Abbreviations

A4WP	Alliance for Wireless Power
AC	Alternating Current
ADS	Advanced Design System
BSIM	Berkeley Short-channel IGFET Model
CAD	Computer Aided Design
CCD	Critical Coupling Distance
dB	Decibel
dBm	Decibel with respect to 1 Milliwatt
DC	Direct Current
EM	Electromagnetic
EMI	Electromagnetic Interference
EMPro	Electromagnetic Professional
FEM	Finite Element Method
FET	Field Effect Transistor

FR4	Flame Retardant 4
HF	High Frequency
IPC	Association Connecting Electronics Industries (formerly -Institute Printed for Circuits)
kHz	kiloHertz
MCR-WPT	Magnetically Coupled Resonant Wireless Power Transmission/Transfer
MCU	Micro Controller Unit
MHz	MegaHertz
mil	one-thousandth of an inch
MOM	Method of Moments
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PA	Power Amplifier
PCB	Printed Circuit Board
PEC	Perfect Electric Conductor
PRU	Power Receiving Unit
PSC	Printed Spiral Coil
PTU	Power Transmitting Unit
Rx	Receiver

SRF	Self-Resonant Frequency
Tx	Transmitter
WPC	Wireless Power Consortium
WPT	Wireless Power Transmission/Transfer

Chapter 1

1 Introduction

The Airfuel (formerly known as A4WP) Rezence Wireless Power Transmission (WPT) standard was established 2012 [1] to wirelessly power portable devices. Researchers from MIT developed the Magnetically Coupled Resonant Wireless Power Transmission (MCR-WPT) techniques in 2007 [2] which the Rezence technology is based on. Some of the applications that the MCR-WPT technique is used in are charging TVs, electric vehicles and other large electronics [3], [4] and [5]. With this technique, Rezence has the ability to charge in smaller electronic devices such as tablets, smartphones and Bluetooth headsets [6]. These devices can be charged at a distance allowing for freedom of placement in horizontal and vertical dimensions for a true drop and go user experience [1]. Power solutions from 1-50W range allow it to support multi-device charging.

In this chapter, the basic background of the Rezence standard is presented in section 1.1. We then go through some of the design issues associated with the Rezence standard in section 1.2. This is followed by the contributions of this thesis in section 1.3. Then the thesis organization is briefly described in section 1.4. Finally, we conclude this chapter in section 1.5.

1.1 Background and Literature Review

Wireless Power Transmission (WPT) has been around for more than a century. One of the earliest research done used wireless power and resonance techniques for a transformer system for electric railways in 1894 by M. Hutin and M. Leblanc [7], [8]. Extensive research was later done by Nicola Tesla on WPT, who by 1910s held many patents [9] for WPT applications including WPT using high-tension tesla coils [10], and an apparatus for transmitting electrical energy [11]. Tesla also did multiple other experiments with WPT, in one of them he used the experimental setup shown in Figure 1.1-1 to wirelessly power an electric light bulb using a pair of coils. Because of his broad and cutting-edge research on WPT, Tesla is considered a pioneer of the field [7].

There are multiple works done by Tesla in WPT that have helped to pave the way for the establishment of WPT. After Tesla, there was a pause in WPT research until after WWII [12], wherein 1962 the first long-range microwave WPT system was demonstrated by William C. Brown [13]. At around the same time in the 1960s, research was being done with short-range WPT systems for biomedical applications using inductive WPT such as in [14] and [15]. Lots more research was done over the next few decades using various types of WPT in different applications, which is discussed in more detail in [7]and [12].

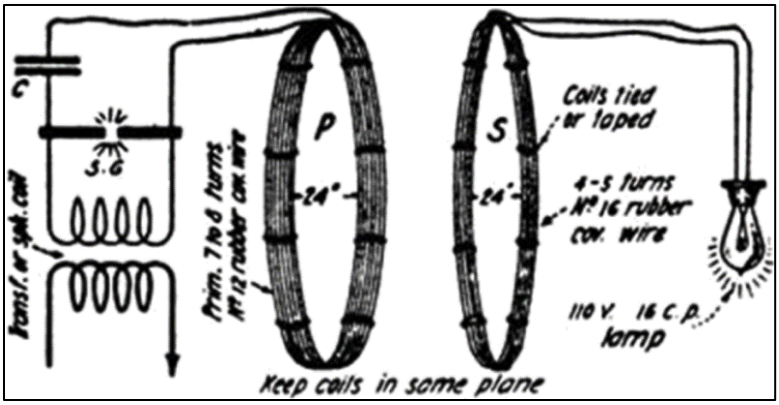


Figure 1.1-1 One of Tesla's wireless power transmission experiment [7]

In 2007, a group of researchers from MIT demonstrated Wireless power transmission using strongly coupled magnetic resonance [2], also known as MCR-WPT [16]. The work uses impedance matching and resonance to extend the transmission distance to mid-range WPT. This new approach is the foundation of the WiTricity Drive11 WPT standard for cars [4], and the Airfuel Rezence WPT standard portable electronic devices [17].

1.1.1 Basic overall Architecture

The Rezence WPT standard uses magnetic resonance, instead of inductance to wirelessly charge portable electronic devices. According to [6], it brings many improvements over its inductive counterparts for wireless charging, which include:

- **Large charging range** – instead of being limited to a charging pad, the device can be placed anywhere in the charging range.
- **Multiple device charging** – devices with different power requirements (such as smartphones and tablets) can be charged simultaneously.
- **Real world safe charging** – Stray metallic objects such as keys and utensils tend to heat up in the presence of magnetic fields due to eddy currents generated in the metals. Due to the resonant nature of MCR-WPT, most of these object won't heat up unless they resonate at the transmission frequency, which reduces the risk of power loss in nearby stray metallic objects. Also using Bluetooth 4.0 LE, Rezence charging surfaces will only transmit power when compatible devices are present, thereby further reducing this hazard.

To accomplish these improvements, the Rezence WPT standard uses the system architecture provided in Figure 1.1-2. The standard transmits power using 6.78MHz resonators. The overall system which is composed of a Power Transmit Unit (PTU) and a Power Receiving

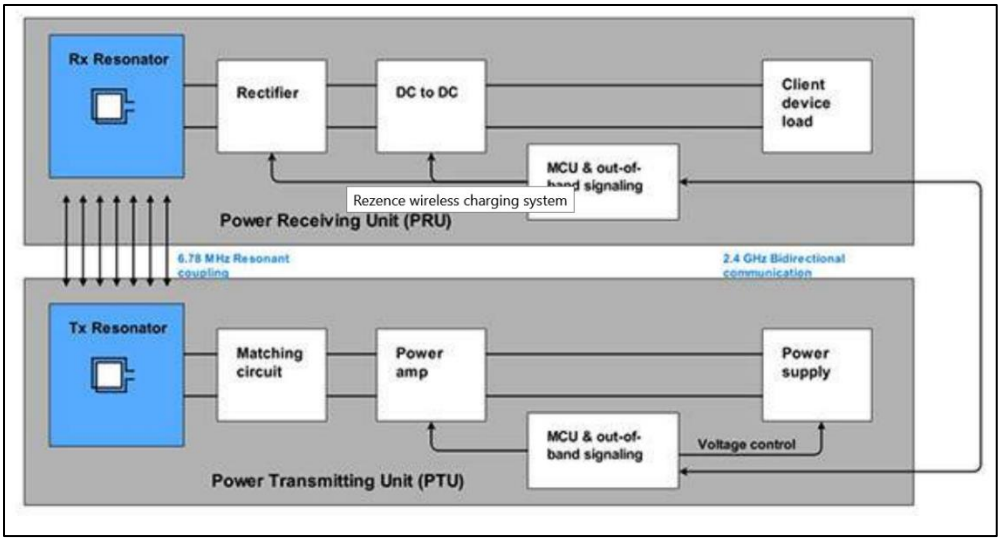


Figure 1.1-2 Rezence magnetic resonance wireless power specification [18]

Unit (PRU). The PTU is has a power supply block, Power Amplifier, matching network and transmitter Resonator (Tx). The PRU is has a Receiver Resonator (Rx), Rectifier, and DC-DC Converter. There are two Microcontroller Units (MCU), one at the PTU and PRU respectively. Each Block will be briefly discussed here and more detail in the subsequent chapters. There are 5 categories of PRU and 5 classes of PRUs which are presented in Table 1.1-1.

1.1.2 Communication between the MCU

The MCUs uses a propriety protocol via Bluetooth 4.0 LE (smart) to allow to PTU and PRUs to communicate with one another. This enables the PTU to identify compatible PRU

Table 1.1-1 PRU and PTU device classifications [6].

Power Receiving Unit (PRU)			Power Transmitting Unit (PTU)	
Category 1	Bluetooth Headset	(On Roadmap)	Class 1	(On Roadmap) – Supporting 1 category 1 device
Category 2	Feature Phone	3.5 Watts	Class 2	10 Watts– Supporting 1 category 1, 2 or 3 device
Category 3	Smart Phone	6 Watts	Class 3	16 Watts – Supporting 2 category 1, 2, or 3 devices, or 1 category 4 device
Category 4	Tablet	(On Roadmap)	Class 4	22 Watts – Supporting 3 category 1, 2, or 3 devices, or 1 category 4 device.
Category 5	Laptop	(On Roadmap)	Class 5	(On Roadmap) – TBD

devices before it starts transmitting power. This is done to ensure that power is not transmitted in the presence of stray metallic objects. It is also used to adjust the Impedance Matching Network to improve the efficiency when the device is not at the optimal location for maximum efficiency. The protocol allows for the communication between PTU and PRUs so that the Power Amplifier input power can be adjusted to accommodate the number of PRUs in range

1.1.3 Power Supply, Oscillator, and Gate driver

The Power Supply block is composed of 3 sub-blocks including the Power Supply, Oscillator and Gate Driver as illustrated in Figure 1.1-3. The power supply provides a stable voltage supply for the oscillator, gate driver and PA. It can be adjusted to by the MCU to deliver a more or less power to the PA depending on how many Load devices need to be powered up. Since the oscillator and gate driver blocks need a constant voltage supply, a voltage regulator could be used to supply constant supply voltage in the presence of the changing power supply

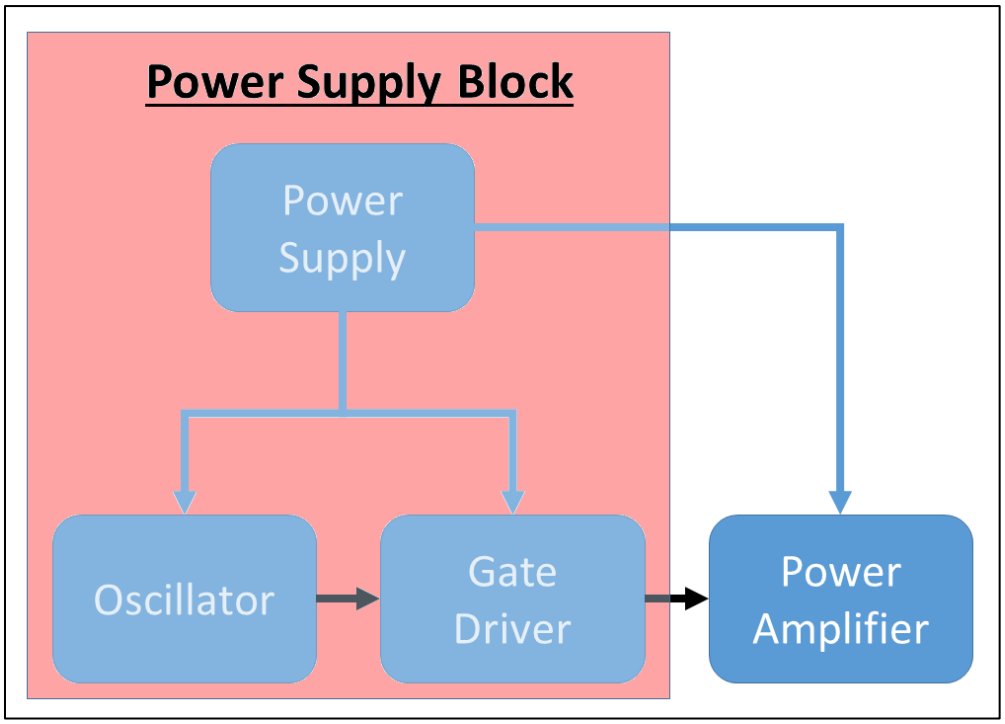


Figure 1.1-3 Rezence power supply sub-blocks

There are many types of oscillators, such as the Colpitts, Crystal and Hartley Oscillators among others. Since the Rezence frequency specification is 6.78MHz ±15kHz, the oscillator accuracy and stability are a primary concern. Extra attention should be given to the selection of oscillator components that are unaffected by temperature and voltage variations.

Gate Drivers are used to supply the PA input with enough power so that it can function correctly. The gate of switch mode PAs must be charged and discharged quickly so that it acts as a switch, and can be done with two types of gate drivers, a square or sine wave. Both types of gate drivers need additional circuitry to operate correctly, where the square wave gate drivers need an analog to digital converter between the oscillator output and its input, and the sine wave gate driver needs an impedance matching network between its output and the PA input. The selection of the gate driver is dependent on which gate driver enables the PA to achieve higher output efficiency when applied to the PA input.

1.1.4 Power Amplifier and Impedance Matching

The Power Amplifier (PA) supplies to the power that the Tx Resonator transmits to the Rx resonator. There are many types of PAs available which are grouped into two main categories, namely controlled conduction angle and switch mode PAs. The controlled conduction angle PAs are composed of the common class A, AB, B and C PAs which have simpler designs, with the exception of the class C PA, generally have higher input to output power linearity at the cost of a lower efficiency. Switch mode amplifiers which include D, E, and other PA classes, use digital input signals to constantly drive the transistor output into saturation and cut-off regions by switching the input between “fully-ON” and “fully-OFF”. These PAs generally have a higher efficiency, with some PAs achieving 100% efficiency, but they are non-linear, so additional circuitry is required to ensure the amplified input signal is not altered at the output. Power

Amplifier (PA) linearity is highly important when transmitting information and data. The Rezence resonators are not concerned with PA linearly since they only transmit power. Because of this switch-mode PAs like the class D and E are used for their high efficiency.

Regardless of the type of PA used to supply power to the TX resonator, the output must be impedance matched to the Tx resonator input to ensure maximum power transfer. This is done with a power matching network composed of capacitors and inductors which ideally have purely imaginary impedances with no resistive losses. In reality, all passive devices exhibit some resistive loss, but since the 6.78MHz Rezence operating frequency is much less than 300MHz (the frequency where transmission line effects should be taken into account the frequency wavelength is comparable to the wire trace lengths). There are a few basic impedance matching network topologies such as the L, π and T networks which are shown in Figure 1.1-4. Impedance matching theory is not discussed in detail in this thesis, but many books and articles that discuss the theory of these networks, example [19].

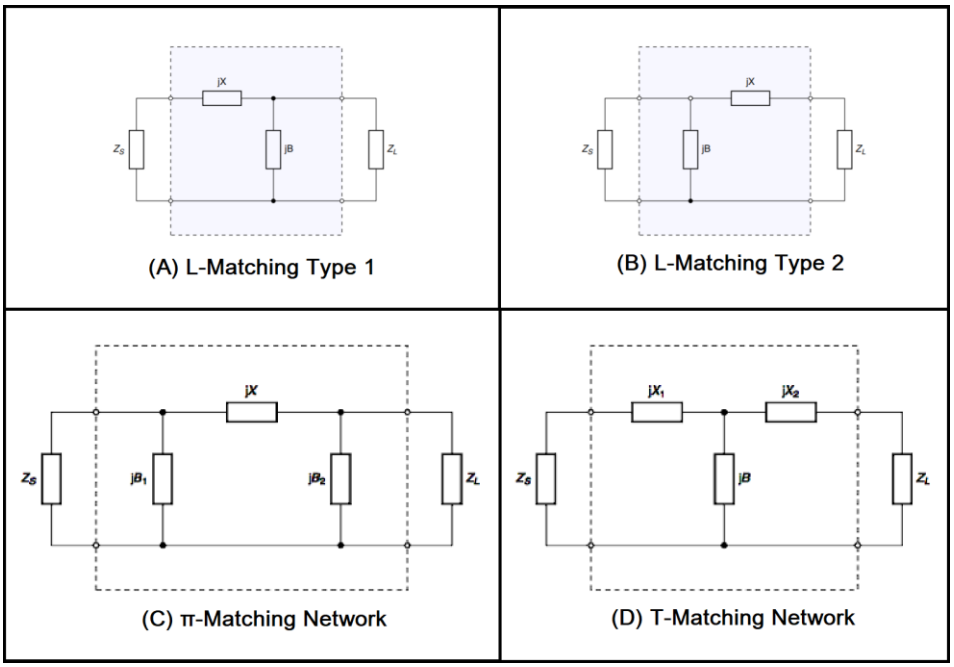


Figure 1.1-4 Basic impedance matching networks using lumped components

1.1.5 Magnetic Coupling Resonant Wireless Power Transmission Coils

The Magnetic Coupling Resonant Wireless Power Transmission (MCR-WPT) coils used to design the Tx and Rx resonators, supply power to the PRU from the PTU. It does so by converting AC current to a resonant magnetic field at the Tx resonator, which is received by the Rx resonator and converted back to an AC current. The physical dimensions of the Tx and Rx resonators such as the number of turns, wire width, wire thickness, wire spacing, inner and outer coil diameters, and the number of layers have a direct impact on the self-inductance and self-capacitance. These parameters also determine the efficiency, Self-Resonant Frequency (SRF), and the transmission distance between the Tx and Rx. There are multiple inductor coil geometries available which can be used for the resonator designs.

1.1.6 Rectifiers and DC-to-DC converters

AC to DC rectification is generally implemented using a rectifier. There are many types of rectifiers used for both single and three phase systems which can be categorized into 3 groups, uncontrolled, half-controlled and fully controlled rectifiers, which are shown in Figure 1.1-5. When designing or selecting a rectifier for frequencies above 1MHz, extra attention should be placed on the reverse recovery time and reverse bias capacitance as they significantly reduce the rectifier efficiency.

DC-DC converters are used in a multitude of applications including electric motor drives, Switch mode DC power supplies, etc. There are two device categories, linear voltage regulators which have low efficiency, and switch mode DC-DC converters which can have efficiencies near 90%. The switch mode DC-DC converters can also be subdivided into types, converters with without isolation, such as the boost and buck converters, and converters with isolation, such as the full-bridge and push-pull converters among others [20]. For WPT system the Buck converters are

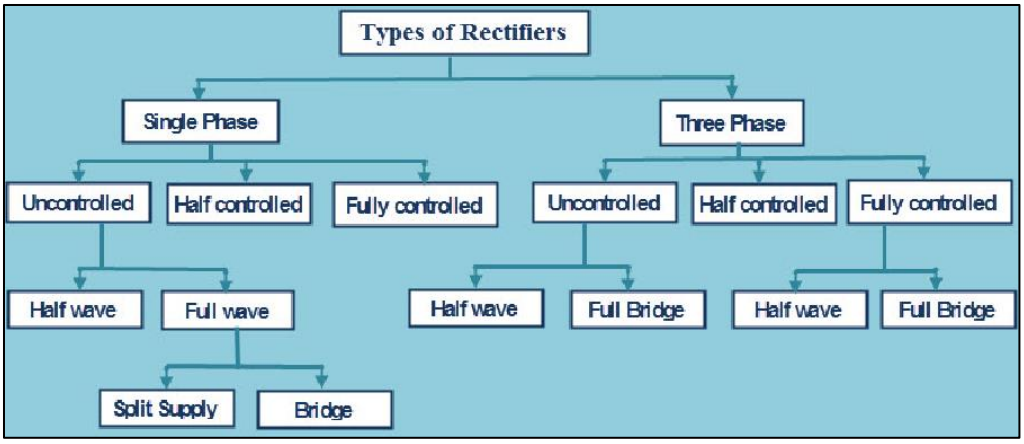


Figure 1.1-5 Types of rectifiers [21]

mostly used. The above material about converters are provided for informational purposes and is not discussed in detail in this thesis, but many books and articles that provide this information.

1.2 Motivations and Objectives

Even with all these advantages, the Rezence standard has over the other WPT standards, the system suffers from an overall low transmission efficiency [22]. These efficiency challenges include difficulties designing high-efficiency PAs as revealed in section 1.2.1. Also low-efficiency MCR-WPT Tx and Rx resonators due to coil size restrictions on the coil parameters as mentioned in section 1.2.2. Finally, reduced efficiency occurs when the Rx resonator is not placed at the optimal separation distance from the Tx resonator which is brought up in section 1.2.3. Our objectives are, therefore, to simplify the design flow for a high power Class E PA, design MCR-WPT PSCs to achieve high efficiency at the 6.78MHz Rezence frequency specification, and to implement impedance match tuning to counteract changes in mutual inductance due to distance changes and improve efficiency

1.2.1 Class E PA design

Ideal Class-E PAs can achieve high efficiency using a relatively compact circuit topology, but they are difficult to design. The original work [23] takes into consideration a 50% duty and

presents 3 equations that use the design frequency, output power, supply voltage, and knee voltage to determine the Class-E parallel capacitor, shifting inductor and load resistor values. These equations are simple but they don't give much insight into how to design a Class-E PA for a given specification, or how to impedance match the output. Therefore, there is a need to create a Class-E PA design flow that speeds up the design.

There are other parameters besides those used in [23] that should be considered when designing a Class-E PA. At a 50% duty cycle, large peak voltage and currents waveforms, which are high multiples of the supply voltages and currents, appear at the drain of the Power FET, so the Power FET's absolute maximum voltages and currents should be above these values to guarantee device reliability. Since the magnitude of these peak values is dependent on duty cycle, using a duty cycle other than 50% would decrease these current and voltage values enough, to allow for Class-E PA design using power FET devices unable to handle the 50% duty cycle peak values. There are theoretical design equations which include the duty cycle [24]. But these equations are lengthy, which makes them difficult to use to analytically design a Class-E PA. Other factors such as the Power FET's intrinsic output capacitance, should be considered to ensure proper Class-E operation during simulations and device reliability. There are also many other factors that need to be considered to realize physical prototype such as power FET power dissipation limits and temperature, passive component tolerances and available discrete values, capacitor maximum currents and voltages, inductor maximum current and SRF to name a few.

This thesis presents a proposed design flow based on [25], that simplifies and speeds up Class-E design for shortwave HF applications such as the Rezence 6.78MHz. Using this flow it is shown that a high-efficiency Class-E PA can be designed using a low-cost Power FET.

1.2.2 Coil Design

Due to their small size Bluetooth devices, Feature phones and Smartphones place restrictions on the physical dimensions of an embedded MCR-WPT Rx Resonator. These size restrictions significantly affect the maximum efficiency and the minimum SRF that can be achieved when designing the MCR-WPT Rx Resonator. This is because the dimensions of the coils used in their design are directly related to the coil inductance. To increase the inductance of the coil, the number of turns and the inner and outer diameter must be increased, but this is limited by the device restrictions.

The available coil types that can be used to design the Rx is also limited. Previous MCR-WPT coil designs with high efficiency and low SRF using 4-coil helix [2], inner magnetic core [26], and non-planar (wire-wound) coils [27] designs can't be used in this application due to the thickness restrictions of these devices. However Printed Spiral Coils (PSC), whose design is based on spiral inductors that have been broadly used in RF Integrated circuit for many years [28] can be used in this application due to their small size

Single layer MCR-WPT PSCs can be designed to achieve a high efficiency in small devices. But when their size is decreased to fit in the devices, the SRF increases. This can be overcome by significantly increasing the wire thickness to increase capacitance and inductance, or by adding an external capacitor [16]. But this makes the coils too bulky for our application. Double layer MCR-WPT coils based on series stacked inductors which have been shown to reduce the SRF [29] and [30] have been used.

A proposed modified version of the double layer MCR-WPT PSCs without vias is presented in this thesis. We demonstrate that the efficiency can be increased and the SRF can be

reduced to meet the specifications in the Rezence system without external passive components. It is also shown that the design can be further improved by changing the dielectric substrate and increasing the number of layers.

1.2.3 Impedance Matching, and Tuning to Counteract Frequency Splitting

The Rezence system can wirelessly transmit power over a wide distance range and is capable of high-efficiency WPT at the optimal separation distance known as the Critical Coupling Distance (CCD), between the Tx and Rx resonators. However, when the Rx resonator is placed at a distance that is less than the CCD, the transmission efficiency decreases. This decrease in efficiency is from the frequency splitting phenomenon which is inherent to all MCR-WPT coils. Frequency splitting is caused by the change in mutual induction due to a change in separation distance less than the CCD, resulting in a reduced efficiency at the design frequency and the system resonating at two new frequencies which are higher and lower than the original design frequency.

To get the system back into resonance, either the transmission frequency, inductance or capacitance should be adjusted. The operating frequency can't be changed because the Rezence operating frequency specification is fixed and the Class E PA is a highly tuned frequency dependent circuit. Changes in the MCR-WPT coil Inductance is dependent on the physical parameters of the coils, and since these parameters are fixed after they are manufactured, they cannot be changed. Therefore, the only method that can be used counteract the effects of frequency splitting and bring the MCR-WPT coils system back to resonance is capacitive changes.

In this thesis, we propose a capacitive tuning method to counteract the effect of frequency splitting using a Maximum Peak Detection and Auto-Tuning circuit. We demonstrate through simulations that the system efficiency can be rapidly improved through this method.

1.3 Contributions of Thesis

This section gives a summary of the original contributions contained in the different chapters of this thesis,

1.3.1 High-Efficiency, Cost-Effective Class E Amplifier Design

This thesis proposes a high-efficiency Class E PA design flow. The design flow modified from [25] to design the Class-E PA at frequencies below 100MHz. The flow allows for rapid CAD design and assessment of Class-E PA using different Power FETs, and supply voltage, duty cycle and output power combinations. By following this flow, a Class-E PA circuit that has a low supply current and high supply voltage, and using a low-cost power FET was design with efficiency. Detailed information on the simulation and experimental setups and results are given

1.3.2 Multilayer Spiral MCR-WPT PSC Design

A new planar spiral MCR-WPT PSC design with multiple layers is put forth in this thesis. Identical copies of the outer resonator coil which are rotated on the Z axis, or mirrored on the X or Y-axis, are placed on subsequent layers. This allows for a simple and symmetric design. Using this design we show that coil SRF is continually reduced with each additional metal layer while maintaining a relatively constant efficiency, and outer length, width and thickness dimensions. We also show that by changing the dielectric substrate material, the SRF can be further reduced with the efficiency kept relatively constant, or the efficiency can be increased with a constant frequency. This makes it possible to design smaller Tx and Rx resonators with high efficiency, making them attractive for smartphone and small Bluetooth device changing applications. Detailed MCR-WPT PSC simulation and experimental setups information and results are provided.

1.3.3 Capacitive Auto-Tuning Impedance Matching Technique for Improved Efficiency

We propose a novel impedance matching auto tuning technique at the PRU of the Rezence system. This technique will both tune the resonant frequency of the coils and impedance match them to the Class E output. We demonstrate that it reduces energy loss through the Class E Power FET due to impedance mismatch and efficiency loss in the coils due to frequency splitting. The novel matching technique includes: (1) a discrete varactor tuning technique which includes a binary counter, MOS switches and discrete capacitor components, and (2) a self-tuning technique which use maximum peak voltage detection circuit composed of a negative voltage level shifter and comparator. Detailed simulation setup information and results are provided

1.4 Thesis Organisation

This thesis presents the newly proposed techniques to improve the overall system efficiency, and is organized in the following order:

Chapter 2 presents the design of the component blocks of the Rezence system architecture. These blocks include the Power Supply, Class-E PA, and Rectifier blocks. The design of a 1:1 isolation transformer, required for the implementation of the auto-tuning system at the PRU, is also included. Particular focus is placed on the new Class-E design flow and the design of a high-efficiency Class E PA. It includes extensive simulation and experimental results

Chapter 3 presents the design of the novel small profile, low SRF, and high-efficiency multi-layer spiral MCR-WPT PSC coils.

Chapter 4 presents the issues associated with MCR-WPT PSC coil systems, mainly frequency splitting. It then explores previous methods used to reduce the effects of this issue and then presents the new auto-tuning method used to counteract frequency splitting and improve efficiency with simulation results provided.

Chapter 5 we conclude this thesis and present future works that could be done for improved results.

1.5 Chapter Summary

In this chapter, we presented an overview of the Rezence standard. The potential benefits of the Rezence standard were discussed as well as the basic building blocks that make up the Rezence architecture were introduced with brief descriptions. A short description of the design challenges associated with PA and MCR-WPT coil design that make it difficult to achieve high-efficiency at 6.78MHz is given. Another issue that was briefly discussed is the frequency splitting phenomenon which causes a decrease in transmission efficiency. New and novel methods used to address these issues by creating a modified design flow that simplifies Class-E PA design, a new multilayer planar spiral MCR-WPT PSC design achieve higher efficiency in small devices, and an auto-tuning design to counteract frequency splitting were presented.

Chapter 2

2 Rezence WPT System Analog Component Blocks Design.

Rezence is the name given to the Airfuel (formerly the Alliance for Wireless Power - A4WP) WPT system standard in 2013 [6]. It is one of two main standards used for WPT in mobile devices, with the other being the WPC Qi standard. Based on the MCR-WPT design introduced in 2007 by a group of researchers from MIT [2], the Rezence WPT standard has the ability to transmit power over short distances. As mentioned in section 1.1.1, it is composed of PTU with a front-end power supply (which include an Oscillator and Gate Driver), an MCU, and Power Amplifier (PA) with impedance matching, and a Tx Resonator. It also has a PRU with an Rx transmitter, a regulator (which includes a rectifier according to [31]), DC-DC converter and an MCU.

We present the selection and design of the PTU and PRU analog blocks within the Rezence WPT system excluding the MCUs, DC-DC converter, and transmitters in this chapter. These analog blocks are the foundational circuitry required for the design and test of the novel MCR-WPT PSCs and Maximum Peak Detection and Auto-Tuning circuits presented in the later chapters of this thesis. The blocks are designed with the Rezence standard operating frequency of 6.78MHz, with the PTU unit between a Class3 and Class4 to supply power to category 4 devices and below.

This chapter presents the design, simulations, and results of the analog component block of the Rezence WPT system. In section 2.1 we cover the specifications and derivations of the Rezence WPT system components. This is followed by the front end oscillator and gate driver selection and design discussed in Section 2.2. Then section 2.3 presents the design methodology, simulations, and results of the Class-E Power Amplifier. Next, the design and simulations of the RF bridge rectifier circuit are presented in Section 2.4. Finally, we conclude the chapter with the design and test results of an RF 1:1 transformer which is required for the implementation of the maximum peak detection and auto-tuning circuitry discussed in Section 2.5.

2.1 Rezence WPT System Blocks Efficiency Specifications.

As mentioned in the chapter introduction, the Rezence WPT system standard is composed of a PTU and PRU, which include an Oscillator, Gate Driver, Power Amplifier, and Rectifier among other component blocks. These blocks, and an additional 1:1 transformer are required for

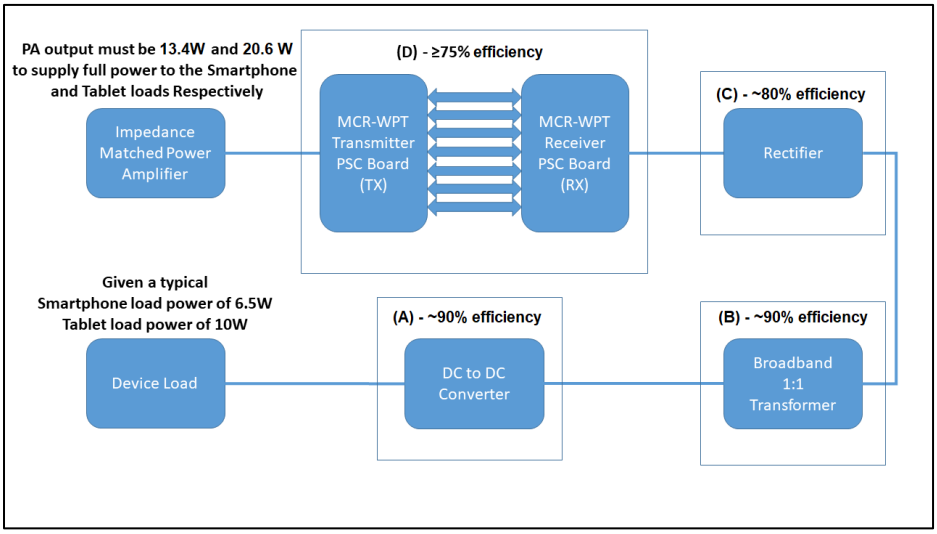


Figure 2.1-1 Rezence system block diagram with block component efficiencies to calculate the minimum output power of the PA.

the design and test of the novel MCR-WPT PSCs and Maximum Peak Detection and Auto-Tuning circuits. Before we go through the selection and design of each block, we must first determine their minimum efficiency specifications.

To determine these specifications, the efficiency of the RWPT system is broken down into 4 main blocks as shown in Figure 2.1-1. The expected efficiencies of each block are then determined by finding the average efficiency of off the shelf components. Then starting from the Device load on the receiver side and working our way backward, we divide the load power by the product of the efficiencies of each system block provided. The output power of the PA was calculated to be 13.4-20.6 Watts as seen Figure 2.1-1.

2.2 Oscillator on Gate Driver Circuitry

The front end of the Rezence standard is composed of a frequency generator and a Class-E power amplifier. The frequency generator circuitry needs to be accurate and stable to meet the 6.78MHz ±15kHz requirement, and be able to supply enough power to the Class-E PA input for it to operate at maximum efficiency. By itself, an oscillator is unable to supply the Class-E PA with enough power. So a gate driver is used to supply the required input power to the Class-E PA. We go through the selection and design of the Oscillator and Gate Driver in this section.

2.2.1 Oscillator Selection and Design

There are many types of oscillator circuit topologies that can be used in our oscillator design. Since our operating frequency is larger than 1MHz, basic RL, RC, and amplifier based oscillators cannot be used. Other oscillator typologies and devices such as crystal, Colpitts, Hartley oscillator, were then looked into. Their benefits and drawbacks I discussed below.

2.2.1.1 Oscillator Selection

Among the three oscillators, crystal oscillators are the best at generating a stable frequency source. This makes them ideal for our application because we require a stable operating frequency. Unfortunately, there are no available discrete crystal oscillator components that operate at our 6.78 MHz frequency for purchase. A 13.56 MHz Crystal oscillator could be used with frequency divider circuits, such as the Miller frequency divider circuit and a digital counter, to achieve our 6.78 MHz frequency. But doing so increases the overall complexity of the circuit.

The alternative Hartley and Colpitts oscillators can also generate relatively stable frequency source. The frequency source's stability is mainly dependant on the type of capacitors used, where np0 and Silver Mica capacitors which are designed for tuning circuits maintain their capacitance value in the presence of higher temperatures and voltages. Both oscillators have the same simple a simple circuit design. They differ when it comes to their resonant tuning tank configuration, where The Hartley tank is composed of two inductors and a capacitor, and the Colpitts tank is composed two capacitors and an inductor, as shown in Figure 2.2-1 (A) and (B) respectively. To calculate the resonant frequency of the Hartley tank we use equation (*2.1*).

$$f_0 = \frac{1}{2\pi\sqrt{\left(L_1 + L_2 + k\sqrt{L_1 \cdot L_2}\right) \cdot C}} \tag{2.1}$$

For the resonant frequency of the Colpitts tank, we use equation (*2.2*).

$$f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)}} \tag{2.2}$$

Due to the simplicity of its design, and the high stability that can be achieved us the Colpitts oscillator was selected for our design. It was chosen over the Hartley oscillator because it is slightly

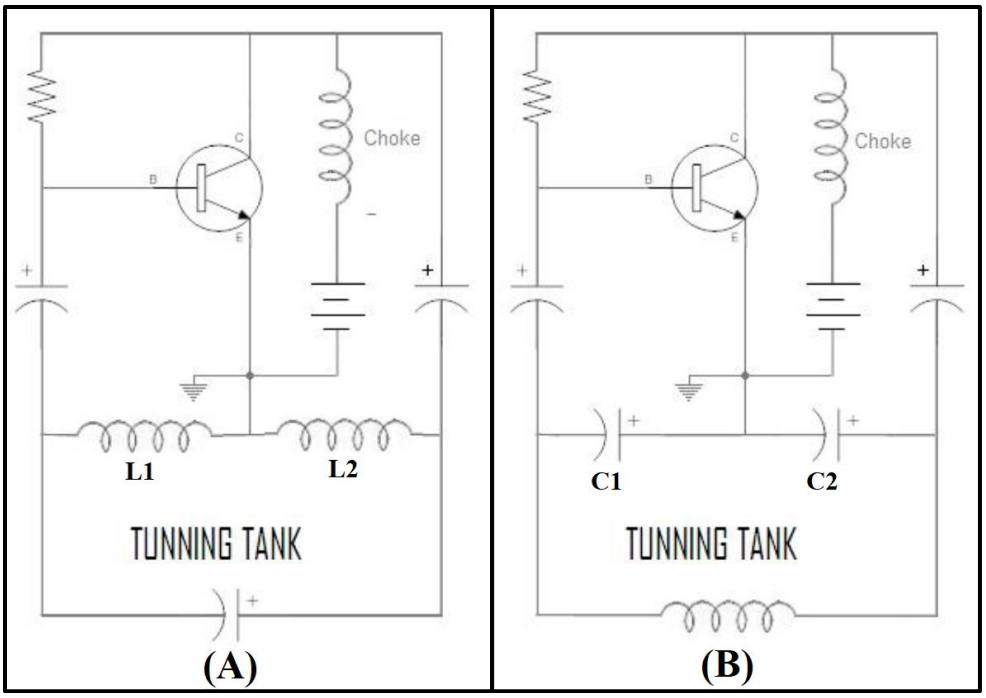


Figure 2.2-1 Circuit comparison between (A) Hartley oscillator; (B) Colpitts oscillator.

easier to obtain capacitors and inductors and the operating frequency equation is also simpler. The design and simulation of the Colpitts oscillator for our application are discussed in the next section.

2.2.1.2 Design and Simulations of the Colpitts Oscillator

Before going through the simulation result, we establish the specifications for the Colpitts Oscillator. The specifications are as follows

- Fundamental Frequency of operation (f) 6.78MHz ±0.015
- Output Power >0.02Watts (~13dBm)

To satisfy the frequency requirement, we selected a 470pF and 460pF capacitors, and a 2.2uH inductor for the tuning tank. A buffer circuit was added at the output to isolate the oscillator circuit and to increase that output power. The PN2222A was used in both circuits with a 18V Vdc, 10nF DC blocking capacitors, and bias resistor values as shown in the schematic in Figure 2.2-2.

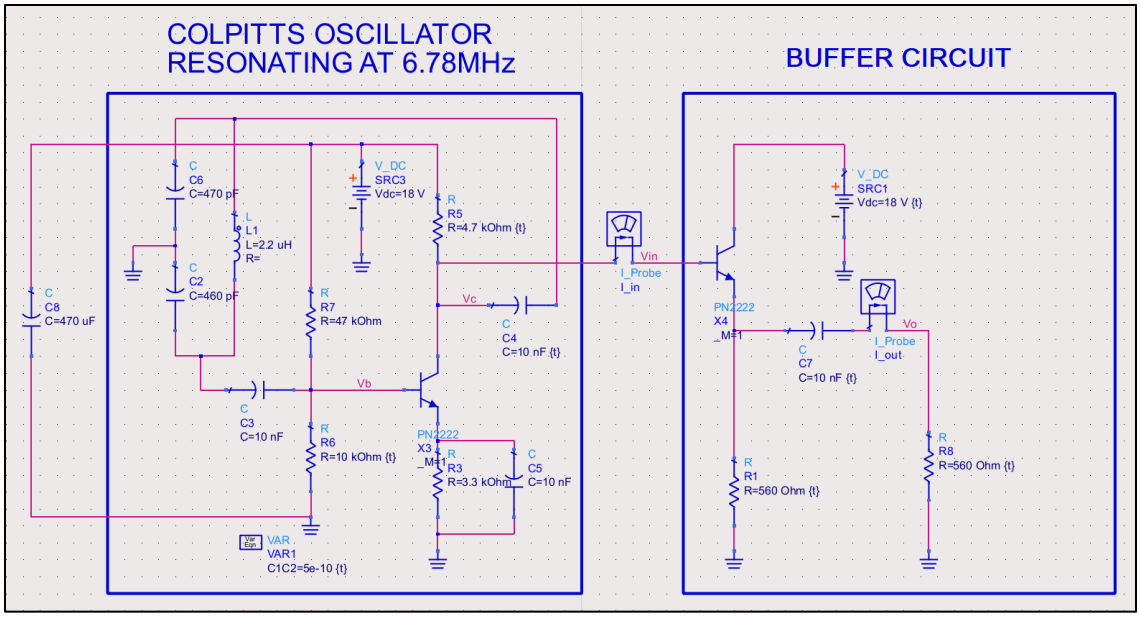


Figure 2.2-2 Colpitts oscillator and buffer circuit schematic in ADS.

A Harmonic Balance simulation was run in Keysight's ADS software to determine the frequency and output power of the circuit. An OscPort component is required to run the Harmonic Balance simulation, and it is placed between the C4 DC blocking capacitor and the resonant tuning tank. The simulation frequency settings tab is set to run with 5 harmonics at the fundamental frequency of 6.78MHz. The oscillator setting tab has the "Enable Oscillator Analysis" selected and the Method is "Use OscPort". All other tab settings are left with their default values.

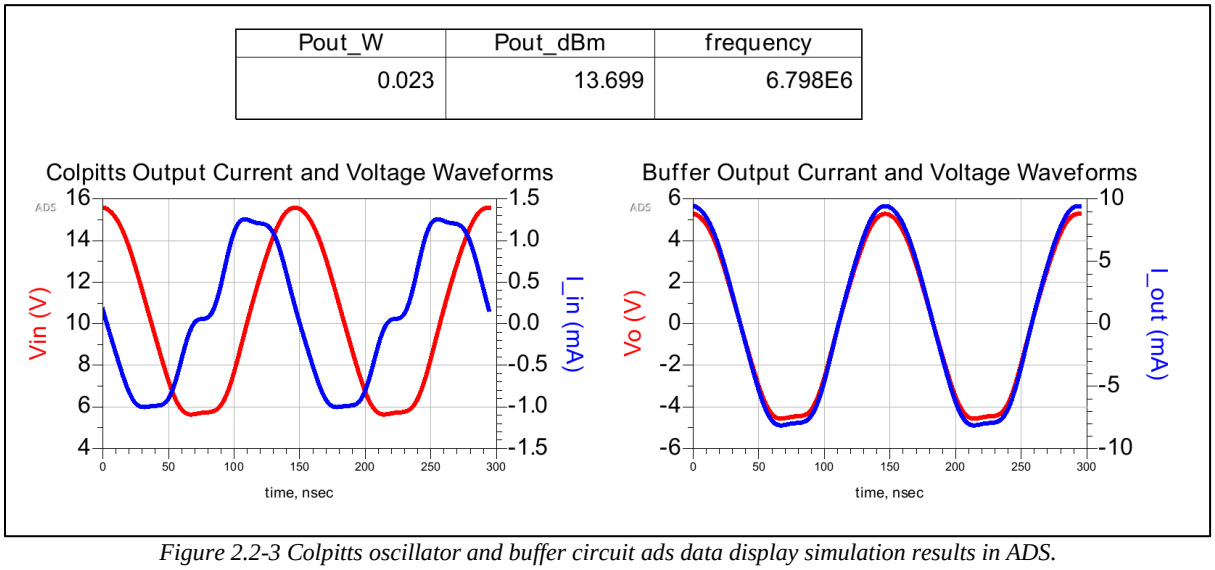


Figure 2.2-3 Colpitts oscillator and buffer circuit ads data display simulation results in ADS.

The resulting Waveform, operating frequency, and output power are in Figure 2.2-3. With this design we achieve an output power of 13.7dBm and a resonant frequency of 6.798MHz. These values are slightly above our specifications. An experimental PCB prototype was constructed as seen in blue in Figure 2.3-11. It is seen that there were some harmonic ripples at the outputs of the Colpitts and buffer circuits from the simulation plots. Therefore, a series RL circuit was put at the output of the buffer, before the gate driver on the PCB board, to remove these high-frequency components. Test measured test results showed that a frequency of 6.78MHZ was generated.

2.2.2 Gate Driver Circuit Selection and Design.

Gate driver circuits are required to supply enough current to the input of switch mode PAs so that they can operate correctly. The reason for this is the PA transistor gate requires sufficient current, to supply the input gate capacitance with the required charge to turn the transistor ON and OFF fast enough, such that it acts like a switch. The type of gate driver used depends on the gate charge and the type of input waveform of the Class-E PA, which we investigate below.

2.2.2.1 Gate Driver Selection

There two types of gate drivers used for switch mode PAs, an input a square wave or an input a sine wave. Sine wave gate drivers are used when impedance matching is required, and square wave gate driver when impedance matching is not necessary. Both of these gate drivers should have a large enough output power to turn the transistor gate ON and OFF fast enough.

Square wave gate drivers are more common in low-frequency applications. These gate drivers are commercially available or they can be designed from scratch. The selection of the correct device depends on the power handling and peak drive current specifications of the device

as described in [32]. They require an input square wave for their correct operation. Therefore an intermediate circuit is needed in between the oscillator and the gate driver to transform the sinusoidal oscillator output, to a square wave gate driver input. Commercially available devices like the Schmitt trigger are designed for this purpose. This addition of this component slight increase the circuit complexity.

Sinusoidal gate drives are usually used in RF and microwave applications where impedance matching is required, and high current square waves are more difficult to create at these frequencies. Many types of PAs can be used for this purpose, and since the use a sinusoidal input, they can be placed between the oscillator buffer output and the Class-E input without additional components. Power Amplifiers can be purchased commercially or be designed from scratch.

Both types of gate driver were tested on the input of the Class-E PA. The square wave pulse with a varying resistor was applied directly to the Class-E input, and a sine wave port with the varying power was connected to an input impedance matched Class-E PA. They were simulated to determine which gate driver allowed the output impedance matched Class-E PA to operate with a higher efficiency, which resulted in the selection of and the sinusoidal gate driver.

2.2.2.2 Design and Simulation of the Class-AB Gate Driver

Before going through the simulation result, we establish the specifications for the PA. The specifications are as follows

- Fundamental Frequency of operation (f) 6.78MHz ±0.02
- Output Power >2Watts (~33dBm)
- Efficiency >50%
- Output Resistance 27Ω ±2Ω

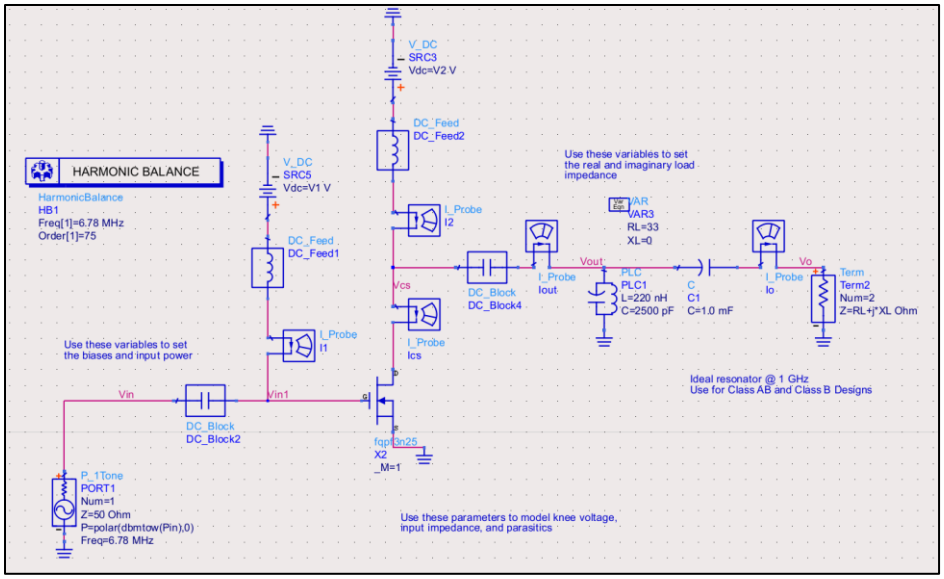


Figure 2.2-4 Class-AB gate driver schematic in ADS.

To satisfy the efficiency requirement, a Class-AB design was used. The FQPF3n25 power MOSFET was used in the Class-AB design. The Keysight ADS design methodology and workspace presented in [33], was used to design the Class-AB PA. The Class-AB PA simulation schematic is shown in Figure 2.2-4. The V1 gate bias voltage and V2 supply voltage are 4V and 18V respectively. The high Q parallel LC resonator circuit is placed on the output to short circuit all higher harmonic components and ensures that a sinusoidal output waveform appears. The input power was varied between 10dBm and 15dBm

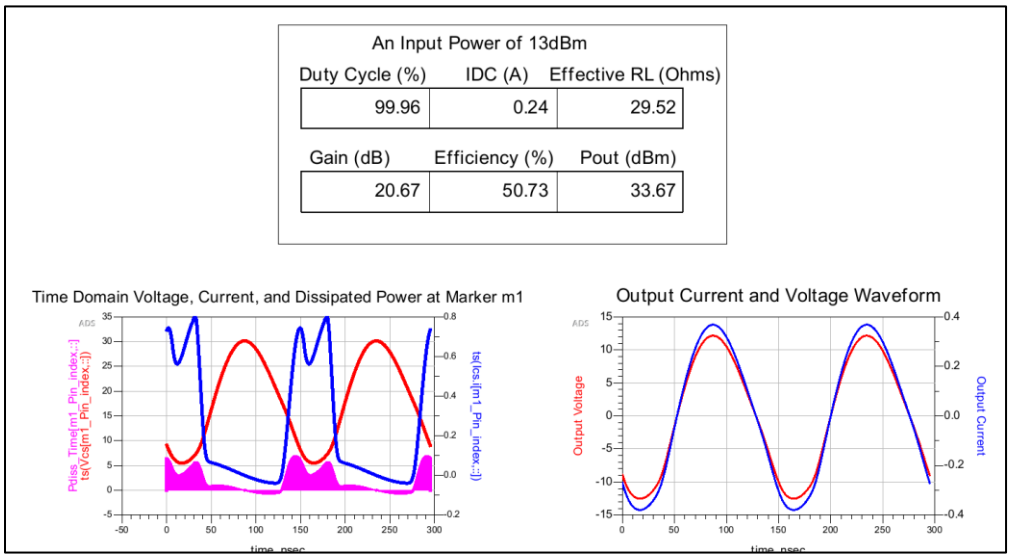


Figure 2.2-5 Class-AB gate driver simulation data display results in ADS.

. A Harmonic Balance simulation was run in ADS to determine the efficiency, output power and effective output resistance of the circuit. All tab settings for the workspace were obtained from [33] and were left with their default values. These results as well as the Output and Drain current and voltage Waveforms for a 13dBm input sinusoid are in Figure 2.2-5. With this design, we achieve an output power and efficiency of 33.7Bm and 50.73% respectively which meets our targets nicely. The Effective load resistance of 29.52Ω with this input power is slightly above our target and will affect the efficiency of the Class-E amplifier which is impedance match to 27Ω. Since this resistance changes with respect to the input power, a variable resistor is connected between the buffer LPF and the Class-AB input, to adjust the resistance at the cost increasing or lowering the output power.

2.3 Class-E Power Amplifier with High Efficiency.

A Power Amplifier (PA) is required to power up the MCR-WPT coils system so that enough power can be supplied to the load. According to [34], there are two main types of PAs. The controlled conduction angle amplifiers are the first group of PAs which is composed of the common amplifier classes A, B, AB and C PAs. These PAs are defined by the length of their conduction state over some portion of the output waveform, from completely ON to completely OFF. The other group is the switch mode amplifiers which include most other PA classes. These PAs use digital circuits and pulse width modulation (PWM) to constantly switch the signal between “fully-ON” and “fully-OFF” driving the transistor output hard into the saturation and cut-off regions. Among these switch-mode PAs is the Class-E amplifier, which has a 100% theoretical efficiency.

Due to its high efficiency, the Class-E PA power loss is low, and most of the power goes to the Transmitter MCR-WPT PSC coils. Also, the fundamental load of the Class E PA is inductive, which is good for driving WPT coils. For these reasons, the Class-E is used as the PA within our Rezence MCR-WPT System. But the complete design equations of the Class-E derived in [24] are not compact, which makes it difficult to design this PA. So in this section, we go through the basic operation of a Class-E amplifier. Next, we briefly go through the design flow obtained from [25], used to design the Class-E. Then the discrete electronic component design limitations are discussed. Finally, the Simulations and Experimental results Class-E and the Power transmitter unit from the oscillator to the Class-E output are presented.

2.3.1 Class-E Amplifier Basics and Theory

As mentioned above, the Class-E amplifier has a potential theoretical efficiency of 100%. It was first proposed in [23], and a detailed analysis was done in [24]. In order for a high-efficiency design is to be made, a basic understanding of how it works, the reasons for its circuit topology, and some basic design equation is needed. We go through these basics in this section.

2.3.1.1 Switch Mode PA Operation and Topology

The Class-E amplifier is a switch mode amplifier, which means that the Power FET is used as an ON-OFF switch. The basic switch-mode PA operates as follows. When the switch is closed AC current flows into the switch, and when it is open current flows into the load causing a voltage. The operation of this PA and resulting current and voltage waveforms are shown in Figure 2.3-1. With this topology, square voltage and current waveforms are generated at the switch. A theoretical efficiency of 100% would be expected, but in reality, the maximum efficiency is ~81% [25], which is due to losses from all other odd harmonics besides the fundamental.

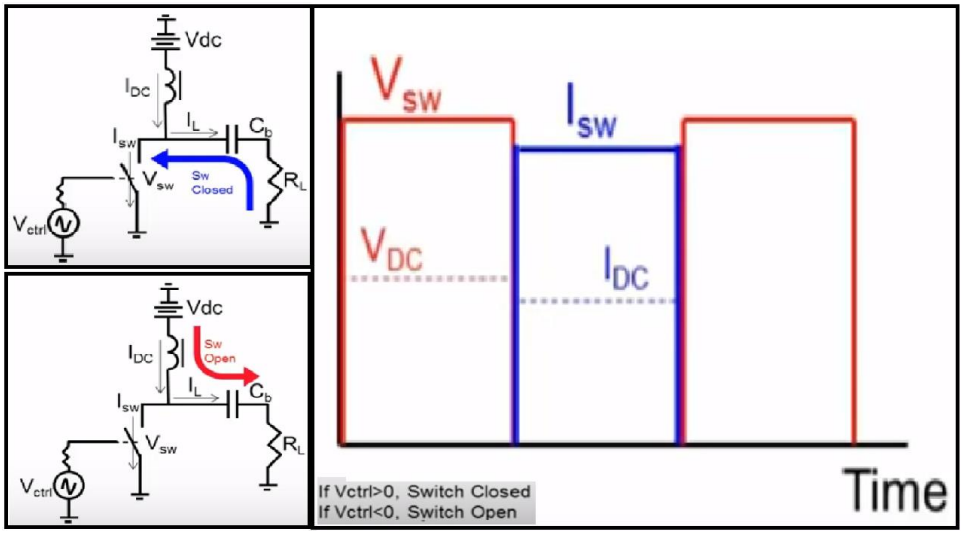


Figure 2.3-1 Ideal basic switch-mode PA circuit, with current and voltage waveforms from [25].

2.3.1.2 Class-E Operation and Circuit Topology

The Class-E PA improves on this design adding a series resonator at the output, a capacitor in parallel with the switch, and an inductor in series with the resonator. Its circuit topology is shown in Figure 2.3-2. The resonator acts like a short at the fundamental frequency, and an open at all other harmonics. This ensures that a sinusoidal waveform flowing throughout the circuit when the switch opens and closes. When the switch is closed, AC current flows from the resonator through the switch, and when the switch is open, current flows from the capacitor in parallel with

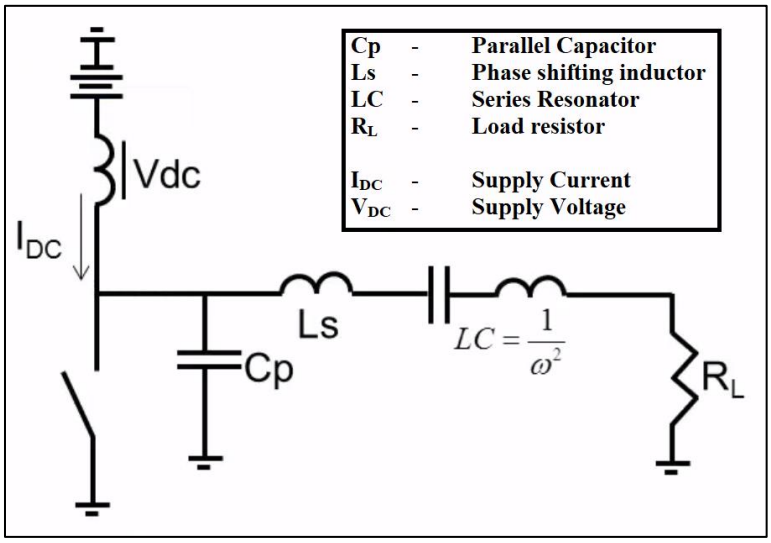


Figure 2.3-2 Ideal Class E circuit topology [25].

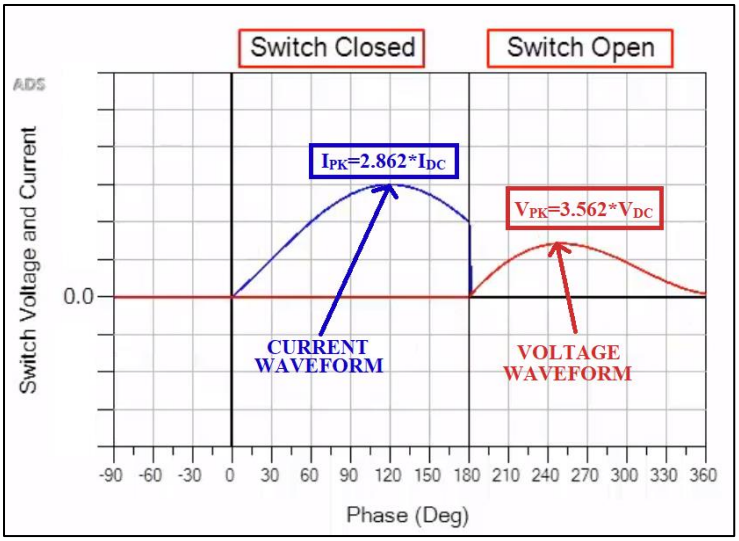


Figure 2.3-3 Ideal 50% duty cycle Class-E switch voltage and current waveforms, with the peak voltage and current values [25].

the switch back into the resonator. Finally, the series inductor is used to phase shift the current waveform.

To understand the purpose of the series inductor, we need to look at the voltage (**V**) and current (**I**) boundary conditions of the switch's opening and closing points. At the closing point, the voltage across and current through the transistor must be ZERO (**V**=0 and **I**=0). This is where the biggest potential for high current draw occurs. At the switch open point, only the voltage must be ZERO (**V**=0) since no current will flow from the switch. Since current waveform at the switch is a DC offset sinusoid, the series inductor is used to phase shift the current to ensure it is ZERO (**I**=0) at the switch closing point. Figure 2.3-3 shows the current and voltage waveforms at the switch.

2.3.1.3 Class-E Design Equations at 50% Duty Cycle

The design equations for a Class-E PA with a 50% duty cycle was derived in [23]. A theoretical efficiency of 100% can only be achieved using this duty cycle. Before we can determine the switch parallel capacitance (C_P) and phase shift series inductance (L_S) values, the supply

voltage (V_{DC}), power FET output knee/on voltage (V_{knee}), output power (P_{out}), and operation frequency (f) parameters must be determined beforehand. Using V_{DC}, V_{knee}, and P_{out} parameters, the output resistance (R_L) can be calculated using (*2.3*).

$$R_L = \frac{0.577 \cdot (V_{DC} - V_{knee})^2}{P_{out}} \tag{2.3}$$

After determining R_L, it is used with the f to determine the C_P and L_S, where $\omega=2\pi f$

$$C_P = \frac{1}{\omega R_L \cdot 5.447} \tag{2.4}$$

$$L_S = \frac{1.1525 \cdot R_L}{\omega} \tag{2.5}$$

Using these equations, the Peak current and voltages swings were derived in [23]. They are large multiples of the supply current and voltage, as defined in Figure 2.3-3. These large drain values significantly limit the available transistors devices selection that can be used for Class-E design.

2.3.2 Class-E Design Methodology

The above equations could be used exclusively to design 50% duty cycle Class-E PA. But they have severely limited design capabilities s, as no insight given as to how the predetermined parameters used are selected. They also ignore other important design parameters which must be considered when designing a realizable Class-E PA. This section briefly describes the design methodology presented in [25] using Keysight's ADS software, to design the Class-E PA.

2.3.2.1 Additional Parameter Effects on Class-E PA design,

Before using going through the design flow, we first discuss the effects of additional parameters on Class-E PA power FET selection. Besides the V_{DC}, V_{knee}, P_{out}, and f, other parameters other such as the maximum currents and voltage, and intrinsic drain capacitance of the power FET directly determines whether the transistor can be used in a design. The switching duty

cycle of the Class-E, which can be less than 50%, also indirectly determines if the transistor can be used. These effects are examined below.

When designing a Class-E PA, the most important factors which decide whether a power FET can be used in a design are its absolute maximum ratings. The peak drain-current and voltage swings of the 50% duty cycle Class-PA are large multiples of the input supply current and voltage in Figure 2.3-3. Therefore, they limit the range of reliable power FET devices that can be used in the design. The power FET must be within the safe operating device limits for reliable use.

Another design factor to be considered is the intrinsic device output capacitance (C_{DEV}) as it determines if a power FET could be used within the design. The C_{DEV} is combined with an external capacitor to meet the theoretically determined C_p. From equations (*2.3*) and (*2.4*), C_p is directly related to the predetermined V_{DC}, V_{knee}, P_{out}, and f values. Any increase in f or V_{DC}, or decrease in V_{knee} or P_{out}, decreases the C_P capacitance needed to collect charge from the DC supply and supply current to the resonant circuit so that switching conditions for Class E operation are met. If C_P is continually decreased by these parameters, there comes a point where $C_{DEV} > C_P$. At this point, Class E operation can no longer be achieved using this power FET in the design.

Finally, the duty cycle of the Class-E PA is the other factor that should be considered, as it directly determines the peak drain current and voltage swing values of the power FET. At 50% duty cycle, theoretical peak drain current and voltage swings are their largest, and 100% efficiency can be achieved. There are times when the design requires a specific power FET. If the FET cannot operate reliably with a 50% duty cycle due to peak drain current and voltage swings exceeding the device's absolute maximum ratings, a smaller duty cycle could be used at the cost of a reduced maximum efficiency. Generalized Ideal Class-E PA design equations that include duty cycle are given in [24], but they are lengthy, which makes them difficult to use for theoretical analysis.

2.3.2.2 Class-E PA Design Flow

First, a fixed operating frequency needs to be specified. Then a range of acceptable supply voltages and output powers, and a variety of possible power FETs are determined. Next, the knee voltage, device intrinsic capacitance, and the maximum supply currents and voltage of each power FET are taken from its datasheet. These parameters are then entered into the ideal Class-E PA synthesis tool in [25] which uses the equations from [24]. The V_{DC} and P_{out} parameters are adjusted next to assess whether intrinsic device capacitance is less than C_P so that Class-E operation can be achieved, and that the FET device will work within its safe operating limits. Finally, the V_{DC} and P_{out} parameters are tweaked to obtain readily available discrete R, L and C component values.

Next, verification is then run on an ideal circuit shown in Figure 2.3-4. The resulting R, L and C values generated from the synthesis tool are used for the passive circuit components, and the power FET V_{DC}, V_{knee}, f, C_{DEV} and duty cycle values are used in the ideal switch as seen in the red box of Figure 2.3-4. A Harmonic Balance simulation with 75 harmonics is then run to verify the efficiency, and time domain drain current and voltage waveforms shown in Figure 2.3-5 (a).

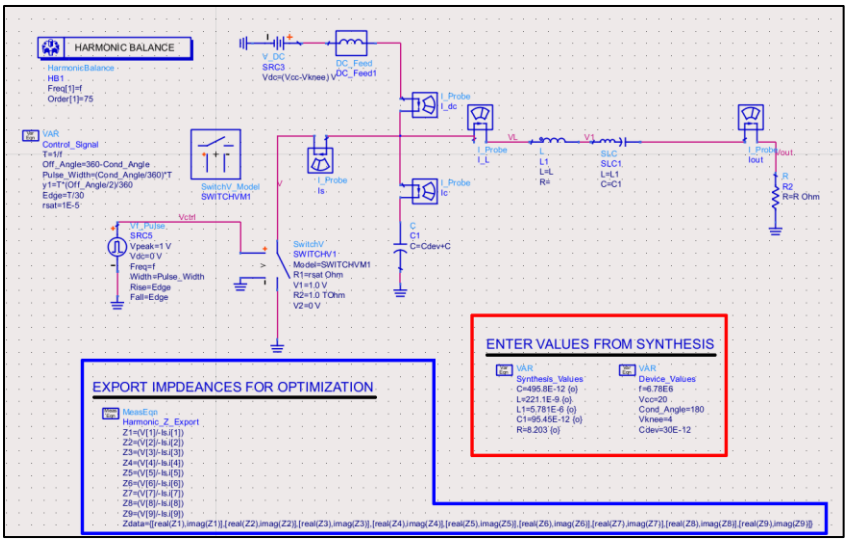


Figure 2.3-4 Ideal Class E verification schematic in ADS.

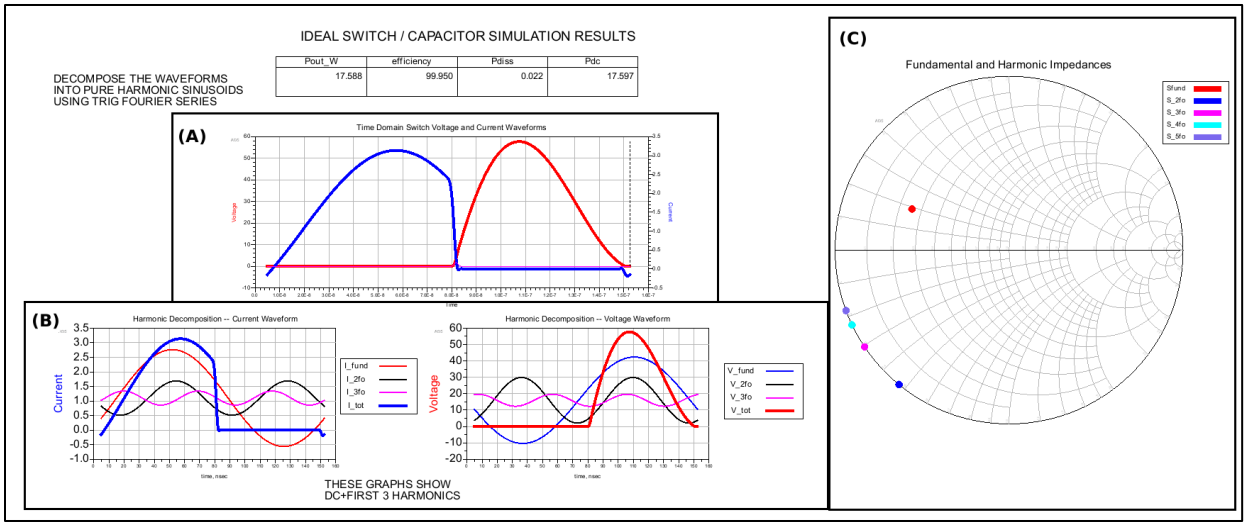


Figure 2.3-5 Ideal Class-E harmonic balance simulation data display results in ADS: (A) time domain drain voltage and currents; (B) time domain drain current and voltage harmonics; (C) frequency domain harmonic impedances.

These waveforms at the drain of the FET are subsequently broken down into their fundamental and harmonic frequency components using Fourier analysis by doing a Harmonic Balance simulation. The resulting time domain current and voltage harmonic waveforms are seen in Figure 2.3-5 (b). The currents and voltages are then used to obtain the respective ideal frequency domain impedance components, that generate the time domain drain current and voltage harmonic waveforms found through Fourier analysis. These impedance components are obtained using the

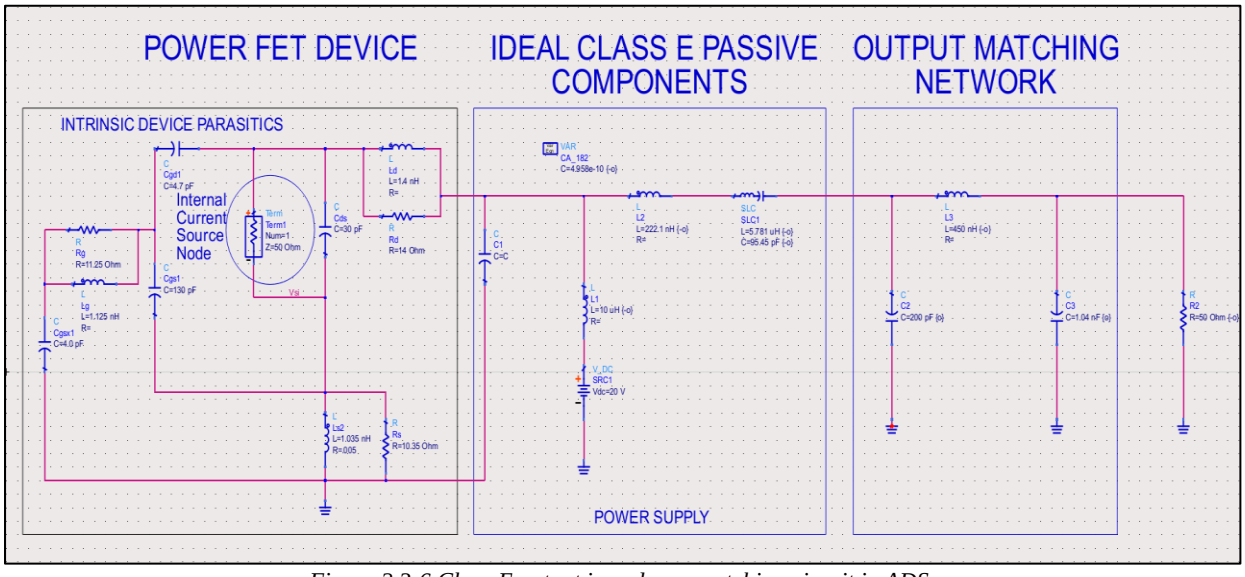


Figure 2.3-6 Class-E output impedance matching circuit in ADS.

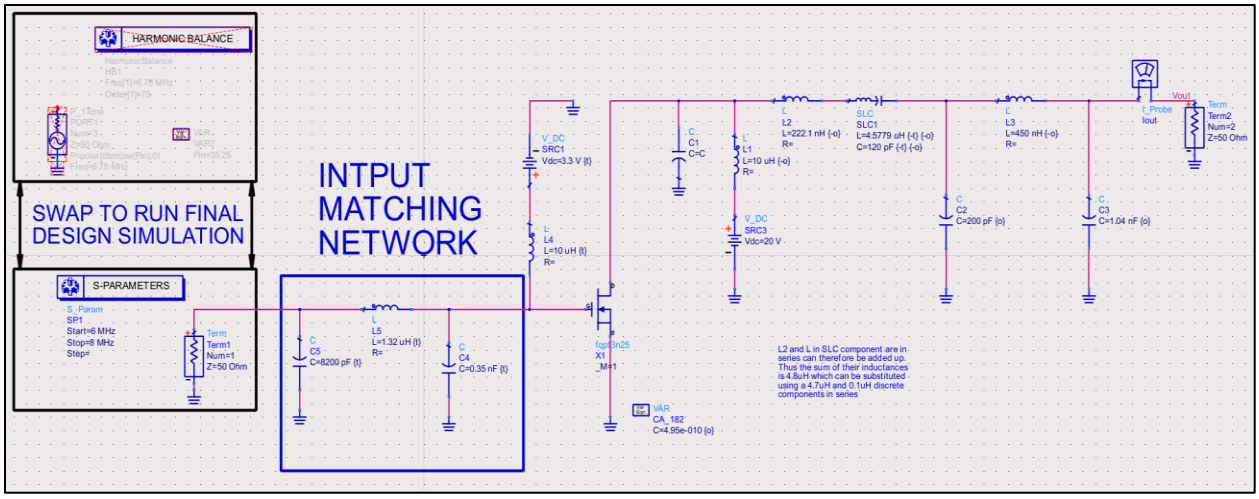


Figure 2.3-7 Class-E input impedance and final circuit design schematic in ADS.

equations bounded in blue in Figure 2.3-4, and the smith chart harmonic impedances are in Figure 2.3-5 (c). Usually, only the first 5 harmonics are needed to get close to the ideal Class-E waveform.

Using these ideal harmonic drain impedances as a target, output impedance matching is done on the real FET device. To do this the power FET spice model is first imported into ADS. The FET BSIM3 (or LEVEL 3) model is then removed and replaced with a term component so device parasitics could be used in the impedance match analysis. We note that since our operating frequency is below 100MHz by more than one order of magnitude, discrete capacitors and inductors close to the ideal Class-E circuit values can be used with little concern with parasitic impedance shifts due to trace lengths, shapes, etc. Therefore the respective V_{DC}, f, L and C values of the ideal Class-E are added to the circuit. Finally, a π or T matching network is added between the output of the resonator and a 50Ω load resistor. The resulting schematic is shown in Figure 2.3-6. Four S-Parameter simulations are done at the fundamental, second, third and fourth Harmonic frequencies with the fundamental frequency set to 6.78MHz, and the π or T matching network components are varied using Optimisation and/or Tuning to achieve smith chart harmonic drain impedances that are close to the ideal target values in Figure 2.3-5(c).

After the output impedance matching is complete, the input is impedance matched. The input impedance matching is an optional step since it is only required when a sine wave is used, as the Class-E input can be driven by either a square or sine wave. A π or T matching network is placed at the input gate terminal of the power FET, and the gate biased adjusted to achieve the desired switching duty cycle. The resulting circuit is shown in Figure 2.3-7. An S-Parameter simulation is run with a frequency range from 6-8MHz, and a step size of 1kHz. All other settings were left at the default values.

Finally, a Harmonic Balance simulation is done on the final circuit design which is the same as Figure 2.3-7, except for port component is used instead of a term component as the input. The simulation frequency settings tab is set to run with up to 500 harmonics with the fundamental frequency of 6.78MHz. In the Initial guess tab, “transient assisted harmonic balance” is set to "on", and the “harmonic balance assisted harmonic balance” is set to "on". In the solver tab, the “convergence mode” is set to "basic (fast)", the “max duration” is set to" robust", the “solver type” is set to "direct", and the “matrix re-use” is set to "robust".

The Class-E efficiency and time domain current and voltage waveforms at drain are then verified from the simulation results. If the efficiency is below the desired values, either V_{DC} or P_{out} values can be adjusted, or a new device selected, and go through the design flow again. A flowchart of the complete design flow is presented in Figure 2.3-8.

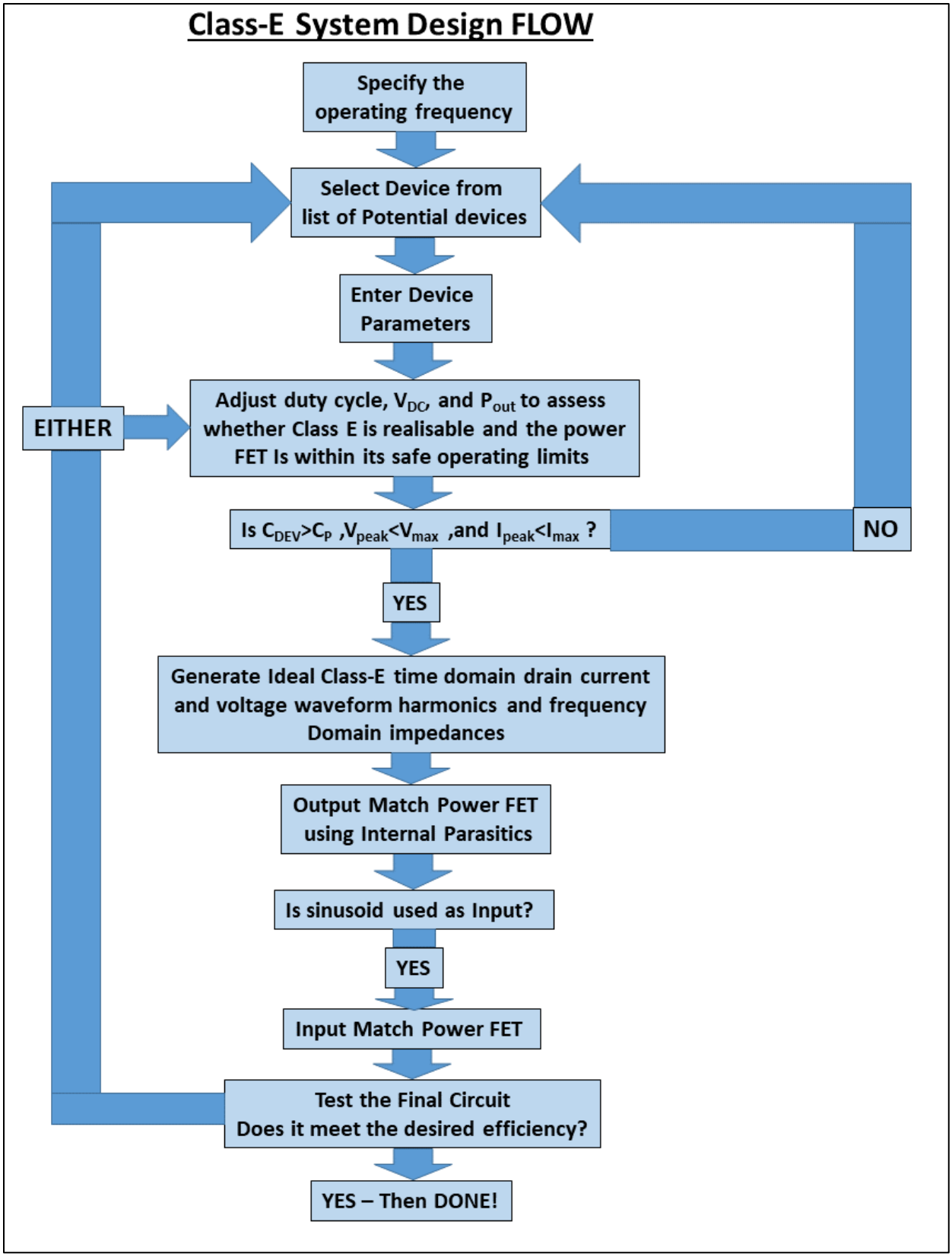


Figure 2.3-8 Class-E Design Methodology Flow Chart.

2.3.3 Other Class-E Design Considerations

Besides the design parameters mentioned in 2.3.2.1, there are other factors that should be considered when designing the Class-E PA. These factors include the power FET power dissipation limits and temperature, passive component tolerances and available discrete values, capacitor maximum currents and voltages, inductor maximum current and SRF, quality factor and electronic component costs. The effects of these factors are briefly explained below.

Power dissipated through Power FET transistors is converted to heat, which increases the operating temperature. Operation temperature levels should be maintained since the FET performance is greatly affected by temperature changes. An increase in device temperature increases the FET on-resistance which affects V_{knee} but decreases maximum current and power dissipation limit capabilities, which are part of the device's safe operating limits. So reducing device heating due to power loss is required to avoid these issues. Thermal calculations for heat sinking and device power dissipation limits need to be considered

- The tolerances and values of passive electronic components are standardized within the industry. The Class-E amplifier is a tuned circuit, so any deviation from the Class-E design passive component values could result in significantly lowered efficiency. So it is desirable to have capacitors and inductors with very low tolerance, especially at the resonator circuit. The available discrete passive component values are proportional and/or inversely proportional to the V_{DC} and P_{out} used in the Class-E. It's important to achieve a design where the simulation values as close as possible to a single or combination of discrete component values, to obtain the highest efficiency

Capacitor absolute maximum current and voltage ratings determine the peak drain voltages which could be as high as 2.8 and 3.5 times the supply current and voltage. The voltage rating

should be twice the expected maximum value to account for voltage spikes. The current rating of capacitors is important for the Class-E resonator capacitor, as it needs to handle the large currents flowing through the output. The maximum current rating is not usually included in the component datasheet but can be calculated using equation (*2.6*) for up to 500kHz taken from [35].

$$I = 2\pi \cdot V_{AC} \cdot f \cdot C \tag{2.6}$$

From equation (*2.6*), smaller the capacitors have a smaller maximum current handling capability. For higher frequencies, the temperature rise due to power dissipation determines the maximum current. These specifications can be obtained by request from the manufacturer. So, the maximum current rating should be twice the expected maximum current to ensure component reliability.

Inductors maximum current rating and SRF must be considered when designing the class-E. The choke, phase shifting, and resonator inductors should all be able to handle the large drain currents which could be as high as 2.8 times the supply current. So maximum current values should be at least double the expected maximum current to ensure component reliability. All inductors have an SRF due to parasitic capacitances in between its turn wire. At frequencies larger than the SRF, the inductor behaves like a capacitor. It is therefore important that the SRF of the selected inductors is well above the fundamental operating frequency so that the inductor does not behave as a capacitor at the higher harmonics, which would degrade Class-E efficiency. The range of available inductors is heavily dependent on the current rating and SRF. There are very few inductor values with a large maximum current and SRF. So it is important to keep the Class-E I_{DC} low, by using a large V_{DC}, to increase the range of available discrete inductors

Quality (Q) factor and cost are the other factors affecting Class-E PA design. The Q factor is the measure of stored energy vs lost energy in capacitors and inductors. So higher Q factor

components are desired for higher efficiency operation. Inductors generally have lower Q factor than capacitors, so they are the limiting factor. The device and component costs are determined by their tolerances, absolute maximum ratings, capacitor stability, and inductor resonant frequency, among other things.

2.3.4 Class-E PA Specifications, Simulations and Experimental Result

2.3.4.1 Class-E Design Specifications

Before going into the simulation setup, we establish the specifications for the Class-E PA design. The specifications are as follows

- Overall Class-E Specifications
    - Fundamental Frequency of Operation — 6.78MHz ±0.5MHz
    - Efficiency — >70%
    - Duty Cycle — 50%
    - Output Power — 12.7-19.6 Watts
    - Supply Voltage (V_{DC}) — 24V, 36V, or 48V
    - Supply Power Maximum rating — >35 Watts
- Power FET Specifications
    - Drain-source breakdown voltage — $>(2V_{DC}\bullet 3.6)$
    - Maximum DC current — >1A
    - Power Dissipation — >20 Watts
- Capacitors and Inductors
    - Tolerance — ≤2%
    - Maximum current — >1A

- Quality Factor 50
- Capacitor breakdown voltage >($2V_{DC}$•3.6)
- Inductor SRF >68MHz

The overall design specifications were met using a V_{DC} of 36V and P_{out} of 20Watts. With this configuration, the largest efficiency was achieved with an I_{DC} ~= 0.6A. This lower I_{DC} was important since it increased the range of available discrete inductors for the design. The power supply is rated at 60 Watts.

After using the design flow in (Figure 2.3-1) with multiple power FETs, the IPP50R190CE power MOSFET was selected. It has a 550V maximum drain-source voltage which is larger than the ($2V_{DC}$•3.6) resulting V_{peak} of 259.2V. A maximum current of more than 15A, Power Dissipation above 100Watts is well above the specification values. A sinusoidal gate driver provided better efficiency that a square wave gate driver, so the power FET was input matched.

Both the inductors and capacitors had a current rating above 1A and tolerances of either 1% or 2% depending on availability except for the choke inductors. The capacitors had a voltage rating of 500V, and the SRF of all the inductors were above 100MHz, which meet the specifications.

2.3.4.2 Simulations Results

The final design parameters are summarized in Table 2.3-1, and the design schematic in Figure 2.3-9. The input impedance is matched to 27Ω simplify the Class-AB gate driver design. The input C7 capacitor is large since it doubles as the Class-AB output DC block. The inherent C_P-internal capacitance of the IPP50R190CE MOSFET is not shown in the schematic. The C_P-external and L_{shift} components are the C1 capacitor and L2 inductor values respectively. The C_{res}

Table 2.3-1 Class-E PA final design parameters.

Parameter	Value (experiment value)
Ideal Class Parameters	
V_{DC}	36V
C_P-external	68pF
C_p-internal	68pF
L_{shift}+L_{res}	15uH
C_{res}	39pF
Output Matching Network	
C2	470pF
C3	620pF (150+470)
L3	500nH
Input Matching Network	
C6	2750pF (1600+820+330)
C7	10nF
C8	220pF
L6	500nH
Miscellaneous	
Choke Inductors (L1 and L4)	15uH
Input bias voltage	3V
Input Power	2Watts
Input impedance	27Ω

and L_{res} are the SLC1 (series inductor and capacitor component) capacitor and inductor values. Finally, there were no single discrete C3 and C6 capacitor value available, so they were made by adding multiple capacitors in parallel as shown in brackets in Table 2.3-1.

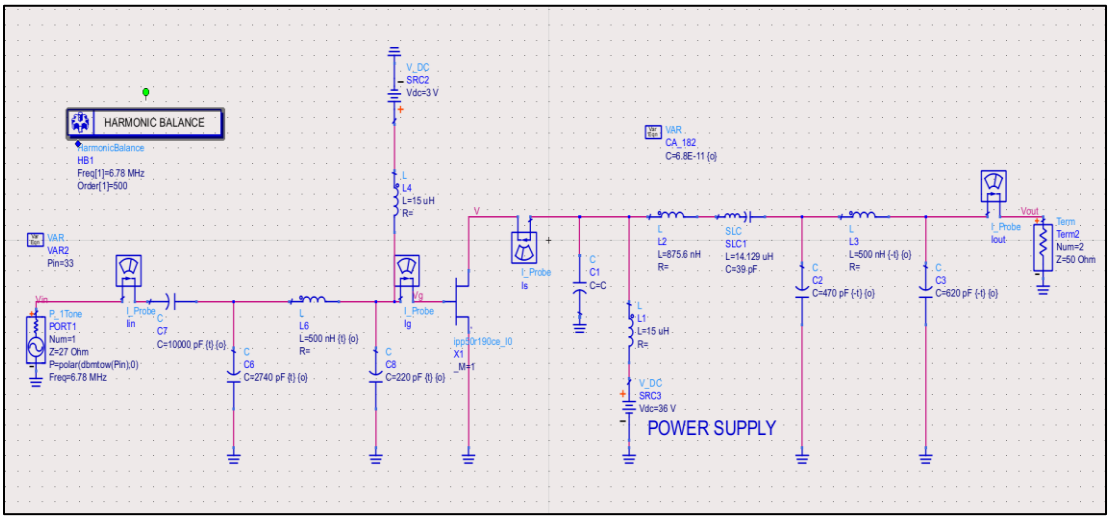


Figure 2.3-9 Class-E final design schematic in ADS.

Pout_W	efficiency	Pgain	Idc	Pdc
17.913	89.818	14.905	0.554	19.943

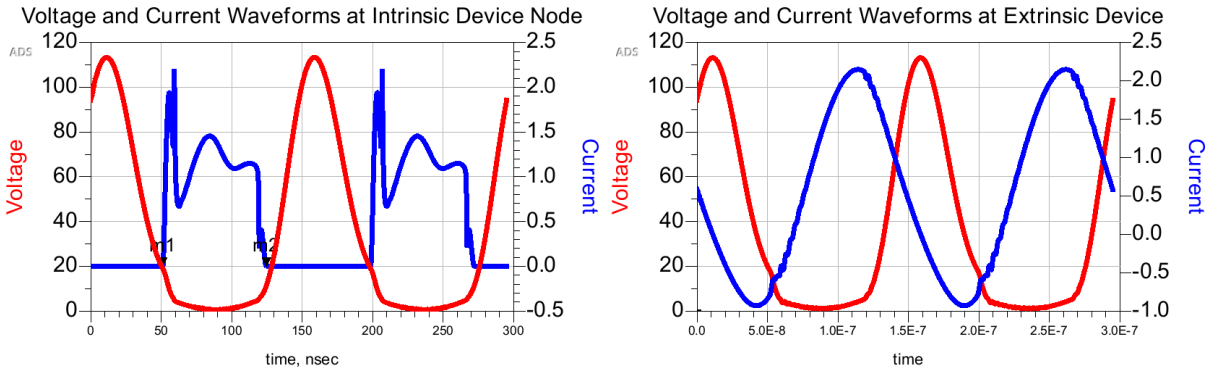


Figure 2.3-10 Simulation data display results of the Class-E Design done in ADS.

A Harmonic Balance simulation was run on the schematic in Figure 2.3-9 using the setting specified as follows. The simulation frequency settings tab is set to run with up to 500 harmonics with the fundamental frequency of 6.78MHz. In the Initial guess tab, “transient assisted harmonic balance” is set to "on", and the “harmonic balance assisted harmonic balance” is set to "on". In the solver tab, the “convergence mode” is set to "basic (fast)", the “max duration” is set to" robust", the “solver type” is set to "direct", and the “matrix re-use” is set to "robust".

The simulation results are shown in Figure 2.3-10. The results show that an efficiency of 89.9% was achieved with this design, with a DC current of 0.554A. Besides some current ripple at the device’s intrinsic drain node, the current and voltage waveforms at the acts like a high-efficiency class-E.

2.3.4.3 Experimental Results and Discussion

The Class-E experimental setup used a double layer PCB shown in Figure 2.3-11. It is composed of the Colpitts oscillator, buffer and low pass filter circuit in blue. The Class-AB driver circuit in Red, which has a blue variable resistor at its input, which is used to adjust Class-B gate

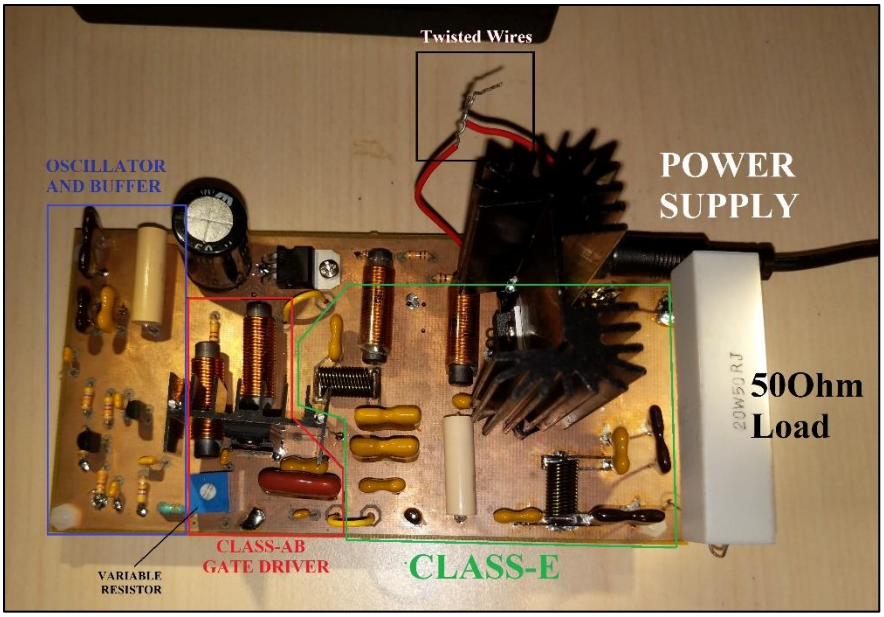


Figure 2.3-11 Class-E PCB experimental test circuit.

driver to provide sufficient input power to the Class-E. The Class-E PA outlined in green is connected to a 20watt 50Ω output load resistor. A 36V DC desktop power supply was used as the input power, and the twisted wires connected to a DMM4050 to measure the DC current of the PA. All other measurements were done with the MSOX3024A oscilloscope

The measurement results are shown in Table 2.3-2. The results show that an efficiency of 71% was achieved with this design, which has a DC supply current of 0.69A. The final design meets our efficiency specification.

The efficiencies of simulation and measured results vary from one another. To determine the cause of this difference, the capacitances of all the Class-E capacitor components were measured to check their actual value. It was found that the 39pF C_{res} capacitor with a 2% tolerance had a measured capacitance of 40pf. This value was plugged into final design schematic and the

Table 2.3-2 Class-E PA measurement results.

Measurement	Results
Output Peak voltage	$42V_{peak}$
Input DC Current	0.69A
Efficiency	71%

Harmonic Balance simulations were rerun. The simulation result showed that the efficiency drops by more than 10%, which suggests that this a major part of the reduced efficiency.

2.4 High Frequency, Power Rectifiers

The rectifier circuit in the Rezence WPT standard is used to convert the output RX Resonator AC power to DC. In this section focus on the Bridge Rectifier circuit design. This circuit topology is chosen due to its simplicity of implementation and good efficiency. We go through the design parameters the must be considered in its design. Then we discuss types of diodes that were considered with benefits and drawbacks. Finally, we show the simulations and experimental results of the finalized circuit and discuss possible alternatives.

2.4.1 Rectifier and Diodes Basics and Considerations

The bridge rectifier with a filter capacitor was chosen due to its high efficiency and simplicity of implementation. Ideally, with reference to Appendix E, this rectifier is shown to have a maximum efficiency of ~81% without a filter capacitor. But with the addition of the filter capacitor in parallel with R_L, efficiencies of 84% and higher have been reported [36] [37]. To get these high efficiencies, the parasitics of the diodes have to be taken into consideration, because at higher frequencies their effects are no longer negligible.

Before we go through the effects of the diode parasitics, the desired behavior of our diodes for high efficiency had to be determined. We wanted the diode to act as close to the ideal diode as possible. According to ideal rectifier equation in *(E.3*), we needed the series resistance (R_s) to be near 0. We also needed the Reverse Recovery Time (τ_{rr}) and the Reverse Junction Capacitance (C_j) to be zero. With these characteristics established we can now analyze the parasitic effects.

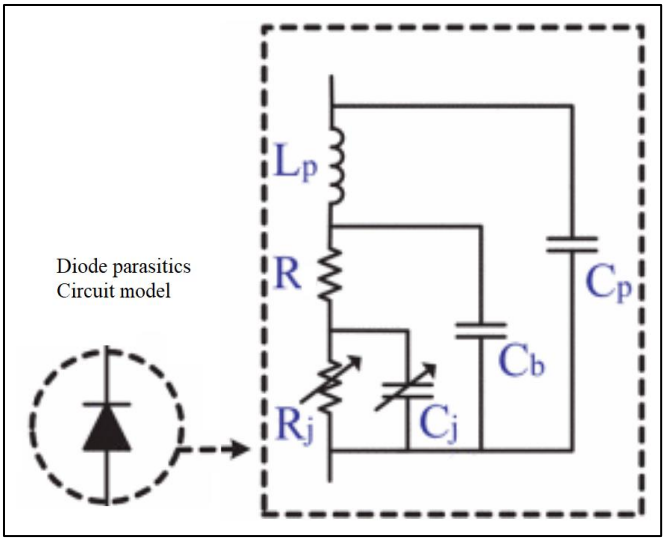


Figure 2.4-1 Model of a real diode parasitics [36].

2.4.1.1 Reverse Junction Capacitance (C_r)

One of the main parameters of concern in selecting a diode is its reverse junction capacitance (C_r). In Figure 2.4-1 we see the diode capacitance is composed of a fixed device package capacitance (C_p) and bond-wire capacitance (C_b), as well as a variable junction capacitance (C_j). The reactance equation for C_r is defined as follows

$$X_c = \frac{1}{2 \cdot \pi \cdot f \cdot C_r} \tag{2.7}$$

Ideally, the diode capacitance Cr = 0. From (2.9) this leads to a reactance $X_c \rightarrow \infty$. Therefore from Figure 2.4-2, assuming R_f is negligible, all the AC signal would go to the filter capacitor (C_{filter}) and R_L. In reality, nearly all diodes have a finite variable capacitance Cr, which is dependent on the reverse voltage (Vr), as can be seen in a typical diode datasheet show in Figure 2.4-3. Since the capacitance decreases for increasing V_r.

Ignoring the variability of C_r and using the highest capacitance (~710pF) with a 6.78MHz operating frequency, and plugging the values into *(2.7)* we get $X_c \approx 33\Omega$. Since C_r shunts both the large C_{filter} capacitance and 50 Ω R_L resistance, using *(G.4)* we get the current ratio through C_r to

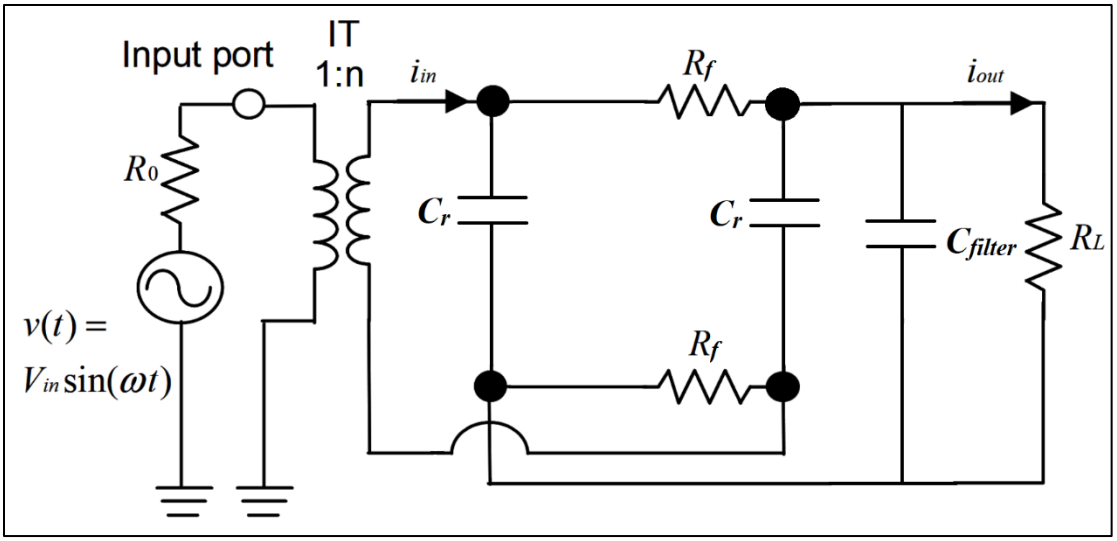


Figure 2.4-2 Rectifier with parasitic forward resistance and reverse capacitance and filter capacitor.

be $I_r/I_{eq}\approx 60\%$. This means most of the i_{in} input current is shunted to ground by C_r and any charge on C_{filter} is discharged to ground through C_r, resulting in a small current going through R_L. So to get 90% or more of the current to go through R_L, using *(G.4)* X_c should be at least10 times R_L.

2.4.1.2 Diode Reverse Recovery Time (t_r)

Diode reverse recovery time is another factor that affects the performance of real diodes. From [38], the reverse recovery time is the amount of time a diode or rectifier takes to discharge

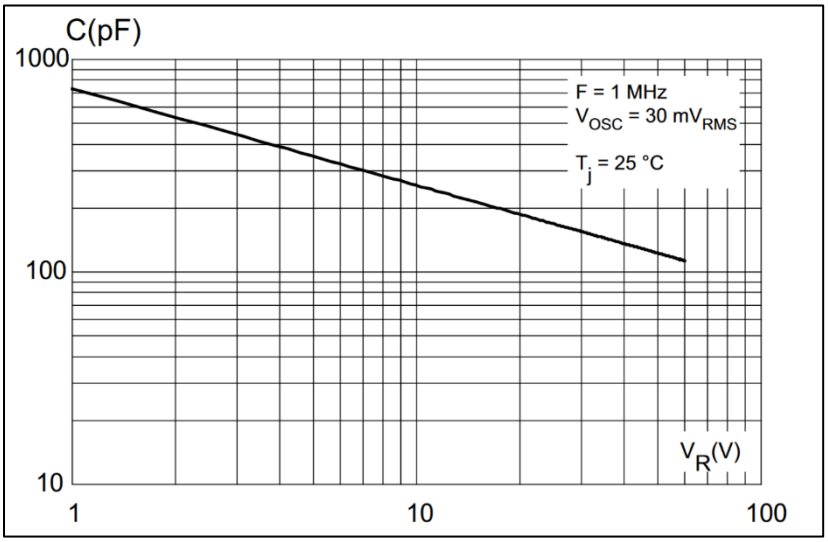


Figure 2.4-3 Typical junction capacitance for stps5l60 Schottky diode [39].

the stored charge when switching from the conducting to the blocking state. We know that for a bridge rectifier, the reverse bias time (t_r) of the diodes defined as

$$t_r = \frac{1}{2 \cdot f} \tag{2.8}$$

Using these facts, for any frequency, t_{rr} needs to be substantially t_r. To have 99% blocking time, we would need $t_r \geq 100 \cdot t_r$.

2.4.1.3 Forward Resistance (R_f)

As shown in Figure 2.4-1, the diode series resistance R_s is a series combination of a fixed resistor R due to lead and packaging resistances, and a variable junction resistor (R_j). We can further break down R_j into its forward-bias resistance (R_f) and reverse resistance. The reverse resistance R_r is assumed to be infinity due to the low leakage current. Following from Figure 5.2-14 from Appendix E, the forward resistance (R_f) is defined as follows

$$R_f = \frac{V_f}{I_f} \tag{2.9}$$

From *(2.9)* we see that R_j is a function of I_f since the forward voltage drop (V_f) relatively constant when the diode conducts. Therefore to minimize losses due to heat caused by R_j during the conduction cycle, V_f needs to be, as low as possible.

Finally, the maximum voltages and currents going through the device need to be no more than 70% of its absolute maximum rating. In other words, the Peak, RMS and DC reverse voltages and forward currents, need be below the device maxima so as to avoid the reverse barrier breakdown surge currents and excessive overheating respectively. Another parameter that should also be considered is the reverse leakage current.

2.4.2 Types of Rectifier Diodes

There were 3 main types of rectifier diodes that were considered, namely Silicon PiN, Schottky, and SiC (Silicon Carbide) Schottky diodes. Each has their benefits and drawbacks and we will go through them individually.

2.4.2.1 Silicon PiN Diode

Silicon PiN diode is made up of heavily doped P and N regions, with an intrinsic semiconductor region in between [40]. They are used for a large range of frequencies and applications. They can support large reverse voltages and forward currents which make them good for power rectifier applications. All of these types of diodes have a t_{rr} that should be taken into consideration. Their C_j values range widely depending on device structure and application. When selecting one for high power RF rectification applications, they should be specified as ultrafast PiN diodes or have their t_{rr} value specified in the datasheet.

2.4.2.2 Schottky Diode

Schottky diodes are composed of a metal coming into contact with moderately doped n-type region [41]. Unlike PiN diodes, they have virtually no t_{rr} due to the minority carrier charge effects in the metal. They also have a lower V_f than PiN diodes. The C_r of these devices is comparable to PiN diodes so they should be taken into consideration.

2.4.2.3 Silicon Carbide (SiC) Diode

Silicon Carbide (SiC) diodes are Schottky diodes that use SiC semiconductor instead of silicon [42]. Like regular Schottky diodes, that have virtually no t_{rr}. Their C_j values are generally lower, and the V_r much higher when compared to the other diodes, which make them ideal for high

power switch mode applications [43]. On the flip side, due to their current high power niche applications, their V_f is the highest of the three in lower power applications.

2.4.3 Simulations and Results

Before using the design considerations mentioned in the previous section, we establish the specifications for the bridge rectifier with filter capacitor. The specifications are as follows

- Fundamental Frequency of operation (f) 6.78MHz
- Maximum DC forward current (I_F) 1.2A
- Maximum reverse voltage (V_R) 40V peak or ~28Vrms
- Reverse recovery time (tr) $<1/(100 \cdot f)$
- Reverse junction capacitance (C_r) $<1/(2 \cdot \pi \cdot f \cdot X_c)$ where $X_c = 250\Omega$
- Forward voltage (V_f) <1V
- Efficiency 70%

To satisfy these requirements, we selected the CSD01060 SiC diode from Wolfspeed. Inc. The datasheet parameters [15] are listed in Table 4 1. From Table 4 1 we see that the maximum C_r

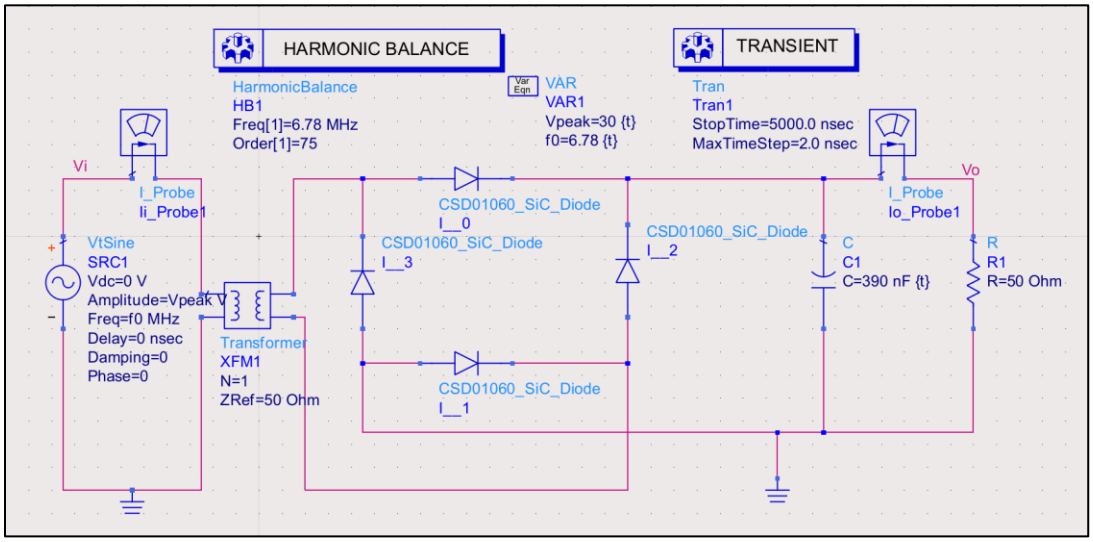


Figure 2.4-4 CSD01060 SiC diode bridge rectifier ADS schematic test bench.

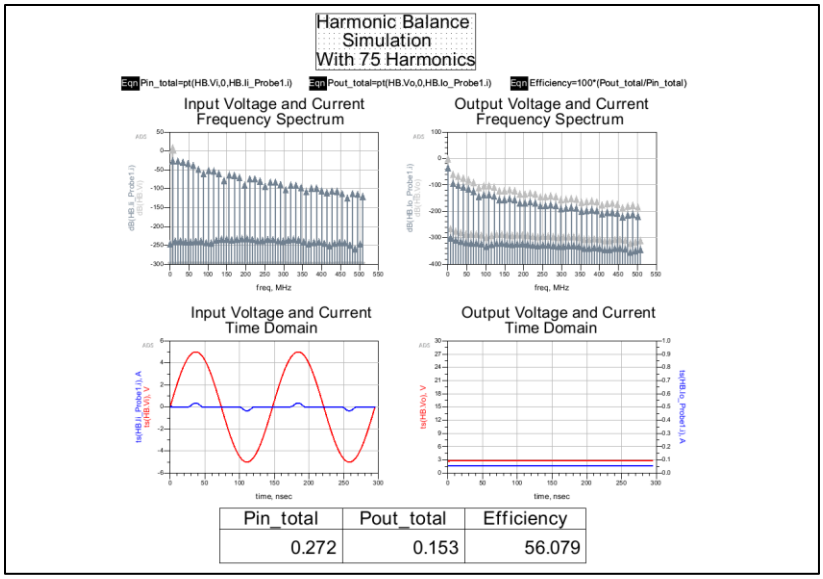


Figure 2.4-5 5V input signal simulation data display results for the CSD01060 SiC diode bridge rectifier.

or 45pF at V_R = 4V. Plugging this value into (*2.7*), we get $X_c \approx 520\Omega > 250\ \Omega$, which meets our specification. With an I_F = 4A, a V_R = 600V, and $t_r \approx 0$s (inherent to SiC diodes), the diode meets these require specifications. The only parameter that is not met is the V_f which can have voltage values up to 2V. This large V_f value would affect the efficiency of the bridge rectifier, particularly for smaller AC voltage peaks.

To check the effects of the large V_f on the bridge rectifier, a Harmonic Balance simulation was done in Keysight's ADS software. The schematic of the test circuit is provided in Figure 2.4-4. The csd01060 component is the spice model of the SiC diode obtained from Wolfspeed's website. The transformer component is ideal, with a 1:1 ratio and 50Ω impedance. Harmonic Balance simulations were run on the circuit to generate the frequency spectrum of the input and output currents and voltages. The simulation frequency settings tab is set to run with 75 harmonics at the fundamental frequency of 6.78MHz. All other tab settings are left with their default values. To calculate the efficiency, the built-in pt() function was used to calculate the RMS power of input and output frequency spectrums. Two simulations were performed at the expected lowest and highest input peak voltages of 5V and 30V respectively to compare the efficiencies.

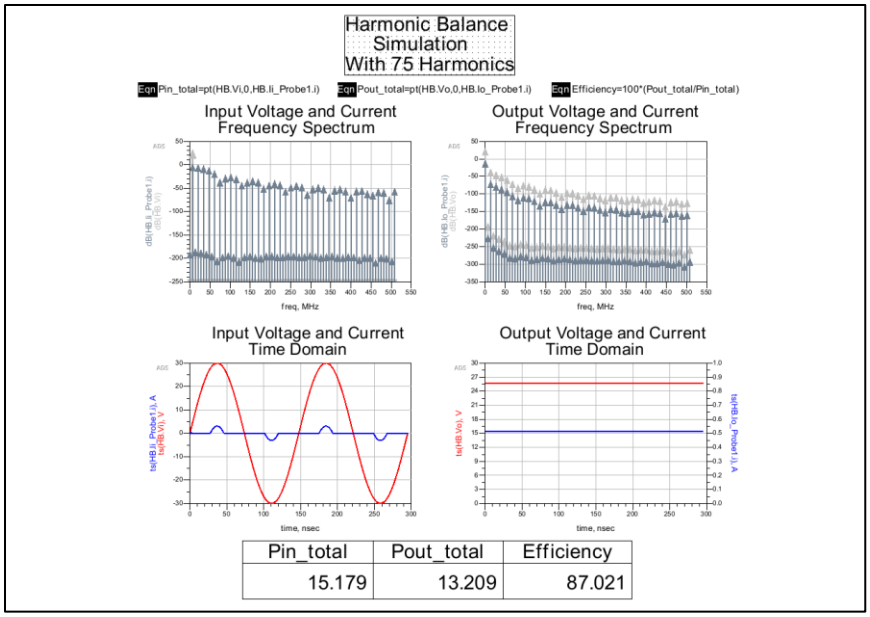


Figure 2.4-6 30V input signal simulation data display results in ADS for the CSD01060 SiC diode bridge rectifier.

The 5V and 30V peak voltage simulations are shown in Figure 2.4-5 and Figure 2.4-6 respectively. The of the 5V peak simulation is 56% and the efficiency of the 30V simulation is 87%. As suspected, the efficiency is much lower when the input signal is small, and this can mainly be attributed to the large V_f voltage of the device.

On another note, the rectifier efficiency could not be calculated as shown in (*2.10*)

$$\eta = \frac{V_{outDC} \cdot I_{outDC}}{{V_{INpeak}}^2/(2 \cdot 50)} \tag{2.10}$$

The reason it won't work is that the input current is composed of multiple harmonic resulting in a non-sinusoidal periodic function.

Table 2.4-1 CSD01060 SiC diode datasheet parameters.

Parameter	Value	Specification
maximum C_r @ V_R = 4V	45pF	100pF
I_F	4A	1.2A
V_R	600V	40V
t_r	0s	1.47ns
V_f max	2V	1V
Efficiency (from simulation)	Vin peak = 5V -> 56% Vin peak = 30V -> 87%	70%

2.5 Broadband DC Isolation Transformers

Transformers are used in many areas of electrical and electronics engineering. They are simple to implement and can be designed to provide DC isolation, EMI suppression, impedance matching, and specific current and voltage ratios [44] [45]. For these reasons, they are found in Power, Broadband, Pulse and Impedance matching applications in a broad range of industries.

In this section, we will go through the design of a DC Isolation Transformer. According to Figure 1.1-2 of in section 1.1.1, transformers are not part of the Rezence specification. It is however required for the implementation of the auto-tuning method which will be described in section 4.2.1 of this chapter. During the design of the auto-tuning portion of the system, we found that there were no available isolated transformers components available for purchase that met our specifications. Because of this, we had to design the transformer ourselves. Therefore, this section will go through the theory and considerations used to design the Isolation transformer as described in [44] and [45], as well as the physical testing and results.

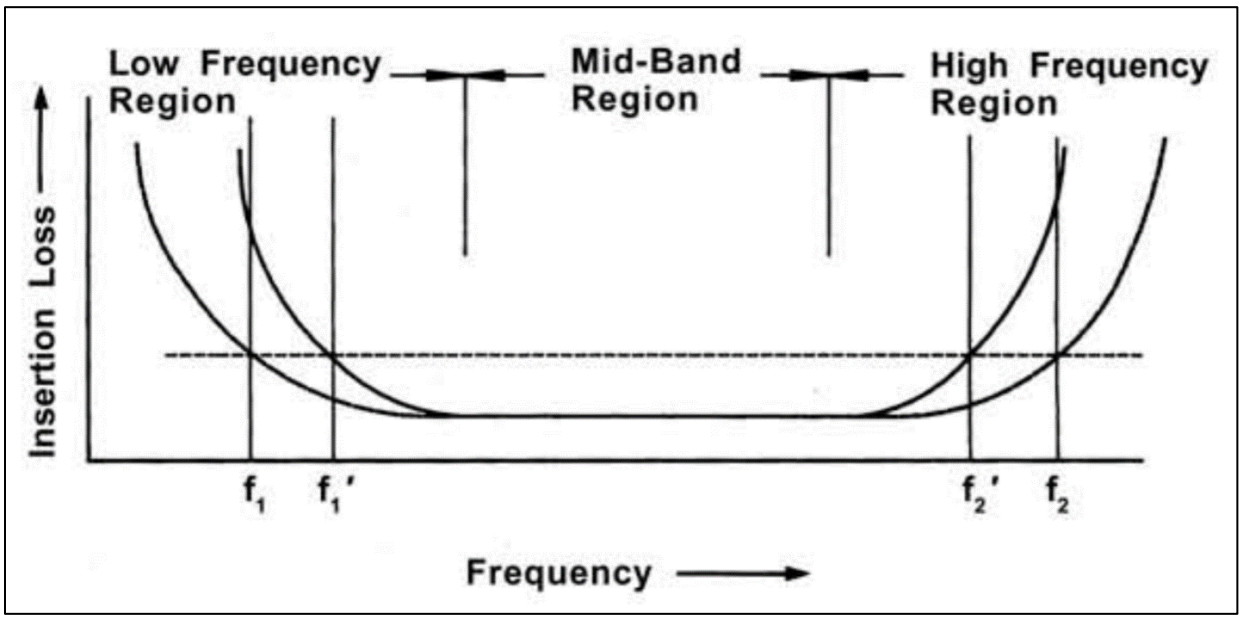


Figure 2.5-1 Typical broadband transformer insertion loss vs frequency characteristic curve [44].

2.5.1 Isolation Transformer Theory and Considerations

Broadband transformers are wound devices used to transfer energy [44]. As shown in Figure 2.5-1, the typical insertion loss characteristic curve of broadband transformers is broken down into 3 regions, the Mid-Band Frequency region where $f_1 \leq f \leq f_2$, the Low-Frequency region $f < f_1$, and the High-Frequency region $f > f_2$. The transformer bandwidth is defined as $f_2 - f_1$ and is a function of the transformer transfer function steepness and the specified insertion loss. The lumped circuit element schematic diagram for the transformer and its simplified circuit model is shown Figure 2.5-2 Transformer equivalent circuit models: (a) Lumped model; (b) Simplified model. Using these models, we can determine the factors that affect the frequency regions.

2.5.1.1 Low-Frequency Region Considerations

When $f < f_1$, the low-frequency attenuation is caused by the lowering of the shunt impedance. This attenuation is caused by the shunt inductance L_p, the load resistance R_b', and the

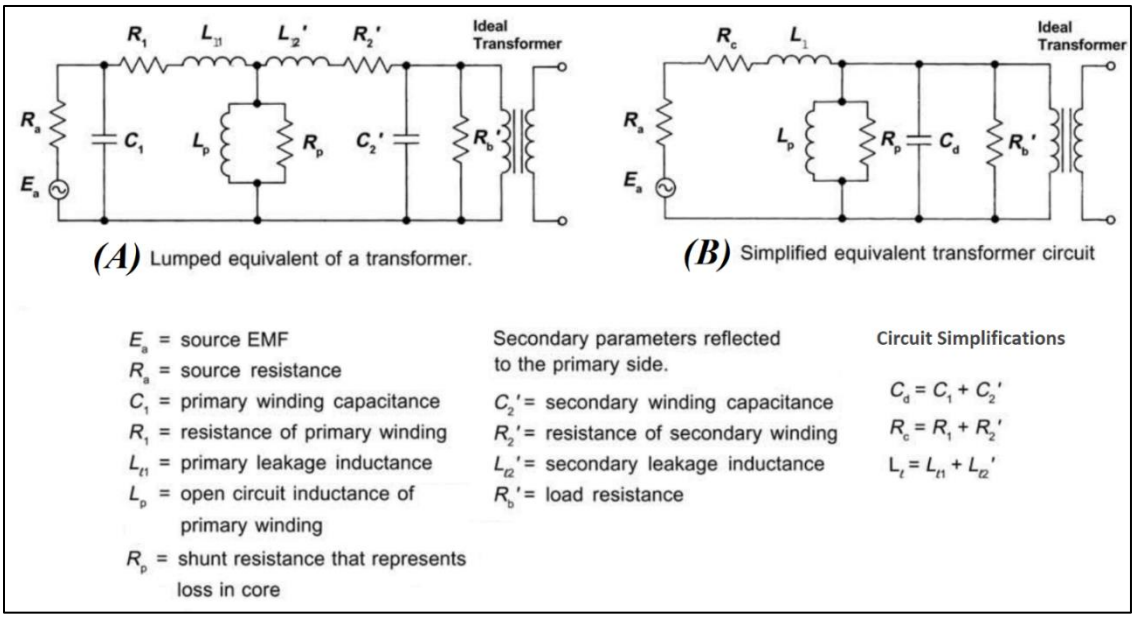


Figure 2.5-2 Transformer equivalent circuit models: (a) Lumped model; (b) Simplified model [44].

shunt resistance R_p. R_p is very small at low frequencies is neglected and attenuation defined as

$$A = 10 \cdot \log_{10}\left(1 + \left(\frac{R_b{}'}{(\omega L_p)}\right)^2\right) dB \tag{2.11}$$

where A is the attenuation. The impedance mainly a function of L_p since the load is usually fixed. As can be seen, with decreasing frequency, the attenuation level increases.

2.5.1.2 Mid-band Region Considerations

When $f_1 \leq f \leq f_2$ in the Mid-Band region, transmission is affected mainly by the resistances R_c in the transformer windings defined in Figure 2.5-2. These losses are determined mainly by the resistance due to the skin effect at the fundamental frequency which is discussed in section 3.1.4.3 and defined in (*3.8*). This loss can be calculated as shown in *(2.12*).

$$A = 20 \log_{10}\left(1 + \frac{R_c}{R_a + R_b{}'}\right) dB \tag{2.12}$$

2.5.1.3 High-Frequency Region Considerations

In the third region where $f > f_2$, the high-frequency attenuation is caused by leakage inductance L_l and shunt capacitance C. These are defined as follows.

$$A = 10 \log_{10}\left(1 + \left(\frac{\omega L_l}{R_a + R_b{}'}\right)^2\right) dB \tag{2.13}$$

$$A = 10 \log_{10}(1 + (\omega CR)^2)\ dB \tag{2.14}$$

Another factor mentioned in [45] that must be taken into consideration is the complex permeability of the inductive core of the transformer. The core permeability is defined by real and imaginary parameters μ'_s μ''_s, which are used to calculate the series inductance and series resistive loss of the core material as defined in [46] and shown below

$$L_s = \mu' L_0 \quad R_s = \omega \mu'' L_0 \tag{2.15}$$

The parameter L_0 is defined by the core shape which could be toroidal or multi-aperture. In general for all ferromagnetic materials, at low frequencies μ'_s is larger than μ''_s, but as the frequency increases μ''_s becomes the dominant parameter, which is supported by the equations in (*2.15*).

2.5.1.4 Other Considerations

Other isolation transformer design parameters taken into consideration, are the transformer core material types and core shapes, and the temperature effects on the core material. There are many magnetic core materials used to design transformers at low frequencies such as iron and steel. But at frequencies where losses due to eddy currents become more significant, ceramics ferrites are preferred. Core shapes vary depending on the application. For higher frequency transformer applications, toroidal and multi-aperture cores seen in are recommended [44]. Changes in temperature cause changes in the core material's permeability. At high temperatures, the material can lose its magnetic properties. This is known as the Curie temperature.

2.5.1.5 Considerations Summary

In summary, the f_1 and f_2 frequencies, the number of turns, wire winding thickness, the core shape and the changes in temperature the device will be exposed to, are the factors to consider in high-frequency transformer design. To reduce insertion loss at f_1, materials with the highest μ''_s at f_1 should be selected. The number of windings should be minimized to reduce leakage inductance and parasitic capacitances. In the mid-band region, due to the resistive losses caused by the skin effect, the frequencies of operation and the amount of current that the transformer is required to support should be taken into consideration to determine the wire windings size. Finally, Toroidal and Multi-aperture cores shapes are preferred for high-frequency transformers.

2.5.2 Isolation Transformer Design, Testing, and Results

Before using the design considerations mentioned in the previous section, we establish the specifications for the DC Isolation transformer. The specifications are as follows

- Fundamental Frequency of Operation 6.78MHz ±2MHz
- Maximum Output Power 12Watts
- Maximum Current 1.2A
- Maximum Voltage 40V peak or ~28Vrms
- Load impedance 50Ω
- Operating Temperature ~25ºC
- Winding Ratio 1:1
- Efficiency 90%

To satisfy the efficiency, frequency, impedance and temperature specifications, we selected the 2861000102 multi-aperture binocular ferrite core with the high frequency 61 NiZn ferrite material [47]. The multi-aperture binocular core has high flux density than standard toroid cores. From the complex permeability graph provided in Figure 2.4-1, we see that $\mu''_s < 1$ up to 7MHz, and according to *(2.15)* we know that we should have little loss due to R_s which should result in high efficiency at the fundamental frequency. Also $\mu'_s > 100$ until 40MHz, which should provide sufficient inductance for our transformer. The temperature effects of the core are negligible according to the temperature graph in [47],

A solid 24AWG wire was selected to satisfy the current specification. This wire is able to handle 2A of current with good insulation according to [48]. With a diameter of ~0.5mm for the

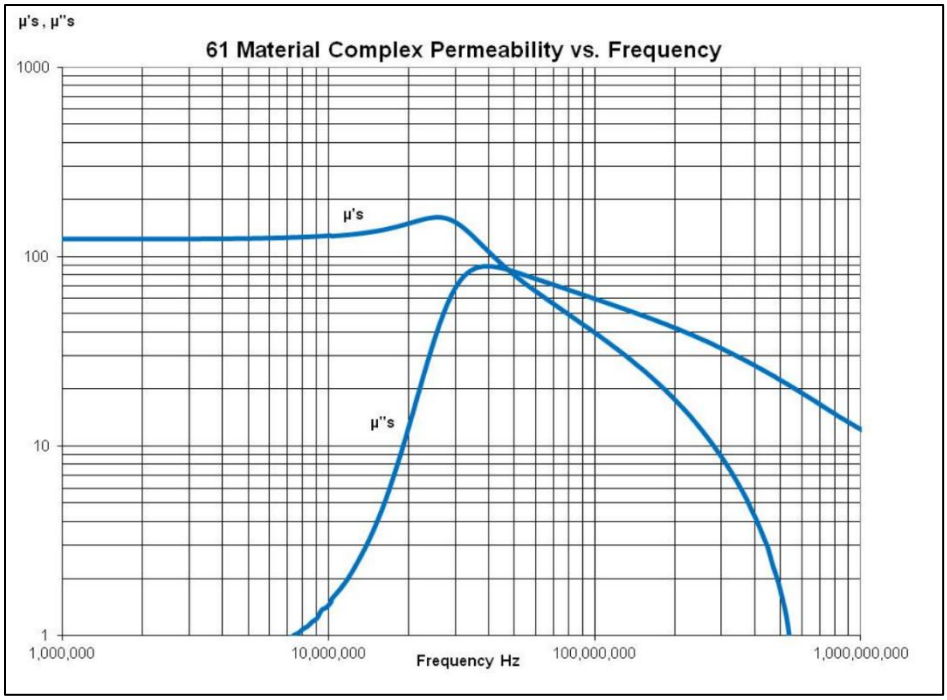


Figure 2.5-3 Complex permeability vs frequency measured on standard toroids (18/10/6 mm) at 25°C [47].

24 AWG wire and a 3.8mm hole diameter for the 2861000102 multi-aperture binocular core, we can create up to a 4:4 winding ratio for the transformer.

An insertion loss testbench was then set up to determine the optimal number of winding for maximum efficiency. The test setup uses a $5V_{p\text{-}p}$ input signal using the DMM4050. As a

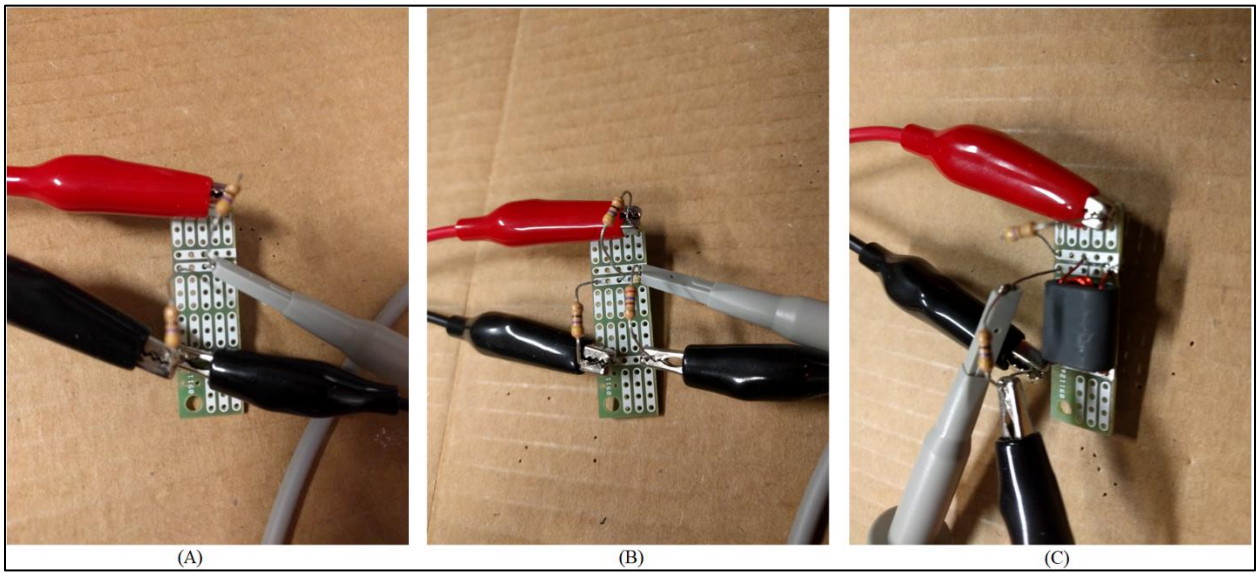


Figure 2.5-4 Transformer insertion loss test setup: (A) Before Insertion; (B) 270Ω resistor inserted; (C) Transformer inserted.

Table 2.5-1 Transformer insertion loss measurements and results.

Frequency (MHz)	**4.78**	**5.78**	**6.78**	**7.78**	**8.78**
47Ω (Vo_{RMS}/IL(dB))	1.198/0	1.199/0	1.2/0	1.201/0	1.202/0
270Ω (Vo_{RMS}/IL(dB))	1.063/1.038	1.066/1.021	1.068/1.012	1.07/1.003	1.071/1.002
2 Turns (Vo_{RMS}/IL(dB))	1.175/0.168	1.179/-0.146	1.178/-0.161	1.179/-0.161	1.178/0.175
3 Turns (Vo_{RMS}/IL(dB))	1.170/0.205	1.175/-0.175	1.176/-0.175	1.177/-0.175	1.178/0.175
4 Turns (Vo_{RMS}/IL(dB))	1.170/0.205	1.176/0.168	1.176/-0.175	1.177/-0.175	1.178/0.175

reference point, the input signal is sent through a source resistor and load resistor of 47Ω each as seen in Figure 2.5-4 (a), and the Vo_{RMS} is measured across the load at different frequencies. A 270Ω resistor is placed in parallel with the load as a reference point as shown in Figure 2.5-4 (b) and the output is re-measured. All measurements were done with the MSOX3024A oscilloscope. Finally, the transformer is put in place of the parallel resistor as shown in Figure 2.5-4 (c) with a 1:1 turn ratio of 2, 3 and 4 winding on the primary and secondary sides, and the Vo_{RMS} measurements were retaken. The results are presented in Table 2.5-1. The insertion loss is defined in (*G.1*), where V_o is the voltage at the load before the insertion, and V_o' the load voltage after insertion. Using the data calculated in Table 2.5-1, we see that there is negligible difference in IL(dB) between the 3 winding configurations. The largest and smallest IL(dB) values in Table 2.5-1 are -0.205dB and -0.147dB respectively. This translates to efficiencies of 95% and 96% which meets our specification.

2.6 Chapter Summary and Conclusions

In this chapter, we went through the basics, theory, and design of the Rezence WPT system analog component blocks. We first went through the method used to decide the minimum

efficiency specifications for each block in the system, by working backward from the Device load to the PA output. Using this method the DC-DC Converter, Broadband 1:1 Transformer, Rectifier, and Rx and Tx resonators were efficiency specifications and the PA output power were determined.

Next, we presented the design of the oscillator. Potential oscillator circuit topologies that can generate a 6.78MHz were looked into and the Colpitts oscillator was selected. The oscillator was then designed with a buffer on the output to meet our 6.78MHz and 0.02Watt specifications. Simulations and physical tests were done on the oscillator design, which showed that the physical test met our requirements.

We then presented the design of the PA Gate Driver. The differences between the sinusoidal and square wave implementations were discussed, including the additional circuitry required for them to operate effectively. A comparison was done between the gate drivers to see which one allowed the output impedance matched Class-E PA to operate with a higher efficiency, and the sinusoidal gate driver which performed better was selected. The sinusoidal gate driver was realized using a 6.78MHz Class-AB PA design and was simulated to verify if it meets our efficiency, load resistance, and output power requirements. Results show that the efficiency and output power specifications were met but the load resistance was slightly above our target.

Class-E PA design was explored next. Here we introduced the basic types of PAs available and gave reasons for the selection of the Class-E PA, such as its high efficiency, and its fundamental inductive load which is good for driving WPT coils. We then went through the basic and theory of the basic switch mode and Class-E PA. From there we found that the original equations, which use a 50% duty cycle, are simple but do not give enough meaningful information to analytically design a Class-E PA. There is a generalized set of ideal Class-E PA design equations

which takes duty cycle into account and give more insight into Class-E PA design, but they are too lengthy to be used for design analysis. These equations ignore many other parameters required to design the Class-E PA.

To overcome these issues, we presented a Class-E PA Design Methodology modified from [25]. This design flow uses the generalized Class-PA design equations to generate current and voltage waveforms at the drain of an ideal switch. These ideal waveforms are then broken down into their harmonic current and voltage waveforms, which are converted to harmonic impedances. These drain impedances are then used as a target to output impedance match the power FET using discrete components. Finally, the input is optionally impedance matched and the design simulated.

The design of a Class-E PA using a low-cost power MOSFET then done. Using the design flow, a simulation efficiency of 89.9% was achieved with this design, with a DC current of 0.554A and an output power of 18Watts. The Design then prototyped and tested, and measurement results show an efficiency of 71% was achieved, having a DC current of 0.69A, and 18Watt output power. It was found that the differences between the simulation and measurement results were caused by the capacitance value of the resonator capacitor being 40pF instead of 39pF.

Design of the Rectifier was discussed next. At frequencies in the HF range, the parasitics of the rectifier diode cannot be ignored. To achieve high-efficiency rectification we needed the series resistance to be small, and the Reverse Recovery Time and Reverse Junction Capacitance to be zero. Using equations (*2.7*), (*2.8*), and (*2.9*) the acceptable rectifier diode series resistance, reverse recovery time, and reverse junction capacitance values were determined and the CSD01060 SiC diode was selected. A Harmonic Balance simulation was done on the rectifier at peak voltages of 5V and 30V, resulting in 56% and 87% efficiencies. The low-efficiency value when a small input is applied was attributed to the large V_f voltage of the device.

Finally design of the 1:1 isolation transformer which is required for the implementation of the auto-tuning method described in chapter 4. There are many factors to be considered when designing an HF isolation transformer such as the f_1 frequency, number of turns, wire winding thickness, and the core shape. These factors whose effects were described in section 2.5.1, were used to design the isolation transformer, and a 4 turn transformer with a 2861000102 multi-aperture binocular ferrite core with 61 NiZn ferrite material was selected. The physical Transformer was designed and an insertion loss analysis was done. The measurement results showed that the transformer had 96% efficiency.

Chapter 3

3 Magnetically Coupled Resonant Wireless Power Transmission Coils for Small Electronic Devices

The key element of the Rezence WPT standard is the Magnetic Inductance and Resonant Coupling coils, which is also known as Magnetic Resonant Coupling Wireless Power Transmission (MCR-WPT) coils [49]. The MCR-WPT coils were introduced in 2007 by a group of researchers from MIT [2]. The main draw of this technology is the ability to wirelessly power any device at a distance [5]. The technology has seen applications such as wirelessly charging cars and smartphones using the Drive11 and Rezence Standards Respectively. Although The Drive11 standard is steadily being adopted for charging electric cars [4], due to stiff competition from the WPC Qi standard used in the iPhone X [50], the Rezence standard has not been as widely adopted. This is mainly due to difficulties in designing small MCR-WPT coils that resonate at 6.78MHz with high efficiency. It has been reported that Rezence devices achieve only 40% efficiency [22].

We present a new approach to designing Rezence MCR-WPT coils for smartphones and tablets. Our approach uses a double layer Printed Spiral Coil (PSC) design, which consists of 3 individual coils per PSC board on an FR4 substrate, without vias and external capacitors. This configuration allows us to take advantage of the parasitic capacitance between layers which

enables us to reduce the size of the coils. The simulations and test results show that our $5x2.5in^2$ design has ~60% and 43% percent and our $8x4In^2$ design has ~75% and 51% efficiency respectively. Simulations using higher ε_r materials also suggest that greater efficiency numbers can be achieved.

This chapter presents the design methodology, simulations, and results of our novel MCR-WPT PSC design. In section 3.1 we cover the basics of spiral inductors, including their parasitics, dimensions and modeling equations. The single layer MCR-WPT coils are discussed in Section 3.2 along with their pros and cons. Section 3.3 introduces different double layer MCR-WPT coils, and our novel MCR-WPT design and design approach. Simulations and Experimental results are presented and discussed in Section 3.4. Finally, we conclude the chapter in Section 3.5.

3.1 Spiral Inductor Basics and Theory

In the chapter introduction, we highlighted the technological progression of wireless power transmission using MCR-WPT coils. In particular, we focused on its application in small electronic devices such as smartphones and tablets, where PSCs are used for their design. These PSCs are based on the basic spiral inductors which have been broadly used in RF integrated circuits for many years [28], due to having a smaller 2D geometry than their 3D Helical counterparts. There are many geometries available to design these coils in which their resulting inductances are dependent on each of their physical dimensions. But there are also many parasitics that are associated with them that need to be considered when modeling and designing these coils. In this section, we will discuss these design considerations for spiral inductors which were retrieved from [51].

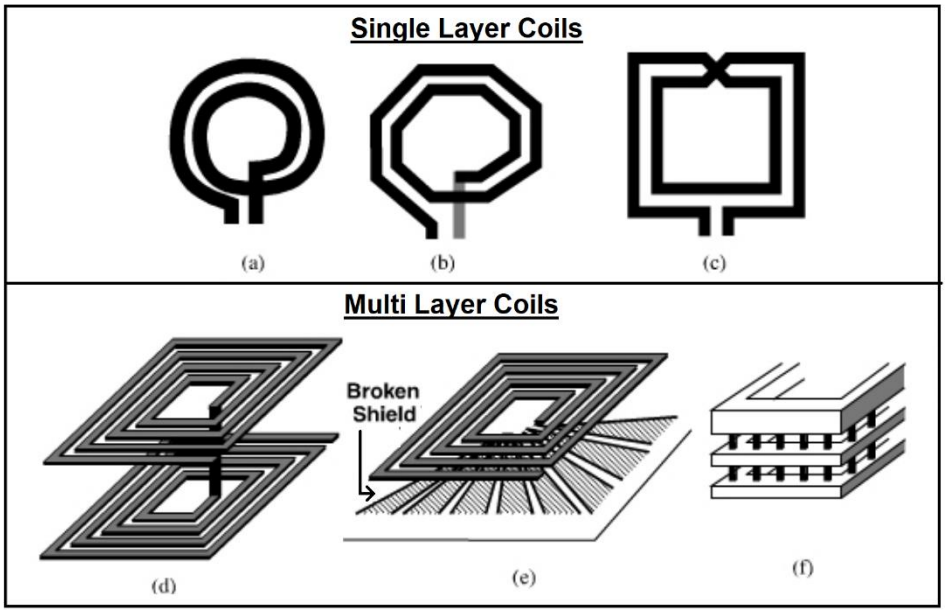


Figure 3.1-1 Various spiral inductor structures: (a) circular; (b) octagonal; (c) symmetric; (d) series stacked; (e) with ground shield; (f) parallel stacked.

3.1.1 Spiral Inductor Geometries

In addition to the basic square spiral inductor, there are many other geometries available that add to spiral inductor design flexibility. Some of the common single layer alternative structures that currently exist include the circular, octagonal and symmetric configurations. There are also series stacked, shielded, and parallel stacked multilayer inductor configurations available. The geometry of each of these spirals is shown in Figure 3.1-1. Each structure has their advantages over one another allowing for their use in different applications.

3.1.2 Effects of Single Layer Inductor Dimensions on Inductance

A Two-dimensional square spiral inductor is specified by four main physical parameters. These parameters are the outer length D_{out}, the number of turns N, wire spacing S, and wire width W, and there are defined in Figure 3.1-2 (A). The inner length D_{in} is also defined and is a function of the other parameters. The inductance of spiral inductors mainly depends on the number of turns and the diameter of each turn, but these parameters are affected by the wire width and spacing.

With reference to the 3 turn spiral inductor in Figure 3.1-2 (B), the inductance was calculated in [51] as shown in (*3.1*) below where L_1, L_2, and L_3 are the inductances of each turn AB, BC, and CD the mutual inductances between L_1 and L_2 to be M_{12}, etc.

$$L_{tot} = L_1 + L_2 + L_3 + M_{12} + M_{13} + M_{23} \tag{3.1}$$

Although equation (3.1) suggests that inductance increases with the square of the number of turns (N), due to an N-turn structure having N(N+1)/2 terms in the equation, there are few factors that limit such an increase. First, assuming we hold all other parameters constant and we increase N, each additional inner turn is smaller, hence has lower inductance. Next, the mutual coupling factor is 0.7 between neighboring turns and is less for turns further apart. Finally, as the number of turns increases, the effect of the two opposite legs of the innermost turn produces opposing magnetic field that partially cancels each other's inductance increases since the turn diameter decreases.

Although the number of turns directly affects inductance, the effects other parameters should be considered as they have an indirect effect on the parameters in equation (*3.1*). When we

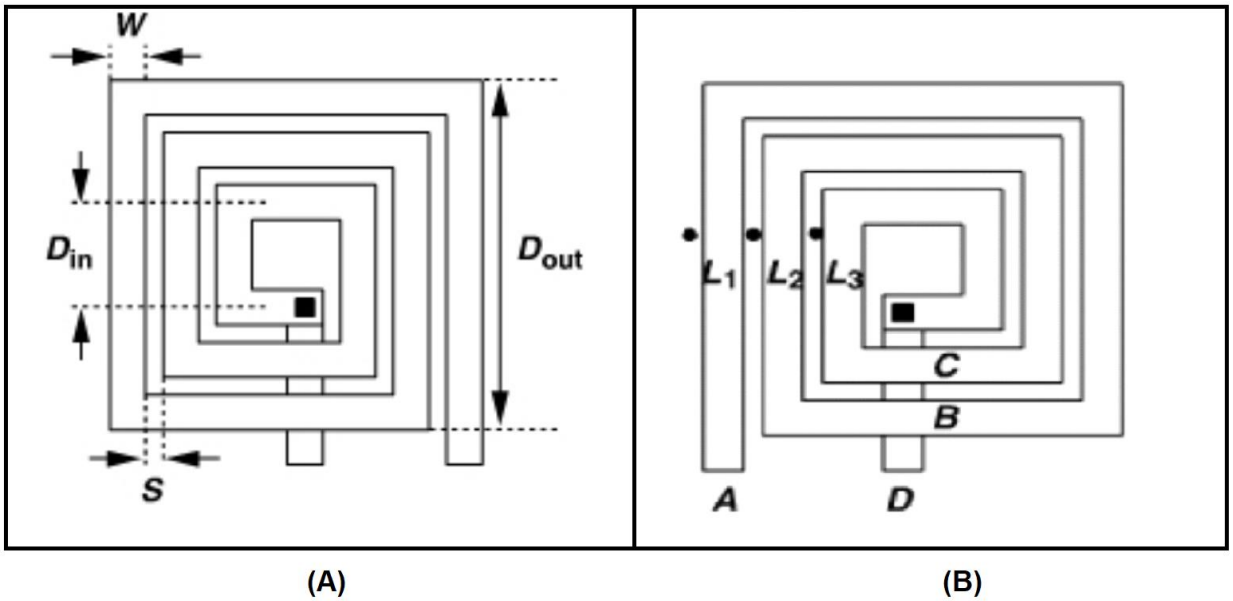


Figure 3.1-2 Simple spiral inductor: (A) various physical parameter dimensions; (B) inductance and turn definitions [51].

Table 3.1-1 Summary of the effect on physical parameters on spiral coil inductance.

Increasing Parameter	Effects	
	Pros	**Cons**
***N* (Number of turns)**	Increases inductance	D_{in} decreased
***D_{out}* (Outer Diameter)**	Max *N* increased	Limits small area applications
	D_{in} increased	
***W* (Wire width)**	Wire resistance decreased	D_{in} decreased
		Max *N* decreased
***S* (Wire Spacing)**	Reduced stray capacitance	Mutual inductance reduced

increase W, holding all other parameters constant, the line resistance would be reduced but the diameter of the inner turns and the maximum number of turns decrease resulting in reduced inductance. Increasing D_{out} increases the maximum number of turns and inner turn diameter but limits small area applications. Finally increasing S results in reduced stray capacitances from adjacent turns but reduces inner turn diameter. These effects are summarized in Table 3.1-1 above.

3.1.3 Effects of Multilayer Inductor Parameters on Inductance

As mentioned in section 3.1.1, there are a few multilayer geometries available. Among them are the series and parallel stacked spiral inductor structures. The addition of a second layer affects the total inductance of each structure differently. In this section, we explore these effects on their inductance and define their inductance equations.

3.1.3.1 Series Stacked Spiral Inductors

The idea of series stacked spiral inductors is to reduce the area occupied, and increase the inductance of a spiral coil [51]. This is done by placing them on top of each other and connecting the ends points of the inner turns together with a via as shown in Figure 3.1-3. Using this structure, the inductance is increased by the inductors being in series and the strong mutual inductance in between layers. Thus the total inductance for the double layer spiral in Figure 3.1-3 is defined as

$$L_{tot} = L_1 + L_2 + 2M \tag{3.2}$$

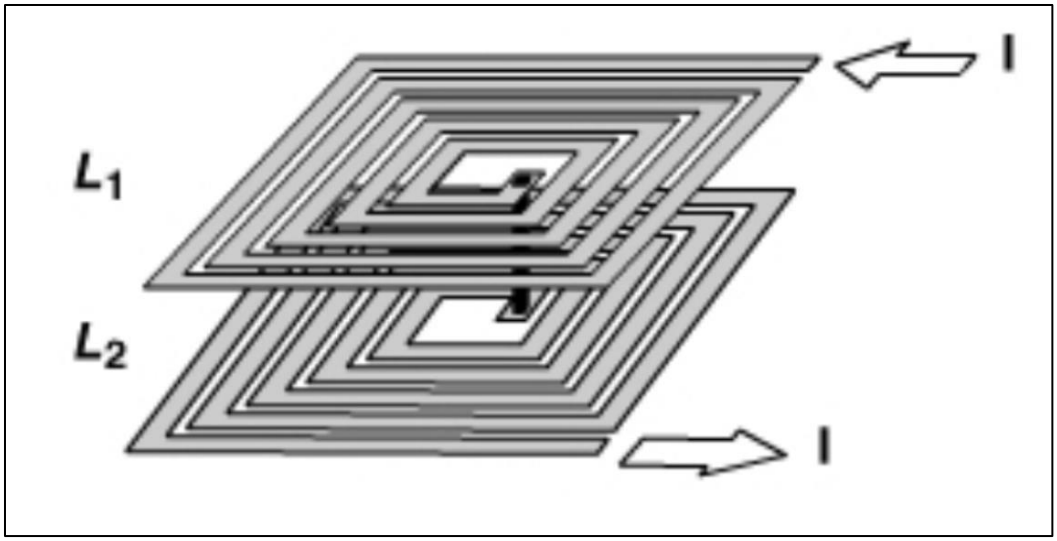


Figure 3.1-3 Series stacked spiral inductors.

Since the vertical spacing between L_1 and L_2 is much smaller than their horizontal dimensions, the mutual inductance coupling between L_1 and L_2 is nearly perfect. Therefore $M \approx L_1 = L_2$, and from (*3.2*) $L_{tot} \approx 4L_1$. In general for a multilayer spiral, the total inductance is increased by a factor of approximately n^2, where n is the number of layers. In reality, because no mutual coupling is seen from the perpendicular legs, and the inner turn of each layer is about $7/8^{th}$ of a complete turn, the multiplication factor is a little less than n^2.

3.1.3.2 Parallel Stacked Spiral Inductors

Parallel stacked spiral inductors improve the quality factor of a single layer spiral inductor, by keeping the inductance constant and reducing the coil's resistive losses. This is done by placing the spiral inductors on top of each other and connecting vias in between the layers as seen in Figure 3.1-1 (f). The net inductance of double layer parallel spiral coil calculated from Figure 3.1-4 is

$$L_{net} = \frac{L_1 L_2 - M^2}{L_1 + L_2 - 2M} \tag{3.3}$$

where L_1 and L_2 are the self-inductances, and M is the mutual coupling between the inductors. The horizontal dimensions of the parallel stacked spiral inductors in Figure 3.1-1 (f) are much larger

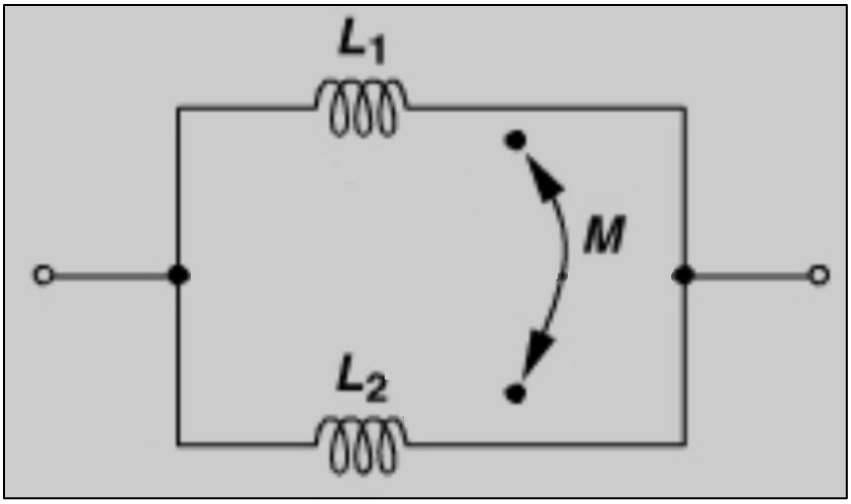


Figure 3.1-4 Effect of placing tightly coupled inductors in parallel.

than their vertical spacing, and the layers experience strong mutual inductance. Therefore $M \approx L_1 = L_2$, and the resulting net inductance $L_{net} = L_1$ from (*3.3*).

3.1.4 Spiral Inductor Parasitics and Loss Mechanisms

There many parasitics and loss mechanisms associated with spiral inductors. The parasitics are due to the capacitances between individual layers in multilayer coils and between the bottom layer and the ground shield or substrate. Resistive losses such as dc wire resistance, skin effect, and proximity effect, capacitive coupling losses from the stray capacitances and inductive coupling losses into the ground plane all contribute to the parasitics. We will briefly go through their effects and equation definitions in this section. For more detailed explanations of these effects and their equation derivations, see [51]

3.1.4.1 Parasitic Capacitance and Capacitive Coupling

Planar spiral inductors are susceptible parasitic capacitances between their surfaces and the substrate materials they are built upon. There are 2 main types of parasitic capacitances. The first type is parallel plate and fringe capacitances formed between the metal lines of the inductor and the substrate for single layer inductor illustrated in Figure 3.1-5(a), and adjacent layer wires

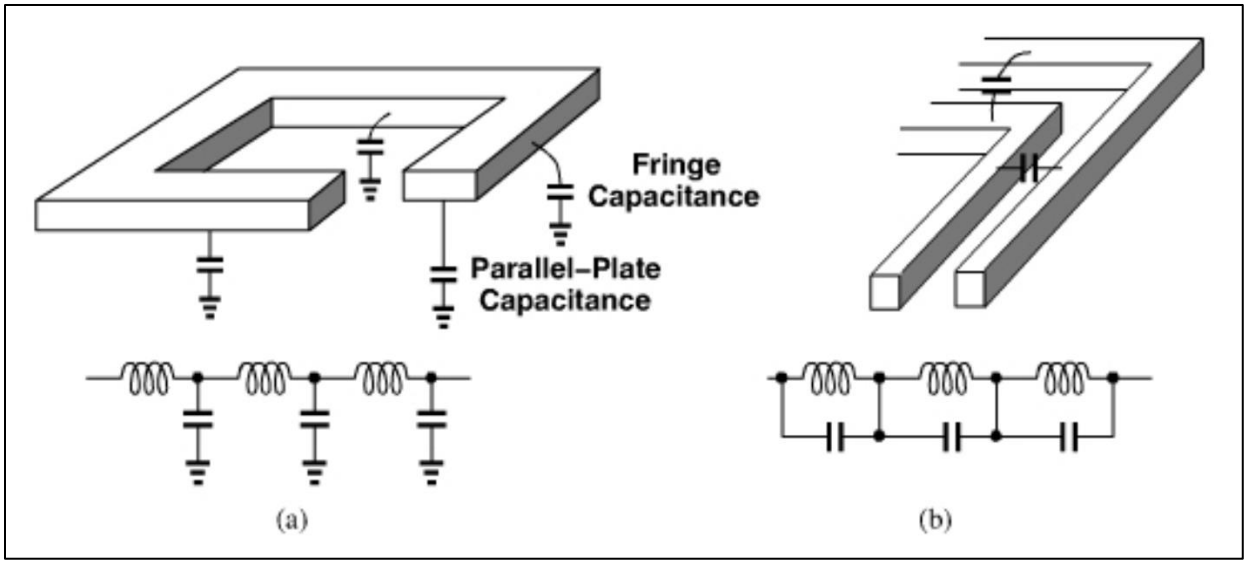


Figure 3.1-5 Capacitance types and their models: (a) bottom plate capacitance and or multilayer series inductor capacitance; (b) interwinding Capacitance.

for multi-layer inductors as shown in Figure 3.1-6. The fringe capacitance between adjacent turns of the inductor is the other type of parasitic capacitance illustrated in Figure 3.1-5(b). Therefore if the wire width or thickness is increased to reduce the line resistance, these component capacitances increase and must be considered.

The lumped model of the capacitances on each leg of the square spiral inductor representing the parallel plate and fringe capacitances are shown in Figure 3-3(a). Using an energy-based analysis on a modified distributed capacitance model based on the lumped model as described in [51], the estimated equivalent lumped capacitance equation was derived and the results are shown in (*3.4*) below. The parameters K and C_u represent the total number of legs in the spiral inductor and the average capacitance of all the legs due to the parallel plate and fringe capacitances to the substrate.

$$C_{eq} = C_u \cdot \frac{(K+1)(2k+1)}{6K} \tag{3.4}$$

For the parallel turn-to-turn Interwinding capacitances, the lumped model capacitance is shown in Figure 3-3(b). Using the same energy-based analysis, the equivalent lumped capacitance equation

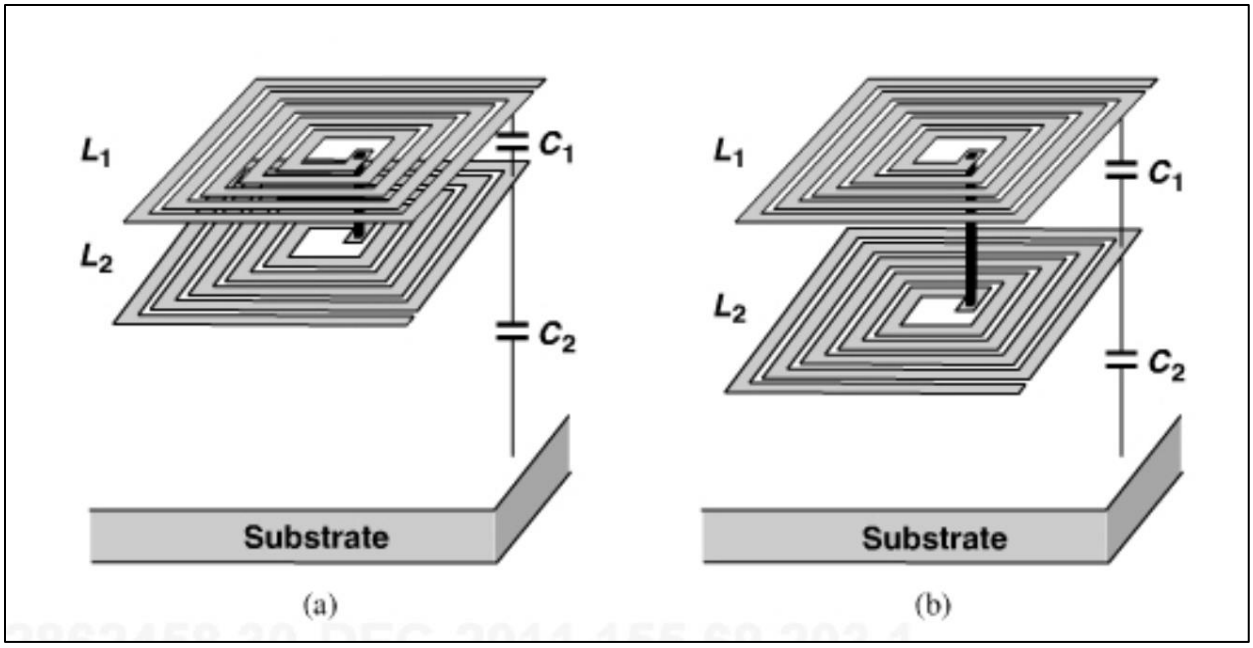


Figure 3.1-6 Equivalent capacitance for series stacked inductors: (a) layers close together; (b) layers further apart.

was derived and shown in (*3.5*). The K and C_F represent the total number of spiral inductor legs and the average capacitance of all the legs due to parallel fringe capacitances of all the turn-to-turn inter-windings.

$$C_{eq} = \frac{1}{K} \cdot C_F \tag{3.5}$$

We now consider the parasitic capacitances of the multilayer inductor, in particular, the series and parallel stacked inductors. First, we consider the equivalent capacitance of the series stacked inductors as shown in Figure 3.1-6. The lumped capacitances between layers and the lower layer and substrate are defined by C_1 and C_2 respectively. Using an analysis similar to before, the equivalent lumped capacitance equation was derived and the result shown in (*3.6*).

$$C_{eq} = \frac{4C_1 + C_2}{12} \tag{3.6}$$

For stacked parallel inductors with multiple vias seen in Figure 3.1-1 (f), when a time varying voltage is applied, the voltage difference between layer segments is 0V. This results in a net capacitance of 0F. In reality, there's a small capacitance but it's too small to have an effect.

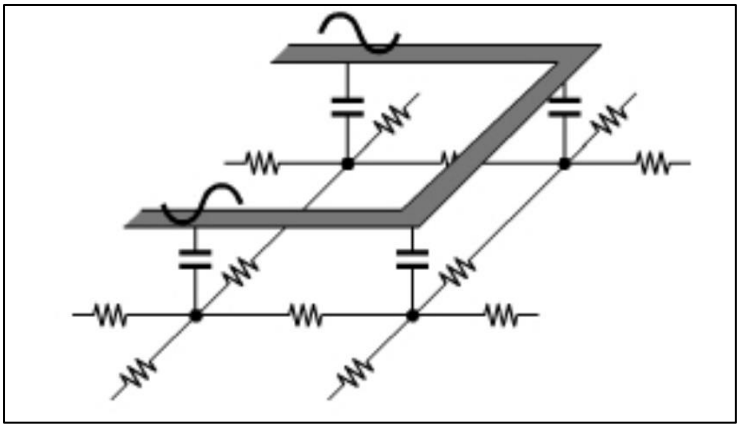


Figure 3.1-7 Substrate loss due to capacitive coupling.

All of our analysis with spiral inductor capacitances was associated with their parasitic characteristics, but there are however losses associated with the capacitive coupling to the substrate where the resistivity is neither infinity nor zero. Illustrated in Figure 3.1-7, since we have the rising and falling of voltage at each segment of the spiral inductor, a time-varying displacement current is flowing in the substrate. This current flow causes some power loss in the substrate during each cycle. The loss due to capacitive substrate coupling is dependent on the specified loss tangent of the substrate. A low loss tangent measured at a high frequency means that at our low frequency, the loss due to substrate coupling is small enough to be ignored.

3.1.4.2 Low Frequency (DC) Metal Resistance

All conductors exhibit a small resistance at DC and low frequencies. For spiral inductors, only the series resistance as illustrated in Figure 3.1-8. The total series resistance of the inductor is dependent on the total unwound wire length (l), the cross-sectional area (A), and the resistivity of the metal (ρ), and is determined using equation (*3.7*).

$$R_s = \frac{\rho_c \cdot l}{A} \tag{3.7}$$

To reduce the loss of from R_s we need to identify and adjust the inductor parameters that affect its value. First, we know l is directly related to the N of the inductor when we hold all other

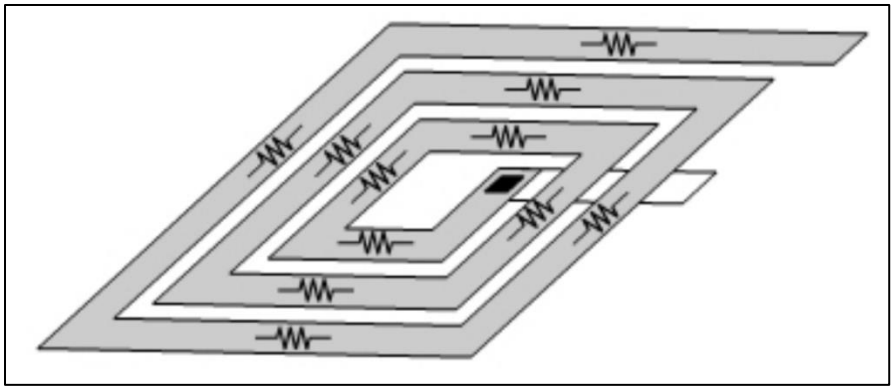


Figure 3.1-8 Metal resistance in spiral inductors.

parameters constant. Also, the cross-sectional area is a function of W and wire thickness. Thus from the above equation, we see that the wire resistance of the conducting material can be reduced by increasing the wire width or decreasing the number of turns.

There are however some trade-offs that need to be considered when increasing W to reduce R_s. As described in sections 3.1.2 and 3.1.4.1, increasing the wire width reduces the diameter of the inner turns and the maximum N as well as increases the parasitic capacitance. Also decreasing N decreases the overall inductance.

3.1.4.3 Skin Effect

Current through conductors tend to flow near the conductor's surface at high frequencies as shown in Figure 3.1-9. Because of this the area where current flows is reduced resulting in a higher resistance. This is due to the attenuation of the amplitude of an EM wave when trying to penetrate a conductive medium [52]. The measure of the attenuation decrease by a factor of e^{-1} into the medium is known as the skin depth. The skin depth is a function of the conductor permeability (μ), conductivity (σ), as well as frequency (f), and is defined in equation (*3.8*).

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{3.8}$$

The resistance due to skin effect is defined in (*3.9*) as follows.

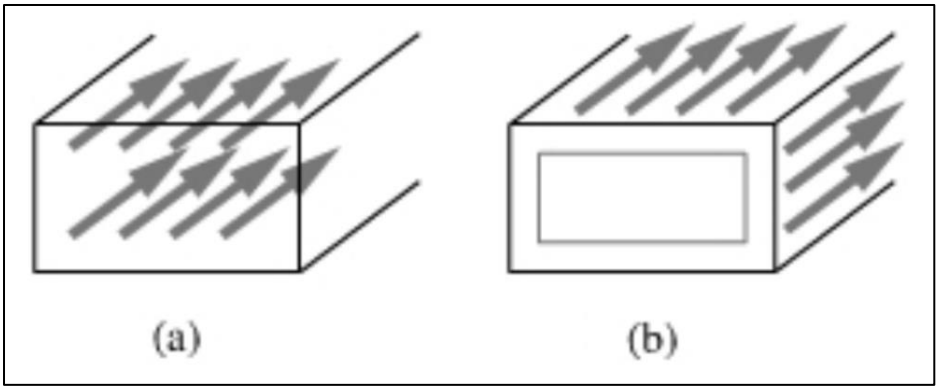


Figure 3.1-9 Current distribution in a conductor: (a) low frequencies; (b) high frequencies

$$R_{skin} = \frac{1}{\sigma\delta} \tag{3.9}$$

During high-frequency operation where δ is larger than the wire thickness, the loss due to R_{skin} may be significant. To reduce R_{skin}, we can use stacked parallel inductors with an individual thickness less than δ to increase the conductive surface area. The overall loss due R_{skin} is reduced considerably when the sum of the individual wire thicknesses is greater than δ.

3.1.4.4 Proximity Effect and Current Crowding

With the adjacent wires in the spiral inductor having small distances between them, their close proximity starts to affect the current distribution throughout the inductor. As seen in Figure 3.1-10 (a), the current is condensed into a smaller area near the edge of the wire. To understand why this happens, we do a quick analysis the effect of the current flowing through one turn on an adjacent turn which is illustrated in Figure 3.1-10 (b). The inductors time-varying current i(t) in one turn generates a time-varying magnetic field by Biot-Savart's law. From Faraday's law, this changing magnetic field passes through nearby turns and generates current loops in the center of the wire known as eddy currents. These eddy current flow opposite and concurrent with i(t) which adds and subtracts to it. Because of this, current is crowded at one side of the conductor. This current crowding due to nearby adjacent turns is known as the proximity effect.

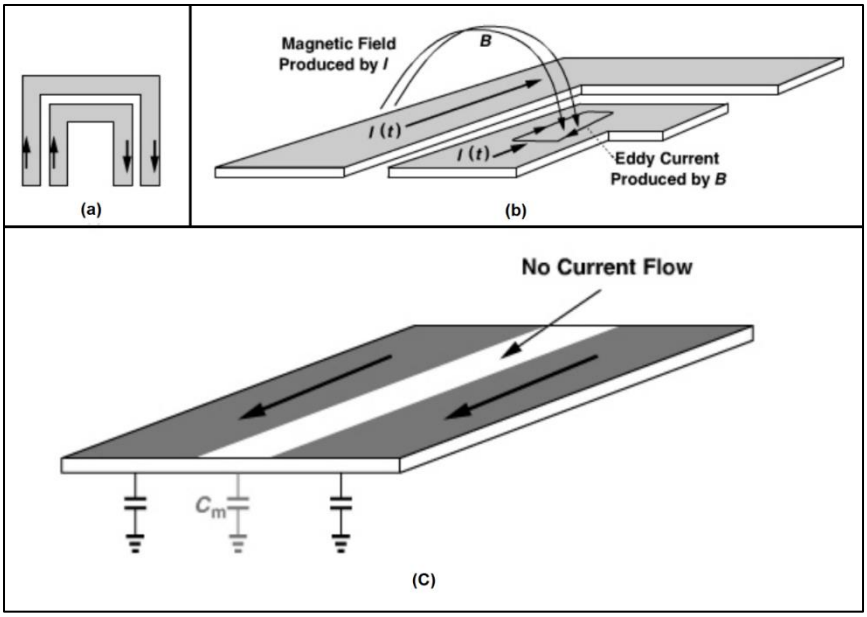


Figure 3.1-10 Proximity effect: (a) current distribution in adjacent turns; (b) eddy currents in the wire due to the magnetic field generated from a nearby adjacent wire; (c) reduction of the substrate and multilayer capacitance due to current crowding.

The resistance due to the proximity effect is a function of frequency. This because the induced voltage (V_{emf}) in the conductor is proportional to the frequency (f) from Faraday's law. Therefore when f increases, the V_{emf} increases proportionally producing an increase in the eddy currents in adjacent turns, resulting in the i(t) current concentrating into an increasingly smaller area at the edge of the wire, and hence causes an increase in the inductor resistance. Using this information, the equation for proximity effect derived and shown in (*3.10*).

$$R_{eff} = R_{dc} \cdot \left(1 + \frac{1}{10} \cdot \left(\frac{f}{f_{crit}}\right)^2\right) \tag{3.10}$$

The R_{dc} in the above equation represents the dc resistance and f_{crit} is frequency where current crowding begins and is defined as follows

$$f_{crit} = \frac{3.1}{2\pi\mu} \cdot \frac{W+S}{W^2} \cdot R_{sheet} \tag{3.11}$$

where W and S are the wire spacing and separation distance in the inductor, μ and R_{sheet} are the permeability and sheet resistance of the metal.

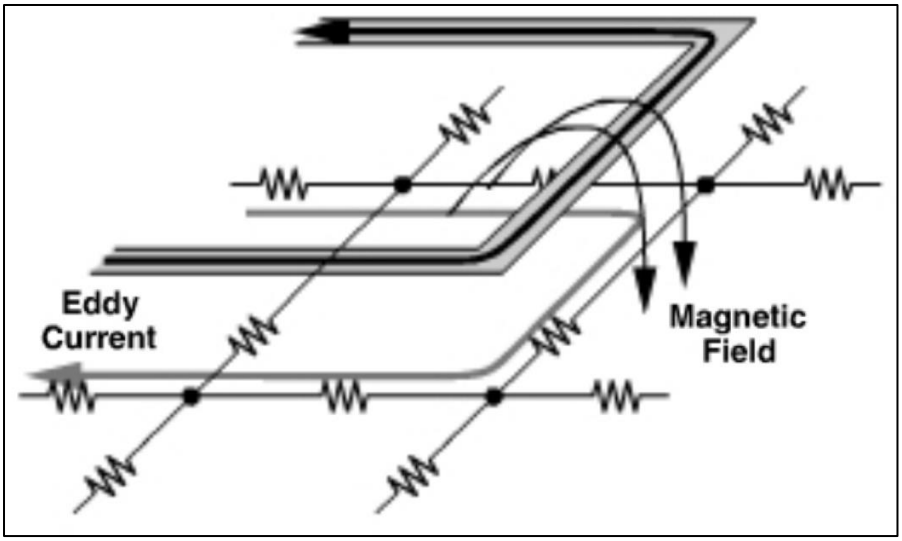


Figure 3.1-11 Magnetic coupling to the substrate.

There are other effects of current crowding. Since the current is concentrated at the edge of the wire, each turn's equivalent diameter changes a little resulting in a different inductance than the low-frequency value. Since the current is concentrated at the wire's edge, the wire has no current in the middle, and therefore the total capacitance (C_{tot}) is reduced which is seen in Figure 3.1-10 (c). Thus as shown in equation (*3.12*), the total capacitance is inversely proportional to the wire resistance where C_{dc} is the dc capacitance.

$$C_{tot} = \frac{R_{dc}}{R_{eff}} \cdot C_{dc} \tag{3.12}$$

3.1.4.5 Magnetic Coupling in the Substrate

The final set of losses to be considered in spiral inductor design are the losses associated with the magnetic coupling to the substrate where the resistivity is neither infinity nor zero. Illustrated in Figure 3.1-11, we see that eddy currents are produced in the substrate from the magnetic fields generated by the current flow in the inductor's turns. These eddy currents translate into losses in the substrate during each cycle. Like the capacitive coupling to the substrate, the loss due to inductive substrate coupling is dependent on the specified loss tangent of the substrate. A

Table 3.1-2 Types of resistive loss, their description, and methods to reduce their effects.

Resistive Loss Mechanisms	Loss Effect Description	Methods to reduce Effect
DC	Metal DC sheet resistance	Thicker and wider wire
Skin effect	Increased resistance from high frequency current flowing on the conductor surface due to the EM waves inability to penetrate the material	Use stacked parallel inductors with individual thickness less than the shin depth to increase the conductive surface area
Proximity Effect	Current crowds in a small area near the edge of the wire due to eddy currents formed by the magnetic field created from nearby adjacent wires	Larger spacing between wires and thicker wires.
Capacitive and Magnetic coupling to substrate	Losses due to currents in the substrate caused by the changing line voltages	Due to our relatively low application frequency, this effect can be ignored

low loss tangent measured at a high frequency means that at our low frequency, the loss due to substrate coupling is small enough to be ignored

3.1.4.6 Inductors Parasitics and Loss Mechanisms Summary

There are many types of capacitive parasitics and resistive losses associated with inductor design. We summarise the resistive loss types, their description and reduction methods in Table 3.1-2. The capacitive parasitics, their description, benefits, and effects are provided in Table 3.1-3.

Table 3.1-3 Types of spiral inductor capacitive parasitics, their benefits, and drawbacks.

Capacitive Parasitic	Description	Benefits and Effects
Substrate Capacitance	Parallel plate and fringe capacitances between the wires and the substrate	Substrate resistance losses from time-varying substrate currents caused by substrate capacitance (Small enough to be ignored).
Inter-wire Capacitance	Fringe capacitances between adjacent turns of the inductor	An increase in the number of turns and number of layers increases the inter-wire and inter-layer parasitic capacitances, resulting in a lower resonant frequency, but at the cost of increased resistance due to the proximity effect
Inter-layer capacitance	Parallel plate and fringe capacitances between wires on multiple layers	

3.1.5 Spiral Inductor Basics Summary and its relationship to MCR-WPT Coils

In this section, we covered the effects of the key inductor dimension parameters on its inductance as well as its associated passive capacitive parasitics and loss mechanisms. We will now briefly summarize their effects and how they can be mitigated

When constructing the spiral inductor, the number of turns and the outer dimension of the spiral inductor are the main contributors to the inductance. Other parameters such as the wire spacing and width indirectly affect these parameters and must be considered. The effects of these spiral inductor dimensions on its inductance are summarized in Table 3.1-1. Ideally, the inductance is the square of the number of turns from (*3.1*). But because each added turn has a smaller diameter with a smaller inductance and increased inductive loss from opposing legs, and are also further from the outer turns, the inductance and mutual inductance they add to the total inductance is incrementally smaller. Another way to increase inductance is by using stacked series spiral inductors but this also causes an increase the parasitic capacitance.

Spiral inductor capacitive parasitics are important because these capacitances and the inductance of the inductor determines its self-resonant frequency (SRF), and an increase in parasitic capacitance causes a decrease in the SRF. Therefore when trying to the increase inductance by increasing the number of turns and or the number of layers (between series stacked spirals), the parasitic capacitance increases due to an increase in fringe capacitances between adjacent turns and parallel plate and fringe capacitances between wires on multiple layers respectively, and must be taken into consideration. The parasitic capacitance to the substrate is also present and may need to be considered depending on the operation frequency.

Finally, there are resistive loss mechanisms that reduce the quality factor of the spiral

inductor. Low frequency/DC sheet resistance is a characteristic of the metal being used. Resistance due to the skin effect is dependent on frequency and the permeability of the metal. Proximity effect resistance is dependent on frequency, the permeability of the metal, the wire spacing and wire width. There are also losses from generated magnetically coupled eddy currents and capacitively coupled displacement currents flowing through the resistance in the substrate. These losses are summarized in tangent measured at a high frequency means that at our low frequency, the loss due to substrate coupling is small enough to be ignored

3.1.5.1 Inductors Parasitics and Loss Mechanisms Summary

There are many types of capacitive parasitics and resistive losses associated with inductor design. We summarise the resistive loss types, their description and reduction methods in Table 3.1-2. The capacitive parasitics, their description, benefits, and effects are provided in Table 3.1-3.

3.2 Single Layer MCR-WPT Coils

Single layer MCR-WPT printed spiral coils (PSCs) using the Rezence standard with a frequency of 6.78MHz share all the loss mechanisms and parasitic capacitances with their single layer spiral inductor counterparts. Like the spiral inductor, the low frequency/DC sheet resistance, skin effect and proximity effect loss mechanisms must be taken into consideration since they affect the Q factor of the system. There are also substrate losses due to magnetically and capacitively coupled currents flowing through the substrate resistances, but are these small and can be ignored because of our low operating frequency.

Unlike its spiral inductor counterpart which mainly focuses on design to achieve a large

inductance is a small space, the design of small MCR-WPT PSCs to fit in smartphones with the low Rezence SRF and a high Q. To achieve this low frequency we can add external capacitors to the spiral coil, but this can't be done since it requires additional space in the cellphone which is expensive. We try to reduce the SRF by changing the physical parameters that affect the parasitic fringe capacitances between turns. In this section, we go through the basics of MCR-WPT PSCs, the step by step method used to design and determine the SRF through simulations, the simulation results, and discussions with a summary.

3.2.1 MCR-WPT PSC Basics

MCR-WPT PSCs are composed of 4 spiral inductors with 2 spiral inductors each on the transmitter and receiver PSC boards. The basic circuit diagram of the MCR-WPT coils system obtained from [53] is shown in Figure 3.2-1. From the diagram, the first and second coils known as the 1-Source and 2-Sending/Transmitting coils are on the transmitter side PSC board, and the third and fourth coils known as the 3-Receiving and 4-Load coils are on receiver side PSC board. other reasons for this configuration. Firstly, since the outer coil on the PSC board has more turns and is inductively coupled with the inner coil, it has a higher voltage across it. The outer coils

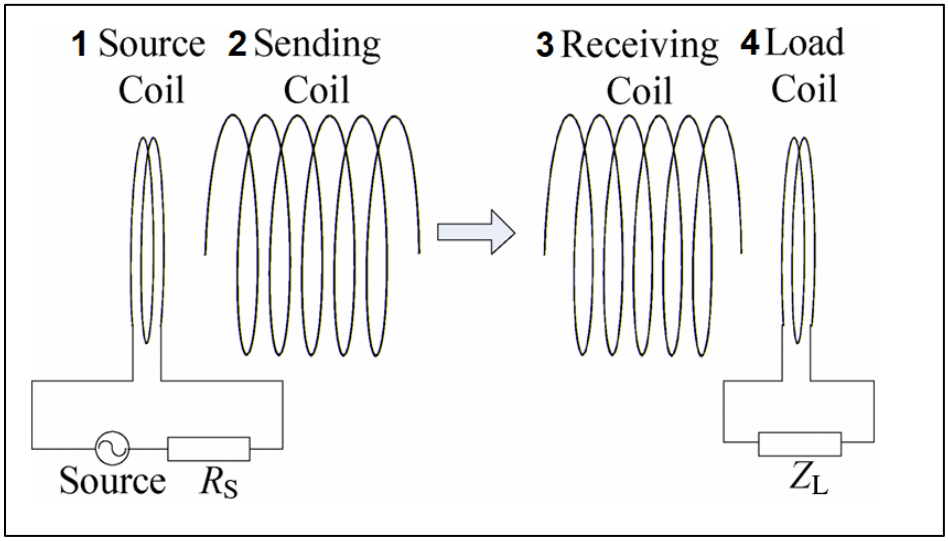


Figure 3.2-1 Basic circuit diagram of an MCR-WPT coils system connected to a source and load [53].

on both PSC boards are loosely coupled and magnetically resonant. Because of this, the separation distance where maximum efficiency occurs is increased, and when this separation distance is smaller than the optimal efficiency distance. Another reason is that since the coils are impedance matched, they can be tuned to bring the system back into resonance when the separation distance is shorter than the optimal efficiency distance as shown in sections 4.1.3 and 4.1.4.

Each coil in the MCR-WPT coils system is composed of individual capacitances, inductances, and resistances. Like their spiral coil counterpart, their inductance is determined by the dimensions of the inductor as discussed in section 3.1.2. The exception to this is that the efficiency is directly related to the amount of flux through the inner coil, so a larger inner coil dimension is needed for higher efficiency. The same loss mechanisms and parasitic capacitances described in section 3.1.4. The resistance values of each of the spiral coils were taken from the Ohmic losses in the wires, due to the low-frequency DC metal sheet resistance, the skin effect, and the proximity effect. The capacitance values were obtained from fringe capacitances between adjacent turns of the inductor. These passive values can be lumped together for circuit analysis.

Using these passive components, with reference to Figure 3.2-1, the simplified and complete equivalent lumped circuit models are constructed as seen in Figure 3.2-2. The capacitive, inductive and resistive elements of each inductive coil are represented as C_i, $L_{i,}$ and R_i, and the mutual inductance between the inductive coils defined by M_{ij}, where i,j = 1,2,3,4 and $i \neq j$. The numbers for i and j represent the source, sending, receiving and load coils respectively.

Looking at the equivalent circuit models in Figure 3.2-2, it can be seen that the resistances R1 and R4 are ignored in both models. This is because the Source resistance R_S and the load resistance R_L are much larger than the corresponding R1 and R4 resistances of the source and load coils respectively, and are thus ignored.

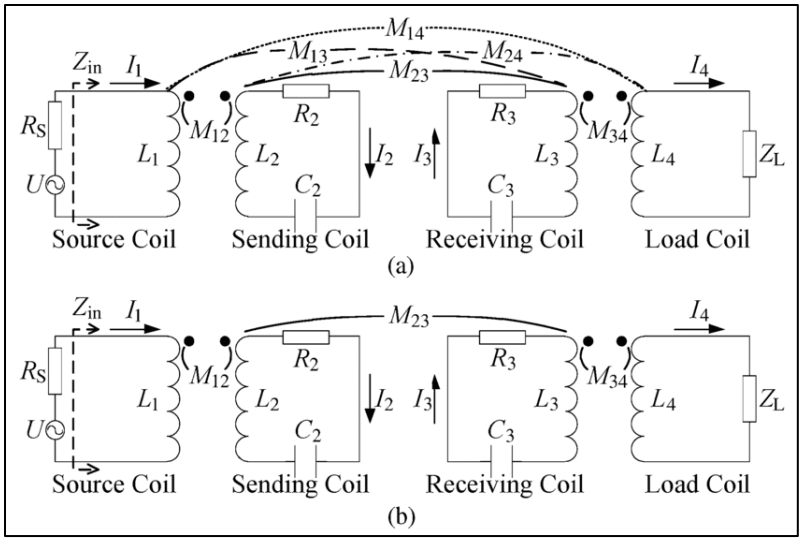


Figure 3.2-2 Equivalent lumped circuit models of the MCR-WPT 4-coil system: (a) complete model; (b) simplified model [53].

The inner and outer adjacent coils on the same PSC board are inductively coupled with mutual inductances M_{12} and M_{34}, while the outer coils on the different PSC boards are loosely coupled and magnetically resonant with a mutual inductance of M_{23}. There are other mutual inductances in the system between the source and load coils, the source and receiving coils, and the sending and receiving coils which are defined as M_{14}, M_{13}, and M_{24} respectively. The difference between the complete and simplified circuit models is the mutual inductances that are considered in the system. In the complete circuit model, the mutual induction between the non-adjacent coils is taken into consideration but are ignored in the simplified model.

Using these models, a detailed theoretical analysis of the frequency splitting phenomenon which affects MCR-WPT coils was done in [53]. We do no use this theoretical analysis to design our coils, but the reader is encouraged to go through [53] to get a better understanding of this phenomenon. For the remainder of this chapter, we will use the separation distance where maximum efficiency occurs, also known as the critical coupling distance (CCD), to assess our design. We briefly describe the basic theory of Frequency Splitting and the resulting MCR-WPT coils system modes of operation it causes in section 4.1.1.

3.2.2 Design Methodology and Simulation Setup.

Before we present our single layer MCR-WPT results, we go through the design methodology used to design the self-resonant coils. Two simulation tools, namely Momentum and EMPro, provided by Keysight technologies are used in this methodology. It first involves the use of Momentum's Method Of Moments (MOM) simulations (which take roughly 2 minutes to complete) on the individual PSC boards with an inner and outer coil each. PSC board is then imported into EMPro to conduct lengthy Finite Element Method (FEM) simulations at multiple distances on the entire MCR-WPT coils system to verify SRF and efficiency.

3.2.2.1 Momentum - Simulation setup

We begin Momentum simulation setup by establishing copper foil and PSC board overall thickness, and substrate material. Standard value board and copper foil thicknesses of 1/32inch or 1/16inch, and 1oz or 2oz respectively were used in simulations, as they allowed for easy prototyping. The FR4 substrate is easily accessed for prototyping and is mainly used for simulations, but simulations were also done with other materials to see their effects on the coils.

Using these parameters the Momentum substrate was set up. Copper layer thicknesses (one or more layers) values were entered directly. The substrate thickness was determined by subtracting the overall copper thickness from board thickness. Finally, using a method adopted from Sonnet software spiral inductor design [54], a PEC ground plane was placed 2 inches below the design with an air layer in between to minimize the field effects the PEC has on the PSC board.

3.2.2.2 Momentum - Creation of Spiral Coils and Simulation

The Inner and outer coils are then created using the macros available in Momentum. Using the T-lines macro the inner source/load coil is created. It has a single turn, a large diameter and to

allow more flux, and a wire width and thickness large enough to lower DC resistance without exceeding 3 times the skin depth of copper. For the outer (sending/receiving coil) coil, the T-lines macro was used for single layer coils, and the double layer spiral (part of an inductor workspace from Keysight's website) was used for double layer coils. The outer diameters of the coils were limited by cellphone and tablet sizes, and the number of turns was used to lower the frequency. Since there is less current flow through the outer coils due to inductive coupling between inner and outer coils, its wire width is made smaller than the inner coil which allows for more turns, but at the cost of increased resistive losses. Care was also taken to ensure the outer coils inner diameter was larger than the inner coil diameter so that there is no layer overlap.

Since these coils are for smartphones and tablets applications, using these factors, it was determined that rectangular coils with outer coil outer dimensions of $5x2.5in^2$ and $8x4in^2$ for smartphones and tablets respectively would be designed. The inner source/load coils diameter is limited by the shorter of its 2 sides. An initial guess of wire widths, wire spacing, diameters and number of turn for both coils were done. Two ports were connected to the ends of the inner coil as

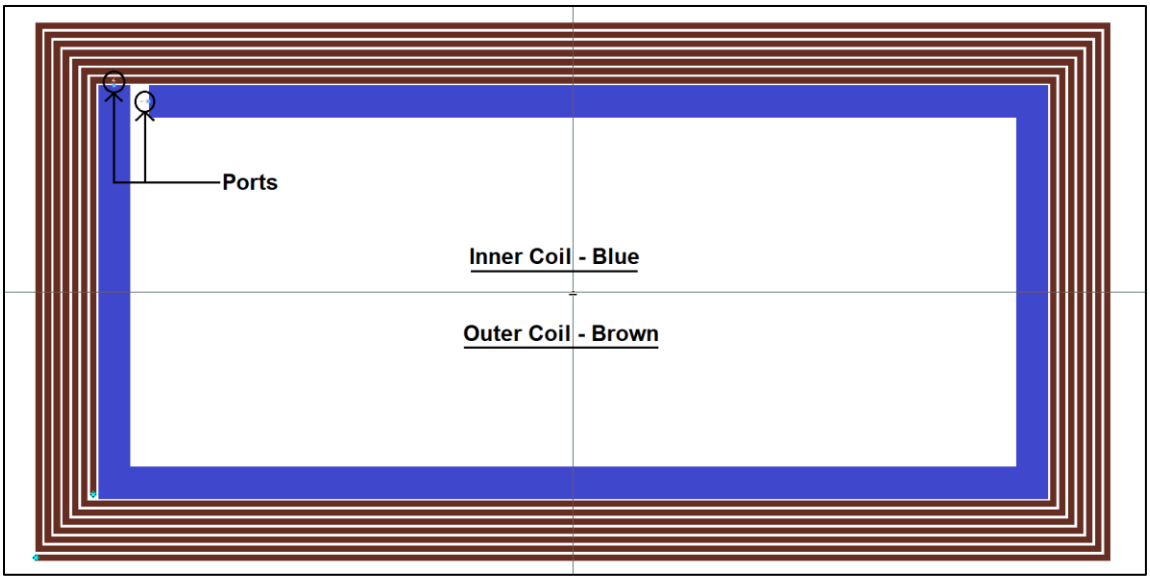


Figure 3.2-3 Layout of PSC board with inner and outer coils and port connections in momentum.

shown in Figure 3.2-3, and the other ends are connected to ground automatically. The frequency range of S-Parameter simulations are set to 0.5-35MHz with a step size of 1kHz. All other settings were left at the default values. The simulation was the run and S-Parameter results were generated.

3.2.2.3 Momentum - Post Simulation Setup and Analysis

S-Parameter simulation results are stored in the dataset files, which we used to generate the S11 dB and the S11-Resistance vs frequency graphs. The S11 (as well as S12, S21, S22) vs frequency plot is generated in the Momentum Data Display by default. To obtain the graph of the S11-Resistance vs frequency, we first convert the S(1,1) matrix to the Z matrix, then plot the real value (R) of the complex number matrix using the equations (*3.13*) and (*3.14*) below.

$$Z = stoz(s(1,1)) \tag{3.13}$$

$$R = real(Z) \tag{3.14}$$

Using these plots we find the SRF of the PSC board. We obtain the board SRF by getting frequency where the peak S11-Resistance (R) value occurs and the lowest frequency where a sharp peak S11 dB values occurs. These frequency values are more often than not exactly the same. The differences are found to be more pronounced when the frequency range was larger suggesting that accuracy is affected interpolation errors.

The PSC board SRF value, obtained from the peak R and S11 values, gives a good estimation of the MCR-WPT coils' SRF at the critical coupling. Assuming the spacing between the inner and outer coils is roughly equal to the outer coil wire spacing, the error ranges from 0.2-1.5MHz larger than the MCR-WPT coils' SRF from the EMPro simulation. The error magnitude is dependent on outer coil wire width to wire spacing ratio (W/S), where W/S ratios near 0.5, 1 and 1.5, result in errors of 0.2-0.5MHz, 0.5-1.1MHz, and 1.1-1.5MHz of respectively.

3.2.2.4 Momentum – Insertion Loss, and MCR-WPT S21 and Efficiency Calculation

Since we have identical coils, we can get an estimated max efficiency of the 4 coil system doing insertion loss analysis using the peak S11-Resistance value which is at resonance. With reference to Appendix F, assuming that ZG and ZL are matched, the insertion loss is that same as the S21 and S12 S-parameters. Therefore we set up the insertion loss analysis by inserting 2 resistance values in parallel with ZL as shown in Figure 3.2-4.These resistances represent the identical loss through the transmitter coils and receiver coils of the MCR-WPT coils system. We then get the V_{LA} and V_{LB} voltages before and after the insertion of the resistors by basic circuit analysis. Equation (*F.1*) is then used to calculate the insertion loss, which is the equal to -S21.

Through many simulations, it has been observed that the maximum S21 dB peak values seen from the EMPro FEM simulations during the over coupled frequency splitting region (defined in section 4.1.1) are consistently near the value obtained from insertion loss analysis. The CCD value is slightly lower with an error of 1dB depending on FEM accuracy settings. There is a possible issue with this method, due to an oversight that could not be verified with ADS technical support beforehand. When converting from S to Z parameters, S11 was used as the stoz() variable. But according to the stoz() documentation, the S matrix should be used as a variable.

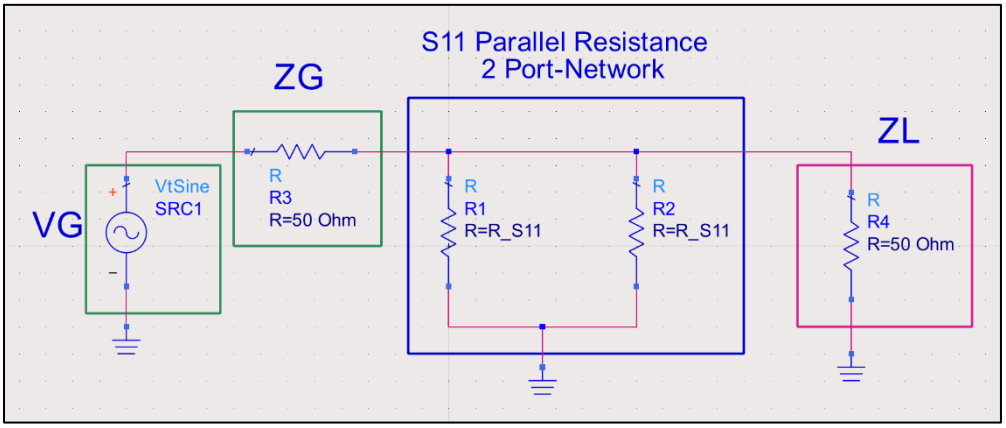


Figure 3.2-4 Insertion loss analysis schematic used to calculate and predict the maximum S21 MCR-WPT coils system.

Table 3.2-1 Benefits and drawbacks of changing MCR-WPT coil parameters on SRF & efficiency. All other parameters are constant.

COIL	PARAMETER	CHANGE	BENEFITS	DRAWBACKS
Inner	Diameter	Increase	• improved magnetic flux • improved efficiency	• maximum number of outer coil turns reduced
Outer	Number of turns	Increase	• lowers frequency	• inner diameter may need to be reduced
Outer	Wire width	Increase	• reduces the DC resistance • reduces the frequency	• increase in proximity effect resistance
Outer	Wire spacing	Decrease	• reduces the frequency	• increase in proximity effect resistance

3.2.2.5 Momentum – MCR-WPT Coil Design Assessment

After using the insertion loss and the peak S11 to predict the efficiency and SRF of the EMPro MCR-WPT coils simulation, we compare the results to our specifications. If the design doesn't meet the frequency and/or efficiency goals, the parameters of both coils are re-adjusted to meet the targets. Using Table 3.1-1 as a reference, the parameters that affect frequency and efficiency of the coils are presented with their benefits and drawbacks in Table 3.2-1.

3.2.2.6 EMPro setup and simulations

When the estimated efficiency and SRF results from the Momentum simulation on the PSC board meet the specifications, the board is imported into EMPro. The MCR-WPT coil design is

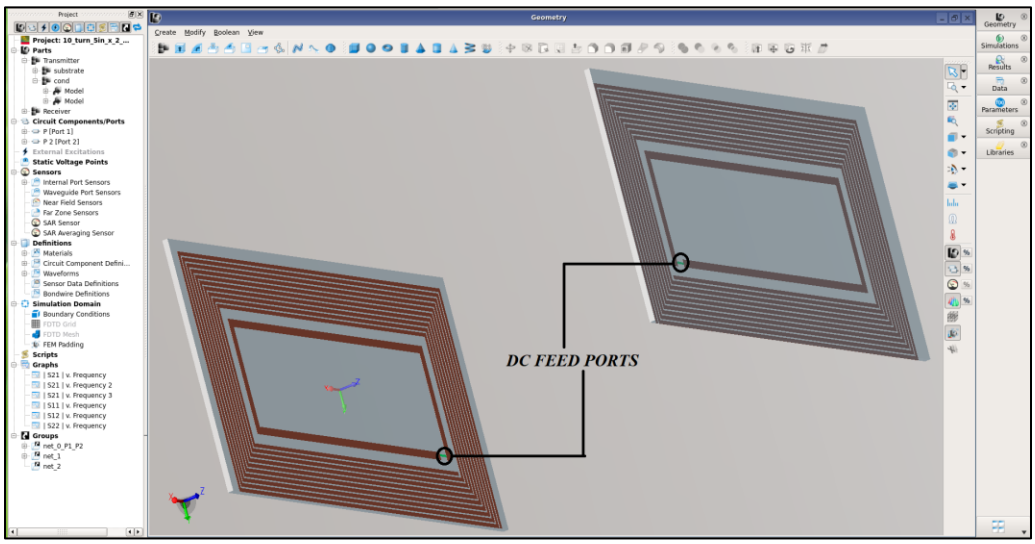


Figure 3.2-5 Example EMPro 3D assembly of the MCR-WPT coils system with 2 ports.

then set up for simulations by removing the simulation box, PEC ground plane, and the waveguide planes objects. A copy of the board assembly is then created, and its orientation and location are changed. The FEM padding is set to “absorbing” for the x, y and z-axes and boundary conditions are set to the length and width of the PSC boards in the x and y-axes, and the separation distance in the z-axis. DC feed ports are added. Finally, the FEM simulation setup is adjusted as follows:

Frequency Plans section

- Fields storage tab
    - "all frequencies from the frequency plan and mesh frequency" is turned on.

mesh/refinement properties section

- advanced tab
    - "use initial minimal mesh size" is selected
    - “automatically determine” button is used to generate initial mesh size value.
- initial mesh tab
    - "fixed for all conductors" is turned on
    - “edge mesh length” and “vertex mesh length” values are filled in with the value obtained from the "use initial minimal mesh size".
    - turned on "custom Target mesh size" and "wavelength(25e6)/10" value is entered.

A parametric sweep of the separation distance is executed to determine the CCD, efficiency, and SRF. An example of the final design is shown in Figure 3.2-5.

The S-Parameter results of the parametric simulations are plotted. The peak efficiency and SRF results at the CCD are checked against our specifications. If the targets aren’t met, the board design is changed again according to section 3.2.2.5. Otherwise, the design is complete. A flowchart of the complete design flow is presented in Figure 3.2-6

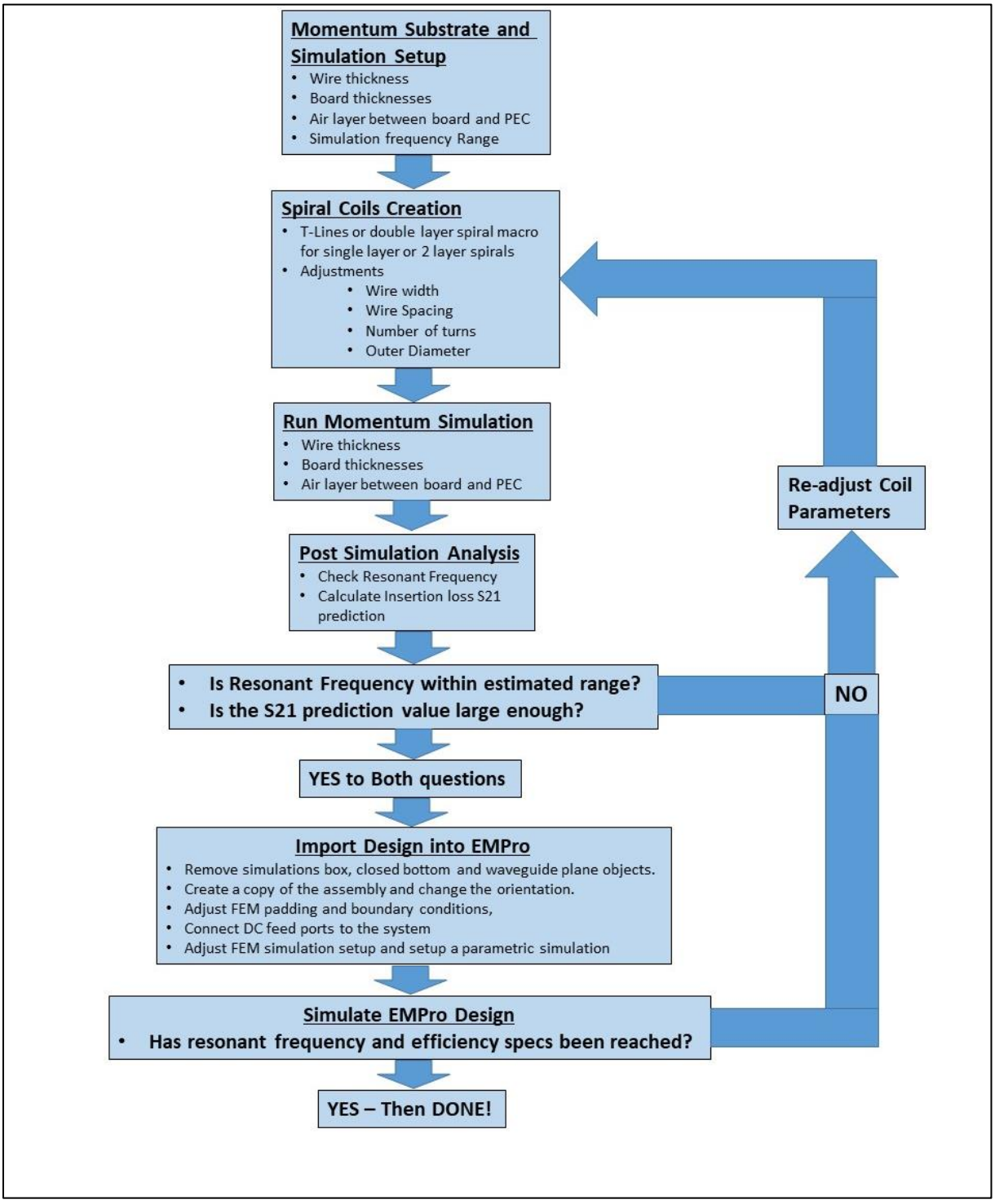


Figure 3.2-6 MCR-WPT COILS SYSTEM DESIGN FLOW.

3.2.3 Simulations, Results, and Summary

3.2.3.1 Single Layer MCR-WPT PCB Coils Specifications

Before going into the simulation setup, we establish the specifications for the Single Layer self-resonant MCR-WPT coil system. The specifications are as follows

- Maximum current through source/load coils 1.2A
- Number of outer coil turns 10
- Minimum trace width design rule 8 mils
- Maximum Length (Cellphone) 5 inches
- Maximum Width (Cellphone) 2.5 inches
- Minimum S21 -1.3dB
- Fundamental Frequency of Operation 6.78MHz ±0.5MHz

To satisfy the current specification we used the PCB trace width calculator based on the IPC-2221 standard [55] with 1oz copper to calculate the wire width. For internal and external layer traces, the minimum wire widths are 15.2mil (386μm) and 39.6mil (1mm) respectively. We used an inner coil wire width of 80 mils, which is twice the minimum to account for current spikes.

Since the outer coils inductively coupled to the inner coil with a 1:10 ratio, the maximum current, and minimum wire width are 1/10th the inner coil values resulting in a 0.12A maximum current requiring a 1.65mil(0.042mm) internal layer wire width. This width is below the PCB milling machine's minimum trace width design rule, and also has a large DC resistance loss of 0.306Ω/inch. We must use a much larger wire width for the outer coil. An exhaustive set of parametric simulations with multiple wire widths and spacings were done in 2mil increments to determine their optimal values to achieve the lowest SRF, which were found to be 40 and 16mils.

Table 3.2-2 Single layer MCR-WPT PSC parameters.

Parameter	Inner Coil (mils/mm)	Outer Coil (mils/mm)
Wire Width	*80/2.032*	*40 /1.016*
Wire Spacing	*NA*	*16/0.406*
Length 1	*3880/98.6*	*5000/127*
Length 2	*1380/33.0*	*2500/63.5*
Number of turns	*1*	*10*

respectively. The design parameters of our single layer MCR-WPT PSC boards are summarized in Table 3.2-2.

3.2.3.2 Simulations and Results of the Single Layer MCR-WPT PCB Coils

Following the Design methodology in section 3.2.2 and using the parameters in Table 3.2-2, the PSC board layout of the inner and outer coils was created in ADS Momentum. An S-Parameter simulation was run in the coils with a frequency range of 0.5 - 35MHz. The resulting S11 and S11-Resistance graphs are shown in Figure 3.2-7 and Figure 3.2-8 below.

Using the frequency value where the peak S11 occurs in Figure 3.2-7, the PSC board SRF is estimated to be 19.94MHz. The S11-resistance at 19.70MHz is 411.81Ω as seen in Figure 3.2-8.

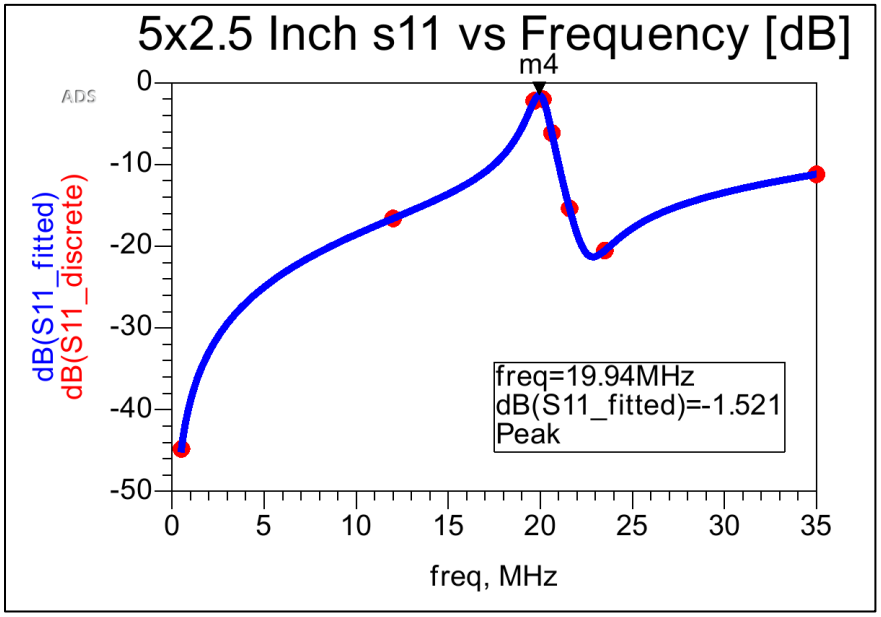


Figure 3.2-7 5x2.5in single layer PSC board S11 momentum simulation data display result.

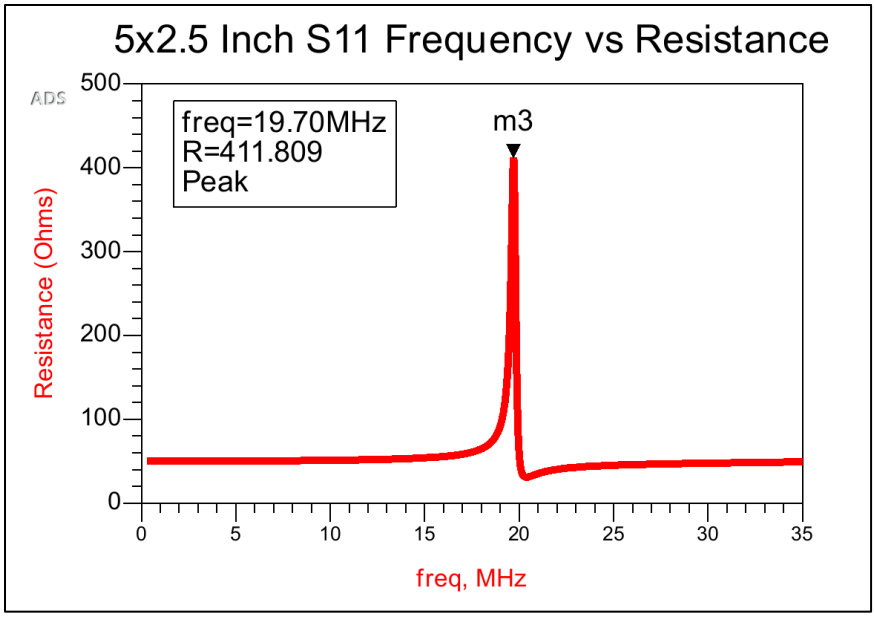


Figure 3.2-8 5x2.5in single layer PSC board S11-resistance momentum simulation data display result.

The estimated maximum *S21* of the MCR-WPT coils simulations using the insertion loss analysis was calculated to be 0.995dB.

Figure 3.2-9 shows the EMPro S21 simulation results for 1-3 inch separation distances in 0.5in increments. The resulting SRF, maximum S21, and CCD peak S21 are ~19.65MHz, -0.972dB and -1.494dB respectively. The results are summarized in Table 3.2-3.

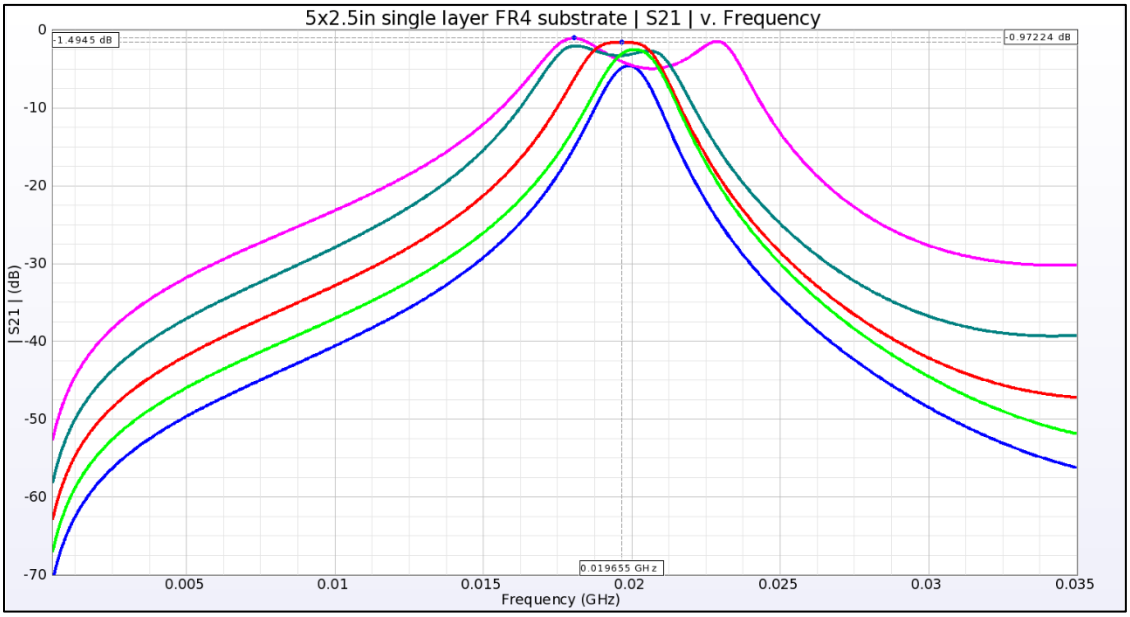


Figure 3.2-9 single layer MCR-WPT coils S21 EMPro simulation result.

Table 3.2-3 single layer MCR-WPT coils SRF and S21dB specifications vs simulation results.

Parameter	**Specification**	**Momentum Results**	**EMPro Results**
Self-Resonant Frequency (SRF)	6.78MHz	19.94MHz	19.65MHz
S21 dB at the CCD	-1.3dB	-0.995dB	-1.494dB
Maximum EMPro S21 observed	NA	NA	-0.972dB

From Table 3.2-3, the S21 and the SRF values from the EMPro and Momentum simulations closely match. The predicted Momentum S21, and the EMPro maximum peak and critical coupling peak S21 values are -0.995dB, -0.972dB and -1.494dB respectively. The SRF obtained from the EMPro and Momentum simulations are both near ~20MHz with a difference of 0.3MHz, which is much higher than our 6.78MHz specification. To achieve our frequency specification with single layer MCR-WPT coils, we must either increase the number of turns or add an external capacitor.

In the first instance, increasing the number of turns of the outer coil reduces the inner coil diameter. This would allow less flux to flow through the coils resulting in decreased efficiency. We also can't increase the number of turns beyond the maximum number of turns specification.

Other alternatives are to add an external capacitor as done in [16] and [56], or to increase wire thickness. Adding an external capacitor to the outer coils or increasing the wire thickness makes them too bulky for our portable electronics application. For these reasons, single layer design was aborted and double layer MCR-WPT design was explored.

3.3 Double and Multi-Layer MCR-WPT Coils and Proposed 6.78MHz MCR-WPT Coils for small electronics Devices

Multi-layer MCR-WPT PSCs using the Rezence standard with a frequency of 6.78MHz share all the loss mechanisms and parasitic capacitances of their single layer MCR-WPT PSC

counterparts. Due to the additional parasitic capacitances in-between layers, the self-resonant frequency (SRF) of the coils is reduced. On the other hand, there are additional resistive losses due to the proximity effect between layers that also need to be considered.

In this section, we look at different types of multilayer MCR-WPT coils proposed in other papers. We then present a novel multilayer MCR-WPT design for small electronic devices. Finally, we analyze the effects of multilayer parameters on the SRF and efficiency of the novel design.

3.3.1 Double Layer Parallel and Series Stacked MCR-WPT coils

As mentioned in section 3.1.1, the stacked series and stacked parallel inductors shown in Figure 3.1-1 (d) and (f) respectively are 2 types of multi-layer inductors in RF Applications. Both of these configurations have been investigated for use in MCR-WPT coils in other publications with the purpose of increasing system efficiency, reducing SRF, and reducing the dimensions of the MCR-WPT coils. We briefly go through their findings below.

3.3.1.1 Parallel Stacked MCR-WPT Coils

Parallel stacked MCR-WPT coils were studied in [57], with an operation frequency of 13.56MHz. The layers were connected with a conductive shorting wall on the outside edges of the

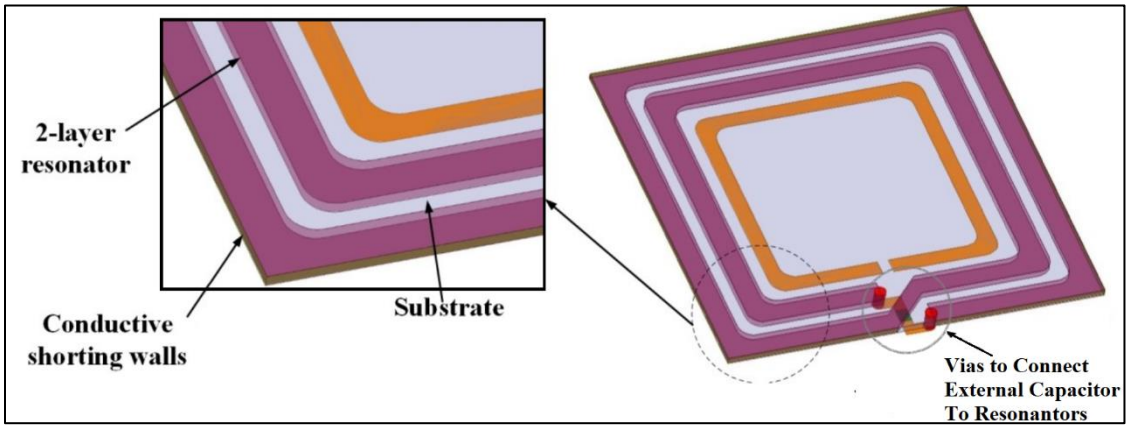


Figure 3.3-1 Geometry of double layer parallel stacked MCR-WPT coils proposed in [57].

PSC board as well as 2 vias at the ends of the spirals which can connect to an external capacitor. Figure 3.3-1 shows the geometry of the parallel double layer MCR-WPT board.

Their results show an improvement in transmission efficiency over the single layer MCR-WPT counterpart from 77.51% to 83.51%, with relatively no change to the SRF. The constant SRF is expected as there is no voltage difference between layers, resulting in no interlayer capacitance. Also by placing the spiral inductors in parallel, where their separation distances are much less than their lateral dimensions, they experience strong mutual inductance resulting in no change to the overall inductance as discussed in section 3.1.3.2. Since using a stacked parallel MCR-WPT coils configuration is unable to reduce the SRF of our system, they can't be used in our application.

3.3.1.2 Series Stacked MCR-WPT Coils

Series stacked inductors have been used to implement multilayer double layer MCR-WPT coils in [29] and [30]. They used slightly different implementation approaches for different applications. We go through these implementations in this section.

The MCR-WPT Series stacked coils studied in [29], uses the series inductor design found in Figure 3.1-1 (d) as a resonator. They use square shaped coils with an outer length of 11.3inches

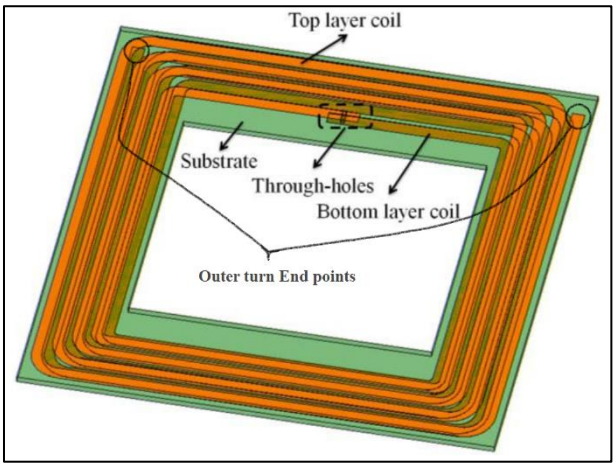


Figure 3.3-2 Geometry of double layer series stacked MCR-WPT resonator coil proposed in [29].

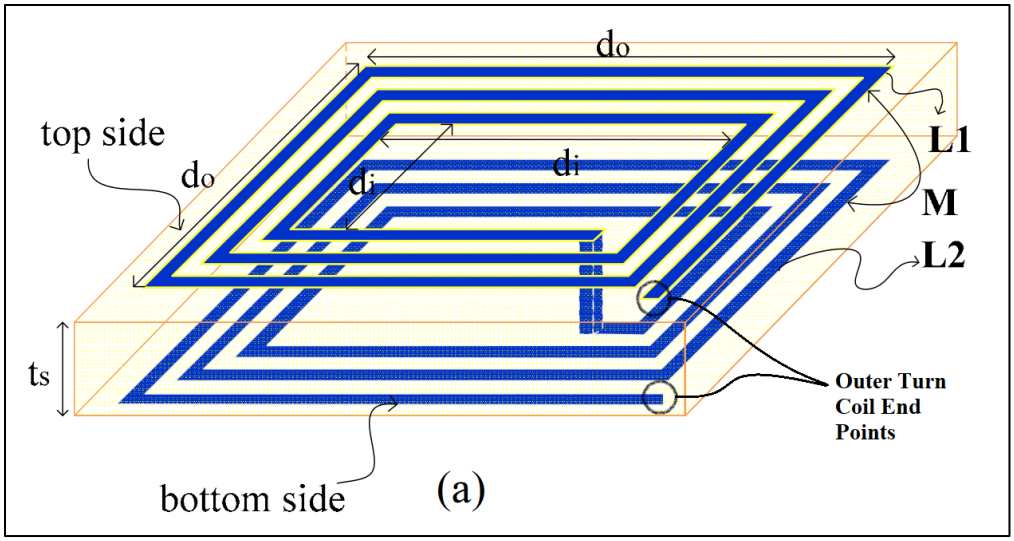


Figure 3.3-3 Geometry of double layer series stacked MCR-WPT resonator coil proposed in [30].

(288mm). Both layers have 3.875 turns and layers were connected with one via at the endpoints on the innermost turns. The geometry of the resonator is shown in Figure 3.3-2. This configuration was shown to have an SRF of ~4MHz through simulations and measurements. Simulations with 5.875 turns were also shown to have an SRF of below 3MHz

In [30], a comparison between resonant single layer and double layer series stacked spirals with the same size was conducted. Square shaped spiral coils with an outer length of 0.787inch (20mm) were used and with ~17 turns each. The series stacked spiral coil geometry that was used is shown in Figure 3.3-3. It is slightly different than the resonator geometry shown in Figure 3.3-2, as has the outer ends points of both coils in the same corner. This allowed for the upper and bottom layers to have a whole number turn values. Measurements were done on the coils without an inner coil, and the resulting SRF of the single and double layer coils were 71MHz and 21.5MHz.

These research studies have shown that a lower SRF can be realized by using resonant stacked series coils. The SRF of the coils in [30] was reduced by a factor of 3.3 and an SRF below 3MHz was achieved in [29]. This reduction in SRF is due to the increased coupling capacitance in between layers and the increased inductance by placing the inductors in series. From section

3.1.4.1, the capacitance was shown to ideally increase by 4 according to equation (*3.6*), and the inductance with each additional layer ideally by a factor of n^2 from equation (*3.2*) in 3.1.3.1. These capacitance and inductance increases translate into a decrease in SRF by 1/4.

There is a drawback associated with the series stacked spiral coils presented in [29] and [30]. The main disadvantage is that a via is required in-between the layers on the innermost turn. Because of this, a complete turn cannot be created on the innermost turn of both layers since the leg where the via connects the layers does not have wires on top one another. This causes the total inductance and interlayer capacitance to be reduced. Another issue is that we also do not have access to machinery to create PSC boards with vias for prototyping.

3.3.2 Novel MCR-WPT Multi-Layer Design

In this section, we present our novel multilayer MCR-WPT PSC board design. Similar to the series stacked spiral coils, it reduces the SRF of the MCR-WPT coils system by taking advantage of the interlayer capacitance and mutual inductance between layers. On the other hand, it does not require any vias which simplifies its design and increases interlayer capacitance.

An example double layer MCR-WPT PSC using our novel design is shown in Figure 3.3-4. The dark red bottom layer consists of an inner source/load coil with a larger wire width, and multi-turn outer resonator coil with a smaller wire width. The yellow top layer has an identical multi-turn resonator coil which has been mirrored on the green Y-axis so that the coil endpoints are located as seen in Figure 3.3-4. Both resonators have outer diameters of D1 and D2 and are separated by a dielectric substrate with a thickness of T_s.

The new design is not limited to the structure shown in Figure 3.3-4. The additional resonator coil on the second layer can be mirrored on the red X-axis, mirrored on the green Y-axis,

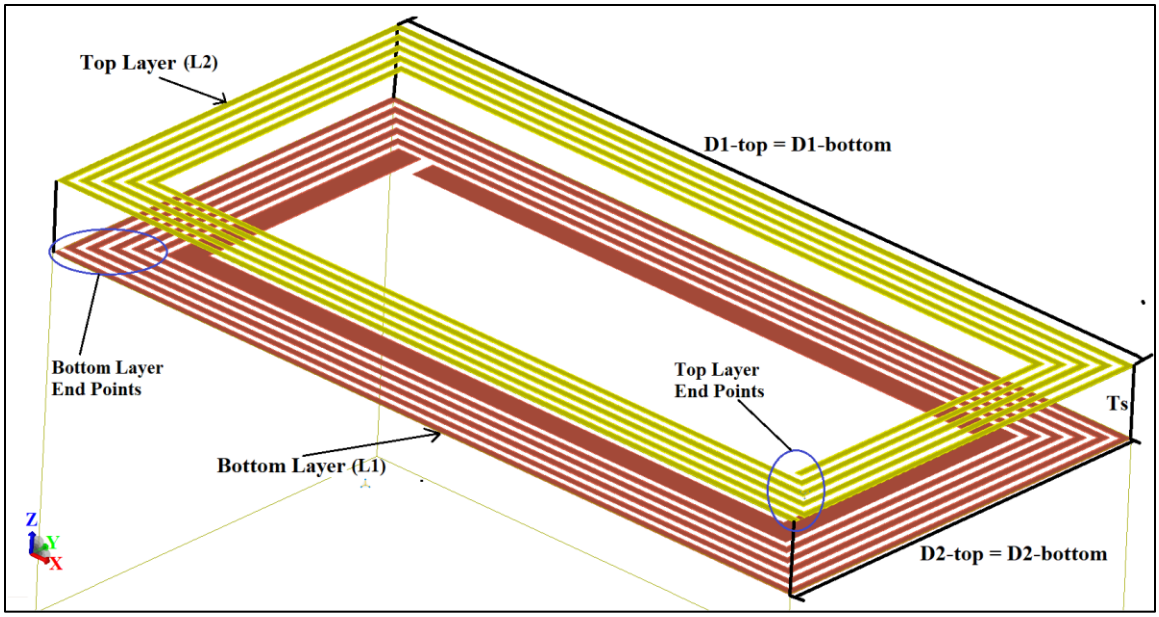


Figure 3.3-4 Novel double layer MCR-WPT resonator coils design to reduce the SRF.

or rotated around the Z-axis in blue, or any combination of these. It can also be used for any shape spiral coil such as hexagonal and circular spiral coils. More than one resonator coil can also be added on more layers to further reduce the SRF of the MCR-WPT coils system.

It should be noted that in the example shown in Figure 3.3-4, the corners of the turns are 90^{o} and not rounded. Rounded or curved corners could be used but the overall benefit is not expected to be significant. This is because it is easier to redesign the coils with 90^{o} turns as there are rectangular spiral inductor design macros in ADS Momentum with 90^{o} turns. Another reason is the wavelength of our frequency of operation is much longer than the longest side of coils. Hence loss due to wave reflections is small and can be ignored according to [58].

3.3.3 Effects of Multilayer Parameters on Resonance of Novel design

As mentioned in the previous section, our novel design can have two or more layers and have different dielectric substrate thicknesses. We will, therefore, analyze the effects of changing the number of layers, the substrate thickness, and the type of dielectric substrate have on the SRF and efficiency of the PSC board. This is done running simulations in Momentum to generate the

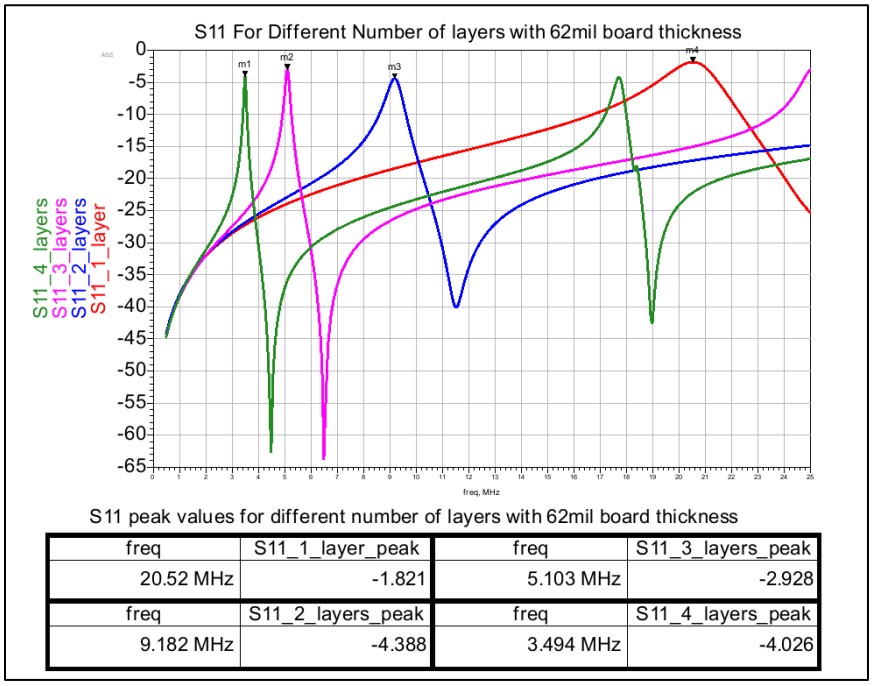
Table 3.3-1 MCR-WPT PSC parameters used in the different number of layers simulation test.

Parameters	**Inner Coil (mils/mm)**	**Outer Coil (mils/mm)**
Diameter 1 (D1)	**4420/112.2**	5000/127
Diameter 2 (D2)	1920/48.8	2500/63.5
Wire Width (W)	150/3.81	30/0.762
Wire Spacing (S)	10/0.254	12/0.305
Number of Turns (N)	1	7
PSC board thickness (T_s)	62.5/1.58	
Metal thickness (t)	1.4/0.0356	

S-Parameter results, then using the frequency value where the peak S11 dB value occurs we determine the resulting SRF of each simulation as described in section 3.2.2.3. All S-Parameter simulations were run with a frequency range of 0.5 - 25MHz and a step size of 1kHz.

3.3.3.1 Increasing the Number of Layers

Our first analysis investigates the effects of adding more resonator coil layers on the PSC board SRF. The simulation setup consists of an inner source/load coil and an outer resonator coil with the dimensions, and dielectric substrate thickness parameter values described in Table 3.3-1.



S11 peak values for different number of layers with 62mil board thickness

freq	S11_1_layer_peak	freq	S11_3_layers_peak
20.52 MHz	-1.821	5.103 MHz	-2.928
freq	S11_2_layers_peak	freq	S11_4_layers_peak
9.182 MHz	-4.388	3.494 MHz	-4.026

Figure 3.3-5 Momentum data display results for the effects of changing the number of layers on the SRF in the novel design with a 62mil PSC board thickness.

All of these parameters were held constant during the simulation analysis. Every resonator was identical except for the resonators on an even number layers, which were layer one mirrored about the Y-axis. The substrate thickness in between layers was 59.7mils, 29.15mils, and 19mils for the 2, 3 and 4 layer PSC boards respectively

The S11 simulation results for 1-4 layers is shown in Figure 3.3-5. The SRF of the PSC board is reduced with every layer added and the efficiency slightly fluctuated. But the SRF reduction factor (rf_{SRF}), which is the ratio of the SRFs when another layer is added, also decreases. The rf_{SRF} between the PSC boards with 1 and 2 layers and have SRFs of 20.52MHz and 9.182MHz respectively is 2.23. The rf_{SRF} between 2 and 3 layers, and 3 and 4 layers are 1.80 and 1.46 respectively. This decrease in rf_{SRF} is because the mutual inductance coupling and capacitive coupling between non-adjacent layers are not as strong as the coupling between adjacent layers.

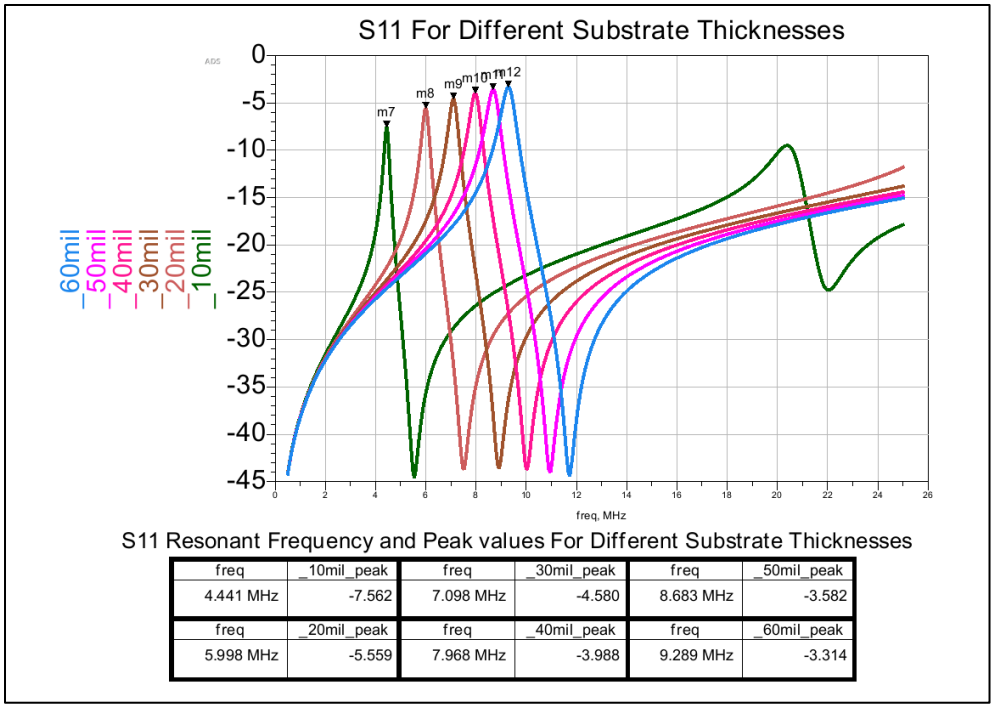
Finally, we can see that the peak S11 dB decreases between the boards with 3 and 4 layers. This is due to the reduced interlayer substrate thickness. We analyze the effects on different substrate thicknesses next.

3.3.3.2 Decreasing the Thickness of Substrate

For the next analysis, we investigate the effects of changing the substrate thickness on the SRF. The simulation setup consists of an inner source/load coil and an outer resonator coil with

Table 3.3-2 MCR-WPT PSC parameters for different substrate thicknesses simulation test.

Parameters	**Inner Coil (mils/mm)**	**Outer Coil (mils/mm)**
Diameter 1 (D1)	**4420/112.2**	5000/127
Diameter 2 (D2)	1920/48.8	2500/63.5
Wire Width (W)	50/1.27	21/0.533
Wire Spacing (S)	10/0.254	21/0.533
Number of Turns (N)	1	7
Metal thickness (t)	**2.8/0.0711**	



S11 Resonant Frequency and Peak values For Different Substrate Thicknesses

freq	_10mil_peak	freq	_30mil_peak	freq	_50mil_peak
4.441 MHz	-7.562	7.098 MHz	-4.580	8.683 MHz	-3.582
freq	_20mil_peak	freq	_40mil_peak	freq	_60mil_peak
5.998 MHz	-5.559	7.968 MHz	-3.988	9.289 MHz	-3.314

Figure 3.3-6 Momentum data display results for the effects of changing the dielectric substrate thickness on SRF in the double layer novel design.

the dimensions and dielectric substrate thickness parameter values described in Table 3.3-2. All the parameters were held constant and a double layer PSC board was used during the simulation analysis. The substrate thickness is changed in 10mil increments, ranging between 10-60mils.

The S11 simulation results for changing substrate thickness is shown in Figure 3.3-5. Both the PSC board SRF and peak S11 dB reduced as the dielectric substrate thickness decreased. The reduced SRF is caused by increased mutual induction between layers when the separation distance decreases as described in 3.1.3.2. The peak S11 dB also reduces with decreasing substrate thickness suggesting an efficiency reduction. As mentioned in section 3.1.4.4, this is caused by the proximity effect resistive losses which increase when the spacing between layer wires decreases.

3.3.3.3 Type of Substrate

In our final analysis, we investigate the effects of changing the type of dielectric substrate on the SRF. The simulation setup consists of an inner source/load coil and an outer resonator coil

Table 3.3-3 MCR-WPT PSC parameters for different dielectric substrate types simulation test.

Parameters	**Inner Coil (mils/mm)**	**Outer Coil (mils/mm)**
Diameter 1 (D1)	**7000/177.8**	8000/203.2
Diameter 2 (D2)	3000/76.2	4000/101.6
Wire Width (W)	50/1.27	50/1.27
Wire Spacing (S)	10/0.254	75/1.905
Number of Turns (N)	1	4
PSC board thickness (T_s)	32/1.58	
Metal thickness (t)	**2.8/0.0711**	

with the dimensions, and dielectric substrate thickness parameter values described in Table 3.3-3. All the parameters were held constant and a double layer PSC board was used during the simulation analysis. The dielectric substrates used in this investigation have a ε_r ranging from 2 and 12.9.

The S11 simulation results for multiple the dielectric substrates with different ε_r is shown in Figure 3.3-5. The SRF of the PSC board was reduced as the ε_r of the substrate increased. The increased ε_r causes the parasitic capacitance between layers to increase, resulting in a reduced SRF. On the other hand, the peak S11 dB remains constant while changing ε_r.

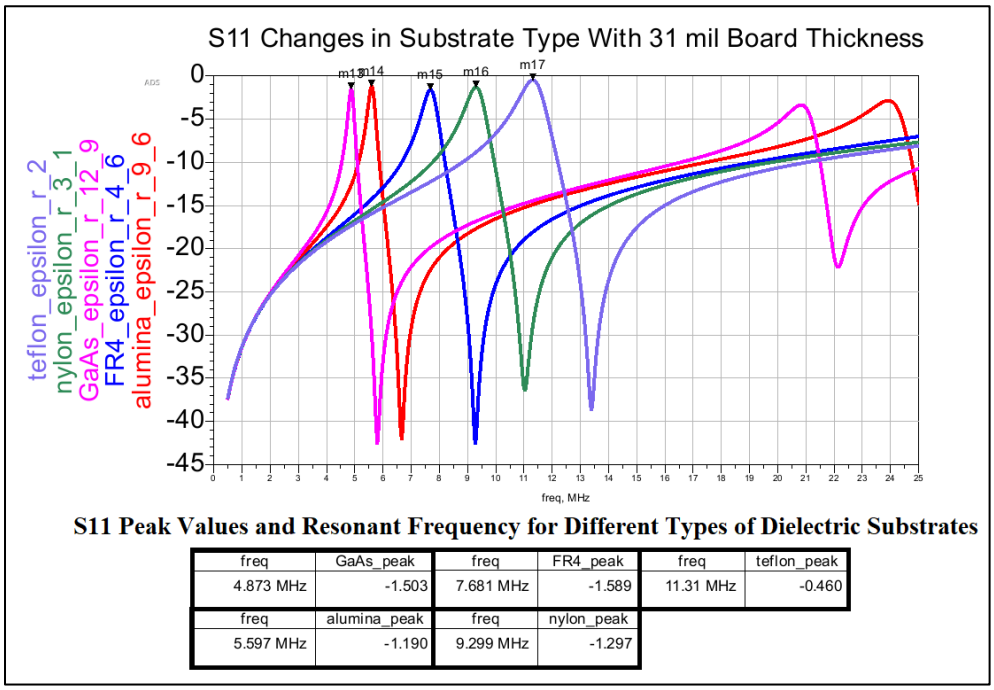


Figure 3.3-7 Momentum data display results for the effects of changing the type of dielectric substrate on SRF in the double layer novel design.

3.4 Simulations and Experimental Results, and Discussion of Proposed System.

3.4.1 Double Layer MCR-WPT PCB Coil Specifications

Before going into the simulation setup, we re-establish the specifications for the Double Layer self-resonant MCR-WPT coil system, which are the same for the single layer MCR-WPT coils. The specifications are as follows

- Maximum current through source/load coils 1.2A
- Number of outer coil turns 10
- Minimum trace width design rule 8 mils
- Maximum Length (Cellphone) 5 inches
- Maximum Length (Tablet) 8 inches
- Maximum Width (Cellphone) 2.5 inches
- Maximum Width (Cellphone) 4 inches
- Minimum S21 -1.3dB
- Fundamental Frequency of Operation 6.78MHz ±0.5MHz

To satisfy the current specification we took into consideration the added proximity effect resistive loss from the second layer coil as well as the IPC-2221 PCB trace width standard. The thickness couldn't be too large as we are limited by the skin depth. A maximum thickness of 2oz could be used, which is the approximately 3X the skin depth of copper. Using the PCB trace width calculator based on the IPC-2221 standard [55] with 2oz copper, for external and internal layer traces, the minimum wire widths are 7.6mil (193µm) and 19.8mil (0.5mm) respectively. We used

an inner coil wire width of 50mils, which is twice the minimum to account for current spikes. The PSC board thickness (T_s) of all the designs is 32mils/1.58mm.

3.4.2 5x2.5in^2 FR4 Double Layer MCR-WPT PSC Coil Design for Smartphones

3.4.2.1 Design Specifications

We achieved a resonant frequency close to our 6.78MHz target at the CCD using a 1:7 inner to outer coil turn ratio. The maximum current through the outer coil wire is 1/7th the inner coil value, resulting in ~0.172A maximum current requiring a minimum inner layer wire width of 1.3mil(0.033mm). This wire width is below the PCB milling machine's minimum trace width design rule and has a large DC resistance loss of 0.601Ω/inch. A much larger wire width for the outer coil was used. Using the design flow illustrated in Figure 3.2-6, the wire width and spacing of 40 and 16 mils respectively was used. The design parameters of our single layer MCR-WPT PSC boards are summarized in Table 3.4-1.

3.4.2.2 Momentum and EMPro Simulation Results and Discussion

Following the Design methodology in section 3.2.2 and using the parameters in Table 3.4-1, the PSC board layout of the inner and outer coils was created in Momentum. An S-Parameter simulation was run on the coils with a frequency range of 0.5 - 25MHz and a step size of 1kHz. The resulting S11dB and S11-Resistance graphs are shown in Figure 3.4-1 and Figure 3.4-2 below.

Table 3.4-1 5x2.5in^2 double layer FR4 MCR-WPT PSC parameters.

Parameter	Inner Coil (mils/mm)	Outer Coil (mils/mm)
Wire Width	*50/1.27*	*21/0.533*
Wire Spacing	*NA*	*21/0.533*
Length 1	*4420/112*	*5000/127*
Length 2	*1920/48.8*	*2500/63.5*
Number of turns	*1*	*7*

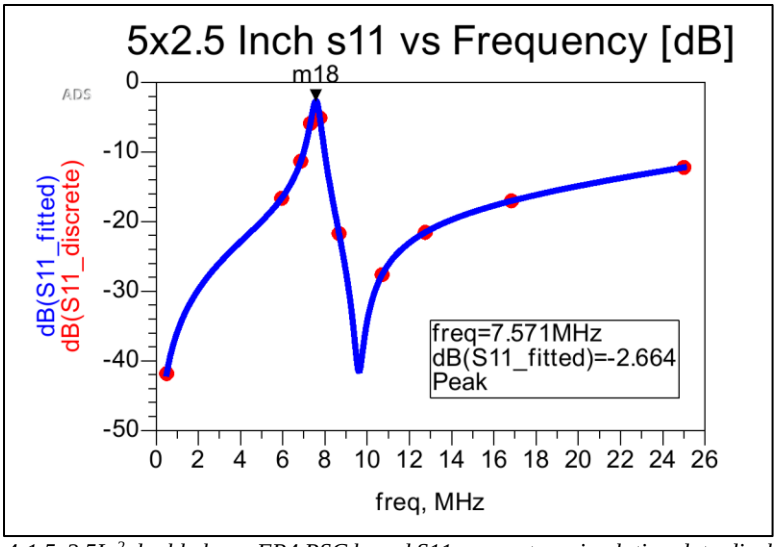


Figure 3.4-1 5x2.5In^2 double layer FR4 PSC board S11 momentum simulation data display result.

Using the frequency value where peak S11 dB occurs in Figure 3.4-1, the PSC board SRF is estimated to be 7.571MHz. The S11-resistance at 7.586MHz is 326.9Ω as seen in Figure 3.4-2.The estimated maximum *S21* of the MCR-WPT coils simulations using the insertion loss analysis was calculated to be 1.235dB.

Figure 3.4-3 shows the EMPro S21 simulation results for 0.5-3 inches separation distances in 0.5in increments. The resulting SRF, maximum S21, and CCD peak S21 are ~6.43MHz, -1.472dB and -2.099dB respectively. The results are summarized in Table 3.4-2.

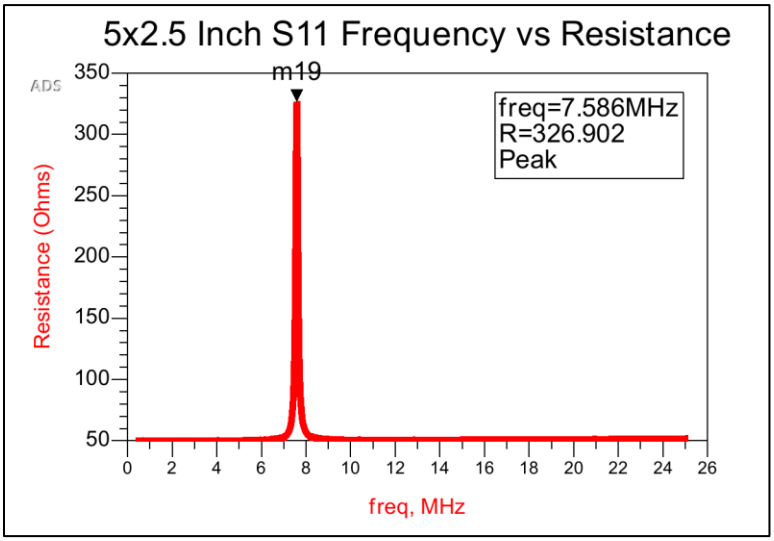


Figure 3.4-2 5x2.5In^2 double layer FR4 PSC board S11-resistance momentum simulation data display result.

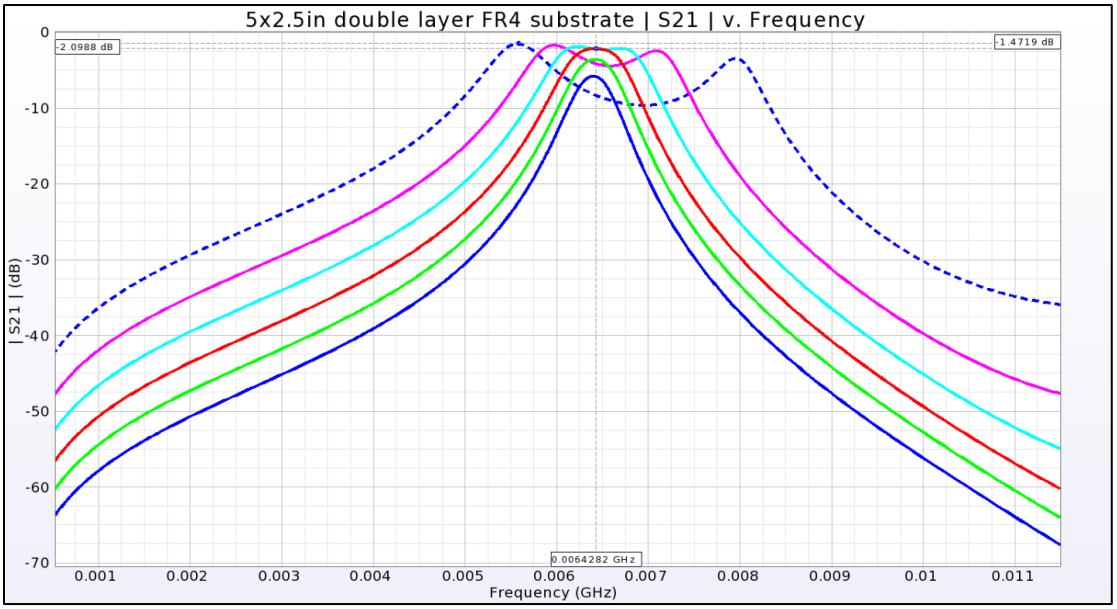


Figure 3.4-3 5x2.5in^2 double layer FR4 MCR-WPT coils S21 EMPro simulation result.

From Table 3.4-2 we see that the S21 and the SRF values from the EMPro and Momentum simulations closely matched. The SRF from Momentum and EMPro simulations differ by ~1.1MHz, and the EMPro CCD SRF is ~0.35MHz less than our target operational frequency. There are a few benefits of having a lower CCD SRF as described in section 4.1.3.1. The predicted Momentum S21dB is within 0.2dB and 0.9dB of the maximum peak and the critical coupling peak EMPro S21dB values, but both of the EMPro S21dB values are below the -1.3dB specification. Finally, the efficiency at the 2.0in CCD with a S21 of -2.099dB was calculated to be 61.7%.

3.4.2.3 Post EMRro Harmonic Balance Transient Simulation Results at 6.78MHZ

Harmonic Balance simulations were run on the 5x2.5In FR4 double layer MCR-WPT coils at 0.5in, 1in, and 1.5in separation distances. The simulation is set up as seen in Figure 3.4, and the EMPro FEM S-Parameter simulation result EM model placement for each separation distance

Table 3.4-2 5x2.5In^2 double layer FR4 MCR-WPT coils SRF and S21dB specifications vs simulation results.

Parameter	**Specification**	**Momentum Results**	**EMPro Results**
Self-Resonant Frequency (SRF)	6.78MHz	7.571MHz	6.43MHz
S21 dB at CCD	-1.3dB	-1.236dB	-2.099dB
Maximum EMPro S21 observed	NA	NA	-1.472dB

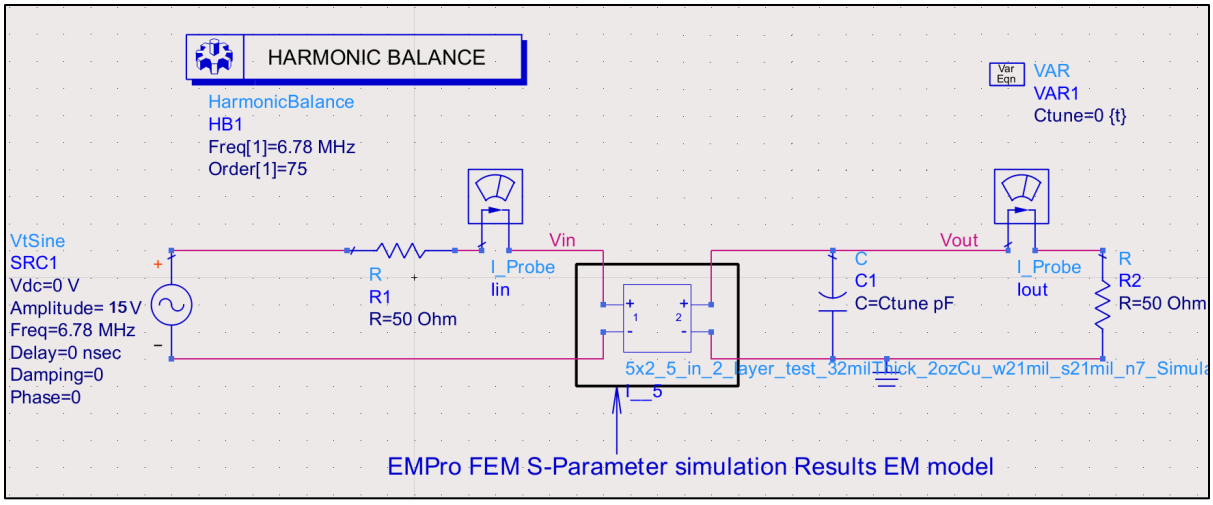
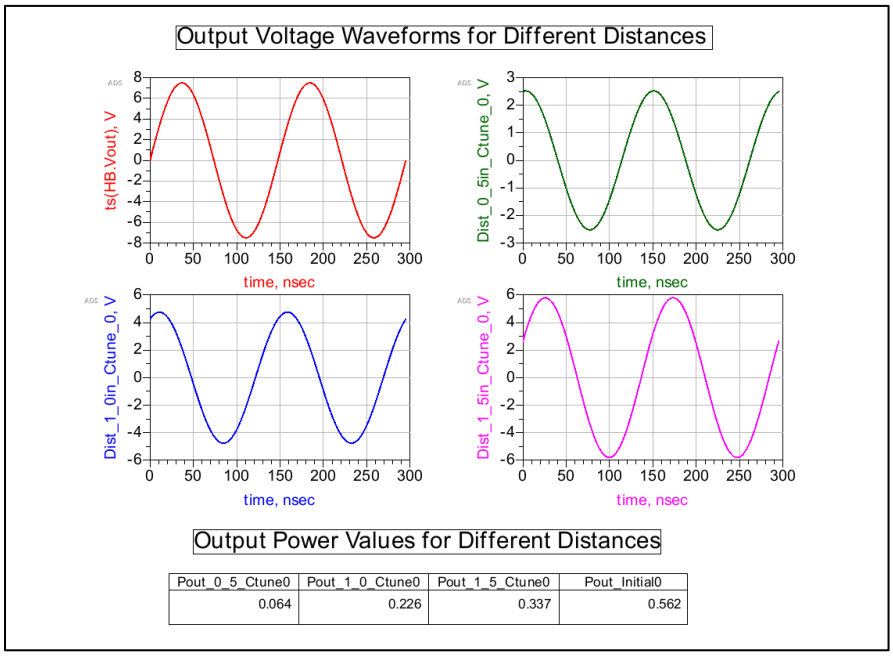


Figure 3.4 4 Post EMPro schematic setup for harmonic balance simulation on the MCR-WPT coils in Keysight ADS

is shown. The transient waveforms simulation results were plotted and the results are shown in Figure 3.4-4. The output power is tabulated below the plots.

3.4.2.4 Experimental Results

To verify the 5x2.5in^2 FR4 double layer MCR-WPT coils design, experimental tests were done using a function generator input. The design was connected at the input to a sine wave with



Pout_0_5_Ctune0	Pout_1_0_Ctune0	Pout_1_5_Ctune0	Pout_Initial0
0.064	0.226	0.337	0.562

Figure 3.4-4 5x2.5In^2 double layer FR4 MCR-WPT coil design harmonic balance transient and output power simulation data display results for multiple separation distances.

Table 3.4-3 5x2.5in^2 double layer FR4 MCR-WPT coils output peak voltage and apparent power at different separation distances.

Separation Distance	Peak Voltage (V)	Apparent Power (Watt)
0.5 Inch	2.4	0.0576
1.0 Inch	4.9	0.2401
1.5 Inch	3.95	0.156

a 7.5V peak at 6.78MHz and the output was connected to a 50Ω load resistor. To hold the coils in place at the same distances as the simulations, 0.5in slots were cut into cardboard and the coils are slotted into place and the voltage signal was then measured. The test setups can be seen in Figure 4.1-10 in section 4.1.4, where the input alligator clips are connected to the output of the Function Generator, and the output is connected to a 50Ω resistor.

The output voltage test results using the Agilent 200MHz oscilloscope. The test results for 0.5in, 1.0in and 1.5in separation distances are shown in Figure 3.4-5. The output power was calculated using equation (G.*1*). The output peak voltages and the calculated output powers are tabulated in Table 3.4-3. A peak efficiency of 42.7% was calculated at the 1.0in CCD.

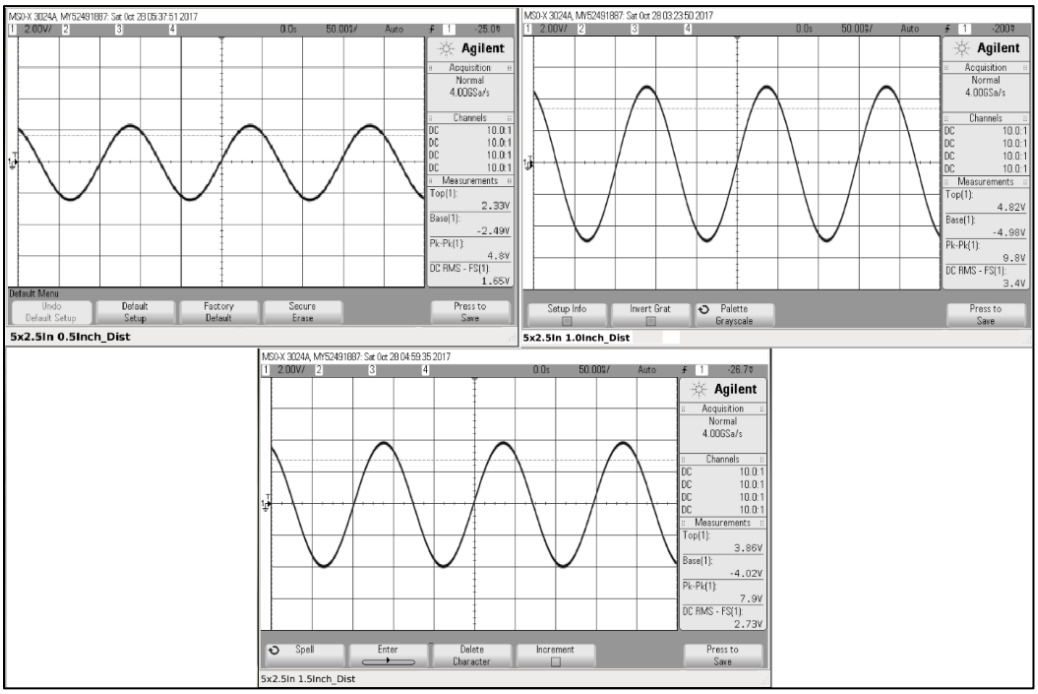


Figure 3.4-5 5x2.5In^2 double layer FR4 MCR-WPT Coil test with function generator input at 0.5-1.5 inch separation distances.

3.4.2.5 Harmonic Balance Simulation and Experimental Tests Results Summary

The output power values of the Harmonic Balance and function generator experimental results at different separation distance are shown in Table 3.4-4. From the table we see that the Harmonic Balance and experimental output power results are pretty close at the 0.5in and 1.0in distances. At the 1.5 inch distance, the Harmonic Balance power increased but the experimental decreased. This suggests that the maximum operating distance is smaller for the experimental test.

Table 3.4-4 5x2.5In^2 double layer FR4 MCR-WPT coils harmonic balance and experimental peak output power results comparison.

Separation Distance	Harmonic Balance Output Power	Function Generator Output power
0.5 Inch	0.064 Watt	0.0576 Watt
1.0 Inch	0.226 Watt	**0.2401 Watt**
1.5 Inch	0.337 Watt	0.156 Watt

3.4.3 5x2.5in^2 Alumina Double Layer MCR-WPT PCB Coil Cellphone Design

3.4.3.1 Design Specifications

As mentioned in section 3.4.2.2, the critical coupling peak EMPro S21dB value of the FR4 double layer design, was below the -1.3dB Rezence specification. Since changing the dielectric substrate with another material with a higher permittivity was shown to reduce the resonant frequency while maintaining a relatively constant efficiency, we investigate an alternative double late design with an alumina ceramic substrate. Only Momentum and EMPro simulations were conducted since we did not have access to the alumina ceramic material for prototyping.

We achieved a resonant frequency close to our 6.78MHz target at the CCD using a 1:5 inner to outer coil turn ratio. The maximum current through the outer coil wire are 1/5th the inner coil value, resulting in ~0.24A maximum current, requiring a minimum inner layer wire width of

Table 3.4-5 5x2.5In^2 double layer alumina MCR-WPT PSC parameters.

Parameter	Inner Coil (mils/mm)	Outer Coil (mils/mm)
Wire Width	*50/1.27*	*30/0.762*
Wire Spacing	*NA*	*29/0.737*
Length 1	*4420/112*	*5000/127*
Length 2	*1920/48.8*	*2500/63.5*
Number of turns	*1*	*5*

2.1mil(0.055mm). This wire width is below the PCB milling machine's minimum trace width design rule and has a large DC resistance loss of 0.231Ω/inch. A much larger wire width for the outer coil was used. Using the design flow illustrated in Figure 3.2-6, the wire width and spacing of 30 and 29 mils respectively was used. The design parameters of our single layer MCR-WPT PSC boards are summarized in Table 3.4-5.

3.4.3.2 Momentum and EMPro Simulation Results and Discussion

Following the Design methodology in section 3.2.2 and using the parameters in Table 3.4-5, the PSC board layout of the inner and outer coils was created in Momentum. An S-Parameter simulation was run on the coils with a frequency range of 0.5-25MHz and a step size of 1kHz. The resulting S11dB and S11-Resistance graphs are shown in Figure 3.4-6 and Figure 3.4-7 below.

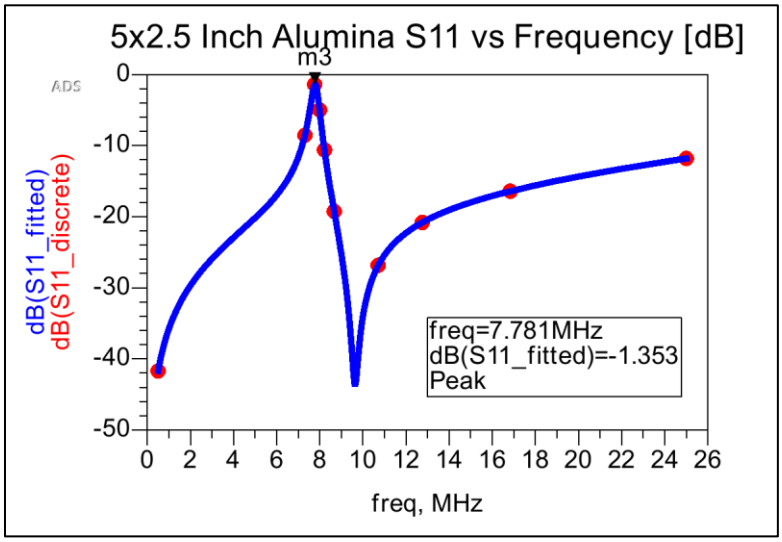


Figure 3.4-6 5x2.5in double layer Alumina PSC board S11 momentum simulation data display result.

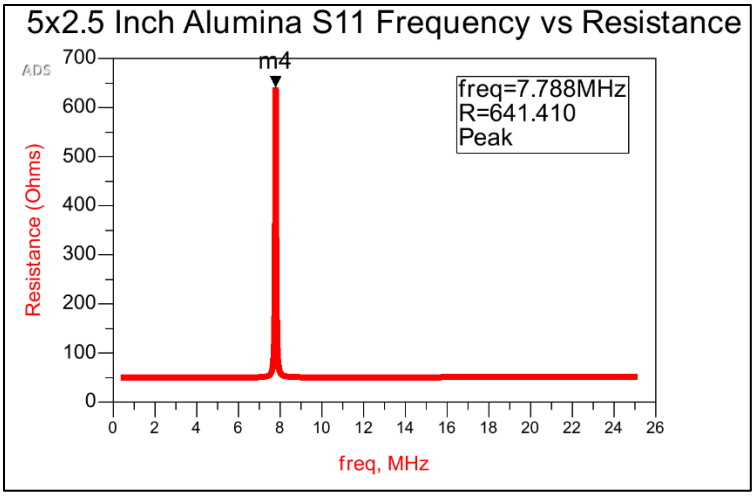


Figure 3.4-7 5x2.5in double layer Alumina PSC board S11-resistance momentum simulation data display result.

At the peak S11 dB in Figure 3.4-6, the PSC board SRF is estimated to be 7.781MHz. The S11-resistance at 7.788MHz is 641.4Ω as seen in Figure 3.4-7. The estimated maximum *S21* of the MCR-WPT coils simulations using the insertion loss analysis was calculated to be 0.652dB.

Figure 3.4-8 shows the EMPro S21 simulation results for 0.5-3 inches separation distances in 0.5in increments. The resulting SRF, maximum S21, and CCD peak S21 are ~6.65MHz, -0.618dB and -0.938dB respectively. The results are summarized in Table 3.4-6.

From Table 3.4-6 we see that the S21 and the SRF values from the EMPro and Momentum simulations closely matched. The SRF from the Momentum and EMPro simulations differ by ~1.1MHz, and the EMPro CCD SRF is ~0.12MHz less than the target operational frequency. The predicted Momentum S21dB is within 0.03dB and 0.3dB of the maximum peak and the critical coupling peak EMPro S21dB values. Both the maximum peak and the critical coupling peak EMPro S21dB values are above the -1.3dB specification by 0.682dB and 0.362dB respectively. Finally, the efficiency at the 2.0in CCD with a S21 of -0.938dB was calculated to be 80.6%.

Table 3.4-6 5x2.5in^2 double layer alumina MCR-WPT coils SRF and S21dB specifications vs simulation results.

Parameter	**Specification**	**Momentum Results**	**EMPro Results**
Self-Resonant Frequency (SRF)	6.78MHz	7.781MHz	6.65MHz
S21 dB at CCD	-1.3dB	-0.652dB	-0.938dB
Maximum EMPro S21 observed	NA	NA	-0.618dB

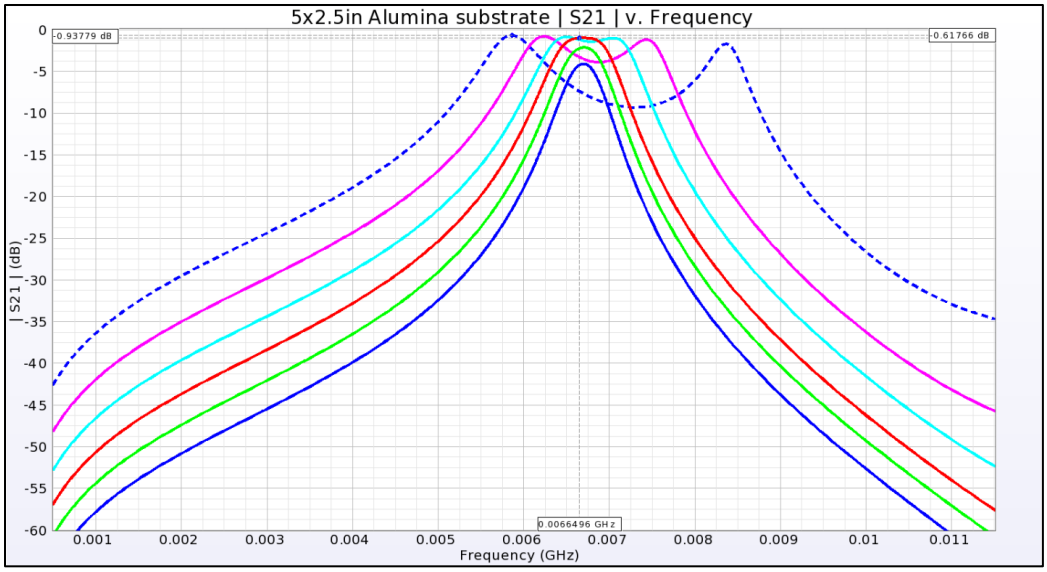


Figure 3.4-8 5x2.5in^2 double layer Alumina MCR-WPT coils S21 EMPro simulation results.

3.4.4 8x4in^2 FR4 Double Layer MCR-WPT PCB Coil Design for Tablets

3.4.4.1 Design Specifications

Using a 1:4 inner to outer coil turn ratio, a resonant frequency close to our 6.78MHz target at the CCD was realized. The maximum current through the outer coil wire is 1/4 the inner coil value, resulting in ~0.3A maximum current, requiring a minimum inner layer wire width of 2.9mil(0.074mm). This wire width is below the PCB milling machine's minimum trace width design rule and has a large DC resistance loss of 0.170Ω/inch. A much larger wire width for the outer coil was used. Using the design flow illustrated in Figure 3.2-6, the wire width and spacing of 50 and 75 mils respectively was used. The design parameters of our single layer MCR-WPT PSC boards are summarized in Table 3.4-7.

3.4.4.2 Momentum and EMPro Simulation Results and Discussion

Following the Design methodology in section 3.2.2 and using the parameters in Table 3.4-7, the PSC board layout of the inner and outer coils was created in Momentum. An S-Parameter

Table 3.4-7 8x4in² double layer FR4 MCR-WPT PSC parameters.

Parameter	Inner Coil (mils/mm)	Outer Coil (mils/mm)
Wire Width	*50/1.27*	*50/1.27*
Wire Spacing	*NA*	*75/1.91*
Length 1	*7000/178*	*8000/203*
Length 2	*3000/76.2*	*4000/102*
Number of turns	*1*	*7*

simulation was run on the coils with a frequency range of 0.5 - 25MHz and a step size of 1kHz. The resulting S11dB and S11-Resistance graphs are shown in Figure 3.4-9 and Figure 3.4-10.

Using the frequency value where peak S11dB occurs in Figure 3.4-9, the PSC board SRF is estimated to be 7.8MHz. The S11-resistance at 7.816MHz is 481.3Ω as seen in Figure 3.4-10.The estimated maximum S21dB of the MCR-WPT coils simulations using the insertion loss analysis was calculated to be 0.858dB.

Figure 3.4-11 shows the EMPro S21 simulation results for 0.5-3.5 inch separation distances in 0.5in increments. The resulting SRF, maximum S21, and CCD peak S21 are ~6.61MHz, -0.943dB and -1.276dB respectively. The results are summarized in Table 3.4-8.

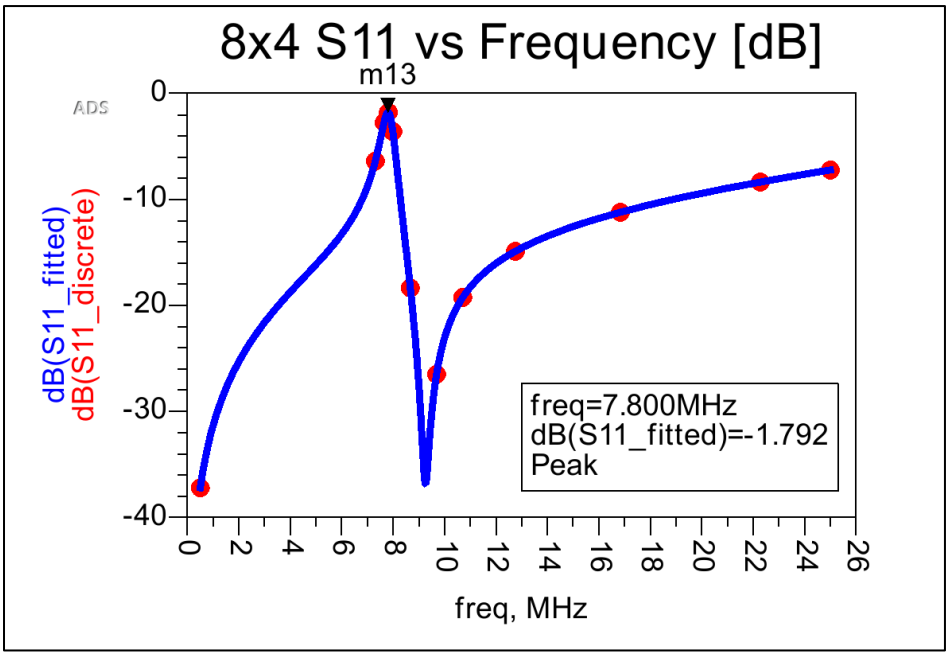


Figure 3.4-9 8x4In² double layer FR4 PSC board S11 momentum simulation data display result.

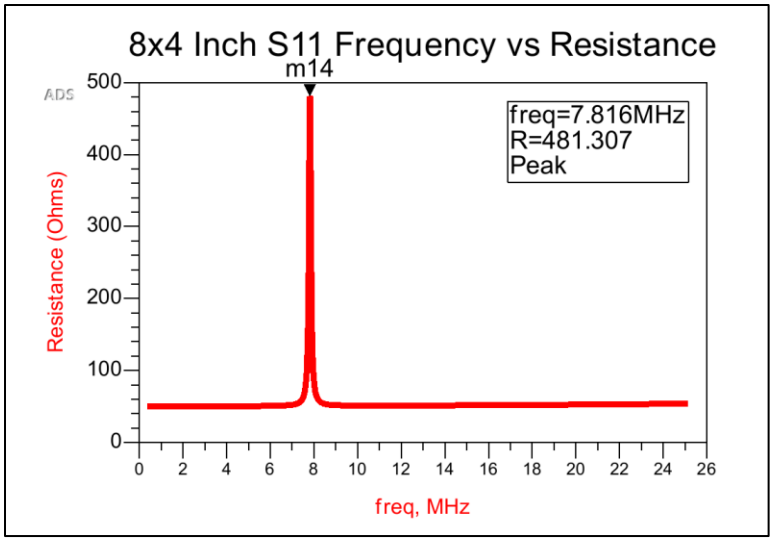


Figure 3.4-10 8x4In^2 double layer FR4 PSC board S11-resistance momentum simulation data display result.

From Table 3.4-8 we see that the S21dB and the SRF values from the EMPro and Momentum simulations closely matched. The SRF from Momentum and EMPro simulations differ by ~1.2MHz, and the EMPro CCD SRF is ~0.17MHz less than our target operational frequency. The predicted Momentum S21dB value is within 0.09dB of the maximum EMPro S21dB value, and 0.42dB within the critical coupling peak EMPro S21. Both the maximum peak and the critical coupling peak EMPro S21dB values are above the -1.3dB specification by 0.357dB and 0.024dB respectively. Finally, with a S21 of -1.276dB at the 2.5in CCD, results in a 74.5% efficiency.

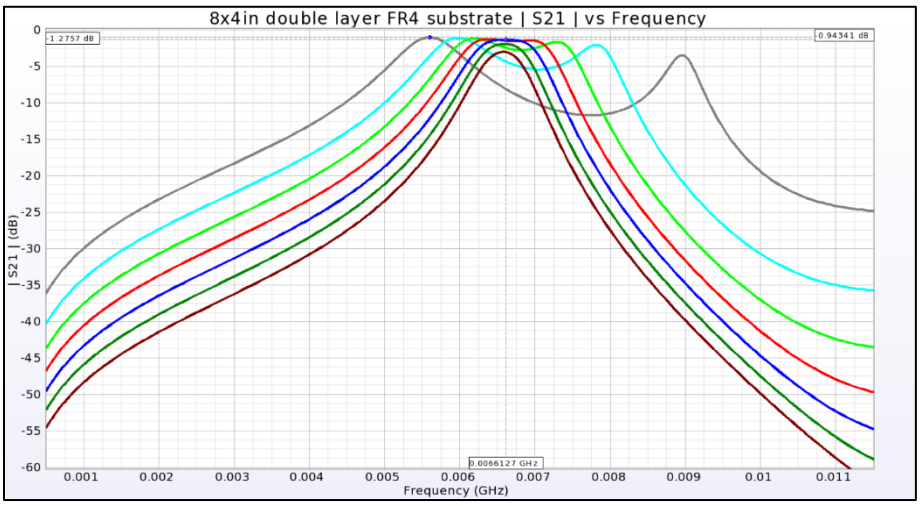


Figure 3.4-11 8x4In^2 double layer FR4 MCR-WPT coils S21 EMPro simulation result.

Table 3.4-8 8x4In^2 double layer FR4 MCR-WPT coils SRF and S21dB specifications vs simulation results.

Parameter	Specification	Momentum Results	EMPro Results
Self-Resonant Frequency (SRF)	6.78MHz	7.8MHz	6.61MHz
S21 dB at CCD	-1.3dB	-0.858dB	-1.276dB
Maximum EMPro S21 observed	NA	NA	-0.943dB

3.4.4.3 Post EMRro Harmonic Balance Transient Simulation Results at 6.78MHZ

Harmonic Balance simulations were run on the 5x2.5In FR4 double layer MCR-WPT coils at 0.5in, 1in, and 1.5in separation distances. The simulation is set up as seen in Figure 3.4, and the EMPro FEM S-Parameter simulation result EM model placement for each separation distance is shown. The transient waveforms simulation results were plotted and the results are shown in Figure 3.4-12. The output power is tabulated below the plots.

3.4.4.4 Experimental Results

To verify the 8x4in^2 FR4 double layer MCR-WPT coils design, experimental tests were done using a function generator input. The design was connected at the input to a sine wave with

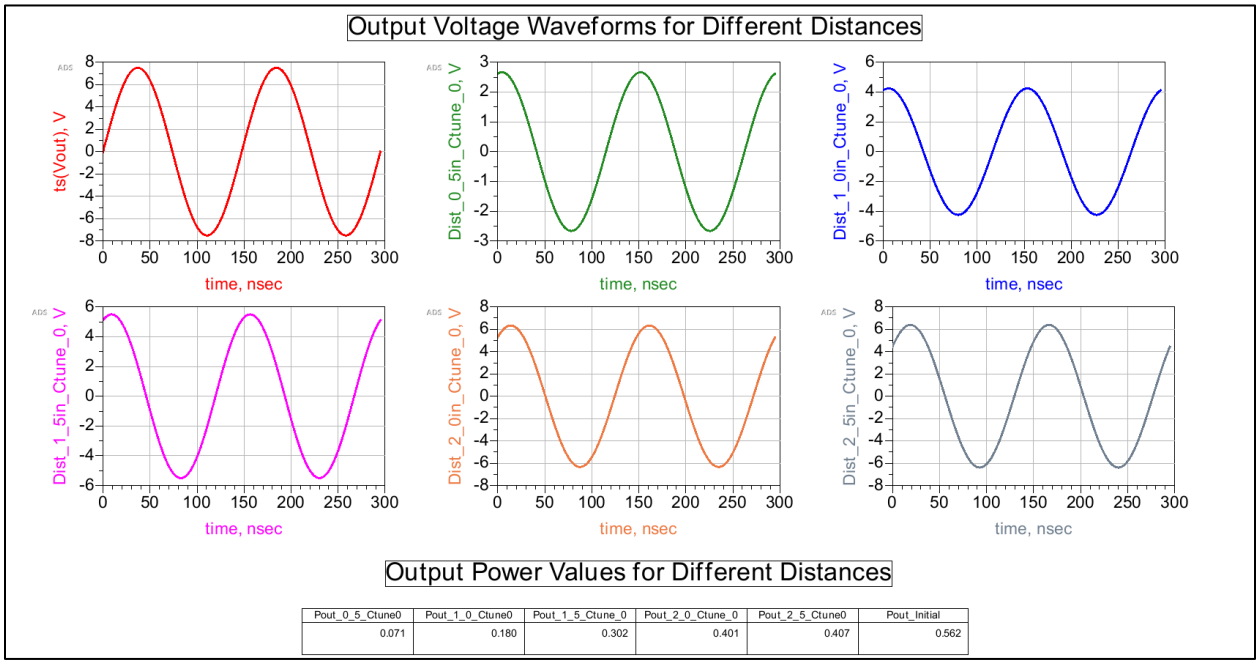


Figure 3.4-12 8x4In^2 double layer FR4 MCR-WPT coil design harmonic balance transient and output power simulation data display results for multiple separation distances.

Table 3.4-9 8x4in^2 double layer FR4 MCR-WPT coils output peak voltage and apparent power at different separation distances.

Separation Distance	Peak Voltage (V)	Apparent Power (Watt)
0.5 Inch	3.2	0.1024
1.0 Inch	5.35	0.2862
1.5 Inch	5.05	0.255
2.0 Inch	3.5	0.1225
2.5 Inch	2.55	0.065

a 7.5V peak at 6.78MHz and the output was connected to a 50Ω load resistor. To hold the coils in place at the same distances as the simulations, 0.5in slots were cut into cardboard and the coils are slotted into place and the voltage signal was then measured. The test setups can be seen in Figure 4.1-10 in section 4.1.4, where the input alligator clips are connected to the output of the Function Generator, and the output is connected to a 50Ω resistor.

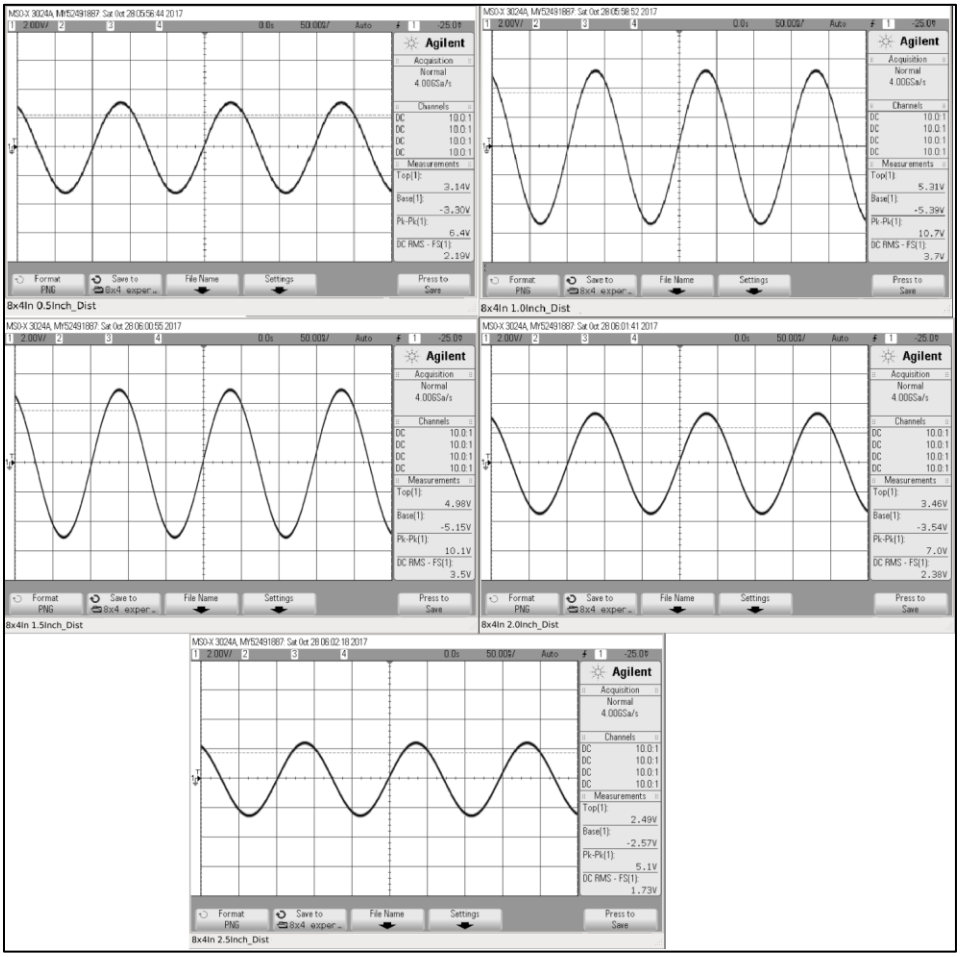


Figure 3.4-13 8x4In^2 double layer FR4 MCR-WPT Coil test with function generation input at 0.5-2.5 inch separation distances

Table 3.4-10 8x4In^2 FR4 double layer MCR-WPT coils harmonic balance and experimental peak output power results comparison.

Separation Distance	Harmonic Balance Output Power	Function Generator Output power
0.5 Inch	0.071 Watt	0.1024 Watt
1.0 Inch	0.180 Watt	**0.2862 Watt**
1.5 Inch	0.302 Watt	0.255 Watt
2.0 Inch	0.401 Watt	0.1225 Watt
2.5 Inch	0.562 Watt	0.065 Watt

The output voltage test results using the Agilent 200MHz oscilloscope. The test results for 0.5in, 1.0in, 1.5in, 2.0in and 2.5in separation distances are shown in Figure 3.4-13. The output power was calculated using equation (G.*1*). The output peak voltages and the calculated output powers are tabulated in Table 3.4-9. A peak efficiency of 50.8% was found at the 1.0in CCD

3.4.4.5 Harmonic Balance Simulation and Experimental Tests Results Summary

The output power values of the Harmonic Balance and function generator experimental results at different separation distance are shown in Table 3.4-10. From the table, we see that for 0.5in to 1.0in distances, the experimental output power values are larger and rises more rapidly than the Harmonic Balance power values. When the distance is increased to 1.5 inches or more, the experimental output power values start to decrease whereas the Harmonic Balance power values continue to increase. The experimental output power values are also smaller than the harmonic power values. This suggests that the maximum operating distance is much smaller for the experimental test.

3.4.5 Results Summary

Looking at the simulation results, we see that the Momentum predictions are close to the EMPro simulation results for all three designs. It can also be seen that it seem the error is smaller, the higher the efficiency. Based on these design tests, an S11-resistance peak resistance ≥480Ω should be sufficient enough to meet the -1.3dB Rezence specification. A more comprehensive set

Table 3.4-11 MCR-WPT PSC efficiency summary

Efficiency	**FR4 5x2.5in^2**	**Alumina 5x2.5in^2**	**FR4 8x4in^2**
Simulated EMPro	61.7% @ 2.0in	80.6% @ 2.0in	74.5% @ 2.5in
Simulated Harmonic Balance	60% @ 1.5in	NA	72.4% @ 2.5in
Measured Function Generator	42.7% @ 1.0in	NA	50.8% @ 1.0in

of MCR-WPT coil designs should be used to test the Momentum prediction vs the EMPro simulation results.

Another observation is that for the smaller dimension MCR-WPT coils design for smartphones, the FR4 substrate material does not have a large enough permittivity to create the capacitance necessary to achieve -1.3dB Rezence specification. This can be fixed by using dielectric materials with a higher permittivity such as alumina.

There were some differences between the simulations and experimental results. Table 3.4-11 present a summary of the efficiency results for the EMPro and Harmonic Balance simulations, and the experimental measurements for the MCR-WPT PSC designs. From the table, a slight difference in the efficiency between the Harmonic Balance and EMPro simulation results can be seen. This is because the SRF of the MCR-WPT PSC is less than the operating frequency, which results in a shift in the efficiency. There are also efficiency and operational range reductions between the function generator measurement results and simulations for both MCR-WPT PSC designs as seen in the table. Slight changes in the wire widths and/or wire spacings can change the CCD SRF of the MCR-WPT PSCs, which could have occurred during PSC fabrication. The differences, however, seem to be less prominent when the MCR-WPT coils were tested with the class-E amplifier as the input as described in section 4.1.4. But surge currents due to separation distance changes caused the class-e resonator capacitor component to fail, which limited the number of tests that could be conducted.

Table 3.4-12 Size, SRF and efficiency comparisons between the novel double layer 5x2.5in^2 FR4 MCR-WPT PSC and other double layer coil research.

Parameters	[57]	[29]	[30]		**Proposed Design**
			Transmitter	**Receiver**	
Outer Diameter (inches)	3.94	11.3	0.79	0.43	5x2.5in^2
Number of turns	2	3.876	17	8	7
SRF (MHz)	13.56	4	21.5	90.8	6.43
Distance (inches)	3.94	19.7	~0.2		1-2in
Efficiency simulated	**77.5%**	NA	NA		61.7%
Measured	**77.2%**	~50%	79.8%*		42.7%

*79.8% efficiency was achieved using inductive WPT at 5MHz operating frequency.

Finally, we compare the efficiency, size and SRF results of the novel double layer 5x2.5in^2 FR4 MCR-WPT PSC with the 3 other double layer WPT coil designs. All other coil design had a square design while our proposed design was rectangular. Our Novel MCR-WPT PSC have an SRF that is half the SRF of the MCR-WPT coils from [57] have a similar overall area. The coils in [29] have a lower SRF than our design but the surface area of each of their MCR-WPT coils is an order of magnitude larger than ours. The coils in [30] are much smaller than our design but their SRF were much larger. Finally, the efficiency of our design was lower than the other designs. However, our efficiency can be improved by using a dielectric with higher permittivity and by using more layers.

3.5 Chapter Summary and Conclusions

In this chapter went through basics and theory of spiral inductors, which is the foundation for MCR-WPT PSC coil design. We looked at the types of geometries available, and then analyzed the effects of single layer and double layer square spiral inductor physical parameters on their inductance. We then analyzed the parasitic capacitances and the loss mechanisms inherent to spiral inductors and presented ways to mitigate their effects.

Next, we presented the basics of MCR-WPT 4-coil system PSC. The basic structure of the

coils was shown and lumped circuit model circuit with all the parasitics and mutual inductances shown. The main purpose of the MCR-WPT 4-coil system if to make it easier to impedance match the coils and to boost the power transfer distance. Since the coils are impedance matched, they can be capacitively tuned to bring the system back into resonance, and thereby improve efficiency when the separation distance is less than the CCD.

We then presented Design Methodology to run multiple quick MCR-WPT PSC design simulations in Momentum, which gives a good prediction of the expected resonant frequency and peak S21dB results in EMPro. This design flow assumes that the spacing between the inner and outer coil wire are approximately equal to the outer coil wire spacing. The simulation results between the Momentum and EMPro simulations show that the SRF error is dependent on the outer coil W/S ratio, where a smaller W/S ratio results in a larger SRF difference. Using the peak S11-resistance value and insertion loss analysis, the maximum peak and CCD peak S21 EMPro values can be predicted within 0.3dB and 1dB with a predicted S21 greater than -1.3dB. There is some is a known potential error mentioned in 3.2.2.4, which could not be verified with ADS technical support in time.

Simulations were then run on single layer MCR-WPT coils system for cellphone to achieve an SRF of 6.78MHz, which complies with the Rezence frequency specification. Using the design flow, an SRF of 19MHz was achieved. The SRF could not be further reduced without having an unreasonably large wire thickness to increase the capacitance and inductance, reduce dc resistance. An external capacitor can also be added, but this makes the coils too bulky for our application.

Multi-layer MCR-WPT coil designs were then investigated, and a new double layer design was proposed. A study [57] has shown that parallel stacked inductors on the outer coils increase efficiency but the SRF remained the same. Other research has shown that using series stacked coils

for the outer coil, were shown to increase the efficiency and decrease the resonant frequency. The disadvantage of the stacked spiral coil design is that a via is required in-between the layers on the innermost turn, which prevent a complete turn being created on the innermost turn on both layers. To overcome this, a novel double layer design was presented without vias. We then investigated the effects of changing the number of layers, and the dielectric substrate thickness and materials.

Finally, MCR-WPT designs for smartphones and tablets were simulated, and prototypes were built and tested using an FR4 substrate. The smaller dimension MCR-WPT design for smartphones, was compared with other double layer designs of with similar SRF and size. Coil designs that were similar in size to our design had a higher SRF and coils with a similar SRF had a larger size. However our design's efficiency was less than the other designs. This low efficiency is due to the low permittivity of the FR4 substrate material, which is also the reason why a minimum S21 of -1.3dB could not be achieved so that the Rezence specification could be met. This was shown to be fixed by using an Alumina dielectric which has a higher permittivity. There were some large differences between the Harmonic Balance simulations and experimental results. The operational range and the maximum output power for both coils were reduced.

Chapter 4

4 Auto-Tuning Technique to Overcome Frequency Splitting and Improve System Efficiency

Although the Rezence Wireless Power standard is seeing steady adoption due to the benefits of up to 5cm [6] of separation distance for wireless power transmission, the efficiency of this system is low compared to other wireless power standards. This low efficiency is due to flux leakage [59] caused by frequency splitting phenomenon. Frequency splitting occurs when the change in separation distance between the transmitter and receiver is less than the critical coupling distance (CCD). This distance change causes a change in mutual inductance, which results in an altered impedance and resonant frequency. There are a few methods to bring the system back into resonance, such as changing the inductance, the transmission frequency as seen in [60] and [61], or impedance tuning capacitance using variable capacitance such as [62], [63], and [64]. Since the frequency bandwidth is very limited and inductance are fixed due to coils dimensions, only the capacitance can be changed to compensate for the changed in mutual inductance.

We present a novel technique in this chapter to tune the output impedance of the coils and return them to resonance at its fundamental frequency. This allows us to achieve greatly improved power transmission efficiency from the Class E amplifier to the Rectifier. The technique uses a

feedback loop to tune the MCR-WPT coils' output impedance by shunting discrete capacitors across the terminals of the coils and are enabled using a counter. Simulation results show that for separation distances less than the critical distance, the output impedance of the coils and matched and returned to resonance, resulting in maximum power transmission.

This chapter will cover the effects of frequency on the MCR-WPT coils and present a novel Maximum Peak Detection and Auto-Tuning system. In Section 4.1 looks at theory of Frequency Splitting in Magnetically Coupled Resonance Wireless Power Transmission (MCR-WPT) coils and investigates the effects of adding tuning capacitors at the output. Section 4.2 goes through the theory and operation of the maximum peak detection and Auto-Tuning circuit blocks. Section 4.3 presents the simulation setup, results, and discussion of findings. Finally, the chapter is concluded in Section 4.4.

4.1 Magnetically Coupled Resonance (MCR) and Frequency Splitting Theory and Tuning

As discussed in the chapter introduction, although the MCR-WPT coils system benefits from longer transmission distances compared to other WPT systems, it suffers from a rapid decrease in transmission efficiency when the receiver is not located at the optimal distance away from the transmitter. This is due to the mutual inductive coupling between the transmitter and receiver coils is directly proportional to the separation distances between these coils. Therefore according to equation (*G.5*), the distance changes would cause the resonant frequency of the MCR-WPT coils system changes and consequently cause the system efficiency to drop. To overcome the effects of frequency splitting and bring back the system into resonance, 3 different tuning

methods have been proposed, namely, inductive tuning, frequency tuning [60] [61] and capacitive tuning [62], [63], and [64]. Inductive tuning can't be used in our application since the dimensions and/or materials of the coils have to be changed to change the inductance. Also, frequency tuning can't be used because our frequency bandwidth is fixed by the Rezence Standard. Therefore, we are left with capacitance tuning which is explored in this section.

4.1.1 Frequency Splitting Theory, Modes of Operation for MCR-WPT Coils

Taking this into account, the MCR-WPT Coils coupling efficiency can be divided into 3 different modes of operation as defined in [65]. These modes are based on the mutual inductive coupling coefficient and are defined as follows:

1. **Critically-Coupled**: This is when the MCR-WPT coil system is at the optimal separation distance. The maximum transmission efficiency of the system occurs at this location.
2. **Over-Coupled**: When the separation distance between the transmitter and the receiver is less than the critical coupling distance (CCD), the efficiency of the system at the fundamental frequency is reduced. This is due to a the frequency splitting phenomenon. According to [65], when multiple coupled resonators form a single system which can oscillate in two modes, one of higher and one of lower frequency than the fundamental frequency, where the frequency separation of the two modes is dependent on the coupling strength between the resonant components, is known as frequency splitting. In the MCR-WPT coil system, the coupling strength is dependent on the separation distance. With decreasing separation distance, we get increasing coupling, and increasing frequency separation between the resonant modes.
3. **Under-Coupled**: Beyond the critically-coupled distance, when the separation distance is increased, the coupling between the transmitter and receiver coils is decreased. The system

transmission efficiency drops, and it operates in the under-coupled region.

Detailed theoretical analysis of these modes is discussed thoroughly in [65].

4.1.2 Example Visual Representation of Frequency Splitting Operation Modes.

The three modes of operation are shown in Figure 4.1-1 below. The experimental results (the black lines) are compared to a theoretical model data (the multi-color plot), where the experimental setup is described in [65]. The region defined by the red dotted line is where over-coupling occurs and frequency splitting is present.

4.1.3 Simulation Results for Tuning Frequency Splitting

To check the effects of tuning capacitance on the MCR-WPT coils Harmonic Balance and S-Parameter simulations were done using Keysight's ADS software, and the schematics of the test

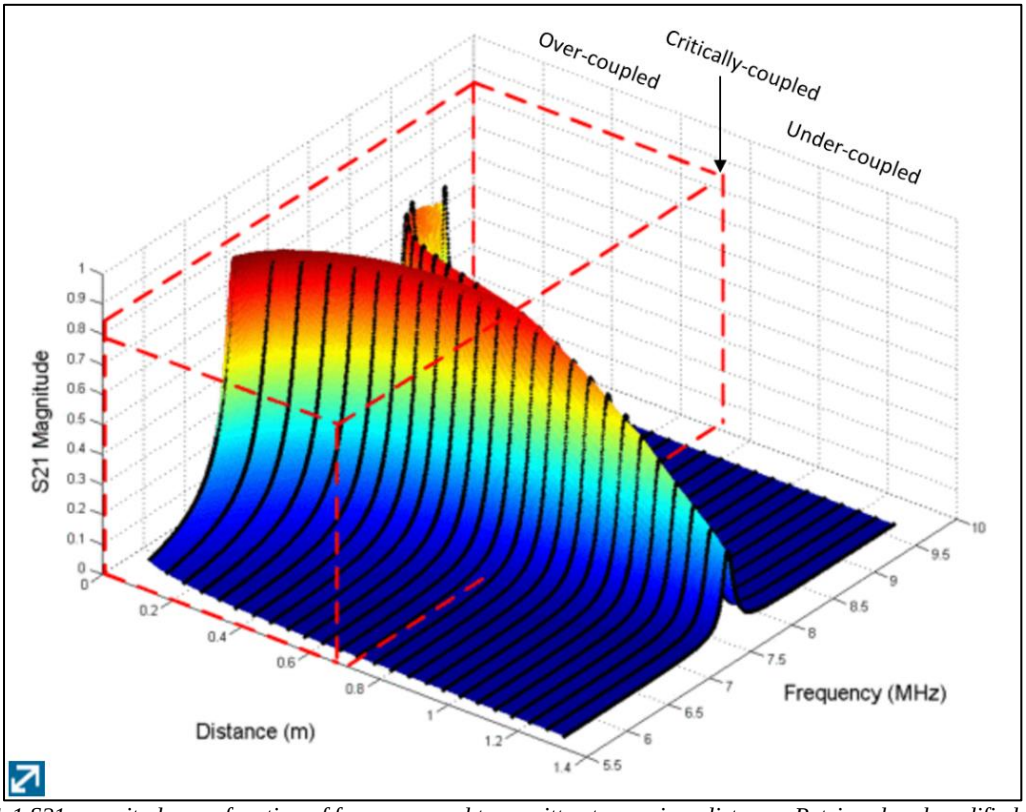


Figure 4.1-1 S21 magnitude as a function of frequency and transmitter-to-receiver distance. Retrieved and modified from [65].

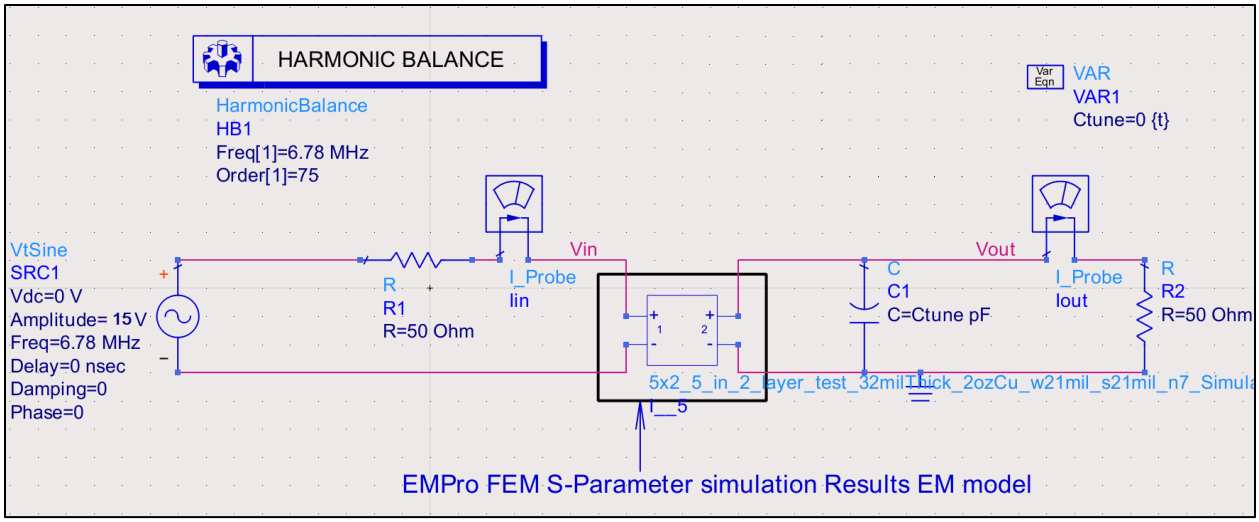


Figure 4.1-2 Schematic Setup for harmonic balance simulation on the MCR-WPT coils in Keysight ADS.

circuit and simulation setups are provided in Figure 4.1-2 and Figure 4.1-3 respectively. The EM models from the EMPro S-Parameter simulation results for various separation distances were used for the capacitance tuning simulations done on the 5in x 2.5in coils and the 8in x 4in coils designs. The transmission coefficient (S21) S-Parameter tuning capacitor (C_{tune}) parameter sweep simulations were done to show the effects of capacitor tuning on frequency spitting. The Harmonic Balance simulation was done with 75 harmonics for accuracy. The simulation was used to determine the output power and to generate the transient plots before capacitance tuning and after the optimal tuning capacitance value for maximum efficiency was added.

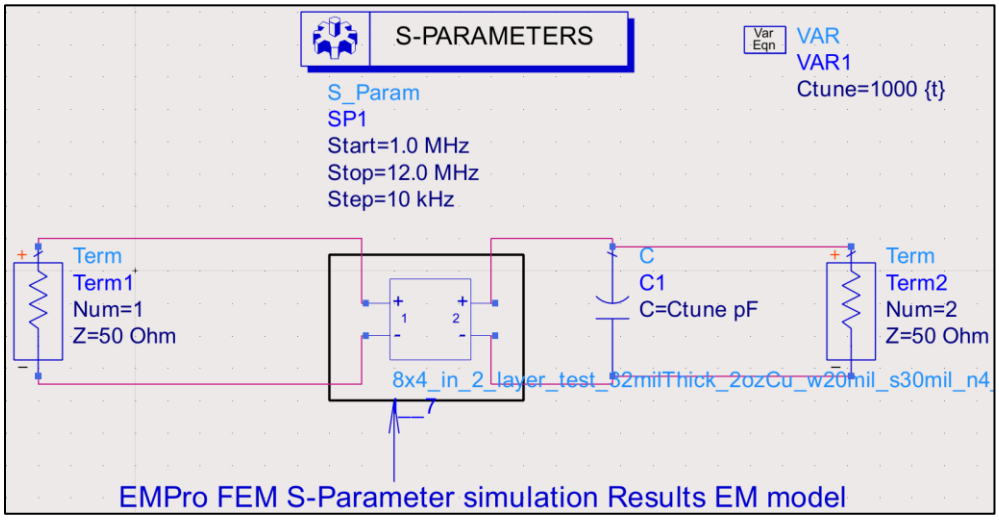
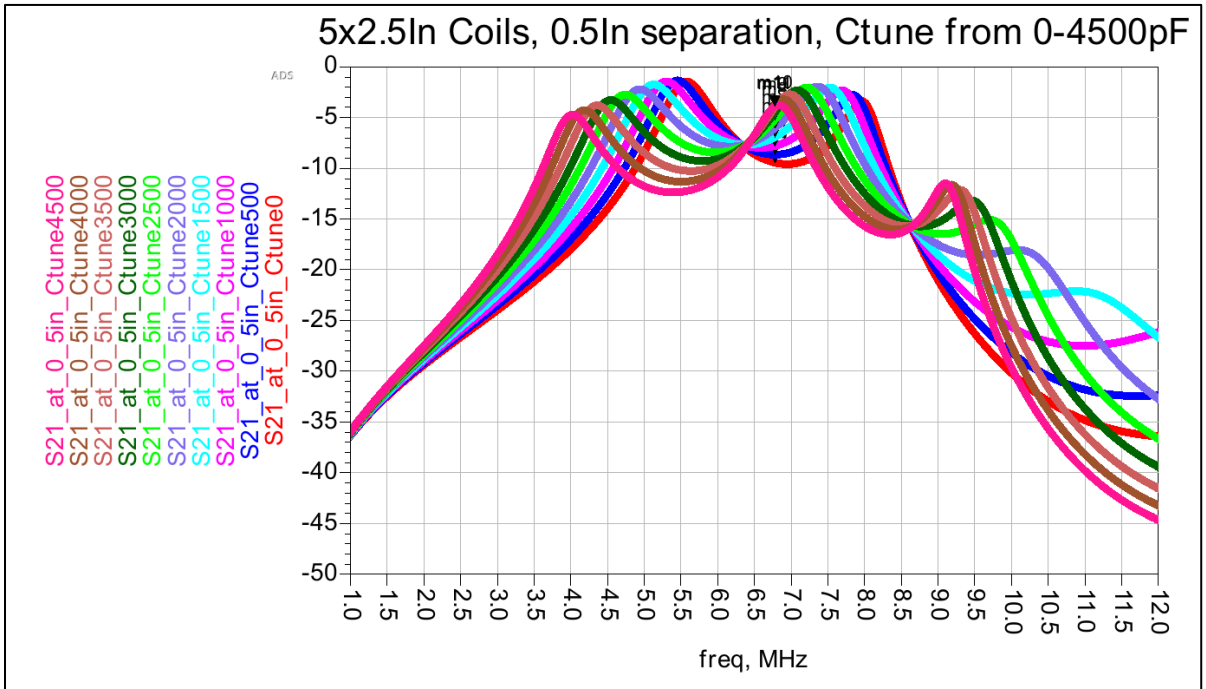


Figure 4.1-3 Schematic setup for s-parameter simulation on the MCR-WPT coils in Keysight ADS.

4.1.3.1 S-Parameters

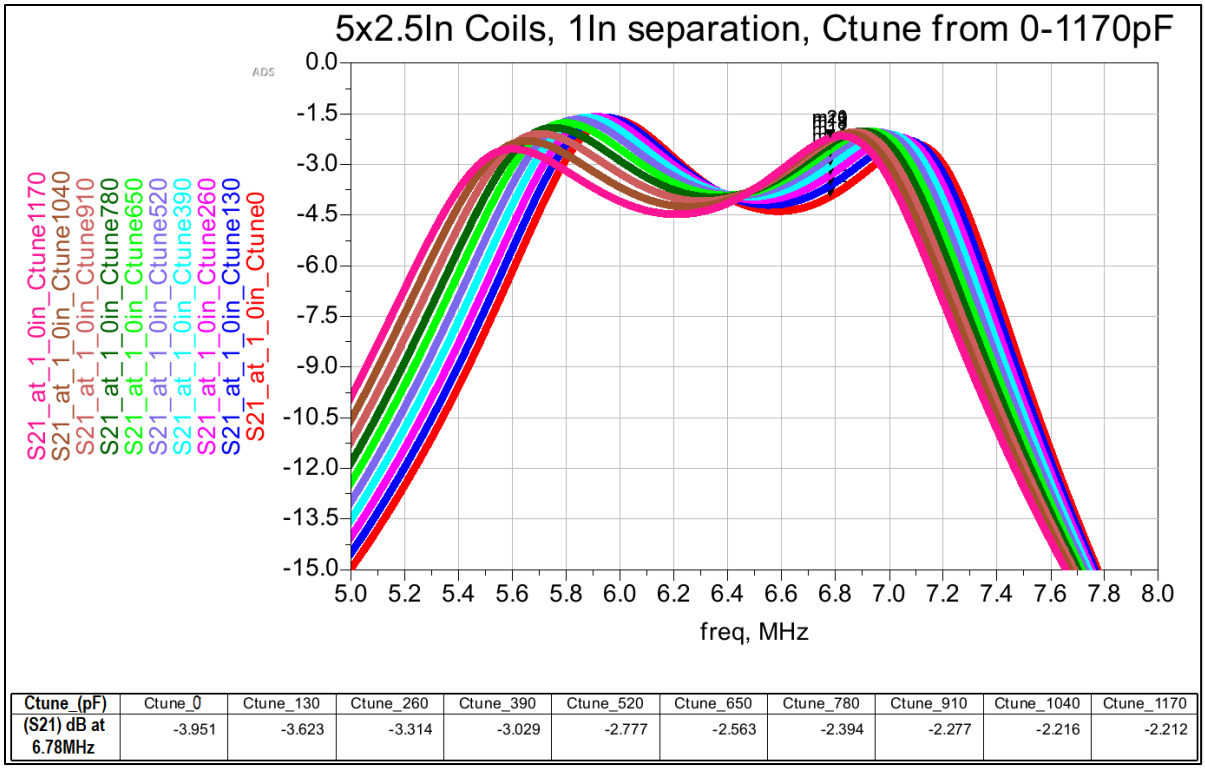
The S-Parameter C_{tune} parameter sweep simulations were run on the 5x2.5in MCR-WPT coils at 0.5in and 1in separation distances, and the S21 results are plotted in Figure 4.1-4 and Figure 4.1-5 respectively. The S-Parameter C_{tune} parameter sweep simulations were also run on the 8x4in MCR-WPT coils at 0.5in and 1.5in separation distances, and the S21 results are plotted in Figure 4.1-6 and Figure 4.1-7 respectively. In all the graphs, markers were placed on plots for each value C_{tune} at the 6.78MHz target frequency, and the S21 results are shown in the table below each graph.

From the results in Figure 4.1-4 and Figure 4.1-6, when the MCR-WPT coils are close at separation distances of 0.5 inch, it can be seen when C_{tune} is 0pF that the frequency splitting is significant. As a result, large C_{tune} capacitance values near of 4.0nF and 3.5nF for the 5x2.5In and



Ctune_(pF)	Ctune_0	Ctune_500	Ctune_1000	Ctune_1500	Ctune_2000	Ctune_2500	Ctune_3000	Ctune_3500	Ctune_4000	Ctune_4500
(S21) dB at 6.78MHz	-9.458	-8.653	-7.807	-6.932	-6.052	-5.211	-4.481	-3.961	-3.744	-3.880

Figure 4.1-4 5x2.5In MCR-WPT coil design s-parameter (S21) simulation data display results in ADS for 0.5 inch coil separation, C_{tune} 0-4500pF.



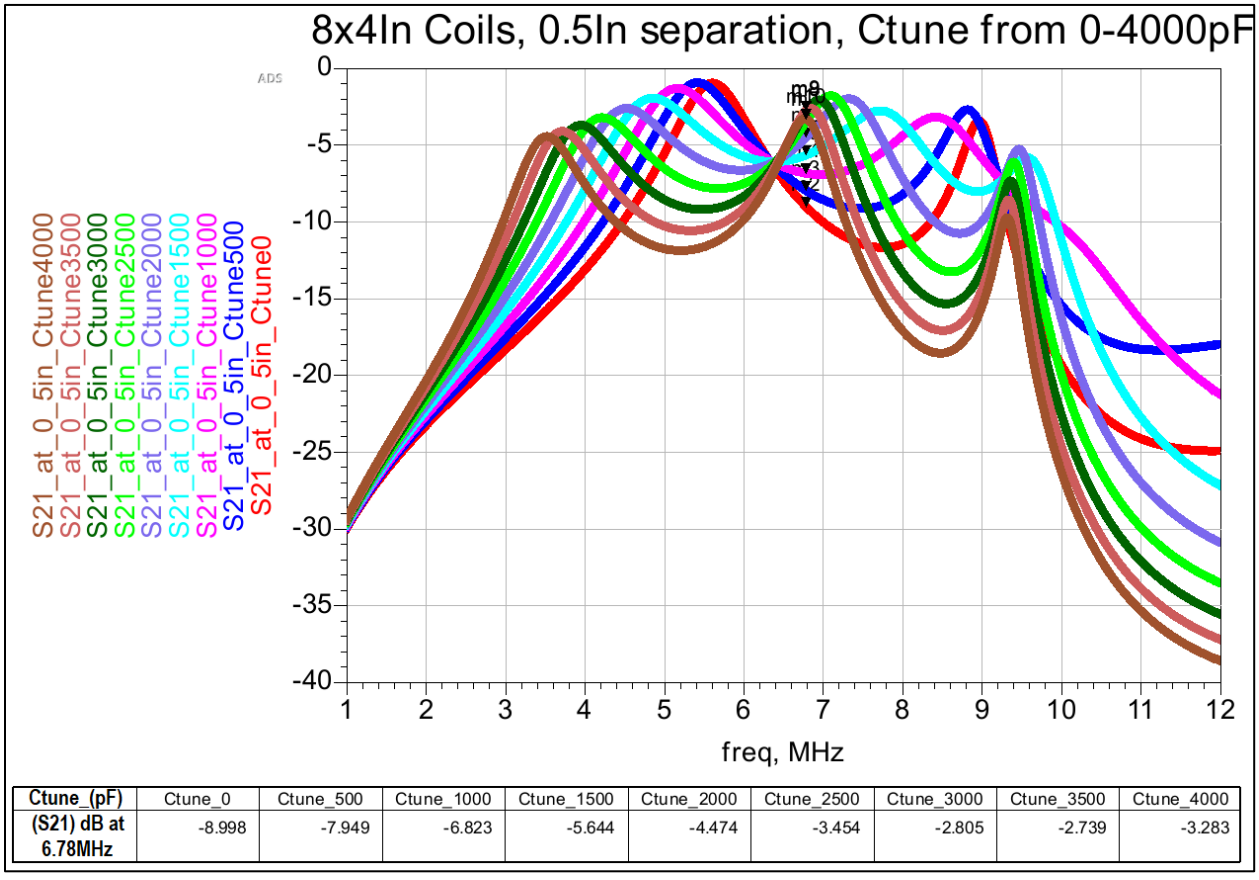
Ctune_(pF)	Ctune_0	Ctune_130	Ctune_260	Ctune_390	Ctune_520	Ctune_650	Ctune_780	Ctune_910	Ctune_1040	Ctune_1170
(S21) dB at 6.78MHz	-3.951	-3.623	-3.314	-3.029	-2.777	-2.563	-2.394	-2.277	-2.216	-2.212

Figure 4.1-5 5x2.5In MCR-WPT coil design s-parameter (S21) simulation data display results in ADS for 1in coil separation, C_{tune} 0-1170pF.

the 8x4In MCR-WPT coils respectively are needed to bring the systems back to resonance and get the maximum S21 value. On the other hand, when the coils separations distances were increased to 1 inch for the 5x2.5In coils and 1.5 inches for the 8x4In coils, it can be seen from Figure 4.1-5 and Figure 4.1-7 that the frequency splitting is less pronounced when C_{tune} is 0nF. Therefore smaller capacitance values near 1170pF for the 5x2.5In coils and 875pF for the 8x4In coils are needed to bring the systems back to resonance and get the maximum S21 value. These frequency splitting observations support the over-coupling theory discussed in section 4.1.1.

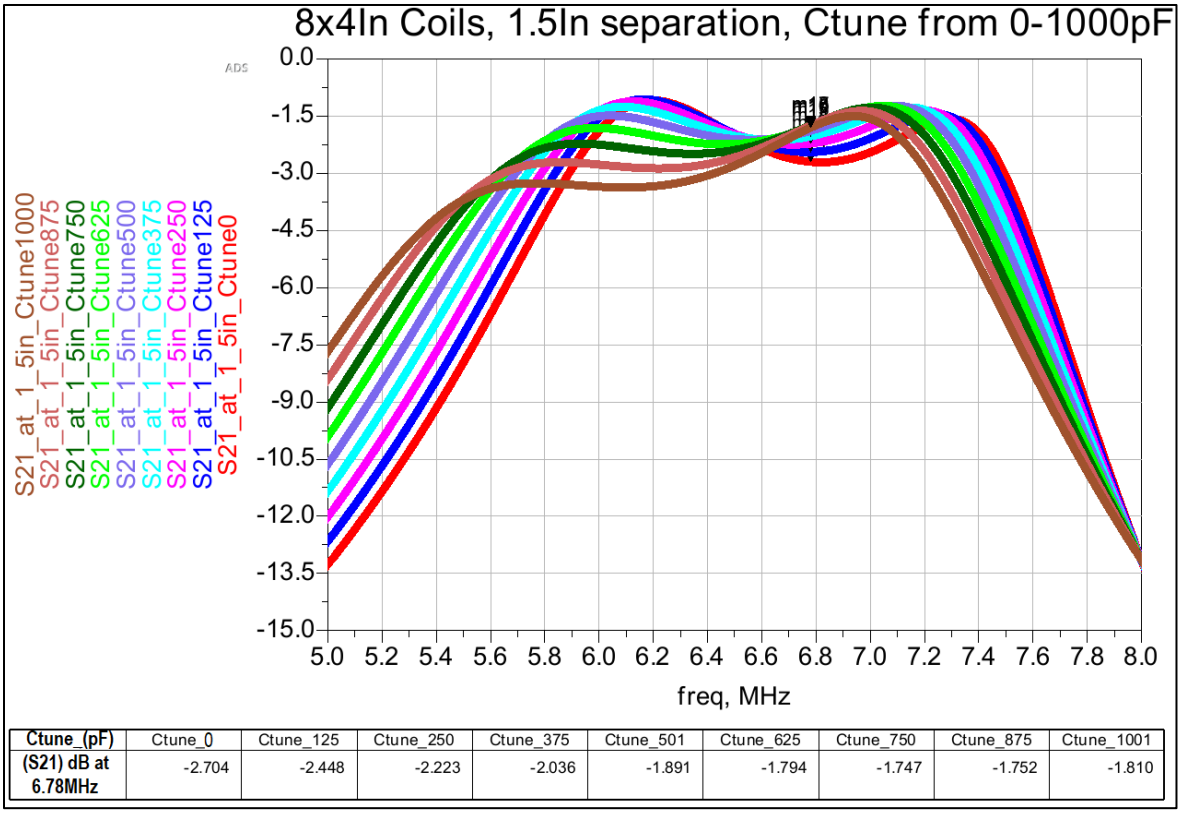
Another observation can be made from all the graphs when adjusting the value of the C_{tune} capacitance parameter. With reference to the 0.5 inch separation for the 5x2.5In coils in Figure 4.1-4, if we change our target frequency to 7.36MHz and look at the purple plot represented by the C_{tune} capacitance value of 2nF, the systems is in resonance and achieves maximum S21 value is -1.961dB, which is much higher S21 value than the -3.744dB at our 6.78MHz design frequency.

In all the other graphs it is seen that at certain frequencies larger than our target frequency, we achieve a higher maximum S21 at a lower C_{tune} value than the maximum S21 value achieved after capacitance tuning at our target frequency. On the other hand with reference to the S21 graph results of the 1 inch separation for the 5x2.5In coils in Figure 4.1-5, at 7.36MHz for a C_{tune} of 0pF we get an S21 value of -5.946dB and it cannot be tuned, and it is much less than the -2.212dB tuned value achieved at 6.78MHz for a C_{tune} of 1170pF. These observations suggest that we can design the MCR-WPT coils to resonate at a lower frequency than our target frequency in the under-coupled region, then we can use the coils in the over-coupled region and tune them at our target frequency to achieve larger maximum S21values. On the flip side, doing so will reduce the tuning distance range MCR-WPT coils.



Ctune_(pF)	Ctune_0	Ctune_500	Ctune_1000	Ctune_1500	Ctune_2000	Ctune_2500	Ctune_3000	Ctune_3500	Ctune_4000
(S21) dB at 6.78MHz	-8.998	-7.949	-6.823	-5.644	-4.474	-3.454	-2.805	-2.739	-3.283

Figure 4.1-6 8x4In MCR-WPT coil design s-parameter (S21) simulation data display results in ADS for 0.5 inch separation, C_{tune} 0-4000pF.



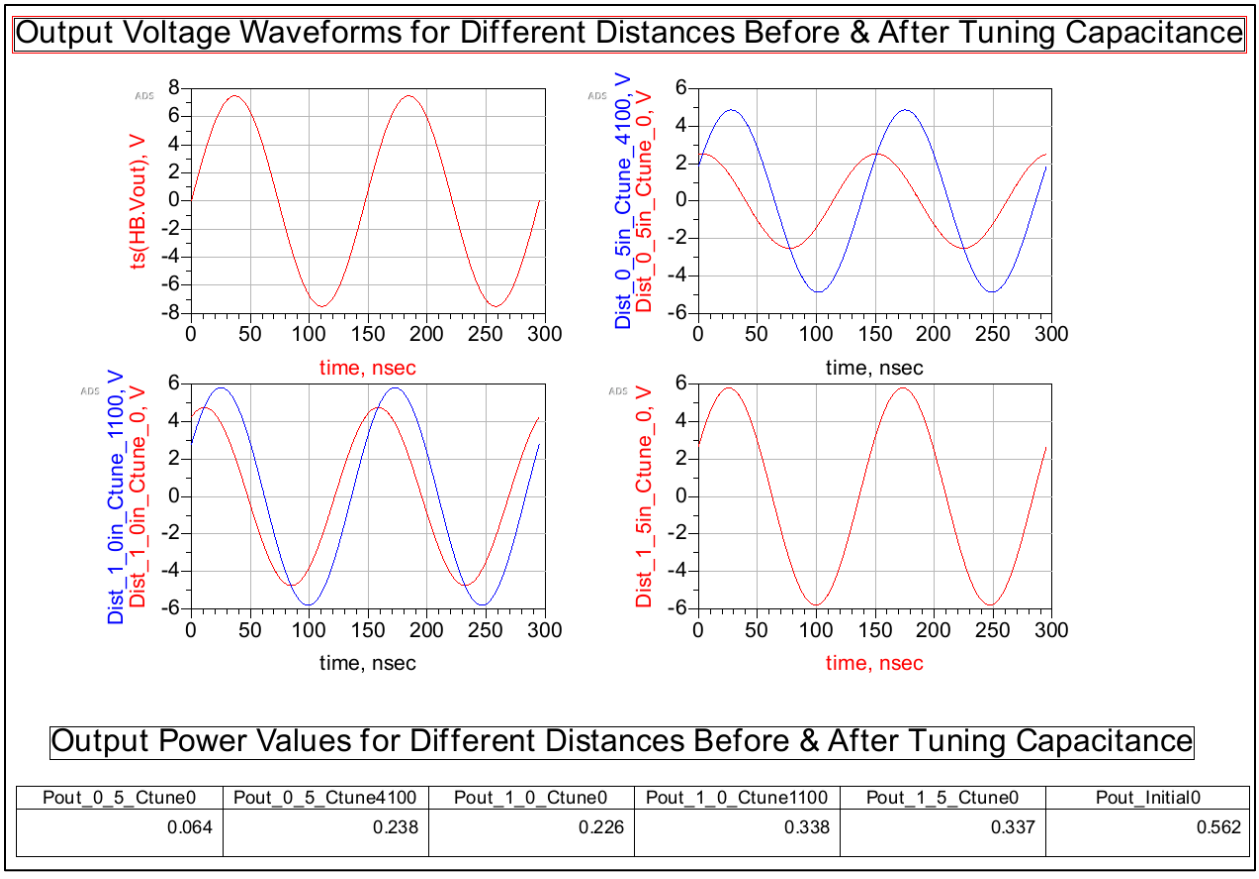
Ctune_(pF)	Ctune_0	Ctune_125	Ctune_250	Ctune_375	Ctune_501	Ctune_625	Ctune_750	Ctune_875	Ctune_1001
(S21) dB at 6.78MHz	-2.704	-2.448	-2.223	-2.036	-1.891	-1.794	-1.747	-1.752	-1.810

Figure 4.1-7 8x4In MCR-WPT coil design s-parameter (S21) simulation data display results in ADS for 1.5inh separation, C_{tune} 0-1000pF.

4.1.3.2 Harmonic Balance

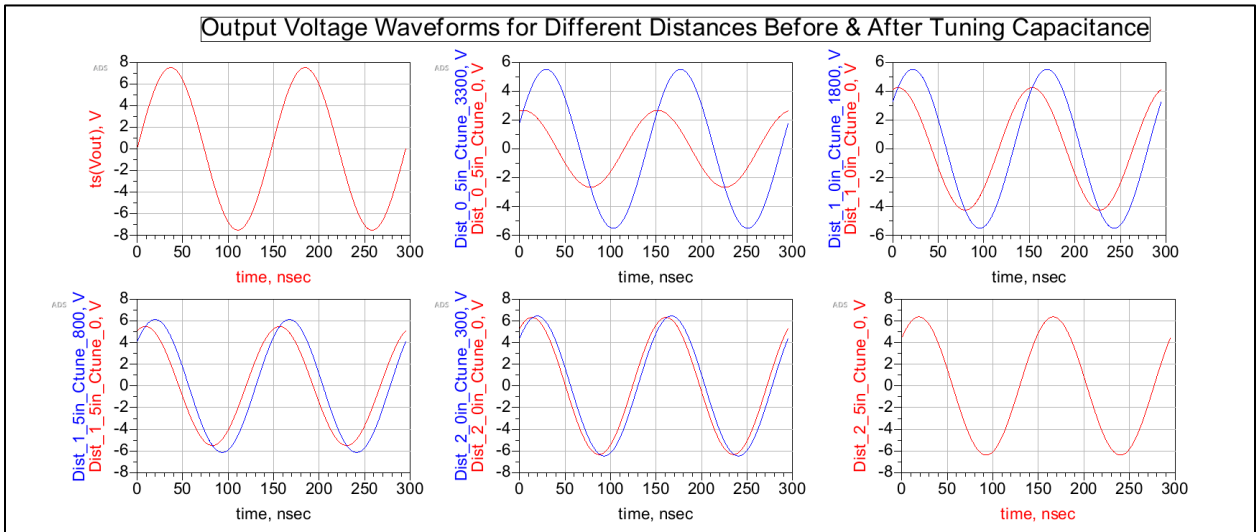
The Harmonic Balance simulations were run on the 5x2.5In MCR-WPT coils at 0.5in, 1in, and 1.5in separation distances, as well as on the 8x4In MCR-WPT coils at 0.5in, 1in, 1.5in, 2in and 2.5in separation distances and the results are shown in Figure 4.1-8 and Figure 4.1-9 respectively. The simulations were run before (taken from sections 3.4.2.5 and 3.4.4.5) and after adjusting the C_{tune} capacitance for maximum transmission. The transient waveforms simulation results were plotted with C_{tune} at 0pF waveform in red and C_{tune} tuned for near max transmission in blue, and the output power before and after tuning C_{tune} is tabulated below the plots.

We can see from the plots that tuning on small separation distances provides a significant improvement to the output power and voltage signal. We also see that when the separation distance increases towards the CCD the transmission improvement decreases.



Pout_0_5_Ctune0	Pout_0_5_Ctune4100	Pout_1_0_Ctune0	Pout_1_0_Ctune1100	Pout_1_5_Ctune0	Pout_Initial0
0.064	0.238	0.226	0.338	0.337	0.562

Figure 4.1-8 5x2.5In MCR-WPT coil design harmonic balance transient and output power simulation data display results for multiple separation distances before and after capacitance tuning.



Pout_0_5_Ctune0	Pout_0_5_Ctune3300	Pout_1_0_Ctune0	Pout_1_0_Ctune_1800	Pout_1_5_Ctune_0	Pout_1_5_Ctune_800	Pout_2_0_Ctune_0	Pout_2_0_Ctune_300	Pout_2_5_Ctune0	Pout_Initial
0.071	0.303	0.180	0.303	0.302	0.377	0.401	0.417	0.407	0.562

Figure 4.1-9 8x4In MCR-WPT coil design harmonic balance transient and output power simulation data display results for multiple separation distances before and after capacitance tuning.

4.1.4 Physical Results for Capacitance Tuning Frequency Splitting

To verify the effects of tuning capacitance on the MCR-WPT coils two sets of experimental tests were done. One set of tests was done with a 7.5V peak input signal at 6.78MHz from a function generator. The other setup was done with 17 Watt input from a class-e amplifier at 6.78MHz. Both test setups were calibrated with only a 50Ω load at the output. To hold the coils in place at the same distances as the simulations, 0.5in slots were cut into cardboard and the coils are slotted into place and the voltage signal was then measured. The test setups can be seen in Figure 4.1-10, where the input alligator clips are connected to the output of the Function Generator or Class-E amplifier, and the output is connected to a 50Ω resistor.

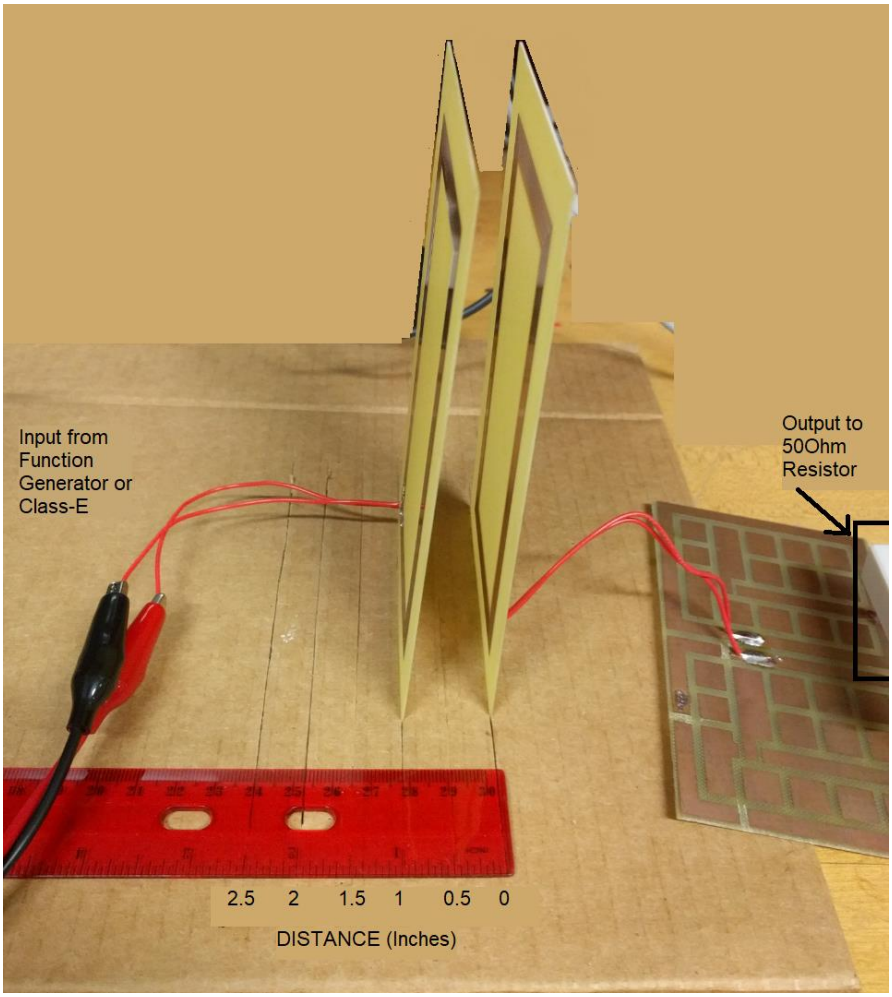


Figure 4.1-10 Experimental test setup for MCR-WPT coil tuning during frequency splitting.

The output voltage test results using the Agilent 200MHz oscilloscope are shown in the following subsections. In section 4.1.4.1, Figure 4.1-11 shows the output voltage waveforms for 0pF and 1600pF connected to the output of the Class-E Amplifier connected to the 8x4In MCR-WPT coils with 0.5in separation distance. It should be noted that these were the only measurements that could be collected at the time using the Class-E input. This is because any separation distance changes made while the Class-E amplifier was on, caused the surge current to exceed the maximum current of the resonator capacitor according to [35], causing it to fail. An appropriate replacement capacitor capable of handling this changes could not be found in time.

The output waveforms of the 5x2.5In MCR-WPT coils connected to the function generator are shown in section 4.1.4.2. The test results for 0.5in, 1.0in and 1.5in separation distances are shown in Figure 4.1-12, Figure 4.1-13, and Figure 4.1-14 respectively, with output capacitance values ranging from 0pF to 1200pF in approximately 400pF increments. Output capacitance values of 1600pF and 3300pF were also tested at 0.5in separation distance. Finally, Section4.1.4.2 4.1.4.3 shows the output waveforms of the 8x4In MCR-WPT coils connected to the function generator. The test results for 0.5in, 1.0in, 1.5in, 2.0in, and 2.5in separation distances are shown in Figure 4.1-15, Figure 4.1-16, Figure 4.1-17, Figure 4.1-18, and Figure 4.1-19, respectively, with output capacitance values ranging from 0pF to 1200pF in approximately 400pF increments. The output power was calculated using equation (G.*1*). In section 4.1.4.4, the output peak voltages and the calculated output power are tabulated in Table 4.1-2 with the maximum peak voltages during tuning highlighted in orange. The observations from the experiments are also discussed in this section.

4.1.4.1 8x4In MCR-WPT Coils test with Class-E Amplifier Input

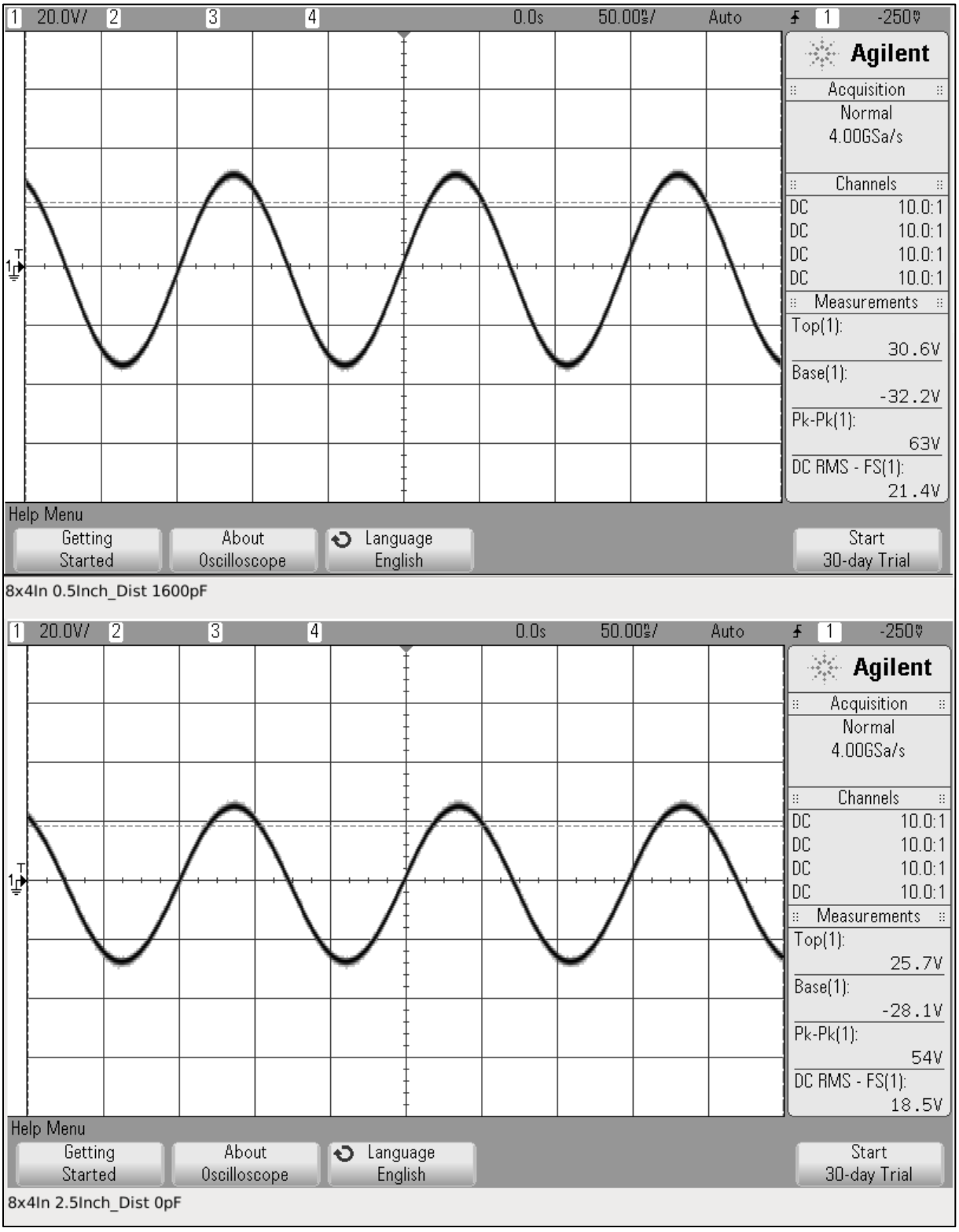


Figure 4.1-11 8x4In MCR-WPT coils capacitive tuning test with Class-E PA input at 0.5in separation distance.

4.1.4.2 5x2.5In MCR-WPT Coils test with Function Generator Input

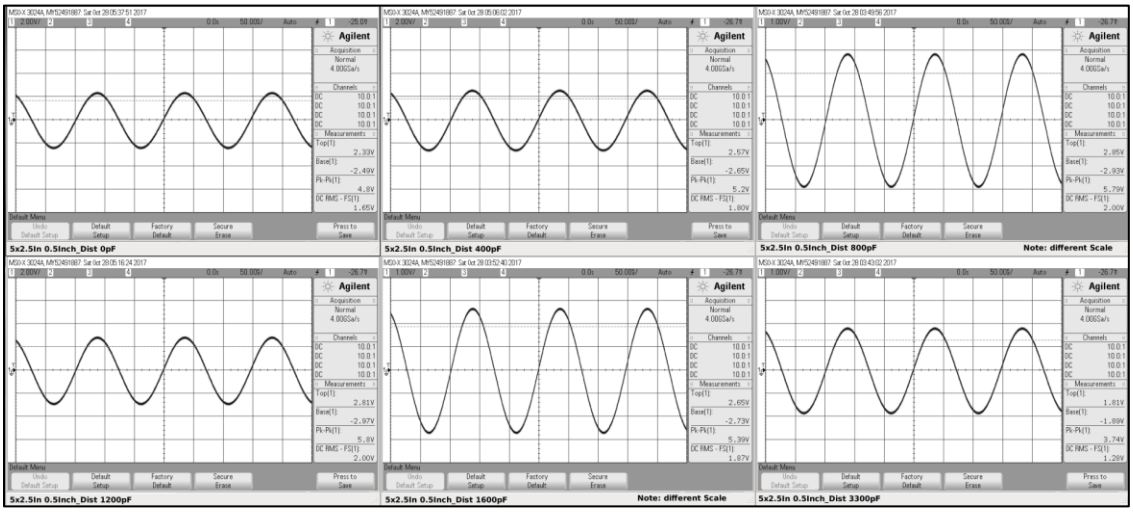


Figure 4.1-12 5x2.5In MCR-WPT coils capacitive tuning tests with function generation input at 0.5in separation distance.

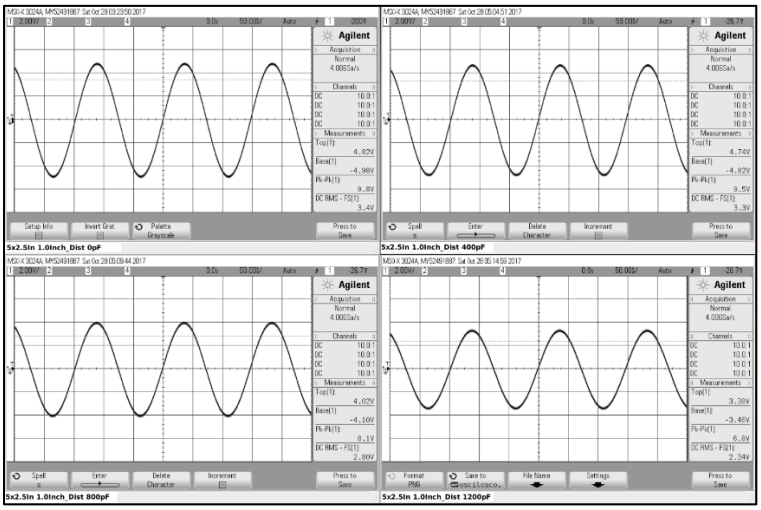


Figure 4.1-135x2.5In MCR-WPT coils capacitive tuning tests with function generation input at 1.0in separation distance.

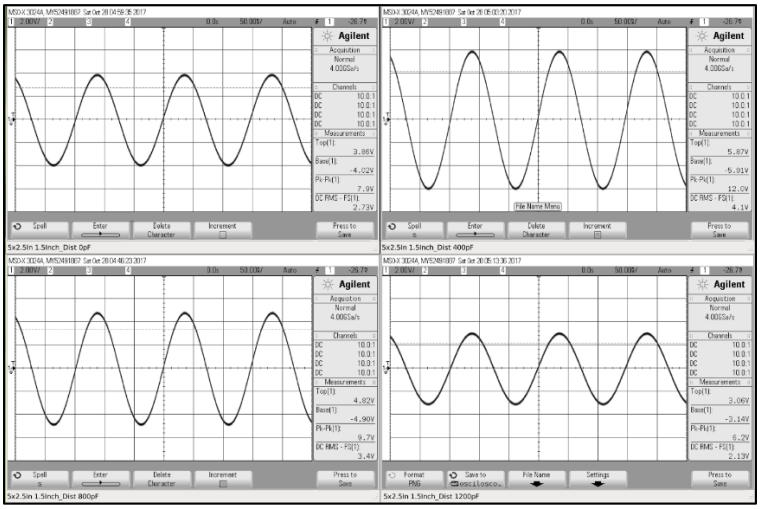


Figure 4.1-14 5x2.5In MCR-WPT coils capacitive tuning tests with function generation input at 1.5in separation distance.

4.1.4.3 8x4In MCR-WPT Coils test with Function Generator Input

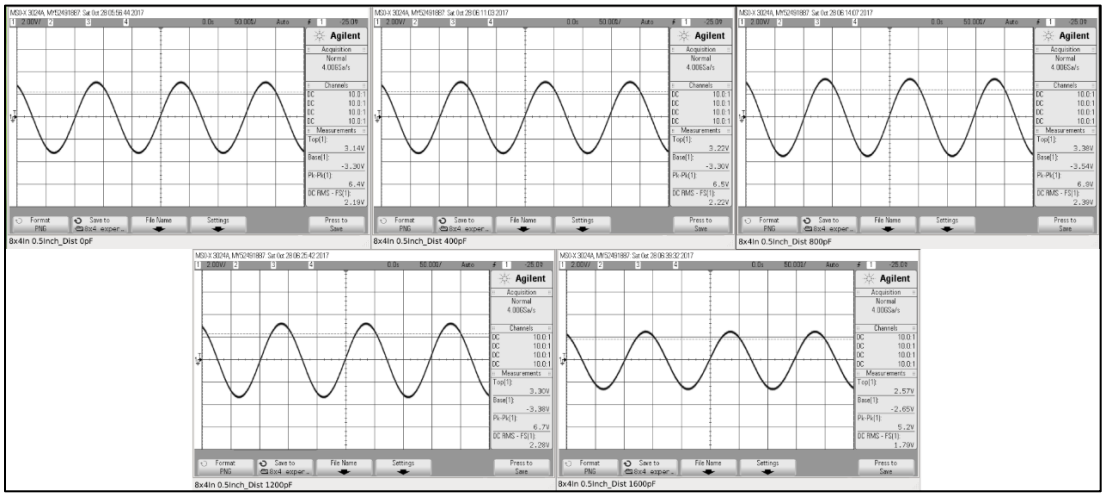


Figure 4.1-15 8x4In MCR-WPT coils capacitive tuning tests with function generation input at 0.5in separation distance.

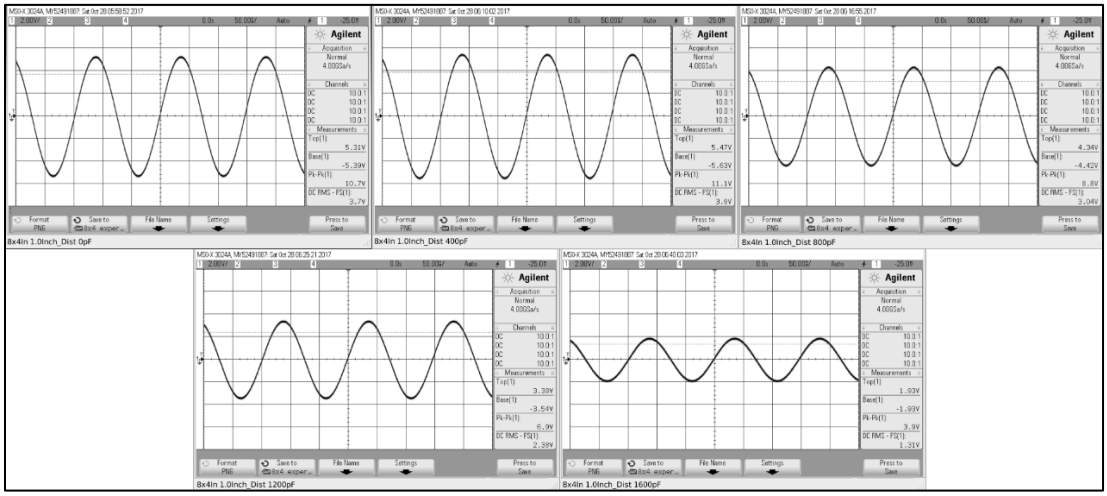


Figure 4.1-16 8x4In MCR-WPT coils capacitive tuning tests with function generation input at 1.0in separation distance.

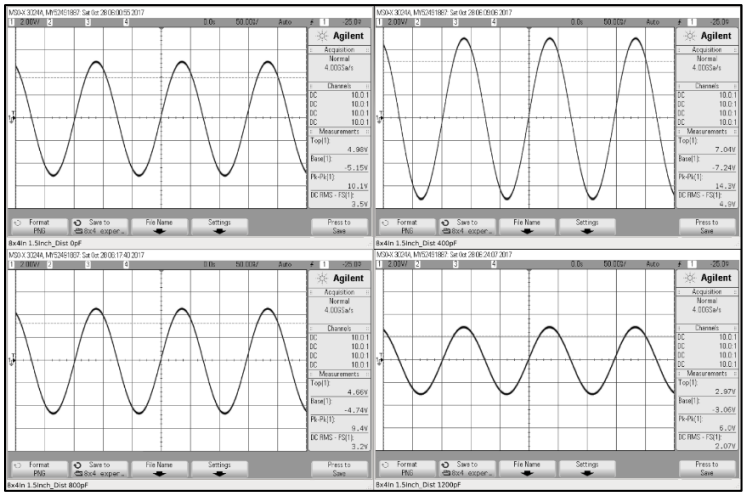


Figure 4.1-17 8x4In MCR-WPT coils capacitive tuning tests with function generation input at 1.5in separation distance.

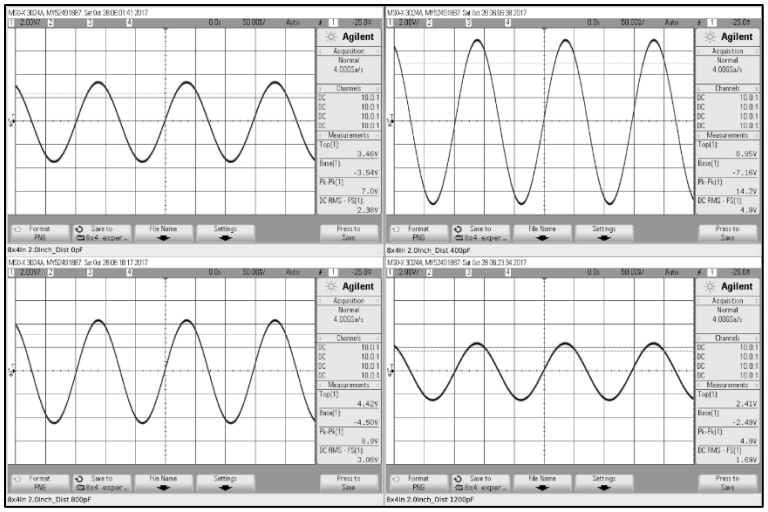


Figure 4.1-18 8x4In MCR-WPT coils capacitive tuning tests with function generation input at 2.0in separation distance.

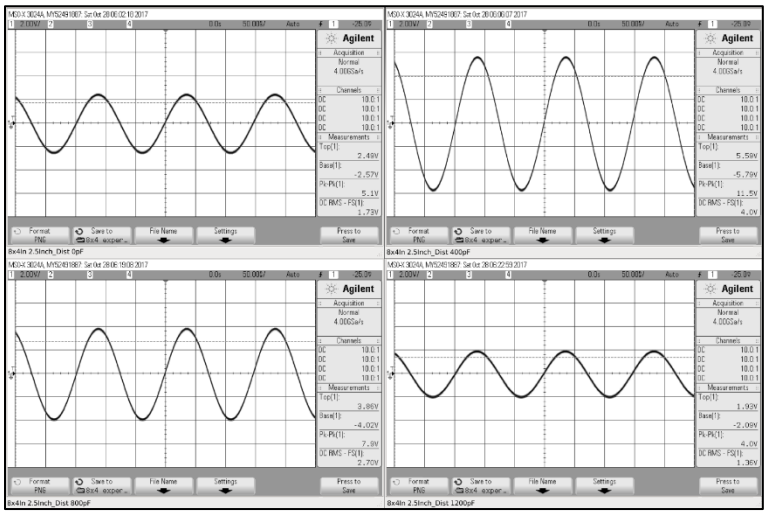


Figure 4.1-19 8x4In MCR-WPT coils capacitive tuning tests with function generation input at 2.5in separation distance.

4.1.4.4 Results Summary and Discussion

From the experimental results, adding a tuning capacitance improves the overall efficiency of the MCR-WPT coils, but there are differences between the experimental and simulation results. The first difference between the experimental results and Harmonic Balance simulations results is

Table 4.1-1 Comparison between harmonic balance and experimental MCR-WPT tuning capacitance and peak output power.

Separation Distance		0.5 Inch		1.0 Inch		1.5 Inch		2.0 Inch		2.5 Inch	
5x2.5In Design	Harmonic Balance	4100pF	0.238	1100pF	0.338	0pF	0.337		NA		NA
	Function Generator	1200pF	0.084	0pF	0.24	400pF	0.36		NA		NA
8x4In Design	Harmonic Balance	3300pF	0.303	1800pF	0.303	800pF	0.377	300pF	0.417	0pF	0.407
	Function Generator	800pF	0.119	400pF	0.308	400pF	0.511	400pF	0.504	400pF	0.331

Table 4.1-2 Output peak voltage and apparent power of the 8x4In and 5x2.5In MCR-WPT coils for different inputs and at different separation distances and capacitance tuning values.

Input Type	MCR-WPT Coils	Separation Distance	Tuning Capacitance	Output Peak Voltage (V)	Output Apparent Power (Watts)
Class-E Amplifier	No Coils	NA	NA	42	17.6400
	8x4In Design	0.5 Inch	0pF	27	7.2900
			1600pF	31.5	9.9225
Function Generator	No Coils	NA	NA	7.5	0.5625
	5x2.5In Design	0.5 Inch	0pF	2.4	0.0576
			400pF	2.6	0.0676
			800pF	2.895	0.0838
			1200pF	2.9	0.0841
			1600pF	2.695	0.0726
			3300pF	1.87	0.0350
		1.0 Inch	0pF	4.9	0.2401
			400pF	4.75	0.2256
			800pF	4.05	0.1640
			1200pF	3.4	0.1156
		1.5 Inch	0pF	3.95	0.1560
			400pF	6	0.3600
			800pF	4.85	0.2352
			1200pF	3.1	0.0961
	8x4In Design	0.5 Inch	0pF	3.2	0.1024
			400pF	3.25	0.1056
			800pF	3.45	0.1190
			1200pF	3.35	0.1122
			1600pF	2.6	0.0676
		1.0 Inch	0pF	5.35	0.2862
			400pF	5.55	0.3080
			800pF	4.4	0.1936
			1200pF	3.45	0.1190
			1600pF	1.95	0.0380
		1.5 Inch	0pF	5.05	0.2550
			400pF	7.15	0.5112
			800pF	4.7	0.2209
			1200pF	3	0.0900
		2.0 Inch	0pF	3.5	0.1225
			400pF	7.1	0.5041
			800pF	4.45	0.1980
			1200pF	2.45	0.0600
		2.5 Inch	0pF	2.55	0.0650
			400pF	5.75	0.3306
			800pF	3.95	0.1560
			1200pF	2	0.0400

the tuning capacitance values where peak efficiency occurs are different which are summarized in Table 4.1-1. With reference to the table, in the Harmonic Balance simulations, the maximum efficiency occurs at larger tuning capacitance values than the experiments.

Another difference seen between the function generator and the Class-E power amplifier results with a tuning capacitance of 1600pF at 0.5 inch separation distance which is shown in Table 4.1-3. We see from the table that using the function generator as an input into the MCR-WPT coils with a 1600pF tuning capacitance the efficiency worsens, on the other hand, there is an efficiency improvement when using the Class-E as an input. We also note that the 1600pF tuning capacitor in parallel with 50Ω output resistor act like a low-pass filter with a cut-off frequency near 2MHz. This could partially explain the efficiency decrease after adding the 1600pF tuning capacitance. Also with the larger input power from the Class-E amplifier, a larger current is presented to the tuning capacitor which allows it to charge and discharge faster than our frequency and helps to bring the system back into resonance. However, these theories could not be explored more since we were limited to 2 Class-E Amplifier experiments due to reasons described in section 4.1.4.

A third observation is seen with the function generator input and a small tuning capacitor at the output of the MCR-WPT coils. There is an efficiency improvement at separation distances greater than the critical coupling distances found using the S-Parameter simulations. No reasons could be found to explain observation and can be further explored during future work.

Table 4.1-3 Comparison between the harmonic balance simulation results and the Class-E PA and function generator experimental results at 1600pF tuning capacitance and 0.5in separation distance.

8x4In Design, Tuning at 0.5 Inch Separation Distance			
Result Type	Output Power at Ctune = 0pF	Output Power at Ctune = 1600pF	Power Improvement
Harmonic Balance	0.071	0.162	128.17%
Function Generator	0.1024	0.0676	-33.98%
Class-E Amplifier	7.29	9.9225	36.11%

4.2 Maximum Peak Detection and Auto-Tuning

The maximum peak detection and auto-tuning portion of this thesis is based on the circuitry proposed in [66]. In the original work, the accumulation MOS varactor was designed using IBM CMRF8SF 130 nm 1.2V CMOS technology, with a tuning range of between 26.4fF and 70.7fF. The frequency of operation was greater than 2GHz and the voltage swing at the output of the secondary winding of the transformer was $4V_{p\text{-}p}$. At such a high frequency, this calibration tuning range was sufficient enough to improve the output efficiency by tuning the impedance and resonant frequency of the transformer matching network.

In our application, the Rezence standard specifies an operating frequency of 6.78MHz, and therefore much higher tuning capacitance range is required. As discussed in Appendix C, after exploring the three different types of analog varactors configurations, it was determined that they cannot be used within our auto-tuning system. This is because there are no off the shelf discrete accumulation MOS varactors available and that Vericaps and regular MOSFETs used as varactors are limited to operating in the reverse bias and the off regions respectively and cannot handle the expected ±30V at the outputs coils. An alternative discrete varactor is discussed in Appendix D and seen in Figure 5.2-12. Using this circuit configuration we can implement the auto-tuning system.

4.2.1 Maximum Peak Detection

To detect whether the amplitude (V_m) of the output load coil voltage signal ($v_o(t)$) has achieved the maximum peak value or not, we input $v_o(t)$ into the circuit which we refer to as V_{in} in Figure 4.2-1. The circuit is composed of 3 separate circuit blocks, a negative voltage shifter, half wave rectifier, and Comparator. The function of each circuit block within the maximum peak

detection system is discussed below.

4.2.1.1 Negative Voltage Level Shift

The V_{in} signal is the input of a negative voltage level shifter, formed by clamping capacitor C_{clamp} and the equivalent series Schottky diodes represented by D_{shift}. To ensure signal loss through this stage is 1% or less, according to Appendix A and using equation *(A.2)* we want $C_{clamp} \geq 100C_d$, where C_d is the equivalent series capacitance of the diodes. Therefore at the output of the negative voltage level shifter on node V_{shift}, the resulting signal has been shifted down by $V_m - V_{feq}$ where V_{feq} is the equivalent forward voltage drop across D_{shift}. Thus we get a signal with a positive peak value of V_{feq}, and a negative peak of $-(2V_m - V_{feq})$ as seen in the graphs in the second column of Figure 4.2-1. The positive pulse duration of time T_s can be calculated using the following equation

$$T_s = \frac{\pi - 2 \cdot \left(\sin^{-1}\left(\frac{V_M - V_{feq}}{V_M}\right)\right)}{2\pi f} \tag{4.1}$$

The reader is encouraged to go through Appendix A for more information about passive voltage level shifters.

4.2.1.2 High-Speed Half Wave Rectifier

Next, the V_{shift} signal is sent through a half-wave rectifier composed of a high-speed diode and resistor as shown in Figure 4.2-1. This circuit is not in the original design [66], but due to the ±30V V_{in} signal entering the system it must be included in our design, to ensure that at the V_{rect} node the voltage swing is within the absolute maximum input voltage rating of the comparator at the following stage. Since all real diodes exhibit a forward voltage drop, it must be taken into consideration. Therefore at the output of the rectifier at node V_{rect} the peak signal voltage

$$V_{req} = V_{feq} - V_{frect} \tag{4.2}$$

where V_{frect} is the forward voltage drop across the

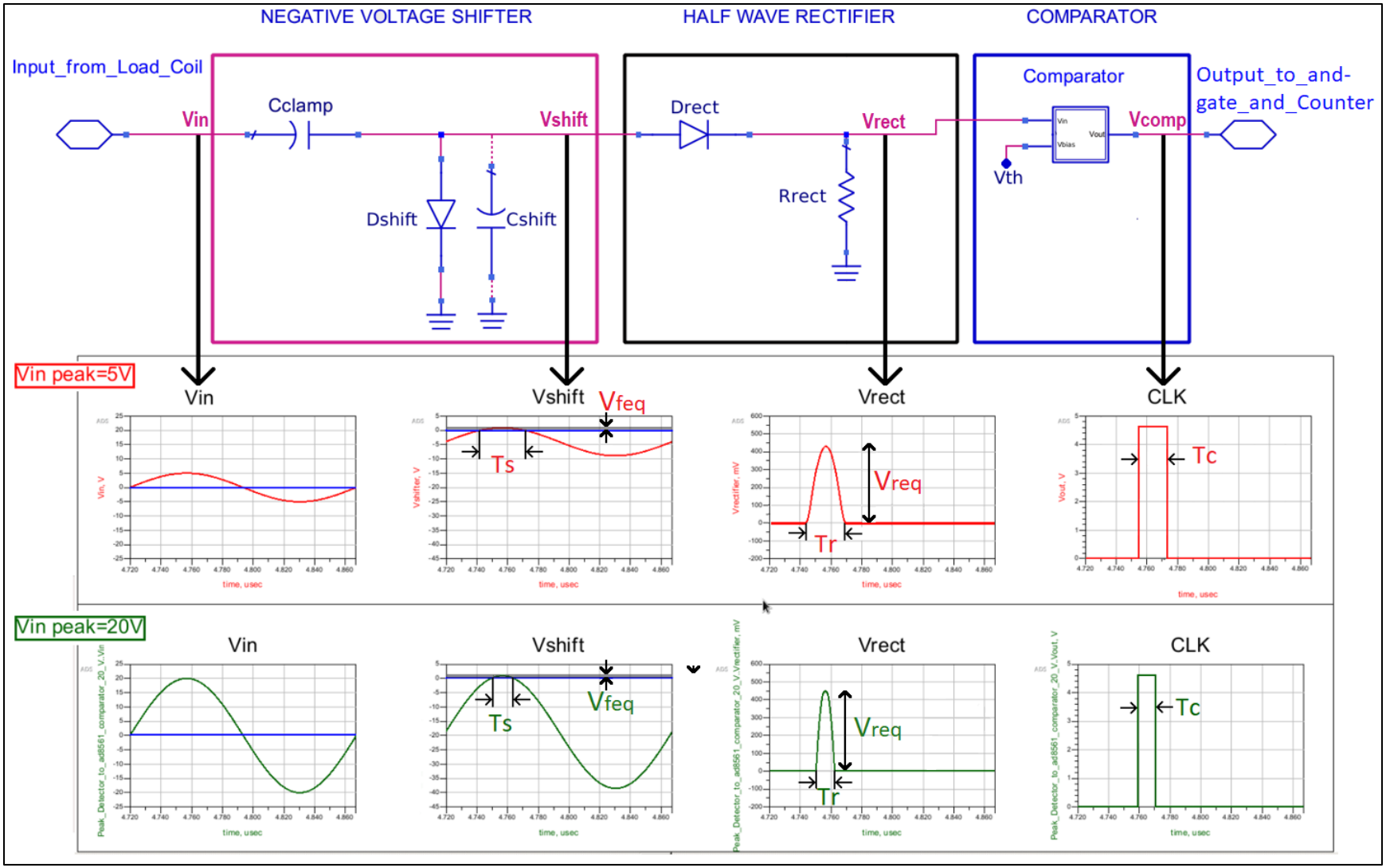


Figure 4.2-1: Maximum peak detection circuit and with ideal nodal waveforms for 5V and 20V peak signals.

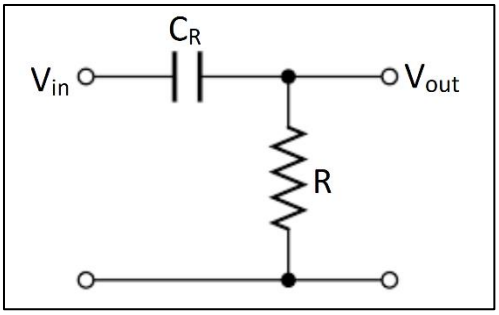


Figure 4.2-2: High-pass filter formed by the half-wave rectifier in reverse bias mode, where C_r is the reverse bias capacitance.

diode D_{rect} as shown in the graphs in the third column in Figure 4.2-1. The resulting pulse duration is T_r is calculated using equation (4.3) below. Another factor that must be taken into consideration

$$T_r = \frac{\pi - 2 \cdot \left(\sin^{-1}\left(\frac{V_M - V_{req}}{V_M}\right)\right)}{2\pi f} \tag{4.3}$$

when selecting a rectifier diode is the reverse bias capacitance (C_r). As seen in Figure 4.2-2, when the circuit is in reverse bias it forms a high pass filter. Therefore that to ensure the signal is cut off during reverse bias mode, C_r needs to be as small as possible. According to equation (*G.3*), f_c is inversely proportional to both R and C_R, therefore when selecting the resistor value there is a trade-off between rectifier power consumption and rectifier functionality.

4.2.1.3 High-Speed Comparator

Finally, the Vrect signal is inputted into the comparator as seen in Figure 4.2-1. The comparator performs a few key functions within the maximum peak detection and auto-tuning system. Its fundamental function is to generate a digital pulse on the output V_{comp} node when the input signal pulse from the rectifier exceeds the comparator's input threshold voltage. The pulse is then inputted to an AND-gate at the first stage of the auto-tuning system. To further describe its functionality, we refer to Figure 4.2-3. Assuming an ideal comparator with zero propagation delay (T_{PD}) and a threshold voltage (Vth) of 0V, we see that the output rectifier pulse width T_r and

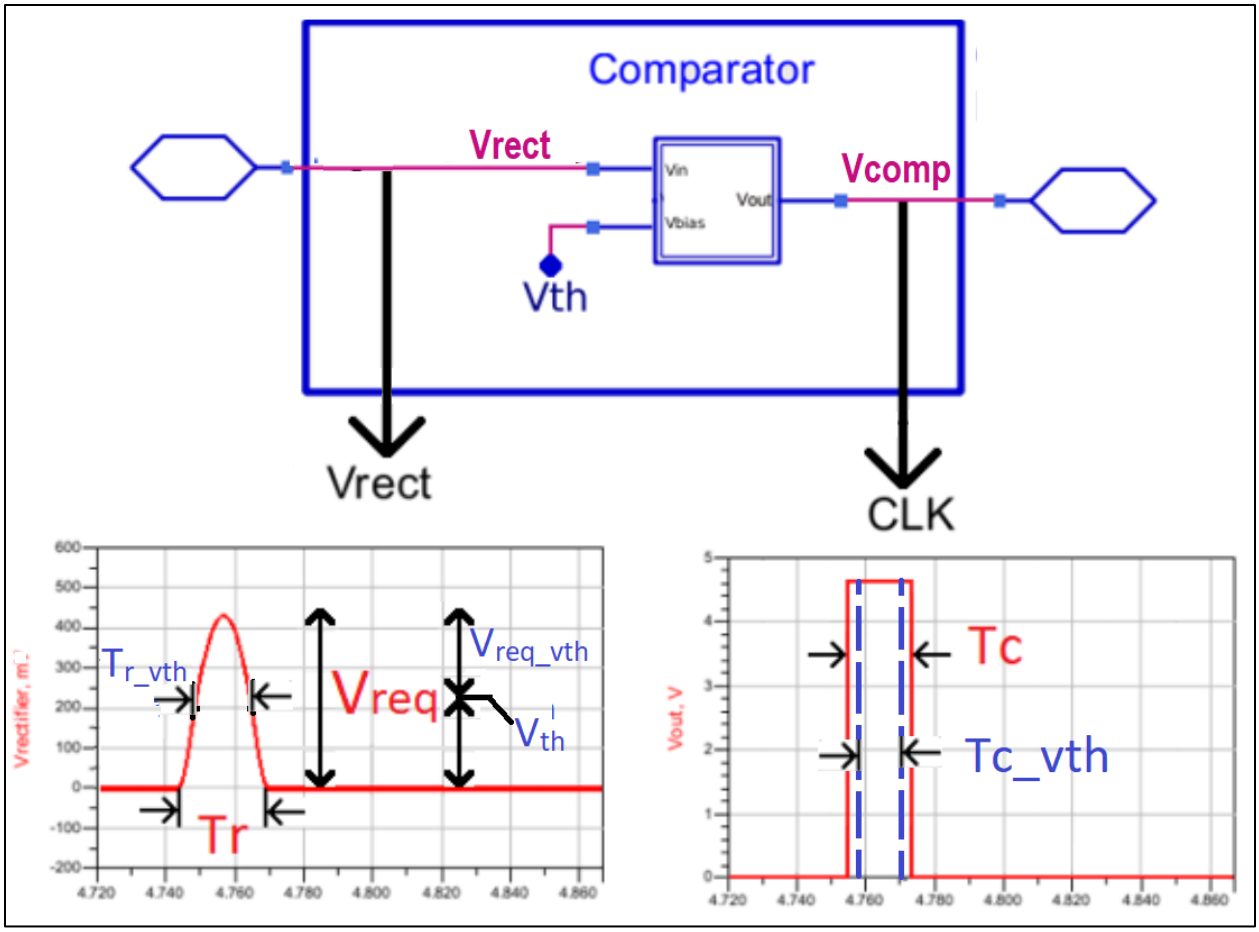


Figure 4.2-3: Maximum peak detector comparator functionality when v_{th} = 0V and V > 0V.

the input pulse width seen by the comparator are the same, and the comparator generates a digital pulse with a width T_C shown in red. On the other hand when Vth > 0, the pulse width T_{r_vth} seen at the input of the comparator is smaller than T_r, resulting in a smaller comparator output digital pulse with a width of T_{c_vth} shown in blue. We can calculate the pulse duration of T_{c_vth} by substituting V_{req} with V_{req_vth} from equation *(4.3)*, to get

$$T_{r\_vth} = \frac{\pi - 2 \cdot \left(\sin^{-1} \left(\frac{V_M - V_{req\_vth}}{V_M} \right) \right)}{2\pi f} \tag{4.4}$$

where $V_{req\_vth} = V_{req} - V_{th}$. This functionality is very useful when calibrating the system to detect the maximum peak.

The second function of the comparator, together with the AND-gate and the counter from the auto-tuning circuit (whose functions are discussed further in section 4.4.2) is to detect when the maximum peak of the system has been achieved. In other words, the accuracy of the maximum peak detection circuit is limited by the sum of the propagation delays (T_{PDeq}) of the comparator (T_{PDcomp}), AND-gate (T_{PDand}) and Counter ($T_{PDcount}$). So when the condition for equation (*4.5*) is fulfilled, the system has determined that the maximum peak has been detected.

$$T_{PDeq} \leq T_{PDcomp} + T_{PDand} + T_{PDcount} \tag{4.5}$$

4.2.1.4 Maximum Peak Detection Circuit Design Considerations & Functionality Overview

In the overall operation of the Maximum Peak Detection circuit, the system shuts off when the maximum peak is detected. With reference to Figure 4.2-1, we inputted a V_{in} of 5V and 20V and display the results for each stage of the system in 2 separate rows. We can see that at every stage the pulse widths for the 20V input signal are smaller than the 5V input signal. Assuming that 20V is the maximum peak of the MCR-WPT coils we, can adjust the comparator V_{th} so that the input detected pulse with $T_{r\_vth} \approx T_{PDeq}$. So the system is designed to shut off when the peak is detected.

When designing the maximum peak detection circuitry, we must consider the peak voltages, the pulse widths and the propagation delays at each stage. We are given the maximum expected peak voltages of the MCR-WPT coils based on its design specifications and can extract the propagation delays and the forward voltage drops from the digital circuits and diodes respectively. Working backward, we calculate the T_{PDeq} which limits the accuracy of maximum peak detection circuit using equation *(4.5)*. Since $T_{r\_vth} \approx T_{PDeq}$ at the maximum expected peak value, we can work our way backward and calculate the peak voltages V_{feq}, V_{req}, V_{req_vth} that we

need. Using this information and Appendix A.2, B.2, and D.3, we can select passive and active components for the maximum peak detection circuit.

4.2.2 Auto-tuning

To change the capacitance at the output of the load coil after every maximum peak detection step, we input the output pulse from the comparator (Vcomp) to the auto-tuning circuit as shown in Figure 4.2-4 below. The circuit is composed of 3 separate circuit blocks, namely an AND-gate, a high-speed counter and the digitally tuned capacitance circuit. The function of each circuit block within the auto-tuning system is discussed below.

4.2.2.1 High-Speed AND-Gate

The AND-gate is the first circuit block in the auto-tuning system. Its main functions are to delay the auto-tuning circuitry during the initial setup time of the negative voltage shifter and to control the periodicity of each tuning step. These tuning steps are needed when the maximum Peak detection circuit is initiated because the C_{clamp} capacitor (from section 4.2.1.1) is large and needs some setup time to charge before the auto-tuning circuitry should start auto-tuning. Also depending on the severity of the frequency splitting, the MCR-WPT system coils can require up to a few nanoFarads of capacitance before the maximum peak is detected. These large capacitance values have time constants longer than the period of our f_o frequency. Thus the tuning step pulse (Enable_Pulse) can be adjusted to allow each incremental capacitance increase sufficient time to charge before checking the following maximum peak detection step. This prevents the auto-tuning circuit from locking at a larger capacitance value than the actual maximum peak capacitance value at the output, causing the peak detected to smaller than the actual maximum peak.

The second function of the AND-gate is its contribution to the overall accuracy of the

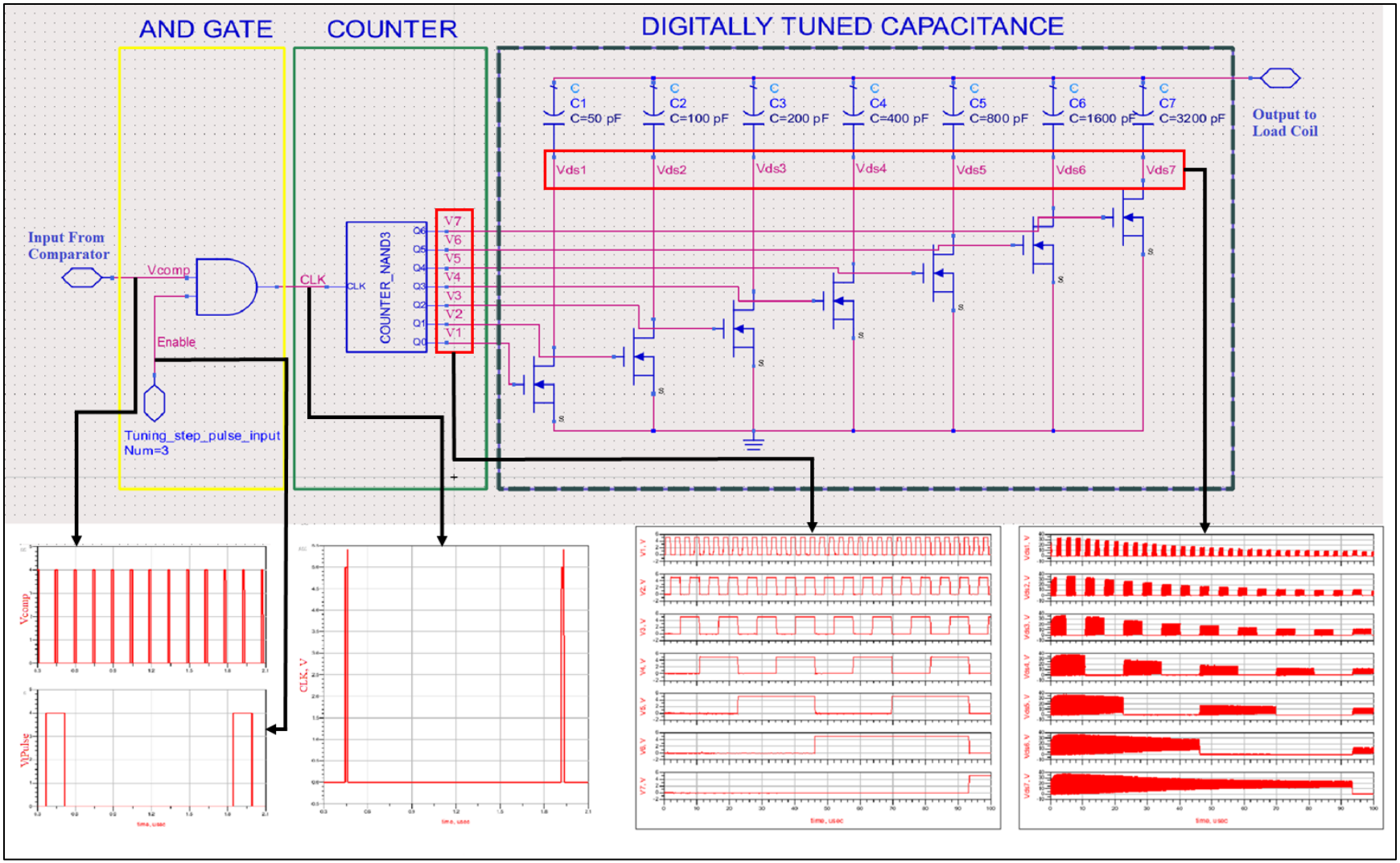


Figure 4.2-4 Auto-tuning circuit with output plots at each node.

maximum peak detection circuitry. This is because AND-gate propagation delay contributes to overall accuracy as shown in equation *(4.5)*, and must thus be considered in the design.

4.2.2.2 High-Speed Binary Counter and Digitally Tuned Capacitance Circuit

For our implementation of the auto-tuning system, we use a combination of a High-Speed Binary Counter and a digitally tuned capacitance circuit to replace the charge pump and analog varactor in the originally proposed auto-tuning circuit in [66]. We settled on this configuration when it was discovered that a suitable analog varactor device that meets our design specifications could not be found. The original accumulation MOS varactors used in [66] are limited to ASIC design and no discrete devices are manufactured. The alternative PN-junction varactor and regular MOSFETs as a varactor devices can't be used because they are sent into forward-bias due to the large voltage swings at the output of the MCR-WPT coils. These issues are discussed further in Appendix C for the reader's convenience.

The high-speed binary counter has 2 main functions with the auto-tuning system. Its primary function is to discretely increment the capacitance on the output of the MCR-WPT coils with every tuning step. And like the comparator and AND-gate before it, the propagation delay of the counter partially contributes to the overall accuracy of the maximum peak detection system as shown in equation *(4.5)*. Besides the propagation delay, there are other parameters that should be considered when selecting a high-speed counter. These parameters are further discussed in Appendix D.1.

The MOS switches are used to connect the capacitors to the output MCR-WPT coils. The gate each MOS switch is connected to a binary output of the counter and the drain is connected to a capacitor as outlined by in the Digitally Tuned Capacitance portion the auto-tuning circuit in

Figure 4.2-4. So with every tuning step, the capacitance is incremented. The design parameter for selecting the MOS switches such as a small gate charge, a low drain-source resistance and current among other parameters are discussed in more detail in Appendix D.2.

4.3 Simulation Results

4.3.1 Specifications

Before going into the simulation setup, we establish the specifications for the Maximum Peak Detection and Auto-Tuning simulations test Setup. The specifications are as follows

- Negative Voltage Shifter
    - D_{shift} Diode junction capacitance (C_j) ≤100pF
    - D_{shift} Diode Reverse Voltage (V_R) ≥40V
    - Clamp Capacitance ≥10nF
- Half Wave Rectifier
    - Diode junction capacitance (C_j) ≤1pF
    - Diode Reverse Voltage (V_R) ≥40V
    - Diode on Resistance ($R_{DS(ON)}$) ≤250Ω
    - Resistance (R) ≤250Ω
- High-Speed Comparator
    - T_{PD} ≤10ns
    - VIO ≤10mV
- AND-Gate
    - T_{PD} ≤5ns

- High-Speed Binary Counter
    - T_{PD} ≤5ns
- MOS Switch
    - $R_{DS(ON)}$ ≤5Ω
    - Ciss ≤50pF

To satisfy the specifications for the negative voltage level shifter, the STPS5L60 Schottky diode was chosen. Although it has a 700pF max C_j, since multiple components are connected in series this is reduced to within our desired specification. For the half wave rectifier, the BAS70 was selected. It was the fastest diode available that meets our $V_R \geq 40V$ specification, but it has a 5pF max C_j which is larger than our desired max value of 1pF. For circuit simplicity, the comparator and standard logic devices have VDD = 5V. With a 7ns t_{PD}, the AD8561 ultrafast comparator was selected. The 74LVC1G08 AND-gate and the SN74LV4040A counter were selected having a t_{PD} of 4ns and 3.5ns respectively. Finally, the DMG1029SV with a maximum $R_{DS(ON)}$ of 3Ω and Ciss of 42pF will be used as the MOS switch. The selected components and their parameter values are summarised in Table 4.3-1 below.

Table 4.3-1 List of discrete electronic components and key parameters used in maximum peak detection and auto-tuning simulations.

Component	Parameter	Value (max value or range)	Description
STPS5L60	C_j	100-700pF	Negative Voltage Shift Diode
	V_R	60V	
BAS70	C_j	1-5pF	Half Wave Rectifier Diode
	V_R	70V	
	$R_{DS(ON)}$	8-250Ω	
AD8561	t_{PD}	7ns	High-Speed Comparator
	VIO	7mV	
74LVC1G08	t_{PD}	4ns	High-Speed AND-Gate
SN74LV4040A	t_{PD}	3.5ns	High-Speed Counter
DMG1029SV	$R_{DS(ON)}$	3Ω	MOS Switch
	Ciss	42pF	

4.3.2 Simulations Setup

The schematic of the simulation test bench is shown in Figure 4.3-1 with all of the circuit blocks labeled. A simulation test bench was set up using Keysight's ADS software to verify the Maximum Peak Detection and Auto-Tuning theory proposed in this chapter. A 40V and 16Watt input signal is sent through the EM models from the EMPro S-Parameter simulation results for various separation distances in 0.5in increments until the CCD. An ideal 1:1 transformer, and the CSD01060 SiC diode bridge rectifier and smoothing capacitor used in section 2.4.3 are connected to the output of the EM models of the MCR-WPT coils. The maximum peak detection and auto-tuning circuit, composed of a delay switch, negative voltage level shifter, half wave rectifier, tuning step input pulse, AND gate, counter, and digitally tuned capacitance, is integrated into the system by connecting the input of the delay switch and the discrete capacitors to the output.

All components and their respective circuit blocks are set up as follows. The delay switch has a timer of 200μs for smaller separation distances where there is lower efficiency due to severe frequency splitting and a small output power before tuning, and 400μs for larger distances closer to the CCD. This was done to allow enough setup time for the MCR-WPT coil system to stabilize before the maximum peak detection and auto-tuning circuitry was enabled. The negative voltage level shifter has is a clamping capacitor of 10nF connected to 8 STPS5L60 diodes in series allowing an output signal with a positive peak value of ~3.2V. In the half-wave rectifier, the BAS70 diode is connected in series to a 200Ω resistor. The AD8561 high-speed comparator input threshold voltage is 110mV. The Enable tuning step input pulse width is set to (1/6.78MHz) seconds and the period to (250*6.78MHz) seconds. The 74LVC1G08 AND gate, SN74LV4040A counter and MOS switches are connected as shown, with binary-valued capacitors of 100pF, 200pF, 400pF, 800pF, 1600pF, and 3200pF are connected to the drain of the MOS switches.

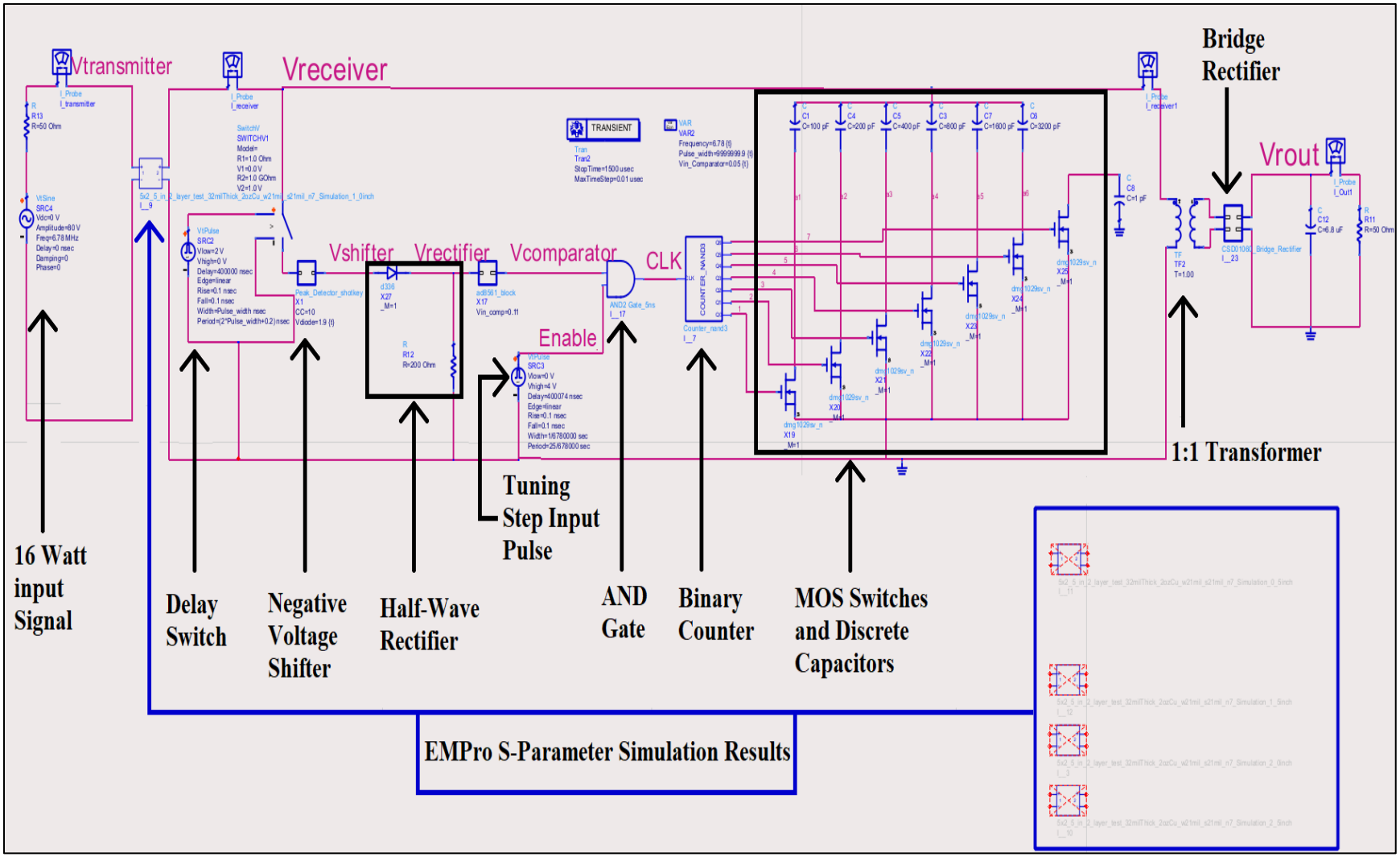


Figure 4.3-1 Maximum peak detection and auto-tuning simulation test bench schematic in ADS.

There are some issues that were encountered which affect the simulation setup that should be mentioned. The Pspice models for most of the components were retrieved from their respective manufacturers' websites and used in the simulations. Pspice models for the high-speed AND-Gate and counter could not be found. Since they are Standard Logic Gate components, the industry standard IBIS (I/O Buffer Info Specification) models are provided. The IBIS model is an input and output port behavior model instead of a functional circuit model like the pspice and hspice. This means that a closed loop transient simulation could not be run using this model. To overcome this issue, an AND gate and a counter were made in ADS by modifying the pspice model of the DMG1029SV MOSPHET by changing the capacitances and resistances in the NMOS and PMOS spice models so that they switch at a higher rate of speed. Using these components, we created an AND Gate and D-flip-flops used to create the counter and simulated them to get their timings as close as possible to the timing characteristics found in their respective datasheets.

Simulations were done on the 5in x 2.5in and 8in x 4in MCR-WPT coil designs and the results are shown in the following sections. The 6 graphs in each of the figures describe the following information. The red plot is the **Vreceiver** voltage output of the MCR-WPT coils. In purple is the **Vshifter** voltage at the output of the negative voltage shifter. Represented by the orange plot is the **Vrectifier** voltage at the output of the half wave rectifier. Next is the **Vcomparator** voltage at the comparator output in light blue. Then the AND gate output voltage **CLK** in green. And finally the Vrout voltage output of the bridge rectifier.

4.3.3 Auto-Tuning 5x2.5In MCR-WPT Coils

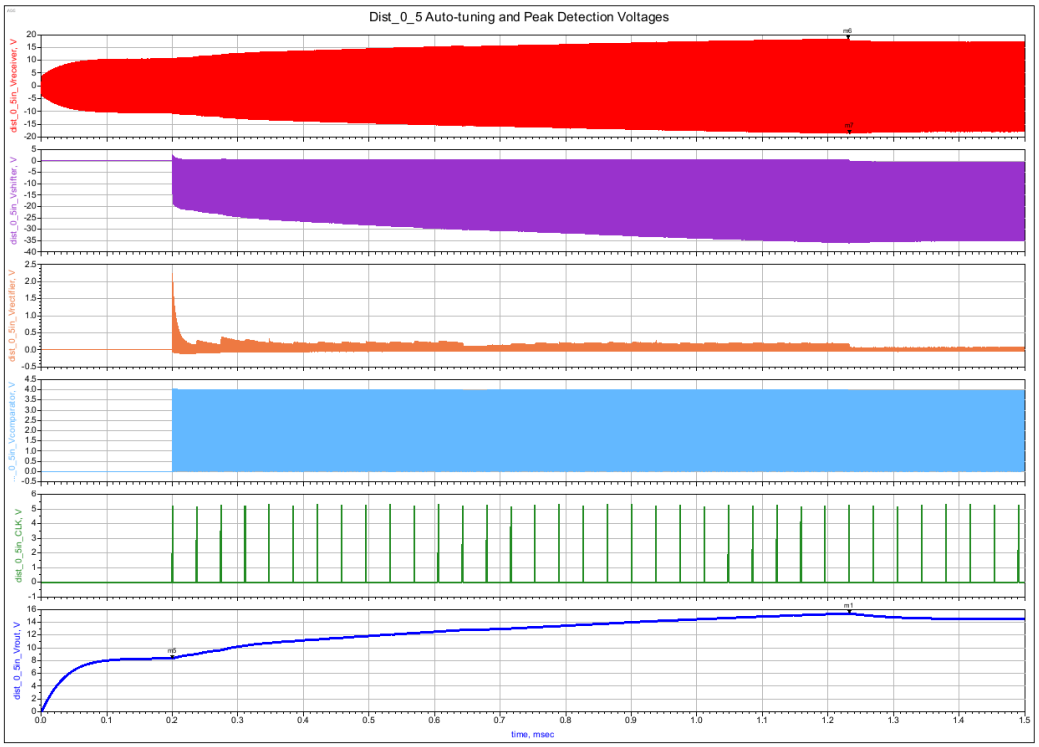


Figure 4.3-2 5x2.5In MCR-WPT coil design maximum peak detection and auto-tuning simulation data display results in ADS at 0.5in distance.

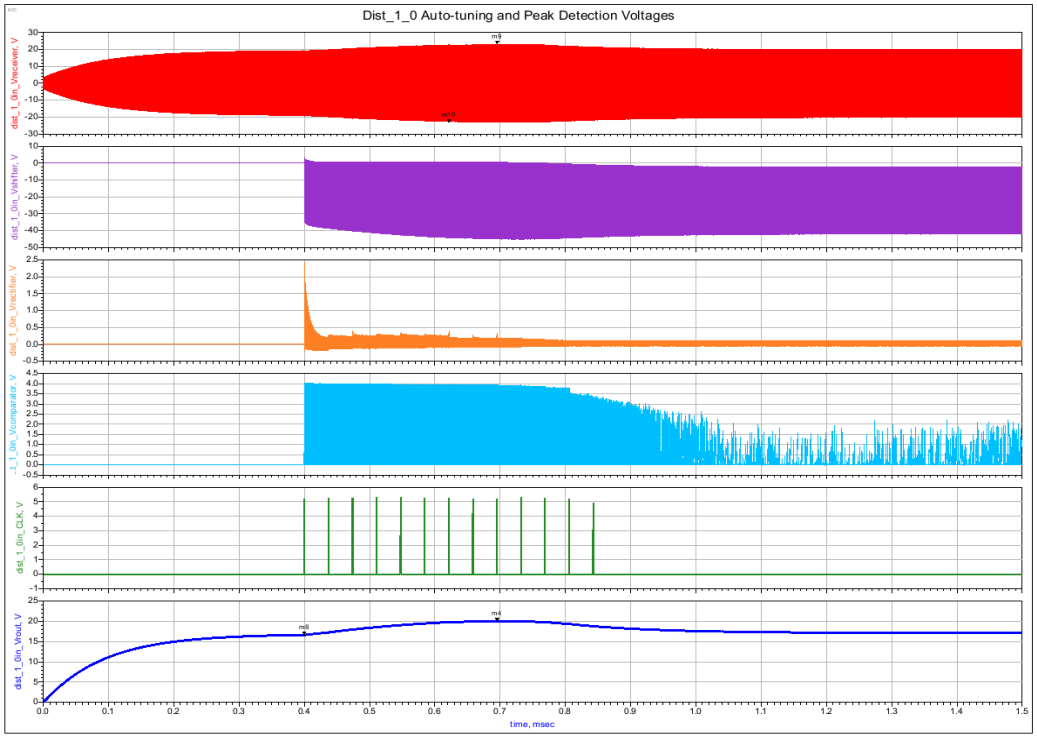


Figure 4.3-3 5x2.5In MCR-WPT coil design maximum peak detection and auto-tuning simulation data display results in ADS at 1.0ih distance.

4.3.4 Auto-Tuning 8x4In MCR-WPT Coils

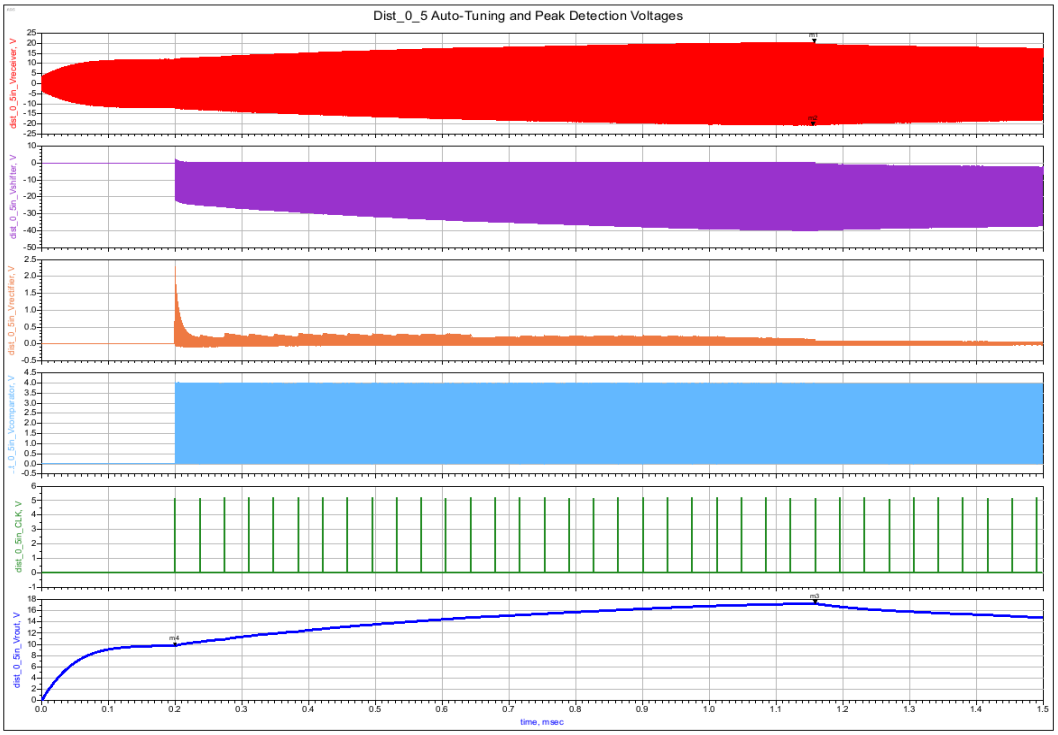


Figure 4.3-48x4In MCR-WPT coil design maximum peak detection and auto-tuning simulation data display results in ADS at 0.5in distance.

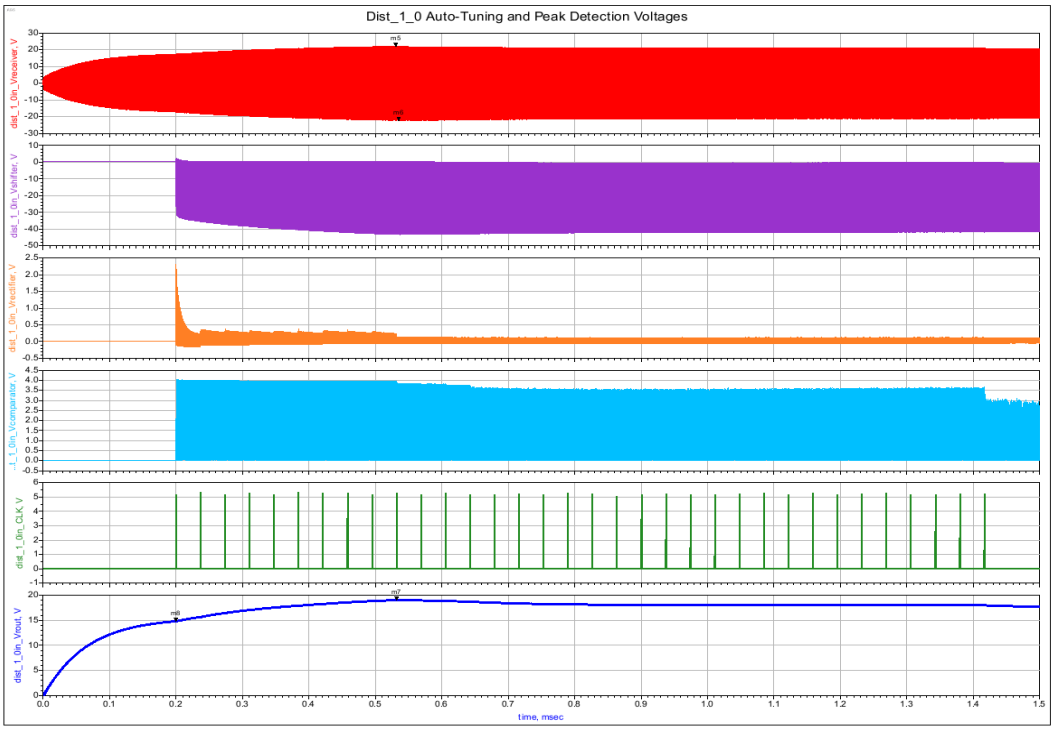


Figure 4.3-5 8x4In MCR-WPT coil design maximum peak detection and auto-tuning simulation data display results in ADS at 1.0in distance.

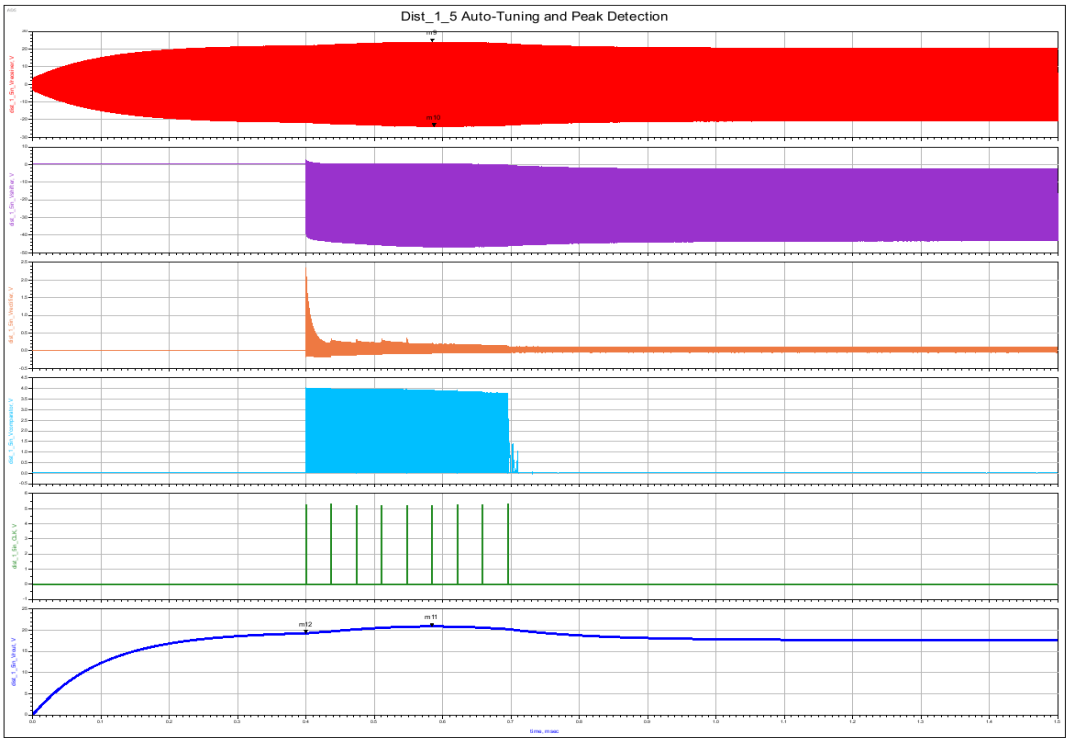


Figure 4.3-6 8x4In MCR-WPT coil design maximum peak detection and auto-tuning simulation data display results in ADS at 1.5in distance.

4.3.5 Results Summary and Discussion

Looking at the simulation results we see that overall the auto-tuning system generally works. When we turn on the maximum peak detection and auto-tuning system, the Enable signal at the input of the AND gate is high for one frequency pulse width. This allows the Vreceiver signal go from the negative voltage level shifter through the whole system and the CLK signal pulse generated from the comparator through the AND gate increments the counter connecting the 100pF capacitor. The system then waits for 250 more frequency cycles to allow the system time to approach steady state before the next enable pulse. These CLK pulses are plotted in green as seen in Figure 4.3-2, Figure 4.3-3, Figure 4.3-4, Figure 4.3-5, and Figure 4.3-6 above. In between each pulse, we see that immediately after each incrementation of the counter, the amplitude of the Vrectifier output signal from half wave rectifier (plotted in orange) jump up and then slowly decays. This pattern occurs every tuning step and can especially be seen in Figure 4.3-2 and Figure

4.3-4 where frequency splitting is severe. These patterns are due to the charging of the C_{clamp} capacitor in the negative voltage shifter due to the increased amplitude of Vreceiver (in red) after every tuning step. The tuning continues until the amplitude of the decayed Vrectifier output signal is lower than the input comparator threshold voltage. The tuning improvements for all the simulations are marked in the bridge rectifier Vrout plots (in blue) in their respective figures.

To get a better view of the tuning improvements, the bridge rectifier output power plots for maximum peak detection and auto-tuning simulations done on the 5in x 2.5in and 8in x 4in MCR-WPT coil designs at multiple separation distances shown in Figures 4 40 and 4 41 respectively. The output power values before tuning and at maximum output power are shown below each plot and summarised in Table 4.3-2 . From the table, we see that the longest tuning times of 1.033ms and 0.959ms occur at the smallest separation distances when frequency splitting is most severe. These worst case tuning values when compared to other tuning methods perform reasonably as shown in Table 4.3-3. It can also be seen in Table 4.3-2 that this is where we get the most significant output power improvements of 240% and 212%. The improvements however gradually decrease as we increase the separation distance. This result expected since as we increase the distance we get closer to the CCD as was shown in section 4.1.3. Except at the 0.5in separation distances

Table 4.3-2 Tuning time, tuning capacitance and bridge rectifier output power before tuning and at maximum efficiency for 8x4In and 5x2.5In MCR-WPT coils maximum peak detection and auto-tuning simulations at different separation distances.

MCR-WPT Coil Design	Separation Distance (inches)	Output Power Before Tuning (Watts)	Peak Output Power (Watts)	Tuning Capacitance (pF)	Output Power Increase	Tuning time (ms)
5in x 2.5in	0.5	1.388	4.725	3100	240%	1.033
	1	5.38	8.002	1200	49%	0.295
8in x 4in	0.5	1.913	5.961	3100	212%	0.959
	1	4.375	7.229	1600	65%	0.332
	1.5	7.401	8.739	900	18%	0.185

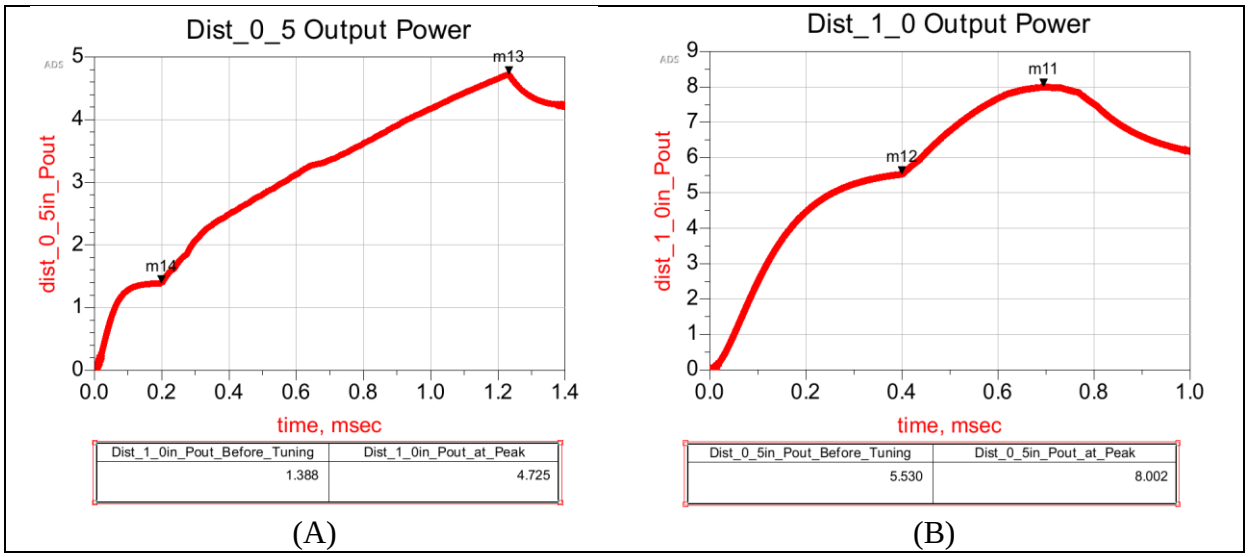


Figure 4.3-7 5x2.5In MCR-WPT coil design maximum peak detection and auto-tuning output power simulation data display results plots: (A) 0.5 inch separation distance; (B) 1.0 inch separation distance.

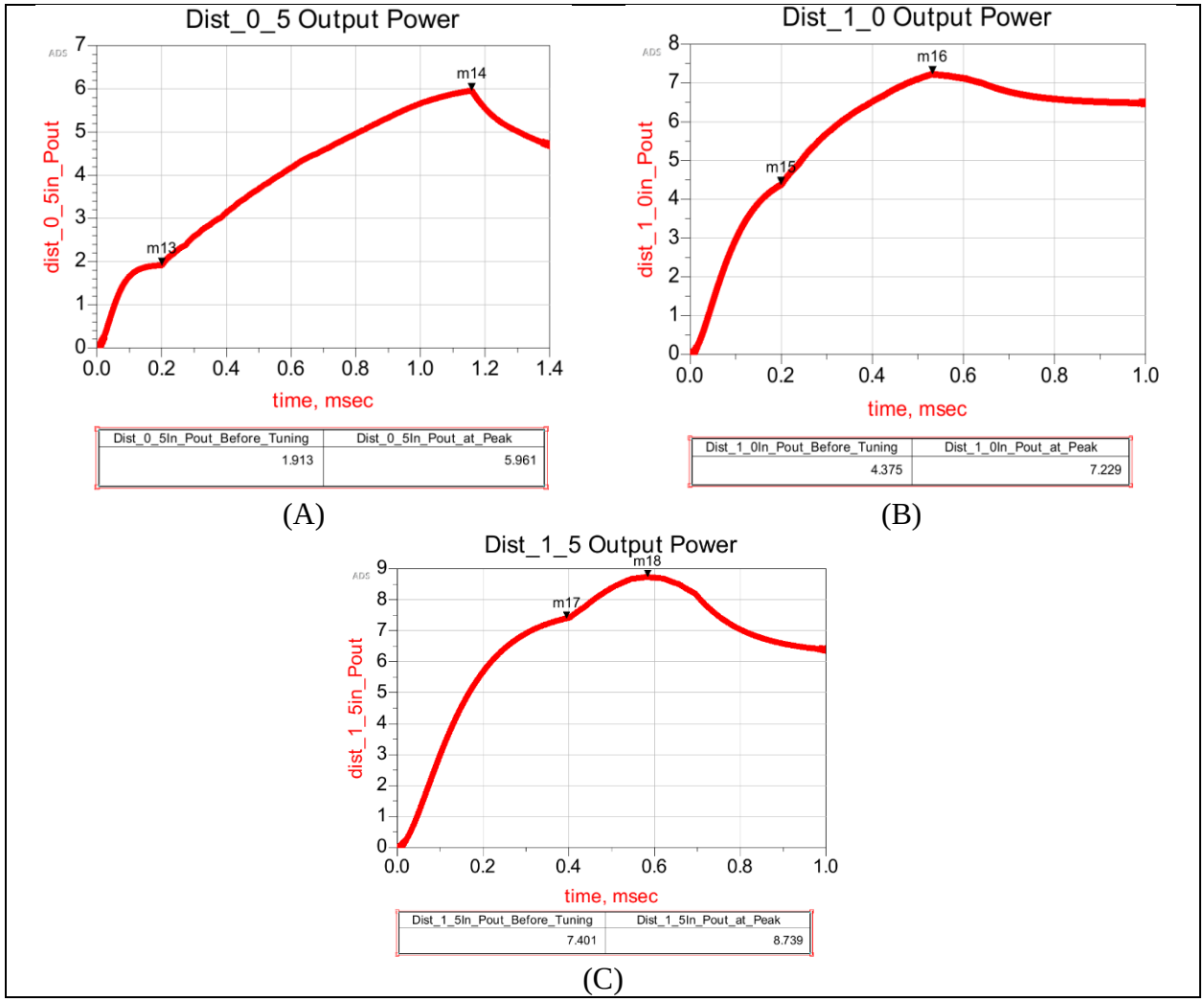


Figure 4.3-8 8x4In MCR-WPT coil design maximum peak detection and auto-tuning output power simulation data display results plots: (A) 0.5in separation distance; (B) 1.0in separation distance; (C) 1.5in separation distance.

Table 4.3-3 Comparison of tuning times to reconfigure the system for maximum efficiency with other methods.

Parameter	[67]	[68]	[69]	**Proposed Method**
Response Time (To reconfigure system for maximum efficiency)	6s (tune impedance)	3.5ms (tune frequency)	~ 0.3s (tune frequency)	1.033ms (to tune output impedance)

the capacitance values where maximum output power occurs are close to the Harmonic Balance tuning values from in Table 4.1-1. There are however other issues that arose from the simulations

With reference to the output power plots for both coils designs with 0.5 separation distances shown in Figure 4.3-7 (A) and Figure 4.3-8 (A), we see that right after the maximum peak power, there is a sharp decline in output power as the tuning capacitance continues to increase. This sudden change from increasing to decreasing output power happens when changing from 3100pF to 3200pF. This can be attributed to all capacitors connected to the 5 lower bits of the binary counter (the 100pF, 200pF, 400pF, 800pF and 1600pF capacitors) being disabled and the 3200pF being enabled. The exact cause of this issue could not be determined in time but one possibility for this is that because the 3200pF has a large time constant, the initial charge is near small causing a dip. A more likely cause is that the large capacitor acts more like a low pass filter that a bandpass filter due to insufficient current flow, causing the output power to decrease. This situation was also observed when conducting the physical frequency splitting tuning tests as described in section 4.1.4

. The next issue which arose is seen from all the plots in Figures 4 40 and 4 41, where the maximum peak detection circuitry didn't detect the maximum peak and the auto-tuning circuitry increased the capacitance past the capacitance for maximum efficiency. This issue is mainly due having to the inaccuracies associated with propagation delay times of the created AND gate and counter deviating from the timing values found in their respective the data sheets.

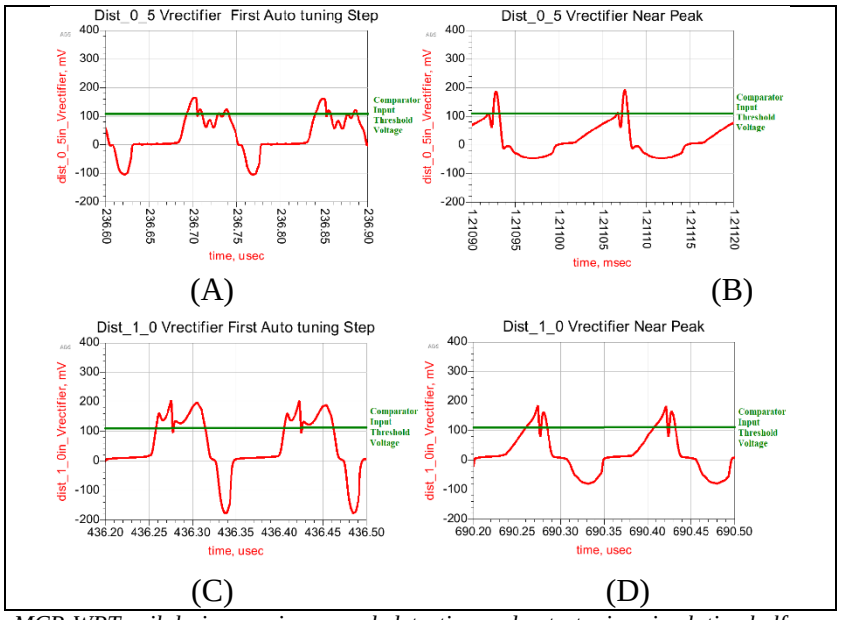


Figure 4.3-9 5x2.5In MCR-WPT coil design maximum peak detection and auto-tuning simulation half wave rectifier simulation data display results plots: (A) and (B) first tuning step and near peak at 0.5in separation; (C) and (D) first tuning step and near peak at 1.0in separation.

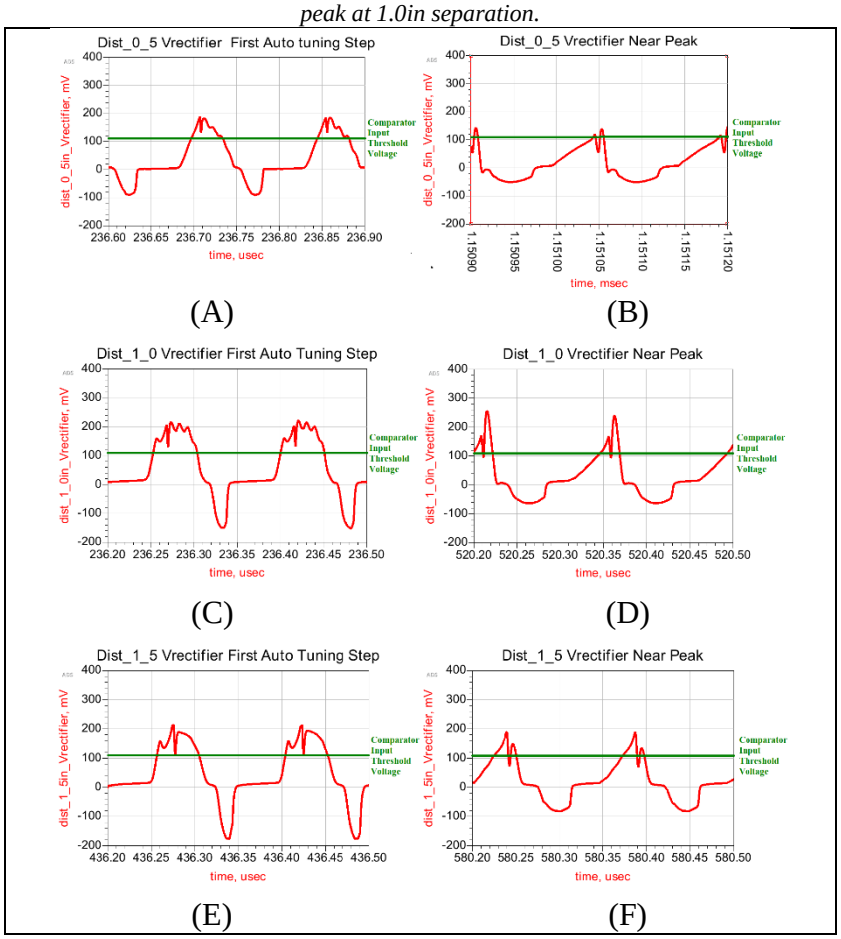


Figure 4.3-10 8x4In MCR-WPT coil design maximum peak detection and auto-tuning simulation half wave rectifier simulation data display results plots: (A) and (B) first tuning step and near peak at 0.5 inch separation; (C) and (D) first tuning step and near peak at 1.0 inch separation; (E) and (F) first tuning step and near peak at 1.5 inch separation distance

An issue is also found in the half-wave rectifier. The plots of the Vrectifier output signal of the half wave rectifier for 2 cycles (~300ns) when the maximum peak detection and auto-tuning system is initially turned on and near maximum power is achieved is plotted for the simulations and are shown in Figure 4.3-9 and Figure 4.3-10 to help with analysis. Referring to these figures, the problem contributing this issue is that the resulting output pulses aren't as smooth and stable as compared to the pulses seen in Figure 4.2-3. This is because the reverse bias capacitance of the diode gets larger as the input signal from the negative voltage level shifter gets near the 0V mark, and then drops rapidly once in forward-bias. As mentioned in section 4.2.1.2, when this capacitance is too large input signal leakage feed-though occurs causing changes to the output signal. There causes a slow voltage increase on Vrectifier as the input signal nears the 0V mark. When the diode goes into forward-bias, the voltage would dip and then increase again revealing the desire pulse signal. Afterwards, the diode would the go into reverse bias mode, and the large capacitance near the 0V would cause a decrease in voltage below 0V before the settling at 0V. These observations are best seen in Figure 4.3-9 (B) and (D), and Figure 4.3-10 (B), (D), and (F) when the tuning is near maximum efficiency. Because of this issue, it makes it difficult to bias the comparator threshold voltage and causes the auto-tuning capacitance to overshoot the peak capacitance value.

Another issue that arose is that the number pulses seen in the green CLK plots from the figures in sections 4.3.3 and 4.3.4 do not match the capacitance values where maximum efficiency occurs. This is due to irregular peaks and valleys sometimes occurring above and below the comparator threshold voltage which can be seen in Figure 4.3-9 (A) and (D) as well as in Figure 4.3-10 (B), (D), and (F). This causes the comparator to generate 2 pulses during the ~150ns Enable tuning cycle. Since the green CLK plots from the figures in sections 4.3.3 and 4.3.4 are multiple

milliseconds long, the nanosecond pulses cannot be distinguished in these pulses.

4.4 Chapter Summary and Conclusions

In this chapter, we first explored what frequency splitting is and the problems associated with it. We analyzed the effect of adding a tuning capacitance to the output of the MCR-WPT coils designed in chapter 3 through simulations and physical tests. S-Parameter simulations showed through observations discussed in section 4.1.3.1, that if the MCR-WPT coil critical coupling distance SRF is less than the operational frequency, the efficiency gain is larger than the gain at the operational frequency than at the SRF. The trade-off is that the MCR-WPT operational distance range is reduced.

There were some discrepancies between the experimental and simulation results, which were attributed to the large tuning capacitances in parallel with the load resistance. System efficiency decreased when a small input power signal is present. In this case, it seems that the tuning capacitor in parallel with the load resistance acts like a low pass filter, thereby decreasing the efficiency. However, in the presence of a larger input power, the system efficiency improved. The tuning capacitance improves the resonance of the system resulting in improved efficiency.

A method of improving the efficiency of the MCR-WPT coils in the presence of frequency splitting was presented. We proposed a Maximum Peak Detection and Auto-Tuning technique to automatically improve MCR-WPT coil efficiency in the presence of frequency splitting. The proposed system is composed of a negative voltage shifter, half wave rectifier, comparator, AND gate, binary counter, MOS switches and discrete capacitances circuit blocks, connected to the output of the MCR-WPT coils in a feedback loop. The operation of each block is described using mathematical analysis where applicable, and showing the input and output waveforms. The

selection process the discrete components for each block is discussed also

Finally, the simulation model of the system is built and tested. Overall the simulated system works giving efficiency improvements as high as 240% in the presence of severe frequency splitting. The worst case tuning time to achieve maximum efficiency was ~1ms, which is shown to be good when compared to other methods. On the other hand, there are some problems seen in the simulation results. One of the main issues is that the tuning would overshoot the capacitance where maximum efficiency occurs. This is due to the propagation delay errors between the datasheets and the created AND gate and counter. The signal feed-through from the input to the output also contributed to the irregular pulses, making it difficult to bias the threshold voltage of the comparator so that it turns off when the peak occurs. The irregular pulses also caused another error, where the comparator generates 2 pulses during the ~150ns Enable tuning cycle due to the irregular peaks and valleys sometimes occurring above and below the comparator threshold voltage. Finally, there is a sharp decline in output power as the tuning capacitance continues to increase changing from 3100pF to 3200pF. This can be attributed to all capacitors connected to the 5 lower bits of the binary counter (the 100pF, 200pF, 400pF, 800pF and 1600pF capacitors) being disabled and the 3200pF being enabled.

Chapter 5

5 Conclusions and Future Works

5.1 Conclusions

The design of the analog Rezence Blocks was presented. The oscillator was designed using the Colpitts circuit and silver mica capacitors. Simulations and measurements verify the accuracy of the frequency generated. The efficiency specification of the devices from the Rectifier to the Class-E PA output was determined. We went through the selection of each block and the designed them to meet the respective specifications. Simulations and measurements were run on each block, and with the exception rectifier with a small input peak signal, the efficiency targets were met.

A Class-E PA Design Methodology modified from [25] for HF design is presented to simplify its design. Class-E PAs can theoretically achieve 100% efficiency and have a simplified circuit topology, but they are generally difficult to design. The various design equations are either simple and don't provide insufficient information [23], or the too lengthy [24] to be used for design analysis. The design methodology uses the ideal Class-E design equation from [23] to generate ideal Class-E drain impedances, used to impedance match the power FET output for Class-E operation. A Class-AB sinusoidal gate driver whose output was impedance matched to the Class-

E input was designed to drive the gate, as it enabled the Class-E to achieve higher output efficiency than the square wave input gate driver. Using this methodology, it was demonstrated that a high-efficiency Class-E PA using a low-cost power MOSFET can be designed.

Various types of MCR-WPT coil designs were explored in this thesis. A new multi-layer MCR-WPT PSC design is introduced which increases the efficiency and decrease the SRF of the coils. These coils are symmetric and simple to design as no vias are required. The coils can be stacked more than 2 layers, and the dielectric substrate material can be replaced with a substrate with a higher permittivity, to further improve the MCR-WPT PSC coil efficiency and SRF. Using this design MCR-WPT Rx receivers with high efficiency can be created to fit in Smartphones and smaller devices to meet the Rezence standard.

To design these coils a new MCR-WPT design flow was created. The flow takes advantage of the speed of the Momentum to do rapid simulations of MCR-WPT coil designs that give a good prediction of the MCR-WPT system SRF and efficiency. The design flow assumes that the spacing between the inner coil wire and outer coil inner turn is close to the wire spacing of the outer coil. Multiple simulations have verified the accuracy of the Momentum simulation estimations. Using this design flow, and the new MCR-WPT design, MCR-WPT coils were designed to meet the Rezence standard for a smartphone PRU using an alumina substrate.

An impedance matching auto-tuning technique to maximize the power transmission efficiency of the Rezence Tx and Rx resonators was proposed. It was shown that efficiency and resonant frequency are sensitive to distance changes due to frequency splitting. The tuning is achieved using a binary counter which increments a digitally tuned capacitance connected to the Rx resonator, composed of MOS switches and discrete capacitors in parallel. A maximum peak detection technique was used to identify the optimal tuning capacitance at which the maximum

power transmission efficiency was introduced. Multiple simulations were conducted using the MCR-WPT coils which verify the general operation of the tuning technique. The simulations were not perfect, as there were issues identified prevent optimal circuit operation.

5.2 Future works

The works that were presented in this thesis can be extended in many ways to achieve better performance and applied to other applications. We present some potential works that can be done based on this thesis. These works include fixing the auto-tuning design, and modifying the design to account for PRU position shifts and saving PRU space by moving some of the circuitry to the PTU

5.2.1 Fix Auto-Tuning Circuitry and Verify with Simulations and Measurements

There is more work to be done on the novel Auto-Tuning circuitry presented in this thesis to ensure proper operation. The peak detection problems with the half wave rectifier could potentially be alleviated with 2 diodes in series or better circuitry. Better simulation methods could be explored to account for the of the propagation delay of the AND gate and counter components. To counteract the issues when switching to the 3200pF capacitance, parallel capacitors could potentially be used instead of a lumped capacitor. Finally, the physical auto-tuning system could be built and test. Also, the MCR-WPT PSCs with an alumina dielectric could also be constructed to verify the efficiency improvements.

5.2.2 Redesign Auto Tuning Circuitry to Account for PRU Movement Shifts

The auto-tuning circuit topology presented in this thesis only accounts for the initial placement of the PRU in the PTU charging Region. This means that if there are any shifts, movement, or repositioning of the PRU after the initial auto-tuning is complete, additional auto-tuning will not be done because the system is not recalibrated. There are two methods which can be explored to account for these PRU positioning shifts, which we describe below.

In the first method, the binary counter would be replaced with an up-down binary counter. Additional logic components such as a latch and XOR gate could be added to perform an if-else function to check if the peak has increased immediately after every tuning step. If the peak is not further increased (i.e. the maximum peak has been found), then it will decrement the counter reducing the tuning capacitance. The tuning capacitance will continually decrease until a peak is detected again. Therefore, if the maximum peak was already detected, the capacitance would alternate between increasing and decreasing the tuning capacitance, and if the PRU's position is shifted, the tuning capacitance would be continually increased or decreased until the maximum peak is achieved again.

The alternative method is to implement auto-tuning using a circuit in [66]. To do this, a MOS varactor prototype is required to replace the up-down counter. A pll charge pump and D flip-flop would replace the AND gate and if else circuitry in the previous method. The charge pump charging and discharging currents, and the size of the charge pump capacitor can be adjusted to tune the MOS varactor voltage up and down at the appropriate speed. This method operates in the same way as the discrete version above, but it has the added benefit to fine tune the peak detection.

5.2.3 Reposition Impedance Matching Auto-Tuning to the PTU.

The complete maximum peak detection and auto-tuning circuit configuration presented in

section 4.2 was located on the receiver side of the Rezence system. One problem with this is that the capacitors used for the capacitance tuning could be bulky. This is a major drawback for this system being in smartphones and other small electronic devices, which have very limited space.

To work around this problem, the complete maximum peak detection and auto-tuning circuit configuration should be broken up into two parts. The maximum peak detection circuitry which includes the negative voltage shifter, half wave rectifier, and comparator would be at the receiver, and the auto-tuning circuitry with the AND gate, binary counter, MOS switches and discrete capacitors are placed on the Transmitter. The 1:1 isolation transformer would no longer be needed, which saves additional space. With this configuration, the maximum peak detection would be done on the receiving coils as before. The comparator output pulse signal would then be sent to the counter input via the Rezence MCU units using Bluetooth 4.0 LE communication. Then the auto-tuning can be done on the transmitter side, with the discrete capacitors connected to the input node of the transmitter PSC.

Appendices

A. Passive Voltage Level Shifters

Voltage level shifters techniques are used to convert a bi-polar voltage signal to a positive or negative unipolar voltage signal or to generate a larger positive or negative DC voltage output from a lower AC source [70]. They are used in applications where suitable step-up or step-down transformers may not be available [71] [72].They are the initial part of the auto-tuning circuit proposed in section 4.2.1. In this section, we will go through the basic operation of a voltage doubler, and the negative voltage level shifter. Finally, we will summarize the design considerations.

A.1. Basic Operation and Considerations

From [70], the basic positive voltage level shifter circuit (also known as the Villard circuit) is shown in Figure 5.2-1(a). It is composed of 2 capacitors connected in series, and the cathode of a diode connected in between them at v_{clamp} and its anode connected to ground. To create the negative voltage level shifter, the diode is reversed. With a sinusoidal input voltage $v_{in}(t) = V_m\sin(2\pi Ft)$, the output DC offset voltage (V_{offset}) and peak signal (V_{clamp}) at $v_{clamp}(t)$ can be

calculated using capacitive voltage division as seen in *(A.1*)

$$v_{clamp}(t) = V_{clamp} \cdot \left(\frac{C_1}{C_1 + C_2}\right) \cdot \sin(2\pi f t) + V_{offset} \tag{A.1}$$

where

$$V_{clamp} = V_{offset} = V_m \cdot \left(\frac{C_1}{C_1 + C_2}\right) \tag{A.2}$$

As shown in (*A.2*), if we leave C_2 constant, when $C_1 \downarrow$, then $V_{offset}\downarrow$ and $V_{clamp}\downarrow$. And when $C_1 \uparrow$, then $V_{offset}\uparrow$ and $V_{clamp}\uparrow$. Therefore to get a signal loss 1% or less, we want $C_1 \geq 100C_2$.

In Figure 2.4-1 we have the circuit for a positive voltage doubler using ideal diodes, and a sinusoidal input $v_{in}(t)$. With the assumption that $C_1 >> C_2$ (or $C_1 \geq 100C_2$), the operation of this circuit is described in [73] and shown follows. "In the negative half cycle of v_{in}, C_1 is charged by v_{in}, and v_{clamp} is kept at 0V by D_1. When v_{in} passes its minimum at $t = t_1$, $v_{clamp} = v_{in} + v_{c1} > 0$, and D1 turns off. Since $v_{clamp} = v_{in} + v_{c1}$, with $v_{c1}(t_1^-) = V_m$, v_{clamp} rises to V_m and remains at V_m until the end of the negative half cycle ($t=t_2$). During $t_1<t\leq t_2$, D1 is off and v_{clamp} climbs to V_m. In the following positive cycle, of v_{in}, i.e. $t_2 < t \leq t_4$, since D1 is off, v_o will follow v_{in} with a voltage

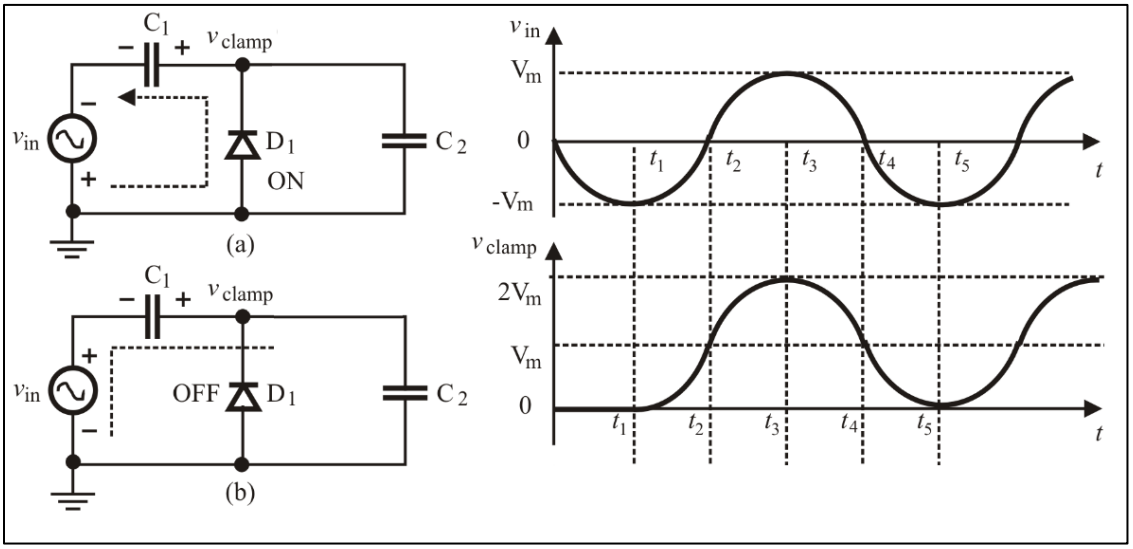


Figure 5.2-1 Positive voltage doubler with ideal diodes. The clamping node voltage v_0 is an up-shifted version of the input [73].

offset V_m. It is evident that v_{clamp} is the up-shifted version of v_{in}. The voltage clamper thus behaves as a voltage level shifter that shifts the median value of the input signal by V_m." Therefore voltage swing of the v_{clamp} node is $0 \leq v_{clamp} \leq 2V_m$. To create a negative voltage level shifter, the D1 diode should be reversed as shown in Figure 5.2-2.

There are other factors that affect the operation of the voltage level shifter. In real diodes, there is a forward voltage drop (V_f) across the diodes. When this voltage is taken into consideration, the voltage swing at v_{clamp} node becomes $-V_f \leq V_{clamp} \leq 2V_m - V_f$. Another factor to consider is the size of the C1 capacitor, as it determines the time it takes for the V_{offset} voltage at $v_{clamp}(t)$ to go from 0 to V_{offset}. As described earlier, when the signal is first applied to the input, C_1 is charged by v_{in} through on resistance in D1. Therefore, larger the capacitance, the larger time constant, and the longer the charging time. This is also known as the setup time.

A.2. Considerations Summary

The main consideration when designing the passive voltage shifter is to have C1 >> C2 (or $C1 \geq 100C2$). This ensures that negligible signal loss occurs at the output. Due to the V_f inherent

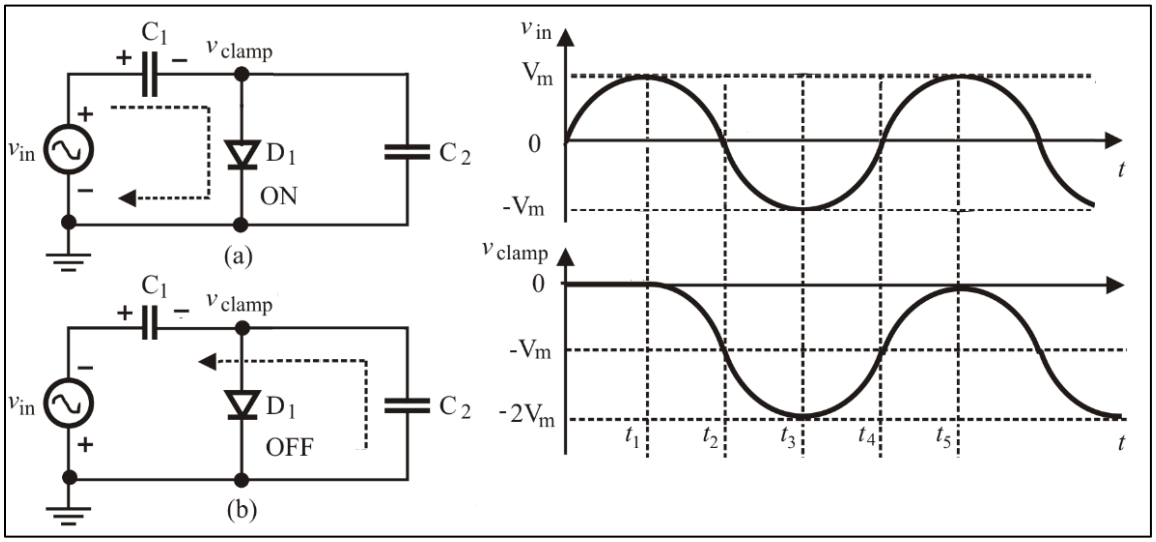


Figure 5.2-2 Negative voltage doubler ideal diodes. The clamping node voltage v_{clamp} is a downshifted version of the input [73].

in most diodes, the voltage swing at v_{clamp} node becomes $-V_f \leq V_{clamp} \leq 2V_m - V_f$. Finally, careful selection of C_1 needs to be considered if a short setup time is of concern.

B. Comparators

Comparators, unlike operational amplifiers, are designed to operate in the open loop configuration without negative feedback. They are optimized for higher speed (propagation delay), and their overall gain [74]. Because if this, they can be used in high-speed applications such as fast response overvoltage protection, and high-speed adaptive trigger circuits [75], peak detectors, high-speed differential circuits and fast A to D converters [76] to name a few. Another benefit of comparators is that they are design standard TTL or CMOS levels [77], eliminating the need for clamping or level shifting.

The comparator is the second part of the auto-tuning circuit proposed in section 4.2.1. In this section, we will go through the basic considerations when selecting a suitable comparator. Then we will summarize the design considerations at the end.

B.1. Comparator Considerations

When selecting a comparator for high-speed applications, the main parameters to be considered are classified as follows:

- Input offset voltage (V_{os} or V_{IO} depending on manufacturer)
- Hysteresis
- Input common mode voltage range (V_{ICM} or V_{CM})
- Propagation delay (t_{PD})

- Common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR)
- Input capacitance.

We go briefly through each parameter as describe their effects below:

B.1.1. Input Offset Voltage (V_{IO})

The input offset voltage (V_{IO}) is defined in [74] as the differential input voltage to apply in order to be at the toggling level. A graphical representation of $_{VIO}$ is shown in Figure 5.2-3. This value limits the resolution of the comparator. So to get a small input signal level, V_{IO} should be as small as possible. The downside of having a higher resolution would be increased concern of input noise that is comparable in size to V_{IO}, which could cause oscillations. Therefore the input should be filtered to reduce noise [77].

B.1.2. Hysteresis

When the input doesn't require fine grain resolution, hysteresis can be considered to reduce oscillations [77]. Many comparators have built-in hysteresis. In this case, the V_{IO} is computed as

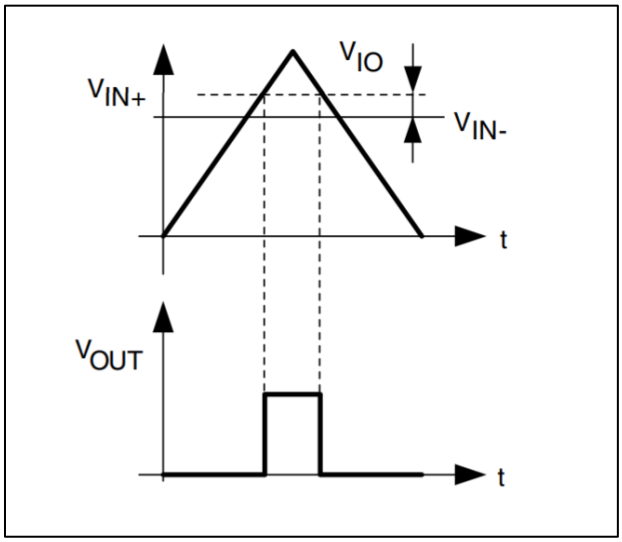


Figure 5.2-3 Input offset voltage V_{IO} [74].

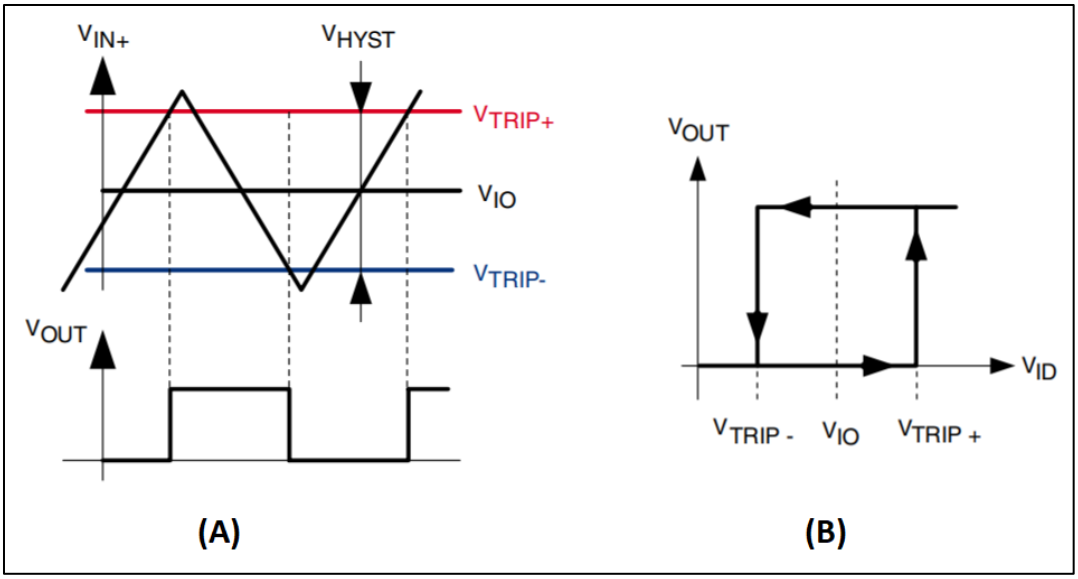


Figure 5.2-4 (a) Trip point voltage definition, (b) Input hysteresis [74].

the average of the lower (V_{TRIP-}) and upper (V_{TRIP+}) threshold voltages. The hysteresis (H_{HYST}) on the other hand is defined as the difference between V_{TRIP+} and V_{TRIP-}. These parameters are shown in Figure 5.2-4.

Hysteresis can also be implemented as an external circuit when the V_{IO} or built-in hysteresis values are insufficiently small. A few methods of implementation are described on pages 17 to 20 in [74], as well as on page 20 of [77].

B.1.3. Input Common Mode Voltage Range (V_{ICM})

The input common mode voltage range is the voltage range where both inputs must remain to guarantee device functionality [74]. When V_{ICM} range goes from V_{CC} to V_{CC+}, it is known as a rail-to-rail (R2R) comparator. When selecting between similar devices, if R2R is not required, then it always better to select one with V_{ICM} < R2R, which is cheaper and reduces power consumption.

B.1.4. Propagation Delay (t_{PD})

One of the main parameters used to determine the correct comparator in many applications

is the propagation delay. The reason for this is the t_{PD} limits the maximum frequency which can be processed. It is defined as the time difference between the moment the input signal crosses the threshold and the output stage changes. It is important to note that changes in other parameters such as load capacitance, temperature, source resistance and overdrive voltage, will cause t_{PD} increase thereby decreasing the maximum frequency that can be processed. Therefore these effects should be taken into consideration, to ensure that the desired operating frequency will always be less than the maximum frequency.

B.1.5. Other Parameters to Be Considered

Some of the other parameters that should be considered are the common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and the input capacitance. The CMRR is the relationship between V_{IO} and V_{ICM} [74]. It is defined in *(B.1)*

$$CMRR[dB] = 20 \cdot \log\left(\left|\frac{\Delta V_{ICM}}{\Delta V_{IO}}\right|\right) \tag{B.1}$$

The PSRR is the relationship between Power supply voltage and V_{IO} [74] and is defined in *(B.2)*

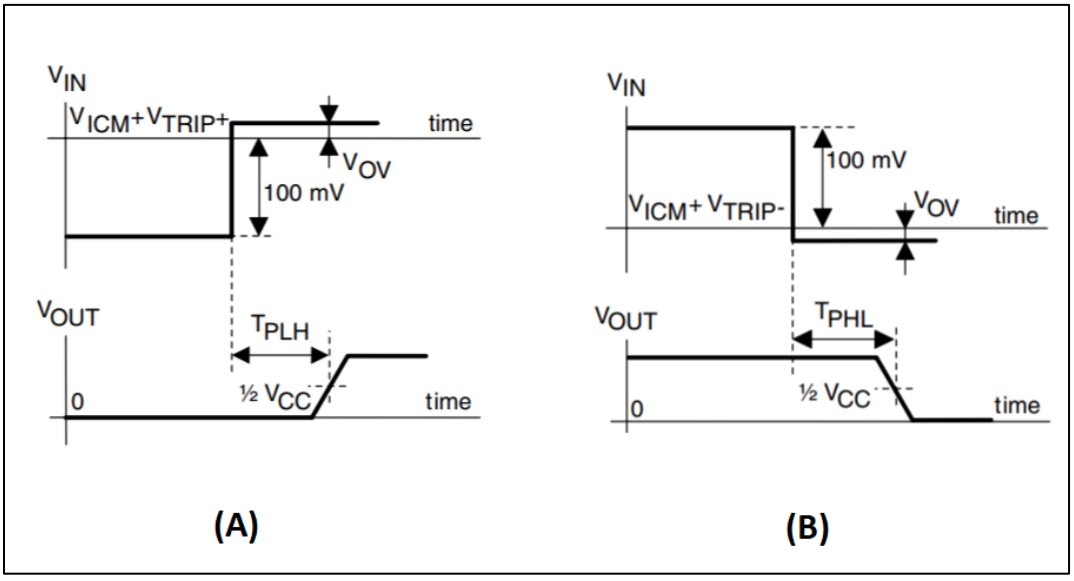


Figure 5.2-5 (A) Propagation delay from low to high (T_{PLH}), (B) Propagation delay from high to low (T_{PHL}).

$$PSRR[dB] = 20 \cdot \log\left(\left|\frac{\Delta V_{CC}}{\Delta V_{IO}}\right|\right) \quad \text{(B.2)}$$

Any changes in V_{ICM} or V_{CC} will cause changes in V_{IO}. Therefore the higher CMRR and PSRR the less the effect changes in V_{ICM} or V_{CC} will have on V_{IO}. Finally, input capacitance on the comparator should be very low for high-speed operation. This is so that the capacitance will have a minimal effect on the previous stage.

B.2. Comparator Considerations Summary

The t_{PD} of a comparator limits its maximum frequency operation. Changes in other parameters such as load capacitance, temperature, source resistance and overdrive voltage, will cause t_{PD} to increase and must be considered to ensure the fundamental frequency will always be within the devices operating frequency range. For cases where increased input resolution is key, V_{IO} has to be as small as possible. This will also make it more sensitive to noise, so noise filtering may need to be considered. Otherwise, when the input doesn't require fine grain resolution, hysteresis can be considered to reduce oscillations due to noise. It always better to select a comparator with the smallest V_{ICM} that the input signal can comfortably fit, to reduce cost and power consumption. Finally, CMRR and PSRR are measures of the effect that changes in V_{ICM} or V_{CC}, will cause changes in V_{IO}. Therefore the higher CMRR and PSRR the less the effect

C. Varactors

Varactors are analog voltage-dependent capacitors. Their simplicity and small size have made them an essential part of RF LC VCOs and they are also used on occasion to tune the resonant frequency of tuned amplifiers [78]. They are an essential part of the original auto-tuning circuit proposed in [66] and modified as described in section 4.2.1. In this section discuss three types of analog varactors, namely pn-junction varactors (known as the Vericap), regular MOSFETs used

as varactors, and accumulation mode MOS varactors. We go through the basic structure and theory, as well as their benefits, drawbacks, and their availability as discrete electronic components. Finally, we will summarize our findings.

C.1. PN-Junction Varactors (Vericap)

C.1.1. Basic Operation and Theory

All diodes exhibit variable capacitance when reversed biased [79]. This due to the nonlinear relationship between charge stored in the depletion region, and the reverse bias voltage resulting in a voltage controlled capacitance. The vericap exploits this variable capacitance effect by changing the doping concentration so that carrier concentration is made to change gradually from one side of the junction to the other [79], allowing for a larger voltage tuning range. The modeling equation for the junction capacitance from is written in (*C.1*), where C_{jo} is the zero bias

$$C_j = \frac{C_{jo}}{\left(1 + \frac{V_D}{V_0}\right)^m} \tag{C.1}$$

capacitance, V_D is the applied reverse voltage, V_0 is the built-in voltage potential (~0.7V-0.8V) and m is the grading coefficient. The m and C_{j0} values are generally not given in vericap datasheets. To obtain these values, two C_j values at two different V_D voltages are first taken from the datasheet or extracted from a typical C_j vs V_D graph like the one shown in Figure 5.2-6. These values are then plugged into *(C.1*) to create two equations with two unknowns which are easily solved.

When used in tuned circuits, vericaps have to be configured in the circuit so that it is always in reverse bias operation, and the reverse DC bias voltage should be isolated from the circuit. There are a couple of ways is to ensure reverse bias operation [80]. One way is to ground the cathode and the bias voltage applied to the anode. The bias circuitry is isolated from the RF using the C_B

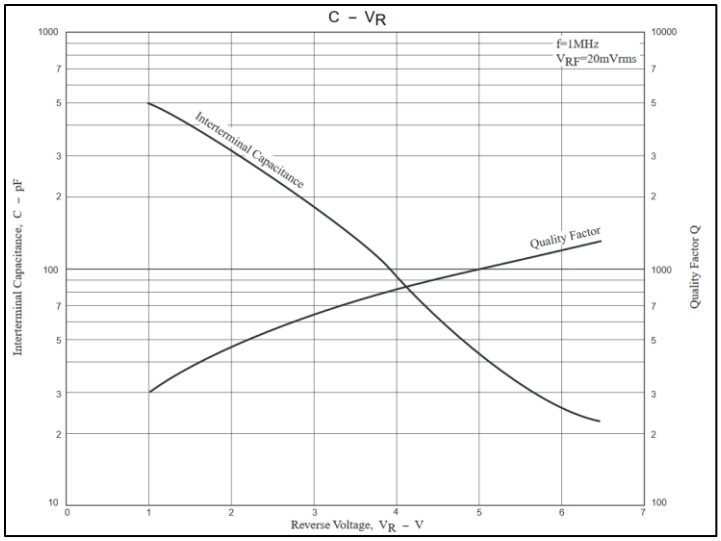


Figure 5.2-6 Capacitance and quality factor (Q) vs reverse voltage (V_D) graph for SVC383 vericap [81].

capacitor. The other method is to put the place them back-to-back. This has the benefit of symmetry at the cost of reduced capacitance due to having the vericaps in series.

C.1.2. Benefits, Drawbacks, and Availability

The main benefit of Vericaps is that they are small and inexpensive [82]. There are many discrete components with varying voltage and capacitor ranges available. They also have large maximum tuning capacitance range values up to 500nF as seen in [81].Their drawbacks are that

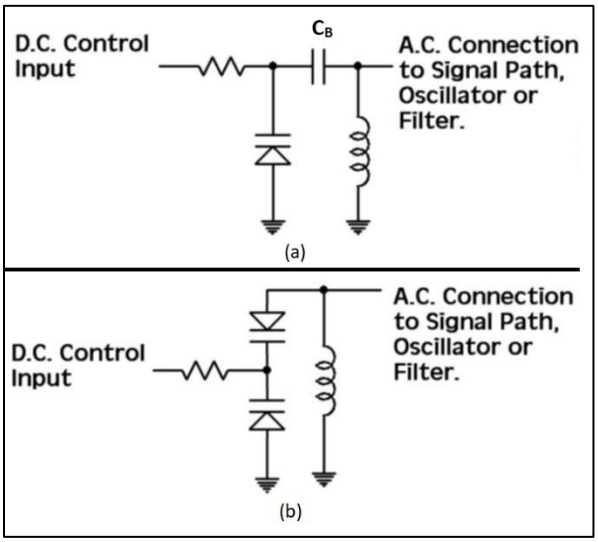


Figure 5.2-7 (a) single vericap configuration with DC blocking capacitor, (b) back-to-back vericap configuration.

they have a non-linear tuning range and are limited to reverse bias operation, which subsequently limits the voltage tuning range. The amplitude of the signal must also limited so that the vericap doesn't go into forward-bias [80].

C.2. Regular MOSFETs as varactors

Similar to their diode counterparts, regular MOSFETs show a voltage dependent gate capacitance [78]. When the MOSFET's drain and source are shorted as seen in Figure 5.2-8 (a) and a varying V_{GS} voltage is applied, the resulting C_{GS} graph is seen in Figure 5.2-8 (b). This non-monotonic behavior limits design flexibility, as the capacitance will change from increasing to decreasing with a constantly increasing voltage. Thus if used, it must be designed to operate in either the strong inversion or accumulation region exclusively. In discrete MOSFET datasheets, the C_{GS} is called C_{iss}, which from page 4 of [83] is defined in (*C.2*).When seeking a MOSFET to use as a varactor, it becomes apparent that all MOSFETs are designed to have a constant C_{iss} over a large input voltage range. This further reduces its use as a varactor in this configuration.

$$C_{iss} = C_{GS} + C_{GD} \tag{C.2}$$

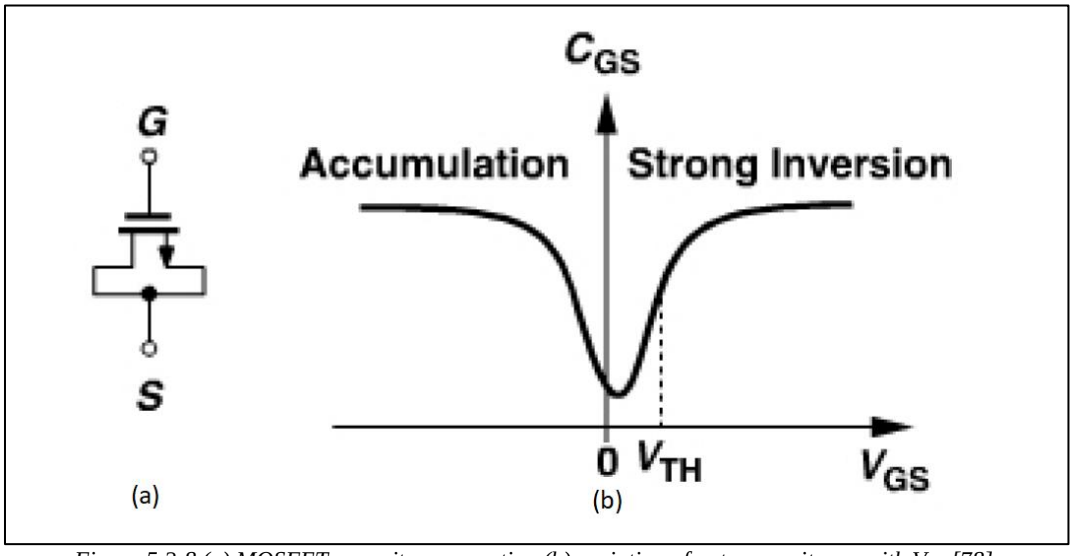


Figure 5.2-8 (a) MOSFET capacitor connection (b) variation of gate capacitance with V_{GS} [78].

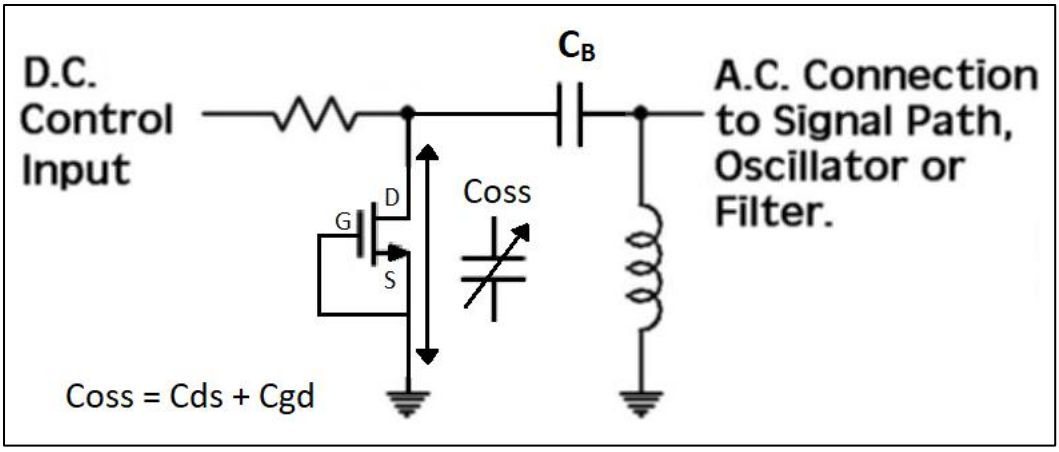


Figure 5.2-9 MOSFET used as a varactor where C_{oss} is varied with changing V_{DS}.

$$C_{oss} = C_{GD} + C_{DS} \tag{C.3}$$

Although the Ciss in most MOSFETs is designed to be constant with changing V_{GS}, output capacitance (C_{oss}) varies with changing V_{DS}. From [83], the C_{oss} is defined in (*C.3*). Knowing this, we can reconfigure the circuit as shown in Figure 5.2-9, to exploit the variability of C_{oss}.in the off region. Similar to Vericaps, the amplitude of the signal must be limited so that the MOSFET doesn't turn on. Finally, since MOSFETs aren't intended to be used in this configuration, the variability of C_{oss} due to changing V_{DS} is rarely included in the SPICE model netlist, and in many cases can't be simulated.

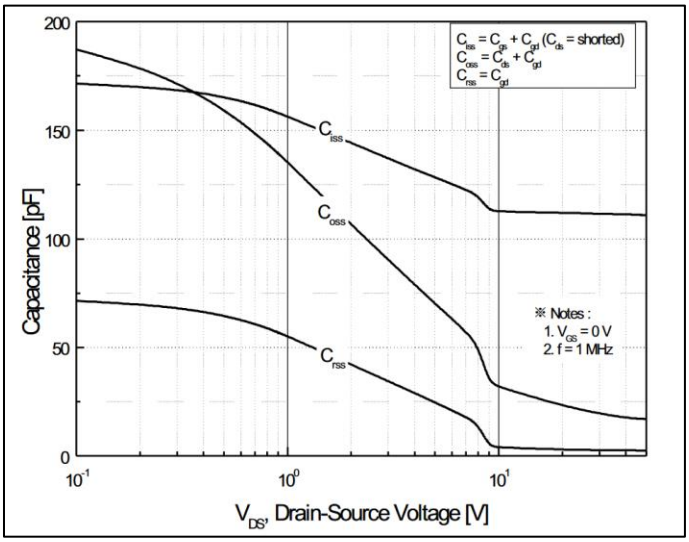


Figure 5.2-10 FQP1N50 capacitance vs V_{GS} graph [84]

C.3. Accumulation MOS Varactors

C.3.1. Basic Operation and Theory

An alternative to using regular MOSFETs as varactors is to use what is called an "accumulation-mode MOS varactor". This type of varactor is commonly designed and used in modern RF IC design. According to [78], this is an NMOS within an n-well, with the added benefit that applying a positive voltage will not cause strong inversion underneath the gate. Therefore the MOS varactor operates as follows. First, when $V_G < V_S$, then the MOS varactor operates in the depletion region where the electrons under the gate are repelled thereby causing a reduced capacitance. Alternatively, when $V_G > V_S$, the MOS varactor now forms an accumulation layer where electrons are attracted to the gate. The MOS varactor's structure, depletion region operation, accumulation mode operation, and the capacitance vs V_G graph are shown in Figure 5.2-11 (a), (b), (c) and (d) respectively.

$$C_{var}(V_{GS}) = \frac{C_{max} - C_{min}}{2} \tanh\left(a + \frac{V_{GS}}{V_0}\right) + \frac{C_{max} + C_{min}}{2} \cdot V_{GS} \qquad \text{(C.4)}$$

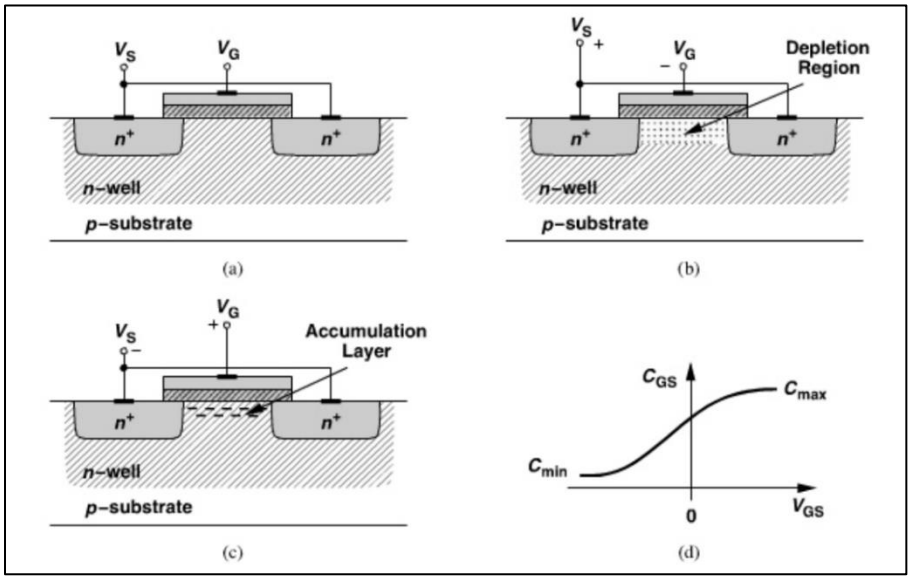


Figure 5.2-11 The MOS varactor: (a) its overall structure; (b) negative gate voltage operation; (c) positive gate voltage operation; (d) resulting C/V graph.

From in Figure 5.2-11 (d), the C/V characteristic curve of the MOS varactor goes from C_{min} when V_{GS} is negative, to C_{max} when V_{GS} is positive. To model this behavior, the hyperbolic tangent function can be used because it is a continuous function that has positive and negative saturation characteristics. The resulting equation is shown in (*C.4*), where a and V_0 are variables are used for intercept and slope adjustments, and C_{min} and C_{max} which include the overlap and fringe capacitances of the MOS varactor provide the minimum and maximum saturation capacitances. This model was then used to do ideal MOS varactor simulations within ADS, but since there are no discrete MOS varactor components were found for purchase, research and simulations were halted.

C.3.2. Benefits, Drawbacks, and Availability

This type of varactor has many benefits over its PN-junction and MOSFET counterparts. The major benefit is that it can tolerate both positive and negative bias voltages. Next is that they can operate in with low supply voltage, which has enabled them to be the device of choice in modern RF IC design. Unfortunately, there are no discrete accumulation MOS varactors anywhere for purchase, as only the vericaps could be found.

C.4. Varactors Summary

There are three types of varactors that were discussed in this section. They are the PN-junction diode varactor (Vericap), the MOSFET as a varactor, and the accumulation MOS varactor. The vericaps and MOSFETs are inexpensive and benefit from a wide variety of capacitance ranges to choose from. Their major drawback is that they must be carefully implemented within the design to ensure that they don’t go into forward-bias or turn on respectively. On the other hand, the accumulation MOS can tolerate both positive and negative

voltages. Unfortunately, there are no discrete electronic devices available

The original auto-tuning circuit described in [66] requires the use of an analog varactor as part of the maximum peak detection and auto-tuning system. Due to large voltage swings of maximum ±30V seen at the output of the receiver coils, it would not be possible to use vericaps or regular MOSFETs as varactors since these peaks will cause them to go into forward-bias or turn on respectively. The accumulation MOS varactor viable alternative that can operate with such large voltage swings, but unfortunately there are no discrete available components for purchase. Because of these issues, none of these devices are can be used within the circuit. An alternative discrete varactor circuit is described in the next section.

D. Discrete Charge Pump and Varactor using a Counter, MOS Switches, and Discrete Capacitors

As mentioned in section C.4 varactors are an essential part of the original maximum peak detection and auto-tuning system described in [66]. Unfortunately, none of those analog varactors can be used within our Rezence RWPT system prototype for reasons described in section C.4.

An alternative discrete varactor circuit is shown in Figure 5.2-12. It is made up of a high-speed binary-counter, MOS switches, and discrete capacitance values. It works as follows. For every rising edge on the clock, the binary-counter will be incremented. The least significant bit will switch between ground and the supply voltage (0V and 5V) at half the frequency of the clk signal, and each of the following bits would change between 0V and 5V at half the frequency of its prior bit. The 0V and 5V output of the counter then applied to the gate of its corresponding MOSFET

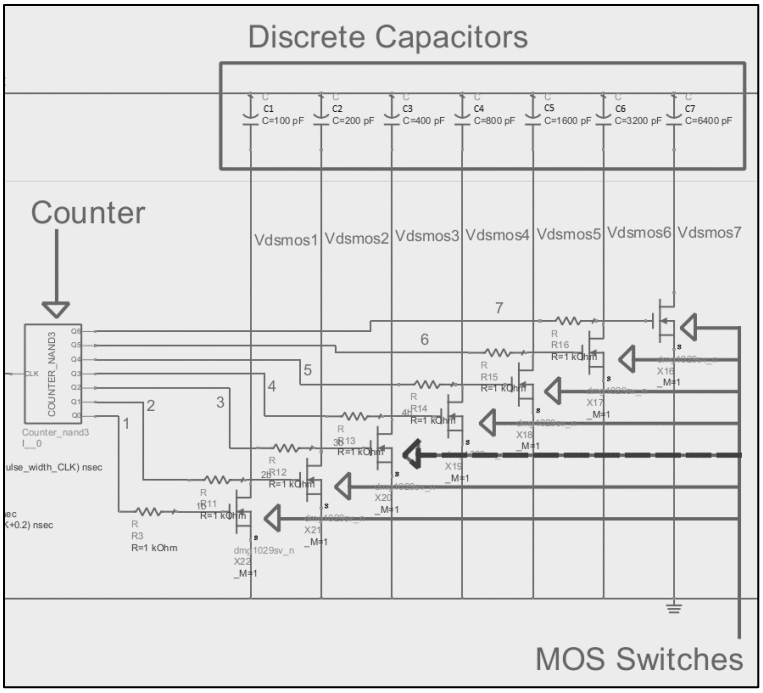


Figure 5.2-12 discrete MOS varactor.

turning it off and on, which in-turn connects and disconnects the capacitor to the circuit. Therefore, by using capacitors that double in value for every bit increase, we implement a discrete varactor.

The discrete varactor is the final part of the auto-tuning circuit proposed in section 4.2.1. In this section, we will go through the basic considerations when selecting a suitable counter and MOS switch. Then we will summarize the design considerations at the end.

D.1. Counters

Counters are sequential logic circuits that proceed through a well-defined sequence of states [85]. When selecting a high-speed counter, the main parameters to be considered are classified as follows:

- Maximum clock frequency (f_{max}), Propagation delay (t_{PD}), Setup and hold time (t_{su} and t_u)
- Input transition rise or fall rate ($\Delta t/\Delta v$)
- Logic Compatibility between devices and effects of different supply voltages (VCC).

We go briefly through each parameter as describe their effects below.

D.1.1. Maximum Clock Frequency (f_{max}), Propagation Delay (t_{PD}), Setup and Hold Time (tsu and tw)

The maximum clock frequency (f_{max}) is defined as the highest rate at which the clock of an integrated circuit can be driven while maintaining proper operation [86]. It is the primary factor determining the maximum operating frequency. Assuming the counter is enabled and the clock is the only input, f_{max} is directly related to the propagation delay (t_{PD}) as shown in equation (*D.1*). On the other hand, when multiple input signal events occur, the setup and hold times which are the time intervals between two signal events as described on pages 48-49 in [86] should be considered.

$$f_{max} \approx \frac{1}{t_{PD}} \tag{D.1}$$

D.1.2. Input transition rise or fall rate (Δt/Δv)

The Input transition rise and fall rate (Δt/Δv) is the rate of change of the input voltage waveform during logic state transition [86]. When input transition rates slower than the maximum recommended rate will cause large amounts of current to be drawn from Vcc to ground. This results is possible oscillations on the output or even device malfunction and is further described on page 31 of [86]. This should be taken into consideration to ensure that the output of the comparator is fast enough to switch the counter.

D.1.3. Logic Compatibility between Devices and Effects of Different Supply Voltages (VCC).

Many modern logic devices have multiple supply voltage (V_{CC}) levels for compatibility with older 5-V devices as well as newer low-power supply devices, such as the 3.3-V and the 2.5-V devices. The V_{CC} level of the device changes the operation of the device which affects all the

switching, timing, and electrical characteristics, as well as the recommended operating conditions. Care should be taken to ensure that parameters selected correspond to the correct V_{CC} level.

Some other factors that should be taken into consideration for inter-device compatibility are the high-level input and output voltages (V_{IH} and V_{OH}), and low-level input and output voltages (V_{IL} and V_{OL}). According to [86] on page 56, to ensure compatibility, "simply compare the V_{OH} min and V_{OL} max levels to the input threshold (V_{IH} min and V_{IL} max). If the output dc steady-state logic-high and logic-low voltage levels (V_{OH} and V_{OL}) are outside of the minimum V_{IH} and maximum V_{OL} range of an input port, then the ports are generally considered compatible". A visual representation of this criteria is shown in Figure 5.2-13. This has to be considered between the comparator and the comparator and the counter to ensure proper operation of the auto-tuning circuit. To a lesser extent, this is done as well between the counter and the MOS switch.

D.2. MOS Switches

When selecting a high-speed MOSFET to be used as a switch, the main parameters to be considered are classified as follows:

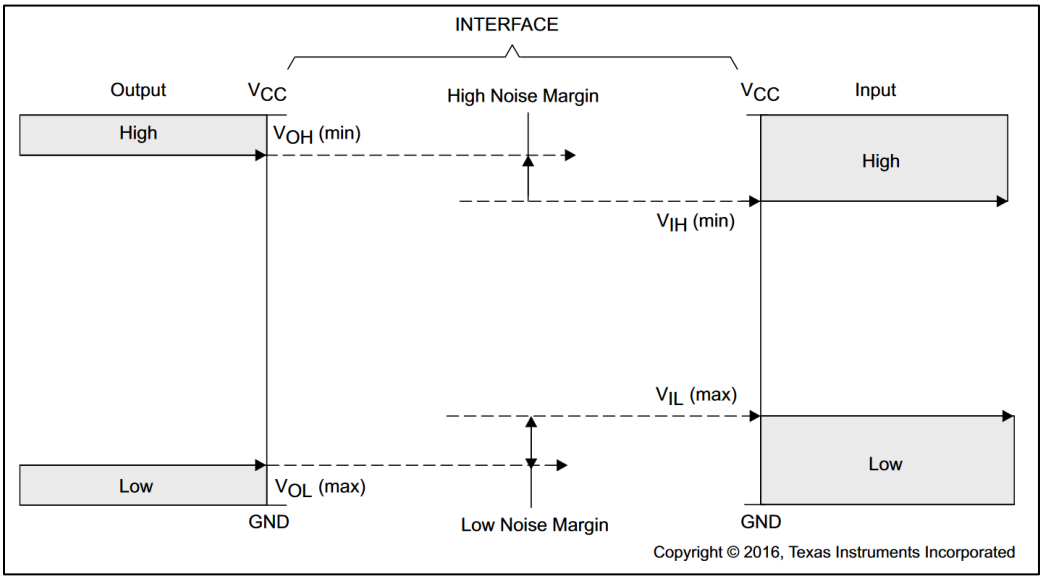


Figure 5.2-13 logic compatibility between I/Os [86]

- Drain-source breakdown voltage (BV_{DSS}), and Static drain-source on resistance ($R_{DS(ON)}$)
- Gate threshold voltage ($V_{GS(th)}$), Input Capacitance (C_{iss}), and Gate drain Charge (Q_g)

We go briefly through each parameter as describe their effects below:

D.2.1. Drain-Source Breakdown Voltage (BV_{DSS}), Static Drain-Source On-Resistance ($R_{DS(ON)}$)

At the output of the MOS switch, there are two main parameters of concern, the drain-source breakdown voltage (BV_{DSS}) and static drain-source on resistance ($R_{DS(ON)}$). The BV_{DSS} is the maximum voltage that the device is guaranteed to block between the drain and the source [87]. Therefore, for proper operation of the MOS switch, the peak voltage swing at the output of the receiver coils should be less than the BV_{DSS} so as to ensure device functionality. On the other hand, since power loss will occur through $R_{DS(ON)}$ when the MOS switch is on, it has to be taken into consideration. The smaller the resistance the better.

D.2.2. Gate Threshold Voltage ($V_{GS(th)}$), Input Capacitance (C_{iss}), Gate-Drain Charge (Q_g)

Since the input of the MOS switch directly connected to the output of the counter, the gate threshold voltage ($V_{GS(th)}$), input capacitance (C_{iss}), and gate-drain charge (Q_g) need to be taken into consideration for inter-device compatibility. To accomplish this, the following must happen. First, the $V_{GS(th)}$ should be between the V_{OH} min and V_{OL} max levels for proper switching. Also, the C_{iss} should be lower than the maximum output load capacitance of the counter to ensure proper counter operation. Finally, during the turn-on of the MOS switch, a current (i_G) flows to the gate charging the C_{iss} capacitance. Given that $Q_g = i_G \cdot t$, The Q_g should be as small as possible so as to minimize turn-on time and minimize the current required from the counter to turn on the MOS switch.

D.3. Summary

The discrete varactor is composed of a binary-counter, MOS switches and discrete shunt capacitors that double in size for every subsequent bit. The counter and MOS switch should operate at high-speed and be compatible with one another as well as the comparator.

To determine a suitable counter for the auto-tuning system, the primary parameter of concern is the speed of the clock signal (clk), which is determined by f_{max}. When the clk is the only input signal, f_{max} is directly related to t_{PD} as shown in (*D.1*). On the other, if multiple input signals occur at different inputs, the setup and hold time (tsu and tu) should also contribute to f_{max}. To ensure compatibility between the counter and the comparator (and to a lesser extent the counter and the MOS switch), the output dc steady-state logic-high and logic-low voltage levels (V_{OH} and V_{OL}) of the comparator should be outside of the minimum V_{IH} and maximum V_{OL} range of an input port of counter. The other parameter to consider is the minimum transition rise or fall rate ($\Delta t/\Delta v$). They should be taken into consideration to ensure that the output of the comparator is fast enough to switch the counter

To determine a suitable MOS switch, the following must be taken into consideration. At the output of the MOS switch, the drain-source breakdown voltage (BV_{DSS}) should be larger than the peak voltage swing at the output of the receiver coils. Also, the static drain-source on resistance ($R_{DS(ON)}$), should be as small as possible so as to minimize power loss through the resistor. At the input of the MOS switch, the gate threshold voltage ($V_{GS(th)}$) should be between the V_{OH} min and V_{OL} max levels for proper switching. The input capacitance (C_{iss}) should be less than the maximum load capacitance of the counter to ensure so as not to overload the counter. Finally, the gate-drain charge (Q_g) should be as small as possible so as to minimize turn-on time and minimize the current required from the counter to turn on the MOS switch.

E. Bridge Rectifier and Filter Capacitor Background Theory

This analysis of the ideal rectifier is done to give background theory of efficiency limit without a filter capacitor. Taken from [88], the circuit model for the RF Bridge Rectifier and the dc characteristic model of the Schottky Barrier Diode (SBD) is shown in Figure 5.2-14. From the circuit, the general equation for rectifier efficiency is

$$\eta = \frac{P_{in}}{P_{out}} = \frac{{I_{out}}^2 R_L}{{V_{in}}^2/(8R_o)} \tag{E.1}$$

After analysis of the circuit in [88], it is found to be

$$\eta = \frac{1}{\pi^2} \cdot \frac{8R_0R_L}{(n^2R_0 + 2R_s + R_L)^2} \left\{ 2n \cdot cos\theta_1 - \frac{2V_T}{V_{in}}(\pi - 2\theta_1) \right\}^2 \tag{E.2}$$

In the ideal circuit θ_1=0 and R_s=0, therefore (*E.2*) is simplified to

$$\eta = \frac{32}{\pi^2} \cdot \frac{R_0R_L}{(n^2R_0 + R_L)^2} \tag{E.3}$$

Since $\partial\eta/\partial R_L = 0$, then $R_L=n^2R_0$. Therefore the efficiency limit is

$$\eta = \frac{8}{\pi} \approx 0.811 = 81.11\% \tag{E.4}$$

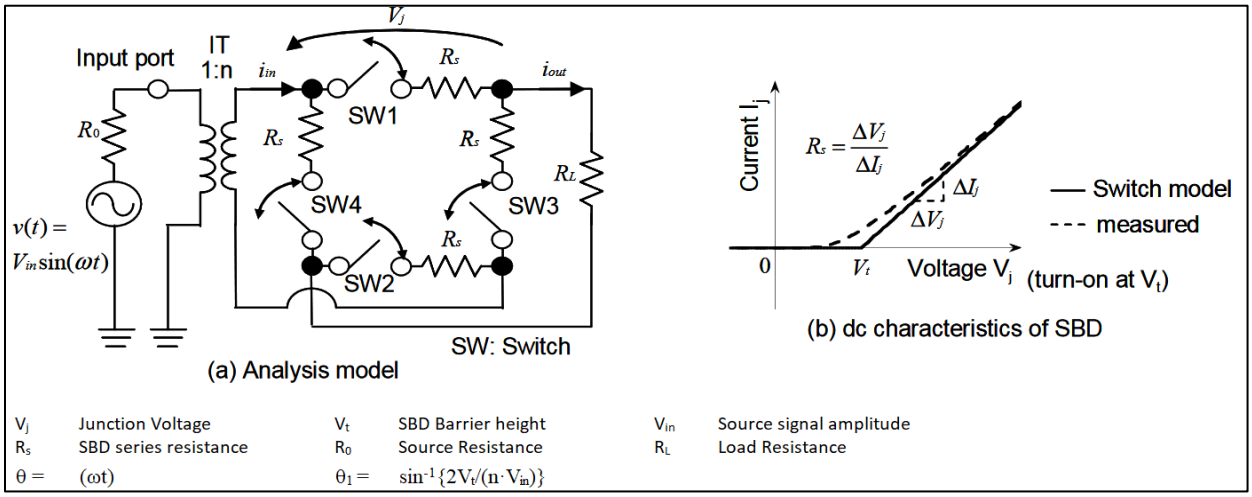


Figure 5.2-14: (a) RF bridge rectifier analysis model with impedance transformer; (b) DC characteristics of SBD for the

analysis.

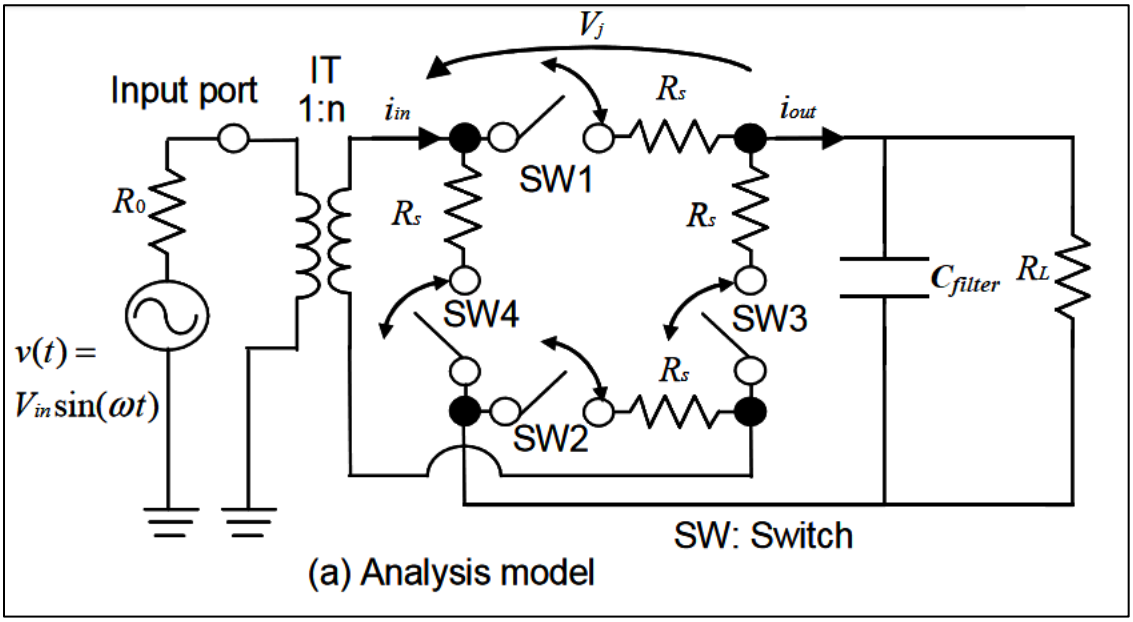


Figure 5.2-15 analysis model of the bridge RF rectifier with an impedance transformer and filter capacitor

From (*E.4*), we see that the bridge rectifier efficiency is less than 100%. The efficiency loss is due to ripple that is superimposed on the DC waveform. To counter this, a filter capacitor is added in parallel with the load resistor R_L, which is presented in Figure 5.2-15. As described in [89], when the diode conducts, this capacitor is being charged until the output voltage (V_o) equals the peak input voltage (V_p). The diode then shuts off, and the capacitor discharges current to R_L until $V_o=V_{in}$.

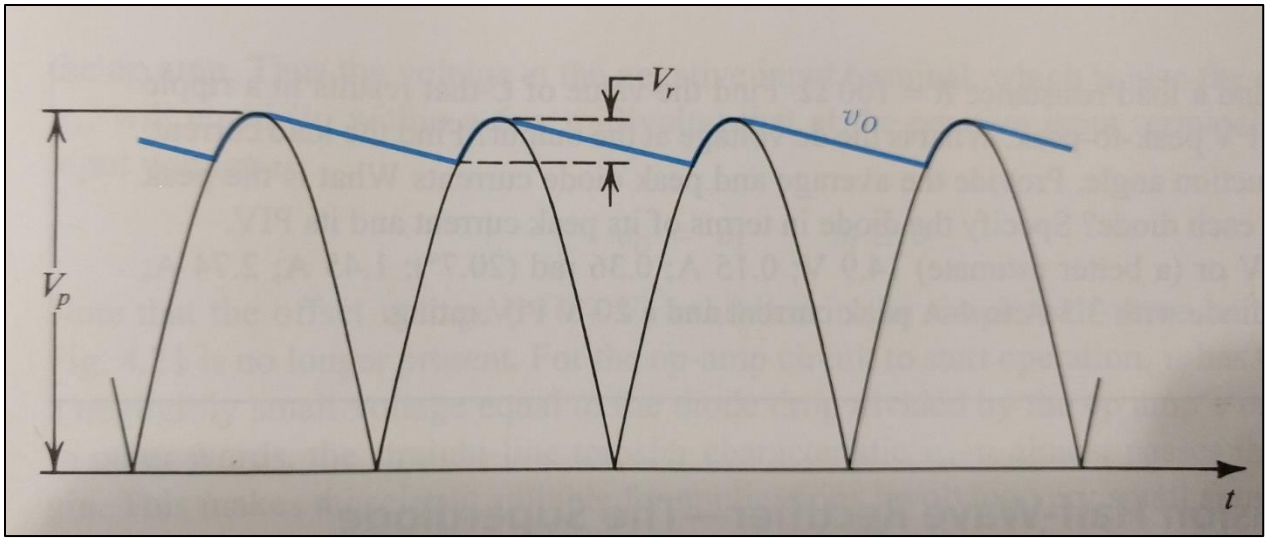


Figure 5.2-16 Waveforms in the full-wave peak rectifier.

Then the diode turns on and the capacitor charging again and repeats itself. This results in the rippled waveform V_o shown in Figure 5.2-16 below. The equation for the peak to peak ripple voltage (V_{ripple}) is then derived in [89] to be

$$V_{ripple} = \frac{V_p}{2fCR} \tag{E.5}$$

F. Insertion Loss/Gain

Insertion loss defined as the power loss resulting from the insertion of a device into an electrical system and is usually expressed in decibels (dB) [90]. The analysis is limited to 2-Port-Network. To get an understanding of Insertion Loss, we briefly go through how it is measured.

In Figure 5.2-17 we have a circuit composed of a voltage generator V_G with an impedance of Z_G connected to a load impedance Z_L, where the impedances aren't necessarily matched. The initial load voltage (V_{LA}) and current (Z_{LA}) are then measured. The two-port network is then inserted between the generator and load impedances as shown in Figure 5.2-18. The resulting load

voltage

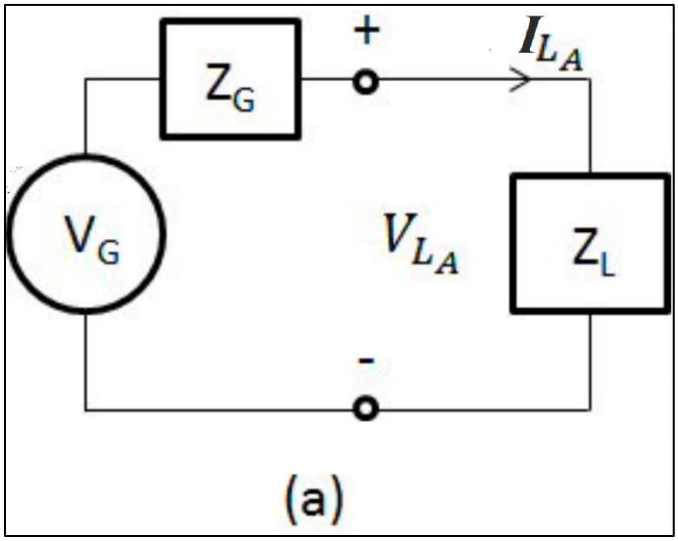


Figure 5.2-17 Testbench before the insertion of the two-port network.

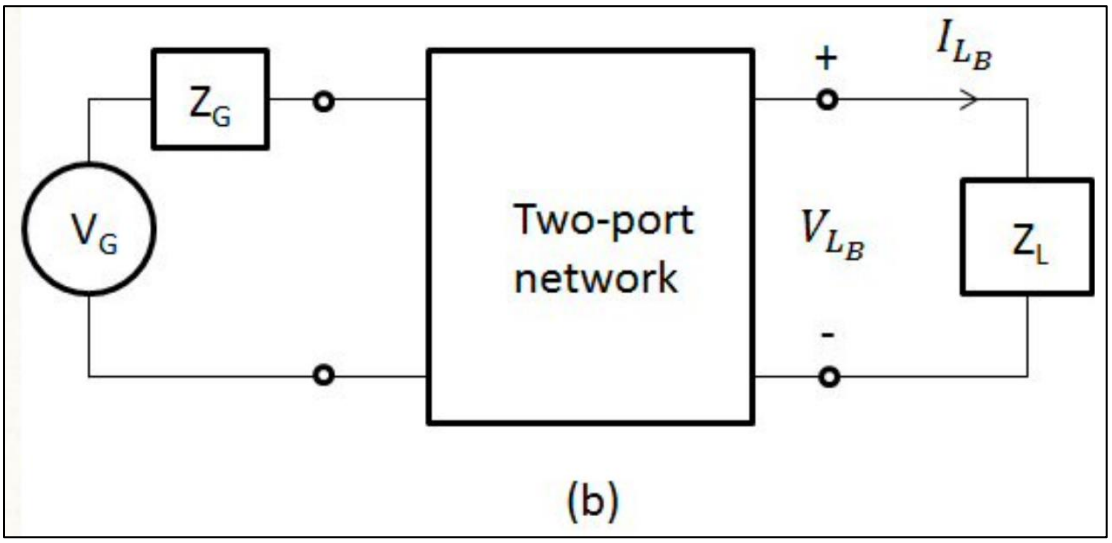


Figure 5.2-18 Testbench after two-port network insertion.

(V_{LB}) and current (Z_{LB}) are then measured. If the Two-Port Network is passive we use the following equation to calculate the insertion loss.

$$IL(dB) = -10\log_{10}\left(\frac{V_{LA}}{V_{LB}}\right)^2 = -20\log_{10}\left(\frac{V_{LA}}{V_{LB}}\right) \quad \text{(F.1)}$$

For an active network, we get the insertion gain, so we change the sign to positive.

When the generator and load impedances are matched, insertion loss is equal the negative

S12 and S21 S-Parameter values (i.e. IL(dB) = -S21(dB) = -S12(dB)) for a Two-Port passive network.

G. Useful Equations

Apparent Power

$$S = |\boldsymbol{S}| = \frac{{V_{RMS}}^2}{Z} \tag{G.1}$$

Equivalent parallel Impedance

$$Z_{eq} = \frac{z_1 z_2 \dots z_n}{z_1 + z_2 + \cdots + z_n} \tag{G.2}$$

High pass filter

$$f_c = \frac{1}{2\pi RC} \tag{G.3}$$

Percentage current through a node

$$I_x = \frac{V/Z_x}{V/Z_{eq}} = \frac{Z_{eq}}{Z_x} \tag{G.4}$$

Resonant frequency of an LC circuit

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{G.5}$$

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