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Optimization of a compact thermal model for a Ball Grid Array (BGA) package using experimental data

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OPTIMIZATION OF A COMPACT THERMAL MODEL FOR A BALL GRID ARRAY (BGA) PACKAGE USING EXPERIMENTAL DATA

By

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Abstract

Tayaz Fakhry
Optimization of a Compact Thermal Model
For a Ball Grid Array (BGA) Package Using Experimental Data

Master of Applied Science, Electrical and Computer Engineering
Ryerson University, Toronto, 2011

The goal of this research is to optimize a *static* & *dynamic* compact thermal model for a ball grid array (BGA) package using experimental data. The general objectives of thermal modeling are to increase the accuracy of electrical analysis to enhance the performance of the electronic systems. The project is focused on generating the static and dynamic compact thermal model of a Bipolar Junction Transistor (BJT) and a Ball Grid Array (BGA) based on experimental results of infrared (IR) camera system, so that the steady state and transient thermal behaviors of the package could be predicted fast with required accuracy. The approach proposed by a previous study based on generation of dynamic compact thermal model of a BGA package using simulation tools, is extended in this work to generate the static and dynamic compact model of the same package represented by a RC (thermal) network or admittance matrix based upon a methodology which couples different layers of experimental data to the error minimization notion of the problem. This optimization problem sets the temperature profile experimental data as a standard and compares the compact model's computed temperature and refines itself with a feedback, until reaching a desired point.

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I would like to thank my parents, my brother and sister, my girlfriend, my friends and whom I love with all my heart, for all their support and tolerance.

Last but not least, I thank God for whatever I am and have right now.

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CHAPTER 1

1.1 Introduction

More component density in electronic boards, more speed of VLSI circuits and unwillingly more power dissipation of fast electronic devices seem to be bundled together. Dramatic increase of applications of such circuits and devices, urges the *thermal analysis and power management* studies of such systems a vital design requirement. The amount of dissipated power by the chip is directly related to its temperature which is a crucial parameter in electrical behavior of electronic components, circuit performance, and reliability of the electronic system. Thermal analysis is an important part of modern electronic design thus that enables the designer to calculate the critical thermal variables as key factors in electrical analysis and accurate performance estimation. In general, there are three levels of thermal analysis: *component, package or system level*. Depending on the level of the design an electronic designer is engaged with, one of these analyzing levels must be chosen that gives out only the sufficient and relevant information about the thermal behavior of the subject of the thermal analysis [1-5].

In many cases of thermal analysis most of the information provided as the detailed model is unnecessary for the consumer because it includes the thermal characteristics of undesired locations. A smaller model that is capable of calculating only the hot spots, the temperatures and heat fluxes at some desired locations can help the designer to perform the thermal analysis much more easily and quickly with the required accuracy. Such model is called Compact Thermal Model (CTM). CTM can be generated from the detailed numerical model or the experimental data. This thesis focuses on generation of CTM at package level using experimental test.

The key to successful experimental test (for the purpose of thermal analysis) is the ability to obtain comprehensive and accurate prediction of temperature gradients influencing the quality of electronic products under near real-time operating conditions. However, the commonly used method of gathering these temperature gradients using thermocouples is limited by the large number of points to be monitored and the small size of the components being measured. Connecting tens to hundreds of thermocouples is very time consuming. In addition, thermocouples can act as heatsinks and conduct away heat, affecting the accuracy of measurements since the action of the heatsink may lower device temperatures.

Infrared (IR) thermal imaging system is a method which addresses the above-mentioned issues by providing comprehensive two-dimensional temperatures gradients of components under test [6,7], [46]. This is accomplished without the need to make contact with the components. Therefore, the thesis focuses on generation of CTM at package level using experimental testing data obtained from infrared thermal imaging system.

1.2 Literature Review

1.2.1 Thermal Analysis of Electronic Components

There are three levels of macroscopic thermal analysis and depending on the level of the design an electronic designer is engaged with, one of these analyzing levels must be chosen that gives out only the sufficient and not unnecessary information about the thermal behavior of the subject of the thermal analysis. These levels are as follows:

1.2.1.1 Component Level of Thermal Analysis

In component level a single component or some specific components of the electronic circuit are the subjects of thermal analysis. It's desirable for the designer to study the effect of thermal behavior of components on their own electrical behaviors and the mutual effects of the thermal behaviors of components on the electrical behaviors and operating points of their adjacent components. This level of analysis is usually used in electro-thermal analysis of the electronic circuit [6-9]. Electro-thermal analysis of the circuit is necessary, when there are some components which play key roles in the circuit

and it's very important for the designer to predict their electrical and thermal operating points in order to design a stable, predictable, and reliable circuit. Unlike ordinary electrical analysis by which the electrical operating point of the circuit is calculated for a fixed and predetermined temperature (usually room temperature), electro-thermal analysis performs both electrical and thermal analyses concurrently. It is well known that electrical current flowing through the materials causes heat dissipation and temperature elevation. This phenomenon is called Joule heating and in most cases changes the electrical operating point of the component and the circuit in which it is operating. Electrical analysis with fixed temperature thus is not sufficient for an accurate analysis and electro-thermal analysis should be performed so the mutual effects of temperature variation and electrical operating point variation are taken into consideration.

1.2.1.2 Package Level of Thermal Analysis

This level of thermal analysis is useful when the electronic designer needs to calculate the temperature profile and inward/outward heat fluxes of an electronic package working as a part of an electronic system. A package can be analyzed thermally using a simulation software or by its compact thermal model as explained later in this chapter and the rest of this work. Detailed analysis of package is expensive in terms of money and simulation time but it gives a relatively accurate temperature profile for every location inside or on the surface of package. Compact thermal model of package on the other hand is fast, almost free, and easy to use but it calculates the average temperature and heat flows for predetermined volumes inside or areas on the surface of the package with acceptable accuracy. The subject of this project is thermal analysis in package level and in future chapters detailed and compact modeling of electronic packages will be explained thoroughly.

1.2.1.3 System Level of Thermal Analysis

Accurate thermal analysis of a complex electronic system including several packages, discrete elements, printed circuit boards, connectors and mechanical parts, heat sinks and cooling mechanisms, and covering cases is almost impossible with currently available thermal simulation softwares, because of its complexity and the large number of thermal characteristics and the excessive amount of unnecessary information carried in the output of the analysis. The alternative solution is to separately, generate the compact model of packages, boards, and other parts of the system and use them as the building blocks of the thermal model of the system. This system level model is then used to generate the thermal variables at the desired locations within the system.

1.2.2 Detailed Thermal Analysis

The temperature profile (temperature at any desirable location of a solid object) and inward/outward heat flux from the surfaces of the solid object obey the heat transfer equation by conduction (this will be explained in Chapter 2 in more detail). However, if an object with a complex geometry such as a modern electronic package with several layers of materials is the subject of the thermal analysis problem, it's impossible to find an analytical solution for this equation.

One of the first alternatives to overcome this problem is employing experimental methods developed for generating the heat transfer equation with specified boundary and initial conditions and obtaining the temperature profile and outward/inward heat fluxes as they occur during the experiment. Some other ways, like numerical methods, do exist in the literature where each of these methods have their own privileges and drawbacks; numerical methods such as Boundary Elements Method (BEM), Finite Difference Method (FDM), and Finite Elements Method (FEM). Detail discussion and explanation on these methods are available in [12, 13] and other numerical analysis and heat transfer text books [14]. The first issue that rises immediately is the cost of analysis in terms of tools, time and accessibility. Unless the object has a very simple geometry, a high price software package such as ANSYS© [16] or COMSOL© [18] *Multi-physics* specially designed for numerical calculation of partial differential equations is needed to be

installed and made available on a powerful machine and the computation time is also considerably long. This makes the use of numerical method expensive and inefficient for the customer of the electronic package and makes the experimental method ideal for such a case; the second issue is the confidentiality of the electronic packages. Furthermore, to perform the detailed thermal analysis of an electronic package, exact information about the internal structure of the package, dimensions and physical properties such as thermal conductivities, thermal capacities, and densities of the different layers of the package are necessary in a simulation solution. Package producers, however, usually consider these specifications as classified information and don't publish them in the public domain. This makes the detailed thermal analysis hard for the package customer. The solution to overcome this situation is Compact Thermal Modeling (CTM) of packages using experimental data.

1.2.3 Compact Thermal Analysis

There are two types of CTM: static and dynamic. Static models are capable of calculating the thermal behavior and operating point under steady state conditions [10, 20]. Dynamic models on the other hand are more complex and capable of calculating the temperature profile and heat flows during transition times in which the temperature has not reached to its final value yet or the electrical and environmental conditions are not stable [19, 44, 45, 47]. A detailed description of CTM is presented in Chapter 2, Section 2.1.3.

1.3 Thesis Objective

The goal of this research is to develop an optimized c*ompact thermal model* of electronic package using experimental data. The objective of the compact thermal modeling process is to create a simplified model that represents the thermal behavior of the package to perform a quick thermal analysis with the required accuracy in system design process. This research project aims to create methodology to enable *rapid, precise* and *inexpensive* assessment of thermal behavior of packages in electronic equipment

under real-time experimental testing. This methodology is applied to predict the thermal behavior of the Ball Grid Array (BGA) package.

The Static and dynamic compact thermal model generation methodology based on experimental test data and the resistor/capacitor (RC) network approach for a typical BGA package is discussed. A feasibility study was performed to verify the proposed approach of the CTM development based on thermal measurement data. The CTM is generated and optimized by MATLAB for different work-loads for an FPGA with a PBGA-H technology.

1.4 Thesis Outline

In this research we attempt to provide coverage of a methodology based on experimental test data via infrared camera system required for optimization of static & dynamic compact thermal modeling of an electronic package.

In Chapter 2, the fundamental building blocks to generate a compact thermal model of a Ball Grid Array (BGA) technology and packages were introduced. Heat conduction mechanism was discussed. The infrared (IR) thermography measurement setup and major equipments used in the experiment setup were also presented.

Chapter 3 is allocated to various proposed software blocks used in the research which have an important role on progressing these steps. A variety of experimental, code-based, object-oriented or text-based software were applied and processed sequentially or concurrently to obtain static and dynamic CTM.

Chapter 4 concentrates on the feasibility study to generate the compact thermal model for a BJT device using infrared camera system.

In Chapter 5 a methodology to generate the static & dynamic compact thermal model based on the resistor and capacitor network for a typical BGA package using experimental data are reported.

The conclusion and suggested future works are summarized in Chapter 6.

CHAPTER 2

Basics of BGA Compact Thermal Modeling

2.1 Introdution

In this chapter, different *BGA packages* and their manufacturing technology are described. Then, *Governing Heat Transfer Equations* which are the founding infrastructure of the thermal analysis dynamics are stipulated. In addition, CTM for a BGA Package is introduced. Finally, *infrared (IR) camera's application in thermal analysis of electronic package is illustrated*.

2.1.1 BGA Packages

There are many types of electronic packages which are divided into several categories based on the material used for fabrication, the method they are mounted on the PCB, pin arrangements, and other characteristics. For example, materials used in packages can be plastic, ceramic, or epoxy. The mounting methods include insertion, surface, chip carrier, socket, and ball grid array (BGA). Before moving to a thorough explanation about BGA packaging technology some of the other types of packages which are popular and produced by manufacturers are introduced in the following section.

Dual Inline Parallel (DIP) package which is also called DIL is a rectangular shape package with two parallel rows of electrical connecting pins coming out of the two sides of the package. Material used in this type of packages is either plastic or ceramic. The method of connecting DIP package to the PCB is insertion. It means the metal pins of DIP are inserted from one side of the PCB to the holes already drilled in the board and soldered on the other side of the board. Some of the characteristics of DIP are as follows:

- Lead Pitch (Pin spacing): 2.54 mm or 0.1" and 1.778 mm (0.07").
- Row spacing (the distance between the rows): 7.62 mm (0.3") and 15.24 mm (0.6").
- Pin counts (number of electrical pins): 8, 14, 16, 18, 20, 22, 24, and 28 for 0.3" row spacing and 24, 28, 32, 36, 40, 48, and 52 for 0.6" row spacing.

A typical 18 pins, 0.3" row spacing plastic DIP package [27] is shown in Figure 2.1.

Figure 2.1: Dual Inline Parallel (DIP) Package.

Small Outline Integrated Circuit (SOIC), **Plastic Leaded Chip Carrier (PLCC)**, **Quad Flat Pack (QFP)**, **Pin Grid Array (PGA)** are samples of other types of traditional popular electronic packages [27-29].

The Ball Grid Array or BGA is an advanced packaging technology, which has descended from PGA. Like PGA packages one side of the BGA is fully or partially covered by electrical pins and the other side is exposed to the free or forced convection or in contact with the heat sink. Unlike other types of packages in BGA technology electrical connections between the chip and PCB are established via solder balls instead of metal pins. The process of mounting the BGA package on the PCB involves three steps:

1- BGA is precisely placed and aligned on top of the PCB so the balls are in contact with PCB pads.

2- The contact location is then heated usually by infrared heater so the solder balls start melting.

3- The last step is cooling down so the solder starts to solidify. This process of mounting is considerably more complex than what is needed for other types of packaging.

There are, however, some key advantages that make this technology desirable for microelectronic designers. These advantages are:

1- High connection density: in order to connect other types of package to the PCB, pins must be soldered. This will restrict the proximity of the pins so the danger of unwanted bridging between two adjacent pins is reduced. BGA, however, does not have this problem so the number of pins can be increased up to 1152 leads when the lead pitch is 1.0 mm.

2- Increased heat conduction: the thermal resistance between the BGA package and PCB lower than other packages. The operating temperature is, therefore, lower.

3- Low inductance of connections: the small size of leads in BGA technology compared to the metal pins reduces electrical inductance, switching noise and other distortions.

4- Higher reliability: the short length of balls compared to the pins reduces the danger of failures caused by mechanical tensions and vibrations.

There are several variants of BGA packages and some of them are as follows: **Fine Ball Grid Array (FBGA), Ceramic Ball Grid Array (CBGA), Plastic Ball Grid Array (PBGA), Plastic Ball Grid Array - Heat Spreader (PBGA-H), Plastic Ball Grid Array - Multi Die (PBGA-MD), Enhanced Ball Grid Array (EBGA), Tape Ball Grid Array Package (TBGA).**

Figure 2.2 illustrates two different BGA packages [30]. More information on the technology, material properties, and specification of BGA packages may be found in [22, 31].

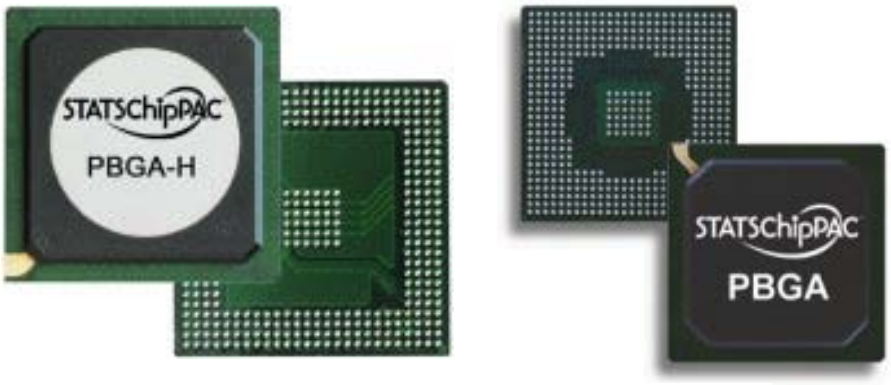


Figure 2.2: PBGA-h and PBGA Ball Grid Arrays.

In this work the single chip PBGA-h package proposed in [1] has been selected as a case study of Compact Thermal Model (CTM) generation process in order to be consistent with the literature review study. More information can be reviewed in the datasheet of this package [21, 25].

This package has several layers as follows:

- Leads or balls that establish the electrical connections between the PCB and the electronic circuit inside the package. This layer includes inner balls which will be called LEAD1 later in this work and outer balls which will be LEAD2.
- Air is the empty space between inner and outer balls.
- Substrate 1 which is located on top of the inner balls.
- Substrate 2 which is located on top of the air layer.
- Substrate 3 which is located on top of the outer layer.
- Substrate top layer which is located on top of the substrate 1, 2, and 3 layers.
- Die attach is located on top of the substrate top layer and align with the substrate 1 and inner balls layers.

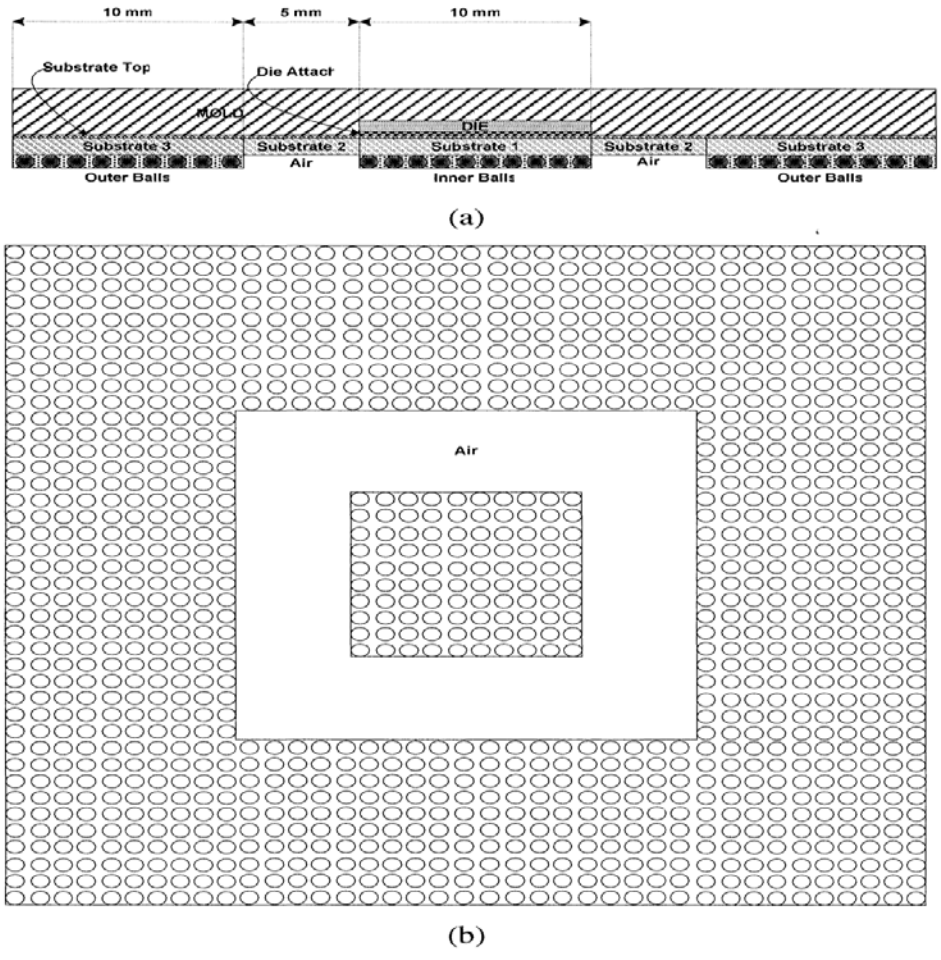


Figure 2.3: PBGA-h Layout in the Literature Research (a) Cross Section (b) Bottom View.

- Die which is the silicon chip on which the electronic circuit is built and which is located on top of the die attach layer.
- Mold which is the covering material located on top and around the die and encapsulates it for protection.

These layers have been illustrated in figure 2.3 (a) which is a cross section view of the BGA package. Figure 2.3 (b) illustrate the bottom view of the package.

Figure 2.4 shows these mentioned layers. The area of different nodes considered in the layout due to different surfaces (and different heat flux and properties) as listed in table 2.1 in the BGA simulation with the finite element software of COMSOL for the literature review and also this study whenever they are needed.

Node		Area m^2
Top 1 (inner top)	T1	4.12036E-5
Top 2 (outer top)	T2	3.58796E-4
Lead 1 (inner leads)	L1	2.5E-5
Lead 2 (outer leads)	L2	3E-4
Bottom	B	7.5E-5
Side	S	6.6E-5
Junction J (Volume)		5E-10 m^3

Table 2.1: Different Nodes in the Layout and Their Surface Areas.

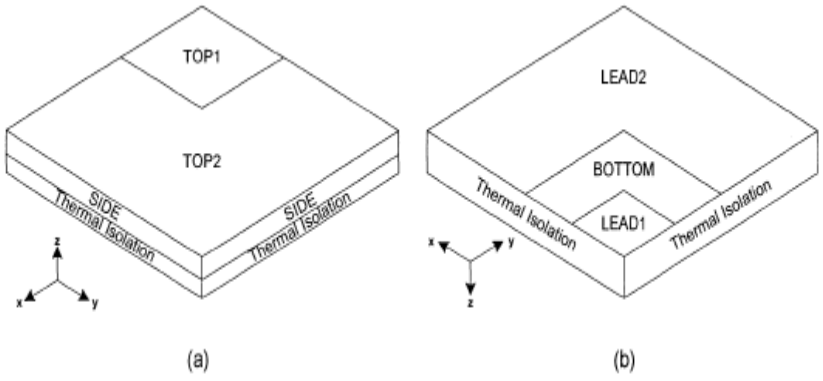


Figure 2.4: (a) Top1, Top2, Side areas, (b) Lead1, Lead2, Bottom areas.

2.1.2 Governing Heat Transfer Equations

Heat transfer mechanisms are *Conduction, Convection, and Radiation* [14, 23]. For most electronic component, heat conduction is the most important heat transfer phenomenon; therefore most researchers consider a component that has thermal conduction as its only mode of internal heat transfer. Therefore, heat conduction equation described by equation (2.1) will be used for thermal modeling of electronic component in this research work.

$$q_g + \nabla \cdot (k \nabla T) = \rho \cdot C \cdot \frac{\partial T}{\partial t} \tag{2.1}$$

where:
C *(J/K)* is the specific heat capacity of solid material, and
p (Kg/m3) is the density of material, and
q *(J)* is the heat energy generated inside a solid, and
T (*K*) is the temperature of the solid, and
, is the vector of divergence operator.

$\nabla = \frac{\partial}{\partial x}\vec{i} + \frac{\partial}{\partial y}\vec{j} + \frac{\partial}{\partial z}\vec{k}$ For a homogeneous and isotropic solid material where thermal conductivity is a scalar parameter independent of direction and location, equation (2.2) is simplified as follows:

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{q_g}{k} = \frac{1}{\alpha}\frac{\partial T}{\partial t} \tag{2.2}$$

where:

$\alpha = \frac{k}{C \cdot \rho}$, is thermal diffusivity of the solid material.

Numerical methods such as finite element method and finite difference method can be applied to various kinds of heat conduction problems (e.g. isotropic, non-isotropic, linear, non-linear, homogeneous, and non-homogeneous) for thermal analysis of electronic system. Nevertheless using such numerical methods might be time-consuming and could be replaced by experimental results for gaining the boundary conditions temperatures of a device under test.

2.1.3 Compact Thermal Modeling

The temperature profile (temperature at any desirable location of a solid object) and inward/outward heat flux from the surfaces of the solid object obey the heat transfer equation by conduction as stipulated. Nevertheless, if an object with a complex geometry such as a modern electronic package with several layers of materials is the subject of the thermal analysis problem, it's hard to find an analytical solution for this equation.

Employing numerical methods developed for solving the heat transfer equation with specified boundary and initial conditions is a sophisticated solution which exists in order to obtain the temperature profile and outward/inward heat fluxes. However, another solution is using experimental case studies for different workloads which could be more practical for a different set of applications, especially when time and computations are in higher priorities than abstract and precise, yet time-unbounded methods. The idea of generating a compact thermal model stems from such a preference. In fact, this method enables elimination of the redundant or extra data in all nodes except one (the junction is set for this node in this work.) The full-detailed thermal profile is tracked in junction node to get proper and valuable data from only one point in the board; knowing that the other nodes have logical thermal restrictions and a relationship with the tracking node.

The numerical simulation approach may be expensive and inefficient for the customer of the electronic package. Another issue is the confidentiality of the electronic packages which guides the researchers to new solutions [1]. In order to perform the detailed thermal analysis of an electronic package with simulation-based software such as COMSOL, exact information about the internal structure of the package, dimensions and physical properties such as thermal conductivities, thermal capacities, and densities of the different layers of the package is necessary. Package producers however usually consider these specifications as classified information and do not publish them in the public domain. The solution to overcome this situation is *Compact Thermal Modeling* (CTM) of packages. Nevertheless in this work generating such CTMs are examined regardless of, or with the least amount of knowledge from inside the packages using experimental techniques such as Infrared (IR) camera system.

A smaller or *compact model* that is capable of calculating only the hot spots, the temperatures and heat fluxes at some desired locations can help the designer to perform the thermal analysis much more easily and quickly, and with the required accuracy.

2.1.3.1 DELPHI compact thermal model

There are several methods of compact model generation; however for steady state compact modeling purpose there is one dominant approach proposed by DELPHI consortium (a collaborative European project) which is based on resistor network. The main goal of this project which involved six end-user electronic equipment companies from five European states was to propose a methodology to generate compact thermal models for electronic packages [15]. The DELPHI consortium members were Thomson CSF, Philips CFT, Alcatel Bell, Alcatel Space, Flomerics, and the National Microelectronics Research Centre in Ireland. The first four companies which were the industrial partners of project are well known producers of electronic equipment in the area of civil and military radar, lighting and consumer electronics, telecommunications equipments, and satellite electronics. The fifth partner of project Flomerics is a developer of a thermal CAD tool used in the electronic industry.

The DELPHI procedure of generating static (steady state) compact thermal model has several steps as following:

1- A detailed thermal model of the package is generated by a thermal CAD tool.

2- Using the thermal CAD tool, thermal simulations are performed on package for a set of boundary conditions proposed by DELPHI consortium and average temperatures and heat fluxes of desired locations (thermal nodes that correspond to the volumes and areas inside or on the surfaces of package) are obtained.

3- A network is postulated. This network consists of several resistors that connect the thermal nodes to each other.

4- The values of resistors are then calculated using the detailed model results.

2.1.3.2 Static compact model definition

Following the DELPHI methodology, the thermal characteristics of the package can be modeled by a resistor network as mentioned earlier. Using node analysis method, the general formula relating the voltages (temperatures) and currents (heat fluxes) of the electric network can be expressed as:

$$q_i = \sum_{k=0}^{N} Y_{ik} T_k \tag{2.3}$$

where:

Y is the conductance matrix,

N is the number of nodes,

qi (Watts) is the heat flux leaving the node i,

and Ti (Volt) is the voltage of node i.

If the package is considered a linear thermal system (i.e. the thermal conductance and other physical properties of the package are temperature independent), it can be modeled by a linear system such as equation (2.3) and matrix Y. This can represent the static compact thermal model of the package. The higher value of N, the higher accuracy will be achieved by this modeling. Note that each node in equation (2.3) represents a specified area or volume within or on the surfaces of the package such as junction region, side walls, top surface, leads… Node voltages calculated by the equation (2.3) are equal to the average temperature of their corresponding volume or area

2.1.4 Infrared (IR) Camera in Thermal Analysis of Electronic Packages

A recent infrared thermography setup for thermal analysis of electronic packages was proposed by [2] in 2009. The measurement setup is used to perform two types of analysis a) steady state analysis, b) transient analysis. In steady state analysis, after switching the power ON, a time interval is given to the system to reach its steady state condition. This is due to the fact that oil based heat-sink takes some period of time to completely cover the whole surface of the device under test (DUT) and remove the heat homogenously. To perform transient analysis on the DUT, an abnormal stress is imposed to a system in the form of different load work conditions.

The major apparatus used in the proposed experimental setup include an FLIR infrared camera system, data acquisition system, digital thermometer, infrared transparent oil (Aldrich oil), oil pump and power supply. A typical measurement setup is shown in figure 2.5. The measurement setup is capable of capturing up to 420 frames per second (fps) with a 10μm ×10μm spatial resolution, and it can be applied to multiple chips with relative simplicity. The IR camera frame rate can be increased up to 10 KHz as long as the bandwidth of the camera stays under 1GB/s. The equipment and instrumentation used to conduct the experimental measurement are discussed in this chapter.

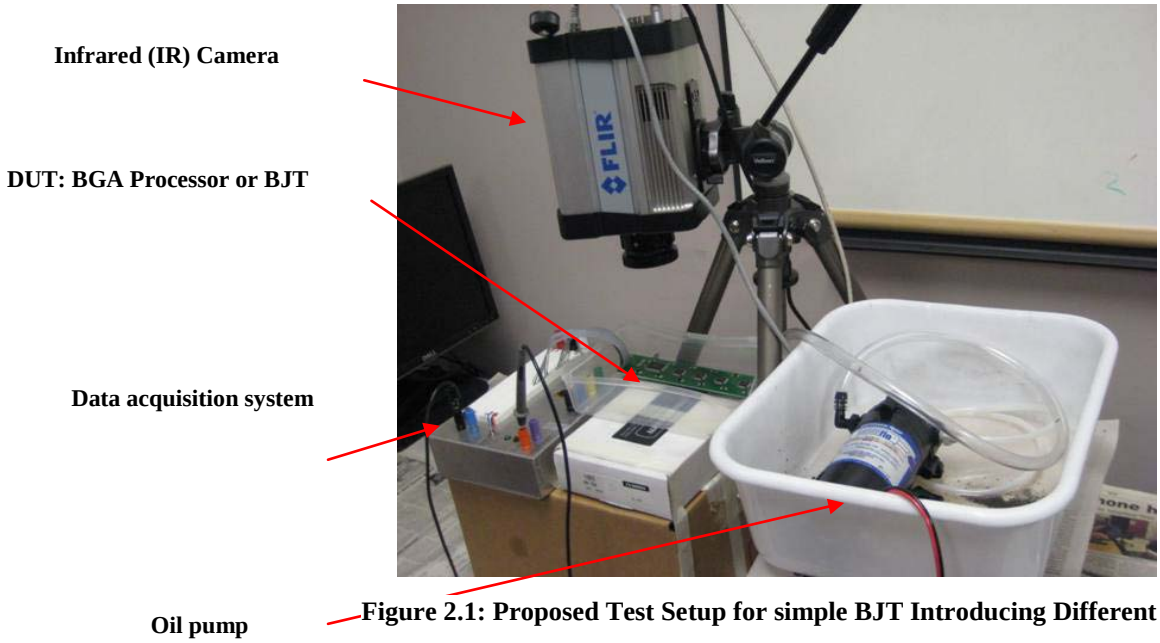


Figure 2.1: Proposed Test Setup for simple BJT Introducing Different Equipment.

2.1.4.1 Infrared Camera

The infrared camera used in this measuring setup is a FLIR SC4000 camera (Fig. 2.6) which is a high-speed, high-resolution, high sensitivity, science-grade infrared camera with Gigabit Ethernet, Camera Link and USB interfaces for maximum flexibility and performance. With a 320 × 256 pixel Indium Antimonide (InSb) detector, the ThermoVision SC4000 camera offers unmatched resolution and thermal sensitivity. An extremely sensitive detector and high speed read out design, provide the camera with extraordinary image quality for the most demanding applications.

Figure 2.6: Infrared (IR) Camera SC4000.

The Thermo Vision SC4000 outputs 14-bit digital data at rates up to 50 Mega pixels per second, yielding 420Hz frame rates for 320 × 256 pixel imagery. For high speed applications and increased frame rates the ThermoVision SC4000 supports windowed readout modes, allowing a subset of the total image to be selectively read out with user-adjustable window size at a much higher frame rate. The sub-sample window sizes and locations can be arbitrarily chosen and are easily defined using the camera control software [24].

2.1.4.2 Data Acquisition System

The data was captured and analyzed using the integrated data acquisition system of the optical system, supported by PC-based ThermaCAM Researcher software for data acquisition, analysis and reporting. ThermaCAM Researcher software contains powerful measurement and analysis functions for extensive temperature analysis, including

isotherms, line profiles, area histograms and image subtraction capability. The acquired input data were recorded in real time for subsequent analysis using this software package. Additionally, the SC4000 camera system has an optional Software Development Kit (SDK) for custom programming and interfacing to the camera which is introduced in detail in Chapter 3.

2.1.4.3 Heat-sink

A heat-sink is a medium that enhances heat dissipation from a hot surface, usually the case of a heat generating component, to a cooler ambient, usually air. In most situations, heat transfers across the interface between the solid surface and the coolant air and the solid-air interface represents the greatest barrier for heat dissipation. A heat-sink lowers this barrier mainly by increasing the surface area that is in direct contact with the coolant. This allows more heat to be dissipated and/or lowers the device operating temperature.

The primary purpose of a heat-sink is to maintain the device temperature below the maximum allowable temperature specified by the device manufacturer [19]. Using temperatures and the rate of heat dissipation, a quantitative measure of heat transfer efficiency across two locations of a thermal component can be expressed in terms of thermal resistance *R*, defined as:

$$R = \frac{\Delta T}{Q} \tag{2.4}$$

where ΔT is the temperature difference between the two locations. Figure 2.7 shows the thermal resistance circuit between junction and ambient of a chip. The measurement unit of thermal resistance is in °C/W, indicating the temperature rise per unit rate of heat dissipation. This thermal resistance is analogous to the electrical resistance R_e, given by Ohm's law:

$$R_e = \frac{\Delta V}{I} \tag{2.5}$$

with ΔV being the voltage difference and I the current.

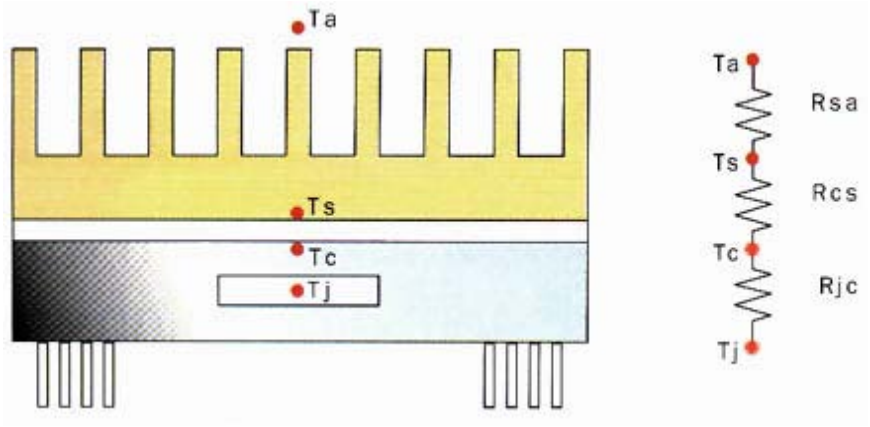


Figure 2.7: Thermal Resistance Circuit.

A) Heatsink Selection

One of the most important considerations in this measuring setup is to have the DUT operating in the conditions under which it was designed to operate. Under these conditions the cooling system of our DUT (a FPGA processor with BGA technology or a simple BJT) is a passive air cooling system which uses a fan with variable speed to remove the heat according to power dissipation.

The temperature distribution of the DUT with a cooling fan is shown in figure 2.8. The thermocouple installed under the heat-sink (LO1) indicates temperature of 52.3^{o}C. However the heat-sink is not transparent to IR radiation, therefore; the DUT temperature cannot be obtained directly.

Several liquids to act as coolants were explored in [2]. Water, which has a very high specific heat, makes it ideal for such experiments, but it is opaque to the IR camera. Several fluoride materials are extremely transparent to IR with a high capacity to cool down modern processors, but their toxic nature makes them unsuitable. The most transparent IR material was olive oil which was transparent enough to perform good measurement, but difficult to be pumped due to its high viscosity.

Aldrich Mineral Oil 161403 was selected as the heat-sink for the test setup due to its elevated transparency in the infrared spectrum, high specific heat, relatively high thermal conductivity, relatively low viscosity, and chemical safety. The oil was pumped to the surface of the chip and is capable of removing 100W heat from the DUT.

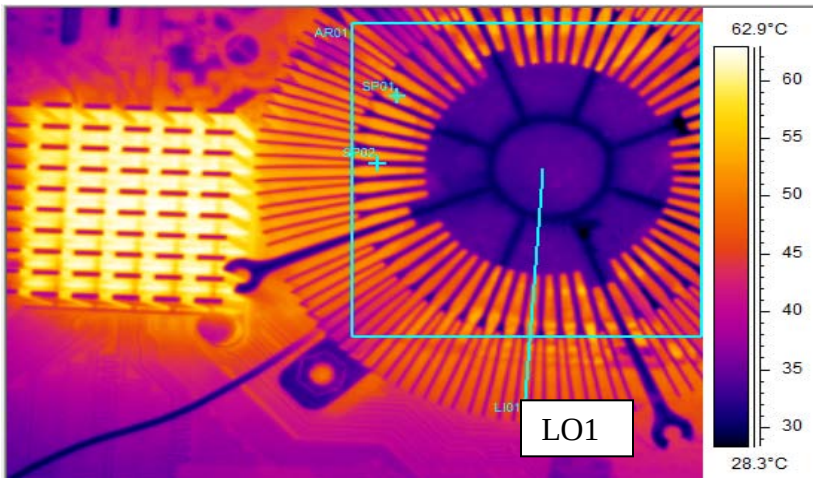


Figure 2.8: Temperature Distribution of the DUT with Air Cooling.

B) Heatsink Flow

The oil flow regime is a major factor affecting the temperature measurement of the DUT in the experimental setup. Several different oil flow scenarios were studied below.

1) Turbulent flow: the oil pipe is positioned about 5 cm above the DUT and the oil was pumped directly to the surface of the DUT. The magnitude of the temperature versus time is represented in figure 2.9.

2) Turbulent flow at an angle of 45 degree: the oil pipe is positioned about 5 cm above the DUT, but the oil was pumped with a 45 degree angle. The magnitude of the temperature versus time is represented in figure 2.10.

3) Laminar flow: oil flows over the DUT with an almost angle of zero and in parallel layers. The magnitude of the temperature versus time is represented in figure 2.11.

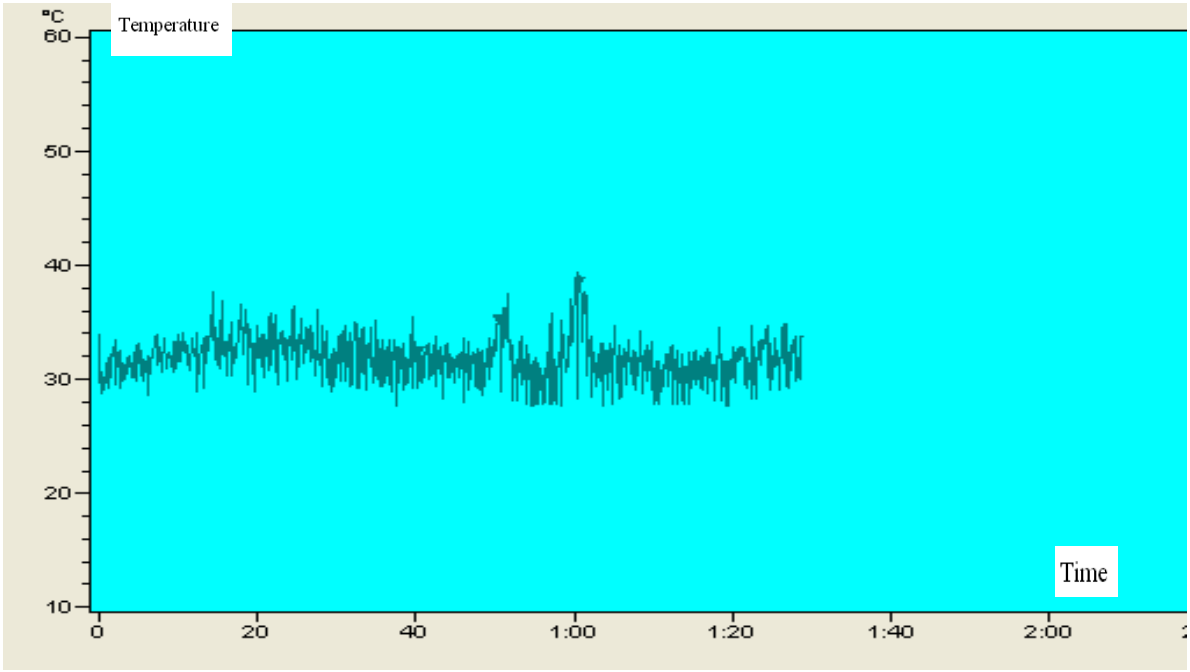


Figure 2.9: Temperature Measurement with Turbulent Oil Flow.

The obtained results indicate that the turbulent flow in both figure 2.9 and figure 2.10 has more fluctuations in temperature than laminar flow shown in figure 2.11. Laminar oil flow regime was chosen as the heat-sink system.

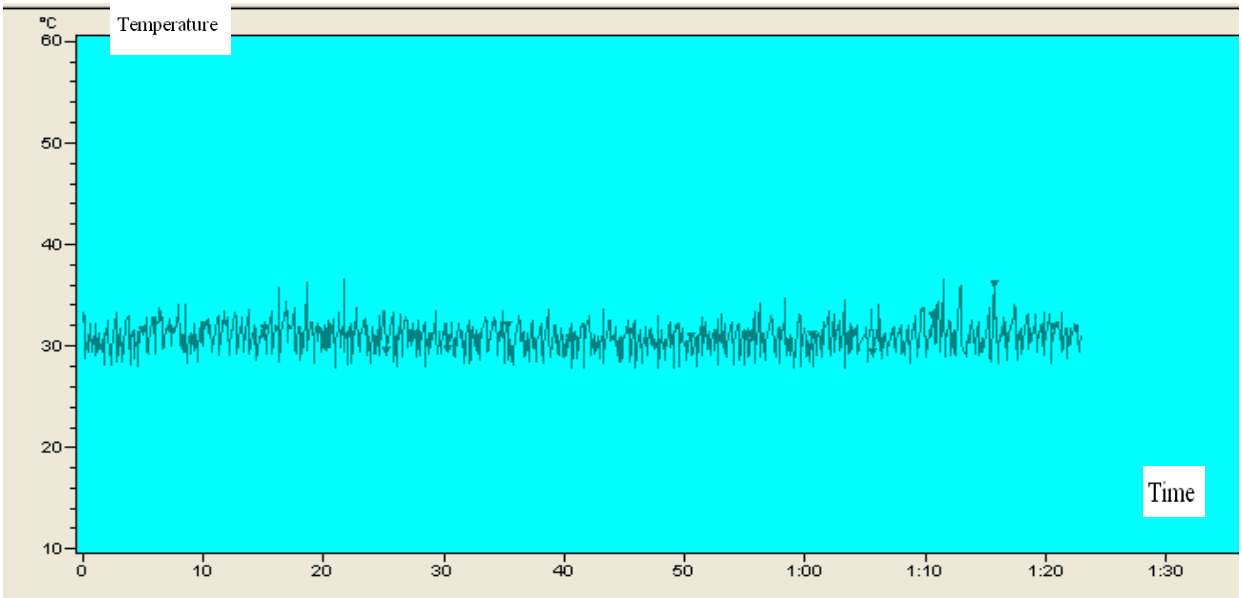


Figure 2.10: Temperature Measurement with Turbulent Oil Flow at an Angle of 45^{o}.

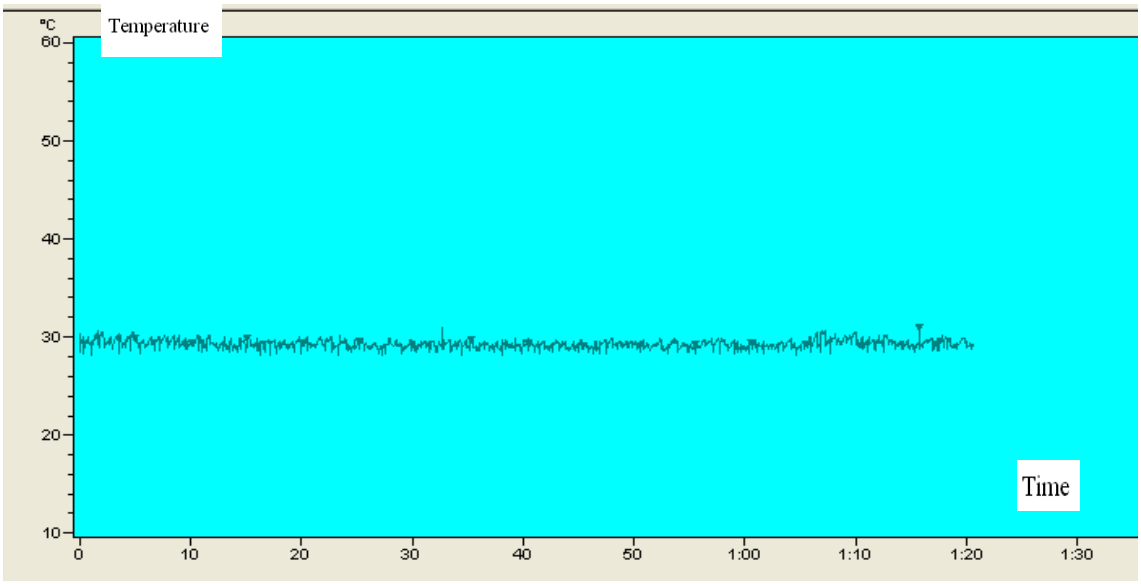


Figure 2.11: Temperature Measurement with Laminar Oil Flow.

2.1.4.4 Oil Pump

The utility pump shown in the figure 2.12 is suitable for variety of tasks such as pumping mineral oil since it is designed especially for harsh fluid transfer. A 12V DC battery was used to power the pump.

Figure 2.12: Utility Pump

2.1.4.5 Thermocouple and Digital Thermometer

The measured temperature in this setup is initially verified by using a thermocouple. A variety of thermocouples are available for different measuring applications. They are usually selected based on the temperature range and sensitivity needed. Thermocouples with low sensitivities (B, R, and S types) have correspondingly lower resolutions. In this setup a type K (*chromel–alumel*) thermocouple is used which is the most common general purpose thermocouple. It is inexpensive and available in a wide variety of probes. They are available in the −200 °C to +1350 °C range.

An Omega HH-23A digital thermometer was used with the thermocouple probe to record and display the temperature of the DUT [32].

2.1.4.6 Emissivity

One of the most important parameters that affect the temperature measurement of the DUT is emissivity. As described previously it defines the fraction of radiation emitted by an object as compared with emitted by a perfect radiator (blackbody). Emissivity value is between 0 and 1 and depends on the material of the object, surface condition (surfacing method, geometry), the temperature of the object, wavelength, and direction of radiation.

The default emissivity of camera is set to 0.93; however the real emissivity might be different from this value. Figure 2.13 illustrate the temperature measurement of the DUT using different emissivity values and the average error percentage of the IR thermography measurement with reference to thermocouple measurement, respectively.

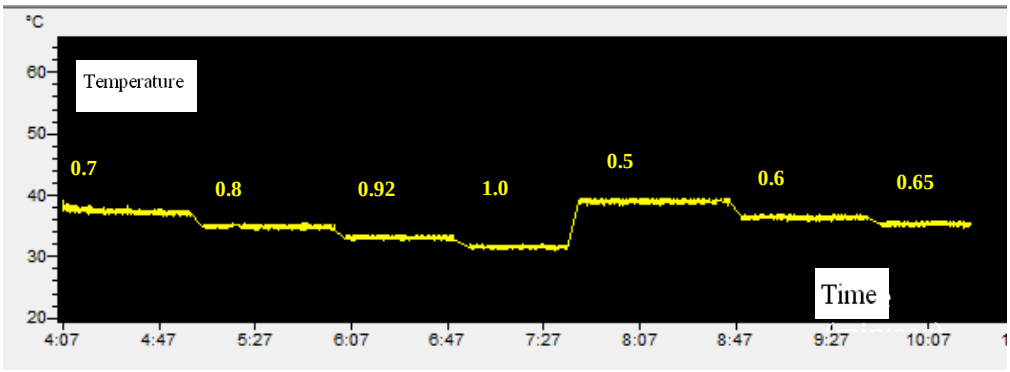


Figure 2.13: Emissivity Effect on Temperture Measurement of the DUT.

2.2 Summary

Different Ball Grid Array (BGA) technology and packages were introduced. This type of package was selected to the subject of thermal analysis in this work. In addition, adequate layout description of BGA was presented.

The heat conduction mechanism which is the most important heat transfer phenomenon for most electronic components, including the BGA, was discussed. CTM approach with applications to a BGA is also presented.

The infrared (IR) thermography measurement setup used to obtain the temperature profile and power dissipation of a BGA was discussed. The major equipments and the systems used in the experiment setup were discussed in this chapter. The effect of various parameters such as the oil flow condition and emissivity of the target were studied and the proposed setup for this work was presented.

CHAPTER 3

Software and Computing

3.1 Introduction

Various hardware and software pieces are required to obtain a compact thermal model of a package. This chapter describes the software and computing tools used during this work. These tools were applied to the test setup (pre-experimental section), various Coding programs, execution and running the experimental case studies and post-processing analysis.

The application of the developed software and computing tools was illustrated via a number of obtained figures, equations and tables to clarify the process.

Three different categories of software were applied in this work: Pre-Experimental software is those related to the programming of a BGA, due to its functionality as a microprocessor. Then, infrared (IR) camera system's dedicated software is discussed as part of the data acquisition system. The last category is mathematical and post-processing software to obtain the compact thermal model for a BJT and a BGA.

The hierarchy of these sets of software is shown in figure 3.1. The flowchart shows the time-line of the software application in this work. The dashed box shows the concurrent flow of finding the power and current with the respective software.

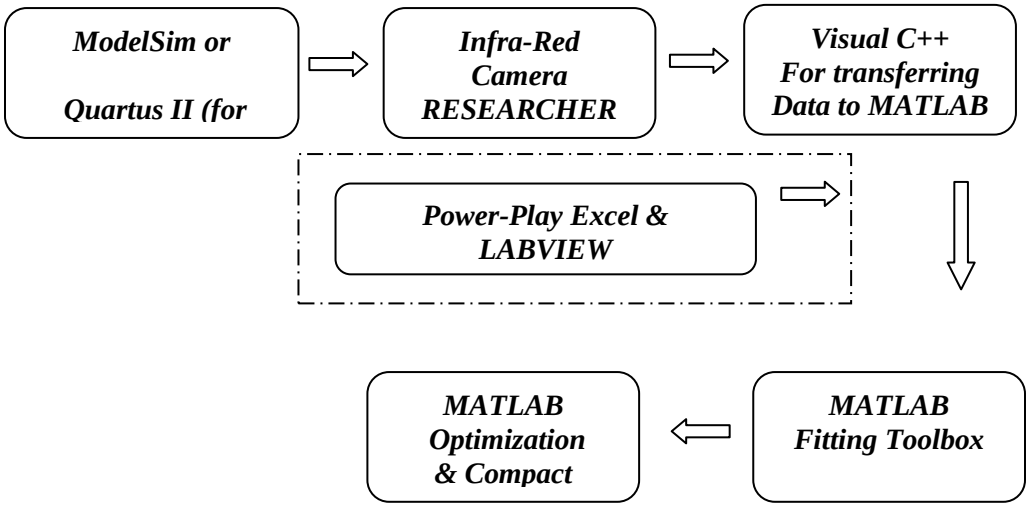


Figure 3.1: Flowchart of Software Application.

3.2 ModelSim & Quartus II

The application of the ModelSim [33] and Quartus II [33] module to run the BGA is described in this section. The aim of implementing this module is to run the BGA in a way that the circuitry and as such the BGA, drives a current into the circuit and by calculating the power (/ current) of the BGA and having the temperature profile of the BULK (of the device under test (DUT) and tracking the junction spot's profile) the static and dynamic compact thermal model may be obtained. The major difference between these two modules in programming a FPGA is the fact that the Quartus II is a block diagram-based and hence *object-oriented* software whereas ModelSim consists of Verilog codes (a hardware description language) which are in *C* and *C++* coding structure [33]. Therefore, using this module is more appropriate in terms of the availability of more authorities, basic machine language; in contrast, more time is needed to make the codes compatible with different DUTs.

The development kit of the BGA has sets of example demonstration codes of Verilogs (with *.v format) [25, 34], which were used in the analysis efforts.

Beside the "No Load" situation of the FPGA, which the whole board was on the idle mode and no instructions were implemented, several different codes were developed as independent experiments and their sets of thermal analysis (temperature profiles and maximum currents/ powers) were acquired with the infrared camera. Two of these sets were developed in Verilog format and two others in Quartus II block diagram basis. Parts of the Verilog scribe is illustrated in figure 3.2.

Music Synthesizer Demonstration: This code is a complex code consisted of different modules to cooperate in order to synthesize a set of different elements of the board simultaneously to get more power in a less time-consuming ways from the circuit. More details on the implementation aspect are described in [34] (Advanced Examples section).

```
183  ////////////////////////Music-Synthesizer Block////////////
184  //////Timing or Clock generater///////////////////////
185      reg    [31:0]VGA_CLK_o;
186      wire   keyboard_sysclk=VGA_CLK_o[11];
187      wire   demo_clock     =VGA_CLK_o[18];
188      assign VGA_CLK        =VGA_CLK_o[0];
189      always @(posedge CLOCK_50) VGA_CLK_o=VGA_CLK_o+1;
190
191  //////////DEMO Sound/////////////////////////////////////
192  //////demo-sound-CH1//////
193      wire [7:0]demo_code1;
194      demo_sound1 dd1(
195          .clock(demo_clock),
196          .key_code(demo_code1),
197          .k_tr(KEY[1])
198      );
199  //////demo-sound-CH2///////
200      wire [7:0]demo_code2;
201      demo_sound2 dd2(
202          .clock(demo_clock),
203          .key_code(demo_code2),
204          .k_tr(KEY[1])
205      );
206
207  ////////////////////KeyBoard Scan/////////////////////////
208      wire [7:0]scan_code;
209      wire get_gate;
210      wire key1_on;
211      wire key2_on;
212      wire [7:0]key1_code;
213      wire [7:0]key2_code;
214      PS2_KEYBOARD keyboard(
215          .ps2_dat  (PS2_DAT),        //ps2bus data               inout
216          .ps2_clk  (PS2_CLK),        //ps2bus clk                inout
217          .sys_clk  (keyboard_sysclk),//system clock      input
218          .reset    (KEY[3]),         //system reset              input
219          .reset1   (KEY[2]),         //keyboard reset            input
220          .scandata (scan_code),      //scan code             output
221          .key1_on(key1_on),          //key1 triger
222          .key2_on(key2_on),          //key2 triger
223          .key1_code(key1_code),      //key1 code
224          .key2_code(key2_code)       //key2 code
225      );
226
227  ////////////Sound Select/////////////
228      wire [15:0]sound1;
229      wire [15:0]sound2;
230      wire [15:0]sound3;
231      wire [15:0]sound4;
232      wire sound_off1;
233      wire sound_off2;
234      wire sound_off3;
235      wire sound_off4;
236      wire [7:0]sound_code1=(!SW[9])?demo_code1:key1_code;//SW[9]=0 is DEMO SOUND,otherwise key
237      wire [7:0]sound_code2=(!SW[9])?demo_code2:key2_code;//SW[9]=0 is DEMO SOUND,otherwise key
238      wire [7:0]sound_code3=8'hf0;
```

Figure 3.2: Parts of the Verilog code for a Music Synthesizer Implemented in the BGA.

The block which represents the more complicated instruction in the Quartus II compared to a simple Multiplier, is shown in figure 3.3. This figure would also be used as the schematics of the Load 3 in the Chapter 5 Section 5.2. It consists of a Multiplier, an Adder and a Multiplexer and gets two 8 bit input signals and generates a 16 bit output. The typical result obtained from this block diagram is shown in figure 3.4. The simulated noise for each block is present and affects the ultimate results.

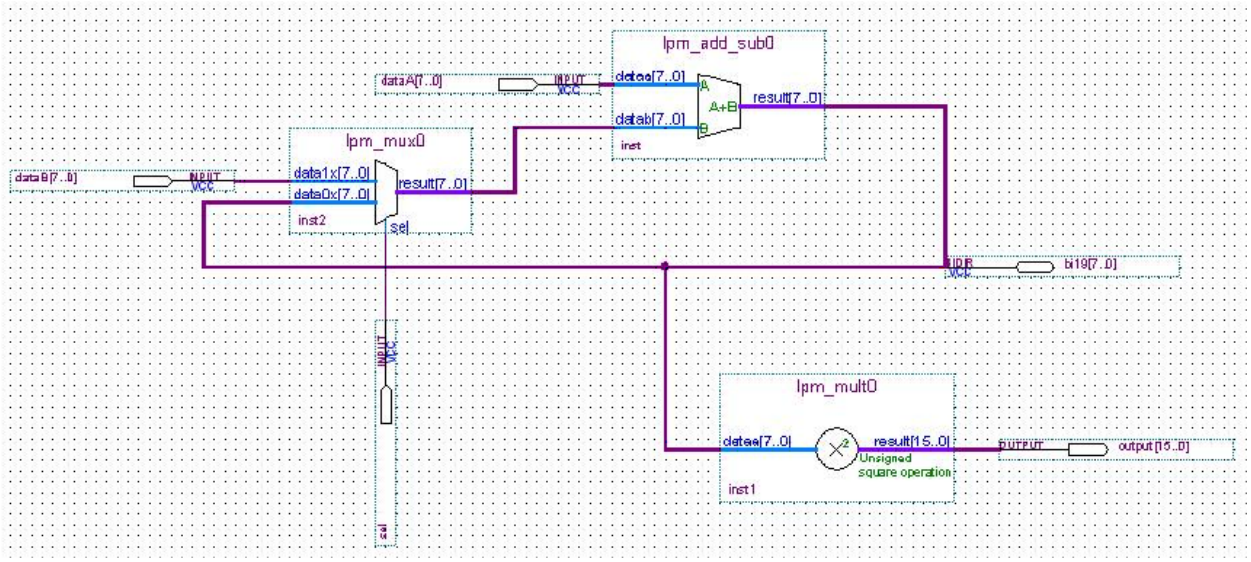


Figure 3.3: Relatively Complex Block Diagram for a Quartus II Instruction for the FPGA.

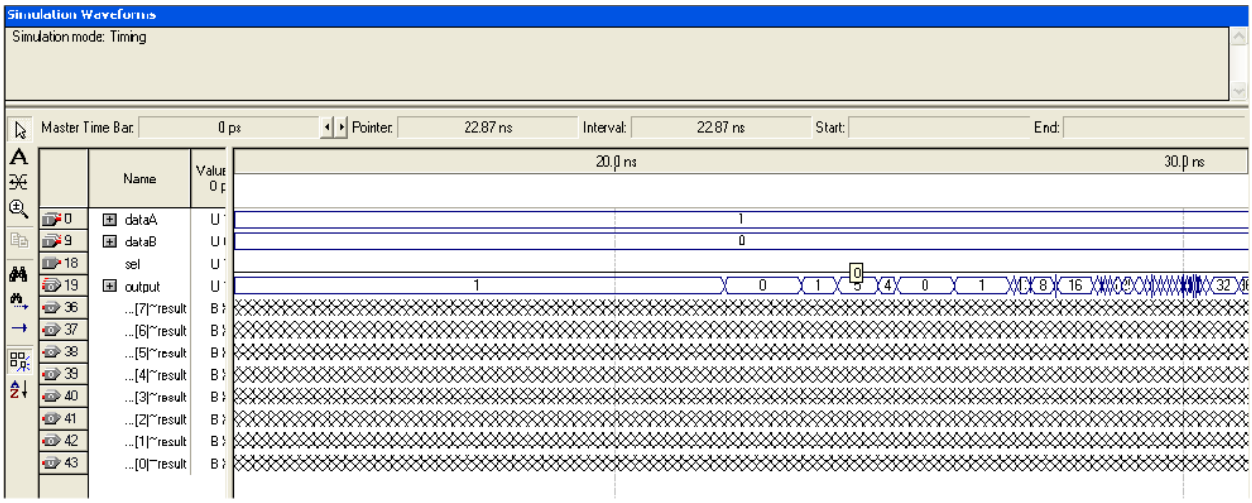


Figure 3.4: Results for the Complex Quartus II Code.

3.3 Infrared (IR) Camera's Dedicated Softwares

3.3.1 ThermaCam Researcher Software

When the implementation was accomplished in either mode of Instruction and with Quartus II or Verilog codes, the "ThermaCam Researcher" (Researcher) and the "Software Development Kit" (SDK) were applied as the dedicated softwares related to the IR camera system to record and to track the temperature profile of the BGA. Figures 3.5 and 3.6 are helpful to understand an instance of the implementation of the Verilog code or the Quartus II Block-based instruction into the DUT while the IR camera is tracking the temperature profile using Researcher software.

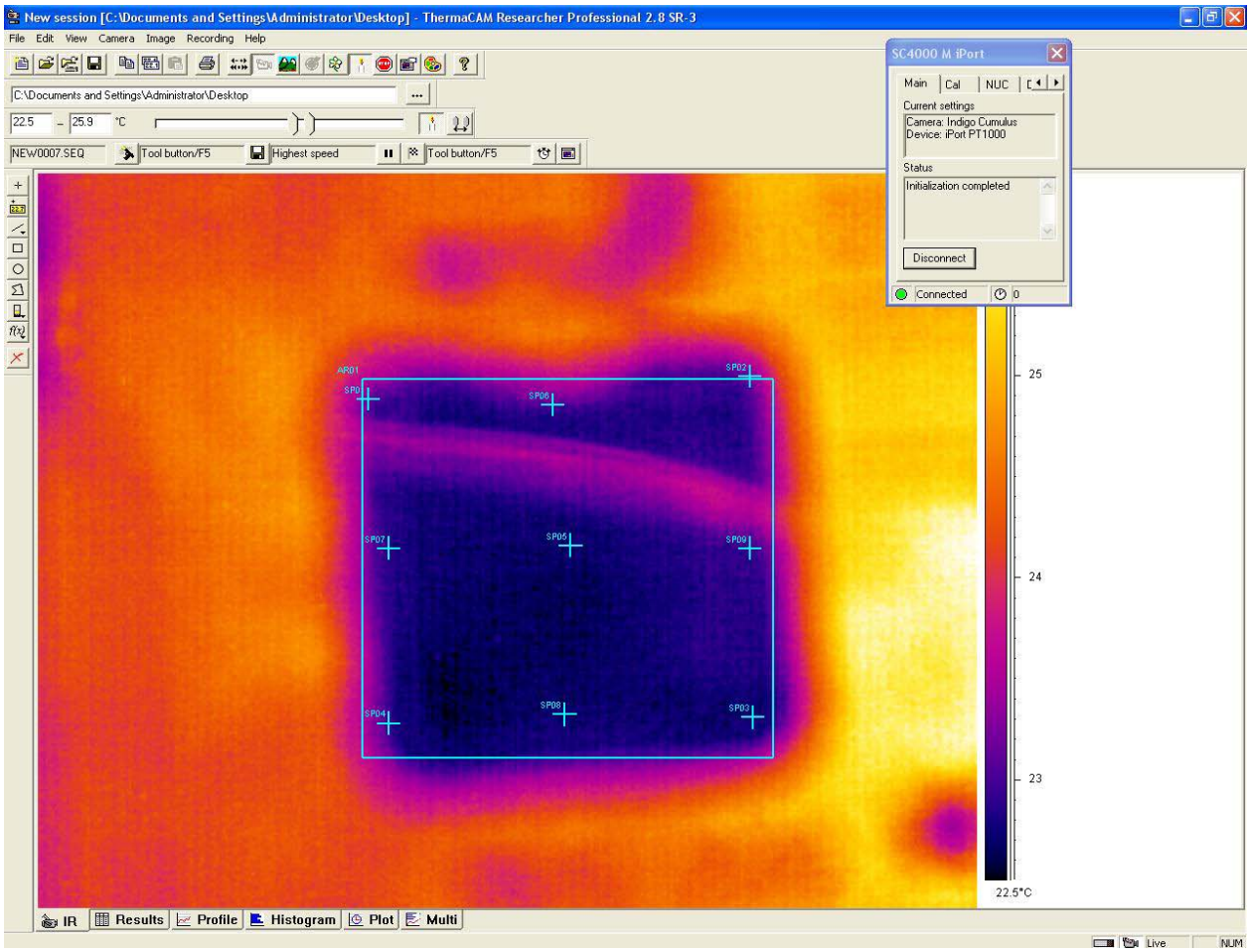


Figure 3.5: Temperature Profile of the BGA at a Given Time Frame by Showing the Physical BGA under its Screen before Starting the Power.

It can be observed from these figures that the environment of the Researcher contains a Graphic User Interface (GUI) which allows acquiring and saving of the data (in this case the temperature profile) of each time step in the screen. Figure 3.5 showed the physical BGA under its screen before starting the power while figure 3.6 is after the start-up.

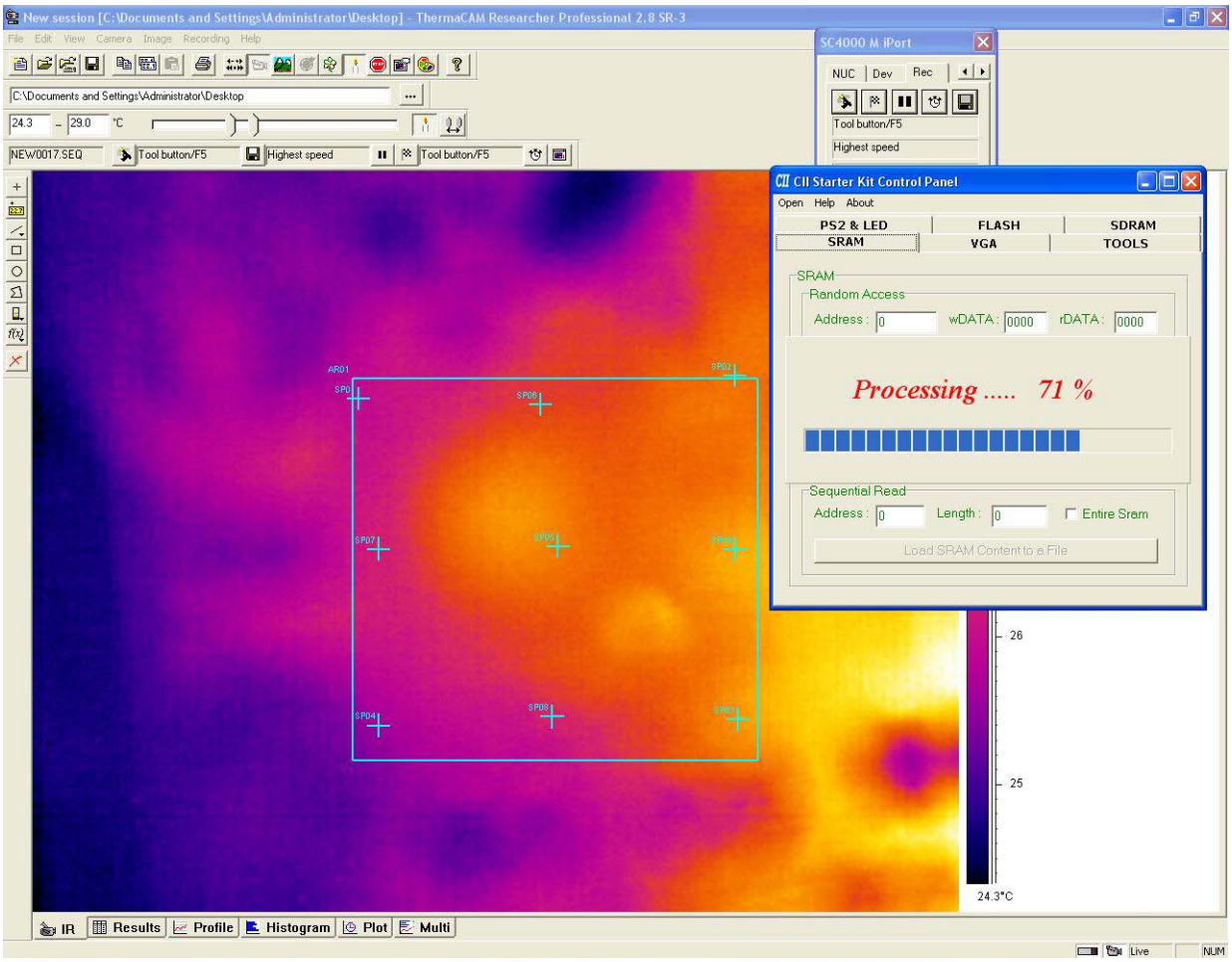


Figure 3.6: Indicating the Implementation Process While Acquiring Temperature Profile in a Researcher.

Figure 3.6 also shows the implementation process while acquiring the temperature profile using Researcher software. It's also helpful to notice from figure 3.5 & 3.6 that the BGA was recognized with at least 4 nodes of a square. This is a drawback of the Researcher compare to the SDK that in order to track a point in the surface the exact coordinates should be defined.

3.3.2 Software Development Kit (SDK)

Software Development Kit (SDK) of the IR camera system SC4000 is a collection of several custom programming, each with a specific function. The SDK allows users to write applications that can control and acquire the temperature profile as a collection of data points. The IR camera's SDK diagrams as component layers are shown in the figure 3.7.

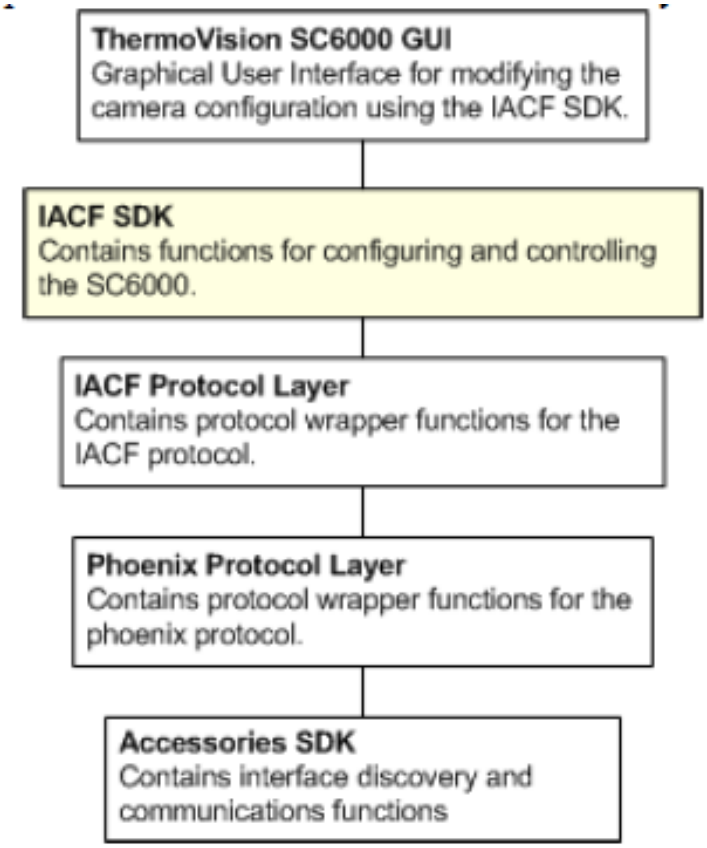


Figure 3.7: IR Camera's SDK Diagrams as Component Layers.

In summary the SDK works in the *Command Prompt level* which gives more options to communicate with these different layers and obtain the data directly without any restricting interface. This setup and data acquisition system was applied as the data in transfer to the next levels in this work; nevertheless the figures of the Researcher were selected to demonstrate some facts and suggest some clarifications and apply the presentation privileges of Researcher as in Section 4.3 in the next chapter.

3.4 Visual C++

All the work stations at the *Electrothermal Laboratory* works with the Visual Studio Version 2008 which enables the Researcher program to run the (Visual) C++ coding applied in this work. To use the raw data from SDK software which is in the form of several thousands of Excel frames for every experiment, where each file stands for a given time frame, another code is necessary in the command prompt window of Visual Studio software to transfer these raw data in another Excel file where the specified data is highlighted or picked and the extra costly information which is useless for the compact thermal model generation is ignored. The first lines of this preliminary code and the Visual C++ libraries maintained are shown in figure 3.8.

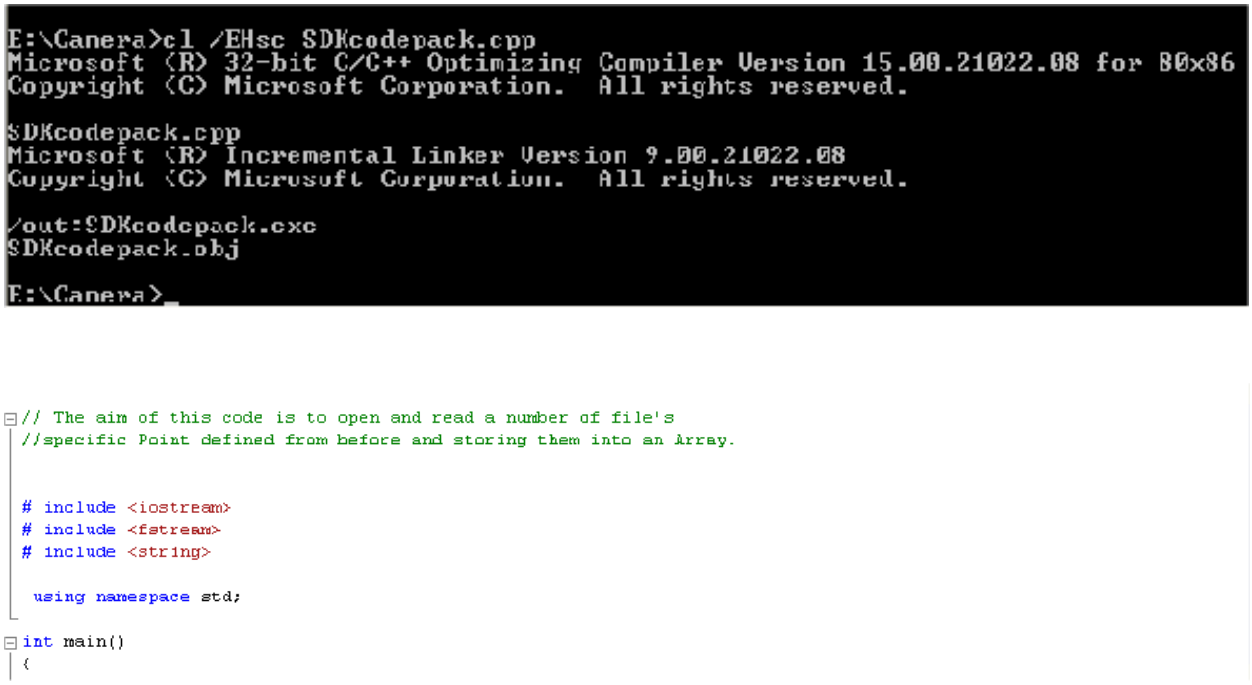


Figure 3.8: First Lines of a Visual C++ Code Including the Libraries Maintained and the Command Prompt Environment.

This code was written to transfer the .CSV formatted files of the output of the SDK software to Excel files focusing on a specific point or node, in this work mainly the junction temperature, which is the input and typically hottest spot on the surface of a chip.

The output frames of the SDK software for the BGA were set to 2700 frames which displays a couple of minutes after the device is turned on and the implementation is done. Figure 3.9 shows the rise in the temperature with the sampling rate of 1/10th of Maximum 30frame /sec for the IR camera in the BGA with a specific Quartus II code instruction called “Load 1” which was a simple Multiplier. In this figure the temperature is indicated in the Y axis and X axis is demonstrating the frame sequence which is in linear relationship with time of the operation.

The challenge of C++ code was I/O issue of inserting 2700 files and working with so many files to extract a specific point’s temperature profile (In this case the junction temperature or the hottest spot was in coordinates: Row = 121 & Column = 61); keeping in mind the fact that C++ is only able to work with less than 50 files open at the same time, due to I/O coding limitations [35]. The time of this extraction takes a couple of minutes with that many files and exporting a new file with the optional coordinate’s temperature profile.

Given that the results are on a discrete basis, it makes it suitable for the *Fast Fourier Transform* (FFT) process. A method was used to obtain these files data with a less optional frequency which maintains a total of 27 frames less than the total frames. This would definitely increase the maximum error marginally, while cutting the time consumed to export the whole files in one fetch. This method of coding is applicable especially if the trend of the increase or decrease in the temperature is relatively smooth and doesn’t imply any external temperature shocks.

3.5 MATLAB

3.5.1 MATLAB as a Mathematical Fitting Toolbox

MATLAB was used as a computational tool. The experimental data are processed and the results are post analyzed to obtain a compact thermal model. In order to find the static

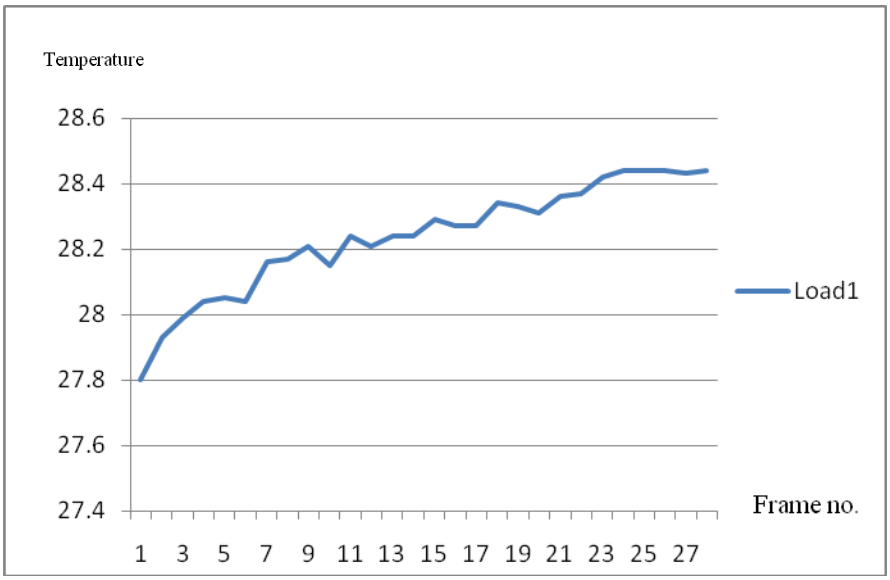


Figure 3.9: Temperature (Celsius) Profile of Junction Temperature in a BGA in a Specific Experiment of a Quartus II Instruction Called Load 1 which was Simple Multiplier Vs the Frame no.(× 100).

And especially the dynamic compact thermal model as the last element of the desired outcome, the fitting toolbox was applied both for the BJT and BGA experiments. The reason is that the transient time always refers to the capacitor properties and dynamic mode of the change in the profile must be taken into account. However, the static model may be obtained by using the end of the experiment or final temperature value and the initial value or starting point (this could be different from the ambient temperature of the experiment, since the delay run time of the SDK software should be considered). This toolbox in MATLAB is shown in figure 3.10. In addition, the obtained result for the junction temperature profile is shown in figure 3.11.

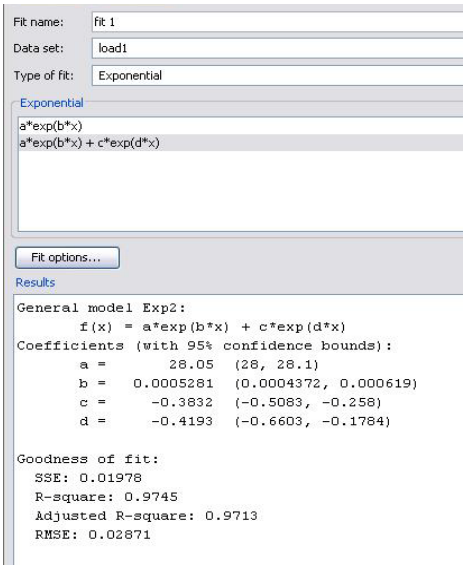


Figure 3.10: Applied MATLAB Toolbox for the Same Quartus II Instruction as Figure 3.9.

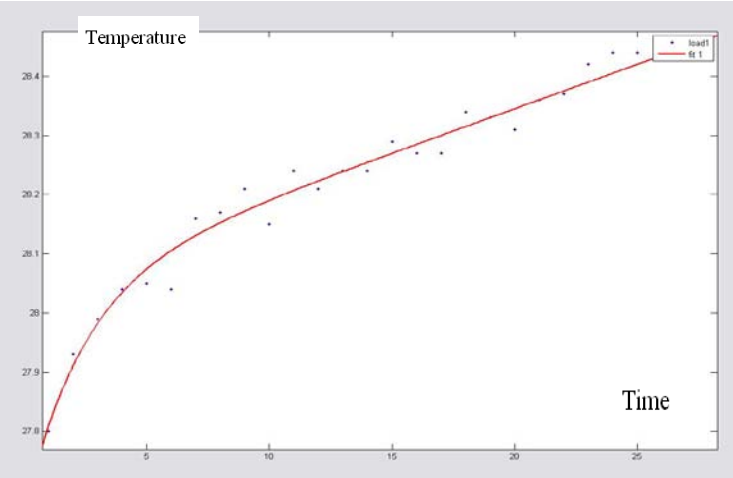


Figure 3.11: Junction Temperature Profile for the Same Quartus II Instruction as Figure 3.9.

As shown in figure 3.10 the best way to find the temperature profile for the junction temperature according to the input data is finding a mathematical expression as the sum of 2 exponential functions as stated in equation (3.1). The reason is that, among the proposed default settings in the MATLAB "Fitting Toolbox" the error would be the least in this case.

$$T(t) = 28.05U(t) - 0.3832 * \exp(-0.4 * t) \qquad (3.1)$$

More details on this toolbox and the mathematical method application could be found in [17].

3.5.2 MATLAB as an Optimization Tool

To generate the compact thermal model of a BGA, the number of the *unknown* parameters is typically more than the known equations obtained through the experimental test [1]. An alternative approach is trying to guess some values for the *unknown* parameters. To use this solution we need to define a cost function that calculates the difference between the compact and experimental data and try to fit some unknown parameters' value that minimize this cost function. In other words, compact thermal model calculation is an optimization process. The cost function used to represent this

deviation is (detailed discussion on this cost function will be provided in Chapter 4, Section 4.4):

$$COST_{SS} = \frac{1}{BC}\sum_{i=1}^{BC}(|T_j^d(\omega_k)| - |T_j^c(\omega_k)|)^2 \quad (3.2)$$

This deviation is basically relying on the difference of temperature of the junction which the proposed model predicts and the real temperature which is described in this work by the detailed thermal profile of the junction spot; these two factors are indexed with “c” and “d”, respectively as stated in the cost function equation (3.2). Equation (3.2) is a typical cost function in the steady state mode, where the index “BC” is the number of applied boundary conditions.

Equation (2.3) (see Section 2.1.3.2) was used in the MALTAB optimization process. It computes the temperature every time the cost function is going to be calculated, by a resistor set in the Y matrix which represents the admittance matrix.

The BGA layout model includes TOP1, TOP2, and SIDE areas, LEAD1, LEAD2, and BOTTOM areas to generate a model with minimum required accuracy; thus the resistor network must have seven nodes that represent these regions. Therefore, only 6 maximum independent equations for 7 unknown resistors are required to use the optimization technique.

In this case several programs were written to generate the static and dynamic compact thermal models. These programs compute and minimize the proposed cost functions.

The number of equations respects for the number of experiments performed in this work was 3 and therefore 3 unknown elements in the dynamic compact thermal model is expected to be predicted. This means that in this work 3 different sets of experiments are needed to obtain the CTM with three (3) unknowns as the resistor or capacitor matrix elements for static or dynamic modes. In summary, the procedure of generating the static compact thermal model as the initiation preceding the dynamic mode consists of these steps: First, the experimental tests were performed and then these tests results were compared to results of simulations of the BGA package for the similar boundary conditions. The difference between them would lead to more precise simulations and a network is postulated. This network consists of several resistors that connect the thermal nodes to each other. The same process applies to the dynamic compact mode. There are

two major differences between these two models as was verified in this work. First, the boundary conditions in this work have to be optimized themselves as the heat transfer coefficients of the DUT. Also the definition of errors in the dynamic mode depends on the samplings of the temperature profiles which increases the errors hypothetically and hardens the convergence of the optimization.

Part of different scribe developed to compute the value of dynamic cost function and the temperature junction predicted by the proposed model is shown in figure 3.12 [36]. The applied optimization toolbox is based on Gauss-Newton nonlinear least square roots method [37, 38].

```
1   function f = CostSS( R)
2
3 -  Q=[0.966 0.313:0 0:0 0:0 0:0 0:0 0:];
4 -  Td=[312.4000  301.3161];
5    %BC=length(Q(1,:));
6 -  BC=2;
7 -  for i=1:BC
8
9 -      x= Temp(10000, 50, 10, 500, R(1), 100, R(2
10 -     f = ( ( x(i)-Td(i) )^2 |/BC;
```

Figure 3.12: Codes of Dynamic Cost Function and Temperature Computed by the Proposed Model.

3.6 Other software (FPGA Programmer and Power-Play Excel)

Some other software was applied during this work, which is worth mentioning. The other input which has to be known to obtain the compact thermal model is the power / current. As mentioned earlier in the Section 3.1, the process of finding the power / current of the experiment is independent from the temperature measurements and computations. This would be a great prerogative in order to gain more time savings to generate the compact thermal models if the generation of the compact thermal model is performed with a relatively fast multi-task processor.

The process of measuring the current directly as was performed in Chapter 5 will be explained in Section 5.3 by the test setup instrumentation; nevertheless it was verified with the Power-Play Excel-based Power Estimator software shown in the figure 3.13.

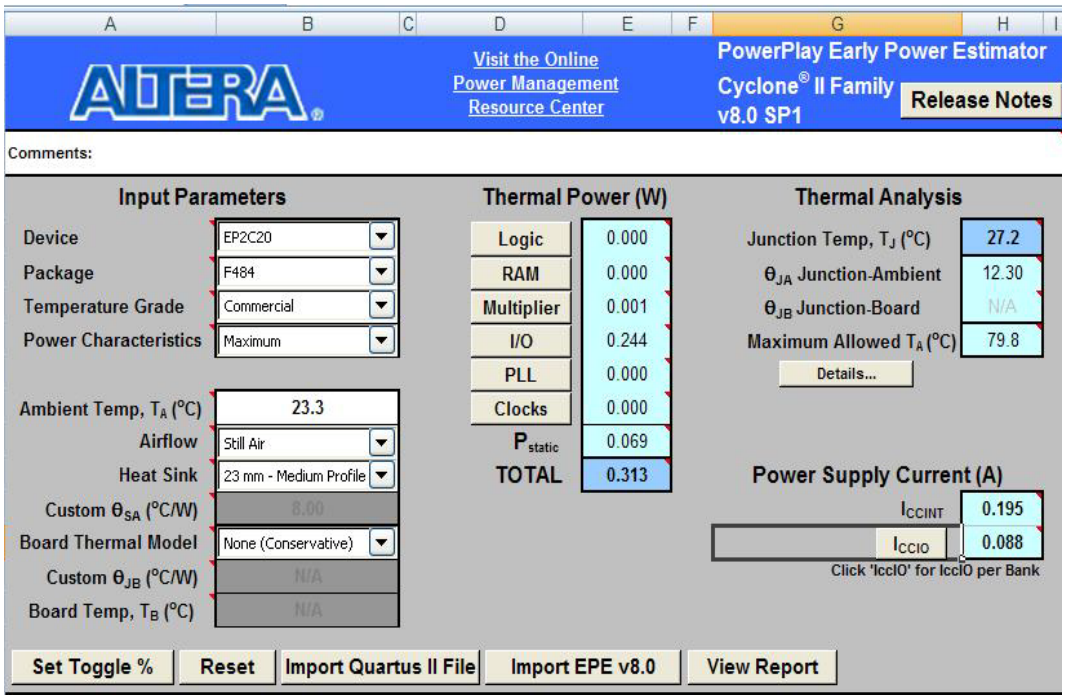


Figure 3.13: Power-Play Excel-Based Power Estimator Used to Verify the Power Measured from the Same Instruction Used in Figure 3.9.

This figure shows the details of the test setup for the used FPGA. The power estimated according to the number of Input / Output and other elements of the circuitry applied in the Quartus II instruction. Another prerogative of using Quartus II instead of Verilog coding is the ability to verify the power measured and computed by the prediction given by the Power-Play Power Estimator.

The FPGA controller starts up in an external monitor. To implement in a code a specific program dedicated to the FPGA is necessary. An appropriate test setup and dealing with the special GUI of the FPGA was imperative to carry on further levels of the work. More details of how these guidelines and the language could be structured, is discussed in [32].

3.7 Summary

Due to numerous and different software application in this work, it was deemed necessary to describe the elementary usage of each of these pieces of software and their interfaces with the reader to better understand the methodology of generation of compact thermal modeling. The Modelsim and Quartus II which were applied in the design level of the experiments were discussed.

The integrated data acquisition system of the optical system, supported by PC-based ThermaCAM Researcher software for data acquisition, analysis and reporting was discussed. Additionally the infrared camera system has an optional Software Developers Kit (SDK) for custom programming. The differences and properties of both of the systems were compared to each other.

An algorithm was developed in MATLAB to calculate the proper values for the RC network. These values are optimized by a cost function and optimization algorithm. The optimization algorithm was based on the Gauss-Newton and Levenberg-Marquardt methods.

CHAPTER 4

Feasibility Study: Generation of the Compact Thermal Model for a BJT

4.1 Introduction

A feasibility study was performed to verify the proposed approach of the development of compact thermal model based on transient thermal measurement at the device level [9, 39, 47]. Therefore, a Power BJT ***2N39014*** transistor was considered as the target device. Some literature review in this chapter touches upon the datasheet of this transistor and its architecture, and also the test setup for the experimental test using the Infrared (IR) camera system. The key initiative of this chapter rolls around the comparison of simulation results of a detailed thermal analysis on the Silicon BJT and experimental results under different conditions.

In addition, the measurement results were processed by MATLAB to obtain the static and dynamic compact thermal model of the BJT. The obtained results were compared to the results in literature [40] to verify the feasibility of the approach. An active (Biased) BJT circuit with $V_{BE} = 0.85\ Volts$ and $V_{CE} = 10\ Volts$ is shown in figure 4.1. These would lead to power dissipation of 1.83 Watts as an input to the BJT according to [40].

The Static Compact Thermal Model (SCTM) of the BJT was developed in the 3rd Section of this chapter and the studies for finding a methodology for the dynamic compact thermal model under two different boundary conditions proceeds in the 4th Section. The summary would conclude this chapter.

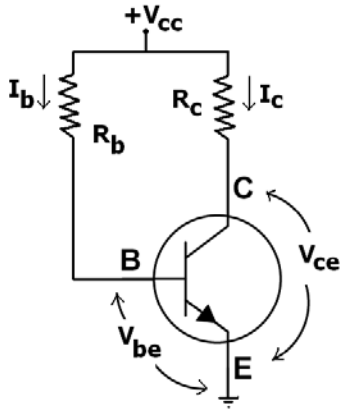


Figure 4.1: Fixed Biased Activated BJT.

4.2 Test Setup & Literature Review for BJT 2N39014

A test setup similar to one presented in Chapter 2, Section 2.1.4, was used to perform the thermal measurement of the BJT 2N39014. The room temperature in 10 different days is listed in table 4.1. The average room temperature of 23.88°C can be obtained.

T_{amb} (°C)	23.7	24.2	23.5	23.3	23.8	24	24.2	24.4	23.9

Table4.1: Room's Temperature in 10 Consecutive Days before the Experiment.

Since the experiments were run under the normal conditions, all of the boundary conditions are equal and this average ambient temperature applies to them. The average ambient temperature for experiments on BGA dropped later to 23.3 °C. In addition, all of the other assumptions were based on the data and test setup discussed in details in Section 2.1.4.

4.3 Static Compact Thermal Model for the BJT

Nine (9) optional points were chosen as an arbitrary focus structure to model the BJT's area on board, which is a feature, empowered by the Researcher software and is shown in the figure 4.2.

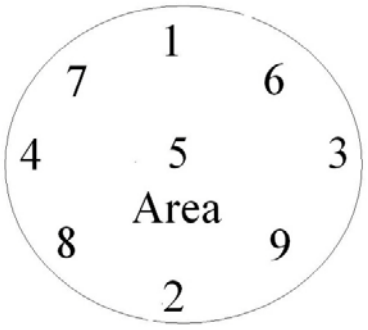


Figure 4.2: Researcher's Focus Structure Modeled for the BJT's area to track some sample temperatures.

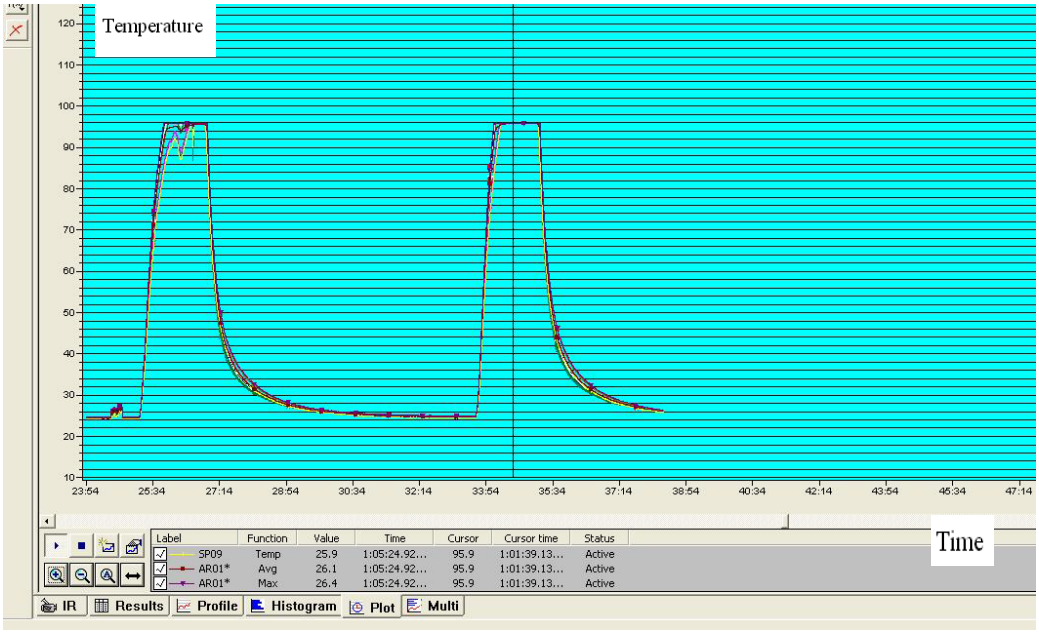


Figure 4.3: Measured BJT Temperatures for the Second BJT;
Indicating Two Almost Identical Rises for Temperature; Getting Cut-Off.

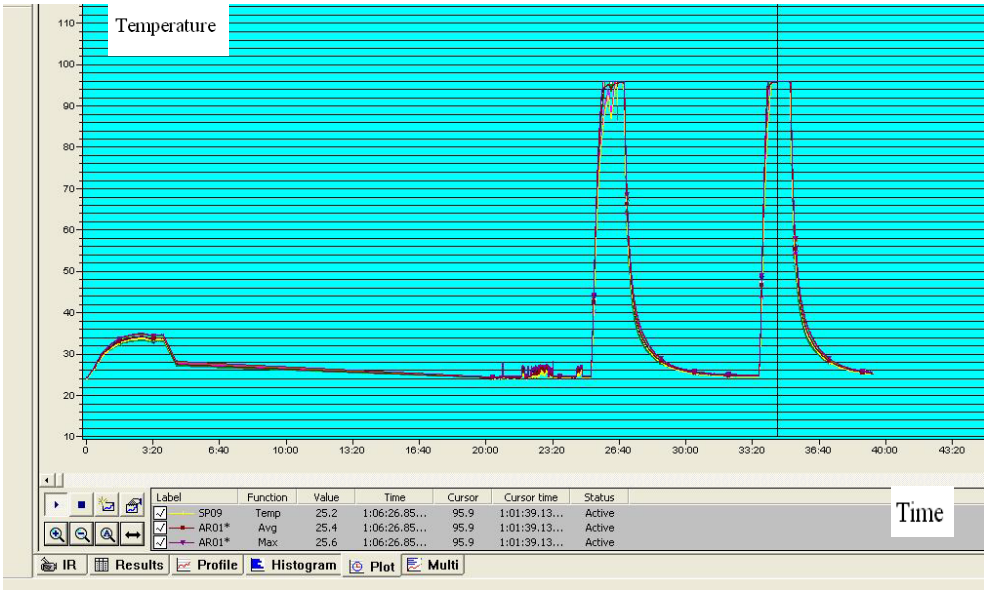


Figure 4.4: Measured BJT Temperatures for the Second BJT;
Comparing to the First BJT; Getting Cut-off.

Transistor	Temperature(T)	Measured Current(Ic)	Power Dissipation(Q)
1	31 °C	31mA	0.31 Watts
2	123 °C	276mA	2.76 Watts
3	116 °C	266mA	2.66 Watts

Table 4.2: Power Dissipation Computed on Measured Output Current during the Experiments.

Three transistors were tested. The obtained results are shown in figure 4.3 and 4.4. The X axis in these diagrams shows the time evolution and the Y axis shows the temperature. Each of the picks in the two figures shows each transistor switching during the experiments so as to allow comparison between the two. Thus, the different colors of the profiles, track temperature's profiles for various spots on the surface of each transistor, yet correspond to a similar point coordinates on them.

According to the datasheet of the 2N3904 Si transistors the maximum nominal input Voltage is 0.85 *Volts* which is on the edge of the operation point input voltage in the literature. This means that transistors might be damaged and burnt out due to small perturbations and violations of input Voltage. According to the figure 4.4 this has happened to transistor #1. Figures 4.3, 4.4 would also verify the fact that new transistors #2 and #3 are functioning in their similar and right operational point, while the first transistor is malfunctioning. This also justifies the difference in power dissipation listed in the table 4.2 between the first transistor and the other two. In figures 4.5, 4.6 and 4.7 a new format of pointing out to the whole surface of the DUT is indicated via SDK. The whole screen is corresponding to the whole board divided by 320×256 cells and the

blue section holds the portion of the surface which has exclusively high temperature which responds to the BJT surface. SDK gives out more precise results than Researcher, knowing the fact that the frame 600th consists of the highest temperature cells in the 1800 frames obtained; the maximum Temperature is 31.82 °C. Furthermore, the average temperature on the board is 25.6 °C, on that exact instance. This indicates an approximately 8% relative error between SDK and Researcher, which is justified by the fact that the experiments were not identical. In other words, since the Transistor #1 was burnt out, the characteristics of the transistor are dynamic and its changes affected upon two different test experiments; one for obtaining SDK results and the other for obtaining Researcher results. The figure 4.3, 4.4 and transistor #3's Researcher images verified this proposition. Furthermore, the figure 4.7 shows a maximum temperature of 118 °C for the second transistor, in its 1200th frame for SDK, while Researcher indicated this as 123.2 °C; which means a 4% relative error in again two different experiments but one identical operating transistor. This error is much more tolerable than the first transistor's error (between SDK & Researcher). This also stipulates that the whole process of comparison between the SDK and Researcher work better in higher temperatures, which is more pleasant for future studies.

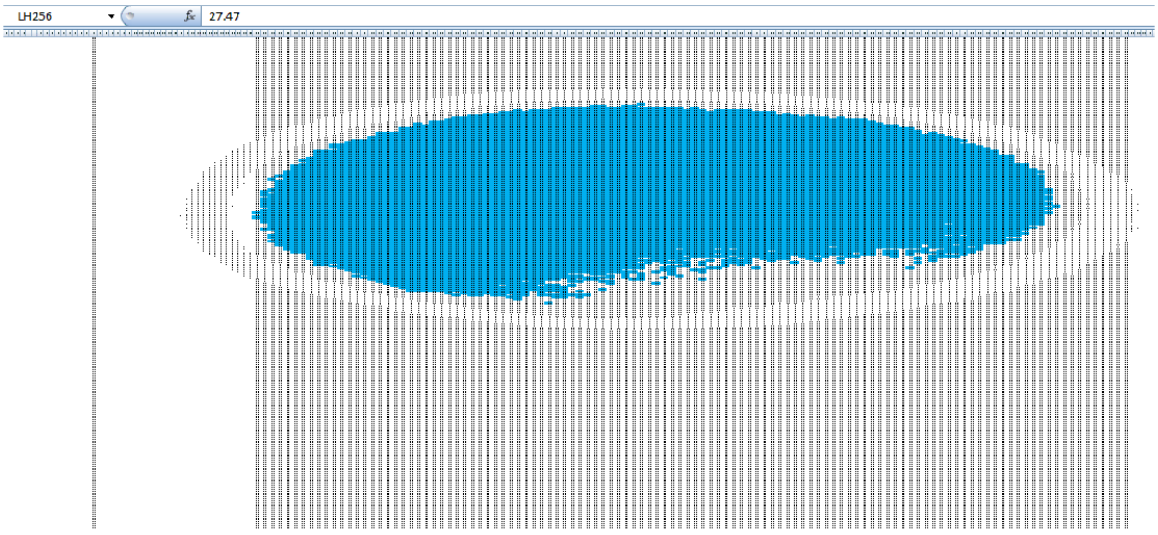
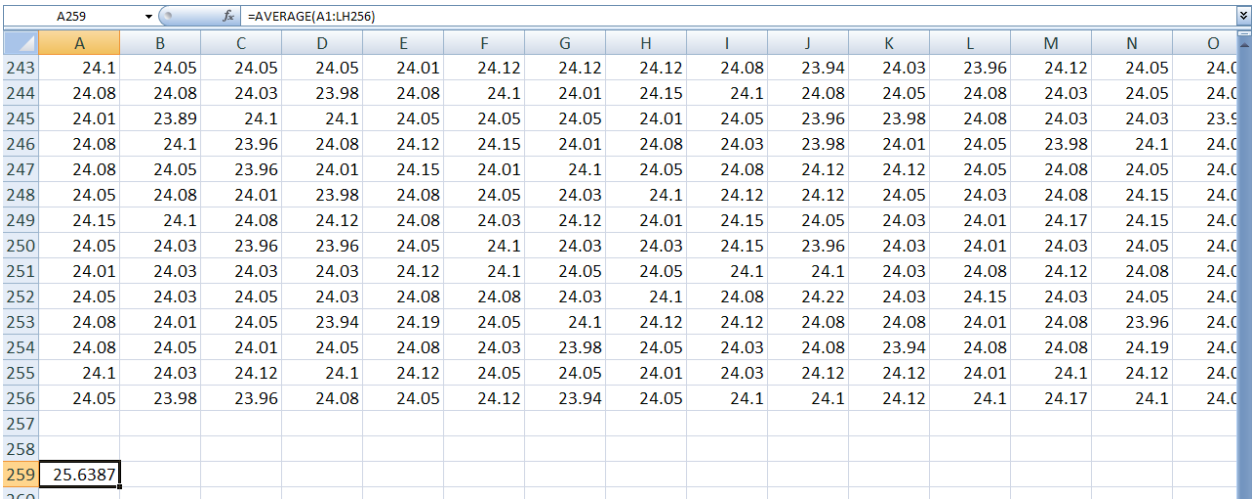


Figure 4.5: SDK Measured BJT Temperatures for the First BJT Frame 600; Identifying Temperature more than 31^{c} on Board.



A259 =AVERAGE(A1:LH256)

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
243	24.1	24.05	24.05	24.05	24.01	24.12	24.12	24.12	24.08	23.94	24.03	23.96	24.12	24.05	24.0
244	24.08	24.08	24.03	23.98	24.08	24.1	24.01	24.15	24.1	24.08	24.05	24.08	24.03	24.05	24.0
245	24.01	23.89	24.1	24.1	24.05	24.05	24.05	24.01	24.05	23.96	23.98	24.08	24.03	24.03	23.9
246	24.08	24.1	23.96	24.08	24.12	24.15	24.01	24.08	24.03	23.98	24.01	24.05	23.98	24.1	24.0
247	24.08	24.05	23.96	24.01	24.15	24.01	24.1	24.05	24.08	24.12	24.12	24.05	24.08	24.05	24.0
248	24.05	24.08	24.01	23.98	24.08	24.05	24.03	24.1	24.12	24.12	24.05	24.03	24.08	24.15	24.0
249	24.15	24.1	24.08	24.12	24.08	24.03	24.12	24.01	24.15	24.05	24.03	24.01	24.17	24.15	24.0
250	24.05	24.03	23.96	23.96	24.05	24.1	24.03	24.03	24.15	23.96	24.03	24.01	24.03	24.05	24.0
251	24.01	24.03	24.03	24.03	24.12	24.1	24.05	24.05	24.1	24.1	24.03	24.08	24.12	24.08	24.0
252	24.05	24.03	24.05	24.03	24.08	24.08	24.03	24.1	24.08	24.22	24.03	24.15	24.03	24.05	24.0
253	24.08	24.01	24.05	23.94	24.19	24.05	24.1	24.12	24.12	24.08	24.08	24.01	24.08	23.96	24.0
254	24.08	24.05	24.01	24.05	24.08	24.03	23.98	24.05	24.03	24.08	23.94	24.08	24.08	24.19	24.0
255	24.1	24.03	24.12	24.1	24.12	24.05	24.05	24.01	24.03	24.12	24.12	24.01	24.1	24.12	24.0
256	24.05	23.98	23.96	24.08	24.05	24.12	23.94	24.05	24.1	24.1	24.12	24.1	24.17	24.1	24.0
257															
258															
259	25.6387														

Figure 4.6: SDK Measured BJT Temperatures for the First BJT Frame 600; Identifying Some Sample Cells and Average Temp on Board.

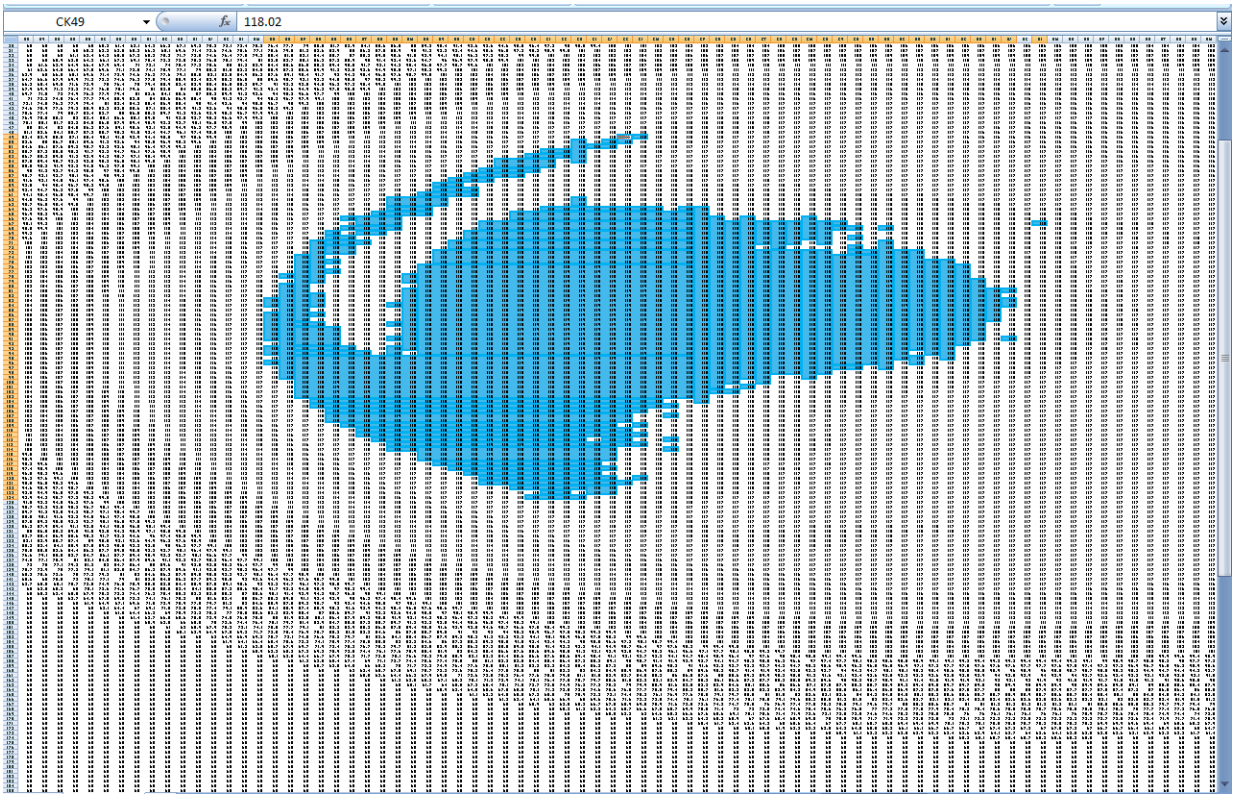


Figure 4.7: SDK Measured BJT Temperatures for the Third BJT Frame 1200; Identifying Temperature More than 118^{c} on Board.

As [40] illustrated, the thermal static model of a simple Si BJT can be simplified by a single resistance modeling the internal heat transfers in the transistors. The literature [40] mentions that the backside thermal resistance between the substrate and the chuck was estimated to be ***16 cm^2K/W*** based on the comparison of the measured maximum surface temperature and the simulated temperature for one power level. To find the resistance value according to the power dissipation, ambient temperature and temperature difference listed in table 4.1 and 4.2 and (between the junction which has the highest temperature and the ambient temperature). Therefore, for Transistors #2 and #3 the obtained thermal resistances was calculated as **35.86 K/W** and **34.58 K/W,** respectively.

The figures 4.5 and 4.7 showed how the two classes of BJT in our model are realistic. Recall that the blue cells which represent a 61% of the *eclipse* of the BJT's surface indicates the cells which are closer to the junction temperature than the rest of the cells in a given time frame of the heating process (after getting stabilized). This approximate number (approximate since the standard of 118ºC is not a rigid requisite for classification of the temperature of the surface of the BJT) is in good agreement with the measurement results stated in the next paragraph.

Under the assumption of this simplification of the area around the BJT, this value was computed as 91.65 mm^2 (according to the average number of blue cells and the actual value of area of each cell). To understand the effect of the surface on the resistor value, found by dividing it into this surface around the DUT and considering the ratio of 61% which corresponds to our one-parameter model (Junction-to-Ambient or Hot Spot-to-Heat Sink) a resistor of ***17.466 cm2·K/W*** was derived according to a combination of equations (4.1) & (4.2), which is reasonably close to our literature reference of ***16 cm^2·K/W*** [40] or a 8.39 % reasonable relative error in the static model.

Since the experiments were run under the normal conditions all of the boundary conditions were similar and the average ambient temperature (23.88°C) applies. As for the BJT applied in the previous experiment under the power dissipation of 2.66 Watts, and temperature of 118°C the heat transfer coefficient, was calculated via equations (4.1) & (4.2) as **572.73(W/m^2.K)** in all sides of the BJT. The governing heat transfer here as a specific condition to equation (4.1) is:

$$Q = \nabla.\left(-k\nabla T\right) = h(T_S - T_{amb}) \qquad (4.1)$$

Where: $Q\ (W/m^2)$ is heat source, h is the heat transfer coefficient(W/m^2k), T_S denotes the surface temperature, and T_{amb} is the ambient temperature of the room. k is the thermal conductivity$(W/\ mk)$. The boundary conditions for the experiments on the basis of an average Ambient Temperature of the room is relative to the Power Dissipation (Q) of that run and is computable with the mentioned equation. Also the heat transfer coefficients are defined as:

$$R \times h = \frac{1}{A} \quad h(^{W}/_{m^2K}) \tag{4.2}$$

Equation (4.2) shows that the boundary conditions have a counter effect on the natural resistance of the different layers of the BGA.

4.4 Dynamic Compact Thermal Model for the BJT

The general objective of a dynamic compact thermal model is to simulate the transient and time dependent thermal behaviors so that the temperatures and heat fluxes of the desired and predetermined location of the package could be calculated fast and with high accuracy. Our approach is to expand the resistor model (Section 4.3) with discrete thermal capacitor, calculating the capacitor's value by optimization method, and validation efforts. A typical dynamic compact model is a time domain first order system (thermal resistors and thermal capacitors) biased by a pulse input. This system's thermal response to the input would be an exponential diagram which saturates on a specific temperature due to the ambient temperature, heat transfer coefficients and the other dynamics of the system [1,3]. This happens while decreasing the penetrated current after reaching a maximum value (peak). This is consistent with the static and dynamic model of thermal resistors and capacitors as for the system to model such a behavior.

The major difference of the current approach with the one presented in [1] is that the exponential time-domain response of the system which is the detailed temperature of a node like junction as the input, is not obtained by the simulation, rather using the thermal measurement by infrared (IR) camera system. Therefore, our approach to obtain the dynamic compact thermal model is basically an extension of static compact thermal model to include the dynamic behavior

of the system. Using node voltage analysis, the governing equation of solving network can be obtained (Equation (4.3)) in frequency domain [1].

Where, [C] is the thermal capacitance matrix, [T(ω)] is the temperature vector, [G] is the thermal conductance matrix, And [P(ω)] is the nodal loads and sources which express the heat source connected to the junction node and boundary conditions applied to the external nodes.

Equation (4.3) is basically the transformed version on equation (4.1) in frequency domain.

$$[T(\omega)] = (j\omega[C] + [G])^{-1}[P(\omega)] \tag{4.3}$$

$$COST = \sum_{i=1}^{N}\sum_{k=1}^{n}\left(\frac{\left|Tj_i^d(\omega_k)\right| - \left|Tj_i^c(\omega_k)\right|}{\left|Tj_i^d(\omega_k)\right|}\right)^2 \tag{4.4}$$

$$COST = \frac{1}{BC}\sum_{k=1}^{BC}\left(\frac{T_J^c(k) - T_J^d(k)}{T_J^d(k) - T_{amb}}\right)^2 \tag{4.5}$$

Equation (4.3) is the definition of the RC network dynamic compact model. Matrix G or conductance matrix is equal to the static model generated in Section 4.3 and matrix C is the additional part that upgrades the model from static to dynamic. Following paragraphs and the next chapter explains how the matrix C was calculated for BJT and BGA, respectively. Initially, the equation (4.4) used as the cost function for the optimization purpose for the dynamic model is now slightly different than the one used for static model equation (4.5). Secondly, the equation used for minimizing the cost function has two more summation which is important in terms of the computational time. The dynamic model for a BJT could be derived in two different fashions. First, working on the discrete time analysis and finding the 512 samples is required to solve the case from the FFT transformation of the exponential sample obtained for the Static Compact Thermal Model (SCTM); then using those samples for the new problem to extract the unknown capacitor. Second approach is to find an exponential continuous function interpolated from the samples obtained from SDK (in Discrete Mode), transform it into frequency domain and again start sampling from this new function to reach a new set of data.

The problem of a BJT thermal compact modeling differs from the BGA compact thermal modeling with respect to the number of the unknown parameters (capacitors and/or resistors) in comparison with the number of equations (Nodes' Temperatures). In the dynamic mode, the difference between the dimension of Matrices [C] and [T] would enforce the resolution to be applied. If the number of equations exceeds the number of the unknowns like in the BGA case (Due to model's layout) [1], then an optimization tool should be used to minimize the least square of a function which was defined as the Error in equation (4.4) (distance of the real temperature and the simulated temperature generated by the arbitrary resistors) and by repeating the procedure in an iterative procedure a desired error would be obtained. Contrarily, in the BJT case, the RC network has only one resistor and capacitor, for the DUT and one equation, so the RC network of the DUT would be derived directly of the governing equation. The RC network was obtained based on the measurement results for the third BJT under two different conditions of ambient temperatures of 24 °C and 29°C with operation temperatures of 118°C and 84.5 °C, respectively. Applying the fact that the response function would be in the exponential form of equation (4.6) as explained in Section 3.5:

$$(\alpha * U(t) - \beta * \exp(-\gamma * t) U(t) = 0) \tag{4.6}$$

where all α, β, γ are certain constants and t is the time factor.

Then by substituting and unifying the above equation and omitting the step functions such as P (t) (due to the uniformity of both sides of equation (4.6)) and their derivatives:

$$-C * \left(\alpha * \gamma * \exp(-\gamma * t) U(t)\right) + G * \left(\alpha * \exp(-\gamma * t) U(t)\right) = 0$$

Or:

$$[C] = \frac{1}{\gamma} * [G] = {}^{1}/_{R * \gamma} \qquad \frac{J}{K} \tag{4.7}$$

where γ is the exponential temperature profile constant and R and C are the resistor and capacitor's set. The dimension of the C in the equation (4.7) requires that the factor of area of the DUT is disregarded. This is because to be consistent with the proposed dimensions of the capacitors for a BGA in the literature [1, 3].

The curve fitting toolbox was applied in this study as well to find the α, β and γ of the temperature profile parameters. The data which was applied in two different conditions were from the third transistor used before and are presented in the second and third column of the table 4.3 and was elaborated of how they were obtained after the steps for static compact thermal modeling in Section 4.3.

Sequence (1/30 sec)	First Transistor ~ 24 °C	Third Transistor ~ 24 °C	Third Transistor ~ 30 °C
100	23.96	59.98	59.98
200	24.01	83.69	59.98
300	25.33	90.32	62.47
400	26.2	105.82	69.08
500	28.57	111.49	73.7
600	30.17	113.94	76.95
700	29.46	115.79	79.22
800	30.8	116.44	80.8
900	29.62	117.04	81.91
1000	28.73	116.3	82.7
1100	28.12	118.3	83.23
1200	27.61	118.2	83.1
1300	27.19	116.66	64.4
1400	26.8	89.91	59.98
1500	26.53	63.2	59.98
1600	26.26	59.98	59.98
1700	26.03	59.98	59.98
1800	25.91	59.98	59.98

Table 4.3: Power Dissipation Computed on Measured Output Current during the Experiments.

The presented data were collected using the Visual C++ code line through 18 files (or frames) obtained using the SDK software and the Infrared (IR) camera with a 30 frame/seconds method in 60 seconds period. Just as a clarification note, the reason the second and third column starts

from the 59.98 is because of the calibrated regions of the Infrared (IR) camera, and the limitation of showing the whole region of 20 to 150 °C.

Figure 4.8 shows the results for such a process in the curve fitting toolbox for MATLAB.

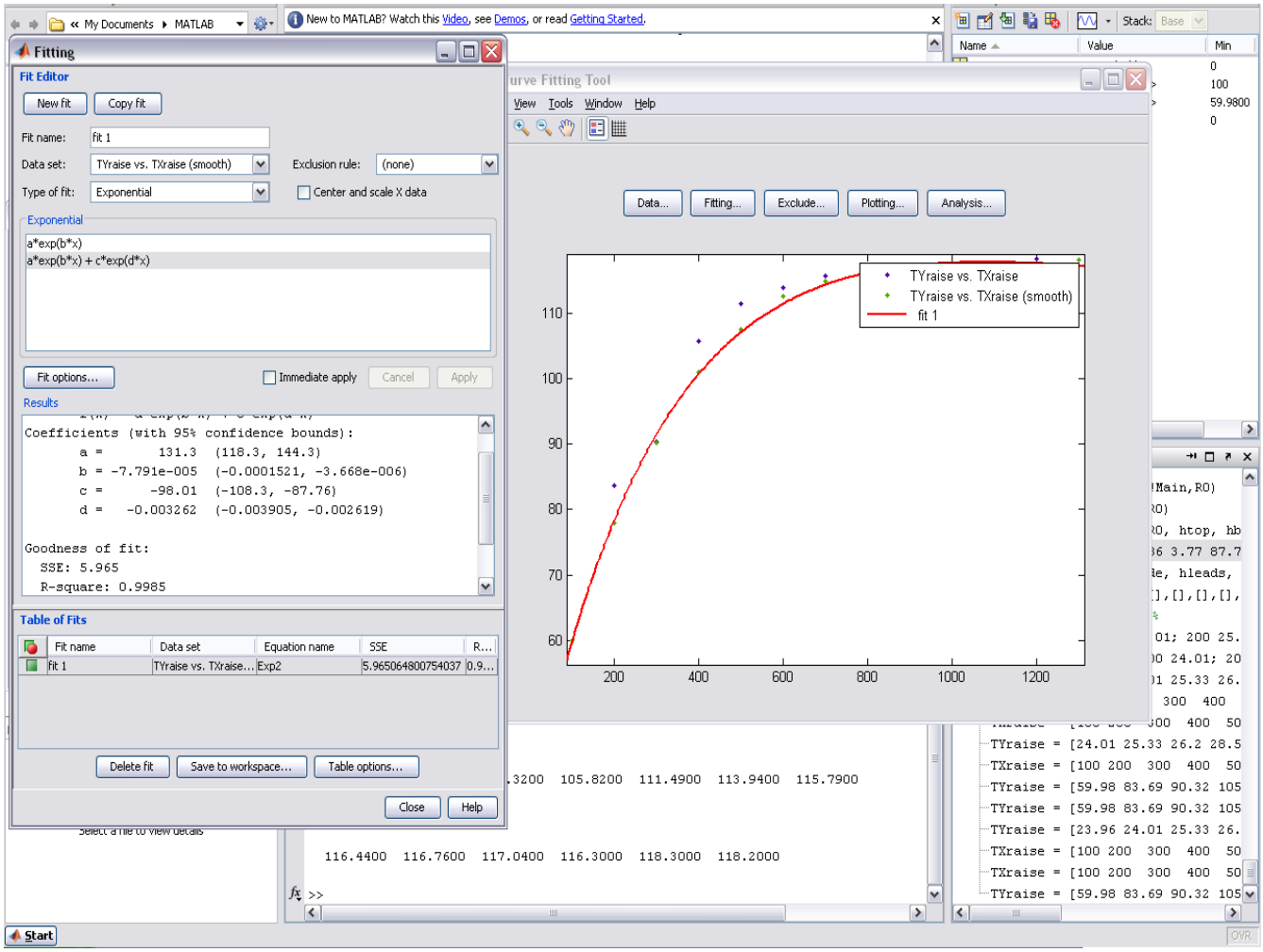


Figure 4.8: Process of Interpolation of the Temperature Profile to Find the Dynamic Compact Thermal Model of the BJT.

After using the curve fitting toolbox and by creating a smooth data set as shown in the figure 4.9, the exponential model could be derived as in equation (4.6) & equation (4.7) for two different conditions:

$$T(x) = 118.3U(t) - 98.01 * \exp(-0.003262 * x)$$

Or by regarding the real time instead of the x which represents the frames;

$$T(t) = 118.3U(t) - 98.01 * \exp(-0.10873 * t) \quad (4.6)$$

Using the equation (4.6), the value of the capacitor (C) under condition #1 would be **0.26598 J/K**.

Also for the 3rd column (second transistor) the temperature profile can be expressed as:

$$T(x) = 84.5U(t) - 64.31 * \exp(-0.003571 * x) \qquad (4.7)$$

As a result, the value of the capacitor (C) under condition #2 can be calculated as **0.24296 J/K**.
The obtained error for static and dynamic models was listed in the table 4.4.

Static Model (Resistor)	Static Model Error Comparing to the literature	Dynamic Model Condition #1	Dynamic Model Condition #2	Dynamic Model Error For two conditions
17.466 cm2·K/W	**8.39%**	**0.26598 J/K**	**0.24296 J/K**	**8.654%**

Table 4.4: Static and Compact Thermal Model for a BJT in Two Different Conditions of Different Ambient Temperatures.

It can be seen in the table 4.4 (second column) that the error between the value of the resistor obtained from the experimental data and available data from literature is less than 9%. In addition, comparing the two obtained capacitor's value for the dynamic mode as listed in the last column of table 4.4 is an indicator of the verification and consistency in the results for the dynamic model.

4.5 Summary

The feasibility study of generating the compact thermal model for a BJT ***2N3904*** was described. A Power BJT ***2N39014*** transistor was considered as the target device since the previous literature review on a simple test results were available and could be verified by the new methodology in this chapter. Thus, the obtained results for the static and dynamic compact thermal models using infrared camera (experimental data) were in good agreement with reported results in literature. Detailed explanation of the procedure of the generation of this compact model for a more complicated device is stipulated and an extension of the material of this chapter was applied for experiments on a BGA.

CHAPTER 5

Static & Dynamic Compact Thermal Model for a BGA

5.1 Introduction

The input data required to obtain a methodology to generate the static & dynamic compact thermal model under two/several applied boundary conditions are reported along with the simultaneous current/power measurements required for developing these compact models. After a literature review, the preparations of the boundary conditions are described. Parallel measurements and calculations regarding the power (consumption, generated) of the BGA (see figure 5.1) are also described. The thermal analysis and measurements are both performed by the infrared (IR) camera system's Researcher software and SDK. In addition, the results of the SDK are post-analyzed by the VISUAL C++ for ultimate use by MATLAB optimization process.

Similar to the 4th Chapter, first the static compact thermal model of the BGA is obtained, followed by the dynamic compact thermal model generation. The methodology to generate the compact thermal models is described for applied experimental boundary conditions based on the number of different maximum currents or different experiments to assess the performance of this methodology.

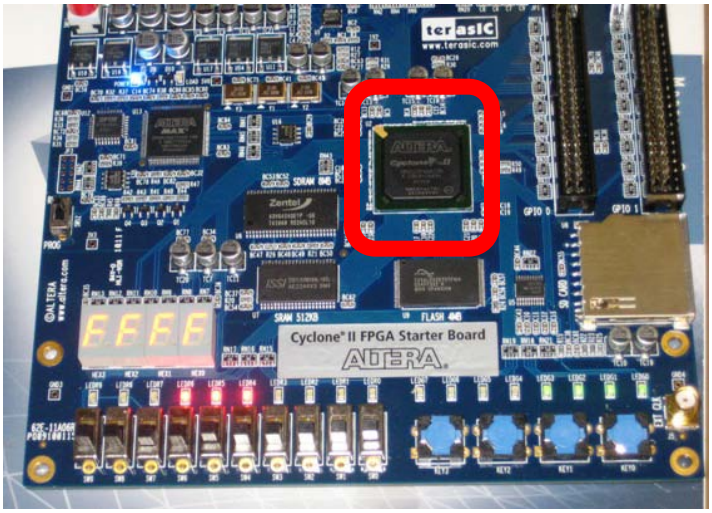


Figure 5.1: ALTERA FPGA is a BGA Electronic Package and Device under Test (DUT) Highlighted

5.2 Test Configuration

The instruction on implementation of Verilog and Quartus II codes were discussed briefly in Section 3.2 of Chapter 3. Two different sets of data (in terms of the temperature profile) were collected from the BGA (CYCLONE II FPGA Development Kit (ALTERA) [25, 34]) using two approaches: IR camera Researcher and the software development kit (SDK) of the IR camera, using Verilog and Quartus II instruction code. The experimental test configuration was identical to the one presented in Section 2.1.4 of Chapter 2. Selected parameters for the BGA test configuration is listed in table 5.1.

Configuration Parameter	Description
DC Voltage Supplier	7.5 Volts
IR Camera constants: Speed	30 f/s- 2700 frames
IR Camera constants: Pixels	320×256
IR Camera constants: Distance	30 cm
Oil Pump distance	30 cm, identical level
Heat-sink flow	Laminar
Fixed Emissivity	0.92
Average Ambient Temperature	23.3 °C

Table 5.1: Parameters for the BGA Test Configuration.

Although in table 5.1 the frame rates are still running at 30f/s speed for 320×256 pixel imagery, the distance from the object is reduced to 30 cm. The reason is to try to focus inside of the chip so that to occupy a bigger space of the screen by the DUT. Furthermore, based on [1] black paint spray was used to make the real emissivity close to the listed emissivity (0.92), with acceptable error. The fundamental use of an oil heat sink during the experimental efforts as a cooling system which also stabilizes the temperature distribution is a crucial portion in the test configuration. This was discussed in depth in 2.1.4.3.

The test results were collected based on the Quartus II codes. It offered lower time consumption of the coding process. Two different sets of schematics Quartus II codes were applied in these experiments to generate output data under different boundary conditions. The obtained results were referred as Load 1 and Load 3, contrary to No Load condition where the BGA was not programmed but the circuitry was in the active range. The schematic for a Load 3 is shown in figure 3.3.

5.3 Parallel Current/Power Measurements

There are two ways to calculate and/or measure the current or power related to the operating BGA. First, from the Power-Play Early power estimator [41] which is a customized file accompanied by the BGA as described earlier in Section 3.6 of Chapter 3. The other option is to find the power through the calculation and estimation of current/ power by measuring the total current of the board using LABVIEW software and reducing the illuminating LEDs power while at the operating mode. To understand better, this method is explained in this section and the first method was used as a verification process in the next chapter. Thus, considering the 7.5 volts fixed voltage of the board and the maximum current of 165.22 mAmps for the board during the third experiment the maximum total instance power of the board would be calculated as 1237 mW. This is not the current drained by the BGA due to the existence of the other electronic devices like LEDs 7segments and so forth, which are also active in the No Load mode according to the Section 3.2 and [21, 42, 43]. Hence, by deducting the No load power, it will be 1072 mW. This is close enough to the results for power of Load 3 estimated by the Power-Play power estimator. For Load 1 with a maximum current of 61.17 mAmps the power was obtained as 307.5 mW which is believed to be close enough to the verified results in the datasheet and would be discussed in the next Section (see Section 5.4).

Maximum current modes, with the calculated powers for each individual experiment and the respective maximum temperature values are listed in table 5.2.

Input Mode	**Maximum Current (m Amps)**	**Maximum Obtained Power of the BGA (m Watts)**	**Respective Maximum Temperature (°C)**
No Load	21.96	165	~27
Load 1 – Multiplier	61.17	307.5	~30
Load 2 & 3– Adder/Mux/Multiplier	165.22	1072	~35

Table 5.2: Maximum Current Generated by the BGA with Different Experiments.

5.4 Verification of Current/ Power Measurements

In previous section (Section 5.3), it was mentioned that one way to verify the current or power related to the operating BGA is from the Power-Play Early power Estimator [42]. This is Excel-based software, attached to the type of BGA purchased from the factory. It could be used to verify and estimate the power/ current and junction temperature of the BGA under test, according to some parameters used as test setup configuration in table 5.1. Environmental parameters such as the cooling system and the ambient temperature obviously has a great impact on the results as well as the quantity of different elements or electronic devices implemented in the FPGA such as different dimensional adders, multipliers, LEDs and so on. Two typical files for Load 1 and Load 3 experiments are shown in figure 5.2 and 5.3, respectively.

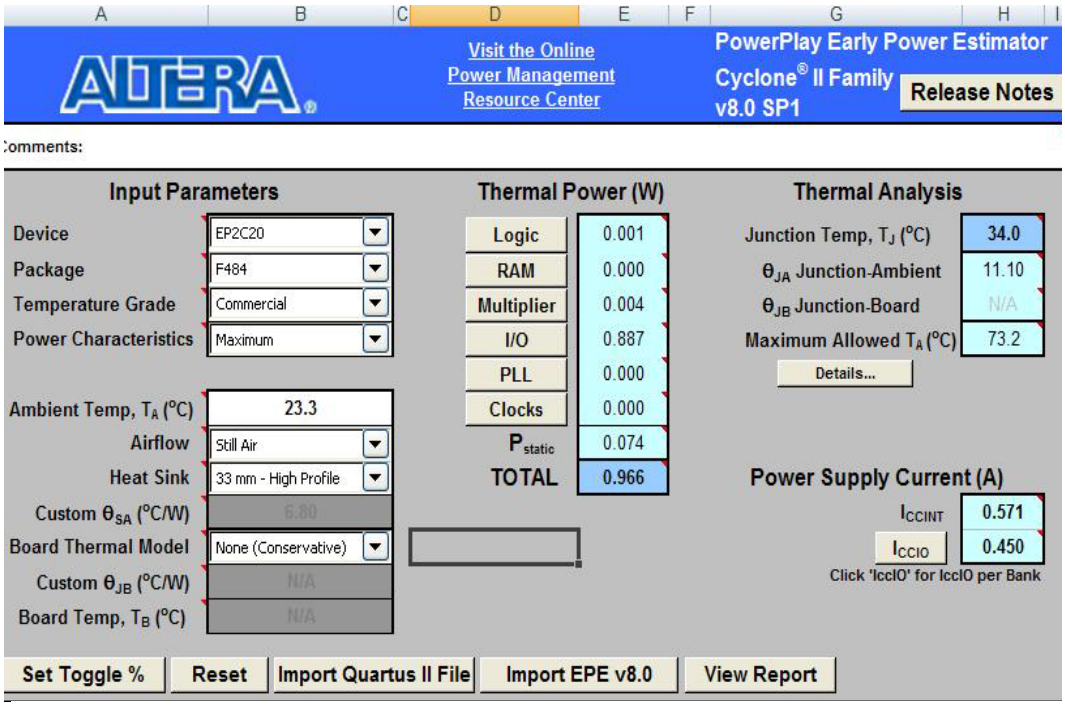


Figure 5.2: Power-Play Power Estimator different parameters for load 1.

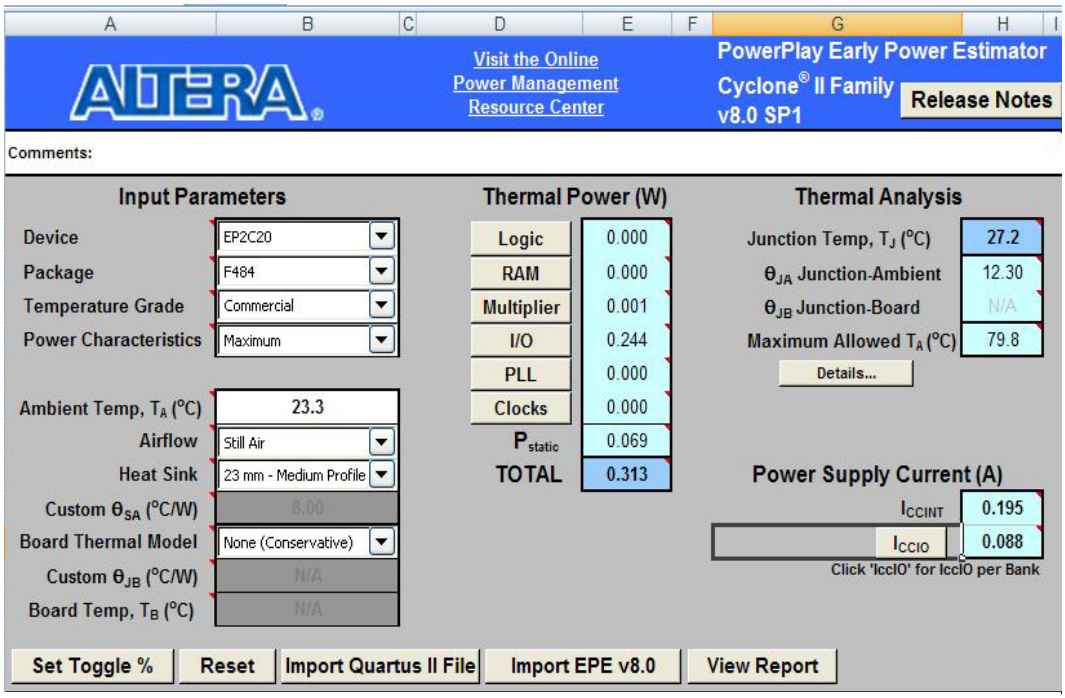


Figure 5.3: Power-Play Power Estimator different parameters for load 3.

The Maximum obtained power from table 4.2 has the slightest relative errors with the estimation of Power-Play Estimator as listed in table 5.3.

Maximum obtained power from the BGA in Load 1	Power-play Estimated Power for Load 1	Relative Error %	Maximum obtained power from the BGA in Load 1	Power-play Estimated Power for Load 1	Relative Error %
307.5 (m Watts)	313	1.75	1072	966	0.98

Table 5.3: Relative Errors of the Powers of BGA with the Estimation of Power-Play Estimator File.

These relatively small errors verify the calculations and assumptions and calculations methodology described in previous section (Section 5.3).

5.5 Static Compact Thermal Model Results for a BGA

Process of generating the compact thermal model for a BGA is illustrated in the flowchart of table 5.4. First the frames (figure 5.4) corresponding to the temperature profiles of the surface of the BGA are obtained via the SDK as explained in the Section 3.3.2. To perform the procedure of fetching the frames the software application of Visual C++ was used as described in Section 3.4. Basically, the developed program looked for the X and Y coordinates of a specific element (here the temperature of the junction spot) in a raw data file obtained by SDK.

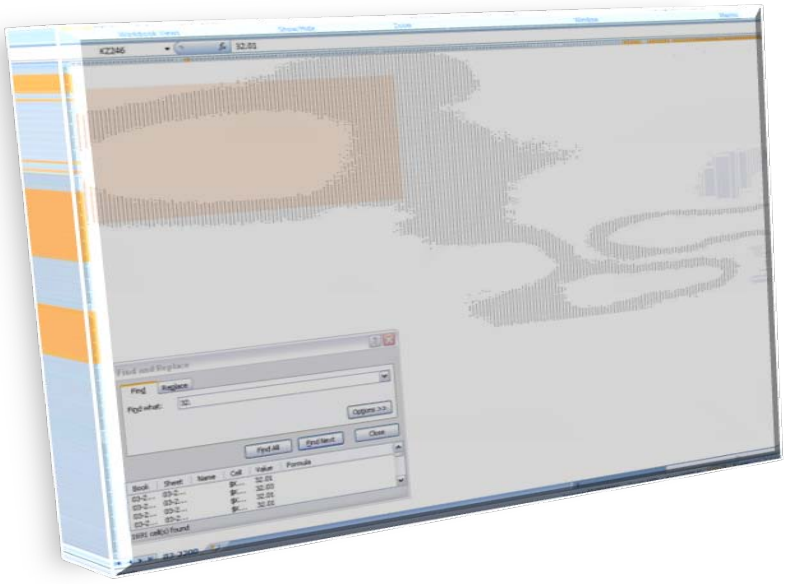


Figure 5.4: 2700 Frames for the One of the BGA Experiments Processed by the Visual C++.

In addition, a random sample frame no. 2200 from the total 2700 frames applied in this experiment is shown in the figure 5.4. The orange selection is the BGA's rectangle coordinates. The rest of the circuitry should not influence the analysis in terms of the data required for the detailed temperature profile. In other words, part of the detailed temperature data obtained by the SDK rests for the portions of the surface of the board that not only includes the BGA's surface, but also infringes the borders of it; thus, is useless in the generation of the compact thermal model.

In other words, the whole thermal compact analysis should be confined to the colored section of the figure 5.4 and all of the other frames in any individual experiment.Hence,

moving on to the next steps in the table 5.4 the estimated exponential function is obtained by applying the curve fitting toolboxes in MATLAB.

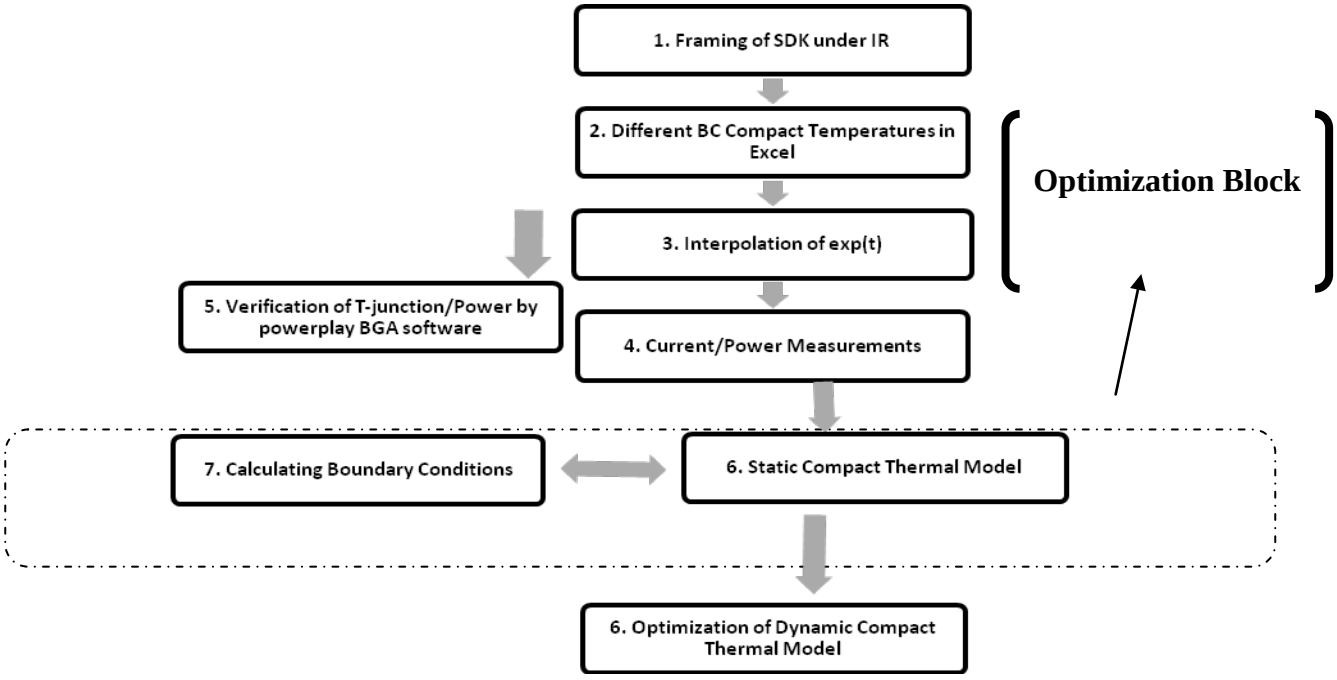


Table 5.4: Flowchart of Generating the Compact Thermal Model for a BGA.

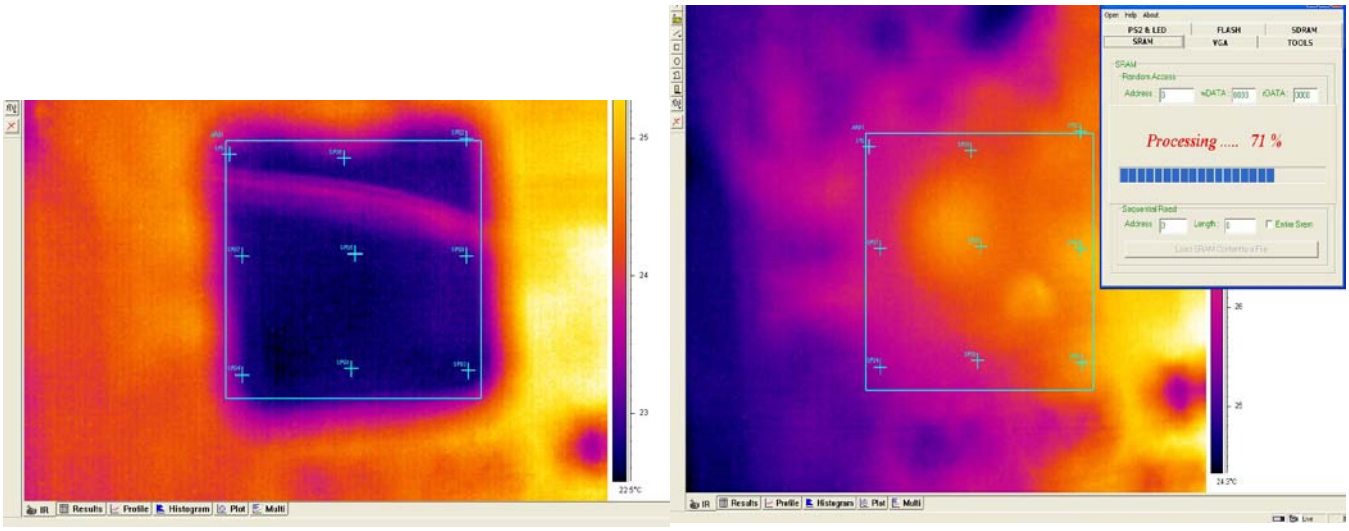


Figure 5.5: Transient Analysis of the BGA under Researcher; 2D Temperature Profile at t=0S, and as the 71% of the Implementation of the Instruction.

The 2D temperature profile at t=0s of the BGA running the third instruction is shown in figure 5.5. Via the Researcher (see Section 3.3). The rectangular coordinates are the exact coordinates of the BGA getting hotter continuously. Also this figure contains another snapshot during the experiment while implementing one of the instructions inside the FPGA in its 70% instance of the process. The contours can be easily compared to each other and would emphasize in the temperature dramatic change all over the board and the BGA. See Appendix I for more temperature profiles of the BJT & BGA under the Researcher at various times and various spots inside the BJT & BGA's coordinates.

To exemplify two of the cases on which the three experiments were performed, the temperature evolution of junction versus frame number of the BGA running the load case 1 and load case 3 is shown in figures 5.6(a) and (b), respectively.

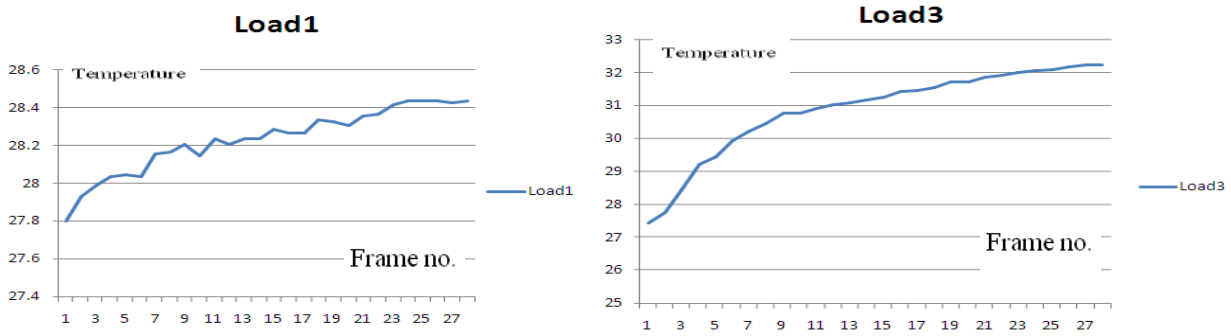
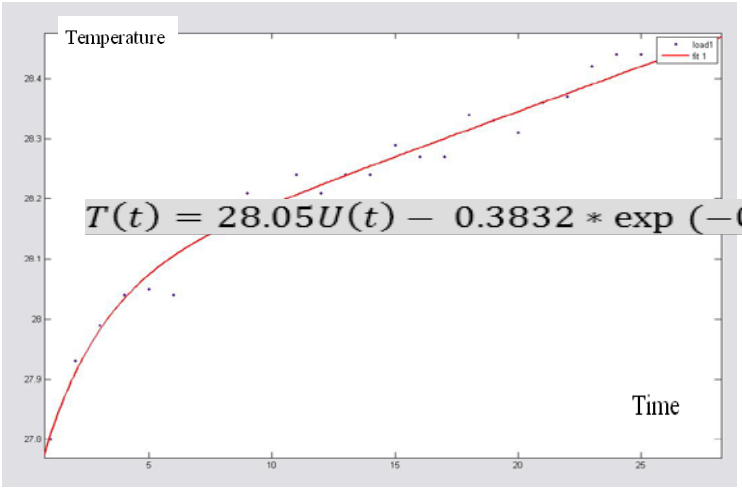


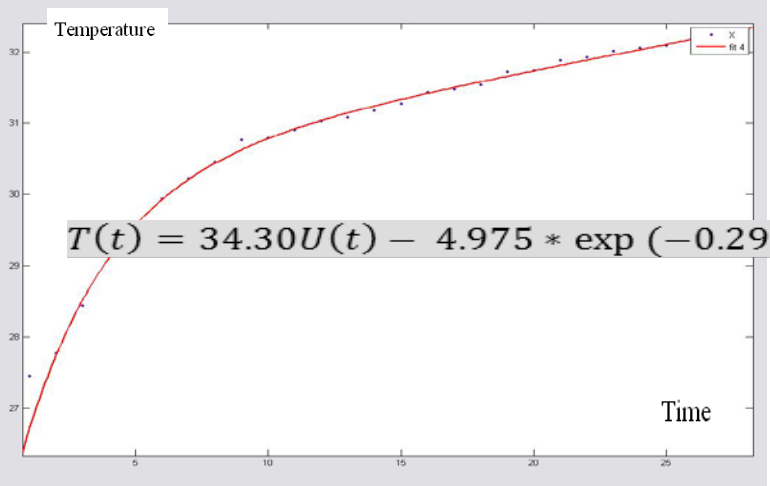
Figure 5.6: Diagrams of Temperatures of Junction for two Different Instruction Loads Vs the Frame no. (× 100).

examples of interpolation of Load 1 & 3 (a Multiplier and a Complicated Multi-Level Code) with the Curve Fitting Toolbox of MATLAB. So the X and Y axis of these figures correspond to time and the detailed junction temperature, respectively. The exponential result model for junction temperature is expressed in the following equations (5.1) & (5.2).



(5.1)

Figure 5.7: Interpolation of Junction's Temperature Profile for load 1.



(5.2)

Figure 5.8: Interpolation of Junction's Temperature Profile for load 3.

The resistor network approach was explained in Section 2.1.3.2. The general formula relating the voltages (temperatures) and currents (heat fluxes) of the electric network can be expressed as:

$$q_i = \sum_{k=0}^{N} Y_{ik}.T_k \tag{5.3}$$

In addition as discussed in Chapter 3 (Section 3.5.2) and Chapter 4 (Section 4.4) compact thermal model calculations is an optimization process which requires a cost function similar to:

$$COST_{SS} = \frac{1}{BC} \sum_{i=1}^{BC} (|T_j^d(\omega_k)| - |T_j^c(\omega_k)|)^2 \tag{5.4}$$

Equations (5.3) & (5.4) are the basis of the MATLAB optimization in the static mode and are applied in the optimization Toolbox as stated in Section 3.5.2. In fact, the equation (5.3) is the transformed version of equation (4.1), where q and T represent the power and temperature in each RC network element of the compact model, respectively. It's imperative to note that this is an experimental-based model and the temperature profile here is obtained by the infrared camera system. Thus the basis of the cost function is still the junction temperature differences between the detailed and compact model under each boundary condition can still be expressed by cost function

(equation (5.4)), similarly to the literature. Resistor network static compact model of BGA package shown in figure 5.9 was proposed by [1, 10]. The value of the admittance static matrix (Y) for the heat transfer equation (5.3) is listed in table 5.5.

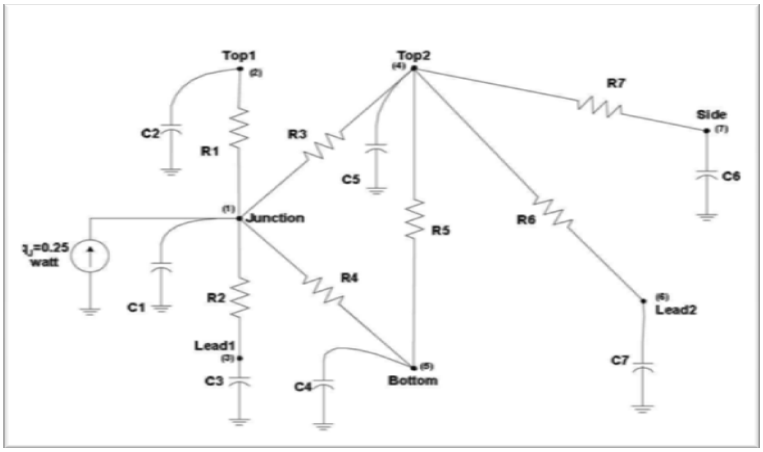


Figure 5.9: Compact Thermal Representation of a BGA.

Static Compact Thermal Model	
Resistor's Name	**Value** (K/W)
R_{JT1}	32.8
R_{JB}	402
R_{JT2}	66.6
R_{JL1}	4.86
R_{T2L2}	3.77
R_{T2S}	87.7
R_{T2B}	439

Table 5.5: Admittance Static Matrix for the Heat Transfer Equation.

Contrary to [1] in many other experimental works such as [11] and [12] the boundary conditions or the heat transfer coefficients are not applied; yet they are part of the computations and the model itself. The literature reviews in these cases have different approaches; for instance one of them assumes a temperature-variant complex heat transfer while the second one which is more popular, uses as fix heat transfer variant by the inherent characterizations of the BGA. In order to link main equations (5.3) and (4.1), equation (5.5) can be used. These convection boundary conditions are related to the heat transfer coefficients (manufacturing qualities) and couldn't be ignored of their role represented as natural or inherent resistors added to figure 5.9.) Nevertheless they can't be specifically measured or calculated, unless the model itself is obtained.

$$R \times h = \frac{1}{A} \quad h\left(W/m^2K\right) \tag{5.5}$$

Hence the only way to find h and R is to increase the number of experiments to have more equations and refining the guess via those equations. That's the reason, even in the static mode, an optimization problem is required and boundary conditions are linked to the number of experiments. MATLAB optimization toolbox nonlinear least squares (lsqnonlin) was applied with two different methods of Gauss-Newton and Levenberg-Marquardt Methods to get the desired results. Area specifications were also applied according to the table 2.1.

By using admittance static matrix values (listed in table 5.5) for the heat transfer equation, matrix h was derived as such; 58 fixed boundary conditions reported in [1] and the new power specifications were applied to find the junction temperature using equation (5.3) and were compared to the measured temperatures in the new experiments. The closest boundary condition to two reported experiments (see Section 3.2) was chosen, which occurred via the 48^{th} boundary condition. This process of finding a best suitable initiation point for the optimization problem according to the boundary conditions [1] is shown in figure 5.10 & 5.11. (For notations (htop, hbot, hside and hleads) see Section 2.4.)

[htop hbot hside hleads] = [1000; 50; 10; 500;]

Td = [312.4; 301.31;].

This was chosen as the first guess towards the real H matrix. Figure 5.7 & figure 5.8 show the temperature calculated by the equation (2.3) versus the items of 58 fixed boundary conditions according to [1]. These figures also show that by increasing the number of boundary conditions as in the same order of [1], the inherent resistance would drop which was mentioned before in equation (5.5), since the overall h is rising in this order. It is valuable to remind that according to the temperatures profile expressed in the equations (5.1) & (5.2) the real Td derived by the detailed model should converge to Td= [301; 307.3;] which was measured by the infrared camera and interpolated by MATLAB in these figures.

After this stage, an optimization block was designed to optimize the H and R matrixes recursive manner, until the differences to the previous elements or the ideal case is

negligible. Therefore, with this method, the H and R matrixes would be derived simultaneously. The MATLAB scribes are presented in Appendix III.

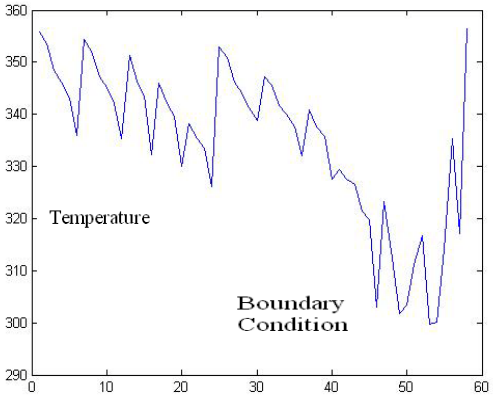


Figure 5.10: Applying 58 Boundary conditions to find the Initial H matrix for load 1; Temperature vs. # Boundary Condition.

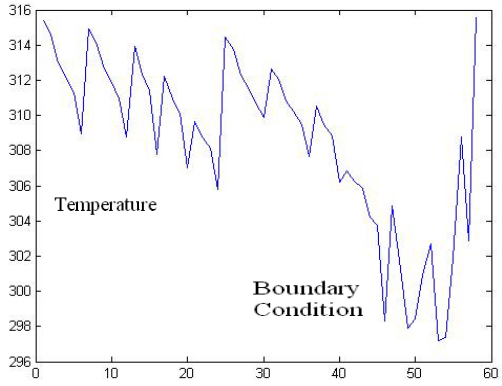


Figure 5.11: Applying 58 Boundary conditions to find the Initial H matrix for load 3; Temperature vs. # Boundary Condition.

The value of the Admittance static matrix for the compact model is:

[***54.353; 116.34; 106.56; 4.87; 3.77; 87.7; 4.39;***].

The first three elements of R had been chosen to be unknown since three total different experiments were acquired.

The optimization process or refining of the boundary conditions process is shown in figure 5.12. The difference between the detailed matrix of temperature profile and the temperature profile results from the equation (5.3) is the standard for the static compact thermal model, exactly as in the [1]. This complex computational comparison would be performed numerous times in MATLAB loops until it converges (theoretically it could diverge) to a desired value less than a desired cost function. In the same process the other unknown set of the problems which was the H matrix or the boundary condition would be guessed and found during the optimization process. It should be reminded that the reason that the optimization is applied here instead of the direct method of finding the unknowns according to the number of equations is that the number of the unknowns are more than the known equations. One of the contributions of this study is replicating such a method with the same procedure each time with a hypothetical H and unknown set of R and improving R and then doing the reverse direction by acquiring the new set of R as the initiation point and finding the new H, until both converge with

a reasonable error. By applying this method, a recursive optimization block of H and R is generated which self-optimizes itself. As mentioned earlier, all of the MATLAB codes for such a block would be shown in Appendix III. Thus, figure 5.12 shows this left to right procedure which converges after four optimizations. In each optimization step shown by the arrow, the blue blocks in the end of the arrow show the improved and the ultimate obtained H or R matrix; while the white blocks in the beginning of the arrow, show the starting point as a fixed value and old H or R matrix.

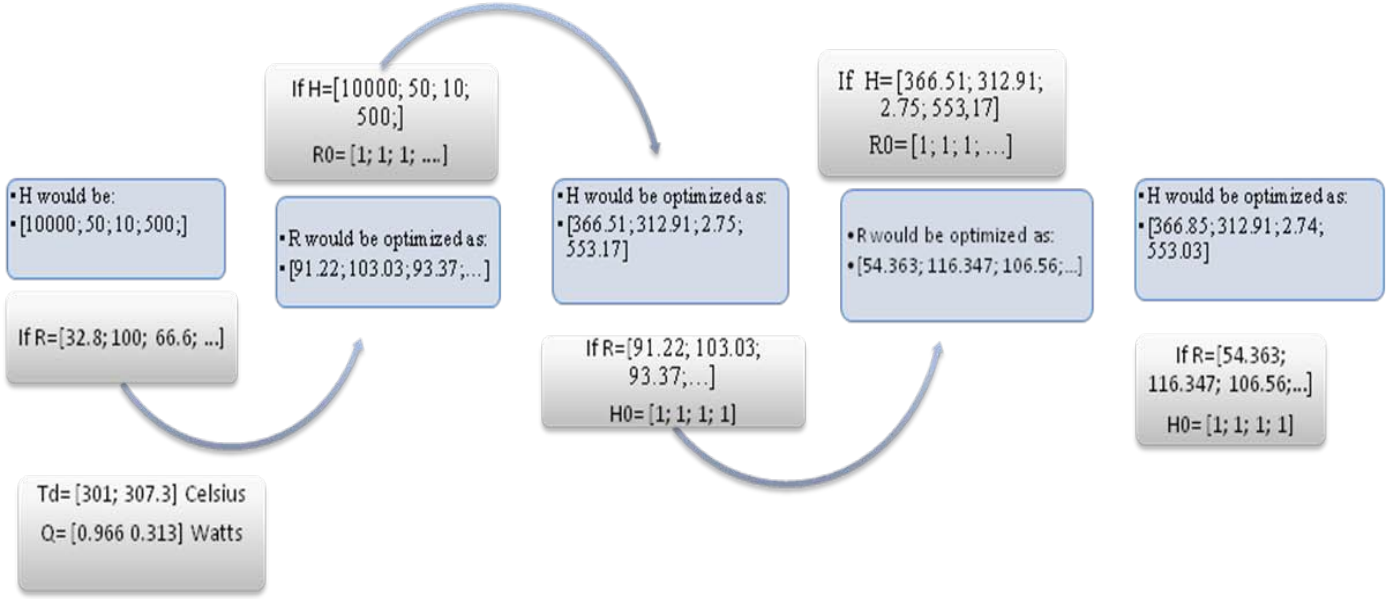


Figure 5.12: Optimization Block and Boundary Condition Refinement Using MATLAB Optimization Toolbox.

5.6 Dynamic Compact Thermal Model Results for a BGA

Equations (5.6) & (5.7) are the basis of the MATLAB optimization to generate the dynamic mode1. 'P' is the power in each link of thermal resistance network; 'T' is the temperature in that node.

The thermal resistance network shown in figure 5.9 could be proposed as the compact thermal representation. The values of matrix [C] for the heat transfer coefficient in the equation (5.6) are obtained from the simulation results and are listed in the table 5.6 [1].

$$[T(\omega)] = (j\omega[C] + [G])^{-1}[P(\omega)] \tag{5.6}$$

$$COST_D = \frac{1}{BC}\sum_{i=1}^{BC}\sum_{k=1}^{Samples}\left(T_{J_i}^{c}(k) - T_{J_i}^{d}(k)\right)^2 \tag{5.7}$$

The procedure to obtain and verify [C] matrix is similar to the static model with a slightly difference in performing all the calculations on equations in fast Fourier transform mode using MATLAB and then optimizing equation (5.7) in 512 samples from the transient time. Also note that the new transformed version of the equation (5.3) would be equation (5.6). The R and H matrix inside the G would be applied as known in these formulations. Therefore the only challenge to keep the optimization's error as desired is for the extra summation in equation (5.7). This would make the computations longer due to the number of samples (512) in the temperature profiles.

Capacitor	Value (J/K)	Description
C_1	0.10284	Junction Capacitor
C_2	0.0415	Top1 Capacitor
C_3	0.0015	Lead1 Capacitor
C_4	1.8057	Bottom Capacitor
C_5	0.00042	Top2 Capacitor
C_6	0.0327	Side Capacitor
C_7	0.00024	Lead2 Capacitor

Table 5.6: Capacitors' value of Dynamic Compact Thermal Model

It is important to note that equation (5.7) only uses the magnitude of T in the frequency domain to optimize cost function in the dynamic mode.

The capacitance dynamic matrix results for the dynamic compact thermal model with 3 unknowns and 3 experiments were obtained as:

[***0.088; 0.026; 1.8057; 0.0015; 0.00042; 0.04; 0.00024***],

whereas the initial values for the first, second and the sixth elements which were unknown were chosen as 0.1 [J/K].

According to the values measured by the optimization block in the last round, the cost function (absolute value) related to H and R matrix are 1.18e-5 and 4.268e-6, respectively.

A summary of the resistors' and capacitors' values of dynamic compact thermal model is listed in table 5.7.

Admittance Static Compact Model (K/W)	**54.353**	**116.34**	**106.56**	**4.87**	**3.77**	**87.7**	**4.39**
Capacitance Dynamic Compact Model (J/K)	**0.088**	**0.026**	**1.8057**	**0.0015**	**0.00042**	**0.04**	**0.00024**

Table 5.7: Static & Dynamic Compact Thermal Models for a BGA Obtained.

It is essential to note that table 5.7 shows one of the applicable RC networks which was generated by this work. In theory there are many different models which might not be close in their elements together at all. It is crucial that where the starting point for the optimization is and what the values of the detailed junction temperatures are. Therefore, the elements for the static model are not close to the table 5.5 (and shouldn't be necessarily) in [1] while the perturbations of the current CTM listed in the next section are satisfactory (around 17%).

5.7 Effect of Small Perturbation

The relative and absolute error of the DCTM under small perturbation was also studied. These errors are listed in table 5.8.

Turbulence of 10% into Capacitors for DCTM	**[*0.088; 0.026; 1.8057; 0.0015; 0.00042; 0.04; 0.00024*]**	**Sum of Absolute Cost Function via Equation (4.7)**	**Sum of Relative Error %**
First Capacitor	[***0.097; 0.026; 1.8057; 0.0015; 0.00042; 0.04; 0.00024***]	4.6011	23.01%
Second Capacitor	[***0.088; 0.029; 1.8057; 0.0015; 0.00042; 0.04; 0.00024***]	4.2852	23.82%
Third Capacitor	[***0.088; 0.026; 1.9957; 0.0015; 0.00042; 0.04; 0.00024***]	4.2843	17.56%
Fourth Capacitor	[***0.088; 0.026; 1.8057; 0.0016; 0.00042; 0.04; 0.00024***]	4.2843	17.55%
Fifth Capacitor	[***0.088; 0.026; 1.8057; 0.0015; 0.00046; 0.04; 0.00024***]	4.2843	17.56%
Sixth Capacitor	[***0.088; 0.026; 1.8057; 0.0015; 0.00042; 0.044; 0.00024***]	4.2843	23.81%
Seventh Capacitor	[***0.088; 0.026; 1.8057; 0.0015; 0.00042; 0.04; 0.00026***]	4.2843	17.56%

Table 5.8: Dynamic Compact Thermal Model Absolute and Relative Errors with a Known Turbulence.

It can be observed from this table that the optimization process has optimized and stabilized the values for the first, second and the sixth capacitors in a way that a very small perturbation would increase the relative error with a larger extent. This also approved the values obtained as the dynamic compact thermal model and shows that the rest of the capacitors haven't been minimized and could be minimized with more experiments. Further application of this methodology for layout selection is briefly discussed in Appendix II.

5.8 Summary

A methodology to generate the static & dynamic compact thermal model under two/several applied boundary conditions for a ball grid array (BGA) package using experimental data are reported. The simultaneous current/power measurements required for developing these compact models are also discussed. The duality between the thermal and electrical capacitance was employed and resistor network was expanded by adding some capacitors so it can predict the dynamic thermal behavior of the BGA package. The dynamic model thus is a RC network.

CHAPTER 6

Conclusions and Future Work

A methodology for generation of static and dynamic compact thermal model using an experimental infrared measurement technique was presented. This method was applied for a Ball Grid Array (BGA). The methodology was based on previous studies over generating such models via numerical simulation techniques. In this work, coupling the IR thermography measurement with the optimization process to generate a compact thermal model was performed. The experimental setup is capable of performing steady state and transient analyses.

The optimization process was developed by using an optimization block in order to calculate and optimize the boundary conditions required for the compact thermal modeling, simultaneously with the static model itself (set of resistors). When the static model was verified with the test results in the current experiments results the dynamic model was performed in a similar methodology.

The feasibility study of generating the compact thermal model for a power BJT 2N3904 was performed. Comparison of the resistor and capacitor value obtained for the static and dynamic CTM model of BJT with reported results in literature was within the maximum relative error of 9%. In addition, validation of experimental results was performed by comparing the temperature profiles in a numerous clusters of spreadsheet files obtained by the IR camera to the simulated and optimized static and dynamic compact models.

The static (resistor network) & dynamic (resistor/capacitor) compact thermal model under two/several applied boundary conditions for a ball grid array (BGA) package using

experimental data were obtained. The study of the relative and absolute error of the DCTM under small perturbation indicated a maximum

The obtained results were satisfactory knowing that there were limitations in the experimental equipments and some simplifications were considered, such as, the heat transfers were considered constant during the experiments and the toolboxes of MATLAB applied for the interpolation, data fitting and calculating the different defined errors were not perfectly matched with reality.

Electronic package thermal analysis and compact modeling is an increasingly popular research area in the fields of electronic packaging, MEMS, and consumer electronics. The future works in this area is trying to improve the performance of dynamic CTM. This may be done by modeling the package using transmission lines rather than lumped resistors and capacitors. Another suggestion is investigating on the effect of surface allocation to the compact model nodes. It was also observed that, if the equipment is well-organized, the major time consumer of the generation of the CTMs is the optimization part which would make the methodology a big leap towards future works in this area. The notion of reducing the data required as the layout area properties has a huge impact in the process of DCTM generation via infrared camera system.

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Appendix I

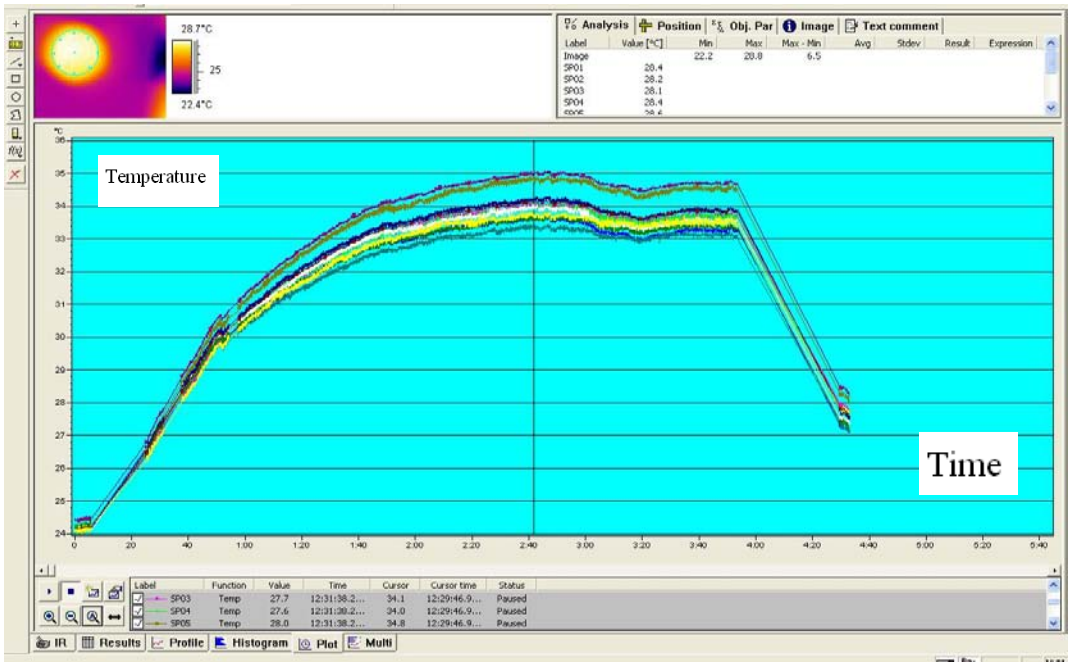

Figure I.1: Measured BJT Temperatures for 10 cm distance from the First BJT; Identifying Maximum Temperature for Points 3, 4, 5 on the Surface. See Figure 4.2.

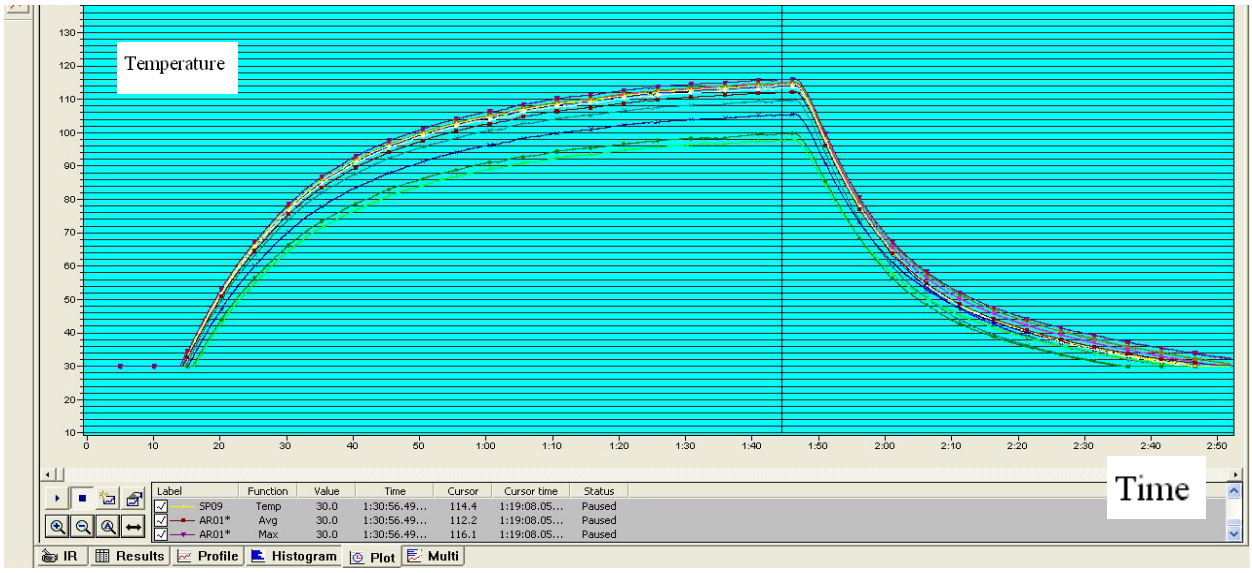

Figure I.2: Measured BJT Temperatures; Identifying its Rise and Fall Vs Time.

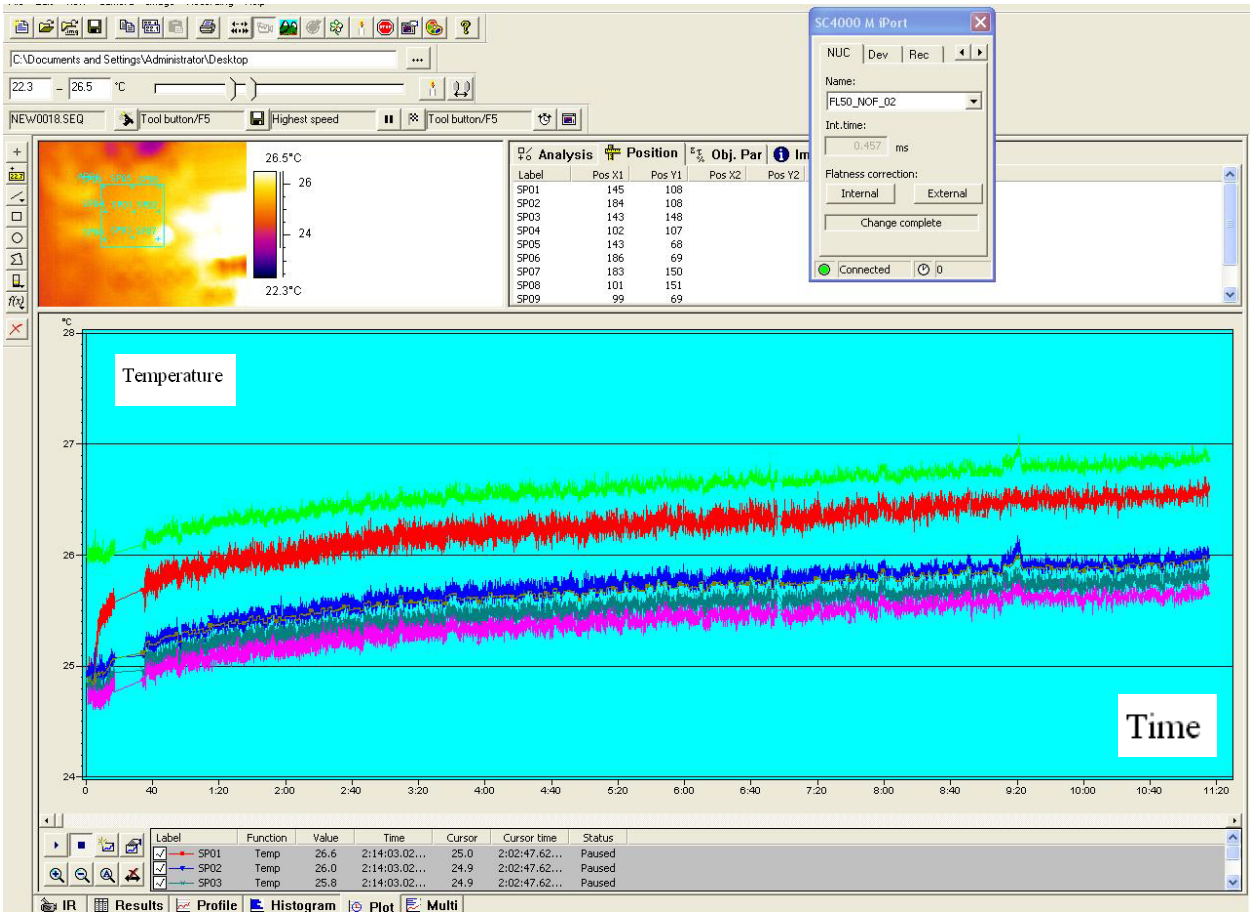

Figure I.3: Measured BGA Temperatures; Identifying the Visible Noise due to Less Variance in Temperature.

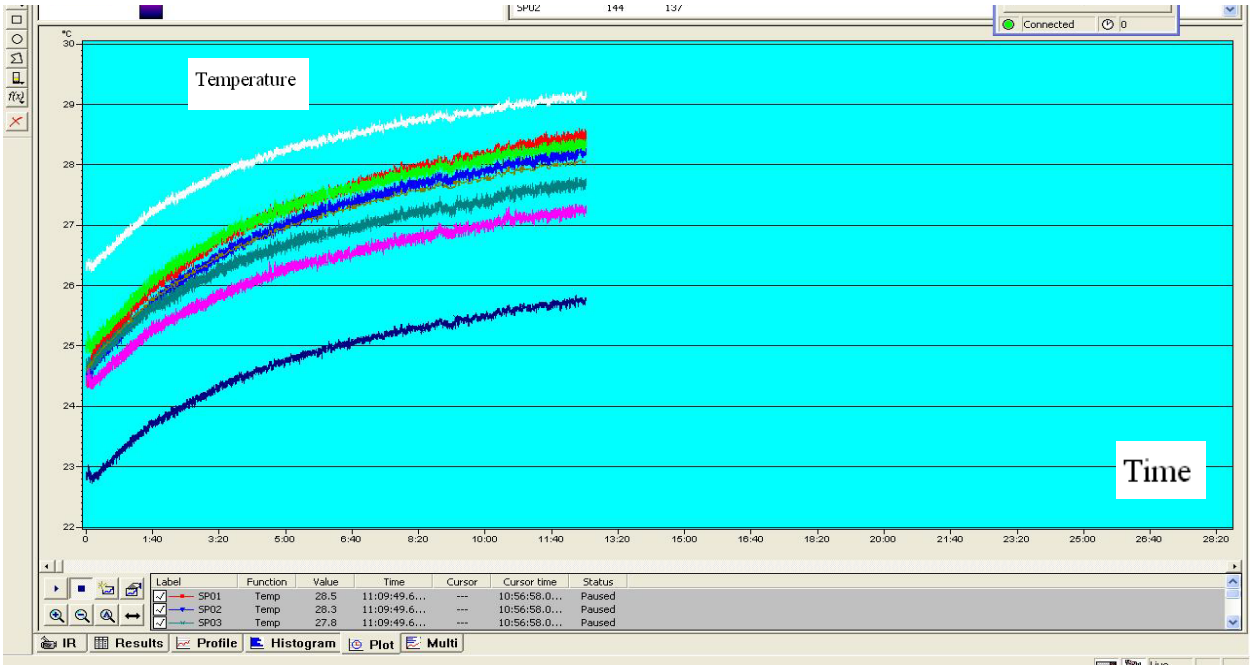

Figure I.4: Measured BGA Temperatures in different spots (See Figure 5.5); identifying Less Noise due to More Variance in Temperature.

Appendix II

The holistic view of the IR camera with SDK is shown in figure 1. The comparison may be perormed between the BGA size and the top level size of the board which was not acquired by the datasheet or specifications of the BGA. Measuring through the number of cells in a proportional method, the proportional area of the top level (in pink) in figure 2 is around (28/100 × 38/100) which would be **0.01064** of the whole area of the BGA. While in the table 2.1 the same proportion of area for the top level relative to the whole BGA could be calculated as **0.103** which are close with holds just a **3.3%** relative error. This is simply part of the capability of the current methodology to predict at least in this case some more information regarding the competence of the chosen layout model.

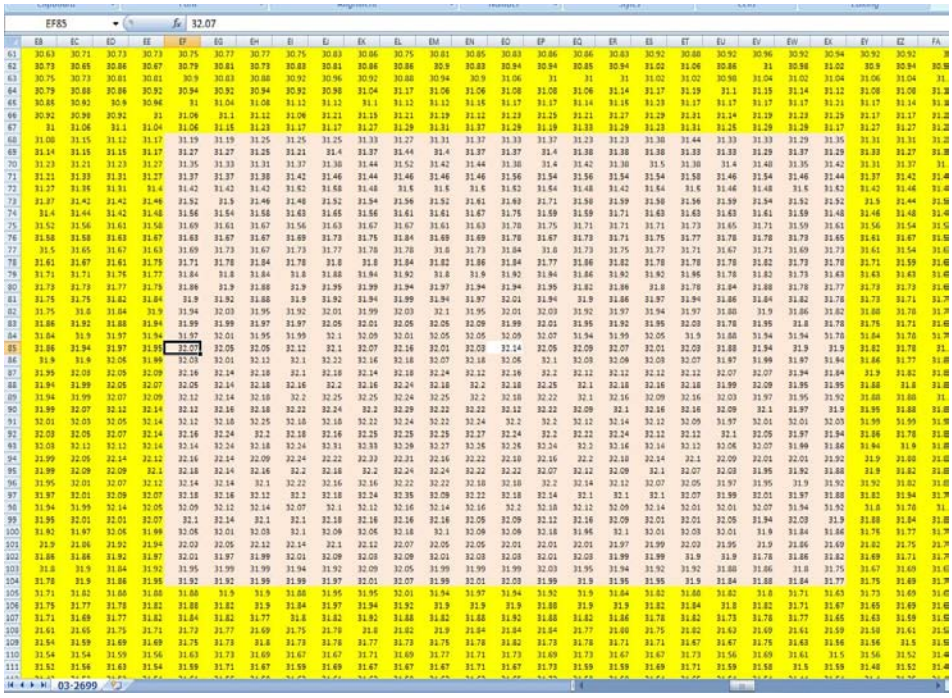

Figure II.1: View of the BGA under the IR Camera with SDK and the Junction Estimated

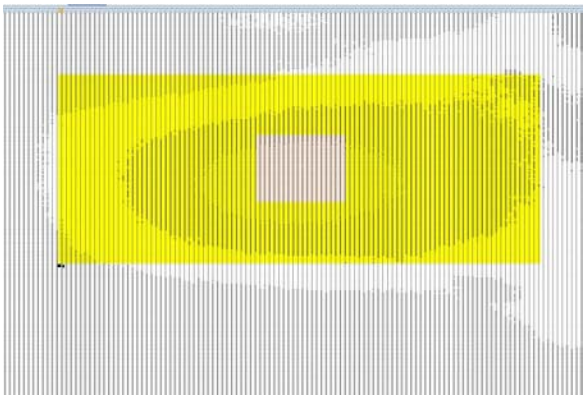

Figure II.2: Holistic View of the Board with the BGA in it under the IR Camera with SDK.

Appendix III

```
function Temp= Temp(C1, C2, C3, C4, C5, C6, C7)
%RT1=ones(length(htop));
%RL1=ones(length(htop));
%RT2=ones(length(htop));
%RL2=ones(length(htop));
%RB=ones(length(htop));
%RL2=ones(length(htop));
%RS=ones(length(htop));
%Temp=ones(length(htop));
htop= 366.5140;
hbot= 312.9179;
hside= 2.7520;
hleads= 553.1787;
%htop= 1000;
%hbot= 1000;
%hside= 1000;
%hleads= 1000;

RJT1=54.353;
RJB=116.34;
RJT2= 106.56;
RJL1= 4.87;
RT2L2= 3.77;
RT2S= 87.7;
RT2B= 4.39;
Q=[0.966 0.313;0 0;0 0;0 0;0 0;0 0;0 0;];

%for k=1:length(htop)

RT1=1/(htop*4.12e-5);
RL1=1/(hleads*2.5e-5);
RT2=1/(htop* 3.58e-4);
RB=1/(hbot* 7.5e-5);
RL2=1/(hleads*3e-4);
RS=1/(hside*6.6e-5);

%Using more complicated problem by adding uknown parameters of Area;
when the layout is not clear.
%RT1(i)=1/(htop(i)*Atop1);
%RL1(i)=1/(hleads(i)*Alead1);
%RT2(i)=1/(htop(i)* Atop2);
%RB(i)=1/(hbot(i)* Abot);
%RL2(i)=1/(hleads(i)*Alead2);
%RS(i)=1/(hside(i)*Aside);



G = [1/RJT1+1/RJT2+1/RJB+1/RJL1 -1/RJT1 -1/RJT2 -1/RJL1 -1/RJB 0 0;...
-1/RJT1              1/RJT1+1/RT1  0       0    0   0 0;...
-1/RJT2 0 1/RJT2+1/RT2B+1/RT2L2+1/RT2S+1/RT2   0  -1/RT2B -1/RT2L2 -
1/RT2S;...
-1/RJL1               0    0     1/RJL1+1/RL1   0   0 0;...
```

```
-1/RJB                0   -1/RT2B  0   1/RJB+1/RT2B+1/RB 0 0;...
0                   0    -1/RT2L2      0     0   1/RT2L2+ 1/RL2
0;...
0                   0    -1/RT2S 0     0   0 1/RT2S+1/RS;];

%G = [1/RJT1+1/RJT2+1/RJB+1/RJL1 -1/RJT1 -1/RJT2 -1/RJL1 -1/RJB 0;...
%-1/RJT1              1/RJT1  0       0    0   0;...
%-1/RJT2 0 1/RJT2+1/RT2B+1/RT2L2+1/RT2S 0  -1/RT2B -1/RT2S;...
%-1/RJL1               0    0     1/RJL1   0   0;...
%-1/RJB                0   -1/RT2B  0   1/RJB+1/RT2B 0;...
%0                   0    -1/RT2S 0     0   1/RT2S;];

C= [C1 0 0 0 0 0 0;...
    0 C2 0 0 0 0 0;...
    0 0 C3 0 0 0 0;...
    0 0 0 C4 0 0 0;...
    0 0 0 0 C5 0 0;...
    0 0 0 0 0 C6 0;...
    0 0 0 0 0 0 C7;];

%A= inv(G)*Q;

for k=1:27
Y= (1i*2*pi*k*C*0.3+G);

Y=Y\Q;

Temp(k,1)= abs(Y(1,1));
Temp(k,2)=abs(Y(1,2));

%Temp(k)= Y(1,1)+296;
%Temp(k+1)=Y(1,2)+296;

%Temp=Temp(:,1);

end

end
```