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3.3V Transmitter Using 1.8V Transistors In A Cascode Configuration

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1.8V TRANSISTORS IN A

CASCODE CONFIGURATION

By

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A project
presented to Ryerson University
in partial fulfillment of the
requirements for the degree of
Master of Engineering
in the Program of
Electrical and Computer Engineering
Toronto, Ontario, Canada, 2013

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3.3V TRANSMITTER USING 1.8V TRANSISTORS IN A CASCODE CONFIGURATION

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Abstract

A voltage-mode transmitter using a 1.8V-to-3.3V levelshifter and cascoded output buffer is proposed.

1.8V TSMC 65nm transistors are used. The design is targeted to meet JEDEC Interface Standard for

Nominal 3 V/3.3 V Supply Digital Integrated Circuits DC Specifications as well as an AC transmission rate

of 200 MHz on a 30 cm 50Ω board trace terminated with a 4 pF capacitive load. Overstress voltages will

not be exceeded in order to avoid device failure due to breaching Gate Oxide Integrity, Hot Carrier

Injection, or Negative Bias Temperature Instability.

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1   Introduction

Today's device geometries continue to scale downward as Gordon E. Moore predicted in 1965, enabling higher performance per unit area and power consumption. The operational voltage for these ever-shrinking devices also continues to scale downward into the sub-1V region in order to gain more speed and lower power consumption. However, many System-on-a-Chip (SoC)'s I/O interfaces still have to support legacy specifications. These specifications often signal at voltage levels much higher than the core voltage of these devices. Example specifications are shown in the table below.

IO Standard	Supply Voltage
3.3V LVCMOS [1]	
PCI-33/PCI-66 [2]	
I2C [3]	3.3V
MMC [4]	
SSTL3 [5]	

Table 1: Supply Voltage of Legacy IO Specifications

In order to support a signaling level of 3.3V, there are generally two approaches. The simplest approach is to use 3.3V-tolerant transistors as the second gate-oxide device, where the overstress voltage for gate-to-source, gate-to-drain, and drain-to-source is >3.3V. This allows for the simplest design. However, the poor performance and large area they require renders them unusable for building analog IP needed in a given design. Thus, higher performance devices are needed which leads to the use of second gate-oxide devices with smaller gate lengths. As gate lengths shrink, maximum V_{gs} also shrinks [6] (as can be seen in Figure 1 below).
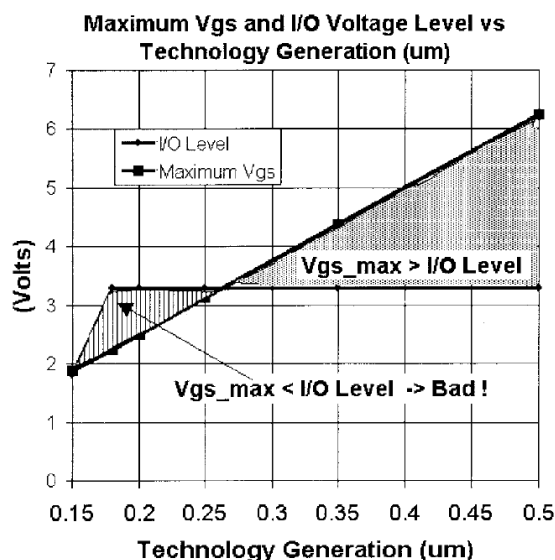
Figure 1: Gate-Oxide Breakdown and I/O Level vs. Technology Generation

Currently, ASICs are built on dual gate-oxide processes where the second gate-oxide support an overstress voltage of 1.8V, and adding 3.3V-tolerant devices would be prohibitively expensive, owing to the fact that any company choosing such a process would likely be in the minority. Besides cost, another good reason to choose a popular process is that foundries tend to commit significant resources to perfecting processes which produce the highest volumes, likely at the cost of resources available to low-volume alternatives. Thus, the predominately popular solution is to cascode (stack) two devices in series such that any one device would never see an overstress condition. The main drawback of this approach is the need for a bias voltage to the gate of the second device in the stack to ensure that the overstress voltage condition does not occur to V_{gs}, V_{gd}, or V_{ds}.

1.1 Device failure

CMOS transistors are fabricated to perform nominally up to a maximum voltage difference between gate and source, gate and drain, and drain and source. The process used for this project is Taiwan Semiconductor Manufacturing Company's (TSMC's) 65nm GP process, which is a dual gate-oxide process. This means two different devices are available: a 1.0V core device and a 2.5V-underdrive-1.8V I/O device. Exceeding these voltages will result in shortening their lifetime. The design in this paper refers mainly to the use of the second gate-oxide (1.8V) devices and their maximum overstress voltage is unfortunately not shown in any formal document. Typically, the foundry will ascertain this information through statistical analysis and determine a value for a given area and lifetime and provide it internally to their customer(s). For the purposes of this paper, an overstress voltage of 2.1V will be used.

1.2 Mechanisms for Device Failure

1.2.1 Gate Oxide Integrity (GOI)

GOI is the ability of the gate oxide in a CMOS device to withstand the stress induced by an electric field which is created when a gate voltage is applied. Simply applying a gate voltage in normal operation will begin to degrade the device. However, TSMC rates their transistors to operate at the rated voltage and temperature (<65⁰C) for 10 years. Exceeding the rated voltage and/or temperature will begin to shorten device lifetime. TSMC provides the following Gate Oxide Lifetime prediction model [7]:

$$Time\ to\ Failure \sim (V_{CC})^{-n} \times exp\left(\frac{E_a}{kT}\right) \times (A_{OX})^{-1/\beta}$$

where

A_{OX} is the total gate oxide area on silicon (unit: μm²)
T is the absolute junction temperature (unit: K)
V_{CC} is the gate voltage (unit: V)
n is the power law exponent for core thin gate oxide
E_a is the thermal activation energy
k is the Boltzmann constant ($8.617 \times 10^{-5}\ cV/K$)
B is the Weibull shape factor (distribution spread)

When an electric current is passed through the gate oxide of the transistor, defects such as electron traps, interface states, positively charged donor-like traps, etc. gradually build up in the gate oxide until a conduction path is established. This is followed by thermal run away and device failure. According to the anode hole injection model [8] [9] [10], injected electrons generate holes at the anode that can tunnel back into the oxide. Intrinsic breakdown occurs when critical hole density is reached.

1.2.2 Hot Carrier Injection (HCI) Effect and Negative Bias Temperature Instability (NBTI)

In the formation of a MOSFET transistor, gate oxide is grown over the silicon channel. At the silicon-to-oxide interface, some of the Si bonds remain dangling and can act as interface traps which can lead to poor device characteristics. Thus, another step is added to the manufacturing process in which the transistors are annealed with hydrogen atoms so that Si-H bonds form and the traps are eliminated. However, as device sizes continue to miniaturize, oxide thickness shrinks. This and process modifications such as using nitride oxides to prevent boron penetration of the poly-gate have led to accelerated Si-H bond breakage at the interface over time during device operation. The newly created traps shifts threshold voltage, reduces channel mobility due to scattering, and induces parasitic capacitances. These effects lead to a reduction in drain current and thus poor device performance. The most important mechanisms which break the Si-H bonds are HCI [11] and NBTI [12].

1.2.2.1 Hot Carrier Injection Effect

HCI occurs when electrons attain a very high kinetic energy while accelerated in the channel's lateral electric field. These energetic carriers can be injected into normally forbidden regions of the device (e.g. gate oxide) and once there they can break Si-H bonds and become trapped. The trapped charges from HCI stress can have the following effect on the transistors:

1. Shift in device threshold voltage (V_t)
2. Reduced mobility of conducting carriers
3. Reduced device drain current
4. Increased effective series resistance, from a charge trapped above the S/D extension region
5. Degraded sub-threshold slope

HCI is a major degradation effect in NMOSFETs. To avoid, or at least minimize hot carrier degradation, several device design modification can be made. These are for example a larger channel length, double diffusion of source and drain, and graded drain junctions to name a few.

TSMC provides the following model for predicting the lifetime of device degradation due to HCI [7]:

$$MTTF = A \times f\left(L, W\right) \times \left(\Delta\%\right)^{1/n} \times exp\left[B \times \left(\frac{1}{V_{ds}}\right)\right] \times exp\left(\frac{E_a}{k} \times \frac{1}{T}\right)$$

where:

$MTTF$ is the mean time to failure
L is the drawn channel length (unit: μm)

W is the drawn channel length (unit: μm)

$\Delta\%$ is the percentage of degradation of an electrical parameter (e.g. 10% I_{DSsat})

V_{ds} is the drain to source bias (unit: V)

n is the power law factor of time dependent degradation

E_a is the activation energy

k is the Boltzmann constant (8.617 × 10⁻⁵ $^{cV}/_{K}$)

T is the absolute junction temperature (unit: K)

A and B are empirical fitting parameters

1.2.2.2 *Negative Bias Temperature Instability*

NBTI occurs in negatively biased transistors at elevated temperatures. Inversion layer holes tunnel into the oxide and their interaction with passivated Si atoms can break Si-H bonds and leave behind interface traps while the associated H atoms diffuses away from the Si-Oxide interface. NBTI will change device characteristics by increasing threshold voltage, decreasing the drain current, and decreasing transconductance.

TSMC provides the following model for predicting the lifetime of device degradation due to NBTI [7]:

$$MTTF = A \times f(L, W) \times (I_{dsat}\%)^{1/n} \times exp[-\gamma \times V_g] \times exp\left(\frac{E_a}{k} \times \frac{1}{T}\right)$$

where:

$MTTF$ is the mean time to failure

L is the drawn channel length (unit: μm)

W is the drawn channel length (unit: μm)

$I_{dsat}\%$ is the criteria of I_dsat degradation percentage

n is the power law factor of time dependent degradation

V_g is the operation gate bias (unit: V)

γ is the voltage acceleration factor

E_a is the activation energy

k is the Boltzmann constant (8.617 × 10⁻⁵ $^{cV}/_{K}$)

T is the absolute junction temperature (unit: K)

A is a constant

1.2.3 Testing

Compliance testing of production ASICs for GOI, HCI, and NBTI, can be done according to the JEDEC/FSA Foundry Process Qualification Guidelines Document JP001.01 [13]. Models for various stress tests are outlined in [14].

2 Design

2.1 Simulator

All designs for this project was simulated using the Cadence Virtuoso Design Environment software package version IC6.1.5.500. The simulator used is Spectre. Model files used are provided by TSMC.

2.2 Transmitter

A typical voltage-mode transmitter consists of signals which enter the I/O cell powered off the core power domain. A levelshifter block will translate these signals into the 1.8V power domain. The data will then need one more translation to the 1.8V/3.3V domain in order to properly control a PMOS device in the Output Buffer. This block is called a Pre-Buffer. Finally, the Output Buffer is used to drive a (typically large) off-chip load in the 3.3V domain. This is the proposed design for this project (Figure 2).
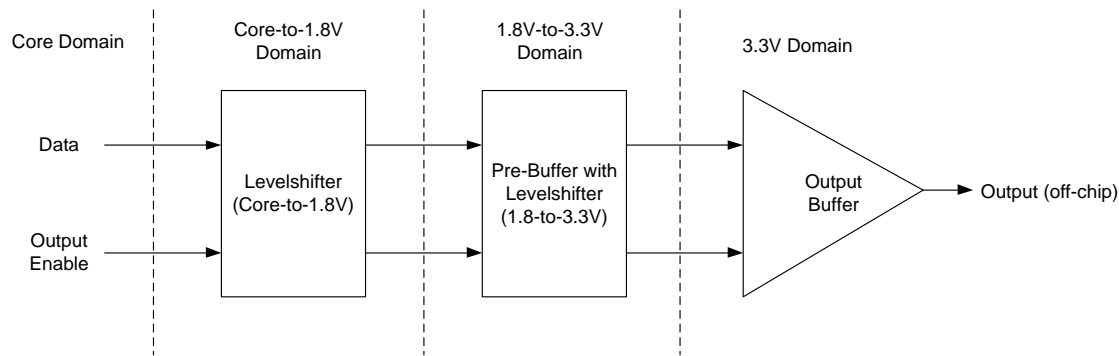
Figure 2: Typical 3.3V Transmitter Topology

In designing each major sub-block of the GPIO, a set of specifications will be defined. In many cases, the specification will be taken directly from the JEDEC Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits Document [1]. Some blocks may not have a relevant specification from the JEDEC document, thus the specifications used will be defined by the designer.

2.2.1 Output Buffer

The output buffer stage of the transmitter is built using 2 PMOS and 2 NMOS devices connected in a cascode configuration. As explained previously, this configuration is chosen due to the lack of availability of 3.3V-tolerant devices at this node.

The following is the circuit schematic for the output buffer:
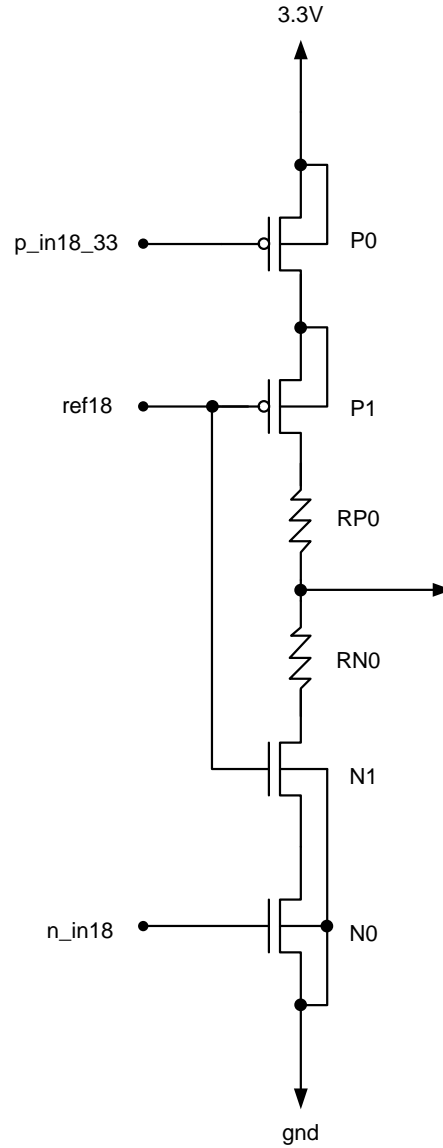
Figure 3: Output Buffer

The PMOS input signal 'p_in18_33' will swing from 1.8V – 3.3V while the NMOS input signal 'n_in18' will swing from 0V – 1.8V.

2.2.1.1   ref_18 Generation

In order to keep the $|V_{sg}|$ voltage for all transistors within the 2.1V over-voltage tolerance, the gate voltages of transistors P1 and N1 are biased with a 1.8V reference. This reference can be generated in a variety of ways, including:

1.   a resistor network voltage divider from 3.3V,
2.   a diode network voltage divider from 3.3V [6],

3. a Feedback Circuit which generates a complementary signal from PAD which is then coupled back to ref_18 through small capacitors to oppose initial coupling effect on ref_18 due to a PAD transition [15],
4. a small resistor connected to 1.8V with a decoupling capacitor to ground.

A resistor network voltage divider can create this reference from the 3.3V rail. There are two drawbacks with this approach. First, there will be static current consumption through the divider. In order to keep this current small, a large impedance is needed, which leads to the second drawback. Since P1 and N1 are typically large (as they are in series with their respective cascoded devices), there is a large Miller capacitance from the drain to the gates of P1 and N1. This large parasitic capacitor will couple the high frequency components of the fast switch edge during output buffer transitions onto 'ref_18'. This, in turn will change overall output impedance of the buffer and cause jitter on the output signal. To decouple 'ref_18' from this, a decoupling capacitor can be added. However, as shown in [15], the needed capacitance is more than 9 times the C_{gd} of P1 and N1 combined.

A diode network voltage divider can also create the 1.8V reference from the 3.3V rail [6]. This will also consume static current during mission mode although the author adds a sleep functionality to the circuit in order to turn off this bias while it is in a low-power non-operational state.

A feedback circuit shown in [15] is an interesting and effective approach to reduce the amount of noise coupled onto 'ref_18' while using significantly less area than adding a large decoupling capacitor. However, for brevity, simplicity, and effectiveness this paper will choose solution 4, seen below in Figure 4. A small resistor will provide a low impedance path to AC ground (1.8V) for the high frequency components of the fast switch edge to dissipate while providing ESD protection to the gates of N1 and P1. The decoupling capacitor will also aid in stabilizing the reference node. The drawback of the large decoupling capacitor (large area consumption) has been previously explained, but in this solution there is no dc current consumption (as opposed to the resistor voltage divider in solution 1).
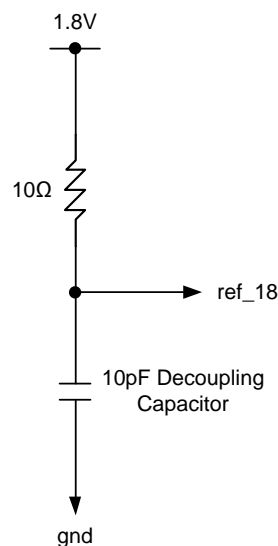
Figure 4: ref_18 Generator

2.2.1.1.1 Simulation

The Maximum and minimum value of 'ref_18' is measured with the transmitter is toggling at 200 MHz. The results are tabulated in the following table:

ref_18	TT 50˚C (V)	SS 110˚C (V)	FF 0˚C (V)	Variance (%)	Notes
Min	1.62	1.64	1.66	-10%	1.8V Rail at Nominal
Max	1.90	1.89	1.91	+6.1	1.8V Rail at Nominal

Table 2: Min and Max Values of ref_18 During 200 MHz Transmission

These results show that the V_{gs} and V_{gd} voltages for P1 and N1 do not exceed the maximum voltage overstress level of 2.1V.

2.2.1.2 Output Buffer Impedance Considerations

The variance of 'ref_18' will affect the impedance of P1 and N1 since it will change the $|V_{gs}|$ of those devices. The change in the impedance of P1/N1 can be mitigated by selecting the value of a resistor RP0/RN0 to account for a large portion of the target impedance. So, for example, for the target impedance of 50Ω, the selected resistance of RP0 is 40Ω. Thus, P0 and P1 (and subsequently N0 and N1) will account for roughly 10Ω of the output impedance. Assuming this is split evenly, each transistor will be ~5Ω. If the change in P1's $|V_{sg}|$ is 200mV, this may change its impedance by 20%, which will be ~1Ω, thus affecting the overall impedance by 2%. This amount is well within the range of impedance mismatch that the output buffer will see due to Process-Voltage-Temperature (PVT) corner variation.

2.2.1.3 Output Buffer Design Objectives

2.2.1.3.1 Recommended Operating Conditions

Before beginning the output buffer design, the operating conditions for the circuit must be defined. This design will follow the recommended operating condition specified in the JEDEC Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits Document [1]. These conditions are summarized in the following table:

Power Supply Range	Symbol	Narrow Range	Normal Range	Extended Range
Nominal Supply Voltage	V_{DDR}	3.3V	3.3V	3.0V
Rail Power Supply Voltage	V_{DDR}	3.15V to 3.45V	3.0V to 3.6V	2.7V to 3.6V
Reference Power Supply Voltage	V_{DD18}	-	1.71V to 1.89V	-

Table 3: Recommended Operating Conditions

2.2.1.3.2 DC Specifications

In sizing the devices in the Output Buffer, certain specifications are targeted. First, a DC impedance of 50Ω is targeted. This is done in order to match the characteristic impedance Z_0 of a typical board trace and minimize reflections. Both the PMOS pull-up driver and NMOS pull-down driver will target this

impedance. It should be noted, however, that 50Ω can only be met in 1 PVT corner. The sizing of devices will therefore be done such that 50Ω is met at the TT, 50°C, nominal voltage corner. Impedance will be higher in slow corner and lower in fast corner.

Secondly, the design will aim at the DC specification from the JEDEC Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits Document [1], which is shown in the following table:

Symbol	Parameter	Test Condition	Min	Max	Units
V_{OH}	Output High Voltage	V_{DDR} = min, IOH = -100 µA	$V_{DDR} - 0.2$		V
V_{OL}	Output Low Voltage	V_{DDR} = min, IOL = 100 µA		0.2	V

Table 4: LVCMOS Output Specifications

2.2.1.3.3   DC Impedance

There are several considerations with regards to Output Buffer impedance:

1. How is DC impedance measured?
2. How much of the impedance is attributed to transistor vs. resistor and why?
3. Electrostatic Discharge (ESD) consideration?

How is DC impedance measured?

DC impedance is measure with the PAD node set to half rail voltage (Figure 5). This is an industry standard practice. Specifically, it is calculated as the ratio of V_{PAD} to I_{PAD}. Note that the I-V characteristic for a transistor is not linear, as illustrated by the fact that a transistor's I-V curve is not a straight line. Thus, it is considered a best practice to size the transistor in such a way that the impedance target is met at half way between the power rail and ground with the reasoning that if, for example, it was tuned to the target impedance close to rail, its corresponding impedance when close to ground would be substantially greater, thus having the most error. It is interesting to note that during a transition, the 'ON' path transistors' dc operating point will traverse the I-V curve as V_{ds} decreases as they start in saturation and end in triode.
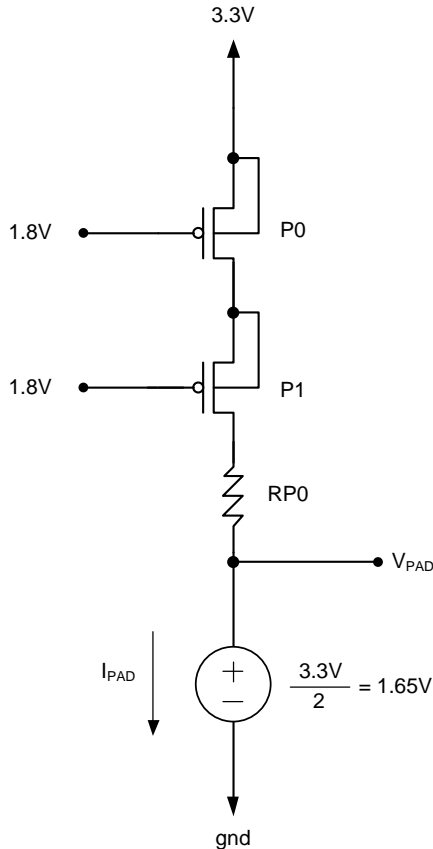
Figure 5: PMOS Output Impedance Testbench for Nominal Corner

How much of the impedance is attributed to transistor vs. resistor and why?

Considering that the current path during a transition exists between PAD and either power or ground, the impedance of the 'ON' path will be through transistors in series with a resistor. While a resistor I-V characteristic is linear, a transistor's $I_{ds} - V_{ds}$ characteristic is not. This means that the impedance value of the 'ON' path does not have a static value. In order to improve the linearity of this path, it is wise to attribute a significant portion of the target 50Ω to the resistor. A larger resistor will lead to larger (width) transistors because the 'ON' impedance of a transistor lowers when it is sized larger. The larger transistors are more apt to survive device failure due to electromigration (EM) as their EM rating increases with size. Also, the number of contacts and vias and the amount of metal used to connect to the larger transistors will aid in increasing EM survivability.

The benefit of keeping the impedance variance small during a switching event is that it will help keep reflections from transmission line effects to a minimum. This is important since in the JEDEC Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits spec, there is no termination at the destination. Thus, if the source impedance matches Z_0, the incident voltage wave will travel down the transmission line at half the rail voltage, reflect fully when it reaches the destination and the reflected wave will traverse back to the source where it is fully absorbed by the 50Ω source impedance (this acts as a termination to AC ground).

Electrostatic Discharge (ESD) Consideration?

Electrostatic Discharge is the sudden flow of electric current between two objects caused by contact, an electrical short, or dielectric breakdown. In general, an ESD zap to an IC will go through the I/O pins as they provide the connection to the outside world. Thus, I/O circuits need to properly conduct a large amount of current over a short amount of time and prevent circuits from seeing a high voltage to sensitive nodes which, if the voltage was high enough, can cause device failure. The TSMC 65nm design document [7] specifies a minimum device size for both PMOS and NMOS transistors to ensure ESD survivability. These rules include: $L_{min} \geq 0.2um$ (ESD.26g), $W_{min} \geq 360um$ (ESD.24g/25g), and unit fingers width = 15um (ESD.3g). However, because only 2.5V-underdrive-1.8V devices are available in the CLN65GP process (Section 12.1.4 in [7]), $L_{min} = 0.26um$ for these devices, which satisfies the ESD requirement.

With the previous 3 considerations in mind, the following table shows the sizes of the devices in the Output Buffer.

Device	L (um)	W (um)	Unit Finger (um)	Impedance (Ω)
P0/P1	0.26	720	15	4.38
RP0	1	18.56	4.64	41.33
RN0	1	15.76	3.94	48.78
N0/N1	0.26	360	15	0.66

Table 5: Output Buffer Device Sizing

2.2.1.4   Simulation Results

2.2.1.4.1   Impedance over PVT

The follow table is the Output Buffer Impedance for 3 PVT corners. Again, 50Ω was targeted for TT 50°C only.

Corner	TT 50˚C	SS 110˚C	FF 0˚C	Note
Pull-up Impedance (Ω)	50.1	61.8	40.1	Voltage Rails at Nominal
Pull-down Impedance (Ω)	50.1	60.9	40.5	Voltage Rails at Nominal

Table 6: Output Buffer Impedance

Impedance results across all corners are found in Table 12 and Table 13 in Appendix A – Simulation Results.

2.2.1.4.2   Linearity

As mentioned before, by attributing a significant portion of the pull-up/pull-down impedance to the resistors, the impedance variance would be kept to a minimum. This is shown in the following plot generated by sweeping the voltage at PAD and measuring the impedance.
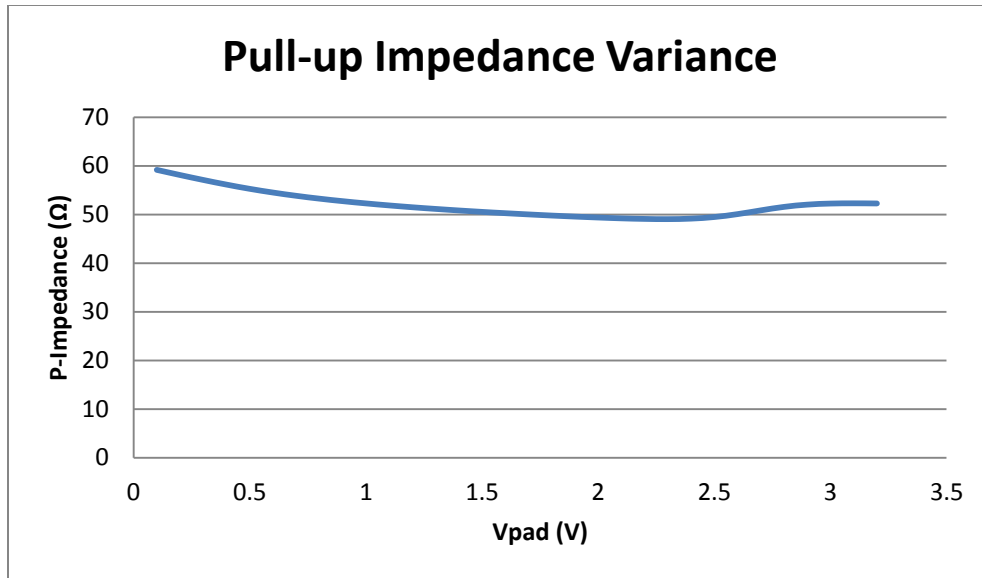
Figure 6: PMOS Buffer Impedance Variance

It can be seen that the impedance varies from approximately 49Ω to 58Ω. One point of interest is that form 0 to 2.5V, the impedance decrease but after 2.5V it starts increasing. This is due to the fact that the PMOS transistors make a transition from saturation to triode mode at 2.5V. A similar exercise can be used to show the pull-down impedance of the Output Buffer.
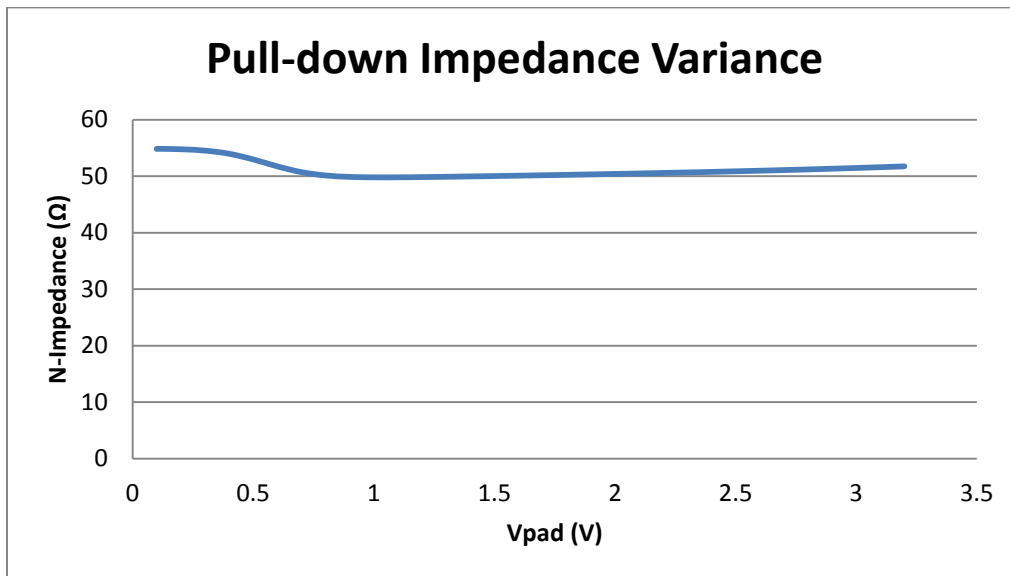
Figure 7: NMOS Buffer Impedance Variance

2.2.1.4.3   Output Buffer DC V_{OH}/V_{OL} Measurements

As outlined in the JEDEC Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits Document [1], V_{OH} and V_{OL} are measured against a current source of 100 uA. Figures Figure 8 and Figure 9 show the testbenches for measuring these parameters.

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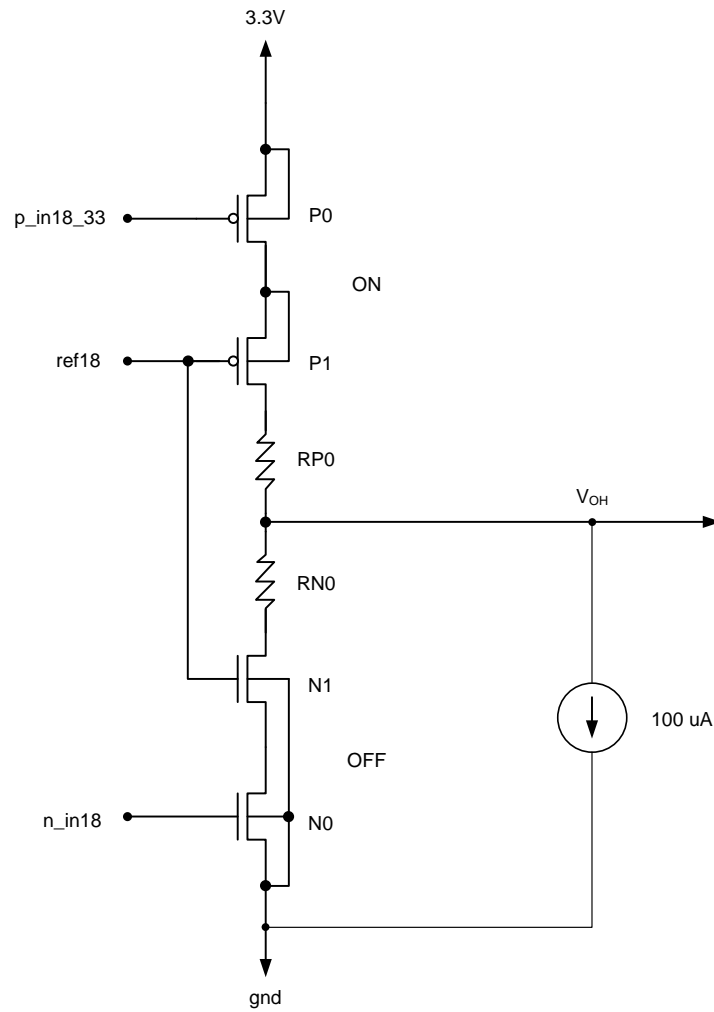
Figure 8: Testbench for Measuring V$_{OH}$
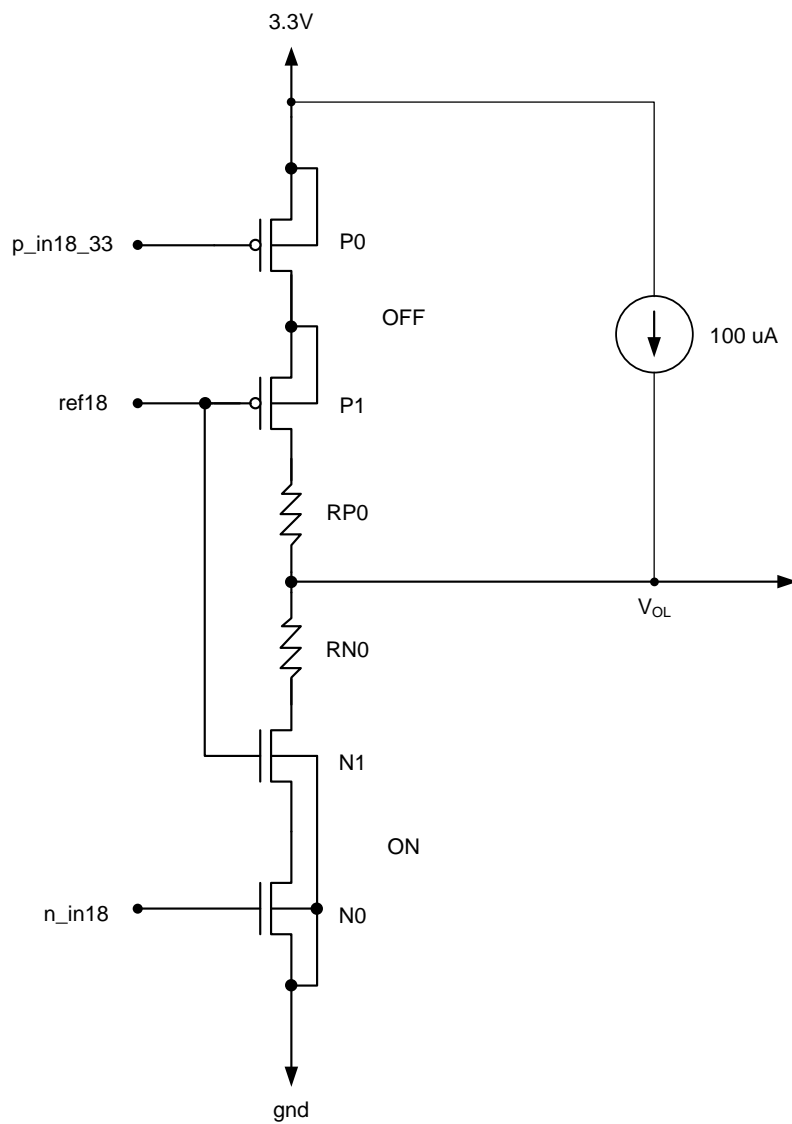
Figure 9: Testbench for Measuring V$_{OL}$

The following table are the results of the measurements. Note that they these number pass the JEDEC spec.

Corner	TT 50˚C	SS 110˚C	FF 0˚C	Note
V$_{OH}$ (V)	2.965	2.964	2.965	V$_{DDR}$ = 2.97V
V$_{OL}$ (V)	0.0048	0.0050	0.0045	V$_{DDR}$ = 2.97V

Table 7: Output Buffer V$_{OH}$/V$_{OL}$ Measurements

Complete results are shown in Table 14 and Table 15 in Appendix A – Simulation Results.

2.3 1.8V-to-3.3V Levelshifter

2.3.1 Background

Along the data path, it is necessary to levelshift data from the $0V - 1.8V$ domain to the $1.8V - 3.3V$ domain. This levelshifted signal will control the gate P0 in Figure 3 and is labeled 'p_in18_33'. There are a couple approaches to the design of such a levelshifter. The first is a full-swing transistor network [6] [16] and the second is a dynamically biased differential amplifier [17]. These are shown in Figure 10, Figure 11, and Figure 12 respectively. Both earn the distinction of preventing overstress conditions on all devices.
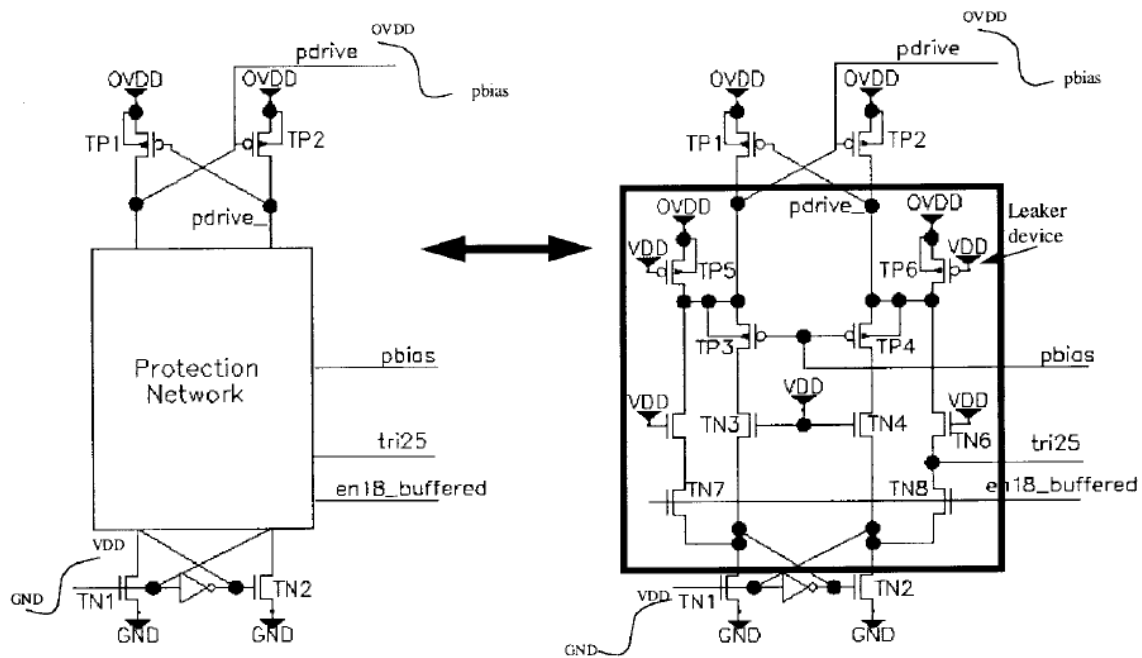
Figure 10: Full-Swing Transistor Network Levelshifter [6]
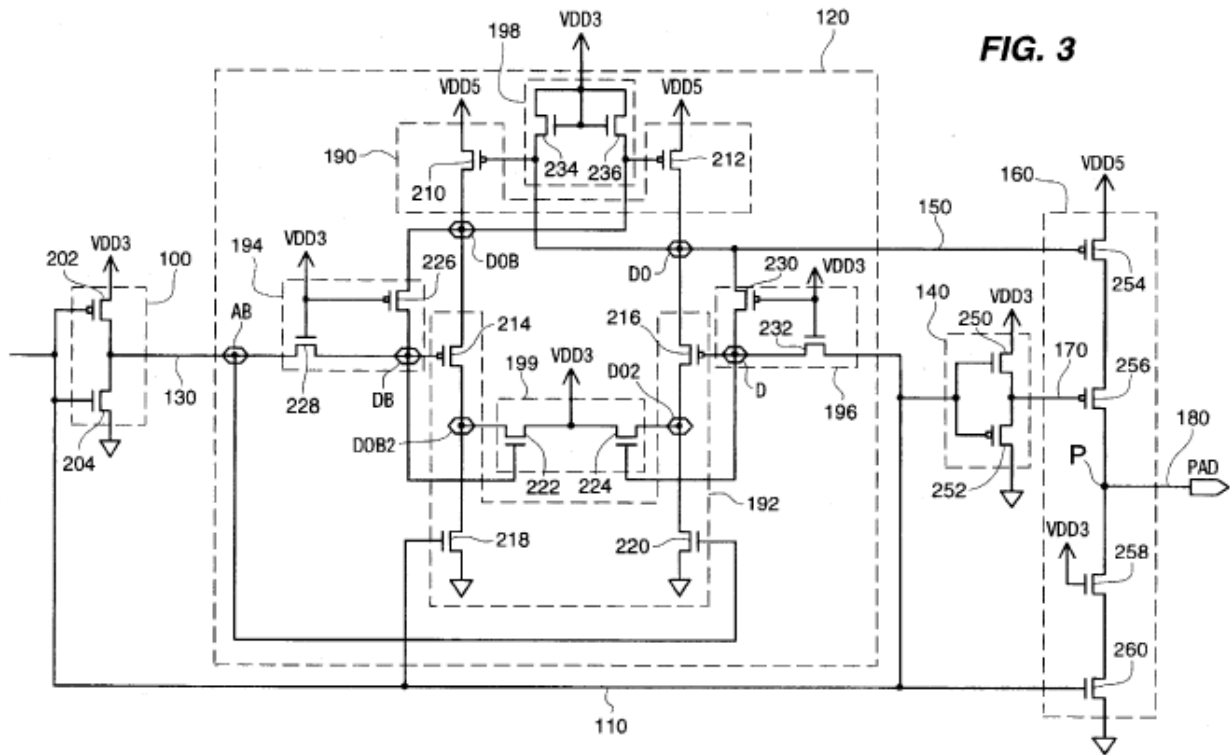
Figure 11: Full-Swing Transistor Network Levelshifter [13]
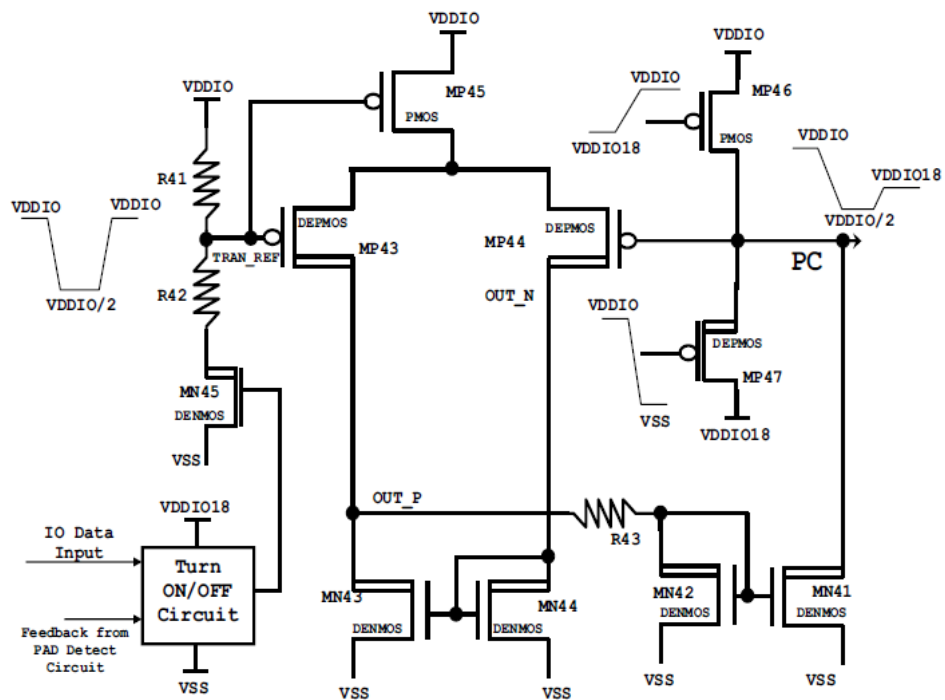
Figure 12: Dynamically Biased Differential Amplifier Levelshifter [14]

As shown, [6] uses 16 transistors, [16] uses 14 transistors, and [17] uses 9 transistors and 2 resistors (not counting the Turn ON/OFF circuit since the contents were not divulged). The referenced articles do not document the amount of dynamic or static power consumed by the circuits so it is difficult to compare. The full-swing transistor networks of [6] [16] will consume little static current. The differential amplifier [17] will also consume little static current because it has a low power mode in which the input data and feedback from a PAD Detect circuit will shut off the bias and current source.

The goal of the levelshifter design for this project is to ensure that it will toggle at the rated speed of 200 MHz while consuming a negligible amount of static current and use the minimum number of devices possible while keeping all transistors from overstress conditions.

2.3.2 Design Theory

Along the data path, it is necessary to levelshift data from the $0V - 1.8V$ domain to the $1.8V - 3.3V$ domain. This signal is the p_in18_33 signal in Figure 3 and is used to control the gate of transistor P0 (which will either turn on the pull-up portion of the output buffer or tri-state it). The schematic for the 1.8V-to-3.3V Levelshifter is shown in Figure 13 below.
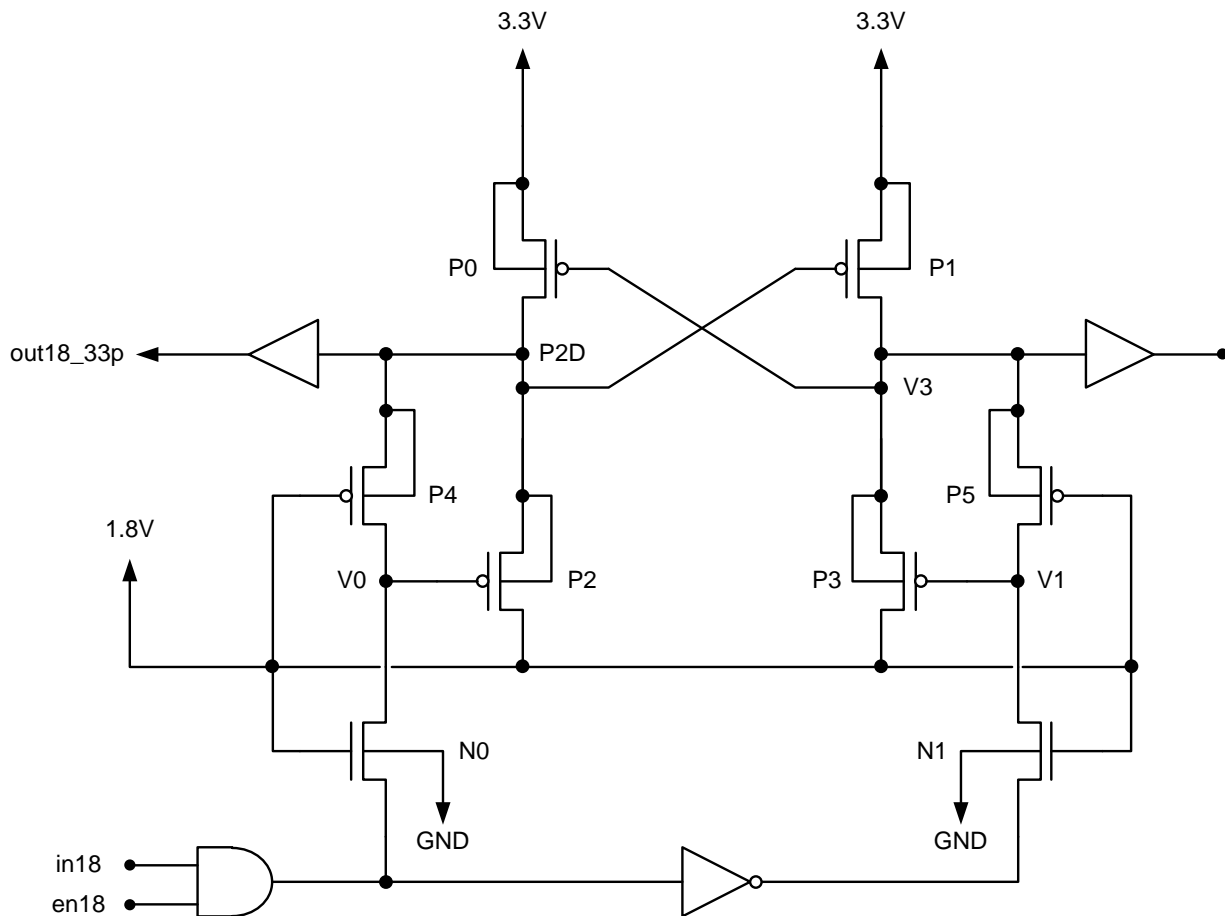
Figure 13: 1.8V-to-3.3V Levelshifter

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Before proceeding with the circuit analysis, it should be pointed out that the intended voltage swing of 'out18_33p' is from 1.8V to 3.3V. This allows P0 in the Output Buffer to not be overstressed while giving enough overdrive voltage ($|V_{sg}| - V_{thp}$) such that it performs adequately without extreme sizing.

The circuit analysis is as follows: data enters the circuit to the 'data_in' node of the AND gate. Assuming data is '1', it will be 1.8V and so the source of N0 is 1.8V and the source of N1 is 0V. Since is the gate of the N0 is connected to 1.8V, N1 is on and its drain (V1 node) will be pulled to 0V. This will turn P3 on and it will pull its drain (V3 node) to 1.8V since its source is tied to 1.8V. The gate of P0 is also connected to V3 and since it is now 1.8V, P0 is on and 'out18_33p' will be pulled up to 3.3V, thereby levelshifting the incoming logic-1 from 1.8V to 3.3V. If the incoming data was a logic-0, the reverse happens as this circuit is symmetric. Figure 14 shows the transient simulation results of the output node 'out18_33p' toggling at 200MHz (FF in green, TT in orange, SS in purple):
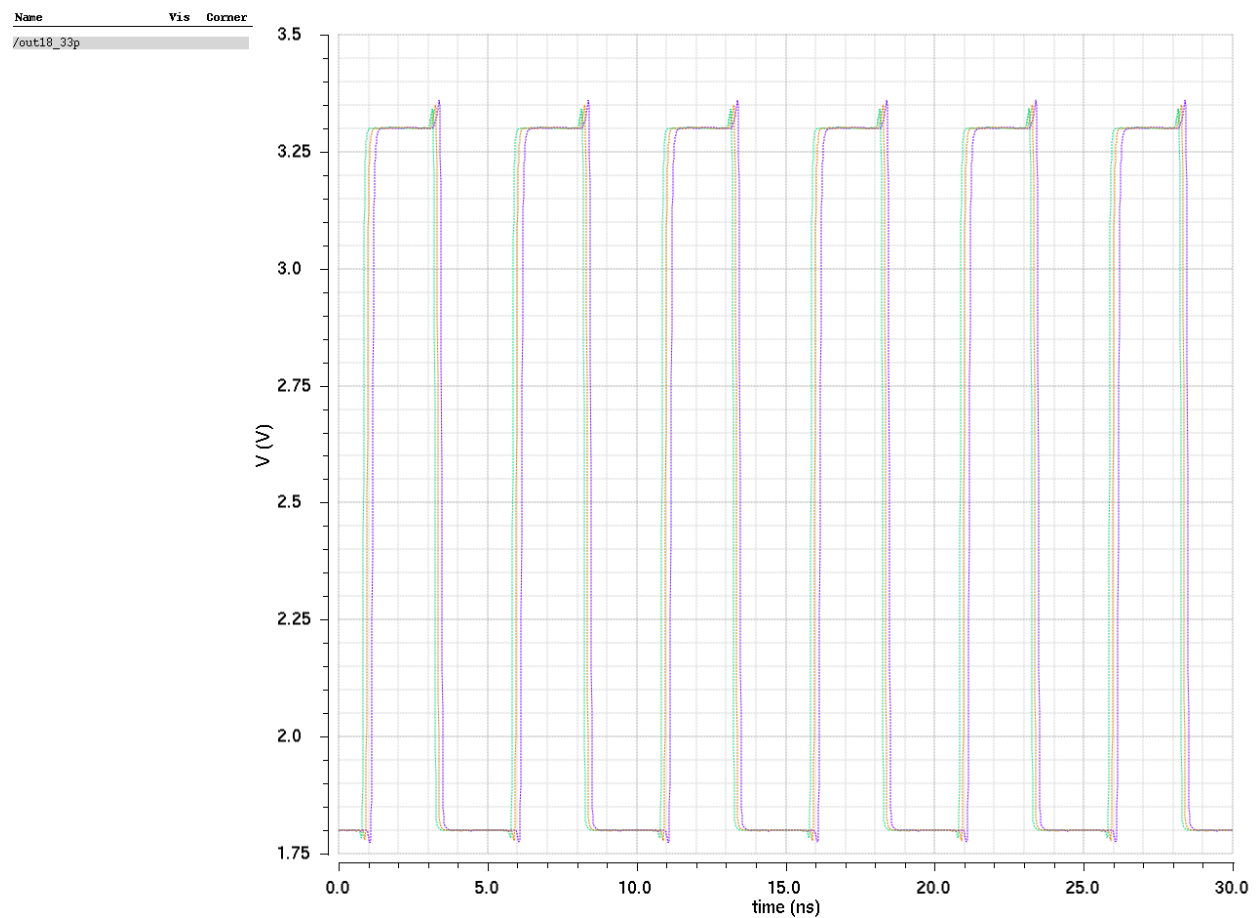
Figure 14: 'out18_33p' Toggling at 200 MHz at TT, SS, FF, 50C, Nominal Voltage Corners

It is important to note that the nodes V0 and V1 will swing from 0V to 3.3V. However, the drains of P2 and P3 will track this swing from 1.8V to 3.3V and will prevent these two transistors from enter an over-voltage state. Simulation results confirm this.

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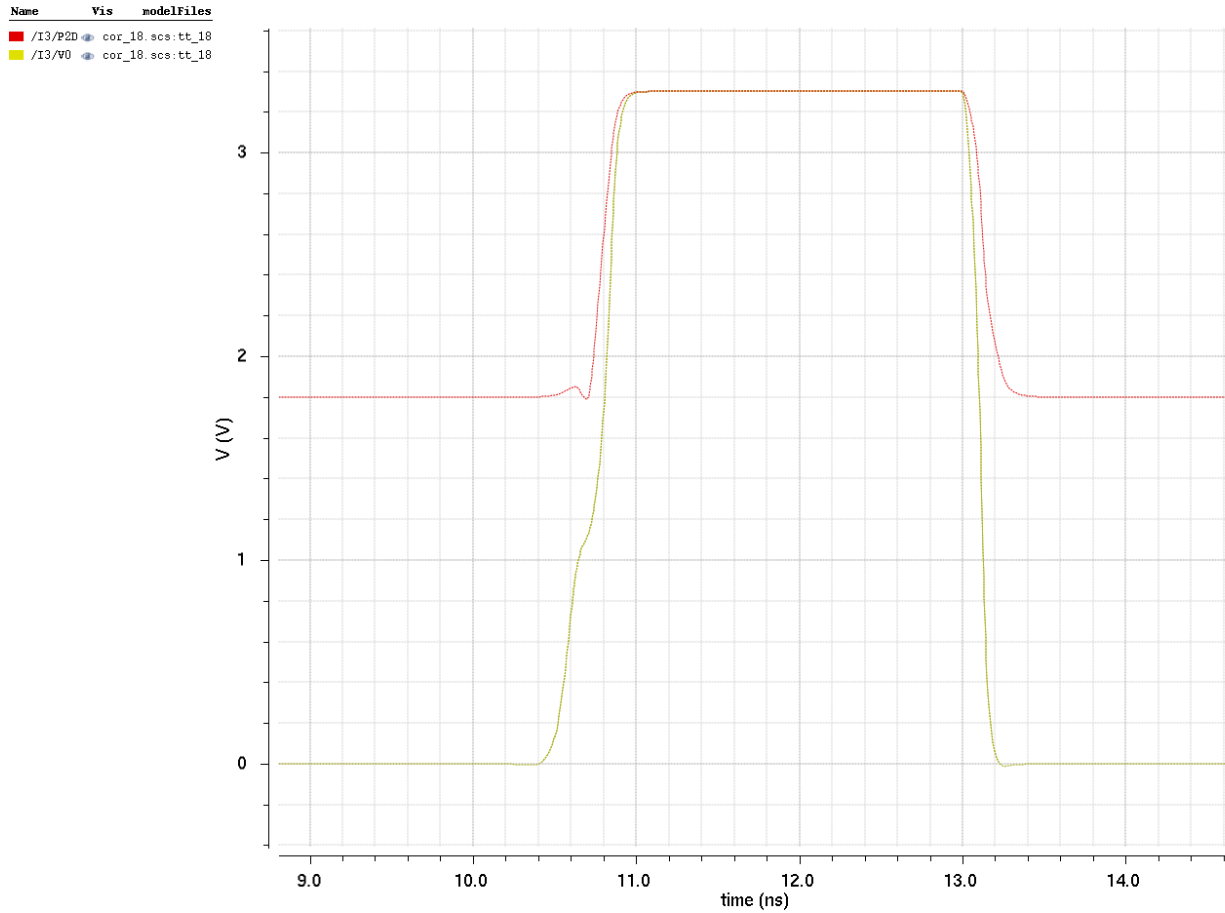
Figure 15: Node V0 tracking Node P2D to Prevent Overvoltage

2.3.3   Overstress Voltage Check

In order to check for overvoltage conditions for the entire design, spectre simulations were run with the following assert statements:

nmos18_vgs assert sub=nch_18_mac dev=nch_18_mac param=vgs min=-2.1 max=2.1 duration=100p level=error
nmos18_vds assert sub=nch_18_mac dev=nch_18_mac param=vds min=-2.1 max=2.1 duration=100p level=error
pmos18_vgs assert sub=pch_18_mac dev=pch_18_mac param=vgs min=-2.1 max=2.1 duration=100p level=error
pmos18_vds assert sub=pch_18_mac dev=pch_18_mac param=vds min=-2.1 max=2.1 duration=100p level=error

These statements will check for V_{gs} and V_{ds} overvoltage conditions of ±2.1V for a duration of 100ps. If the failure threshold is triggered, the simulation would fail and an error message displayed. This design was verified across the corners of 3.3V±10%, 1.8V±5%, TT, SS, FF, FNSP, SNFP, 0°C, 50°C, and 110°C (135 corners total) with no overvoltage failures.

2.3.4   Current Consumption

Current consumption is measured the voltage source powering the 1.8V and 3.3V rails in the levelshifter testbench. Note that the 1.8V static leakage measurement is negative. This is due to current leaking

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from the 3.3V rail to the 1.8V rail. Also note that this current path exists when the levelshifter is switching dynamically. The current which flows out the 1.8V rail will charge an onboard capacitor which is part of the circuitry of the 1.8V power regulator. This negative current will cancel positive current drawn from the 1.8V power regulator, thus ensuring that this measurement is not double-counting the current from drawn from the 3.3V with the current sunk to the 1.8V rail.

Current	TT 50˚C (A)	SS 110˚C (A)	FF 0˚C (A)	Note
1.8V Dynamic (200MHz)	27.9u	28.6u	25.8u	Average Current
1.8V Static (Leakage)	-1.33n	2.04n	-737p	-
3.3V Dynamic (200MHz)	85.5u	82.0u	90.0u	Average Current
3.3V Static (Leakage)	8.16n	10.3n	8.57n	-

Table 8: 1.8V-to-3.3V Levelshifter Current Consumption

2.4   1.0V-to-1.8V Levelshifter

2.4.1   Design Theory
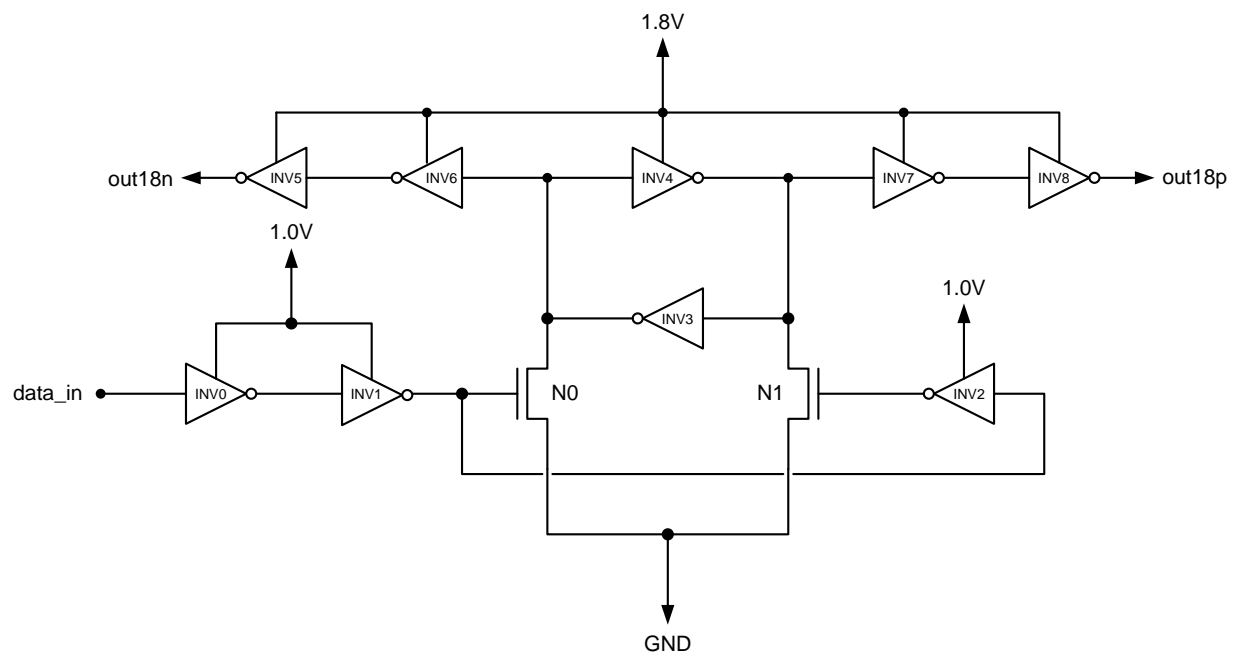
Figure 16: 1.0V-to-1.8V Levelshifter

The 1.0V-to-1.8V levelshifter is used for shifting from the ASIC's core-level voltage to the 1.8V domain. INV0, INV1, and INV2 are all thin-gate devices (L=60nm) while transistors N0, N1 and inverters INV3-8

are thick-gate devices. The voltage domain crossing occurs at the gates of N0 and N1. The main concern in this design is to make sure that N0 and N1 are overdriven with enough voltage to turn on with enough strength to overcome the latch made up of INV3 and INV4. This can be a concern if the 1.0V supply is too low and the 1.8V supply is too high. Assuming a specification of ±10% on the 1.0V supply, the lower end of this range is 0.9V. For 1.8V, the tolerance is ±5% so the worst case is if it is at 1.89V. As such, the levelshifter works within spec at these voltage extremes as shown in Figure 17.

2.4.2   Target Specifications

The specifications used for the 1.0V-to-1.8V levelshifter are listed in the following table.

Parameter	Spec	Units
Duty_Cycle	48 - 52	%
T_{RISE}	100	ps
T_{FALL}	100	ps

Table 9: 1.0V-to-1.8V Levelshifter Target Specifications

2.4.3   Simulation Results

2.4.3.1   Levelshifter Output with 0.9V Input Swing
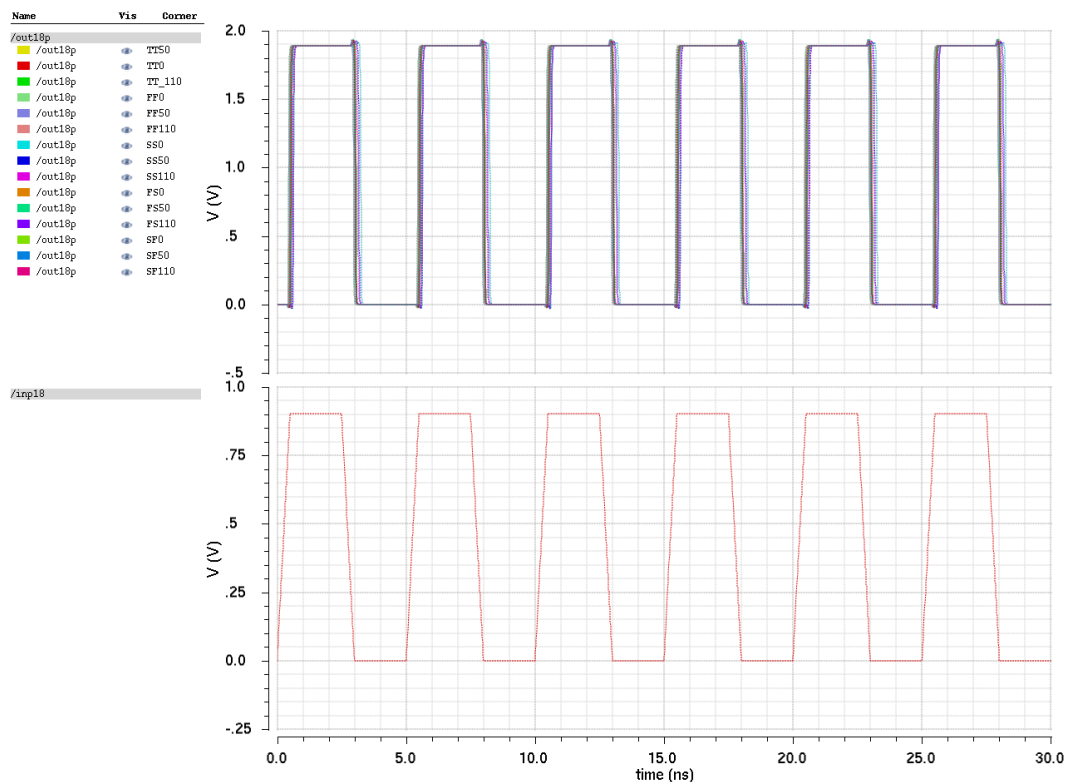
Figure 17: Levelshifter Output with 0.9V Input Swing

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2.4.3.2 Duty Cycle and Slew-Rates

Parameter	TT 50˚C	SS 110˚C	FF 0˚C	Units	Note	Meet Spec?
Duty_Cycle	49.88	49.79	50.29	%	V_{DD_CORE} = 1.0V V_{DD18} = 1.8V	Yes
T_{RISE}	28.8	30.78	22.78	ps		Yes
T_{FALL}	35.05	37.5	27.61	ps		Yes

Table 10: 1.0V-to-1.8V Levelshifter Simulation Results

2.5 Transmitter Path Simulation

The final simulation to run is the toggling of the entire transit path at 200 MHz while driving a 30 cm, 50Ω transmission line with a 4 pF capacitive load termination. The transmission line is modeled with the following parameters: L=2.42n/cm, C=1p/cm, and 10 mΩ/cm. The stimulus driving the data input of the transmitter is a random stimulus generator which produces a Pseudo Random Bit Stream (PRBS) from the adhlLib library. At the same time, 4 other transmitters are also stimulated with different PRBS data inputs. The 3.3V and 1.8V power rails are modeled with a series inductor (L=2nH) and resistance (R=1Ω) in order to model jitter effects due to Simultaneous Switching Noise (SSN). The following is the transient simulation result for transmitting PRBS data at TT corner:
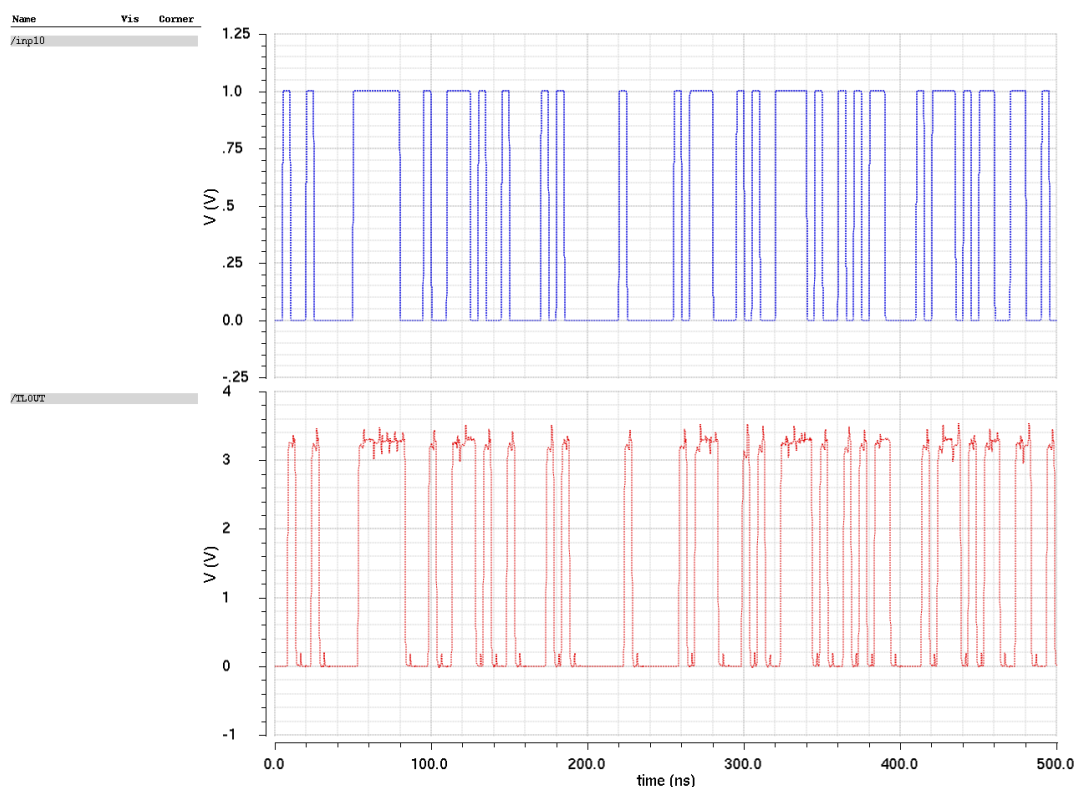
Figure 18: Transient Simulation Results for Transmitting 200 MHz PRBS Data for TT, 50°C, Nominal Voltage Corner

The following is the Eye Diagram from a transient simulation of 500 ns:
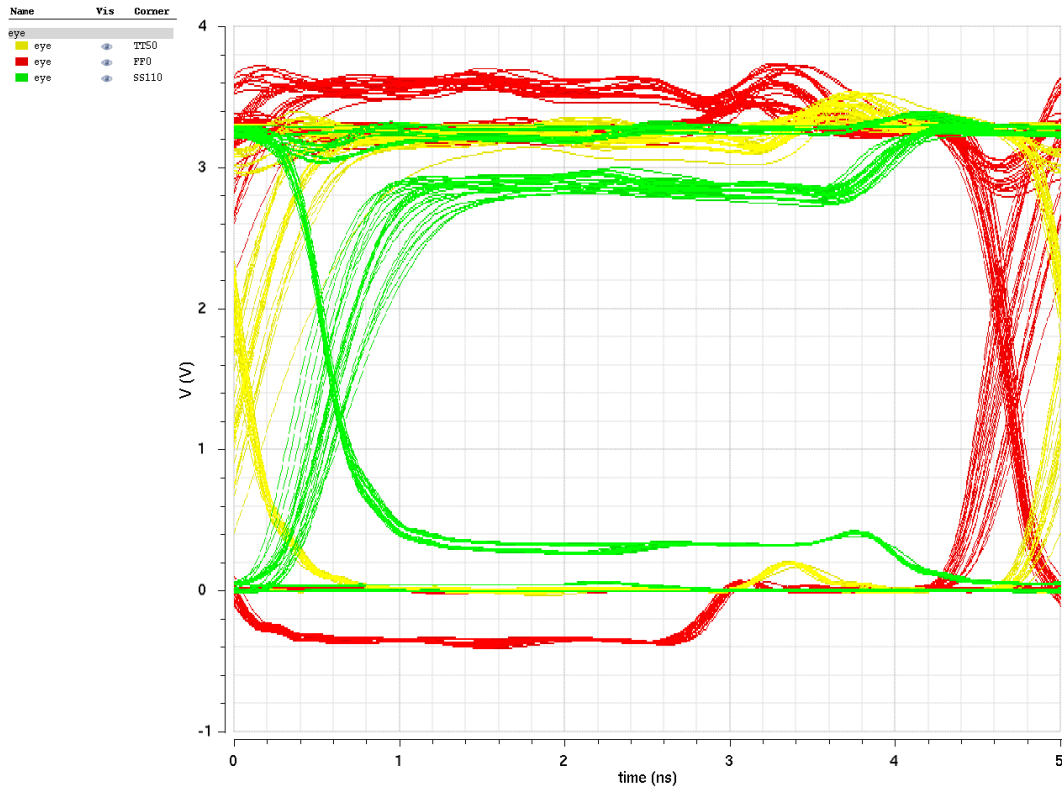
Figure 19: Eye Diagram for 200 MHz PRBS Data Transmission for TT50, SS110, FF0, Nom V Corners

2.5.1   JEDEC Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits DC Input Specification

In order to determine if the Eye Diagram above satisfies the necessary requirement for the transmitted signal to be received properly, it is useful to look at the JEDEC DC Input Specification:

Symbol	Parameter	Test Condition	Min	Max	Units
V_{IH}	Input High Voltage	$V_{OUT} \geq V_{OH\,(Min)}$	2	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	$V_{OUT} \leq V_{OL\,(Max)}$	-0.3	0.8	V

Table 11: JEDEC DC Input Specifications

From Figure 19, it can be seen that the worst case is the SS110 waveform in green. V_{OL} in the worst case is ≈0.4V while V_{OL} in the worst case is ≈2.6V. As such, they easily satisfy the JEDEC DC Input specification.

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3 Conclusion

The goal of this paper was to address the issues concerning the design of a high-voltage (3.3V) voltage-mode transmitter using 1.8V devices. These issues include the avoidance of device failure mechanisms such as GOI, NBTI, and HCI so as to not exceed overstress conditions on the devices used. Also, appropriate analysis was done on buffer output impedance, reference voltage variance, signal levelshifting, and transmission line effects. It is concluded that the final design achieved the goal of PRBS data transmission at 200 MHz while meeting JEDEC Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits Document [1] DC Specifications. The Eye Diagram shows that the transmitted signal should be received without problem as JEDEC DC Input Specifications were met.

4 Appendix A – Simulation Results

Point		Min	Max	TT50 tt_18	TT0 tt_18	TT_110 tt_18	FF0 ff_18	FF50 ff_18	FF110 ff_18	SS0 ss_18	SS50 ss_18	SS110 ss_18	FS0 fs_18	FS50 fs_18	FS110 fs_18	SF0 sf_18	SF50 sf_18	SF110 sf_18
Temp				50	0	110	0	50	110	0	50	110	0	50	110	0	85	110
vddrval=2.97, vdd18val=1.71	1	43.03	69.06	54.76	53.02	56.75	43.03	44.62	46.51	64.73	66.79	69.06	53.6	55.26	57.12	52.49	55.53	56.4
vddrval=2.97, vdd18val=1.8	2	45.33	75.44	58.56	56.66	60.57	45.33	47.13	49.16	71.48	73.5	75.44	57.62	59.35	61.12	55.79	59.15	60.04
vddrval=2.97, vdd18val=1.89	3	49.27	87.41	65.52	63.86	67.01	49.27	51.25	53.27	85.98	86.94	87.41	65.85	67.03	67.99	62.1	65.34	66.1
vddrval=3.3, vdd18val=1.71	4	39.3	60.05	48.97	47.77	50.52	39.3	40.4	41.84	56.85	58.25	60.05	48	49.18	50.69	47.55	49.68	50.36
vddrval=3.3, vdd18val=1.8	5	40.06	61.84	50.14	48.79	51.84	40.06	41.29	42.87	58.27	59.86	61.84	49.07	50.39	52.04	48.52	50.9	51.64
vddrval=3.3, vdd18val=1.89	6	41.06	64.26	51.69	50.16	53.55	41.06	42.44	44.17	60.24	62.07	64.26	50.53	52.02	53.81	49.81	52.49	53.3
vddrval=3.63, vdd18val=1.71	7	37.67	56.33	46.49	45.64	47.68	37.67	38.47	39.59	54.03	54.98	56.33	45.78	46.62	47.79	45.5	47.04	47.57
vddrval=3.63, vdd18val=1.8	8	38.04	57.19	47.06	46.12	48.35	38.04	38.93	40.13	54.65	55.72	57.19	46.28	47.21	48.48	45.96	47.66	48.24
vddrval=3.63, vdd18val=1.89	9	38.5	58.24	47.75	46.71	49.16	38.5	39.47	40.78	55.42	56.62	58.24	46.89	47.92	49.3	46.53	48.4	49.02

Table 12: P-Imp over all PVT

Point	Min	Max	TT50 tt_18 50	TT0 tt_18 0	TT_110 tt_18 110	FF0 ff_18 0	FF50 ff_18 50	FF110 ff_18 110	SS0 ss_18 0	SS50 ss_18 50	SS110 ss_18 110	FS0 fs_18 0	FS50 fs_18 50	FS110 fs_18 110	SF0 sf_18 0	SF50 sf_18 85	SF110 sf_18 110
1 vddrval=2.97, vdd18val=1.71	40.66	61.45	50.44	49.76	51.58	40.66	41.26	42.24	59.28	60.1	61.45	49.44	50.04	51.08	50.11	51.56	52.12
2 vddrval=2.97, vdd18val=1.8	40.4	60.73	50.01	49.42	51.04	40.4	40.93	41.83	58.83	59.53	60.73	49.13	49.65	50.59	49.74	51.02	51.52
3 vddrval=2.97, vdd18val=1.89	40.19	60.15	49.66	49.14	50.59	40.19	40.66	41.48	58.46	59.07	60.15	48.87	49.33	50.18	49.43	50.57	51.04
4 vddrval=3.3, vdd18val=1.71	40.75	61.69	50.58	49.86	51.78	40.75	41.38	42.42	59.41	60.27	61.69	49.53	50.17	51.26	50.22	51.76	52.34
5 vddrval=3.3, vdd18val=1.8	40.47	60.93	50.13	49.5	51.2	40.47	41.03	41.97	58.93	59.67	60.93	49.2	49.76	50.73	49.83	51.18	51.71
6 vddrval=3.3, vdd18val=1.89	40.25	60.31	49.76	49.21	50.73	40.25	40.75	41.61	58.55	59.18	60.31	48.94	49.42	50.3	49.51	50.71	51.19
7 vddrval=3.63, vdd18val=1.71	40.84	61.96	50.74	49.97	51.99	40.84	41.51	42.61	59.54	60.46	61.96	49.63	50.31	51.45	50.35	51.97	52.59
8 vddrval=3.63, vdd18val=1.8	40.55	61.14	50.25	49.59	51.38	40.55	41.14	42.13	59.04	59.82	61.14	49.28	49.87	50.89	49.93	51.35	51.9
9 vddrval=3.63, vdd18val=1.89	40.32	60.49	49.86	49.29	50.87	40.32	40.84	41.74	58.63	59.31	60.49	49	49.51	50.43	49.59	50.85	51.35

Table 13: N-Impedance over all PVT

Point	Spec	Pass/Fail	Min	Max	TT50 tt_18 50	TT0 tt_18 0	TT_110 tt_18 110	FF0 ff_18 0	FF50 ff_18 50	FF110 ff_18 110	SS0 ss_18 0	SS50 ss_18 50	SS110 ss_18 110	FS0 fs_18 0	FS50 fs_18 50	FS110 fs_18 110	SF0 sf_18 0	SF50 sf_18 85	SF110 sf_18 110
1 vddrval=2.97, vdd18val=1.71	> 2.77	pass	2.96	2.97	2.97	2.97	2.96	2.97	2.97	2.97	2.96	2.96	2.96	2.97	2.97	2.96	2.97	2.96	2.96
2 vddrval=2.97, vdd18val=1.8	> 2.77	pass	2.96	2.97	2.96	2.97	2.96	2.97	2.97	2.97	2.96	2.96	2.96	2.97	2.96	2.96	2.97	2.96	2.96
3 vddrval=2.97, vdd18val=1.89	> 2.77	pass	2.96	2.97	2.96	2.96	2.96	2.97	2.97	2.97	2.96	2.96	2.96	2.96	2.96	2.96	2.96	2.96	2.96
4 vddrval=3.3, vdd18val=1.71	> 2.77	pass	3.29	3.30	3.30	3.30	3.30	3.30	3.30	3.30	3.29	3.29	3.29	3.30	3.30	3.30	3.30	3.30	3.30
5 vddrval=3.3, vdd18val=1.8	> 2.77	pass	3.29	3.30	3.30	3.30	3.30	3.30	3.30	3.30	3.29	3.29	3.29	3.30	3.30	3.30	3.30	3.30	3.30
6 vddrval=3.3, vdd18val=1.89	> 2.77	pass	3.29	3.30	3.30	3.30	3.30	3.30	3.30	3.30	3.29	3.29	3.29	3.30	3.30	3.30	3.30	3.30	3.30
7 vddrval=3.63, vdd18val=1.71	> 2.77	pass	3.62	3.63	3.63	3.63	3.63	3.63	3.63	3.63	3.62	3.62	3.62	3.63	3.63	3.63	3.63	3.63	3.63
8 vddrval=3.63, vdd18val=1.8	> 2.77	pass	3.62	3.63	3.63	3.63	3.63	3.63	3.63	3.63	3.62	3.62	3.62	3.63	3.63	3.63	3.63	3.63	3.63
9 vddrval=3.63, vdd18val=1.89	> 2.77	pass	3.62	3.63	3.63	3.63	3.63	3.63	3.63	3.63	3.62	3.62	3.62	3.63	3.63	3.63	3.63	3.63	3.63

Table 14: V$_{OH}$ over all PVT

					TT50	TT0	TT_110	FF0	FF50	FF110	SS0	SS50	SS110	FS0	FS50	FS110	SF0	SF50	SF110
					tt_18	tt_18	tt_18	ff_18	ff_18	ff_18	ss_18	ss_18	ss_18	fs_18	fs_18	fs_18	sf_18	sf_18	sf_18
				Temp	50	0	110	0	50	110	0	50	110	0	50	110	0	85	110
Point		Spec	Min	Max	TT50	TT0	TT_110	FF0	FF50	FF110	SS0	SS50	SS110	FS0	FS50	FS110	SF0	SF50	SF110
vddnval=2.97, vdd18val=1.71	1	< 200m	4.48E-03	6.67E-03	5.52E-03	5.48E-03	5.72E-03	4.48E-03	4.57E-03	5.19E-03	6.53E-03	6.57E-03	6.67E-03	5.45E-03	5.49E-03	5.65E-03	5.51E-03	5.65E-03	5.79E-03
vddnval=2.97, vdd18val=1.8	2	< 200m	4.46E-03	6.62E-03	5.49E-03	5.46E-03	5.67E-03	4.46E-03	4.54E-03	5.09E-03	6.50E-03	6.53E-03	6.62E-03	5.43E-03	5.46E-03	5.61E-03	5.48E-03	5.61E-03	5.73E-03
vddnval=2.97, vdd18val=1.89	3	< 200m	4.44E-03	6.58E-03	5.47E-03	5.44E-03	5.62E-03	4.44E-03	4.52E-03	4.99E-03	6.47E-03	6.50E-03	6.58E-03	5.42E-03	5.44E-03	5.57E-03	5.46E-03	5.57E-03	5.69E-03
vddnval=3.3, vdd18val=1.71	4	< 200m	4.48E-03	6.67E-03	5.53E-03	5.48E-03	5.79E-03	4.48E-03	4.64E-03	5.61E-03	6.53E-03	6.57E-03	6.67E-03	5.45E-03	5.49E-03	5.70E-03	5.51E-03	5.69E-03	5.89E-03
vddnval=3.3, vdd18val=1.8	5	< 200m	4.46E-03	6.63E-03	5.50E-03	5.46E-03	5.73E-03	4.46E-03	4.60E-03	5.45E-03	6.50E-03	6.53E-03	6.63E-03	5.43E-03	5.47E-03	5.66E-03	5.48E-03	5.65E-03	5.82E-03
vddnval=3.3, vdd18val=1.89	6	< 200m	4.45E-03	6.59E-03	5.47E-03	5.44E-03	5.68E-03	4.45E-03	4.56E-03	5.32E-03	6.47E-03	6.50E-03	6.59E-03	5.42E-03	5.44E-03	5.61E-03	5.46E-03	5.61E-03	5.76E-03
vddnval=3.63, vdd18val=1.71	7	< 200m	4.50E-03	6.69E-03	5.54E-03	5.48E-03	5.90E-03	4.50E-03	4.75E-03	6.28E-03	6.53E-03	6.57E-03	6.69E-03	5.46E-03	5.50E-03	5.78E-03	5.51E-03	5.76E-03	6.05E-03
vddnval=3.63, vdd18val=1.8	8	< 200m	4.48E-03	6.64E-03	5.51E-03	5.46E-03	5.83E-03	4.48E-03	4.69E-03	6.05E-03	6.50E-03	6.53E-03	6.64E-03	5.43E-03	5.47E-03	5.73E-03	5.48E-03	5.71E-03	5.96E-03
vddnval=3.63, vdd18val=1.89	9	< 200m	4.46E-03	6.60E-03	5.48E-03	5.44E-03	5.77E-03	4.46E-03	4.64E-03	5.84E-03	6.47E-03	6.50E-03	6.60E-03	5.42E-03	5.45E-03	5.68E-03	5.46E-03	5.66E-03	5.89E-03

Table 15: V$_{OL}$ over all PVT

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Table 16: 1.8V-to-3.3V Levelshifter Output Slew-Rates

Point	Output	Spec	Min	Max	TT0	TT85	TT_110	FF0	FF85	FF110	SS0	SS85	SS110	FS0	FS85	FS110	SF0	SFB5	SF110
		Temp			tt_18 / 0	tt_18 / 85	tt_18 / 110	ff_18 / 0	ff_18 / 85	ff_18 / 110	ss_18 / 0	ss_18 / 85	ss_18 / 110	fs_18 / 0	fs_18 / 85	fs_18 / 110	sf_18 / 0	sf_18 / 85	sf_18 / 110
vdrval=2.97,vdd18val=1.71	duty_cycle_out		0.45	0.48	0.47	0.46	0.46	0.48	0.47	0.47	0.45	0.45	0.45	0.48	0.47	0.47	0.46	0.46	0.46
1	rise_time	<100p	31.9E-12	60.1E-12	39.8E-12	45.8E-12	47.3E-12	31.9E-12	36.7E-12	38.1E-12	50.2E-12	58.2E-12	60.1E-12	37.4E-12	43.6E-12	45.0E-12	42.6E-12	48.6E-12	50.0E-12
1	fall_time	<100p	27.4E-12	51.8E-12	33.8E-12	40.2E-12	42.1E-12	27.4E-12	33.7E-12	36.0E-12	42.4E-12	49.8E-12	51.8E-12	33.1E-12	39.4E-12	41.3E-12	34.1E-12	41.0E-12	42.8E-12
vdrval=2.97,vdd18val=1.8	duty_cycle_out		0.44	0.47	0.46	0.46	0.46	0.47	0.47	0.47	0.44	0.44	0.44	0.47	0.47	0.47	0.45	0.45	0.45
2	rise_time	<100p	30.3E-12	59.4E-12	38.4E-12	43.9E-12	45.3E-12	30.5E-12	34.2E-12	35.2E-12	51.4E-12	57.8E-12	59.4E-12	35.5E-12	41.1E-12	42.4E-12	41.8E-12	47.3E-12	48.5E-12
2	fall_time	<100p	25.4E-12	50.6E-12	32.3E-12	37.9E-12	39.5E-12	25.4E-12	30.8E-12	32.3E-12	43.2E-12	49.0E-12	50.6E-12	31.6E-12	36.6E-12	38.4E-12	33.2E-12	39.0E-12	40.6E-12
vdrval=2.97,vdd18val=1.89	duty_cycle_out		0.42	0.47	0.45	0.45	0.45	0.47	0.47	0.47	0.42	0.42	0.42	0.46	0.46	0.46	0.44	0.44	0.44
3	rise_time	<100p	27.2E-12	58.0E-12	36.8E-12	40.4E-12	41.3E-12	27.2E-12	30.5E-12	31.2E-12	54.4E-12	57.0E-12	58.0E-12	32.7E-12	37.3E-12	38.2E-12	40.6E-12	44.6E-12	45.5E-12
3	fall_time	<100p	22.8E-12	48.9E-12	30.5E-12	34.6E-12	35.7E-12	22.8E-12	26.7E-12	28.0E-12	44.7E-12	48.0E-12	48.9E-12	29.3E-12	33.3E-12	34.4E-12	31.9E-12	36.0E-12	37.1E-12
vdrval=3.3,vdd18val=1.71	duty_cycle_out		0.46	0.48	0.48	0.47	0.47	0.48	0.48	0.48	0.47	0.46	0.46	0.48	0.48	0.48	0.47	0.47	0.47
4	rise_time	<100p	30.6E-12	53.1E-12	35.8E-12	42.7E-12	45.0E-12	30.8E-12	38.4E-12	40.9E-12	43.1E-12	50.9E-12	53.1E-12	34.4E-12	41.1E-12	43.6E-12	36.8E-12	44.3E-12	46.8E-12
4	fall_time	<100p	27.3E-12	46.7E-12	30.9E-12	38.8E-12	41.4E-12	27.3E-12	35.5E-12	38.2E-12	36.1E-12	44.3E-12	46.7E-12	30.8E-12	38.6E-12	41.0E-12	31.1E-12	39.4E-12	41.9E-12
vdrval=3.3,vdd18val=1.8	duty_cycle_out		0.46	0.48	0.48	0.47	0.47	0.48	0.48	0.48	0.47	0.46	0.46	0.48	0.48	0.48	0.47	0.46	0.46
5	rise_time	<100p	29.2E-12	52.7E-12	35.1E-12	41.2E-12	43.2E-12	29.2E-12	35.8E-12	37.9E-12	42.8E-12	50.6E-12	52.7E-12	33.8E-12	39.6E-12	41.5E-12	36.7E-12	42.9E-12	45.0E-12
5	fall_time	<100p	25.9E-12	45.7E-12	30.2E-12	37.2E-12	39.6E-12	25.9E-12	33.3E-12	35.8E-12	35.5E-12	43.3E-12	45.7E-12	30.8E-12	36.6E-12	38.9E-12	30.3E-12	37.6E-12	40.0E-12
vdrval=3.3,vdd18val=1.89	duty_cycle_out		0.45	0.48	0.47	0.47	0.47	0.48	0.48	0.47	0.46	0.46	0.45	0.48	0.48	0.47	0.47	0.46	0.46
6	rise_time	<100p	27.9E-12	51.8E-12	34.6E-12	39.9E-12	41.6E-12	27.9E-12	33.1E-12	35.1E-12	42.3E-12	50.0E-12	51.8E-12	32.9E-12	38.3E-12	39.6E-12	36.5E-12	42.0E-12	43.4E-12
6	fall_time	<100p	24.4E-12	44.3E-12	28.8E-12	35.4E-12	37.5E-12	24.4E-12	31.1E-12	33.0E-12	35.1E-12	42.4E-12	44.3E-12	28.8E-12	35.0E-12	36.9E-12	29.3E-12	36.0E-12	38.0E-12
vdrval=3.63,vdd18val=1.71	duty_cycle_out		0.47	0.49	0.48	0.48	0.48	0.49	0.48	0.48	0.48	0.47	0.47	0.49	0.49	0.49	0.48	0.47	0.47
7	rise_time	<100p	32.1E-12	50.5E-12	34.3E-12	43.7E-12	46.9E-12	32.1E-12	41.6E-12	44.8E-12	38.5E-12	47.4E-12	50.5E-12	33.4E-12	42.1E-12	45.5E-12	35.4E-12	45.0E-12	48.2E-12
7	fall_time	<100p	28.2E-12	44.8E-12	30.2E-12	39.1E-12	42.0E-12	28.2E-12	37.1E-12	40.0E-12	33.2E-12	42.0E-12	44.8E-12	30.3E-12	39.0E-12	41.8E-12	30.4E-12	39.5E-12	42.4E-12
vdrval=3.63,vdd18val=1.8	duty_cycle_out		0.47	0.49	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.47	0.47	0.49	0.48	0.48	0.48	0.47	0.47
8	rise_time	<100p	30.2E-12	48.5E-12	32.9E-12	41.3E-12	44.1E-12	30.2E-12	38.8E-12	41.7E-12	38.0E-12	46.1E-12	48.5E-12	32.0E-12	40.0E-12	42.8E-12	34.0E-12	42.7E-12	45.4E-12
8	fall_time	<100p	26.8E-12	43.4E-12	29.1E-12	37.5E-12	40.2E-12	26.8E-12	35.1E-12	37.9E-12	32.6E-12	40.6E-12	43.4E-12	29.1E-12	37.4E-12	40.0E-12	29.5E-12	37.8E-12	40.6E-12
vdrval=3.63,vdd18val=1.89	duty_cycle_out		0.47	0.49	0.48	0.48	0.47	0.48	0.48	0.48	0.47	0.47	0.47	0.49	0.48	0.48	0.47	0.47	0.47
9	rise_time	<100p	28.5E-12	47.3E-12	31.8E-12	39.2E-12	41.6E-12	28.5E-12	36.1E-12	38.6E-12	38.0E-12	45.1E-12	47.3E-12	30.9E-12	37.9E-12	40.2E-12	33.0E-12	40.6E-12	43.1E-12
9	fall_time	<100p	25.4E-12	42.1E-12	28.1E-12	35.8E-12	38.3E-12	25.4E-12	33.3E-12	35.9E-12	32.0E-12	39.7E-12	42.1E-12	28.0E-12	35.5E-12	38.0E-12	28.2E-12	36.2E-12	38.6E-12

Table 16: 1.8V-to-3.3V Levelshifter Output Slew-Rates
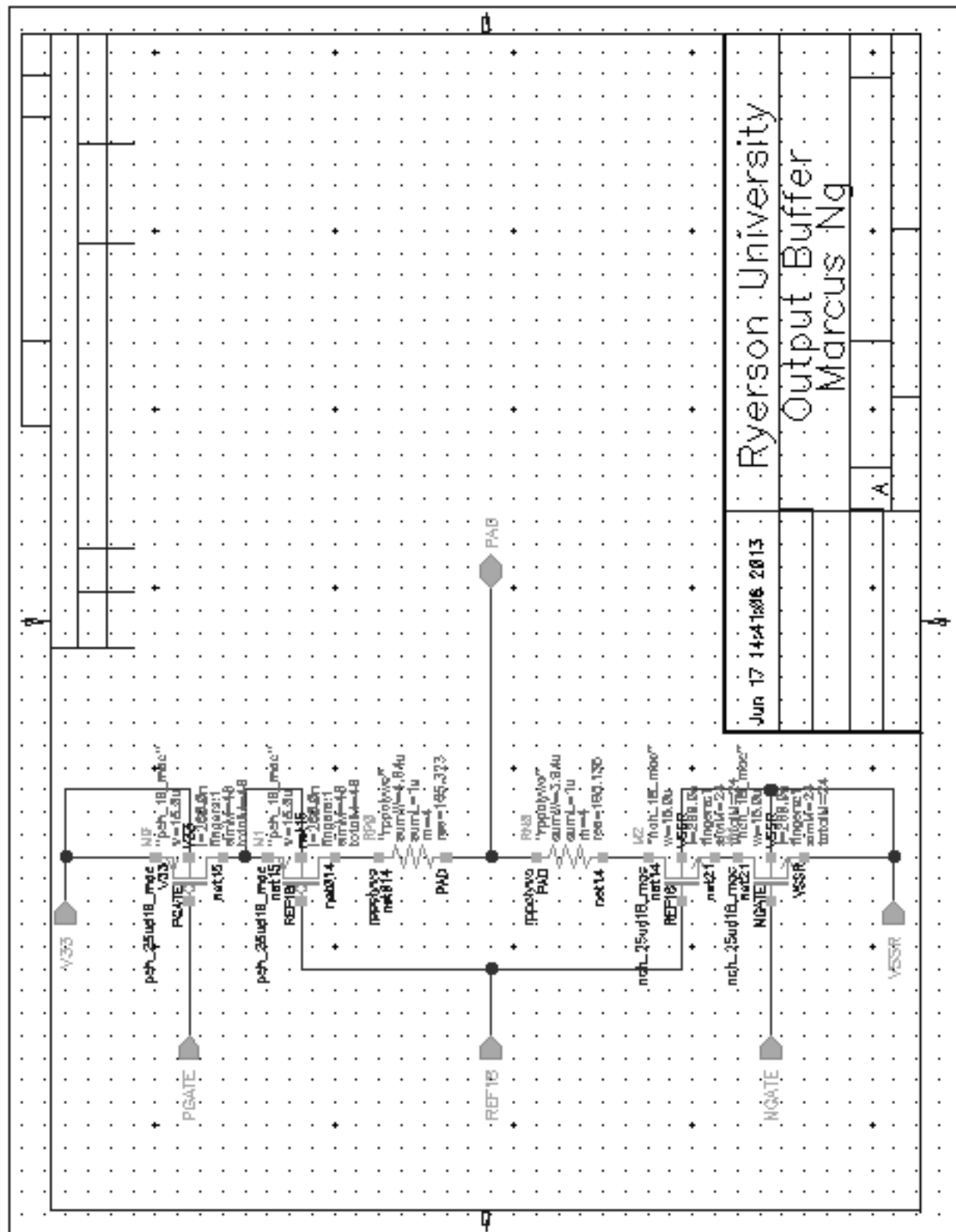
29

5 Appendix B – Circuit and Testbench Schematics

Figure 20: Output Buffer Schematic

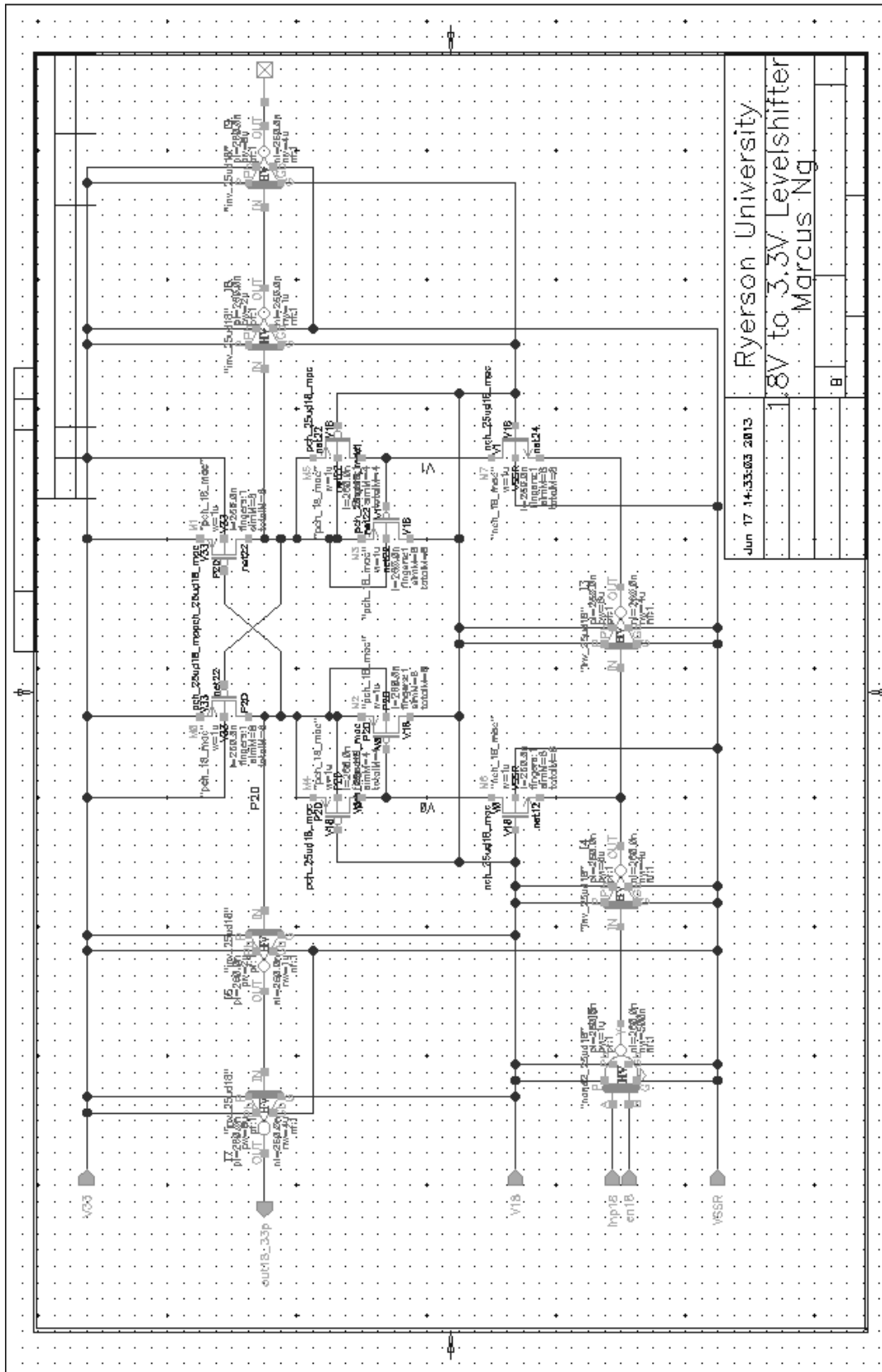**Figure 21: Output Buffer Testbench (Impedance)**

Figure 22: 1.8V-to-3.3V Levelshifter Schematic
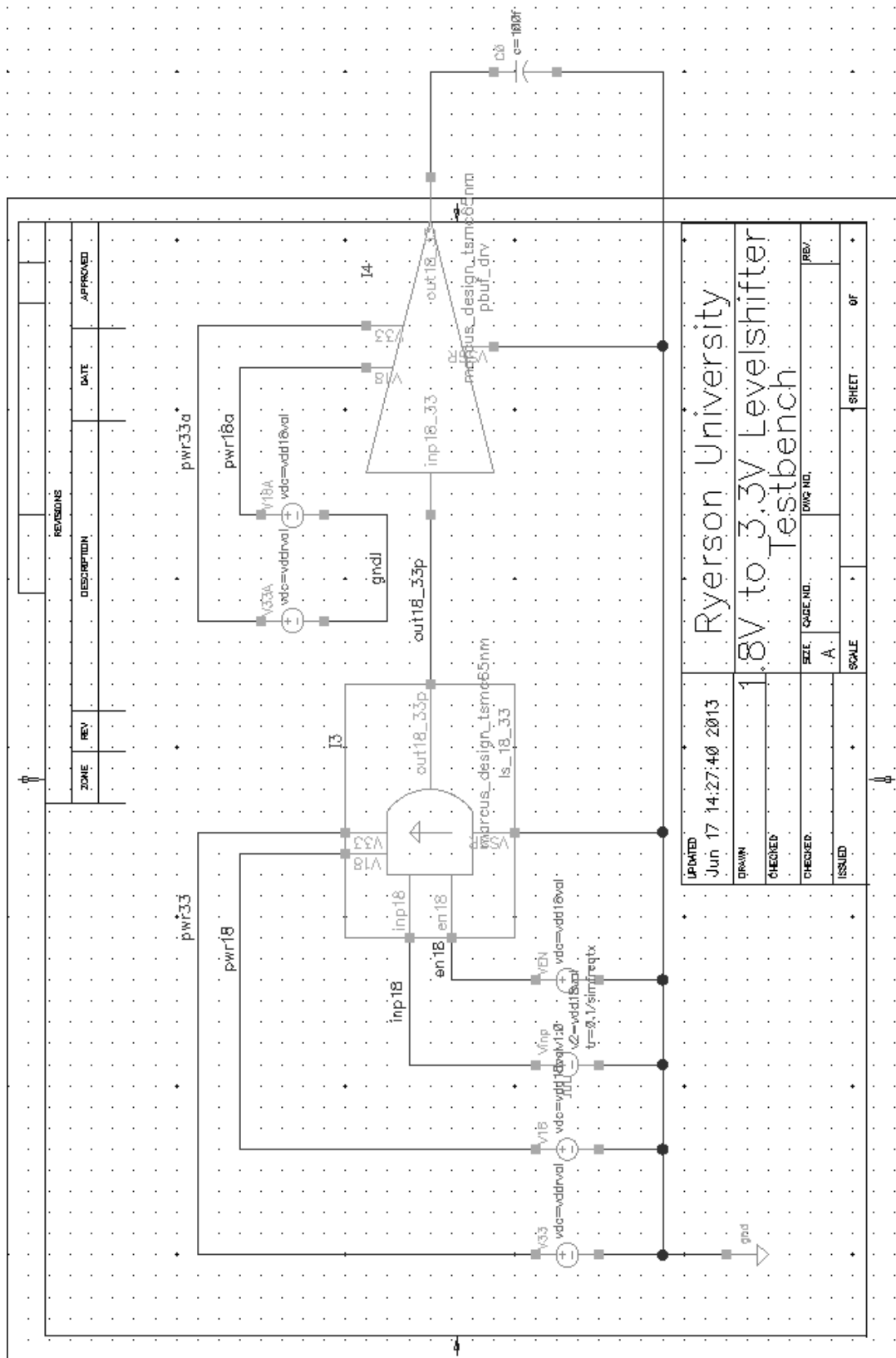
Figure 23: 1.8V-to-3.3V Levelshifter Testbench

Figure 24: Transmitter Schematic
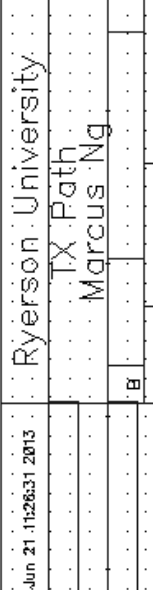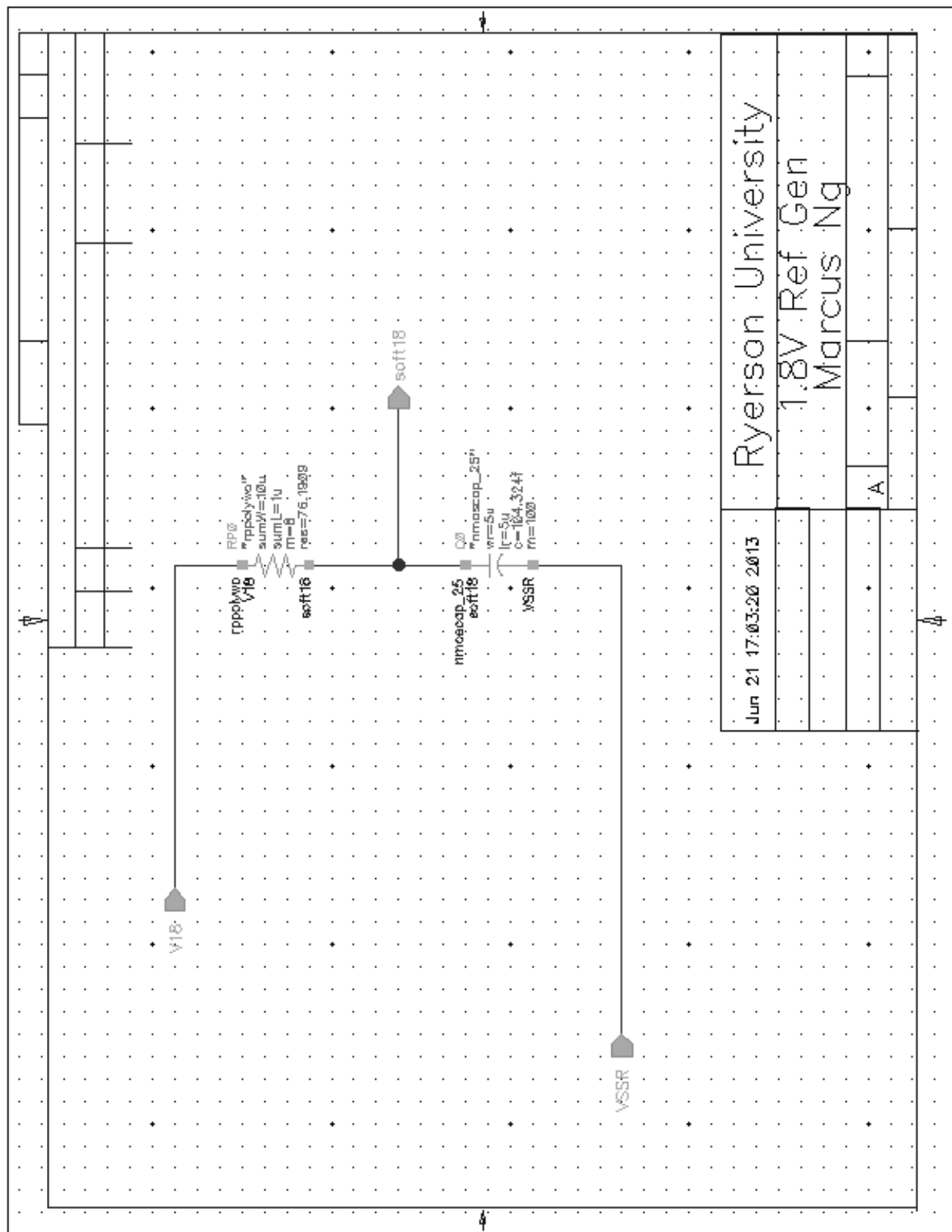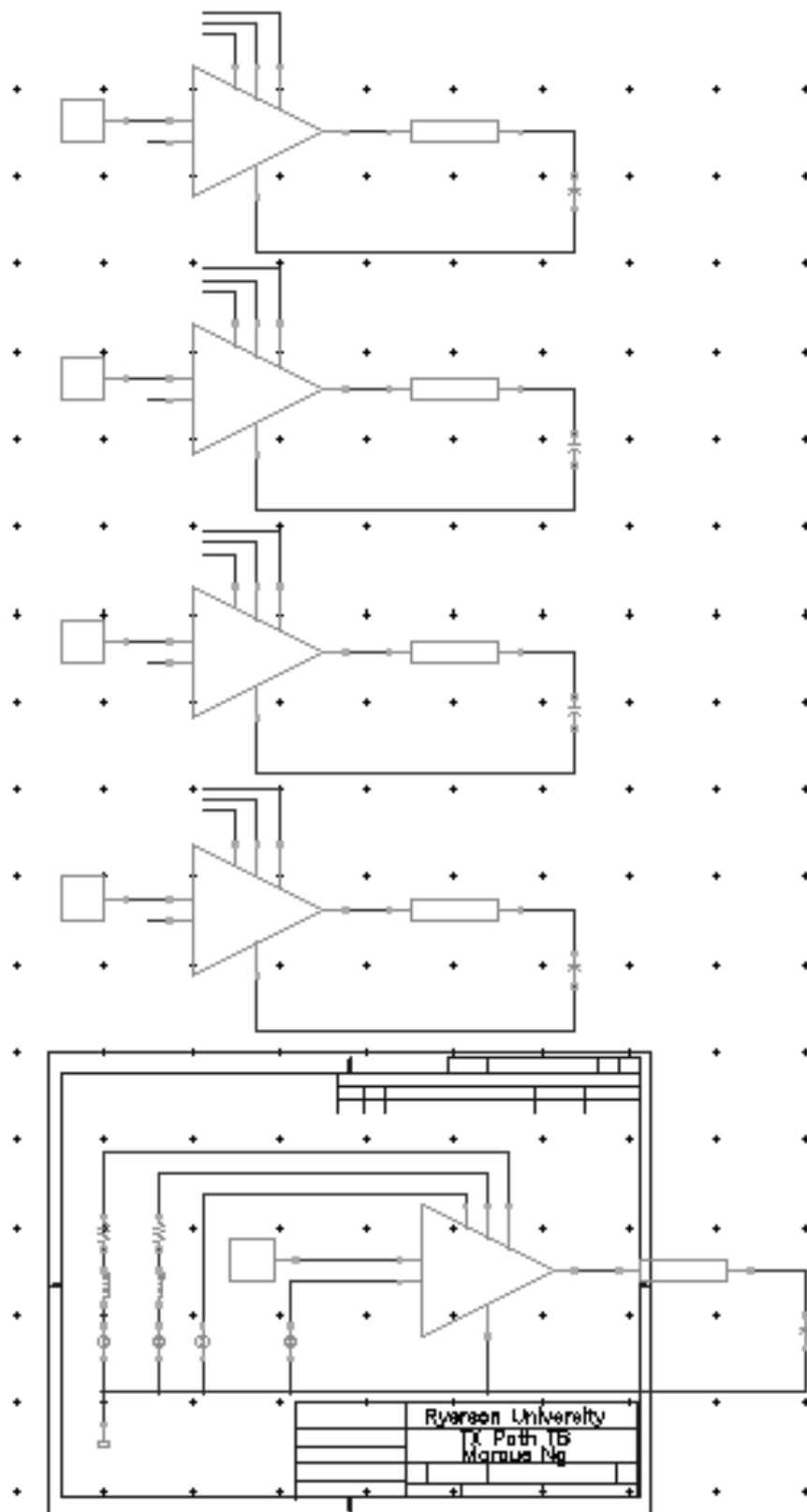
Figure 25: 1.8V Reference Generator

Figure 26: 200 MHz Tx Simulation Testbench
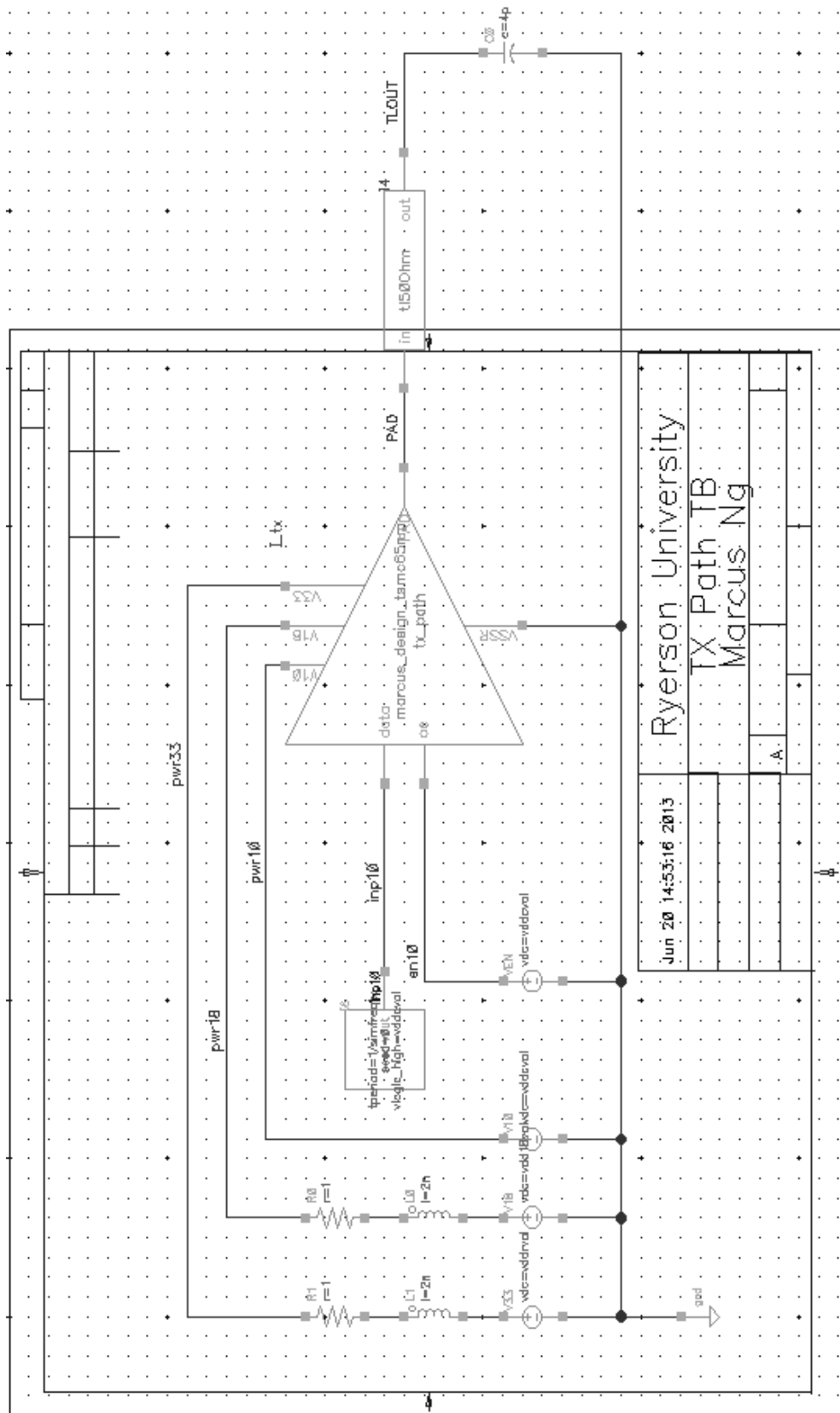
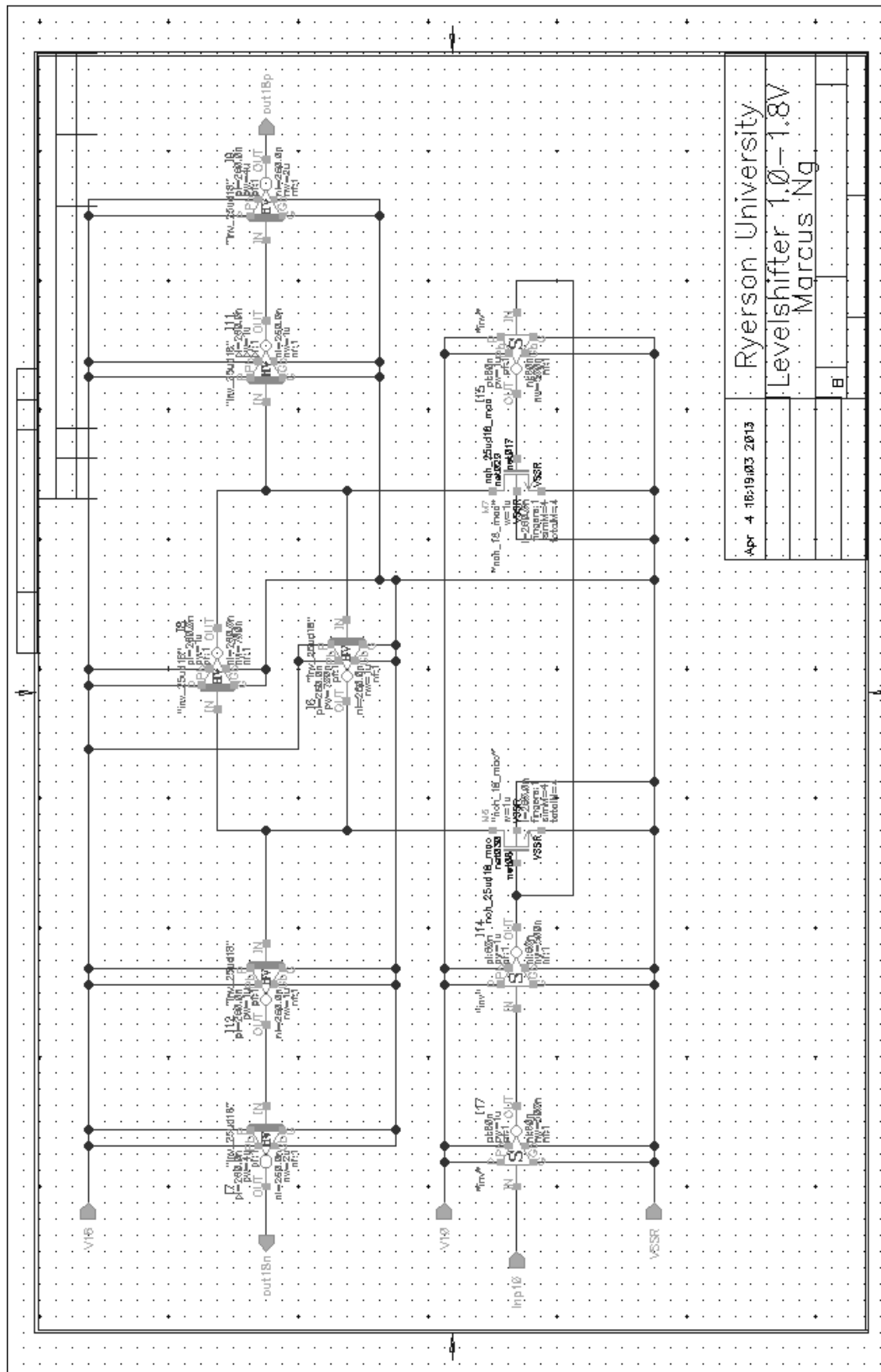**Figure 27: 200 MHz Tx Testbench (Zoomed) with PRBS Stimulus**

Figure 28: 1.0V-to-1.8V Levelshifter

Figure 29: 1.0V-to-1.8V Levelshifter Testbench

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