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# Five-level parallel current source converter for high power drives with DC current balance control and superior harmonic performance

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# Five-Level Parallel Current Source Converter for High Power Drives with DC Current Balance control and Superior Harmonic Performance

By

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**Bachelor of Science, University of Tehran, Tehran, Iran, 2008**

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# Five-Level Parallel Current Source Converter for High Power Drives with DC Current Balance Control and Superior Harmonic Performance

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Master of Applied Science
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# Abstract

In this thesis, space vector modulation is developed for a 5-level parallel current source converter for high power drives. The modulation scheme is designed to bring superior harmonic performance to the currents on the AC sides. This method synthesizes the rotating reference current vector in the converter's space vector plane with three adjacent switching vectors. Unbalanced currents of DC links become a practical challenge when two converters are connected in parallel. To balance the DC currents, the proper switching state for every Small and Medium switching vector is chosen from redundant switching states corresponding to the vector based on circuit circumstances and the designed switching sequence. Simulated results verify the effectiveness of the method. In addition, the switching sequence is designed to lower the switching frequency and minimize the switching loss. Finally, the proposed converter and switching scheme are simulated and steady state and dynamic performance are investigated in detail.

# Acknowledgment

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Last but not the least I should humbly thank my mother, Zhila my father, Rasool and the dearest sisters, Sevgili and Gilda who brought color, warmth and energy to my life. They were always supporting and inspiring me with their best wishes.

Dedicated to my grandmother

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# Chapter 1
# Introduction

Recent demand for speed drives in industrial applications at high power and medium voltages has prompted researchers to focus on multi-level converters. Multi-level voltage source inverter (VSI) drives have been applied in many industrial applications. In addition, to provide a higher power range, multi-level VSIs have some other benefits such as reductions in harmonics, $\frac{dv}{dt}$, electromagnetic interference and filter size. The most typical topologies include diode clamped inverters, H-bridge inverters and flying capacitor multi-level inverters. Since many voltage levels are needed in very high power usage, some problems limit the drives' functionality. Complex capacitor voltage control in diode clamped, costly and bulky phase-shifting transformer and reduced reliability caused by using so many low power components in H-bridge, and large amount of capacitors and pre-charged circuits in flying capacitor multi-level VSIs reduced the practical usage of these drives [1].

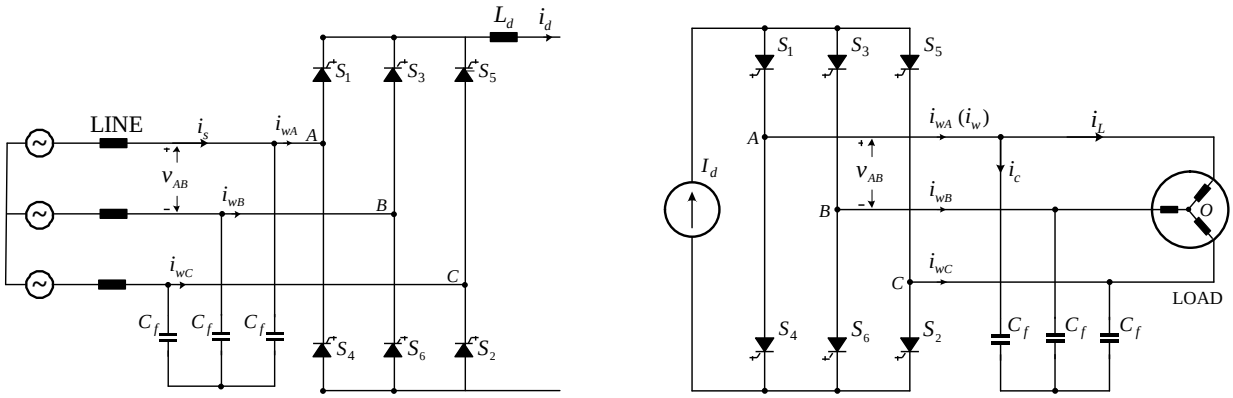
Voltage source converters (VSC) are widely used in industry, while current source converters (CSC) are primarily applied when fast dynamic performance is not needed such as in fans and pumps [2]. The PWM current source inverter (CSI) was proposed in the early 1970s [3] and gained more attention during the 1980s [4]. In comparison to VSCs, CSCs have a simpler topology with a lower switch count, friendly waveforms, inherent four quadrant operation and reliable overcurrent and short-circuit protection [5, 6].

In this thesis, a multi-level CSC is proposed for high and very high power applications. Comprehensive work was carried out to modify and develop space vector modulation (SVM) that

not only brings superior harmonic performance, but also provides a DC current balance control. This chapter introduces and analyzes single-bridge CSCs followed by elaboration of a multi-level CSC topology. The organization of the thesis is summarized at the end.

## 1.1 Single bridge current source converter

Fig. 1-1 shows a single-bridge current source rectifier (CSR) and a single-bridge current source inverter (CSI).




a) Single-bridge CSR b) Single-bridge CSI

Fig. 1-1 Single-bridge current source converters.

Six switches, two switches per leg, constitute every single-bridge CSC. Today, symmetrical type GCT devices with a reverse voltage blocking are used in CSCs. This kind of switches does not need anti-parallel free-wheeling diodes. When the rectifier is used as a front end in high power MV drives, two or more GCTs can be connected in series to provide a higher range of voltage.

Three-phase capacitors used in the input terminal of CSR and the output terminal of CSI are necessary in the commutation process. When each switch changes its state from ON to OFF, the

current in that switch decreases to zero in a very short time. This current needs a path to continue during the short commutation time or a huge voltage spike will be induced that damages the switching devices. Three-phase capacitor $C_f$ provides the path for the current of switches during the commutation of devices. In addition, the capacitors act as a high frequency harmonic filter, improving the AC current and the AC voltage waveforms. The capacitor's per-phase value depends on the switching frequency and the THD required for the line current. In addition, the input power factor and LC resonant mode should be counted on the rectifier side. Normally the capacitor per-phase value would be in the range of 0.3 to 0.6 pu for a high power CSC operating with a switching frequency of a few hundred Hz.

A DC choke $L_d$ is required for each DC link to maintain the DC output current within an acceptable range. Generally, the DC current should contain less than 15% ripple. The size of the DC choke is normally in the range of 0.5 to 0.8 pu.

PWM strategies are applied to generate acceptable input and output waveforms. Different switching strategies yield distinctive performances which may be applied in industry. It is very critical to analyze each of these features in order to match industry demand. Generally speaking, selective harmonic elimination (SHE) switching strategy provides higher harmonic performance, whereas SVM switching pattern brings higher dynamic performance and variable modulation index $m_a$ to the converter [6-8].

CSC possesses its own features, merits and drawbacks which are detailed as following [6-10].

1) Simple converter topology

CSC employs symmetrical gate commutated thyristor (GCT) devices. The AC voltage can reach up to 6.6 kV by simply connecting devices in series. Therefore, the topology retains its

simplicity and low device count even at high voltages. This feature is favorable in applications at high power and medium voltage.

2) AC line and AC load friendly waveforms

Employing PWM causes the input current of CSR and the output current of CSI to exhibit chopped-shaped waveforms. The three-phase capacitor will filter the chopped waveforms resulting in power supply side and load side currents that are close to sinusoidal. In addition, CSC inherently avoids high *dv/dt* and wave reflection issues.

3) Limited device switching frequency

To minimize power losses and device thermal stress, the device's switching frequency is usually limited to some hundred Hz.

4) Reliable short-circuit and overcurrent protection

VSC generates a large amount of short-circuit current because of the high voltage across the DC link capacitor and the very small inductance between the rectifier and the power supply. In contrast, DC link inductances of CSC limits the current changing rate if a line short-circuit fault occurs.

5) Limited dynamic performance

The main drawback of a CSC is its limited dynamic performance, which is caused by the large DC link inductance. In addition, a switching scheme such as SHE provides less flexibility. Advancements in device characteristics and optimized modulation schemes can improve the dynamic performance of CSC.

6) Possible LC resonances

The three-phase filter capacitor increases the possibility of LC resonances between the harmonic filter and the line inductances. Some active damping and power factor control methods are introduced to mitigate the possible resonances [11].

As mentioned, symmetrical GCT devices are used in CSCs. The input voltage is chosen from common medium range voltages including 2.3 kV, 3.3 kV, 4.16kV and 6.6kV. The output power rating is from 0.1 MW to 7 MW. Power demand in medium voltage applications such as pumps, fans, compressors and conveyors has been increased to more than 15 MW. Therefore, single-bridge CSC is unable to satisfy power demand of some drive applications. The need for drives with higher power ratings encourage researcher to extend work on high power drives. Multi-level CSC is one of the available solutions.

## 1.2 Multi-level current source converter

Industry demand for a higher power range and superior performance provide a vast opportunity to devise new converters which are a combination of conventional converters. This way, multi-level and multi-module converters came up. Multi-level converters have become an accepted and thus a commercially available alternative [12].

The main advantage of multi-level CSCs is that they provide a higher range of power. Employing specific configurations and applying moderated switching modulations brings higher performance and, consequently, more industry applications. Providing lower harmonic distortion on the AC side is one of the most significant benefits of using multi-level CSC. When using PWM strategies operated at acceptable switching frequencies, multi-level CSC generates AC

current and voltage waveforms which satisfy stringent harmonic requirements established by line and load standards.

On the other hand, increased size, additional mass and higher costs are inevitable when combining converters. In addition, control methods must be augmented to eliminate unwanted and adverse phenomena such as circulating current and unbalanced DC currents [13-16].

The configuration proposed and employed in this thesis is a back to back CSC, a multi-level CSR connected through a common DC link to a multi-level CSI. Each multi-level converter is built up by two parallel single-bridge CSCs. The AC source is connected to the rectifier side and the load is supplied from the inverter side. Fig. 1-2 illustrates a block diagram of the designed model.

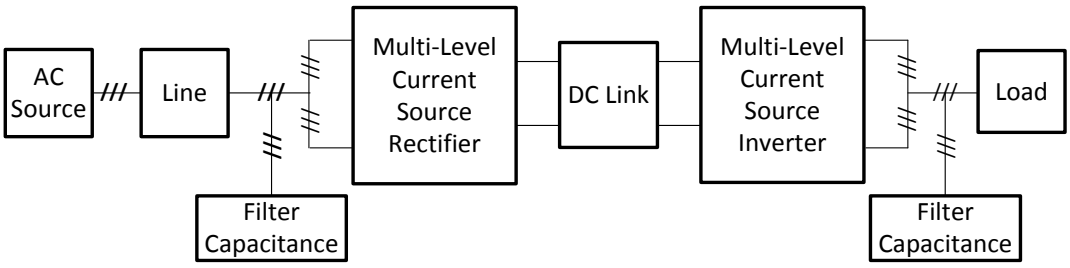



Fig. 1-2 System block diagram

The power source is a three-phase AC voltage in the medium voltage range (i.e. 4.16 kV) connected to a three-phase line which is modeled with a resistance and an inductance in series. The circuit topology is elaborated in detail for two rectifier and inverter sides.

### 1.2.1 Multi-level current source rectifier

Fig. 1-3 shows a 5-level parallel CSR constituted of two parallel single-bridge rectifiers. Corresponding AC phases are connected together at the input terminals and similar DC link buses

are connected at the output terminals of the multi-level rectifier. When the rectifier is used as a front end in high power MV drives, two or more GCTs can be connected in series to provide a higher range of voltage.

The three-phase capacitor $C_f$ at the input of the CSR assists in commutation of switches and provides a high order harmonic filter. As stated, the value of the capacitor per phase depends on the switching frequency, the input power factor and the LC resonant mode. Since the AC currents and voltages greeted by the multi-level converter contain less harmonic distortion, the size of the filter capacitor can be reduced to a great extent.

To limit the DC output current ripples to an acceptable range, a 0.5-0.8 pu DC choke $L_d$ is required for each DC link. There are a total of four DC chokes in the designed model.

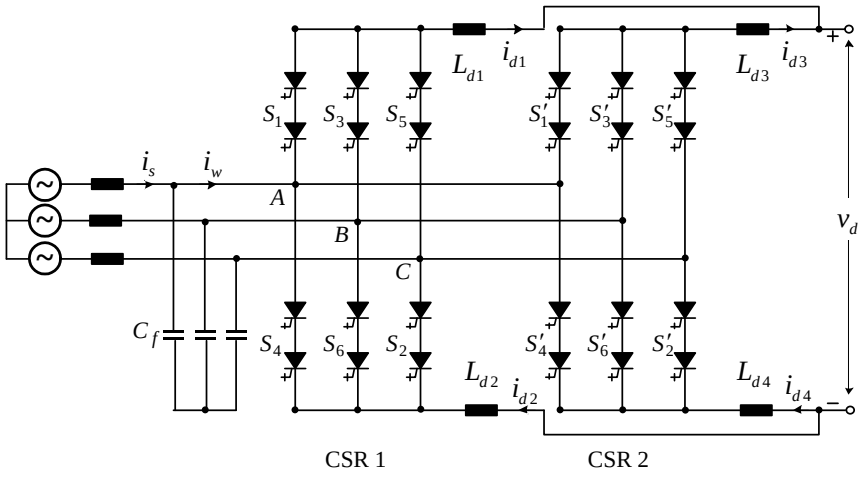



Fig. 1-3 5-level parallel current source rectifier

### 1.2.2 Multi-level current source inverter

Fig. 1-4 illustrates the 5-level CSI constituted of two parallel single-bridge inverters. The inverter is fed by DC current coming from the rectifier side through four DC inductances $L_{d1}$- $L_{d4}$. A three-phase capacitor is required at the output terminal of CSI.

## 1.3 PWM switching schemes

Any modulation scheme for the CSI must satisfy a basic constraint. At any time instant, two and only two switches in the converter, one connected to the positive DC bus and the other to the negative, must be ON to carry the DC current.

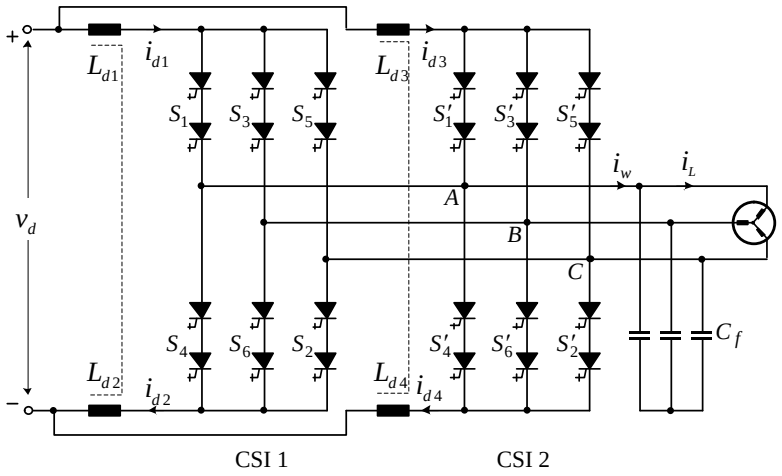



Fig. 1-4 5-level current source inverter

The major modulation schemes for the CSC are trapezoidal pulse-width modulation (TPWM), selective harmonic elimination (SHE) and space vector modulation (SVM). The above mentioned modulation schemes can be applied to both CSR and CSI. The typical switching frequency for practical high power CSC is about *400 Hz* to *600 Hz* [17].

### 1.3.1 Trapezoidal pulse-width modulation

The TPWM method is a carrier based modulation scheme. The carrier and modulation waves for TPWM are specially designed to meet the switching constraints in CSC. The design of TPWM ensures that during a $\frac{\pi}{3}$ period, three devices out of the six are always off. Among the remaining three, one device is always ON by keeping its carrier wave zero and modulation wave positive; the modulation and carrier waves for the other two devices are arranged to produce complementary gating signals such that only one of them is ON at any time instant. The switching constraints of CSC are thus satisfied.

TPWM is essentially an over-modulation scheme. Although it allows the modulation index to be changed from *0* to *1*, the controllable range of output current magnitude is quite limited. In addition, the switching scheme does not provide satisfactory harmonic performance. This is mainly because the trapezoidal modulation waveform itself contains the $5^{th}$ and $7^{th}$ harmonics.

### 1.3.2 Selective harmonic elimination

SHE is an offline designed modulation scheme that can eliminate a number of unwanted low order harmonics with limited number of pulses. In order to achieve better harmonic performance and to reduce the complexity in finding switching patterns solutions, the pulses are normally arranged in such a way that the derived waveforms have a quarter-wave symmetrical shape. The total number of harmonics to be eliminated by the SHE, *k*, is related to the number of pulses in each half fundamental cycle, $N_p$,

$$k = \frac{N_p - 1}{2} \tag{1.1}$$

There is one degree of freedom per each independent firing angle. Mainly, the degree of freedom gives the flexibility to either eliminate harmonics or control the magnitude. For

instance, with two firing angles, you may choose to eliminate two harmonics or eliminate a harmonic and provide an adjustable modulation index. However, a set of offline calculated angles is only valid at a certain modulation index. In practice, SHE is normally utilized with fixed modulation index. If variation of the modulation index is needed, the solutions for all the required modulation indices have to be calculated offline and stored in the system prior to operation. This adds to the complexity of system control and is not practical in real applications. Moreover, the calculation of SHE angle with a large number of pulses per fundamental cycle sometimes involves equations that have no solutions. For example, the SHE scheme is unable to eliminate $5^{th}$, $7^{th}$, $11^{th}$, $13^{th}$ and $17^{th}$ simultaneously.

In addition to being able to remove low order harmonics, which is important in power systems, there is a capability to eliminate other harmonics that could cause undesired situations such as LC resonance. For instance, there may be an obligation to eliminate $5^{th}$ and $11^{th}$ harmonics instead of $5^{th}$ and $7^{th}$.

### 1.3.3 Space vector modulation

Every switching state can be represented as a vector in the converters α-β space vector plane. The three phase currents can be transformed into two phase currents in α-β plane as represented below.

$$\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_{wA}(t) \\ i_{wB}(t) \\ i_{wC}(t) \end{bmatrix} \tag{1.2}$$

A resulted space vector can be expressed as equation (1.3).

$$\vec{I}(t) = i_\alpha(t) + j i_\beta(t) \tag{1.3}$$

The resulted vectors are shown in a diagram which is called space vector diagram. Since, the space vectors do not move, they are called stationary vectors. On the other hand, the desired

three-phase current on the AC side $i_w$ can be expressed as a reference vector rotating counterclockwise in the vector plane. Each revolution of the reference vector corresponds to an entire fundamental cycle of the AC current. In other words, the reference current vector rotates at the desired AC frequency. The ratio between the magnitudes of the reference vector and the DC current determines the modulation index of the converter.

The reference vector can be synthesized by the adjacent space vectors based on the principle of ampere-second balance. Several switching sequences are available but they are associated with different device switching frequencies and harmonic profiles.

The harmonic profile of the conventional SVM is undesirable for AC filter design in the CSC. The AC capacitor together with the power supply side inductance or machine side inductance will cause LC resonances. The resonance frequency is normally between 3.5pu to 4.5 pu of the fundamental frequency to ensure not only desired current quality but also acceptable cost. The low order harmonic currents, $5^{th}$ and $7^{th}$ orders in specific, will cause harmonic voltages as well as resonance problems.

### 1.3.4 Comparison of modulation schemes

SHE provides the best harmonic performance. It is widely used due to its capability of eliminating unwanted low order harmonics with limited switching frequency. However, smooth and flexible modulation index control in real-time is difficult since one set of firing angles is only optimized for a certain modulation index [18-20].

Both TPWM and SVM provide the flexibility of modulation index control. With gating signals generated in real time, both methods have excellent dynamic performances. The practical applications of TPWM and SVM in CSC have been limited to the low fundamental frequency range. This is because of the fact that their currents contain low order harmonics, lying very close to the resonance frequencies of the AC filters and will be amplified if the system damping

is insufficient. However, the TPWM has limited line-side power factor control as well as weak dynamic performance during startup [19-21].

In this thesis, SVM is chosen and will be designed and modified for 5-level parallel CSC. The modulation provides full range modulation index control. In addition, the harmonic profile of the AC currents and voltages will be improved to a great significant by generating multi-level waveforms.

## 1.4 Objectives

The main objective of this thesis is to research and develop a novel switching modulation for a 5-level parallel CSC to fulfill industry demands and constraints for high power drive applications. To aim proper objectives to the thesis, first, technical challenges and difficulties must be determined and studied. The industry demand brings distinctive technical challenges. However, some of them are common in most applications.

For instance, the proper operation of multi-level parallel CSC requires the operation of parallel converters with balanced DC link currents. The reasons behind unbalanced DC link currents are discussed later in detail in Chapter 3. However, it can be summarized that the operation of parallel current source converters in practice involves unbalanced DC currents. Operation under unbalanced DC currents is undesirable. Therefore, the need for a practical, effective and fast controller to balance the DC link currents is evident.

Every drive application requires specific harmonic performance. It is thus necessary to develop switching schemes and design controllers to satisfy such harmonic performance. As mentioned in section 1.3.4, the SVM generates AC waveforms with an amount of distortion that is not negligible. In specific, low order harmonics generated by SVM considerably limit the

application of SVM based switching schemes. Hence, the designed switching scheme must be modified and developed to improve the harmonic performance of the converter.

Another technical challenge is the limitation of the switching frequency. Higher switching frequency brings higher total loss and severe thermal stress to the converter system. It is more critical in high power applications, when the converter operates at higher currents and voltages, to limit the switching frequency. It is a great achievement to reach the same performance with lower switching frequency. In this thesis, the switching frequency is minimized without limiting the converter general performance.

Based on technical challenges and difficulties discussed above, several objectives are taken into account, summarized as follows.

**1) Balanced DC currents**

When connecting two converters in parallel, (either rectifiers or inverters), there will be two positive DC link buses and two negative DC link buses. Different circuit parameters, especially manufacturing tolerance in DC chokes and un-equal ON-state voltages of the switching devices may cause unbalanced DC link currents. Generally speaking, unbalanced DC currents generate current harmonics and higher current distortion. In addition, the imbalance increases total loss of the system and leads to uneven division of power between parallel converters. Therefore, the designed switching modulation must generate balanced DC link currents. An additional controller is necessary to secure balanced DC current (the “DC current balance control”).

**2) Low harmonic distortion**

Multi-level CSC can improve the harmonic distortion content of AC currents and voltages if the switching scheme is designed properly. In this thesis, the switching scheme is designed to decrease the distortion of AC waveforms and improve the harmonic profile of the AC line and

AC load currents and voltages. The improved converter does not need a large filter capacitor to satisfy stringent AC side harmonic demands. Therefore, the size of the filter capacitor can be reduced. In addition, decreasing the low order harmonics will eliminate the need for costly and bulky phase-shifting transformers.

**3) Minimized switching frequency**

Switching the device less frequently reduces the switching loss and places less thermal stress on each device. It is more critical in high power drive application in specific to limit the switching frequency. Usually, the switching frequency is limited to a few hundred Hertz in high power drive applications. In this thesis, the switching sequence is designed to minimize the switching frequency as much as possible.

**4) Dynamic performance**

As mentioned, the main drawback of a CSC is its limited dynamic performance. Providing active full range modulation index control improves the dynamic performance of converter. SHE switching modulation as dominant switching modulation for CSCs employs off-line tables for different modulation indices and thus cannot provide continuous $m_a$ control. On the other hand, SVM is capable of providing full range active control. Consequently, the active $m_a$ control on the CSR maintains the DC current at the desired value while the active $m_a$ control on the CSI adjusts the AC load voltage at the desired value. In this way, the conducted power is adjusted through the value of the DC link current and adjustable load voltage is achievable.

## 1.5 Thesis outline

In this thesis, a novel SVM switching scheme is introduced and elaborated for a 5-level parallel CSC which is applicable on both 5-level parallel CSRs and CSIs. The modulation is augmented

with DC current balance control. The modulation is designed to bring superior harmonic and dynamic performance to the converter system. This thesis consists of six chapters.

Chapter 1 presents the background and introduction of the thesis.

Chapter 2 elaborates the proposed SVM method. Several aspects such as switching states, switching vectors, space vector diagram, reference vector and dwell times are reviewed.

Chapter 3 develops the DC current balance control. Effects of redundant switching states on DC currents are investigated. Small and Medium vectors are employed to balance the DC link currents.

Chapter 4 investigates the steady state and dynamic performance of the proposed modulation. Several aspects such as harmonic profile, DC current control and AC load voltage control.

Chapter 5 summarizes the main contributions and conclusions of the thesis.

# Chapter 2
# Space Vector Modulation for 5-Level Current Source Converter

## 2.1 Introduction

Several switching modulations are available for multi-level current source converters (CSC). In this thesis, space vector modulation (SVM) is chosen to satisfy the objectives of the design. The basic idea of SVM was presented in the previous chapter. In this chapter, SVM method is specifically modified and developed for 5-level parallel current source converter in specific. The available switching states are introduced. Every switching state can be represented by a vector in the space vector plane. The resulted space vectors constitute the space vector diagram. The switching method of SVM is elaborated thereafter. Three adjacent space vectors are chosen for each area of space vector diagram to synthesize the reference current vector. The order of vectors is designed to minimize the switching frequency. Dwell time calculations are presented at the end of this chapter.

## 2.2 Switching states

Several switching modulations are available for multi-level CSCs. Generally, whichever one is used as a switching modulation, it should satisfy two requirements: the DC current $i_d$ should be continuous and the switching chopped current $i_w$ should be defined [3]. Disregarding to the first

requirement causes very high voltage induced by the DC choke and damages the switches. The second requirement is the main objective of the switching scheme.

Obviously, with no or only one switch ON, the requirement of continuous DC current cannot be satisfied. With more than two switches ON simultaneously, the output current will not follow the switching pattern. In this case, the output current is AC side- line in rectifiers and load in inverters- dependent. So, each switching state should have only two switches ON, one in the top half of the bridge and the other in the bottom half. This rule excludes commutation intervals. Consequently, any designed switching scheme, whether for current source rectifier (CSR) or current source inverter (CSI), must satisfy a constraint that only two switches can be at ON state, one connected to the positive DC bus while the other is connected to the negative DC bus.

Three switches are available at each half of the CSC. One of them must be selected to be at ON state. The others will be remained OFF. Consequently, there are 9 switching states available at each converter. Two converters are connected in parallel to constitute the multi-level converter. Under the mentioned constraint, 81 switching states are feasible in total. Table 2-1 provides the available switching states. Every switching state is represented by 4 digits. The first 2 digits express two switches ON in the first converter and the second 2 digits state two switches ON in the second converter. For example, the expression [16 56] represents the switching state in which switches number 1 and 6 in the first converter and switches number 5 and 6 in the second converter are at ON state. Fig. 2-1 illustrates the current paths when the mentioned switching state is applied in the multi-level parallel CSI.

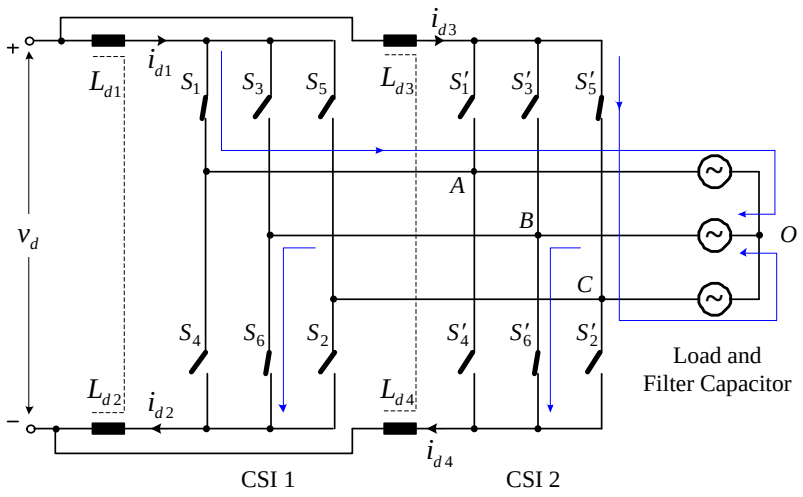



Fig. 2-1 Current paths in parallel inverters with switching state [16 56].

Table 2-1 Switching states.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| [12 12] | [12 32] | [12 52] | [12 16] | [12 36] | [12 56] | [12 14] | [12 34] | [12 54] |
| [32 12] | [32 32] | [32 52] | [32 16] | [32 36] | [32 56] | [32 14] | [32 34] | [32 54] |
| [52 12] | [52 32] | [52 52] | [52 16] | [52 36] | [52 56] | [52 14] | [52 34] | [52 54] |
| [16 12] | [16 32] | [16 52] | [16 16] | [16 36] | [16 56] | [16 14] | [16 34] | [16 54] |
| [36 12] | [36 32] | [36 52] | [36 16] | [36 36] | [36 56] | [36 14] | [36 34] | [36 54] |
| [56 12] | [56 32] | [56 52] | [56 16] | [56 36] | [56 56] | [56 14] | [56 34] | [56 54] |
| [14 12] | [14 32] | [14 52] | [14 16] | [14 36] | [14 56] | [14 14] | [14 34] | [14 54] |
| [34 12] | [34 32] | [34 52] | [34 16] | [34 36] | [34 56] | [34 14] | [34 34] | [34 54] |
| [54 12] | [54 32] | [54 52] | [54 16] | [54 36] | [54 56] | [54 14] | [54 34] | [54 54] |

## 2.3 Space vectors

Each switching state can be represented by a vector in the converter's space vector plane. To derive the relationship between the switching states and space vectors assume that the converter whether rectifier or inverter is at balanced three phase operation. Therefore,

$$i_{wA}(t)+i_{wB}(t)+i_{wC}(t)=0 \tag{2.1}$$

where $i_{wA}$, $i_{wB}$ and $i_{wC}$ are the instantaneous AC side currents, before the filter capacitor, corresponding to phases A, B and C respectively. The three phase currents can be transformed into two phase currents in α-β plane as represented below.

$$\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_{wA}(t) \\ i_{wB}(t) \\ i_{wC}(t) \end{bmatrix} \tag{2.2}$$

A resulted space vector can be expressed as equation (2.3).

$$\vec{I}(t) = i_\alpha(t) + j i_\beta(t) \tag{2.3}$$

which can be rewritten as equation (2.4).

$$\vec{I}(t) = \frac{2}{3}\left[ i_{wA}(t)e^{j0} + i_{wB}(t)e^{j\frac{2\pi}{3}} + i_{wC}(t)e^{j\frac{4\pi}{3}} \right] \tag{2.4}$$

in which $i_{wA}$, $i_{wB}$ and $i_{wC}$ are determined according to the switching state. For example, for the switching state [16 56] mentioned before, switching currents are presented at (2.5).

$$i_{wA} = \frac{I_d}{2},\ i_{wB} = -I_d,\ i_{wC} = \frac{I_d}{2} \tag{2.5}$$

Substituting the switching currents into equation (2.4), the resulted vector of switching state [16 56] can be driven as equation (2.6).

$$\vec{I}_{[16\ 56]} = I_d\ e^{j-60} \tag{2.6}$$

The same calculations can be derived and the corresponding space vector is found for the other switching states. Some of the switching states result in a same vector. Considering that, there are 19 space vectors in total. These vectors are divided to 4 different kinds based on their length; Large, Medium, Small and Zero.

### 2.3.1 Large vectors

Assume that the converter is operating at the switching state [16 16]. Under the mentioned condition,

$$i_{wA} = I_d,\ i_{wB} = -I_d,\ i_{wC} = 0 \tag{2.7}$$

Substituting the switching currents into equation (2.4), the resulted vector of switching state [16 16] can be driven as equation (2.8).

$$\vec{I}_{[16\ 16]} = \frac{2\sqrt{3}}{3} I_d\ e^{j-30} \tag{2.8}$$

This vector and 5 other vectors have the largest length among space vectors. Table 2-2 presents the switching states result in Large vectors and the corresponding space vectors. Large vectors are labeled $\vec{I}_1$ to $\vec{I}_6$.

Table 2-2 Large switching states.

| Switching State | Vector | Space Vector |
|---|---|---|
| [16 16] | $\frac{2\sqrt{3}}{3} I_d\ e^{j-30}$ | $\vec{I}_1$ |
| [12 12] | $\frac{2\sqrt{3}}{3} I_d\ e^{j30}$ | $\vec{I}_2$ |
| [32 32] | $\frac{2\sqrt{3}}{3} I_d\ e^{j90}$ | $\vec{I}_3$ |
| [34 34] | $\frac{2\sqrt{3}}{3} I_d\ e^{j150}$ | $\vec{I}_4$ |
| [54 54] | $\frac{2\sqrt{3}}{3} I_d\ e^{j-150}$ | $\vec{I}_5$ |
| [56 56] | $\frac{2\sqrt{3}}{3} I_d\ e^{j-90}$ | $\vec{I}_6$ |

Large vectors employ same switches at both converters. In other words, current paths are symmetrical in both converters. Since, the same AC phases are connected to converters, equal voltages are applied to DC link chokes. Identical changes to DC link currents are expected.

### 2.3.2 Medium vectors

Assume that the converter is operating at the switching state [12 16]. Under the mentioned condition,

$$i_{wA} = I_d,\ i_{wB} = \frac{-I_d}{2},\ i_{wC} = \frac{-I_d}{2} \tag{2.9}$$

Substituting the switching currents into equation (2.4), the resulted vector of switching state [12 16] can be driven as equation (2.10).

$$\vec{I}_{[12\ 16]} = I_d\ e^{j0} \tag{2.10}$$

Now, assume that the converter is operating at the switching state [16 12]. Under the mentioned condition,

$$i_{wA} = I_d,\ i_{wB} = \frac{-I_d}{2},\ i_{wC} = \frac{-I_d}{2} \tag{2.11}$$

Substituting the switching currents into equation (2.4), the resulted vector of switching state [16 56] can be driven as equation (2.12).

$$\vec{I}_{[16\ 12]} = I_d\ e^{j0} \tag{2.12}$$

In conclusion, switching states [12 16] and [16 12] result in an identical space vector. This vector and 5 other vectors resulted from 12 switching states, have same length among space

vectors. Table 2-3 presents the switching states result in Medium vectors and the corresponding space vectors. Medium vectors are labeled $\vec{I}_7$ to $\vec{I}_{12}$.

Table 2-3 Medium switching states.

| Switching State | | Vector | Space Vector |
|---|---|---|---|
| [12 16] | [16 12] | $I_d\ e^{j0}$ | $\vec{I}_7$ |
| [32 12] | [12 32] | $I_d\ e^{j60}$ | $\vec{I}_8$ |
| [32 34] | [34 32] | $I_d\ e^{j120}$ | $\vec{I}_9$ |
| [34 54] | [54 34] | $I_d\ e^{j180}$ | $\vec{I}_{10}$ |
| [54 56] | [56 54] | $I_d\ e^{j-120}$ | $\vec{I}_{11}$ |
| [16 56] | [56 16] | $I_d\ e^{j-60}$ | $\vec{I}_{12}$ |

There are two redundant switching states for every Medium vector. In fact, two redundant switching states employ same switches on either top half or bottom half. Different switches are at ON state for the other half. Since, different phases are connected to DC links in converters, asymmetrical changes on DC links are expected.

### 2.3.3 Small vectors

Assume that the converter is operating at the switching state [14 16]. Under the mentioned condition,

$$i_{wA} = \frac{I_d}{2},\ i_{wB} = \frac{-I_d}{2},\ i_{wC} = 0 \tag{2.13}$$

Substituting the switching currents into equation (2.4), the resulted vector of switching state [14 16] can be driven as equation (2.14).

$$\vec{I}_{[14\ 16]} = \frac{\sqrt{3}}{3} I_d\ e^{j-30} \tag{2.14}$$

The switching state [16 14] results in the same vector. Operating at these two switching states, one of the converters bypasses the DC current to the AC side through switches 1 and 4, while DC current is conducted to the AC side through switches 1 and 6. In addition to mentioned switching states, switching states [16 36], [36 16], [16 52] and [52 16] bring the same manner to the converter. The only difference is that the bypass process is conducted through other phases. As expected, calculations show the same space vector resulted from the mentioned switching states.

Now, assume that the converter is operating at the switching states [56 12] or [12 56]. Under the mentioned condition,

$$i_{wA} = \frac{I_d}{2},\ i_{wB} = \frac{-I_d}{2},\ i_{wC} = 0 \tag{2.15}$$

Substituting the switching currents into equation (2.4), the resulted vector of switching state [12 56] can be driven as equation (2.16).

$$\vec{I}_{[56\ 12]} = \frac{\sqrt{3}}{3} I_d\ e^{j-30} \tag{2.16}$$

The resulted vector is same as the last mentioned vector. Although none of the converters bypasses the DC current, the bypass process is conducted with cooperation of two converters on phase C. Phase C is not involved in conduction process which is still carried out with switches 1 and 6.

In summary, 8 redundant switching states result in an identical Small medium vector. This vector and 5 other vectors resulted from 48 switching states, have same length among space vectors. Table 2-4 presents the switching states result in Small vectors and the corresponding space vectors. Small vectors are labeled $\vec{I}_{13}$ to $\vec{I}_{18}$. Since, different phases are connected to DC links in two converters, asymmetrical changes are expected.

Table 2-4 Small switching states.

| Switching State | | | | Vector | Space Vector |
|---|---|---|---|---|---|
| [16 14] | [16 36] | [16 52] | [12 56] | $\frac{\sqrt{3}}{3} I_d \, e^{j-30}$ | $\vec{I}_{13}$ |
| [14 16] | [36 16] | [52 16] | [56 12] | | |
| [12 14] | [12 36] | [12 52] | [16 32] | $\frac{\sqrt{3}}{3} I_d \, e^{j90}$ | $\vec{I}_{14}$ |
| [14 12] | [36 12] | [52 12] | [32 16] | | |
| [32 14] | [32 36] | [32 52] | [34 12] | $\frac{\sqrt{3}}{3} I_d \, e^{j-150}$ | $\vec{I}_{15}$ |
| [14 32] | [36 32] | [52 32] | [12 34] | | |
| [34 14] | [34 36] | [34 52] | [32 54] | $\frac{\sqrt{3}}{3} I_d \, e^{j-30}$ | $\vec{I}_{16}$ |
| [14 34] | [36 34] | [52 34] | [54 32] | | |
| [54 14] | [54 36] | [54 52] | [56 14] | $\frac{\sqrt{3}}{3} I_d \, e^{j90}$ | $\vec{I}_{17}$ |
| [14 54] | [36 54] | [52 54] | [14 56] | | |
| [56 14] | [56 36] | [56 52] | [54 16] | $\frac{\sqrt{3}}{3} I_d \, e^{j-150}$ | $\vec{I}_{18}$ |
| [14 56] | [36 56] | [52 56] | [16 54] | | |

### 2.3.4 Zero vector

Assume that the converter is operating at the switching state [14 14] where both converters bypass the DC link current. Under the mentioned condition,

$$i_{wA} = 0, \; i_{wB} = 0, \; i_{wC} = 0 \tag{2.17}$$

Substituting the switching currents into equation (2.4), the resulted vector of switching state [14 14] can be driven as equation (2.18).

$$\vec{I}_{[14\,14]} = 0 \tag{2.18}$$

The same vector is expected when bypass process is conducted through two other phases. In other words, switching states [36 36] and [52 52] result in Zero vector too. In addition, the

switching states [14 36], [14 52], [36 14], [36 52], [52 14] and [52, 32] bypass the DC currents with cooperation of different phases. These switching states result in Zero vector as well.

Now, assume that the converter is operating at the switching state [12 54] or [54 12] where DC current is bypassed with cooperation of two converters. Under the mentioned condition,

$$i_{wA} = 0,\ i_{wB} = 0,\ i_{wC} = 0 \tag{2.19}$$

Substituting the switching currents into equation (2.4), the resulted vector of switching state [12 54] can be driven as equation (2.20).

$$\vec{I}_{[12\ 54]} = 0 \tag{2.20}$$

The same result is expected for operation under switching states [16 34], [34 16], [32 56] and [56 32].

In conclusion, 15 redundant switching states operate as Zero vector. Table 2-5 presents the switching states result in Zero vector and the corresponding space vectors. Zero vector is labeled $\vec{I}_{19}$. Some statistical points are summarized in Table 2-6.

Table 2-5 Zero switching states.

| **Switching State** | | | **Vector** | **Space Vector** |
|---|---|---|---|---|
| [14 14] | [36 36] | [52 52] | 0 | $\vec{I}_{19}$ |
| [14 36] | [36 52] | [52 14] | | |
| [36 14] | [52 36] | [14 52] | | |
| [12 54] | [34 16] | [56 32] | | |
| [54 12] | [16 34] | [32 56] | | |

Table 2-6 Space vectors specifications.

| Space Vector Type | Large | Medium | Small | Zero |
|---|---|---|---|---|
| **Length of Vectors** | $\frac{2\sqrt{3}}{3} I_d$ | $I_d$ | $\frac{\sqrt{3}}{3} I_d$ | 0 |
| **Number of Vectors** | 6 | 6 | 6 | 1 |
| **Number of Switching States** | 6 | 12 | 48 | 15 |
| **Number of Redundant States** | 1 | 2 | 8 | 15 |

## 2.4 Space vector diagram

Eighty one switching states result in 19 space vectors. Space vectors form the space vector diagram. Fig. 2-2 illustrates the space vector diagram.

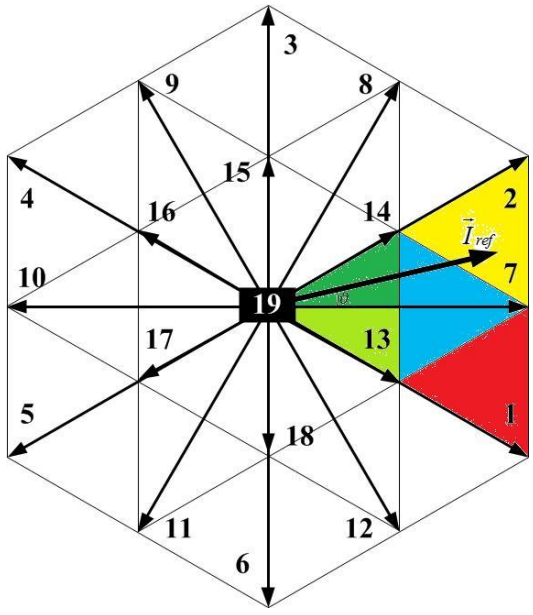



Fig. 2-2 Space vector diagram

In addition to 19 stationary space vectors, one rotating vector is presented on the space vector plane. This vector which is the reference current vector $\vec{I}_{ref}$ , determines the AC current produced with space vector modulation. In other words, the three-phase AC current is expressed as $\vec{I}_{ref}$ that rotates with the desired AC frequency (i.e. 60Hz). The length of $\vec{I}_{ref}$ represents the magnitude of the AC current determined by the modulation index $m_a$ as described in equation (2.21).

$$m_a = \frac{I_{ref}}{i_d} \tag{2.21}$$

The angle of the reference vector $\theta$ determiners the phase of the produced AC current. The purpose of the space vector modulation is to estimate the reference vector with the space vectors. A better estimation of the reference vector brings a better performance to the converter system. To improve the estimation of the reference vector space vector plane is divided to smaller areas. Consequently, the reference current vector is synthesized with closest vectors at each smaller area.

As illustrated in Fig. 2-2, Large vectors divide the space vector plane into 6 sectors. For instance, sector 1 is an area between Large vector 1 and Large vector 2. To improve the estimation of the reference current vector, every sector is divided into 4 regions. Consequently, 24 triangular areas constitute the space vector diagram. The space vector modulation chooses three closest vectors at each area to synthesize the reference current vector.

## 2.5 Vector selection

According to the area that the reference current vector is located in, three vectors estimate the reference vector. As the first step in switching sequence design, three vectors should be selected for every area in the space vector plane.

Sector number 1 is divided into four triangular areas and the assigned number is called region number. Fig. 2-3 illustrates the details of the region numbering. Three switching vectors should be selected for each region. The selected vectors must be able to synthesize every reference vector located in the assigned triangle. In addition, being closer to the triangle, brings a better estimation of the reference current. Vector selection process is presented for outer triangles and inner triangles of sector 1 separately. When the modulation index $m_a$ has lower values, the reference current vector is located in inner triangle R1 (region 1). When the modulation index $m_a$ has higher values, the reference current vector is located in outer triangles labeled with R2 for region 2, R3 for region 3 or R4 for region 4.

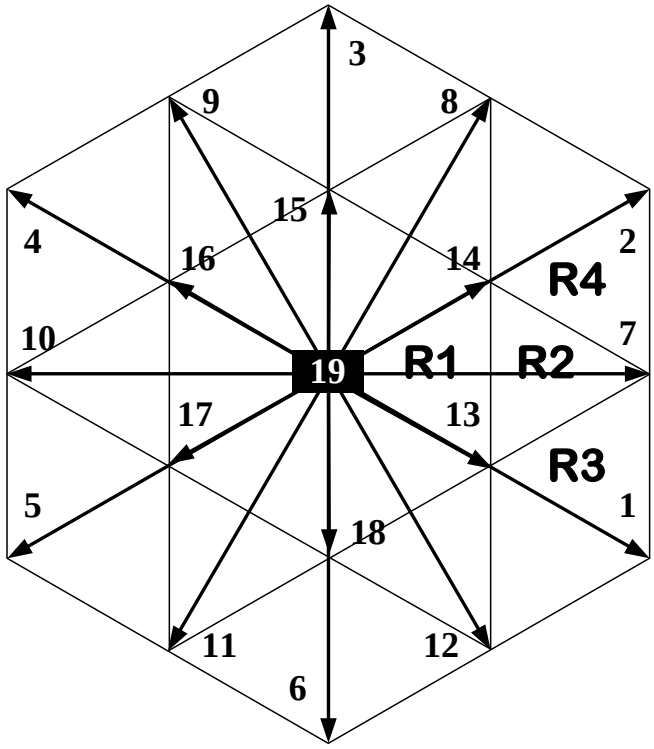



Fig. 2-3 Space vector diagram- region numbering

a) Region 1

In design of switching sequence it is necessary to satisfy the constraint that the transient from one vector to another involves at most one device switch-ON and one device switch-OFF at each inverter to produce a lower switching frequency and minimize the switching loss.

The first guess of switching vectors is ($\vec{I}_{13}, \vec{I}_{19}, \vec{I}_{14}$). Since, the negative DC bus currents are controlled in sector 1, two switching states [14 16] and [16 14] are available for Small vector $\vec{I}_{13}$. Since, the positive DC bus currents are controlled in sector 6, two switching states [36 16] and [16 36] are available for Small vector $\vec{I}_{13}$. If Small vector $\vec{I}_{13}$ is chosen for transient vector between sectors 1 and 6, there might be a transient from switching states [14 16] to [36 16] or [16 14] to [16 36] which include two switches turn-OFF and turn-ON in one of converters. The same analysis can be done for Small vector $\vec{I}_{14}$ in sectors 1 and 2. Consequently, two Small vectors $\vec{I}_{13}$ and $\vec{I}_{14}$ are not proper choices to role as transient vectors.

The other guess of switching vectors is ($\vec{I}_{1}, \vec{I}_{19}, \vec{I}_{2}$). Employing Large vectors $\vec{I}_{1}$ and $\vec{I}_{2}$ as transient vectors solves the issue mentioned before. Unfortunately, there is no Medium or Small vector among the vector set which is necessary for the DC current balance control. In addition, employing two Large vectors in region 1 causes a very high dwell time for Zero vector. Subsequently, degrade in harmonic performance is inevitable. To solve the problem, region 1 is divided to two smaller areas which are called Down and Up. Medium vector $\vec{I}_{7}$ divides triangle 1 to two smaller right triangles which are called Down and Up.

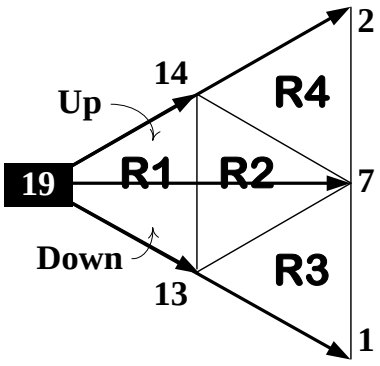



Fig. 2-4 Space vector plane (sector one)

Fig. 2-4 depicts sector 1 and sub-triangles of the sector. The vector sets of ($\vec{I}_{19}, \vec{I}_{13}, \vec{I}_{7}$) and ($\vec{I}_{7}, \vec{I}_{14}, \vec{I}_{19}$) are selected corresponding to Down and Up triangles respectively. Each set includes one Medium, one Small and Zero vector.

b) Region 2

Two sets of options are available for triangle 2 which are ($\vec{I}_{1}, \vec{I}_{19}, \vec{I}_{2}$) and ($\vec{I}_{13}, \vec{I}_{7}, \vec{I}_{14}$). The first set employs Zero vector $\vec{I}_{19}$. Employing Zero vector increases the distortion content of the AC currents and voltages. Besides, Medium and Small vectors are essential in DC current balance control. There is not any Medium or Small vector among first set of vectors which is necessary for DC current balance control. The second set of vectors includes two Small vectors and one Medium vector. These three vectors are employed to synthesize the reference current vector when located in triangle 2.

c) Region 3

The vector set of ($\vec{I}_{1}, \vec{I}_{7}, \vec{I}_{13}$) is selected for triangle 3. The set includes one Large, one Medium and one Small vector.

d) Region 4

The vector set of ($\vec{I}_{14}, \vec{I}_{7}, \vec{I}_{2}$) is selected for triangle 4. The set includes one Large, one Medium and one Small vector.

The same study can be done for the rest of the space vector plane. Each sector can be mirrored on sector 1 and the current vectors are selected same as sector 1. Table 2-7 presents the selected three vectors corresponding to each triangle of the space vector plane.

Table 2-7 Selected vectors for each triangular area of space vector plane.

| | Region | | Vectors | | | | Region | | Vectors | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | a | b | c | | | | a | b | c |
| **Sector 1** | **R1** | **Down** | $\vec{I}_{19}$ | $\vec{I}_{13}$ | $\vec{I}_{7}$ | **Sector 4** | **R1** | **Down** | $\vec{I}_{19}$ | $\vec{I}_{16}$ | $\vec{I}_{10}$ |
| | | **Up** | $\vec{I}_{7}$ | $\vec{I}_{14}$ | $\vec{I}_{19}$ | | | **Up** | $\vec{I}_{10}$ | $\vec{I}_{17}$ | $\vec{I}_{19}$ |
| | **R2** | | $\vec{I}_{13}$ | $\vec{I}_{7}$ | $\vec{I}_{14}$ | | **R2** | | $\vec{I}_{16}$ | $\vec{I}_{10}$ | $\vec{I}_{17}$ |
| | **R3** | | $\vec{I}_{1}$ | $\vec{I}_{7}$ | $\vec{I}_{13}$ | | **R3** | | $\vec{I}_{4}$ | $\vec{I}_{10}$ | $\vec{I}_{16}$ |
| | **R4** | | $\vec{I}_{14}$ | $\vec{I}_{7}$ | $\vec{I}_{2}$ | | **R4** | | $\vec{I}_{17}$ | $\vec{I}_{10}$ | $\vec{I}_{5}$ |
| **Sector 2** | **R1** | **Down** | $\vec{I}_{19}$ | $\vec{I}_{14}$ | $\vec{I}_{8}$ | **Sector 5** | **R1** | **Down** | $\vec{I}_{19}$ | $\vec{I}_{17}$ | $\vec{I}_{11}$ |
| | | **Up** | $\vec{I}_{8}$ | $\vec{I}_{15}$ | $\vec{I}_{19}$ | | | **Up** | $\vec{I}_{11}$ | $\vec{I}_{18}$ | $\vec{I}_{19}$ |
| | **R2** | | $\vec{I}_{14}$ | $\vec{I}_{8}$ | $\vec{I}_{15}$ | | **R2** | | $\vec{I}_{17}$ | $\vec{I}_{11}$ | $\vec{I}_{18}$ |
| | **R3** | | $\vec{I}_{2}$ | $\vec{I}_{8}$ | $\vec{I}_{14}$ | | **R3** | | $\vec{I}_{5}$ | $\vec{I}_{11}$ | $\vec{I}_{17}$ |
| | **R4** | | $\vec{I}_{15}$ | $\vec{I}_{8}$ | $\vec{I}_{3}$ | | **R4** | | $\vec{I}_{18}$ | $\vec{I}_{11}$ | $\vec{I}_{6}$ |
| **Sector 3** | **R1** | **Down** | $\vec{I}_{19}$ | $\vec{I}_{15}$ | $\vec{I}_{9}$ | **Sector 6** | **R1** | **Down** | $\vec{I}_{19}$ | $\vec{I}_{18}$ | $\vec{I}_{12}$ |
| | | **Up** | $\vec{I}_{9}$ | $\vec{I}_{16}$ | $\vec{I}_{19}$ | | | **Up** | $\vec{I}_{12}$ | $\vec{I}_{13}$ | $\vec{I}_{19}$ |
| | **R2** | | $\vec{I}_{15}$ | $\vec{I}_{9}$ | $\vec{I}_{16}$ | | **R2** | | $\vec{I}_{18}$ | $\vec{I}_{12}$ | $\vec{I}_{13}$ |
| | **R3** | | $\vec{I}_{3}$ | $\vec{I}_{9}$ | $\vec{I}_{15}$ | | **R3** | | $\vec{I}_{6}$ | $\vec{I}_{12}$ | $\vec{I}_{18}$ |
| | **R4** | | $\vec{I}_{16}$ | $\vec{I}_{9}$ | $\vec{I}_{4}$ | | **R4** | | $\vec{I}_{13}$ | $\vec{I}_{12}$ | $\vec{I}_{1}$ |

## 2.6 Space vector order design to achieve the minimized switching frequency

The proper switching sequence should accomplish the following:

a) Produce AC currents and voltages with acceptable harmonic distortion on the AC side. Dividing the space vector diagram into smaller areas and selecting proper switching vectors to estimate the reference current vector provide AC currents and voltages with low distortion content.

b) Bring the identical switching frequency and switching sequence in both inverters. Satisfying this constraint secures an equal fatigue and heat design to parallel converters.

c) Satisfy the constraint that the transient from one vector to another involves at most one device switch-ON and one device switch-OFF at each converter to produce a lower switching frequency and minimize the switching loss. However, to produce a lower device switching frequency the switching sequence is designed to minimize the device switching frequency. In this chapter, the switching vector order is designed to minimize the switching frequency.

The space vector order is analyzed in detail for sector 1. The order of vectors at each region is designed in such a way to transient from one switching state to another involves minimum number of devices. Assume that the modulation index has a high value and the reference current is located in region 3 of sector 1. Fig. 2-5 illustrates the location of the reference current vector.

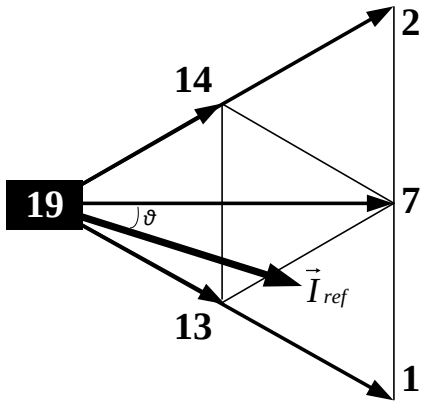



Fig. 2-5 Space vector plane- sector 1, region 3

As discussed heretofore, the vector set of ($\vec{I}_1$, $\vec{I}_7$, $\vec{I}_{13}$) is chosen to estimate the reference current vector. For Large vector $\vec{I}_1$ only switching state [16 16] is available. For Medium vector $\vec{I}_7$ two switching states which are [12 16] and [16 12] are available. DC current balance control chooses the proper switching state based on the circuit circumstances. For Small vector $\vec{I}_{13}$ eight switching states are available. However, only two of them which are [16 14] and [14 16] are taken into consideration according to the discussions on the DC current balance control.

Large vector $\vec{I}_1$ is common in region 3 of sector 1 and region 4 of sector 6. By ending the sector 6 switching and starting the switching of sector 1 with vector $\vec{I}_1$ there will be no device switching in transient from sector 6 to sector 1. Both vectors $\vec{I}_7$ and $\vec{I}_{13}$ are common in region 3 and region 2 and all regions 3, 2 and 4 contain Medium vector $\vec{I}_7$. Assigning Medium vector $\vec{I}_7$ as the middle switching vector in regions 3, 2 and 4 of sector 1, symmetry is brought to the switching vectors. Subsequently, Small vector $\vec{I}_{13}$ is considered as the third vector in region 3. Selecting the same vector as the first vector of region 2, transient from region 3 to region 2 involves an identical vector. Consequently, no or one device switching appears at each parallel

converter. Table 2-9 provides the switching sequence of region 3 of sector 1. It is obvious that transient from one vector to next vector involves at most one switching at each converter.

Table 2-8 Vector order- sector 1, region 3.

| **Sector 1** | | **Region 3** | |
|---|---|---|---|
| **Switching Vector** | $\vec{I}_1$ | $\vec{I}_7$ | $\vec{I}_{13}$ |
| **Switching State** | [16 16] | [16 12] | [14 16] |
| | | [12 16] | [16 14] |

As time runs, the reference current vector rotates and moves to region 2 of sector 1. Fig. 2-6 illustrates the location of the reference current vector.

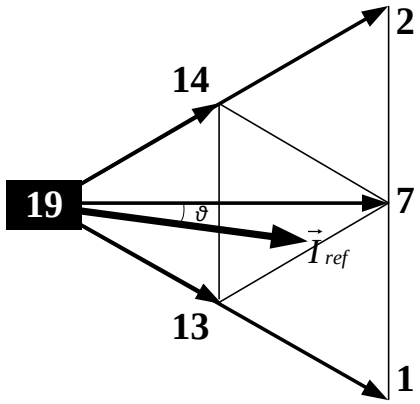



Fig. 2-6 Space vector plane- sector 1, region 2

As discussed heretofore, the vector set of ($\vec{I}_{13}, \vec{I}_7, \vec{I}_{14}$) is chosen to estimate the reference current vector. For Medium vector $\vec{I}_7$ two switching states which are [12 16] and [16 12] are available. The DC current balance control chooses the proper switching state based on the circuit variables. For each Small vectors $\vec{I}_{13}$ and $\vec{I}_{14}$ eight switching states are available. However, only

two of them which are [16 14] and [14 16] for $\vec{I}_{13}$ and [14 12] and [12 14] for $\vec{I}_{14}$ are taken into consideration according to the discussions on the DC current balance control.

Small vector $\vec{I}_{13}$ is common in region 3 and region 2 of sector 1. By ending the region 3 switching and starting the switching of region 2 with vector $\vec{I}_{13}$ there will be no vector change in transient. However, there might be at most one device switching at each parallel converter. As mentioned before, Locating Medium vector $\vec{I}_{7}$ as the middle switching vector in regions 3, 2 and 4 of sector 1 symmetry is brought to the switching vectors. Subsequently, Small vector $\vec{I}_{14}$ is considered as the third vector in region 2. Selecting the same vector as the first vector of region 4, transient from region 2 to region 4 involves an identical vector. Table 2-10 provides the switching sequence of region 2 of sector 1. It is obvious that transient from one vector to next vector involves at most one switching at each converter.

Table 2-9 Vector order- sector 1, region 2.

| **Sector 1** | | **Region 2** | |
|---|---|---|---|
| **Switching Vector** | $\vec{I}_{13}$ | $\vec{I}_{7}$ | $\vec{I}_{14}$ |
| **Switching State** | [14 16] | [16 12] | [14 12] |
| | [16 14] | [12 16] | [12 14] |

As time runs, the reference current vector rotates and moves to region 4 of sector 1. Fig. 2-7 illustrates the location of the reference current vector.

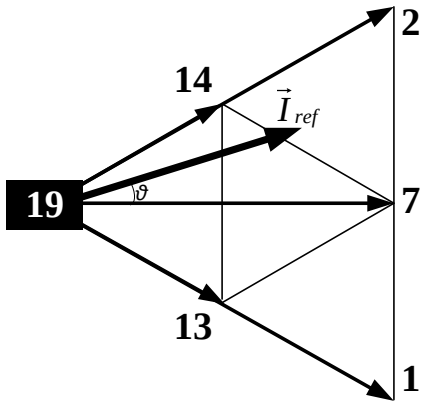



Fig. 2-7 Space vector plane- sector 1, region 4

As discussed heretofore, the vector set of ($\vec{I}_{14}$, $\vec{I}_{7}$, $\vec{I}_{2}$) is chosen to estimate the reference current vector. For Medium vector $\vec{I}_{7}$ two switching states which are [12 16] and [16 12] are available. For Small vector $\vec{I}_{14}$ eight switching states are available. However, only two of them which are [16 14] and [14 16] are taken into consideration according to the discussions on Chapter 3. For Large vector $\vec{I}_{2}$ only the switching state [12 12] is available.

Small vector $\vec{I}_{14}$ is common in region 2 and region 4 of sector 1. By ending the region 2 switching and starting the switching of region 4 with vector $\vec{I}_{14}$ there will be no vector change in transient period. However, there might be a change in switches. As mentioned before, assigning Medium vector $\vec{I}_{7}$ as the middle switching vector in regions 3, 2 and 4 of sector 1, symmetry is brought to the switching vectors. Subsequently, Large vector $\vec{I}_{2}$ is considered as the third vector in region 4. Selecting the same vector as the first vector of region 3 of sector 2, transient from sector 1 to sector 2 involves an identical vector and switching. Table 2-11 provides the switching sequence of region 4 of sector 1. It is obvious that transient from one vector to next vector involves at most one switching at each converter.

Table 2-10 Vector order- sector 1, region 4.

| **Sector 1** | | **Region 2** | |
|---|---|---|---|
| **Switching Vector** | $\vec{I}_{14}$ | $\vec{I}_{7}$ | $\vec{I}_{2}$ |
| **Switching State** | [14 12] | [16 12] | [12 12] |
| | [12 14] | [12 16] | |

Now, assume that the modulation index $m_a$ has lower values such that the reference current vector is located in region 1 of sector 1. The vector sets of ($\vec{I}_{19}, \vec{I}_{13}, \vec{I}_{7}$) and ($\vec{I}_{7}, \vec{I}_{14}, \vec{I}_{19}$) are selected corresponding to Down and Up triangles respectively. Each set includes one Medium, one Small and Zero vector. The switching states corresponding to Medium and Small vectors are discussed before. Zero vector is employed as the transient vector between different sectors. The proper switching state for Zero vector is the one which minimizes the switching frequency. Medium vector is employed as the transient vector between Down and Up areas. Table 2-12 and Table 2-13 provide the space vector order for Down and Up triangles respectively. The same analysis is done for other five Sectors by mirroring them on Sector 1.

Table 2-11 Vector order- sector 1, region 1, Down triangle.

| **Sector 1** | | **Region 2** | |
|---|---|---|---|
| **Switching Vector** | $\vec{I}_{19}$ | $\vec{I}_{13}$ | $\vec{I}_{7}$ |
| **Switching State** | [14 14] | [16 14] | [16 12] |
| | | [14 16] | [12 16] |

Table 2-12 Vector order- sector 1, region 1, Up triangle.

| **Sector 1** | | **Region 2** | |
|---|---|---|---|
| **Switching Vector** | $\vec{I}_{7}$ | $\vec{I}_{14}$ | $\vec{I}_{19}$ |
| **Switching State** | [16 12] | [14 12] | [54 12] |
| | [12 16] | [12 14] | [12 54] |

## 2.7 Dwell times

Considering the triangle which the reference vector is located in, three nearest vectors are chosen to form the reference current vector. The sampling period $T_s$ is divided to three parts which are called dwell times, each part for one of the space vectors. In other words, the multi-level converter operates at a switching state corresponding to the selected space vector for the period of dwell time of that vector.

The dwell time of each vector is calculated to satisfy two constraints:

1) $$\vec{I}_a T_a + \vec{I}_b T_b + \vec{I}_c T_c = \vec{I}_{ref} \quad (2.22)$$

2) $$T_a + T_b + T_c = T_s \quad (2.23)$$

in which $\vec{I}_a$, $\vec{I}_b$ and $\vec{I}_c$ are the chosen adjacent vectors, $T_a$, $T_b$ and $T_c$ are the dwell times for each vector and $T_s$ is the sampling time. The first constraint is the estimation constraint that guarantees that the selected vectors synthesize the reference current vector. The second constraint assures that the sum of three dwell times is equal to the sampling period.

In continue, dwell times corresponding to switching vectors are calculated at each region.

a) Region 1

Region 1 is divided into Down and Up triangles. In respect to space vectors corresponding to Down triangle, for example the set of ($\vec{I}_{19}, \vec{I}_{13}, \vec{I}_7$) for sector 1:

$$\vec{I}_a = 0,\ \vec{I}_b = \frac{\sqrt{3}}{3} I_d e^{-j30},\ \vec{I}_c = I_d e^{j0} \quad (2.24)$$

Replacing the vectors in the first constraint presented in equation (2.22),

$$T_b \frac{\sqrt{3}}{3} I_d e^{-j30} + T_c I_d e^{j0} = T_s m_a I_d e^{j\theta} \tag{2.25}$$

Solving the equation (2.25) for $T_b$ and $T_c$ in terms of system parameters,

$$T_b = -2T_s m_a \sin\theta \tag{2.26}$$

$$T_c = T_s m_a (\frac{\sqrt{3}}{3}\sin\theta + \cos\theta) \tag{2.27}$$

Substituting the parameters to the second constraint presented in equation (2.23),

$$T_a = T_s(1 - m_a(\cos\theta + (\frac{\sqrt{3}}{3} - 2)\sin\theta)) \tag{2.28}$$

In respect to Up triangle of region 1, for example the set of ($\vec{I}_7, \vec{I}_{14}, \vec{I}_{19}$) for sector 1:

$$\vec{I}_a = I_d e^{j0},\ \vec{I}_b = \frac{\sqrt{3}}{3} I_d e^{j30},\ \vec{I}_c = 0 \tag{2.29}$$

Replacing the parameters in the first constraint presented in equation (2.22),

$$T_a I_d e^{j0} + T_b \frac{\sqrt{3}}{3} I_d e^{j30} = T_s m_a I_d e^{j\theta} \tag{2.30}$$

Solving the equation for $T_a$ and $T_b$ in terms of system parameters,

$$T_a = T_s m_a (\cos\theta - \frac{\sqrt{3}}{3}\sin\theta) \tag{2.31}$$

$$T_b = 2T_s m_a \sin\theta \tag{2.32}$$

Substituting the parameters in the second constraint equation (2.23),

$$T_c = T_s(1 + m_a(\cos\theta + (2 - \frac{\sqrt{3}}{3})\sin\theta)) \tag{2.33}$$

b) Region 2

Presenting three selected space vectors in region 2,

$$\vec{I}_a = \frac{\sqrt{3}}{3} I_d e^{j-30},\ \vec{I}_b = I_d e^{j0},\ \vec{I}_c = \frac{\sqrt{3}}{3} I_d e^{j30} \tag{2.34}$$

Replacing the vectors in the equation (2.22),

$$T_a \frac{\sqrt{3}}{3} I_d e^{-j30} + T_b I_d e^{j0} + T_c \frac{\sqrt{3}}{3} I_d e^{j30} = T_s m_a I_d e^{j\theta} \tag{2.35}$$

Solving the equation (2.35) and the equation (2.23) for $T_a$, $T_b$ and $T_c$ in terms of system parameters,

$$T_a = \frac{4}{3} T_s (1 - m_a (\cos\theta + \frac{\sqrt{3}}{2} \sin\theta)) \tag{2.36}$$

$$T_b = T_s (-1 + m_a (2\cos\theta)) \tag{2.37}$$

$$T_c = \frac{2}{3} T_s (1 - m_a (\cos\theta - \sqrt{3}\sin\theta)) \tag{2.38}$$

c) Region 3

Three selected vectors corresponding to region 3 are presented in below.

$$\vec{I}_a = \frac{2}{\sqrt{3}} I_d e^{j-30},\ \vec{I}_b = I_d e^{j0},\ \vec{I}_c = \frac{\sqrt{3}}{3} I_d e^{-j30} \tag{2.39}$$

Replacing the vectors in the first constraint presented in equation (2.22),

$$T_a \frac{2}{\sqrt{3}} I_d e^{j-30} + T_b I_d e^{j0} + T_c \frac{\sqrt{3}}{3} I_d e^{-j30} = T_s m_a I_d e^{j\theta} \tag{2.40}$$

Solving the equation (2.40) and the equation (2.23) for $T_a$, $T_b$ and $T_c$ in terms of system parameters,

$$T_a = T_s (-1 + m_a (\cos\theta - \sqrt{3}\sin\theta)) \tag{2.41}$$

$$T_b = T_s m_a(\cos\theta + \sqrt{3}\sin\theta) \tag{2.42}$$

$$T_c = T_s(2 + m_a(-2\cos\theta)) \tag{2.43}$$

d) Region 4

In respect to region 4,

$$\vec{I}_a = \frac{\sqrt{3}}{3} I_d e^{j30},\ \vec{I}_b = I_d e^{j0},\ \vec{I}_c = \frac{2}{\sqrt{3}} I_d e^{j30} \tag{2.44}$$

Replacing the vectors in the first constraint presented in equation (2.22),

$$T_a \frac{\sqrt{3}}{3} I_d e^{j30} + T_b I_d e^{j0} + T_c \frac{2}{\sqrt{3}} I_d e^{j30} = T_s m_a I_d e^{j\theta} \tag{2.45}$$

Solving the equation and the second constraint for $T_a$, $T_b$ and $T_c$ in terms of system parameters,

$$T_a = T_s(2 + m_a(-2\cos\theta)) \tag{2.46}$$

$$T_b = T_s m_a(\cos\theta - \sqrt{3}\sin\theta) \tag{2.47}$$

$$T_c = T_s(-1 + m_a(\cos\theta + \sqrt{3}\sin\theta)) \tag{2.48}$$

Table 2-8 presents the calculated dwell times for each space vector.

Table 2-13 Dwell times of space vectors.

| **Region** | **$T_a$** | **$T_b$** | **$T_c$** |
|---|---|---|---|
| **1 Down** | $T_a = T_s(1 - m_a(\cos\theta + (\frac{\sqrt{3}}{3} - 2)\sin\theta))$ | $T_b = -2T_s m_a \sin\theta$ | $T_c = T_s m_a(\frac{\sqrt{3}}{3}\sin\theta + \cos\theta)$ |
| **1 Up** | $T_a = T_s m_a(\cos\theta - \frac{\sqrt{3}}{3}\sin\theta)$ | $T_b = 2T_s m_a \sin\theta$ | $T_c = T_s(1 + m_a(\cos\theta + (2 - \frac{\sqrt{3}}{3})\sin\theta))$ |
| **2** | $\frac{4}{3}T_s(1 - m_a(\cos\theta + \frac{\sqrt{3}}{2}\sin\theta))$ | $T_s(-1 + m_a(2\cos\theta))$ | $\frac{2}{3}T_s(1 - m_a(\cos\theta - \sqrt{3}\sin\theta))$ |
| **3** | $T_s(-1 + m_a(\cos\theta - \sqrt{3}\sin\theta))$ | $m_a T_s(\cos\theta + \sqrt{3}\sin\theta)$ | $T_s(2 + m_a(-2\cos\theta)$ |
| **4** | $T_s(2 + m_a(-2\cos\theta))$ | $m_a T_s(\cos\theta - \sqrt{3}\sin\theta)$ | $T_s(-1 + m_a(\cos\theta + \sqrt{3}\sin\theta))$ |

## 2.8 Procedure summary

The SVM method procedure is summarized in 4 major steps as following.

Step 1: The location of the AC current reference vector is determined. The geometrical calculations are carried out to determine the sector number and the region type of which the reference vector is located in.

Step 2: Three adjacent space vectors are chosen with respect to the location of the reference vector and based on Table 2-7. The detailed discussion was presented in Section 2.5.

Step 3: Dwell times are calculated for the selected space vectors based on Table 2-13. The order of the selected vector is designed in Section 2.6. to minimize the switching frequency.

Step 4: At the final step, the switching sequence is applied to the converters.

The theory discussion presented in Chapter 2 covers the first three steps. Since the switching sequence is designed based on DC current balance control, the theory will be continued in the next chapter. The designed switching sequence is presented at the end of Chapter 3.

## 2.9 Conclusion

The space vector modulation for 5-level current source converter is developed in this chapter. The scheme contains 81 switching states and 19 resulting space vectors. Space vectors divide the space vector plane into 6 sectors and each sector is divided into 5 smaller triangular areas. In other words, the space vector diagram is divided into 30 areas. The space vector division is illustrated in space vector diagram. Three vectors are selected at each area to synthesize the reference current vector that represents the AC current. Choosing adjacent vectors at each small area brings a better estimation of the reference current vector. Therefore, improved harmonic

performance is expected which will be studied in Chapter 4. The space vector order is designed to achieve the minimized switching frequency. Dwell time for each vector is calculated to satisfy two estimation constraints. Heretofore, the major steps of space vector modulation are developed. At each moment of switching, to be employed vectors and the dwell time corresponding to each are determined based on the location of the reference current vector. In Chapter 3 the procedure of determining the proper switching state for each vector is introduced. Subsequently, the switching sequence is designed and presented at the end of the next chapter.

# Chapter 3
# DC Current Balance Control

## 3.1 Introduction

One of the practical challenging issues of parallel multi-level current source converters (CSC) is unbalanced DC currents. In this chapter, the reasons, causes and elimination of unbalanced DC currents are discussed. Manufacturing tolerance in circuit and the parameters of switching devices is the main cause of unbalanced DC currents. Unbalanced DC currents lead to the generation of current harmonics, uneven power division between the parallel converters and increase in the total loss of the system. Generally, the elimination of an unbalanced DC current is necessary in multi-level parallel converters. A DC current balance control employing redundant switching states of Medium and Small vectors is proposed in this chapter. The effect of the space vectors on DC link currents is investigated and the switching sequence is designed for distinctive circuit circumstances.

## 3.2 Unbalanced DC currents

Generally, a circuit condition with unequal currents of the DC links is operating with unbalanced DC current conditions. One can divide the unbalanced DC current aspect into two distinctive areas. Suppose that the positive and negative DC link currents are equal at each converter but not equal in parallel converters. Under this circumstance, there is no unbalanced DC

current at each converter and unbalanced DC currents appear at two converters. On the other hand, suppose that even DC link currents are not equal at each converter. Under this circumstance circulating current is inevitable.

Operation of multi-level converter at every conditions of unbalanced DC currents, unwanted degrade of converter's performance appears. Generally, unbalanced DC currents lead to generating current harmonics and higher current distortion, uneven power division between converters and increase in the total loss of the system. Altogether, the overall system performance decline and waste of investment and technology are the results of unbalanced DC link currents.

The main reasons cause unbalanced DC link currents are:

1) Different circuit parameters, especially manufacturing tolerance in DC chokes

2) Different pulse width modulation techniques or asynchronous switching strategies

3) Variations in the time delay of the gating signals of two parallel converters, which affect both transient and steady-state current balance

4) Unequal ON-state voltages of the semiconductor devices, which affect steady state DC currents balance

The circulating current is mainly consists of zero-sequence components. The total impedance within the zero-sequence circuit of parallel converter systems with common DC is very small, and large zero-sequence currents will be circulating in the zero-sequence circuit.

The traditional methods for avoiding circulating current is to use independent and separate AC or DC power supplies or a transformer in the AC side of the parallel converters. Applying either solution, being higher in size, mass and investment costs are certain. Another traditional solution is adding a phase reactor to configuration. Since, the reactors have lower impedance in lower

frequency low-frequency circulating current would not be attenuated. Besides, some dq axis nonlinear control strategies are introduced to limit the zero sequence circulating current [9, 10].

Elimination of unbalanced DC currents and subsequently circulating current is one of the most important aspects of multi-level CSC design. One of the features of the introduced switching modulation is DC link current balance control. The controller results in unbalanced DC current minimization.

## 3.3 Effect of space vectors on DC currents

First of all, it is necessary to analyze the effect of the space vectors on the DC link currents.

a) Large vectors

There is only one switching state available for each Large vector. The switching state employs same switches at both converters. The effect of the Large vector on the DC link currents is identical in both converters. Consequently, Large vectors cannot be employed to balance the DC currents.

b) Medium vectors

As mentioned, two switching states are available for each Medium vector. For detailed analysis the switching states corresponding to Medium vector $\vec{I}_7$ are investigated. Two redundant switching states [12 16] and [16 12] are available. Suppose that the converter is operating at the switching state [12 16]. Fig. 3-1 illustrates the current paths when the mentioned switching state is applied in the multi-level parallel current source inverter (CSI).

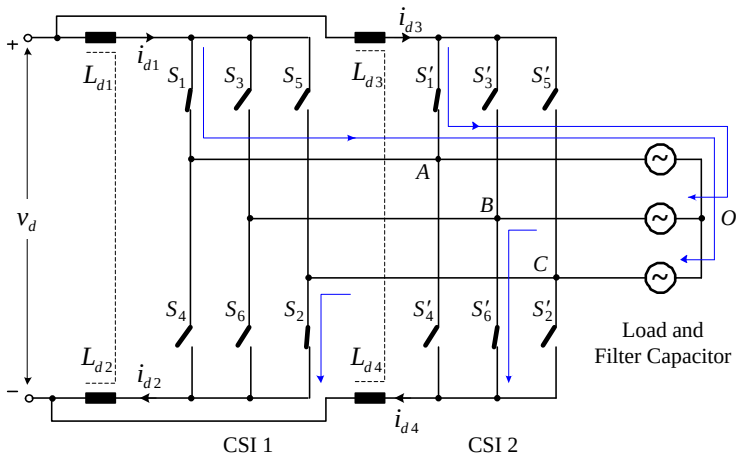



Fig. 3-1 Current paths in parallel inverters with switching state [12 16]

The parameter which controls the change in DC link currents is the voltage across the DC link choke. For the positive DC link, switch number 1 is at ON state in both inverters. Phase A is connected to both positive DC links. Therefore,

$$v_{L_{d1}} = v_d^{+} - v_A \tag{3.1}$$

$$v_{L_{d3}} = v_d^{+} - v_A \tag{3.2}$$

from which,

$$v_{L_{d1}} = v_{L_{d3}} \tag{3.3}$$

So, there is an equal voltage across the positive DC link inductances. In other words, switching state [12 16] has no effect on the positive DC link currents $i_{d1}$ and $i_{d3}$. On the other hand, negative DC buses are connected to different phases. So, the different voltages are expected across the negative DC link chokes.

$$v_{L_{d2}} = v_C - v_d^{-} \tag{3.4}$$

$$v_{L_{d4}} = v_B - v_d^{-} \tag{3.5}$$

from which,

$$v_{L_{d2}} \neq v_{L_{d4}} \tag{3.6}$$

When $v_C > v_B$ then $v_{L_{d2}} > v_{L_{d4}}$, consequently, increase in $i_{d2}$ and decrease in $i_{d4}$ is expected. On the contrary, when $v_C < v_B$ then $v_{L_{d2}} < v_{L_{d4}}$, consequently, increase in $i_{d4}$ and decrease in $i_{d2}$ is expected.

Now, suppose that the converter is operating at switching state [16 12]. Fig. 3-2 illustrates the current paths when the mentioned switching state is applied in a multi-level parallel CSI.

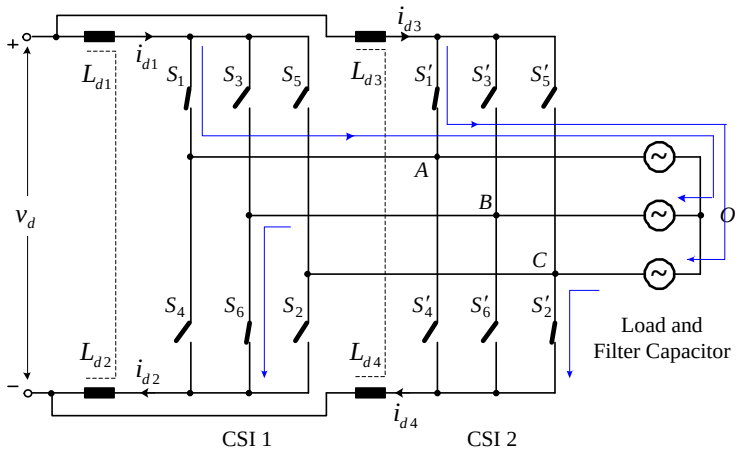



Fig. 3-2 Current paths in parallel inverters with switching state [16 12]

The parameter which controls the change in DC link currents is the voltage across the DC link choke. For the positive DC link, switch number 1 is at ON state in both inverters. Subsequently, phase A is connected to both positive DC links. Therefore,

$$v_{L_{d1}} = v_d^{+} - v_A \tag{3.7}$$

$$v_{L_{d3}} = v_d^{+} - v_A \tag{3.8}$$

from which,

$$v_{L_{d1}} = v_{L_{d3}} \tag{3.9}$$

So, there is an equal voltage across the positive DC link inductances. In other words, switching state [16 12] has no effect on the positive DC link currents $i_{d1}$ and $i_{d3}$. On the other hand, negative DC buses are connected to different phases. So, the different voltages are expected across the negative DC link chokes.

$$v_{L_{d2}} = v_B - v_{d^-} \tag{3.10}$$

$$v_{L_{d4}} = v_C - v_{d^-} \tag{3.11}$$

from which,

$$v_{L_{d2}} \neq v_{L_{d4}} \tag{3.12}$$

When $v_B > v_C$ then $v_{L_{d2}} > v_{L_{d4}}$, consequently, increase in $i_{d2}$ and decrease in $i_{d4}$ is expected. On the contrary, when $v_B < v_C$ then $v_{L_{d2}} < v_{L_{d4}}$, consequently, increase in $i_{d4}$ and decrease in $i_{d2}$ is expected.

Table 3-1 shows the effect of the switching states of Medium vector $\vec{I}_7$ on DC currents. When the switching state has no effect on the DC current it is mentioned with x, while $\downarrow$ means that employing the switching state at mentioned circuit circumstances cause the DC current to decrease and on the contrary, $\uparrow$ means that applying the switching state increases the DC current under the circuit circumstances.

Table 3-1 Effect of switching states of Medium vector $\vec{I}_7$ on DC currents.

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [12 16] or [16 12] | $v_{BO}=v_{CO}$ | x | X | x | x |
| [12 16] | $v_{BO}>v_{CO}$ | x | $\downarrow$ | x | $\uparrow$ |
| | $v_{BO}<v_{CO}$ | x | $\uparrow$ | x | $\downarrow$ |
| [16 12] | $v_{BO}>v_{CO}$ | x | $\uparrow$ | x | $\downarrow$ |
| | $v_{BO}<v_{CO}$ | x | $\downarrow$ | x | $\uparrow$ |

As shown above, Medium vector $\vec{I}_7$ has no effect on $i_{d1}$ and $i_{d3}$. Besides, two redundant switching states [12 16] and [16 12] provide an inverse effect on the negative DC link currents. In conclusion, the negative DC link currents are controllable through choosing either switch number 2 or switch number 6 at ON state in the first inverter. Whichever is chosen the other one should be at ON state in the second inverter.

The same study carried out for other five Medium vectors located in other five sectors is presented in Appendix I.

c) Small vectors

Suppose that the multi-level converter is operating at the state of Small vector $\vec{I}_{13}$ which is located at the boundary of sectors number 1 and 6. Table 3-3 provides the eight redundant switching states corresponding to the mentioned vector.

Table 3-2 Redundant switching states of Small vector $\vec{I}_{13}$.

| **Vector** | **Redundant Switching States** | | | |
|---|---|---|---|---|
| $\vec{I}_{13}$ | [16 14] | [16 36] | [16 52] | [12 56] |
| | [14 16] | [36 16] | [52 16] | [56 12] |

Among available switching states, two of them which are [16 14] and [14 16] employ the same switch at ON state at the top half of both converters. In addition, two of them which are [16 36] and [36 16] employ the same switch at ON state at the bottom half of both converters. First two may be employed to balance negative DC bus currents and second two can be employed in positive DC bus currents balance control. Since, the negative DC bus currents are controlled at odd sectors with Medium vectors, switching states [16 14] and [14 16] corresponding to Small vector are employed when the reference current vector is located at sector number 1 to accompany Medium vector $\vec{I}_7$. On the other hand, switching states [16 36] and [36 16] are employed when

the reference current is located at sector number 6 to accompany Medium vector $\vec{I}_{12}$ in positive DC current balance control. Table 3-4 presents the employed switching states corresponding to Small vector $\vec{I}_{13}$.

Table 3-3 Employed switching states of Small vector $\vec{I}_{13}$.

| Vector | Sector | Switching States | |
|---|---|---|---|
| $\vec{I}_{13}$ | 1 | [14 16] | [16 14] |
| | 6 | [16 36] | [36 16] |

Table 3-5 shows the effect of switching states [14 16] and [16 14] on the DC currents. When the switching state has no effect on the DC current it is mentioned with X, while ↓ means that employing the switching state at mentioned circuit circumstances cause the DC current to decrease and on the contrary, ↑ means that applying the switching state increases the DC current under the circuit circumstances.

Table 3-4 Effect of switching states of Small vector $\vec{I}_{13}$ on DC currents (region 1).

| Switching State | Load Voltage | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [14 16] or [16 14] | $v_{AO}=v_{BO}$ | x | X | x | x |
| [14 16] | $v_{AO}>v_{BO}$ | x | ↓ | x | ↑ |
| | $v_{AO}<v_{BO}$ | x | ↑ | x | ↓ |
| [16 14] | $v_{AO}>v_{BO}$ | x | ↑ | x | ↓ |
| | $v_{AO}<v_{BO}$ | x | ↓ | x | ↑ |

As shown above, Small vector $\vec{I}_{13}$ has no effect on $i_{d1}$ and $i_{d3}$. On the other hand, two redundant switching states [14 16] and [16 14] provide an inverse effect on the negative DC link currents. In conclusion, the negative DC link currents are controllable through choosing either switch number

4 or switch number 6 at ON state in the first inverter. Whichever is chosen the other one should be at ON state in the second inverter.

Table 3-7 shows the effect of switching states [16 36] and [36 16] on the DC currents. As shown below, Small vector $\vec{I}_{13}$ has no effect on $i_{d2}$ and $i_{d4}$, while two redundant switching states [16 36] and [36 16] provide an inverse effect on the negative DC link currents. In conclusion, the negative DC link currents are controllable through choosing either switch number 1 or switch number 3 at ON state in the first inverter. Whichever is chosen the other one should be at ON state in the second inverter. The proper switching state is chosen according to the measured parameters and the designed switching sequence.

Table 3-5 Effect of switching states of Small vector $\vec{I}_{13}$ on DC currents (region 6).

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [16 36] or [36 16] | $v_{AO}=v_{BO}$ | x | X | x | x |
| [16 36] | $v_{AO}>v_{BO}$ | ↓ | X | ↑ | x |
| | $v_{AO}<v_{BO}$ | ↑ | X | ↓ | x |
| [36 16] | $v_{AO}>v_{BO}$ | ↑ | X | ↓ | x |
| | $v_{AO}<v_{BO}$ | ↓ | X | ↑ | x |

The same analysis can be done for other five Small vectors. The resulted tables are presented in Appendix II.

d) Zero vector

Zero switching state bypasses the DC currents. Therefore, higher distortion in AC currents is inevitable. It is preferable to do not employ Zero vector in modulation. Consequently, Zero vector is not employed in DC current balance control. In fact, Zero switching state is used only at lower values of $m_a$ and the proper switching state is chosen to produce lower switching frequency.

## 3.4 DC current balance control method

DC current balance control can be summarized as following:

- Medium and Small vectors are responsible to balance the DC currents.
- Positive DC link currents are controlled in even sectors while the negative DC link currents are controlled in odd evens.
- DC currents and AC voltages are measured and compared to determine the circuit circumstances.
- The proper switching states of Medium and Small vectors are chosen based on circuit circumstances.

As elaborated above, Medium and Small vectors are employed to balance the DC currents. At every switching moment of Medium and Small vectors, the corresponding DC currents and voltages are measured. The comparison of parameters determined the proper switching state. The switching sequence look-up tables are designed to provide the proper switching state at distinctive circuit circumstances.

Suppose that the modulation is operating at Medium vector $\vec{I}_7$. The effect of the vector on the DC currents was elaborated in previous part and is summarized in Table 3-1. The proper switching state is chosen according to the measured parameters and the designed switching sequence. Table 3-6 provides the proper switching state of Medium vector $\vec{I}_7$ at different circuit circumstances.

Table 3-6 Selected switching states of $\vec{I}_7$ at distinctive circuit circumstances.

| Voltage Comparison | Current Comparison | Selected Switching State |
|---|---|---|
| $v_{CO}>v_{BO}$ | $i_{d4}>i_{d2}$ | **[12 16]** |
| $v_{BO}>v_{CO}$ | $i_{d2}>i_{d4}$ | |
| $v_{CO}>v_{BO}$ | $i_{d2}>i_{d4}$ | **[16 12]** |
| $v_{BO}>v_{CO}$ | $i_{d4}>i_{d2}$ | |

Suppose that the modulation is operating at Small vector $\vec{I}_{13}$. This vector is common in sectors 1 and 6. Different switching states of $\vec{I}_{13}$ are employed at each sector. The effects of these switching states are presented in Table 3-4 and Table 3-5. The proper switching state in sector 1 is chosen based on Table 3-7 while Table 3-8 determines the proper switching state of $\vec{I}_{13}$ in sector 6. The same study is carried out for other Medium and Small vectors presented in Appendices I and II.

Table 3-7 Selected switching state of $\vec{I}_{13}$ at distinctive circuit circumstances (region 1).

| Voltage Comparison | Current Comparison | Selected Switching State |
|---|---|---|
| $v_{BO}>v_{AO}$ | $i_{d4}>i_{d2}$ | **[14 16]** |
| $v_{AO}>v_{BO}$ | $i_{d2}>i_{d4}$ | |
| $v_{BO}>v_{AO}$ | $i_{d2}>i_{d4}$ | **[16 14]** |
| $v_{AO}>v_{BO}$ | $i_{d4}>i_{d2}$ | |

Table 3-8 Selected switching state of $\vec{I}_{13}$ at distinctive circuit circumstances (region 6).

| Voltage Comparison | Current Comparison | Selected Switching State |
|---|---|---|
| $v_{AO}>v_{BO}$ | $i_{d1}>i_{d3}$ | **[16 36]** |
| $v_{BO}>v_{AO}$ | $i_{d3}>i_{d1}$ | |
| $v_{AO}>v_{BO}$ | $i_{d3}>i_{d1}$ | **[36 16]** |
| $v_{BO}>v_{AO}$ | $i_{d1}>i_{d3}$ | |

## 3.5 Switching sequence design

According to the DC current balance control, the proper switching state is chosen at each state. For instance, suppose that the reference AC current is located in region 3 of sector 1. Negative DC link currents are controlled in Sector 1. Therefore, $i_{d2}$ and $i_{d4}$ should be measured and compared together. In addition, the comparison between $v_{BO}$ and $v_{AO}$ is needed to determine the proper switching state of Small vector $\vec{I}_{13}$. The comparison between $v_{CO}$ and $v_{BO}$ is needed to determine the proper switching state of Medium vector $\vec{I}_{7}$. Table 3-9 represents the designed switching sequence for region 3 in detail.

Table 3-9 Switching sequence look-up table- sector 1, region 3.

| $i_{d2}>i_{d4}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_{1}$ | $\vec{I}_{7}$ | $\vec{I}_{13}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [16 16] | [16 12] | [14 16] |
| 0 | 0 | 1 | [16 16] | [16 12] | [16 14] |
| 0 | 1 | 0 | [16 16] | [12 16] | [14 16] |
| 0 | 1 | 1 | [16 16] | [12 16] | [16 14] |
| 1 | 0 | 0 | [16 16] | [12 16] | [16 14] |
| 1 | 0 | 1 | [16 16] | [12 16] | [14 16] |
| 1 | 1 | 0 | [16 16] | [16 12] | [16 14] |
| 1 | 1 | 1 | [16 16] | [16 12] | [14 16] |

Now, assume that the reference AC current is located in region 2 of sector 1. $i_{d2}$ and $i_{d4}$ should be measured and compared together. In addition, the comparison between $v_{BO}$ and $v_{AO}$ is needed to determine the proper switching state of Small vector $\vec{I}_{13}$. The comparison between $v_{CO}$ and $v_{BO}$ is needed to determine the proper switching state of Medium vector $\vec{I}_{7}$. The comparison between $v_{AO}$ and $v_{CO}$ is needed to determine the proper switching state of Small vector $\vec{I}_{14}$. Table 3-10 represents the designed switching sequence for region 2 in detail.

Now, assume that the reference AC current is located in region 4 of sector 1. $i_{d2}$ and $i_{d4}$ should be measured and compared together. In addition, the comparison between $v_{BO}$ and $v_{AO}$ is needed to determine the proper switching state of Small vector $\vec{I}_{13}$. The comparison between $v_{CO}$ and $v_{BO}$ is needed to determine the proper switching state of Medium vector $\vec{I}_{7}$. Table 3-11 represents the designed switching sequence for region 4 in detail.

Table 3-10 Switching sequence look-up table- sector 1, region 2.

| $i_{d2}>i_{d4}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{13}$ | $\vec{I}_{7}$ | $\vec{I}_{14}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | [14 16] | [16 12] | [12 14] |
| 0 | 0 | 0 | 1 | [14 16] | [16 12] | [14 12] |
| 0 | 0 | 1 | 0 | [16 14] | [16 12] | [12 14] |
| 0 | 0 | 1 | 1 | [16 14] | [16 12] | [14 12] |
| 0 | 1 | 0 | 0 | [14 16] | [12 16] | [12 14] |
| 0 | 1 | 0 | 1 | [14 16] | [12 16] | [14 12] |
| 0 | 1 | 1 | 0 | [16 14] | [12 16] | [12 14] |
| 0 | 1 | 1 | 1 | [16 14] | [12 16] | [14 12] |
| 1 | 0 | 0 | 0 | [16 14] | [12 16] | [14 12] |
| 1 | 0 | 0 | 1 | [16 14] | [12 16] | [12 14] |
| 1 | 0 | 1 | 0 | [14 16] | [12 16] | [14 12] |
| 1 | 0 | 1 | 1 | [14 16] | [12 16] | [12 14] |
| 1 | 1 | 0 | 0 | [16 14] | [16 12] | [14 12] |
| 1 | 1 | 0 | 1 | [16 14] | [16 12] | [12 14] |
| 1 | 1 | 1 | 0 | [14 16] | [16 12] | [14 12] |
| 1 | 1 | 1 | 1 | [14 16] | [16 12] | [12 14] |

Table 3-11 Switching sequence look-up table- sector 1, region 4.

| $i_{d2}>i_{d4}$ | $v_{CO}>v_{BO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{14}$ | $\vec{I}_{7}$ | $\vec{I}_{2}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [12 14] | [16 12] | [12 12] |
| 0 | 0 | 1 | [14 12] | [16 12] | [12 12] |
| 0 | 1 | 0 | [12 14] | [12 16] | [12 12] |
| 0 | 1 | 1 | [14 12] | [12 16] | [12 12] |
| 1 | 0 | 0 | [14 12] | [12 16] | [12 12] |
| 1 | 0 | 1 | [12 14] | [12 16] | [12 12] |
| 1 | 1 | 0 | [14 12] | [16 12] | [12 12] |
| 1 | 1 | 1 | [12 14] | [16 12] | [12 12] |

Now, assume that the reference AC current is located in region 1 of sector 1. $i_{d2}$ and $i_{d4}$ should be measured and compared together. In addition, the comparison between $v_{BO}$ and $v_{AO}$ is needed to determine the proper switching state of Small vector $\vec{I}_{13}$. The comparison between $v_{CO}$ and $v_{BO}$ is needed to determine the proper switching state of Medium vector $\vec{I}_{7}$. The comparison between $v_{AO}$ and $v_{CO}$ is needed to determine the proper switching state of Small vector $\vec{I}_{14}$.

Table 3-12 Switching sequence look-up table- sector 1, region 1, Down triangle.

| $i_{d2}>i_{d4}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_{19}$ | $\vec{I}_{13}$ | $\vec{I}_{7}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [14 14] | [14 16] | [16 12] |
| 0 | 0 | 1 | [14 14] | [16 14] | [16 12] |
| 0 | 1 | 0 | [14 14] | [14 16] | [12 16] |
| 0 | 1 | 1 | [14 14] | [16 14] | [12 16] |
| 1 | 0 | 0 | [14 14] | [16 14] | [12 16] |
| 1 | 0 | 1 | [14 14] | [14 16] | [12 16] |
| 1 | 1 | 0 | [14 14] | [16 14] | [16 12] |
| 1 | 1 | 1 | [14 14] | [14 16] | [16 12] |

Table 3-12 and Table 3-13 represent the designed switching sequence for Down triangle and Up triangle of region 1 respectively.

Table 3-13 Switching sequence look-up table- sector 1, region 1, Up triangle.

| $i_{d2}>i_{d4}$ | $v_{CO}>v_{BO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{7}$ | $\vec{I}_{14}$ | $\vec{I}_{19}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [16 12] | [12 14] | [12 54] |
| 0 | 0 | 1 | [16 12] | [14 12] | [54 12] |
| 0 | 1 | 0 | [12 16] | [12 14] | [12 54] |
| 0 | 1 | 1 | [12 16] | [14 12] | [54 12] |
| 1 | 0 | 0 | [12 16] | [14 12] | [54 12] |
| 1 | 0 | 1 | [12 16] | [12 14] | [12 54] |
| 1 | 1 | 0 | [16 12] | [14 12] | [54 12] |
| 1 | 1 | 1 | [16 12] | [12 14] | [12 54] |

The same analysis is done for other five sectors by mirroring them on Sector 1. The designed switching sequence for sectors 1 to 6 is presented in Appendix III.

## 3.6 DC current balance control performance

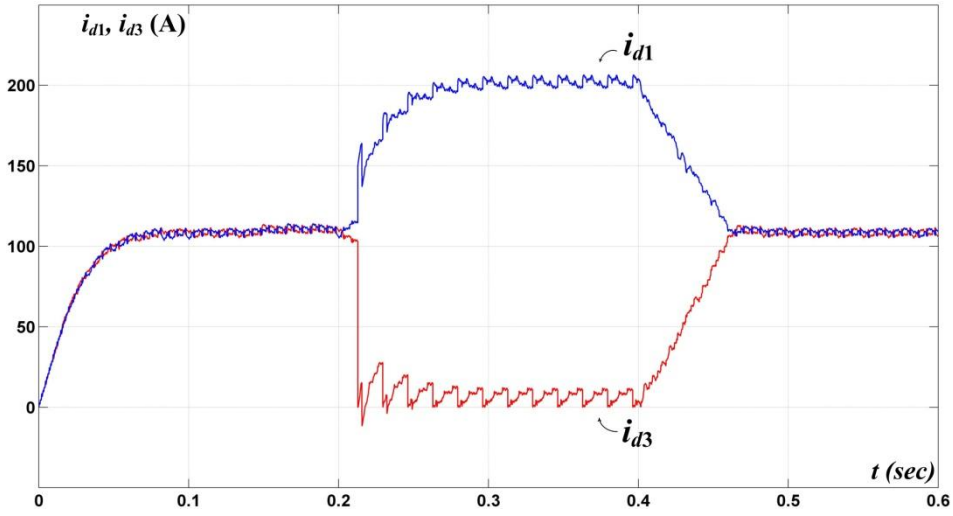
To study the DC current balance control the simulation is run with and without the DC current balance control. The waveforms are shown on the inverter side. However, the same results are appeared on the rectifier side. The simulated DC link currents are shown in Fig. 3-3. The DC current balance control is inactivated between *t= 0.2 sec* and *t= 0.4 sec*.

When the DC current balance control is activated, the DC link currents track the same value (i.e. *110 A*). On the other hand, once the DC current balance control is inactivated at *t= 0.2 sec*, the DC link currents either on positive bus or negative bus diverge to different values. As discussed before, unbalanced DC link currents cause higher loss, higher distortion content on the AC side and uneven power division between converters. At *t= 0.4 sec* when the DC current balance control is activated once more, DC link currents on both positive bus or negative bus converge to the same value. The same results are appeared at the rectifier side.

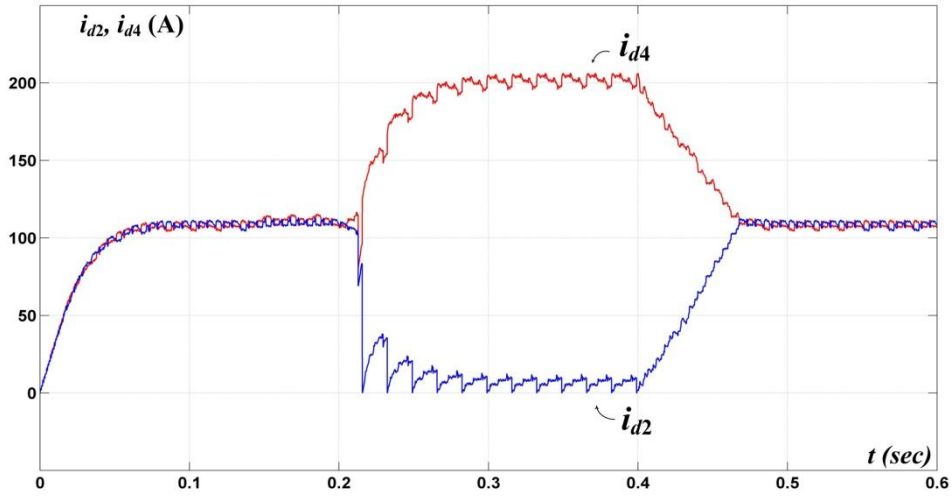
The time which is taken to balance the DC link currents depends on the DC chokes. The large value of DC chokes is chosen to eliminate ripples of DC currents and focus on performance study of the DC current balance control.

As a fact, the proposed DC current balance control method responses instantaneously. Another simulation scenario is used to prove the fast response of the controller. In this scenario the 5-level CSC is operating under symmetrical circumstances. At *t= 0.25 sec* a *0.2 pu* series resistance is added to positive DC link of the first converter. This resistance models any

asymmetrical circumstances that may result in unbalanced DC currents. The simulation results for positive DC link currents are shown in Fig. 3-4.




(a) Positive Bus




(b) Negative Bus

Fig. 3-3 DC link currents with and without current balance control ($L_d$=*1.5 pu*)

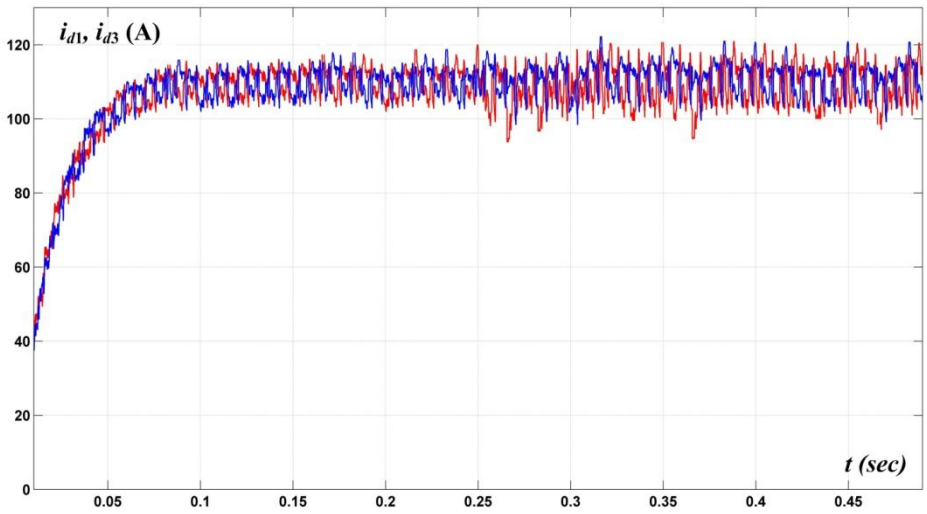



Fig. 3-4 Positive DC link currents under asymmetrical circuit parameters with current balance control ($L_d$=*0.75 pu*)

As shown above, the DC current balance control reacts instantaneously and DC link currents remained balanced. In addition, since the large value of resistance is chosen, the simulation results prove the effectiveness of the operation of the controller even under large asymmetrical circuit parameters. In fact, the converter will not face that huge disturbance in practice.

## 3.7 Conclusion

When two current source converters are connected in parallel, circulating current or unbalanced DC currents in general is unavoidable. Since unbalanced DC currents result in converter system performance decline, it is necessary to enhance the switching modulation with a DC current balance control. An effective and fast DC current balance control scheme has been proposed, which employs the redundant switching states of Medium and Small vectors to eliminate unbalanced DC currents. The proper switching state from available redundant

switching states is chosen based on circuit circumstances and the designed switching sequence presented in Appendix III. The simulation results verify the performance of the proposed DC current balance control. The designed DC current balance control reacts instantaneously to any disturbances and effectively eliminates unbalanced DC currents.

# Chapter 4
# Performance Study - Simulation

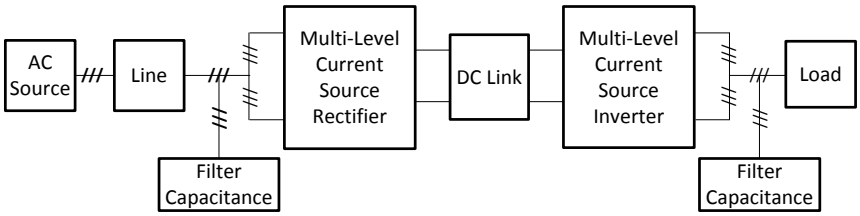
## 4.1 Introduction

To study the performance of the proposed multi-level converter and space vector modulation (SVM), the multi-level configuration and switching modulation are modeled in Simulink. The simulation is used to investigate the steady state and dynamic performance of the current source converter (CSC). As discussed in previous chapters, one of the main objectives of the design is to reduce distortion on AC currents and voltages. Harmonic content of steady state AC waveforms are investigated in detail on both power supply and load sides. The analysis shows that despite the large distortion on each single-bridge converter, the multi-level chopped currents contain much less harmonics. Therefore, it is possible to reduce the size of the filter capacitor. The dynamic performance of the converter is studied by elaboration and investigation of PI controller loops. PI controller loops adjust the modulation index on the rectifier side to control the DC link current and the modulation index value on the inverter side to control the load voltage.

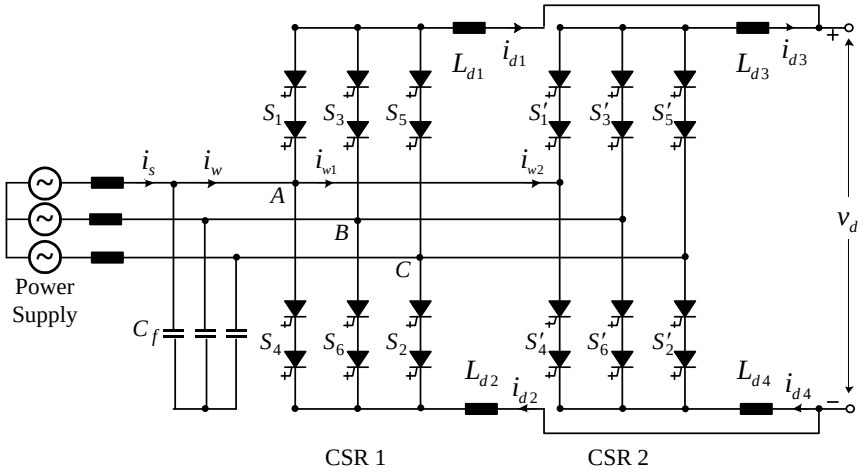
## 4.2 Modeling the Five-level CSC and SVM in Simulink

### 4.2.1 Five-level current source converter

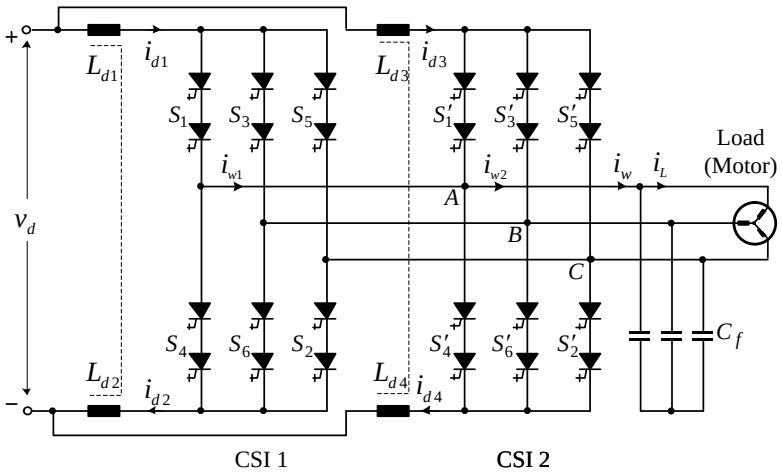
Fig. 4-1 shows the system configuration block diagram and the 5-level converters. The AC source is modeled with three-phase AC voltage working at *4.16 kV* line to line with a frequency of *60 Hz*, which is connected to the multi-level converter through a three-phase line modeled




(a) Converter system block diagram




(b) 5-level parallel current source rectifier




(c) 5-level current source inverter

Fig. 4-1 Converter system configuration

with series resistance and inductance. A three-phase filter capacitor is necessary at the input terminal of the parallel current source rectifiers (CSR). Two parallel single-bridge CSRs constitute the multi-level CSR.

The multi-level CSR is connected to the multi-level current source inverter (CSI) through the DC link chokes. Two parallel single-bridge inverters constitute the multi-level CSI. Three-phase filter capacitor is necessary at the end terminal of the CSI. The three-phase load is connected to the AC side of the multi-level inverter and is modeled with series resistance and inductance at each phase. The load is *1 MW* with *PF=0.9* at nominal operation.

### 4.2.2 Space vector modulation

The simulation model is introduced in this section. Fig. 4-2 presents the switching modulation block diagram. The Time Reference block includes a timer which produces an angle that rotates repetitively from *0* to $2\pi$ with the desired AC frequency (i.e. *60 Hz*). Any additional control related to the angle, such as delay angle control or power factor (PF) correction, may be joined at this point of the model. The produced angle and the modulation index value determine the reference current vector. The next block is called reference vector locator. The location of the reference vector is found in this block. Consequently, the sector number and the region type are the outputs of this block. Since, vector selections and dwell time calculations at every sector are applied to the mirrored sector on sector number 1, the angle of the reference vector is also mirrored on sector 1.

The next step is to calculate the dwell times corresponding to three chosen switching vectors. The dwell time calculator block is responsible for the dwell times. To execute the calculations, the location of the reference vector, modulation index and sampling time are provided as the inputs to the block.

As a final step, the switching sequence is applied to converters by producing proper gating signals. The comparator inputs determine the proper switching sequence at every sampling period. In other words, DC current balance control determines the proper switching states based on the designed off-line look-up tables. The sector number and region type inputs determine the triangle in which the reference vector is located. Three dwell times are provided from previous steps and comparator signals are employed with the DC current balance control method. As mentioned, the output gating signals are applied to parallel converter systems.

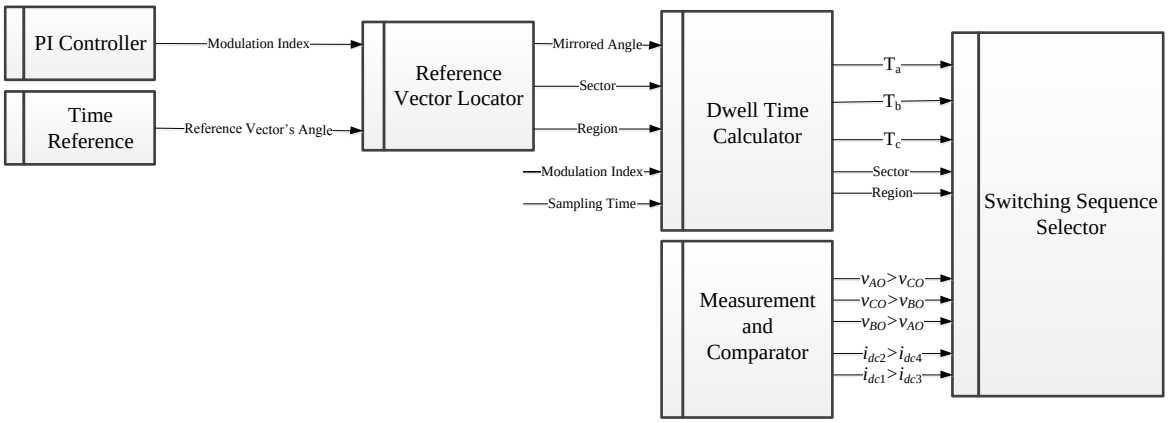



Fig. 4-2 Model of space vector modulation

## 4.3 Steady state analysis - Harmonic performance

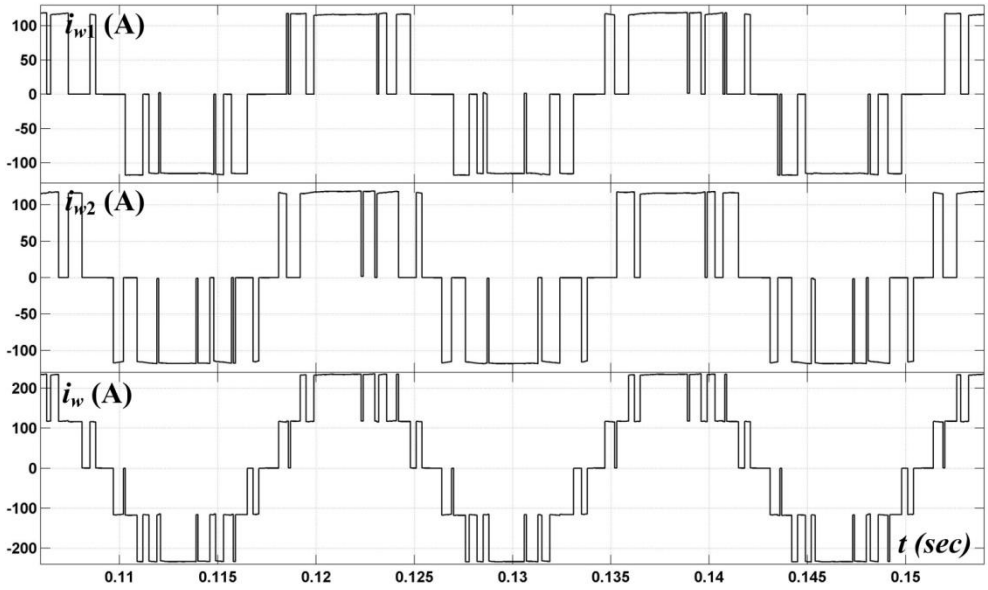
The steady state performance study is carried out on both rectifier and inverter sides. As a matter of fact, the simulation results are almost similar at both sides. Due to the symmetrical topology of CSR and CSI and the fact that same switching modulation is applied on multi-level converters, similar waveforms and harmonic performance are expected.

### 4.3.1 Rectifier

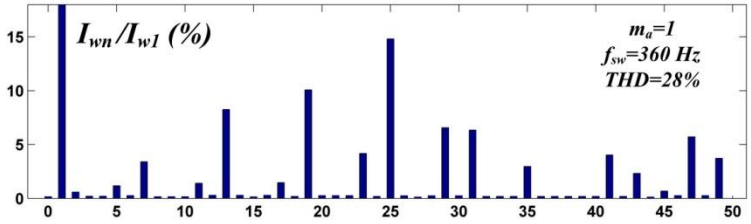
The simulation results for the input current $i_w$ of rectifier working at $f= 60\ Hz$, $T_s= 1/1080\ s$ and $m_a= 1$ is shown in Fig. 4-3. First two waveforms are the input switching currents for each single-level rectifiers and the last waveform is the input current of multi-level parallel rectifier which is sum of the first waveforms. The input current of each rectifier has three levels, while the output current of the multi-level rectifier has five levels.

Minor differences are seen in two 3-level currents as time runs. Since, the DC current balance control employs different switching states due to circuit circumstances, the minor differences are expected. However, analyzing the waveforms in period of some cycles shows that both single-bridge rectifiers produce an almost identical switching current on the AC side. The switching frequency is *360 Hz* at both single-bridge rectifiers. In addition, almost the same conduction time appears at both rectifiers. Therefore, similar fatigue and heat stress are expected in both single-bridge rectifiers.

Different switching states employed with the switching modulation may cause minor differences in switching current of each single-bridge rectifier at different cycles. All those distinctive switching states are representing the same switching vector. Consequently, the 5-level input current still repeats an identical pattern in different cycles. Fig. 4-3-b and c present the harmonic profile of the 5-level rectifier's input current $i_w$ shown on Fig. 4-3-a. Although each single-bridge rectifier contains large harmonic distortion (The THD value is 56% and 54% for the first and second rectifier), the multi-level rectifier contains much less harmonics and the THD value is reduced to a great extent. Reduction in harmonic content of the chopped current brings the opportunity to reduce the filter capacitor size which will be investigated in details in Section 4.3.2.




(a) Waveforms



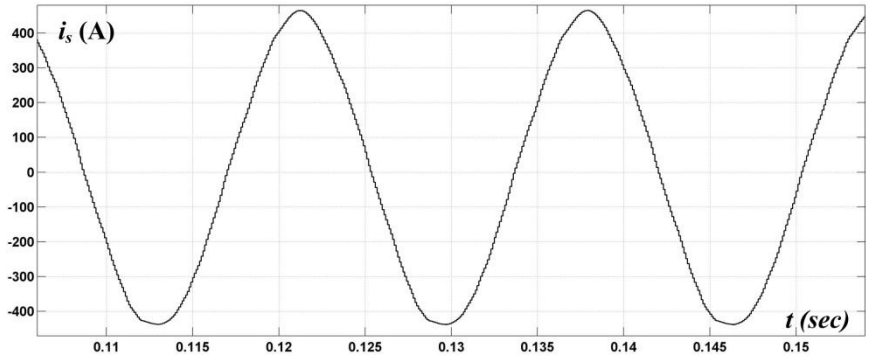

(b) Harmonic profile

(c) Harmonic content.

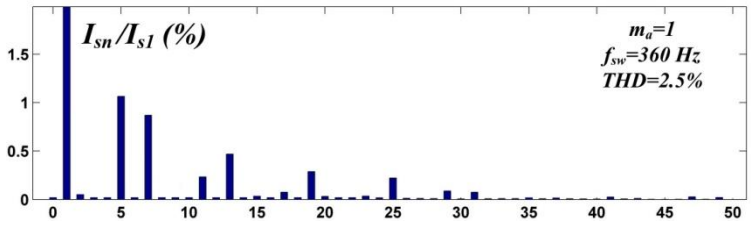
| $5^{th}$ | $7^{th}$ | $11^{th}$ | $13^{th}$ | $17^{th}$ | $19^{th}$ | $23^{th}$ |
|---|---|---|---|---|---|---|
| 1.17% | 3.41% | 1.40% | 8.26% | 1.46% | 10.09% | 4.18% |

Fig. 4-3 Input current of rectifier $i_w$ ($m_a$=*1*)

The input 5-level switching current $i_w$ of the multi-level rectifier contains high order harmonics. The high order harmonic content is eliminated with the three-phase filter capacitor. Consequently, the AC line current contains low distortion. The simulation result for the AC line current $i_s$ is shown in Fig. 4-4.




(a) Waveforms




(b) Harmonic profile

(c) Harmonic content.

| $5^{th}$ | $7^{th}$ | $11^{th}$ | $13^{th}$ | $17^{th}$ | $19^{th}$ | $23^{th}$ |
|---|---|---|---|---|---|---|
| 1.06% | 0.87% | 0.23% | 0.47% | 0.07% | 0.29% | 0.03% |

Fig. 4-4 AC line current $i_s$ ($m_a$=1)

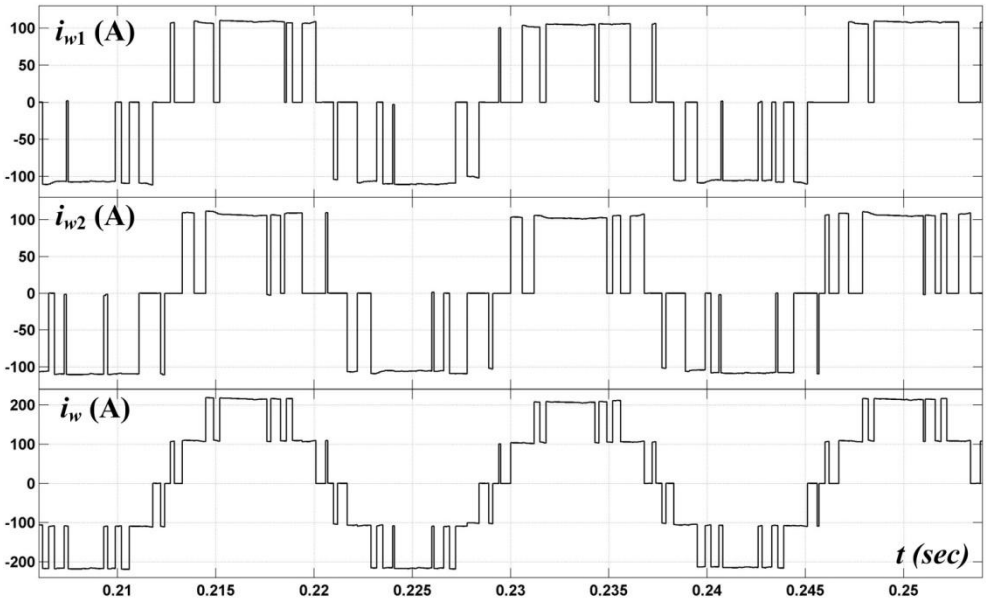
As shown above, the line current is in sinusoidal shape which satisfies power supply side harmonic constraints. Fig. 4-4-b and c present the harmonic profile and content of the AC line current shown in Fig. 4-4-a. High order harmonics are completely eliminated by the three-phase filter capacitor located at the input terminal of the multi-level rectifier. Low order harmonics are reduced to a great extent. Consequently, the proposed converter provides superior harmonic performance on the AC line.

### 4.3.2 Inverter

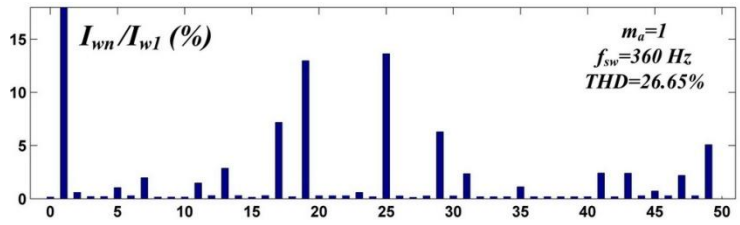
In this section, the harmonic performance of the multi-level inverter is investigated in detail. The simulation results for the output current $i_w$ of inverter is shown in Fig. 4-5 for the multi-level inverter working at $f= 60\ Hz$, $T_s= 1/1080\ s$ and $m_a= 1$. Although there are some differences in the output current of the single-bridge inverters in different cycles, the five-level output current of the multi-level inverter repeats an identical pattern. The switching frequency is *360 Hz* on the both single-bridge inverters. The switching frequency is as same as the switching frequency of the single-bridge inverters.

The output current of each single-bridge inverter has three levels and the output current of the multi-level inverter has five levels. Since, the same switching modulation is applied to the multi-level rectifier and multi-level inverter, almost similar waveforms are expected which is proven with the simulation results. Fig. 4-5-b and c present the harmonic profile and content of the output current of the inverter $i_w$. The THD value of the 5-level inverter is 26.65% while the THD value is % and % for single-bridge inverters. The improvement on the harmonic performance of the multi-level inverter verifies the effectiveness of the designed modulation scheme.

The 5-level switching current $i_w$ of the multi-level inverter contains high order harmonics. The high order harmonic content is eliminated with the filter capacitor. Consequently, the AC load current contains low distortion. The simulation results for the AC load current $i_L$ is shown in Fig. 4-6 when $m_a=1$ and $C_f=0.3$.




(a) Waveforms

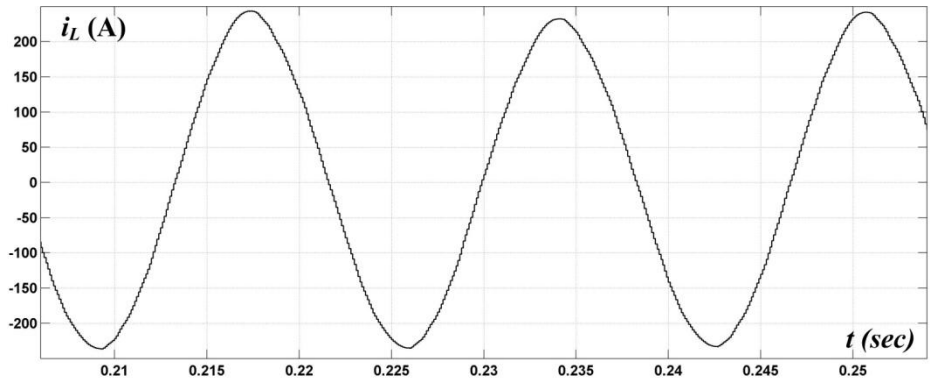



(b) Harmonic profile

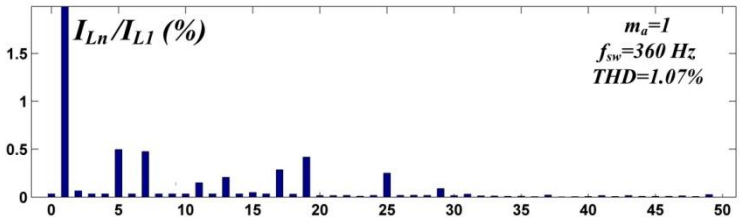
(c) Harmonic content.

| $5^{th}$ | $7^{th}$ | $11^{th}$ | $13^{th}$ | $17^{th}$ | $19^{th}$ | $23^{th}$ |
|---|---|---|---|---|---|---|
| 0.99% | 1.98% | 1.40% | 2.69% | 6.86% | 13.19% | 0.61% |

Fig. 4-5 Output current of inverter $i_w$ ($m_a$=*1*)




(a) Waveforms




(b) Harmonic profile

(c) Harmonic content.

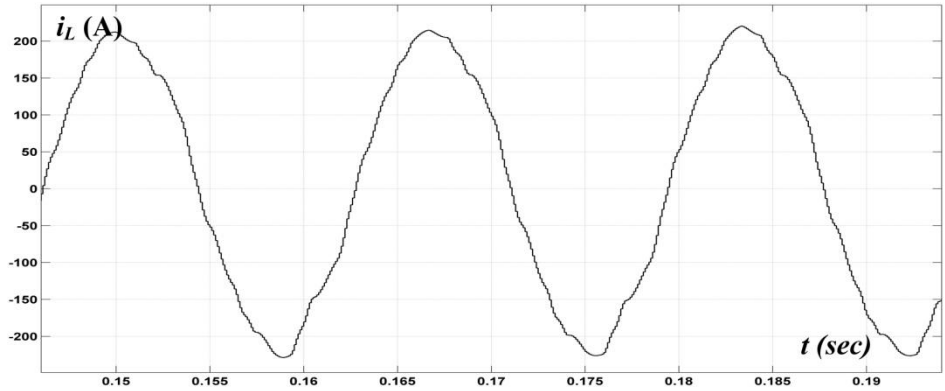
| $5^{th}$ | $7^{th}$ | $11^{th}$ | $13^{th}$ | $17^{th}$ | $19^{th}$ | $23^{th}$ |
|---|---|---|---|---|---|---|
| 0.50% | 0.47% | 0.15% | 0.21% | 0.28% | 0.42% | 0.01% |

Fig. 4-6 AC load current $i_L$ ($m_a$=1, $C_f$=0.3 *pu*)

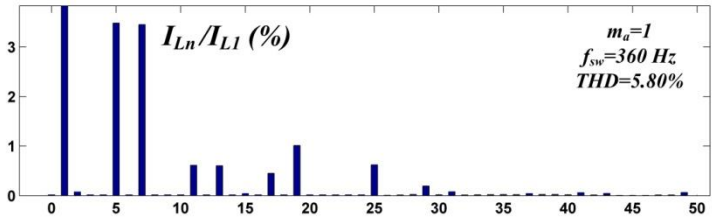
As shown above, the load side current is in sinusoidal shape which satisfies load side harmonic constraints. Fig. 4-6-b and c present the harmonic profile of the AC load current $i_L$ shown on Fig. 4-6-a. High order harmonics are completely eliminated by the three-phase filter capacitor located at the output terminal of multi-level inverter. Low order harmonics are reduced to a great extent. Consequently, the proposed converter provides superior harmonic performance on the AC load side.

Employing the multi-level converter and the proposed switching scheme, the harmonic content of the AC waveforms is reduced to a great extent. Therefore, there is an opportunity to reduce the

size of the filter capacitors. The simulation results for the AC load current $i_L$ is shown in Fig. 4-7 when $m_a=0.95$ and $C_f=0.1$. Fig. 4-7-b and c present the harmonic profile of the AC load current $i_L$ shown on Fig. 4-7-a. The filter capacitor value is reduced to one third. However, the harmonic performance of multi-level converter is still acceptable. It is a responsibility of the designer to choose the proper value of the filter capacitor to satisfy the application demands.




(a) Waveforms




(b) Harmonic profile

(c) Harmonic content.

| $5^{th}$ | $7^{th}$ | $11^{th}$ | $13^{th}$ | $17^{th}$ | $19^{th}$ | $23^{th}$ |
|---|---|---|---|---|---|---|
| 3.49% | 3.46% | 0.65% | 0.59% | 0.46% | 1.02% | 0.05% |

Fig. 4-7 AC load current $i_L$ ($m_a=0.95$, $C_f=0.1$ *pu*)

### 4.3.3 Harmonic performance comparioson between single-bridge and multi-level converters

To compare the harmonic performance of the single-bridge and multi-level converters, simulation is run at different modulation index values for a single-bridge CSI employing controversial space vector modulation and the proposed 5-level CSI employing the proposed space vector modulation.

Table 4-1 provides the comparison of the THD content of the switching current $i_w$ for the proposed multi-level inverter and single-bridge inverter at different $m_a$ values. Fig. 4-8 illustrates the same comparison.

Table 4-1 THD comparison of $i_w$ at different $m_a$ values.

| $m_a$ | 0.3 | 0.4 | 0.5 | 0.6 | 0.7 | 0.8 | 0.9 | 1 |
|---|---|---|---|---|---|---|---|---|
| **Multi-level** | 98% | 84% | 69% | 50% | 41% | 36% | 34% | 28% |
| **Single-bridge** | 178% | 145% | 122% | 103% | 87% | 72% | 59% | 46% |

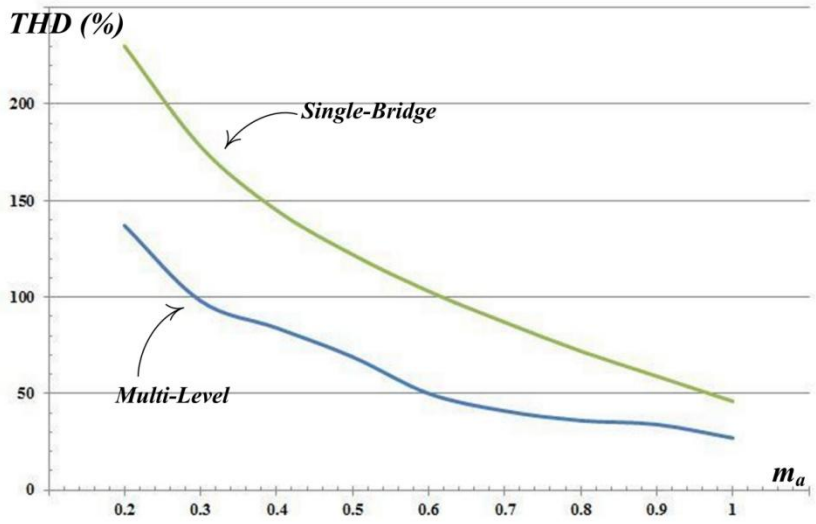



Fig. 4-8 THD comparison of $i_w$ at different $m_a$ values

The THD value corresponding to the multi-level inverter is almost half of the THD value for single-bridge inverter. In other words, the AC output current of the proposed 5-level inverter contains less harmonic content than similar single-bridge inverter.

To investigate the harmonic content of the multi-level converter, the simulation is run at the specific modulation index $m_a$ value. The detailed low order harmonics comparison between the multi-level and single-level inverters at $m_a=1$ is presented in Table 4-2.

Table 4-2 Low order harmonics comparison ($m_a=1$).

| | | **5th** | **7th** | **11th** |
|---|---|---|---|---|
| $i_w$ | Multi-level | 0.99% | 1.98% | 1.40% |
| | Single-bridge | 8.24% | 4.07% | 1.26% |
| $i_L$ | Multi-level | 0.50% | 0.47% | 0.15% |
| | Single-bridge | 3.19% | 0.79% | 0.08% |

Generally, the 5th harmonic content generated in the AC terminal of the proposed multi-level inverter is less than one eighth of the 5th harmonic generated on the single-bridge CSC. The 7th harmonic content is less than half. Since the same filter capacitor is used, the reduction of low order harmonics is a result of the designed SVM. The comparison proves the effectiveness of the proposed modulation scheme. Dividing the space vector diagram to more areas, better estimation of the AC current reference vector and producing five levels at the output terminals of the inverter result in better harmonic performance in the multi-level CSI. Minimization of low order harmonics using the 5-level CSI and the proposed space vector modulation method eliminates the

need for bulky and costly large filters and transformers. It is a great advantage of using the proposed multi-level CSI.

The THD performance is studied on the inverter side. However, the same performance is certain on the rectifier side.

### 4.3.4 Harmonic performance at different switching frequencies

When the switching sequence is designed, the device switching frequency is controllable with the sampling period time $T_s$. The larger the sampling period, the lower switching frequency is achievable. However, a decline in converter's performance is expected at very low switching frequencies. On the other hand, increasing the switching frequency to very high frequencies will not improve the performance. As a matter of fact, the switching frequency and subsequently, the sampling time must be maintained in a specific range. In this part, the harmonic performance of the multi-level converter at different switching frequencies is studied. The chosen frequencies are within the range that the converter system performs its essential features. The THD value of the inverter's output current $i_w$ and AC load current $i_L$ when $C_f$=0.3 pu are presented in Table 4-3.

Table 4-3 THD of $i_w$ and $i_L$ at different switching frequencies when ($m_a=1$).

| $f_{sw}$ | 300 | 360 | 480 | 600 |
|---|---|---|---|---|
| **THD of $i_w$** | 29% | 26% | 27% | 25% |
| **THD of $i_L$** | 2.24% | 2.10% | 0.94% | 0.76% |

Although there is not considerable change in THD value of the output current of the multi-level inverter $i_w$, the THD value of the load current $i_L$ is reduced to one-third by increasing the switching frequency from *300 Hz* to *600 Hz*. As a matter of fact, applying the switching modulation at higher switching frequency reduces the low order harmonics of the AC currents and AC voltages.

The reduced distortion is not that significant to change the THD value of $i_w$. However, it brings a great deduction to the THD value corresponding to $i_L$.

Increasing the switching frequency improves the harmonic performance of the converter, however, increase in switching loss and higher thermal stress is inevitable. It is necessary to choose the proper switching frequency for every application in specific to satisfy the application demand and avoid any extra cost.

## 4.4 Dynamic analysis – DC current and load voltage control

To improve the dynamic performance of the multi-level CSC, SVM switching method is employed which provides active and continuous $m_a$ control. The DC current is measured and compared with the reference DC current. The PI controller on the rectifier side controls the modulation index to adjust the DC current to the reference value. The same process is done on the inverter side to adjust the load voltage to the reference load voltage. PI controllers are illustrated in Fig. 4-9.

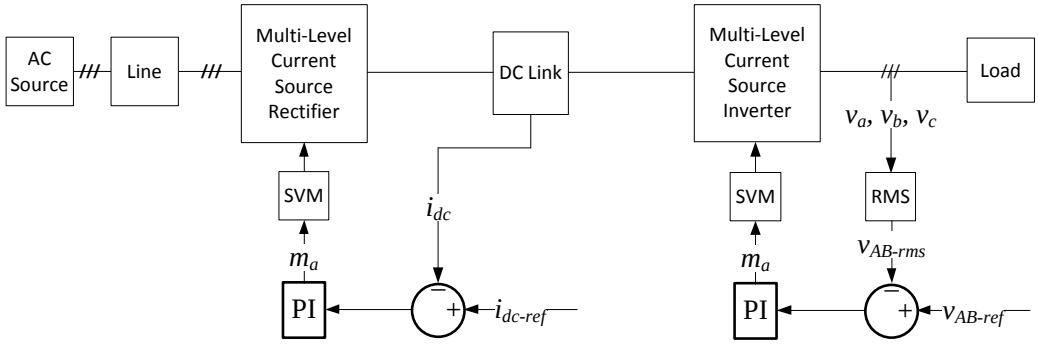



Fig. 4-9 PI controllers block diagram

### 4.4.1 DC current control

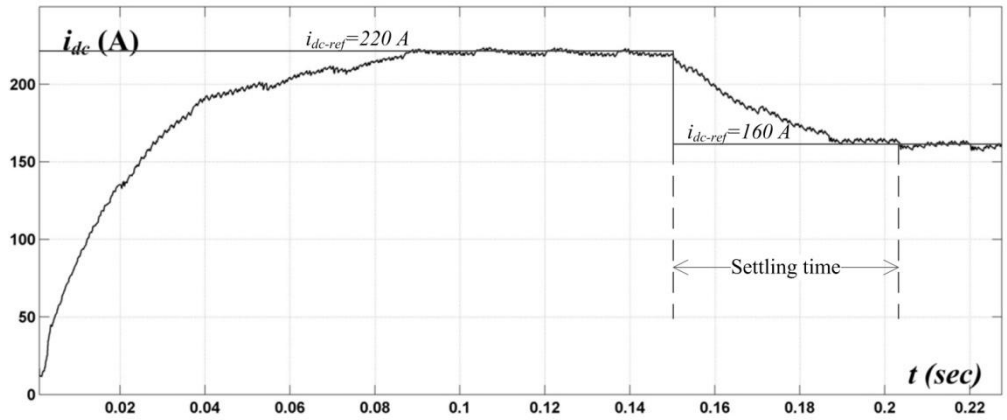
The PI controller on the rectifier side is designed to control the DC link current value $i_{dc}$. Modulation index is adjusted to maintain the DC current at the desired reference value. The most effective parameter in dynamic performance of current source rectifier is DC choke value. Increasing the DC choke, however reduces the ripples of DC link currents, weakens the dynamic performance of the rectifier. Generally, the DC current should contain less than *15%* ripples. The size of the DC choke is normally in the range of *0.5* to *0.8 pu*. In this section, the dynamic performance and ripples of DC link currents are compared at two different DC choke values.

The simulation results for the DC current $i_{dc}$ at the output of the rectifier working at $f= 60\ Hz$, $T_s= 1/1080\ s$ is shown in Fig. 4-10-a. The reference DC current at the PI controller is changed from *220 A* to *160 A* at $t= 0.15\ sec$. The PI controller adjusts $m_a$ to control the DC link current. The modulation index $m_a$ is shown in Fig. 4-10-b.

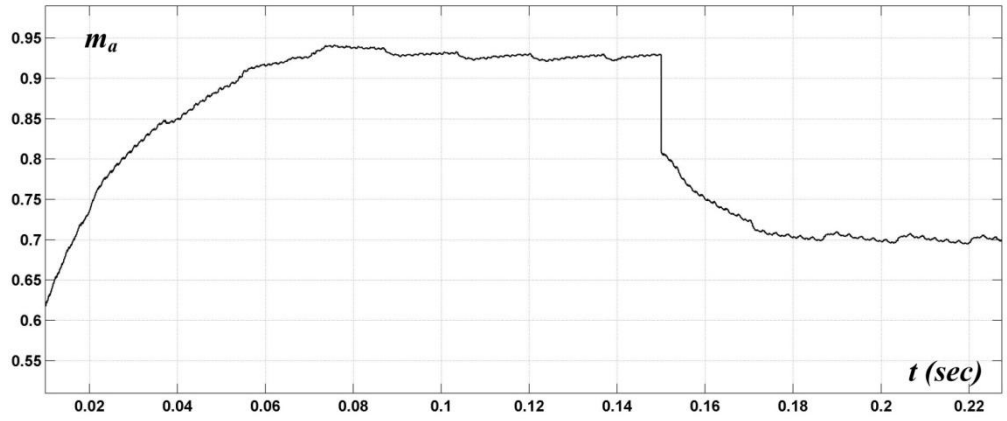
The DC link current $i_{dc}$ increases from zero (the initial value) to reach the reference DC current value which is *220 A*. The DC current is maintained at *220 A*. Once the DC current reference value is changed to *160 A*, the DC link current decreases to reach and track the reference DC current. The modulation index is increased to $m_a=0.93$ to increase and maintain the DC current at the reference value which is *220 A*. Since the reference value is changed to *160 A* at $t= 0.15\ sec$ the modulation index is decreased to $m_a=0.7$ to reduce the DC link current and adjust it to *160 A*.

The chosen $L_d$ is much higher than regular chosen DC chokes in practice. The high DC choke limits the ripples over DC link current to less than *2%*. On the other hand, the rectifier shows slow response to the reference current change. The settling time is *0.05 s*. To investigate the impact of the DC choke value, the $L_d$ in decreased to *0.3 pu* and simulation is run with the same parameters. The simulation results the DC current $i_{dc}$ and modulation index $m_a$ are shown in Fig. 4-11.

The ripples over the DC link current increases to *15%*. On the other hand, dynamic performance of the rectifier is improved. The settling time is reduced to *0.025 s*. Table 4-4 presents a summary of dynamic performance of rectifier investigation. It is a responsibility of designer to choose the proper value of DC chokes to improve the dynamic performance of the current source converter. Besides, the chosen DC chokes must limit the ripples to a desired percentage.

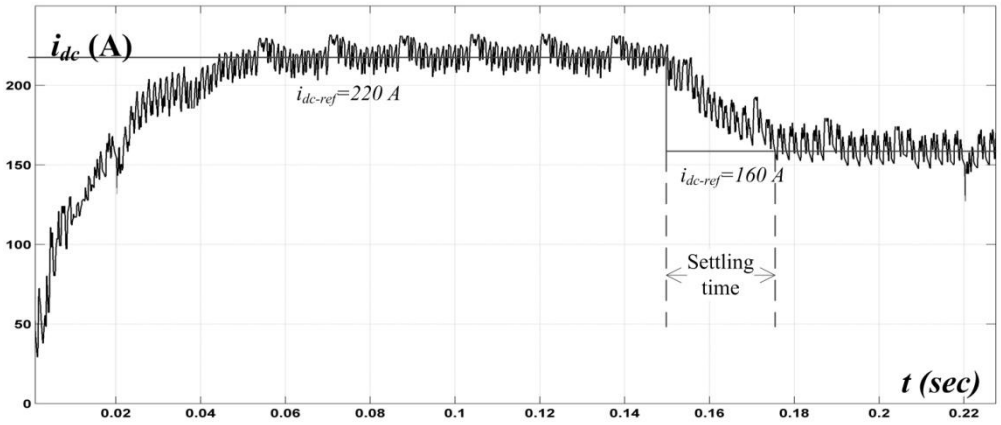



(a) DC link current $i_{dc}$

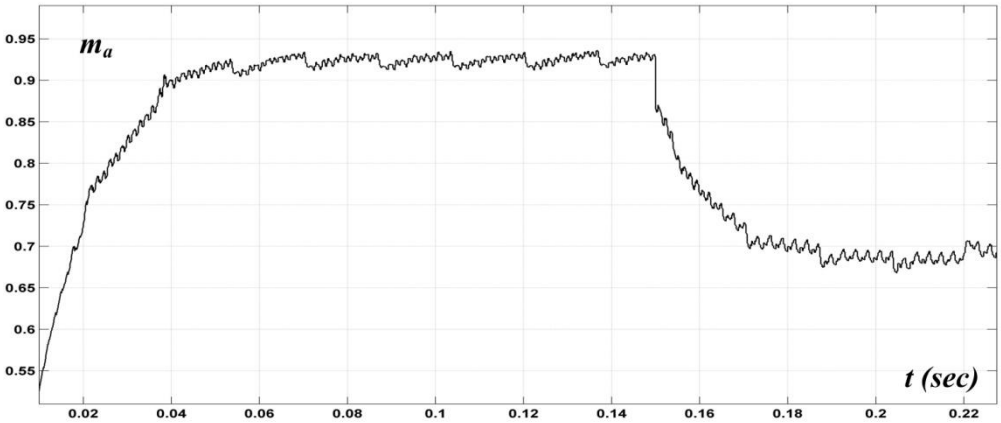



(b) Modulation index $m_a$

Fig. 4-10 DC link current control ($L_d$=*1.5 pu*)




(a) DC link current $i_{dc}$




(b) Modulation index $m_a$

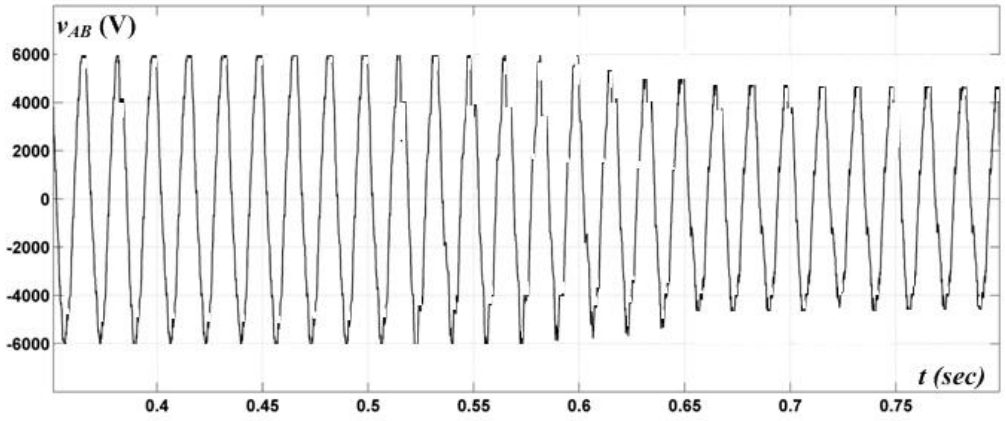
Fig. 4-11 DC link current control ($L_d$=*0.3 pu*)

Table 4-4 Investigation of dynamic performance of rectifier.

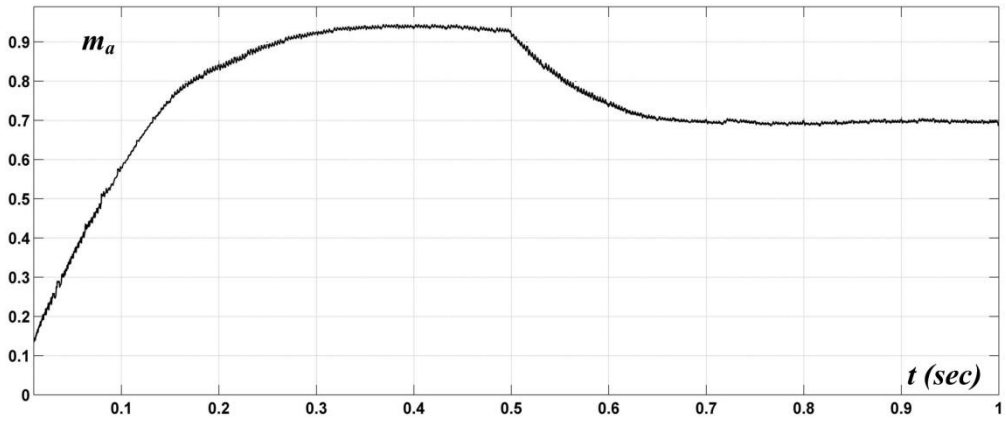
| ***$L_d$ (pu)*** | 1.5 | 0.3 |
|---|---|---|
| **Ripple** | 2% | 15% |
| **Settling time (s)** | 0.05 | 0.025 |

### 4.4.2 AC load voltage control

The PI controller on the inverter side is designed to control the AC load voltage value $v_{AB}$. Modulation index is adjusted to maintain the AC voltage at the desired reference value. The simulation results for the AC load line-line voltage $v_{AB}$ at the output of the inverter working at $f$= *60 Hz*, $T_s$= *1/1080 s* is shown in Fig. 4-12-a. The reference AC voltage at the PI controller changes from *4160 V* to *3200 V* at $t$= *0.5 sec*.




(a) AC load voltage (L-L)




(b) Modulation index $m_a$

Fig. 4-12 Load voltage control

As shown, the modulation index increases to $m_a=0.94$ to increase and maintain the AC load voltage at the reference value which is *4160 V*. Since the reference value is changed to *3200 V* at *t= 0.5 sec* the modulation index is decreased to $m_a=0.7$ to reduce the line to line load voltage and adjust it to *3200 V*.

Once the load voltage reference value is changed to *3200 V*, the load voltage $v_{AB}$ decreases to reach and track the reference voltage. The PI controller adjusts $m_a$ to control the load voltage. The modulation index $m_a$ is shown in Fig. 4-12-b.

## 4.5 Conclusion

The 5-level current source converter and proposed space vector modulation is modeled in Simulink. The simulation is run to investigate the performance of the converter. The steady state performance of the converter is studied by providing the steady state waveforms and harmonic profile of chopped and sinusoidal currents of rectifier and inverter. The chopped switching currents contain high order harmonics. However, the high order harmonics are eliminated by three-phase filter capacitor. Consequently, the AC line and load currents are free of high order harmonics. The investigation shows that the proposed 5-level CSC generates less harmonics in comparison to single-bridge CSC which brings an opportunity to reduce the size of filter capacitors.

The dynamic performance of the converter is studied by discussions on the designed PI controllers. The control loop on the rectifier adjusts the modulation index to control the DC link current while the load voltage is adjustable through controlling the modulation index on the inverter side. The full range and continuous modulation index control improves the dynamic

performance of the 5-level CSC. In addition, reducing the size of DC chokes will bring a faster dynamic response of converter. However, higher ripple is seen on DC links. It is of a great necessity to achieve to a proper DC choke value to satisfy dynamic performance and DC link ripple requirements of any application.

# Chapter 5
# Conclusions

Increasing demand for high power converters in drive applications operating at medium voltage range provides a vast field for multi-level current source converters (CSCs). The main feature of multi-level CSC is to satisfy high power demands. CSC has simple topology and operates at low device switching frequency. The main drawback of CSC is that the dynamic performance is limited by large DC link inductance. In addition, when converters are connected in parallel, different circuit parameters, especially manufacturing tolerance in DC chokes and un-equal ON-state voltages of the switching devices may cause unbalanced DC link currents. Unbalanced DC currents lead to generation of current harmonics, uneven power division between converters, increase in the total loss and the overall performance decline of the converter system. Consequently, elimination of unbalanced DC currents in multi-level CSC is necessary.

The major modulation schemes for the CSC are trapezoidal pulse-width modulation (TPWM), selective harmonic elimination (SHE) and space vector modulation (SVM). SVM provides continuous modulation index control. However, the generated currents contain low order ($5^{th}$ and $7^{th}$) harmonics. To reduce the harmonic content of generated currents and voltages the modulation method must be developed to meet stringent industry requirement. In this thesis, SVM is modified for a 5-level CSC to generate 5-level chopped current which results in less AC current and AC voltage distortion. The modulation is augmented with DC current balance

control. The proposed DC current balance control employs redundant switching states of Small and Medium vectors to equalize DC link currents.

## 5.1 Contributions and conclusions

The main contributions and conclusion of this research work can be summarized as following:

**1) 5-level parallel current source converter topology is presented.**

Industry demand for high power drives motivates researchers to extend research on high power drive systems. Therefore, 5-level parallel CSC is chosen to be developed to meet industry demands. The introduced configuration is a back to back connection of a 5-level CSR and a 5-level CSI with a common DC connection. Two parallel connected single-bridge converters constitute the 5-level converter at rectifier and inverter sides. Three-phase capacitors at the input terminal of CSR and the output terminal of CSI are necessary to assist switching commutation and to filter high order harmonics of generated currents. The DC link connection and DC chokes are discussed in detail. The main responsibility of DC chokes is to limit the DC link current ripples. However, the dynamic performance of the CSC is limited by using large DC chokes.

**2) Space vector modulation is developed for 5-level parallel converter.**

SVM provides active and continuous modulation index control which may be employed to improve the dynamic performance of the multi-level CSC. Unfortunately, currents generated by SVM contain low order ($5^{th}$ and $7^{th}$) harmonics. Therefore, the switching scheme must be modified to improve the harmonic performance of the 5-level CSC. The designed SVM contains eighty one possible switching states. The calculations presented in this thesis show that the switching states result in 19 switching vectors which are illustrated on the space vector diagram. The space vector reference is shown on the diagram which rotates with the AC frequency. The

length of the reference vector represents the $m_a$ value. The modulation method is based on choosing three adjacent space vectors to synthesize the reference vector at every switching state. The switching sequence is designed to improve the harmonic performance of the converter and eliminate unbalanced DC currents.

**3) A fast and effective DC current balance control is proposed.**

The main technical challenge when two current source converters are connected in parallel is circulating current or unbalanced DC current. Since general decline in performance of converter is the result of unbalanced DC currents, it is necessary to augment the proposed 5-level CSC and the switching modulation with a DC current balance control. Investigation of effects of space vectors on the DC currents shows that two redundant switching states with inverse effect on the DC link currents are available for Small and Medium vectors. At every moment of switching, the DC link currents and line to line AC voltages are measured. The proper switching state is determined based circuit circumstances and the designed switching sequence presented in Appendix III. The performance study of the DC current balance control proves that the controller effectively balances the DC currents. The controller reacts instantaneously to any circuit disturbances.

**4) The switching modulation is modified to improve the harmonic performance.**

Since SVM is chosen to generate AC currents and voltages, high distortion is expected on the AC line and load. Industry stringent demand motivates researchers to modify and improve the existing switching schemes. Therefore, the SVM is developed specifically for 5-level parallel current source converter. Dividing the space vector diagram to 30 areas and choosing three adjacent vectors for each area improve the generated estimation of the reference current vector. Hence, the harmonic performance of converter improved effectively. The presented harmonic

performance investigation shows that the THD value of chopped current generated by 5-level converter is half of the same current generated by single-bridge converter. The improvement in harmonic performance brings the opportunity to reduce the size of filter capacitor that reduces the cost of converter system. In addition, the frequency of possible LC resonance is moved to higher frequencies.

**5) The minimized device switching frequency is achieved.**

The device switching frequency is an effective parameter in converter's loss and thermal stress. It is more critical to limit the switching frequency to a few hundred Hertz in high power drive applications. The switching requirements limit the number of devices involved at each transient period to one switch-ON and one switch-OFF at each single-bridge converter. However, the proper switching sequence design can reduce the number of devices involved at each transient period to only one switch-ON and one switch-OFF at multi-level converter. In other words, the switching frequency can be reduced to almost half of the highest possible frequency. In this thesis, the order of space vectors is designed to transient from each space vector to the next vector involves less devices switching. To optimize the design, the transient process between vectors corresponding to the same area and the transient process between adjacent areas are considered. As a result, the switching frequency is the lowest possible switching frequency for each sampling time.

**6) The performance is studied and verified with simulation.**

The simulation results verify the expected superior harmonic performance on both AC line and AC load sides. The proposed multi-level converter generates almost half of harmonic distortion in comparison to single-bridge CSC. In addition, low order harmonics ($5^{th}$ and $7^{th}$) are reduced to a great extent which eliminates the need of bulky and costly phase-shifting

transformers and large filters. The harmonic performance of the converter is studied at different switching frequencies. Increasing the switching frequency improves the harmonic performance of the converter. On the other hand, extra cost caused by increased switching loss is inevitable. The proper switching frequency must be chosen to satisfy application stringent demands and avoid any extra cost.

The study of DC link current balance control performance shows that how DC link currents track the same value of current when the controller is enabled. On the contrary, DC link currents diverge to different values while the controller is disabled.

The dynamic performance study is carried out on both rectifier and inverter. The PI controller on the rectifier side adjusts the value of DC current through $m_a$ control while the $m_a$ controls the AC load voltage on the inverter side. The dynamic performance of the CSC is limited by large DC chokes. The presented investigation shows that the dynamic performance of the 5-level converter is improved by using smaller DC chokes, but this cause higher ripple on the DC link currents. The DC choke must be designed to satisfy dynamic performance demands and DC link ripple requirements of any application in specific.

# Appendix I
# Effect of Medium vectors on DC currents

In this section, the effect of Medium vectors on DC currents is illustrated. For each Medium vector, the effect of the vector on the DC currents is illustrated and then the proper switching state is chosen at distinctive circuit circumstances.

Table I-14 Effect of switching states of Medium vector $\vec{I}_7$ on DC currents

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [12 16] or [16 12] | $v_{BO}=v_{CO}$ | X | X | X | X |
| [12 16] | $v_{BO}>v_{CO}$ | X | ↓ | X | ↑ |
| | $v_{BO}<v_{CO}$ | X | ↑ | X | ↓ |
| [16 12] | $v_{BO}>v_{CO}$ | X | ↑ | X | ↓ |
| | $v_{BO}<v_{CO}$ | X | ↓ | X | ↑ |

Table I-15 Selected switching state of Medium vector $\vec{I}_7$

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{CO}>v_{BO}$ | $i_{d4}>i_{d2}$ | **[12 16]** |
| $v_{BO}>v_{CO}$ | $i_{d2}>i_{d4}$ | |
| $v_{CO}>v_{BO}$ | $i_{d2}>i_{d4}$ | **[16 12]** |
| $v_{BO}>v_{CO}$ | $i_{d4}>i_{d2}$ | |

Table I-16 Effect of switching states of Medium vector $\vec{I}_8$ on DC currents

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [12 32] or [32 12] | $v_{BO}=v_{AO}$ | X | X | X | X |
| [32 12] | $v_{BO}>v_{AO}$ | ↓ | X | ↑ | X |

| | | | | | |
|---|---|---|---|---|---|
| | $v_{BO}<v_{AO}$ | ↑ | X | ↓ | X |
| [12 32] | $v_{BO}>v_{AO}$ | ↑ | X | ↓ | X |
| | $v_{BO}<v_{AO}$ | ↓ | X | ↑ | X |

Table I-17 Selected switching state of Medium vector $\vec{I}_8$

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{BO}>v_{AO}$ | $i_{d1}>i_{d3}$ | **[32 12]** |
| $v_{AO}>v_{BO}$ | $i_{d3}>i_{d1}$ | |
| $v_{BO}>v_{AO}$ | $i_{d3}>i_{d1}$ | **[12 32]** |
| $v_{AO}>v_{BO}$ | $i_{d1}>i_{d3}$ | |

Table I-18 Effect of switching states of Medium vector $\vec{I}_9$ on DC currents

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [32 34] or [34 32] | $v_{AO}=v_{CO}$ | X | X | X | X |
| [32 34] | $v_{AO}>v_{CO}$ | X | ↓ | X | ↑ |
| | $v_{AO}<v_{CO}$ | X | ↑ | X | ↓ |
| [34 32] | $v_{AO}>v_{CO}$ | X | ↑ | X | ↓ |
| | $v_{AO}<v_{CO}$ | X | ↓ | X | ↑ |

Table I-19 Selected switching state of Medium vector $\vec{I}_9$

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{CO}>v_{AO}$ | $i_{d4}>i_{d2}$ | **[32 34]** |
| $v_{AO}>v_{CO}$ | $i_{d2}>i_{d4}$ | |
| $v_{CO}>v_{AO}$ | $i_{d2}>i_{d4}$ | **[34 32]** |
| $v_{AO}>v_{CO}$ | $i_{d4}>i_{d2}$ | |

Table I-20 Effect of switching states of Medium vector $\vec{I}_{10}$ on DC currents

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [34 54] or [54 34] | $v_{BO}=v_{AO}$ | X | X | X | X |
| [34 54] | $v_{BO}>v_{CO}$ | ↓ | X | ↑ | X |
| | $v_{BO}<v_{CO}$ | ↑ | X | ↓ | X |

| | | | | | |
|---|---|---|---|---|---|
| [54 34] | $v_{BO}>v_{CO}$ | ↑ | X | ↓ | X |
| | $v_{BO}<v_{CO}$ | ↓ | X | ↑ | X |

Table I-21 Selected switching state of Medium vector $\vec{I}_{10}$

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{BO}>v_{CO}$ | $i_{d1}>i_{d3}$ | **[34 54]** |
| $v_{CO}>v_{BO}$ | $i_{d3}>i_{d1}$ | |
| $v_{BO}>v_{CO}$ | $i_{d3}>i_{d1}$ | **[54 34]** |
| $v_{CO}>v_{BO}$ | $i_{d1}>i_{d3}$ | |

Table I-22 Effect of switching states of Medium vector $\vec{I}_{11}$ on DC currents

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [54 56] or [56 54] | $v_{AO}=v_{CO}$ | X | X | X | X |
| [54 56] | $v_{AO}>v_{BO}$ | X | ↓ | X | ↑ |
| | $v_{AO}<v_{BO}$ | X | ↑ | X | ↓ |
| [56 54] | $v_{AO}>v_{BO}$ | X | ↑ | X | ↓ |
| | $v_{AO}<v_{BO}$ | X | ↓ | X | ↑ |

Table I-23 Selected switching state of Medium vector $\vec{I}_{11}$

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{AO}>v_{BO}$ | $i_{d4}>i_{d2}$ | **[54 56]** |
| $v_{BO}>v_{AO}$ | $i_{d2}>i_{d4}$ | |
| $v_{AO}>v_{BO}$ | $i_{d2}>i_{d4}$ | **[56 54]** |
| $v_{BO}>v_{AO}$ | $i_{d4}>i_{d2}$ | |

Table I-24 Effect of switching states of Medium vector $\vec{I}_{12}$ on DC currents

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [16 56] or [56 16] | $v_{BO}=v_{AO}$ | X | X | X | X |

| | | | | | |
|---|---|---|---|---|---|
| [16 56] | $v_{AO}>v_{CO}$ | ↓ | X | ↑ | X |
| | $v_{AO}<v_{CO}$ | ↑ | X | ↓ | X |
| [56 16] | $v_{AO}>v_{CO}$ | ↑ | X | ↓ | X |
| | $v_{AO}<v_{CO}$ | ↓ | X | ↑ | X |

Table I-25 Selected switching state of Medium vector $\vec{I}_{12}$

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{AO}>v_{CO}$ | $i_{d1}>i_{d3}$ | **[16 56]** |
| $v_{CO}>v_{AO}$ | $i_{d3}>i_{d1}$ | |
| $v_{AO}>v_{CO}$ | $i_{d3}>i_{d1}$ | **[56 16]** |
| $v_{CO}>v_{AO}$ | $i_{d1}>i_{d3}$ | |

In summary, for each Medium vector, one switching state can make the DC current increase while the other can make the same current decrease. The Medium vectors located in even sectors affect the magnitude of the positive DC bus currents. On the other hand, the Medium vectors belonging to odd sectors affect the magnitude of the negative DC bus currents.

# Appendix II
# Effect of Small vectors on DC currents

In this section, the effect of Small vectors on DC currents is illustrated. For each Small vector, pair of switching states with same switches as the Medium vector of corresponding sector is chosen. Different pair of switching states is chosen for different sectors. The effect of the vector on the DC currents is illustrated at either corresponding sector. Finally, the proper switching state is chosen at distinctive circuit circumstances.

Table II-1 Employed switching states of Small vector $\vec{I}_{13}$

| Vector | Sector | Switching States | |
|---|---|---|---|
| $\vec{I}_{13}$ | 1 | [14 16] | [16 14] |
| | 6 | [16 36] | [36 16] |

Table II-2 Effect of switching states of Small vector $\vec{I}_{13}$ on DC currents (sector 1)

| Switching State | Load Voltage | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [14 16] or [16 14] | $v_{AO}=v_{BO}$ | X | X | X | X |
| [14 16] | $v_{AO}>v_{BO}$ | X | ↓ | X | ↑ |
| | $v_{AO}<v_{BO}$ | X | ↑ | X | ↓ |
| [16 14] | $v_{AO}>v_{BO}$ | X | ↑ | X | ↓ |
| | $v_{AO}<v_{BO}$ | X | ↓ | X | ↑ |

Table II-3 Selected switching state of Small vector $\vec{I}_{13}$ (sector 1)

| Voltage Comparison | Current Comparison | Selected Switching State |
|---|---|---|
| $v_{BO}>v_{AO}$ | $i_{d4}>i_{d2}$ | **[14 16]** |
| $v_{AO}>v_{BO}$ | $i_{d2}>i_{d4}$ | |
| $v_{BO}>v_{AO}$ | $i_{d2}>i_{d4}$ | **[16 14]** |
| $v_{AO}>v_{BO}$ | $i_{d4}>i_{d2}$ | |

Table II-4 Effect of switching states of Small vector $\vec{I}_{13}$ on DC currents (sector 6)

| Switching State | Load Voltage | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [16 36] or [36 16] | $v_{AO}=v_{BO}$ | X | X | X | X |
| [16 36] | $v_{AO}>v_{BO}$ | ↓ | X | ↑ | X |
| | $v_{AO}<v_{BO}$ | ↑ | X | ↓ | X |
| [36 16] | $v_{AO}>v_{BO}$ | ↑ | X | ↓ | X |
| | $v_{AO}<v_{BO}$ | ↓ | X | ↑ | X |

Table II-5 Selected switching state of Small vector $\vec{I}_{13}$ (sector 6)

| Voltage Comparison | Current Comparison | Selected Switching State |
|---|---|---|
| $v_{AO}>v_{BO}$ | $i_{d1}>i_{d3}$ | **[16 36]** |
| $v_{BO}>v_{AO}$ | $i_{d3}>i_{d1}$ | |
| $v_{AO}>v_{BO}$ | $i_{d3}>i_{d1}$ | **[36 16]** |
| $v_{BO}>v_{AO}$ | $i_{d1}>i_{d3}$ | |

Table II-6 Employed switching states of Small vector $\vec{I}_{14}$

| Vector | Sector | Switching States | |
|---|---|---|---|
| $\vec{I}_{14}$ | 1 | [14 12] | [12 14] |
| | 2 | [12 52] | [52 12] |

Table II-7 Effect of switching states of Small vector $\vec{I}_{14}$ on DC currents (sector 1)

| Switching State | Load Voltage | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| [14 12] or [12 14] | $v_{AO}=v_{CO}$ | X | X | X | X |
| [14 12] | $v_{AO}>v_{CO}$ | X | ↓ | X | ↑ |
| | $v_{AO}<v_{CO}$ | X | ↑ | X | ↓ |
| [12 14] | $v_{AO}>v_{CO}$ | X | ↑ | X | ↓ |
| | $v_{AO}<v_{CO}$ | X | ↓ | X | ↑ |

Table II-8 Selected switching state of Small vector $\vec{I}_{14}$ (sector 1)

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{CO}>v_{AO}$ | $i_{d4}>i_{d2}$ | **[14 12]** |
| $v_{AO}>v_{CO}$ | $i_{d2}>i_{d4}$ | |
| $v_{CO}>v_{AO}$ | $i_{d2}>i_{d4}$ | **[12 14]** |
| $v_{AO}>v_{CO}$ | $i_{d4}>i_{d2}$ | |

Table II-9 Effect of switching states of Small vector $\vec{I}_{14}$ on DC currents (sector 2)

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [12 52] or [52 12] | $v_{AO}=v_{CO}$ | X | X | X | X |
| [12 52] | $v_{AO}>v_{CO}$ | ↓ | X | ↑ | X |
| | $v_{AO}<v_{CO}$ | ↑ | X | ↓ | X |
| [52 12] | $v_{AO}>v_{CO}$ | ↑ | X | ↓ | X |
| | $v_{AO}<v_{CO}$ | ↓ | X | ↑ | X |

Table II-10 Selected switching state of Small vector $\vec{I}_{14}$ (sector 2)

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{AO}>v_{CO}$ | $i_{d1}>i_{d3}$ | **[12 52]** |
| $v_{CO}>v_{AO}$ | $i_{d3}>i_{d1}$ | |
| $v_{AO}>v_{CO}$ | $i_{d3}>i_{d1}$ | **[52 12]** |
| $v_{CO}>v_{AO}$ | $i_{d1}>i_{d3}$ | |

Table II-11 Employed switching states of Small vector $\vec{I}_{15}$

| Vector | Sector | Switching States | |
|---|---|---|---|
| $\vec{I}_{15}$ | 3 | [36 32] | [32 36] |
| | 2 | [52 32] | [32 52] |

Table II-12 Effect of switching states of Small vector $\vec{I}_{15}$ on DC currents (sector 3)

| Switching State | Load Voltage | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [36 32] or [32 36] | $v_{BO}=v_{CO}$ | X | X | X | X |
| [36 32] | $v_{BO}>v_{CO}$ | X | ↓ | X | ↑ |
| | $v_{BO}<v_{CO}$ | X | ↑ | X | ↓ |
| [32 36] | $v_{BO}>v_{CO}$ | X | ↑ | X | ↓ |
| | $v_{BO}<v_{CO}$ | X | ↓ | X | ↑ |

Table II-13 Selected switching state of Small vector $\vec{I}_{15}$ (sector 3)

| Voltage Comparison | Current Comparison | Selected Switching State |
|---|---|---|
| $v_{CO}>v_{BO}$ | $i_{d4}>i_{d2}$ | **[36 32]** |
| $v_{BO}>v_{CO}$ | $i_{d2}>i_{d4}$ | |
| $v_{CO}>v_{BO}$ | $i_{d2}>i_{d4}$ | **[32 36]** |
| $v_{BO}>v_{CO}$ | $i_{d4}>i_{d2}$ | |

Table II-14 Effect of switching states of Small vector $\vec{I}_{15}$ on DC currents (sector 2)

| Switching State | Load Voltage | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [32 52] or [52 32] | $v_{BO}=v_{CO}$ | X | X | X | X |
| [32 52] | $v_{BO}>v_{CO}$ | ↓ | X | ↑ | X |
| | $v_{BO}<v_{CO}$ | ↑ | X | ↓ | X |
| [52 32] | $v_{BO}>v_{CO}$ | ↑ | X | ↓ | X |
| | $v_{BO}<v_{CO}$ | ↓ | X | ↑ | X |

Table II-15 Selected switching state of Small vector $\vec{I}_{15}$ (sector 2)

| Voltage Comparison | Current Comparison | Selected Switching State |
|---|---|---|
| $v_{BO}>v_{CO}$ | $i_{d1}>i_{d3}$ | **[32 52]** |
| $v_{CO}>v_{BO}$ | $i_{d3}>i_{d1}$ | |
| $v_{BO}>v_{CO}$ | $i_{d3}>i_{d1}$ | **[52 32]** |
| $v_{CO}>v_{BO}$ | $i_{d1}>i_{d3}$ | |

Table II-16 Employed switching states of Small vector $\vec{I}_{16}$

| Vector | Sector | Switching States | |
|---|---|---|---|
| $\vec{I}_{16}$ | 3 | [36 34] | [34 36] |
| | 4 | [34 14] | [14 34] |

Table II-17 Effect of switching states of Small vector $\vec{I}_{16}$ on DC currents (sector 3)

| Switching State | Load Voltage | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [36 34] or [34 36] | $v_{BO}=v_{AO}$ | X | X | X | X |
| [36 34] | $v_{BO}>v_{AO}$ | X | ↓ | X | ↑ |
| | $v_{BO}<v_{AO}$ | X | ↑ | X | ↓ |
| [34 36] | $v_{BO}>v_{AO}$ | X | ↑ | X | ↓ |
| | $v_{BO}<v_{AO}$ | X | ↓ | X | ↑ |

Table II-18 Selected switching state of Small vector $\vec{I}_{16}$ (sector 3)

| Voltage Comparison | Current Comparison | Selected Switching State |
|---|---|---|
| $v_{AO}>v_{BO}$ | $i_{d4}>i_{d2}$ | **[36 34]** |
| $v_{BO}>v_{AO}$ | $i_{d2}>i_{d4}$ | |
| $v_{AO}>v_{BO}$ | $i_{d2}>i_{d4}$ | **[34 36]** |
| $v_{BO}>v_{AO}$ | $i_{d4}>i_{d2}$ | |

Table II-19 Effect of switching states of Small vector $\vec{I}_{16}$ on DC currents (sector 4)

| Switching State | Load Voltage | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| [34 14] or [14 34] | $v_{BO}=v_{AO}$ | X | X | X | X |
| [34 14] | $v_{BO}>v_{AO}$ | ↓ | X | ↑ | X |
| | $v_{BO}<v_{AO}$ | ↑ | X | ↓ | X |
| [14 34] | $v_{BO}>v_{AO}$ | ↑ | X | ↓ | X |
| | $v_{BO}<v_{AO}$ | ↓ | X | ↑ | X |

Table II-20 Selected switching state of Small vector $\vec{I}_{16}$ (sector 4)

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{BO}>v_{AO}$ | $i_{d1}>i_{d3}$ | **[34 14]** |
| $v_{AO}>v_{BO}$ | $i_{d3}>i_{d1}$ | |
| $v_{BO}>v_{AO}$ | $i_{d3}>i_{d1}$ | **[14 34]** |
| $v_{AO}>v_{BO}$ | $i_{d1}>i_{d3}$ | |

Table II-21 Employed switching states of Small vector $\vec{I}_{17}$

| **Vector** | **Sector** | **Switching States** | |
|---|---|---|---|
| $\vec{I}_{17}$ | 4 | [52 54] | [54 52] |
| | 5 | [54 14] | [14 54] |

Table II-22 Effect of switching states of Small vector $\vec{I}_{17}$ on DC currents (sector 4)

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [52 54] or [54 52] | $v_{CO}=v_{AO}$ | X | X | X | X |
| [52 54] | $v_{CO}>v_{AO}$ | X | ↓ | X | ↑ |
| | $v_{CO}<v_{AO}$ | X | ↑ | X | ↓ |
| [54 54] | $v_{CO}>v_{AO}$ | X | ↑ | X | ↓ |
| | $v_{CO}<v_{AO}$ | X | ↓ | X | ↑ |

Table II-23 Selected switching state of Small vector $\vec{I}_{17}$ (sector 4)

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|

| | | |
|---|---|---|
| $v_{AO}>v_{CO}$ | $i_{d4}>i_{d2}$ | **[52 54]** |
| $v_{CO}>v_{AO}$ | $i_{d2}>i_{d4}$ | |
| $v_{AO}>v_{CO}$ | $i_{d2}>i_{d4}$ | **[54 52]** |
| $v_{CO}>v_{AO}$ | $i_{d4}>i_{d2}$ | |

Table II-24 Effect of switching states of Small vector $\vec{I}_{17}$ on DC currents (sector 5)

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [54 14] or [14 54] | $v_{CO}=v_{AO}$ | X | X | X | X |
| [54 14] | $v_{CO}>v_{AO}$ | ↓ | X | ↑ | X |
| | $v_{CO}<v_{AO}$ | ↑ | X | ↓ | X |
| [14 54] | $v_{CO}>v_{AO}$ | ↑ | X | ↓ | X |
| | $v_{CO}<v_{AO}$ | ↓ | X | ↑ | X |

Table II-25 Selected switching state of Small vector $\vec{I}_{17}$ (sector 5)

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{CO}>v_{AO}$ | $i_{d1}>i_{d3}$ | **[54 14]** |
| $v_{AO}>v_{CO}$ | $i_{d3}>i_{d1}$ | |
| $v_{CO}>v_{AO}$ | $i_{d3}>i_{d1}$ | **[14 54]** |
| $v_{AO}>v_{CO}$ | $i_{d1}>i_{d3}$ | |

Table II-26 Employed switching states of Small vector $\vec{I}_{18}$

| **Vector** | **Sector** | **Switching States** | |
|---|---|---|---|
| $\vec{I}_{18}$ | 6 | [52 56] | [56 52] |
| | 5 | [56 36] | [36 56] |

Table II-27 Effect of switching states of Small vector $\vec{I}_{18}$ on DC currents (sector 6)

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [52 56] or [56 52] | $v_{CO}=v_{BO}$ | X | X | X | X |

| | | | | | |
|---|---|---|---|---|---|
| [52 56] | $v_{CO}>v_{BO}$ | X | ↓ | X | ↑ |
| | $v_{CO}<v_{BO}$ | X | ↑ | X | ↓ |
| [56 52] | $v_{CO}>v_{BO}$ | X | ↑ | X | ↓ |
| | $v_{CO}<v_{BO}$ | X | ↓ | X | ↑ |

Table II-28 Selected switching state of Small vector $\vec{I}_{18}$ (sector 6)

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{BO}>v_{CO}$ | $i_{d4}>i_{d2}$ | **[52 56]** |
| $v_{CO}>v_{BO}$ | $i_{d2}>i_{d4}$ | |
| $v_{BO}>v_{CO}$ | $i_{d2}>i_{d4}$ | **[56 52]** |
| $v_{CO}>v_{BO}$ | $i_{d4}>i_{d2}$ | |

Table II-29 Effect of switching states of Small vector $\vec{I}_{18}$ on DC currents (sector 5)

| **Switching State** | **Load Voltage** | $i_{d1}$ | $i_{d2}$ | $i_{d3}$ | $i_{d4}$ |
|---|---|---|---|---|---|
| [56 36] or [36 56] | $v_{CO}=v_{BO}$ | X | X | X | X |
| [56 36] | $v_{CO}>v_{BO}$ | ↓ | X | ↑ | X |
| | $v_{CO}<v_{BO}$ | ↑ | X | ↓ | X |
| [36 56] | $v_{CO}>v_{BO}$ | ↑ | X | ↓ | X |
| | $v_{CO}<v_{BO}$ | ↓ | X | ↑ | X |

Table II-30 Selected switching state of Small vector $\vec{I}_{18}$ (sector 5)

| **Voltage Comparison** | **Current Comparison** | **Selected Switching State** |
|---|---|---|
| $v_{CO}>v_{BO}$ | $i_{d1}>i_{d3}$ | **[56 36]** |
| $v_{BO}>v_{CO}$ | $i_{d3}>i_{d1}$ | |
| $v_{CO}>v_{BO}$ | $i_{d3}>i_{d1}$ | **[36 56]** |
| $v_{BO}>v_{CO}$ | $i_{d1}>i_{d3}$ | |

# Appendix III
# Switching Sequence Look-Up Tables

The detailed switching sequence for each triangular area is presented in this section.

Table III-1 Sector 1, Region 3

| $i_{d2}>i_{d4}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_1$ | $\vec{I}_7$ | $\vec{I}_{13}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [16 16] | [16 12] | [14 16] |
| 0 | 0 | 1 | [16 16] | [16 12] | [16 14] |
| 0 | 1 | 0 | [16 16] | [12 16] | [14 16] |
| 0 | 1 | 1 | [16 16] | [12 16] | [16 14] |
| 1 | 0 | 0 | [16 16] | [12 16] | [16 14] |
| 1 | 0 | 1 | [16 16] | [12 16] | [14 16] |
| 1 | 1 | 0 | [16 16] | [16 12] | [16 14] |
| 1 | 1 | 1 | [16 16] | [16 12] | [14 16] |

Table III-2 Sector 1, Region 2

| $i_{d2}>i_{d4}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{13}$ | $\vec{I}_7$ | $\vec{I}_{14}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | [14 16] | [16 12] | [12 14] |
| 0 | 0 | 0 | 1 | [14 16] | [16 12] | [14 12] |
| 0 | 0 | 1 | 0 | [16 14] | [16 12] | [12 14] |
| 0 | 0 | 1 | 1 | [16 14] | [16 12] | [14 12] |
| 0 | 1 | 0 | 0 | [14 16] | [12 16] | [12 14] |
| 0 | 1 | 0 | 1 | [14 16] | [12 16] | [14 12] |
| 0 | 1 | 1 | 0 | [16 14] | [12 16] | [12 14] |
| 0 | 1 | 1 | 1 | [16 14] | [12 16] | [14 12] |
| 1 | 0 | 0 | 0 | [16 14] | [12 16] | [14 12] |
| 1 | 0 | 0 | 1 | [16 14] | [12 16] | [12 14] |
| 1 | 0 | 1 | 0 | [14 16] | [12 16] | [14 12] |
| 1 | 0 | 1 | 1 | [14 16] | [12 16] | [12 14] |
| 1 | 1 | 0 | 0 | [16 14] | [16 12] | [14 12] |
| 1 | 1 | 0 | 1 | [16 14] | [16 12] | [12 14] |
| 1 | 1 | 1 | 0 | [14 16] | [16 12] | [14 12] |
| 1 | 1 | 1 | 1 | [14 16] | [16 12] | [12 14] |

Table III-3 Sector 1, Region 4

| $i_{d2}>i_{d4}$ | $v_{CO}>v_{BO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{14}$ | $\vec{I}_{7}$ | $\vec{I}_{2}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [12 14] | [16 12] | [12 12] |
| 0 | 0 | 1 | [14 12] | [16 12] | [12 12] |
| 0 | 1 | 0 | [12 14] | [12 16] | [12 12] |
| 0 | 1 | 1 | [14 12] | [12 16] | [12 12] |
| 1 | 0 | 0 | [14 12] | [12 16] | [12 12] |
| 1 | 0 | 1 | [12 14] | [12 16] | [12 12] |
| 1 | 1 | 0 | [14 12] | [16 12] | [12 12] |
| 1 | 1 | 1 | [12 14] | [16 12] | [12 12] |

Table III-4 Sector 1, Region 1, Down

| $i_{d2}>i_{d4}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_{19}$ | $\vec{I}_{13}$ | $\vec{I}_{7}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [14 14] | [14 16] | [16 12] |
| 0 | 0 | 1 | [14 14] | [16 14] | [16 12] |
| 0 | 1 | 0 | [14 14] | [14 16] | [12 16] |
| 0 | 1 | 1 | [14 14] | [16 14] | [12 16] |
| 1 | 0 | 0 | [14 14] | [16 14] | [12 16] |
| 1 | 0 | 1 | [14 14] | [14 16] | [12 16] |
| 1 | 1 | 0 | [14 14] | [16 14] | [16 12] |
| 1 | 1 | 1 | [14 14] | [14 16] | [16 12] |

Table III-5 Sector 1, Region 1, Up

| $i_{d2}>i_{d4}$ | $v_{CO}>v_{BO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{7}$ | $\vec{I}_{14}$ | $\vec{I}_{19}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [16 12] | [12 14] | [12 54] |
| 0 | 0 | 1 | [16 12] | [14 12] | [54 12] |
| 0 | 1 | 0 | [12 16] | [12 14] | [12 54] |
| 0 | 1 | 1 | [12 16] | [14 12] | [54 12] |
| 1 | 0 | 0 | [12 16] | [14 12] | [54 12] |
| 1 | 0 | 1 | [12 16] | [12 14] | [12 54] |
| 1 | 1 | 0 | [16 12] | [14 12] | [54 12] |
| 1 | 1 | 1 | [16 12] | [12 14] | [12 54] |

Table III-6 Sector 2, Region 3

| $i_{d1}>i_{d3}$ | $v_{BO}>v_{AO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{2}$ | $\vec{I}_{8}$ | $\vec{I}_{14}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [12 12] | [32 12] | [12 52] |
| 0 | 0 | 1 | [12 12] | [32 12] | [52 12] |
| 0 | 1 | 0 | [12 12] | [12 32] | [12 52] |
| 0 | 1 | 1 | [12 12] | [12 32] | [52 12] |
| 1 | 0 | 0 | [12 12] | [12 32] | [52 12] |

| | | | | | |
|---|---|---|---|---|---|
| 1 | 0 | 1 | [12 12] | [12 32] | [12 52] |
| 1 | 1 | 0 | [12 12] | [32 12] | [52 12] |
| 1 | 1 | 1 | [12 12] | [32 12] | [12 52] |

Table III-7 Sector 2, Region 2

| $i_{d1}>i_{d3}$ | $v_{BO}>v_{AO}$ | $v_{AO}>v_{CO}$ | $v_{CO}>v_{BO}$ | $\vec{I}_{14}$ | $\vec{I}_{8}$ | $\vec{I}_{15}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | [12 52] | [32 12] | [52 32] |
| 0 | 0 | 0 | 1 | [12 52] | [32 12] | [32 52] |
| 0 | 0 | 1 | 0 | [52 12] | [32 12] | [52 32] |
| 0 | 0 | 1 | 1 | [52 12] | [32 12] | [32 52] |
| 0 | 1 | 0 | 0 | [12 52] | [12 32] | [52 32] |
| 0 | 1 | 0 | 1 | [12 52] | [12 32] | [32 52] |
| 0 | 1 | 1 | 0 | [52 12] | [12 32] | [52 32] |
| 0 | 1 | 1 | 1 | [52 12] | [12 32] | [32 52] |
| 1 | 0 | 0 | 0 | [52 12] | [12 32] | [32 52] |
| 1 | 0 | 0 | 1 | [52 12] | [12 32] | [52 32] |
| 1 | 0 | 1 | 0 | [12 52] | [12 32] | [32 52] |
| 1 | 0 | 1 | 1 | [12 52] | [12 32] | [52 32] |
| 1 | 1 | 0 | 0 | [52 12] | [32 12] | [32 52] |
| 1 | 1 | 0 | 1 | [52 12] | [32 12] | [52 32] |
| 1 | 1 | 1 | 0 | [12 52] | [32 12] | [32 52] |
| 1 | 1 | 1 | 1 | [12 52] | [32 12] | [52 32] |

Table III-8 Sector 2, Region 4

| $i_{d1}>i_{d3}$ | $v_{BO}>v_{AO}$ | $v_{CO}>v_{BO}$ | $\vec{I}_{15}$ | $\vec{I}_{8}$ | $\vec{I}_{3}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [52 32] | [32 12] | [32 32] |
| 0 | 0 | 1 | [32 52] | [32 12] | [32 32] |
| 0 | 1 | 0 | [52 32] | [12 32] | [32 32] |
| 0 | 1 | 1 | [32 52] | [12 32] | [32 32] |
| 1 | 0 | 0 | [32 52] | [12 32] | [32 32] |
| 1 | 0 | 1 | [52 32] | [12 32] | [32 32] |
| 1 | 1 | 0 | [32 52] | [32 12] | [32 32] |
| 1 | 1 | 1 | [52 32] | [32 12] | [32 32] |

Table III-9 Sector 2, Region 1, Down

| $i_{d1}>i_{d3}$ | $v_{BO}>v_{AO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{19}$ | $\vec{I}_{14}$ | $\vec{I}_{8}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [52 52] | [12 52] | [32 12] |
| 0 | 0 | 1 | [52 52] | [52 12] | [32 12] |
| 0 | 1 | 0 | [52 52] | [12 52] | [12 32] |
| 0 | 1 | 1 | [52 52] | [52 12] | [12 32] |

| | | | | | |
|---|---|---|---|---|---|
| 1 | 0 | 0 | [52 52] | [52 12] | [12 32] |
| 1 | 0 | 1 | [52 52] | [12 52] | [12 32] |
| 1 | 1 | 0 | [52 52] | [52 12] | [32 12] |
| 1 | 1 | 1 | [52 52] | [12 52] | [32 12] |

Table III-10 Sector 2, Region 1, Up

| $i_{d1}>i_{d3}$ | $v_{BO}>v_{AO}$ | $v_{CO}>v_{BO}$ | $\vec{I}_8$ | $\vec{I}_{15}$ | $\vec{I}_{19}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [32 12] | [52 32] | [52 36] |
| 0 | 0 | 1 | [32 12] | [32 52] | [36 52] |
| 0 | 1 | 0 | [12 32] | [52 32] | [52 36] |
| 0 | 1 | 1 | [12 32] | [32 52] | [36 52] |
| 1 | 0 | 0 | [12 32] | [32 52] | [36 52] |
| 1 | 0 | 1 | [12 32] | [52 32] | [52 36] |
| 1 | 1 | 0 | [32 12] | [32 52] | [36 52] |
| 1 | 1 | 1 | [32 12] | [52 32] | [52 36] |

Table III-11 Sector 3, Region 3

| $i_{d2}>i_{d4}$ | $v_{AO}>v_{CO}$ | $v_{CO}>v_{BO}$ | $\vec{I}_3$ | $\vec{I}_9$ | $\vec{I}_{15}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [32 32] | [32 34] | [36 32] |
| 0 | 0 | 1 | [32 32] | [32 34] | [32 36] |
| 0 | 1 | 0 | [32 32] | [34 32] | [36 32] |
| 0 | 1 | 1 | [32 32] | [34 32] | [32 36] |
| 1 | 0 | 0 | [32 32] | [34 32] | [32 36] |
| 1 | 0 | 1 | [32 32] | [34 32] | [36 32] |
| 1 | 1 | 0 | [32 32] | [32 34] | [32 36] |
| 1 | 1 | 1 | [32 32] | [32 34] | [36 32] |

Table III-12 Sector 3, Region 2

| $i_{d2}>i_{d4}$ | $v_{AO}>v_{CO}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_{15}$ | $\vec{I}_9$ | $\vec{I}_{16}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | [36 32] | [32 34] | [34 36] |
| 0 | 0 | 0 | 1 | [36 32] | [32 34] | [36 34] |
| 0 | 0 | 1 | 0 | [32 36] | [32 34] | [34 36] |
| 0 | 0 | 1 | 1 | [32 36] | [32 34] | [36 34] |
| 0 | 1 | 0 | 0 | [36 32] | [34 32] | [34 36] |
| 0 | 1 | 0 | 1 | [36 32] | [34 32] | [36 34] |
| 0 | 1 | 1 | 0 | [32 36] | [34 32] | [34 36] |
| 0 | 1 | 1 | 1 | [32 36] | [34 32] | [36 34] |
| 1 | 0 | 0 | 0 | [32 36] | [34 32] | [36 34] |
| 1 | 0 | 0 | 1 | [32 36] | [34 32] | [34 36] |
| 1 | 0 | 1 | 0 | [36 32] | [34 32] | [36 34] |

| | | | | | | |
|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | [36 32] | [34 32] | [34 36] |
| 1 | 1 | 0 | 0 | [32 36] | [32 34] | [36 34] |
| 1 | 1 | 0 | 1 | [32 36] | [32 34] | [34 36] |
| 1 | 1 | 1 | 0 | [36 32] | [32 34] | [36 34] |
| 1 | 1 | 1 | 1 | [36 32] | [32 34] | [34 36] |

Table III-13 Sector 3, Region 4

| $i_{d2}>i_{d4}$ | $v_{AO}>v_{CO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_{16}$ | $\vec{I}_{9}$ | $\vec{I}_{4}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [34 36] | [32 34] | [34 34] |
| 0 | 0 | 1 | [36 34] | [32 34] | [34 34] |
| 0 | 1 | 0 | [34 36] | [34 32] | [34 34] |
| 0 | 1 | 1 | [36 34] | [34 32] | [34 34] |
| 1 | 0 | 0 | [36 34] | [34 32] | [34 34] |
| 1 | 0 | 1 | [34 36] | [34 32] | [34 34] |
| 1 | 1 | 0 | [36 34] | [32 34] | [34 34] |
| 1 | 1 | 1 | [34 36] | [32 34] | [34 34] |

Table III-14 Sector 3, Region 1, Down

| $i_{d2}>i_{d4}$ | $v_{AO}>v_{CO}$ | $v_{CO}>v_{BO}$ | $\vec{I}_{19}$ | $\vec{I}_{15}$ | $\vec{I}_{9}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [36 36] | [36 32] | [32 34] |
| 0 | 0 | 1 | [36 36] | [32 36] | [32 34] |
| 0 | 1 | 0 | [36 36] | [36 32] | [34 32] |
| 0 | 1 | 1 | [36 36] | [32 36] | [34 32] |
| 1 | 0 | 0 | [36 36] | [32 36] | [34 32] |
| 1 | 0 | 1 | [36 36] | [36 32] | [34 32] |
| 1 | 1 | 0 | [36 36] | [32 36] | [32 34] |
| 1 | 1 | 1 | [36 36] | [36 32] | [32 34] |

Table III-15 Sector 3, Region 1, Up

| $i_{d2}>i_{d4}$ | $v_{AO}>v_{CO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_{9}$ | $\vec{I}_{16}$ | $\vec{I}_{19}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [32 34] | [34 36] | [34 16] |
| 0 | 0 | 1 | [32 34] | [36 34] | [16 34] |
| 0 | 1 | 0 | [34 32] | [34 36] | [34 16] |
| 0 | 1 | 1 | [34 32] | [36 34] | [16 34] |
| 1 | 0 | 0 | [34 32] | [36 34] | [16 34] |
| 1 | 0 | 1 | [34 32] | [34 36] | [34 16] |
| 1 | 1 | 0 | [32 34] | [36 34] | [16 34] |
| 1 | 1 | 1 | [32 34] | [34 36] | [34 16] |

Table III-16 Sector 4, Region 3

| $i_{d1}>i_{d3}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_4$ | $\vec{I}_{10}$ | $\vec{I}_{16}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [34 34] | [54 34] | [34 14] |
| 0 | 0 | 1 | [34 34] | [54 34] | [14 34] |
| 0 | 1 | 0 | [34 34] | [34 54] | [34 14] |
| 0 | 1 | 1 | [34 34] | [34 54] | [14 34] |
| 1 | 0 | 0 | [34 34] | [34 54] | [14 34] |
| 1 | 0 | 1 | [34 34] | [34 54] | [34 14] |
| 1 | 1 | 0 | [34 34] | [54 34] | [14 34] |
| 1 | 1 | 1 | [34 34] | [54 34] | [34 14] |

Table III-17 Sector 4, Region 2

| $i_{d1}>i_{d3}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{16}$ | $\vec{I}_{10}$ | $\vec{I}_{17}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | [34 14] | [54 34] | [14 54] |
| 0 | 0 | 0 | 1 | [34 14] | [54 34] | [54 14] |
| 0 | 0 | 1 | 0 | [14 34] | [54 34] | [14 54] |
| 0 | 0 | 1 | 1 | [14 34] | [54 34] | [54 14] |
| 0 | 1 | 0 | 0 | [34 14] | [34 54] | [14 54] |
| 0 | 1 | 0 | 1 | [34 14] | [34 54] | [54 14] |
| 0 | 1 | 1 | 0 | [14 34] | [34 54] | [14 54] |
| 0 | 1 | 1 | 1 | [14 34] | [34 54] | [54 14] |
| 1 | 0 | 0 | 0 | [14 34] | [34 54] | [54 14] |
| 1 | 0 | 0 | 1 | [14 34] | [34 54] | [14 54] |
| 1 | 0 | 1 | 0 | [34 14] | [34 54] | [54 14] |
| 1 | 0 | 1 | 1 | [34 14] | [34 54] | [14 54] |
| 1 | 1 | 0 | 0 | [14 34] | [54 34] | [54 14] |
| 1 | 1 | 0 | 1 | [14 34] | [54 34] | [14 54] |
| 1 | 1 | 1 | 0 | [34 14] | [54 34] | [54 14] |
| 1 | 1 | 1 | 1 | [34 14] | [54 34] | [14 54] |

Table III-18 Sector 4, Region 2

| $i_{d1}>i_{d3}$ | $v_{CO}>v_{BO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{17}$ | $\vec{I}_{10}$ | $\vec{I}_5$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [14 54] | [54 34] | [54 54] |
| 0 | 0 | 1 | [54 14] | [54 34] | [54 54] |
| 0 | 1 | 0 | [14 54] | [34 54] | [54 54] |
| 0 | 1 | 1 | [54 14] | [34 54] | [54 54] |
| 1 | 0 | 0 | [54 14] | [34 54] | [54 54] |
| 1 | 0 | 1 | [14 54] | [34 54] | [54 54] |
| 1 | 1 | 0 | [54 14] | [54 34] | [54 54] |
| 1 | 1 | 1 | [14 54] | [54 34] | [54 54] |

Table III-19 Sector 4, Region 1, Down

| $i_{d1}>i_{d3}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_{19}$ | $\vec{I}_{16}$ | $\vec{I}_{10}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [14 14] | [34 14] | [54 34] |
| 0 | 0 | 1 | [14 14] | [14 34] | [54 34] |
| 0 | 1 | 0 | [14 14] | [34 14] | [34 54] |
| 0 | 1 | 1 | [14 14] | [14 34] | [34 54] |
| 1 | 0 | 0 | [14 14] | [14 34] | [34 54] |
| 1 | 0 | 1 | [14 14] | [34 14] | [34 54] |
| 1 | 1 | 0 | [14 14] | [14 34] | [54 34] |
| 1 | 1 | 1 | [14 14] | [34 14] | [54 34] |

Table III-20 Sector 4, Region 1, Up

| $i_{d1}>i_{d3}$ | $v_{CO}>v_{BO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{10}$ | $\vec{I}_{17}$ | $\vec{I}_{19}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [54 34] | [14 54] | [12 54] |
| 0 | 0 | 1 | [54 34] | [54 14] | [54 12] |
| 0 | 1 | 0 | [34 54] | [14 54] | [12 54] |
| 0 | 1 | 1 | [34 54] | [54 14] | [54 12] |
| 1 | 0 | 0 | [34 54] | [54 14] | [54 12] |
| 1 | 0 | 1 | [34 54] | [14 54] | [12 54] |
| 1 | 1 | 0 | [54 34] | [54 14] | [54 12] |
| 1 | 1 | 1 | [54 34] | [14 54] | [12 54] |

Table III-21 Sector 5, Region 3

| $i_{d2}>i_{d4}$ | $v_{BO}>v_{AO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{5}$ | $\vec{I}_{11}$ | $\vec{I}_{17}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [54 54] | [54 56] | [52 54] |
| 0 | 0 | 1 | [54 54] | [54 56] | [54 52] |
| 0 | 1 | 0 | [54 54] | [56 54] | [52 54] |
| 0 | 1 | 1 | [54 54] | [56 54] | [54 52] |
| 1 | 0 | 0 | [54 54] | [56 54] | [54 52] |
| 1 | 0 | 1 | [54 54] | [56 54] | [52 54] |
| 1 | 1 | 0 | [54 54] | [54 56] | [54 52] |
| 1 | 1 | 1 | [54 54] | [54 56] | [52 54] |

Table III-22 Sector 5, Region 2

| $i_{d2}>i_{d4}$ | $v_{BO}>v_{AO}$ | $v_{AO}>v_{CO}$ | $v_{CO}>v_{BO}$ | $\vec{I}_{17}$ | $\vec{I}_{11}$ | $\vec{I}_{18}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | [52 54] | [54 56] | [56 52] |
| 0 | 0 | 0 | 1 | [52 54] | [54 56] | [52 56] |
| 0 | 0 | 1 | 0 | [54 52] | [54 56] | [56 52] |
| 0 | 0 | 1 | 1 | [54 52] | [54 56] | [52 56] |
| 0 | 1 | 0 | 0 | [52 54] | [56 54] | [56 52] |

| | | | | | | |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | [52 54] | [56 54] | [52 56] |
| 0 | 1 | 1 | 0 | [54 52] | [56 54] | [56 52] |
| 0 | 1 | 1 | 1 | [54 52] | [56 54] | [52 56] |
| 1 | 0 | 0 | 0 | [54 52] | [56 54] | [52 56] |
| 1 | 0 | 0 | 1 | [54 52] | [56 54] | [56 52] |
| 1 | 0 | 1 | 0 | [52 54] | [56 54] | [52 56] |
| 1 | 0 | 1 | 1 | [52 54] | [56 54] | [56 52] |
| 1 | 1 | 0 | 0 | [54 52] | [54 56] | [52 56] |
| 1 | 1 | 0 | 1 | [54 52] | [54 56] | [56 52] |
| 1 | 1 | 1 | 0 | [52 54] | [54 56] | [52 56] |
| 1 | 1 | 1 | 1 | [52 54] | [54 56] | [56 52] |

Table III-23 Sector 5, Region 4

| $i_{d2}>i_{d4}$ | $v_{BO}>v_{AO}$ | $v_{CO}>v_{BO}$ | $\vec{I}_{18}$ | $\vec{I}_{11}$ | $\vec{I}_{6}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [56 52] | [54 56] | [56 56] |
| 0 | 0 | 1 | [52 56] | [54 56] | [56 56] |
| 0 | 1 | 0 | [56 52] | [56 54] | [56 56] |
| 0 | 1 | 1 | [52 56] | [56 54] | [56 56] |
| 1 | 0 | 0 | [52 56] | [56 54] | [56 56] |
| 1 | 0 | 1 | [56 52] | [56 54] | [56 56] |
| 1 | 1 | 0 | [52 56] | [54 56] | [56 56] |
| 1 | 1 | 1 | [56 52] | [54 56] | [56 56] |

Table III-24 Sector 5, Region 1, Down

| $i_{d2}>i_{d4}$ | $v_{BO}>v_{AO}$ | $v_{AO}>v_{CO}$ | $\vec{I}_{19}$ | $\vec{I}_{17}$ | $\vec{I}_{11}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [52 52] | [52 54] | [54 56] |
| 0 | 0 | 1 | [52 52] | [54 52] | [54 56] |
| 0 | 1 | 0 | [52 52] | [52 54] | [56 54] |
| 0 | 1 | 1 | [52 52] | [54 52] | [56 54] |
| 1 | 0 | 0 | [52 52] | [54 52] | [56 54] |
| 1 | 0 | 1 | [52 52] | [52 54] | [56 54] |
| 1 | 1 | 0 | [52 52] | [54 52] | [54 56] |
| 1 | 1 | 1 | [52 52] | [52 54] | [54 56] |

Table III-25 Sector 5, Region 1, Up

| $i_{d2}>i_{d4}$ | $v_{BO}>v_{AO}$ | $v_{CO}>v_{BO}$ | $\vec{I}_{11}$ | $\vec{I}_{18}$ | $\vec{I}_{19}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [54 56] | [56 52] | [56 32] |
| 0 | 0 | 1 | [54 56] | [52 56] | [32 56] |
| 0 | 1 | 0 | [56 54] | [56 52] | [56 32] |
| 0 | 1 | 1 | [56 54] | [52 56] | [32 56] |

| | | | | | |
|---|---|---|---|---|---|
| 1 | 0 | 0 | [56 54] | [52 56] | [32 56] |
| 1 | 0 | 1 | [56 54] | [56 52] | [56 32] |
| 1 | 1 | 0 | [54 56] | [52 56] | [32 56] |
| 1 | 1 | 1 | [54 56] | [56 52] | [56 32] |

Table III-26 Sector 6, Region 3

| $i_{d1}>i_{d3}$ | $v_{AO}>v_{CO}$ | $v_{CO}>v_{BO}$ | $\vec{I}_6$ | $\vec{I}_{12}$ | $\vec{I}_{18}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [56 56] | [16 56] | [36 16] |
| 0 | 0 | 1 | [56 56] | [16 56] | [16 36] |
| 0 | 1 | 0 | [56 56] | [56 16] | [36 16] |
| 0 | 1 | 1 | [56 56] | [56 16] | [16 36] |
| 1 | 0 | 0 | [56 56] | [56 16] | [16 36] |
| 1 | 0 | 1 | [56 56] | [56 16] | [36 16] |
| 1 | 1 | 0 | [56 56] | [16 56] | [16 36] |
| 1 | 1 | 1 | [56 56] | [16 56] | [36 16] |

Table III-27 Sector 6, Region 2

| $i_{d1}>i_{d3}$ | $v_{AO}>v_{CO}$ | $v_{CO}>v_{BO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_{18}$ | $\vec{I}_{12}$ | $\vec{I}_{13}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | [56 36] | [16 56] | [36 16] |
| 0 | 0 | 0 | 1 | [56 36] | [16 56] | [16 36] |
| 0 | 0 | 1 | 0 | [36 56] | [16 56] | [36 16] |
| 0 | 0 | 1 | 1 | [36 56] | [16 56] | [16 36] |
| 0 | 1 | 0 | 0 | [56 36] | [56 16] | [36 16] |
| 0 | 1 | 0 | 1 | [56 36] | [56 16] | [16 36] |
| 0 | 1 | 1 | 0 | [36 56] | [56 16] | [36 16] |
| 0 | 1 | 1 | 1 | [36 56] | [56 16] | [16 36] |
| 1 | 0 | 0 | 0 | [36 56] | [56 16] | [16 36] |
| 1 | 0 | 0 | 1 | [36 56] | [56 16] | [36 16] |
| 1 | 0 | 1 | 0 | [56 36] | [56 16] | [16 36] |
| 1 | 0 | 1 | 1 | [56 36] | [56 16] | [36 16] |
| 1 | 1 | 0 | 0 | [36 56] | [16 56] | [16 36] |
| 1 | 1 | 0 | 1 | [36 56] | [16 56] | [36 16] |
| 1 | 1 | 1 | 0 | [56 36] | [16 56] | [16 36] |
| 1 | 1 | 1 | 1 | [56 36] | [16 56] | [36 16] |

Table III-28 Sector 6, Region 4

| $i_{d1}>i_{d3}$ | $v_{AO}>v_{CO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_{13}$ | $\vec{I}_{12}$ | $\vec{I}_1$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [36 16] | [16 56] | [16 16] |
| 0 | 0 | 1 | [16 36] | [16 56] | [16 16] |
| 0 | 1 | 0 | [36 16] | [56 16] | [16 16] |

| | | | | | |
|---|---|---|---|---|---|
| 0 | 1 | 1 | [16 36] | [56 16] | [16 16] |
| 1 | 0 | 0 | [16 36] | [56 16] | [16 16] |
| 1 | 0 | 1 | [36 16] | [56 16] | [16 16] |
| 1 | 1 | 0 | [16 36] | [16 56] | [16 16] |
| 1 | 1 | 1 | [36 16] | [16 56] | [16 16] |

Table III-29 Sector 6, Region 1, Down

| $i_{d1}>i_{d3}$ | $v_{AO}>v_{CO}$ | $v_{CO}>v_{BO}$ | $\vec{I}_{19}$ | $\vec{I}_{18}$ | $\vec{I}_{12}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [36 36] | [56 36] | [16 56] |
| 0 | 0 | 1 | [36 36] | [36 56] | [16 56] |
| 0 | 1 | 0 | [36 36] | [56 36] | [56 16] |
| 0 | 1 | 1 | [36 36] | [36 56] | [56 16] |
| 1 | 0 | 0 | [36 36] | [36 56] | [56 16] |
| 1 | 0 | 1 | [36 36] | [56 36] | [56 16] |
| 1 | 1 | 0 | [36 36] | [36 56] | [16 56] |
| 1 | 1 | 1 | [36 36] | [56 36] | [16 56] |

Table III-30 Sector 6, Region 1, Up

| $i_{d1}>i_{d3}$ | $v_{AO}>v_{CO}$ | $v_{BO}>v_{AO}$ | $\vec{I}_{12}$ | $\vec{I}_{13}$ | $\vec{I}_{19}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | [16 56] | [36 16] | [34 16] |
| 0 | 0 | 1 | [16 56] | [16 36] | [16 34] |
| 0 | 1 | 0 | [56 16] | [36 16] | [34 16] |
| 0 | 1 | 1 | [56 16] | [16 36] | [16 34] |
| 1 | 0 | 0 | [56 16] | [16 36] | [16 34] |
| 1 | 0 | 1 | [56 16] | [36 16] | [34 16] |
| 1 | 1 | 0 | [16 56] | [16 36] | [16 34] |
| 1 | 1 | 1 | [16 56] | [36 16] | [34 16] |

# References

[1] D. Xu, B. Wu, “Multi-Level Current Source Inverters with Phase-Shifted Trapezoidal PWM,” *Power Electronics Specialists Conference*, 2005.

[2] B. Wu, *High Power Conductors and AC Drives*, A John Willey and Sons, Inc., Publication, 2005.

[3] K. P. Phillips, “Current Source Converter for AC Motor Drives,” *IEEE Transactions on Industry Applications*, vol. IA-8, no. 6, pp. 679-683, Nov./Dec. 1972.

[4] P. Espelage, J. M. Nowak, and L. H. Walker, “Symmetrical GTO Current Source Inverter for Wide Speed Range Control of 2300 to 4160 Volts, 350 to 7000 HP Induction Motors,” *IEEE IAS Annual Meeting on Conf. Rec.*, pp. 302-307, 1988.

[5] B. Wu, J. Pontt, J. Rodriguez, S. Bernet, S. Kouro, “Current-Source Converter and Cycloconverter Topologies for Industrial Medium-Voltage Drives,” *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, July 2008.

[6] D. Xu, N. R. Zargari, B. Wu, J. Wiseman, B. Yuwen, S. Rizzo, “A Medium Voltage AC Drive with Parallel Current Source Inverter for High Power Applications,” *Power Electronics Specialists Conference*, 2005.

[7] J. C. Wiseman and B. Wu, "Active Damping Control of a High-Power PWM Current-Source Rectifier for Line-Current THD Reduction," *IEEE Transactions on Industrial Electronics*, vol. 52, pp. 758-764, 2005.

[8] J. R. Espinoza, L. A. Moran, “Multi-Level Three-Phase Current Source Inverter based AC Drive for High Performance Applications,” *Power Electronics Specialists Conference*, 2005.

[9] Y. Suh, J. K. Steinke, P. K. Steimer. "Efficiancy Comparison of Voltage-Source and Current-Source Drive Systems for Medium-Voltage Applications," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp 2786-2797, July 2008.

[10] Zh. Bai, Zh. Zhang, Y. Zhang, "A Generalized Three-Phase Multilevel Current Source Inverter with Carrier Phase-Shifted SPWM," *Power Electronics Specialists Conference,* 2007.

[11] J. Dai, Y. Lang, B. Wu,D. Xu, N. Zargari, "A Multi-Sampling SVM Scheme for Current Source Converter with Superior Harmonic Performance," *Applied Power Electronics Conference and Exposition,* 2009.

[12] A. Sato, T. Noguchi, "Multi-Level Current-Source PWM Rectifier Based on Direct Power Control," *33rd Annual Conference of the IEEE Industrial Electronics Society*, pp. 1768-1773, 2007.

[13] F. L. M. Antunes, A. C. Braga, I. Barbi, "Application of a Generalized Current Mulitilevel Cell to Current-Source Inverters," *Proceedings of 1995 IEEE IECON 21st International Conference on Industrial Electronics, Control, and Instumetation,* 1995.

[14] Ch. Wen, J. Li, X. Xu, H. Xu, "Research on Circulation of Parallel Three-Phase Converters in MW Wind Power System," *Workshop on Power Electronics and Intelligent Transportation System,* 2008.

[15] T. P. Chen, "Circulating Zero-sequence Current Control of Parallel Three-phase Inverters,"

[16] R. Abe, Y. Nagai, K. Tsuyuki, H. Nishikawa, T. Shimamura, A. Kawaguchi, K. Shimada, "Development of Multiple Space Vector Control for Direct Connected Parallel Current Source Power Converters," *Proceedings of the power conversion conference*, pp. 283-288, 1997.

[17] Y. Iwaji, T. Sukegawa, T. Okuyama, T. Ikimi, M. Shigyo, and M. Tobise, "A New PWM Method to Reduce Beat Phenomenoon in Large-Capacity Inverters with Low Switching Frequency," *IEEE Transactions on Industry Applications*, vol. 35, pp. 606-612, 1999.

[18] H. R. Karshenas, H. A. Kojori, and S. B. Dewan, "Generalized Techniques of Selective Harmonic Elimination and Current Control in Current Source Inverters/Converters," *IEEE Transactions on Power Electronics*, vol. 10, pp. 566-573, 1995.

[19] Y. Xiao, B. Wu, S. C. Rizzo and S. B. Sotudeh, "A Novel Power Factor Control Scheme for High-Power GTO Current-Source Converter," *IEEE Transactions on Industry Applications*, vol. 34, pp.1278-1283, 1998.

[20] J. R. Espinoza, G. Joos, J. I. Guzman, L. A. Moran, and R. P. Burgos, "Selective Harmonic Elimination and Current/Voltage Control in Current/Voltage-Source Topologies: a Unified Approach," *IEEE Transactions on Industrial Electronics*, vol. 48, pp. 71-81, 2001.

[21] B. Wu, S. B. Dewan, and G. R. Slemon, "PWM-CSI Inverter for Induction Motor Drives," *IEEE Transactions on Industry Applications*, vol. 28, pp. 64-71, 1992.

[22] Y. W. Li, B. Wu, D. Xu, N. R. Zargari, "Space Vector Sequence Investigation and Synchronization Methods for Active Front End Rectifiers in High Power Current Source Drives," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, March 2008.

[23] R. Dawley, S.Bhattacharya, "Control of Multi Level Three Phase Dual Current Source Inverters for High Power Industrial Applications," *Industry Applications Society Annual Meeting*, 4-8 Oct., 2009.

[24] R. Palaniappan, J.Vithayath, S. K. Datta, "Principle of a Dual Current Source Converter for AC Motor Drives," *IEEE Transactions on Industry Applications*, vol. IA-15, no. 4, 1979.

[25] Y. Xiong, D. Chen, X. Yang, Ch. Hu, Zh. Zhang, "Analysis and Experimentation of A New Three-Phase Multilevel Current-Source Inverter," *Power Electronics Specialists Conference*, 2004.

[26] M. H. Rashid, *Power Electronics: Circuits, Devices, and Applications*, Third Edition, Ed Prentice Hall

[27] N. Vazquez, H. Lopez, C. Hernandez, E. Vazquez, R. Osorio, and J. Arau "A Different Multilevel Current-Source Inverter," *IEEE Transactions on Industrial Electronics*, pp. 2623-2632, Aug. 2010.

# Glossary of Acronyms and Symbols

| | |
|---|---|
| CSC | Current Source Converter |
| CSI | Current Source Inverter |
| CSR | Current Source Rectifier |
| L-L | Line to Line Voltage |
| PF | Power Factor |
| PWM | Pulse-Width Modulation |
| SHE | Selective Harmonic Elimination |
| SVM | Space Vector Modulation |
| THD | Total Harmonic Distortion |
| TPWM | Trapezoidal Pulse-width Modulation |
| VSC | Voltage Source Converter |
| VSI | Voltage Source Inverter |
| VSR | Voltage Source Rectifier |

To avoid confusions, the variables in this thesis are represented as follows.

- The lower-case letters normally refer to instantaneous quantities and upper-case letters refer to constants, average, or RMS value.
- A variable with a suffix ‘A’ or ‘B’, or ‘C’ represents its corresponding phase A, phase B or phase C component, respectively.

- A variable with a suffix ‘d’ or ‘q’ stands for the corresponding direct-axis or quadrature-axis components in the defined synchronous reference frame, respectively.

The following provides explanations to the variables that are commonly used in this thesis.

**Components**

| | |
|---|---|
| $L_s$ | Power supply-side equivalent line inductance |
| $R_s$ | Power supply-side equivalent line resistance |
| $L_d$, $L_{d1}$, $L_{d2}$, $L_{d3}$, $L_{d4}$ | DC link chokes (inductances) |
| $C_f$ | Filter capacitor |
| $L_L$ | Load-side equivalent inductance |
| $R_L$ | Load-side equivalent resistance |

**Currents**

| | |
|---|---|
| $i_s$ | Power supply-side line current |
| $i_w$ | Chopped switching current |
| $i_{dc}$, $i_{dc1}$, $i_{dc2}$, $i_{dc3}$, $i_{dc4}$ | DC link currents |
| $i_L$ | Load-side current |

**Voltages**

| | |
|---|---|
| $v_s$ | Line to line source voltage |
| $V_{AO}$, $V_{BO}$, $V_{CO}$ | Line to neutral voltages |
| $V_{dc}$ | DC link voltage |

| | |
|---|---|
| $v_{AB}$ | Load-side line to line voltage |

**Switching modulation related**

| | |
|---|---|
| $f_1$ | Fundamental frequency |
| $f_{sw}$ | Device switching frequency |
| $m_a$ | Modulation index |