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Circuits and architectures for high frequency Synthesizer in CMOS

by

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A thesis presented to
Ryerson University

in partial fulfillment of the
requirements for the degree of
Master of Applied Science
in the Program of
Electrical and Computer Engineering

Toronto, Ontario, Canada, 2011
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Circuits and architectures for high frequency Synthesizer in CMOS

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Master of Applied Science, 2011
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Abstract

This thesis proposes a novel architecture for high frequency synthesizer design focusing mainly on the 60GHz frequency range. It consists of a PLL cascaded to an ILO. In order to generate narrow pulses and to relax the multiplication ratio of the ILO, a DLL with a pulse generator is used. Passive delay line stacked on top of LC VCO is used for power efficiency and replica-biasing technique of frequency tracking is used for increasing the locking range of ILO. The synthesizer operates at 60 GHz with a phase noise of -98, -117 and -128 dBc/Hz at 1 MHz, 10 MHz and 40 MHz respectively. The total power consumed by the frequency synthesizer from 1.2 V supply is 57 mW. To have channel selection capability, fractional PLL may be used. A novel fractional PLL architecture is also proposed which de-couples the residual jitter from the PLL bandwidth.

Acknowledgments

First and foremost, I would like to thank Prof. Eddie Law and Ryerson University for funding my graduate studies. I would also like to thank Prof. Xijia Gu for serving as my supervisor after Prof. Eddie Law left Ryerson.

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This thesis would not have been possible without the support and patience of my better half, Masum. He had always been a friend, took care of me, loved me unconditionally and brought a smile to my face every single day.

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List of Abbreviations

BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BW	Bandwidth
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CMU	Clock Multiplication Unit
DLL	Delay Locked Loop
DSM	Delta-Sigma Modulator
IC	Integrated Circuits
ILO	Injection Locked Oscillator
JTF	Jitter Tracking Function
MDLL	Multiplying Delay Locked Loop
MILO	Multiplying Injection Locked Oscillator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	Negative-Channel Metal Oxide Semiconductor
PLL	Phase Locked Loop
PMOS	Positive-Channel Metal Oxide Semiconductor
UI	Unit Interval
VCO	Voltage Controlled Oscillator

1 Introduction

Portable, high performance consumer products are a current focus of microelectronics research. High speed wireless data transfer has an emerging demand in the market for many applications such as mobile broadband, cellular systems, wireless local area network (WLAN), wireless personal area network (WPAN), portable multimedia streaming, vehicular networks and many more.

1.1 Motivation

1.1.1 Why 60 GHz?

In comparison to wire-line data transfer, the performance of wireless standard is poor mainly due to the lack of bandwidth in unlicensed wireless spectrum e.g. Bluetooth and wireless local area networks (WLANs).

Fortunately, there is an abundance of wide spectrum available around the 60 GHz frequency allowing data communications at rates of several gigabits per second. This is the unlicensed millimeter-wave ISM (Industrial, Scientific, and Medical) band. The assigned bandwidths of this 60-GHz ISM band vary under different jurisdictions. The assigned bandwidth in Australia is the narrowest with 3.4 GHz (59.5 - 62.9 GHz). Then it is 7 GHz (57 - 64 GHz) in the U.S., Canada, and Korea. Although it is also 7 GHz (59 - 66 GHz) in Japan, the operating frequency band is different. And in Europe, the bandwidth is the widest with 9 GHz (57 - 66 GHz) bandwidth [1].

In comparison to other wireless standards like IEEE 802.11 a/b/g with bandwidth of around 20 MHz, IEEE 802.11n with 40 MHz and UWB with 520 MHz, this 60 GHz standard enjoys a wide spectrum of 2,500 MHz per channel. The maximum possible data rate for wireless data transmission depends on the channel bandwidth and effective

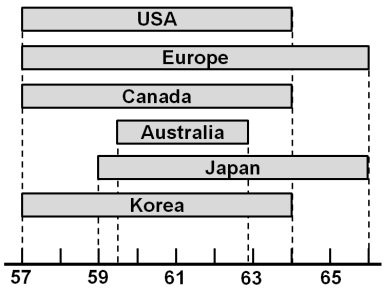


Figure 1.1: Unlicensed millimeter-wave ISM (Industrial, Scientific, and Medical) band spectrum around 60 GHz

power transmission as stated by the Shannon's theorem :

$$C = f_{ch} * log(1 + \frac{P}{N}) \tag{1.1}$$

where C is the channel capacity, f_{ch} is the channel bandwidth, P and N is the power and noise of the transmitted signal. Thus 60 GHz standard is able to achieve much higher data rate compared to IEEE 802.11n and UWB as shown in Table. 1.1 [2].

Table 1.1: Wireless standard specifications

	Effective Channel Bandwidth	**Effective Transmit power**	**Maximum Possible data rate**
UWB	520 MHz	0.4 mW	80 Mbps
802.11n	40 MHz	160 mW	1,100 Mbps
60 GHz	2,500 MHz	8,000 mW	25,000 Mbps

1.1.2 Potential Applications

Despite the advantage of having a wide bandwidth, 60 GHz systems are not suitable for outdoor applications like cellular systems and mobile broadband due to its increased free-space path loss and loss due to atmospheric absorption[3].

On the other hand, because of increased material attenuation and path loss, it provides better security and decreased interference within a single room for 60 GHz indoor

wireless propagation [4]. Another potential application can be the cable replacement for high rate multi-media streaming such as high-definition multimedia interface (HDMI) resulting in cost effective and integrable wireless HDMI solutions. Since 60 GHz signals has low capability to penetrate materials and interfere with other networks, it makes it especially suitable for intra-vehicular wireless networks which works as a wire replacement for communications between multimedia devices (e.g. DVD and MP3 player, back seat screens), portable devices (e.g. Cell phones, Laptops) etc. within any vehicle.

In the commercial area, 60 GHz solutions are best suitable for wireless personal area networks(WPAN) such as Bluetooth and also as a replacement to cables like USB and gigabit Ethernet. In 2009, the IEEE Std 802.15.3c-2009 was released stating the specifications for high rate wireless personal area networks for 60 GHz ISM band. Since this thesis is about the frequency synthesizer, we are only interested in the channelization and modulation scheme.

1.1.3 IEEE 802.15.3c channelization

Four main RF channels were specified in the standard for mmWave PHYs as shown in Table 1.2.

Table 1.2: mmWave PHY Channelization [1]

CHNL ID	Start frequency	Centre Frequency	Stop Frequency
1	57.240 GHz	58.320 GHz	59.400 GHz
2	59.400 GHz	60.480 GHz	61.560 GHz
3	61.560 GHz	62.640 GHz	63.720 GHz
4	63.720 GHz	64.800 GHz	65.880 GHz

A total of three PHYs were defined for the mmWave PHY. They are as follows:

a) Single Carrier mode in mmWave PHY (SC PHY).

b) High Speed Interface mode in mmWave PHY (HSI PHY).

c) Audio/Visual mode in mmWave PHY (AV PHY).

The Single Carrier mode PHY is specified with a high degree of flexibility in order to allow implementers the ability to optimize for different applications. The SC PHY supports operation in NLOS as well as LOS, with or without equalization. The SC PHY

supports a variety of modulation and coding schemes that support up to 5 Gb/s[1]. Depending on the geographical region, its implementation should support at least one channel from the channels allocated in operation as shown in Table 1.2. This PHY mode can be used for low budget applications like kiosk, where data transfer is at a rate of 1.5 Gb/s over a short range(1m) and OFDM PHY is not necessary.

The High Speed Interface mode PHY, is designed for NLOS operation and supports a variety of modulation and coding schemes (MCSs) using different frequency-domain spreading factors, modulations, and LDPC block codes [1]. Similar to the SC PHY, Table 1.2 also represents the set of operating channels for the implementation of the HSI PHY. According to the [1], implementation of HSI PHY should support at least one channel of ID ($CHNL - ID$) 2 or 3. In commercial market, an example of its potential application can be an ad-hoc system to connect computers and devices around a conference table providing bidirectional, NLOS high speed, low-latency communication.

Table 1.3: LRP Channelization [1]

LRP Channel Index	**Start frequency**	**Centre Frequency**	**Stop Frequency**
1	$f_{C(HRP)}$ - 207.625 MHz	$f_{C(HRP)}$ - 158.625 MHz	$f_{C(HRP)}$ - 109.625 MHz
2	$f_{C(HRP)}$ - 49 MHz	$f_{C(HRP)}$	$f_{C(HRP)}$ + 49 MHz
3	$f_{C(HRP)}$ + 109.625 MHz	$f_{C(HRP)}$ + 158.625 MHz	$f_{C(HRP)}$ + 207.625 MHz

The Audio/Visual mode PHY, is designed for NLOS operation and the transport of uncompressed, high definition video and audio. It uses OFDM modulation with convolutional inner code and a Reed Solomon outer code. The AV PHY is implemented with two PHY modes, the high-rate PHY (HRP) and low-rate PHY (LRP). The HRP mode uses the channels defined in Table 1.2. According to the standard, its implementation should support at least the channel, CHNL ID - 2. In each of the HRP channels, three LRP channels are defined. Each of the LRP channels is defined relative to the center frequency of the current HRP channel, $f_{C(HRP)}$. The LRP channels specification can be calculated from the HPR channel as shown in Table 1.3.

The HRP, having a bandwidth of 2 GHz, is used for high definition video streaming,

file transfer and similar applications where multi-gigabit per second data rate is required. The LRP, on the other hand, is used for relatively low data rate asynchronous transfer such as compressed audio, control commands including pilot, beacon and acknowledgment signals, etc.

Although this standard have many potential applications, it commercial use is still limited by the challenges due to the integration of the system. Initially, due to the superior noise characteristics and power handling capabilities at high frequency, non-standard technologies such as GaAs and InGaAs were used to build 60 GHz transceivers. For commercial use, it was not suitable because of their high power consumption, complex and limited digital integration and of course high cost. Hence, the research focus is now on CMOS implementation of 60 GHz transceivers which would provide portability with reduced area consumption, longer battery life with increased power efficiency and low cost for commercialization. CMOS implementation also allows the transceiver to be compatible with the rest of the system.

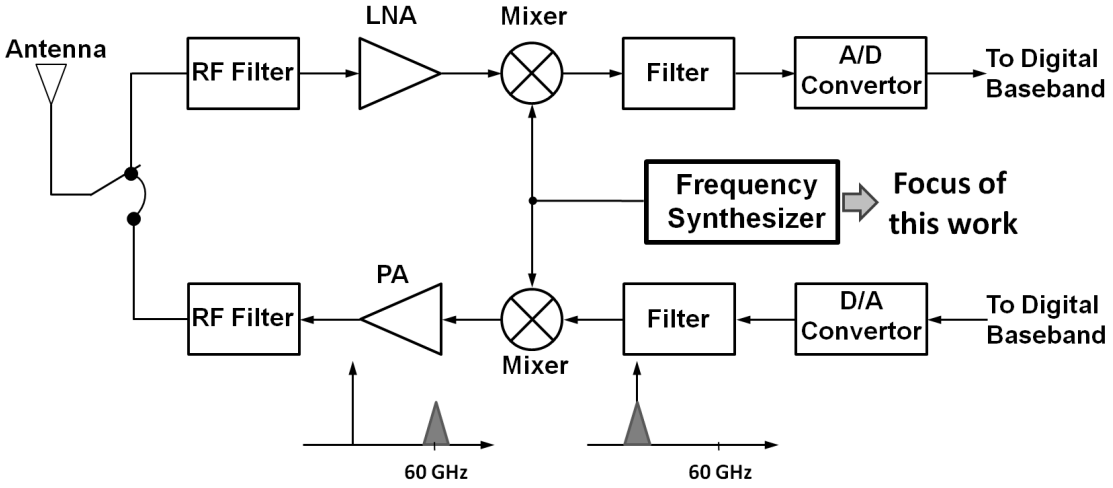


Figure 1.2: Block diagram of a homo-dyne transceiver.

Generally, transceivers can be designed using either homo-dyne or heterodyne architectures. A block diagram of a general homo-dyne transceiver is shown in Fig. 1.2. Homo-dyne receivers directly converts the modulated received signal to its baseband while heterodyne receivers converts the received signal to an intermediate low frequency

and then pass it through a loop filter to filter out any out-of-band and images components. Both these architectures require a frequency synthesizer to provide the local oscillator signal for mixing. When applied to 60 GHz systems, designing the frequency synthesizer block for such high frequency is a challenge since its phase noise and frequency stability determines the sensitivity and bit error rate (BER) of the system. Along with good phase noise performance, the frequency synthesizer also needs to be programmable with a high frequency resolution so that it can cover all the channels.

1.1.4 System Specification

This work focuses on the design of a frequency synthesizer for WPAN IEEE 802.15 standard application. From its channelization, it can be deduced that the frequency synthesizer needs to operate between 57-64 GHz (depending on the geographical region). It needs to have a frequency resolution of at least 2.16 GHz to hop between the center frequencies of channels for high data rate communication. To cover all the channels of LRP PHY, a frequency resolution of 158.625 MHz is needed. The phase noise requirement depends on the modulation scheme, so this work focuses on improving the phase noise as much as possible.

1.2 Thesis Outline

The design challenges of a frequency synthesizer involves both circuit and system level challenges. Specific circuit blocks, such as VCO and divider, are challenging to design due to their phase noise and power consumption constraints. However, system level techniques can alleviate some of the challenges. In this thesis, we approached the problem from both directions - we explored and identified the circuit level limitations and tried to solve them from a system level design approach.

VCO is identified as the single most important component in the synthesizer system since its free-running phase noise dominates the output phase noise of the synthesizer. So, in Chapter 2, different LC VCO topologies are explored and their phase noise trend is studied from 2.4 GHz to 60 GHz. From transistor level simulations, it was found

that for achieving similar phase noise, the cross-coupled oscillator consumes less power while Colpitts oscillators provide inherent buffering. Combination oscillator seemed to be the best solution for high frequency synthesis providing both inherent buffering and power efficiency.

Cadence based transistor level simulation approach is well suited for particular block design. However, transistor level simulation approach is not suitable for architecture study. A behavioral simulation approach is considered efficient to study such systems [5],[6], [7]. In order to study different synthesizer architecture, behavioral model of key blocks in the synthesizer like PLL, DLL and ILO were developed in Chapter 3. To establish confidence in this modeling approach, the simulation results are compared with known experimentally verified results. This provided a platform to evaluate different 60 GHz synthesizer.

In Chapter 4, a literature review of 60 GHz synthesizer is given. An alternate solution is also proposed in this chapter and its benefits compared to existing solutions are evaluated both theoretically and by behavioral simulations. The proposed architecture was also implemented in transistor level in 0.13um CMOS technology in Cadence. The implementation details are given in Chapter 5. The proposed architecture required a 5 GHz fractional - N PLL. A novel architecture for fractional N PLL is proposed in Chapter 6. Finally, the thesis is concluded in Chapter 7 with suggestions for future improvements to this work.

2 Low power high frequency clock generator

Low phase noise VCO is the key to low jitter frequency synthesizer design. LC VCOs are well explored VCO topology for wireless applications. Compared to ring oscillators, LC VCOs can achieve lower phase noise, lower power and they are less sensitive to supply noise. However, they have much narrower tuning range compared to ring VCO. Tuning range becomes even bigger problem as the frequency increases. This chapter studies and compares different VCO topologies in terms of power consumption, phase noise and susceptibility to parasitics. Eventually, we capture the trend about how phase noise would scale as frequency increases. Transistor level simulations were done in Cadence in 0.13um technology.

2.1 VCO phase noise

Before studying different oscillator circuit topology, it is very important to understand the effect of noise in the VCO. The noise in VCO is well explained in [8]. A brief overview of the noise concept in [8] is given in this section.

An ideal VCO has an ideal output sine waveform. Let the amplitude be V_o with constant frequency ω. The instantaneous output voltage is given by

$$V(t) = V_o sin(\omega t + \Phi_o) \tag{2.1}$$

where phase is the argument of the sine function, $\omega t + \Phi_o$, and Φ_o is the initial phase at the (arbitrary) time, $t = 0$.

Phase is simply the integral of frequency, and so when frequency varies in time, the instantaneous phase at time, t is given by

$$\Phi(t) = \int_o^t \omega(t)dt + \Phi_o \tag{2.2}$$

Generally, as shown in Fig. 2.1(a) , the output frequency of a VCO is controlled by an input control voltage, V_{ctrl} such that

$$\omega_{out} = \omega_o + K_o V_{ctrl} \tag{2.3}$$

where ω_o is the center frequency and K_o is the voltage-to-frequency conversion constant (in units of rad/V. s).

Assuming the initial phase, Φ_o, to be zero, the VCO's output phase becomes

$$\Phi(t) = \omega_o t + K_o \int_o^t V_{ctrl}dt \tag{2.4}$$

Ideally, when V_{ctrl} is zero, the VCO runs at its center frequency, ω_o, and the phase increases linearly in time with slope, $\omega_o t$ (Fig. 2.1(b)).

Now, all the noise source in the VCO can be represented as a white noise source at the input i.e. the VCO's control voltage (Fig. 2.1(c)), the output phase executes a random walk over its ideal phase. Note that the variance increases over time. The effect of the white noise can also be seen in the frequency domain as shown in Fig. 2.2. When the white noise power spectrum is integrated, is gives an output phase power spectrum proportional to $1/f^2$. This $1/f^2$ mainly dominates the output free-running phase noise of the VCO.

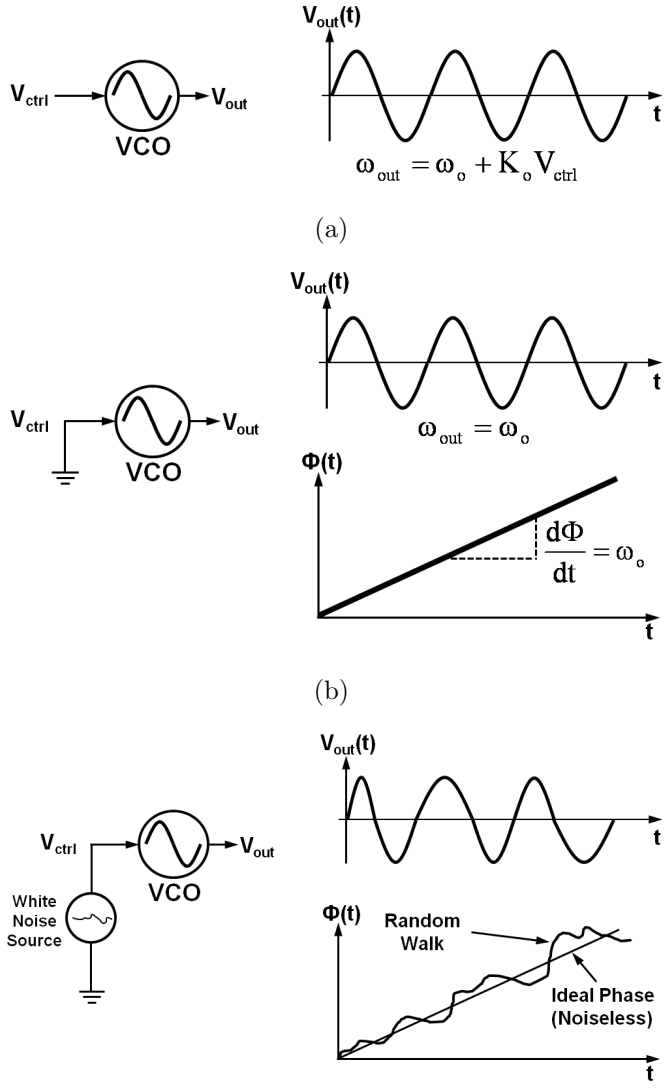


Figure 2.1: Voltage controlled oscillator (a) general definition , (b) ideal free-running with $V_{ctrl} = 0$ and (c) free-running VCO integrating white noise at its input.

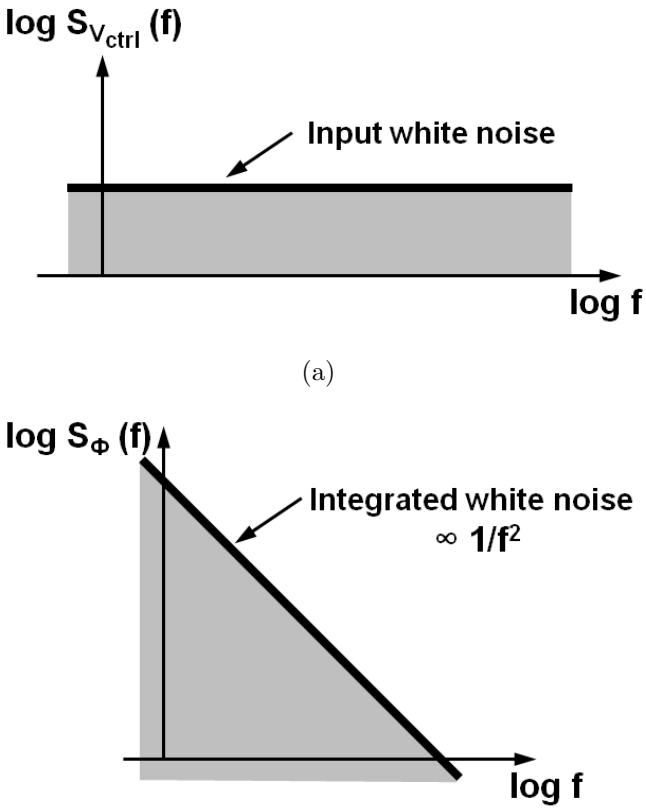


Figure 2.2: Power spectrum of (a) white noise at VCO's input and (b) integrated white noise at the output.

2.2 Cross-coupled Oscillator

A conventional cross-coupled oscillator circuit consists of a LC tank and two cross-coupled transistors, M_1 and M_2 (Fig. 2.3). By varying the variable capacitance, C_{var}, the resonance frequency of oscillation,ω_o can be tuned as,

$$\omega_o \approx \frac{1}{\sqrt{LC_{eq}}} = \frac{1}{\sqrt{L(C_{var} + C_L)}} \tag{2.5}$$

C_L is the load capacitance introduced due to any load connected to the output as well as any parasitic capacitance of the circuit components itself. Higher C_L , as in the case of high frequency VCO's, would result in a smaller tuning range [9]. Hence, a buffer stage is often used to reduce C_L but at the cost of additional power consumption in the buffer.

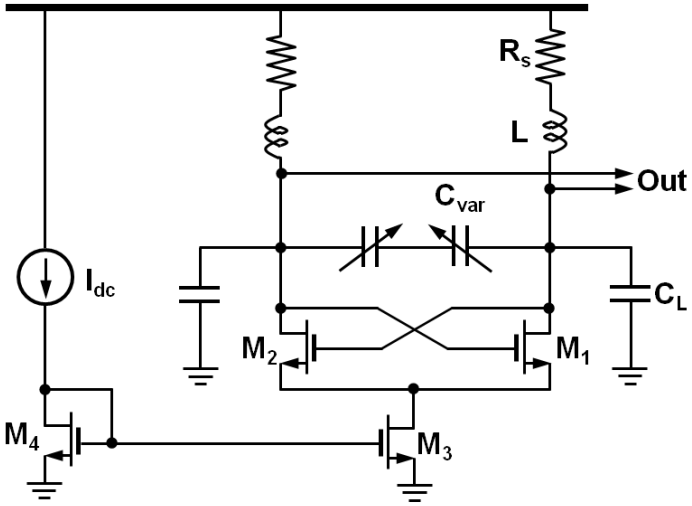


Figure 2.3: Circuit diagram of cross coupled oscillator.

The amplitude of the output voltage,V_{tank} is given by,

$$V_{tank}{}^2 = 2\frac{E_{tank}}{C_{eq}} = 2E_{tank}\omega_o{}^2 L \tag{2.6}$$

where E_{tank} is the energy dissipated at the tank [10].

The phase stability quality factor is given by :

$$Q_{PS} = \frac{1}{R_S}\sqrt{\frac{L}{C_{eq}}} \tag{2.7}$$

A higher $\sqrt{L/C_{eq}}$ would results in a steeper phase roll-off improving phase noise. Thus, for a given frequency (i.e. keeping $\sqrt{LC_{eq}}$ constant) , increasing $\sqrt{L/C_{eq}}$ would result is higher tank swing , lower phase noise and lower power consumption. This

optimization technique is true till it is limited by the supply headroom constraints and beyond that point, the VCO performance would degrade [11].

If R_s represent the series resistance, the inductor quality factor is,

$$Q_L = \frac{\omega L}{R_S} \tag{2.8}$$

where ω is the oscillating frequency.

The parallel equivalent of R_s becomes $R_P = ({Q_L}^2 + 1)R_S$. In order to meet the conditions for oscillation, the parallel equivalent resistance of the LC tank must be equal or greater than the negative resistance provided by the cross-coupling transistors,

$$\frac{1}{g_m} \leq R_P \tag{2.9}$$

$$g_m \geq \frac{1}{R_P} \approx \frac{Q_L}{wL({Q_L}^2 + 1)} \tag{2.10}$$

2.3 Colpitts oscillator

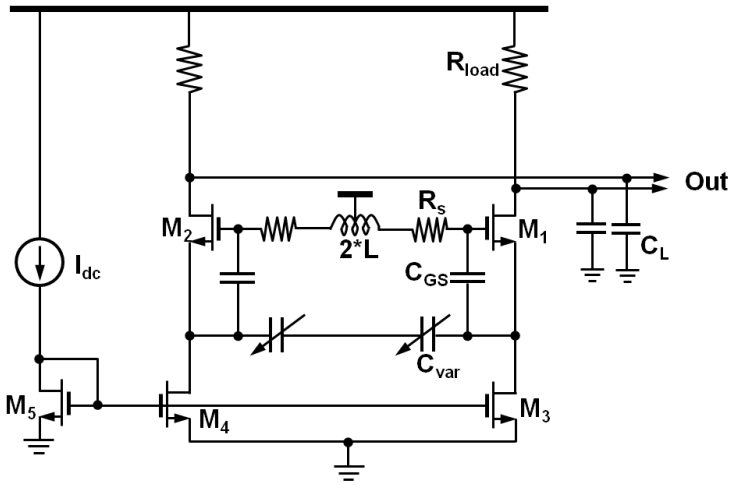


Figure 2.4: Circuit diagram of Colpitts oscillator

As shown in Fig. 2.4, the LC tank of Colpitts oscillator is coupled to the load only through gate to drain capacitance,C_{GD}, of transistors, M_1 and M_2. This is the main advantage of this topology, since it isolates the LC tank from the output capacitive load [12]. The frequency of oscillation,ω_o is :

$$\omega_o \approx \frac{1}{\sqrt{LC_{eq}}} = \frac{1}{\sqrt{L\frac{C_{GS}C_{var}}{C_{GS}+C_{var}}}} \tag{2.11}$$

Unlike the cross-coupled topology, the oscillation frequency in Colpitts is independent of the load capacitor due to the inherent buffering of the topology. Hence, no extra buffer is necessary in this type. Since C_{GS} is in series with C_{var}, at high frequencies when the parasitic capacitances of the transistors are large, C_{eq} would still be small. Thus, for high frequency clock generation, Colpitts oscillator would provide large tuning range compared to cross-coupled VCO.

From the small signal equivalent circuit, the input impedance (Z_{in}), looking into the gate of the $M_{1,2}$, can be derived as:

$$Z_{in} = \frac{-g_m}{\omega^2 C_{GS}C_{var}} + \frac{1}{j\omega}\left(\frac{1}{C_{GS}+C_{var}}\right) \equiv -R_{neg} + \frac{1}{j\omega C_{eq}} \tag{2.12}$$

where R_{neg} is the negative resistance due to M_1 and M_2 and C_{eq} is the equivalent capacitance due to C_{GS} and C_{var} connected in series.

In order to meet the oscillation condition, the series resistance of the tank must be less than or equal to the negative resistance:

$$\begin{aligned} \frac{g_m}{\omega^2 C_{GS}C_{var}} &\geq R_S \\ g_m &\geq \frac{1}{R_P}\frac{(C_{GS}+C_{var})^2}{C_{GS}C_{var}} \end{aligned} \tag{2.13}$$

This factor can be minimized if C_{GS} is equal to C_{var} , resulting in g_m to be greater than or equal to $4/R_P$. Thus, in order to meet the oscillation condition, this topology needs g_m to be four times that for cross-coupled topology consuming more power and area.

2.4 Combination of Colpitts and cross-coupled oscillator

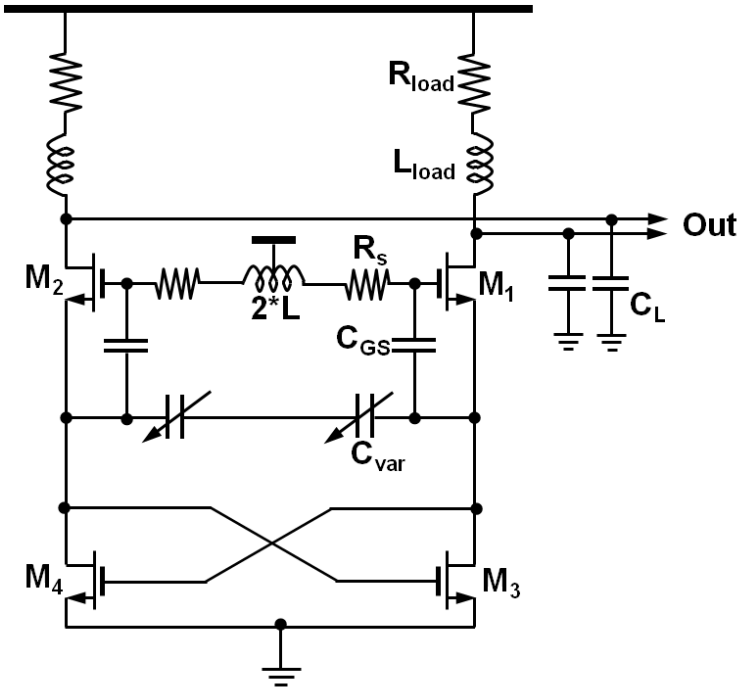


Figure 2.5: Circuit diagram of oscillator combining cross-coupled and Colpitts topology.

The cross-coupled oscillator and the Colpitts oscillator can be combined together as shown in Fig. 2.5[13]. The cross-coupling transistors, M_3 and M_4, mainly provides the negative resistance, which relaxes the oscillation condition and ensures low power oscillation. The transistors, M_1 and M_2, provides the inherent buffering similar to the Colpitts VCO, i.e. it decouples LC tank from the load capacitor. Hence, no extra buffer is needed to drive a high capacitive load and, thus, power consumption is low.

The oscillation frequency is,

$$\omega_o \approx \frac{1}{\sqrt{LC_{eq}}} = \frac{1}{\sqrt{L\frac{C_{GS}C_{var}}{C_{GS}+C_{var}}}} \tag{2.14}$$

The effective quality factor of the tank,(Q_{tank}) in terms of inductor quality factor,Q_L can be derived as,

$$Q_{tank} \approx \frac{Q_L}{1 - R_P \frac{C_{var}}{C_{GS}} g_{m1,2}} \tag{2.15}$$

Thus, this topology helps improve the tank quality factor well beyond Q_L.

The oscillation condition can be derived as,

$$R_{cross-coupled} + R_{colpitts} = g_{m1} + \frac{C_{var}}{C_{GS}} g_{m3} \geq \frac{1}{R_P} \tag{2.16}$$

There are two sets of negative resistance here provided by the bottom cross-coupled pair, $R_{cross-coupled}$ and the top transistors, $R_{colpitts}$. The cross-coupled pair contributes to most of the negative resistance.

2.5 Oscillators at high frequency

For our study, the oscillators mentioned above were simulated in transistor level in CMOS 0.13um technology to operate at 2.4 GHz. Their performance summary is summarized in Table. 2.1. Among the LC tank oscillators, combination oscillator had the advantage of consuming significantly lower power with comparable phase noise and tuning range. All the different topologies of oscillators mentioned above can be scaled to provide high frequency clock. Their behavior at high frequencies like 60GHz can be intuitively understood from their properties at 2.4 GHz.

Table 2.1: Summary of Oscillator Performances

Topology	Frequency (GHz)	Power (mW)		Tuning Range (GHz)	Best Phase Noise (dBc)		
		VCO	Buffer		100 KHz	1MHz	100MHz
Cross-coupled	2.4	12.8	20.4	2.284 to 2.853	-90.6	-114.7	-161.5
Colpitts	2.4	38.3	0	2.222 to 2.467	-89.39	-111.5	-159.2
Combination	2.4	4.22	0	2.396 to 2.790	-91.55	-113.5	-144.5

It is well understood that in general at high frequencies, the parasitic capacitance of the transistors are large. This affects the oscillator performance in several ways. For any LC tank oscillator, the oscillating frequency, $f_{osc} \propto 1/\sqrt{LC_{eq}}$ and the quality factor of the tank, $Q \propto \sqrt{L/C_{eq}}$. So, by keeping the LC_{eq} product constant, and improving the L/C_{eq} ratio, the phase noise of VCO can be improved. However, extending this approach to 60-GHz VCO design is not possible. To illustrate this limitation, lets compare 5 GHz VCO with its 60 GHz counterpart. The LC_{eq} factor for a 5-GHz VCO must be scaled by 144 times to achieve 60-GHz oscillation. To keep the same quality factor both L and C_{eq} should be scaled down by a factor of 12. However, scaling of C_{eq} by factor of 12 leads to a situation where the tank is dominated by parasitic capacitance, C_L. Hence, more practical approach is to scale C_{eq} more conservatively and as a result tank Q is degraded. This is why the phase noise of oscillators is poor at high frequencies.

The parasitic capacitance also hampers the tuning range of the oscillators. C_{eq} of the LC tank has two parts, the parasitic and the variable. The variable capacitance is responsible for the tuning range. Since at high frequencies, the parasitic capacitance is much larger than variable capacitance, the tuning range decreases. In cross-coupled oscillators, in order to increase the tuning range, the equivalent capacitance might be increased by decreasing the inductance value, but at the cost of poor quality factor resulting in poor phase noise. On the other hand in Colpitts oscillator, the tuning range in theory should be relatively greater since the variable capacitor is connected in series with C_{GS}. In the simulation, it was found to be smaller. This is because in order to compare with cross-coupled, the Colpitt's transconductance should be at-least four times that of the cross-coupled, which can be provided by increasing the bias current by four times. Although, the combination oscillator consumes much less power, the tuning range was comparable with the other two oscillators.

Finally, it can be concluded that for high frequency synthesis, combination oscillator is more suitable compared to cross-coupled and Colpitts oscillators.

2.6 Experimental verification

Based on the study, for 60 GHz applications our choice of VCO topology is the combination oscillator because of its inherent buffering, larger tuning range and power efficiency. To capture its frequency trend, we simulated the combination VCO for 5 GHz, 20 GHz and 60 GHz. Their values are summarized in Table 2.2. To gain validation, the simulated values are compared with experimental results(Fig. 2.6). In [13], the combination oscillator was used for generating 20 GHz. In [14], balanced Colpitts oscillator was implemented in 0.18 um CMOS technology for generating 5.6 GHz clock. The measurement results were in good agreement with our simulated phase noise.

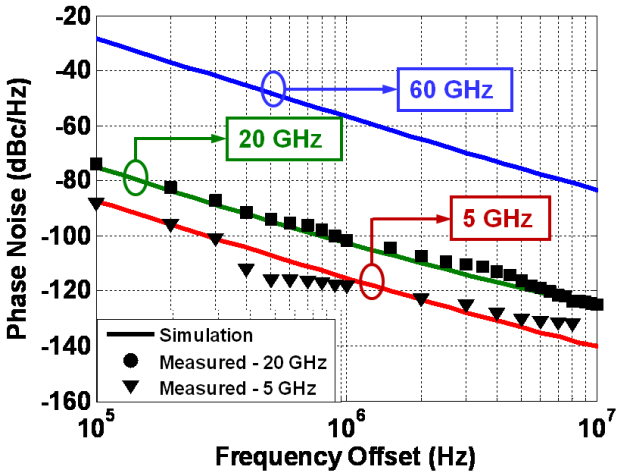


Figure 2.6: VCO phase noise plot at different oscillating frequency.

Table 2.2: Component parameters of oscillators used for experimental verification

Frequency	5.6 GHz	5 GHz	20 GHz	20 GHz	60 GHz
Ref	[14]	This work	[13]	This work	This work
Topology	Balanced Colpitts	Combination	Combination	Combination	Combination
L(um)/W(um)	0.18/30 0.18/105	0.12/30 0.12/80	0.12/16 0.12/16	0.12/16 0.12/16	0.12/40 0.12/40
C_{eq}	1.33pF	1pF	100fF	100fF	167fF
L_{eq}	0.759nF	1nF	500pF	500pF	41pF
Q	5.76	5	4	4	8
VCO Power	2.4 mW (w/o buffer)	5 mW	20 mW (quad. VCO)	10mW	12 mW

3 Behavioral modeling of clock synthesizer

The main purpose of a frequency synthesizer block is to generate a high frequency signal from a low frequency reference signal generally coming from an off-chip crystal oscillator. It corrects the output phase by tracking the input signals phase using a feedback loop. This phase tracking can be generalized into three different techniques: phase-locked loop (PLL), delay-locked loop (DLL) and injection locked oscillator (ILO).

In order to design a PLL, DLL or ILO, several tradeoffs must be made like bandwidth vs. stability and power vs. jitter. To understand these tradeoffs better, and make an optimal design choice, accurate modeling of them is essential. Behavioral modeling has proven to be an excellent method for exploring different clock architecture [6]. For this thesis, Simulink of Matlab was used to do discrete time simulation of each model. The goal of this chapter is to establish behavioral model to represent PLL, DLL and ILO. These models will be verified against theoretical results and then will be later utilized to study proposed architecture.

3.1 Phase Locked Loop (PLL)

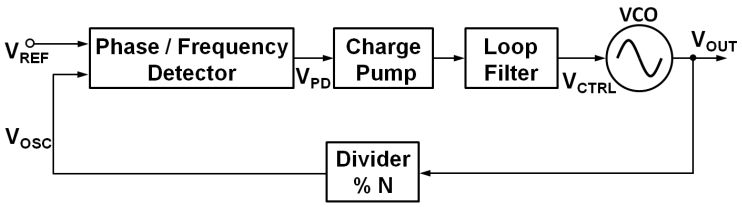


Figure 3.1: PLL Block Diagram

Phase locked loop (PLL) is the most commonly used frequency synthesizer. A simplified block diagram of a phase locked loop is shown in Fig. 3.1. The components

of a PLL generally include a phase / frequency detector, a charge pump, a divider and a voltage controlled oscillator (VCO). The basic functionality is as follows. The nominal frequency of the VCO is N times the reference frequency. Oscillator's output is divided and compared to the reference using a phase/frequency detector (PFD). The PFD output is then filtered using low pass filter and then used to adjust the control voltage of the VCO. When the PLL is in the locked condition, the two inputs of the phase detector are in-phase (or have a fixed phase offset), and the output frequency is equal to the reference frequency multiplied by the divider ratio, N.

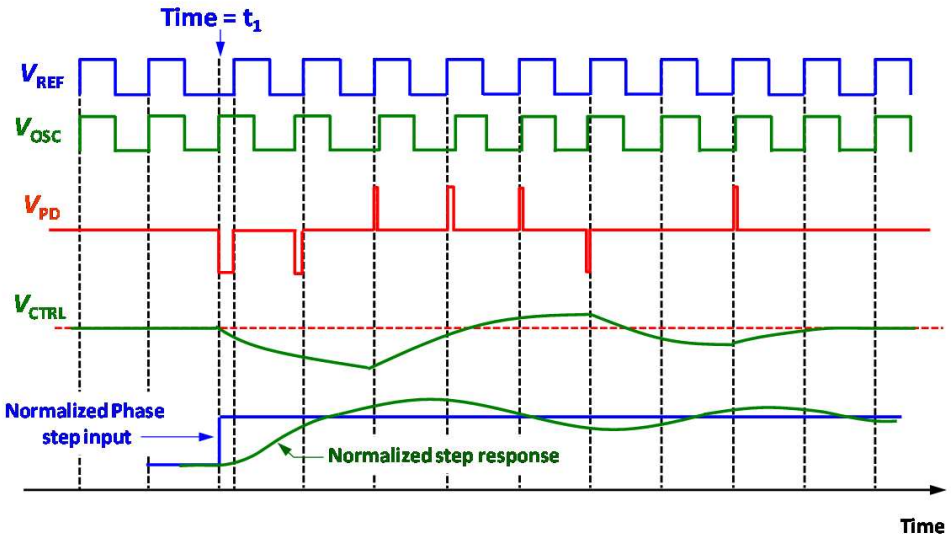


Figure 3.2: Timing diagram of PLL's phase tracking

To help explain PLL operation, let's consider the phase domain step response of a PLL (Fig. 3.2). Assuming the PLL is initially locked and phase detectors output, $V_{PD} \approx 0$. At time t_1 a reference signal is given a phase shift causing a phase difference between the reference and the output. This error is detected in the phase detector and, thus, its output, V_{PD}, has a negative pulse indicating that the output is leading the reference signal. The charge pump and the loop filter then integrates this negative pulse reducing the control voltage, V_{CTRL} of the oscillator such that the oscillating frequency decreases slightly. In the third cycle, the reduced V_{CTRL} actually caused the output to lag the reference signal and hence now the V_{PD} gives a positive pulse

causing V_{CTRL} to increase such that now the oscillator oscillates faster. This process is continued until the phase difference between them is zero and hence the PLL locks.

Note that the output phase follows the input phase with a slightly under-damped response in the time domain. From this response, it can be deduced that the PLL's input transfer function is a 2^{nd} order system with two poles - one generated by the VCO and the other by the loop filter. Hence, to stabilize the system, a zero is included by adding a resistor in the loop filter.

3.1.1 Phase domain model of PLL

A suitable s-domain model of the control loop can be extracted by simply replacing each component in the PLL's block diagram by their equivalent s - domain representation as shown in Fig. 3.3. The phase of the input signal is represented by Φ_{IN} and Φ_{OUT} denotes the PLL's output phase. Since the phase detector detects the phase difference between the input and the output, it can be replaced by a single subtracting block in the s-domain. The gain of the phase detector, K_{pd} is equal to $I_{cp}/2\pi$, where I_{cp} is the charge pump current. VCO in frequency domain is simply an integrator denoted by K_{vco}/s. Loop filter with capacitance, C is indicated by K_I/s. Now since there are two integrators in series along with the feedback, it causes stability concerns. To stabilize the loop, a proportional path, K_p is added which represents series resistance, R, in the filter. The phase noise originating at the VCO is shown as Φ_{VCO}. N is the multiplication ratio of the PLL.

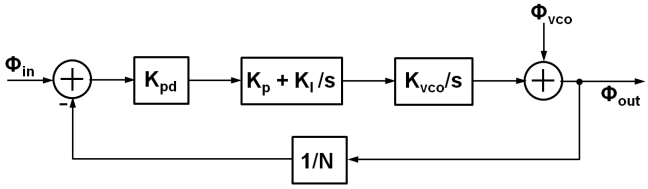


Figure 3.3: Linearized model of a PLL.

In order to derive the input phase noise transfer function,Φ_{OUT}/Φ_{IN} of the PLL, the effect of VCO noise was ignored(i.e. $\Phi_{VCO} = 0$). Thus, from Fig. 3.3, the following transfer function may be derived

$$\frac{\Phi_{OUT}}{\Phi_{IN}} = N * (\frac{K_{pd}K_PK_{VCO}s + K_{pd}K_IK_{VCO}}{Ns^2 + K_{pd}K_PK_{VCO}s + K_{pd}K_IK_{VCO}}) \tag{3.1}$$

Thus, the input to output transfer function is essentially a 2^{nd} order low pass filter. This indicates that any noise generated from the input will pass through the PLL and contribute to the output phase noise at lower frequencies and would be filtered by the PLL at high frequency offsets. Similarly, the VCO jitter transfer function, Φ_{OUT}/Φ_{VCO} can be derived from Fig. 3.3 to be a high pass function as:

$$\frac{\Phi_{OUT}}{\Phi_{VCO}} = \frac{Ns^2}{Ns^2 + K_{pd}K_PK_{VCO}s + K_{pd}K_IK_{VCO}} \tag{3.2}$$

Hence, the free-running phase noise of the VCO will be filtered by the PLL at lower frequencies up to the PLL's bandwidth.

The damping factor of the PLL can be calculated from [15]as,

$$\zeta = \frac{R}{2}\sqrt{\frac{I_{cp}K_{vco}C}{2\pi N}} \tag{3.3}$$

The PLL's bandwidth is given in [15] as

$$\omega_{-3dB} \approx \frac{I_{cp}RK_{vco}}{2\pi N} \tag{3.4}$$

Although all PLL components contribute to its output noise S_{out}, it is mainly dominated by the unfiltered VCO phase noise and the amplified phase noise of the reference signal. This can be represented in equation as:

$$S_{out} \approx S_{ref}\left|\frac{\Phi_{out}}{\Phi_{in}}\right|^2 + S_{vco}\left|\frac{\Phi_{out}}{\Phi_{vco}}\right|^2 \tag{3.5}$$

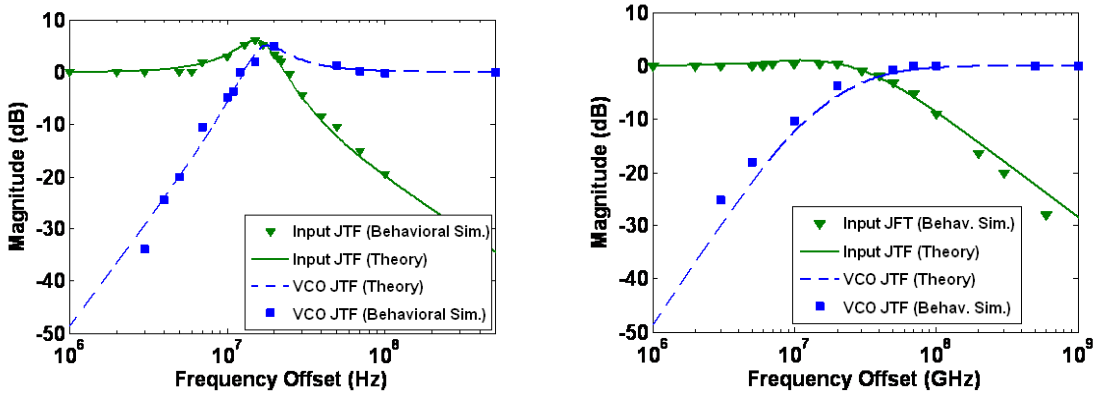
where S_{ref} is the unfiltered phase noise of the reference signal and S_{vco} is the un-

filtered VCO free-running phase noise. The loop bandwidth is generally set at the intersection of S_{vco} and the amplified (by N^2) reference phase noise. Thus, within the bandwidth, the amplified reference phase noise dominates, but beyond the bandwidth, the VCO phase noise dominates the output phase noise of the PLL.

A 2.4 GHz PLL was modeled in this study using Simulink in Matlab. The PLL provides 6x multiplication from a 400 MHz reference. Other pertinent parameters are summarized in Table. 3.1.

Table 3.1: Parameters of PLL behavioral simulation.

Parameter	Value
R	1.8 kΩ
C	7.8 pF
I_{cp}	0.5 mA
K_{vco}	2.4 GHz/V
N	6



(a) (b)

Figure 3.4: Simulated phase noise transfer function of PLL with (a) R = 1.8 kΩ and (b) R = 7.2 kΩ

The effect of proportional gain, K_P on the PLL transfer function was studied and the result is shown in Fig. 3.4. Increasing R from 1.8 kΩ to 7.2 kΩ, the damping factor is improved by 1.345. As a result, the phase overshoot is reduced and bandwidth increased

from around 10 MHz to 30 MHz. As expected, the theoretical result is in very good agreement with simulation results. Depending on the application requirement, the bandwidth of the PLL can be chosen so that an optimized phase noise filtering could be done. However, PLL suffers from several disadvantages:

- Jitter accumulation because the VCO phase noise is never completely corrected,
- Longer locking time due to low bandwidth (normally in the range of 10 to 30 MHz),
- The need for a higher order loop filter due to stability issues.

3.2 Delay Locked Loop (DLL)

DLL is composed of a delay line, consisting of cascaded multiple identical delay cells, whose delay is controlled by the control voltage, V_{CTRL}. To achieve a controlled amount of delay through the delay line, phase of the input and output of the delay line are compared and V_{CTRL} is accordingly adjusted as shown in Fig. 3.5.

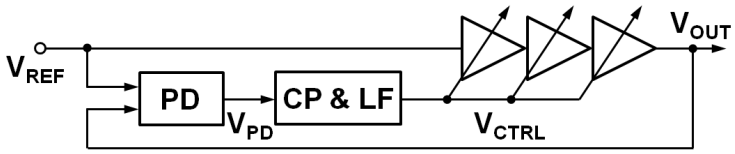


Figure 3.5: DLL Block Diagram

Generally, the delay line provides a delay of one clock cycle i.e. 1 UI so that the output of the last delay stage is in phase with the reference signal. The phase detector detects any phase error between the input and the output of the last delay stage. This error signal is, then, integrated and, then, translated to additional delay so that the total delay is 1 UI.

To gain qualitative understanding, let's consider phase domain step response as shown in Fig. 3.6. Initially, the DLL was in locked condition with the output, V_{OUT}, being in phase with the input signal, V_{REF}. At time t_1 the input is given a phase

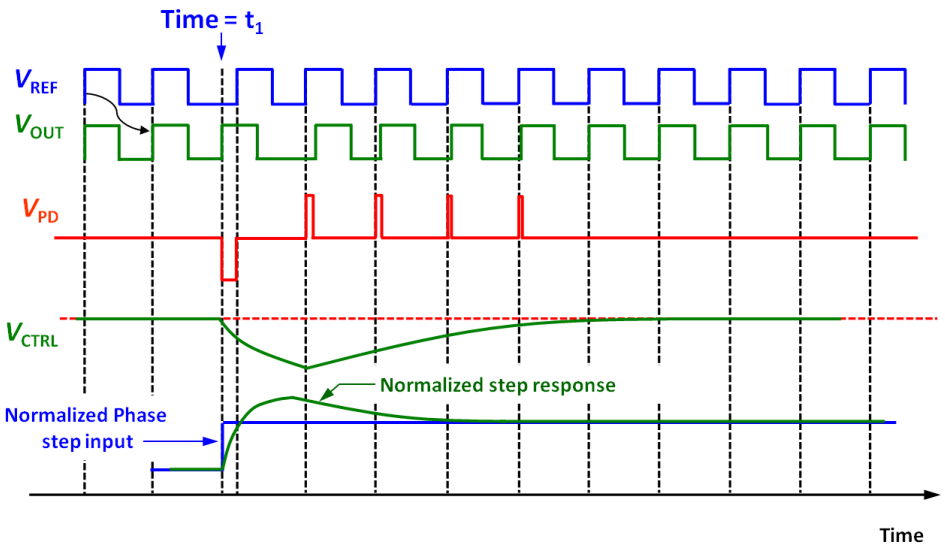


Figure 3.6: Timing diagram of DLL's phase tracking

shift, the output of the DLL remains unchanged and thus at this time, the output lags the input signal. The phase detector detects this phase difference and hence generates a negative pulse. This causes a reduction in the control voltage such that the delay provided by the delay line is increased by an amount equal to the phase difference. In the next cycle, the input and output was expected to be in phase. But from the timing diagram, it can be seen that in the next cycle, the output phase is actually shifted more than it was required. This is because there is a direct path from the input to the output through the delay line. So the phase overshoot at the output in the next clock cycle is caused by mainly two phenomenon:

1. The change in input phase, which is passed directly to the output.
2. The extra delay of the delay line due to the reduced control voltage caused by the phase error in the previous cycle.

Now the output is leading the input and hence the phase detector generates a positive signal causing the control voltage to increase and thus the delay of delay line decreases. Eventually, the two signals are in phase and the DLL becomes locked.

The output follows the input phase with a peak, called jitter peaking, due to the phase overshoot. From the phase step response, it can be deduced that the DLL input

transfer function is all pass with little peaking.

3.2.1 Phase domain model of DLL

A simplified s-domain model of a DLL is shown in Fig. 3.7 [7]. In this model,ϕ_{in} and ϕ_{VCDL} are the noise sources that originate at the input and the delay line respectively. T_{dl} is the total delay introduced by the delay line. ϕ_{out} is the phase noise at the output of the DLL. K_{PD} and K_{dl} are the gain of the phase detector and the delay line respectively. Since the DLL has no stability issue, so a first order loop filter,$1/sC$ was used.

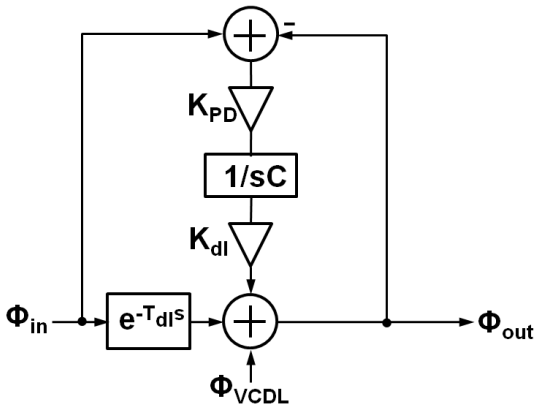


Figure 3.7: Linearized model of a DLL.

From Fig. 3.7, the input phase noise transfer function of the delay locked loop can be derived as :

$$\frac{\Phi_{out}}{\Phi_{in}} = \frac{1 + \frac{s}{\omega_p} e^{-\tau_{dl} s}}{1 + \frac{s}{\omega_p}}. \tag{3.6}$$

where $\omega_p = \frac{K_{PD} K_{dl}}{C}$ is the bandwidth of the DLL.

The delay line phase noise transfer function can similarly be derived to be a high

pass function as :

$$\frac{\Phi_{out}}{\Phi_{VCDL}} = \frac{\frac{s}{\omega_p}}{1+\frac{s}{\omega_p}}. \tag{3.7}$$

Considering only the input noise, S_{in} and the VCDL noise, S_{VCDL} as the main contributors of phase noise, the output phase noise of the DLL becomes

$$S_{out} \approx S_{in}\left|\frac{\Phi_{out}}{\Phi_{in}}\right|^2 + S_{VCDL}\left|\frac{\Phi_{out}}{\Phi_{VCDL}}\right|^2 \tag{3.8}$$

Thus, any noise generated in the delay line will be filtered by the DLL within its bandwidth while the input noise will be unfiltered.

Table 3.2: Parameters of DLL for behavioral simulation.

Parameter	Value
C	1 pF
I_{cp}	2 mA
K_{dl}	261 ps/V

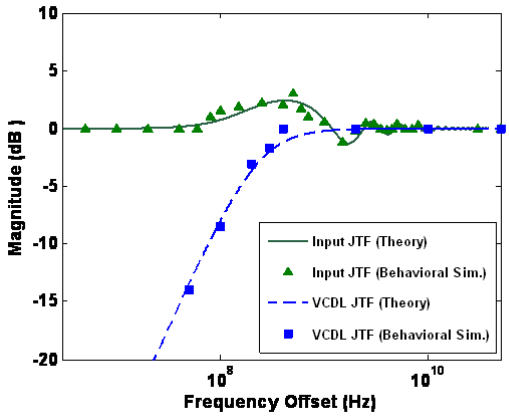


Figure 3.8: Phase noise transfer characteristics of DLL.

Similar to the PLL, DLL was also modeled in simulink with a $2.4GHz$ reference .A

screen-shot of the model is given in the Appendix. The parameters used for simulation is shown in Table. 3.2. In order to obtain the phase noise transfer characteristics, ϕ_{in} and ϕ_{VCDL} was modulated with different frequencies and the effect was observed at the output. The results are plotted in Fig.3.8 along with the theoretical transfer function obtained from the previous equations. The behavioral simulation results matched very closely with the theoretical equation and hence proving that this model is valid. Since the input noise transfer function of the DLL is an all pass function, so any noise at the input will propagate to the output without any attenuation. The peaking is due to the phase overshoot as there is a direct path between the input and the output through the delay line. The VCDL noise transfer function is a high pass function i.e. any low frequency noise of the VCDL will be filtered out by the DLL. The bandwidth of the DLL is set by the bandwidth of the VCDL noise transfer function and generally it can be up-to several 100's of MHz.

DLL offers several advantages in comparison to PLLs.

1. Unlike PLLs, delay locked loops does not have a VCO and thus, no jitter accumulates due to the delay line.

2. DLL does not suffer from any stability issues and hence a simple first order low pass filter may be used as the loop filter without any design complications. That is why their bandwidth can be significantly higher.

3. It has a much larger loop bandwidth causing it to lock much faster to the reference signal.

Main short coming of the conventional DLL is that it does not provide clock multiplication. Although multiplying DLL's are used in literature, their performance is significantly worse compared to PLLs.

3.3 Injection Locked Oscillator (ILO)

The limitations of a PLL due to the low bandwidth range can be overcome using an injection-locked oscillator (ILO). ILOs behave similar to a PLL but without the complexity of having a phase/frequency detector, charge pump, and loop filter. It is basically a simple oscillator. When injected by a reference signal with appropriate

strength, the oscillator phase locks to the reference signal's phase. The oscillator can be an LC VCO, Fig. 3.9(a), or a ring oscillator, Fig. 3.9(b), depending on application requirement. Functionally, both oscillators behave in the same way. For any phase shift in the reference signal, the ILO tracks it gradually like a PLL as shown in Fig. 3.10.

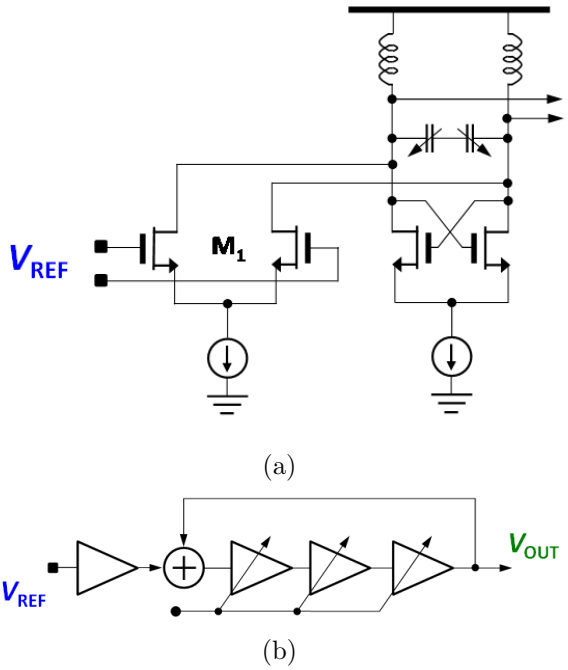


Figure 3.9: (a) LC VCO based ILO and (b) Ring oscillator based ILO

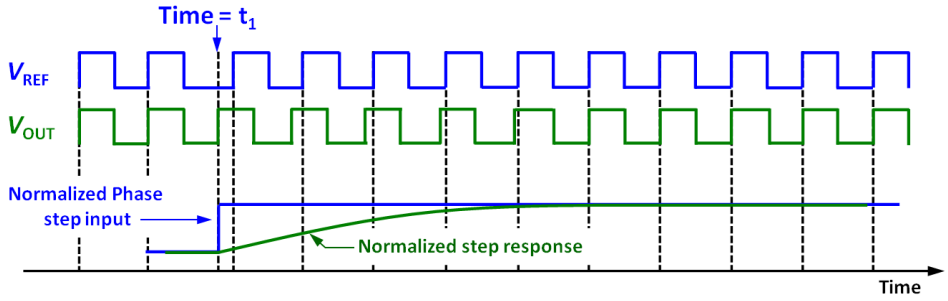


Figure 3.10: Timing diagram of ILO's phase tracking

Frequency multiplication by N times can also be achieved for as long as the N^{th} harmonic of the reference signal falls within the locking range of the ILO. The main advantage of ILO is the fact that it has a relatively higher bandwidth compared to PLL's bandwidth which is limited by its stability issues. Hence, even if the VCO has a poor free-running phase noise, ILO filters it over a wide bandwidth improving the overall phase noise performance.

3.3.1 Phase domain model of ILO

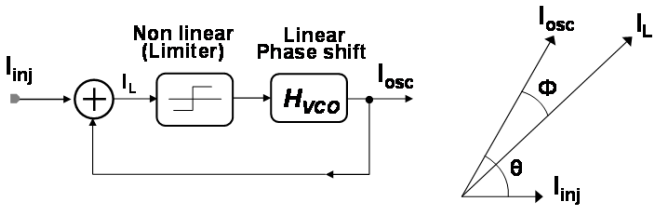


Figure 3.11: ILO model and corresponding vector diagram

We can adopt the ILO model shown in Fig. 3.11 for any injection method and oscillator topology [16][17]. Here, H_{VCO} is the VCO's small-signal open loop frequency response and will depend on the VCO topology. In the case of an LC oscillator, H_{VCO} is a tuned response, whereas, in case of a ring oscillator, H_{VCO} is a low pass response. Nonlinearities associated with the VCOs are taken into account by the nonlinear block. Phase domain model of ILO has not been explored much in the research field. In this work, an s-domain model of sub-rate injected ILO is proposed (Fig. 3.12). The VCO gain is represented by K_{vco} and its free-running frequency is set by a constant voltage, V_c. The pulse generator generates a set of narrow pulses representing the rising/falling edges of the input signal. For frequency multiplication by N times, the switch controlled by the pulse generator ensures that the ILO's phase is corrected by the reference phase on every N^{th} clock cycle.

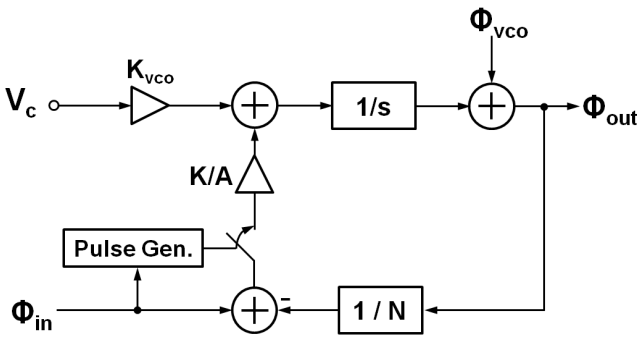


Figure 3.12: Phase domain model of a sub-rate injected ILO

The lock range of ILO can be derived as [13],

$$\omega_{LOCK} = \frac{1}{NA}\frac{K}{\sqrt{1-K^2}} \tag{3.9}$$

where $K = |I_{inj}|/|I_{osc}|$ is the injection strength and A is defined as

$$A \cong \frac{n}{2\omega_o}\sin(\frac{2\pi}{n})....ring - VCO \tag{3.10}$$

$$A = \frac{2Q}{\omega_o}....LC - VCO \tag{3.11}$$

where n is the number of stages in the ring and Q is the quality factor of LC tank.

ILOs are functionally equivalent to a first order PLL [16]. This can be understood by deriving the input and VCO phase noise transfer function from the s-domain model as

$$\frac{\Phi_{out}}{\Phi_{in}} = \frac{N}{1+\frac{s}{\omega_P}} \tag{3.12}$$

$$\frac{\Phi_{out}}{\Phi_{vco}} = \frac{\frac{s}{\omega_P}}{1+\frac{s}{\omega_P}} \tag{3.13}$$

where the bandwidth of the ILO,ω_P is given by

$$\omega_P = \frac{1}{N} \cdot \frac{K}{A} \tag{3.14}$$

Thus similar to a PLL, the input noise is low pass filtered while the VCO noise is high pass filtered. The bandwidth is set by the injection strength, K and the multiplication ratio, N. If S_{inj} is the phase noise of the injected signal and S_{VCO} is the VCO phase noise, then the phase noise of the de-skewed clock is

$$S_{out} = |\frac{\Phi_{out}}{\Phi_{in}}|^2 S_{inj} + |\frac{\Phi_{out}}{\Phi_{vco}}|^2 S_{VCO} \tag{3.15}$$

For simulation, at-first a $5GHz$ 4-stage ring oscillator was injected by a $5GHz$ reference signal. A screen shot of the model used is given in the Appendix. The effect of input and VCO phase noise on the output was observed for different injection strength,K and the results are given in Fig. 3.13. As expected, when K was increased from 0.1 to 0.3, the bandwidth of the ILO proportionally increased from 250 to 750 MHz. For evaluating the effect of multiplication ratio on the bandwidth, K was kept constant at 0.36. As shown in Fig. 3.14, increasing the multiplication ratio from 1 to 4, the bandwidth shifted from 400 MHz to 100 MHz. Note that the simulation results of the input and VCO transfer function are in good agreement with the theory proving that the simulink model does represent the s-domain model of Fig. 3.12.

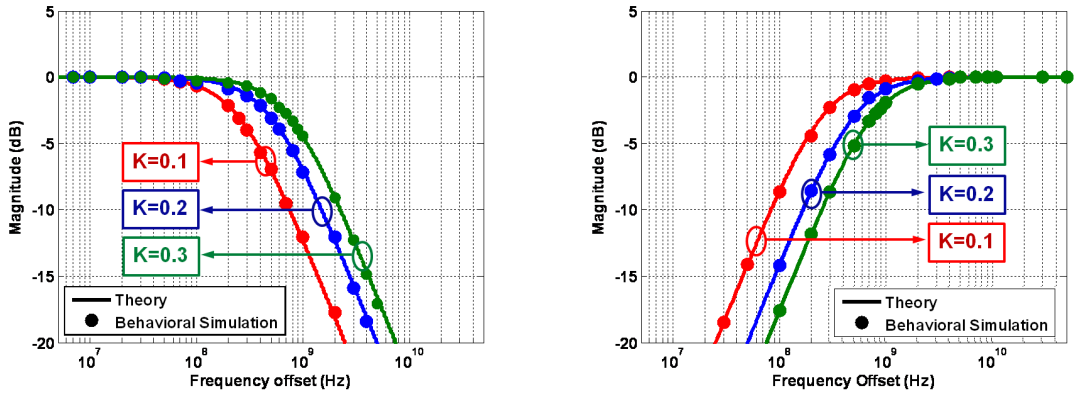
The advantages of ILO can be summarized as follows:

1. No phase/frequency detector, charge pump and loop filter required and hence power and area efficient.

2. Does not suffer from any stability issues.

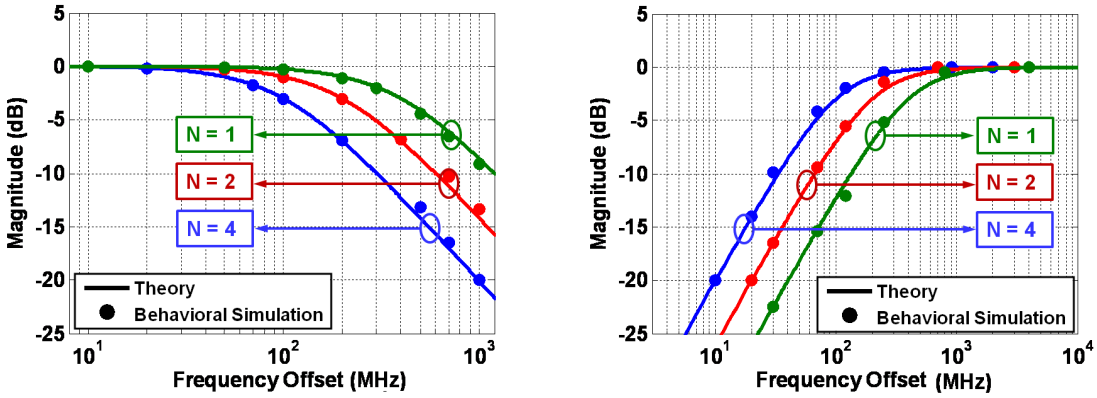
3. Has a wide bandwidth and hence has fast locking time compared to PLLs and DLLs.

On the other hand, for large multiplications, ILO's bandwidth significantly decreases along with the locking range. Hence, if the reference frequency or any of its harmonic does not fall within the locking range, there is no way to ensure that the ILO is locked.



(a) (b)

Figure 3.13: (a) Input phase noise transfer function and (b) VCO phase noise transfer function of an ILO for N = 1.



(a) (b)

Figure 3.14: (a) Input phase noise transfer function and (b) VCO phase noise transfer function of an ILO for K = 0.36.

3.3.2 Experimental Verification

Behavioral model of the ILO is verified with the experimental results. Note that the ILO design and fabrication was not part of this thesis. For model verification and cor-

relation, we are using an existing injection locked oscillator fabricated in 65nm CMOS process. Experimental setup is shown in Fig. 3.16. Experimental results are provided by Dr. Masum Hossain of the University of Toronto. The ILO used in his design was a 4-stage ring oscillator operating at 5 GHz. Based on the provided design variables, the model parameters were calculated and correlated with the jitter transfer functions for different multiplication ratio. As shown in Fig. 3.15, the behavioral simulation is in good agreement with the measured results and which verifies the proposed model of the ILO.

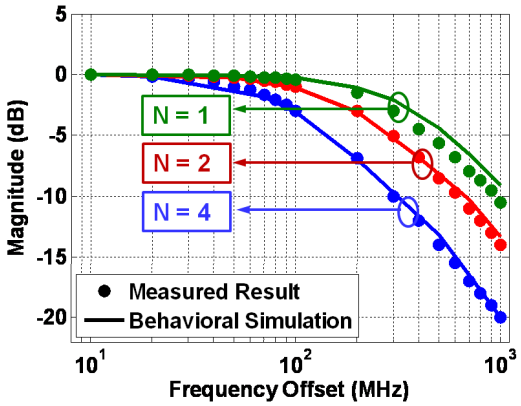


Figure 3.15: Input phase noise transfer characteristics of sub-rate ILO for $K = 0.36$.

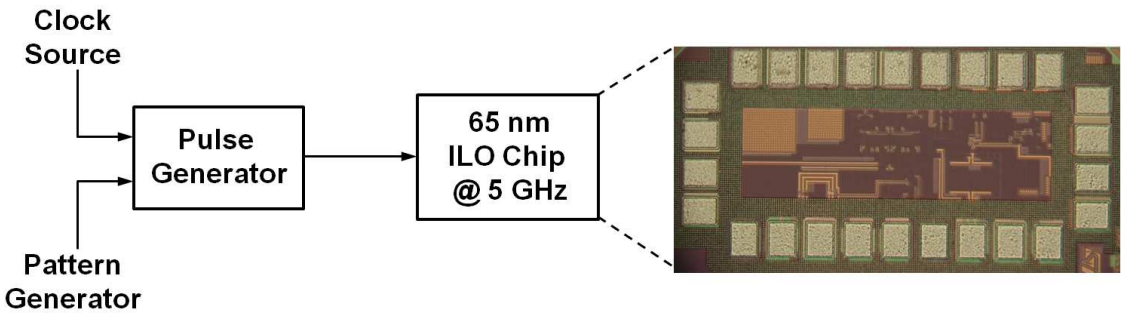
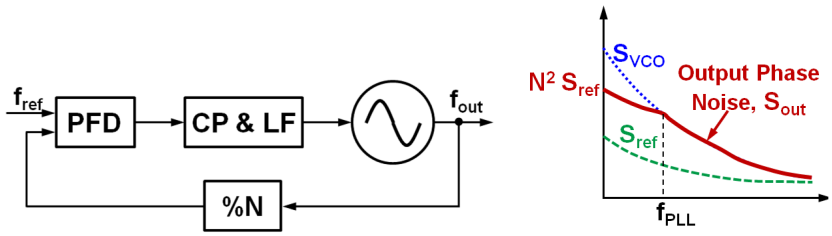


Figure 3.16: Experimental setup for measuring the transfer function of fabricated ILO chip.

4 60 GHz frequency synthesizer-architecture study

From Chapter 2, it is understood that no matter what the oscillator topology, the free-running phase noise of 60 GHz VCO will be poor. In order to filter out its effects, different phase tracking techniques may be used as discussed in Chapter 3. It was found that the output phase noise of the synthesizer may be improved by keeping the bandwidth large so that the VCO phase noise is filtered at lower frequencies. This chapter gives a literature review of the previous work on high frequency synthesizer. Then an alternate solution for achieving a wide bandwidth is proposed. Both behavioral and transistor level simulations were done for the proposed architecture.

4.1 Literature Review



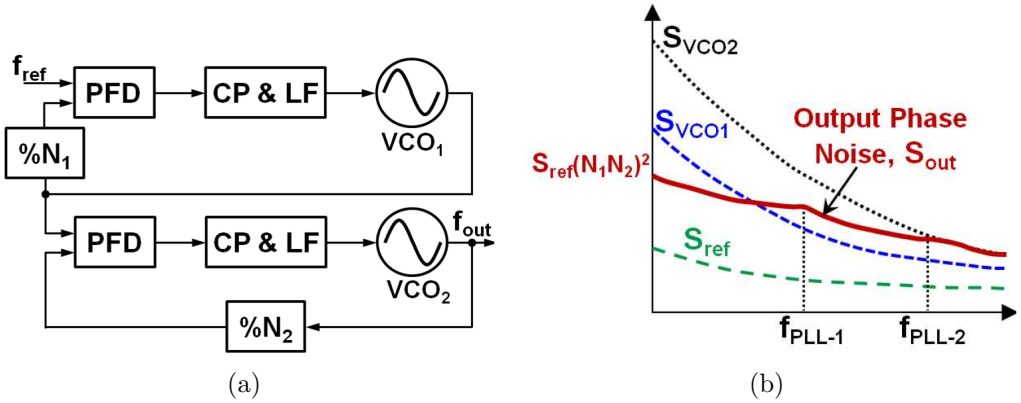
(a) (b)

Figure 4.1: Integer PLL (a) Block Diagram and (b) Phase Noise

PLLs are generally used for high frequency synthesis [18] [19] [20]. The phase noise filtering behavior of PLL is summarized in Fig. 4.1. S_{ref} and S_{vco} represents the unfiltered phase noise originating at the input and VCO respectively and N is the

multiplication ratio. Within the PLL's bandwidth, f_{PLL}, the output phase noise is dominated by the amplified reference phase noise; while outside the PLL bandwidth, it is dominated by VCO phase noise. As stated in the Chapter 2, at high frequency, oscillators have a poor phase noise performance. Hence, in order to minimize its effect on the output, f_{PLL} is preferred to be large.

For better performance, the reference signal is required to have a very good phase noise which is generally met by an off-chip crystal oscillator. Commercially available crystals normally operate around 100 MHz. Hence, in order to generate 60-GHz frequency signal, the multiplication ratio becomes very large, i.e., $N = 60GHz/100MHz = 600$. Since the optimum PLL bandwidth is inversely proportional to N, VCO phase noise would be filtered over a narrow bandwidth degrading the over-all phase noise at the output.



(a) (b)

Figure 4.2: Dual PLL (a) Block Diagram and (b) Phase Noise

To overcome this problem, cascaded or dual PLLs may be used as proposed in [21]. Suppose that first and second PLLs are labeled as PLL-1 and PLL-2, respectively, as shown in Fig. 4.2(a). Each of them contributes partially to the overall multiplication factor, i.e., $N = N_1 \cdot N_2$, where N_1 and N_2 are the multiplication ratios of PLL-1 and PLL-2, respectively [21].

The overall phase noise at the output of the cascaded PLL becomes

$$\begin{aligned} S_{out} &= S_{in}\left|\frac{\Phi_{out1}}{\Phi_{in}}\right|^2\left|\frac{\Phi_{out}}{\Phi_{out1}}\right|^2 + S_{vco1}\left|\frac{\Phi_{out1}}{\Phi_{vco1}}\right|^2\left|\frac{\Phi_{out}}{\Phi_{out1}}\right|^2 \\ &\quad + S_{vco2}\left|\frac{\Phi_{out}}{\Phi_{vco2}}\right|^2 \\ &= S_{in}N_1^2N_2^2\left|H_1(s)\right|^2\left|H_2(s)\right|^2 \\ &\quad + S_{vco1}N_2^2\left|1-H_1(s)\right|^2\left|H_2(s)\right|^2 \\ &\quad + S_{vco2}\left|1-H_2(s)\right|^2 \end{aligned} \tag{4.1}$$

where $\frac{\Phi_{out1}}{\Phi_{in}}$ and $\frac{\Phi_{out}}{\Phi_{out1}}$ are the input jitter transfer functions, and $\frac{\Phi_{out1}}{\Phi_{vco1}}$ and $\frac{\Phi_{out}}{\Phi_{vco2}}$ are the VCO jitter transfer functions of PLL-1 and PLL-2, respectively. The S_{in} is the input reference signal phase noise, S_{vco1} and S_{vco2} are the free-running phase noises of the VCOs in PLL-1 and PLL-2 correspondingly. $H_1(s)$ and $H_2(s)$ represents the high pass transfer functions of PLL-1 and PLL-2 for $N = 1$.

Cascading PLLs are useful, especially, when $(N_1N_2)^2S_{in} > S_{vco2}$. Furthermore, the PLLs should be chosen such that the $f_{PLL-1} < f_{PLL-2}$ and $S_{vco1} < S_{vco2}$, where f_{PLL-1} and f_{PLL-2} are the bandwidths of PLL-1 and PLL-2, respectively. For frequencies below the cut-off frequency of PLL-1, the overall phase noise is dominated by the factor $N_1^2N_2^2S_{in}$. And for $f_{PLL-1} < f < f_{PLL-2}$, the S_{vco1} dominates S_{out}. Then at higher frequencies, the S_{vco2} defines the output phase noise [21]. This is illustrated in Fig. 4.2(b).

In order to generate 60 GHz clock from 100 MHz reference, let's consider $N_1 = 50$ and $N_2 = 12$. Thus the 1^{st} PLL provides majority of the multiplication while the 2^{nd} PLL filters the 60 GHz VCO phase noise over a wider bandwidth. Designing the first PLL for 5 GHz clock is relatively easier [22]. However, designing the second PLL is challenging for several reasons. Firstly, the 60 GHz VCOs phase noise must be filtered up to high frequency offsets. Secondly, designing divider for 60 GHz clock is complex and may consume lots of power. Besides, the phase/frequency detector and charge pump should operate at 5 GHz which may also consume much power. Thus, the performance of the resulting synthesizer is highly constrained by the second PLL.

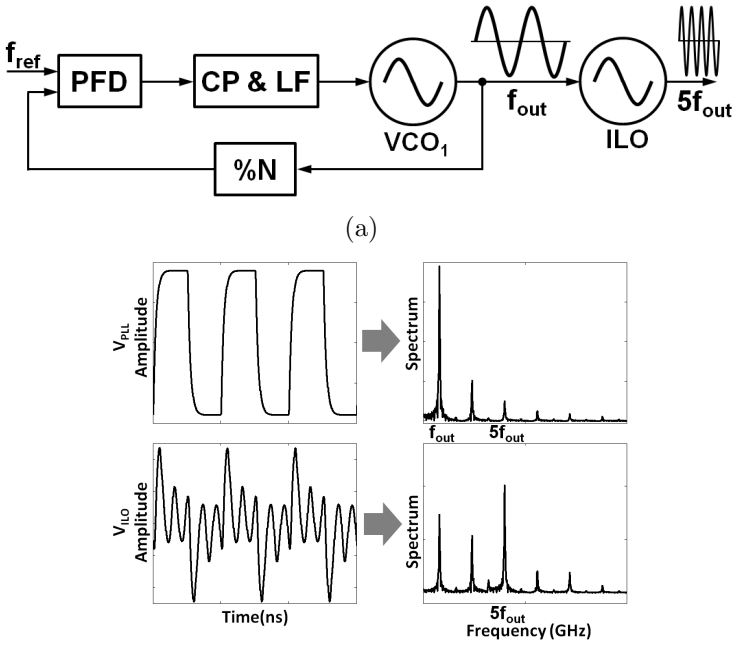


Figure 4.3: Phase locked loop with injection locked oscillator (a) block diagram and (b) transient signal with power spectrum.

In order to subside the design complexity of 60 GHz divider, buffer, etc., the second PLL can be replaced by an ILO [23]. In [23], the first PLL multiplied the reference signal by 32 to provide an 11-GHz output, which was then directly injected into an ILO to generate its 5^{th} harmonic i.e. 55 GHz clock (Fig. 4.3(a)). However, this architecture suffers from a few design challenges. Firstly, with the high multiplication ratio of 5, the ILO in general suffers from a low bandwidth and a low locking range. This architecture carries a disadvantage of having no frequency acquisition loop for the ILO to ensure that the free-running frequency of ILO falls within the locking range. Secondly, there are adverse effects upon injecting the output of the PLL directly in the ILO as shown in Fig. 4.3(b). The power spectrum of the 5^{th} harmonic of the PLL output is much lower than the fundamental frequency and hence the output spectrum of ILO has high power spurs which are difficult to filter out. As a result, the output signal amplitude from ILO will be distorted. Thirdly, the large multiplication ratio of the first PLL results

in low bandwidth, and hence the free-running phase noise of VCO-1 is suppressed only at low frequencies.

4.2 Proposed architecture

From the previous solutions, it is understood that dual PLL architecture provides large bandwidth even for large multiplication ratio, but it is limited by the use of high frequency dividers. Although, PLL-ILO architecture does not require high frequency dividers, it suffers from low bandwidth and low locking range for large multiplications. So, an alternate solution for achieving a higher frequency signal with improved phase noise is proposed in this work. Instead of cascading the ILO directly with the PLL, a DLL with pulse generator is used between them to increase the pulse injection rate (Fig. 4.4).

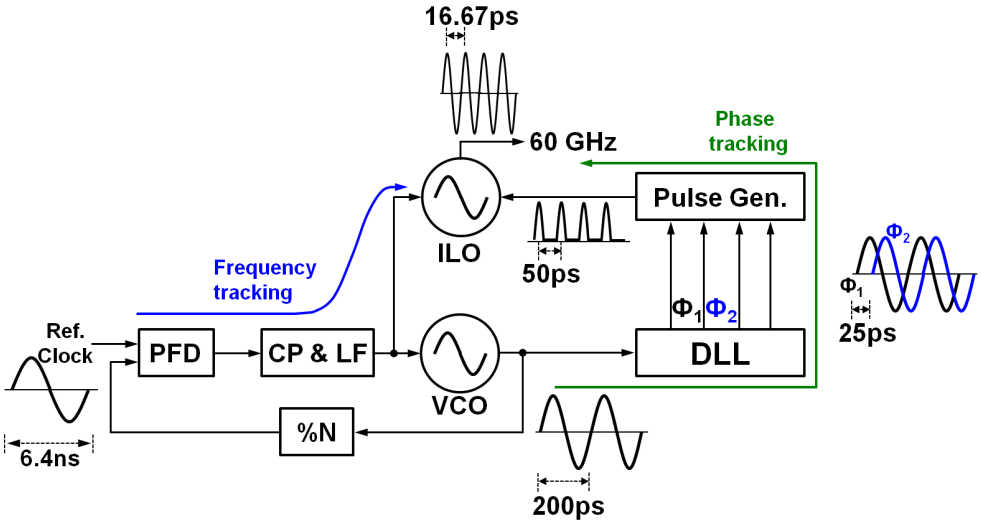


Figure 4.4: Proposed Block Diagram

In this proposed architecture, the first PLL achieves two purposes: 1) it multiplies the 156.25 MHz reference to generate 5 GHz clock; 2) using replica tuning, the first PLL centers the second VCO around 60 GHz. However, it is understood that the replica tuning does not rectify the accumulated phase noise of the second VCO. In

order to improve the phase noise issue, the VCO is injected with pulse train. A pulse generator combines these multi-phase clocks and generates a higher frequency train of pulses. This pulse train has periodicity of 50 ps, which indicates fundamental harmonic at 20 GHz. Thus, the net effect of injecting the 60 GHz VCO with this pulse train is that the free-running phase noise of VCO can be accumulated for 3 clock cycles only. Thus, the phase noise of the 60 GHz VCO can be effectively filtered up to much higher offset frequencies.

Let N_{PLL} and f_{PLL} represent the multiplication ratio and output frequency of the first PLL. If there are N_{DLL} number of delay cells and the total delay introduced by the delay line is equal to half clock cycle, i.e. 0.5 UI, then delay introduced by each cell, T_D becomes,

$$T_D = \frac{1}{2 * N_{DLL} * f_{PLL}} \tag{4.2}$$

The pulse generator generates a pulse on the rising edge of each of these phases and combines them together to form a pulse train with a pulse repetition rate, f_{pulse} of

$$f_{pulse} = \frac{2}{T_D} = N_{DLL} * f_{PLL}. \tag{4.3}$$

Thus, the DLL along with the pulse generator provides a multiplication ratio of $N_{pulse} = N_{DLL}$. The pulse train is then injected into an ILO, which generates the output frequency, f_{out} of

$$f_{out} = M_{ILO} f_{pulse} \tag{4.4}$$

$$= M_{ILO} N_{pulse} N_{PLL} f_{ref} \tag{4.5}$$

where M_{ILO} is the multiplication ratio of the ILO and f_{ref} is the reference frequency of the PLL.

In order to theoretically verify the advantages of the proposed architecture, let's focus on the phase noise characteristics of the proposed system. As explained in Chapter - 3, the output phase noise of each block is given by,

PLL :

$$S_{out-PLL} = S_{in-PLL} N_{PLL}^2 |\frac{\Phi_{out-PLL}}{\Phi_{in-PLL}}|^2 + S_{VCO} |\frac{\Phi_{out-PLL}}{\Phi_{VCO-PLL}}|^2. \tag{4.6}$$

DLL :

$$S_{out-DLL} = S_{in} N_{pulse}^2 |\frac{\Phi_{out-DLL}}{\Phi_{in-DLL}}|^2 + S_{VCDL} |\frac{\Phi_{out-DLL}}{\Phi_{VCDL}}|^2. \tag{4.7}$$

ILO :

$$S_{out-ILO} = S_{in-ILO} M_{ILO}^2 |\frac{\Phi_{out-ILO}}{\Phi_{in-ILO}}|^2 + S_{vco-ILO} |\frac{\Phi_{out-ILO}}{\Phi_{vco-ILO}}|^2 \tag{4.8}$$

For ease of understanding, the multiplication factors are brought outside the transfer functions. Since each output phase of the DLL is responsible for generating N_{pulse} pulses at the output of pulse generator, so even though the DLL does not amplify the PLL output phase noise, phase noise is accumulated (by ${N_{pulse}}^2$ times) at the output of the pulse generator. For the cascaded system, these functions can be combined as:

$$\begin{aligned} S_{out-ILO} = {} & S_{ref} \left|\frac{\Phi_{out-PLL}}{\Phi_{in-PLL}}\right|^2 \left|\frac{\Phi_{out-DLL}}{\Phi_{in-DLL}}\right|^2 \left|\frac{\Phi_{out-ILO}}{\Phi_{in-ILO}}\right|^2 \\ & + S_{vco-PLL} \left|\frac{\Phi_{out-PLL}}{\Phi_{vco}}\right|^2 \left|\frac{\Phi_{out-DLL}}{\Phi_{in-DLL}}\right|^2 \left|\frac{\Phi_{out-ILO}}{\Phi_{in-ILO}}\right|^2 \\ & + S_{VCDL} \left|\frac{\Phi_{out-DLL}}{\Phi_{VCDL}}\right|^2 \left|\frac{\Phi_{out-ILO}}{\Phi_{in-ILO}}\right|^2 \\ & + S_{vco-ILO} \left|\frac{\Phi_{out-ILO}}{\Phi_{vco-ILO}}\right|^2 \end{aligned} \tag{4.9}$$

Let the bandwidth of the PLL, DLL and ILO be f_{PLL}, f_{DLL} and f_{ILO} respectively. Table. 4.1 shows the dominant noise component for each frequency regions. Compared to PLL-ILO architecture in [23], for a given PLL, the proposed architecture relaxes the multiplication ratio for the ILO. Thus, ILO bandwidth can be kept much larger for filtering its accumulated free running phase noise at lower frequencies.

In order to choose the multiplication ratio of each block, the effect of ILO multiplica-

Table 4.1: Break down of output phase noise

Freq. Offset	S_{out}
$f < f_{PLL}$	$S_{ref}N_{PLL}^2N_{pulse}^2M_{ILO}^2$
$f_{PLL} < f < f_{DLL}$	$S_{vco-PLL}N_{pulse}^2M_{ILO}^2$
$f_{DLL} < f < f_{ILO}$	$S_{VCDL}N_{pulse}^2M_{ILO}^2$
$f > f_{ILO}$	$S_{vco-ILO}$

tion factor on its's output jitter was studied by behavioral simulation in Simulink. The phase domain model of each block is explained and verified earlier in Chapter 3. The output frequency of the PLL, f_{PLL} was set at 5 GHz and the free-running frequency of the ILO was set at 60 GHz. The ILO was injected by narrow pulses generated by pulse generator from 5 GHz PLL output. Let f_{pulse} be the pulse repetition rate. When f_{PLL} was given a frequency shift from 5 GHz to 5.1 GHz, the frequency dithering of ILO was observed for three different cases :

- The pulse generator provided no multiplication, i.e. $f_{pulse} = f_{PLL}$. When locked, the ILO provided 12 times multiplication with output frequency, f_{out} of 61.2 GHz.
- Pulse repetition rate of ILO's injection was increased by 4 times while ILO's multiplication ratio was reduced to 3. There was still a frequency offset between the steady-state and free-running ILO frequency.
- The multiplication ratio of ILO was set at 3 and $f_{pulse} = 4 * f_{PLL}$, but the change in PLL frequency was tracked by the ILO. This means that the ILO's free-running frequency has now shifted from 60 GHz to 61.2 GHz with no frequency offset.

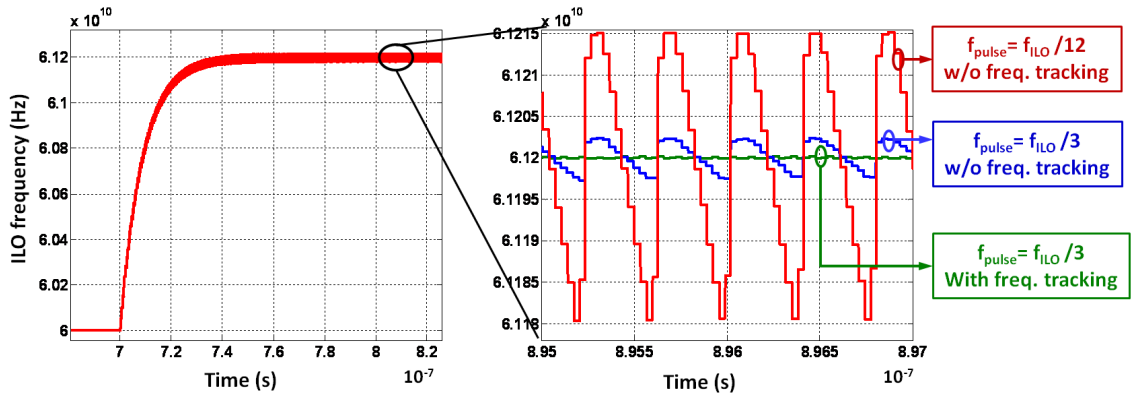


Figure 4.5: Effect of multiplication ratio and frequency tracking on ILO's frequency dithering.

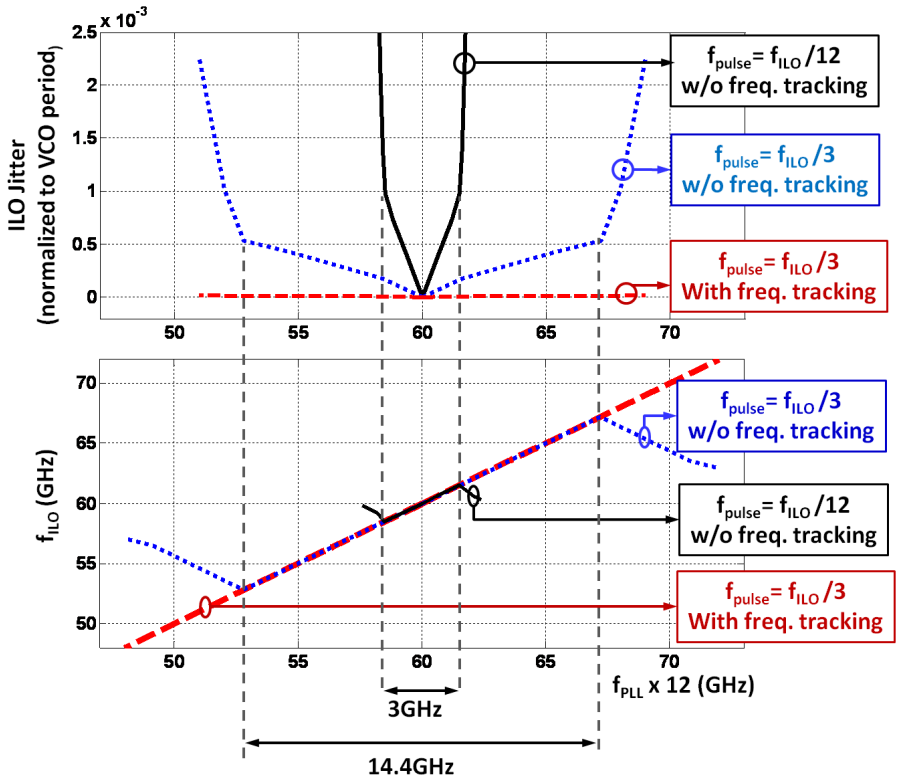


Figure 4.6: Effect of multiplication ratio and frequency tracking on ILO's lock range and jitter.

Referring to Fig. 4.5, the ILO tracks the frequency shift in its input and settles at 61.2 GHz. It was observed that when the injected pulse rate was increased from 5 GHz to 20 GHz, the dithering in the ILO's output frequency decreased significantly. When frequency tracking of ILO was added, the frequency dithering improved even further. The dithering in frequency represents the jitter at the output and so reduced dithering means improved noise performance.

As expected, decreasing the multiplication ratio from 12 to 3, the locking range increased from 3 GHz to 14.4 GHz as shown in Fig. 4.6. Also within the locking range, the jitter increases proportionally with frequency offset. So, even with a small multiplication ratio, the optimum locking range is limited by the jitter. On the other hand, when frequency tracking of ILO was added, the locking range is only limited by the tuning range of the 60 GHz VCO.

For implementing the proposed architecture, the 156.25 MHz reference signal was multiplied to 60 GHz by choosing $N_{PLL} = 32$, $N_{pulse} = 4$ and $M_{ILO} = 3$. Frequency tracking was implemented by replica-tuning approach which is explained in Chapter 5.

5 Implementation of 60 GHz Frequency Synthesizer

The proposed 60 GHz frequency synthesizer architecture (Fig. 5.1) was mentioned in the previous chapter along with explaining its advantages theoretically and with behavioral simulations. This chapter mainly focuses on the implementation of the proposed architecture in transistor level using 0.13 um CMOS technology.

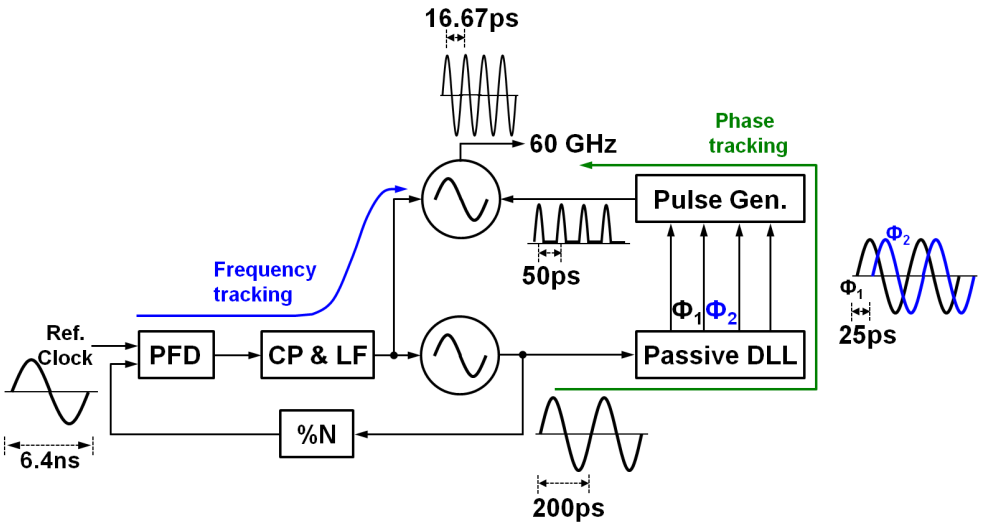


Figure 5.1: Proposed 60 GHz frequency synthesizer block diagram

5.1 5 GHz PLL and replica frequency tracking

The PLL consists of a phase/frequency detector (PFD), charge pump (CP), loop filter (LF), a 5 GHz voltage controlled oscillator (VCO) and a divide-by-32 divider. Combi-

nation topology was used for the 5 GHz VCO design. PFD and CP were implemented as described in [15] and dividers are implemented as flip-flops with feedback to obtain a division of $2^5 = 32$. Resistance, R, and capacitance, C, in the loop filter are chosen to achieve phase margin of greater than 65 degrees. The transient plots of PLL's control voltage, reference signal, V_{ref}, and divided output signal, V_{div}, is shown in Fig. 5.2. Initially, the reference and the divided output were not in phase. When the PLL locked, the control voltage settled to 1V and the two signals were in-phase.

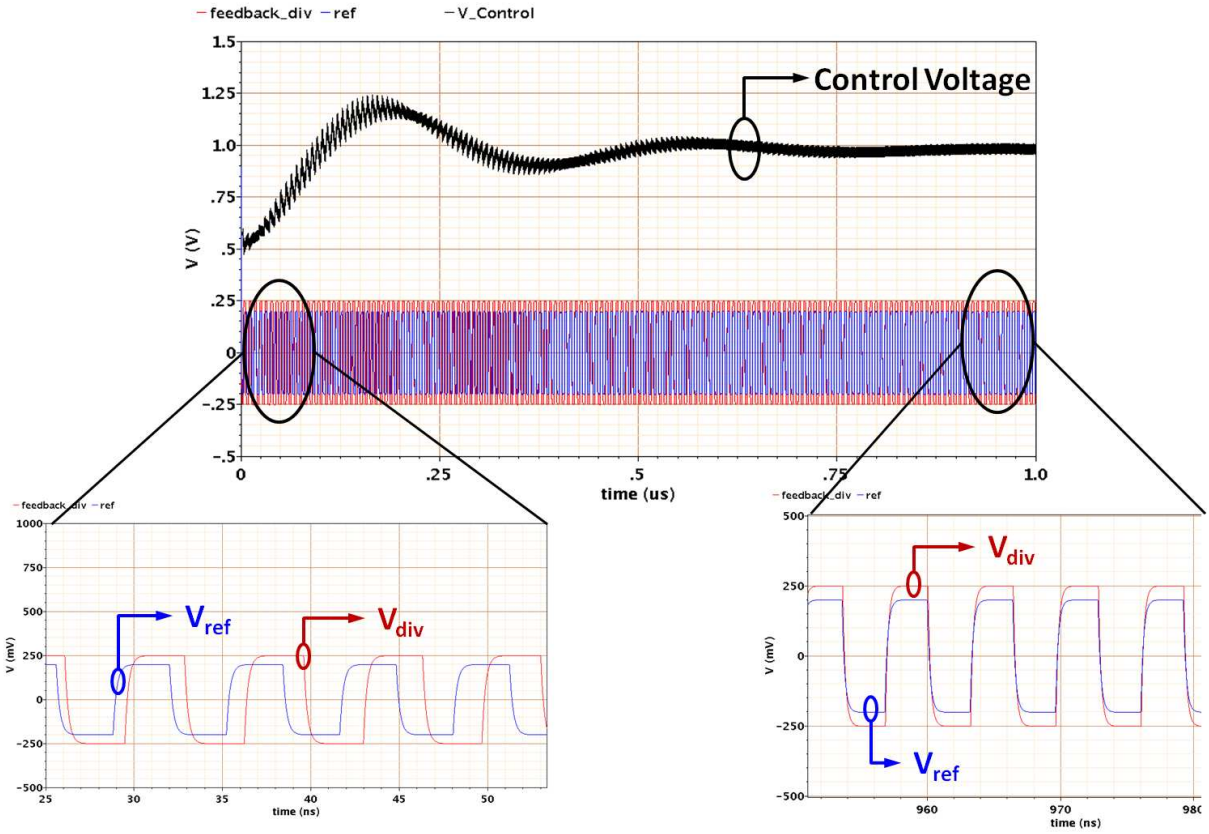
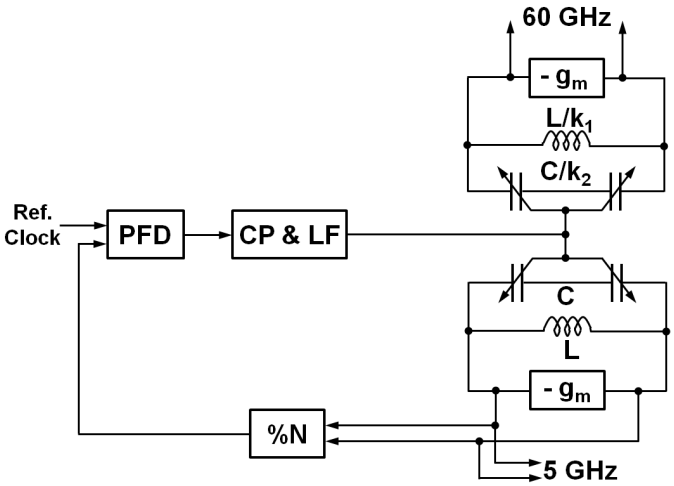
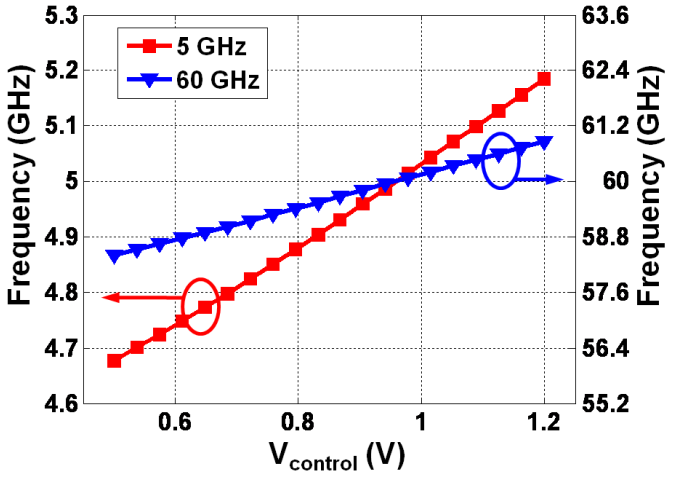


Figure 5.2: Simulated transients of PLL

While locked, the control voltage of the first VCO converges to a value such that the oscillation frequency is 5 GHz. The inductance and capacitance values of the 5 GHz VCO was chosen to be approximately 1 nH and 1 pF respectively. Due to replica



(a)



(b)

Figure 5.3: (a) Frequency Tracking of the VCOs with $k_1 = 24$ and $k_2 = 6$ (b) Simulated frequency tuning curve for 5 GHz and 60 GHz VCO

tuning, this control voltage also brings the second VCO to 60 GHz as shown in Fig. 5.3(b). Replica tuning can be achieved by scaling both capacitance and inductance by a factor, k, and as a result the resonant frequency scales up by the same factor. For example, to achieve 60 GHz oscillation, both L and C can be scaled by 12 which results

in 83.33 pH and 83.33 fF. Note that parasitic capacitance does not scale accordingly and as a result, the tuning range over process corner and temperature is insufficient. To overcome this limitation, the capacitance is only scaled by 6, and hence the inductance has to be scaled by 24 to achieve 12 times the oscillation frequency, as shown in Fig. 5.3. This reduces the L/C ratio, degrades the quality factor, and phase noise performance becomes poor for the 60-GHz VCO. However, in the proposed implementation, this is not an issue since we are achieving wider tracking bandwidth to filter it out.

5.2 DLL with pulse generation

5.2.1 Delay locked loop

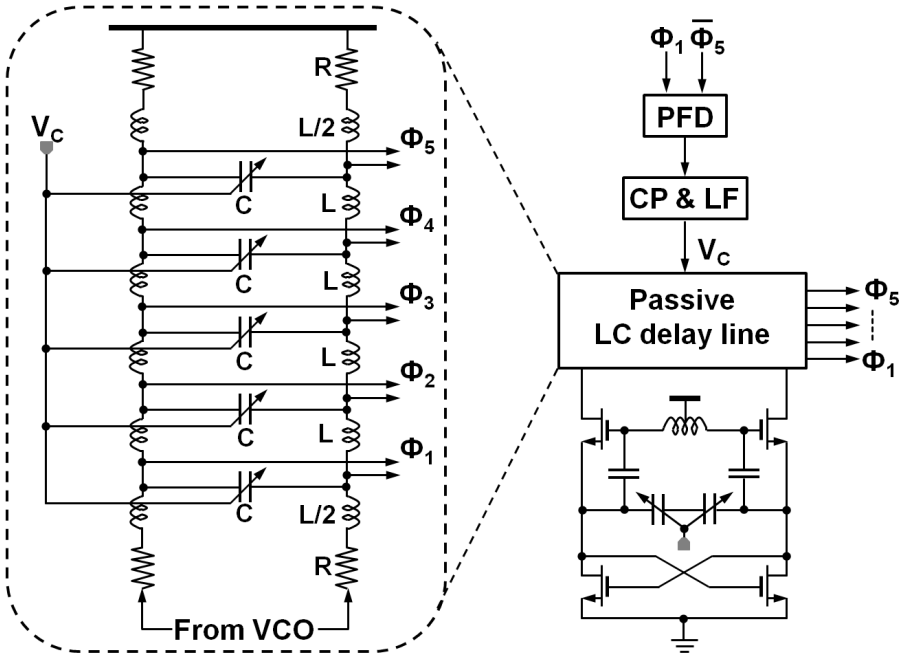


Figure 5.4: 5GHz VCO with passive DLL

Delay locked loops consists of a delay line, phase detector, charge pump and loop filter. Conventionally, active delay lines using buffers as delay cells are commonly used. For high frequency operations and better supply noise rejection, current mode

logic (CML) buffers are preferred over CMOS buffers but at the cost of higher power consumption. In this work, passive delay lines are used to save power. The passive delay line was stacked on top of the 5 GHz VCO as shown in Fig. 5.4. The delay introduced by each stage of the differential LC delay line is given by:

$$T_D = \sqrt{LC} \tag{5.1}$$

where L and C are the inductance and capacitance of each stage of the delay line[24].

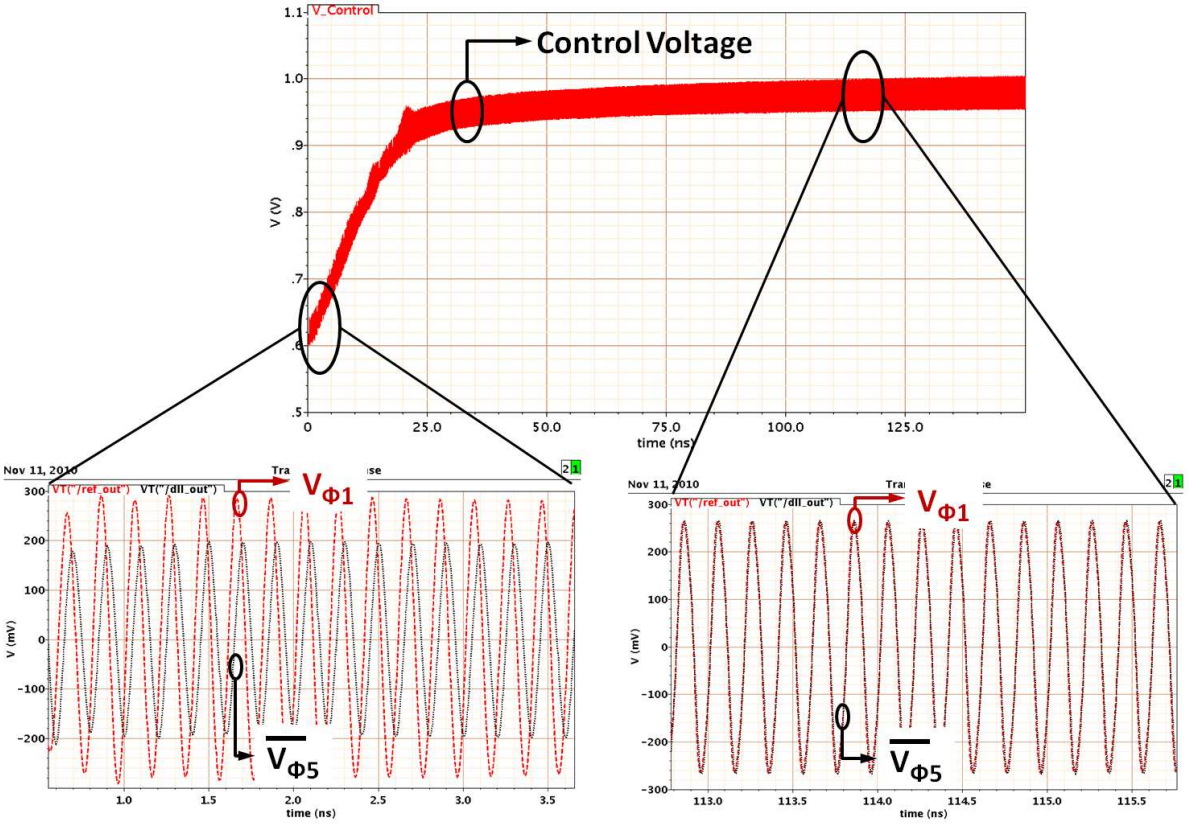


Figure 5.5: Simulated transients of DLL

In order to account for any mismatch in the delay line, the outputs of the first ϕ_1, and the last ϕ_5 delay stages were compared in the phase detector (PD), and integrated by the charge pump and loop filter to generate a control voltage, V_C. This control voltage

controlled the capacitance, C, of the varactor such that the total delay introduced by the delay line was equal to half a clock cycle, i.e., 100 ps. For achieving a delay of 25 ps by each delay stage, the L was chosen to have a value of 1.25 nH and C was kept around 469.2 fF. The resistance R was kept identical to the characteristics impedance, Z_o, of the delay line [24] which is equal to

$$Z_o = \sqrt{\frac{L}{C}}. \tag{5.2}$$

The output of the delay line, ϕ_1 to ϕ_4, are then inserted in the pulse generator. Simulated transient plots of the DLL's input, $V_{\Phi 1}$, and output $\overline{V_{\Phi 5}}$ are shown in Fig. 5.5 for both locked and unlocked conditions.

5.2.2 Pulse Generator

The pulse generator generates narrow pulses at the rising and falling edges of the 5 GHz input signal. This can easily be done by XOR-ing two consecutive outputs of the DLL. Unfortunately, CML XOR consumes additional power with DC offsets and a CMOS XOR gate in 0.13um process fails to operate at 10 GHz frequency. In our solution, multiple CMOS NAND gates were used to perform XOR operations, as shown in the timing diagram of Fig. 5.6. The first two outputs of DLL, ϕ_1 and ϕ_2, and their complements, $\overline{\phi_1}$ and $\overline{\phi_2}$, were NAND-ed to get the signals P and Q. These two NAND gates (Fig. 5.7(b)) need not be oversized since they only need to operate at low frequencies.

With a similar idea, the signals R and S was generated using the last two output phases. $P-Q$ and $R-S$ were NAND-ed again using symmetrical NAND gates to obtain the 10 GHz signals, X and Y. Their outputs were then combined together using the edge combiner which generates a 20 GHz output current, i_L (Fig.5.7(c)). Since these gates need to operate at high frequency, the transistors were sized accordingly.

Note that the pulse generator circuit is CMOS whereas the passive DLL output common mode is set by the VCO. To overcome this issue, an AC coupled CML-CMOS converter is used as shown in Fig. 5.7(a). Simulated transients of the DLL output phases and the pulse generator current is shown in Fig. 5.8.

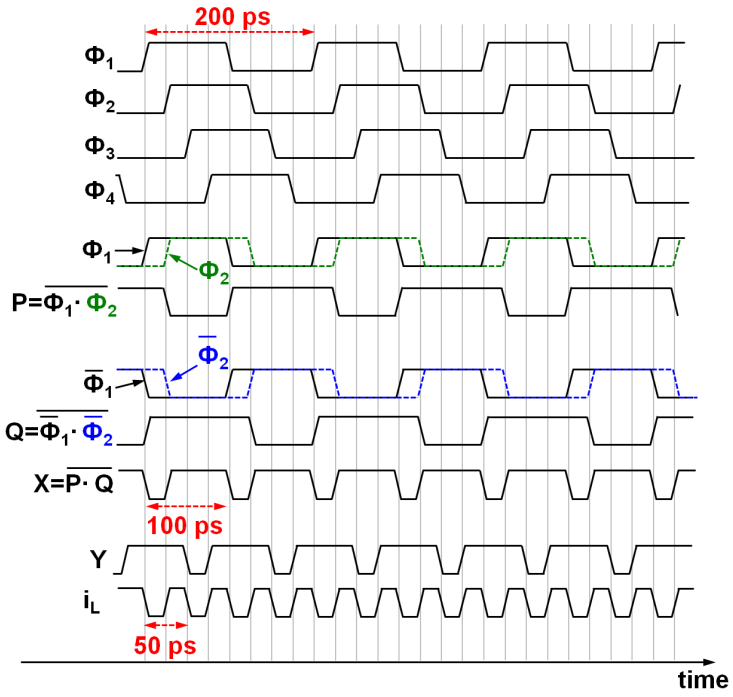
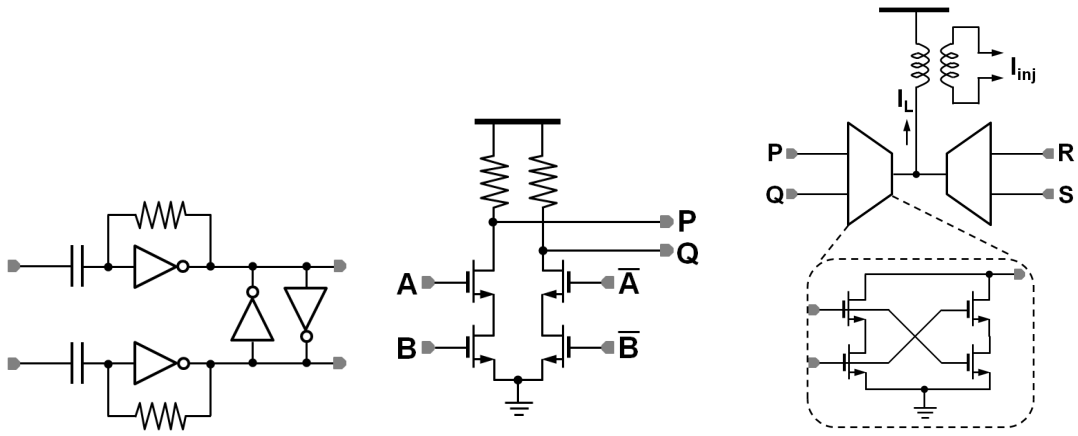


Figure 5.6: Timing diagram of pulse generation.



(a) (b) (c)

Figure 5.7: (a) CML to CMOS converter, (b) AND gate and (c) Edge Combiner.

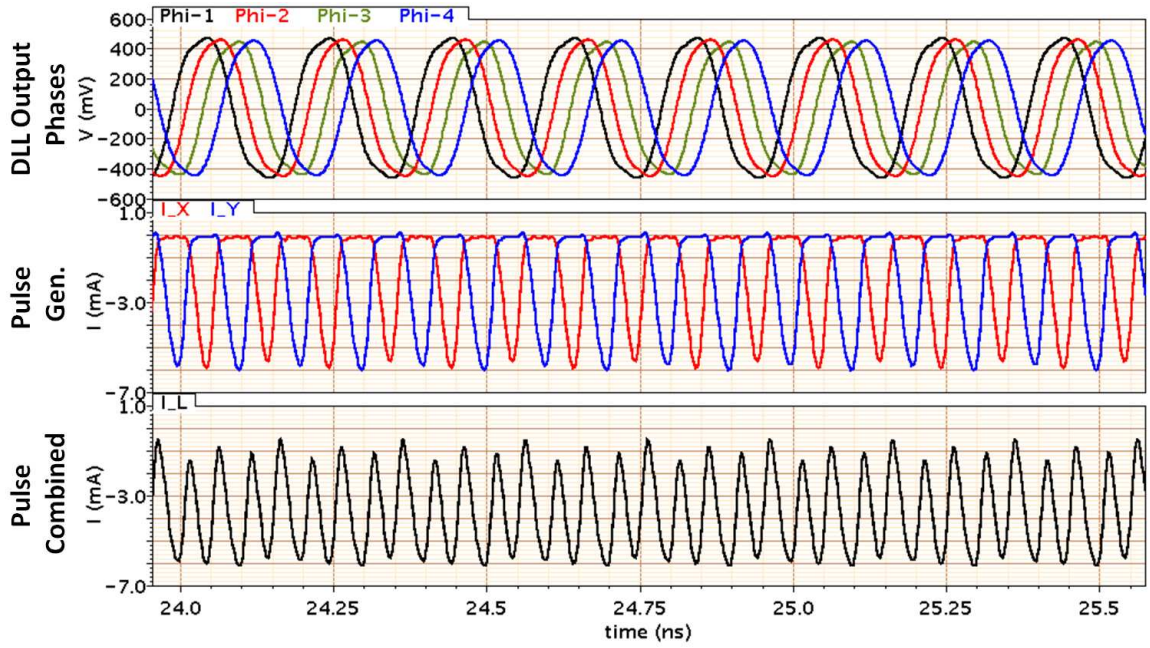
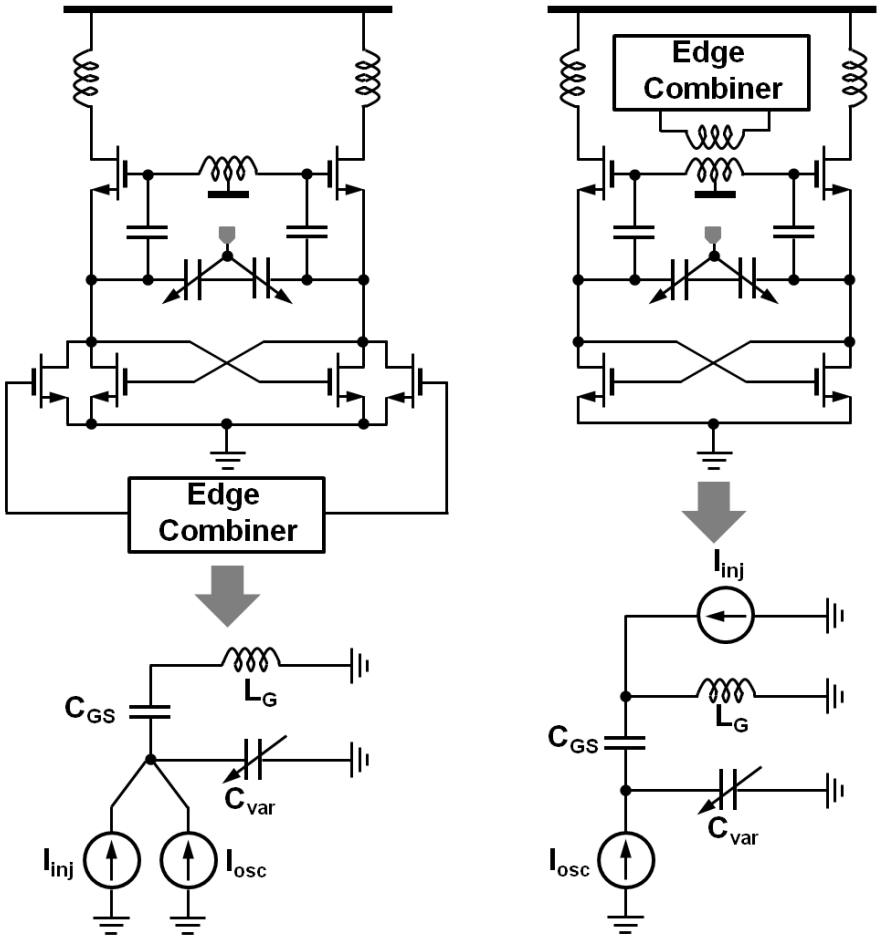


Figure 5.8: Simulated transients of pulse generation.

5.3 Injection Locked Oscillator

The 20 GHz sub-rate pulse train generated from the DLL and edge combiner is injected into the injection locked oscillator(ILO). The ILO oscillates at 60 GHz center frequency which is the 3^{rd} harmonic of its input.

There are two possible techniques of injections using an ILO. The first conventional method is active injection, i.e., a differential amplifier can be used to inject the pulse train into the VCO (Fig. 5.9(a)) [25]. Using this conventional method leads to three limitations: 1) loading the critical nodes with additional capacitance of the differential pair leaves small tuning range; 2) the injection strength K is limited by the gain of the differential stage, g_m, which is relatively low at 20 GHz; 3) lastly, the differential pair used for injection consumes additional power. Hence, we consider the alternative method, which is to use passive injection using transformer coupling as shown in Fig. 5.9(b). This implementation results in reduced loading in the critical node, improves



(a) (b)

Figure 5.9: Injection Locked Oscillator and its equivalent half-circuit with (a) active injection and (b) passive injection

the injection strength [26], and it is more power efficient.

The effect of improved injection strength can be shown using the equivalent half circuit of the two methods of injections. For active injection, the injection strength is given by $K = I_{inj}/I_{osc}$. For passive injection, the injection strength can be derived to

be [13]

$$K = \frac{I_{inj}}{I_{osc}}(1 + \frac{C_{var}}{C_{GS}}). \tag{5.3}$$

Thus, passive injection allows high injection strength and wider lock range. The simulated transient plot of ILO is shown in Fig. 5.10. Initially when the ILO was not injected, i.e. $I_L = 0$, the ILO was oscillating at its free-running frequency. Note that when injection current, I_L, was added, the ILO's phase locked to it. The tank current is represented as I_{inj}.

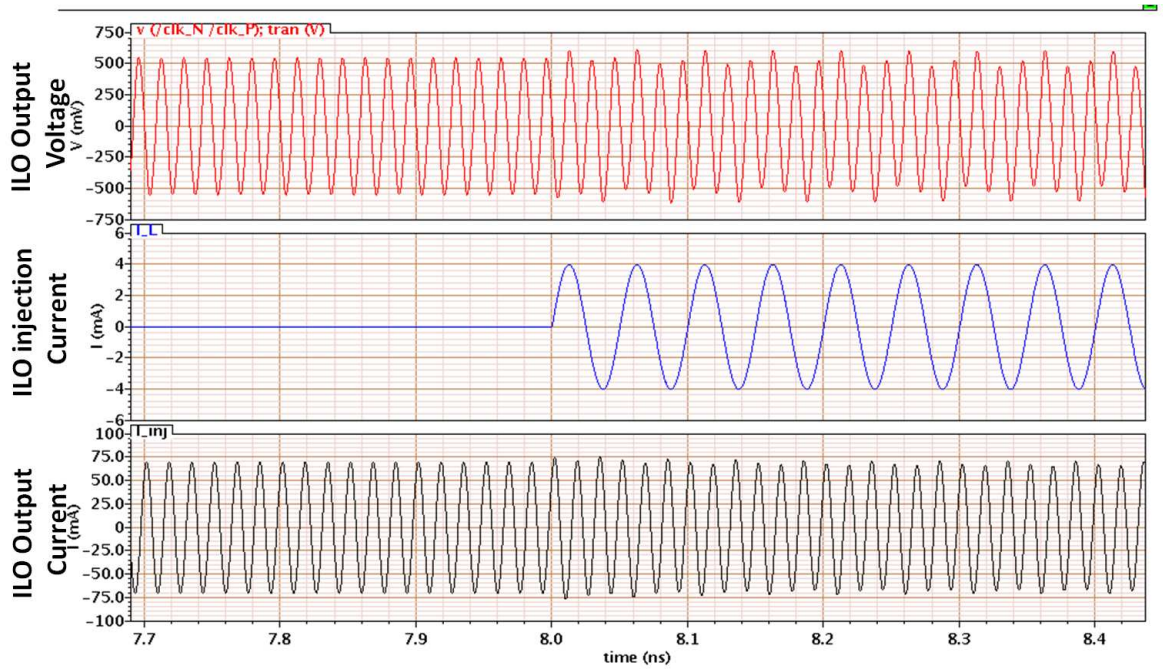


Figure 5.10: Simulated transients of ILO

5.4 Overall performance

The total power consumed by the synthesizer is 57 mW. The power breakdowns are shown in Table 5.1. For phase noise comparison, three types of frequency synthesizers

Table 5.1: Power Summary

Component	Current	Voltage	Power
5 GHz VCO with passive delay line	7.11 mA	1.2 V	8.53 mW
60 GHz ILO	10 mA	1.2 V	12 mW
Pulse Generation	12 mA	1.2 V	14.4 mW
PFD,CP and Divider	10 mA	1.2 V	12 mW
CML to CMOS Converter and Buffers	8 mA	1.2 V	9.6 mW

were simulated to generate 60 GHz clock from 156.25 MHz reference signal (Fig. 5.11). For single PLL architecture, due to its large multiplication ratio, the bandwidth of the PLL was small, around 1.53 MHz. The output phase noise followed the reference phase noise, S_{ref}, which was amplified by $20log(60GHz/156.26MHz) = 52$ dB, up to the bandwidth of reference signal. After which, it followed the free-running phase noise of the 60 GHz VCO, $S_{vco-60GHz}$. The output phase noises of the 60-GHz signal were -87 dBc/Hz @ 1 MHz, -105 dBc/Hz @ 10 MHz, and -118 dBc/Hz @ 40 MHz.

Compared to single PLL, dual PLL allows the flexibility of optimizing the bandwidth to lower the output phase noise. For simulation of the dual PLL architecture, the first and the second PLL operated at 5 GHz and 60 GHz with a bandwidth of 2.5 MHz and 20 MHz respectively. Due to the inductor scaling of the VCOs, the quality factor and the free-running phase noise of the 60 GHz VCO, $S_{vco-60GHz}$, were much poorer than that of 5 GHz VCO,$S_{vco-5GHz}$, as shown in Fig. 5.11. At frequency offset of less than 2.5 MHz, the 60 GHz output phase noise followed that of the S_{ref} amplified by 52 dB. For frequencies up to 20 MHz, the $S_{vco-5GHz}$, amplified by $20log(60GHz/5GHz) = 21$ dB, dominated the output. Beyond that, it followed the $S_{vco-60GHz}$. For this design, the output phase noises were -98 dBc/Hz @ 1 MHz, -111 dBc/Hz @ 10 MHz, and -118.5 dBc/Hz @ 40 MHz.

In the proposed approach, 60 GHz VCOs phase noise was filtered more efficiently which further improves overall phase noise of the synthesizer. The design of the first PLL was identical to the one in the dual-PLL architecture. But the second PLL was replaced by a DLL, a pulse generator, and an ILO. Since DLL does not accumulate

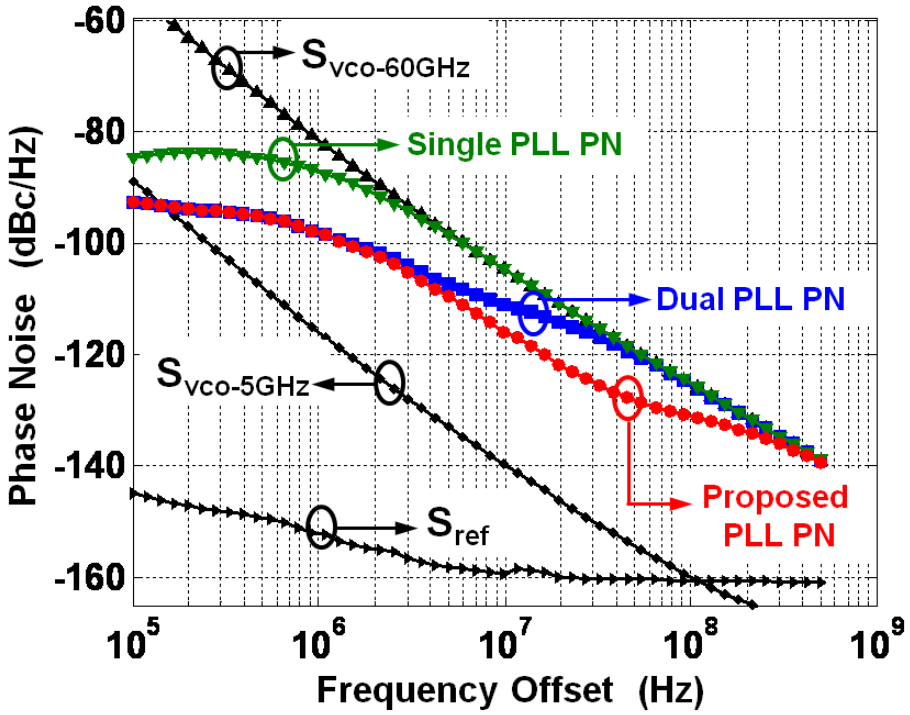


Figure 5.11: Output Phase Noise

phase noise, its contribution to the overall phase noise is negligible. In our design, the ILO provided a multiplication factor of 3, and had a bandwidth of 200 MHz. Similar to the dual-PLL design, the output phase noise followed the amplified S_{ref} up to 2.5 MHz. But in this design, the ILO had a much larger bandwidth upon comparing to the second PLL in the dual-PLL architecture. Hence, the free-running phase noise of the 60 GHz VCO was filtered to much higher frequencies. This led to a significant output phase noise improvement between 10 and 100 MHz. The output phase noises for our proposed architecture were -98 dBc/Hz @ 1 MHz, -117 dBc/Hz @ 10 MHz, and -128 dBc/Hz @ 40 MHz.

Table 5.2: Performance Summary

	[18]	[19]	[20]	[27]	[28]	[23]	**This Work**
Process	CMOS 90nm	CMOS 130 nm	CMOS 90 nm	Bi CMOS $0.13\mu m$	Bi CMOS $0.25\mu m$	CMOS $0.18\mu m$	CMOS 130 nm
Synthesizer Output (GHz)	61.1 – 63.3	45.9 – 50.5	58 - 60.4	56.5 - 63	50 - 53	53 – 58	60
Freq. Synth. Architecture	PLL	PLL	PLL	PLL + Tripler	PLL + Freq. Doubler	PLL +ILO	PLL + Pulse Gen. +ILO
Multiplication Ratio F_{out}/F_{ref}	$\frac{62GHz}{60MHz}$	—	$\frac{60GHz}{230MHz}$	$\frac{63GHz}{285.7MHz}$	$\frac{53GHz}{262MHz}$	$\frac{55GHz}{350MHz}$	$\frac{60GHz}{156.25MHz}$
Power	78mW	57mW	80mW	144mW	160mW	35mW	57mW
VDD	1.2V	1.5 / 0.8 V	1.2 V	1.2 / 2.7V	2.5 V	1.8 V	1.2 V
Phase Noise (dBc @Hz)	-72@100K -80@1M	-64@50K -72@1M	-85@1M -99@10M	**For 16G:** -90@100K -124@10M	-73@100K -81@1M -102@10M	-85.2@1M -90.9@10M	-98@1M -117@10M -128@40M

Performance comparisons among the proposed 60-GHz frequency synthesizer and some recent work are summarized in Table 5.2. Upon comparing to traditional PLL-based solutions, our work offers several advantages. Firstly, the ILO offers larger operating bandwidth than the PLL, and this feature filters out more phase noise of the VCO. Secondly, our architecture removes the need to design a 60-GHz divider. This divider-less DLL-ILO based architecture is more power efficient. Due to its architectural advantage, the performance of this synthesizer is comparable to the one implemented in better process technology such as BiCMOS [27]. Besides, this architecture solves the problem of having spurs due to the injection of output signal of PLL directly into the ILO as discussed in [23]. Moreover, the proposed frequency tracking further decreases the noise and improves the locking range of the ILO. In summary, our proposed architecture offers an elegant design of a low power high frequency synthesizer without sacrificing any phase noise performance.

6 Fractional N Phase Locked Loop

In Chapter 4 and 5, it was shown how the proposed synthesizer can be used to generate 60 GHz clock. But in order to use this synthesizer for wireless personal area networks (WPANs), the synthesizer needs to have tuning properties to allow channel selection. This can be achieved by a simple modification to the existing solution as shown in Fig. 6.1. The first 5 GHz integer PLL can be replaced with a fractional PLL with the remaining pulse generator and ILO unchanged. The only difference between the fractional and integer PLL is that the fractional PLL uses a fractional divider instead of an integer divider. The fractional divider needs to provide a division resolution,ΔN, of 0.0848 such that the output of the PLL has a tuning range of 4.84 GHz to 5.41 GHz with a frequency resolution, Δf of 13.25 MHz.

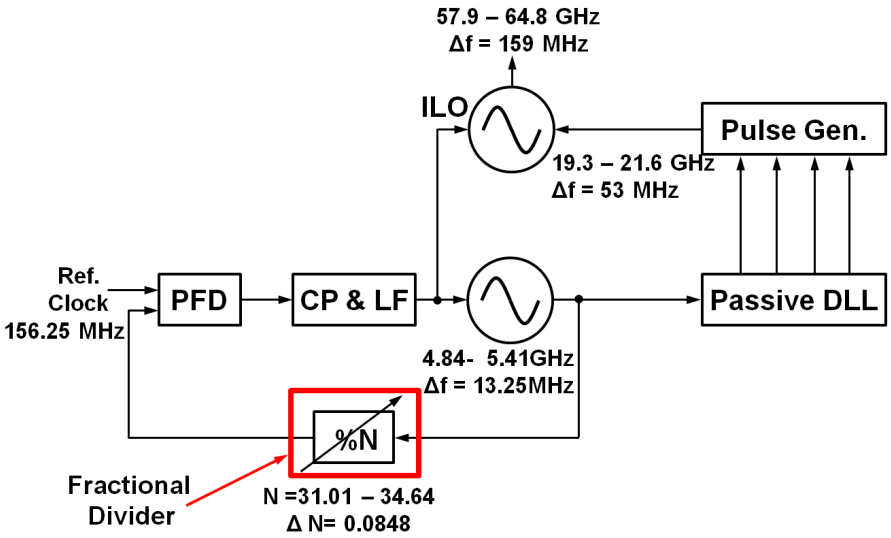


Figure 6.1: Proposed 60 GHz frequency synthesizer with tuning properties

Passive DLL detects output frequency of the VCO and accordingly tunes the delay

of its passive delay cells such that each delay cell provides a delay of 1/8 UI. From these output phases, the pulse generator generates a pulse with a frequency of 4 times that of its input frequency. Hence, the DLL together with the pulse generator provides a pulse train with a frequency of 19.3 GHz to 21.6 GHz depending on its input signal with a frequency resolution of 53 MHz.

The main problem of this architecture is the injection locked oscillator. As mentioned in Chapter 3, the ILO has a smaller locking range which decreases further with multiplication ratio. So it is very difficult to design an ILO which would lock to any frequency from 19.3 GHz to 21.6 GHz and provide an exact 3 times multiplication. Fortunately, in the proposed architecture, the replica tuning of the VCOs take care of the frequency tracking. So when the frequency of oscillation of the 5 GHz VCO changes, the free running oscillation frequency of the ILO also changes accordingly shifting the locking range and hence the frequency of the pulse train would always fall within locking range of the ILO. Hence the proposed frequency synthesizer provides tunability to cover all the channels mentioned by the IEEE 802.15.3c standard for both HRP and LRP transmission as shown in Table 6.1 and Table 6.2. Hence by changing the division ratio of the first PLL,N_{PLL} only, the frequency synthesizer can be tuned to any of the channels.

Table 6.1: Channel Selection for HRP Channels

CHNL ID / HRP	f_{ref}**(MHz)**	N_{PLL}	N_{pulse}	M_{ILO}	f_{OUT} (GHz)
1	156.25	31.104	4	3	58.320
2	156.25	32.256	4	3	60.480
3	156.25	33.408	4	3	62.640
4	156.25	34.560	4	3	64.800

This chapter would mainly focus on the Fractional PLL. A literature review of the existing solutions of frac-N PLL is presented in Section 6.1. A method to eliminate their limitations is proposed in Section 6.2. Due to lack of time and resource, the proposed PLL could not be simulated in Cadence. Only behavioral study was done using MATLAB Simulink and the simulation results are given in Section 6.3. The work is concluded in Section 6.4.

Table 6.2: Channel Selection for LRP Channels

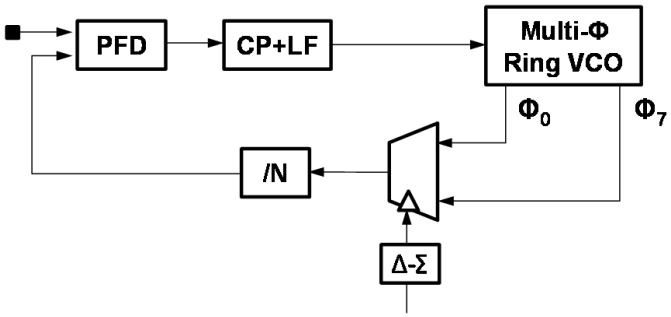
CHNL ID	**HRP**	**LRP**	f_{ref}**(MHz)**	N_{PLL}	N_{pulse}	M_{ILO}	f_{OUT} (GHz)
1		1	156.25	31.0192	4	3	58.161
5	1	2	156.25	31.104	4	3	58.320
9		3	156.25	31.1888	4	3	58.479
2		1	156.25	32.1712	4	3	60.321
6	2	2	156.25	32.256	4	3	60.480
10		3	156.25	32.3408	4	3	60.639
3		1	156.25	33.3232	4	3	62.481
7	3	2	156.25	33.408	4	3	62.640
11		3	156.25	33.4928	4	3	62.799
4		4	156.25	34.4752	4	3	64.641
8	4	4	156.25	34.560	4	3	64.800
12		4	156.25	34.6448	4	3	64.959

6.1 Review of fractional-N PLLs

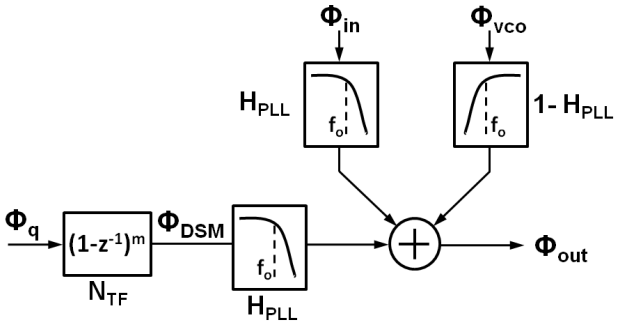
Conventionally, as shown in Fig. 6.2(a), fractional division can be implemented using a phase interpolator (PI). The phase interpolator is inserted between the VCO and the divider to select among different output phases going into the divider. Consequently, alternate output frequencies can be generated [29, 30]. However, the phase selection operation introduces quantization noise. To mitigate this problem, the phase selection can be controlled by a modulator, which randomizes the phase selection in the interpolator such that the quantization noise is shaped at higher frequencies. Generally, the delta-sigma ($\Delta\Sigma$) modulator is used.

A simplified phase noise model of the PI-based frac-N PLL is shown in Fig. 6.2(b). The input phase noise transfer function is represented by H_{PLL}, which is a low pass transfer function with bandwidth f_o [15]. Similarly, the VCO noise transfer function can be represented by a high pass function, $1 - H_{PLL}$, with the cut-off bandwidth at f_o. Thus, the input phase noise of the PLL, Φ_{in}, is low-pass filtered, and the VCO free-running phase noise, Φ_{VCO}, is high-pass filtered. The quantization noise due to the phase selection is Φ_q, which passes through the $\Delta\Sigma$ modulator with transfer function, N_{TF}, and is shaped into high frequency noise. Then, this high frequency

quantization noise is filtered out by H_{PLL} beyond f_o. This shows the trade-off between the quantization noise and VCO phase noise. That is, a narrow PLL bandwidth is preferred to filter out quantization noise, while a wide bandwidth is preferred to reduce the VCO free-running phase noise.



(a)

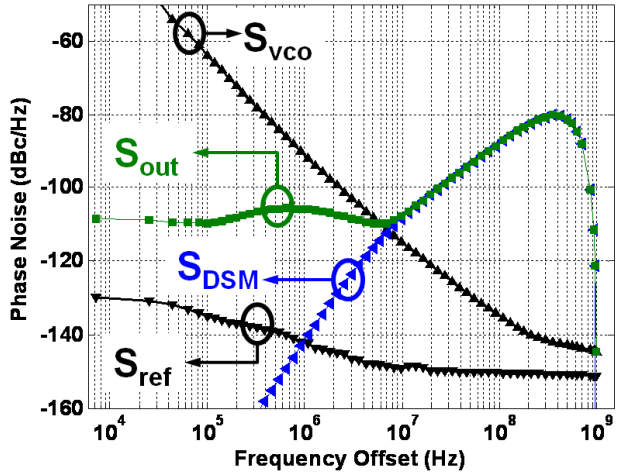


(b)

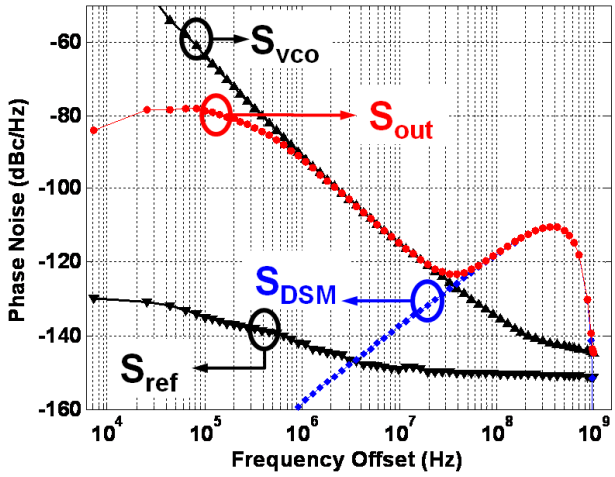
Figure 6.2: Phase Interpolator based frac-N PLL: (a) block diagram, (b) parameterized phase noise model.

To understand this limitation, a model of the PI-based frac-N PLL has been simulated in Simulink, and the results are plotted in the Fig. 6.1. The reference, the VCO free-running, and the output phase noises are represented by S_{ref}, S_{vco}, and S_{out}, respectively. The quantization phase noise of the $\Delta\Sigma$ modulator, after filtered by H_{PLL}, is denoted as S_{DSM}. As shown in Fig. 6.3(a) for wide PLL bandwidth, the output phase noise is dominated by S_{DSM} because the S_{vco} is filtered out at high frequencies. But for a narrow PLL bandwidth, phase noise due to quantization error is insignificant.

That leads to low S_{DSM}, and the S_{out} is mainly dominated by S_{vco}.



(a)



(b)

Figure 6.3: Simulation results of phase noise of PI-based frac-N PLL having (a) wide PLL bandwidth,6 MHz; (b) narrow PLL bandwidth, 0.5 MHz.

Apart from the phase noise trade-off characteristics, the PI-based frac-N PLL suffers a few other design constraints. For a given PLL bandwidth, increasing the over-

sampling ratio (OSR) of the modulator reduces quantization noise. To accomplish this, digital $\Delta\Sigma$ modulator is clocked at higher frequency. Technology scaling makes it achievable. However, clocking the modulator beyond reference frequency is NOT beneficial, because the phase comparison is done by the phase detector on every clock cycle of the reference signal.

Furthermore, the frequency resolution is set by the number of available phases. For higher resolution, the VCO needs larger number of stages. Ring VCO easily generates multiple phase but gives poor phase noise performance. Although LC oscillator offers better phase noise performance, generating multiple phases from it requires additional buffers and dividers, thus consuming extra power.

6.2 Proposed Architecture

In this paper, an alternate solution for achieving fractional multiplication in a PLL without compromising phase noise and frequency resolution is presented. The block diagram of the proposed fractional PLL is shown in Fig. 6.4. The VCO output passing through a set of delay cells generates multiple phases. In order to control the delay introduced by the delay cells, a feedback loop is used in the form of a DLL. The $\Delta\Sigma$ modulator chooses an output of a delay cell for comparing in the phase detector. With varying selections, the delays introduced by the delay line vary and, hence, phase interpolated fractional division is acquired.

Suppose the input signal is $A\sin(2\pi f_{in}t)$, and the divided fractional signal is $A\sin(2\pi f_{frac}t)$, where A, f_{in}, and f_{frac} are the amplitude, the input and fractionally divided output frequencies, respectively. If at time, t_1, the PLL is in locked condition, the input phase, Φ_{IN} and divided output phase Φ_{frac} are equal:

$$\Phi_{IN}(t = t_1) = \Phi_{FRAC}(t = t_1). \tag{6.1}$$

Replacing the phase with its frequency integral, and we have

$$\begin{aligned}\int 2\pi f_{IN} dt &= \int 2\pi f_{frac} dt \\ &= \frac{1}{N}\int 2\pi f_{VCO} dt - \frac{1}{N}\int 2\pi f_{DL} dt \\ \int 2\pi N \frac{1}{T_{IN}} dt &= \int 2\pi \frac{1}{T_{VCO}} dt - \int 2\pi \frac{1}{T_{DL}} dt. \end{aligned} \tag{6.2}$$

Let M represent the ratio of the VCO period by which it is shifted by the DLL and the modulator, i.e., $T_{DL} = MT_{VCO}$. We have

$$\begin{aligned}\int 2\pi N \frac{1}{T_{IN}} dt &= \int 2\pi \frac{1}{T_{VCO}} dt - \int 2\pi \frac{1}{MT_{VCO}} dt \\ &= \int 2\pi \frac{1}{T_{VCO}} (1 - \frac{1}{M}) dt. \end{aligned} \tag{6.3}$$

By comparing the two integrals in the above equation, the output frequency of the PLL becomes

$$f_{VCO} = \frac{MN}{M-1} f_{IN}. \tag{6.4}$$

Hence by varying the value of M, fractional multiples of the input frequency can be produced at the output. M can be controlled by controlling the phase shift of VCO output by the DLL. This can be done in two ways :

1. For coarse phase shift, the MSB of the control signal selects between the output phases of the DLL.

2. For fine phase shift, the LSB's of the control signal sets the control word of the $\Delta\Sigma$ modulator. The DLL accordingly sets the delay of each delay cells and thus controlling the phase shift.

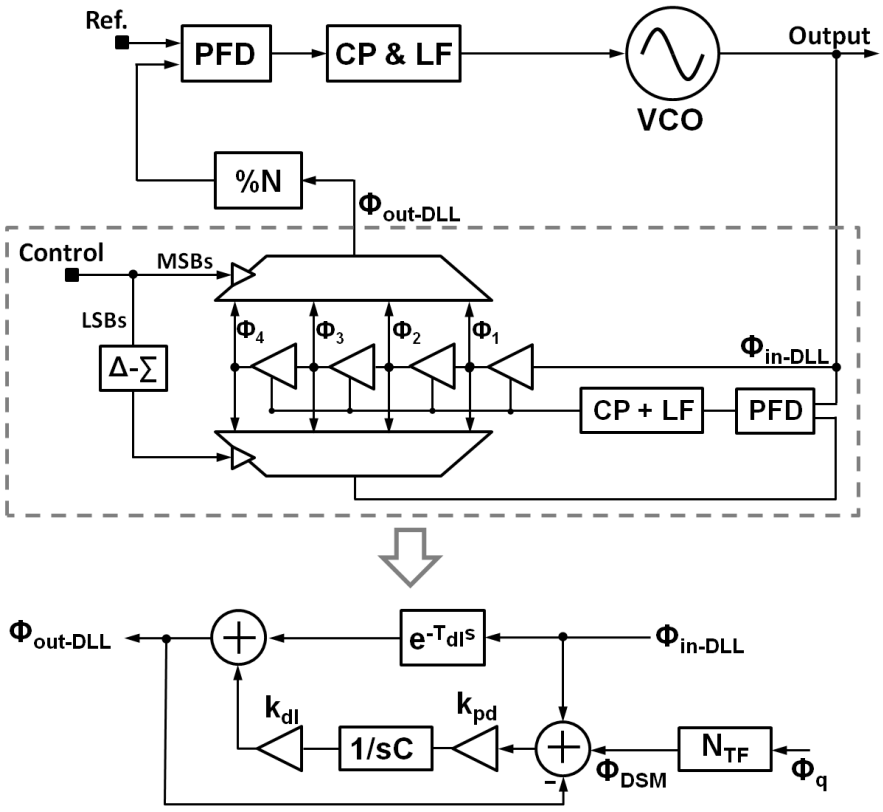


Figure 6.4: Proposed fractional PLL block diagram with equivalent phase domain model of DLL.

The main benefit of this architecture can be understood from the phase domain model. As shown in Fig. 6.4, the phase domain model of the fractional divider is very similar to that of a DLL [7] with the exception of having another input,Φ_{DSM}, in the phase detector. This is due to the phase introduced by the $\Delta\Sigma$ modulator. From this model, the following transfer functions can be derived,

$$\frac{\Phi_{out-DLL}}{\Phi_{in-DLL}} = \frac{1 + \frac{se^{-T_{dl}s}}{\omega_P}}{1 + \frac{s}{\omega_P}} \equiv H_{DLL} \tag{6.5}$$

$$\frac{\Phi_{out-DLL}}{\Phi_{DSM}} = \frac{1}{1 + \frac{s}{\omega_P}} \tag{6.6}$$

where $\omega_p = \frac{k_{pd}k_{dl}}{C}$ is the bandwidth of the DLL, k_{pd} and k_{dl} is the gain of phase detector and delay line respectively, C is the first order loop filter capacitance and T_{dl} is the total delay introduced by the delay line.

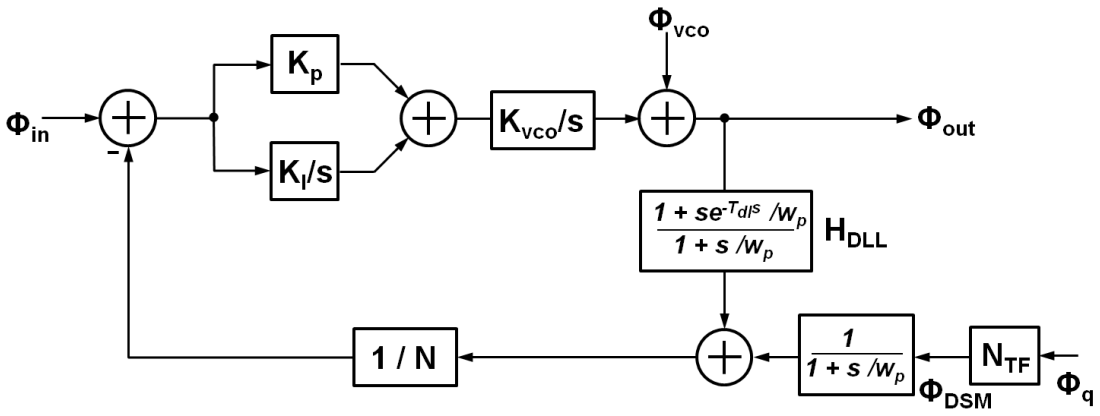


Figure 6.5: Phase model of the proposed fractional PLL

As shown in Fig. 6.5, the DLL transfer functions can be added in the phase domain model of our proposed frac-N PLL model. The input phase noise transfer function is then

$$\frac{\Phi_{OUT}}{\Phi_{IN}} = \frac{N(K_p K_{vco} s + K_I K_{vco})}{Ns^2 + H_{DLL}(K_p K_{vco} s + K_I K_{vco})} \tag{6.7}$$

And the VCO phase noise transfer function can be derived as

$$\frac{\Phi_{OUT}}{\Phi_{VCO}} = \frac{Ns^2}{Ns^2 + H_{DLL}(K_p K_{vco} s + K_I K_{vco})} \tag{6.8}$$

Correspondingly, the quantization phase noise transfer function is

$$\frac{\Phi_{OUT}}{\Phi_Q} = -\frac{1}{N} \cdot N_{TF} \cdot (\frac{1}{1 + \frac{s}{\omega_p}}) \cdot \frac{\Phi_{OUT}}{\Phi_{IN}} \tag{6.9}$$

The H_{DLL} is an all-pass function. Hence, Φ_{OUT}/Φ_{IN} has a low pass characteristics with a gain of N and Φ_{OUT}/Φ_{VCO} is a high pass function. The DLL should have no

effect on the contribution of input and VCO phase noise on the output. On the other hand, Φ_Q will be shaped to high frequencies by the modulator, N_{TF}, low pass filtered by the DLL, $(1/1 + \frac{s}{\omega_p})$ and low pass filtered by PLL, $\frac{\Phi_{OUT}}{\Phi IN}$, before contributing to the output phase noise.

The three main advantages of this architecture is summarized below:

1. Unlike PI-based frac-N PLL, there is no tradeoff between the VCO phase noise filtering and quantization noise filtering. In this architecture, the VCO phase noise filtering depends on the bandwidth of PLL which is set by k_P and k_I. The quantization noise filtering is done by the DLL which is set by the ω_P.

2. This PLL is flexible with the use of any VCO. If ring VCO is used, the PLL bandwidth may be increased to filter out the VCO free-running phase noise over a wide bandwidth. If LC VCO is used, multiple phases is generated by the delay line without consuming any extra power.

3. Since the DLL phase detector is running at full rate, OSR is no longer limited by the reference frequency of the PLL. Therefore, running the $\Delta\Sigma$ modulator at much higher clock rate than the reference is beneficial in our design.

6.3 Simulation Results

The free-running phase noise of a 5 GHz ring VCO and a 416.67 MHz reference phase noise was generated using transistor level simulation in 0.13 μm CMOS using Cadence. Using these results, the output phase noise of the phase-interpolator based and proposed frac-N PLL were simulated in Matlab. The PLL bandwidth was set at 6 MHz while DLL bandwidth was set at 2 MHz. The phase noise contributions of the VCO, S_{vco}, and the reference, S_{ref} on the output of PLL are shown in Fig. 6.6.

In conventional PI-based frac-N PLL, within the operating bandwidth of PLL, the reference phase noise was amplified by $20\log(12) = 21$ dB. Since the PLL bandwidth was kept large, S_{vco} was filtered over a wider bandwidth, but the quantization noise filtered by the PLL, $S_{DSM,conv}$ mainly dominated the output phase noise, $S_{out,conv}$.

In our proposed PLL design, the DLL filtered out the quantization noise beyond 2 MHz and thus the shaped quantization noise of the proposed architecture, $S_{DSM,prop}$, is much smaller than that of the conventional, $S_{DSM,conv}$, which was filtered by PLL beyond 6 MHz. Although within the operating bandwidth, the phase noise performances of both PLL designs were similar, but beyond the operating frequency, the proposed architecture improved the output phase noise, $S_{out,PLL}$, by as much as 40 dBc/Hz.

The PI-based frac-N PLL, and our proposed frac-N PLL were modeled and simulated in Simulink. In simulations, both PLLs had the identical reference signals and output frequencies. In both cases, the phase interpolation between two phases had identical phase shift. Since our interest was on the effect of quantization noise of the modulator on the output of PLL, all other noise sources were ignored in simulations.

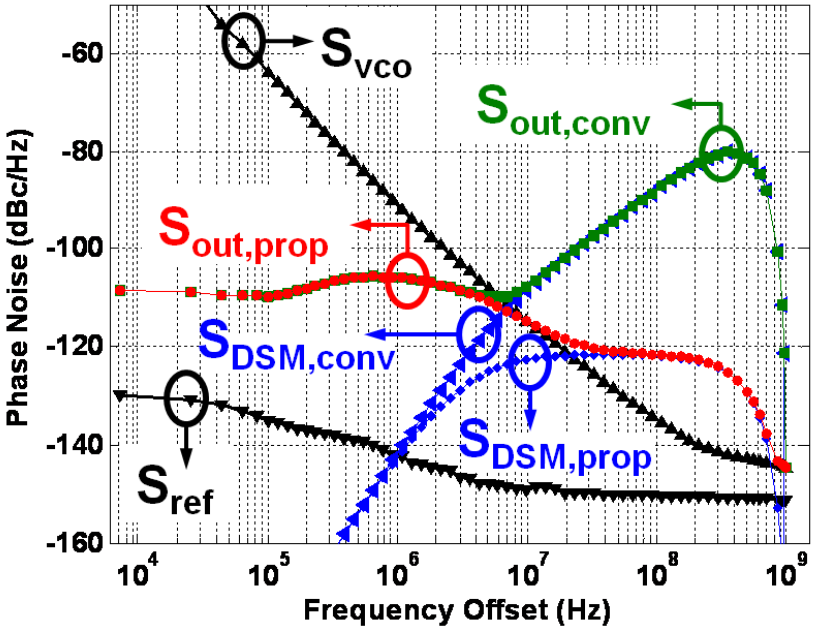


Figure 6.6: Phase noise plot.

The modulators of both PLLs were set to run at the same frequency using the same control word. The jitter at the output of the PLL due to different PLL operating bandwidth was noticed. The results are shown in Fig. 6.7. For generalizing the re-

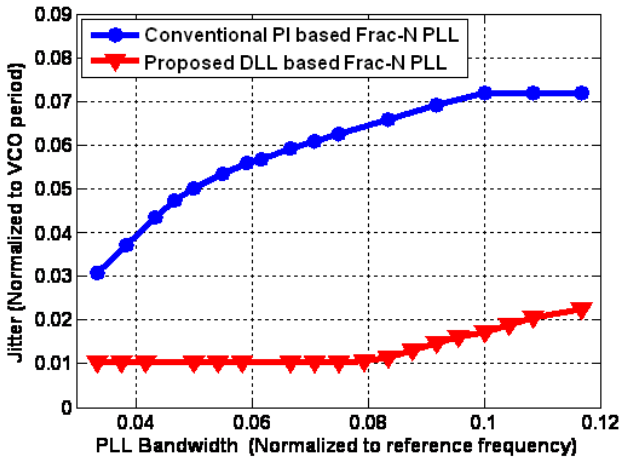


Figure 6.7: Effect of PLL bandwidth on the output of the PLL.

sults, the jitter at the output of the PLL was normalized to its output period, and the bandwidth of PLL was normalized to the reference frequency. In conventional phase interpolator based frac-N PLL, as the operating bandwidth increased, the jitter increased significantly. This is because the $\Delta\Sigma$ modulator has modulated the quantization noise to higher frequency noise components. As expected and discussed, with narrow PLL bandwidth, the high frequency noise is filtered out by the PLL. But with wide operating bandwidth, the quantization noise contributes to the output phase noise significantly.

On the other hand, in our proposed DLL-based frac-N PLL design, for PLL bandwidth up to about $1/10^{th}$ of the reference frequency, the jitter was constant and independent of the bandwidth. This could be interpreted due to the fact that the phase filtering characteristics of DLL filtered out the high frequency quantization noise of the modulator. For understanding the impact of DLL bandwidth on jitter performance, the PLL bandwidth was kept constant, the DLL bandwidth was changed, and the corresponding jitter at the output was plotted in Fig. 6.8. As the DLL bandwidth became narrower, the jitter improved significantly. This is because the high frequency quantization noise due to modulation is now filtered over a narrower bandwidth.

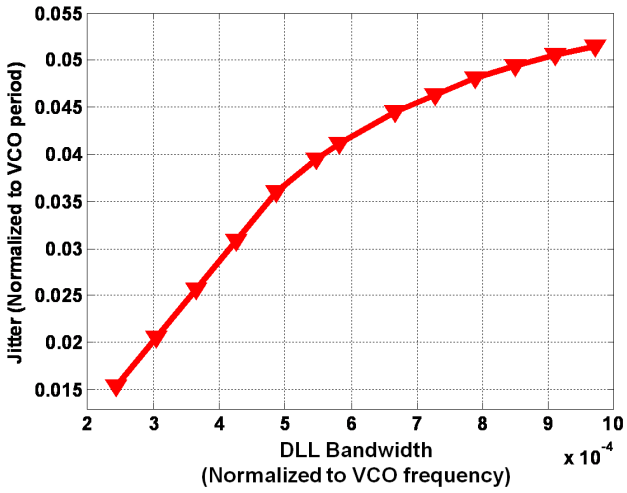


Figure 6.8: Effect of DLL bandwidth on the output of the PLL.

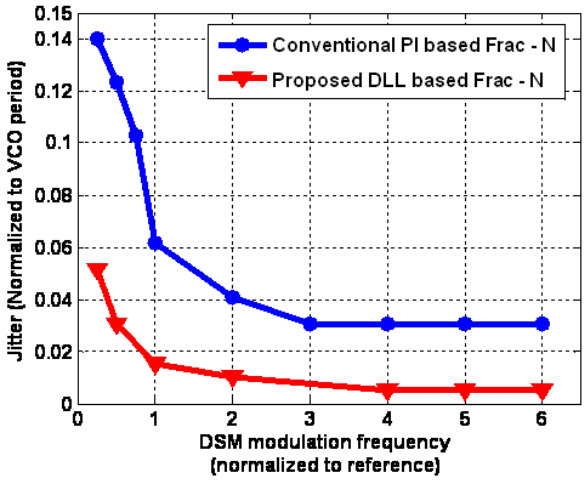


Figure 6.9: Effect of the DSM frequency on the output of the PLL.

The simulation results discussed above was done with the same modulation frequency of the $\Delta\Sigma$ modulator. Now with identical PLL operating and DLL bandwidth, the effect of varying modulation frequency on output jitter is shown in Fig. 6.9. As expected for conventional PI-based frac-N PLL, when the modulator was run at frequencies

less than the reference frequency, the jitter performance degraded significantly. For frequencies larger than the reference frequency, the jitter performance improved but the improvement gradually became negligible. The over-all jitter performance of our proposed PLL design was much better than that of the PI-based PLL for all modulation frequencies. Although for frequencies less than the reference frequency, the jitter did increase, it gradually improved as the modulation frequency increases.

6.4 Conclusion

In this chapter, the design of a DLL-based frac-N PLL has been presented. Our proposed design offers significant improvement of jitter performance at the output of the PLL. Unlike phase interpolator (PI) based frac-N PLL, the proposed design has noticeable improvement on jitter performance, due to quantization noise. Furthermore, this architecture subsides the dependence of the output jitter on the PLL bandwidth. As a result, a wider PLL bandwidth can be used for filtering out VCO phase noise. In summary, our proposed fractional-N PLL offers an elegant design for high frequency synthesis, especially, with a tight requirement for frequency resolution without sacrificing any phase noise performance.

7 Conclusion

7.1 Summary

This thesis focused on high frequency synthesizer solutions. One of the most critical building block of the synthesizer is VCO. A study of different LC VCO topologies is provided in Chapter 2. The goal of this study is to identify the correct VCO topology for high frequency synthesizer. It was found that for achieving similar phase noise performance, the cross-coupled oscillators itself consumed less power than Colpitts. But since cross-coupled oscillators were sensitive to load capacitance, additional buffers were needed increasing the total power consumption. Colpitts and combination oscillators both have the advantage of inherent buffering and wide tuning range, but combination oscillators were much more power efficient. Hence, it was concluded that for high frequency synthesis, combination oscillators are more suitable.

For comparison and study of synthesizer architectures, behavioral simulation capability is essential. In Chapter 3, we developed Matlab Simulink based behavioral simulation flow. To gain confidence in this modeling approach, PLL, DLL and ILO solutions are compared with known experimentally verified results. This provided a platform to evaluate different architectures of 60 GHz synthesizer.

An alternate solution for 60 GHz synthesizer architecture was proposed and verified theoretically and by behavioral simulations in Chapter 4. In comparison to existing solutions, the main benefit of the proposed architecture is that it provides a wider bandwidth and, thus, improves the over-all phase noise performance as explained in Chapter 5. Conventional phase-interpolator based fractional PLL is studied in Chapter 6. A novel DLL based frac-N PLL was proposed to over-come the limitations of conventional frac N PLL.

7.2 Major Contributions

This work mainly focused on designing a 60 GHz frequency synthesizer. However the architecture is general enough to use for other high frequency clock synthesis as well. The main contributions of this work are :

- Chapter 3 introduces a novel phase domain model of ILO for behavioral simulations. Since behavioral model of ILO has not been explored much in the research field, simulation results from the proposed model was verified with the experimental results of a fabricated ILO.

- A novel architecture for high frequency synthesizer was proposed in Chapter 4 and 5. The architecture consists of a PLL cascaded to an ILO. In order to generate narrow pulses and to relax the multiplication ratio of the ILO, a DLL with a pulse generator is used at the output of the PLL. Passive delay line stacked on top of LC VCO was used for power efficiency and replica-biasing technique of frequency tracking was used for increasing the locking range of ILO. The synthesizer operated at 60 GHz with a phase noise of -98, -117 and -128 dBc/Hz at 1 MHz, 10 MHz and 40 MHz respectively. The total power consumed by the frequency synthesizer from 1.2 V supply is 57 mW. This work was submitted in the following journal paper :

  "A Low Power Frequency Synthesizer for 60-GHz Wireless Personal Area Networks", *IEEE Transactions on Circuits and Systems II*, submitted in February 2011.

- Conventional phase-interpolator based frac-N PLL suffer from two limitations. First, the periodic jitter is strongly coupled with PLL bandwidth. Second, increasing DSM frequency beyond reference frequency does not significantly improve jitter performance of the frac-N PLL. To overcome these limitations, we proposed a delay line based frac-N PLL where the PLL bandwidth is de-coupled from the residual jitter in Chapter 6. The proposed frac-N PLL translated into the following conference paper:

"A DLL based Fractional PLL for high frequency synthesis", *European conference on circuit theory and design*, submitted in April 2011.

7.3 Future Work

In this work, experimental validation of the proposed architecture was not possible due to limited fabrication access and experimental facility. However in future, we would like to implement the system.

A Appendix: Phase domain model in Simulink

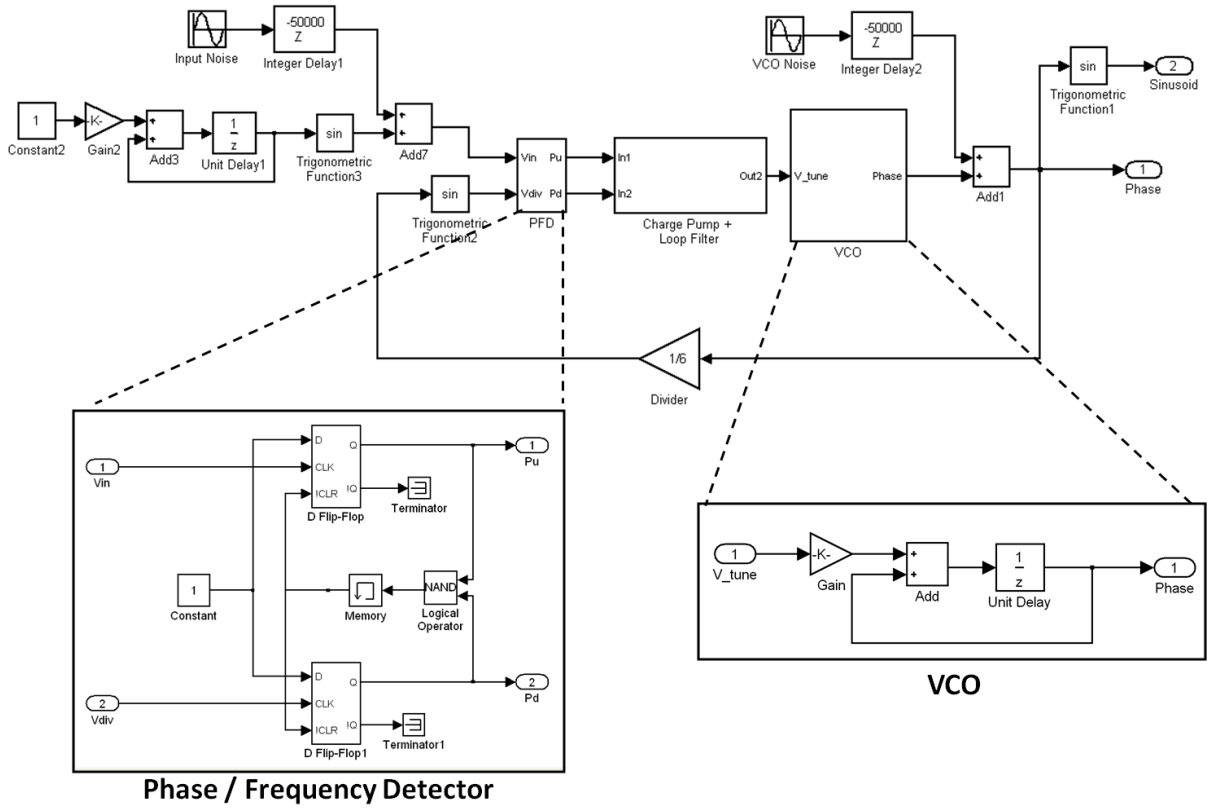


Figure A.1: Screenshot of the simulated model of PLL in Simulink.

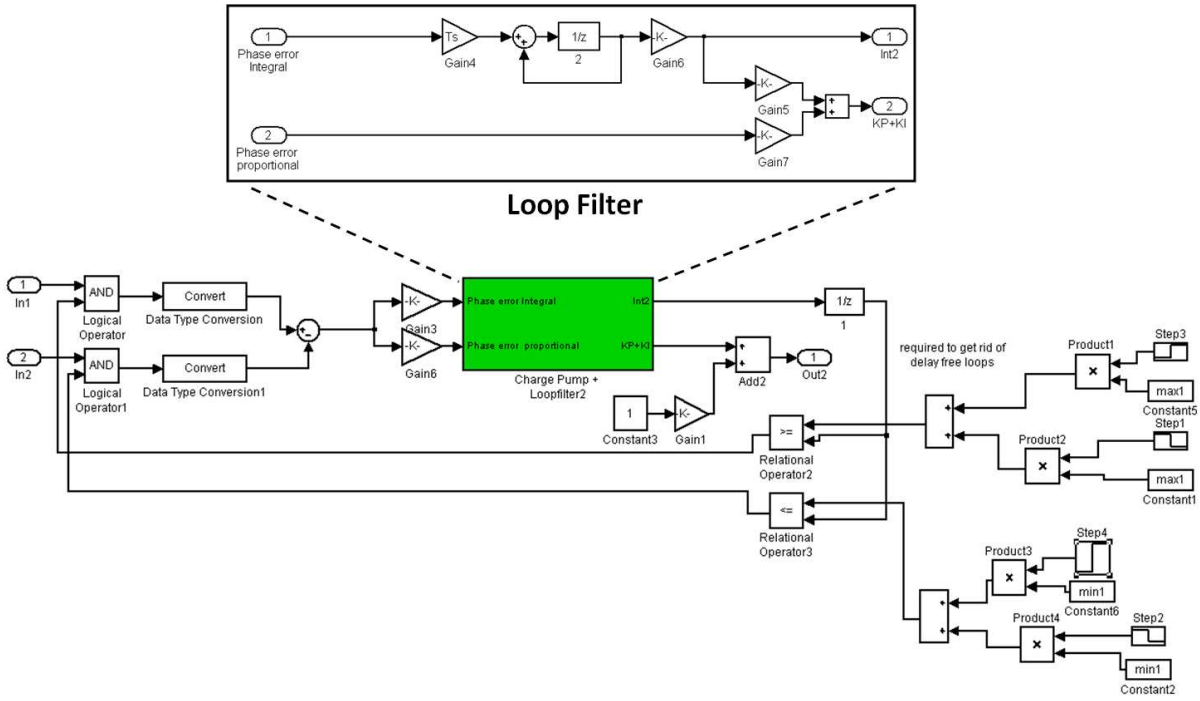


Figure A.2: Screenshot of the simulated model of charge-pump and loop filter in Simulink.

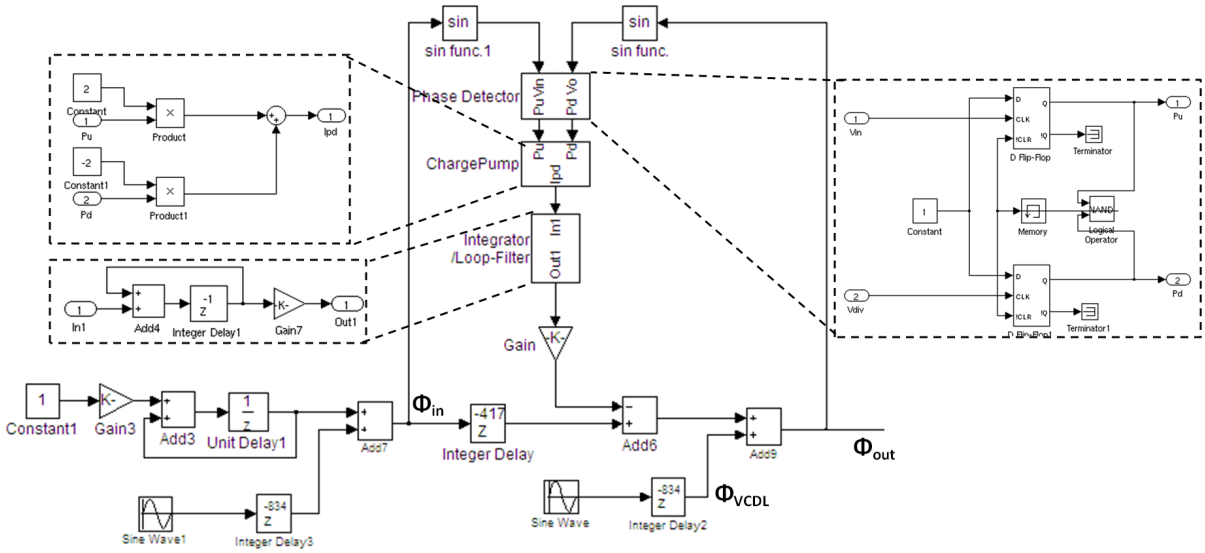


Figure A.3: Screenshot of the simulated model of DLL in Simulink.

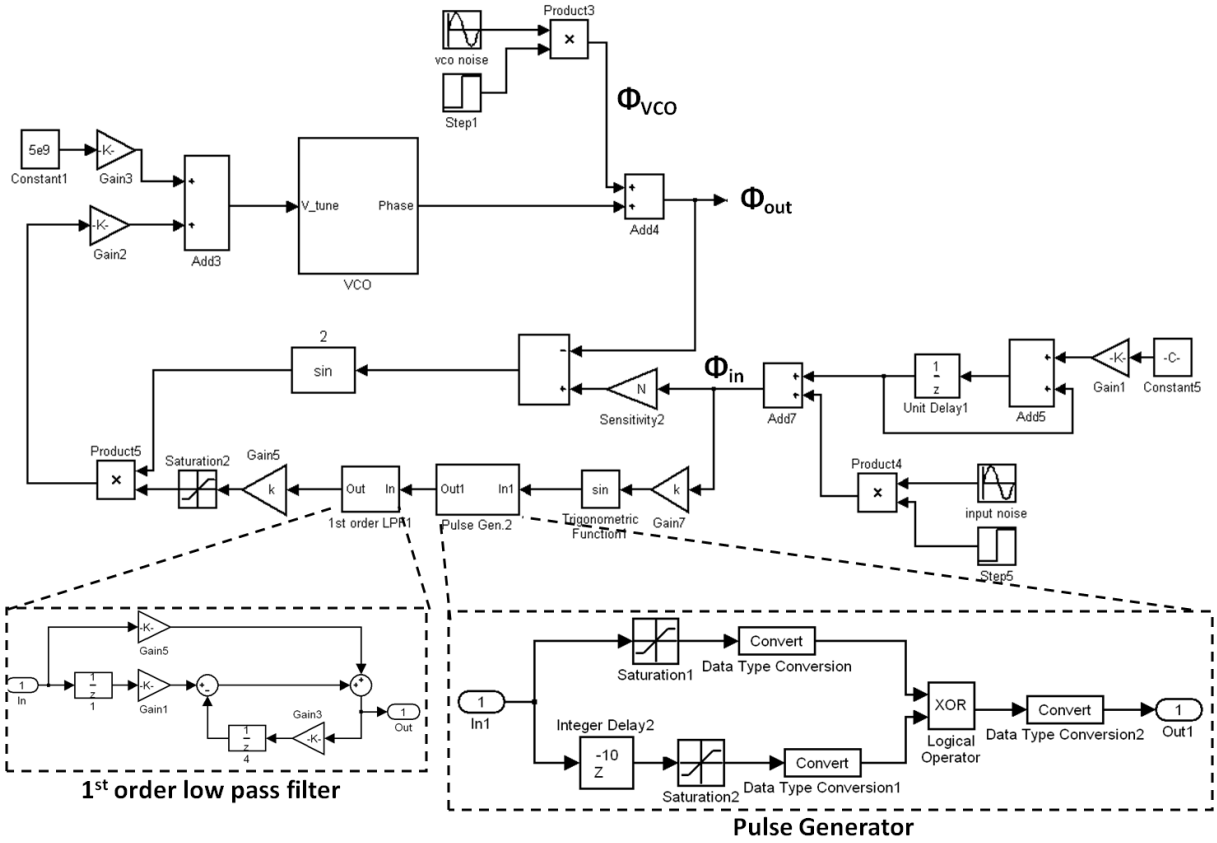


Figure A.4: Screenshot of the simulated model of ILO in Simulink.

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