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Space vector PWM sequence and harmonic comparison for high power current source rectifier

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Space Vector PWM Sequence And Harmonic Comparison For High Power Current Source Rectifier

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ABSTRACT

The space vector PWM (SVPWM) schemes for high power current source drives normally produce low order harmonics due to low switching frequency. To provide a SVPWM with the best harmonic performance, different space vector sequences suitable for a current source rectifier (CSR) are investigated in this project. Details on how to achieve the waveform symmetries with minimum switching frequency for each sequence are discussed. A thorough comparison of the harmonic performance of different space vector sequences based on current source rectifier implementations is carried out. An optimum space vector modulation (SVM) method is proposed to achieve the best line current THD and reduced switching losses. The space vector sequence investigation has been verified in simulation and experimentally using a 10kVA GCT based CSR prototype.

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NOMENCLATURE

Generic Variable Usage Conventions

Variable Format	Meaning
F	CAPITALS: peak AC, rms AC or average DC value
f	LOWER CASE: instantaneous values
[., ., .,]	SQUARE BRACKETS: switching states
(., ., .,)	PARENTHESES: coordinate triple, 3-phase instantaneous values

Specific Variable Definitions

Variable	Meaning
a, b, c, o	inverter output terminals; transformer secondary terminals
(a, b, c)	three phase variables
A, B, C	transformer primary terminals
L	DC link inductor
i_w	rectifier current
I_{dc}	Dc current
f_1	fundamental frequency
f_{sw}	Rectifier switching frequency
h	harmonic order
m_a	amplitude modulation index
s	time second
$S_{1,2}$ ..... $S_{5,2}$	On state switches
$[Sw_a, Sw_b, Sw_c]$	Switching function
T_s	sampling period
THD	total harmonic distortion
I_{1rms}	rms value of the fundamental
$I_{1rms-\max}$	maximum rms value of the fundamental
(v_a, v_b, v_c)	three-phase voltage
V_{ab}	line-to-line voltage
V_{an}	phase voltage
I_{ref}	magnitude of reference vector
θ_{sec}	Angle of reference current
ω	angular frequency

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Chapter 1 Introduction

1.1 Introduction

Three-phase PWM converters are increasingly being considered for use as front end power processing unit. The three-phase current source rectifier (CSR) provides the dc output current and sinusoidal input current with no low frequency harmonics. The input currents contain the fundamental component and the rectifier switching frequency harmonics. The pulse width modulation (PWM) technique used in CSR is mainly for controlling the harmonic contents at the input. Usually, the fundamental component of the rectifier input current is controlled by input filter. The performance of an ac-to-dc converter can be greatly improved by using pulse width modulation techniques.

Selective harmonic elimination (SHE) PWM has been widely used for medium voltage high power current source rectifiers. It is optimized to eliminate certain harmonics through the manipulation of the PWM pattern, and is usually implemented as an off-line technique. On-line PWM techniques, on the other hand, offer fast dynamic response, instantaneous adjustment of modulation index, and therefore precise control of dc current and ac line current magnitude and phase. A widely used digital method to produce on-line PWM patterns is space vector PWM (SVPWM). While as the rectifier switching frequency decreases with a high power CSR, the SVPWM tends to produce more low-order harmonics. Harmonic performance of different sequences for a high power low switching CSR has been investigated in this project.

In this project, different space vector sequences suitable for a CSR are presented. Waveform symmetries and PWM synchronization for each space vector sequence are maintained with minimum rectifier switching frequency by choosing proper number of sequence (N) in each space sector and selecting suitable space vectors at the sector boundary. Harmonic performance of the sequences is compared based on the CSR implementation with a rectifier switching frequency of around 500Hz, which is typical for high power current source drive applications. To achieve best line current THD and

reduced switching losses, an optimum space vector modulation (SVM) method of space vector sequence at the proper modulation index is proposed. Both simulation results from Matlab/Simulink and experimental results obtained using a 10kVA GCT based CSR prototype are provided to verify the space vector sequence investigation and the proposed optimum SVM method.

A PWM rectifier has several advantages such as the elimination of lower-order harmonics and the control of rectifier output current [1]. These advantages are gained at the expense of a more complex control circuit and fast switching devices. To develop a high performance converter with low harmonic pollution and controllable power factor, pulse width modulation techniques have to be employed. In this section, three popular modulation methods are summarized. These three modulation methods are selective harmonic elimination, trapezoidal pulse width modulation (TPWM) and space vector modulation technique. These modulation schemes are developed for high-power rectifiers operating with a rectifier switching frequency of around 500Hz. The operating principle of the modulation schemes is analyzed.

1.2 Background

Solid state ac-to-dc converters are widely used in variable frequency ac motor drive systems, reactive power compensation and uninterruptible power supplies. In general, a high quality ac-to-dc converter should have unity or near unity input power factor, high energy efficiency, two-quadrant operation capability, and low harmonic pollution.

In high power applications, SCR rectifiers are widely used. A SCR rectifier has the advantages of simple structure, low cost and high effiency.However; it injects a substantial amount of current harmonics into power systems and demands lagging reactive power. The limits in the existing 519-1992 document are based predominantly on the harmonic currents produced by six-pulse diode bridge rectifiers [2]. These rectifiers form the front-ends for numerous power converter applications like power supplies and motor drives. However, the total harmonic content produced by such devices

is quite high and may be associated with a poor power factor. Conventional passive filtering can be used to mitigate such problems, but these filters can be bulky and expensive.

The performance of an ac-to-dc converter can be greatly improved by using pulse width modulation PWM techniques [3]. A PWM-type converter has the advantages of improved input power factor, less line current distortion and low output ripple. This implies a substantial reduction in reactive power compensation and filter requirements on both ac and dc sides. In the high power range SCR rectifiers are being gradually replaced by PWM rectifiers [4].

The gate commutated thyristor (GCT), also known as integrated gate commutated thyristor (IGCT), is developed from conventional GTO structure [5]. The GCTs device can provide required voltage and current ratings for implementing PWM techniques in high power applications. The symmetric GCT has reverse voltage blocking capability, making ideal for current source rectifiers. The PWM rectifier features reduced line current distortion, superior dynamic response and improved input power factor. This project will focus on the PWM techniques based on space vector approach are developed for high power CSR. Different space vector sequences suitable for a CSR are presented.

1.3 Current Source Rectifier

Fig. 1.1 shows the circuit diagram of a single-bridge SGCT current source rectifier. When the rectifier is used for high power drives with the utility supply voltage, two or more SGCTs can be connected in series for higher utility voltage [6-8].

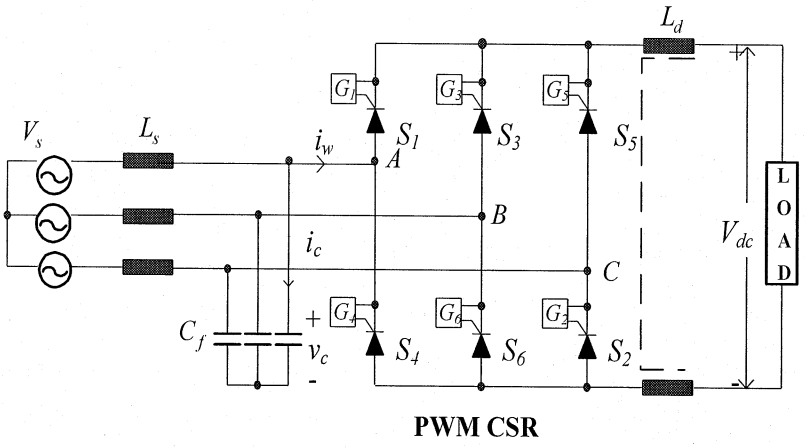


Fig. 1.1 Single-bridge SGCT current source rectifier.

The line inductance L_s on the ac side of the rectifier represents the total inductance between the utility supply and the rectifier, including the equivalent inductance of the utility supply, leakage inductances of isolation transformer if any, and inductance of a three-phase ac reactor will help in line current THD reduction. The line inductance L_s is normally in the range of 0.1 to 0.15 per unit (pu).

As mentioned earlier, the PWM rectifier requires a filter capacitor C_f. The capacitor size is dependent on a number of factors such as the rectifier switching frequency, required line current THD and input power factor. It is normally in the range of 0.3 to 0.6pu for a high power PWM rectifier with a rectifier switching frequency of a few hundred Hertz.

On the dc side of the rectifier, a dc-choke L_d is required to smooth the dc current. The choke usually has a magnetic core with two coils, one in the positive dc bus and the other in the negative bus. Such an arrangement is preferred in practice for motor common-mode voltage reduction [9]. To reduce the dc link current ripple to an acceptable level (< 15%), the size of the dc choke is in the range of 0.5 to 1.0pu.

1.4 PWM Switching Techniques for the CSR

The PWM technique used in CSR is mainly for controlling the harmonic contents at the input. Usually, the fundamental component of the rectifier input current is controlled by input filter. The input current is also controlled by PWM scheme rather than by the input filters. However, this scheme is not commonly used, because of its low efficiency, especially when input current is small. Popular modulation techniques for CSR are:

- Trapezoidal pulse width modulation (TPWM);
- Selective harmonic elimination (SHE); and
- Space vector modulation (SVM).

All the above three modulation scheme principles are discussed below in detail.

The PWM techniques used in the CSR differ from those in the VSR due to the symmetrical constraints for the output current waveform. In order to properly gate the power switches of a CSR, the following main constraints must be meet at any time

- At any instant of time (excluding commutation intervals) there are only two switches conducting;
- One in the top half of the bridge and the other in the bottom half;
- With only one switch turned on, the continuity of the dc current is lost; and
- The rectifier current waveform should be half wave symmetrical.

1.5 Trapezoidal Pulse Width Modulation

The trapezoidal modulation does not generate gatings in the center $\pi/3$ interval of the positive half cycle or in the negative half cycle of the rectifier fundamental frequency. Such arrangements satisfy the switching constraints of current source rectifier.

The trapezoidal PWM technique is some what analogous to the sinusoidal PWM technique. Fig. 1.2 shows the principle of the trapezoidal pulse width modulation, where

V_m is a trapezoidal modulating wave and V_{cr} is a triangular carrier wave. The amplitude modulation index is defined by

$$m = \frac{\hat{V}_m}{\hat{V}_{cr}}$$

where $\hat{V}_m$ and $\hat{V}_{cr}$ are the peak values of the modulating and carrier waves, respectively. Similar to the carrier based PWM schemes for voltage source rectifiers, the gate signal G_1 for switch S_1 is generated by comparing V_m with V_{cr}. However, the trapezoidal modulation does not generate gating in the center $\pi / 3$ interval of the positive half cycle or in the negative half cycle of the supply fundamental frequency. Such an arrangement leads to the satisfaction of the switching constraint for the CSR. It can be observed from the gate signals that only two GCTs conduct at any time.

The rectifier switching frequency of can be calculated by

$$f_{sw} = f \times N_p$$

where f is the fundamental frequency and Np is the number of pulses per half cycle of i_w.

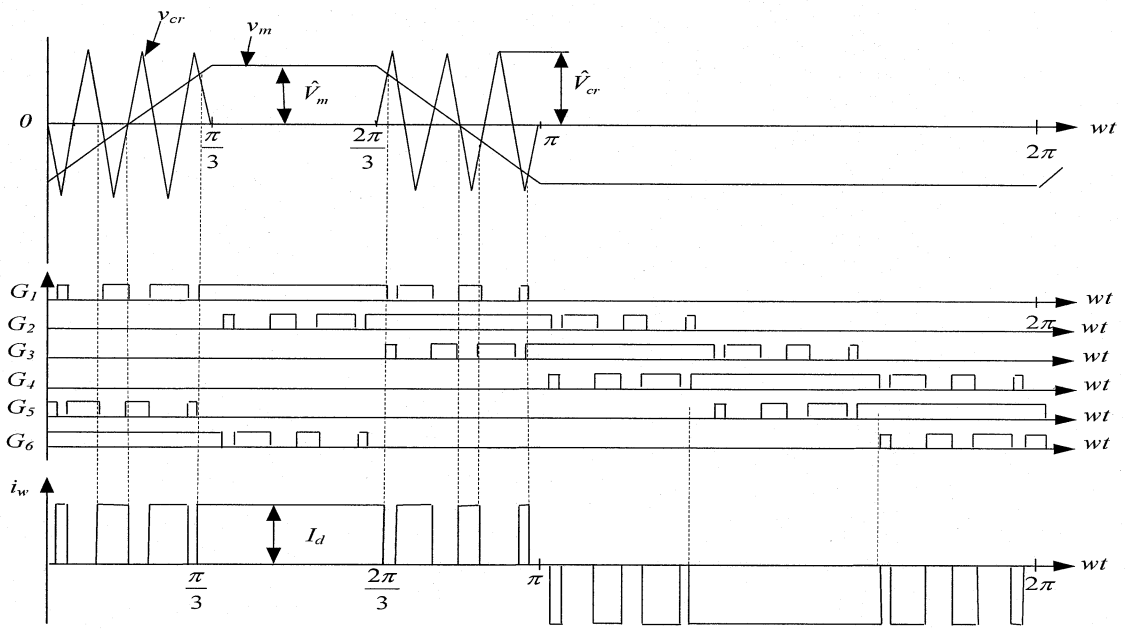


Fig. 1.2 Waveform of Trapezoidal pulse width modulation.

This modulation is proposed specifically for current source rectifier, because it can satisfy the constraint required for current source rectifier operation. The TPWM scheme generates a pair of dominant harmonics whose orders are related to the rectifier switching frequency. These low-order harmonics are difficult to be fully attenuated by the filter capacitor, causing a detrimental effect on the line current THD. Therefore, the applicability of the trapezoidal modulation is diminished for an ac-to-dc converter operating at a low rectifier switching frequency [5].

1.6 Selective Harmonic Elimination (SHE)

Selective harmonic elimination is an off-line modulation scheme, which is able to eliminate a number of low-order unwanted harmonics in the rectifier PWM current i_w. The switching angles are pre-calculated and then imported into a digital controller for implementation. The selective harmonic elimination scheme is considered as an optimum modulation scheme, which provides a superior harmonic profile with a minimum rectifier switching frequency. The SHE scheme for the current source rectifier needs to adjust modulation index in addition to harmonic elimination.

Fig. 1.3 shows a typical half-cycle waveform of the rectifier PWM current i_w. The current waveform in Fig. 1.3 is designed such that the switching constraints for the current source converters discussed above are satisfied. There are six current pulses per half cycle with only three independent angles, β_1, β_2 and β_0. These angles can be used to eliminate two current harmonics and in the meanwhile provide an adjustable modulation index [1].

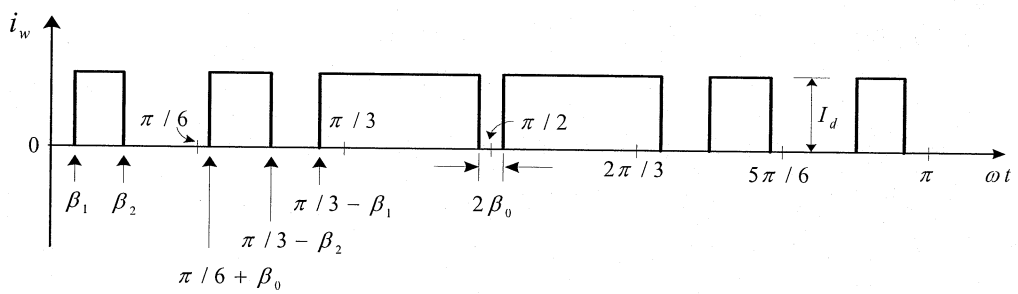


Fig. 1.3 A typical PWM current waveform with three independent switching angles (β_1, β_2 and β_0).

where m_a is amplitude modulation index, given by

$$m_a = \frac{I_{w1}}{I_d}$$

where I_{w1} is the peak fundamental-frequency component of the PWM current and I_d is the average dc current.

The maximum modulation index is 1.03, at which β_0 becomes zero and the notch in the centre of the PWM waveform disappears. The unwanted harmonics can be eliminated by selecting a set of switching angle β_i. For the same number of pulses per half cycle of modulation wave, the degree of freedom available for eliminating the harmonics in a CSR is reduced to about half available in the VSR, because only about half of switching angles are independent in the CSR.

1.7 Space Vector Modulation

In addition to the TPWM and SHE schemes, the current source rectifier can also be controlled by space vector modulation (SVM) [8-10]. The selective harmonic elimination scheme introduced above is an off-line PWM scheme. All the switching angles are pre-calculated and then stored in a look-up table for digital implementation. Although the PWM current waveform generated by the SHE modulation is very efficient in eliminating the dominant harmonics with a minimum rectifier switching frequency, this scheme cannot be used in any control algorithms that require an instantaneous adjustment of modulation index.

The space vector modulation is an on-line scheme suitable for real-time digital implementation. Compared with the SHE modulation, the SVM provides faster dynamic response and greater flexibility since the modulation index and switching signals can be adjusted in each sampling period.

1.7.1 Switching States

The operating status of the six switches in the current source rectifier of Fig. 1.4 can be represented by the switching states given in Table 1.1. The switching state [1] denotes that the upper switch in an inverter phase leg is turned on and the lower switch in the same leg is off. The resultant inverter PWM current i_w is equal to the dc current I_d. State [-1] indicates that the lower switch is on and the upper switch is off, resulting in $i_w = -I_d$. Switching state [0] signifies that none of the two devices in a leg is turned on whereas state [2] denotes both switches conduct and the dc current source I_d is bypassed (short circuited). The bypass operation is allowed in the CSR due to its short duration and the large dc choke that limits the rate of rise of the dc current.

Table 1.1 Definition of switching states

Switching States	Upper Switch Inverter Leg A		Rectifier PWM current i_w
	Lower Switch	Upper switch	
[1]	On	off	I_d
[-1]	Off	On	$-I_d$
[0]	Off	Off	0
[2]	On	On	0

As stated earlier, the PWM switching pattern design for the CSR must satisfy a constraint, that is, two switches in the rectifier conduct at any time instant, one connected to the positive dc bus, and the other to the negative bus. Under this constraint, the three-phase inverter has a total of nine switching states as shown in Table 1.2. These switching states can be classified as active switching states and zero switching states.

Zero state [2 0 0] signifies that switches S_1 and S_4 in inverter phase leg A conduct simultaneously and the other four switches in the inverter are off. The dc current source I_d is bypassed and thus the inverter PWM current i_w is zero. There are three zero states [2 0 0], [0 2 0] and [0 0 2]. Since all the zero states produce zero output current, two of them

seem redundant. As will be seen later, the redundant states can be utilized for rectifier switching frequency reduction.

There exist six active states. The state [1 -1 0] indicates that switch S_1 in leg A and S_6 in leg B are on, and all the remaining switches are off. The definition of other five active states is also given in the table.

Table 1.2 Switching states and space vectors

Type	Switch state (three phases)	On-state Switch	Space Vector
Zero States	[2 0 0]	S_1,S_4	$\vec{I}_0$
	[0 2 0]	S_3,S_6	
	[0 0 2]	S_5,S_2	
Active States	[1 -1 0]	S_6,S_1	$\vec{I}_1$
	[1 0 -1]	S_1,S_2	$\vec{I}_2$
	[0 1 -1]	S_2,S_3	$\vec{I}_3$
	[-1 1 0]	S_3,S_4	$\vec{I}_4$
	[-1 0 1]	S_4,S_5	$\vec{I}_5$
	[0 -1 1]	S_5,S_6	$\vec{I}_6$

1.7.2 Space Vectors

The active and zero switching states can be represented by active and zero space vectors, respectively. A typical space vector diagram for the CSR is shown in Fig. 1.5, where I_1 to I_6 are the active vectors and I_0 is the zero vector. The active vectors form a regular hexagon with six equal sectors while the zero vector I_0 lies on the center of the hexagon.

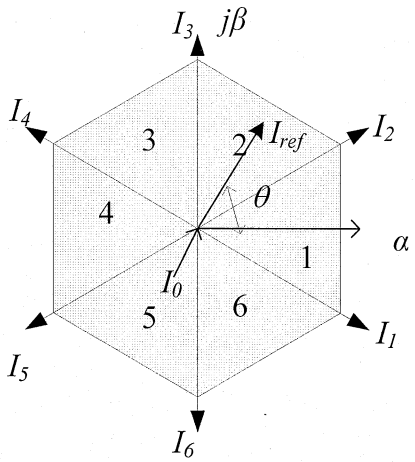


Fig. 1.5 Space vector diagram for the current source rectifier.

To derive the relationship between the space vectors and switching states assuming that the operation of the rectifier is three-phase balanced, we have

$$i_{wA}(t) + i_{wB}(t) + i_{wC}(t) = 0 \tag{1.1}$$

where i_{wA}, i_{wB} and i_{wC} are the instantaneous PWM rectifier currents in the phases A, B and C, respectively. The three-phase currents can be transformed into two-phase currents in the $\alpha - \beta$ plane

$$\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{wA} \\ i_{wB} \\ i_{wC} \end{bmatrix} \tag{1.2}$$

A current space vector can be generally expressed in terms of the two-phase currents as

$$\vec{I}(t) = i_\alpha(t) + j i_\beta(t) \tag{1.3}$$

Substituting (1.2) into (1.3),

$\vec{I}(t)$ can be express in terms of i_{wA} , i_{wB} and i_{wC}

$$\vec{I}(t) = \frac{2}{3}\left[i_{wA}(t)e^{j0} + i_{wB}(t)e^{j2\pi/3} + i_{wC}(t)e^{-j2\pi/3}\right] \tag{1.4}$$

For the active state [1 -1 0], S_1 and S_6 are turned on, the rectifier PWM currents are

$$i_{wA}(t) = I_d \text{ , } i_{wB}(t) = -I_d \quad \text{and} \quad i_{wC}(t) = 0 \tag{1.5}$$

Substituting (5) into (4) yields

$$\vec{I}_1(t) = \frac{2}{\sqrt{3}} I_d e^{j(-\pi/6)} \tag{1.6}$$

Similarly, the other five active vectors can be derived. The active vectors can be generally expressed as

$$\vec{I}_k(t) = \frac{2}{\sqrt{3}} I_d e^{j((k-1)\frac{\pi}{3} - \frac{\pi}{6})} \qquad \text{for } k = 1, 2, 3\ldots, 6 \tag{1.7}$$

The reference vector I_{ref} is also shown in Fig. 1.5 It rotates in space at an angular velocity of

$$\omega = 2\pi f_1 \tag{1.8}$$

where f_1 is the fundamental frequency of i_w . The angular displacement between I_{ref} $\vec{I}_0$ and the α -axis of the α − β plane can be obtained by

$$\theta(t) = \int_0^t \omega(t)dt + \theta(0) \tag{1.9}$$

1.7.3 Dwell Time Calculation

The space vector modulation for the CSR is based on ampere-second balancing principle, that is, the product of the reference vector I_{ref} and sampling period T_s equals the sum of the current vectors multiplied by the time interval of chosen space vectors. Assuming that the sampling period T_s is sufficiently small, the reference vector I_{ref} can be considered constant during T_s. Under this assumption, I_{ref} can be approximated by two adjacent active vectors and a zero vector. For example, with I_{ref} falling into sector I as shown in Fig. 1.5, it can be synthesized by I_1, I_2 and I_0. The ampere-second balancing equation is thus given by

$$0 \le m_a \le 1 \tag{1.10}$$

where T_1 , T_2 and T_0 are the dwell times for the vectors I_1, I_2 and I_0, respectively. Substituting

$$\vec{I}_{ref} = I_{ref} e^{j\theta}, \vec{I}_1 = \frac{2}{\sqrt{3}} I_d e^{-j\frac{\pi}{6}}, \vec{I}_2 = \frac{2}{\sqrt{3}} I_d e^{j\frac{\pi}{6}} \quad \text{and} \quad \vec{I}_0 = 0 \tag{1.11}$$

into (1.10) and then splitting the resultant equation into the real (α – axis) and imaginary (β – axis) components leads to

$$\begin{aligned} \text{Re}: I_{ref}(\cos\theta) T_s &= I_d (T_1 + T_2) \\ \text{Im}: I_{ref}(\sin\theta) T_s &= \frac{1}{\sqrt{3}} I_d (-T_1 + T_2) \end{aligned} \tag{1.12}$$

Solving (1.12) together with $T_s = T_1 + T_2 + T_0$ gives

$$
\begin{aligned}
T_1 &= m_a \sin(\pi/6-\theta)T_s \\
T_2 &= m_a \sin(\pi/6+\theta)T_s \\
T_0 &= T_s - T_1 - T_2 \qquad \text{for } -\pi/6 \le \theta < \pi/6
\end{aligned} \tag{1.13}
$$

where m_a is the modulation index, given by

$$
m_a = \frac{I_{ref}}{I_d} = \frac{\hat{I}_{w1}}{I_d} \tag{1.14}
$$

where $\hat{I}_{w1}$ is the peak value of the fundamental frequency component in i_w.Note that although equation (1.13) is derived when I_{ref} is in sector I, it can also be used when I_{ref} is in other sectors provided that a multiple of $\pi / 3$ is subtracted from the actual angular displacement θ such that the modified angle θ' falls into the range of $-\pi / 6 \le \theta' < \pi / 6$ for use in the equation, that is,

$$
\theta' = \theta-(k-1)\pi/3 \qquad \text{for} \qquad -\pi / 6 \le \theta' < \pi / 6 \tag{1.15}
$$

where k =1, 2, 6 for sectors I, II, VI, respectively.

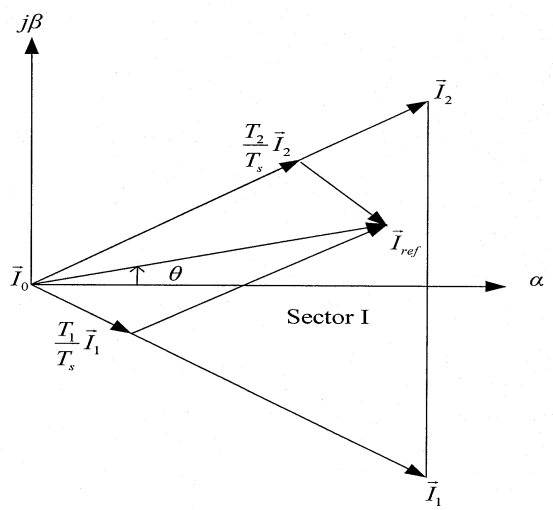


Fig. 1.6 Synthesis of I_{ref} by I_1, I_2 and I_0.

The maximum length of the reference vector, $I_{ref,\,max}$, corresponds to the radius of the largest circle that can be inscribed within the hexagon as shown in Fig. 1.5. Since the hexagon is formed by the six active vectors having a length of $2I_d$ / 3, $I_{ref,\,max}$ can be found from

$$I_{ref,\max} = \frac{2I_d}{\sqrt{3}} \times \frac{\sqrt{3}}{2} = I_d \tag{1.16}$$

Substituting (1.16) into (1.14) gives the maximum modulation index

$$m_{a,\max} = 1$$

from which the modulation index is in the range of $0 \le m_a \le 1$

The space vector modulation is an on-line scheme suitable for real-time digital implementation. The SVM provides faster dynamic response and greater flexibility since the modulation index and switching signals can be adjusted in each sampling period.

1.8 Project Objectives

The main objective of this thesis is to develop a high performance GCT current source ac-dc converter for high power applications. The effort will be focused on solving the potential problems caused by using a low rectifier switching frequency (several hundred Hertz) scheme and low input current distortion for high power GCT current source rectifiers. SVM PWM with different sequence is investigated to get the combined effect of fast dynamic response and low THD. The following research will be conducted:

- To design a space vector PWM sequences for current source rectifier to achieve better performance;
- To evaluate the performance of the current source rectifier;

- To analyze and investigate the harmonic contents and total harmonic distortion of the current source rectifier for different space vector sequence; and
- To verify the performance of the current source rectifier experimentally.

1.9 Project Outline

The work of the thesis is organized in to five chapters.

Chapter 1 provides a general background on high power ac-to-dc converters, PWM technique and device. The rest of this project is organized as follows:

Chapter 2 focuses on the development of six SVM PWM switching sequence for current source rectifier. The SVM sequence technique is proposed to minimize the rectifier switching frequency and Analysis of different SVM sequence in detail. The graphical approach of calculating the dwell time for SVM PWM technique is derived.

Chapter 3 emphasizes on the modeling and analysis. The current source rectifier is modeled and analyzed in detail. Two important SVM sequence are investigated by simulations. The modulation technique performance evaluation is carried out for all the sequence. Detail analysis of lower order harmonics and total harmonic distortion (THD) of switching current and line current for different space vector sequence. The simulation is illustrated by graphics plotted by the results from the simulations.

Chapter 4 provides the experimental verification. A prototype current source rectifier (CSR) has been set up to verify the performance of the proposed space vector modulation PWM six sequences introduced in Chapter 2. The experimental setup includes the IGCT gate driver and IGCT device. The measured waveforms are analyzed and compared with the simulation results. It also verifies the harmonic contents of rectifier current and line current. The current source rectifier is tested on different conditions, and the relevant waveforms of CSR are provided and followed detailed explanation.

Chapter 5 is the conclusions drawn from the research in this project.

Other supporting materials and more detailed waveforms are attached in the appendices.

Chapter 2 SVM PWM Sequences

2.1 Introduction

The pulse width modulation has been one of the most intensively investigated areas of power electronics for many years now, and the number and combination of permutations seem to be endless. The proposed space vector scheme used for current source rectifier is adapted from the VSR topology it is a fixed frequency technique. For space vector modulation (SVM) which calculates the times and selects the switching patterns based upon the two-axis reference current vector, a sample-period based SVM optimization technique, which is based on minimizing THD in every sample period by changing the ratio of two null vector times. Details on how to achieve the waveform symmetries with minimum rectifier switching frequency for each sequence are discussed.

2.2 Current Source Rectifier Space Vectors

The space vector is a complex number that can be associated to any three quantities (not necessarily sinusoidal) which add up to 0. For instance, the space vector associated with the ac line currents of a three-phase CSR is given by

$$I = \frac{2}{3}(i_a + i_b.e^{j\phi} + i_c.e^{-j\phi}) \tag{2.1}$$

where, $\phi = \frac{2\pi}{3}$ and i_a, i_b and i_c are the line current components.

Unlike a three-phase VSR, a three-phase CSR has nine valid switch combinations that are named "states". Each state produces a specific set of ac line currents and thereby, a specific space vector can be associated with each one by using (2.1) [13-14]. Table 2.1

shows the nine possible states with their respective ON switches and normalized line currents.

Like the nine states of a CSR, the instantaneous ac line current reference ([i_{ref}] abc) $I_{ref}.T_s = I_n.T_n + I_{n+1}.T_{n+1} + I_0.T_0$ can be represented by an equivalent space vector (I_{ref}).Noting that this vector has a length proportional to the modulation index (m_a= || I_{ref}||) and a constant rotating angular frequency equal to for sinusoidal references.

Table 2.1 CSR switching states and Switch realizations

Switching State	ON Switches	Switching function			Switching vector (current space vector)
		sw_a	sw_b	sw_c	
1	1,2	1	0	-1	$i_1 = (2/\sqrt{3})e^{j\pi/6} i_{dc}$
2	2,3	0	1	-1	$i_2 = (2/\sqrt{3})e^{j\pi/2} i_{dc}$
3	3,4	-1	1	0	$i_3 = (2/\sqrt{3})e^{j5\pi/6} i_{dc}$
4	4,5	-1	0	1	$i_4 = (2/\sqrt{3})e^{-j5\pi/6} i_{dc}$
5	5,6	0	-1	1	$i_5 = (2/\sqrt{3})e^{-j\pi/2} i_{dc}$
6	6,1	1	-1	0	$i_6 = (2/\sqrt{3})e^{-j\pi/6} i_{dc}$
7	1,4	0	0	0	$i_7 = 0$
8	3,6	0	0	0	$i_8 = 0$
9	5,2	0	0	0	$i_9 = 0$

The CSR space vector $(I_k, k = 1,...,9)$ and the line current reference space vector (i_{ref}) are represented in a complex plane (Fig.2.1). The objective of the SVM technique, which is also the main objective of the gating pattern generator, is to approximate the current reference space vector (i_{ref}) with the nine space vector $(I_k, k = 1,...,9)$ available in CSR. However, it has been reported that by approximating the reference space vector by only the nearest two nonzero (I_n and I_{n+1}) and one zero space vector ($I_0 = I_7$, I_8 or I_9 Fig.2.1), the gain of the technique is maximized [15] and the rectifier switching frequency minimized.

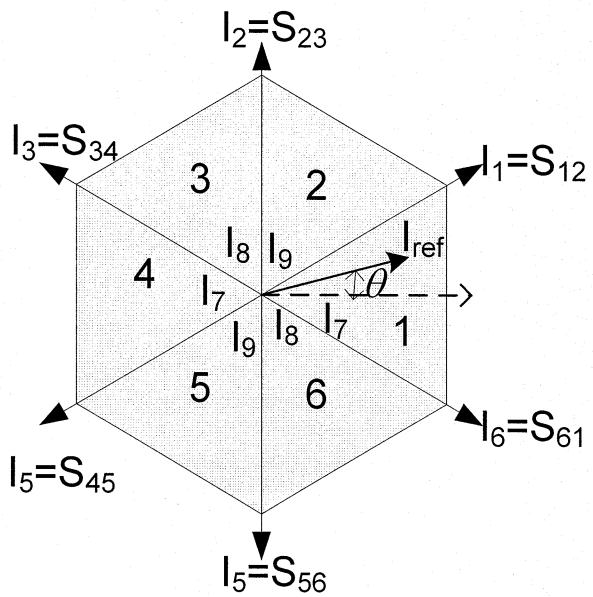


Fig. 2.1 Space vector diagram of a CSR.

With two switches conducting at any time (one and only one in each half of the converter bridge), a three-phase CSR has six active states and three zero states as shown in Fig. 2.1, where the reference current vector is sampled at equal time intervals of T_s, called 'sampling time' or 'PWM frame'. In each sector, the reference can be synthesized by two active vectors and a zero vector with their respective dwell times.

2.3 Six Space Vector Sequences

The SVM technique selects the vectors to be used and their respective ON times. However, the sequence in which they are used to gate the converter remains undetermined. In this thesis, six sequence are studied (Sequence A, Sequence B, Sequence C, Sequence D, Sequence E, and Sequence F Fig. 2.2).Note that the evaluation can be done regardless of the selection of the zero SV, due to the fact that the line current wave shape does not depend upon the selected zero vector

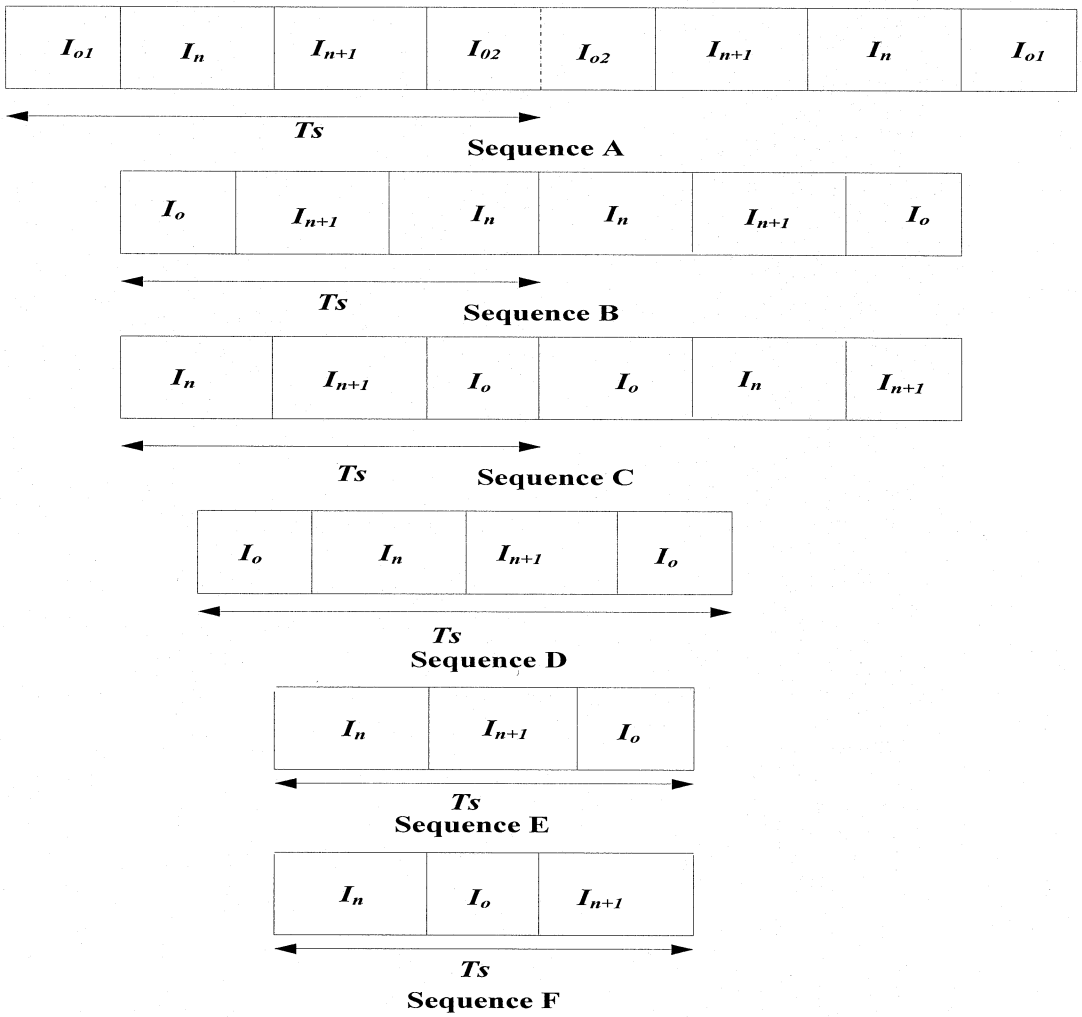


Fig. 2.2 Space vector sequences for a CSR.

The SVM method has been widely adopted due to its ability of vector sequence arrangement and explicit identification of pulse placement. Fig.2.2 (sequence A to sequence F) shows different space vector sequence employed in the literature for the modulation of a CSR [15-17], where Sequence A to Sequence C can be generated by using triangle carrier with asymmetrical sampled PWM and Sequence D to Sequence F can be realized with saw tooth carrier. Each switching vector can be displaced anywhere within the switching cycle because the displacement has no effect on the amp-second average of the resulting current pulses corresponding to the reference vector.

The Sequence A in Fig. 2.3 can be directly derived from VSR continuous PWM. In SVPWM, the zero vectors dwell times in each sample are usually simply selected to be equal and this gives better harmonic performance at certain condition [17]. The number of pulses in each half wave with this sequence will be 6N resulting in a rectifier switching frequency of 360N (with a fundamental frequency of 60 Hz), where N is the number of sequences in one sector. The sequence can start as $I_{01}-I_n-I_{n+1}-I_{02}$ or $I_{02}-I_{n+1}-I_n-I_{01}$ with close harmonic performance. Similarly, three samples (N=1.5) should be used in each sector resulting in a rectifier switching frequency of 540Hz. To maintain waveform symmetries, the sequence should restart (instead of continue) at each sector boundary. With the sequence shown in Fig. 2.3 (sequence A), I_{02} will be the zero vector that crosses the sector boundary and it should be selected as the allocated zero vector for next sector to avoid additional switching. For a sequence beginning with $I_{02}-I_{n+1}-I_n-I_{01}$, the zero vector during sector crossing is selected (i.e. $I_{02}-I_{n+1}-I_n-I_{01}$ will switch to $I_{02}-I_{n+1}-I_n-I_{01}$ in next sector).

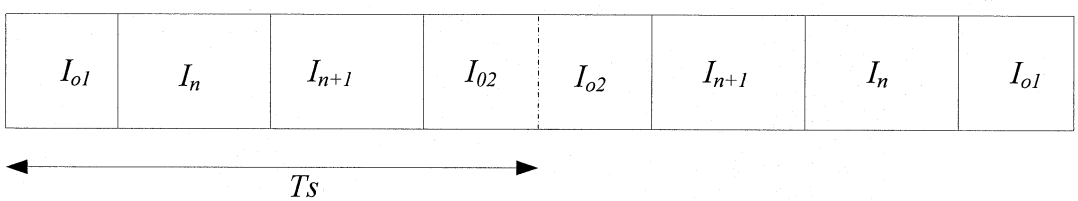


Fig. 2.3 Space vector sequence A for a CSR.

Removing one zero vector in the center of Sequence A results in the discontinuous PWM sequence of Sequence B shown in Fig. 2.4. For Sequence B, if the number of sequences in a sector is N, the number of pulses per half cycle will be 4N and the rectifier switching frequency will be 240N Hz. A suitable rectifier switching frequency for waveform symmetries will be 480Hz. Besides that the sequence B can also start as $I_0-I_n-I_{n+1}$ which results in similar harmonic performance.

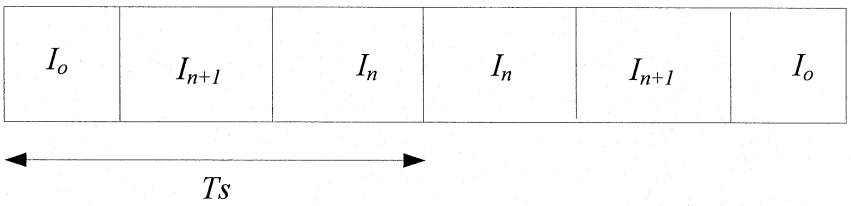


Fig. 2.4 Space vector sequence B for a CSR.

The Sequence C is a discontinuous modulation generated by removing the zero vectors at both sides of Sequence A. As shown in Fig. 2.5 Sequence C is not symmetrical from the sequence center. It is arranged like this to reduce one switching during sector crossing, where I_{n+1} in present sector will be the same as I_n in the next sector. The pulse number per half cycle with Sequence C is therefore $5N-1$, and a suitable rectifier switching frequency to maintain waveform symmetries 540 Hz. In this case Sequence C can have the same sampling frequency as Sequence B.

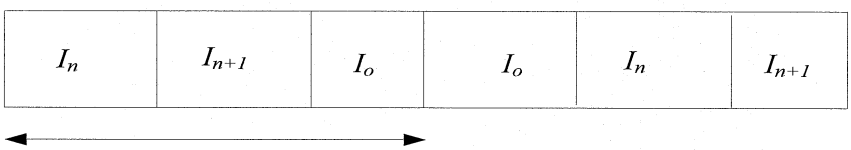


Fig. 2.5 Space vector sequence C for a CSR.

The Sequence D and Sequence E as shown in Fig. 2.6 are both single-edge sequences with the only difference being that instead of using one zero vector at the sequence end, Sequence D divides the zero vector and puts them at both sides. Theoretically, the arrangement of Sequence D can provide better harmonic performance by centering the active vectors in each sample [18]. For Sequence D, at the last sample in a sector, the zero vector at the sequence end should be selected as the zero vector allocated for the next sector. The pulse numbers per half cycle for both sequences are 3N for waveform symmetries and a suitable rectifier switching frequency is 540Hz.

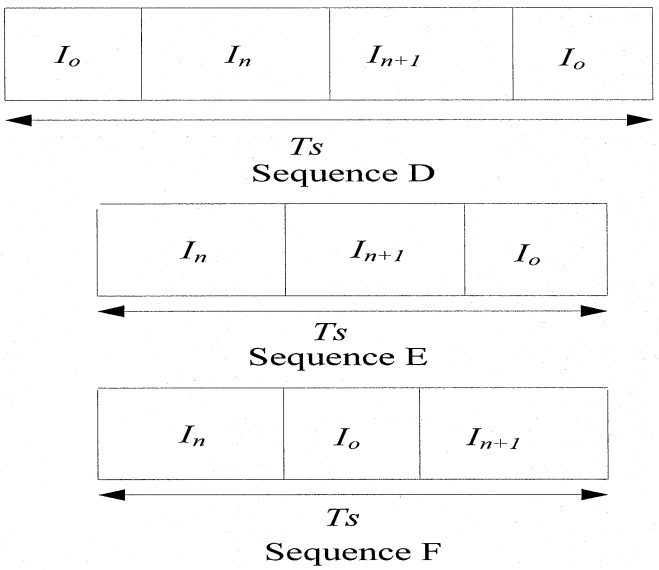


Fig. 2.6 Space vector sequence D - F for a CSR.

Compared to Sequence D and Sequence E, Sequence F can save one switching during the sector crossing by centering the zero vector. The number of pulses per half fundamental cycle is therefore *3N-1* and the suitable rectifier switching frequency for Sequence F would be 480Hz. But centering the zero vector instead of the active vector in each PWM, the harmonic performance is going to be worst.

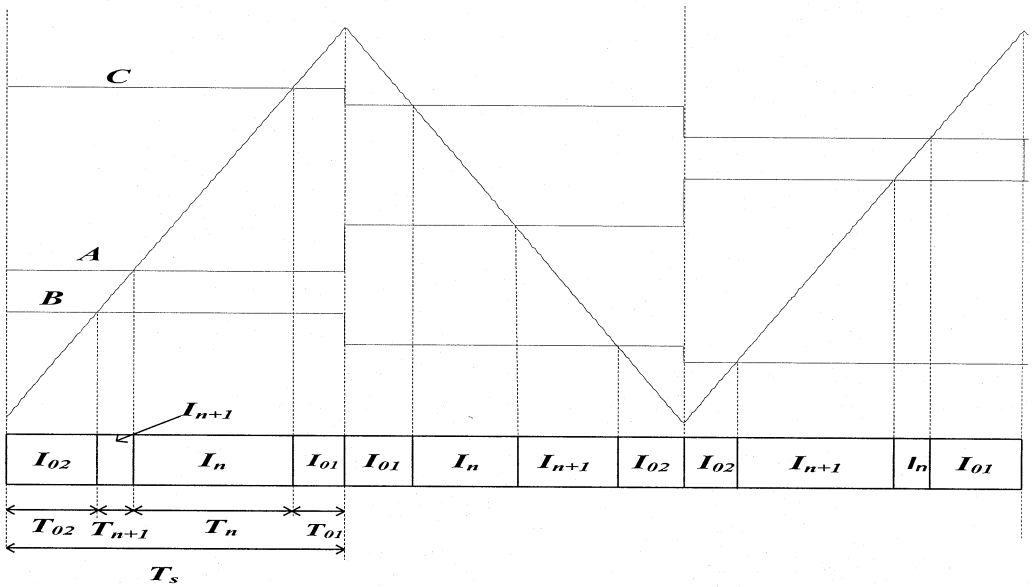


Fig. 2.7 SVPWM of a CSR dwell time T_n, T_{n+1}, T_{01} and T_{02}

To maintain three-phase and half wave symmetries, the space vector sequence should be arranged such that the triangle carrier in Fig. 2.7 starts at a sector boundary and restarts (instead of continue) at each sector crossing. Note the triangle carrier can be started at the positive or negative peak, which results in different sequence (begin with I_{01} or I_{02}), but the harmonic performance of the two alternative sequence are very similar. If the current sequence A B C less than Carrier results in I_{01} and in the next sequence A B C is greater than carrier results in I_{02}.To achieve a rectifier switching frequency around 500Hz, three samples

should be placed in each sector, with a rectifier switching frequency of 540Hz. Furthermore, to avoid the transition of zero states at the sector crossing, special attention should be paid to the zero vectors near a sector boundary. E.g. with the space vector sequence in Fig. 2.7, during a sector crossing, the sequence (I_{02}–I_{n+1}–I_n–I_{01}) will switch to (I_{02}–I_{n+1}–I_n–I_{01}) in next sector. The zero vectors at both sides of the sector boundary must be the same to avoid additional switching, but they cannot be chosen as the zero vector allocated in either of these two sectors (see Fig. 1) as using zero vector in one sector results in one additional switching between the zero vector and its adjacent active vector in the other sector. Therefore the third zero vector should be used during the sector crossing.

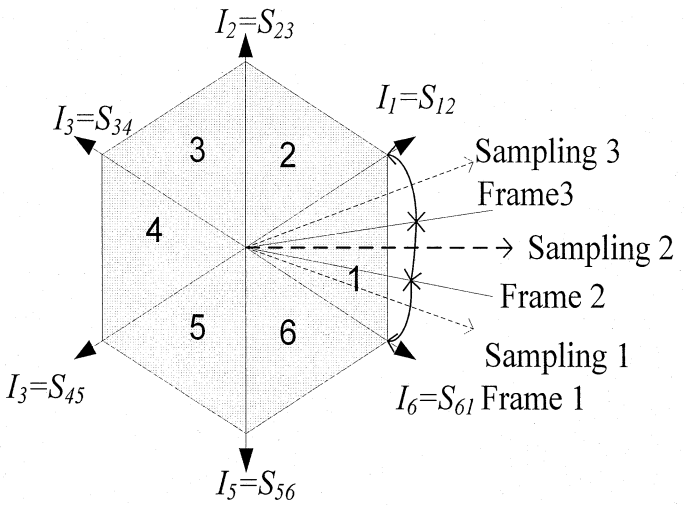


Fig. 2.8 Space vector diagram of a CSR with symmetrical sampling.

Fig. 2.8 shows a symmetrical sampling example which has a sampling frequency of 18 times the fundamental frequency. In sector 1, three sampling PWM frames are placed symmetrically with three sampling points positioned in the center of each frame. By this arrangement, one can avoid the sampling at a sector boundary, and therefore eliminate the minimum pulse width problem associated with GTOs or GCTs.

2.4 Dwell Time Calculation

The space vector modulation for CSR is based on ampere-second balancing principle, that is, the product of the reference vector I_{ref} and sampling period T_s equals the sum of the current vectors multiplied by the time interval of chosen space vectors. The I_n , I_{n+1} are the active space vectors. The I_{01} and I_{02} are the zero space vectors. The triangles in the Fig. 2.9 are considered from the sector 1 of the space vector diagram of Fig 2.1. Fig 2.9 gives the instant of current magnitude with their corresponding dwell time. The space vectors' dwell times T_n, T_{n+1}, T_{01} and T_{02} can be calculated as follows.

Consider the three phase sine wave:

$$A = m_a \sin(\theta_{sec})$$

$$B = m_a \sin(\theta_{sec} - \frac{2\pi}{3})$$

$$C = m_a \sin(\theta_{sec} + \frac{2\pi}{3})$$

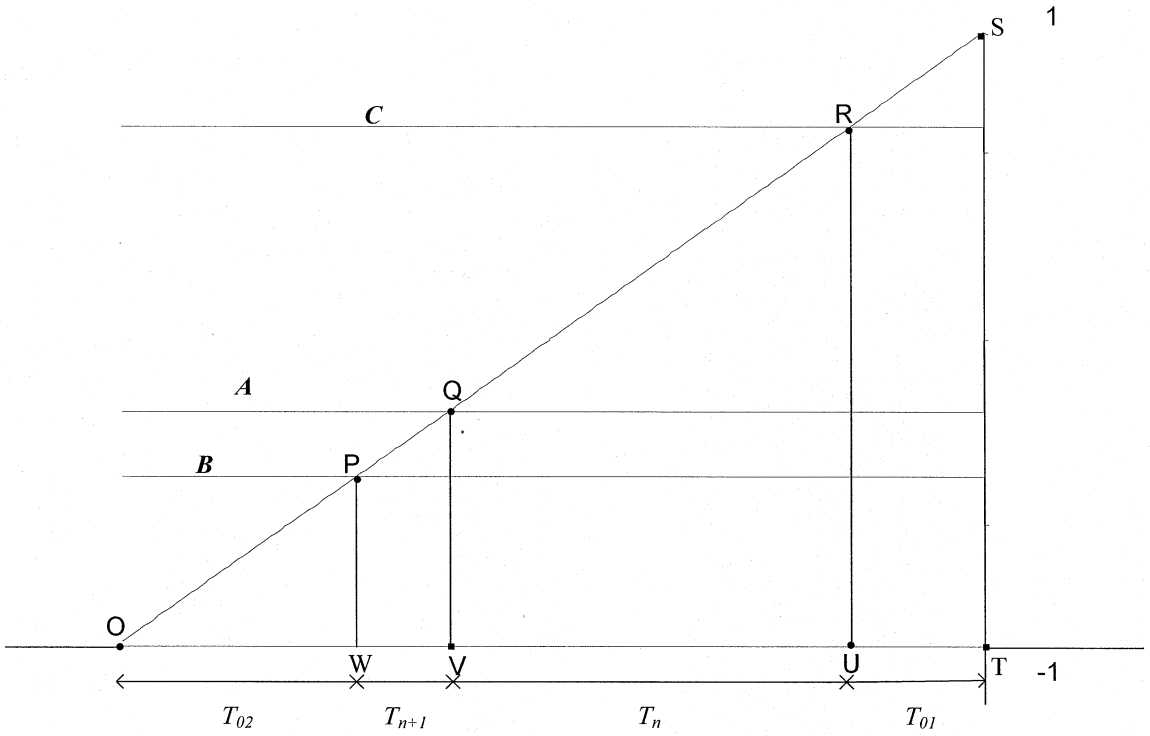


Fig. 2.9 Dwell time T_n, T_{n+1}, T_{01} and T_{02} calculation.

Consider the Fig. 2.9 the triangle **OPWO** and comparing with triangle **OSTO** we can write

$$\frac{PW}{ST} = \frac{OW}{OT}$$

$$\frac{1 + m_a \sin(\theta_{sec} - \frac{2\pi}{3})}{2} = \frac{T_{02}}{T_s}$$; Then solving for T_{o2}

$$T_{02} = T_s.\frac{1}{2}(1+.m_a.\sin(\theta_{\text{sec}} - \frac{2\pi}{3})) \tag{2.2}$$

Consider the Fig. 2.9 the triangle **ORUO** and comparing with triangle **OSTO**

$$\frac{RU}{ST} = \frac{OU}{OT}$$

$$\frac{1+m_a \sin(\theta_{\text{sec}} + \frac{2\pi}{3})}{2} = \frac{T_s - T_{01}}{T_s}$$

Solving for T_{01} we get

$$T_{01} = T_s.\frac{1}{2}(1-.m_a.\sin(\theta_{\text{sec}} + \frac{2\pi}{3})) \tag{2.3}$$

Consider the Fig. 2.9 the triangle **OQVO** and comparing with triangle **OSTO**

$$\frac{QV}{ST} = \frac{OV}{OT}$$

$$\frac{1+m_a \sin(\theta_{\text{sec}})}{2} = \frac{T_{n+1} + T_{02}}{T_s} \tag{2.4}$$

Substituting the value of T_{02} in equation (2.4) and solve for $T_{n+1}(T_2)$

$$T_{n+1} = T_s.\frac{\sqrt{3}}{2}.m_a.\sin(\frac{\pi}{6} + \theta_{\text{sec}}) \tag{2.5}$$

Consider the Fig. 2.9 the triangle **ORUO** and compare with triangle **OSTO**

$$\frac{RU}{ST} = \frac{OU}{OT}$$

$$\frac{1 + m_a \sin(\theta_{sec} + \frac{2\pi}{3})}{2} = \frac{T_n + T_{n+1} + T_{02}}{T_s} \tag{2.6}$$

Substituting the value of T_{n+1} and T_{02} in equation (2.6) and solve for T_n (T_1)

$$T_n = T_s . \frac{\sqrt{3}}{2} . m_a . \sin(\frac{\pi}{6} - \theta_{sec}) \tag{2.7}$$

$$T_0 = T_s - T_n - T_{n+1} \tag{2.8}$$

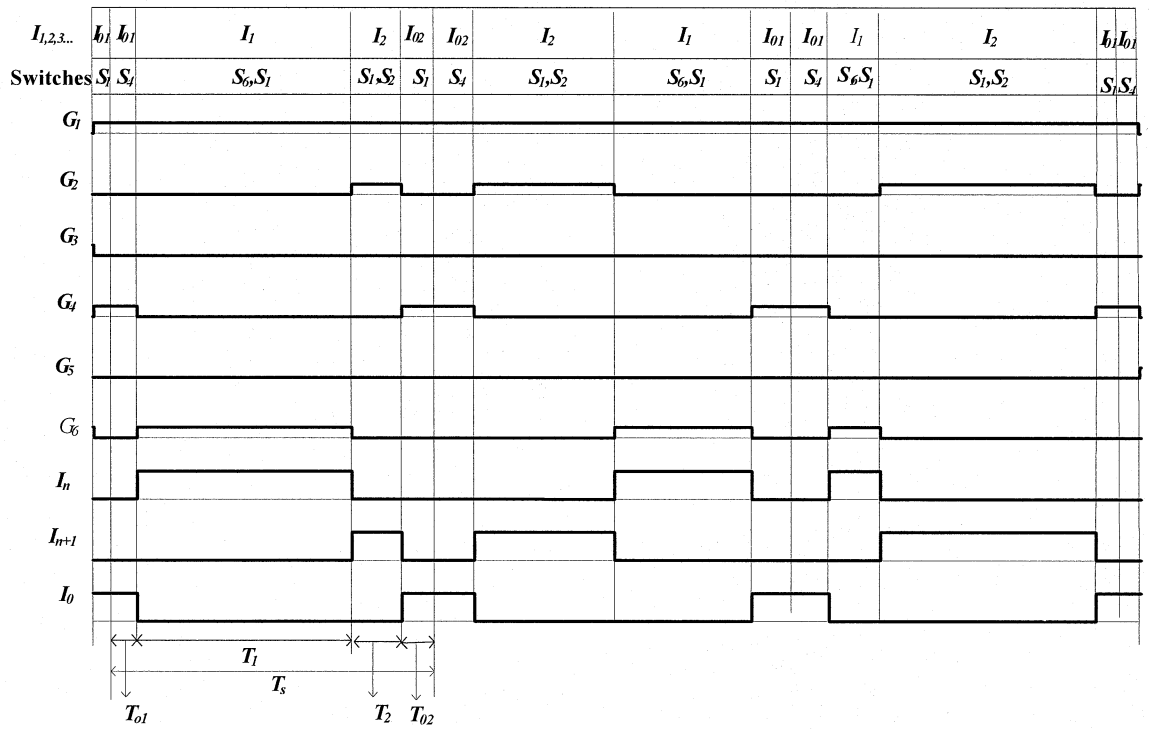
where m_a is the modulation index and θ_{sec} is the angle of the reference current within in a certain space sector ($-\pi/6 < \theta_{sec} < \pi/6$).Therefore, with the current space sector information and the reference vector position within the sector, proper gating pulses can be generated. The modulation index for linear SVM can reach 1.155

2.5 SVM PWM Sequence A at a Rectifier Switching Frequency of 540Hz

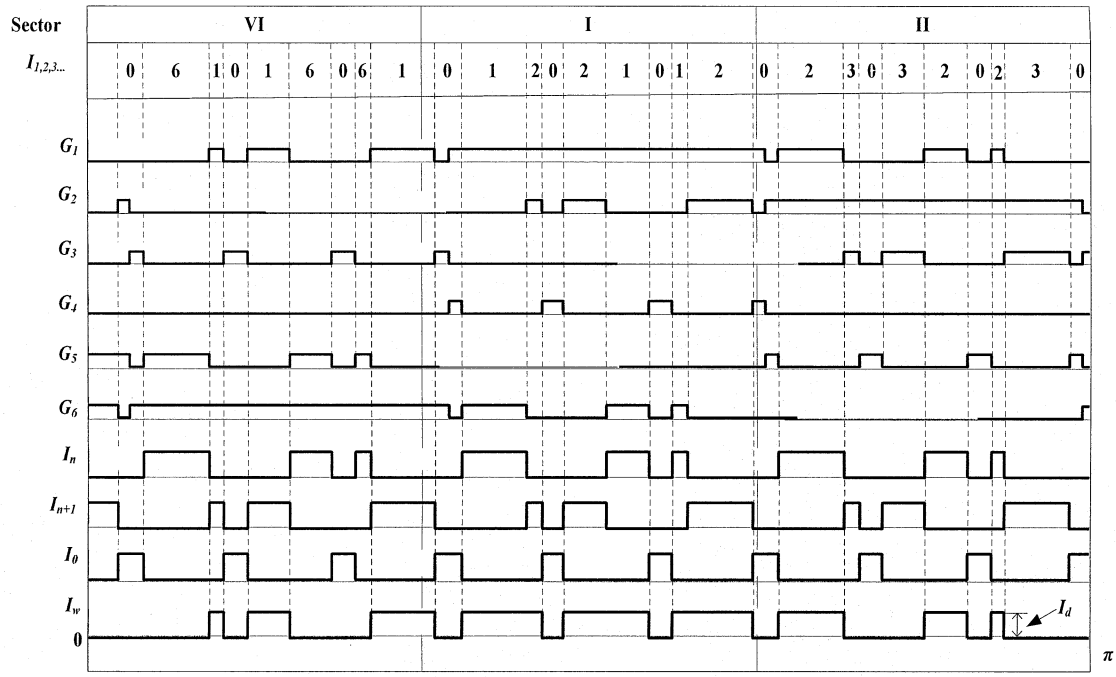
In the sequence A three samples should be used in each sector, resulting in a rectifier switching frequency of 540Hz. The number of pulses in each half cycle is 9.

2.6.1 Switching Sequence A (I_{01}-I_n-I_{n+1}-I_{02}-I_{02}-I_{n+1}-I_n-I_{01})

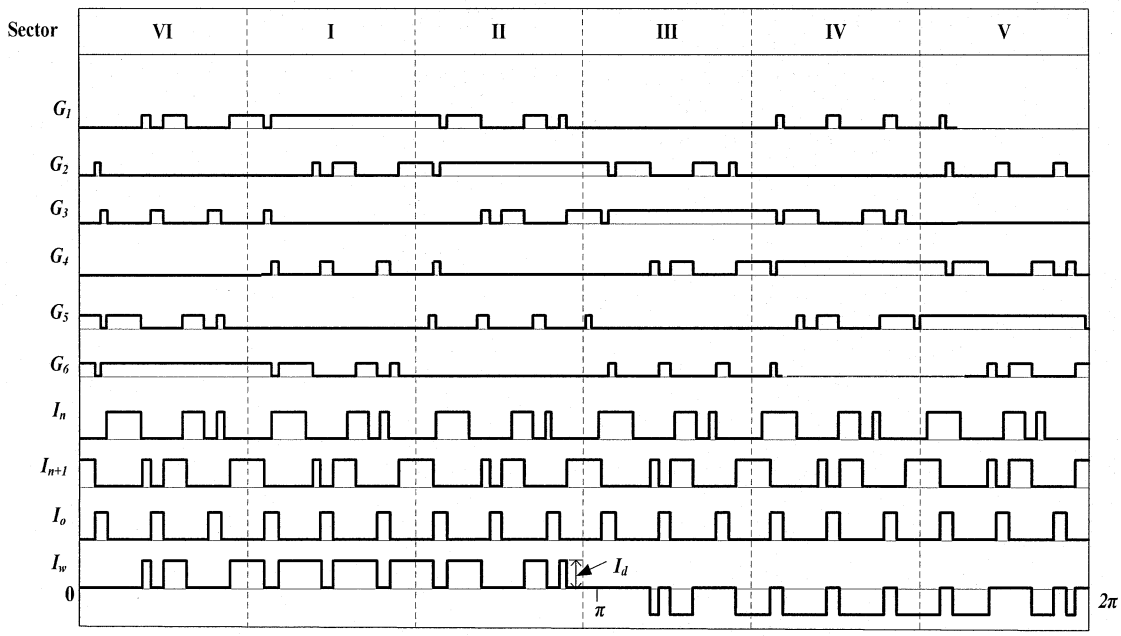
Fig. 2.10(a) shows the four segment sequence A for the reference sector I. The sequence can start as I_{01}-I_n-I_{n+1}-I_{02} *or* I_{02}-I_{n+1}-I_n-I_{01} with close harmonic performance. The sequence should restart at each sector boundary to maintain wave form symmetries as shown in Fig. 2.10(c).



(a) I_{ref} for Sector 1



(b) half fundamental cycle



(c) fundamental frequency cycle

Fig. 2.10 SVM switching sequence A for CSR.

Fig. 2.10(a) shows a four segment sequence for the reference vector I_{ref} residing in sector 1, where G_1 to G_6 are the gate signals for switches S_1 to S_6, respectively. The reference vector is synthesized by I_1, I_2, I_{01} and I_{02}.The sampling period T_s is divided into four segments composed of T_1, T_2, T_{01}, T_{02}.The switching states for vectors I_1 and I_2 are [1 -1 0] and [1 0 -1], and their corresponding on-state switch pairs are (S_1, S_6) and (S_1, S_2).The zero state [2 0 0] is selected for I_{01} and I_{02} their corresponding on-state switch pair are (S_1, S_4) such that the design requirement for CSR is satisfied. Fig. 2.10(b) shows the details of the switching sequence and gate signal arrangement over half fundamental cycle. Fig. 2.10(c) shows the details of the switching sequence and gate signal arrangements over a fundamental frequency cycle and the Sector 1-6 is shown. The rectifier current I_w is having the magnitude of I_d. There are eighteen samples per cycle with only three samples in each sector. It can be observed from Fig. 2.10 such that

- At any time instant, only two switches conduct, one in the top half of the bridge and the other in the bottom half;
- By a proper selection of the redundant switching states for I_{01} and I_{02} the two requirements for switching sequence design are satisfied;
- The dc current I_d is bypassed eighteen times per fundamental frequency cycle by the zero vector. It is the bypass operation that makes the magnitude of i_w adjustable;
- The rectifier PWM current i_w varies one fundamental cycle when the reference vector I_{ref} goes through all six sectors once;

- The rectifier switching frequency f_{sw} can be calculated by $f_{sw} = f_1 \times N_p$; f_1 =60 and N_p=9; f_{sw} = 60*9 =540Hz
- The sampling frequency is $f_{sp} = 1/T_s$, which relates the rectifier switching frequency by $f_{sw} = f_{sp}/2$; f_{sp} = 1080Hz and f_{sw} = 540Hz

The maximum rms fundamental-frequency current that can be found from

$$I_{w1} = \frac{m_{a,\max} \times I_d}{\sqrt{2}} = 0.707 I_d \qquad \text{for} \quad m_{a,\max} = 1$$

The SVM usually requires a reference vector, which is of magnitude I_{ref} and frequency of supply. The dwell time generate the two gating signals G_1 and G_4 for the upper and lower switches S_1 and S_4 respectively. The PWM current I_w contains no even-order harmonics due to its half-wave symmetrical waveform.

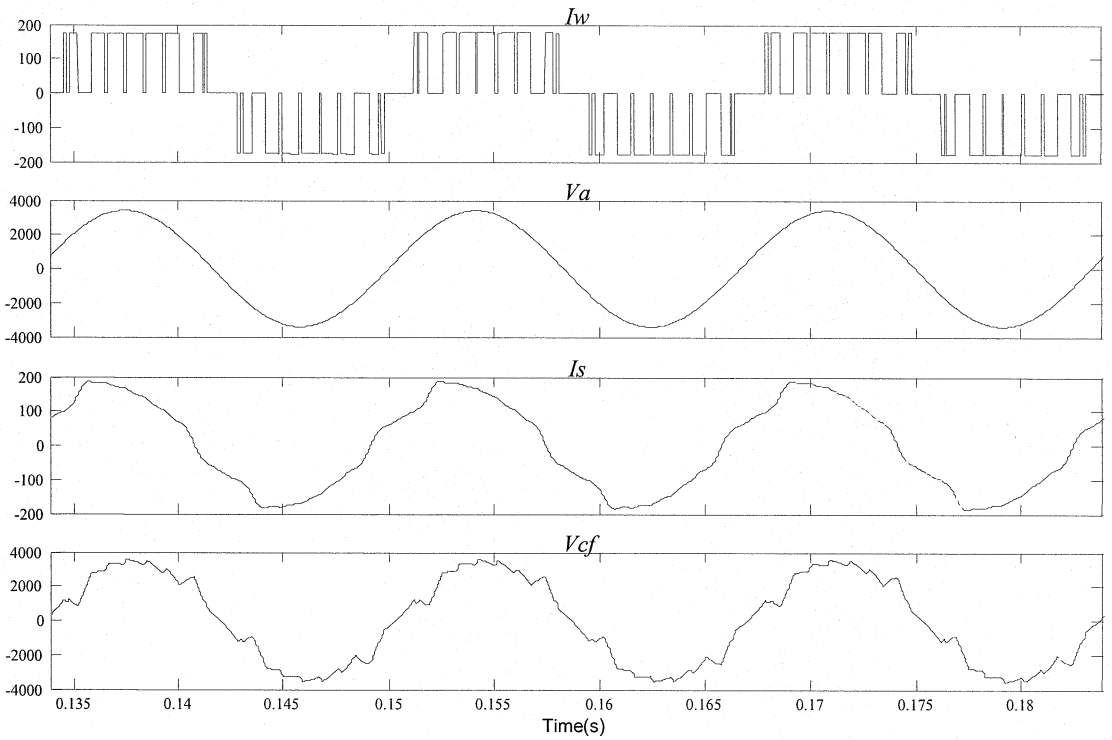


Fig. 2.11 Simulated waveform of rectifier current (I_w), phase voltage (V_a), line current (I_s) and capacitor voltage (V_{cf}) for Sequence A at m_a=0.9.

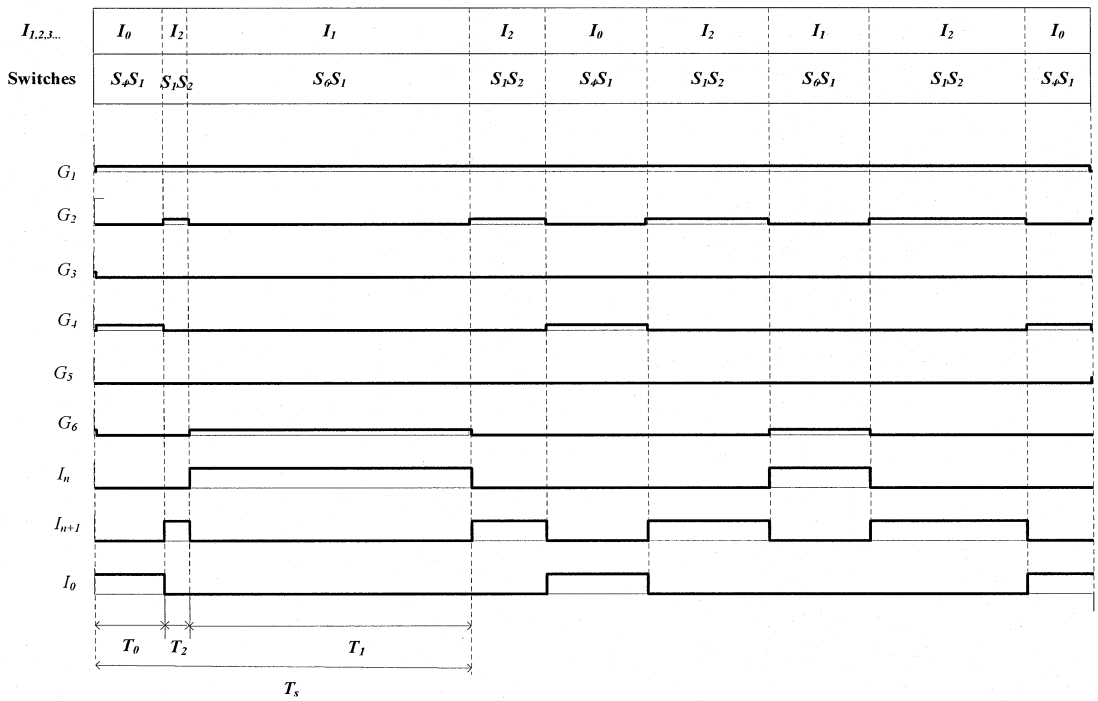
The Fig. 2.11 shows the typical simulated waveform of rectifier current, phase voltage, line current and capacitor voltage of CSR for open loop operation under the Sequence A at rated condition respectively. The rectifier current is having 9 pulses per half cycle. The rectifier switching frequency is 540Hz.

2.7 SVM PWM Sequence B at a Rectifier switching frequency of 480Hz

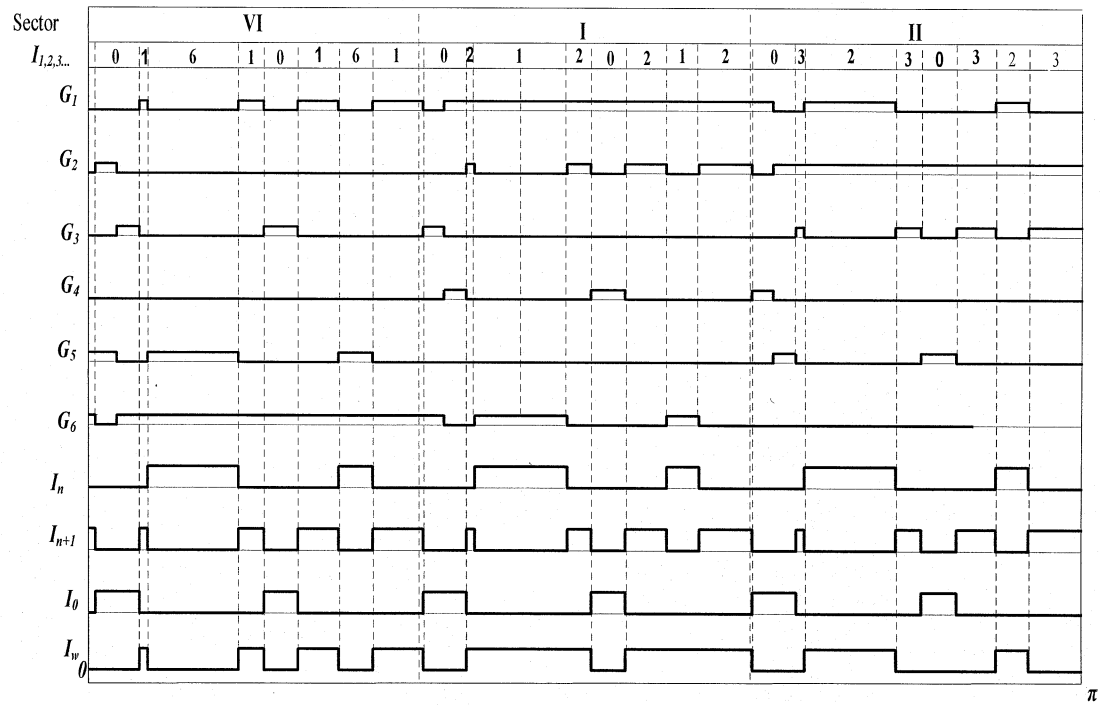
For Sequence B, if the number of sequences in each sector is 2, the number of pulses per half cycle will be 8 and the rectifier switching frequency will be 480 Hz.

2.7.1 Switching Sequence B (I_0-I_{n+1}-I_n-I_n-I_{n+1}-I_0)

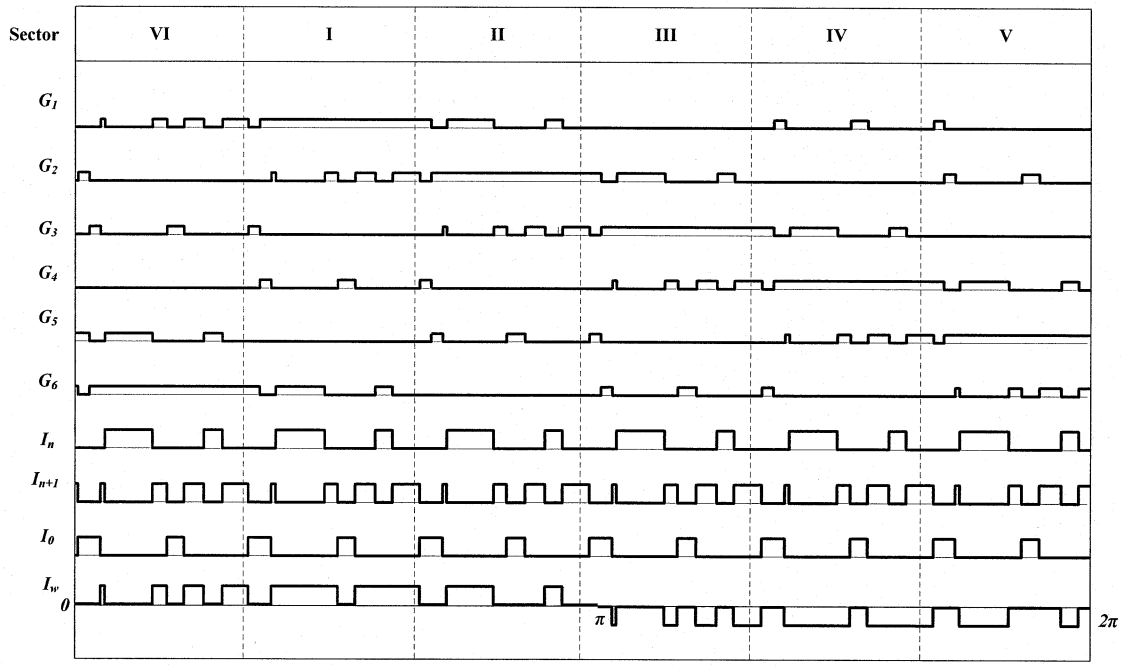
The sequence B can start as I_0-I_{n+1}-I_n *or* I_n-I_{n+1}-I_0 results in same performance. The sequence B is derived from sequence A.



(a) I_{ref} for Sector 1



(b) half fundamental cycle



(c) fundamental frequency cycle

Fig. 2.12 SVM switching sequence B for CSR.

Fig. 2.12 (a) shows a typical three segment sequence for the reference vector I_{ref} residing in sector 1, where G_1 to G_6 are the gate signals for switches S_1 to S_6,respectively.The reference vector is synthesized by I_1, I_2, I_{01} and I_{02}.The sampling period Ts is divided into three segments composed of T_1, T_2, T_0.The switching states for vectors I_1 and I_2 are [1 -1 0] and [1 0 -1],and their corresponding on-state switch pairs are (S_1, S_6) and (S_1, S_2).The zero state [2 0 0] is selected for I_0 their corresponding on-state switch pair are(S_1, S_4) such that the design requirement for CSR is satisfied. Fig. 2.12 (b) shows the details of the switching sequence and gate signal arrangement over half fundamental cycle. Fig. 2.12 (c) shows the details of the switching sequence and gate signal arrangements over a fundamental frequency cycle. For Sequence B, if the number of sequences in a sector is N, the number of pulses per half cycle will be 4N and the rectifier switching frequency will be 240N Hz. A suitable rectifier switching frequency for waveform symmetries will be 480Hz.

It can be observed from Fig. 2.12 such that

- At any time instant, only two switches conduct, one in the top half of the bridge and the other in the bottom half;
- By a proper selection of the redundant switching states for I_0, the two requirements for switching sequence design are satisfied;
- The dc current I_d is bypassed twelve times per fundamental frequency cycle by the zero vector. It is the bypass operation that makes the magnitude of I_w adjustable;
- The rectifier PWM current I_w varies one fundamental cycle when the reference vector I_{ref} goes through all six sectors once;
- The rectifier switching frequency f_{sw} can be calculated by $f_{sw} = f_1 \times N_p$; $f_1 = 60$Hz and $N_p = 8$, $f_{sw} = 8*60 = 480$Hz.
- The sampling frequency is $f_{sp} = 1/T_s$, which relates the rectifier switching frequency by $f_{sw} = f_{sp}/2$; $f_{sp} = 960$Hz and $f_{sw} = 480$Hz.

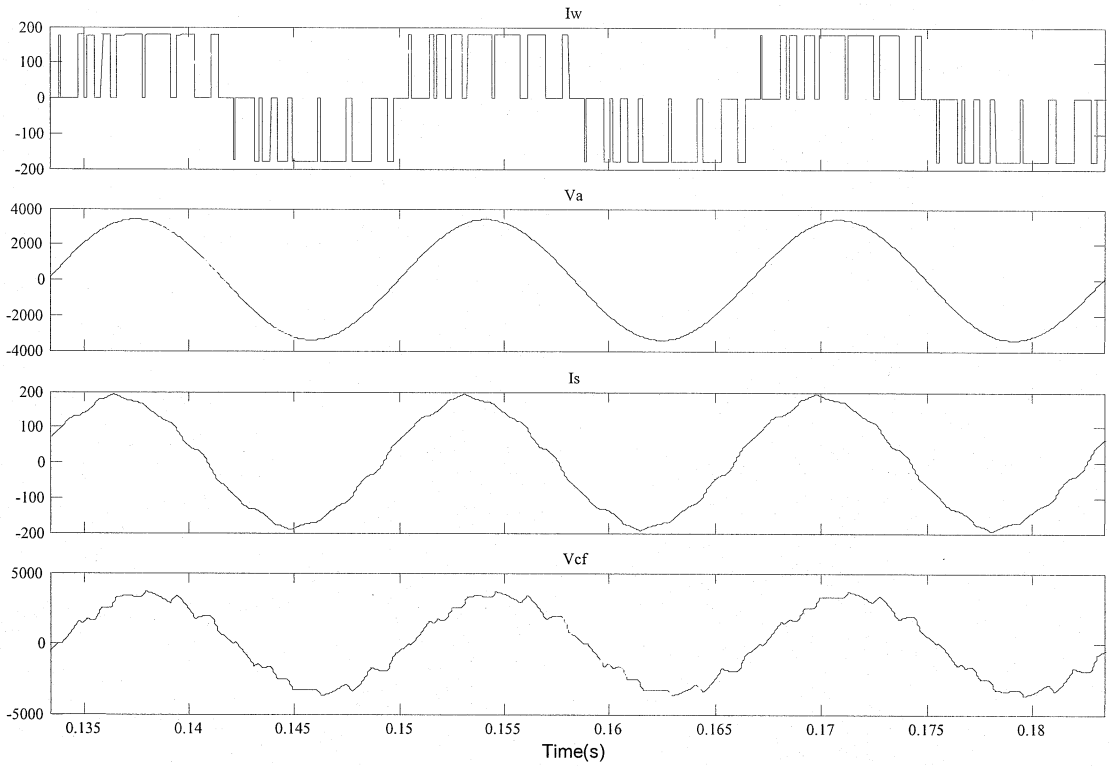


Fig. 2.13 Simulated waveform of rectifier current (I_w), phase voltage (V_a), line current (I_s) and capacitor voltage (V_{cf}) for Sequence B at $m_a = 0.9$.

Fig. 2.13 show the simulated waveform of rectifier current, phase voltage, line current and capacitor voltage of CSR for open loop operation under the Sequence B best sequence at rated condition. The rectifier switching frequency is 480Hz. The PWM pulses per half cycle is 8.The input supply frequency is 60Hz. Observing the waveform of line current I_s in Fig. 13 we can see clearly the Sequence B is good. The harmonic analysis for these sequences is explained in detail in chapter 4.

2.8 Summary

In this chapter, different space vector sequences suitable for a current source rectifier are investigated. Three sampling PWM frames are placed symmetrically with three sampling points positioned in the center of each frame. By this arrangement, one can avoid the sampling at a sector boundary, and therefore eliminate the minimum pulse width problem

associated with GTOs or GCTs. The zero vectors at both sides of the sector boundary must be the same to avoid additional switching, but they cannot be chosen as the zero vector allocated in either of these two sectors as using zero vector in one sector results in one additional switching between the zero vector and its adjacent active vector in the other sector. The Dwell time calculation from graphical approach is discussed. Details of sequence arrangements of sequence A and sequence B to achieve waveform symmetries with minimum rectifier switching frequency are discussed. The remaining sequence C, D, E, and F provided in Appendix C. The typical simulated waveform of rectifier current, phase voltage, line current and capacitor voltage of CSR is discussed. The harmonic content comparison with different sequence is discussed in detail in Chapter 4.

Chapter 3 Analysis of SVM PWM Sequence

3.1 Introduction

Space vector PWM schemes for high power current source rectifier normally produce low order harmonics and sub-order harmonics due to the low rectifier switching frequency. To achieve best harmonic performance, different space vector sequences suitable for a current source rectifier are investigated. New regulations impose more stringent limits to current harmonics injected by power converters, what is achieved with pulse width modulated rectifiers. For the grid connected current source rectifier, the input line current instead of the switching current is strictly regulated by the harmonic guidelines such as IEEE standard 519. Therefore, the line current harmonics of each space vector sequence should be considered and the performance is to be evaluated.

3.2 Theoretical Performance of PWM strategies

There are essentially two major classes of PWM – naturally and regular sampled (both symmetric and asymmetric). In terms of base band harmonic performance, these classes refer to the nature of the signal waveform supplied to modulator. Both types of modulation can be implemented using analog technology, although the regular sampled approach is more commonly applied to digital implementations.

Theoretical solutions for either class of PWM strategy can be obtained using double integral Fourier analysis of the Switched waveform [19] and lead to a general solution of:

$$F(t) = \frac{A_{00}}{2} + \sum \{A_{0n}\cos(n\omega_0 t) + B_{0n}\sin(n\omega_0 t)\}$$
$$+ \sum_{m=1}^{\infty} \{A_{m0}\cos(m\omega_c t) + B_{m0}\sin(m\omega_c + n\omega_c t)\}$$
$$+ \sum_{m=1}^{\infty} \sum_{n=-\infty,\neq 0}^{\infty} \{A_{mn}\cos(m\omega_c + n\omega_0) + B_{mn}\sin(m\omega_c + n\omega_0)\}$$

The general solution consist of (dc offset, fundamental and base band harmonics) + (carrier harmonics) + (carrier sideband harmonics) in all harmonic calculation. In either

sequence, the consequence is to advantage modulation schemes that reduce low order harmonics in favor of higher order harmonics. Hence " better" sequence(modulation) strategies simply distribute their harmonics at the expense of increased magnitude higher order harmonics(which is regarded as easier to filter).Selection between sequence strategies is then really a selection of which strategy distributes more of its harmonic energy into higher frequency spectrum under the operating conditions of interest.

$$DF = \frac{100}{H(1)}\sqrt{\sum_{n=2}^{\infty}\left(\frac{H(n)}{n^2}\right)^2}$$

where H (n) is the r.m.s value of the nth harmonic component. With consideration of only the second order term in the LC filter, [20] is valid only at high order harmonics for evaluation of fast switching converter applications.

Harmonics in power PWM systems are unavoidable because of the switched nature of the modulation process, and the development of a common performance index to compare different PWM schemes has been a major research interest for many years. One well known index is THD. It is immediately obvious that I_{rms} for a waveform which switches between $+I_{dc}$ and $-I_{dc}$, i_w is always I_{dc}, and that THD as defined by Appendix A is therefore always constant irrespective of modulation strategy.

While the specifics of the harmonics produced by the various modulation strategies are complex. Most researchers usually resolve this dilemma in one of
Two ways, viz:

- Implicitly or explicitly limit the number of harmonics to be included in the THD calculation (a simple band stop function), or;
- Use an alternative performance parameter such as Weighted THD, Distortion Factor or HDDF [20], which rolls off the impact of higher order harmonics on the performance index and hence gives them preference.

The IEEE 519-1992 harmonic limits [21] are a function of the ratio of line short circuit, I_{sc}, to drive rated current, I (line-line). For ratios below twenty, the harmonic current

limits expressed in terms of Total Demand Distortion (TDD) are given in Table 3.1. This measure differs from total harmonic distortion since harmonic content is measured relative to drive rated current. Overall current TDD must be less than five percent.

Table 3.1 IEEE-519-1992 Harmonic Current Limit Requirements

Harmonic(h) Range	TDD Limit
1 < h < 13	4% h odd-1% h even
11 < h < 19	2% h odd-0.5% h even
17 < h < 25	1.5% h odd-0.375% h even
23 < h < 35	0.6% h odd-0.15% h even

3.3 Analysis of THD for different SVM Sequence

The current source rectifier is analyzed at modulation index m_a =0.95 with resistive load and constant power output in steady state.

3.3.1 Rectifier Current Harmonic Analysis

The current source rectifier switching current harmonic content is analyzed for six space vector PWM sequence.

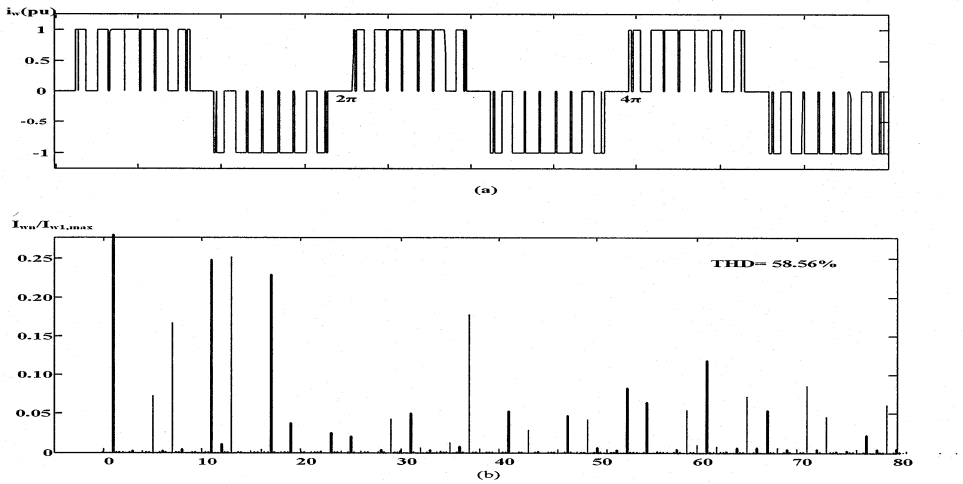


Fig. 3.1 Waveforms produced by SVM CSR _ Sequence A with f_{sw} = 540,N_p=9 and m_a=0.95 (a) Rectifier current i_w (b) Harmonic spectrum.

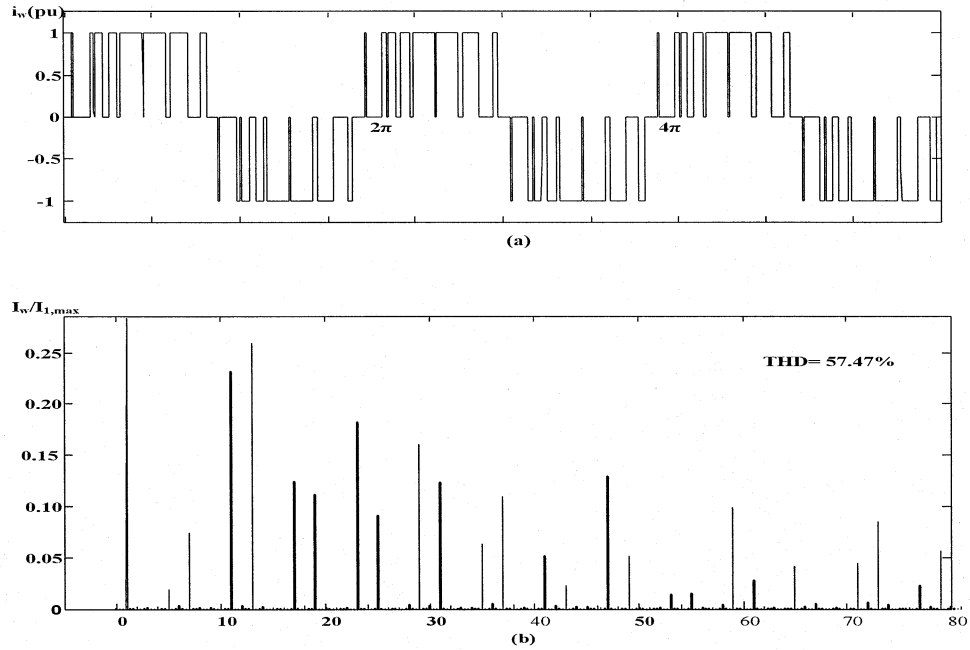


Fig. 3.2 Waveforms produced by SVM CSR _ Sequence B with f_{sw} = 480,N_p=8 and m_a=0.95 (a) Rectifier current i_w (b) Harmonic spectrum.

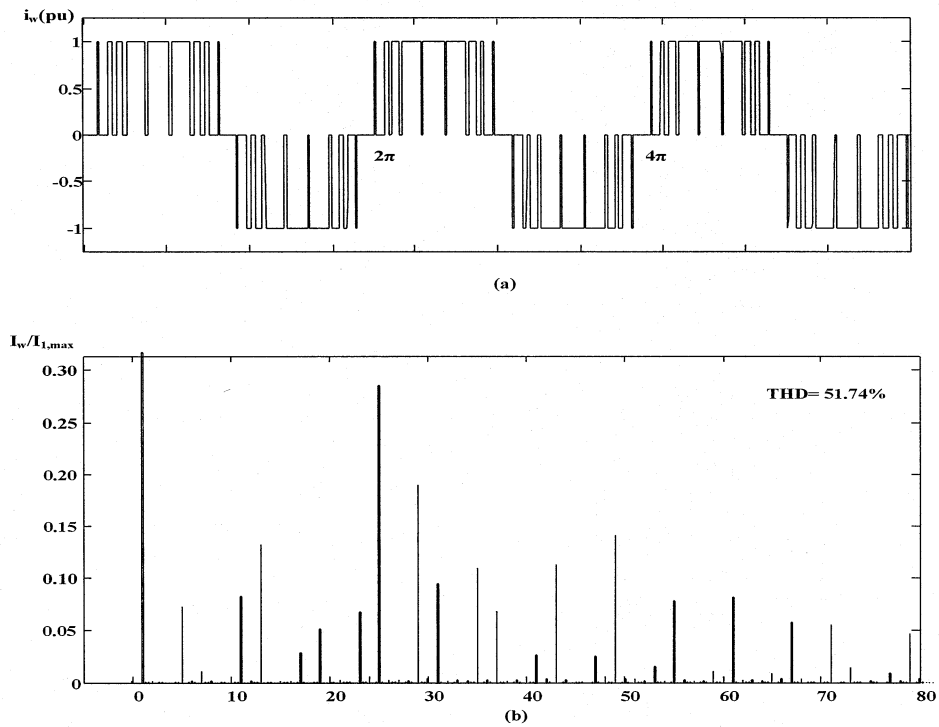


Fig. 3.3 Waveforms produced by SVM CSR _ Sequence C with f_{sw} = 540, N_p=9 and m_a=0.95 (a) Rectifier current i_w (b) Harmonic spectrum.

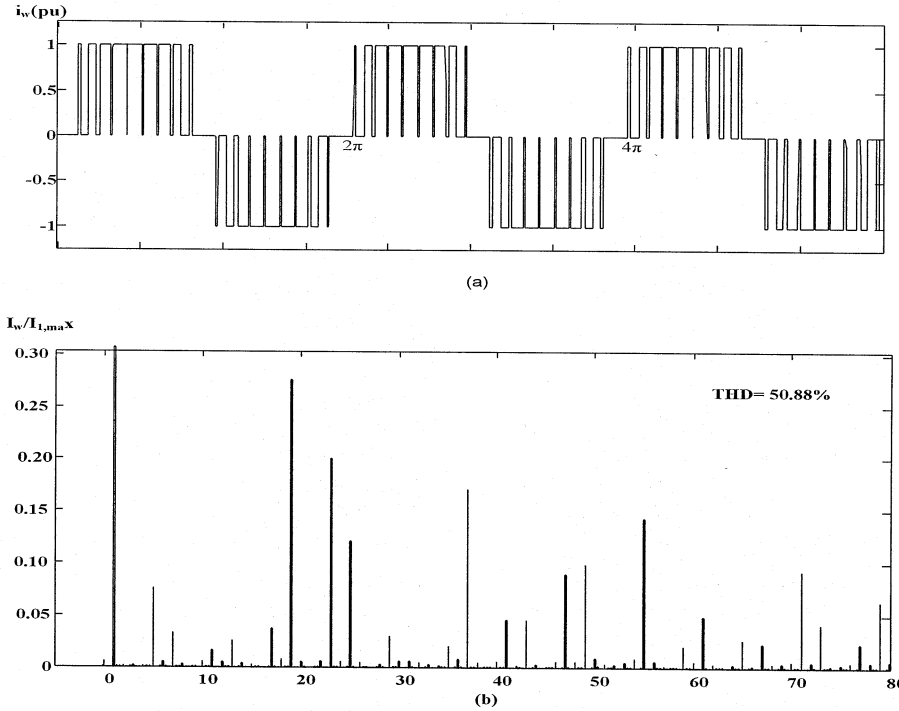


Fig. 3.4 Waveforms produced by SVM CSR _ Sequence D with f_{sw} = 540, N_p=9 and m_a=0.95 (a) Rectifier current i_w (b) Harmonic spectrum.

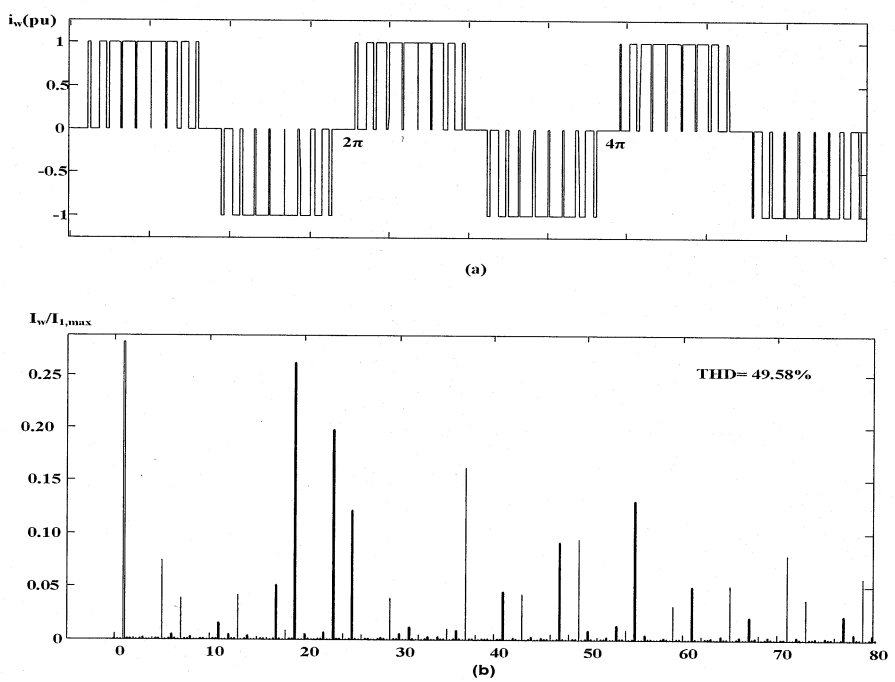
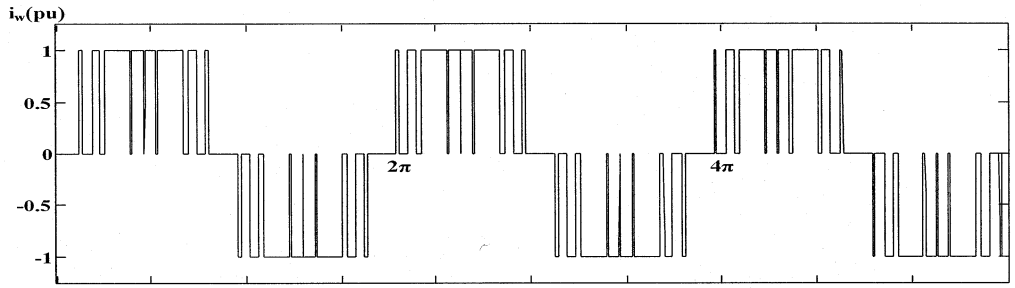
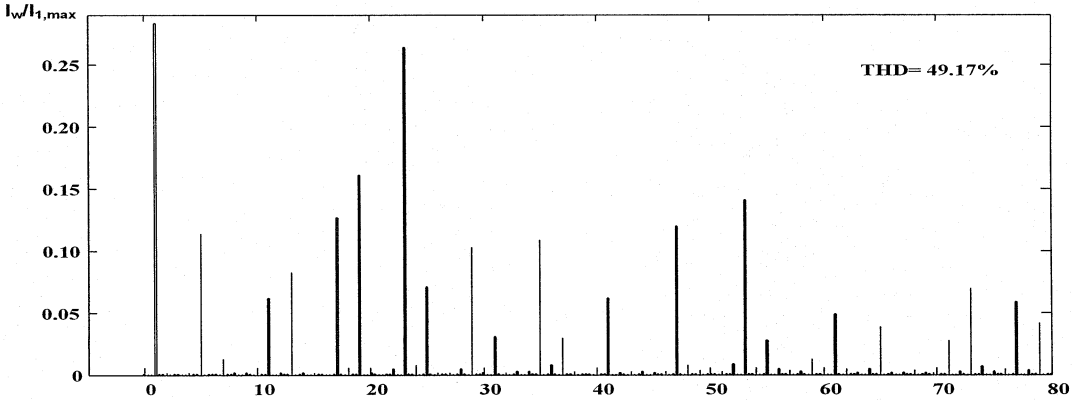


Fig. 3.5 Waveforms produced by SVM CSR _ Sequence E with f_{sw} = 540, N_p=9 and m_a=0.95 (a) Rectifier current i_w (b) Harmonic spectrum.



(a)



(b)

Fig. 3.6 waveforms produced by SVM CSR _ Sequence F with f_{sw} = 480, Np=8 and m_a=0.95 (a) Rectifier current i_w (b) Harmonic spectrum.

The THDs is high in the Sequence B and Sequence C is due to the high order harmonics (such as 11th, 13th and 17th) and if implemented on a CSR, those high order harmonics can be attenuated effectively by the input filter.

Fig. 3.2 and 3.4 shows the simulation waveforms of CSR switching and its frequency spectrum with asynchronous PWM (Sequence B) and synchronous PWM (Sequence E) respectively. It clearly shows that the lower order harmonics magnitude is low in both the sequence under the certain operating condition.

3.3.2 Input Line Current Harmonic Analysis

The current source rectifier is analyzed for input current and harmonic content at constant power with resistive load.

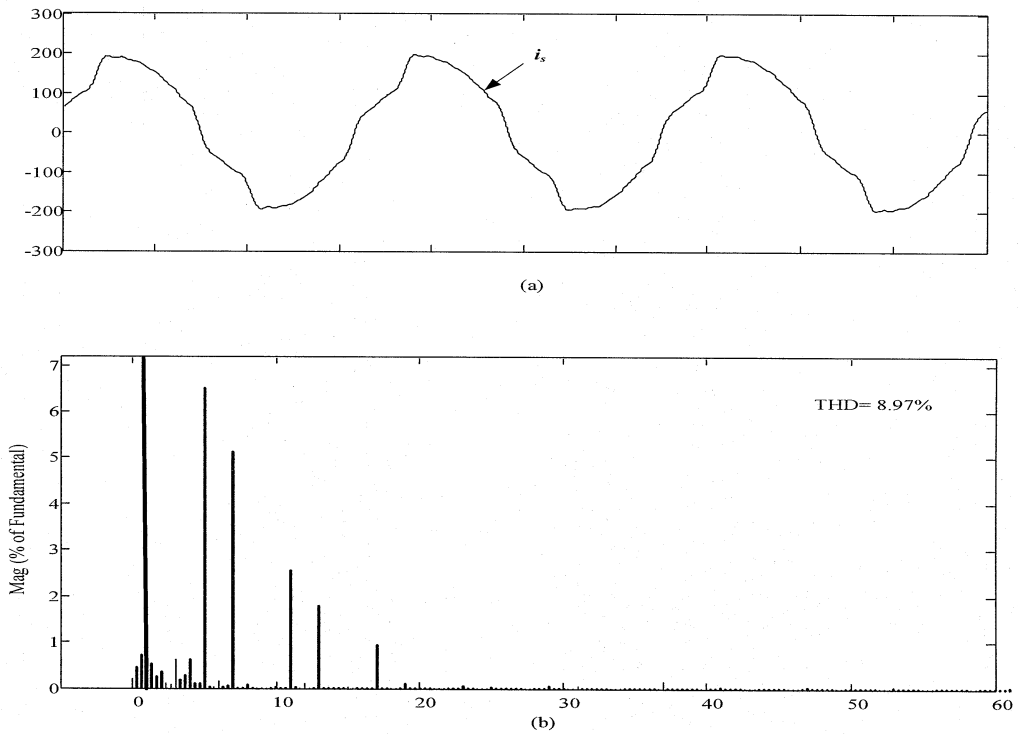


Fig. 3.7 Waveforms produced by SVM CSR _ Sequence A with m_a=0.95
(a) Input supply current i_s (b) Harmonic spectrum.

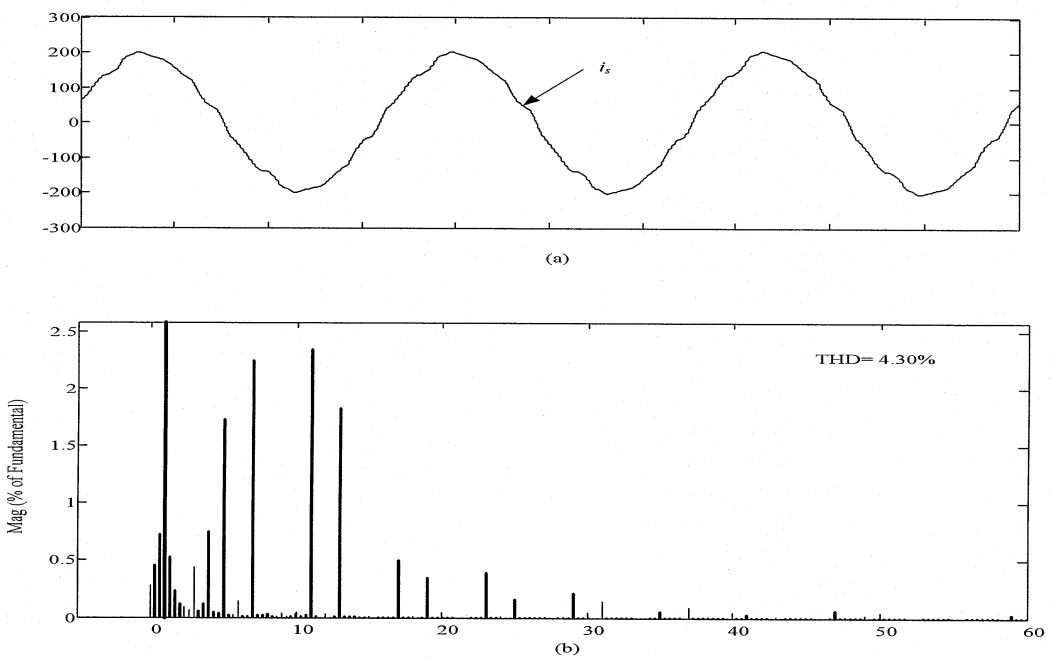


Fig. 3.8 Waveforms produced by SVM CSR _ Sequence B with m_a=0.95
(a) Input supply current i_s (b) Harmonic spectrum.

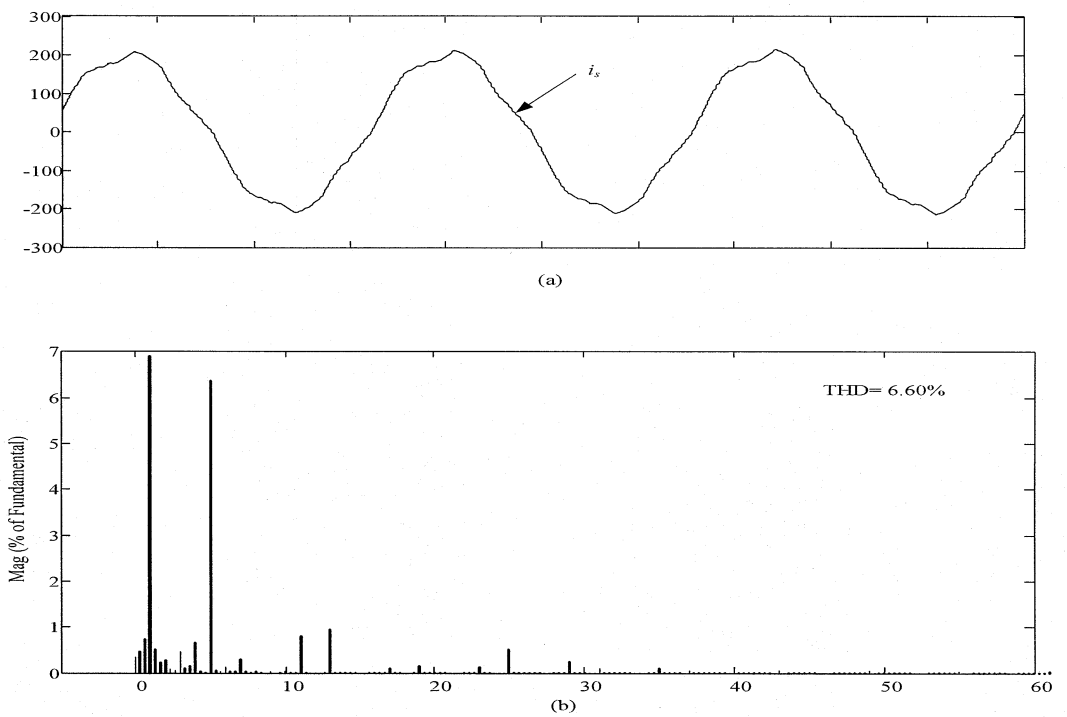


Fig. 3.9 Waveforms produced by SVM CSR _ Sequence C with m_a=0.95
(a) Input supply current i_s (b) Harmonic spectrum.

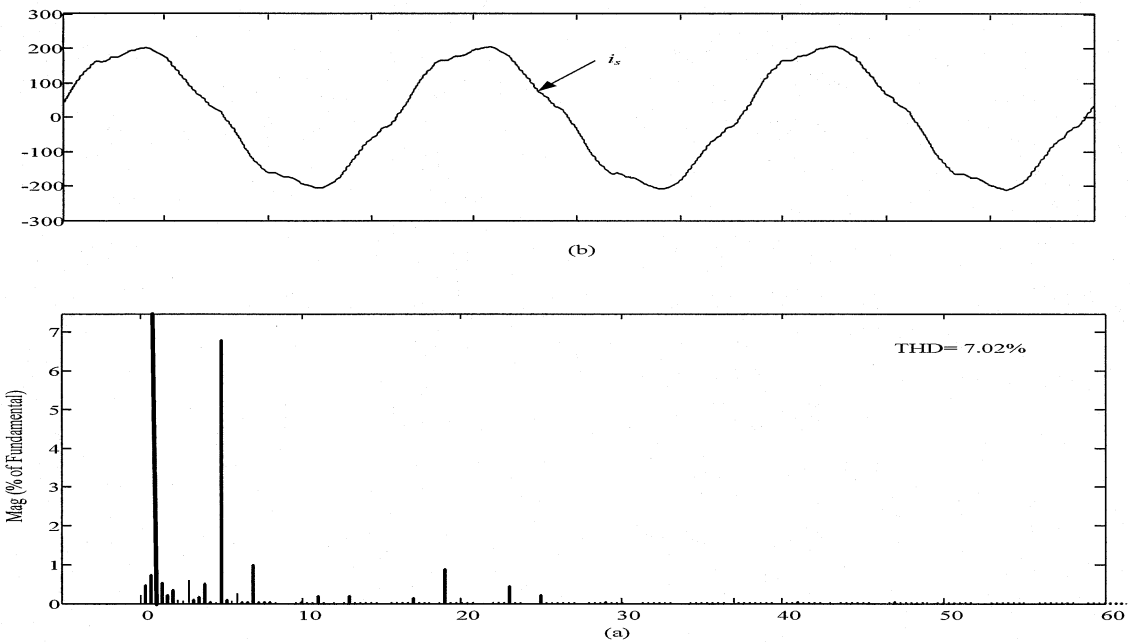


Fig. 3.10 Waveforms produced by SVM CSR _ Sequence D with m_a=0.95
(a) Input supply current i_s (b) Harmonic spectrum.

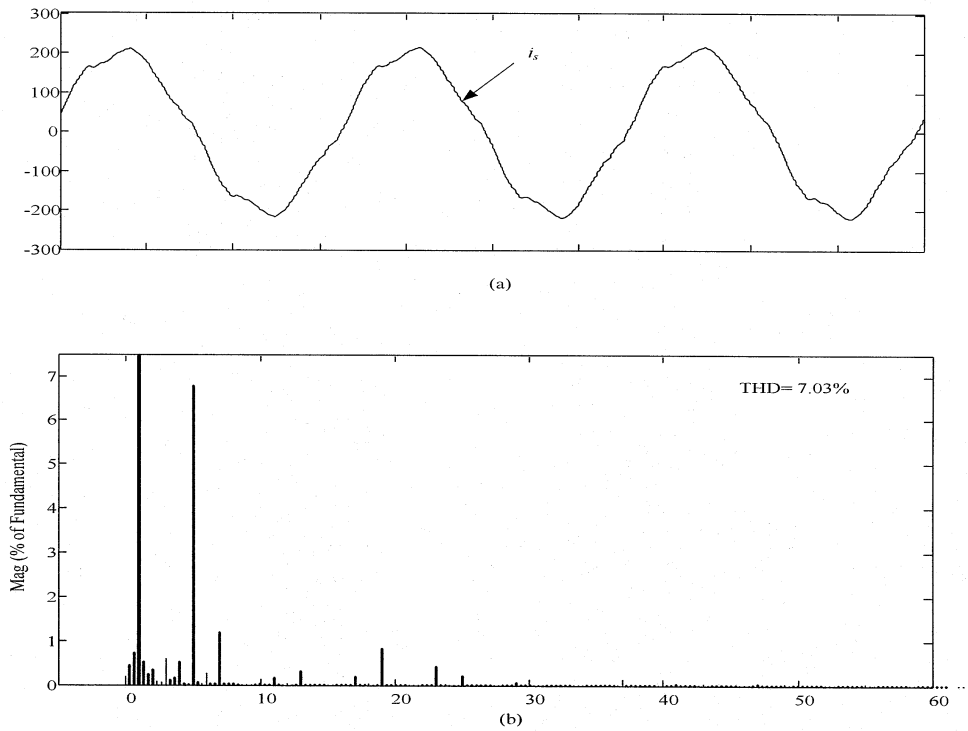


Fig. 3.11 Waveforms produced by SVM CSR _ Sequence E with m_a=0.95
(a) Input supply current i_s (b) Harmonic spectrum.

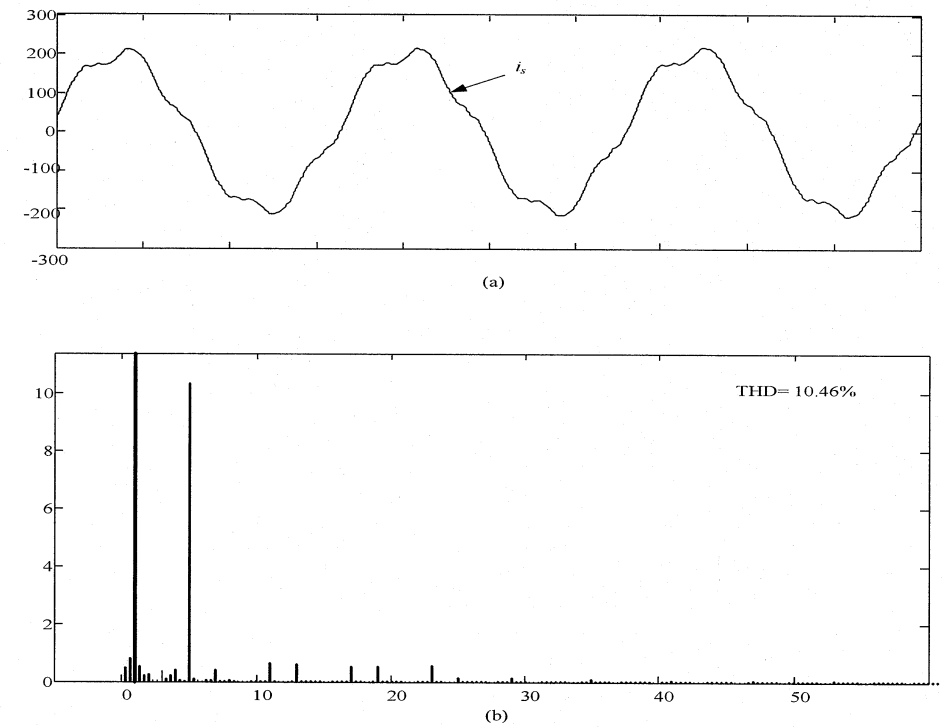


Fig. 3.12 Waveforms produced by SVM CSR _ Sequence F with m_a=0.95
(a) Input supply current i_s (b) Harmonic spectrum.

Fig. 3.7 to 3.12 shows an input line current and its harmonic spectrum of the SVM PWM of six sequences. If you observe the harmonic spectrum of the sequence B which is having a lower THD compared to other six sequences. The line current THD of sequence B is 4.3% which is less than the IEEE-519 recommendation. The sequence C, THD is 6.60%, sequence D and E THD is around 7 %.The sequence A THD is 8.96 % and sequence F THD is 10.46% which is the worst compared to the other sequences.

3.4 SVM Pulse-Width Modulation

Fig. 3.13 to 3.18 shows a set of typical waveform of the SVM PWM of six sequence ,where V_a is phase A input voltage, I_s is the input current, V_{cf} is voltage across the capacitor and I_w is the rectifier current. The line current waveform of the sequence B looks pure sinusoidal. The phase voltage magnitude of the capacitor is almost equal to that of supply phase voltage if we neglect the line drop.

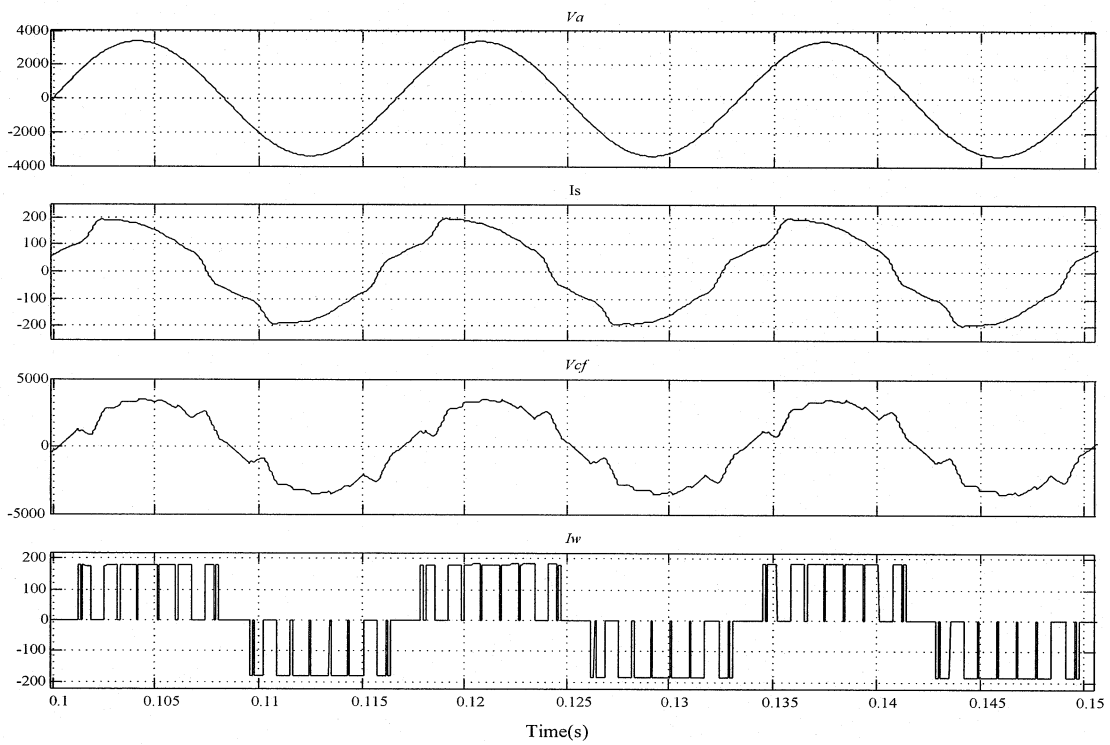


Fig.3.13 Simulated waveform of SVM for Sequence A with f= 60Hz, f_{sw} = 540Hz, m_a=0.95.

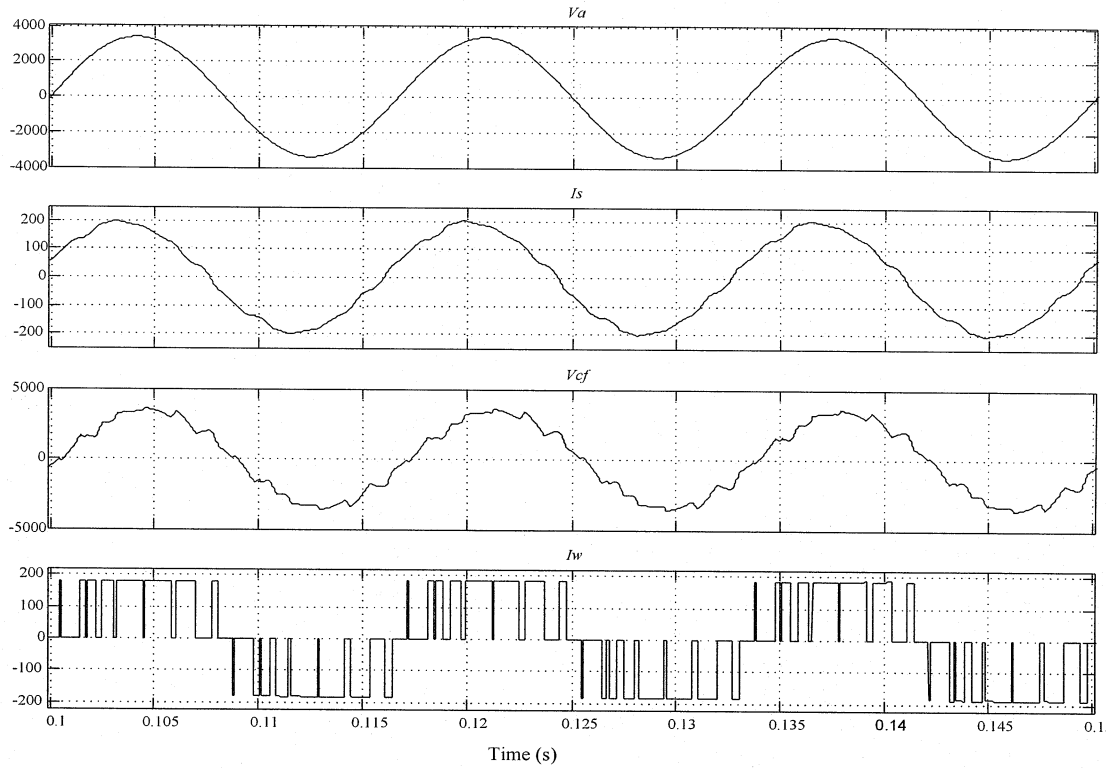


Fig.3.14 Simulated waveform of SVM for Sequence B with f= 60Hz, f_{sw} = 540Hz, m_a =0.95.

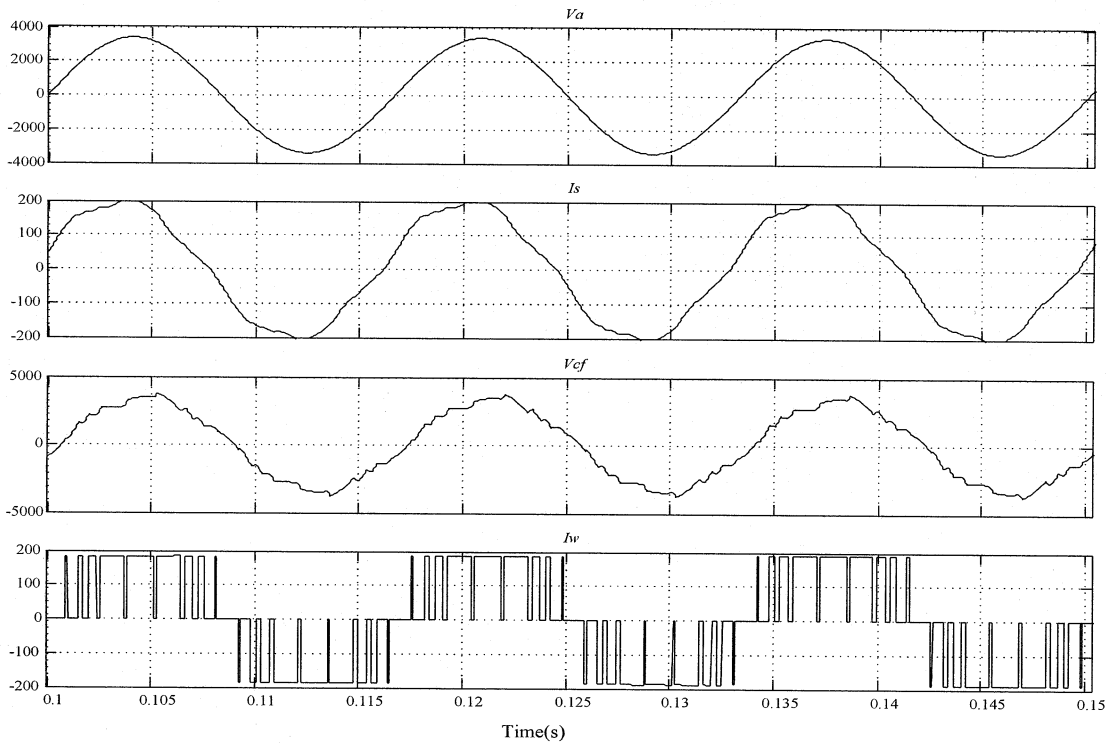


Fig. 3.15 Simulated waveform of SVM for Sequence C with f= 60Hz, f_{sw} = 540Hz, m_a =0.95.

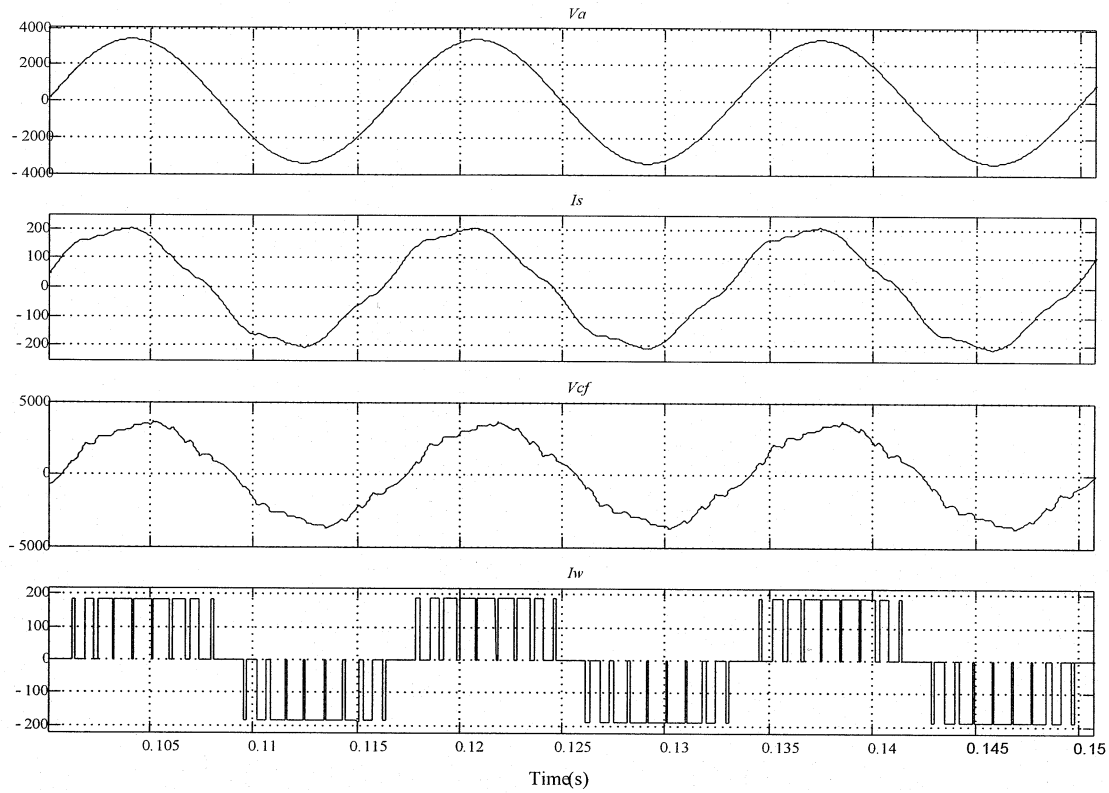


Fig. 3.16 Simulated waveform of SVM for Sequence D with f= 60Hz, f_{sw} = 540Hz, m_a=0.95.

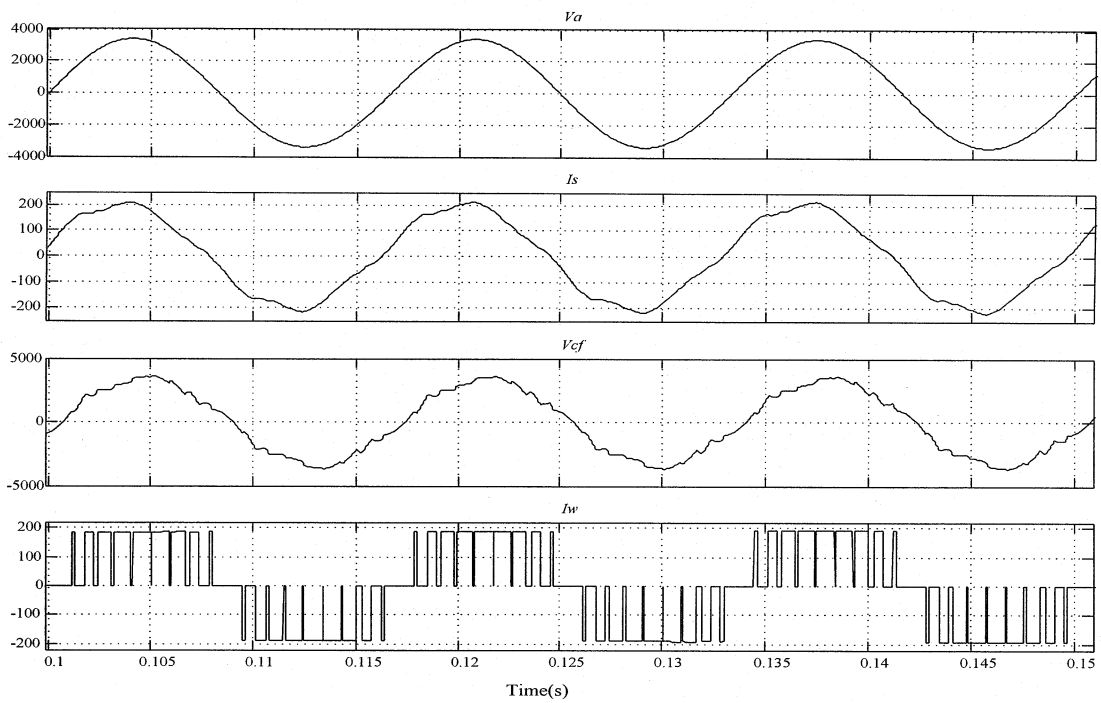


Fig.3.17 Simulated waveform of SVM for Sequence E with f= 60Hz, f_{sw} = 540Hz, m_a=0.95.

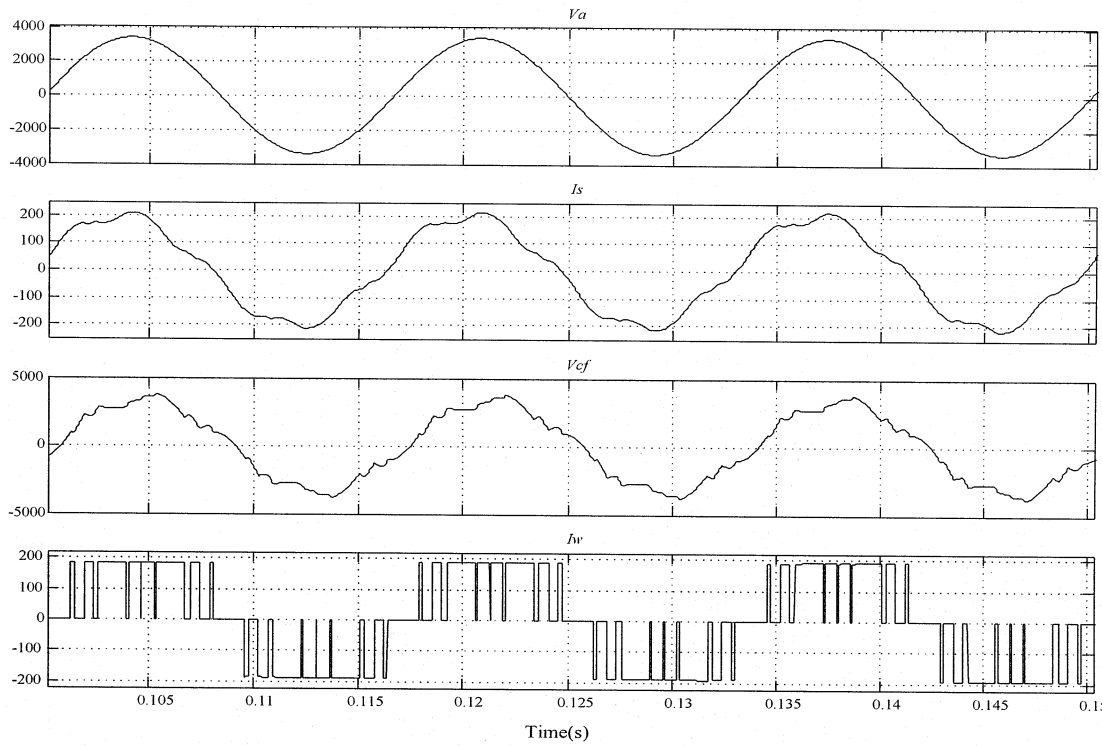


Fig.3.18 Simulated waveform of SVM for Sequence F
with f= 60Hz, f_{sw} = 480Hz, m_a =0.95.

3.5 SVM Sequence Performance Evaluation

In this section the current source rectifier is analyzed for lower order harmonics of six SVM sequence.

3.5.1 Analysis of Lower Order Harmonic for Different Space Vector Sequence

The space vector PWM six sequences are analyzed for lower order harmonic rectifier current for a variation with modulation index. Observing Fig. 3.19 and 3.20 one can find that Sequence B, C, D, and E are worth for further investigation.

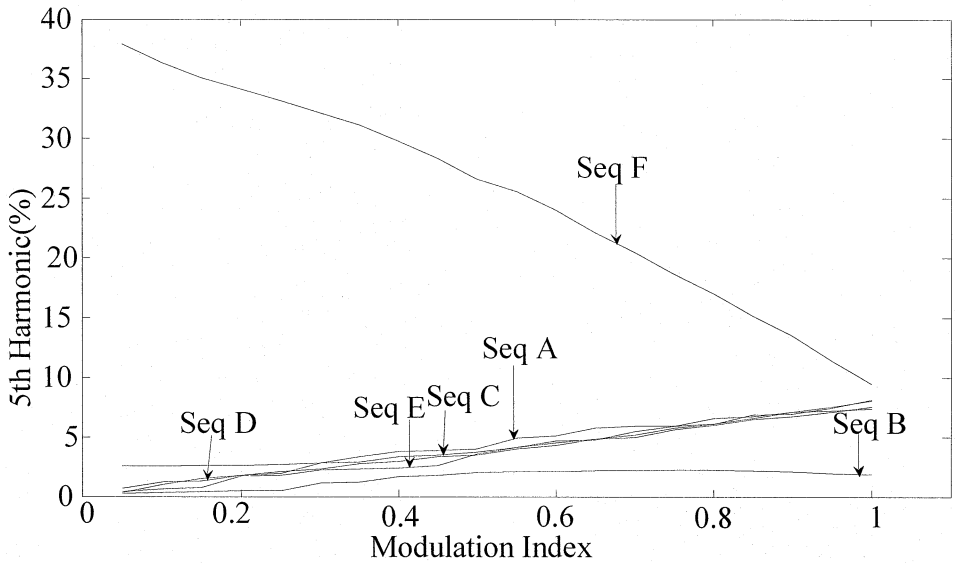


Fig. 3.19 5th Harmonic of CSR switching current.

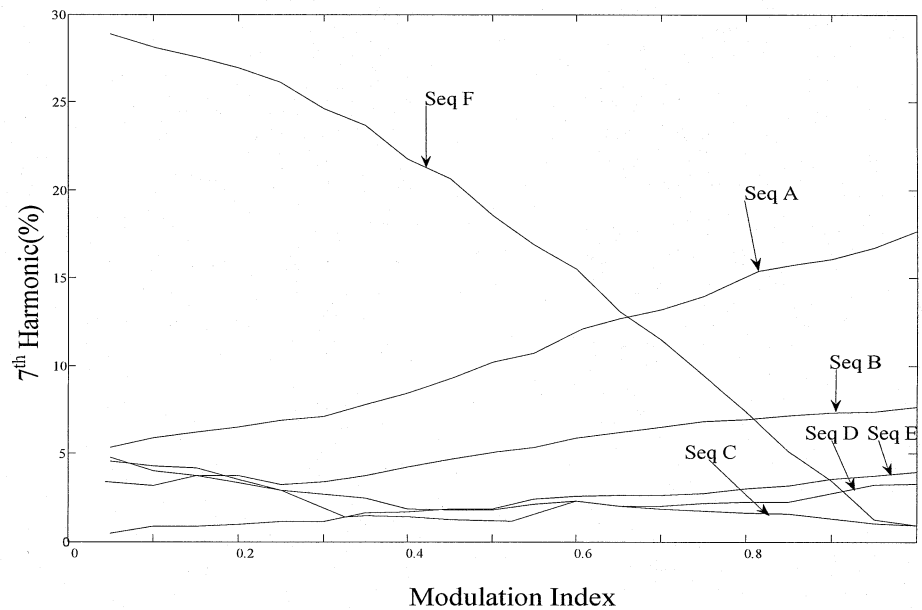


Fig. 3.20 7th Harmonic of a CSR switching current.

The large harmonics at both 5th and 7th orders make Sequence A unsuitable for the high power CSR. Due to the placement of zero vectors at the side, Sequence D has better harmonic performance than Sequence E especially at low modulation index. The Sequence E is recommended to be used at m_a<085 (light load condition) due to its best harmonic performance and easy implementation. On the other hand, when m_a>0.85, Sequence B is the best sequence as it gives the lowest THD in this range. In addition

Sequence B is implemented with lower rectifier switching frequency and therefore with lower switching losses, which is especially beneficial under heavy loading conditions with a higher modulation index (m_a>0.85).

Fig. 3.19 and 3.20 show the 5th and 7th harmonic of CSR switching current for the Sequence A to Sequence F. Which clearly indicate that the performance of Sequence B is best among other sequence under certain operating condition. The sequence A and F whose lower order harmonic content 5th and 7th is high compared to other sequences.

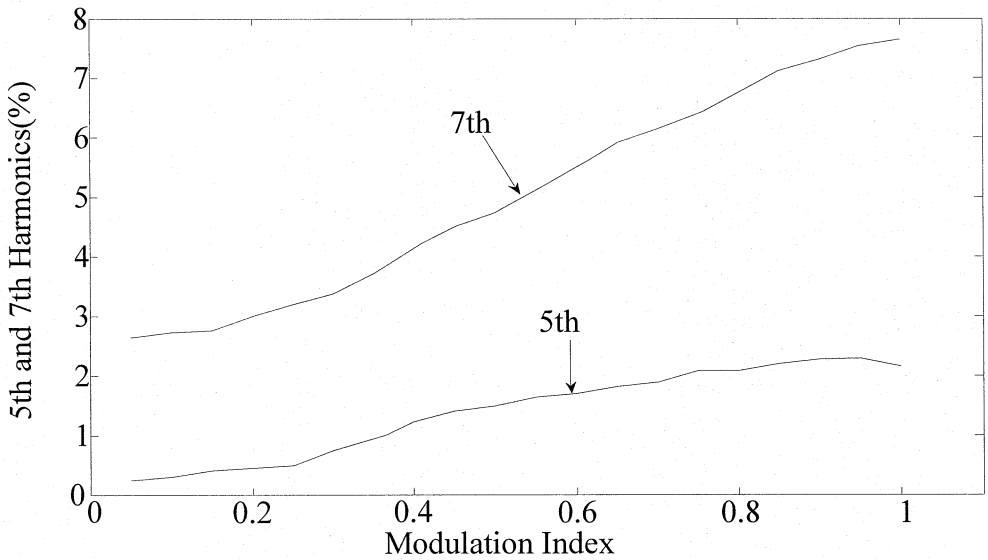


Fig. 3.21 5th and 7th Harmonics of a Sequence B.

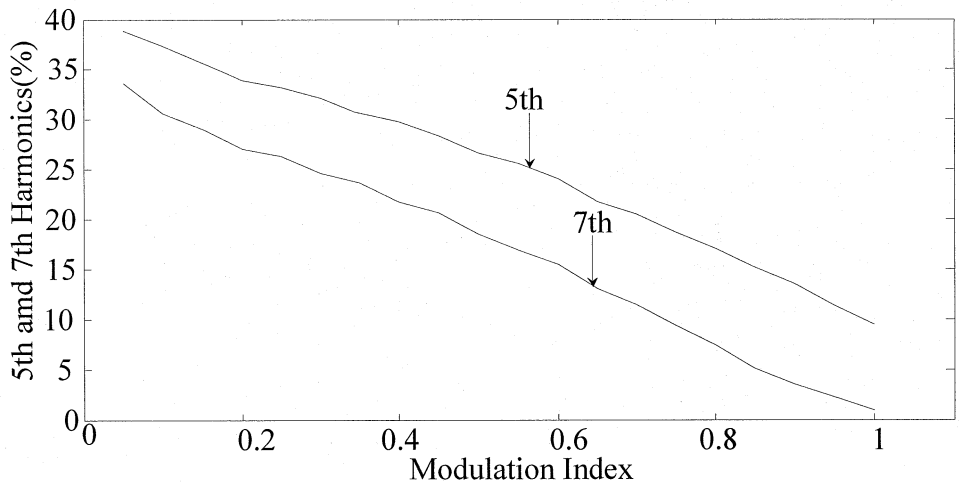


Fig. 3.22 5th and 7th harmonics of a Sequence F.

Fig. 3.21 and 3.22 shows the lower order harmonic contents 5th and 7th for the sequence B and Sequence F respectively. The 5th and 7th harmonic of sequence B at m_a=0.95 is 1.89% and 7.32% respectively. On the other hand 5th and 7th harmonic for sequence F at m_a =0.95 is 11.4% and 1.26% respectively. The lower order harmonics for Sequence F is too high. Fig. 3.23 show the THD of switching current for all the six sequence. Observing the THD graph we can say THD will be very high when modulation index is low as the modulation index increases the THD decreases.

3.5.2 Analysis of THD for Different Space Vector Sequence

Table 3.2 gives the data of the lower order harmonic content from 5th to 25th. There is no even order harmonics since the wave form is half wave symmetrical. The Table 3.3 gives the switching current THD of different sequence at m_a=0.95.

Table 3.2 Switching current of 5th to 25th harmonics at m_a = 0.95

Harmonics	**5**	**7**	**11**	**13**	**17**	**19**	**23**	**25**
Sequence A	7.37%	16.67%	24.84%	25.24%	22.95%	3.79%	2.55%	2.03%
Sequence B	1.89%	7.32%	23.34%	26.16%	12.58%	11.29%	18.3%	9.13%
Sequence C	7.13%	1.02%	8.01%	13.39%	3.02%	4.83%	6.86%	28.54%
Sequence D	7.54%	3.29%	1.68%	2.58%	3.76%	27.56%	20.02%	12.14%
Sequence E	7.49%	3.97%	1.61%	4.18%	5.08%	26.18%	19.76%	12.19%
Sequence F	11.4%	1.26%	6.21%	8.27%	12.73%	16.07%	26.45%	7.01%

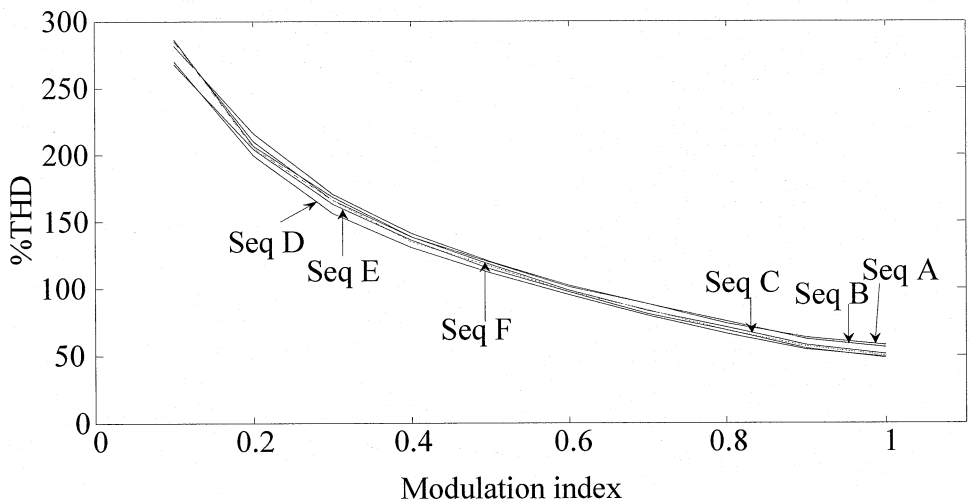


Fig. 3.23 THD of CSR switching current.

Table 3.3 Switching current THD of different sequence at m_a=0.95

Sequence	Switching Current THD
A	58.36%
B	57.63%
C	51.71%
D	50.93%
E	49.64%
F	49.25%

3.5.3 Analysis of Line Current THD for Different Space Vector Sequence

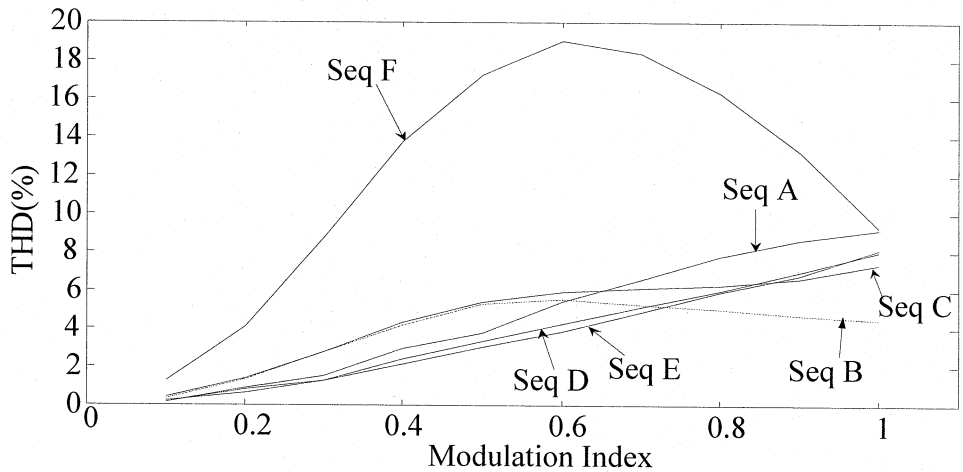


Fig. 3.24 THD of line current for a different sequence.

To improve the line current harmonics under SVM and to avoid the possible LC resonance caused by the input filter, the LC cutoff frequency should be selected such that it will not obviously amplify the 5th and 7th harmonics in the CSR switching current. The Sequence B as shown in Fig. 3.24 meets the IEEE recommendation of THD of 5% especially at higher modulation index (m_a>0.85).For grid connected CSR, the input line current (or filtered current) instead of the switching current is strictly regulated by the harmonic guidelines such as IEEE standard 519 in North America [11].Therefore, the line current harmonics of each space vector sequence should be considered. The Table 3.4 gives the data of line THD of different sequence at m_a =0.9. Table 3.5 provides the simulation parameters for the SVM PWM for Sequence A to Sequence F.

Table 3.4 Line current THD of different sequence at m_a=0.9

Sequence	Line Current THD
A	8.62%
B	4.68%
C	6.61%
D	6.99%
E	6.81%
F	13.26%

Table 3.5 Simulation system parameters

Parameters	**Simulation**
Nominal grid line-line Voltage(rms)	4160V
Nominal Power	1MVA
Frequency	60Hz
Rectifier switching frequency	480/540Hz
Sampling frequency for Virtual R loop	3240Hz
Sampling frequency for DC current loop	1080Hz
Equivalent input filter inductance(L_f+L_s)	0.2.p.u
Equivalent input filter resistance(R_f+R_s)	0.03 p.u
Input filter capacitance(C_f)	0.3 p.u
DC link Inductance (L_d)	2 p.u
DC load (R_{load})	0.35 p.u

3.6 Summary

In this chapter, different space vector sequences suitable for a Current Source Rectifier simulation is carried out and their harmonic performance is compared. Details of sequence arrangements to achieve waveform symmetries with minimum rectifier switching frequency are discussed in chapter 2. A thorough comparison of the harmonic performance of different space vector sequences is carried out in this chapter. The most suitable space vector sequences are identified at light/heavy loading conditions respectively with consideration of minimal THD and switching losses.

The performance of input current waveforms with their harmonic contents is investigated. It can be concluding that:

1) The current waveforms, harmonic content are consistence with the IEEE -519 requirement for current source rectifier;
2) The proposed space vector pulse width modulation first choice is sequence B and second choice is sequence E are the two best sequence out of six different SVM sequence; and
3) The performance of the proposed SVM-PWM sequence is verified by the experiment.

Chapter 4 Experiment

4.1 Introduction

A prototype converter system is used to verify the performance of the proposed six SVM sequences. In this chapter the constructed 208V, 10kVA GCT based CSR experimental set up and the DSP-FPGA control system are described. The experimental waveform of rectifier current and line current is explained. The prototype operation and protection are discussed. The experimental results of the harmonic contents of the input current and switching currents are discussed. The measured waveforms will be analyzed and compared with the simulation results.

4.2 CSR Prototype Configuration

To experimentally verify the proposed six SVM sequence for harmonic analysis, a scaled 208V, 10 kVA hardware prototype of the PWM CSR has been constructed. The circuit diagram of the CSR experimental setup is shown in Fig. 4.1 and the photo of the prototype is shown in Fig. 4.2.

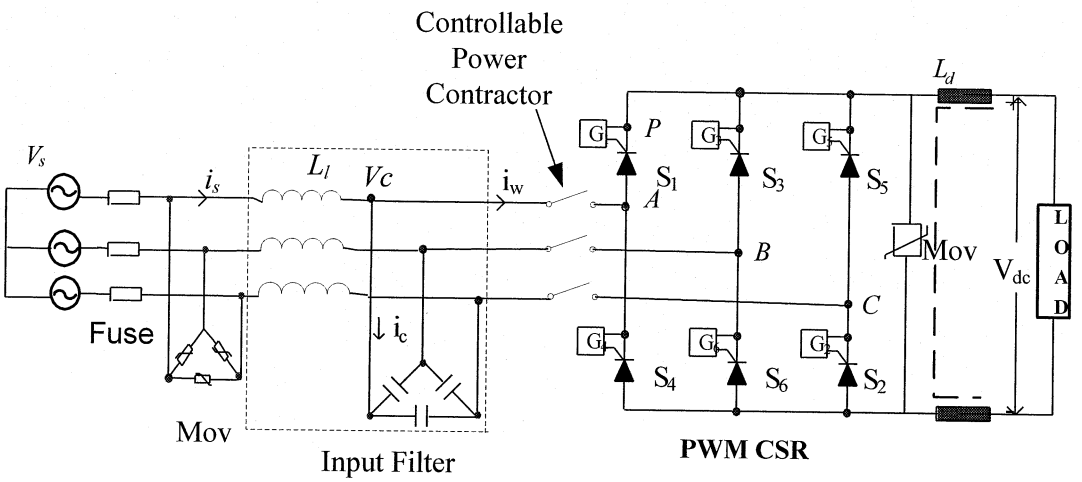


Fig. 4.1 A 208V-10 kVA PWM CSR prototype.

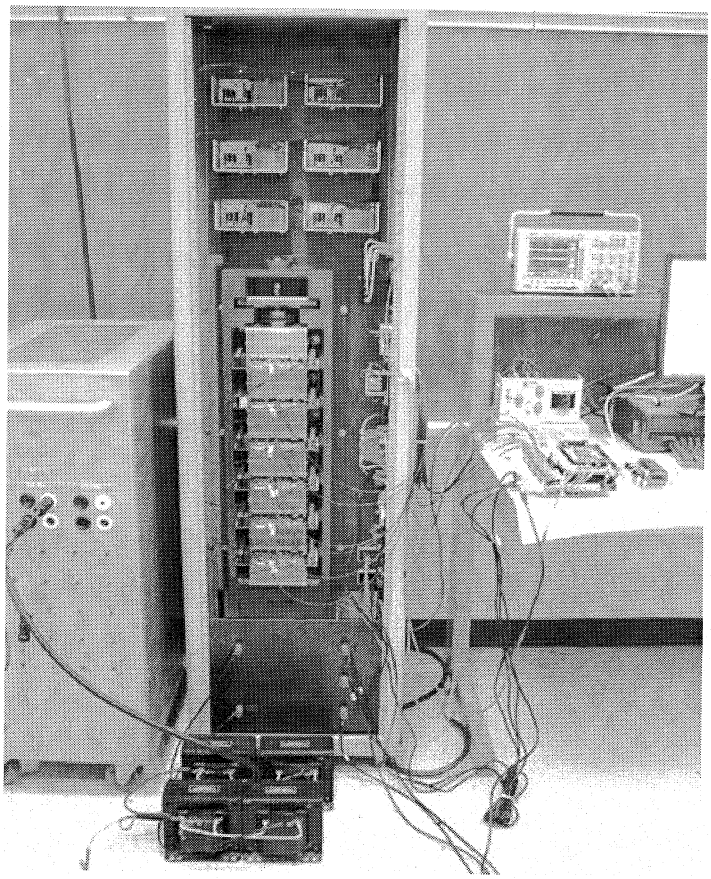


Fig. 4.2 A Photo of the CSR prototype.

For the experimental system, the grid voltage is provided by a 5250VA three-phase AC source at 208 V, which can be programmed to generate a voltage needed in the experiment. The input LC filter is comprised of three filter inductors and three delta-connected filter capacitors. The rectifier bridge is built using 6 reverse blocking IGCTs produced by ABB (donated by Rockwell Automation Canada). Snuber circuits with series connected resistors (10Ω, 25W) and capacitors (0.1uF, 2000Vdc) are put in parallel with each GCT. The CSR Bridge is controlled with a Space Vector PWM at rectifier switching frequency of 480/540Hz. The system parameters are listed in Table 4.1 (filter capacitance in Table 4.1 is the equivalent star-connected value).

Table 4.1 System Parameters

Parameters	Experimental
Nominal grid line-line Voltage(rms)	208 V
Nominal Power	10 kVA
Frequency	60Hz
Rectifier switching frequency	480/540Hz
Sampling frequency for Virtual R loop	3240Hz
Sampling frequency for DC current loop	1080Hz
Equivalent input filter inductance(L_f+L_s)	0.22 p.u.
Equivalent input filter resistance(R_f+R_s)	0.06 p.u.
Input filter capacitance(C_f)	0.3 p.u
DC link Inductance (L_d)	2.6 p.u
DC load (R_{load})	1.5 p.u

For the system protection, three fuses rated at 30A are connected at the input side. Three movs are also delta-connected before the input filter inductors to clamp the inductor induced high voltage (and the possible arc) when the voltage supply is disconnected suddenly. To protect the GCT devices, a mov is also connected across the CSR output dc rails to clamp the high voltage and to absorb the surge energy induced by the dc choke during an open circuit of the dc current flow loop. Considering the frequent start/stop of the experiment for various testing purposes, a three-phase controllable power contactor is connected between the input filter circuit and the CSR Bridge. With one leg of the rectifier bridge shorted, the power contactor can connect and disconnect the CSR with the source voltage smoothly during system startup and shunt down without causing any transient high current/voltage.

Parameters of the protection components are listed as following:

Fuse: 30A

AC Mov: ERZ-V14D621 (MAX 385 *Vac*, current surge 4500A).

DC Mov: V172BB60 (2150Vdc, 5000J-2ms, current surge 70000A).

Three-phase Power Contactor: P40P42D12P1-24 (50A, 24Vdc coil voltage).

4.3 DSP-FPGA Control System

The CSR prototype is digitally controlled by a DSP-FPGA control system, with a TMS F2812 fixed-point DSP for implementation of the control algorithms and the FPGA for the PWM signal generation and system protection. The photo of the DSP-FPGA control system is shown in Fig. 4.3.

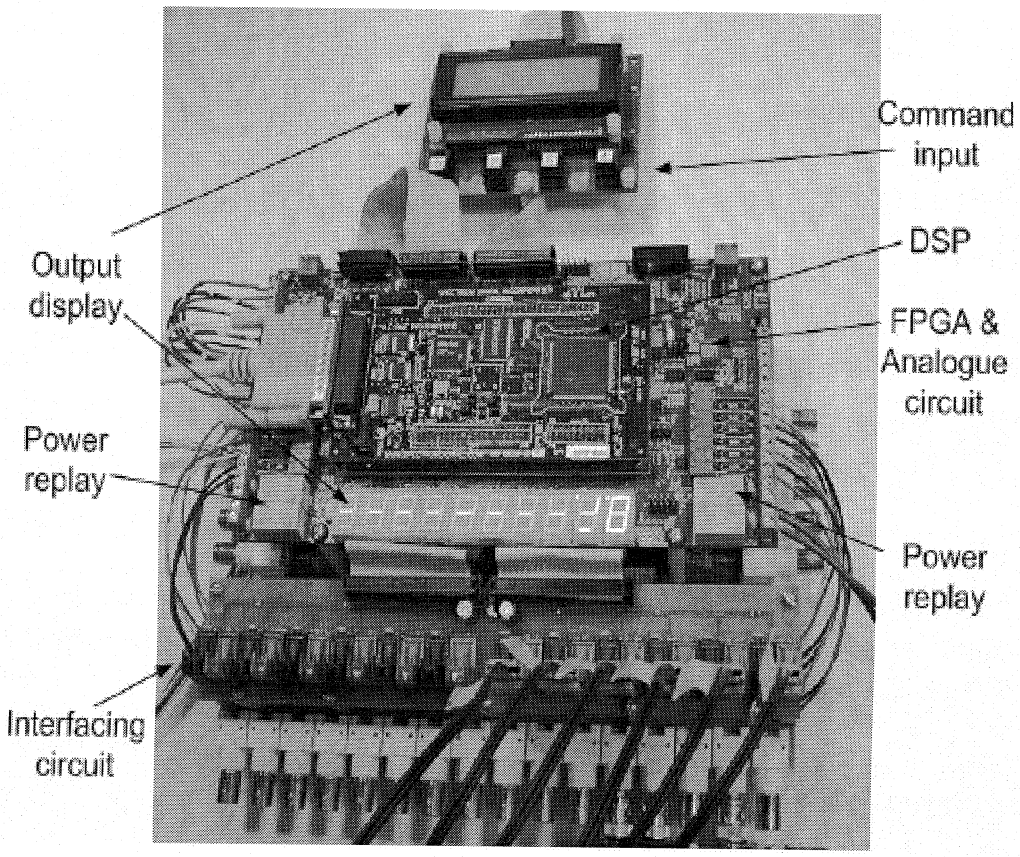


Fig. 4.3 Photo of the DSP-FPGA control system.

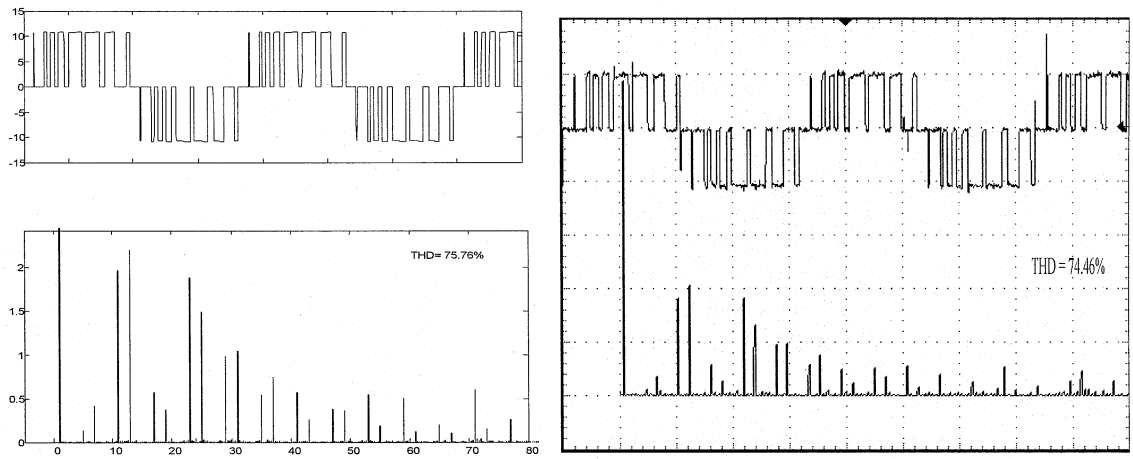
The DSP-FPGA control system which can be conveniently and effectively used in any power electronic converter system control, such as motor drive, grid interfacing converter, active filter etc, with enhanced computation power, superior performance and increased reliability than a single DSP controller. The control system is comprised of an analogue circuit board, a switching signal interfacing board, a DSP, a FPGA and the output display and command input devices. Specifically, the analogue circuit is used for feedback signal conditioning, protection signal generation and output command realization, the DSP is programmed with the main control algorithms in accordance to different converter system application, the FPGA is employed for DPLL implementation, switching signal generation and power electronic device protection, the interfacing circuit is used for switching command conversion (between different voltage or power levels or between voltage signals and optic signals), and finally the output display and input components such as LEDs and LCD and keyboard are embedded to the control system for control status monitoring and control command input.

Upon powered up, the FPGA would be at the protection state and output the pre-programmed switching status to ensure that the converter bridge is at a known safe condition. After the DSP initialization, the FPGA parameters are updated (through the DSP external memory writing) with the controllable power contactor opened and one leg of the CSR bridge shorted. After the CSR Bridge is connected to the voltage source (by closing the controllable power contactor), the DPLL in FPGA starts to pull in with the input signal. Therefore when the control loop interrupt in the DSP is enabled by an external command input (from keyboard), the entire control system will function properly with the DPLL already locked.

4.4 Experiment Results

The Performance of the current source rectifier with best two SVM PWM sequence is compared at amplitude modulation index (m_a =0.8).

4.4.1 Harmonic contents of Sequence B

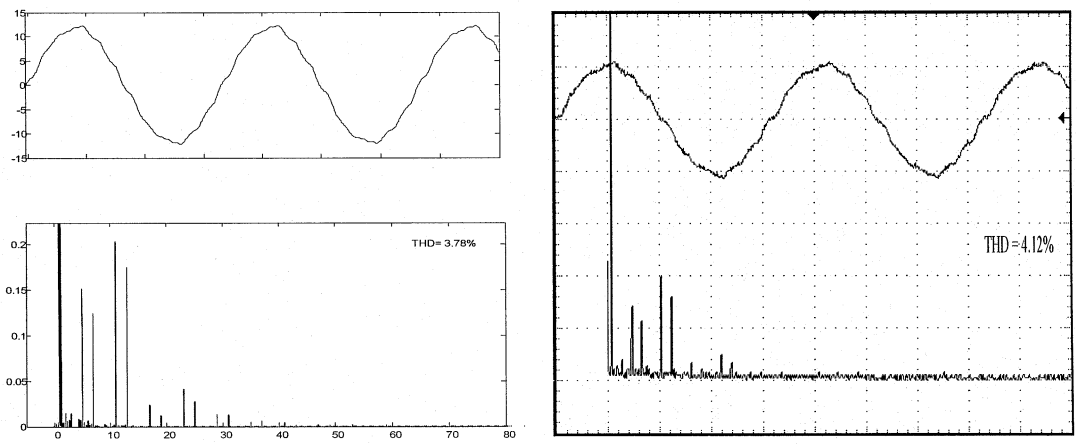


(a) Simulated (b) Experimented

Fig.4.4 Switching current waveform and its harmonic current of Sequence B. (a) Simulated x-axis harmonic order, Y-axis magnitude of harmonic content. (b) Experimented switching current X-axis 4ms/div, 10A/div Y-axis and harmonic spectrum 625Hz/div X-axis,1A/div Y-axis (f = 60Hz, m_a = 0.8 f_{sw} = 480Hz).

Simulated and experimented switching current of current source rectifier is illustrated in Fig. 4.4. The current source rectifier operates under the condition of $f = 60\text{Hz}$, and $m_a = 0.8$ the device rectifier switching frequency can be found from $f_{sw,dev} = f \times N_p = 480\text{Hz}$. The waveform of i_w consists of eight pulses in each half cycle. Whose harmonics appear as 5th, 7th, 11th, 13th, 17th, 19th and 23rd. The triplen harmonics does not appear in i_w due to the three-phase balanced supply system. The even harmonics will not appear since the waveform is half wave symmetry. The fundamental value of switching current from simulation is 6.07A (rms) and THD is 75.76%.The fundamental value of the switching current from the experimental is 5.98 A (rms) and THD is 74.56%.

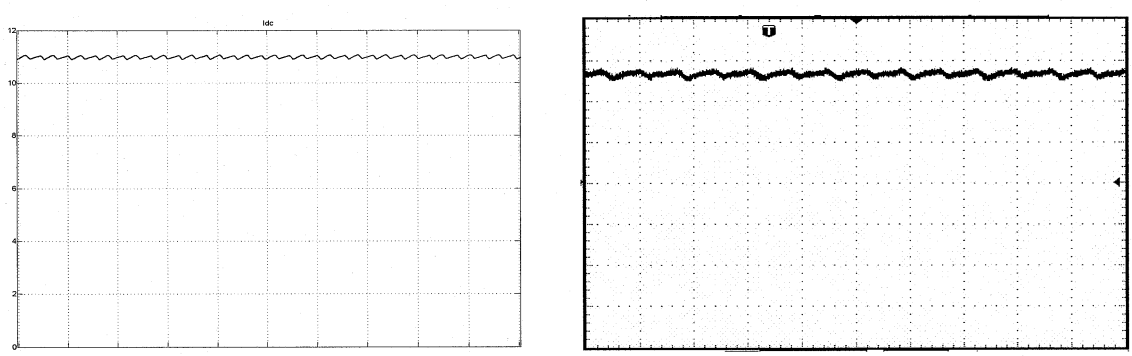
Simulated and experimented line current of current source rectifier is illustrated in Fig. 4.5. The current source rectifier operates under the condition of $f = 60\text{Hz}$, and $m_a = 0.8$ the current waveform of i_s is a smooth sinusoidal. Whose harmonics appear as 5th, 7th, 11th, 13th, 17th, 19th and 23rd. The triplen harmonics does not appear in i_s due to the three-phase balanced system. In sequence B the 11th and 13th harmonic magnitude is more than 17th and 19th order harmonic. From the simulation the fundamental line current is 8.39A (rms) and THD is 3.78%.From experimental the fundamental line current is 8.27 A (rms) and THD=4.12%.



(a) Simulated (b) Experimented

Fig. 4.5 Line current waveform and its harmonic current of Sequence B.
(a) Simulated x-axis harmonic order, Y-axis magnitude of harmonic content. (b) Experimented switching current X-axis 4ms/div,10A/div Y-axis and harmonic spectrum 0.1A/div Y-axis 625Hz/div, X-axis (f= 60Hz, m_a = 0.8 f_{sw} = 480Hz).

The harmonic spectrum pattern in Fig.4.4 and Fig.4.5 of the switching and line current respectively for simulated are identical to that of experimental.

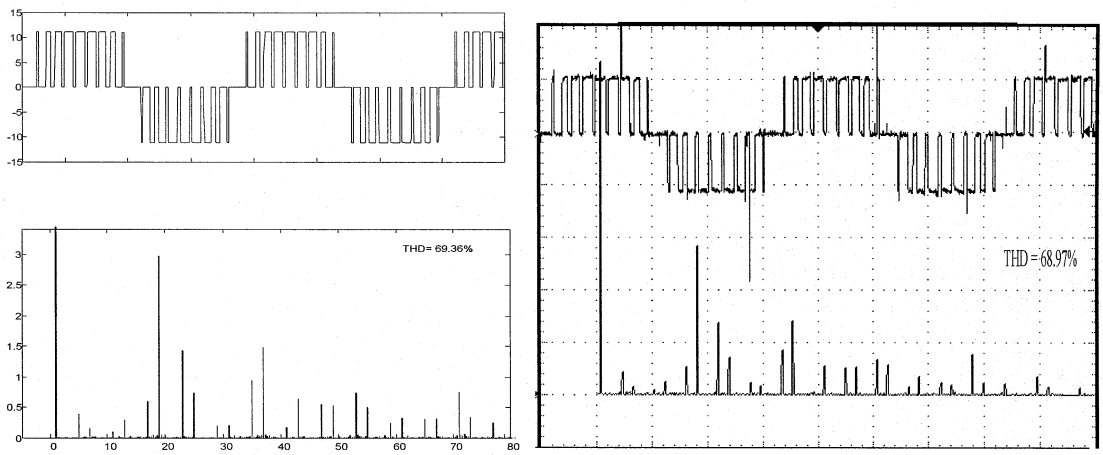


(a)Simulated (b) Experimented

Fig. 4.6 DC Current ripple (X-axis 4ms/div, Y-axis 4A/div) of sequence B.

Fig.4.6 is the simulated and experimental output current of current source rectifier whose dc current ripple is 8.85 % which is less than limit15% for current source rectifier.

4.4.2 Harmonic contents of Sequence E



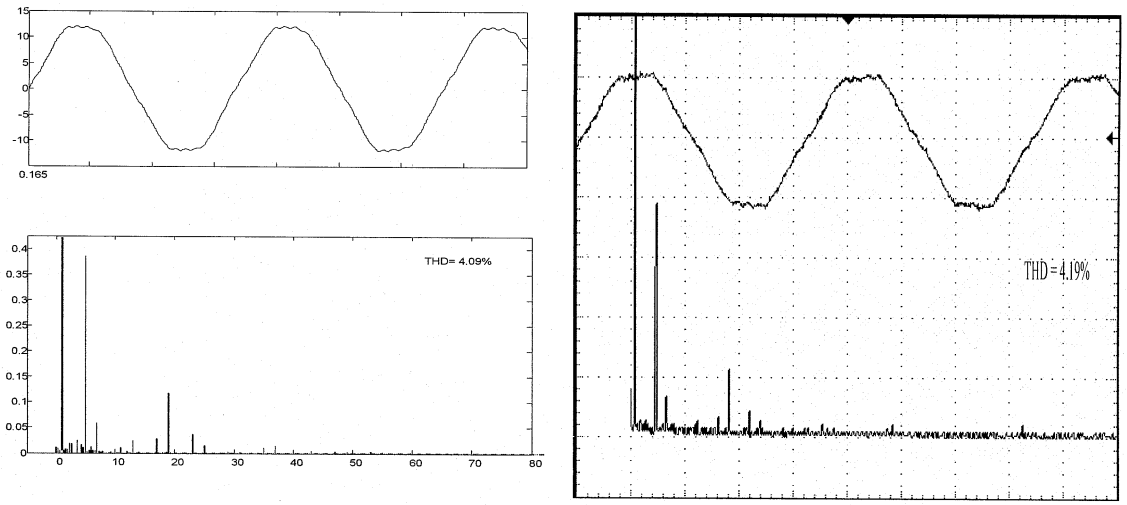
(a) Simulated (b) Experimented

Fig. 4.7 Switching current waveform and its harmonic current of Sequence E.
(a) Simulated x-axis harmonic order, Y-axis mag. of harmonic content (b) Experimented switching current X-axis 4ms/div, 10A/div Y-axis and harmonic spectrum Y-axis 1A/div X-axis 625Hz/div (f= 60Hz, m_a = 0.8 f_{sw} = 540Hz).

Simulated and experimented switching current of current source rectifier is illustrated in Fig. 4.7. The current source rectifier operates under the condition of $f = 60\text{Hz}$, and $m_a = 0.8$ the rectifier switching frequency can be found from $f_{sw,dev} = f \times N_p = 540\text{Hz}$. The waveform of i_w consist of nine pulses in each half cycle. Whose harmonics appear as 5th, 7th, 11th, 13th, 17th, 19th and 23rd. The triplen harmonics does not appear in i_w due to the three-phase balanced supply system. The even harmonics will not appear since the waveform is half wave symmetry. In sequence E the 11th and 13th harmonic magnitude is less than 17th and 19th order harmonic. The fundamental current from simulation is 6.48A (rms) and THD is 69.36%.The fundamental switching current from experimental is 6.39 A (rms) and THD is 68.71%.

Simulated and experimented line current of current source rectifier is illustrated in Fig. 4.8. The current source rectifier operates under the condition of, $f = 60\text{Hz}$ and $m_a = 0.8$

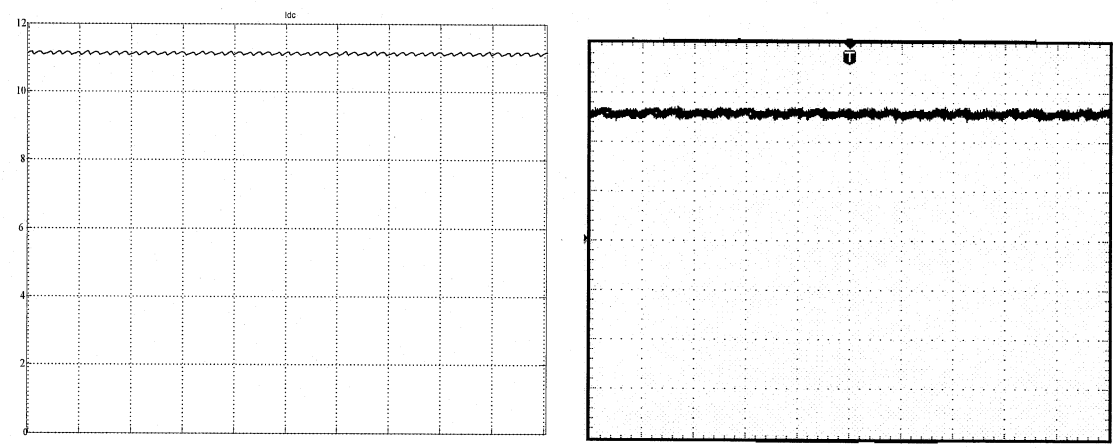
the current waveform of i_s is sinusoidal. The fundamental of line current is 8.702A (rms) and THD is 4.29% from simulation. Whose harmonics appear as 5th, and 7^{th} and we don't observe the 11^{th}, 13th and higher. The triplen harmonics does not appear in i_s due to the three-phase balanced system.



(a) Simulated (b) Experimented

Fig. 4.8 Line current waveform and its harmonic current of Sequence E.
(a) simulated X-axis harmonic order ,Y-axis mag. of harmonic current (b) Experimented switching current X-axis 4ms/div,10A/div Y-axis and harmonic spectrum 0.1A/div Y-axis 625Hz/div X-axis(f = 60Hz, $m_a = 0.8$ f_{sw} = 540Hz).

The harmonic spectrum pattern in Fig. 4.7 and Fig. 4.8 of the switching and line current respectively for simulated are identical to that of experimental.



(a) Simulated (b) Experimented

Fig. 4.9 DC current ripple of current source rectifier for sequence E
(X-axis 4ms/div, Y-axis 4A/div).

Fig 4.9(a) is simulated dc current ripple, which is very close to the experimented waveform. Fig. 4.9 (b) is the experimented output current of current source rectifier whose dc current ripple is 10.26% which is less than limit 15% for current source rectifier.

4.5 Summary

This chapter presents the experimental results. A prototype current source rectifier has been set up to verify the performance of the SVM sequences. The experimental setup includes the IGCT gate driver and IGCT device. Experiments are carried out to investigate the harmonic content of two best sequences out of six SVM PWM sequence on current source rectifier. The performance of input current and switching current waveforms with their harmonic contents is investigated. The waveforms of CSR on different conditions are provided and analyzed. From the experimental results, it can conclude that:

1) The measured and simulated waveforms are well matched.
2) The proposed SVM PWM sequence B and Sequence E are the two best sequences among the six sequences; and
3) The performance of the proposed six SVM PWM sequence is verified by the experiment.

Chapter 5 Conclusion

In this project, different vector sequences suitable for a CSR are investigated. Details of sequence arrangements to achieve waveform symmetries with minimum rectifier switching frequency are discussed. The harmonic performance of different sequences is compared for CSR implementation. An optimum method of first choice is sequence B and the second choice is sequence E at proper modulation index is proposed to obtain the best line current THD and minimum switching losses. Two switching patterns are developed with rectifier switching frequency of 480Hz and 540Hz.

The single bridge current source PWM rectifier features reduced line current distortion, superior dynamic response and improved input power factor. When the processing of voltages is higher than the device rating two or more symmetrical GCTs can be connected in series.

The proposed topology is particularly suitable for medium voltage (2300 V and up) applications. No GCT devices are connected in series in the proposed topology. The dynamic/steady-state voltage sharing problem for the series devices in a single converter topology is completely avoided. Also, a relatively small size filter capacitor can be used, which will facilitate the operation near unity displacement factor.

This project is devoted to the development of a space vector pulse width modulation for current source rectifier. The research can be divided in to two parts: the space vector pulse width modulation of different sequences and experimental verification, both of which involve extensive theoretical analysis and computer simulation. The main contributions of the thesis project are as follows:

Design a space vector pulse width modulation scheme for the current source rectifier. This involves theoretical analysis of input current waveforms and harmonic contents.

Computer simulation has been carried out using various PWM techniques and finally arrived at space vector pulse width modulation sequences.

Verify the proposed space vector pulse width modulation scheme for the current source rectifier by experiment. The experiment has carried out on a prototype converter with DSP-FPGA control systems. The measured waveforms are analyzed and compared with the simulated waveforms. The CSR is tested on different conditions, and the relevant waveforms of CSR are provided and analyzed. The experimental results closely match the simulation results and effectively verified the proposed principle. Comparison of input current waveforms and harmonic contents has performed under various rectifier operating conditions.

The performance of the proposed different space vector pulse width modulation scheme for current source rectifier has been verified by experiment.

For future work, it is suggested to

1. further verify the device switching losses in different sequence by experiment; and
2. compare the input waveforms, harmonic contents, THD and performance with other SVM PWM sequences.
3. apply the six SVM PWM sequences to Inverter.

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Appendix A

Definition of THD and PF

Assume that the phase voltage v_a of the utility supply is sinusoidal

$$V_a = \sqrt{2} V_a Sin\omega t \tag{1}$$

The line current i_a drawn by a rectifier is generally periodical but non-sinusoidal. The line current can be expressed by a Fourier series

$$i_a = \sum_{n=1,2,3...}^{\infty} \sqrt{2} I_{an} (\sin(\omega_n t) - \phi_n) \tag{2}$$

where n is the harmonic order, I_{an} and ω_n are the rms value and angular frequency of the nth harmonic current, and ϕ_n is the phase displacement between V_a and I_{an}, respectively. The rms value of the distorted line current i_a can be calculated by

$$I_a = \left(\frac{1}{2\pi} \int_0^{2\pi} (i_a)^2 d(\omega t) \right)^{1/2} = \left(\sum_{n=1,2,3...}^{\infty} I_{an}^2 \right)^{1/2} \tag{3}$$

The total harmonic distortion is defined by

$$THD = \frac{\sqrt{I_a^2 - I_{a1}^2}}{I_{a1}} \tag{4}$$

where I_{a1} is the rms value of the fundamental current. The per-phase average power delivered from the supply to the rectifier is

$$P = \frac{1}{2\pi} \int_0^{2\pi} v_a \times i_a d(\omega t) \tag{5}$$

Substituting (1) and (2) into (5) yields

$$P = V_a I_{a1} cos\phi_1 \tag{6}$$

where $\phi_{1\,1}$ is the phase displacement between V_a and I_{a1}. The per-phase apparent power is given by

$$S = V_a I_a \tag{7}$$

The input power factor is defined as

$$PF = \frac{P}{S} = \frac{I_{a1}}{I_a}\cos\phi_1 = DF \times DPF \tag{8}$$

Where DF is the distortion factor and DPF is the displacement power factor, given by

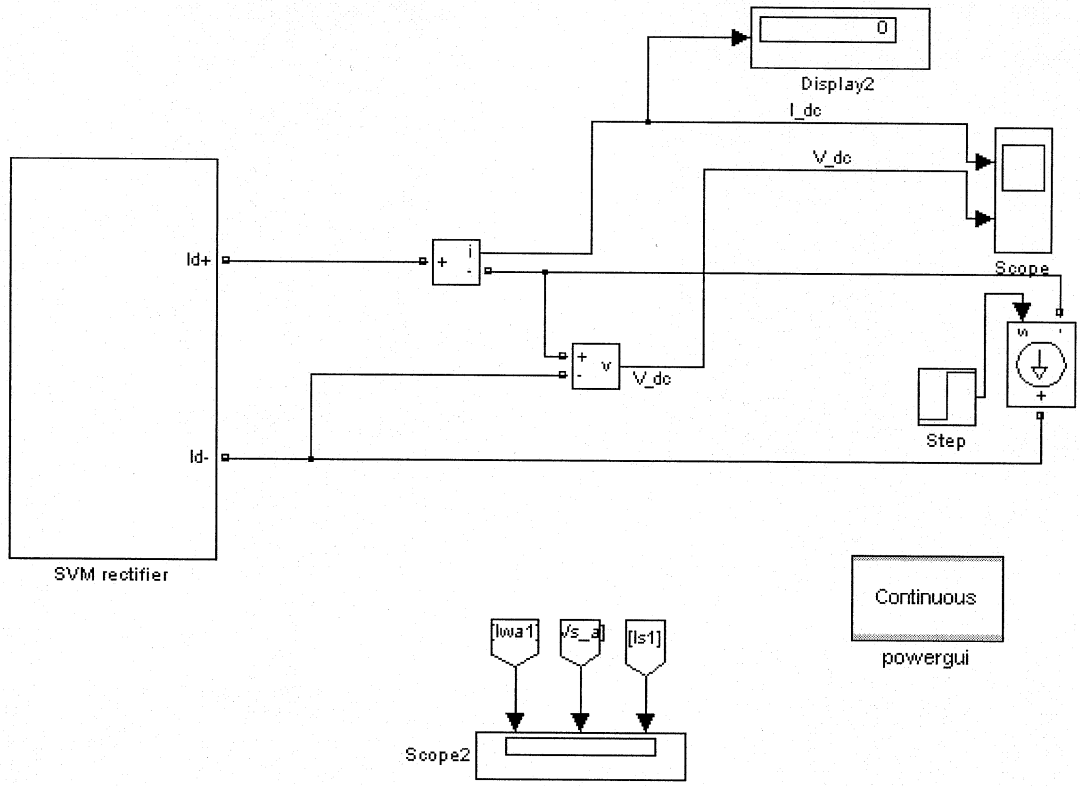
$$DF = I_{a1} / I_a \quad \text{and} \quad DPF = \cos\phi_1 \tag{9}$$

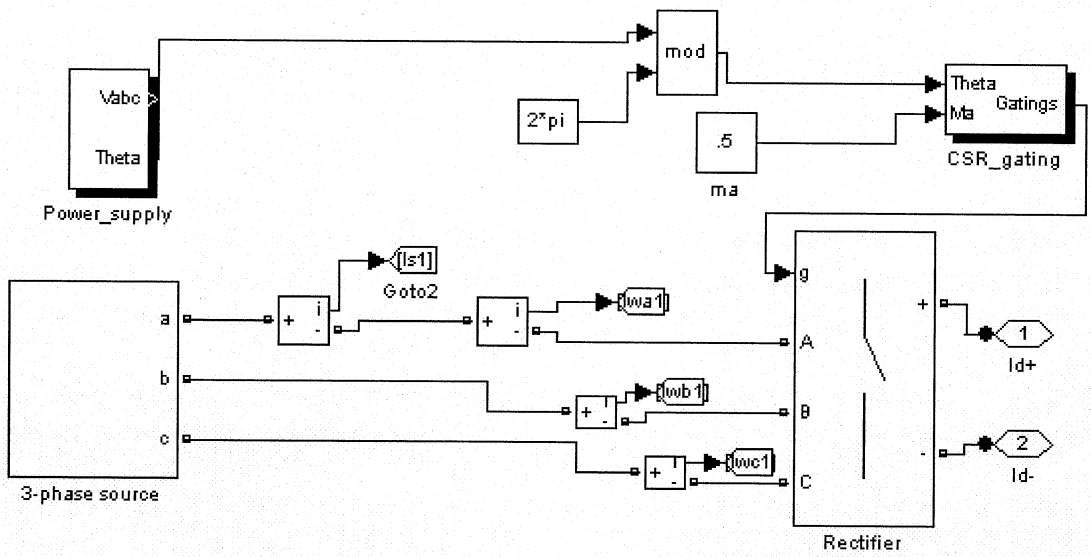
For a given THD and DPF, the power factor can also be calculated by

$$PF = \frac{DPF}{\sqrt{1 + THD^2}} \tag{10}$$

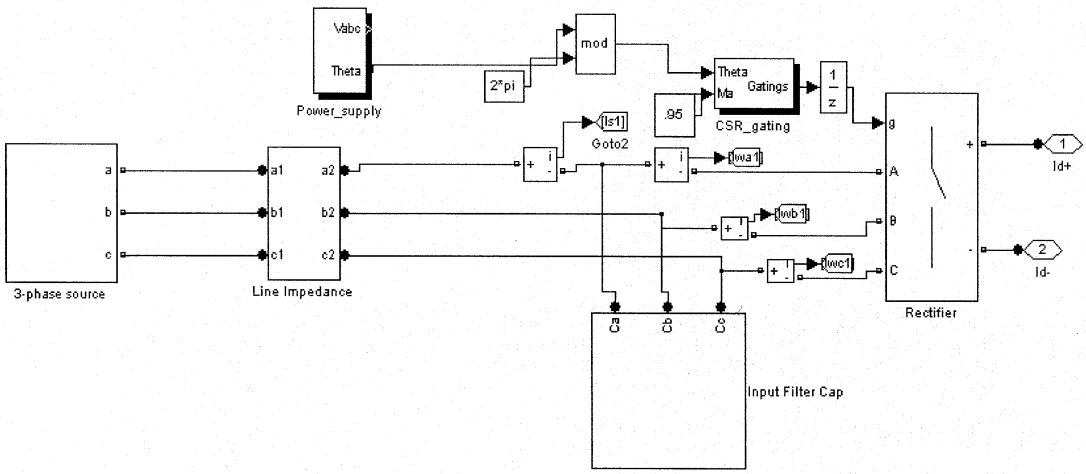
Appendix B

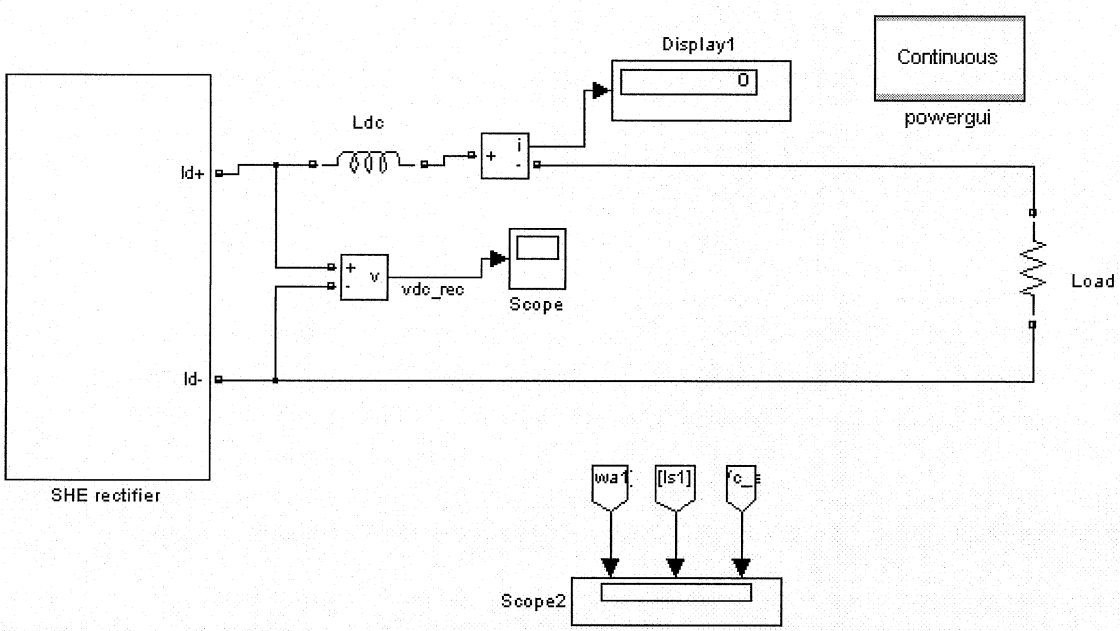
Ideal Current Source Rectifier





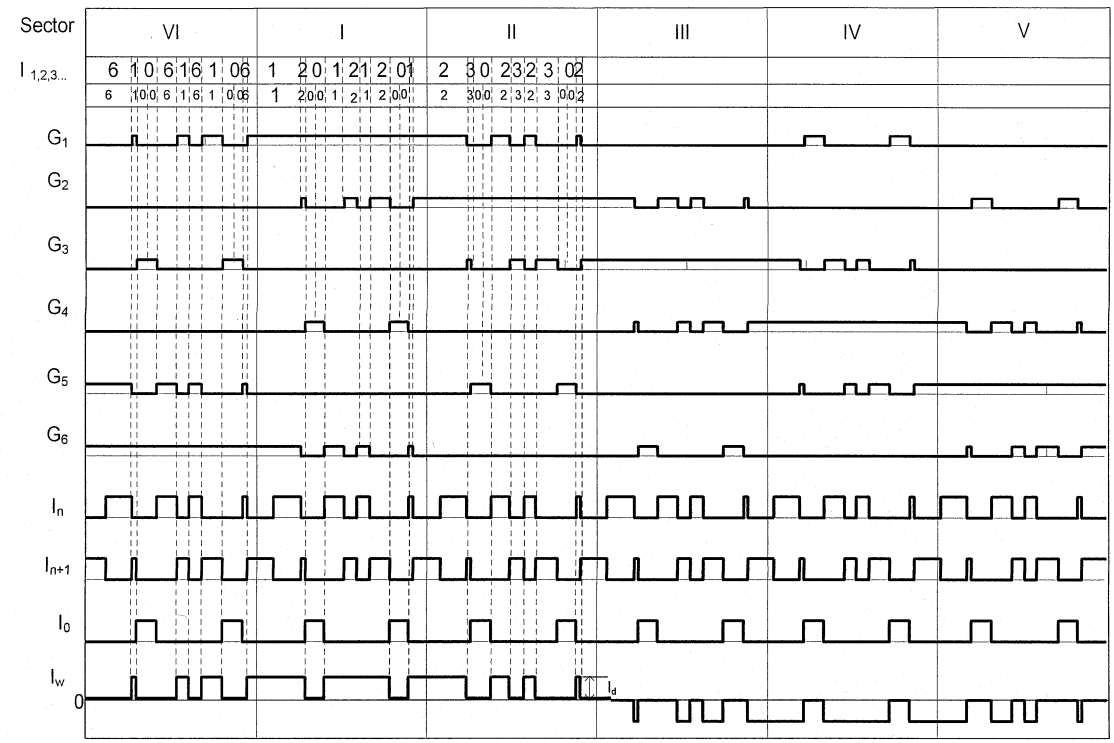
Practical Current Source Rectifier



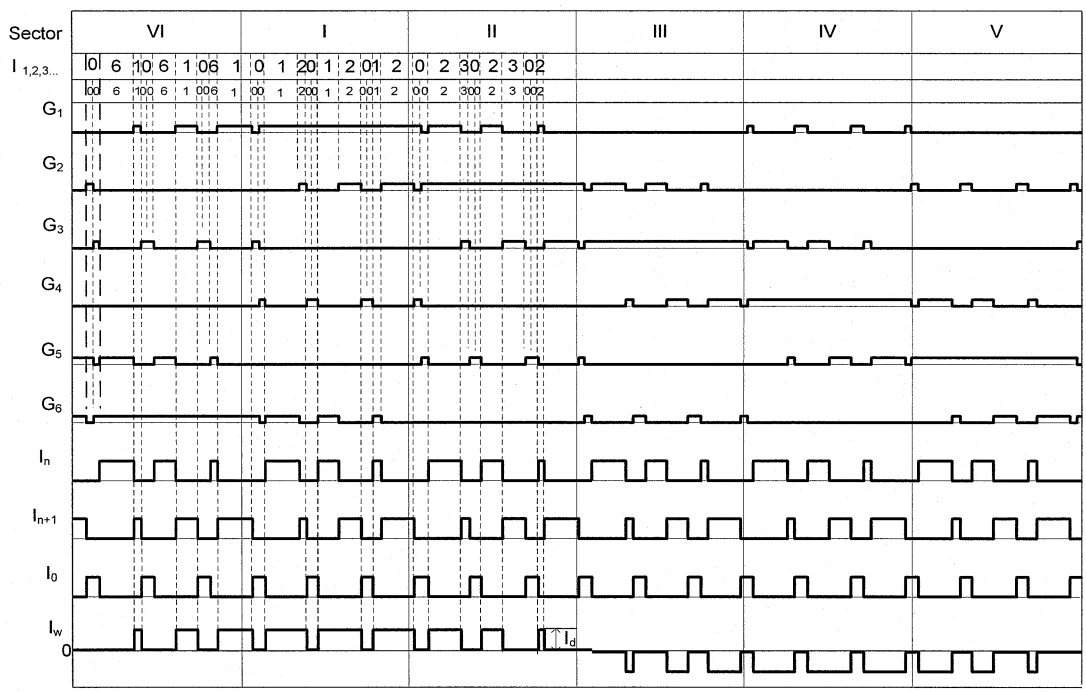


Appendix C

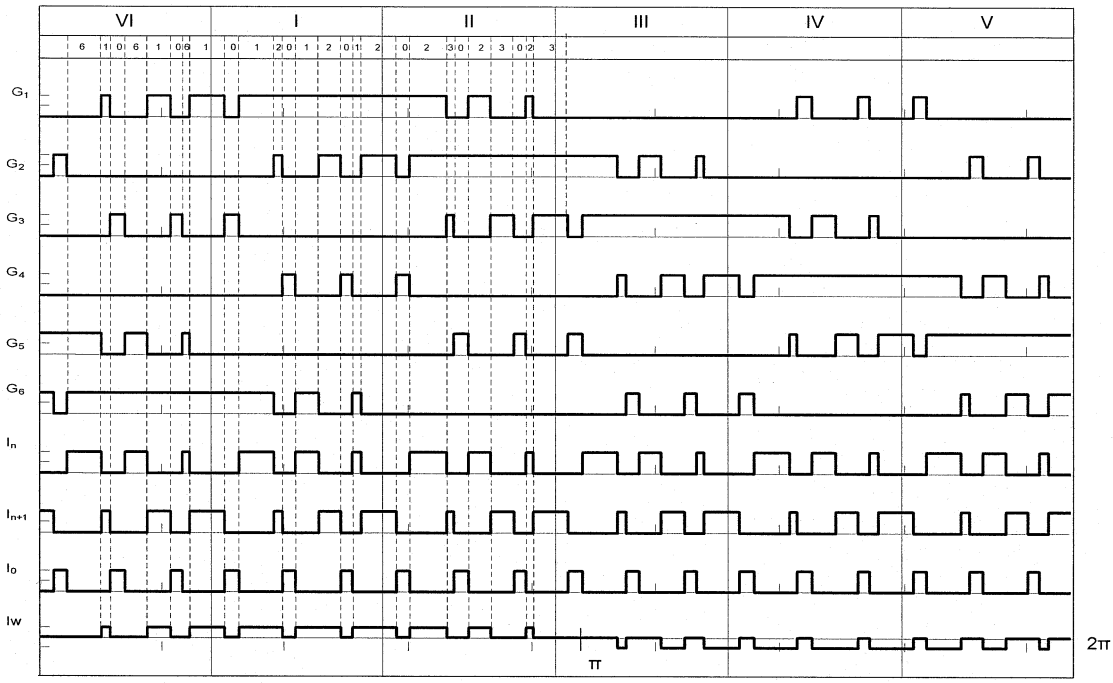
Switching Sequence C (I_n-I_{n+1}-I_0-I_0-I_n-I_{n+1})



Switching Sequence D (I_0-I_n-I_{n+1}-I_0)

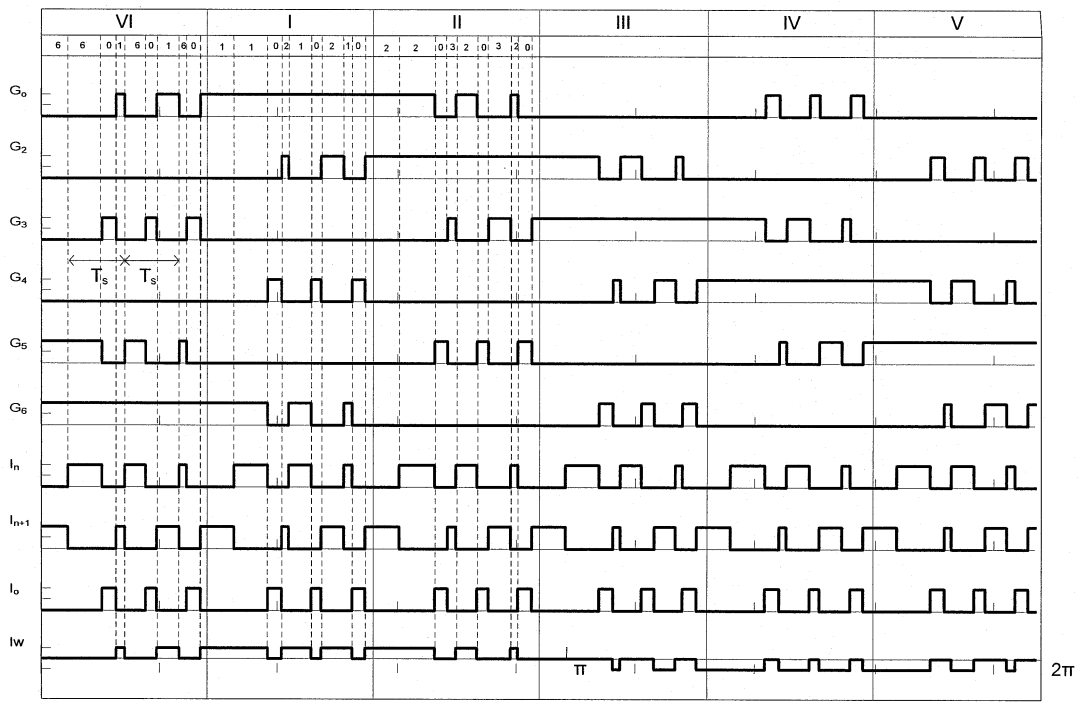


Switching Sequence E (I_n-I_{n+1}-I_0)



Sequence E

Switching Sequence F (I_n-I_0-I_{n+1})



Sequence F