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A novel digital modulation scheme for multilevel cascaded H-bridge inverters in high power AC drives

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A Novel Digital Modulation Scheme for Multilevel Cascaded H-bridge Inverters in High Power AC Drives

by

Mouzhi Dong

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ABSTRACT

The multilevel cascaded H-bridge (CHB) inverters are widely used in megawatt variable speed drives, where the voltage level normally varies from seven to thirteen and the number of active switching devices used in the inverter is in the range of 36 to 72. The design of a simple modulation scheme for such inverters with superior harmonic performance is a challenging task.

This project presents a novel digital multilevel modulation (DMM) scheme for multilevel CHB inverters. This scheme is very simple, flexible and easy to implement. To generate gate signals for all the active switches in the inverter, the scheme needs only to calculate a three-phase sine function once followed by a number of subtractions in each sampling period. In this project, the principle of the proposed modulation scheme is elaborated and its harmonic performance is analyzed. Comparisons are carried out between the DMM scheme and carrier based modulation schemes including phase-shifted and level-shifted

modulations. It is demonstrated that the harmonic performance of the DMM scheme is on par with the best of carrier based modulation techniques. On the inverter side, line-to-line voltage THD of inverter output for the proposed modulation scheme is as low as IPD modulation scheme. On the line side, line current THD is as low as phase-shifted modulation scheme because of balanced power consumption in each power cell.

Under the condition of device switching frequency unchanged, a new algorithm is developed to combine the advantages from both phase-shifted and IPD modulation schemes and conquer the drawback of both schemes. The simulation result shows that new modulation scheme has almost same line-to-line voltage harmonic spectrum from light to rated load with balanced power cells.

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I also wish to share my achievements with my parents, and I am very grateful for their strong support.

TABLE OF CONTENTS

Chapter 1 Introduction 1

1.1 High Power AC Drives 1

1.2 Modulation Schemes 6

1.3 Technical Challenges 9

1.4 Research Objectives 10

1.5 Project Outline 10

Chapter 2 Modulation Schemes for CHB Inverters 12

2.1 Introduction 12

2.2 Phase-Shifted Modulation Schemes 14

2.3 Level-Shifted Multicarrier Modulation 16

2.4 Rotating Switching Pattern Modulation Schemes 19

2.5 Summary 21

Chapter 3 DMM Scheme for CHB Inverters 23

3.1 Introduction 23

3.2 Principle of the Proposed Digital Modulation Scheme 23

3.3 Pattern Rotation for Even Power Distribution 29

3.3.1 Switching Mode and Rotating Sequence in a Positive Half Cycle 29

3.3.2 Switching Mode and Rotating Sequence during a Negative Half Cycle 35

3.4 Computer Simulation 38

3.5 Comparison with Carrier Based Modulation Schemes 41

3.6 Summary 44

Chapter 4 Line Current THD Analysis of AC Drives 45
4.1 Introduction 45
4.2 System simulation 45
4.2 Line Current THD of AC Drives with Phase Shifted Scheme 47
4.3 Line Current THD of AC Drives with IPD Scheme 49
4.4 Line Current THD of AC Drives with DMM Scheme 51
4.5 Line Current THD Comparison with IPD, Phased Shifted and DMM 53
4.6 Summary 54
Chapter 5 Conclusions 55
5.1 Conclusions 55
5.2 Future Works 56
References 58
Appendix I 62

LIST OF FIGURES

Figure 1-1 General block diagram of the MV drive. 2

Figure 1-2 12-pulses rectifier. 3

Figure 1-3 Neutral Point Clamped (NPC) Inverter. 4

Figure 1-4 Flying Capacitor Inverter. 4

Figure 1-5 Cascaded H-bridge (CHB) Inverter. 5

Figure 1-6 Space vector diagram. 7

Figure 1-7 Phase-shifted modulation scheme. 8

Figure 1-8 Level-shifted multicarrier modulation for seven-level inverters. 9

Figure 2-1 A seven-level CHB inverter topology. 13

Figure 2-2 Phase-shifted PWM for seven-level CHB inverters ($m_f = 3$, $m_a = 1$, $f_m = 60Hz$ and $f_{cr} = 180Hz$). 15

Figure 2-3 Level-shifted PWM for seven-level CHB inverters ($m_f = 15$, $m_a = 1$, $f_m = 60Hz$ and $f_{cr} = 900Hz$). 17

Figure 2-4 Line-to-line voltage v_{AB} and THD of IPD, APOD, POD and phase-shifted modulation scheme for seven-level CHB inverters ($m_a = 1.0$, $m_f = 60Hz$, and $f_{sw,dev} = 600Hz$). 18

Figure 2-5 Rotating switching pattern modulation schemes based on modulation

frequency. 20

Figure 2-6 Modulation operating principle: a) Traditional IPD PWM, b) Modified rotative IPD PWM 21

Figure 3-1 Seven-level cascaded H-Bridger inverter. 24

Figure 3-2 Principle of DMM scheme for a seven-level CHB inverter 25

Figure 3-3 Inverter output voltage waveforms produced by the DMM scheme during a positive half cycle ($\hat{V}_r = 2.25(75\%), f_r = 60$ Hz and $T_s = 1/2700$ sec). 34

Figure 3-4 Turn-on pulse during the negative half cycle of the inverter fundamental voltage. 35

Figure 3-5 Simulated waveforms and harmonic spectra for a seven-level CHB inverter 39

Figure 3-6 Waveform and harmonic spectrum of v_{AB} produced by carrier based modulation and proposed DMM schemes 42

Figure 3-7 THD curves of the inverter line-to-line voltage v_{AB} generated by carrier based and DMM schemes. 43

Figure 3-8 THD profile of inverter line-to-line voltage v_{AB} generated by DMM schemes with various device switching frequencies. 44

Figure 4-1 Seven-level CHB inverter-fed drives topology and parameters 46

Figure 4-2 Harmonic spectrum of phase shifted for i_A ($m_a = 1, f_r = 60Hz$, $f_s = 600Hz$, and $f_{sw,dev} = 600Hz$). 47

Figure 4-3 Harmonic spectrum of phase shifted for i_A. 48

Figure 4-4 Harmonic spectrum of IPD for i_A ($m_a = 1$, $f_r = 60Hz$, $f_s = 3600Hz$, and $f_{sw,dev} = 600Hz$). 49

Figure 4-5 Harmonic spectrum of IPD for i_A. 50

Figure 4-6 Harmonic spectrum of DMM for i_A ($m_a = 1$, $f_r = 60Hz$, $f_s = 3600Hz$, and $f_{sw,dev} = 600Hz$). 51

Figure 4-7 Harmonic spectrum of DMM for i_A. 52

Figure 4-8 Line current THD of i_A for phase shifted, IPD and DMM. 53

LIST OF TABLES

Table 2-1 Switching state of single-phase H-bridge inverter power cell 14

Table 3-1 Distribution of total duty cycle $D_{T(k)}$ for a seven-level CHB inverter in the first forth sampling period 28

Table 3-2 Duty cycle and rotating sequence I 30

Table 3-3 Output voltage waveforms of a seven-level CHB inverter with rotating sequence I 31

Table 3-4 Duty cycle and rotating sequence II 32

Table 3-5 Output voltage waveforms of a seven-level CHB inverter with rotating sequence II 33

Table 3-6 Duty cycle and rotating sequence during a negative half cycle 36

Table 3-7 Output voltage waveforms of a seven-level CHB inverter during negative half cycle 37

Table 3-8 Conduction angle of each switch for IPD modulation scheme ($m_a = 1$, $f_m = 60Hz$, $T_{cr} = 1/3600\,\text{sec}$) 40

Table 3-9 Conduction angle of each switch for DMM scheme ($\hat{V}_r = 3(100\%)$, $f_r = 60Hz$, $T_s = 1/3600\,\text{sec}$) 41

Chapter 1 Introduction

With technology development in semiconductor devices, modern high-power medium-voltage (MV) drives are widely used in various industries such as the petrochemical industry, the metals industry, and transportation industry [1]. The MV drives cover power ratings from 0.4 MW to 100 MW at the voltage level of 2.3 kV to 13.8 kV [2]. The most MV drive applications are pumps, fans and conveyors. However, only 3% of them are controlled by variable-speed MV drives which can reduce energy cost significantly compared to conventional mechanical methods [3]. The potential market for MV AC drive is tremendous.

This chapter starts with an introduction of MV high power AC drives, followed by an analysis on advantage and disadvantage of several inverter topologies. Several modulation schemes are compared with merit and drawback. The objectives and motivation to develop a novel modulation scheme is presented. The chapter also draws an outline of the project.

1.1 High Power AC Drives

A general block diagram of the MV drives is shown in Figure 1-1. A phase shifting transformer with multiple secondary windings is often used for the reduction of line current distortion and electrical isolation. The rectifier converts the three-phase AC voltage to the dc voltage by using the capacitors to make voltage source inverter (VSI), or to a dc current by using the inductors to make current source inverter (CSI). Depending on the system requirements, the rectifiers can be multipulse diode rectifiers, multipulse

SCR rectifiers, or pulse-width-modulated (PWM) rectifiers.

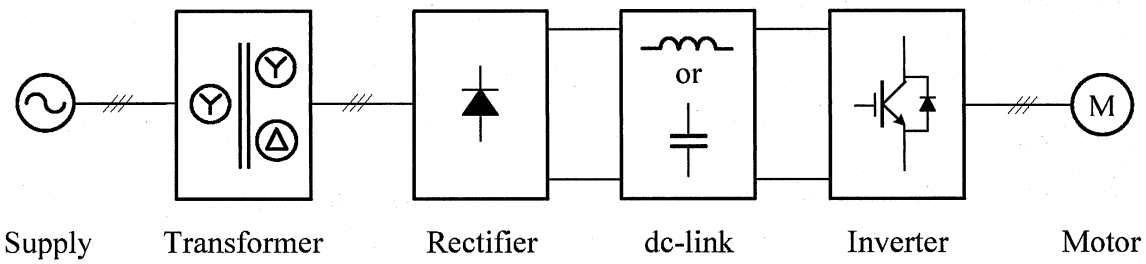


Figure 1-1 General block diagram of the MV drive.

To improve the performance of the MV drive system, there are a number of challenging task on both the line-side converter and the motor-side inverter design. Line-side aspects include line current distortion, input power factor and LC resonance suppression. Motor-side challenges include *dv/dt* and wave reflections, common-mode voltage stress, motor derating, LC resonances and torsional vibration.

On the supply side, with the stringent harmonic requirements set by North American and European standards such as 519-1992 [4], major high-power drive manufacturers are increasingly using multipulse rectifiers in their drives as front end converters [5]. Figure 1-2 illustrates a block diagram of 12-pulse rectifier, one of the simplest multipulse rectifiers. In practice, 18-pulse and 24-pulse may be employed to further reduce line-side current harmonic. Each multipulse rectifier is composed of a phase shifting transformer with multipulse secondary windings connecting to a several identical six-pulse rectifier. Diode and SCR rectifiers are low manufacturing cost, small physical size and high reliability rectifier, but if an application requires four-quadrant operation, PWM rectifiers using IGBT or GCT device can be applied.

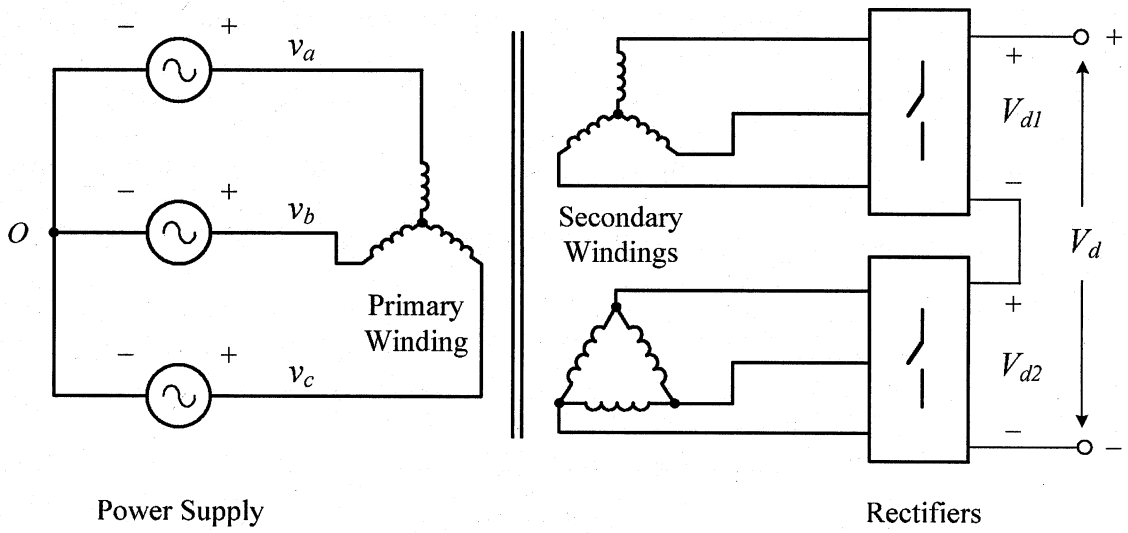


Figure 1-2 12-pulses rectifier.

On the motor side, several typical three-phase inverter topologies for the MV drive include a two-level inverter, a three-level neutral-point clamped (NPC) inverter, a seven-level cascaded H-bridge inverter and a four-level flying-capacitor inverter [6-11]. The switching devices are either IGBT or GCT.

In the above mentioned inverter topologies, two-level inverter has the advantages of modular structure using power converter building block, simple pulse width modulation (PWM) scheme, and ease of dc capacitor pre-charging. However, there are drawbacks such as high *dv/dt* in the inverter output voltage and motor harmonic losses. Fast switching speed of IGBTs results in high *dv/dt* at the rising and falling edges of the inverter output voltage waveform. High *dv/dt* can cause many problems like premature failure of motor winding insulation, early bearing failure and wave reflections. The two-level inverter usually requires LC filter between the inverter output and the motor, but using LC filter will increase manufacturing cost, fundamental voltage drops, and circulating current between the filter and dc circuits [12].

Three-level NPC inverter is shown in Figure 1-3, which has less harmonic distortion in output voltage and output filter size than two-level inverter [6,10,13]. In addition, NPC inverter can operate at the medium voltage up to 4160V without switching devices connected in series, which increases the reliability due to the low component count.

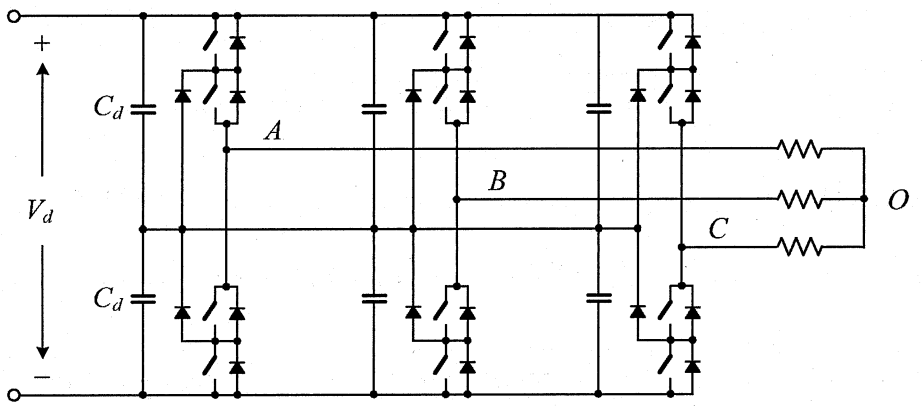


Figure 1-3 Neutral Point Clamped (NPC) Inverter.

Flying-capacitor inverter is shown in Figure 1-4, which consists of a large number of dc capacitors with separate pre-charge circuits. Complex capacitor voltage balancing control also limits the practical use of the flying-capacitor inverter in the drive system [14].

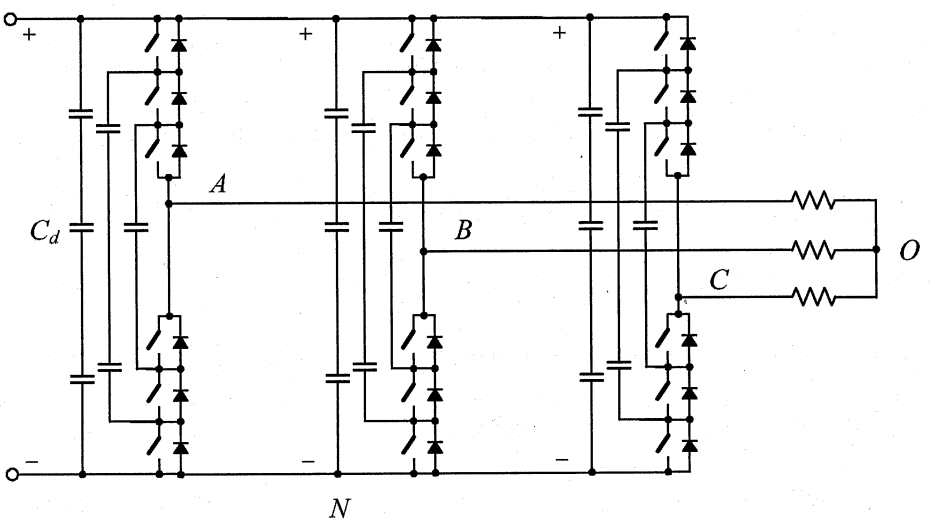


Figure 1-4 Flying Capacitor Inverter.

Unlike above-mentioned multilevel inverters, the CHB inverter shown in Figure 1-5 enable to generate nearly sinusoidal AC output voltage waveforms with small voltage steps, and normally does not require any filters at its output. The motor is protected from high *dv/dt* stresses and minimal harmonic power losses. Modular construction reduces the cost and easily replacement for the defective power cells. Using the multipulse diode rectifier as front end converter with proper PWM scheme, the multilevel CHB inverter produces almost sinusoidal current waveform on line-side. Although it has disadvantages of high cost of phase-shifting transformer, large number of cables and components, the multilevel CHB inverter is still one of the popular inverter topologies for the MV drive [15, 16].

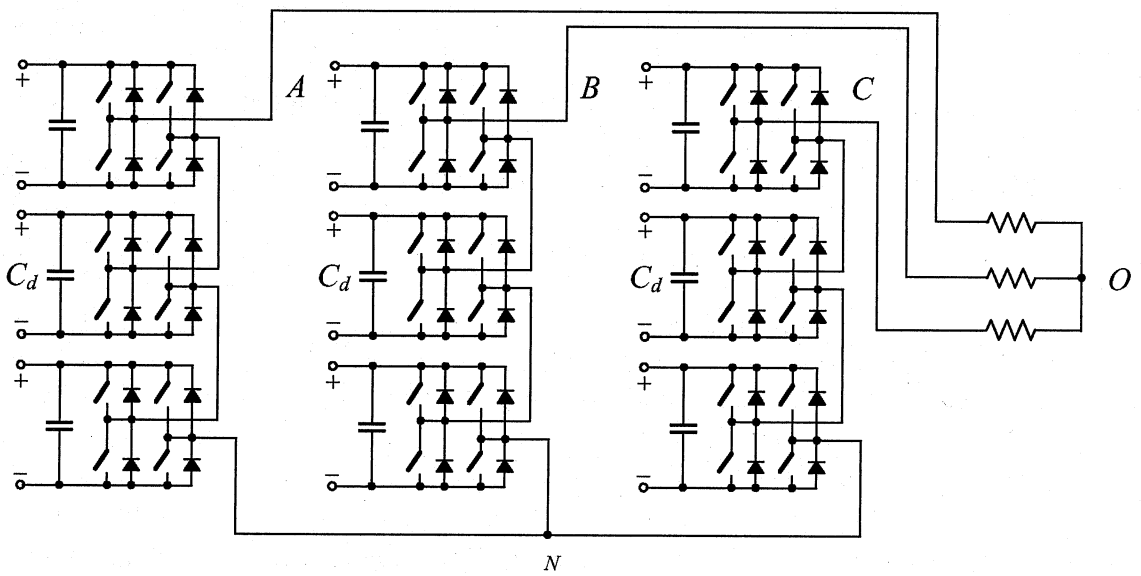


Figure 1-5 Cascaded H-bridge (CHB) Inverter.

After comparison and analysis the above-mentioned topologies, the CHB inverters have been selected as a preferred inverter topology for high voltage and high power applications because they possess the features: lower voltage THD and *dv/dt*, modular

structure and high voltage operation without switching devices in series.

1.2 Modulation Schemes

The conventional modulation schemes for the multilevel CHB inverter include spave vector modulation and carrier-based sinusoidal modulations with phase- and level-shifted techniques [15-18].

(a) Space Vector Modulation

The space vector modulation (SVM) for multilevel inverters is suitable for digital implementation. However, it is a very complex modulation scheme for high-level inverters due to the high number of space vectors and redundant switching states [19-21]. The practical application of the SVM scheme in multilevel CHB inverters seems not reported. Figure 1-6 illustrated the space vector diagram, in which the vectors from inner to outer are from 2 to 9-level inverters. Figure 1-6 contains many small triangles and the vertex of each triangle represents a space vector. For the 7-level inverter, there are 216 small triangles, 343 switching states which correspond to 127 voltage vectors. Each space vector corresponds to a switching state, and each switching state produces a defined inverter output voltage. The reference voltage vector $\vec{V}_{ref}$ rotates in space for one revolution, the inverter output voltage changes one fundamental cycle. The magnitude of the inverter fundamental output voltage corresponds to length of the reference vector while its frequency corresponds to the rotating speed of the reference vector.

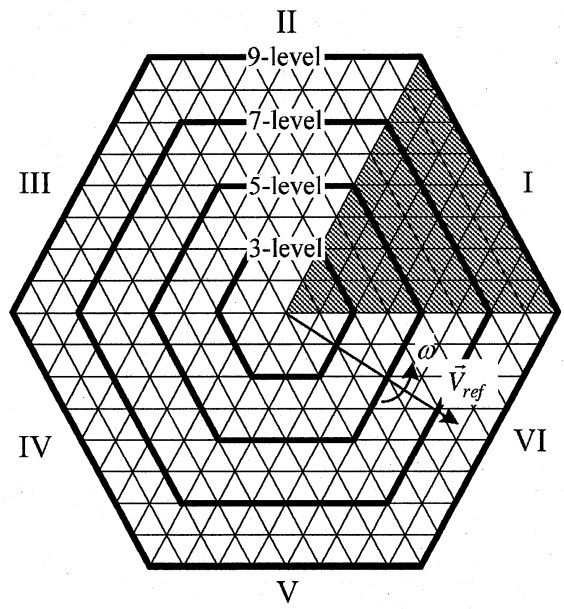


Figure 1-6 Space vector diagram.

(b) Carrier-based Modulation

The carrier-based modulation schemes for multilevel inverter can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the CHB inverters [23, 24].

Figure 1-7 shows the phase-shifted modulation for seven-level inverters. For the cascaded inverter, phase-shifted carrier PWM is the most common strategy using in industry. In general, a multilevel inverter with m voltage levels needs (m–1) triangular carriers. In the phase shifted modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase-shift between any two adjacent carrier waves, given by $\phi_{cr} = 360°/(m-1)$. The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with the carrier waves. However, from motor-side

point of view, line-to-line voltage THD is worse than one of level-shifted modulation scheme called in-phase disposition (IPD). Comparison will be provided by the later chapter.

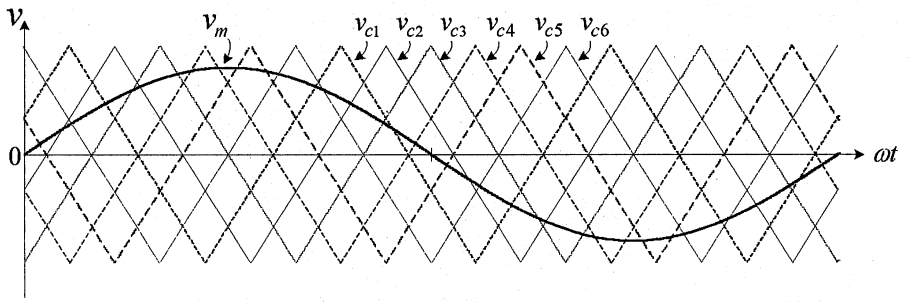


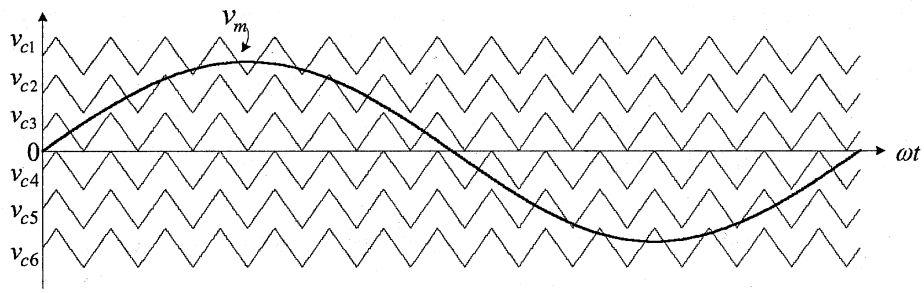
Figure 1-7 Phase-shifted modulation scheme.

Similar to the phase-shifted modulation, a *m*-level inverter using level-shifted modulation scheme requires (*m*–1) triangular carriers, all having the same frequency and amplitude. The (*m*–1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. Figure 1-8 illustrates the principle of the level-shifted modulation scheme for a seven-level CHB inverter.

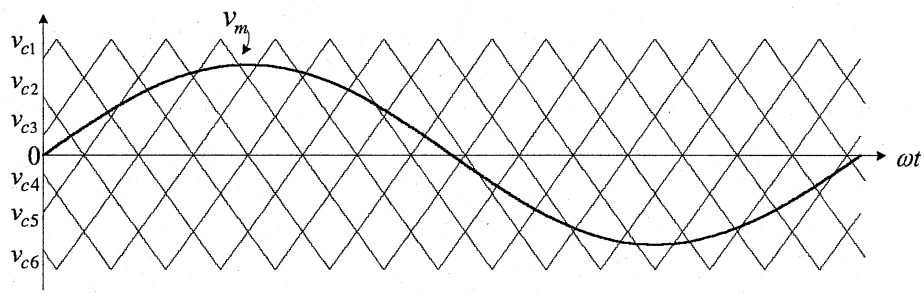
Level-Shifted modulation schemes are generally classified by three categories: (a) In-Phase Disposition (IPD), where the phase for all carriers are same; (b) Alternative Phase Opposition Disposition (APOD), where the phase for each carrier is 180° difference; and (c) Phase Opposition Disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference. Figure 1-8 illustrates level-shifted multicarrier modulation for seven-level inverters.

IPD modulation scheme has its fatal weakness – unequal switching frequency among the switching devices. To evenly distribute the switching and conduction losses, the

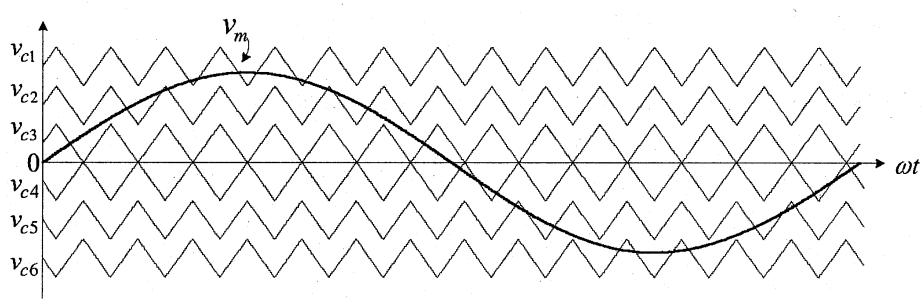
switching pattern should rotate among the H-bridge cells.



(a) In-phase disposition (IPD)



(b) Alternative phase opposition disposition (APOD)



(c) Phase opposition disposition (POD)

Figure 1-8 Level-shifted multicarrier modulation for seven-level inverters.

1.3 Technical Challenges

Two traditional modulation schemes, phase-shifted and IPD, both have drawback and merit. THD of v_{AB} generated by the phase-shifted modulation is higher than the level-shifted modulation in all range from $m_a = 0.2$ to 1.0.

Although IPD possess better line-to-line voltage THD on motor-side, its unbalanced

power distribution feature makes it impossible to cancel low order harmonics on line-side by multipulse shifted transformer. Technique challenge for this research project is to keep advantage of both modulation schemes and overcome the drawbacks.

1.4 Research Objectives

The main objectives of this project are to develop a novel modulation scheme for Cascaded H-bridge (CHB) multilevel inverters in order to possess the following advantages: 1) balanced power consumption in each power cell like phase-shifted modulation scheme; 2) line-to-line voltage THD of inverter output as low as IPD level-shifted modulation scheme; 3) easily digital implementation to beat SVM; and 4) without increasing device switching frequency.

1.5 Project Outline

The project consists of five chapters. Chapter 1 provides a critical review of multilevel inverter topologies and its modulation schemes for high power AC drives, technique difficulty and the objectives of the project.

Chapter 2 introduces several modulation schemes for the CHB multilevel inverter including phase-shifted, level-shifted and some rotating pattern schemes. Theoretical analysis and compare the merit and drawback of phase-shifted and level-shifted (IPD) and current rotating pattern.

Chapter 3 presents the algorithm of Digital Multilevel Modulation (DMM) scheme and emphatically analyzes the results obtained through computer simulation. THD profile of inverter line-to-line voltage on motor side generated by phase-shifted, IPD and DMM

schemes are analyzed and compared.

Chapter 4 presents the analysis and comparison of line current THD profile generated by phase-shifted, IPD and DMM schemes. It shows that DMM scheme keeps the low THD feature of line-to-line voltage as IPD modulation scheme on motor-side and prevents the unbalance consumption problem of power cells.

Chapter 5 summarizes the conclusions of the project and gives the recommendation for the future works. Other supporting materials and more detailed waveforms are attached in the appendices.

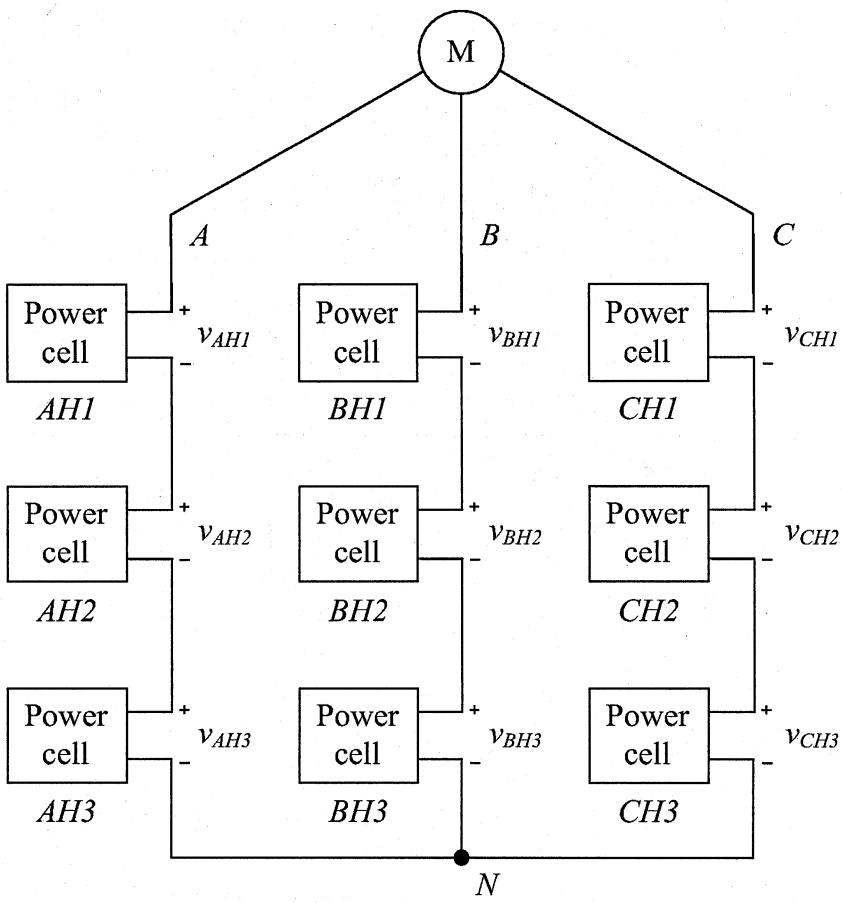
Chapter 2 Modulation Schemes for CHB Inverters

2.1 Introduction

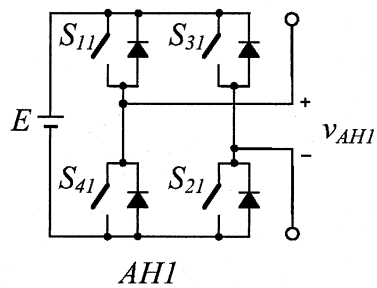
The multilevel CHB inverters are one of the popular inverter topologies for the MV drive due to higher voltage operating capability, lower *dv/dt* and more sinusoidal output [15, 16]. They have been particularly used in very high power applications because of their modularity and attractive input current harmonics cancellation.

PWM techniques are widely used to generate gating signals for the switching devices. By proper design of the gating pattern, the output amplitude and frequency can be conveniently adjusted, and lower frequency harmonics can be removed or substantially reduced. Level-Shifted and phase-shifted modulation schemes are two categories of carrier-based PWM schemes.

This chapter introduces the CHB topology and modulation scheme for high-power MV drives. The performance of level-shifted modulation is compared with phase-shifted modulation. This chapter analyzes the characteristics of IPD modulation scheme which has better line-to-line voltage THD than the others. Recent several even power distribution modulation schemes are compared with merit and drawback.



(a) Block diagram



(b) Power cell

Figure 2-1 A seven-level CHB inverter topology.

Fig. 2-1 shows a seven-level CHB inverter topology with block diagram and power cell. The upper and lower switches in the same inverter leg operate in a complementary manner. The switching state of power cell is summarized in Table 2-1. When $v_{AH1}=0$,

there are a redundant switching state. It can be by turning on S_{11} and S_{31} or turning on S_{21} and S_{41}.

Table 2-1 Switching state of single-phase H-bridge inverter power cell

S_{11}	S_{21}	S_{31}	S_{41}	v_{AH1}
On	On	Off	Off	E
Off	Off	On	On	$-E$
On	Off	On	Off	0
Off	On	Off	On	0

2.2 Phase-Shifted Modulation Schemes

A multilevel inverter with m voltage levels requires $(m - 1)$ triangular carriers. A phase shift between any two adjacent carrier waves is given by the following formula.

$$\phi_{cr} = 360°/(m-1) \tag{2-1}$$

For seven-level phase shifted modulation, it consists of three modulating signals v_{mA}, v_{mB}, v_{mC} and six triangular carrier signals v_{cr1}, v_{cr2}, v_{cr3}, v_{cr1-}, v_{cr2-}, v_{cr3-}. The modulating signal is usually a three-phase sinusoidal wave. The triangular carrier signal has a 60° phase displacement between any two adjacent carriers for each phase.

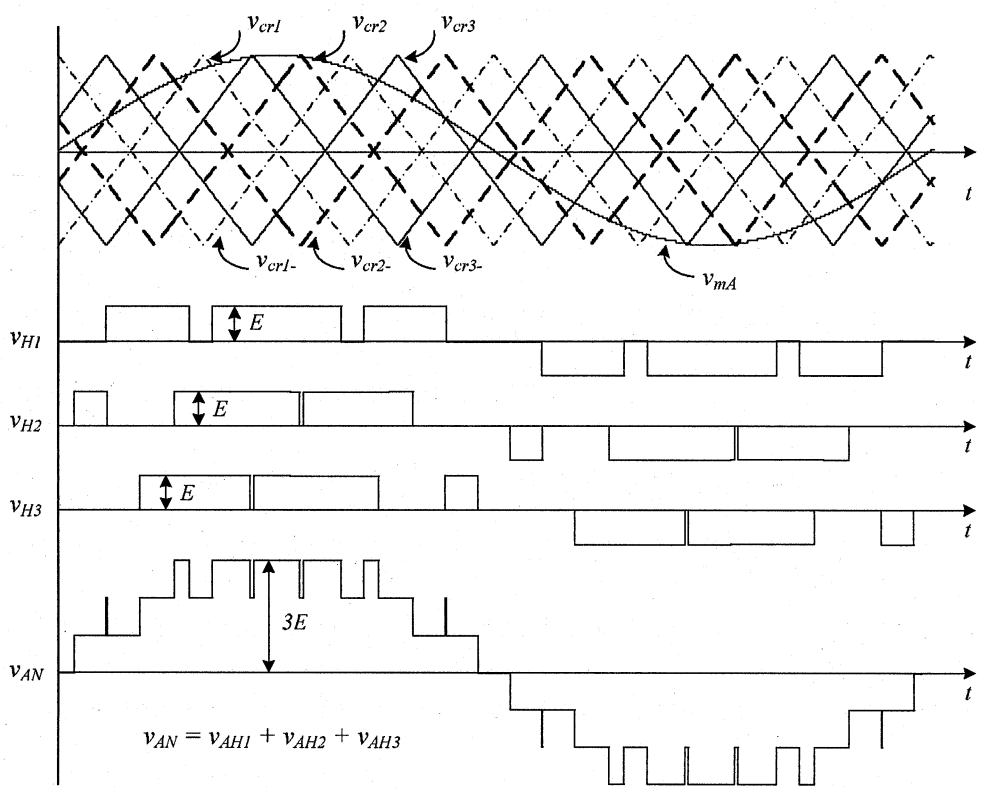


Figure 2-2 Phase-shifted PWM for seven-level CHB inverters ($m_f = 3$, $m_a = 1$, $f_m = 60Hz$ and $f_{cr} = 180Hz$).

The carriers, v_{cr1}, v_{cr2} and v_{cr3} are used to generate gate signals for the upper switches S_{11}, S_{12} and S_{13} in the left legs of power cells *H1*, *H2* and *H3*, respectively. For example, the output of gate signal v_{g11} is high when $v_{mA} \geq v_{cr1}$. The other three carriers, v_{cr1-}, v_{cr2-} and v_{cr3-}, are 180° out of phase with v_{cr1}, v_{cr2} and v_{cr3}, respectively. The carriers of v_{cr1-}, v_{cr2-} and v_{cr3-} will produce the gate signals for the upper switches S_{31}, S_{32} and S_{33} in the right legs of the H-bridge cells. For instance, the output of gate signal v_{g31} is high when $v_{mA} \leq v_{cr1-}$. Figure 2-2 illustrates simulated waveforms for a seven-level CHB inverters with phase-shifted PWM operated under the condition of $m_f = 3$, $m_a = 1.0$, $f_m = 60Hz$

and $f_{cr} = 180Hz$. The inverter phase voltage can be found by the following equation

$$v_{AN} = v_{H1} + v_{H2} + v_{H3} \tag{3-2}$$

In general, it is assumed that the average device switching frequency is same for both schemes in order to compare the performance of modulation scheme. The device switching frequency of phase-shifted PWM scheme is defined as $f_{sw,dev} = f_{cr} = f_m \times m_f$. When the device switching frequency of phase-shifted modulation scheme is 180Hz under the condition shown in Figure 2-2, there are total 18 pulses in modulation wave cycle where each power cells produce 6 pulses. Three waveforms of v_{H1}, v_{H2} and v_{H3} have a small phase displacement caused by the phase-shifted carriers, but they are almost identical. That makes phase-shifted modulation scheme much more widely used in industry because balanced power consumption in each power cell can reduce line current THD on supply side by using multi-pulse shifted transformer.

2.3 Level-Shifted Multicarrier Modulation

Although phase-shifted modulation scheme is already widely used in industry, it cannot provide the best harmonic profile on motor side compared with IPD, one of level-shifted modulation scheme. Similar to the phase-shifted modulation, level-shifted modulation require same number carriers. However, in level shifted PWM scheme, the carriers are shifted not in phase, but in voltage. The rules for generating gate signals are also same. When v_{mA} is higher than the corresponding carriers, v_{cr1}, v_{cr2} and v_{cr3} are used to generate gate signals for the upper switches S_{11}, S_{12} and S_{13} in the left legs of power cells *H1*, *H2* and *H3*, respectively. When v_{mA} is lower than the corresponding carriers, v_{cr1-},

v_{cr2-} and v_{cr3-} will produce the gate signals for the upper switches S_{31}, S_{32} and S_{33} in the right legs of the H-bridge cells. Figure 2-3 illustrates simulated waveforms for a seven-level CHB inverters with IPD modulation operated under the condition of $m_f = 15$, $m_a = 0.8$, $f_m = 60Hz$ and $f_{cr} = 900Hz$.

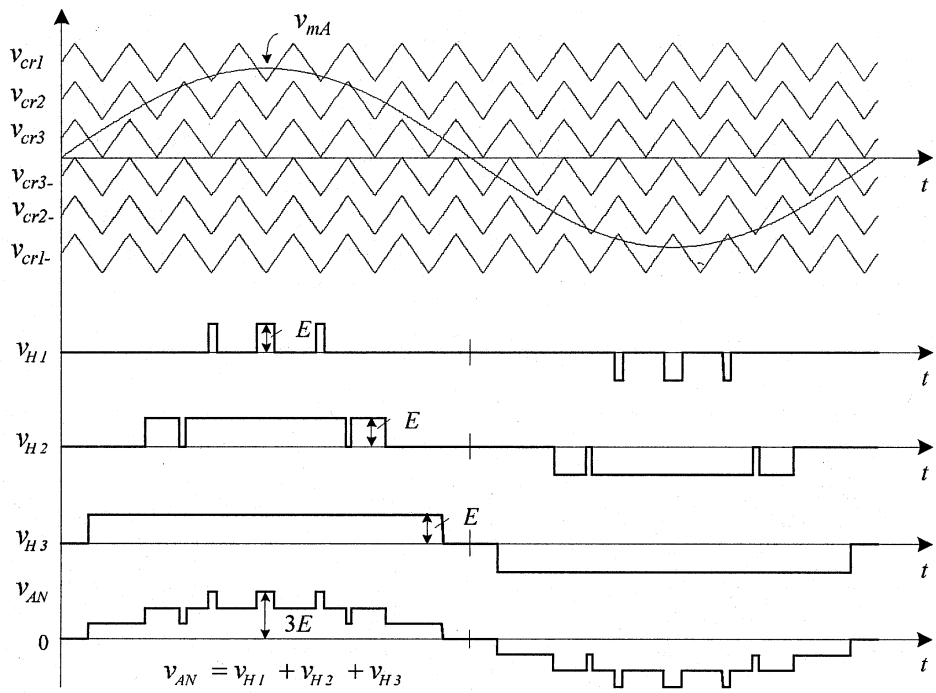


Figure 2-3 IPD PWM for seven-level CHB inverters ($m_f = 15$, $m_a = 0.8$, $f_m = 60Hz$ and $f_{cr} = 900Hz$).

Figure 2-4 shows line-to-line voltage v_{AB} and THD of IPD, APOD, POD and phase shifted modulation scheme for seven-level CHB inverters under the condition $m_a = 1.0$, $m_f = 60Hz$, and $f_{sw,dev} = 600Hz$. The THD of v_{AB} produced by IPD is 10.31%, much lower than other modulation scheme.

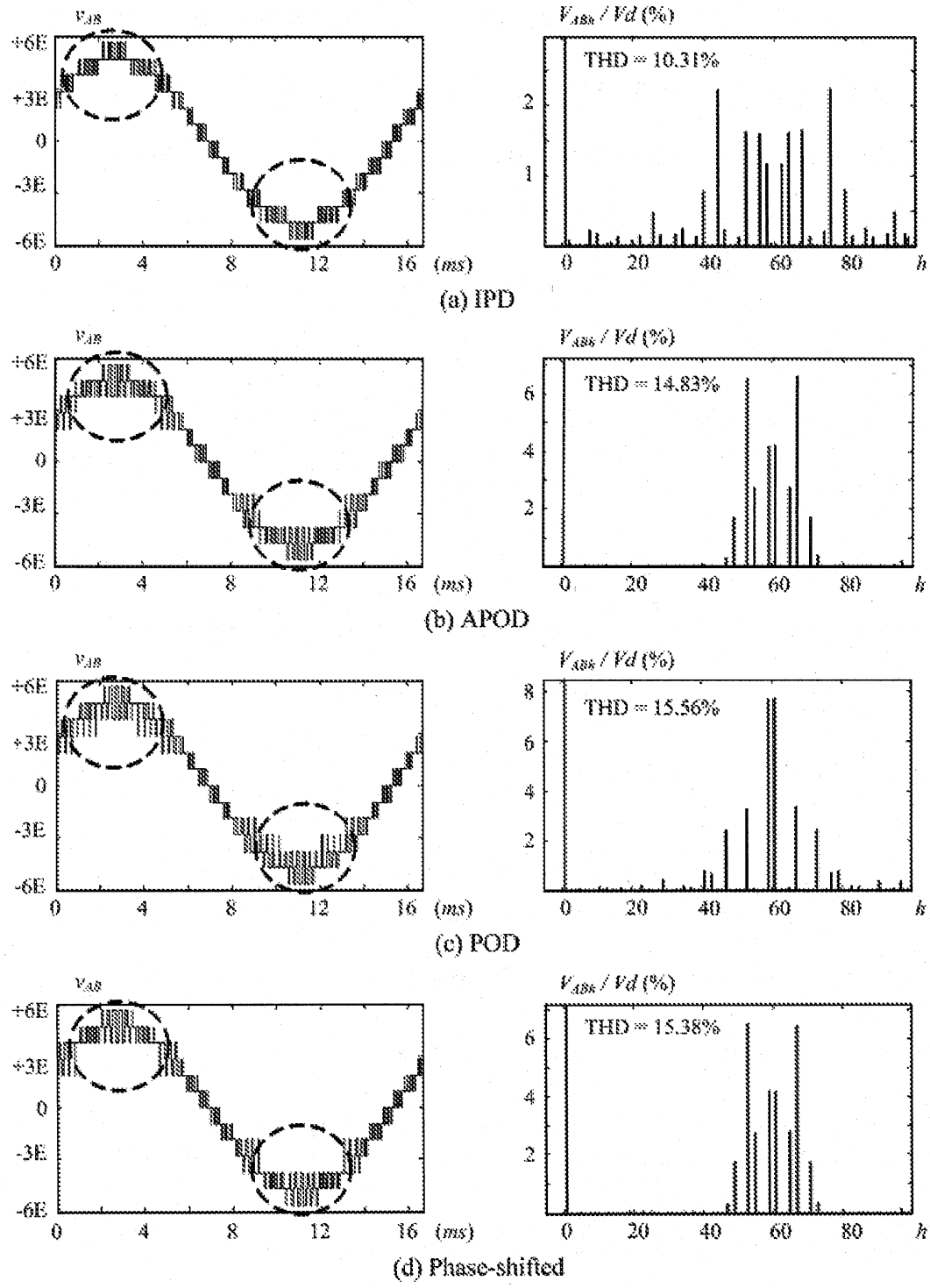


Figure 2-4 Line-to-line voltage v_{AB} and THD of IPD, APOD, POD and phase-shifted modulation scheme for seven-level CHB inverters ($m_a = 1.0$, $m_f = 60Hz$, and $f_{sw,dev} = 600Hz$).

Double Fourier analysis can be used for decomposing the switched waveforms into harmonic series to compare v_{AB} of IPD against the others. In principle, any time-varying waveform can be described by an infinite series of harmonic components. In practice, the switched waveform is representing as a double variable controlled function that is periodic across both the carrier and the modulating waveforms. The harmonics of this function can be expressed in general form as a double summation Fourier series

$$\begin{aligned} F(t) = \frac{A_{00}}{2} &+ \sum_{n=1}^{\infty}\{A_{0n}\cos(n\omega_0 t) + B_{0n}\sin(n\omega_0 t)\} \\ &+ \sum_{m=1}^{\infty}\{A_{m0}\cos(n\omega_c t) + B_{m0}\sin(n\omega_c t)\} \\ &+ \sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}\{A_{mn}\cos(n\omega_c t + n\omega_0 t) + B_{mn}\sin(m\omega_c t + n\omega_0 t)\} \end{aligned} \tag{3-3}$$

The coefficients of (1) are obtained for any particular PWM strategy by evaluating the double Fourier integral of

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} F(x,y)e^{j(mx+ny)}dxdy, \tag{3-4}$$
$$x = \omega_c t;\ y = \omega_0 t$$

From these solutions offered by some papers, it can be seen how IPD modulation achieves its superior line-to-line harmonic performance from theoretic aspect.

2.4 Rotating Switching Pattern Modulation Schemes

IPD modulation scheme operates under the unequal switching frequency among the switching devices, and the conduction time of the devices is not evenly distributed either. To evenly distribute the switching and conduction losses, the switching pattern should

rotate among the H-bridge cells. Rotating switching pattern modulation schemes can be classified into two categories: based on modulation frequency and based on control frequency.

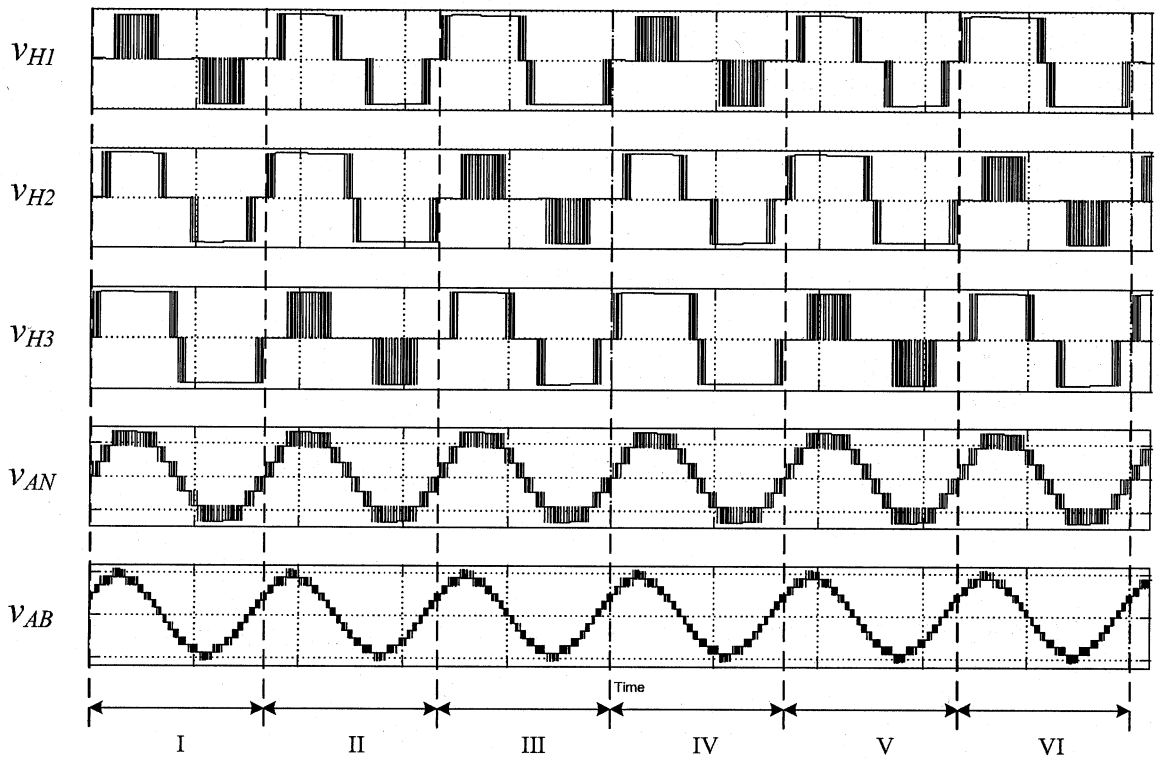


Figure 2-5 Rotating switching pattern modulation schemes based on modulation frequency.

Figure 2-5 illustrates rotating switching pattern modulation schemes based on modulation frequency. In Figure 2-5, this rotating switching pattern scheme shows six periods from period I to VI. It has the following features: operating under the equal switching frequency among the switching devices in three periods; evenly distributed the conduction time of the devices in three periods; evenly distributed switching and conduction losses; not increasing device switching frequency. However, as high power AC drive application, line current i_A on utility supply side shows non-periodical

waveform. Period I is same as period IV. Period II is same as V. Period III is same as VI. Harmonic analysis based on non-periodical waveform is meaningless.

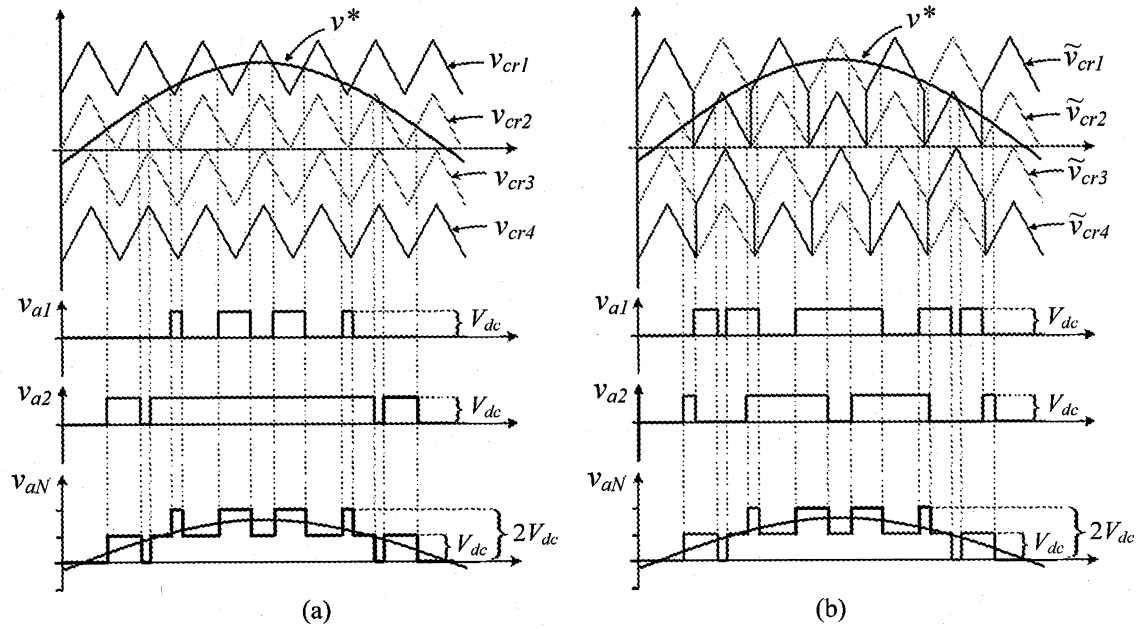


Figure 2-6 Modulation operating principle: a) Traditional IPD PWM, b) Modified rotative IPD PWM.

Due to the drawback of rotating switching pattern based on modulation frequency, mostly current researches focus on rotating switching pattern based on control frequency. Figure 2-6 illustrates one of methods to IPD modulation scheme for CHB inverters with even power distribution [17]. This modulation scheme simply alternate the level shifts between the carriers associated to each cell. Figure 2-7 shows that the carriers are alternated each modulation cycle. However, this strategy obviously increases the device switching frequency especially when the carrier frequencies are higher.

2.5 Summary

This chapter focuses on the modulation schemes for CHB multilevel inverters.

Conversional two carrier based PWM schemes, modulation scheme phase-shifted and level-shifted are investigated in detail. The operating principle of these schemes is discussed and the gate signal arrangements for the switching devices are introduced. Comparison between phase-shifted and IPD modulation scheme are made. This chapter also analyzes the feature and reason why IPD scheme has better line-to-line voltage harmonic profile on inverter side.

To balance the output power of all H-bridge cells in CHB multilevel inverters, pulse rotation patterns for the IPD scheme should be investigated. Rotating switching pattern modulation schemes based on modulation frequency and control frequency are introduced.

Chapter 3 DMM Scheme for CHB Inverters

3.1 Introduction

IPD modulation schemes have good THD profile for analog implementation. However, they are unbalanced power distribution and difficult to swap. Therefore, IPD schemes have limited practical applications.

A new digital multilevel modulation (DMM) scheme is proposed in this chapter. This scheme is very simple to implement and provides good THD profile, and solves the problems in IPD modulation scheme.

In this chapter, theory and algorithm for DMM scheme is elaborated, and its harmonic performance is analyzed. Comparisons are carried out between the DMM scheme and carrier based modulation schemes including phase-shifted and IPD modulations. It is demonstrated that the harmonics of DMM scheme are on a par with the best of carrier based modulation techniques.

3.2 Principle of the Proposed Digital Modulation Scheme

In general, a m-level CHB inverter produces m voltage levels: $+\frac{(m-1)}{2}E$, ..., $+2E$, $+E$, 0, $-E$, $-2E$, ..., $-\frac{(m-1)}{2}E$, where E is the dc voltage of an H-bridge power cell. Figure 3-1 shows a seven-level CHB inverters.

Conventional IPD modulation scheme is easily implemented by analog circuits. However, it is difficult to achieve in a digital modulation system because the intersection between

the modulating sinusoid wave and the triangular carrier is complex to calculate. To overcome this limitation, the DMM scheme calculates sine function only once in the middle of each sampling period on sinusoidal reference wave. This unique simple sampling method is very easy for digital implementation like DSP.

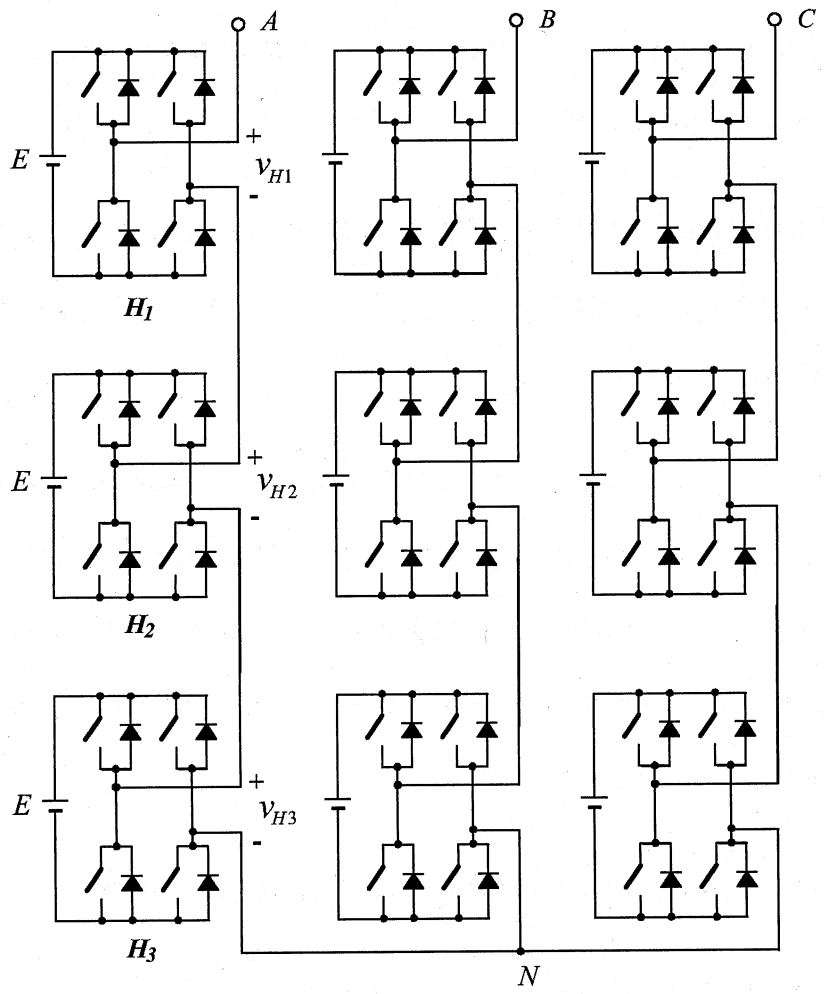


Figure 3-1 Seven-level cascaded H-Bridger inverter.

The principle of DMM scheme for a seven-level CHB inverter is shown in Figure 3-2, where a reference voltage based on DMM scheme is developed. Horizontal axis represents time and vertical axis represents voltage level. In Figure 3-2, DMM scheme directly distribute horizontal-axis into 15 equidistant in one sinusoidal reference cycle

and vertical-axis into 7 voltage levels from -3E to +3E. For simplicity, the reference voltages for other two inverter phases are not illustrated.

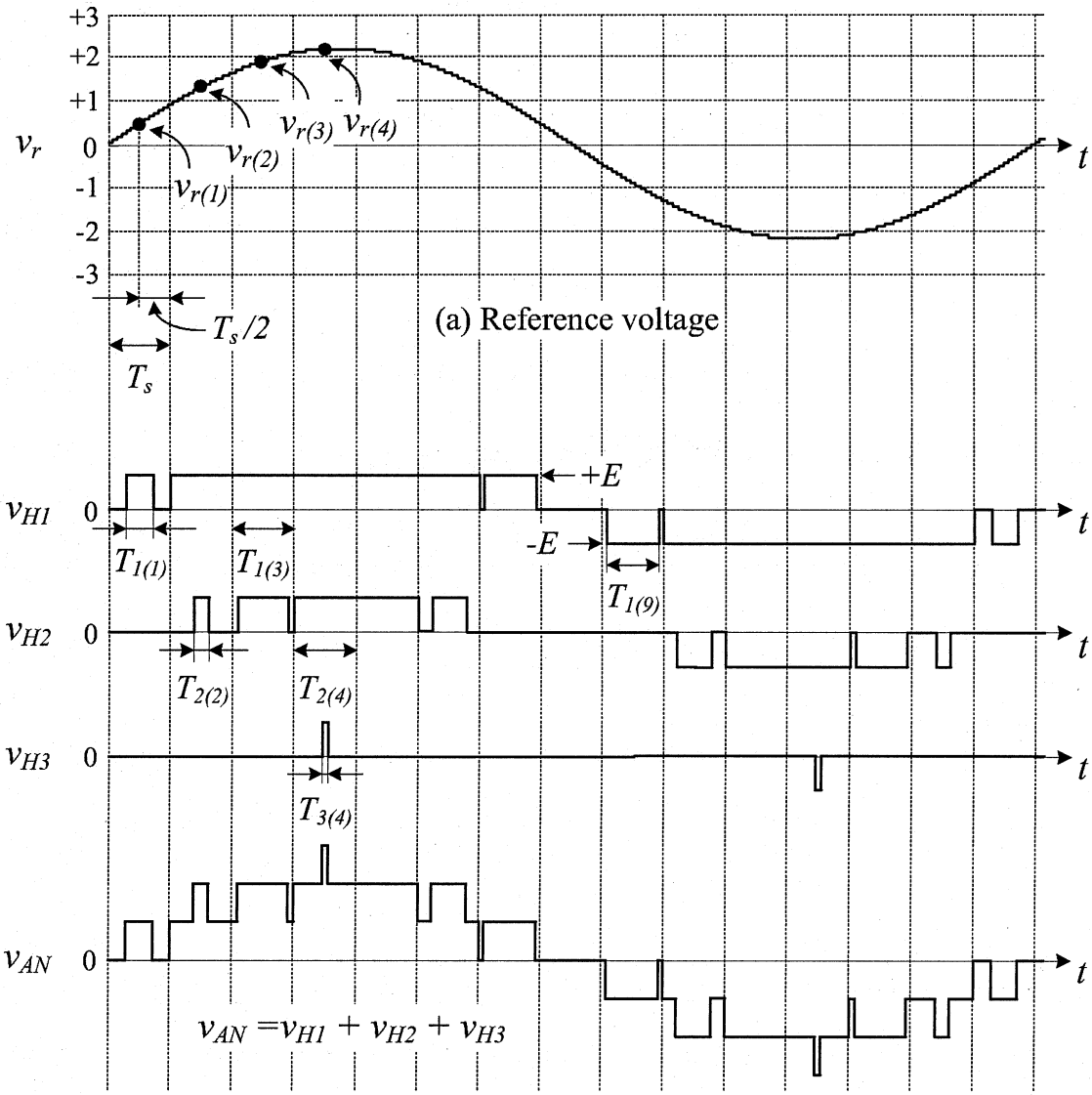


Figure 3-2 Principle of DMM scheme for a seven-level CHB inverter

The reference voltage can be expressed as

$$v_r = \hat{V}_r \sin(2\pi f_r t) \tag{3-1}$$

where $\hat{V}_r$ and f_r are the peak value and frequency of the reference voltage. Similar to carrier based modulation schemes, the amplitude and frequency of the inverter fundamental output voltage can be adjusted by adjusting $\hat{V}_r$ and f_r respectively.

For a given multilevel inverter, the maximum peak value of the reference voltage is

$$\hat{V}_{r,\max} = n = \frac{m-1}{2} \tag{3-2}$$

where n is the number of H-bridges in cascade per phase and m is the number of voltage levels of the CHB inverter. For a seven-level inverter, $\hat{V}_{r,\max} = 3$.

The period of the reference voltage v_r can be divided into a number of sampling periods of T_s as shown in Fig. 3-2. The sampled reference voltage in the k^{th} sampling period can be calculated by

$$v_{r(k)} = \hat{V}_r \sin\left[2\pi f_r\left(k-\frac{1}{2}\right)T_s\right] \qquad k = 1, 2, 3, \ldots \tag{3-3}$$

The sampled reference voltage $v_{r(k)}$ is then used to generate the gating signals for the switching devices in the inverter.

To facilitate the analysis, let's define the duty cycle for the individual H-bridges:

$$\begin{cases} D_{1(k)} = T_{1(k)} / T_s & 0 \le D_{1(k)} \le 1 \quad \text{for } H_1 \\ D_{2(k)} = T_{2(k)} / T_s & 0 \le D_{2(k)} \le 1 \quad \text{for } H_2 \\ \quad \ldots\ldots & \\ D_{n(k)} = T_{n(k)} / T_s & 0 \le D_{n(k)} \le 1 \quad \text{for } H_n \end{cases} \tag{3-4}$$

where $D_{1(k)}$, $D_{2(k)}$ and $D_{n(k)}$ are the duty cycles for the H-bridges H_1, H_2 and H_n, and $T_{1(k)}$, $T_{2(k)}$ and $T_{n(k)}$ are their corresponding turn-on times during sampling period k, respectively. The turn-on time refers to the time period that an H-bridge outputs a $+E$ or $-E$ as shown in Figure 3-2, where E is the dc voltage of an H-bridge.

The total duty cycle of the multilevel CHB inverter is then defined by

$$D_{T(k)} = D_{1(k)} + D_{2(k)} + ... + D_{n(k)} \qquad 0 \leq D_{T(k)} < n \tag{3-5}$$

Since the maximum duty cycle for an H-bridge is 1.0, the maximum total duty cycle for the multilevel CHB inverter is equal to the number of H-bridges in cascade, which is also equal to maximum peak reference voltage, i.e.,

$$D_{T,\max} = n = \hat{V}_{r,\max} \tag{3-6}$$

Correspondingly, the total duty cycle of the CHB inverter in a sampling period is equal to the reference voltage:

$$D_{T(k)} = \left| v_{r(k)} \right| \tag{3-7}$$

There are only three simple steps to implement the proposed DMM scheme: i) calculate the reference voltage $v_{r(k)}$ and total duty cycle $D_{T(k)}$ given in equation (3-1) and (3-7), ii) distribute among the H-bridges, and iii) generate gate signals based on the duty cycle of each H-bridge.

Table 3-1 shows the distribution of total duty cycle $D_{T(k)}$ for a seven-level CHB inverter during the first four sampling periods in Figure 3-2. During sampling period 1, the

reference voltage $v_{r(1)}$ in the middle of the sampling period can be calculated as follows:

$v_{r(1)} = 2.1 * \sin\left\{2 * 3.14 * 60 * \left[\left(1 - \frac{1}{2}\right) * \frac{1}{900}\right]\right\} = +0.4$, and the total duty cycle of 0.4 is assigned to only one of the H-bridges. During period 2, the reference voltage $v_{r(2)}$ is 1.2, which is higher than the maximum duty cycle of an H-bridge. The total duty cycle of 1.2 is distributed to two H-bridges. During sampling period 4, the reference voltage $v_{r(4)}$ is 2.1, which is higher than the sum of the two maximum duty cycles for two H-bridges. The total duty cycle of 2.1 is then distributed among three H-bridges. It should be noted that the distribution of $D_{T(k)}$ is not unique, and Table 1 is the simplest method. Further discussions on this issue are provided in the subsequent sections.

Table 3-1 Distribution of total duty cycle $D_{T(k)}$ for a seven-level CHB inverter in the first forth sampling period

Sampling Period k	1	2	3	4
$D_{T(k)} = \lvert v_{r(k)} \rvert$	0.4	1.2	1.8	2.1
$D_{1(k)} = T_{1(k)} / T_s$	0.4	1	1	1
$D_{2(k)} = T_{2(k)} / T_s$	0	0.2	0.8	1
$D_{3(k)} = T_{3(k)} / T_s$	0	0	0	0.1

Once the duty cycle for the H-bridges is determined, the gating signals for the switching devices can be generated, and resultant PWM output voltages, v_{H1}, v_{H2} and v_{H3}, are shown in Figure 3-2. The phased voltage of the seven-level CHB inverter is then given by

$$v_{AN} = v_{H1} + v_{H2} + v_{H3} \tag{3-8}$$

Obviously, the inverter phase voltage v_{AN} contains seven voltage levels.

Through the observation of the waveform v_{H1}, v_{H2} and v_{H3}, it is not difficult to find that power distribution for each power cell is not balanced. To evenly distribute the switching conduction losses, rotating switching pattern among the H-bridge cells is the way to solve the problem.

3.3 Pattern Rotation for Even Power Distribution

It can be observed from Figure 3-2 that the three H-bridges in cascade have neither the same duty cycle nor the switching frequency. This implies that the H-bridges do not deliver the same output power and their conduction/switching losses are not the same either. This phenomenon also occurs in the level-shifted modulation scheme. However, the proposed DMM scheme can easily solve the problem by the rotating the switching modes of the H-bridges.

3.3.1 Switching Mode and Rotating Sequence in a Positive Half Cycle

For m-level CHB inverters, there exist (m-1)/2 switching modes. Table 3-2 provides a summary of three switching modes for a seven-level CHB inverter and their rotating sequence during a positive half cycle of the inverter output voltage. Modes I, II and III are employed in the 1st, 2nd and 3rd sampling periods, respectively, and this sequence is repeated every three sampling periods. Such an arrangement can ensure a balanced output power and equal power losses among the H-bridges in multilevel CHB inverters.

Table 3-2 Duty cycle and rotating sequence I

Duty Cycle		Mode I	Mode II	Mode III
$0 \le D_{T(k)} \le 1$	$D_{1(k)}$	$D_{T(k)}$	0	0
	$D_{2(k)}$	0	$D_{T(k)}$	0
	$D_{3(k)}$	0	0	$D_{T(k)}$
$1 < D_{T(k)} \le 2$	$D_{1(k)}$	1	0	$D_{T(k)} - 1$
	$D_{2(k)}$	$D_{T(k)} - 1$	1	0
	$D_{3(k)}$	0	$D_{T(k)} - 1$	1
$2 < D_{T(k)} \le 3$	$D_{1(k)}$	1	$D_{T(k)} - 2$	1
	$D_{2(k)}$	1	1	$D_{T(k)} - 2$
	$D_{3(k)}$	$D_{T(k)} - 2$	1	1

The output waveforms of the CHB inverter using the rotating sequence I are illustrated in Table 3-3. It can be observed that i) the rotation of the switching modes does not affect the waveform of the inverter phase voltage v_{AN}, and ii) extra switchings may occur due to the change of switching modes as indicated by circles in the table. Pulse pattern in accordance with Table 3-2 is not unique. Pulse can be produced by any power cells such as H_1, H_2 or H_3.

Table 3-3 Output voltage waveforms of a seven-level CHB inverter with rotating sequence I

D_T	V_H	Mode I	Mode II	Mode III
$0 \le D_{T(k)} \le 1$	$V_{H1(k)}$	0 E 0	0 0 0	0 0 0
	$V_{H2(k)}$	0 0 0	0 E 0	0 0 0
	$V_{H3(k)}$	0 0 0	0 0 0	0 E 0
	$V_{AN(k)}$	0 E 0	0 E 0	0 E 0
$1 < D_{T(k)} \le 2$	$V_{H1(k)}$	E E E	0 0 0	0 E 0
	$V_{H2(k)}$	0 E 0	E E E	0 0 0
	$V_{H3(k)}$	0 0 0	0 E 0	E E E
	$V_{AN(k)}$	2E / E E	2E / E E	2E / E E
$2 < D_{T(k)} \le 3$	$V_{H1(k)}$	E E E	0 E 0	E E E
	$V_{H2(k)}$	E E E	E E E	0 E 0
	$V_{H3(k)}$	0 E 0	E E E	E E E
	$V_{AN(k)}$	3E / 2E 2E	3E / 2E 2E	3E / 2E 2E

To avoid extra switchings, the total duty cycle of the CHB inverter can be redistributed without affecting the inverter phase voltage v_{AN}. Table 3-4 shows the redistributed duty cycles and rotating sequence II during a positive half cycle of the inverter fundamental voltage. The corresponding voltage waveforms are given in Table 3-5. It is clearly shown

that i) no extra switchings take place during the change of the switching modes, and ii) for a given duty cycle the inverter phase voltage v_{AN} is not affected by the rotation of the switching modes.

Table 3-4 Duty cycle and rotating sequence II

Duty Cycle		Mode I	Mode II	Mode III
$0 \le D_{T(k)} \le 1$	$D_{1(k)}$	$D_{T(k)}$	0	0
	$D_{2(k)}$	0	$D_{T(k)}$	0
	$D_{3(k)}$	0	0	$D_{T(k)}$
$1 < D_{T(k)} \le 2$	$D_{1(k)}$	$D_{T(k)} / 2$	0	$D_{T(k)} / 2$
	$D_{2(k)}$	$D_{T(k)} / 2$	$D_{T(k)} / 2$	0
	$D_{3(k)}$	0	$D_{T(k)} / 2$	$D_{T(k)} / 2$
$2 < D_{T(k)} \le 3$	$D_{1(k)}$	1	$(D_{T(k)} - 1) / 2$	$(D_{T(k)} - 1) / 2$
	$D_{2(k)}$	$(D_{T(k)} - 1) / 2$	$(D_{T(k)} - 1) / 2$	1
	$D_{3(k)}$	$(D_{T(k)} - 1) / 2$	1	$(D_{T(k)} - 1) / 2$

Table 3-5 Output voltage waveforms of a seven-level CHB inverter with rotating sequence II

D_T	V_H	Mode I	Mode II	Mode III
$0 \le D_{T(k)} \le 1$	$V_{H1(k)}$	0 E 0	0 0 0	0 0 0
	$V_{H2(k)}$	0 0 0	0 E 0	0 0 0
	$V_{H3(k)}$	0 0 0	0 0 0	0 E 0
	$V_{AN(k)}$	0 E 0	0 E 0	0 E 0
$1 < D_{T(k)} \le 2$	$V_{H1(k)}$	E E 0	0 0 0	0 E E
	$V_{H2(k)}$	0 E E	E E 0	0 0 0
	$V_{H3(k)}$	0 0 0	0 E E	E E 0
	$V_{AN(k)}$	2E (E E)	2E (E E)	2E (E E)
$2 < D_{T(k)} \le 3$	$V_{H1(k)}$	E E E	E E 0	0 E E
	$V_{H2(k)}$	E E 0	0 E E	E E E
	$V_{H3(k)}$	0 E E	E E E	E E 0
	$V_{AN(k)}$	3E (2E 2E)	3E (2E 2E)	3E (2E 2E)

Based on the DMM scheme presented above, the waveforms of a seven-level CHB inverter under the condition of $\hat{V}_r = 2.25(75\%)$, $f_r = 60$ Hz and $T_s = 1/2700$ sec are shown in Figure 3-3. It can be summarized that

- The switching frequency and conduction angle of all individual H-bridges are made the same, which results in even switching/conduction losses among all the H-bridges; and

- There are no extra switchings during change of switching modes, and switching losses of the CHB inverter are minimized.

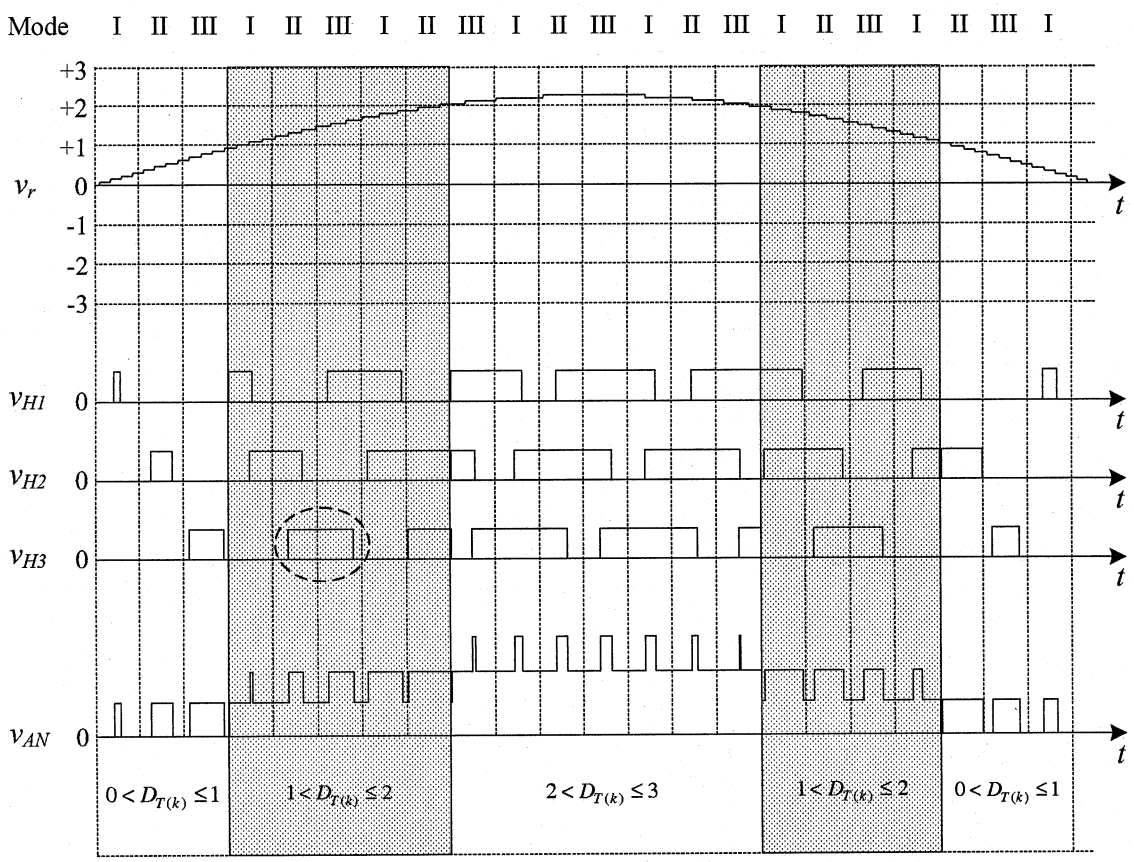
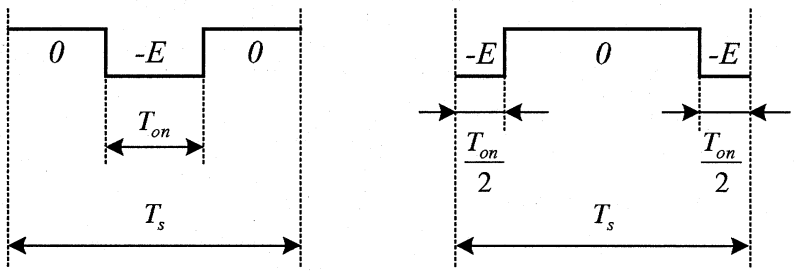


Figure 3-3 Inverter output voltage waveforms produced by the DMM scheme during a positive half cycle ($\hat{V}_r = 2.25(75\%), f_r = 60$ Hz and $T_s = 1/2700$ sec).

3.3.2 Switching Mode and Rotating Sequence during a Negative Half Cycle

For a given duty cycle, the turn-on time T_{on} of an H-bridge during its negative half cycle can have two different arrangements as shown in Figure 3-4. The turn-on time can be centered in the sampling period T_s or can be split into two pulses placed on both sides of the sampling period. The inverter output voltages produced by these two patterns generate an identical fundamental voltage, but have different harmonic spectrum. Further studies have shown that the latter contains less harmonics with lower THD, and therefore is recommended to use.



(a) Pattern I (b) Pattern II

Figure 3-4 Turn-on pulse during the negative half cycle of the inverter fundamental voltage.

Table 3-6 illustrates the distribution of duty cycles and rotating sequence during a negative half cycle of the inverter fundamental voltage in a seven level CHB inverter. The corresponding voltage waveforms are given in Table 3-7, where it is clearly illustrated that i) the turn-on time in v_{AN} is placed on both sides of the sampling period, ii) there are no extra switchings during the change of the switching modes, and iii) the inverter phase voltage v_{AN} does not vary with the switching modes.

Table 3-6 Duty cycle and rotating sequence during a negative half cycle

Duty Cycle		Mode I	Mode II	Mode III
$0 \le D_{T(k)} \le 1$	$D_{1(k)}$	$D_{T(k)} / 2$	0	$D_{T(k)} / 2$
	$D_{2(k)}$	$D_{T(k)} / 2$	$D_{T(k)} / 2$	0
	$D_{3(k)}$	0	$D_{T(k)} / 2$	$D_{T(k)} / 2$
$1 < D_{T(k)} \le 2$	$D_{1(k)}$	1	$(D_{T(k)} - 1) / 2$	$(D_{T(k)} - 1) / 2$
	$D_{2(k)}$	$(D_{T(k)} - 1) / 2$	1	$(D_{T(k)} - 1) / 2$
	$D_{3(k)}$	$(D_{T(k)} - 1) / 2$	$(D_{T(k)} - 1) / 2$	1
$2 < D_{T(k)} \le 3$	$D_{1(k)}$	1	$2 (D_{T(k)} - 2) / 2$	1
	$D_{2(k)}$	1	1	$2 (D_{T(k)} - 2) / 2$
	$D_{3(k)}$	$2 (D_{T(k)} - 2) / 2$	1	1

Table 3-7 Output voltage waveforms of a seven-level CHB inverter during negative half cycle

D_T	V_H	Mode I	Mode II	Mode III
$0 \le D_{T(k)} < 1$	$V_{H1(k)}$	-E 0 0	0 0 0	0 0 -E
	$V_{H2(k)}$	0 0 -E	-E 0 0	0 0 0
	$V_{H3(k)}$	0 0 0	0 0 -E	-E 0 0
	$V_{AN(k)}$	-E 0 -E	-E 0 -E	-E 0 -E
$1 \le D_{T(k)} < 2$	$V_{H1(k)}$	-E -E -E	-E 0 0	0 0 -E
	$V_{H2(k)}$	0 0 -E	-E -E -E	-E 0 0
	$V_{H3(k)}$	-E 0 0	0 0 -E	-E -E -E
	$V_{AN(k)}$	-E -2E -2E	-E -2E -2E	-E -2E -2E
$2 \le D_{T(k)} < 3$	$V_{H1(k)}$	-E -E -E	-E 0 -E	-E -E -E
	$V_{H2(k)}$	-E -E -E	-E -E -E	-E 0 -E
	$V_{H3(k)}$	-E 0 -E	-E -E -E	-E -E -E
	$V_{AN(k)}$	-2E -3E -3E	-2E -3E -3E	-2E -3E -3E

3.4 Computer Simulation

Figure 3-5 illustrates simulated voltage waveforms and their harmonic spectra for a seven-level CHB inverter using the proposed DMM scheme, where V_d is the total dc voltage of an inverter phase given by $V_d = E\ (m - 1) / 2$ and h is the harmonic order. The inverter operates under the condition of $\hat{V}_r = D_T$ =2.4(80%), f_r = 60Hz and T_s = 1/3600sec. It can be observed from the waveforms of v_{H1}, v_{H2} and v_{H3} that the implementation of the rotating sequence makes the H-bridges operate at the same switching frequency with the same conduction period. As a result, the H-bridges operate in a balanced condition with the same power handling capability and power losses. Although the output voltages of v_{H1}, v_{H2} and v_{H3} are slightly different, DMM scheme is much more balanced power distribution than conversional IPD PWM scheme.

The waveforms of the inverter phase voltage v_{AN} and line-to-line voltage v_{AB} are also given in the figure together with their harmonic spectrum. Similar to the carrier based modulations, the DMM scheme generates a number of harmonics centered on the inverter switching frequency of 3600 Hz, which is also the sampling frequency of the system. The inverter phase voltage has a higher THD value due to the triplen harmonics, such as 60^{th} and $(60\pm6)^{th}$. These harmonics do not appear in the line-to-line voltages due to the three-phase balanced operation. It is noted that the magnitude of low order harmonics is negligibly small, which is also a good feature of this modulation scheme.

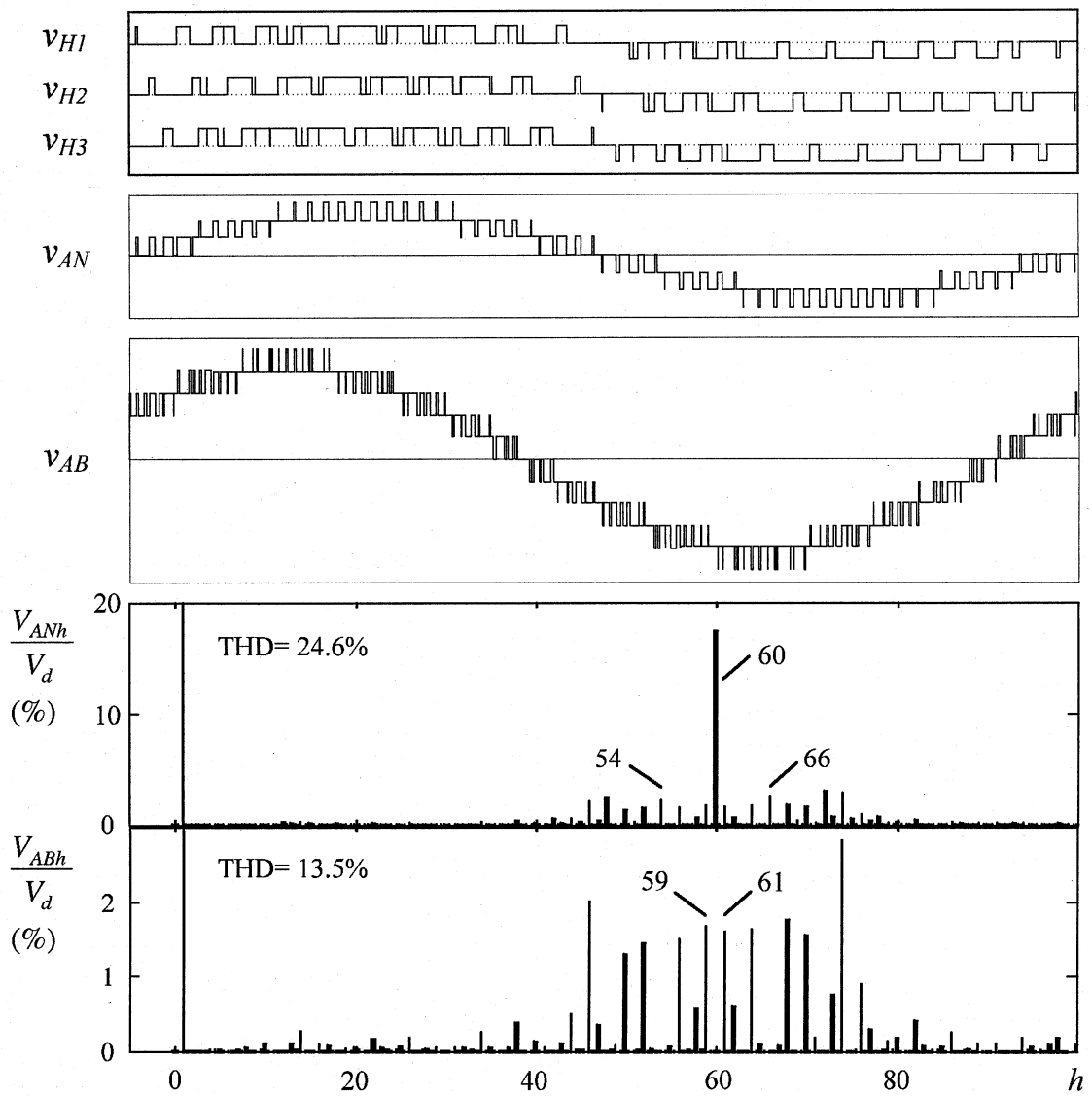


Figure 3-5 Simulated waveforms and harmonic spectra for a seven-level CHB inverter

($\hat{V}_r = 2.4(80\%), f_r = 60\text{Hz}$ and $T_s = 1/3600\text{sec}$).

To prove the power consumption for DMM scheme is balanced, conduction angle of each switch is calculation under the same condition. Table 3-8 and Table 3-9 illustrate conduction angle of switches within one fundamental period for IPD and DMM scheme, respectively. S_1=180 represents that conduction angle for switch S_1 is 180°.

Table 3-8 shows that the conduction angle for IPD modulation scheme in each switch is apparently different from different switch within one power cell. For instant, S_1 in power cell H_1 of phase A is 61°, but become 299° for S_2 in same power cells. For different power cells, conduction angle for IPD modulation scheme is also different. For example, S_2=299° in power cell H_1 in phase A, but change to S_2=240.9° in power cell H_2. However, conduction angle for all switches of DMM scheme are almost same 180°. This table further proved power consumption is balanced for DMM scheme.

Table 3-8 Conduction angle of each switch for IPD modulation scheme ($m_a = 1$, $f_m = 60Hz$, $T_{cr} = 1/3600\,\text{sec}$)

Phase A		Phase B		Phase C	
H_1	S_1=61	H_1	S_1=61	H_1	S_1=61
	S_2=299		S_2=299		S_2=299
	S_3=60.8		S_3=60.8		S_3=60.8
	S_4=299.2		S_4=299.2		S_4=299.2
H_2	S_1=119.1	H_2	S_1=119.1	H_2	S_1=119.1
	S_2=240.9		S_2=240.9		S_2=240.9
	S_3=118.8		S_3=118.8		S_3=118.8
	S_4=241.2		S_4=241.2		S_4=241.2
H_3	S_1=160.6	H_3	S_1=160.6	H_3	S_1=160.6
	S_2=199.4		S_2=199.4		S_2=199.4
	S_3=160.2		S_3=160.2		S_3=160.2
	S_4=199.8		S_4=199.8		S_4=199.8

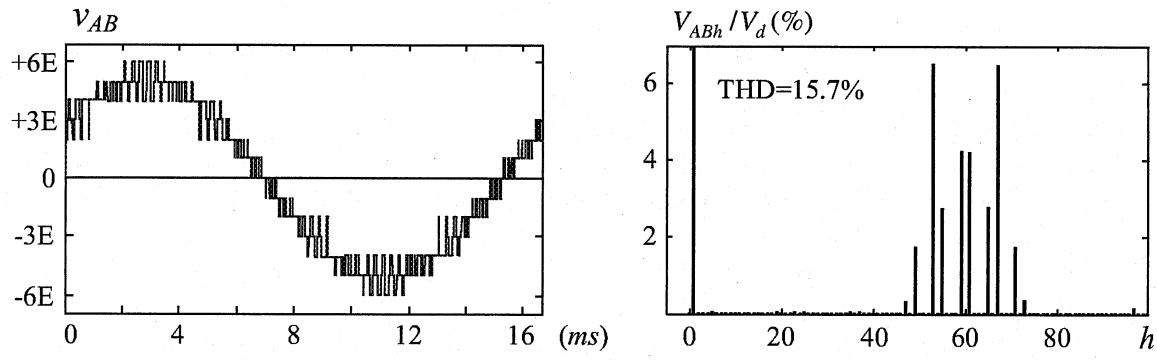
Table 3-9 Conduction angle of each switch for DMM scheme ($\hat{V}_r = 3(100\%)$, $f_r = 60Hz$, $T_s = 1/3600\sec$)

Phase A		Phase B		Phase C	
H_1	S_1=180	H_1	S_1=180	H_1	S_1=180
	S_2=180		S_2=180		S_2=180
	S_3=180.6		S_3=182.7		S_3=176.7
	S_4=179.4		S_4=177.3		S_4=183.3
H_2	S_1=180	H_2	S_1=180	H_2	S_1=180
	S_2=180		S_2=180		S_2=180
	S_3=179.5		S_3=179.9		S_3=180.6
	S_4=180.5		S_4=180.1		S_4=179.4
H_3	S_1=180	H_3	S_1=180	H_3	S_1=180
	S_2=180		S_2=180		S_2=180
	S_3=179.9		S_3=177.5		S_3=182.7
	S_4=180.1		S_4=182.5		S_4=177.3

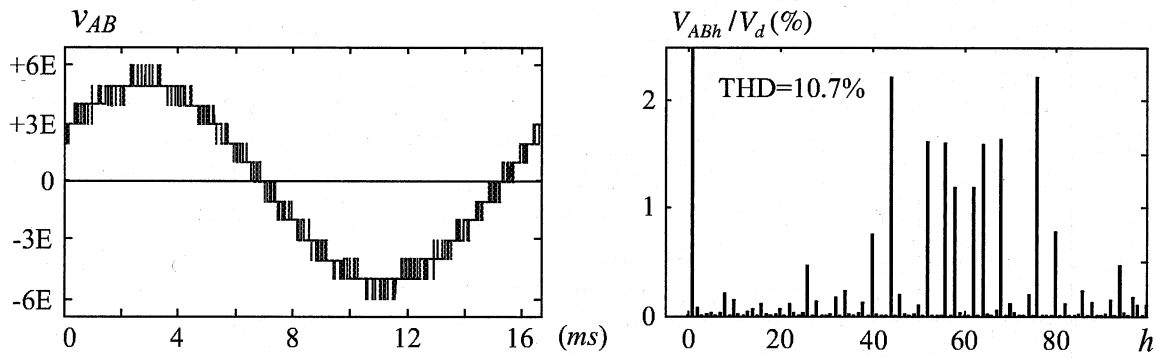
3.5 Comparison with Carrier Based Modulation Schemes

Figure 3-6 illustrates harmonic spectrum of v_{AB} among phase-shifted, IPD and DMM scheme under the same condition. Compare with conversional IPD PWM scheme, THD of line-to-line voltage v_{AB} for DMM scheme is close to IPD and much less than phase-shifted modulation scheme. For $\hat{V}_r = 3.0(100\%)$, THD of DMM has only 11.5%, which is very close to 10.7% in IPD and much lower than phase-shifted 15.6% under the same

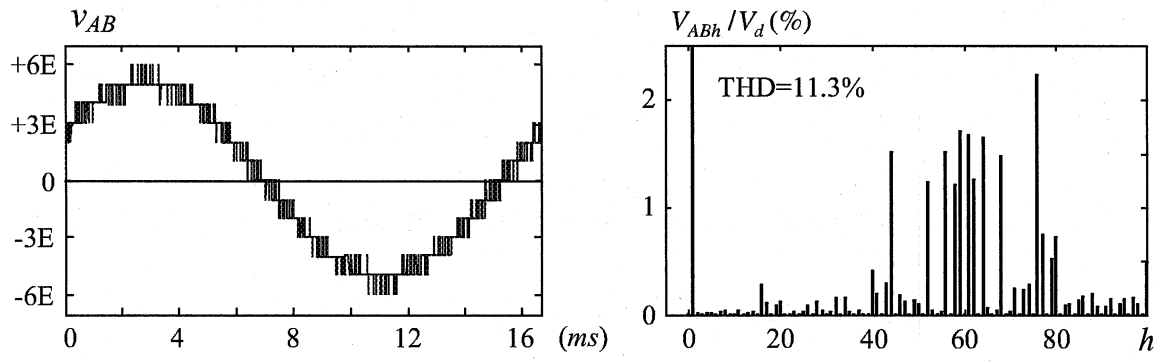
condition.



(a) Phase shifted



(b) IPD



(c) DMM

Figure 3-6 Waveform and harmonic spectrum of v_{AB} produced by carrier based modulation and proposed DMM schemes

($\hat{V}_r = 3.0(100\%)$, $f_r = 60Hz$ and $T_s = 1/3600\,\text{sec}$)

Fig. 3-7 illustrates the THD profile of the inverter line-to-line voltage v_{AB} generated by phase-shifted, IPD and DMM schemes for a seven-level CHB inverter, where m_a is the amplitude modulation index defined as the peak of modulating wave divided by the peak of the carrier wave v_c shown in Figure 3-1. The fundamental frequency of the inverter output voltage is 60Hz, and the switching frequency of switching devices is fixed to 600Hz for all three cases. It is interesting to note that the THD of the inverter output voltage v_{AB} produced by the DMM scheme is almost identical to that of IPD modulation, which is much lower than that produced by the phase-shifted modulation.

Figure 3-8 shows THD profile of inverter line-to-line voltage v_{AB} generated by DMM schemes for device switching frequency 240, 420, 600, 780 and 960 Hz. All curves are overlapped. It reflects THD of DMM scheme is as low as IPD in all frequency range.

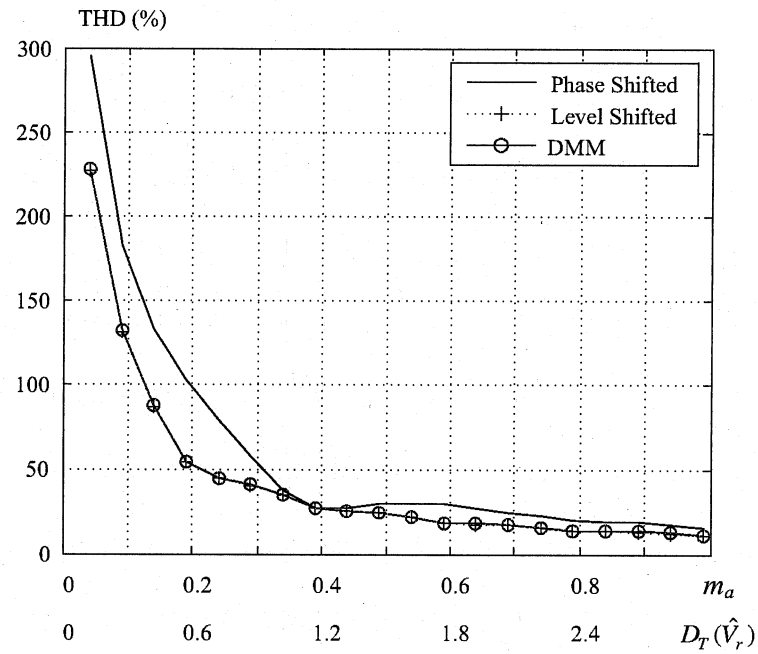


Figure 3-7 THD curves of the inverter line-to-line voltage v_{AB} generated by carrier based and DMM schemes.

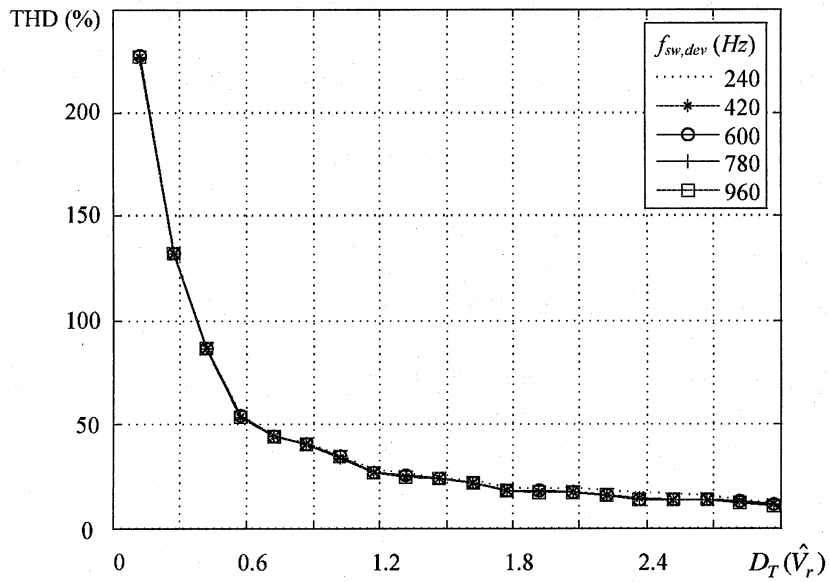


Figure 3-8 THD profile of inverter line-to-line voltage v_{AB} generated by DMM schemes with various device switching frequencies.

3.6 Summary

This chapter provides the detailed theory and algorithm of DMM scheme for CHB multilevel inverters. This scheme is very simple, flexible and easy to implement. To generate gate signals for all the active switches in the inverter, the scheme needs only to calculate a three-phase sine function once followed by a number of subtractions in each sampling period. In this chapter, the principle of the proposed modulation scheme is elaborated and its harmonic performance is analyzed. Comparisons are carried out between the DMM scheme and carrier based modulation schemes including phase-shifted and IPD modulations. It is demonstrated that the harmonic performance of the DMM scheme is on par with the best of carrier based modulation techniques. The proposed digital scheme can be employed for any CHB inverters with any voltage levels.

Chapter 4 Line Current THD Analysis of AC Drives

4.1 Introduction

Multilevel CHB inverter is one of the popular converter topologies used in high-power medium-voltage (MV) drives. It normally uses multipulse diode rectifiers as front-end converters. The main characteristic of multipulse diode rectifiers is to reduce the line current harmonic distortion. The essential prerequisite to reduce the line current THD is balanced loads on secondary windings of phase-shifting transformer.

This chapter focuses on line current THD analysis of AC drives. An AC drive is built by Matlab Simulink. System parameters are assumed for lab experiments. The line current THD of three modulation schemes is analyzed and compared.

4.2 System simulation

Figure 4-1 illustrates a seven-level CHB inverter-drive topology and parameters. The front-end converters for seven-level CHB inverter-fed drives are configured by three 18-pulse diode rectifiers, powered by phase-shifting transformer with nine secondary windings. Each secondary winding feeds a six-pulse diode rectifier. The dc output of the six-pulse rectifier is connected to a voltage source inverter.

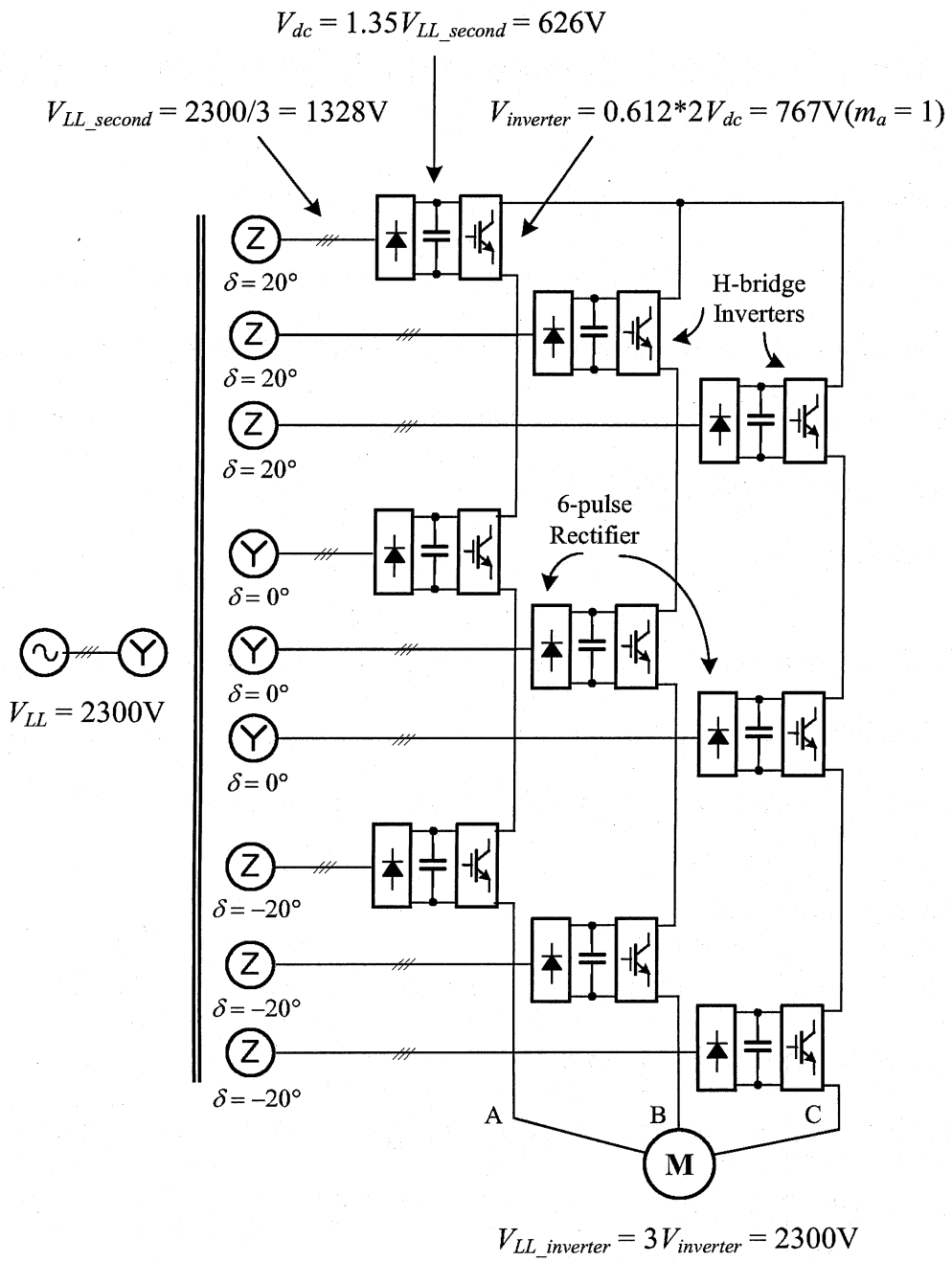


Figure 4-1 Seven-level CHB inverter-fed drives topology and parameters.

The main drawback of the six-pulse diode rectifier is that the line current contains harmonics such as 5^{th}, 7^{th}, 11^{th} and 13^{th}. If the power distribution among H-bridge power cells is not balanced, the low order harmonics existing in six-pulse diode rectifier will be appeared in the line current of seven-level CHB inverter-fed drives. If the power

distribution among H-bridge power cells is balanced, 5th, 7th, 11th and 13th harmonics will be cancelled by phase-shifted transformer. There is the method to see whether DMM scheme is balanced power consumption.

4.2 Line Current THD of AC Drives with Phase-Shifted Scheme

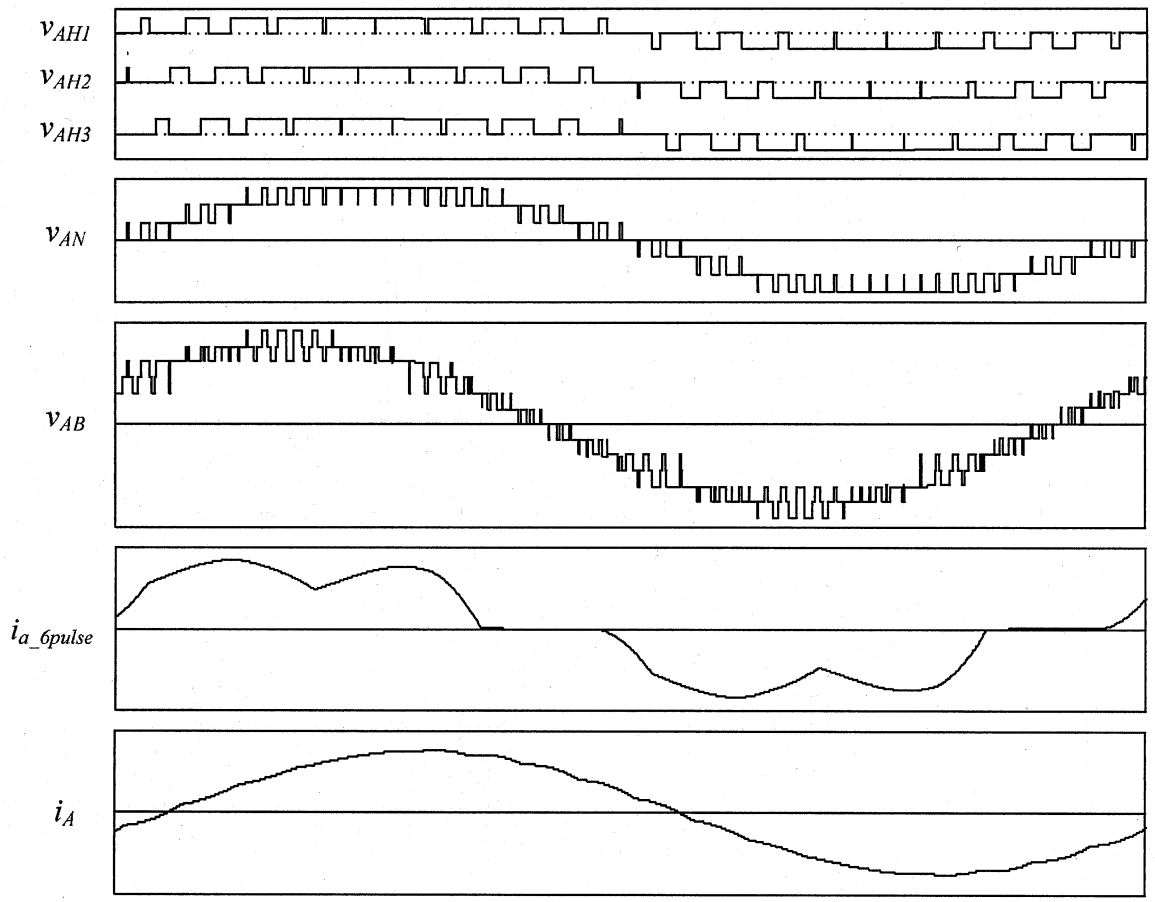
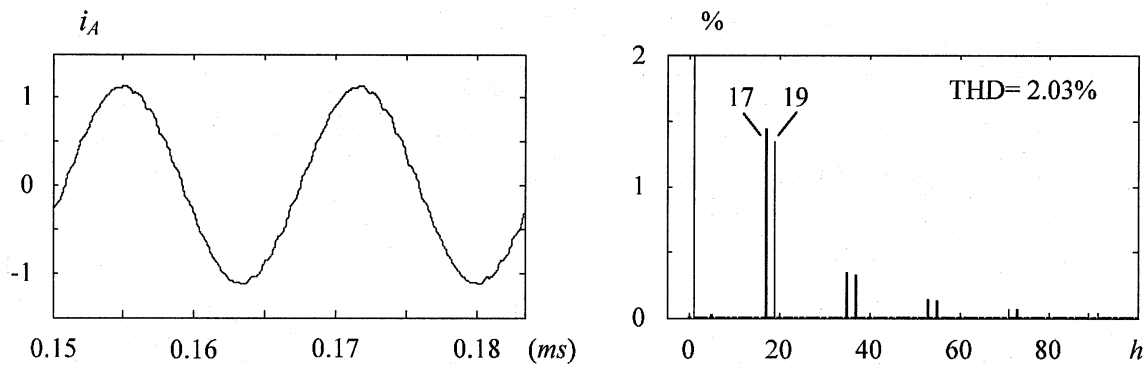


Figure 4-2 Harmonic spectrum of phase shifted for i_A ($m_a = 1$, $f_r = 60Hz$, $f_s = 600Hz$, and $f_{sw,dev} = 600Hz$).

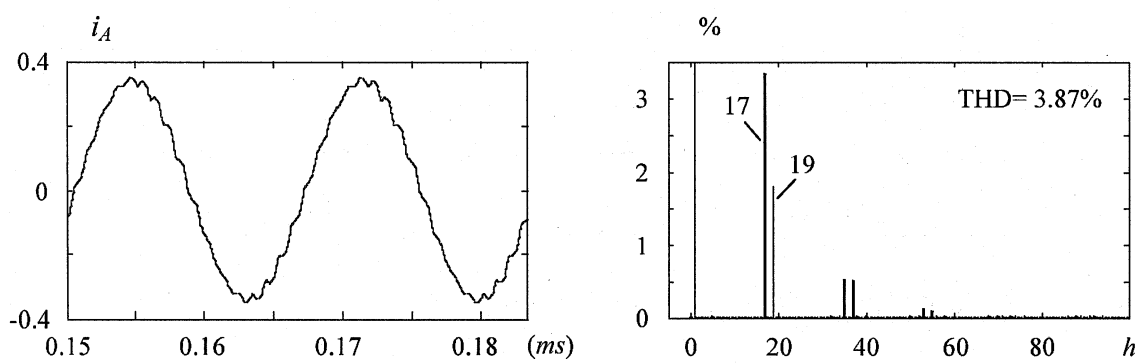
Figure 4-2 shows the phase-shifted simulated inverter output voltage and line current waveform under the condition of $m_a = 1$, $f_r = 60Hz$, $f_s = 600Hz$, and $f_{sw,dev} = 600Hz$. The waveform of v_{H1}, v_{H2} and v_{H3} are almost identical except for a small phase displacement

caused by the phase-shifted carriers.

The waveform of v_{AN} is composed of seven voltage levels with a peak value of $3E$. Since the IGBTs in the different H-bridges do not switch simultaneously, the magnitude of voltage step change during switching is only E. The line-to-line voltage v_{AB} has 13 voltage levels with an amplitude of $6E$. The waveform of i_A illustrates the line current waveform.



(a) $m_a = 1$, $f_m = 60Hz$, $f_{cr} = 600Hz$, and $f_{sw,dev} = 600Hz$



(b) $m_a = 0.5$, $f_m = 30Hz$, $f_{cr} = 600Hz$, and $f_{sw,dev} = 600Hz$

Figure 4-3 Harmonic spectrum of phase shifted for i_A.

Figure 4-3 shows the harmonic spectrum of line current for phase-shifted modulation

under the condition of 600 Hz device switching frequency with $m_a = 1$ and $m_a = 0.5$. The dominant harmonic is 17^{th} and 19^{th}, and the low order harmonic 5^{th} and 7^{th}, 11^{th} and 13^{th} generated by six pulse diode rectifier is cancelled by phase shifted transformer because phase-shifted modulation scheme is balanced power consumption. The line current THD is only 2.03% when $m_a = 1$, and increase to 3.87% when $m_a = 0.5$.

4.3 Line Current THD of AC Drives with IPD Scheme

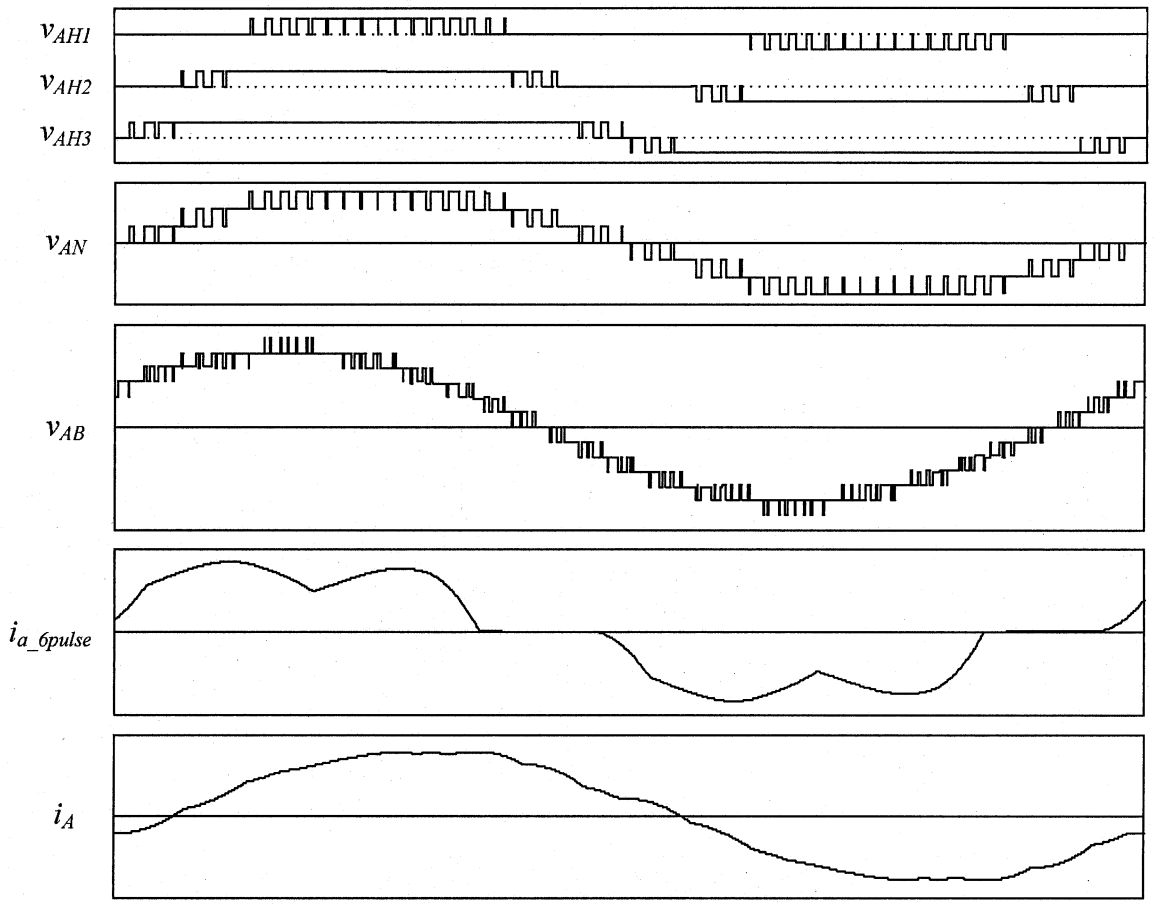
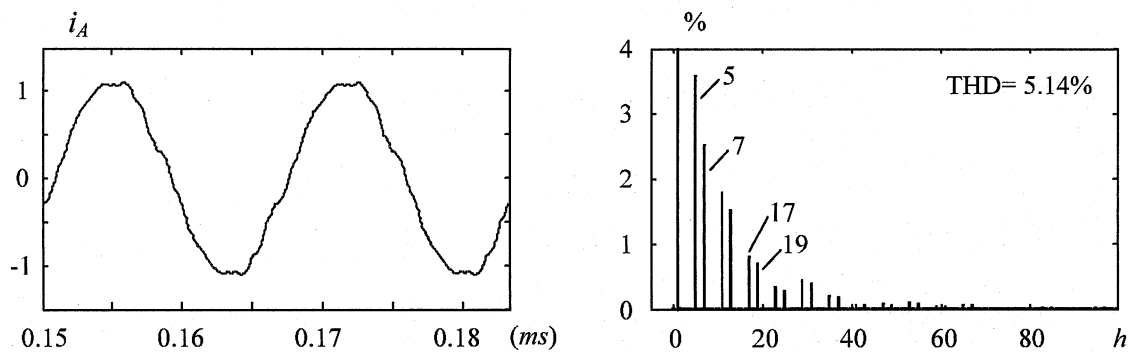


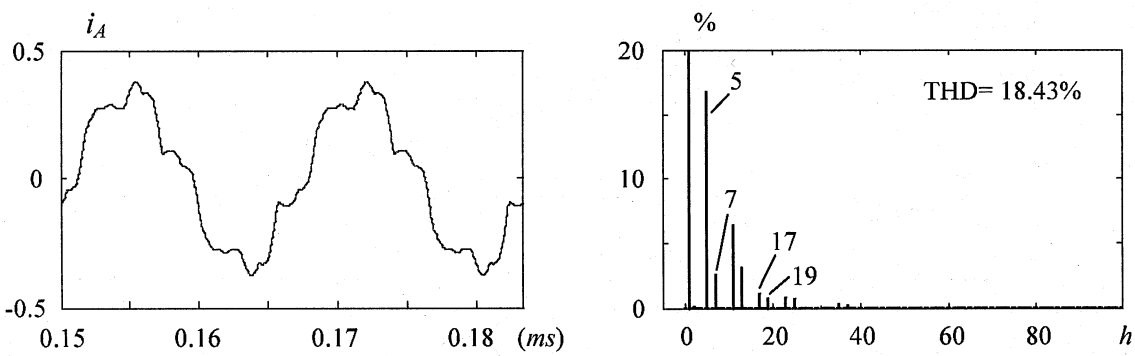
Figure 4-4 Harmonic spectrum of IPD for i_A ($m_a = 1$, $f_r = 60Hz$, $f_s = 3600Hz$, and $f_{sw,dev} = 600Hz$).

Figure 4-4 shows the IPD simulated output voltage and line current waveform for a

seven-level inverter under the condition of $m_a = 1$, $f_r = 60Hz$, $f_s = 3600Hz$, and $f_{sw,dev} = 600Hz$. The waveform of v_{H1}, v_{H2} and v_{H3} are all different. It shows the IGBTs in the different H-bridge cells operate at different switching frequencies with different conduction times. The waveform of i_A illustrates the line current waveform.



(a) $m_a = 1$, $f_r = 60Hz$, $f_s = 3600Hz$, and $f_{sw,dev} = 600Hz$



(b) $m_a = 0.5$, $f_r = 30Hz$, $f_s = 3600Hz$, and $f_{sw,dev} = 600Hz$

Figure 4-5 Harmonic spectrum of IPD for i_A.

Figure 4-5 shows the harmonic spectrum of line current for IPD modulation under the condition of 600 Hz device switching frequency with $m_a = 1$ and $m_a = 0.5$. The dominant harmonic are 5^{th} and 7^{th}, 11^{th} and 13^{th}, and the low order harmonic 5^{th} and 7^{th}, 11^{th} and

13^{th} generated by six pulse diode rectifier cannot be cancelled by phase shifted transformer because phase-shifted modulation scheme is unbalanced power consumption. The line current THD is remarkable increased to 5.14% when $m_a = 1$, and 18.43% when $m_a = 0.5$.

4.4 Line Current THD of AC Drives with DMM Scheme

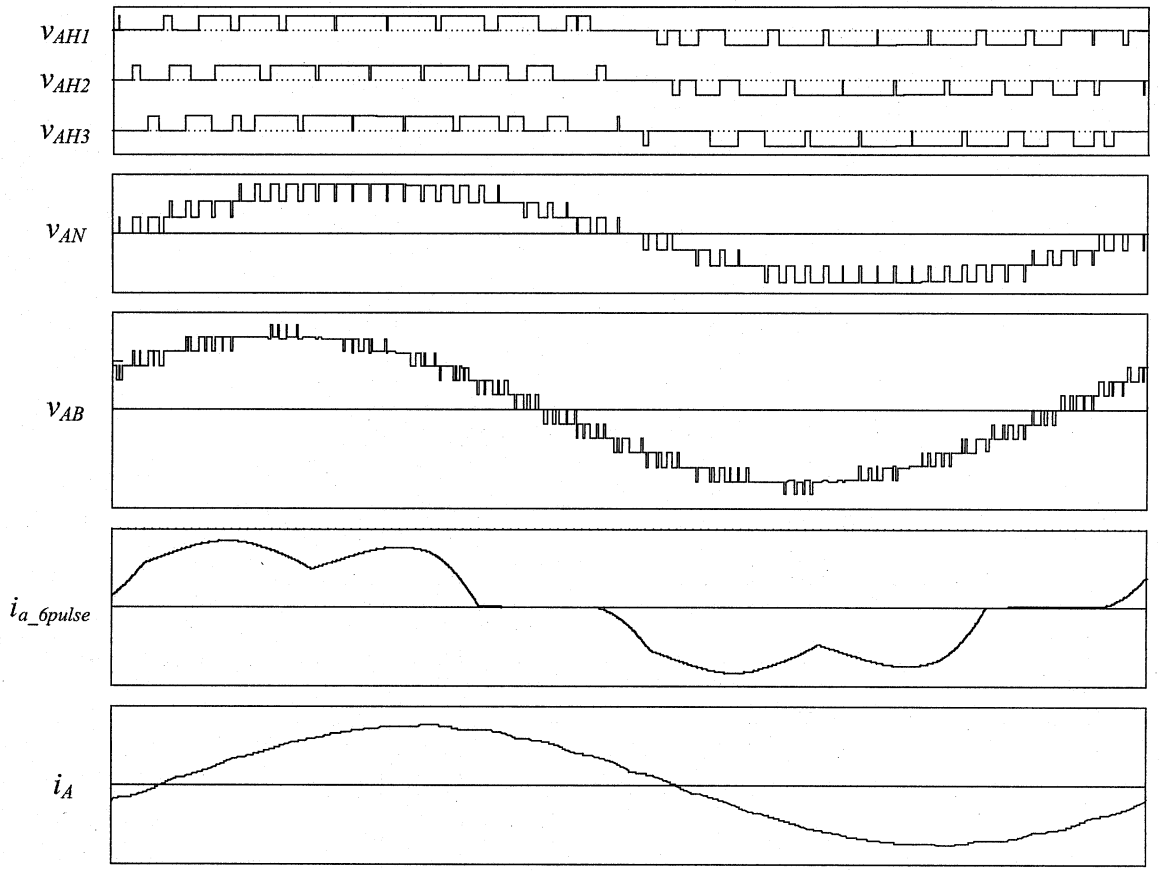
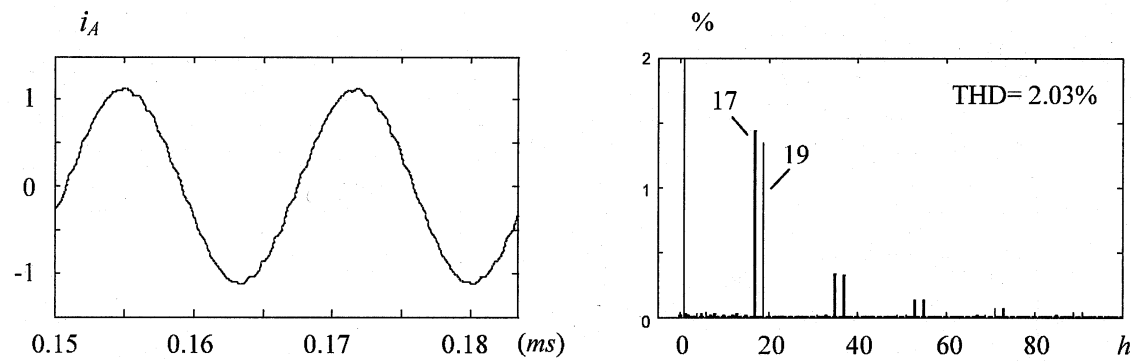


Figure 4-6 Harmonic spectrum of DMM for i_A ($m_a = 1$, $f_r = 60Hz$, $f_s = 3600Hz$, and $f_{sw,dev} = 600Hz$).

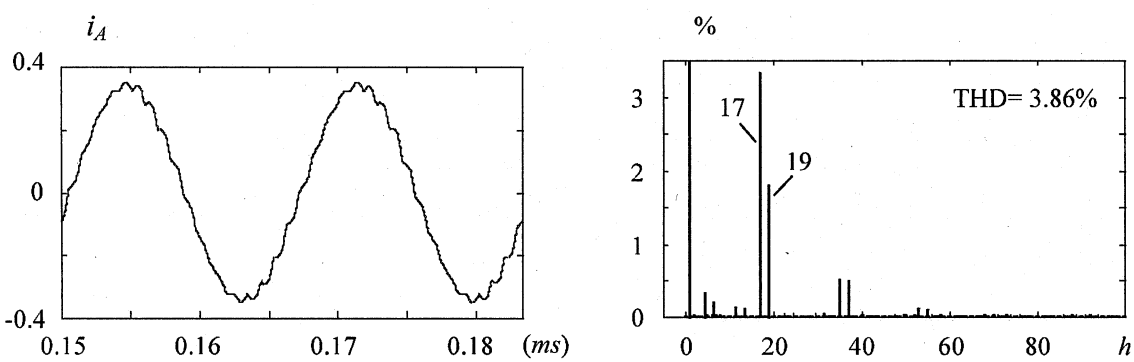
Figure 4-6 shows the DMM simulated inverter output voltage and line current waveform under the condition of $m_a = 1$, $f_r = 60Hz$, $f_s = 600Hz$, and $f_{sw,dev} = 600Hz$. The waveform of

v_{H1}, v_{H2} and v_{H3} are almost identical.

The waveform of v_{AN} is composed of seven voltage levels with a peak value of 3E. Since the IGBTs in the different H-bridges do not switch simultaneously, the magnitude of voltage step change during switching is only E. The line-to-line voltage v_{AB} has 13 voltage levels with an amplitude of 6E. The waveform of i_A illustrates the line current waveform.



(a) $D_T = 3$, $f_r = 60Hz$, $f_s = 3600Hz$, and $f_{sw,dev} = 600Hz$



(b) $D_T = 1.5$, $f_r = 30Hz$, $f_s = 3600Hz$, and $f_{sw,dev} = 600Hz$

Figure 4-7 Harmonic spectrum of DMM for i_A.

4.5 Line Current THD Comparison with IPD, Phased Shifted and DMM

Figures 4-3, 4-5 and 4-7 show line current THD profile for phase-shifted, IPD and DMM schemes, separately. Line current THD of phase shifted and DMM is substantially reduced from 10.30% to 3.35% under the condition of $m_a = 0.8$, $f_r = 60Hz$, $f_s = 3600Hz$, and $f_{sw,dev} = 600Hz$. The dominant harmonics in i_A for IPD are 5th and 7th, but for phase-shifted and DMM scheme are 17th and 19th. Line current THD profile for IPD includes low order 5th and 7th, 11th and 13th reflects unbalanced power consumption for each power cell. THD profile of phase-shifted is almost same as DMM scheme verify power consumption is balanced for both scheme.

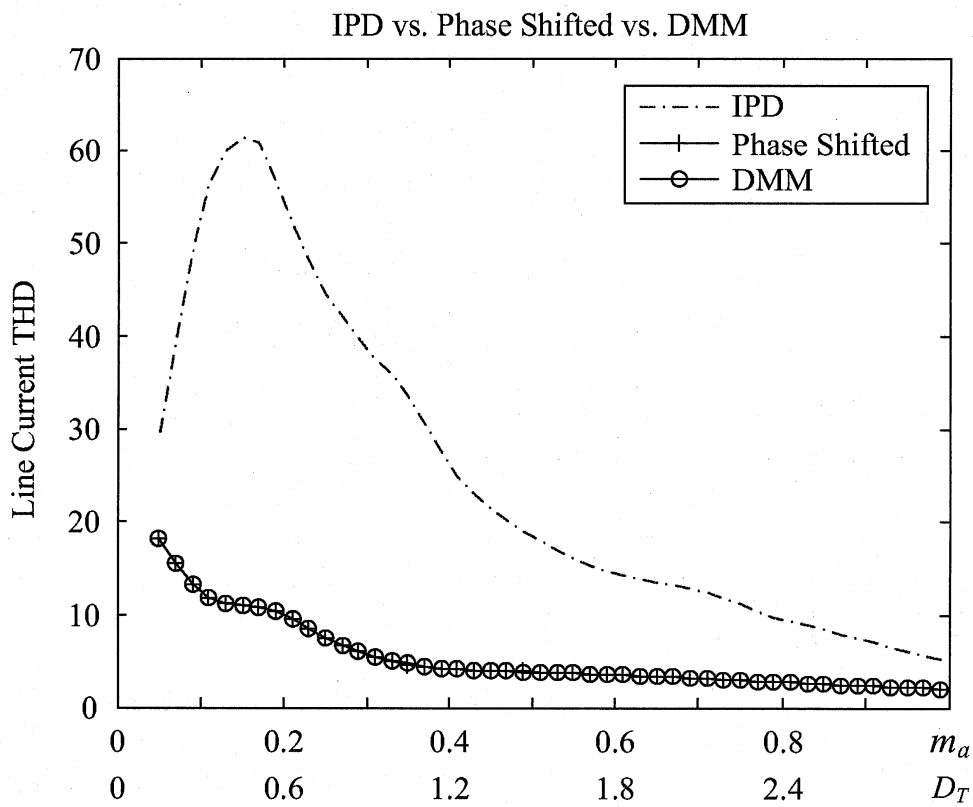


Figure 4-8 Line current THD of i_A for phase shifted, IPD and DMM.

4.6 Summary

This chapter provides line current THD comparison for phase-shifted, IPD and DMM modulation scheme. The simulation results illustrate DMM scheme eliminates low order harmonics such as 5^{th}, 7^{th}, 11^{th} and 13^{th} in line current THD profile. This feature reflects that the power distribution for power cell is balanced.

Chapter 5 Conclusions

5.1 Conclusions

This project presents a novel digital multilevel modulation (DMM) scheme for multilevel CHB inverters in high power AC drives. Conventional carrier based PWM schemes, including phase-shifted and in-phase disposition (IPD) modulation schemes, have their own merits and drawbacks. The IPD scheme possesses the advantage of best line-to-line voltage THD, but has the disadvantage of unbalanced power distribution for each power cell. On the other hand, phase-shifted PWM scheme has the merit of balanced power distribution for each power cell, but provide worse line-to-line voltage THD than IPD PWM scheme. DMM scheme offers a solution to obtain the advantages from both schemes and overcome disadvantages as well.

Compared with other types of modulation scheme for multilevel CHB inverters, DMM scheme has the following advantages: simple algorithm, superior harmonic profile, and balanced power distribution. The simulation results indicate that the new DMM schemes are on par with the best of carrier based modulation techniques for multilevel CHB inverters in high power AC drives.

The main contributions of this project are as follows:

1) **A new simple algorithm for sampling has been proposed.** This algorithm is very simple, flexible and easy to implement by digital processor like DSP. To generate gate signals for all the active switches in the inverter, the scheme needs only to calculate a

three-phase sine function once followed by a number of subtractions in each sampling period. This algorithm of DMM scheme is much easier than that of carrier based modulation schemes, which need to calculate the intersection between the modulation sinusoid wave and the triangular carrier. This algorithm is general and can be employed for any CHB inverters with any voltage levels.

2) **A novel scheme algorithm for multilevel CHB inverters with low THD on inverter side has been developed.** The PWM voltage generated by DMM scheme contains minimal harmonic distortion, THD of DMM scheme is as low as that produced by IPD modulation. It is demonstrated that the harmonic performance of the DMM scheme is on par with the best of carrier based modulation techniques.

3) **A novel balanced power distribution modulation scheme for multilevel CHB inverters in high power AC drives has been developed.** The DMM scheme produces THD as low as IPD modulation in all m_a range and all device switching frequencies. The balanced power distribution feature eliminates low order harmonic and reduces line current THD. DMM scheme is most promising modulation scheme to replace the current phase-shifted modulation scheme in industry.

4) **Effective simulation model for verifying DMM scheme has been established.** This model is for seven-level CHB inverter. However, it can be employed for any CHB inverters with any voltage levels with minor modification.

5.2 Future Works

- The proposed modulation scheme for multilevel CHB inverters is achieved by Matlab

simulation. Experimental verification of DMM scheme is recommended.

- It is also suggested to investigate the possibility to use DMM scheme in other topologies.

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Appendix I

Rectifier Parameter

Rated Supply Voltage:	2300V (rms, line-to-line)
Rated Output Power:	1MVA (dc)
dc capacitor:	C_d=5000μF
Total Leakage Inductance:	0.05pu (Transformer primary and secondary leakages)
Line inductance:	0.05pu (Between the transformer and supply)
Diodes:	Ideal (no power losses, no forward voltage drop)

$$V_{B\_Line} = \frac{V_{LL}}{\sqrt{3}} = \frac{2300}{\sqrt{3}} = 1328V$$

$$I_{B\_Line} = \frac{S_R}{3V_B} = \frac{1\times10^6}{3\times1328} = 251A$$

$$Z_{B\_Line} = \frac{V_B}{I_B} = \frac{1328}{251} = 5.3\Omega$$

$$L_{B\_Line} = \frac{Z_B}{\omega_B} = \frac{5.3}{2\pi f} = \frac{5.3}{2\times\pi\times60} = 14mH$$

$$L_{s\_Line} = 0.05L_B = 0.7\text{m}H$$

$$L_{lk\_Line} = 0.05L_B = 0.7\text{m}H$$

$$C_{B\_Line} = \frac{1}{\omega_B Z_B} = \frac{1}{2\pi f Z_B} = \frac{1}{2\pi\times60\times5.3} = 500\mu F$$

$$V_{dc} = 3E = 3*1.35*V_{LL} = 3*1.35*(1392/3) = 1879V$$

$$V_{AB1,\max} = 1.224V_{dc} = 1.224*1879 = 2300V \qquad \text{for } m_a = 1$$

Inverter Parameter

Inverter Configuration:	Seven-level cascaded H-bridge inverter
Rated Inverter Output Voltage:	2300V (rms fundamental line-to-line voltage)
Rated Inverter Output Power:	1MVA (three phase)
Rated Inverter Output Frequrency:	60Hz
Inverter load:	Three-phase balanced RL load with a lagging power factor of 0.9 at the rated frequency of 60Hz.

$$V_{inverter} = \frac{V_{LL\_inverter}}{\sqrt{3}} = \frac{3800}{\sqrt{3}} = 2194V$$

$$I_{inverter} = \frac{S_R}{3V_{inverter}} = \frac{1\times10^6}{3\times2194} = 152A$$

$$Z_{inverter} = \frac{V_{inverter}}{I_{inverter}} = \frac{2194}{152} = 14.4\Omega$$

$$Z_{inverter} = R + j\omega L$$

$$\omega = 2\pi f$$

$$R = Z_{inverter}\cos\varphi = 14.4\times0.9 = 13\Omega$$

$$L_{inverter} = \frac{Z_{inverter}}{\omega_{inverter}} = \frac{14.4}{2\pi f} = \frac{14.4}{2\times\pi\times60} = 38.2mH$$

$$\cos\varphi = 0.9$$

$$\varphi = \cos^{-1}(0.9) = 25.84°$$

$$L = \frac{Z_{inverter}\sin\varphi}{\omega} = \frac{Z_{inverter}\sin\varphi}{2\pi f} = \frac{14.4\times\sin 25.84}{2\times3.14\times60} = 17mH$$

Inverter Parameter

Inverter Configuration:	Seven-level cascaded H-bridge inverter
Rated Inverter Output Voltage:	2300V (rms fundamental line-to-line voltage)
Rated Inverter Output Power:	1MVA (three phase)
Rated Inverter Output Frequency:	60Hz
Inverter load:	Three-phase balanced RL load with a lagging power factor of 0.9 at the rated frequency of 60Hz.

$$V_{inverter} = \frac{V_{LL\_inverter}}{\sqrt{3}} = \frac{2300}{\sqrt{3}} = 1328V$$

$$I_{inverter} = \frac{S_R}{3V_{inverter}} = \frac{1\times10^6}{3\times1328} = 251A$$

$$Z_{inverter} = \frac{V_{inverter}}{I_{inverter}} = \frac{1328}{251} = 5.3\Omega$$

$$Z_{inverter} = R + j\omega L$$

$$\omega = 2\pi f$$

$$R = Z_{inverter}\cos\varphi = 5.3\times0.9 = 4.8\Omega$$

$$L_{inverter} = \frac{Z_{inverter}}{\omega_{inverter}} = \frac{5.3}{2\pi f} = \frac{5.3}{2\times\pi\times60} = 14mH$$

$$\cos\varphi = 0.9$$

$$\varphi = \cos^{-1}(0.9) = 25.84°$$

$$L = \frac{Z_{inverter}\sin\varphi}{\omega} = \frac{Z_{inverter}\sin\varphi}{2\pi f} = \frac{5.3\times\sin 25.84}{2\times3.14\times60} = 6.1mH$$

BL-10-9