MODELLING, SIMULATION, CONTROL, AND ENHANCED TOPOLOGIES FOR THE MODULAR MULTILEVEL CONVERTER FOR HIGH-VOLTAGE DC (HVDC) APPLICATIONS

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Modelling, Simulation, Control, and Enhanced Topologies for the Modular Multilevel Converter for High-Voltage DC (HVDC) Applications

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Doctor of Philosophy

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Abstract

This thesis is focused on the modular multilevel converter (MMC) for High-Voltage DC (HVDC) systems. It is an attempt to address the issues associated with the modelling, simulation, control, efficiency, and fault-handling capability of the MMC. Thus, to address the modelling of the MMC, a new and more accurate steady-state harmonic model is proposed. The proposed harmonic model is capable of predicting the amplitude of the harmonic components of the MMC arm voltages, submodule capacitor voltages, and arm currents. Further, based on the proposed harmonic model, a capacitor sizing method is proposed to determine the capacitance of the submodule capacitor for a desired level of voltage variation, without a need for numerical algorithms or graphs used by the existing methods. In addition, the proposed capacitor sizing method can accurately determine the required capacitance even if circulating currents are injected to mitigate dc voltage fluctuations. The thesis also proposes a simple equivalent-circuit-based simulation model for MMC-based HVDC systems, which assumes ideal submodule switches to speed up the simulation, but is nonetheless capable of capturing the transients as well as harmonic components of the voltages and currents. Further, the thesis proposes a simple compensation strategy that calculates the magnitude of the second harmonic component of an arm voltage, and uses the calculated value as a feedforward signal to cancel the circulating current of the corresponding MMC leg. The proposed feedforward compensation strategy, if combined with a closed-loop circulating current suppression strategy, greatly mitigates the possibility of control saturation and, also, results in better damped closed-loop dynamics. Finally, the thesis proposes two new MMC topologies for enhanced efficiency and dc-side fault handling capability. In the first proposed topology, that is the *lattice modular multilevel converter* (LMMC), the entire MMC arm is modified to accommodate *networks* that allow shortcuts between the arm capacitors, thus, reducing conduction power losses of the converter. In the second topology proposed, however, only the submodule is modified. In the proposed submodule topology, referred to as *lattice submodule* (LSM), the conduction power losses are decreased, as it is the case for the LMMC, with the difference that the voltage stress in the switches are also reduced.

Keywords: Control, lattice modular multilevel converter, lattice submodule, modelling, modular multilevel converter, simulation model.

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List of Abbreviations

HVDC	High-voltage direct current
VSC	Voltage-sourced converter
LCC	Line-commutated converter
MMC	Modular multilevel converter
LMMC	Lattice modular multilevel converter
LSM	Lattice submodule
HBSM	Half-bridge submodule
FBSM	Full-bridge submodule
CDSM	Clamp-double submodule
SEC	Simplified equivalent-circuit

List of Symbols

v_{dc}	DC voltage
v_g	Grid voltage
v_{ga}	Grid voltage phase *a*
v_{gb}	Grid voltage phase *b*
v_{gc}	Grid voltage phase *c*
v_{gLL}	Grid line-to-line voltage
i_t	Ac-side terminal current
$\widehat{I}$	Ac-side terminal current peak
φ	Ac-side terminal current angle
i_{ta}	Ac-side terminal current of phase *a*
i_{tb}	Ac-side terminal current of phase *b*
i_{tc}	Ac-side terminal current of phase *c*
i_{td}	Ac-side terminal current *d* component in *dq*-frame
i_{tq}	Ac-side terminal current *q* component in *dq*-frame
i_r	Current in the arm r ($r = 1$ for the upper arm and $r = 2$ for the lower arm)
i_{cm}	Circulating current
i'_{cm}	Circulating current dependent on itself
i_{cma}	Circulating current phase *a*
i_{cmb}	Circulating current phase *b*
i_{cmc}	Circulating current phase *c*
v_{Cj}	Submodule capacitor voltage in capacitor j
$\overline{v}_C$	Submodule capacitor average voltage (MMC resolution)

List of Symbols

v_{Sn}	Ac voltage of submodule n
v_1	Upper arm voltage
v_2	Lower arm voltage
e_t	Inner voltage
M	Number of capacitor per arm
N	Number of submodules per arm
n_1	Number of capacitors inserted in the upper arm
n_2	Number of capacitors inserted in the lower arm
L	Arm inductance
C	Submodule capacitance
R	Arm resistance
R_t	Terminal resistance
L_t	Terminal inductance
L'	Equivalent inductance from the ac side
R'	Equivalent resistance from the ac side
m	Modulating function
$\widehat{m}$	Modulation index
θ	Modulating function angle
a	MMC assymetry
T_s	MMC sample time
f_g	Grid frequency
ω	Grid angular frequency

List of Symbols

C_{eqr}	Equivalent capacitance of arm r
v_{ir}	Integrated voltage in arm r
$v_1^{i_t}$	upper arm voltage created by i_t
$v_1^{i_{cm}}$	upper arm voltage created by i_{cm}
I_{cm}^0	Circulating current dc component
$(i_{cm})_2$	Circulating current second harmonic
$(i_{cm})_4$	Circulating current fourth harmonic
$\widehat{I_{cm}}$	Circulating current second harmonic peak
$\widehat{I_{cm4}}$	Circulating current fourth harmonic peak
φ_2	Circulating current angle
P	Active power exchanged with the ac grid
Q	Reactive power exchanged with the ac grid
P_{loss}	Power loss in the MMC arm
i_{trms}	Ac-side terminal current rms value
i_{cmrms}	Circulating current rms value
$\widehat{e_t}$	Inner voltage peak
δ	Inner voltage angle
$(v_C)_1$	Submodule capacitor voltage fundamental
$(v_C)_2$	Submodule capacitor voltage second harmonic
$(v_C)_3$	Submodule capacitor voltage third harmonic

List of Symbols

$\widetilde{v}_{Cn}$	Submodule capacitor approximate voltage, negative half-cycle
$\widetilde{v}_{Cp}$	Submodule capacitor approximate voltage, positive half-cycle
$(\widetilde{v}_C)_{1n}$	Fundamental of the submodule capacitor approximate voltage, negative half-cycle
$(\widetilde{v}_C)_{2n}$	Second harmonic of the submodule capacitor approximate voltage, negative half-cycle
$(\widetilde{v}_C)_{3n}$	Third harmonic of the submodule capacitor approximate voltage, negative half-cycle
$(\widetilde{v}_C)_{1p}$	Fundamental of the submodule capacitor approximate voltage, positive half-cycle
$(\widetilde{v}_C)_{2p}$	Second harmonic of the submodule capacitor approximate voltage, positive half-cycle
$(\widetilde{v}_C)_{3p}$	Third harmonic of the submodule capacitor approximate voltage, positive half-cycle
Δv_C	Submodule capacitor voltage variation
$\Delta\widetilde{v}_C$	Submodule capacitor approximate voltage variation
$(\Delta\widetilde{v}_C)_p$	Submodule capacitor approximate voltage variation, positive half-cycle
$(\Delta\widetilde{v}_C)_n$	Submodule capacitor approximate voltage variation, negative half-cycle

List of Symbols

t_p	Instant where $\widetilde{v}_{Cp}$ reaches its peak
t_n	Instant where $\widetilde{v}_{Cn}$ reaches its peak
r_{n1}	Angle in radians for the peak of the fundamental of the submodule capacitor voltage, negative half-cycle
r_{n2}	Angle in radians for the peak of the second harmonic of the submodule capacitor voltage, negative half-cycle
r_{n3}	Angle in radians for the peak of the third harmonic of the submodule capacitor voltage, negative half-cycle
N_{ss}	Number of series connected switches in an arm
$\overline{N}_{ss}$	Average number of series connected switches in an arm

Chapter 1

Introduction

1.1 Background and Motivation

A high-voltage dc (HVDC) system for bulk transmission of electric energy over large distances is more efficient and economical than an ac counterpart, especially if undersea cables are involved, although HVDC transmission systems are on occasions the only choice, e.g., for interconnecting power systems of different frequencies, or for other strategic purposes. Therefore, for most applications choice of using whether a high-voltage ac (HVAC) transmission system or a HVDC transmission system depends primarily on the distance of the transmission, as illustrated in Fig. 1.1. As the figure shows, the initial cost of an HVDC system is higher than that of an HVAC counterpart. However, the overall cost of the HVAC system rises more rapidly with the distance of transmission, mainly due to the cost of the transmission lines. Therefore, there is a distance, marked on Figure 1.1 as the critical distance, at which HVDC transmission becomes more attractive economically. For underground transmission, this critical distance is in the range 500 km to 800 km [1], whereas it is in the range 700 km to 900 km for overhead transmission [2].

The first HVDC transmission system was commissioned in 1954 and connected Gotland in the island of Ygne, Sweden, with the main land, as Figure 1.2 illustrates. The Gotland HVDC system was designed to process 20 MW at a dc voltage of 100 kV, through 96 km of undersea cables. At that time, mercury-arc valves were used for the rectifier and inverter terminals of the HVDC system. In 1970, the Gotland HVDC system became the first to use the thyristor as the electronic switch for its rectifier and inverter stations; this allowed the rated transmitted power to be raised to 30 MW at 150 kV [4], [5]. Since the Gotland project, the thyristor has served as the switch of choice in HVDC systems. Thyristor-based HVDC systems, using the so-called line-commutated converters (LCCs), can process up to 7600 MW of power, at voltages up to 800 kV, and over distances up to 2090 km, as it is the case for the Jinping-Sunan ultra high voltage direct current (UHVDC) system in China, commissioned in 2013 [6].

The thyristor can only be turned on at will; it turns off only if its current crosses zero. Therefore, the LCC must be interfaced with an adequately stiff ac grid. This, in turn, means that the LCC cannot be used to energize passive islands, not does it offer blackstart capability. In addition, it pulsates with three times the ac grid frequency, requiring costly ac- and dc-side filters. Further, it demands a substantial amount of reactive power, again, requiring a stiff ac

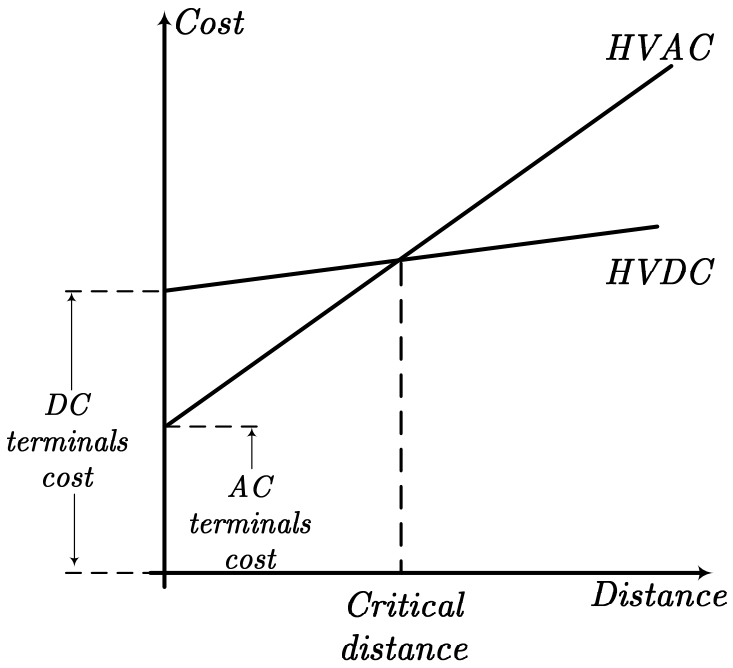

Figure 1.1: Critical distance when HVDC transmission becomes more cost effective in relation to HVAC.

Figure 1.2: Illustration of the location of the first HVDC transmission system, Gotland, Sweden [3].

grid or compensation. Furthermore, due to its unidirectional dc current, it requires reversal of its dc voltage polarity if the power flow is to be reversed [7]-[9]. For these reasons, the LCC is being replaced by the voltage-sourced converters (VSCs) which use electronic switches with gate turn-off capabilities such as the insolated-gate bipolar transistor (IGBT) [10]. The VSC can pulsate at much higher frequencies and, therefore, requires smaller filters. Moreover, it can operate at any power factor and with weak ac grids, it offers blackstart capability, and it allows for a bidirectional power flow while the polarity of its dc voltage remains unchanged [10]. The first VSC-based HVDC system was installed in Sweden (again in Gotland), in 1997 [11], to process 50 MW at a voltage of 80 kV, through 70 km of underground cables; Fig. 1.3

illustrates a schematic diagram of the transmission system.

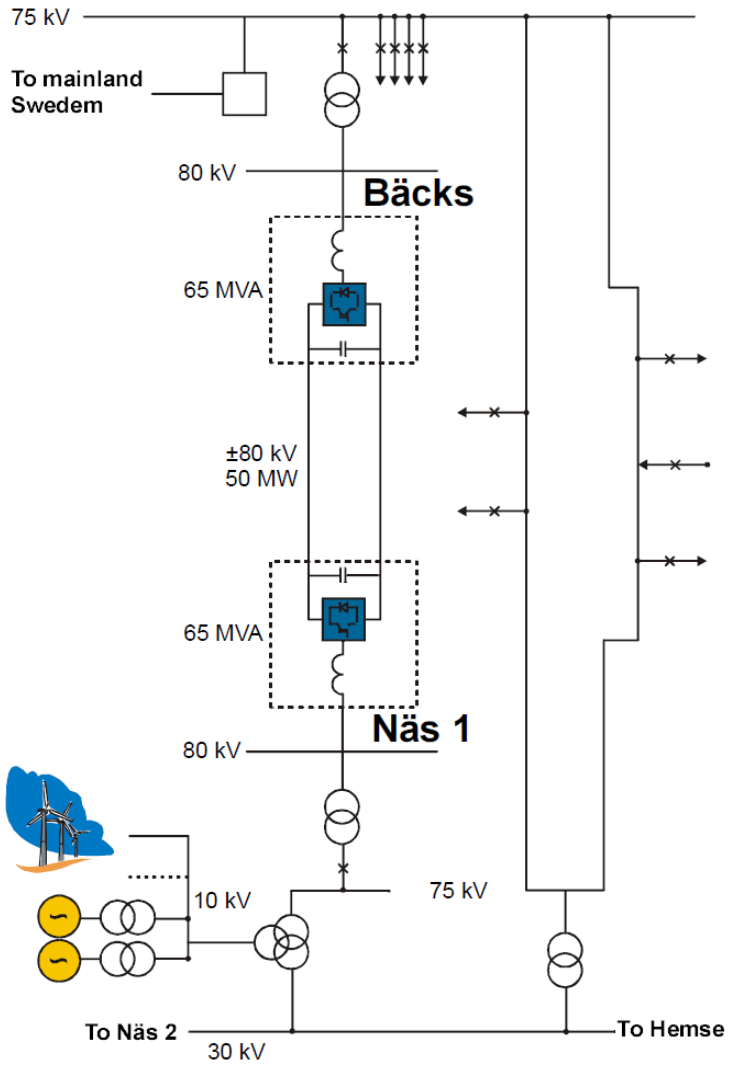

Figure 1.3: Schematic diagram of the VSC-based HVDC transmission system in Gotland, Sweden [11].

In the recent past, the interest in VSC-based HVDC systems has become stronger due to the notion of multi-terminal direct current (MTDC) grids [5]. The idea is to enable mass integration of renewable energy resources scattered over large geographical spans [12], and to offer various energy trade scenarios in a multi-country/multi-continent power system. This would require the co-existence of overhead, underground, and undersea high-voltage transmission lines. However, the conventional technologies for the VSC are limited in terms of voltage and power handling capabilities, relative to the LCC, and, consequently, are deemed unsuitable for MTDCs. Therefore, a new breed of the VSC, known as the modular multilevel converter (MMC) [13], is being seriously considered for HVDC systems. The MMC permits the dc voltage to be divided over multiple modules hosting switches and capacitors. Therefore, the voltage rating of each module can be small, thus allowing for the use of fully-controllable semiconductor switches such as the IGBT [14]-[16]. Further, the modular nature of the MMC enhances its fault tolerance and reliability.

Figure 1.4 shows a conceptual schematic diagram for one leg of the MMC. The MMC basic mechanism is to connect (insert) or disconnect (bypass) voltage sources (denoted by v_{Cj} (j = 1, 2, ..., M in the upper arm, and $j = M + 1$, $M + 2$, ..., $2M$ in the lower arm) in series in an arm, through fully controllable switches, represented in Fig. 1.4 as ideal switches. The voltage sources are inserted in the MMC arm when the switches are in the position *A*, and are bypassed when the switches are in the position *B*. Further, the insertion of voltage sources in both MMC arms generates an *ac-side terminal voltage*, v_t, that controls the power exchange with the ac grid. Each voltage source inserted in an arm, together with another voltage source with equal average magnitude bypassed in the opposite arm, creates a voltage step in the ac-side terminal voltage. If the number of steps is large enough, the ac-side terminal voltage features a very low harmonic distortion, even without the use of filters. As an example, Fig. 1.5 shows the ac-side terminal voltage and its fundamental component of an MMC with 50 voltage sources per arm.

The voltage sources are arranged in "cells", referred to as *submodules*. Each submodule is formed by one or more voltage sources, together with a number of semiconductor switches, represented in Fig. 1.4 by ideal switches. The voltage sources in the MMC leg have the same voltage, regulated to be $1/M$ times the dc-side voltage, v_{dc}, where M is the number of voltage sources in an arm. Moreover, the submodules are arranged in such a way that the voltage across the switches has an average value equal to 0.5, 1, or 2 times the source voltage, depending on the topology of the submodules. In practice, a capacitor plays the role of a voltage source. Therefore, the control of the MMC must regulate the voltage of the capacitors. A detailed description of the MMC and its modelling, is presented in Chapter 2. Finally, the different topologies used for the submodules are discussed in Section 1.3.4, and further in Chapters 5 and 6.

Four projects are cited here as examples of MMC-based HVDC systems: the Transbay Project, the Inelfe Project, the Ultranet Project, and the Nemo Project. The Transbay transmission system connects Pittsburgh, CA to San Francisco, CA, through 88-km undersea cables and can transmit 400 MW at a voltage of ± 220 kV; its MMC has more than 200 SMs per arm in each terminal [17]. Figure 1.6 illustrates the Transbay marine HVDC transmission system. The Inelfe transmission system connects Baixas in France to Santa Llogaia in Spain, through 65 km long underground cables. The system can process 2000 MW through two subsystems, each rated 1000 $MW/\pm 320$ kV. Each station employs a three-phase MMC with 400 SMs per arm [18]-[22]. Figure 1.7 illustrates the location of the Inelfe HVDC transmission system. The Nemo transmission system, scheduled to be commissioned in 2019, will transmit 1000 MW at a voltage of ± 400 kV, through undersea cables [23]. Figure 1.8 illustrates the Nemo transmission system. The fourth example is the Ultranet transmission system, which is still in the planning phase. The Ultranet transmission system is expected to process 2000 MW at a transmission voltage of ± 380 kV, through overhead lines [25]. Transmission of energy through overhead lines, requires a submodule technology that is robust to dc-side faults that strike overhead lines. Therefore, in contrast to the three aforementioned projects, the full-bridge submodule (FBSM) is considered for the Ultranet system. Fig. 1.9 shows the future site of the Ultranet transmission system.

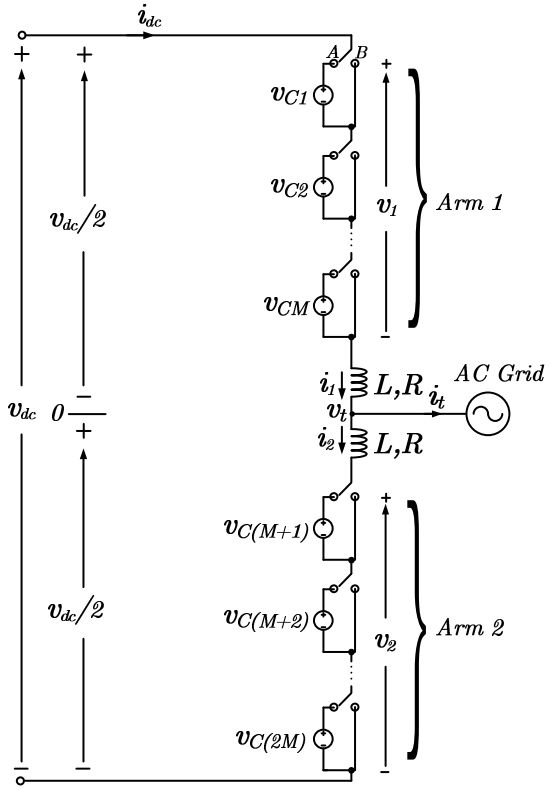

Figure 1.4: Conceptual schematic diagram for one leg of an MMC.

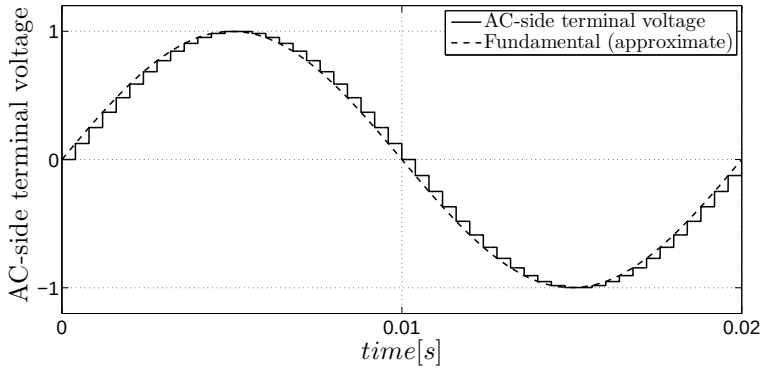

Figure 1.5: AC-side terminal voltage and its fundamental component for an MMC with 50 voltage sources per arm.

Figure 1.6: Transbay HVDC transmission system, connecting Pittsburgh, CA to San Francisco, CA [17].

Figure 1.7: Location of the Inelfe HVDC transmission system, connecting Sta Llogaia, Spain to Baixas, France [21].

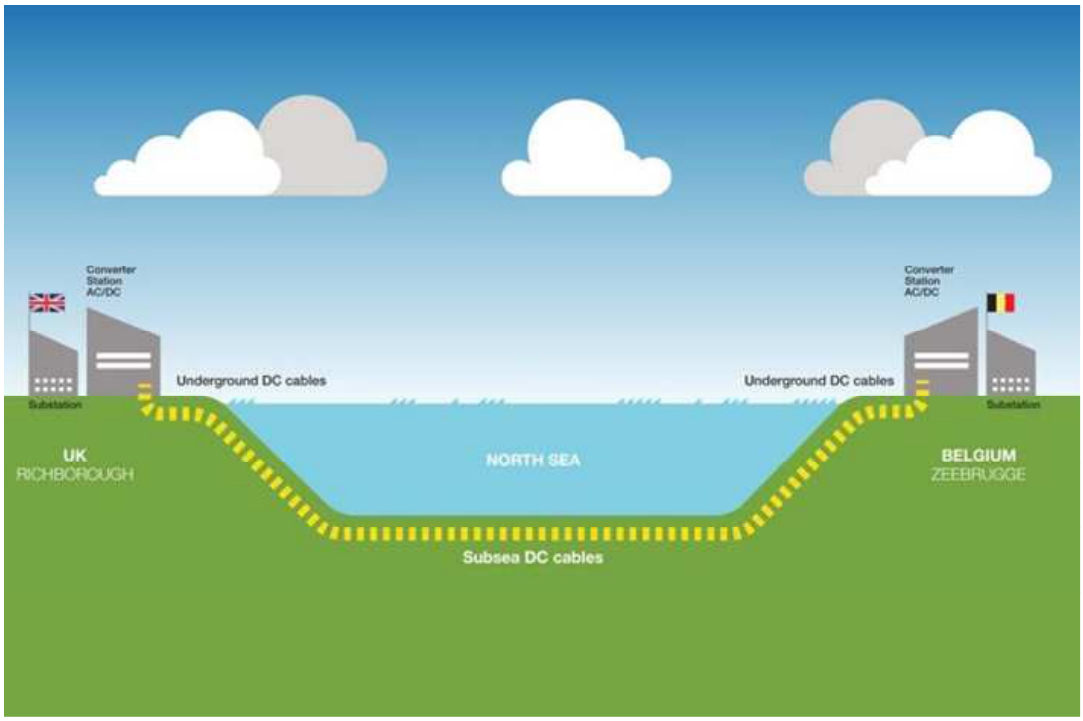

Figure 1.8: Illustration of the Nemo HVDC transmission system, connecting Richborough, UK to Zeebrugge, Belgium [24].

1.2 Statement of Problem and Thesis Objectives

The MMC is a promising technology, but it is still in its infancy. Therefore, there are multiple issues associated with its component sizing, effective control, efficient simulation, and fault handling capability. Thus, this thesis is focused on the development of analytical and simulation models, effective control strategies, and enhanced topologies, for the MMC. The more specific objectives of this thesis are described below.

1. To develop an adequately general, yet, accurate model for the purpose of component sizing and controller design;

2. To develop a simplified and easy-to-implement simulation model for the MMC;

3. To develop a control strategy to efficiently suppress the circulating current in the MMC; and

4. To propose topologies for the MMC that offer higher efficiencies and more economical dc-side fault handling capabilities.

Figure 1.9: Future site of the Ultranet HVDC transmission system, connecting Osterath to Philippsburg, Germany [25].

1.3 Literature Survey Pertinent to the Thesis Objectives

1.3.1 Modelling of the MMC and component sizing

The MMC modelling represents a very important step for understanding the steady-state and the dynamic behavior in different situations. Also, the correct control and component sizing rely heavily in the MMC modeling. Several works have been published on the MMC modelling [26]-[38], and component sizing [39]-[46], but still some gaps remain to be filled, as described below.

In [26], the MMC has been modeled from the point of view of the ac side, considering each submodule (SM) as a constant voltage source, disregarding the submodule capacitor dynamics in the ac-side terminal current controller, and taking into account only the fundamental component of the MMC voltages and currents. This approach is enough for designing the compensator responsible for controlling the power exchanged between the MMC and the ac

grid. However, the submodule capacitor voltage variation and the harmonic components in the arm current are not considered. In [27] the MMC has been modeled in open-loop state and with the submodule capacitive dynamics taken into account, which yields non-linear and time-varying differential equations. The MMC non-linear time-varying model was developed further in [28] and [29]. The proposed model in [28] and [29] considers the ac-side terminal current compensator and the circulating current suppression compensator, following the control strategy described in [30]. Even though the model presented in [29] is adequate, for the control strategies employed, a steady-state model is nonetheless needed for predicting the steady-state magnitude of the MMC quantities, and, in turn, permitting the sizing of the components of the MMC. Thus, in [31], a parametric model for the steady-state magnitude of the circulating current is developed. The described model presents a relative high error, in comparison to the simulation results, and, if applied to HVDC systems, such as described in [18], [22], and [20], the error becomes even higher. Another, more detailed steady-state model is developed in [32]. The presented model correctly predicts the amplitude of the circulating current and, also, predicts the condition for arm current resonance that can destabilize the converter. Then, in [33], a different steady-state model is described, using a different mechanism than [32], and providing simpler equations. The predictions in [33], were shown to be also accurate. However, the models presented in [32] and [33] are still incomplete, in the sense that they do not predict the amplitudes of all harmonic components of the currents and voltages of the MMC. Other dynamic models are described in [34], [35], [36], and another steady-state model is presented in [37], with no advantages added in comparison to the previously commented models, from the point of view of the author. In [38] a new dynamic model is developed in *dq*-frame, facilitating the designing of the MMC compensators. However, the *dq*-frame model proposed in [38], is not suitable for deriving equations for the amplitude of the harmonic components of the voltages and currents of the MMC.

Regarding the component sizing of the MMC, the two main components addressed in the literature are the arm inductor and the SM capacitor. A method for selecting the arm inductor, based on the fact that its reactance limits the circulating current is proposed in [31]. Since the model presented by [31] does not predict correctly the circulating current amplitude for high dc voltages, as previously stated, the proposed method cannot be used for selecting the arm inductors in HVDC systems. Another method, proposed in [39], uses three main points for selecting the arm inductance, which are: a) circulating current limiting, b) dc-side fault current limiting, and c) switching frequency filtering. Two other publications, [40] and [41], also use the same points for selecting the arm inductor. However, in HVDC systems, the circulating current increases the arm power loss. Thus, the circulating current needs to be suppressed. If this suppression is performed solely by the inductor, this means that the inductance needs to be high, which also increases the arm resistance, generating more power loss in the arm. Therefore, the arm inductor cannot be selected using a). Another important feature for HVDC systems is the dc-side fault handling, which means that the SMs themselves have the capability to drive the fault current to zero, a short time after the fault inception. Thus, the arm inductor do not act as a limiting device for the fault current, in case of dc-side faults. As a consequence, the arm inductor can be selected based solely on c), taking into account the method proposed by [39], [40], and [41]. However, there is another important point for the selection of the arm inductance, neglected by the aforementioned authors, the arm resonance.

The most widely used method for sizing the submodule capacitor has been proposed in

[42]. The same method has been used in [30], [39]. However, the equation proposed in [42] results in a minimum capacitance, and not the more adequate capacitance for a specific desired submodule capacitor voltage variation. A more detailed and accurate method to calculate the capacitance for each submodule capacitor is proposed in [43]. The proposed method uses the ac-side terminal current angle to determine, graphically, the stored nominal energy of the submodule capacitor. Then, the stored nominal energy and the modulation index are used to size the submodule capacitor. The resultant capacitance features less error than that provided by the method proposed in [42], but still presents an error. In [44], a numerical method for sizing the submodule capacitor is proposed. However, the proposed method is more complex than the one in [43]. A different approach for sizing the submodule capacitor is proposed in [45]. The proposed method estimates the submodule capacitance analytically, without graphical or numerical aid. On the other hand, for HVDC systems, where the average switching frequency in the switches is low, the capacitor energy fluctuation, calculated in [45], becomes inaccurate, generating, in turn, inexact capacitances. Furthermore, the equation presented in [45] is unnecessarily complex. The submodule capacitor sizing is further addressed in [46]. The method proposed in [46] provides results closer to those simulated, in comparison to the model proposed in [42], but it is not as accurate as those provided by [43]. On the other hand, [46] equations are more tractable than in [45]. However, a completely analytical method, that provides an accurate capacitance (with less than 6% error) for the submodule capacitor, has not been published yet. Further, since the circulating current, in some cases, is injected in the MMC arm to decrease the submodule capacitor voltage variation [47]-[50], the capability of calculating the impact of the circulating current (injected or not) in the submodule capacitor voltage variation, is an important feature of a capacitor sizing method.

1.3.2 Control of the MMC

The control of the MMC follows in two main objectives: the ac-side terminal current control and the circulating current control. The ac-side terminal current can be controlled based on the classical methods applied for years to the conventional two-level VSC [10]. However, for the circulating current, several control strategies have been proposed in the literature [30], and [51]-[61].

One of the first methods for a circulating current suppressing compensator (CCSC) was proposed in [30]. The proposed method relies on calculating the *dq*-frame components for the second harmonic in the circulating current. Since this second harmonic is of negative sequence, the rotating matrix used to calculate the *dq*-frame components, is set to rotate twice the angular velocity of the ac-side terminal current frequency, and in the opposite direction. Thus, a simple PI compensator can be applied to bring the amplitude of the second harmonic to zero. As the second harmonic has the strongest contribution for the circulating current, the latter is, consequently, also driven to approximately zero. On the other hand, if the system is not balanced, the method proposed in [30] becomes inadequate. Thus, a new predictive control strategy is proposed in [51]. In [51], a discrete model of the MMC is created and the $(n + 1)$th sample predicted by a proposed strategy to suppress the circulating current. Further, two other control strategies are proposed in [52], for an MMC featuring redundant SMs, and [53], for unbalanced systems. In [53], the circulating current is separated in zero-sequence, positive-sequence, and negative-sequence, and a compensator is designed to control each component.

A simpler method than [53] is proposed in [54], where each leg of the MMC has its circulating current suppressed by a resonant compensator, tuned to each harmonic component in the circulating current. The method proved to be efficient for unbalanced and single-phase systems. The resonant compensator is, again, addressed in [55]. In [55], the control reference for the circulating current resonant compensator is calculated from instantaneous values of the arm current, suitable for cases where the reference is different than zero. However, to implement a resonant compensator for each harmonic component in the circulating current, in each leg of the MMC, becomes computationally heavy. Therefore, another, simpler method was proposed in [56]. The described method is formed by a PI compensator and a repetitive controller (RC), and showed promised results for suppressing the circulating current. Studies presented in [57] showed the interference of the PI compensator with the RC in [56]. Thus, [57] proposed the use of only a proportional gain together with the RC, first proposed in [56]. The result, once more, proved to be satisfactory. Further, the PI compensator working in parallel with an RC was again addressed in [58], where the RC was modified and the overall circulating current suppression action improved. However, the circulating current suppressing compensator is not completely decoupled from the ac-side terminal current compensator, and the latter, may generate saturation in both control loops, causing instability. For this reason, feedforward strategies are important for the CCSC action attenuation, avoiding saturation, without loss of control efficiency.

The use of feedforwards to improve the action of the CCSC, or to dismiss its use completely, was addressed in [59] and [60]. The feedforward proposed in [59], uses an analytical prediction of the circulating current magnitude to feed the control loop, and no CCSC strategy is applied. However, the magnitude of the arm voltage to be added to the control loop can still be improved, as the feedforward seems not able to suppress the circulating current completely. On the other hand, in [60], another feedforward is designed to address the issue of the third-harmonic component in the ac-side terminal voltage, that is present even when the circulating current is completely suppressed. A different approach is taken in [61], where the arm voltage is the quantity controlled. Nevertheless, the quality of the ac-side terminal current is compromised in the process.

Therefore, the author believes that the use of feedforwards in the control loop can enhance the transient and steady-state response of the CCSC overall. However, the feedforward proposed in [59] can still be improved. Also, the magnitude of the third-order harmonic component in the ac-side terminal voltage, for a completely suppressed circulating current, amounts to 1% in comparison to the fundamental harmonic, in the HVDC system presented in [18]-[22]. Moreover, this 1% in magnitude is too close to the MMC resolution, making it difficult to control without increasing the switching frequency in the SMs. For these reasons, the third-order harmonic component in the ac-side terminal voltage is disregarded in this thesis.

1.3.3 Simulation of the MMC

Simulation of an MMC-based HVDC transmission system with hundreds of SMs per phase is associated with a heavy computational burden if a switched (detailed) model of the MMC is used. Thus, research efforts have been dedicated to solving this issue [62]-[66]. However, the algorithms have been developed for the half-bridge-SM (HBSM) -based MMC and, therefore, are not directly applicable to the full-bridge-SM (FBSM) based MMC, which has been pre-

sented in [67]-[69] as of great importance in dc-side fault handling capability, specially in long distance HVDC transmission systems.

Further, in [66], the simulation models are studied and classified in six types: Full Physics-Based Model (Type 1); Detailed Nonlinear IGBT-Based Model (Type 2); Simplified IGBT-Based Model (Type 3); Detailed Equivalent-Circuit-Based Model (Type 4); Average Value Model Based on Switching Functions (Type 5), and Average Value Model Based on Fundamental Frequency (Type 6). In the aforementioned types, a gap remains between Type 4 and Type 5 models, that is, from a SM model represented by a Thevenin equivalent with time-dependant resistance (Type 4), the classification jumps to an average model where all SM capacitor voltages are assumed to be perfectly balanced and the circulating current completely suppressed (Type 5). Considering that the losses in the SM switches are very small in the MMC, [15], they represent a small contribution for the converter dynamics as a whole, for power systems simulations. Therefore, a simplified equivalent-circuit-based simulation model (SEC) that considers all switches as ideal switches, neglecting its resistances, is more suitable for the simulation of HVDC systems applications, and it has not been developed yet. Furthermore, the SEC simulation model should also be capable of of reproducing the SM switches non-linearity and the instantaneous voltages in every SM capacitor.

1.3.4 Topologies and their dc-side fault handling capabilities

The implementation an MMC based on half-bridge submodule (HBSM) topology, is the simplest and, therefore, the most common type of submodule. The HBSM inserts only one switch in series with the current path, for each ac-side terminal voltage step and, therefore, the resultant MMC features low power losses [15], [70]-[72]. The disadvantage of an HBSM-based MMC, however, is that in case of dc-side faults, the switches are disabled and the SMs become short-circuits, allowing the ac grid to feed the dc fault [18]-[22], and [73]. Therefore, an MMC-based HVDC project using the HBSM relies heavily on the ac-side breakers [72], which do not have an operation time short enough to preclude damages to the converter during faults. The converter and the transmission line have to be designed to uphold this fault current for the time it takes for the ac breaker to operate, increasing the overall cost.

To address the aforementioned shortcoming, the full-bridge submodule-based (FBSM) configuration [18], and the clamp-doubled submodule-based (CDSM) configuration [71], have been proposed. An FBSM-based MMC is capable of driving the fault current down to zero, if its switches are disabled. Therefore, it isolates the ac and dc sides of the converter faster than an ac breaker. However, as compared to an HBSM-based MMC, a FBSM-based MMC has twice the number of series-connected switches in its current path and, consequently, features higher power loss. The CDSM, on the other hand, inserts, effectively, 1.5 switches per ac-side terminal voltage step in its current path and, therefore, it features larger power loss than the HBSM-based configuration, but lower power loss than the FBSM-based configuration. A CDSM-based MMC is immune to dc-side faults, but the voltage that appears, effectively, under dc-side faults and opposes the ac grid voltage is half the total arm voltage [74]. Consequently, the fault current can flow if the grid voltage is adequately large. An in-depth analysis of faulted as well as normal operation of the aforementioned topologies can be found in [15].

Therefore, a SM topology that features the same dc-fault handling capability as the FBSM with lower power loss than that of the CDSM has not been proposed yet.

1.4 Thesis Outline

In Chapter 2, this thesis proposes, a complete harmonic steady-state model of the MMC, capable of predicting the amplitudes of the harmonic components in the converter currents and voltages. Further, the calculation of the amplitude of the harmonic components emerge naturally from the application of the superposition principle in the arm currents, followed by the analysis of the positive feedback loop generated by the circulating current. This mechanism is, in the opinion of the author, a more insightful approach than evaluating the energy stored in the leg. Also, from the positive feedback loop analysis, the resonance condition for the circulating current is readily found, and can be used to evaluate the stability of the converter regarding the circulating current, and sizing of the arm inductor. Finally, the possibility to calculate the amplitude of the harmonic components of the submodule capacitor voltage, allows the development of a more efficient method for sizing the submodule capacitor.

In Chapter 3, this thesis proposes a simulation model for the MMC. The proposed model combines a simple circuit model, constructed in a circuit simulation software environment, with a program code, written in a universally diffused programming language such as *C* and linked to the circuit simulation software. Thus, it drastically reduces simulation runtime and offers a flexible interface through which the number of submodules and other parameters can readily be defined by the user. Further, the program code can be developed in an independent platform and linked to the main circuit simulation software through a general-purpose block. The proposed model can simulate MMCs based on both half-bridge and full-bridge submodule configurations, captures start-up and other dynamic transients, and enables simulation of faulted scenarios. Simulation study cases demonstrate the validity and computational efficiency of the proposed simulation model.

Chapter 4 proposes a new feedforward strategy, based on the off-line calculation of the initial steady-state value for the arm voltage, that corresponds to the arm voltage generated purely by the ac-side terminal current. The initial steady-state value for the arm voltage is, in turn, subtracted from the voltages of both arms, cancelling the cause for the circulating current. Thus, the proposed feedforward has a higher suppressing action than that of the feedforward methods mentioned in Section 1.3.2. Also, since the practical value for the MMC parameters, such as arm inductance and arm resistance for example, may vary, the proposed feedforward action is tested by itself, and together with two different control strategies, applied to back-to-back HVDC systems.

To achieve both dc-side fault current handling capability and higher efficiency, a new MMC configuration is proposed in Chapter 5. The proposed MMC, referred in this thesis to as the *lattice modular multilevel converter* (LMMC) is implemented by two half-bridge converters, a cascade of networks that consist of electronic switches, and multiple capacitors, as discussed in Section 5.1. It features lower power losses than an equivalent HBSM-based MMC, CDSM-based MMC, and FBSM-based MMC, while it offers the same fault handling capability as that offered by a FBSM-based MMC. The aforementioned objective is in line with the prior research efforts. For example, to reduce the cost and switching power loss of the FBSM, the *unipolar voltage full-bridge submodule* has been proposed in [69]. On the other hand, to enhance the dc fault handling capability of the CDSM, with the same conduction power loss, the *five-level cross-connected submodule* has been proposed in [76]. Further, the *three-level cross-connected submodule* proposed in [69] is an improved version of the five-level

cross-connected submodule where the switching power losses are reduced. Moreover, various topologies for multilevel converters with reduced number of dc sources and switching states, including topologies based on the packed *U-cell topology*, are discussed in [77]. However, since the HBSM is the most efficient configuration (regarding power loss in the switches), the CDSM is no less efficient than all the other aforementioned configurations that feature the dc fault handling capability, and the FBSM, when subjected to a dc-side short circuit and disabled, requires the largest grid voltage before it allows the fault current to flow, this thesis concentrates only on the HBSM, FBSM, and CDSM as its baselines. For ease of analysis, it is assumed in this thesis that an MMC consists entirely of FBSMs, HBSMs, or CDSMs.

In Chapter 6, a new submodule configuration is proposed, to achieve approximately the same efficiency as that offered by the HBSM-based MMC, the same dc-side fault handling capability offered by the FBSM-based MMC, and a reduced voltage stress for the switches. The proposed submodule, referred in this thesis to as the *lattice submodule* (LSM), consists of two half-bridge converters, a network of switches, and four capacitors.

Chapter 2

Development of the Steady-State Harmonic Model of the MMC

A complete analytical steady-state model of the MMC can be used for simplified simulation, development of optimization algorithms, component sizing, and assessment of the impact of different parameters on the MMC performance. Thus, this chapter presents the development of such a model.

The model described in this chapter enables one to calculate the magnitude of the harmonic components of the MMC arm voltage, submodule capacitor voltage, and arm current. In addition, the model allows for the calculation of the magnitude and phase angle of the modulating function, and it also presents a criterion for resonance of the arm current.

This chapter also presents, an accurate method of capacitor sizing, based on the steady-state harmonic model mentioned above. The proposed method provides the exact submodule capacitance (i.e., a capacitance that, when used in the MMC, results in dc voltage fluctuation that matches the desired range) for a given submodule capacitor voltage variation and a given injected circulating current.

2.1 Foundation and assumptions regarding the MMC model

Figure 2.1 shows a more detailed schematic diagram of one leg of a three-phase MMC, than the one presented in Chapter 1. As Figure 2.1 shows, the leg has a total of $2N$ SMs which are divided equally between the upper and lower arms and are indexed by n ($n = 1, 2, 3, ..., N$ in the upper arm, and $n = N+1, N+2, N+3, ..., 2N$ in the lower arm). The voltage sources of Fig. 1.4, have been replaced by their practical correspondents, i.e., capacitors, as Fig. 2.2 shows. Moreover, Fig. 2.2 shows that, depending on the topology on which the SMs are based, an SM may contain one capacitor (HBSM) or more capacitors (CDSM). Consequently, the number of capacitors in the arm, M, may be different than the number of SMs per arm, i.e., N. Further, M is determined by the ratio dc-side voltage to average capacitor voltage desired, i.e., $\overline{v}_c = v_{dc}/M$. Thus, if $\overline{v}_c$ is kept the same, the parameter M also remains the same independently of the topology on which the SMs are based. Figure 2.1 also shows the ac voltage of an SM, denoted by v_{Sn}.

The *upper arm current*, which is also the current that flows through SMs 1 through N, is

denoted by i_1, whereas i_2 represents the *lower arm current*, which is the current through SMs $N+1$ through $2N$. The *ac-side terminal current*, i.e., $i_1 - i_2$, is denoted by i_t. The sum of the ac voltages of the upper arm SMs, that is, $v_{S1} + v_{S2} + ... + v_{SN}$, is denoted by v_1, and the sum of voltages of the lower arm SMs, i.e., $v_{S(N+1)} + v_{S(N+2)} + ... + v_{S(2N)}$, is labeled as v_2; hereafter, v_1 and v_2 are referred to as the *upper arm voltage* and *lower arm voltage*, respectively, or to as the *arm voltages*, collectively. Figure 2.1 also shows that each arm is connected in series with a corresponding reactor of inductance L and resistance R. Figure 2.1 further shows the *ac-side terminal voltage*, with reference to node 0, i.e., the (virtual) dc-side midpoint of the MMC. The host ac grid, as seen by the MMC, is represented by a voltage source in series with an inductance, L_t, and a resistance, R_t. The *grid voltage* with reference to node 0 is signified by v_g, and the *dc-side voltage* of the MMC is denoted by v_{dc}. In this paper, it is assumed that the switches are *disabled* by the control, i.e., their gating pulses are blocked, if a dc-side fault is detected; thus, a *disabled* switch may conduct in reverse, through its anti-parallel diode, if such diode is part of the switch.

Also, in the SM topologies that Fig. 2.2 shows, the voltage in each capacitor is referred to, in this thesis, as *submodule capacitor voltage*. Similarly, the difference between the positive and negative peaks of the submodule capacitor voltage, is referred to as *submodule capacitor voltage variation*.

Further, it is important to point out that the arm currents, arm voltages, and submodule capacitor voltages, exhibit harmonic components other than just the fundamental component. More specifically, the even harmonics in the arm current are referred to as *circulating current*, and they are common to both arms.

2.2 Modelling of the MMC

2.2.1 Fundamental harmonic MMC model

The arm voltage is shared evenly between the SMs through a *voltage balancing algorithm* (VBA) (more details are presented in Chapter 3), that controls the average submodule capacitor voltage to

$$\overline{v}_c = \frac{v_{dc}}{M} \tag{2.1}$$

which is hereafter referred to as the MMC "voltage resolution", since this is the smallest average voltage value that the converter is capable to produce in the *inner voltage*, denoted by e_t and given by

$$e_t = \frac{v_2 - v_1}{2} \tag{2.2}$$

Thus, the fundamental component of the voltage on each arm is given by

$$v_1 = n_1 \overline{v}_c \tag{2.3}$$

$$v_2 = n_2 \overline{v}_c \tag{2.4}$$

where n_1, represents the number of SM *inserted* (*on*-state) in the upper arm, and n_2, represents the number of SM *inserted* in the lower arm. If the arm inductances and resistances are assumed

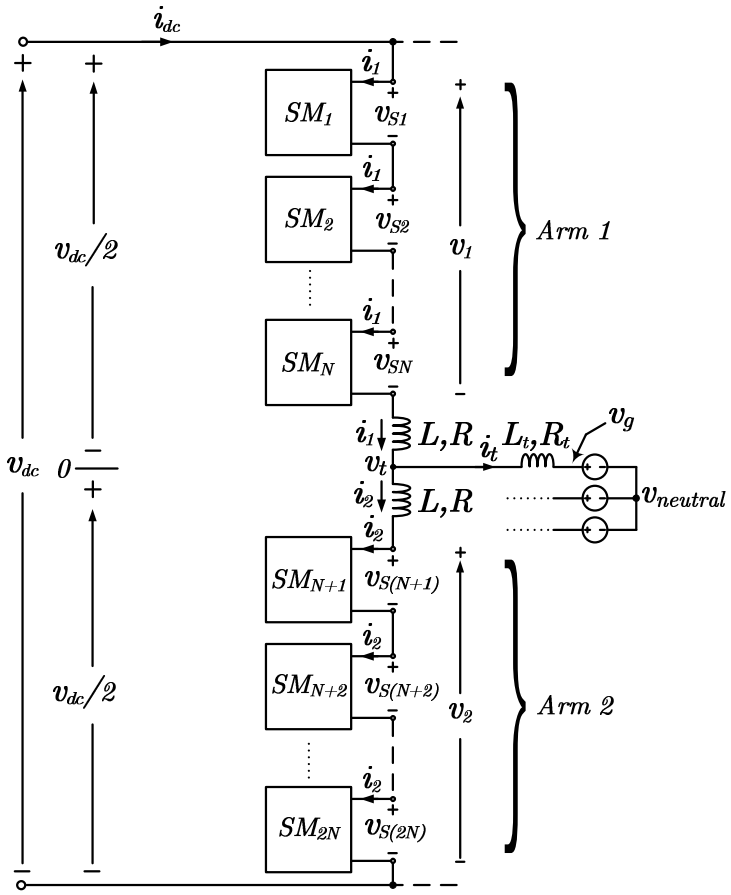

Figure 2.1: Schematic diagram for one leg of a three-phase MMC.

equal in both arms (symmetrical converter), the MMC arms appear connected in parallel from the point of view of the ac grid voltage. Thus, the ac-side terminal current is divided equally between the arms, resulting in the model shown in Figure 2.3.

Applying Kirchhoff voltage law (KVL) in the inner loop of the schematic showed in Figure 2.3, one finds

$$v_{dc} = v_1 + v_2 \tag{2.5}$$

Applying KVL in the outer loop one finds

$$-\frac{v_{dc}}{2} + v_1 + \left(\frac{L}{2} + L_t\right)\frac{di_t}{dt} + \left(\frac{R}{2} + R_t\right)i_t + v_g = 0 \tag{2.6}$$

Let $R' = \left(\frac{R}{2} + R_t\right)$ and $L' = \left(\frac{L}{2} + L_t\right)$, then eliminating v_{dc} between (2.5) and (2.6) results

$$\frac{v_2 - v_1}{2} = L'\frac{di_t}{dt} + R'i_t + v_g \tag{2.7}$$

Applying KVL in the center loop including e_t yields

$$\frac{v_{dc}}{2} - v_2 + e_t = 0 \tag{2.8}$$

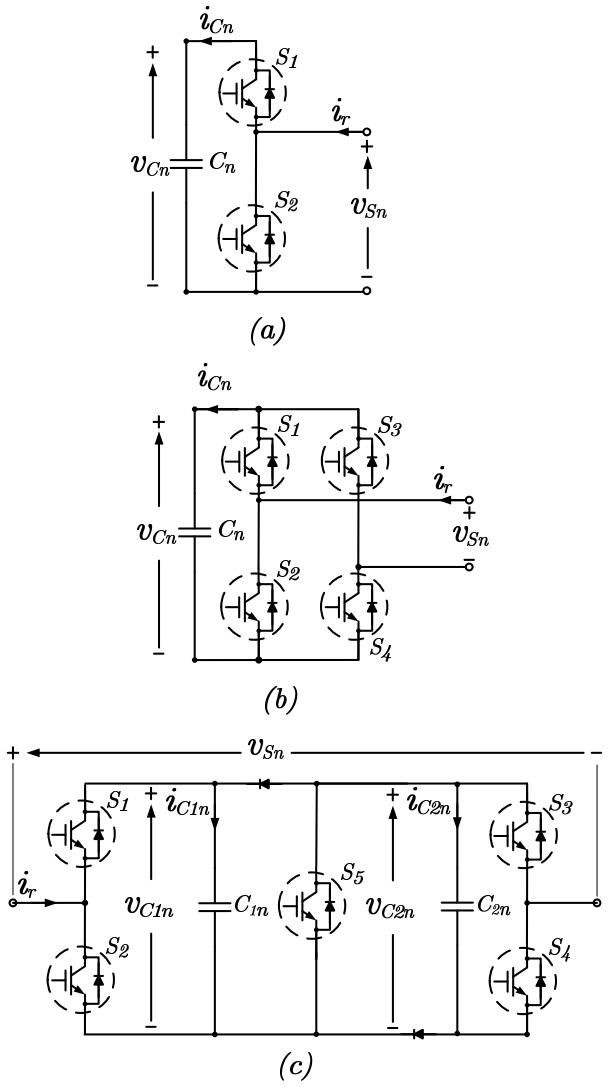

Figure 2.2: Main MMC SM topologies currently known:(a) Half-bridge submodule - HBSM; (b) Clamp-doubled submodule - CDSM; (c) Full-bridge submodule - FBSM.

Solving for e_t and eliminating v_{dc} between (2.5) and (2.8) results

$$e_t = L' \frac{di_t}{dt} + R' i_t + v_g \tag{2.9}$$

Representing (2.9) in a simplified equivalent circuit, one can find the circuit illustrated by Figure 2.4.

Eliminating v_1 and v_2 between (2.3), (2.4), and (2.2) yields

$$e_t = \frac{\overline{v}_c}{2} (n_2 - n_1) \tag{2.10}$$

Equation (2.10) presents the inner voltage as a function of the difference between n_1, and n_2. Assuming, for example, a value of $\frac{M}{2} - 1$ for n_1, and $\frac{M}{2} + 1$ for n_2 (keeping $n_1 + n_2 = M$ for submodule capacitor voltage balancing), corresponding to the bypassing of one submodule in

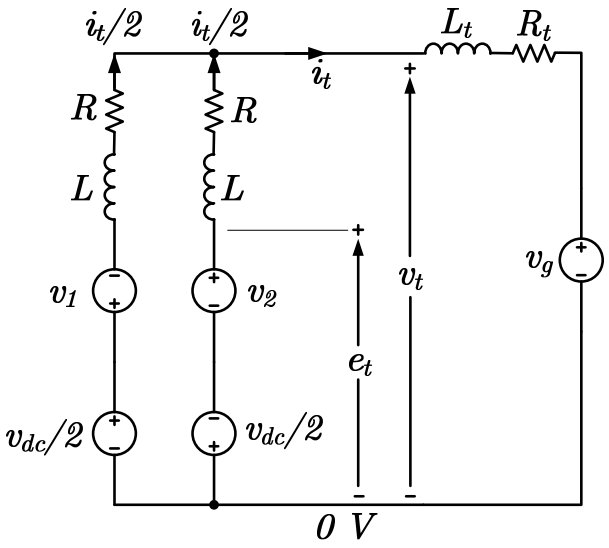

Figure 2.3: MMC equivalent circuit from the point of view of the ac grid.

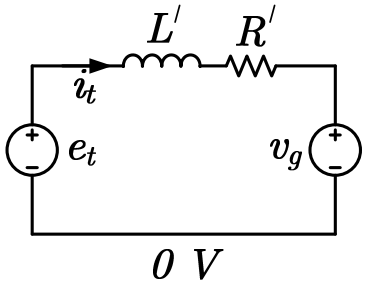

Figure 2.4: Simplified MMC equivalent circuit from the point of view of the ac grid.

the upper arm, and the insertion of one submodule in the lower arm, the resultant inner voltage is $\overline{v}_c$, which confirms that the minimum change in the inner voltage is, indeed, $\overline{v}_c$, as stated previously.

Let

$$\frac{n_2 - n_1}{2} = a \tag{2.11}$$

then, in (2.11), a is hereafter referred to as the *asymmetry* of the MMC. If the asymmetry is positive, the number of SMs inserted in the lower arm, n_2, is higher than the number of SMs inserted in the upper arm, n_1, and vice-versa. If the asymmetry is zero, $n_1 = n_2 = \frac{M}{2}$, and e_t is zero. In the example described above, the asymmetry is equal to one unit of resolution.

Figure 2.5 illustrates the dynamic of the asymmetry for $a = 1$. The maximum asymmetry is M, when all SMs of one arm are inserted and all SMs of the other arm are bypassed, resulting in the maximum value of $\frac{v_{dc}}{2}$ for the inner voltage.

The modulation technique referred to as Near Level Control (NLC) modulation [15], is based, in this thesis, on the calculation of the asymmetry variable, a, knowing that it can only assume integer multiples of $\overline{v}_c$. Therefore, the asymmetry needed to generate the desired e_t^* is

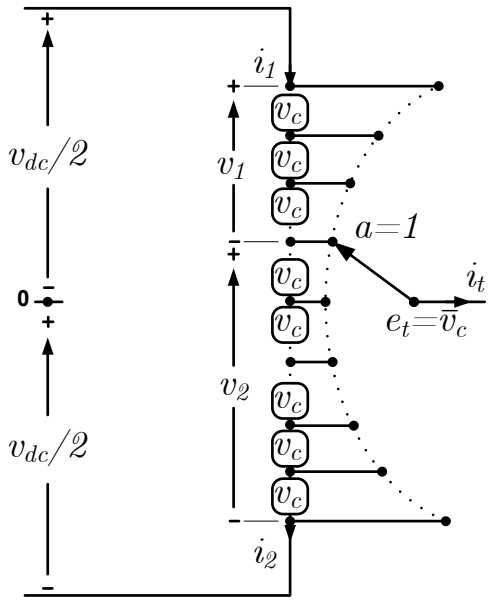

Figure 2.5: Asymmetry dynamic example for $a = 1$.

calculated by

$$a = round\left[\frac{e_t^*(kT_s)}{\bar{v}_c}\right] \tag{2.12}$$

where *round* is a function that rounds the division to the nearest integer value, $e_t^*(kT_s)$ is the discrete function of the reference *inner voltage*, k is the integer sample pointer and T_s is the MMC sample time, calculated by $T_s = 1/\left[2(M+2)f_g\right]$, where $M+1$ is the number of levels of the ac-side terminal voltage, and f_g is the grid frequency.

For a high number of M, the MMC sample time T_s becomes smaller and smaller and the following approximations can be used.

$$\lim_{T_s \to 0} e_t^*(kT_s) = e_t^* \tag{2.13}$$

$$\lim_{\frac{\bar{v}_c}{v_{dc}} \to 0} \left\{round\left(\frac{e_t^*}{\bar{v}_c}\right)\right\} = \frac{e_t^*}{\bar{v}_c} \tag{2.14}$$

The term *high-density* MMC is hereby applied to converters to which (2.13) and (2.14) can be safely applied. In practical terms, when M reaches 130, the total harmonic distortion in e_t is less than 1.5%, complying with the most strict limit indicated in [78], presenting a good threshold for the use of the aforementioned terminology.

Applying the approximations described in (2.13) and (2.14), yields

$$a = \frac{e_t^*}{\bar{v}_c} \tag{2.15}$$

Substituting $M = n_1 + n_2$ into (2.11) and solving for n_1 and then n_2, one can deduce the number of SM inserted in the upper and lower arms as

$$n_1 = \frac{M}{2} - a \tag{2.16}$$

$$n_2 = \frac{M}{2} + a \tag{2.17}$$

The voltage e_t^* is given by the maximum voltage possible to be generated by the MMC, $\frac{v_{dc}}{2}$, times the modulating function, m, as follows

$$e_t^* = \frac{v_{dc}}{2} m \tag{2.18}$$

Substituting (2.1), (2.15), and (2.18) into (2.16), and into (2.17) yields

$$n_1 = \frac{M}{2}(1 - m) \tag{2.19}$$

$$n_2 = \frac{M}{2}(1 + m) \tag{2.20}$$

Eliminating n_1 and n_2 between (2.19), (2.20), (2.3), and (2.4) results

$$v_1 = \frac{v_{dc}}{2}(1 - m) \tag{2.21}$$

$$v_2 = \frac{v_{dc}}{2}(1 + m) \tag{2.22}$$

where m is given by

$$m = \widehat{m} cos(\omega t + \theta) \tag{2.23}$$

, *theta* is the *modulating function angle*, and $\widehat{m}$ is the *modulation index*, estimated by

$$\widehat{m} = \frac{2\widehat{v_g}}{v_{dc} cos\varphi} \tag{2.24}$$

where $\widehat{v_g}$ is the peak of the grid voltage and φ is the angle of the ac-side terminal current. The estimation given by (2.24) is referred to, in this thesis, as *flat estimation*, since it does not change with the arm current.

At this point, neglecting the MMC current and voltage harmonic components different than the fundamental, one can state that the arm voltages are formed by a dc level given by $\frac{v_{dc}}{2}$ and a fundamental component given by $\frac{v_{dc}}{2}\widehat{m} cos(\omega t + \theta)$.

2.2.2 Open-loop MMC model

The average submodule capacitor voltage is controlled by the VBA, as stated previously, but its instantaneous value change with the integral of the arm current. Since the submodule capacitor voltage impacts in the arm voltages and currents, the following analysis complements the

modelling described in Section 2.2.1, and takes into account the submodule capacitor voltage instantaneous value.

Analyzing Figure 2.1, and with the knowledge that the circulating current has the same direction in both arms, the arm currents i_1 and i_2, can be calculated by

$$i_1 = \frac{i_t}{2} + i_{cm} \tag{2.25}$$

$$i_2 = -\frac{i_t}{2} + i_{cm} \tag{2.26}$$

The infinitesimal variation of the *voltage integrated in the arm*[27], v_i, is given by

$$\frac{dv_{ir}}{dt} = {C_{eq_r}}^{-1} i_r \tag{2.27}$$

where $C_{eq_r}^{-1}$ is the reciprocal of the arm equivalent time-varying capacitance, defined as the submodule capacitance divided by the number of inserted SMs. Thus, ${C_{eq_r}}^{-1}$ can be calculated by

$${C_{eq_r}}^{-1} = \frac{n_r}{C} \tag{2.28}$$

where n_r represents the number of inserted SMs in the arm r ($r = 1$ for the upper arm, and $r = 2$ for the lower arm).

Integrating (2.27) and substituting into (2.28), yields the voltage integrated in the arm by

$$v_{ir} = \frac{1}{C} \int n_r i_r dt \tag{2.29}$$

The instantaneous submodule capacitor voltage for the arm r is then given by

$$v_{Cr} = \frac{v_{ir}}{M} \tag{2.30}$$

The instantaneous arm voltages can then be calculated by

$$v_r = n_r v_{Cr} \tag{2.31}$$

The circulating current is produced by the even harmonic components in the arm voltages, generated, in turn, by the integration of the arm current in the submodule capacitor, as it will be explained in detail in Section 2.3. This voltage harmonic components appear with the same polarity and magnitude in both arms. Thus, from (2.2), one concludes that the circulating current circulates through the MMC leg without affecting the steady-state of the ac-side terminal voltage. Figure 2.6 presents the model for the circulating current, i_{cm}.

Applying KVL in the circuit shown in Figure 2.6 yields

$$\frac{di_{cm}}{dt} = \frac{1}{L}\left[\frac{v_{dc}}{2} - \left(\frac{v_1 + v_2}{2}\right) - Ri_{cm}\right] \tag{2.32}$$

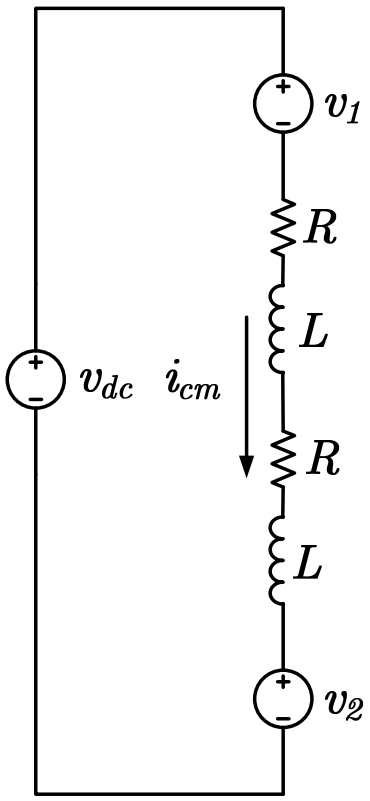

Figure 2.6: Simplified MMC equivalent circuit from the point of view of the dc grid.

Eliminating v_r (for $r = 1$ and $r = 2$) between (2.31) and (2.32), the differential equation for the circulating current can be derived

$$\frac{di_{cm}}{dt} = \frac{1}{L}\left[\frac{v_{dc}}{2} - \left(\frac{n_1 v_{C1} + n_2 v_{C2}}{2}\right) - R i_{cm}\right] \tag{2.33}$$

Eliminating n_1 and n_2 between (2.19), (2.20), and (2.33), yields

$$\frac{di_{cm}}{dt} = -\frac{M}{4L}(1-m)v_{C1} - \frac{M}{4L}(1+m)v_{C2} - \frac{R}{L}i_{cm} + \frac{v_{dc}}{2L} \tag{2.34}$$

Eliminating v_1 and v_2 between (2.7), (2.19), (2.20), and (2.31), and solving for $\frac{di_t}{dt}$ one can derive

$$\frac{di_t}{dt} = -\frac{M}{4L'}(1-m)v_{C1} + \frac{M}{4L'}(1+m)v_{C2} - \frac{R'}{L'}i_t - \frac{1}{L'}v_g \tag{2.35}$$

Substituting (2.30) into (2.27) yields

$$\frac{dv_{Cr}}{dt} = \frac{1}{MC}n_r i_r \tag{2.36}$$

Eliminating i_1 and i_2 between (2.25), (2.26), and (2.36) results

$$\frac{dv_{C1}}{dt} = \frac{1}{4C}(1-m)i_t + \frac{1}{2C}(1-m)i_{cm} \tag{2.37}$$

$$\frac{dv_{C2}}{dt} = -\frac{1}{4C}(1+m)i_t + \frac{1}{2C}(1+m)i_{cm} \tag{2.38}$$

Assuming $\frac{dv_{C1}}{dt}$, $\frac{dv_{C2}}{dt}$, $\frac{di_t}{dt}$, and $\frac{di_{cm}}{dt}$ as state variables, the open-loop state equation of the MMC for one phase is given by

$$\frac{d}{dt}\begin{bmatrix} v_{C1} \\ v_{C2} \\ i_t \\ i_{cm} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & a_{33} & a_{34} \\ a_{41} & a_{42} & a_{43} & a_{44} \end{bmatrix}\begin{bmatrix} v_{C1} \\ v_{C2} \\ i_t \\ i_{cm} \end{bmatrix} + \begin{bmatrix} b_{11} \\ b_{21} \\ b_{31} \\ b_{41} \end{bmatrix} \tag{2.39}$$

where

$$a_{11} = 0, a_{12} = 0, a_{13} = \frac{1}{4C}(1-m), a_{14} = \frac{1}{2C}(1-m) \tag{2.40}$$

$$a_{21} = 0, a_{22} = 0, a_{23} = -\frac{1}{4C}(1+m), a_{24} = \frac{1}{2C}(1+m) \tag{2.41}$$

$$a_{31} = -\frac{M}{4L'}(1-m), a_{32} = \frac{M}{4L'}(1+m), a_{33} = -\frac{R'}{L'}, a_{34} = 0 \tag{2.42}$$

$$a_{41} = -\frac{M}{4L}(1-m), a_{32} = -\frac{M}{4L}(1+m), a_{33} = 0, a_{34} = -\frac{R}{L} \tag{2.43}$$

$$b_{11} = 0 \tag{2.44}$$

$$b_{21} = 0 \tag{2.45}$$

$$b_{31} = \frac{v_g}{L'} \tag{2.46}$$

$$b_{41} = \frac{v_{dc}}{2L} \tag{2.47}$$

Equation (2.39) form the complete open-loop MMC model.

The open-loop model presented in this section can be augmented to a closed-loop model. The MMC closed-loop model for a specific control strategy is proposed in [28] and [29].

2.3 Proposed steady-state harmonic model of the MMC

As the arm capacitance in the MMC is time-varying, (2.28), the differential equations (2.32) and (2.35) exhibit time-varying coefficients. Therefore, the analytical solution for the arm currents and voltages, for analysis purposes, becomes complex. The method proposed in this thesis, is based on dividing the arm current in i_t and i_{cm}, analysing the impact of each in the arm voltages, and applying *geometric series* to find the convergence point. The analysis of the series convergence, identify the stability conditions for the arm currents.

Substituting (2.25), (2.26), (2.29), and (2.30) into (2.31) yields

$$v_r = \frac{n_r}{CM}\int n_r\left(\frac{i_t}{2} + i_{cm}\right)dt \tag{2.48}$$

Dividing (2.48) in two parts, $v_r^{i_t}$ and $v_r^{i_{cm}}$, representing the contribution of i_t and i_{cm} in the *arm voltage* v_r, results

$$v_r^{i_t} = \frac{n_r}{2CM}\int n_r i_t dt \tag{2.49}$$

$$v_r^{i_{cm}} = \frac{n_r}{CM}\int n_r i_{cm} dt \tag{2.50}$$

and

$$v_r = v_r^{i_t} + v_r^{i_{cm}} \tag{2.51}$$

Considering that the active and reactive power exchanged with the ac grid are controlled by the ac-side terminal current compensator, described in [10], the magnitude and phase of the ac-side terminal current are constant and known. Therefore, i_t is expressed by

$$i_t = \widehat{I}cos(\omega t + \varphi) \tag{2.52}$$

where $\widehat{I}$ is estimated by

$$\widehat{I} = \frac{\sqrt{P^2 + Q^2}}{\sqrt{\frac{3}{2}}v_{gLL}} \tag{2.53}$$

In (2.53), v_{gLL} represents the line-to-line grid voltage ($\sqrt{3}v_g$), P and Q are the active and reactive powers exchanged with the ac grid, respectively.

From (2.49), the voltage $v_r^{i_t}$, in the upper and lower arms, can be derived as

$$\begin{aligned} v_1^{i_t} = &\left(\frac{M\widehat{I}}{8\omega C} + \frac{M\widehat{m}^2\widehat{I}}{64\omega C}\right) sin(\omega t + \varphi) \\ &- \left(\frac{M\widehat{m}\widehat{I}}{16\omega C} + \frac{M\widehat{m}\widehat{I}}{32\omega C}\right) sin(2\omega t + \varphi + \theta) \\ &+ \left(\frac{M\widehat{m}^2\widehat{I}}{64\omega C}\right) sin(3\omega t + \varphi + 2\theta) \\ &- \left(\frac{M\widehat{m}\widehat{I}}{16\omega C}\right) sin(\varphi - \theta) \\ &+ \left[\frac{M\widehat{m}^2\widehat{I}}{16C} cos(\varphi - \theta) cos(\omega t + \theta) - \frac{M\widehat{m}\widehat{I}}{16C} cos(\varphi - \theta)\right] t \end{aligned} \tag{2.54}$$

$$
\begin{aligned}
v_2^{i_t} = &-\left(\frac{M\widehat{I}}{8\omega C} + \frac{M\widehat{m^2 I}}{64\omega C}\right) sin(\omega t + \varphi) \\
&-\left(\frac{M\widehat{mI}}{16\omega C} + \frac{M\widehat{mI}}{32\omega C}\right) sin(2\omega t + \varphi + \theta) \\
&-\left(\frac{M\widehat{m^2 I}}{64\omega C}\right) sin(3\omega t + \varphi + 2\theta) \\
&-\left(\frac{M\widehat{mI}}{16\omega C}\right) sin(\varphi - \theta) + \\
&\left[-\frac{M\widehat{m^2 I}}{16C} cos(\varphi - \theta) cos(\omega t + \theta) - \frac{M\widehat{mI}}{16C} cos(\varphi - \theta)\right] t
\end{aligned}
\tag{2.55}
$$

The ac-side terminal current contribution in the leg voltage is calculated by

$$
\begin{aligned}
(v_1 + v_2)^{i_t} = &-\left(\frac{3M\widehat{mI}}{16\omega C}\right) sin(2\omega t + \varphi + \theta) \\
&-\left(\frac{M\widehat{mI}}{8\omega C}\right) sin(\varphi - \theta) \\
&-\left[\frac{M\widehat{mI}}{8C} cos(\varphi - \theta)\right] t
\end{aligned}
\tag{2.56}
$$

Equation (2.56) shows that the fundamental and the third harmonic components are cancelled in the *leg voltage* ($v_1 + v_2$), leaving only the second harmonic component, the dc component, and the ramp component. The predominance of the second harmonic component is in accordance to the MMC simulations performed for this paper. The second harmonic component of the arm voltages is the origin of the circulating current, which starts circulating in the leg in a positive feedback, as it is integrated in the leg submodule capacitors, increasing its own magnitude. This positive feedback has a geometric increase and its convergence can be analyzed by applying geometric series theory. If the series converges, the system is stable. On the other hand, if the series diverges, the circulating current presents an unstable exponential function of time. Therefore, the goal of this approach is to derive an equation that depends only on the circulating current, and apply geometric series theory to it.

Moreover, for a stable system the ramp component in (2.56) should be zero. Thus, the contribution of i_{cm} to the leg voltage must have a component that cancels the ramp component.

2.3.1 Circulating current amplitude calculation

In this thesis, a circulating current compensator with zero as control reference is referred to as *circulating current suppressing control* (CCSC). On the other hand, when an injected circulating current is desired, the circulating current compensator is referred to as *circulating current*

control (CCC). The equations developed in this section take into account the circulating current effect, for a disabled CCSC. For an enabled CCSC, the amplitude of the circulating current, $\widehat{I_{cm}}$, is approximately zero.

Integrating (2.32) yields

$$i_{cm} = \frac{1}{L}\int\left[\frac{v_{dc}}{2} - \left(\frac{v_1 + v_2}{2}\right) - Ri_{cm}\right]dt \tag{2.57}$$

where $(v_1 + v_2)$ can be divided in

$$(v_1 + v_2) = (v_1 + v_2)^{i_t} + (v_1 + v_2)^{i_{cm}} \tag{2.58}$$

Separating the integral components results

$$i_{cm} = \frac{v_{dc}}{2L}t - \frac{1}{2L}\int(v_1 + v_2)dt - \frac{R}{L}\int i_{cm}dt \tag{2.59}$$

It is noted that, if (2.58) is substituted into (2.59), the result is an iterative equation, in which i_{cm} depends on itself. Thus, if (2.59) can be converted into a geometric series, the conversion can be readily calculated, indicating the steady-state magnitude for i_{cm}. Then, the series ratio can provide more information regarding the system stability.

Eliminating m and n_r (for $n = 1$) between (2.23), (2.19), and (2.50) yields

$$\begin{aligned} v_1^{i_{cm}} = &\left[\frac{M}{4C} - \frac{M\widehat{m}}{4C}cos(\omega t + \theta)\right]\int i_{cm}dt \\ &- \left[\frac{M\widehat{m}}{4C} - \frac{M\widehat{m}^2}{4C}cos(\omega t + \theta)\right]\int cos(\omega t + \theta)i_{cm}dt \end{aligned} \tag{2.60}$$

$$\begin{aligned} v_2^{i_{cm}} = &\left(\frac{M}{4C} + \frac{M\widehat{m}}{4C}cos(\omega t + \theta)\right)\int i_{cm}dt \\ &+ \left[\frac{M\widehat{m}}{4C} + \frac{M\widehat{m}^2}{4C}cos(\omega t + \theta)\right]\int cos(\omega t + \theta)i_{cm}dt \end{aligned} \tag{2.61}$$

The circulating current contribution in the leg voltage is calculated by

$$\begin{aligned} (v_1 + v_2)^{i_{cm}} = &\frac{M}{2C}\int i_{cm}dt \\ &+ \frac{M\widehat{m}^2}{2C}cos(\omega t + \theta)\int cos(\omega t + \theta)i_{cm}dt \end{aligned} \tag{2.62}$$

Substituting (2.62), (2.56), and (2.58) into (2.59) yields

$$\begin{aligned} i_{cm} = & \frac{V_{dc}}{2L}t - \left(\frac{3M\widehat{mI}}{64\omega^2 LC}\right)cos(2\omega t + \varphi + \theta) \\ & - \left(\frac{M\widehat{mI}}{16\omega LC}\right)sin(\varphi - \theta)t \\ & + \left(\frac{M\widehat{mI}}{32LC}\right)cos(\varphi - \theta)t^2 \\ & - \frac{1}{2L}\int (v_1 + v_2)^{i_{cm}}dt - \frac{R}{L}\int i_{cm}dt \end{aligned} \tag{2.63}$$

Let

$$i'_{cm} = -\frac{1}{2L}\int (v_1 + v_2)^{i_{cm}}dt - \frac{R}{L}\int i_{cm}dt \tag{2.64}$$

Then, eliminating $(v_1 + v_2)^{i_{cm}}$ between (2.62) and (2.64) yields

$$\begin{aligned} i'_{cm} = & -\frac{M}{4LC}\int\int i_{cm}dt^2 \\ & - \frac{M\widehat{m}^2}{4LC}\int cos(\omega t + \theta)\int cos(\omega t + \theta)i_{cm}dt^2 \\ & - \frac{R}{L}\int i_{cm}dt \end{aligned} \tag{2.65}$$

Assuming that the odd harmonic components in i_{cm} are either cancelled, as in the case of (2.56), or are small, the circulating current can be expressed as

$$i_{cm} = \widehat{I}_{cm}cos(2\omega t + \varphi_2) + I^0_{cm} \tag{2.66}$$

where $\hat{I}_{cm}$ is the amplitude of the second harmonic component, and I^0_{cm} is the dc component of the circulating current. The component I^0_{cm} represents the current resultant from the power needed to charge the submodule capacitors after they have been discharged to the ac grid. Thus, the dc component is calculated taking into account the active power delivered to the ac grid plus the losses in the arm resistances.

Since each MMC leg delivers one third of the total active power in a three-phase system, I^0_{cm} can be calculated by

$$I^0_{cm} = \frac{P + P_{loss}}{3v_{dc}} \tag{2.67}$$

The power loss in the MMC leg is given by

$$P_{loss} = 2R(i^2_{t_{rms}} + i^2_{cm_{rms}}) \tag{2.68}$$

As P_{loss} is very small compared to P, and $i_{cm_{rms}}$ is not known a priori, for an approximate calculation, P_{loss} can be calculated taking into account only $i_{t_{rms}}$.

Eliminating i_{cm} between (2.66) and (2.65) and solving the integrals results

$$\begin{aligned} i'_{cm} = & \\ & k_{cm}\left(\frac{\widehat{I_{cm}}}{4\widehat{m}^2} + \frac{2R\omega C\widehat{I_{cm}}}{M\widehat{m}^2} + \frac{\widehat{I_{cm}}}{6}\right)cos(2\omega t + \varphi) \\ & + k_{cm}\left(\frac{I^0_{cm}}{4}\right)cos(2\omega t + 2\theta) \\ & + k_{cm}\left(\frac{\widehat{I_{cm}}}{48}\right)cos(4\omega t + \varphi + 2\theta) \\ & - k_{cm}\left(\frac{4R\omega^2 C}{M\widehat{m}^2} + \frac{\omega\widehat{I_{cm}}sin(\varphi)}{4}\right)t \\ & - k_{cm}\left(\frac{\omega^2 I^0_{cm}}{2\widehat{m}^2}\right)t^2 \end{aligned} \tag{2.69}$$

where

$$k_{cm} = \frac{M\widehat{m}^2}{4\omega^2 LC} \tag{2.70}$$

Eliminating i'_{cm} between (2.63), (2.64), and (2.69) yields the full equation for i_{cm} given by

$$\begin{aligned} i_{cm} = & \\ & k_{cm}\left(\frac{\widehat{I_{cm}}}{4\widehat{m}^2} + \frac{2R\omega C\widehat{I_{cm}}}{M\widehat{m}^2} + \frac{\widehat{I_{cm}}}{6}\right)cos(2\omega t + \varphi) \\ & - k_{cm}\left(\frac{3\widehat{I}}{16\widehat{m}}\right)cos(2\omega t + \varphi + \theta) \\ & + k_{cm}\left(\frac{I^0_{cm}}{4}\right)cos(2\omega t + 2\theta) \\ & + k_{cm}\left(\frac{\widehat{I_{cm}}}{48}\right)cos(4\omega t + \varphi + 2\theta) \\ & - k_{cm}\left[\frac{4R\omega^2 C}{M\widehat{m}^2} + \frac{\omega\widehat{I_{cm}}sin(\varphi)}{4}\right. \\ & \left. + \frac{\widehat{I}\omega sin(\varphi - \theta)}{4\widehat{m}} - \frac{2v_{dc}C\omega^2}{M\widehat{m}^2}\right]t \\ & - k_{cm}\left[\frac{I^0_{cm}\omega^2}{2\widehat{m}^2} + \frac{\widehat{I}\omega^2 cos(\varphi - \theta)}{8\widehat{m}}\right]t^2 \end{aligned} \tag{2.71}$$

which can be expressed as the superposition of a second harmonic component $(i_{cm})_2$, a fourth harmonic component $(i_{cm})_4$, a ramp component $(i_{cm})_{ramp}$, and a parabolic component $(i_{cm})_{parab}$:

$$i_{cm} = (i_{cm})_2 + (i_{cm})_4 + (i_{cm})_{ramp} + (i_{cm})_{parab} \tag{2.72}$$

where

$$\begin{aligned}(i_{cm})_2 = \\ & k_{cm}\left(\frac{\widehat{I_{cm}}}{4\widehat{m}^2} + \frac{2R\omega C\widehat{I_{cm}}}{M\widehat{m}^2} + \frac{\widehat{I_{cm}}}{6}\right)cos(2\omega t + \varphi) \\ & - k_{cm}\left(\frac{3\widehat{I}}{16\widehat{m}}\right)cos(2\omega t + \varphi + \theta) \\ & + \left(\frac{{I_{cm}}^0}{4}\right)cos(2\omega t + 2\theta)\end{aligned} \tag{2.73}$$

$$(i_{cm})_4 = k_{cm}\left(\frac{\widehat{I_{cm}}}{48}\right)cos(4\omega t + \varphi + 2\theta) \tag{2.74}$$

$$\begin{aligned}(i_{cm})_{ramp} = \\ & - k_{cm}\left[\frac{4R\omega^2 C}{M\widehat{m}^2} + \frac{\omega\widehat{I_{cm}}sin\varphi}{4}\right. \\ & \left. + \frac{\widehat{I}\omega sin(\varphi - \theta)}{4\widehat{m}} - \frac{2v_{dc}C\omega^2}{M\widehat{m}^2}\right]t\end{aligned} \tag{2.75}$$

$$(i_{cm})_{parab} = -k_{cm}\left[\frac{\omega^2 I_{cm}^0}{2\widehat{m}^2} - \frac{\widehat{I}\omega^2 cos(\varphi - \theta)}{8\widehat{m}}\right]t^2 \tag{2.76}$$

For a stable system, the ramp (2.75) and parabolic (2.76) terms must be cancelled by the ramp and parabolic terms generated by the ac-side terminal current, i_t. This cancelling is indeed observed in the simulation of stable systems. Thus, the ramp and parabolic terms are disregarded, for now, if the system is assumed stable.

Let

$$(i_{cm})_2 = \widehat{I_{cm}}cos(2\omega t + \varphi_2) \tag{2.77}$$

and

$$(i_{cm})_4 = \widehat{I_{cm4}}cos(4\omega t + \varphi_4) \tag{2.78}$$

thus

$$\begin{aligned}&\widehat{I_{cm}}cos(2\omega t+\varphi_2)=\\&k_{cm}\left(\frac{\widehat{I_{cm}}}{4\widehat{m}^2}+\frac{2R\omega C\widehat{I_{cm}}}{M\widehat{m}^2}+\frac{\widehat{I_{cm}}}{6}\right)cos(2\omega t+\varphi)\\&-k_{cm}\left(\frac{3\widehat{I}}{16\widehat{m}}\right)cos(2\omega t+\varphi+\theta)\\&+\left(\frac{{I_{cm}}^0}{4}\right)cos(2\omega t+2\theta)\end{aligned} \tag{2.79}$$

and

$$\widehat{I_{cm4}}cos(4\omega t+\varphi_4)=k_{cm}\left(\frac{\widehat{I_{cm}}}{48}\right)cos(4\omega t+\varphi+2\theta) \tag{2.80}$$

Equation (2.80) is used to calculate $\widehat{I_{cm4}}$, if $\widehat{I_{cm}}$ is known.

Taking into account only the second harmonic component, (2.73), the respective amplitude can be represented by the following geometric series

$$\widehat{I_{cm}}=\sum_{n=0}^{\infty}a_2{z_2}^n=a_2z_2^0+a_2z_2^1+a_2z_2^2+...+a_2z_2^n \tag{2.81}$$

where a_2 is a constant, and z_2 is the series ratio.

Since the angle θ is known to be small, the following steps where calculated assuming $\theta\approx 0$, and $\varphi_2\approx\varphi$. Thus, (2.73) is rewritten to

$$\begin{aligned}{(i_{cm})}_2&=k_{cm}\left(\frac{\widehat{I_{cm}}}{4\widehat{m}^2}+\frac{\widehat{I_{cm}}}{6}-\frac{3\widehat{I}}{16\widehat{m}}\right)cos(2\omega t+\varphi)\\&+k_{cm}\left(\frac{{I_{cm}}^0}{4}\right)cos(2\omega t)\end{aligned} \tag{2.82}$$

Let

$$C_1=\frac{1}{4\widehat{m}^2}+\frac{1}{6} \tag{2.83}$$

$$C_2=\frac{3\widehat{I}}{16\widehat{m}} \tag{2.84}$$

$$C_3=\frac{{I_{cm}}^0}{4} \tag{2.85}$$

then

$$\begin{aligned}{(i_{cm})}_2&=k_{cm}\left(\widehat{I_{cm}}C_1-C_2\right)cos(2\omega t+\varphi)\\&+k_{cm}C_3cos2\omega t\end{aligned} \tag{2.86}$$

Grouping the terms in (2.86) in the same axis in the plane that Fig. 2.7 illustrates, results

$$(i_{cm})_2 = k_{cm}\left[\left(\widehat{I}_{cm}C_1 - C_2\right) + (C_3 cos\varphi)\right] cos(2\omega t + \varphi) \tag{2.87}$$

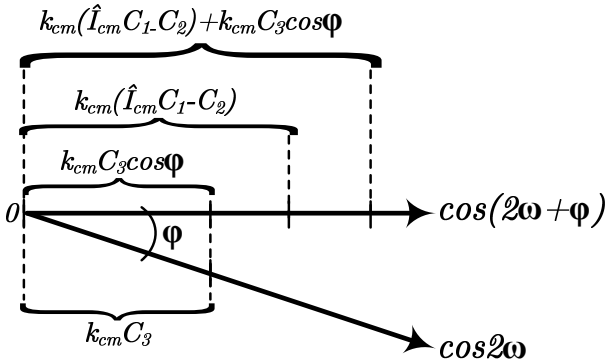

Figure 2.7: Grouping of the terms in (2.86) in the same axis.

Separating the constant terms from the iterative terms in (2.87) yields

$$\begin{aligned}(i_{cm})_2 &= \widehat{I}_{cm}cos(2\omega t + \varphi) \\ &= k_{cm}[(C_3 cos\varphi - C_2) + (\widehat{I}_{cm}C1)]cos(2\omega t + \varphi)\end{aligned} \tag{2.88}$$

Taking into account only the function magnitude, $\widehat{I}_{cm}$ results

$$\widehat{I}_{cm} = k_{cm}[(C_3 cos\varphi - C_2) + (\widehat{I}_{cm}C1)] \tag{2.89}$$

The term a_2 is the initial term of the series, when the exponent is zero, as it can be observed in (2.81). In (2.89), the first term of the series is found when $\widehat{I}_{cm} = 0$, or $a_2 = C_3 cos\varphi - C_2$. The series *ratio*, z_2, is given by the term that changes in every increment of n, or $z_2 = \widehat{I}_{cm}C1$. Thus, the circulating current magnitude geometric series is given by

$$\begin{aligned}\widehat{I}_{cm} &= k_{cm}\sum_{n=0}^{\infty}(C_3 cos\varphi - C_2)(\widehat{I}_{cm}C1)^n \\ &= k_{cm}\Big[(C_3 cos\varphi - C_2)(\widehat{I}_{cm}C1)^0 \\ &+ (C_3 cos\varphi - C_2)(\widehat{I}_{cm}C1)^1 \\ &+ ... + (C_3 cos\varphi - C_2)(\widehat{I}_{cm}C1)^n\Big]\end{aligned} \tag{2.90}$$

If the system is stable, the second component geometric series, represented by (2.90), converges, and its convergence value is given by, [79]

$$\widehat{I_{cm}} = a_2 \frac{1}{1 - z_2} \tag{2.91}$$

Thus, the convergence of (2.90) can be calculated by

$$\widehat{I_{cm}} = k_{cm}(C_3 cos\varphi - C_2)\frac{1}{1 - k_{cm}C_1} \tag{2.92}$$

If the series (2.90) converges, the system is stable. Also, the ramp and parabolic terms observed in (2.71) must be zero for the system to be stable. Thus, for a stable system the following three conditions must be satisfied.

$$\begin{cases} (i_{cm})_{ramp} = 0 \\ (i_{cm})_{parab} = 0 \\ |k_{cm}C_1| < 1 \end{cases} \tag{2.93}$$

The amplitude of the fourth harmonic in the circulating current, is very small in comparison to the second harmonic, as it can be observed in (2.80). Therefore, the fourth harmonic is neglected in this thesis.

2.3.2 Capacitor voltage harmonic components calculation

The submodule capacitor voltage is given by the integration of the arm current in each SM, as (2.29) and (2.30) show. Therefore, the voltage in the submodule capacitor has a contribution from the ac-side terminal current and from the circulating current.

Combining (2.29), (2.30), (2.19), (2.52), and (2.66), the submodule capacitor voltage in the upper arm is calculated as follows

$$\begin{aligned} {v_{C1}}^{i_t} + {v_{C1}}^{i_{cm}} &= \\ v_{C1} &= \\ & k_c\left[(\widehat{I} + \widehat{I_{cm}}\widehat{m})cos(\varphi) - 2\widehat{m}I^0_{cm}\right] sin(\omega t) \\ & - k_c\left[(\widehat{I} + \widehat{I_{cm}}\widehat{m})sin(\varphi)\right] cos(\omega t) \\ & - k_c\left(\frac{\widehat{I}\widehat{m}}{4} + \widehat{I_{cm}}\right) sin(2\omega t + \varphi) \\ & + k_c\left(\frac{\widehat{I_{cm}}\widehat{m}}{3}\right) sin(3\omega t + \varphi) \\ & - k_c\left(\frac{\widehat{I}\widehat{m}}{4} + \frac{\widehat{I_{cm}}\widehat{m}^2}{4}\right) sin(\varphi) \end{aligned} \tag{2.94}$$

where

$$k_c = \frac{1}{4\omega C} \tag{2.95}$$

It can be concluded from (2.94) that the submodule capacitor voltage is heavily based on harmonic components up to the third order. After that, the other components contribute with very little or nothing. Furthermore, the submodule capacitor voltage has the contribution of the circulating current on the first, second, and third harmonic components. This explains why the submodule capacitor voltage variation decreases when the circulating current is driven to zero by the CCSC.

Following the same logic used to calculate (2.94) for the upper arm, the submodule capacitor voltage in the lower arm is given by

$$\begin{aligned}
{v_{C2}}^{i_t} + {v_{C2}}^{i_{cm}} &= \\
v_{C2} &= \\
-k_c &\left[\left(\widehat{I} + \widehat{I}_{cm}\widehat{m}\right) cos(\varphi) + 2\widehat{m}I_{cm}^{0}\right] sin(\omega t) \\
&+ k_c \left[\left(\widehat{I} + \widehat{I}_{cm}\widehat{m}\right) sin(\varphi)\right] cos(\omega t) \\
&- k_c \left(\frac{\widehat{I}\widehat{m}}{4} + \widehat{I}_{cm}\right) sin(2\omega t + \varphi) \\
&- k_c \left(\frac{\widehat{I}_{cm}\widehat{m}}{3}\right) sin(3\omega t + \varphi) \\
&- k_c \left(\frac{\widehat{I}\widehat{m}}{4} + \frac{\widehat{I}_{cm}\widehat{m}^2}{4}\right) sin(\varphi)
\end{aligned} \tag{2.96}$$

2.3.3 Arm voltage harmonic components calculation

Eliminating n_r (for $r = 1$) and v_{C1} between (2.19), (2.31), and (2.94) results in the upper arm voltage

$$\begin{aligned} v_1 = & \\ & k_{arm}\left[\widehat{I}\left(1+\frac{\widehat{m}^2}{8}\right)+\widehat{I}_{cm}\left(\frac{3\widehat{m}}{2}\right)\right]sin(\omega t+\varphi) \\ & -k_{arm}\left(2I_{cm}^0\widehat{m}\right)sin(\omega t) \\ & -k_{arm}\left[\widehat{I}\left(\frac{3\widehat{m}}{4}\right)\widehat{I}_{cm}\left(\frac{2\widehat{m}^2}{3}+1\right)\right]sin(2\omega t+\varphi) \\ & -k_{arm}\left(I_{cm}^0\widehat{m}^2\right)sin(2\omega t) \\ & k_{arm}\left[\widehat{I}\left(\frac{\widehat{m}^2}{8}\right)+\widehat{I}_{cm}\left(\frac{5\widehat{m}}{6}\right)\right]sin(3\omega t+\varphi) \\ & -k_{arm}\left[\widehat{I}_{cm}\left(\frac{\widehat{m}^2}{6}\right)\right]sin(4\omega t+\varphi) \end{aligned} \tag{2.97}$$

where

$$k_{arm} = \frac{M}{8\omega C} \tag{2.98}$$

Equation (2.97) must be completed with the previously derived equation for the arm voltage fundamental component, (2.21), for v_1 in Section 2.2.1. Thus, a complete set of equations describing the arm voltages are

$$\begin{aligned} v_1 = & \\ & k_{arm}\left[\widehat{I}\left(1+\frac{\widehat{m}^2}{8}\right)\widehat{I}_{cm}\left(\frac{3\widehat{m}}{2}\right)\right]sin(\omega t+\varphi) \\ & -k_{arm}\left(2I_{cm}^0\widehat{m}\right)sin(\omega t) \\ & -k_{arm}\left[\widehat{I}\left(\frac{3\widehat{m}}{4}\right)\widehat{I}_{cm}\left(\frac{2\widehat{m}^2}{3}+1\right)\right]sin(2\omega t+\varphi) \\ & -k_{arm}\left(I_{cm}^0\widehat{m}^2\right)sin(2\omega t) \\ & +k_{arm}\left[\widehat{I}\left(\frac{\widehat{m}^2}{8}\right)+\widehat{I}_{cm}\left(\frac{5\widehat{m}}{6}\right)\right]sin(3\omega t+\varphi) \\ & -k_{arm}\left[\widehat{I}_{cm}\left(\frac{\widehat{m}^2}{6}\right)\right]sin(4\omega t+\varphi) \\ & +\frac{v_{dc}}{2}+k_{arm}\left(\widehat{m}\frac{v_{dc}}{2}\right)cos(\omega t+\theta) \end{aligned} \tag{2.99}$$

Table 2.1: Circulating current, submodule capacitor voltage, and arm voltage harmonic components amplitudes

Harmonic order	$\widehat{I}_{cm}$	$\widehat{v}_{Cr}$	$\widehat{v}_r$
0	$\frac{P+P_{loss}}{3V_{dc}}$	$\overline{v_c} - k_c\left(\frac{\widehat{I}\widehat{m}}{4} + \frac{\widehat{I}_{cm}\widehat{m}^2}{4}\right)sin\varphi$	$\frac{v_{dc}}{2}$
1	0	$k_c\sqrt{(C_6 cos\varphi - C_7)^2 + (C_6 sin\varphi)^2}$	$\sqrt{(k_{arm}C_4 sin\varphi + C_5)^2 + [k_{arm}(C_4 cos\varphi - 2I^0_{cm}\widehat{m})]^2}$
2	$k_{cm}(C_3 cos\varphi - C_2)\frac{1}{1-k_{cm}C_1}$	$-k_c\left(\frac{\widehat{I}\widehat{m}}{4} + \widehat{I}_{cm}\right)$	$-k_{arm}\sqrt{(C_8 cos\varphi - C_9)^2 + (C_8 sin\varphi)^2}$
3	0	$k_c\left(\frac{\widehat{I}_{cm}\widehat{m}}{3}\right)$	$k_{arm}\left[\widehat{I}\left(\frac{\widehat{m}^2}{8}\right) + \widehat{I}_{cm}\left(\frac{5\widehat{m}}{6}\right)\right]$
4	$\frac{\widehat{I}_{cm}}{48}$	0	$-k_{arm}\left[\widehat{I}_{cm}\left(\frac{\widehat{m}^2}{6}\right)\right]$

$$
\begin{aligned}
v_2 = & \\
& - k_{arm}\left[\widehat{I}\left(1 + \frac{\widehat{m}^2}{8}\right)\widehat{I}_{cm}\left(\frac{3\widehat{m}}{2}\right)\right] sin(\omega t + \varphi) \\
& + k_{arm}\left(2I^0_{cm}\widehat{m}\right) sin(\omega t) \\
& - k_{arm}\left[\widehat{I}\left(\frac{3\widehat{m}}{4}\right)\widehat{I}_{cm}\left(\frac{2\widehat{m}^2}{3} + 1\right)\right] sin(2\omega t + \varphi) \\
& - k_{arm}\left(I^0_{cm}\widehat{m}^2\right) sin(2\omega t) \\
& - k_{arm}\left[\widehat{I}\left(\frac{\widehat{m}^2}{8}\right) + \widehat{I}_{cm}\left(\frac{5\widehat{m}}{6}\right)\right] sin(3\omega t + \varphi) \\
& - k_{arm}\left[\widehat{I}_{cm}\left(\frac{\widehat{m}^2}{6}\right)\right] sin(4\omega t + \varphi) \\
& + \frac{v_{dc}}{2} - k_{arm}\left(\widehat{m}\frac{v_{dc}}{2}\right) cos(\omega t + \theta)
\end{aligned}
\tag{2.100}
$$

Table 2.1 presents a summary of the equations giving the magnitudes of the harmonic components in the circulating current, submodule capacitor voltages, and arm voltages.

The magnitudes in Table 2.1 are calculated based on the following parameters for i_{cm}

$$
\begin{aligned}
k_{cm} &= \frac{M\widehat{m}^2}{4\omega^2 LC} \\
C_1 &= \frac{1}{4\widehat{m}^2} + \frac{1}{6} \\
C_2 &= \frac{3\widehat{I}}{16\widehat{m}} \\
C_3 &= \frac{{I_{cm}}^0}{4}
\end{aligned}
\tag{2.101}
$$

, for v_{Cr}

$$
\begin{aligned}
k_c &= \frac{1}{4\omega C} \\
C_6 &= \widehat{I} + \widehat{I_{cm}}\widehat{m} \\
C_7 &= 2\widehat{m}I_{cm}^0
\end{aligned}
\tag{2.102}
$$

, and for v_r

$$
\begin{aligned}
k_{arm} &= \frac{M}{8\omega C} \\
C_4 &= \widehat{I}\left(1 + \frac{\widehat{m}^2}{8}\right) + \widehat{I_{cm}}\left(\frac{3\widehat{m}}{2}\right) \\
C_5 &= \frac{\widehat{m}v_{dc}}{2} \\
C_8 &= \widehat{I}\left(\frac{3\widehat{m}}{4}\right) + \widehat{I_{cm}}\left(\frac{2\widehat{m}^2}{3} + 1\right) \\
C_9 &= I_{cm}^0\widehat{m}^2
\end{aligned}
\tag{2.103}
$$

2.3.4 Modulating function calculation

In this subsection, initially, the injection of circulating current is not taken into account. Therefore, when the CCSC is enabled, the amplitude of the circulating current is assumed to be zero. On the other hand, if the CCSC is disabled, the amplitude of the circulating current assumes its natural magnitude given by the convergence of the geometric series described in Section 2.3.1.

It can be observed from Table 2.1, and in (2.101) through (2.103), that the modulation index, $\widehat{m}$, is a parameter that impacts all harmonic amplitudes. Thus, the more accurate its estimation, the closer to reality the calculated harmonic amplitudes are. In Section 2.2.1, (2.24) was used to estimate the modulation index (flat estimation). However, a more detailed analysis showed that (2.24), in closed-loop systems, where the modulation index is given by the combination of the ac-side terminal current control and the CCSC [30], its magnitude does not follow the estimated trend.

A more accurate way of calculating the steady-state value of the modulation index, is to assume a known ac-side terminal current, kept constant by its compensator [10], and apply KVL as illustrated in Figure 2.8, where $\vec{i}_t$, $\vec{e}_t$ and $\vec{v}_g$ are the phasors of the ac-side terminal current, the inner voltage, and the grid voltage, and $\widehat{e_t}$ and $\widehat{v_g}$, are the peak values of the inner voltage and the grid voltage, respectively.

Analysing only the fundamental component of the arm voltages, the resultant $\vec{e}_t$ calculated applying KVL on the circuit presented in Figure 2.8, can be equate to (2.18), which yields

$$
\begin{aligned}
\widehat{m}\frac{v_{dc}}{2}cos(\omega t + \theta) &= \widehat{e_t}cos(\omega t + \delta) \\
\widehat{m}\frac{v_{dc}}{2}(cos\theta cos\omega t - sin\theta sin\omega t) &= \widehat{e_t}(cos\delta cos\omega t - sin\delta sin\omega t)
\end{aligned}
\tag{2.104}
$$

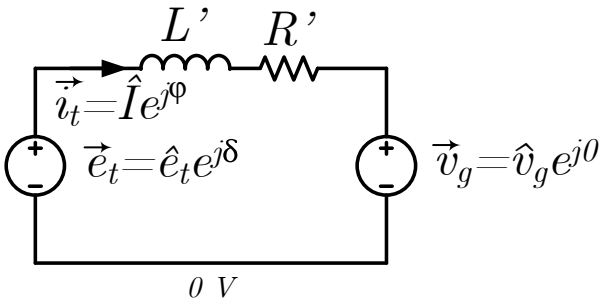

Figure 2.8: Simplified circuit representing the inner voltage phasor $\vec{e}_t$.

Solving for $\hat{m}$ and considering only the cosine component of (2.104) yields

$$\widehat{m} = \frac{2\widehat{e_t}cos\delta}{v_{dc}cos\theta} \tag{2.105}$$

It can be observed that in (2.105), the modulating function angle, θ, is no longer considered zero.

However, the modulating function calculated by (2.104) does not contemplate the contribution of the circulating current in the arm voltages, and consequently, in the magnitude and angle of the modulating function. Thus, a new method for calculating the modulation index and the angle of the modulating function is needed.

The angle of the modulating function, θ, can be calculated using the parabolic term from i_{cm}, (2.76). Assuming that the parabolic term must be cancelled in a stable system, yields

$$-k_{cm}\left(\frac{\omega^2 I_{cm}^0}{2\widehat{m}^2} - \frac{\widehat{I}\omega^2 cos(\varphi-\theta)}{8\widehat{m}}\right) = 0 \tag{2.106}$$

Solving for θ results

$$\theta = acos\left(\frac{4I_{cm}^0}{\widehat{m}\widehat{I}}\right) - \varphi \tag{2.107}$$

In (2.107) the modulating function angle is still dependant on $\widehat{m}$, so another equation that relates both parameters, $\widehat{m}$ and θ, must be derived. In a balanced converter, with equal values of L and R in both arms, the upper arm voltage and the lower arm voltage are equal in magnitude, with the only difference being the signal of the odd harmonics, as shown in (2.94) and (2.97). Thus,

$$(v_1)_1 = \widehat{e_t}cos\delta \tag{2.108}$$

Substituting the cosine component of the magnitude of the fundamental harmonic, presented in Table 2.1 into (2.108) yields

$$\begin{aligned} &-\frac{M\widehat{I}sin\varphi}{8\omega C} - \frac{M\widehat{I}\widehat{m}^2 sin\varphi}{64\omega C} \\ &-\frac{0.9M\widehat{I_{cm}}\widehat{m}sin\varphi}{8\omega C} + \frac{v_{dc}}{2} = \widehat{e_t}cos\delta \end{aligned} \tag{2.109}$$

Isolating the term containing $\widehat{I_{cm}}$ and simplifying (2.109) results

$$\begin{aligned} -0.9M\widehat{m}sin\varphi\widehat{I_{cm}} = {} & M\widehat{I}sin\varphi \\ & + \frac{M\widehat{I}\widehat{m}^2 sin\varphi}{8} - 4\omega C v_{dc}\widehat{m} \\ & + 8\widehat{e_t}cos\delta\omega C \end{aligned} \tag{2.110}$$

Substituting the parameters from (2.101) into (2.92) yields

$$\widehat{I_{cm}} = \frac{1.5M\widehat{m}^2 I_{cm}^0 cos\varphi - 1.125\widehat{I}M\widehat{m}}{24\omega^2 LC - 1.5M - M\widehat{m}^2} \tag{2.111}$$

Eliminating $\widehat{I_{cm}}$ between (2.111) and (2.110), generates a polynomial function whose only variable is $\widehat{m}$. Depending on the operating condition of the MMC, e.g. CCSC enabled or disabled, and different values of active and reactive power, the polynomial function features different degrees, as Table 2.2 presents.

Table 2.2: Modulation index calculation

Case	$i_{cm} = 0$, CCSC activated	$Q = 0$	Polynomial degree	Polynomial
1	false	false	4 (Quartic)	$a\widehat{m}^4 + b\widehat{m}^3 + c\widehat{m}^2 + d\widehat{m} + e = 0$
2	false	true	3 (Cubic)	$b\widehat{m}^3 + c\widehat{m}^2 + d\widehat{m} + e = 0$
3	true	false	2 (Square)	$c\widehat{m}^2 + d\widehat{m} + e = 0$
4	true	true	1 (Linear)	$\widehat{m} = \frac{2\widehat{e_t}cos\delta}{v_{dc}cos\theta}$

In Table 2.2, *true* means that the statement in the column title is true, and *false* means the opposite.

In Table 2.2, the a, b, c, d, and e parameters are given by

$$\begin{aligned} a &= -\frac{M\hat{I}sin\varphi}{8} \\ b &= 4\omega C v_{dc} - 1.35MI^0 cmcos\varphi sin\varphi \\ c &= 3\omega^2 LC\hat{I}sin\varphi - 0.1875M\hat{I}sin\varphi - \frac{8\widehat{e_t}cos\delta\omega C}{cos\theta} \\ d &= 6\omega C v_{dc} - \frac{96\omega^3 LC^2 v_{dc}}{M} \\ e &= \frac{192\widehat{e_t}cos\delta\omega^3 LC^2}{Mcos\theta} + 24\omega^2 LC\hat{I}sin\varphi \\ &\quad - 1.5M\widehat{I}sin\varphi - \frac{12\widehat{e_t}cos\delta\omega C}{cos\theta} \end{aligned} \tag{2.112}$$

The parameters that differ from one case to the other are the ac-side terminal current angle φ, and the circulating current magnitude $\widehat{I_{cm}}$. When there is no reactive power being exchanged with the grid, $\varphi = 0$, the a term in the quartic polynomial function is cancelled, and a cubic polynomial function is formed. If the CCSC is enabled, $\widehat{I_{cm}} = 0$, (2.111) is equal to zero, and

the function becomes a quadratic polynomial function. When both φ and $\widehat{I_{cm}}$ are equal to zero, the reactive power is zero, and the CCSC is active, then the polynomial function becomes a linear function and the modulation index, $\widehat{m}$, is given by the equation presented in row 4 of Table 2.2.

The roots of the polynomial functions showed in Table 2.2 can be calculated using several methods, with varying accuracy. The method chosen in this thesis is the Newton-Raphson algorithm (NR), described in Section 2.3.4. The algorithm showed a fast conversion (less than 3 iterations), for an error of 0.01 and a flat start of $\widehat{m} = 1$. The NR is executed, first, for a $\theta = 0$, and then, after the solution is found, θ is updated using (2.107). This process is repeated for five times.

If the CCC is used, instead of a CCSC, there is an injected circulating current in the MMC leg, for operating region enlarging purposes [50]. In this case, (2.24) is used to calculate $\widehat{m}$.

Polynomial roots calculation using Newton-Raphson

Taking as example the polynomial in the first row of Table 2.2, the first step to calculate the solution, is to solve the polynomial for e, that is, separate the terms with exponents different than zero, from the constant term. Then, a function $f(\widehat{m})$ is created from the terms with exponents different than zero, such that, $f(\widehat{m}) = a\widehat{m}^4 + b\widehat{m}^3 + c\widehat{m}^2 + d\widehat{m}$. Thus, the solution for $f(\widehat{m})$, i.e., $\widehat{m}^*$, is such that $f(\widehat{m}^*) = -e$.

With $f(\widehat{m})$ created, a starting point is established, $\widehat{m}_0$. It must be pointed out that the starting point is an educated "guess", and is based on the knowledge one has about the process being investigated. In the case of the modulation index, $\widehat{m}_0 = 1$.

To test how far $\widehat{m}_0$ is from $\widehat{m}^*$, $\Delta f(\widehat{m})$ is calculated as

$$\Delta f(\widehat{m}) = f(\widehat{m}^*) - f(\widehat{m}_0) \tag{2.113}$$

The smaller the $\Delta f(\widehat{m})$, the better. However, a $\Delta f(\widehat{m})$ equal to zero may take a long time to be reached, or it may never happen. Therefore, a threshold must be created for the acceptance of $\Delta f(\widehat{m})$, and, consequently, $\widehat{m}$. Such threshold, or error, is represented, in this thesis, by ε.

If the value of $\Delta f(\widehat{m})$ is higher than ε, it means that $\widehat{m}_0$ is not an acceptable solution and must be changed by a value of $\Delta\widehat{m}$. The value of $\Delta\widehat{m}$ is found by, first, calculating the linearized function of $f(\widehat{m})$, i.e., $f'(\widehat{m})$, using Taylor Series (in this case, the first two terms are enough), around $\widehat{m}_0$, and then calculating the value of $\Delta\widehat{m}$ that gives $f'(\Delta\widehat{m}) = f(\widehat{m}^*)$. Thus,

$$\Delta\widehat{m} = \frac{f(\widehat{m}^*) - f(\widehat{m}_0)}{\frac{\partial f(\widehat{m}_0)}{\partial \widehat{m}}} = \frac{\Delta f(\widehat{m})}{\frac{\partial f(\widehat{m}_0)}{\partial \widehat{m}}} \tag{2.114}$$

The last step consists in adding $\Delta\widehat{m}$ to $\widehat{m}_0$ to find $\widehat{m}(k+1)$, where $k+1$ indicates that one iteration is complete. If $\Delta\widehat{m}$ is smaller or equal to ε, $\widehat{m}(k+1)$ is accepted as the solution for the modulation index.

Fig. 2.9 illustrates the process for the first iteration. The function $f(\widehat{m})$ shown in Fig. 2.9 is to be understood as an example to help illustrate the NR method, and not as a function with real parameters of a, b, c, and d.

For an iterative algorithm, (2.113) and (2.114) are changed to the more generic form of

$$\Delta f[\widehat{m}(k)] = f(\widehat{m}^*) - f[\widehat{m}(k)] \tag{2.115}$$

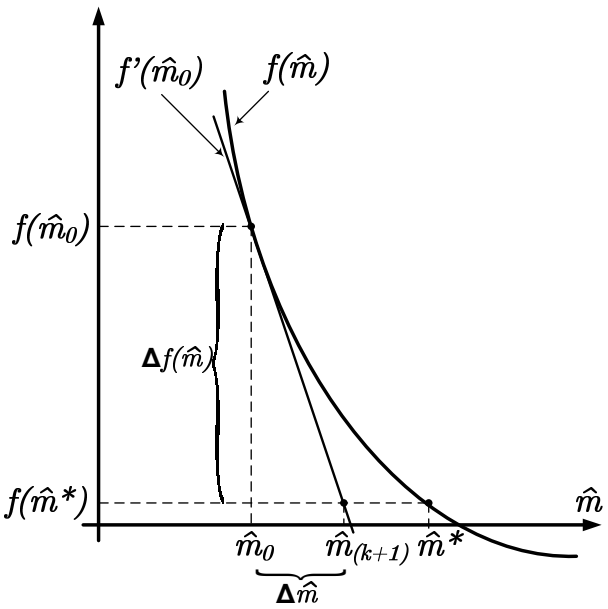

Figure 2.9: Newton-Raphson method illustration, first iteration.

and

$$\Delta\widehat{m}(k) = \frac{\Delta f[\widehat{m}(k)]}{\frac{\partial f[\widehat{m}(k)]}{\partial \widehat{m}}} \tag{2.116}$$

and $m(k+1) = m(k) + \Delta\widehat{m}(k)$.

Fig. 2.10 illustrates the NR algorithm for two iterations. In Fig. 2.10, the solution for $\widehat{m}$ is given by $\widehat{m}(k+2)$.

The equations presented in Table 2.1 combined with the modulating function calculation presented in Subsection 2.3.4, provide a complete steady-state harmonic model for the MMC, whose input parameters are $M, R, L, C, R_t, L_t, P, Q, v_{dc}, v_g$ and ω.

2.4 MMC component sizing

2.4.1 Proposed submodule capacitor sizing method

The method proposed in this section, takes into account the amplitude of the harmonic components of the submodule capacitor voltage for calculating the required submodule capacitance for a desired submodule capacitor voltage variation, Δv_c. Therefore, one can calculate the submodule capacitor voltage variation with the contribution of the circulating current, or without it, in case of an active CCSC, or CCC.

Table 2.1 shows that the even harmonic components are of negative-sequence (minus sign), whereas the odd harmonics are of positive sequence (positive sign). This indicates that the harmonic components, of the submodule capacitor voltage, align as Fig. 2.11 shows, assuming, for example, the following magnitudes: $(v_C)_1 = 0.3\ kV$, $(v_C)_2 = 0.24\ kV$, and $(v_C)_3 = 0.06\ kV$. In Fig. 2.11, the ac-side terminal current angle φ is set to zero.

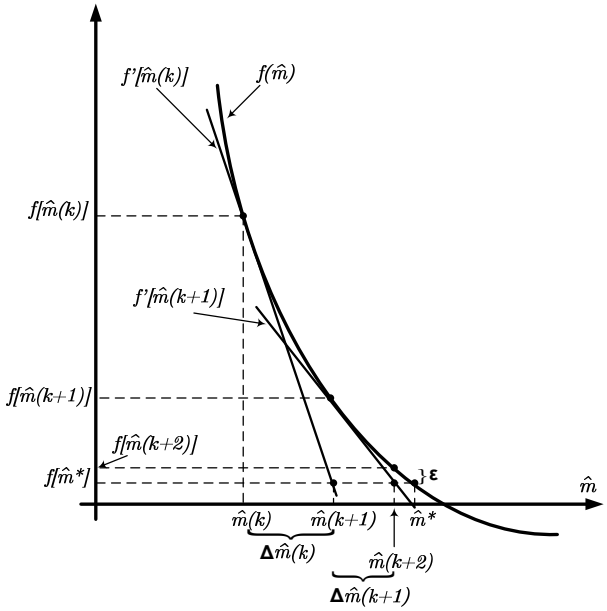

Figure 2.10: Newton-Raphson method illustration.

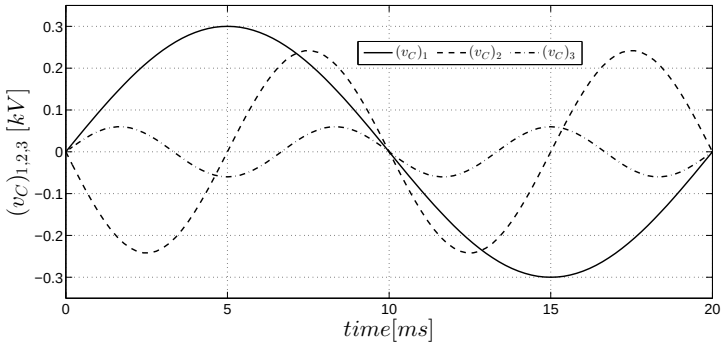

Figure 2.11: First, second, and third harmonic components in the submodule capacitor voltage for $\varphi = 0$.

The ac-side terminal current angle, φ, changes the position of the harmonic components in the submodule capacitor voltage. Figure 2.12 shows the position of the submodule capacitor voltage harmonic components for $\varphi = -30$ degrees.

The submodule capacitor voltage variation is given by the subtraction of the submodule capacitor voltage maximum and minimum values. However, in a function $v_C(t)$, given by,

$$v_C(t) = (v_C)_1(t) + (v_C)_2(t) + (v_C)_3(t) \tag{2.117}$$

where $(v_C)_1(t) = \widehat{v}_{C1} sin(\omega t + \delta_1)$, $(v_C)_2(t) = \widehat{v}_{C2} sin(2\omega t + \delta_2)$, and $(v_C)_3(t) = \widehat{v}_{C1} sin(3\omega t + \delta_3)$, the maximum and minimum values are troublesome to be calculated precisely, since $v_C(t)$ is a trigonometric function with three different frequencies. Therefore, approximate models for each harmonic component are proposed in this section, to facilitate the calculation of the maximum (peak) and minimum (trough) values in the submodule capacitor voltage. Thus, the submodule capacitor voltage harmonic components are split into positive half-cycle and negative half-cycle, taking as a middle point, an imaginary axis, e.g., at $t = 10\ ms$ in Fig. 2.11,

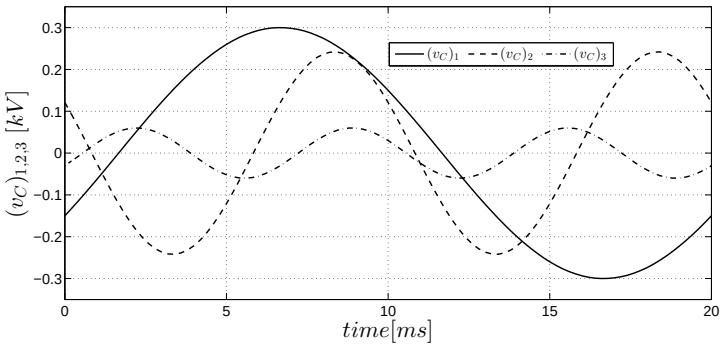

Figure 2.12: First, second, and third harmonic components in the submodule capacitor voltage for $\varphi = -30$ degrees.

with each half-cycle represented by a quadratic function, as follows:

$$\begin{aligned}
&(v_C)_{1p}(t) \approx \\
&\qquad \widetilde{(v_C)}_{1p}(t) = -\widehat{v}_{C1} a_1 (t - b_1 - d_1)^2 + \widehat{v}_{C1} \\
&(v_C)_{2p}(t) \approx \\
&\qquad \widetilde{(v_C)}_{2p}(t) = -\widehat{v}_{C2} a_2 (t - b_2 - d_2)^2 + \widehat{v}_{C2} \\
&(v_C)_{3p}(t) \approx \\
&\qquad \widetilde{(v_C)}_{3p}(t) = -\widehat{v}_{C3} a_3 (t - b_3 - d_3)^2 + \widehat{v}_{C3}
\end{aligned} \tag{2.118}$$

$$\begin{aligned}
&(v_C)_{1n}(t) \approx \\
&\qquad \widetilde{(v_C)}_{1n}(t) = -\widehat{v}_{C1} a_1 (t - b_1 + d_1)^2 + \widehat{v}_{C1} \\
&(v_C)_{2n}(t) \approx \\
&\qquad \widetilde{(v_C)}_{2n}(t) = -\widehat{v}_{C2} a_2 (t - b_2 + d_2)^2 + \widehat{v}_{C2} \\
&(v_C)_{3n}(t) \approx \\
&\qquad \widetilde{(v_C)}_{3n}(t) = -\widehat{v}_{C3} a_3 (t - b_3 + d_3)^2 + \widehat{v}_{C3}
\end{aligned} \tag{2.119}$$

Equation (2.118) represents the positive half-cycle of the voltage harmonic components, whereas (2.119) represents the negative half-cycle. Taking as an example $\widetilde{(v_C)}_{1p}(t)$, the instant when the voltage peak happens can be calculated from

$$\frac{d\widetilde{(v_C)}_{1p}(t)}{dt} = 0 \tag{2.120}$$

From (2.120), it becomes known that the peak of $\widetilde{(v_C)}_{1p}(t)$ occurs at b_1, assuming a $d_1 = 0$. Therefore, the parabola must be displaced by a quarter of a cycle, resulting in $b_1 = 1/(4 f_g)$ (i.e., $\pi/2$ in radians), in order to align with $(v_C)_1(t)$. Further, the roots of the parabola must be zero

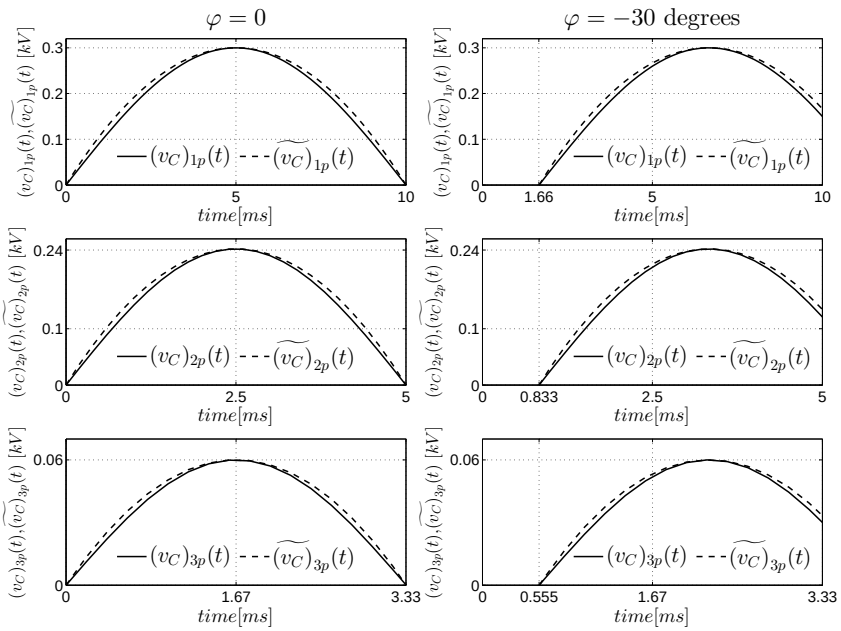

Figure 2.13: Approximate quadratic functions $(\widetilde{v_C})_{1p}(t)$, $(\widetilde{v_C})_{2p}(t)$, and $(\widetilde{v_C})_{3p}(t)$, in contrast with $(v_C)_{1p}(t)$, $(v_C)_{2p}(t)$, and $(v_C)_{3p}(t)$, for $\varphi = 0$ and $\varphi = -30$ degrees.

and $f_g/2$ (i.e., 0 and π in radians). Thus, solving the quadratic equation for the first root (zero), and solve for a_1, yields $a_1 = 1/b_1^2$. The last parameter, d_1, represents the displacement in the parabola caused by φ. Calculating the displacement, in seconds, caused by φ_r (φ in radians) yields $d_1 = \varphi_r/(2\pi f_g)$. The parameters a, b, and d for the second and third harmonics, are given, as a function of the first harmonic parameters, that is, $b_2 = b_1/2$, $b_3 = b_1/3$, $a_2 = 4a_1$, $a_3 = 9a_1$, $d_2 = d_1/2$, and $d_3 = d_1/3$. To facilitate the analysis, the negative half-cycle has been reflected to the positive side. Hence, all parabolas in (2.119) feature negative a parameters. Thus, the difference between the positive half-cycle and the negative half-cycle is only the direction of the displacement d, as it is observed in (2.118) and (2.119).

Figure 2.13 shows the positive half-cycle for the approximate quadratic functions for each submodule capacitor voltage harmonic component, in contrast with $(v_C)_{1p}(t)$, $(v_C)_{2p}(t)$, and $(v_C)_{3p}(t)$. In Fig. 2.13, the first column shows the functions for $\varphi = 0$, and the second column for $\varphi = -30$ degrees.

Let $\widetilde{v}_{Cp}(t) = (\widetilde{v_C})_{1p}(t) + (\widetilde{v_C})_{2p}(t) + (\widetilde{v_C})_{3p}(t)$, and $\widetilde{v}_{Cn}(t) = (\widetilde{v_C})_{1n}(t) + (\widetilde{v_C})_{2n}(t) + (\widetilde{v_C})_{3n}(t)$

then, working on $\widetilde{v}_{Cn}(t)$, for example, adding the similar terms and applying the multiplication distributive property, yields

$$\begin{aligned}\widetilde{v}_{Cn}(t) = {} & a_1(-\widehat{v}_{C1} - 4\widehat{v}_{C2} - 9\widehat{v}_{C3})t^2 \\ & + (2a_1b_1 - 2a_1d_1)(\widehat{v}_{C1} + 2\widehat{v}_{C2} + 3\widehat{v}_{C3})t \\ & + (2a_1b_1d_1 - a_1d_1^2)(\widehat{v}_{C1} + \widehat{v}_{C2} + \widehat{v}_{C3})\end{aligned} \tag{2.121}$$

Substituting the equations for a_1, b_1, and d_1 in (2.121) results

$$\begin{aligned}\widetilde{v}_{Cn}(t) = {} & 16 f_g^2(-\widehat{v}_{C1} - 4\widehat{v}_{C2} - 9\widehat{v}_{C3})t^2 \\ & + 8 f_g \left(1 - \frac{\varphi}{90}\right)(\widehat{v}_{C1} + 2\widehat{v}_{C2} + 3\widehat{v}_{C3})t \\ & + \frac{\varphi}{45}\left(1 - \frac{\varphi}{180}\right)(\widehat{v}_{C1} + \widehat{v}_{C2} + \widehat{v}_{C3})\end{aligned} \tag{2.122}$$

The instant at which $\widetilde{v}_{Cn}(t)$ reaches its peak, that is, t_n, is calculated by

$$\frac{d\widetilde{v}_{Cn}(t_n)}{dt} = 0 \tag{2.123}$$

Since the negative half-cycle has been reflected to the positive side, as stated earlier, t_n actually indicates the instant when the trough takes place for $\widetilde{v}_{Cn}(t)$.

Solving (2.123) for t_n results

$$t_n = \frac{1}{4 f_g}\left(-1 + \frac{\varphi}{90}\right)\frac{(\widehat{v}_{C1} + 2\widehat{v}_{C2} + 3\widehat{v}_{C3})}{(-\widehat{v}_{C1} - 4\widehat{v}_{C2} - 9\widehat{v}_{C3})} \tag{2.124}$$

A similar analysis yields the instant when $\widetilde{v}_{Cp}(t)$ reaches its peak, that is, t_p, given by

$$t_p = \frac{1}{4 f_g}\left(-1 - \frac{\varphi}{90}\right)\frac{(\widehat{v}_{C1} + 2\widehat{v}_{C2} + 3\widehat{v}_{C3})}{(-\widehat{v}_{C1} - 4\widehat{v}_{C2} - 9\widehat{v}_{C3})} \tag{2.125}$$

The numerator and the denominator of the fraction term in (2.124) and (2.125) both depend on k_c. Thus, cancelling k_c, and by extension C, from (2.124) and (2.125) yields

$$t_n = \frac{1}{4 f_g}\left(-1 + \frac{\varphi}{90}\right)\frac{(\widehat{v}'_{C1} + 2\widehat{v}'_{C2} + 3\widehat{v}'_{C3})}{(-\widehat{v}'_{C1} - 4\widehat{v}'_{C2} - 9\widehat{v}'_{C3})} \tag{2.126}$$

$$t_p = \frac{1}{4 f_g}\left(-1 - \frac{\varphi}{90}\right)\frac{(\widehat{v}'_{C1} + 2\widehat{v}'_{C2} + 3\widehat{v}'_{C3})}{(-\widehat{v}'_{C1} - 4\widehat{v}'_{C2} - 9\widehat{v}'_{C3})} \tag{2.127}$$

where $\widehat{v}'_{C1}$, $\widehat{v}'_{C2}$, and $\widehat{v}'_{C3}$ represent the amplitude of the first, second, and third harmonic components of the submodule capacitor voltage, calculated by Table 2.1 without multiplying by k_c, i.e., $\widehat{v}'_{C1} = \sqrt{(C_6 cos\varphi - C_7)^2 + (C_6 sin\varphi)^2}$.

The equivalent in radians of t_n and t_p, for the first harmonic, denoted by r_{n1} and r_{p1}, are

$$\begin{aligned} r_{p1} &= 2\pi f_g t_p \\ r_{n1} &= 2\pi f_g t_n \end{aligned} \tag{2.128}$$

The t_n and t_p equivalent in radians for the second and third harmonics are given as function of r_{n1} and r_{p1}. Thus, $r_{n2} = 2r_{n1}$, $r_{p2} = 2r_{p1}$, $r_{n3} = 3r_{n1}$, and $r_{p3} = 3r_{p1}$.

Figure 2.14 illustrates the submodule capacitor voltage harmonic components representation in the trigonometric plane at $t = t_p$. In Fig. 2.14 $\theta_1 = r_{p1} - \varphi_r$, $\theta_2 = r_{p2} - \varphi_r$, and

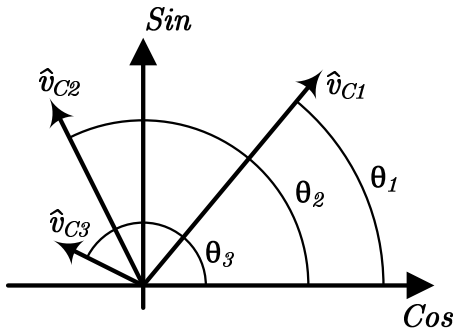

Figure 2.14: Submodule capacitor voltage harmonic components representation in the trigonometric plane at $t = t_p$.

$\theta_3 = r_{p3} - \varphi_r$. The maximum value in the positive half-cycle, i.e., at $t = t_p$, can be calculated by the sine components of the submodule capacitor voltage harmonics representation in the trigonometric plane, as follows.

$$\begin{aligned}\Delta\widetilde{(v_C)}_p = {} & \widehat{v}_{C1} sin(r_{p1} - \varphi_r) \\ & + \widehat{v}_{C2} sin(r_{p2} - \varphi_r) + \widehat{v}_{C3} sin(r_{p3} - \varphi_r)\end{aligned} \tag{2.129}$$

Similarly

$$\begin{aligned}\Delta\widetilde{(v_C)}_n = {} & \widehat{v}_{C1} sin(r_{n1} + \varphi_r) \\ & + \widehat{v}_{C2} sin(r_{n2} + \varphi_r) + \widehat{v}_{C3} sin(r_{n3} + \varphi_r)\end{aligned} \tag{2.130}$$

Thus, the submodule capacitor voltage variation is given by

$$\Delta\widetilde{v}_C = \Delta\widetilde{(v_C)}_p + \Delta\widetilde{(v_C)}_n \tag{2.131}$$

Joining the similar terms, yields

$$\begin{aligned}&\Delta\widetilde{v}_C = \frac{1}{4\omega C}\times \\ &\Big\{\widehat{v}_{C1}[cos\varphi(sinr_{n1} + sinr_{p1}) + sin\varphi(cosr_{n1} - cosr_{p1})]+ \\ &\widehat{v}_{C2}[cos\varphi(sin2r_{n1} + sin2r_{p1}) + sin\varphi(cos2r_{n1} - cos2r_{p1})]+ \\ &\widehat{v}_{C3}[cos\varphi(sin3r_{n1} + sin3r_{p1}) + sin\varphi(cos3r_{n1} - cos3r_{p1})]\Big\}\end{aligned} \tag{2.132}$$

Solving for C

$$C = \frac{1}{4\omega\Delta\widetilde{v}_C}(T_1 + T_2 + T_3) \tag{2.133}$$

where

$$T_1 = \widehat{v}_{C1} \times \left[cos\varphi(sinr_{n1} + sinr_{p1}) + sin\varphi(cosr_{n1} - cosr_{p1}) \right] \tag{2.134}$$

$$T_2 = \widehat{v}_{C2} \times \left[cos\varphi(sin2r_{n1} + sin2r_{p1}) + sin\varphi(cos2r_{n1} - cos2r_{p1}) \right] \tag{2.135}$$

$$T_3 = \widehat{v}_{C3} \times \left[cos\varphi(sin3r_{n1} + sin3r_{p1}) + sin\varphi(cos3r_{n1} - cos3r_{p1}) \right] \tag{2.136}$$

Equation (2.133) allows the calculation of the submodule capacitance, C, as a function of the desired $\Delta\widetilde{v}_C$, φ, and $\widehat{v}_{C1}$, $\widehat{v}_{C2}$, and $\widehat{v}_{C3}$. However, the calculation of $\widehat{v}_{C1}$, $\widehat{v}_{C2}$, and $\widehat{v}_{C3}$ depend themselves on C. Therefore, the method proposed in this thesis considers, at first, the amplitude of the circulating current, $\widehat{I}_{cm}$, as being zero, i.e., an active CCSC. After the calculation of C, then the contribution of $\widehat{I}_{cm}$ in $\Delta\widetilde{v}_C$ is calculated.

Capacitor Sizing Method for Injected Circulating Current

In the case of an injected circulating current, the control reference phase is shifted in such a way that the submodule capacitor voltage harmonic components align differently than shown in Fig. 2.11 and Fig. 2.12. Fig. 2.15 presents the alignment of the harmonic components of the submodule capacitor voltage for a injected circulating current, for $\varphi = 0$. It is noted that the harmonic component peaks align perfectly. More specifically, the second harmonic component have its peak added to the submodule capacitor voltage peak and subtracted from the trough. Thus, the second harmonic, is cancelled in the calculation of the submodule capacitor voltage variation. Then, the submodule capacitor voltage variation, for an injected circulating current, is given by

$$\Delta\widetilde{v}_C = \frac{2}{4\omega C}[\widehat{v}_{C1} + \widehat{v}_{C3}]cos\varphi \tag{2.137}$$

solving for C yields

$$C = \frac{2}{4\omega\Delta\widetilde{v}_C}[\widehat{v}_{C1} + \widehat{v}_{C3}]cos\varphi \tag{2.138}$$

Taking as an example, the HVDC system described in [22], for a desired $\Delta\widetilde{v}_C$ of 20% of $\overline{v}_c$ and an CCSC strategy based on [30], (2.133) yields an submodule capacitor of 8.4 mF.

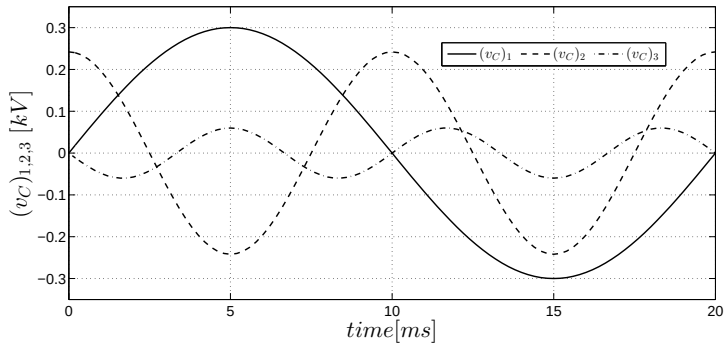

Figure 2.15: First, second, and third harmonics in the submodule capacitor voltage, for $\varphi = 0$, assuming an injected i_{cm}.

However, if the CCSC is disabled, (2.132) yields a $\Delta\widetilde{v_C}$ of 70% of $\overline{v}_c$. On the other hand, if the desired $\Delta\widetilde{v_C}$ is increased to 16.8% of $\overline{v}_c$, and the CCSC is enabled, the resultant capacitor is exactly the value selected in [22], i.e, $C = 10\ mF$.

The proposed method, in this thesis, for sizing the submodule capacitor is summarized on following steps.

1. Calculation of $\widehat{I}$, $\widehat{m}$, and I_{cm}^0 using (2.53), (2.24), and (2.67);
2. Calculation of C_6 and C_7 using (2.102), for $\widehat{I_{cm}} = 0$;
3. Calculation of $\widehat{v}_{C1}$, $\widehat{v}_{C2}$, and $\widehat{v}_{C3}$ using Table 2.1;
4. Calculation of t_p, t_n, r_{p1}, and r_{n1} using (2.126), (2.127), and (2.128);
5. Calculation of C for a designed $\Delta\widetilde{v_C}$ using (2.133).

If desired, the impact of $\widehat{I_{cm}}$ in the submodule capacitor voltage variation can be calculated by the extra following steps.

6. Calculation of $\widehat{m}$ following the method described in Section 2.3.4;
7. Calculation of $\widehat{I_{cm}}$ for $\widehat{m}$ calculated in the previous step;
8. Calculation of $\Delta\widetilde{v_C}$ using (2.132).

For an injected i_{cm}, $\widehat{I_{cm}}$ is known, and C can be calculated using (2.138).

Table 2.3 shows the resultant submodule selected capacitance, using the proposed method and three other methods ([15], [43], and [46]), for a three-phase MMC inverter. The inverter features 400 capacitors per arm, an arm reactor of 50 mH and 0.338 Ω, connected to an 192.3 kV (rms) ac grid (resultant from a line-to-line voltage of 333 kV) through a 60 mH, and 0.377 Ω, terminal reactor. The inverter is delivering to the ac grid an active power of 1000 MW, and absorbing a reactive power of 0 in the first moment, and 500 $MVAr$ in a second moment. The dc voltage is 640 kV and the submodule capacitor has a value of 10 mF. The control reference for the circulating current control was kept at zero for the first two columns. In the last column, a circulating current of 0.613 kA was injected in the MMC arm. The submodule capacitor

Table 2.3: Comparison between different methods for capacitor sizing assuming circulating current control *on*

Method	Calculated C [mF] for $\Delta v_C = 0.285$ [kV] and $Q = 0$ $MVAr$, $\widehat{I}_{cm} = 0$	Calculated C [mF] for $\Delta v_C = 0.346$ [kV] and $Q = 500$ $MVAr$, $\widehat{I}_{cm} = 0$	Calculated C [mF] for $\Delta v_C = 0.2$ kV and $Q = 0$ $MVAr$, $\widehat{I}_{cm} = 0.613$ kA
Proposed	10.1	10.1	9.65
Reference [46]	7.1	6.54	-
Reference [43]	9.1	7	-
Reference [15]	5.1	4.5	-

voltage variation was obtained by simulation of the aforementioned system. Therefore, the correct result for the submodule capacitor sizing method is 10 mF, and the result of each method is compared to this value, for the purpose of judging its accuracy.

Table 2.3 shows that the proposed submodule capacitor sizing method provides results closer to 10 mF, than those provided by the aforementioned methods, with errors of 1%, 1%, and 3.5%.

2.4.2 Arm inductor sizing based on leg current resonance

Once the submodule capacitor has been selected, the leg current resonance can be addressed by analysing the convergence of the circulating current geometric series in (2.90). The series convergence depends on the arm inductor, thus, assuming a maximum modulation index of 1, and solving the convergence condition in (2.93) for L, yields

$$L > \frac{2.5M}{24\omega^2 C} \tag{2.139}$$

Assuming that the instability of the converter is due to resonance between the arm equivalent capacitance and the arm inductance, then the condition presented in (2.139) is modified to

$$L_c \neq \frac{2.5M}{24\omega^2 C} \tag{2.140}$$

where L_c represents the critical value for the arm inductance where the resonance takes place. Thus, the arm inductance value must be different than L_c. Assuming that the MMC features a SM technology that does not allow a dc-side fault current to circulate in the leg (CDSM or FBSM), and that the CCSC is always active, the arm inductance, L, can be calculated only to filtrate the arm switching frequency, respecting the limitation given by (2.140).

2.5 Validation of the harmonic steady-state model

To test the proposed steady-state harmonic model, a back-to-back system, similar to the system presented in [18] and [20]-[22], was simulated in the PSCAD/EMTDC software environment [80]. The schematic diagram for this system is shown in Fig. 2.16. An *equivalent-circuit-based simulation model*, described in detail in Chapter 3, was created to simulate each MMC of the back-to-back system. Therefore, the mathematical equations that describe different variables

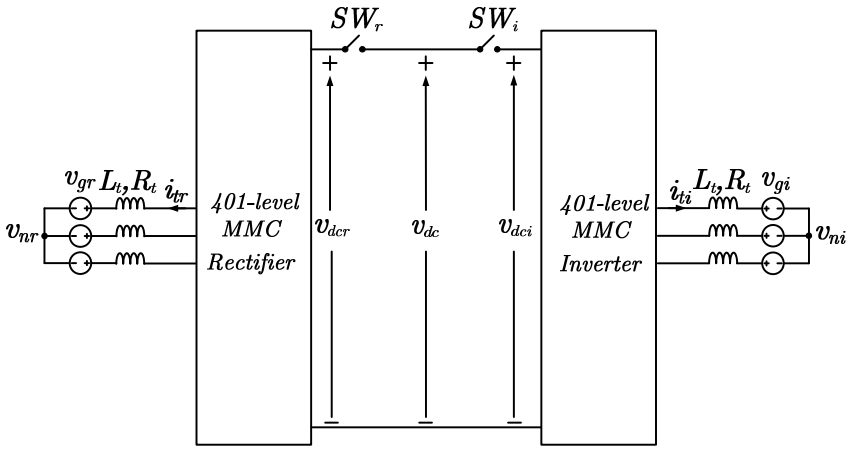

Figure 2.16: Schematic diagram of the back-to-back MMC HVDC system simulated.

of the MMCs were developed in a program and linked to the host circuit simulation software, i.e., PSCAD/EMTDC; the code, thus, generated the control signals for the dependent voltage sources. The validity and accuracy of the equivalent-circuit-based simulation model were first confirmed by comparing its dynamics with the dynamics of detailed models with different values of M (4, 6, 8, 10, 12, and 20). For clarity purposes, the electrical quantities were identified with the indexes i =inverter and r =rectifier. Also, the simulation model included a scheme for circulating current suppression [30], and schemes for ac-side terminal current control and dc-side voltage regulation [10]. The parameters for both MMCs are the same as described in Section 2.4.1, with the difference that the submodule capacitor assumed values from 10 to 40 mF, increased in steps of 2.5 mF, and the reactive power was regulated at 0, 300, and 500 $MVAr$, for some of the simulation cases.

Even though the proposed steady-state harmonic model and the submodule capacitor sizing method work for injected circulating current cases, only cases with enabled or disabled CCSC were considered in this section, due to space limitations. The simulation results involving the magnitude of harmonic components calculated by the proposed steady-state harmonic model, are considered the same in all arms of both MMCs, as they share the same parameters.

2.5.1 Submodule capacitor voltage variation

Figure 2.17 shows the dc-side voltage, the active power, and the ac-side terminal current in dq-frame, for the back-to-back system illustrated in Fig. 2.16.

In the beginning of the simulation, switches SW_i and SW_r are open and all compensators are disabled. In this state, the submodule capacitors pre-charge with energy drawn from the respective grid (v_{gr} for the rectifier and v_{gi} for the inverter). Then, at $t = 0.03$ s, the ac-side terminal current compensators, and the dc-side voltage regulators are enabled, and the dc-side voltage rises to the nominal voltage in both MMCs. At $t = 0.25$ s, both switches, SW_i and SW_r, are closed and the connection between the rectifier and the inverter is established. Still at $t = 0.25$ s, the dc-side voltage regulator in the rectifier is disabled, whereas this same regulator in the inverter is kept running. Thus, from this moment on, the rectifier controls the power exchange between v_{gr} and v_{gi}, whereas the inverter controls the dc-side voltage shared by both

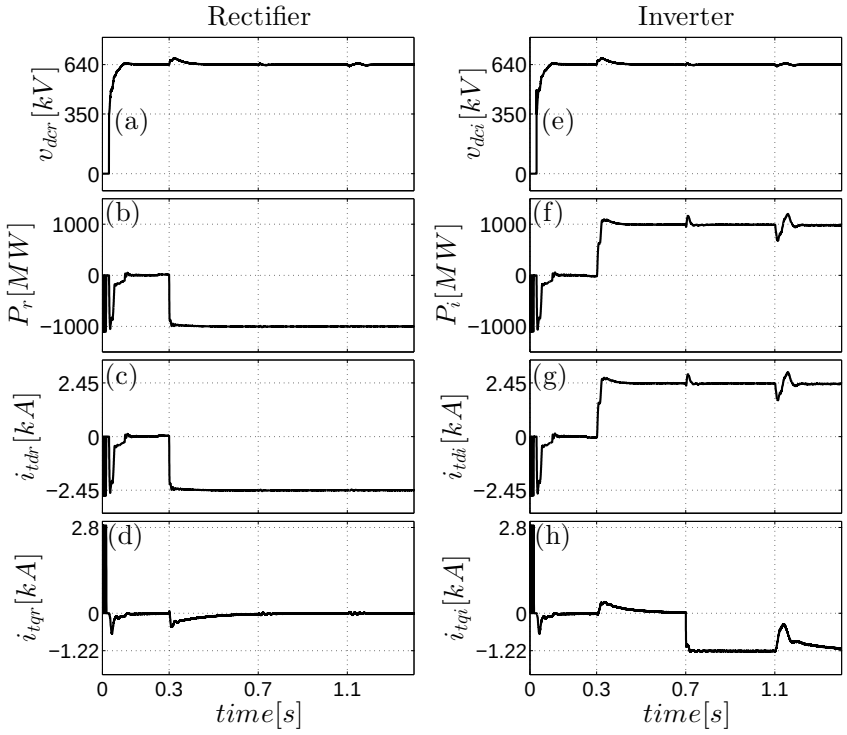

Figure 2.17: Voltages and currents for the back-to-back system illustrated in Fig. 2.16 submitted to different disturbances.

MMCs. Also, at this same moment, the control reference for the active power, P_r, and the reactive power, Q_r, are kept zero. Later, at $t = 0.3$ *s*, the active power control reference in the rectifier is changed to -1000 *MW*, generating a small transient in the dc-side voltage, a negative change in amplitude in i_{tdr}, and a positive change in i_{tdi}, as expected. Then, at $t = 0.7$ *s*, the reactive power control reference in the inverter is changed from zero to 500 *MVAr*, what makes the inverter absorb reactive power from v_{gi}. This change does not affect the rectifier, as observed in Fig. 2.17. Finally, at $t = 1.1$ *s*, the CCSC, in the inverter, is turned *off* and a considerable transient is observed in its ac-side terminal current *dq*-frame components. Again, the rectifier is not affected.

Figure 2.19 shows the circulating current, the submodule capacitor voltage (in capacitor 3 from the upper arm), and the ac-side terminal current for phase *a* in the rectifier and the inverter, for the afore mentioned disturbances. It can be observed in Fig. 2.18, that, as expected, i_{cmar}, v_{C3ar}, and i_{tar} are very little affected by the change in Q_i and CCSC in the inverter. On the other hand, the submodule capacitor voltage variation increased with the absorbtion of reactive power by the inverter, and, later, by the deactivation of the CCSC. The ac-side terminal current also increases with the increase of reactive power in the inverter, but its steady-state is not affected by the deactivation of CCSC, as Fig. 2.18 (f) shows. The submodule capacitor voltage variation for all disturbances, Figs. 2.18 (b) and (e), agree well with the model proposed in this chapter.

Figure 2.19 shows the calculated submodule capacitor voltage variation Δv_C, using the proposed method, and the comparison with the simulation of system illustrated in Fig. 2.16. In fig. 2.19, the submodule capacitance is changed from 10 to 40 *mF*, in steps of 2.5 *mF*, and the

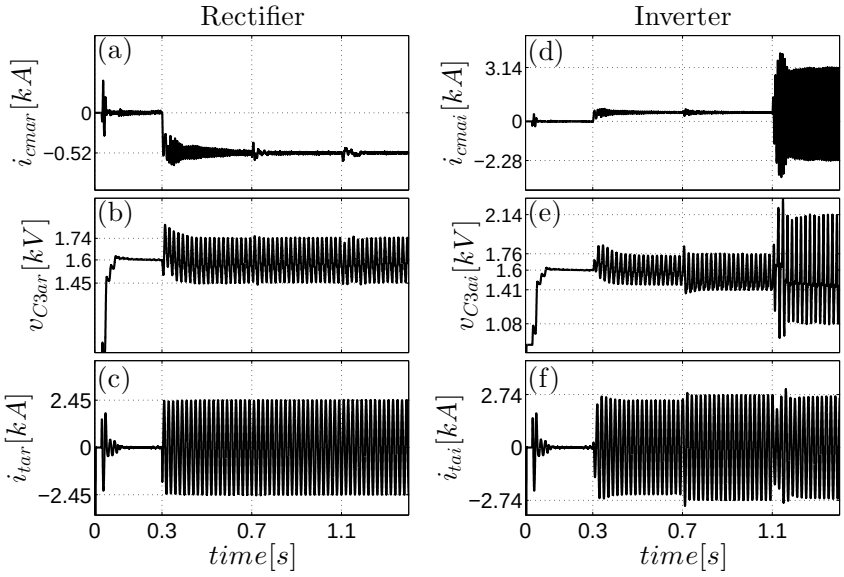

Figure 2.18: Circulating current, submodule capacitor voltage, and ac-side terminal current for the back-to-back system illustrated in Fig. (2.16) submitted to different disturbances.

reactive power assumes values of 0, 300, and 500 *MVAr*. Moreover, to further test the efficacy of the proposed model, the CCSC was turned *on* and *off* for every change in Q. As fig. 2.19

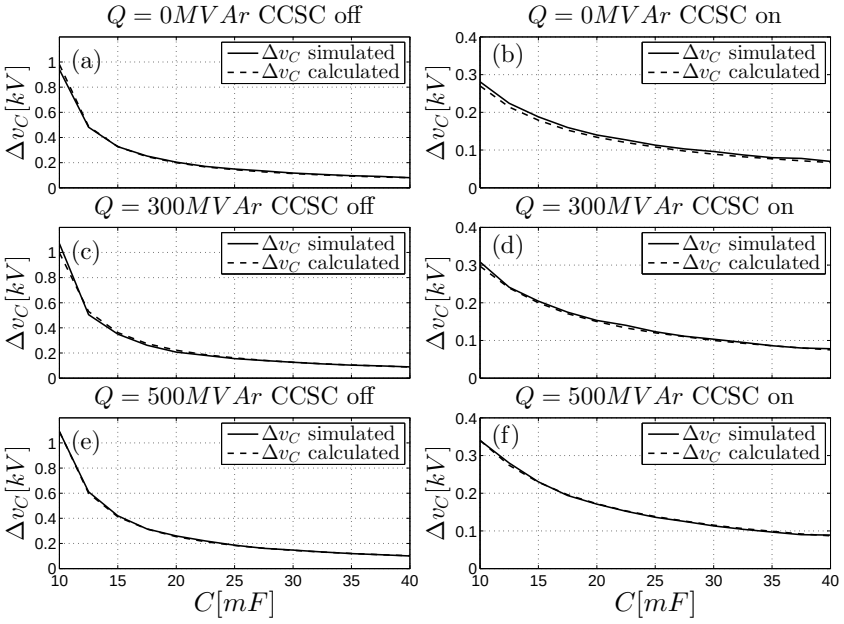

Figure 2.19: Comparison between the proposed steady-state model and the simulation results for Δv_C. (a) No reactive power and CCSC off; (b) No reactive power and CCSC on; (c) 300*MVAr* reactive power and CCSC off; (d) 300*MVAr* reactive power and CCSC on; (e) 500*MVAr* reactive power and CCSC off; (f) 300*MVAr* reactive power and CCSC on.

shows, the proposed model matches the simulation results.

2.5.2 Modulation index

In this subsection, the modulation index, resultant from the method described in Section 2.3.4, is compared to the flat estimation from (2.24). The simulated system is still the same as in Section 2.4.1, and Subsection 2.5.1, for the same changes in C. The reactive power assumed the values of 0 and 500 $MVAr$, and the CCSC was turned *on* and *off* for both values. As Fig.

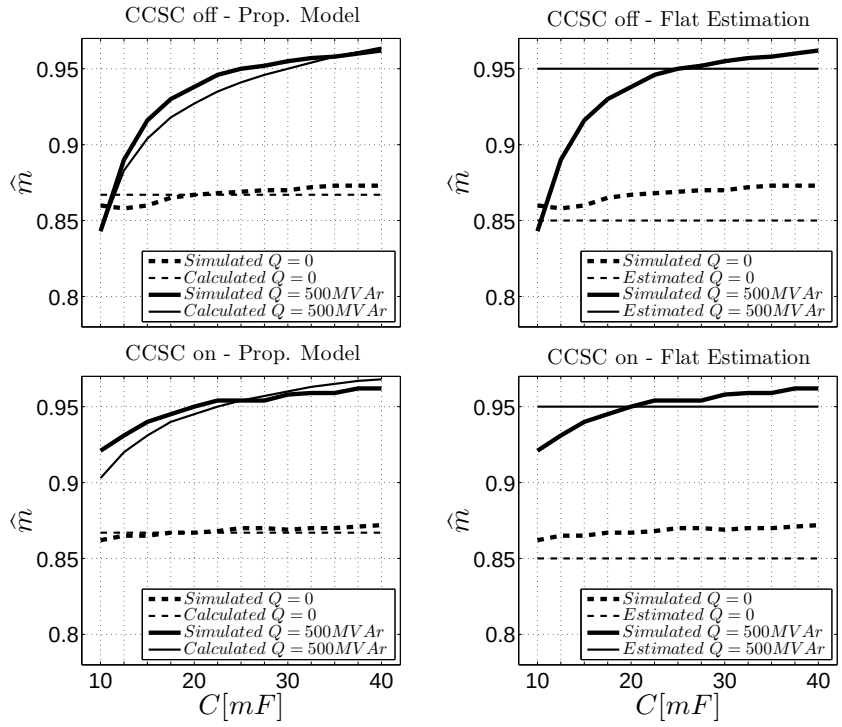

Figure 2.20: Comparison between $\widehat{m}$ calculated by the proposed model and estimated by (2.24).

2.20 shows, the flat estimation of the modulation index generates a much higher error than in the proposed model. This error is then propagated to all harmonic component amplitudes calculated.

2.5.3 Circulating current, submodule capacitor voltage, and Arm voltage

This subsection presents, the comparison between the proposed steady-state harmonic model and the simulation results for the harmonic amplitudes in the circulating current, Fig. 2.21 and Fig. 2.22, submodule capacitor voltage, Fig. 2.21, and the arm voltage, Fig. 2.23. Fig. 2.21 shows the harmonic amplitudes for the second harmonic, in the circulating current, and the first, second and third harmonics, in the submodule capacitor voltage, for a reactive power of $0MVAr$ and $500MVAr$. Further, Fig. 2.22 shows the comparison between the proposed steady-state harmonic model and the simulation results only for the amplitude of the circulating current second harmonic, for the same change in capacitance presented in Fig. 2.21, added to a change in the reactive power absorbed by the MMC, from $0-500$ $MVAr$, in steps of 50 $MVAr$. Finally, Fig. 2.23 shows the comparison between the proposed steady-state harmonic model and the

simulation results for the MMC upper arm voltage first, second ,third, and fourth harmonics, for a reactive power of $0MVAr$ and $500MVAr$.

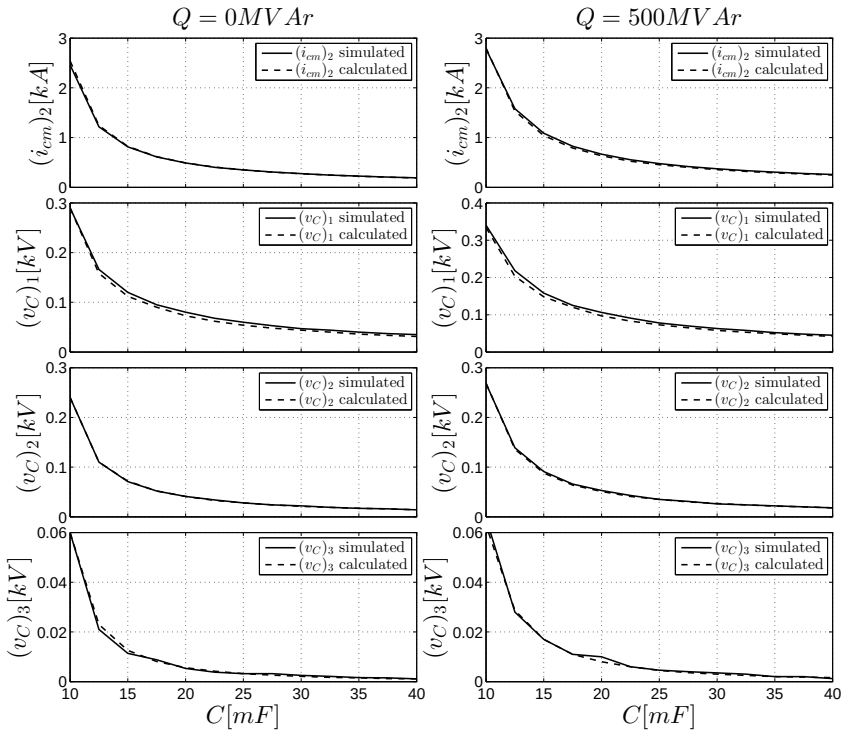

Figure 2.21: Comparison between the proposed steady-state harmonic model and the simulation results for $(i_{cm})_2$, $(v_C)_1$, $(v_C)_2$ and $(v_C)_3$.

All figures, 2.21, 2.22, and 2.23, confirm the accuracy of the steady-state proposed model.

2.5.4 Circulating current series convergence (resonance)

Figure 2.24 shows the *d* component of the ac-side terminal current, in the rectifier and inverter (see Fig. 2.16), for different values of arm inductance (25 *mH*, 45 *mH*, and 50 *mH*). The value of *C* is kept constant at 10 *mF*.

In Fig. 2.24, the active power control reference is set to -1000 *MW*, in the rectifier, at $t = 0.3$ *s*, and the reactive power control reference is kept at zero. The CCSC in the inverter is kept *off*, for the purpose of resonance visualization, whereas the CCSC in the rectifier is activated, also, at $t = 0.3$ *s*. It can be observed that for an arm inductance of 25 *mH*, the system is stable and there is no resonance. When the system is simulated with an arm inductance of 45 *mH*, which is the critical inductance calculated by (2.140), the inverter ac-side terminal current presents an stable oscillation in *dq*-frame, indicating that the system is resonating. In the rectifier ac-side terminal current *d* component, the oscillation is damped by the CCSC. Further, when the system is simulated with an arm inductance of 50 *mH*, the value adopted in [18] and [20]-[22], the system is oscillation-free again.

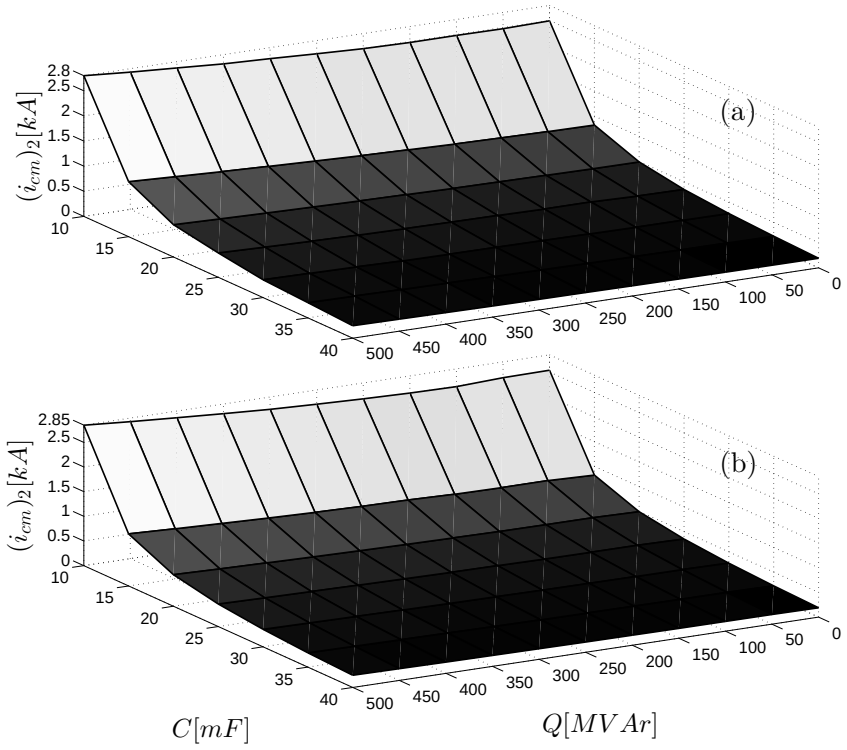

Figure 2.22: Comparison between the simulation, (a), and the proposed steady-state harmonic model results, (b), for $(i_{cm})_2$ amplitude with Q changing from $0 - 500MVAr$.

2.6 Validation of the capacitor sizing method

Four references ([45], [54], [56], and [58]) containing experimental results were used, in this thesis, to validate the submodule capacitor sizing method accuracy. The parameters needed for the calculation of the capacitance of the submodule capacitor, such as ac-side terminal current peak, submodule capacitor voltage variation, etc, were acquired from experimental results published in scaled charts, whereas other parameters, such as M, L, etc, were taken from tables in the respective papers.

Table 2.4 shows the comparison between the capacitance calculated using the proposed method and the capacitance of the physical capacitors installed in the experimental set-ups.

Table 2.4: Comparison between the proposed capacitor sizing method and experimental set-ups

Reference	$\widehat{I_{cm}}$, $[A]$	Calculated C from proposed method, $[mF]$	Physical capacitor installed in the experimental set-up, $[mF]$
[45]	0	0.785	0.77
	6	0.517	0.52
[54]	0	0.634	0.66
[56]	0	1.368	1.36
[58]	0	0.633	0.623

It can be noted in Table 2.4 that in the first row, reference [45] presents two values for the capacitance of the submodule capacitors: one for a completely suppressed circulating current, and another for an injected circulating current. References [54], [56], and [58] present only

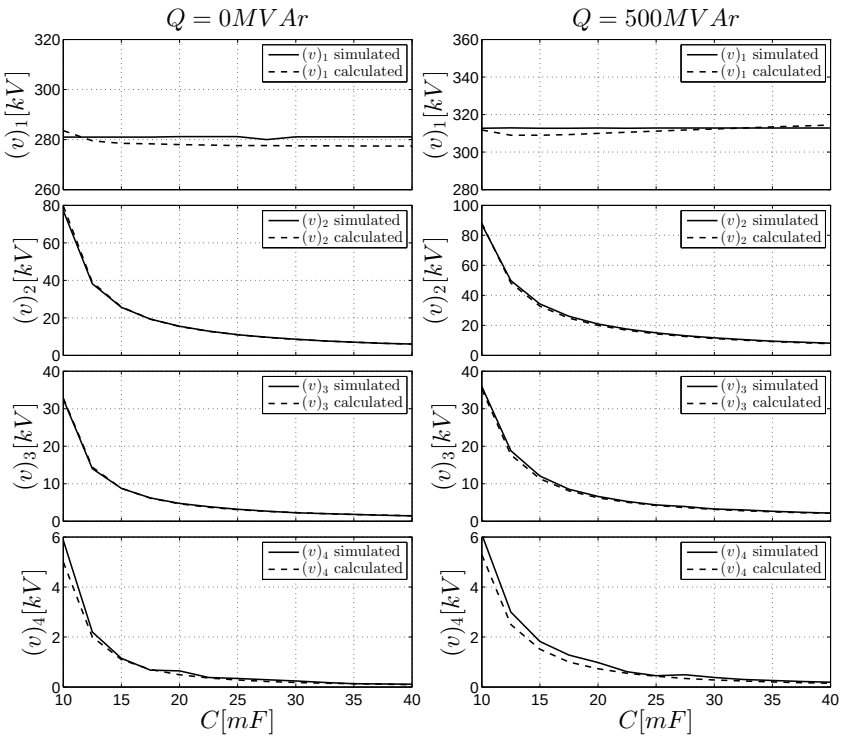

Figure 2.23: Comparison between the proposed steady-state harmonic model and the simulation results for $(v)_1$, $(v)_2$, $(v)_3$, and $(v)_4$.

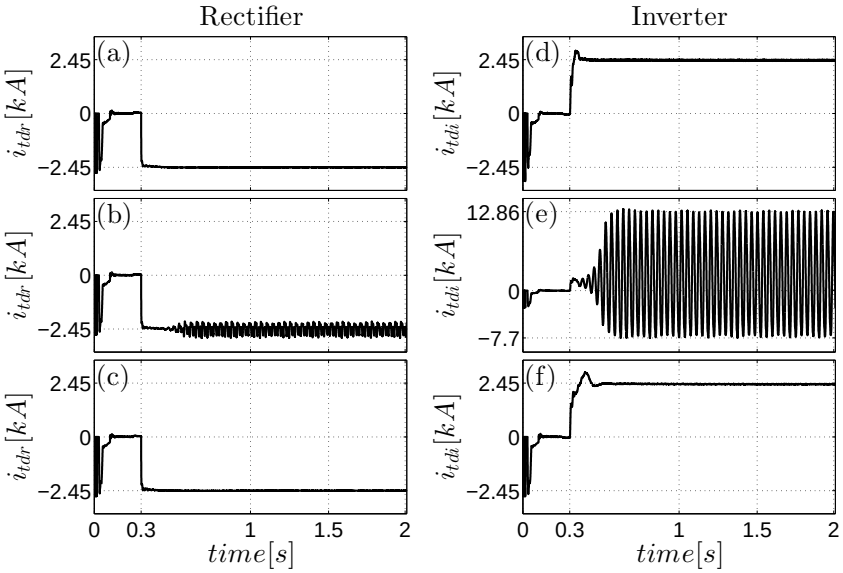

Figure 2.24: *d* component of the ac-side terminal current, in the rectifier and the inverter, for an arm inductance of 25 *mH* (a) and (d), 45 *mH* (b) and (e), and 50 *mH* (c) and (f).

experimental results with a suppressed circulating current.

One can conclude, observing Table 2.4, that the proposed method provides satisfactory results for the sizing of the submodule capacitor, since the highest error observed in Table 2.4 is of 4.1% in the second row.

2.7 Summary and Conclusions

In this chapter, a complete steady-state model that allows the calculation of the steady-state amplitude of all harmonic components of the MMC voltages and currents, was proposed. The method applied resulted in simple and tractable equations that relate the MMC parameters and their impact on the generation of each harmonic component in the arm current, submodule capacitor voltage, and arm voltages. Also in this chapter, it was shown that the proposed model can be used to calculate the modulation index and the modulating function angle, without relying on inaccurate estimations. Therefore, the proposed model is more accurate than the previously published models. Further, the proposed model was used in the development of a new submodule capacitor sizing method. The new submodule capacitor sizing method was shown to be completely analytical, that is, it does not rely on charts or numerical algorithms, but simple calculation steps. The proposed method provides the necessary capacitance value for a desired submodule capacitor voltage variation as a function of the MMC parameters. Furthermore, simulation results proved the accuracy of the proposed steady-state harmonic model, in predicting the amplitudes of the harmonic components in the submodule capacitor voltage, the arm voltage, and the circulating current in the MMC arm. Finally, the results given by the proposed method for sizing the submodule capacitor were compared to experimental results published in the literature, showing a satisfactory similarity.

Chapter 3

Development of a Simulation Model of the MMC

Due to the large number of switches and capacitors in an MMC arm, for HVDC systems, detailed nonlinear IGBT-based (Type 2) simulation models [66], and even simplified IGBT-based simulation models (Type 3) require several hours for building the model, and the followed simulations take a long time to be completed. Thus, equivalent-circuit-based models are used to simulate the MMC-based HVDC system. However, for an MMC with a large arm reactance, the impact of the switch in the converter dynamics is negligible. Therefore, the simplified-equivalent-circuit (SEC) developed in this chapter, takes into account the dynamic of the submodule capacitors only, in each submodule, and considers the switches as ideal switches.

Also, the SEC simulation model assumes that the MMC has its SMs based on the FBSM topology, Fig. 2.2c. Since the SEC simulation model is focused in the converter dynamic behavior, it also works when the SM topology is different than the FBSM, but retains the same dc-side fault handling capability for disable switches. Therefore, the SEC simulation model can be applied to simulate the LMMC, described in Chapter 5, and the LSM, described in Chapter 6.

3.1 Simplified Equivalent-Circuit Simulation Model

Fig. 3.1 shows a schematic diagram of the proposed simplified equivalent-circuit (SEC) simulation model of an MMC, as implemented in this thesis. As Fig. 3.1 illustrates, the model consists of an electric circuit model and a program code, which embeds the proposed simulation model. The electric circuit is the same as that of Fig. 2.1, except that each arm is replaced by a corresponding dependant voltage source. Thus, the control signals of the two sources, i.e., the values of the arm voltages v_1 and v_2, are generated by the proposed simulation model in the program code. The program code is written in *C* programming language since it is generally regarded as the most low-level universally diffused programming language of the present time (as *assembly* programming language is rarely used). Further, most circuit simulation software packages have the capability of compiling a *C* language code. For example, if the circuit model is to be developed in Matlab/Simulink environment, the program code can be linked to Matlab/Simulink [81] through a *s-function* block and the *Engine Library*. If, as

another example, PSIM [82] is the circuit simulation software, the program code can be called in Matlab/Simulnik by a *s-function* block, which, in turn, is linked to PSIM. For the simulation model developed for this paper, the program code was linked to PSCAD/EMTDC [80] through a *Component Block* and the *Project Settings* tab.

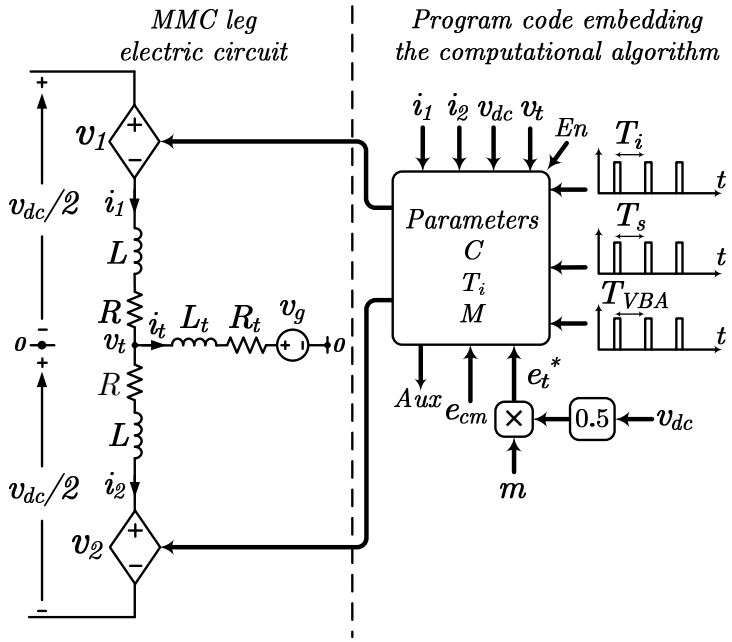

Figure 3.1: Schematic diagram of the proposed SEC simulation model for one leg of an MMC.

As Fig. 3.1 shows, the program code requires, as its user-defined inputs, the number of capacitors per arm, M, the submodule capacitor value, C, and the *integration time step*, T_i. The program code also requires the following variables from the host circuit simulation software:

1. The binary signal *enable*, denoted by En, which is set by the control scheme of the MMC to one (for normal operation) or zero (in faulted conditions);

2. An auxiliary set of output signals, *Aux*, defined by the user to monitor or plot desired variables internal to the program code, such as the dc voltage of particular SMs, the number of inserted SMs in an arm, and so on;

3. The arm currents i_1 and i_2;

4. The ac-side terminal voltage, v_t, relative to the virtual midpoint of the dc side, and the dc-side voltage v_{dc};

5. The desired inner voltage, e_t^*, which, in turn, is generated by the multiplying $v_{dc}/2$ by the desired modulating function for the leg, m;

6. The *integration signal*, which is a pulsetrain whose period, i.e., the *integration period*, T_i, should be equal to, at least, two times the simulation time step of the host circuit simulation software;

7. The *sampling signal*, which is a pulsetrain whose period, i.e., the *sampling period*, T_s, is calculated as $T_s = 1/\lfloor 2(M+2) f_g \rfloor$, and f_g is the grid frequency;

8. The *voltage balancing algorithm (VBA) signal*, which is a pulsetrain whose period, T_{VBA}, must be larger than or equal to the *sampling frequency*, T_s; and

9. The common-mode current suppressing control signal, e_{cm}.

The aforementioned parameters/variables are transferred to the program code by a set of *pointers* which are embedded in a *function* called by a *Component Block* of the host circuit simulation software, to create the necessary link to the file where the program code resides. The *integration frequency*, *sampling frequency*, and *VBA frequency* pulse trains can be readily produced by corresponding signal sources of the circuit simulation software.

3.2 Program code for the simplified equivalent-circuit simulation model

The objective of the program code is to calculate the values of the arm voltages, for the circuit part of the SEC simulation model of Fig. 2.1; each arm voltage value is calculated by adding the submodule capacitor voltages of the M capacitors in the arm. To this end, the program code uses, for each arm, the states for each capacitor, defined as: inserted, i.e., v_{Cj} ($j = 1, ..., M$ in the upper arm, and $j = M+1, ..., 2M$ in the lower arm) is connected in series to the arm, or bypassed. A *disabled* state is used by the code to process the arm voltage as a whole, disregarding the submodule capacitor voltages. A submodule capacitor voltage value, in turn, is updated based on the state of the capacitor and the host arm current (in terms of both magnitude and direction). The submodule capacitor voltages in an arm are then stored in a corresponding *SM voltage array*. Also, the states of the capacitors are stored in a respective *activation array*; each element of the activation array is a binary variable whose value 0 corresponds to a bypassed capacitor, and whose value 1 represents an inserted capacitor.

The program code embeds four routines: *modulation routine*, *VBA routine*, *submodule capacitor voltage calculation routine*, and *arm voltage calculation routine*. These routines are described in detail, next, with reference to the flowchart of Fig. 3.2.

3.2.1 Modulation routine

The modulation routine is based on the calculation of n_1 and n_2, given by (2.16) and (2.17). However, as the CCSC (or CCC) action, e_{cm}, is taken into account, (2.16) and (2.17) must be augmented to

$$n_1 = \frac{M}{2} - a - a_{cm} \tag{3.1}$$

$$n_2 = \frac{M}{2} + a - a_{cm} \tag{3.2}$$

where $a_{cm} = round(e_{cm}/\overline{v}_c)$.

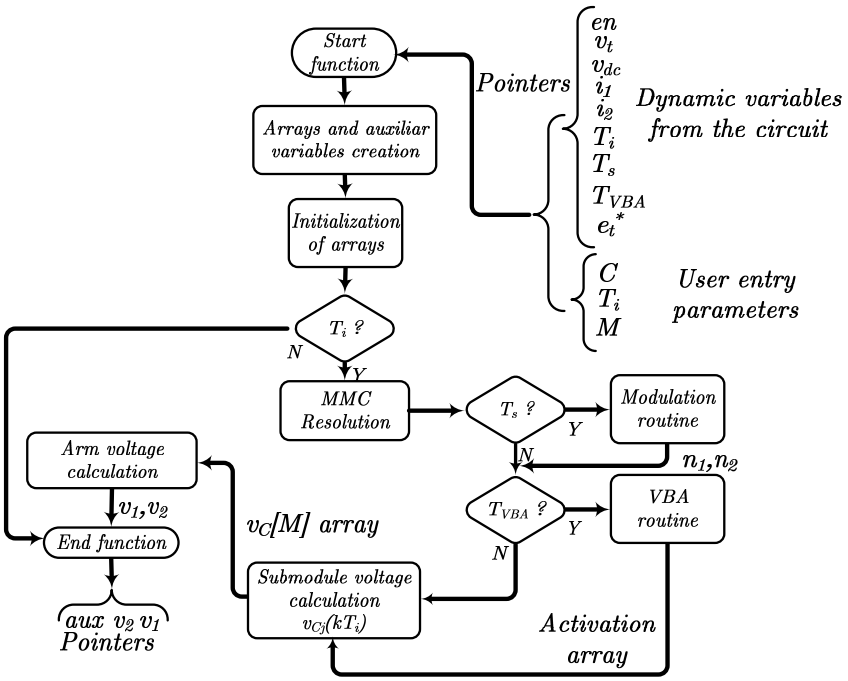

Figure 3.2: Flowchart of the program code of the proposed simulation model.

The modulation routine also ensures that n_1 and n_2 are within the interval $[0, M]$ (saturation). After the calculation of n_1 and n_2, these values are sent further on to the *VBA routine*. Figure 3.3 shows the flowchart of the modulation routine.

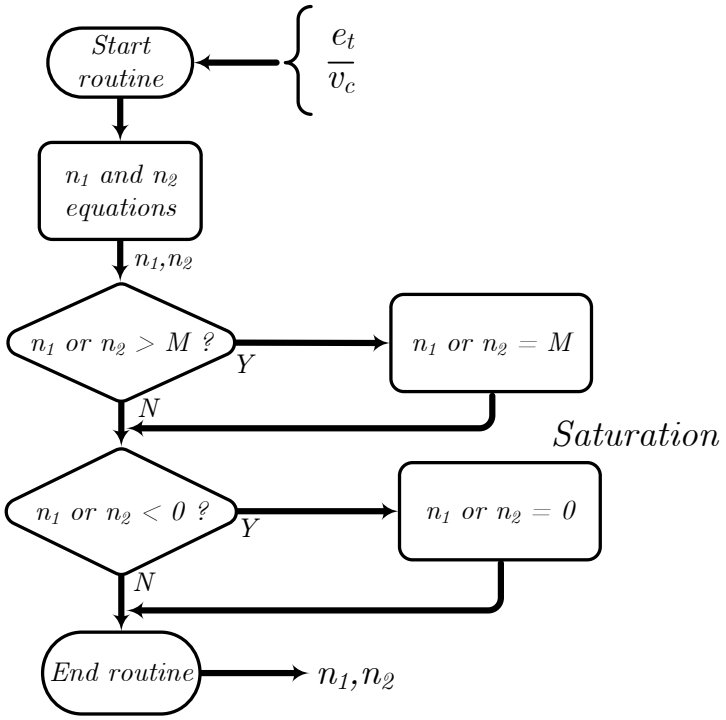

Figure 3.3: Flowchart of the modulation routine.

3.2.2 Voltage balancing algorithm (VBA) routine

The function of the VBA routine is to equalize the average values of the submodule capacitor voltages at the resolution (see Section 2.2.1) value, based, for example, on the *sorting algorithm* which was chosen in this paper for its simplicity [15]. The VBA routine receives the number capacitors that need to be inserted in the arm, n_1 and n_2, from the modulation routine and determines which capacitors, from each arm, will be inserted. Thus, the VBA routine inserts a capacitor with the smallest voltage, if the host arm current is positive, hence charging the corresponding capacitor. Similarly, it inserts a capacitor with the largest voltage if the arm current is negative, to discharge the capacitor. Based on the inserted capacitors, the *activation arrays* of the two arms are updated and delivered to the submodule capacitor voltage calculation routine discussed in Section 3.2.3. As Fig. 3.2 indicates, the VBA routine is started every time a VBA signal pulse is detected, that is, once every T_{VBA} seconds.

Fig. 3.4 illustrates the flowchart of the VBA routine.

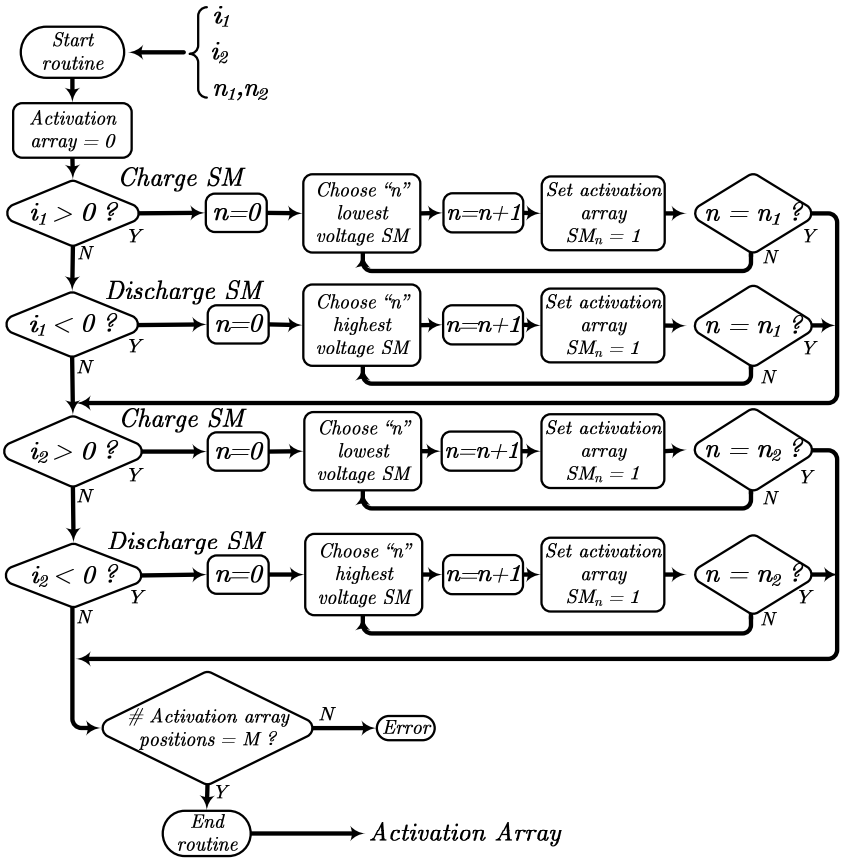

Figure 3.4: Flowchart of the VBA routine.

3.2.3 Submodule capacitor voltage calculation routine

The task of the submodule capacitor voltage calculation routine is to calculate, and provide to the arm voltage calculation routine, the voltages of the inserted submodule capacitors. The

calculation of the submodule capacitor voltage is executed differently for an arm with *enabled* SMs and for an arm with *disabled* SM, as follows.

Capacitor voltage calculation for enabled submodules

For each arm, the inserted capacitors are identified in the corresponding activation array by the VBA routine. The capacitor voltage values of each arm are stored in a corresponding *SM voltage array*. The voltage values of the inserted capacitors are updated through integration of the host arm current values, using, for example, the trapezoidal method:

$$\begin{aligned} & v_{Cj}[kT_i] \\ & = v_{Cj}[(k-1)T_i] + \frac{T_i}{2C}\{i_r[kT_i] + i_r[(k-1)T_i]\} \end{aligned} \tag{3.3}$$

where integer k is the sample number ($r = 1$ for the upper arm, and $r = 2$ for the lower arm). The capacitor voltage value is left unchanged if the respective capacitor is bypassed according to the activation array. The submodule capacitor voltage calculation routine limits $v_{Cj}[kT_i]$ to zero from the low side, since the diodes of the SMs, Fig. 2.2 c, do not allow the development of negative capacitor voltages. A bypassed capacitor, which is marked by 0 in the respective activation array, corresponds to a zero ac voltage value.

Capacitor voltage calculation for disabled submodules

In the case where the SMs are *disabled*, e.g. during capacitor pre-charge or a dc-side fault, the activation array is overrun and all capacitors are updated in the presence of an arm current, in the same manner as if the switches were enabled. The only difference is that the arm current integrated in Eq. (3.3) is always positive, due to the anti-parallel diodes of the switches.

As Fig. 3.2 indicates, the submodule capacitor voltage calculation routine is started every time an integration signal pulse is detected, that is, once every T_i seconds.

3.2.4 Arm voltage calculation routine

The objective of the *arm voltage calculation routine* is to determine the arm voltage values v_1 and v_2, to be communicated to the circuit simulation software, for the dependent voltage sources which emulate the MMC arms, Fig. 3.1. As Fig. 3.2 indicates, the arm voltage calculation routine is started every time an integration signal pulse is detected, that is, once every T_i seconds. Similarly to the SM capacitor voltages calculation described in Section 3.2.3, the arm voltage calculation is differently computed for *enabled* SMs that for *disabled* SMs.

Arm voltage calculation for enabled submodules

For each arm, the aforementioned objective is achieved by adding the entries of the SM voltage array corresponding to non-zero elements of the respective activation array. In mathematical

terms, the operation is equivalent to:

$$v_1 = \sum_{j=1}^{M} v_{Cj} \tag{3.4}$$

and

$$v_2 = \sum_{j=M+1}^{2M} v_{Cj} \tag{3.5}$$

where v_{Cj} is the voltage in the capacitor j.

Arm voltage calculation for disabled submodules

In a *disabled* FBSM-based MMC, the anti-parallel diodes of the switches are on (conducting) if the summation of *grid voltage* and the induced voltage in the MMC inductors is higher than the arm voltage, that is, if the arm current is different than zero for disabled switches. In both cases, the arm voltage is computed using Eq (3.4) and Eq (3.5) with the difference that all elements of the *SM voltage array* are added together (all SMs voltages are taken into account), and the *activation array* is neglected. Also, since the current is always positive in the SM capacitor for a disable SM, the arm voltage polarity follows the direction of the arm current. For instance, for a positive arm current, the arm voltage in the upper arm is given by v_1, and if the arm current is negative, the upper arm voltage is given by $-v_1$.

In the case where the arm voltage is higher than the *grid voltage* and the arm current is zero, the anti-parallel diodes of the switches are not conducting, and the arm voltage is given by

$$v_1 = \frac{v_{dc}}{2} - v_g \tag{3.6}$$

and

$$v_2 = \frac{v_{dc}}{2} + v_g \tag{3.7}$$

An example of the SEC complete code, used in this thesis, is presented in Appendix A.

3.3 Validation of the simplified equivalent-circuit simulation model

To validate the proposed simulation model, several MMC-based systems were simulated for faulted as well as normal operating conditions, in the PSCAD/EMTDC software environment [80]. The simulated cases included back-to-back systems with schemes for *ac-side terminal current* control, circulating current suppression, and *dc-side voltage* regulation. For PSCAD/EMTDC, the simulation time-step and plot-step were 0.5 μs and 1 μs, respectively.

For the program code, $T_i = 1\ \mu s$ (two times the simulation time-step), $T_s = 1/[2(M+1)f_g]$, and $T_{VBA} = T_s$, for cases I, II, and III, and $T_{VBA} = T_s/10$ for Case IV. All simulations were run on a PC embedding an Intel Core i3-2120 @ 3.3GHz processor, 4 GB of RAM, and Windows 7 Professional operating system. The PSCAD version used was v4.5.2.0.

For cases I, II and III, the corresponding simulated results were captured both by the Type 2 simulation model, as mentioned in Section 1.3.3, and the proposed SEC simulation models. For Case IV, only the proposed SEC simulation model was used, as the number of SMs per arm is too large for the Type 2 simulation model.

The simulated cases are discussed below.

3.3.1 Case I - FBSM-based single-phase MMC inverter for $M = 4$

In this case, a single-phase MMC inverter, Fig. 3.5, was simulated with 4 FBSMs (i.e., $M = 4$) and under open-loop control. A *dc-side voltage* of $v_{dc} = 8\ kV$ was impressed by two identical dc sources, as Fig. 3.5 shows. The connection to the common terminal of the two sources, node 0, closed the load circuit. The modulating signal for the control was $m = \sin(2\pi f_g t)$ where $f_g = 60\ Hz$. The other parameters of the system were: $C = 3.1\ mF$, $R = 15\ m\Omega$, $L = 2\ mH$, $R_t = 2\ \Omega$, $L_t = 0$. The grid voltage was $v_g = 2\sin(2\pi f_g t)\ kV$. The system also included a fault detection logics that compared the peak values of the arm currents, i_1 and i_2, with a threshold of 1.5 *kA*. Thus, the fault detection mechanism blocked the gating pulses of the switches, for 100-*ms*, if either of the two peak values exceeded the threshold.

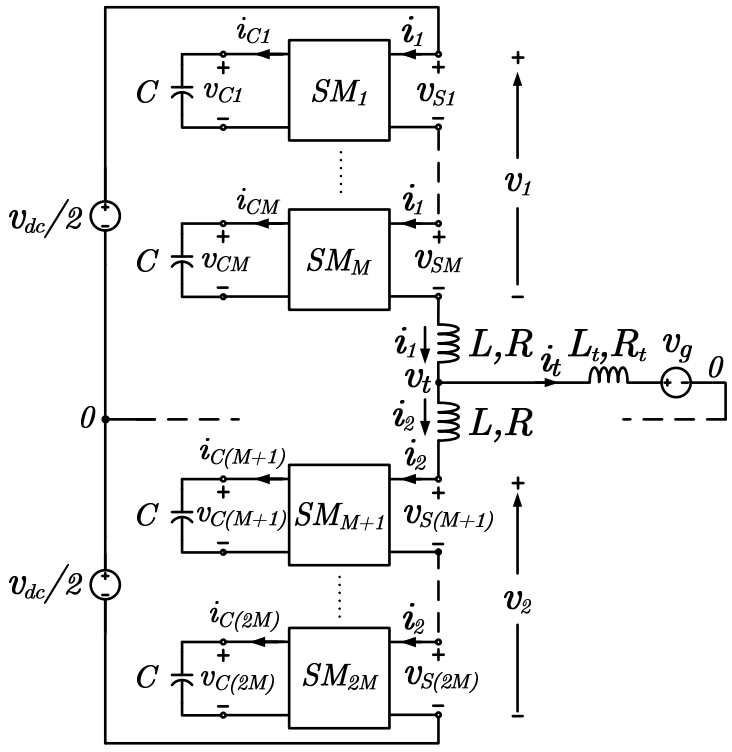

Figure 3.5: Schematic diagram of a single-phase MMC inverter system.

The Case I simulation results using the proposed SEC model, were compared to the simula-

tion results from the same case using a Type 2 simulation model. Both models were simulated in two scenarios: 1) SM capacitor pre-charge, and 2) dc-side fault. These two scenarios are described below.

Submodule capacitor pre-charge

In the SM capacitor pre-charge scenario, all switches in the SMs are *disabled*, leaving only the switches anti-parallel diodes to control the series connection of the SM capacitors to the MMC arm. Fig. 3.6 presents the arm equivalent RLC circuit for *disable* switches, where diodes D_1 and D_2 represent the behavior of the forward biased anti-parallel diodes in the arm SMs switches S_1 and S_4 (Fig. 2.2 c). Further, in Fig. 3.6, the equivalent capacitance in the MMC arm is given by the series connection of all SM capacitors, C/M, and the summation of the capacitor voltages is represented by V_{dc0}.

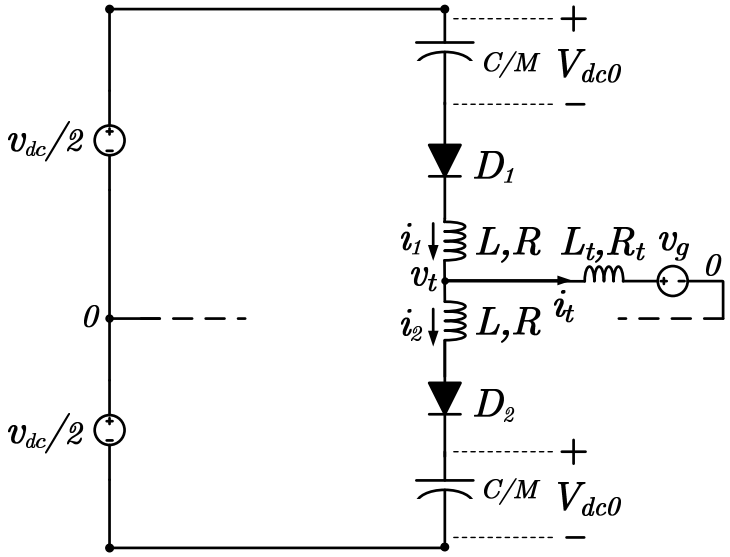

Figure 3.6: Equivalent circuit for the MMC arm during pre-charge.

Fig. 3.7 shows the arm voltages (a,b), the ac-side terminal current (c) and the capacitor 4 voltage, v_{C4} (d) waveforms for the pre-charge scenario using the proposed SEC simulation model and the Type 2 simulation model.

In the beginning, $t = 0$ *s*, all switches were *disabled*. Thus, the arm voltages and terminal current followed the expected dynamics of the RLC circuit, Fig. 3.6. Then, the SM capacitors charged up to the maximum voltage value allowed by the circuit (in the upper arm, the maximum voltage value for the SM capacitor is lower than the maximum voltage value in the lower arm, due to the fact that in the upper arm, v_g is subtracting $v_{dc}/2$). Later, when the SM capacitor voltage reached the maximum voltage value for the arm, D_1 and D_2 became reversely biased and the ac-side terminal current assumed zero value. Furthermore, since the arm circuit is open (diode reversely biased) the upper arm voltage was formed by the grid voltage added to $-v_{dc}/2$. In the same manner, the lower arm voltage was formed by the grid voltage added to $v_{dc}/2$. At $t = 0.03$ *s*, the SM switches are *enabled* and the converter starts producing the ac-side terminal

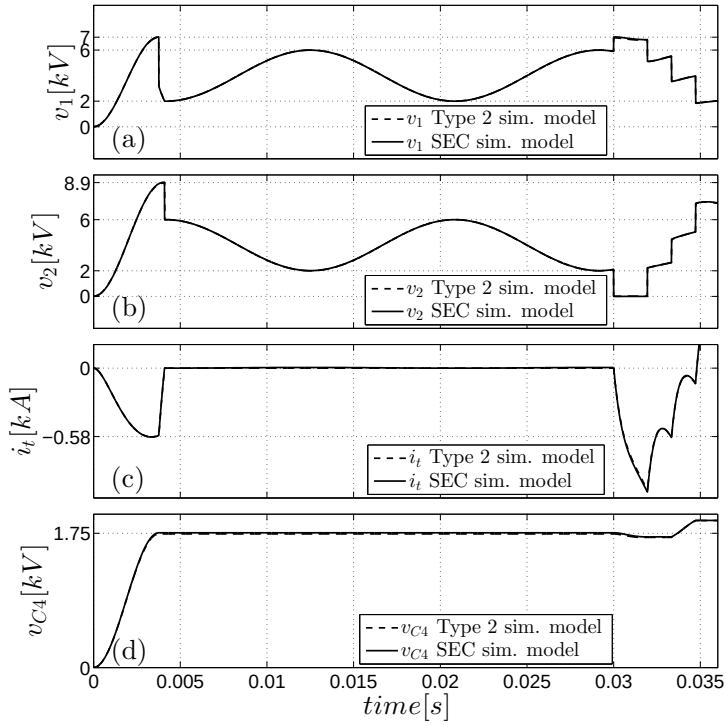

Figure 3.7: Case I system during pre-charge. (a) Upper arm voltage. (b) Lower arm voltage. (c) Ac-side terminal current. (d) Capacitor 4 voltage.

voltage steps, following the control reference m. The capacitor voltage remains constant after the arm diodes become reversely biased.

Simulation of a dc-side fault situation

After the SM capacitors pre-charge, the MMC runs in normal operation until $t = 0.1\ s$, when a short-circuit, featuring an impedance of 2 $m\Omega$, was placed across v_{dc}, simulating a 50 ms long dc-side fault. Fig. 3.8 shows the MMC arm equivalent circuit for a dc-side fault, where the equivalent diodes are formed, by the anti-parallel diodes in the upper arm SM switches S_3 and S_2 and the anti-parallel diodes in the lower arm SM switches S_1 and S_4.

Fig. 3.9 shows the arm voltages (a,b), the ac-side terminal current (c), and the dc-side voltage (d) waveforms for the dc-side fault scenario using the proposed SEC simulation model and the Type 2 simulation model.

When the dc-side fault occurred, at $t = 0.1\ s$, the dc-side voltage became approximately zero and the fault detection mechanism blocks the pulses in the switches. Moreover, for this scenario, all SM capacitors were charged to their rated voltage $\overline{v}_c$ before the fault occurred. Therefore, V_{dc0} had a magnitude higher than the peak of the grid voltage, forcing the equivalent diodes, to be reversely biased. Thus, the ac-side terminal current, i_t, was driven to zero and the arm voltages, v_1 and v_2, became equal to $-v_g$ and v_g, respectively, after a small transient from the arm reactors.

Fig. 3.10 shows the arm voltages (a,b), the ac-side terminal current (c), and the capacitor 4 voltage, v_{C4} (d) waveforms for Case I using the proposed SEC simulation model and the Type

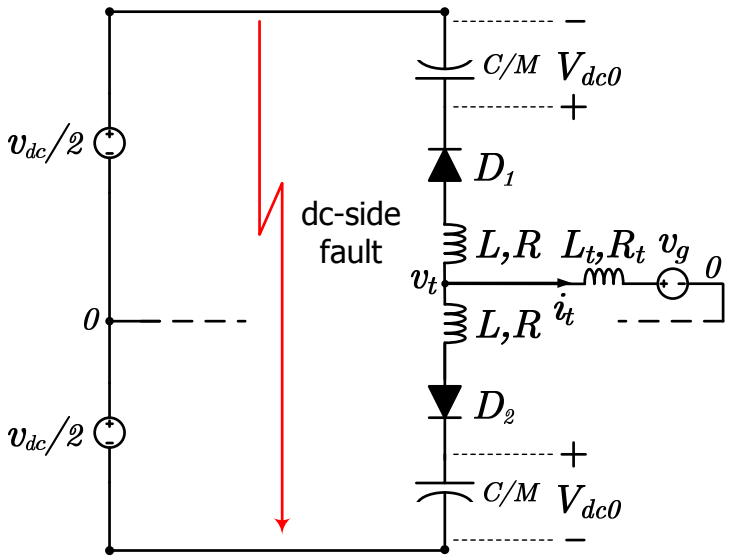

Figure 3.8: Equivalent circuit for the MMC arm during a dc-side fault.

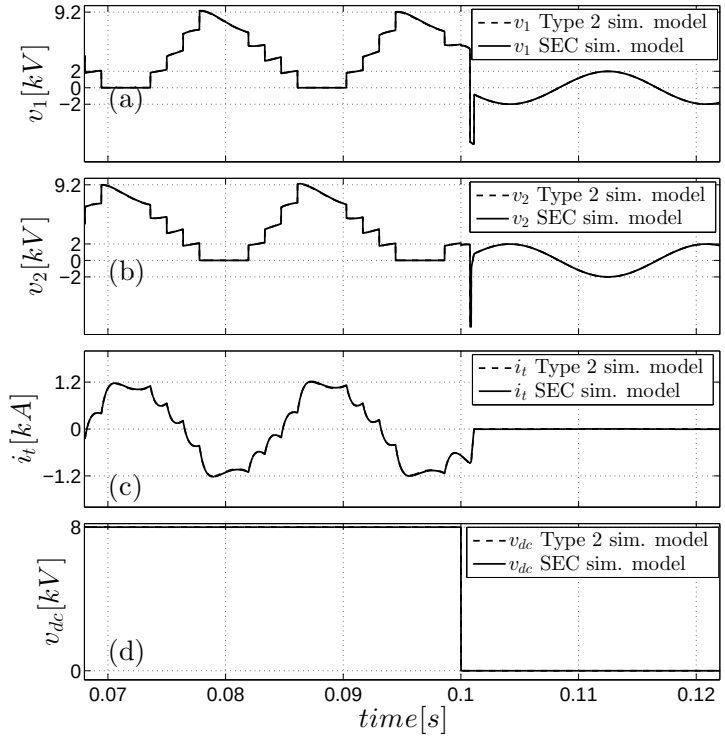

Figure 3.9: Case I system during a dc-side fault. (a) Upper arm voltage. (b) Lower arm voltage. (c) Ac-side terminal current. (d) Dc-side voltage.

2 simulation model for the full simulated range, i.e., from $t = 0$ to $t = 0.31$ s.

After 50 ms, $t = 0.15$ s, the dc-side fault was cleared and $v_{dc}/2$ is added to the arm voltages, Fig. 3.10 (a) and (b). At $t = 0.2$ s the fault detection mechanism release the pulses in the switches and the MMC resumed its normal operation. Fig. 3.10 (d) shows that the VBA in the

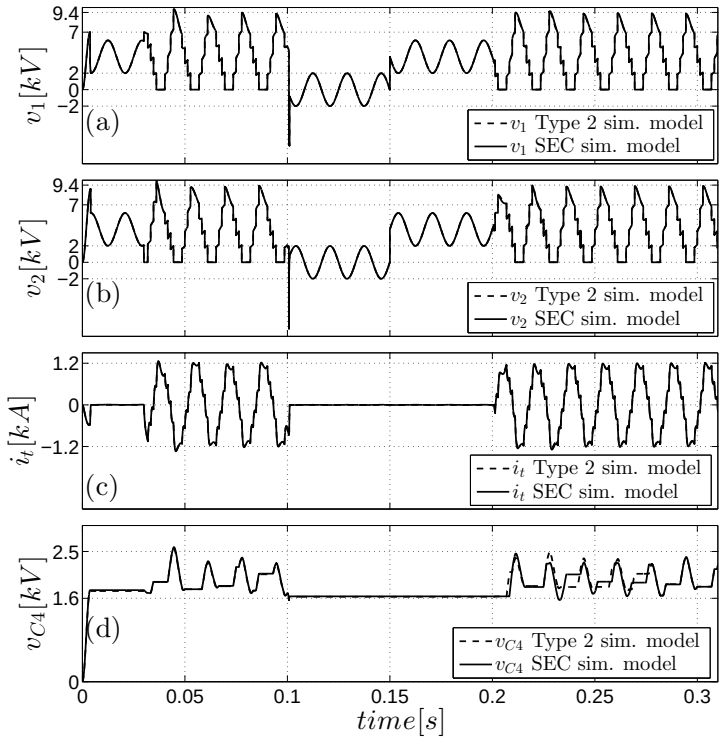

Figure 3.10: Case I system full simulated range. (a) Upper arm voltage. (b) Lower arm voltage. (c) Ac-side terminal current. (d) Capacitor 4 voltage.

SEC simulation model and in the Type 2 simulation model do not always allow the same SMs to be *on* at the same time, which causes different charging and discharging times in the SM capacitor voltage. The dynamics in the arm and ac-side terminal quantities in both simulation models remain very close despite the small differences in the SM capacitor voltages.

3.3.2 Case II - FBSM-based single-phase MMC rectifier for $M = 4$

This simulation case captures the response of a single-phase MMC rectifier, Fig. 3.11, simulated with 4 FBSMs (i.e., $M = 4$) and under open-loop control. The parameters used and the disturbances applied in Case II are the same as those of Case I, with the difference that the dc voltage sources used in Case I were substituted by two 50 Ω resistors, R_{L1} and R_{L2}, behaving as a dc-side load. Also, the terminal resistance, R_t value used is 100 $m\Omega$. The fault detection mechanism used was also the same as Case I, with the exception that the current threshold was 0.05 *kA*.

The same simulation scenarios from Case I were applied to Case II, as follows.

SM capacitor pre-charge

As it was the case for Subsection 3.3.1, all switches in the SMs were *disabled* at the beginning. For Case II, the pre-charge power flow is inverse. During the pre-charge, the load resistors are bypassed by a temporary short-circuit to increase the SM capacitors full-charge voltage, and the equivalent circuit approaches the one that Fig. 3.8 shows.

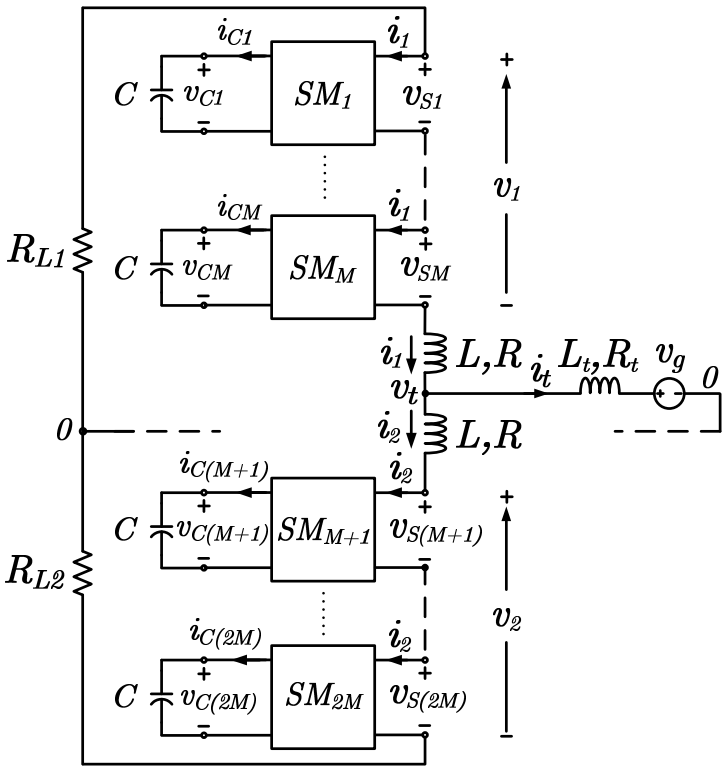

Figure 3.11: Schematic diagram of a single-phase MMC rectifier system.

Fig. 3.12 shows the arm voltages (a,b), the ac-side terminal current (c), and the dc-side voltage (d) waveforms for the pre-charge scenario using the proposed SEC simulation model and the Type 2 simulation model.

When the arm voltage reached its maximum and the arm current became zero, the switches anti-parallel diodes became reversely biased (if $V_{dc0} > v_g$), the arm voltages became equal to the grid voltage ($v_1 = -v_g$ and $v_2 = v_g$) and the terminal current assumed zero value. At $t = 0.03\ s$, the pulses for the SM switches were released and the MMC rectifier started to produce the ac-side terminal voltage steps. Also, the SM capacitor voltages added up to form v_{dc}.

Simulation of a dc-side fault situation

After the SM capacitors pre-charge, the MMC ran in normal operation until $t = 0.1\ s$, when a short-circuit, featuring an impedance of $2\ m\Omega$, was placed across v_{dc}, simulating a $50\ ms$ long dc-side fault. The equivalent circuit for this scenario is the same as the one in Subsection 3.3.2.

Fig. 3.13 presents the arm voltages (a,b), the ac-side terminal current (c), and the dc-side voltage (d) waveforms for the dc-side fault scenario using the proposed SEC simulation model and the Type 2 simulation model.

When the dc-side fault occurred, at $t = 0.1\ s$, a similar effect observed in Subsection 3.3.1 took place. In Case II, since the dc-side voltage is generated by the MMC when in normal operation, after the dc-side fault was cleared, the arm voltages were not added to $v_{dc}/2$, as it happened for Case I. The arm voltages remain following the grid voltage in the same manner

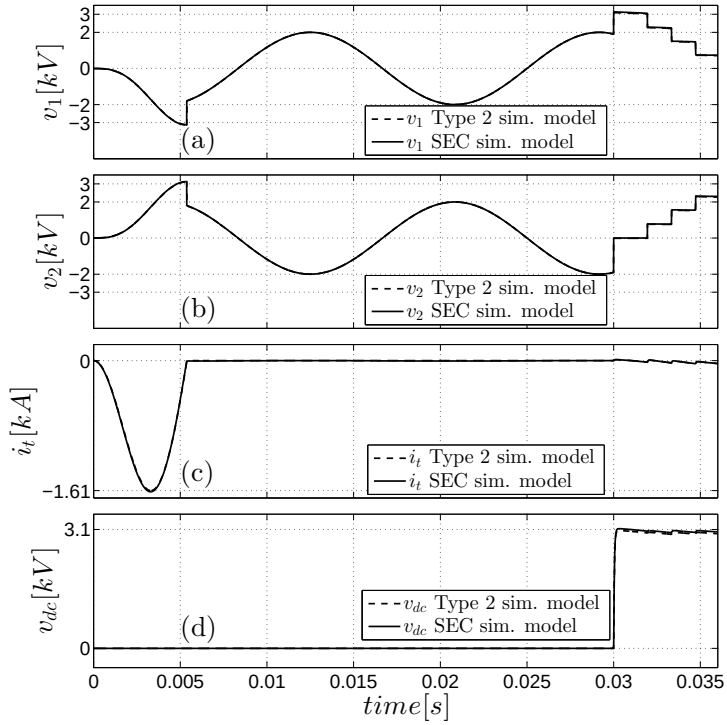

Figure 3.12: Case II system during pre-charge. (a) Upper arm voltage. (b) Lower arm voltage. (c) Ac-side terminal current. (d) Dc-side voltage.

before and after the fault clearance, as long as the switches are *disabled*.

3.3.3 Case III - FBSM-based three-phase MMC inverter for $M = 8$

In this case, a SEC simulation model of a three-phase 9-level MMC, operated as an inverter in a system such as shown in Fig. 2.1, was simulated under closed-loop control. The parameters were $C = 6\ mF$, $R = 0.1\ \Omega$, $L = 4\ mH$, $R_t = 0.8\ \Omega$, and $L_t = 10\ mH$. The grid voltage had a peak value of 2 *kV* and its frequency was 50-*Hz*. The MMC was current-controlled in a *dq* frame synchronized to the grid voltage, [10]. The converter was also equipped with a fault detection mechanism that compared the peak value of the arm currents with a threshold of 1.0 *kA* and disabled the current controller and the gating pulses for 100 *ms*, if any of the six arm current peak values exceeded the threshold. The fault detection mechanism also set the setpoint for the *d*-axis component of the ac-side terminal current to zero.

From the start to $t = 0.03\ s$, the gating pulses and the current controller were *disabled*. At $t = 0.03\ s$, the gating pulses were released and the current controller was activated, with the real- and reactive-power setpoints both set to zero. At $t = 0.15\ s$, the real-power setpoint was stepped to 2 *MW*, thus raising the setpoint for the *d*-axis component of the ac-side terminal current to $i_d^* = 0.66\ kA$. At $t = 0.4\ s$, a short link was placed across the dc-side terminals of the MMC, and was removed after 50 *ms*. The fault detection mechanism detected the fault, almost immediately, blocked the gating pulses, disabled the current controller, and set i_d^* to zero. At $t = 0.5\ s$, the gating pulses were unblocked, the current controller was enabled, and i_d^* was reset to its pre-disturbance value of 0.66 *kA*.

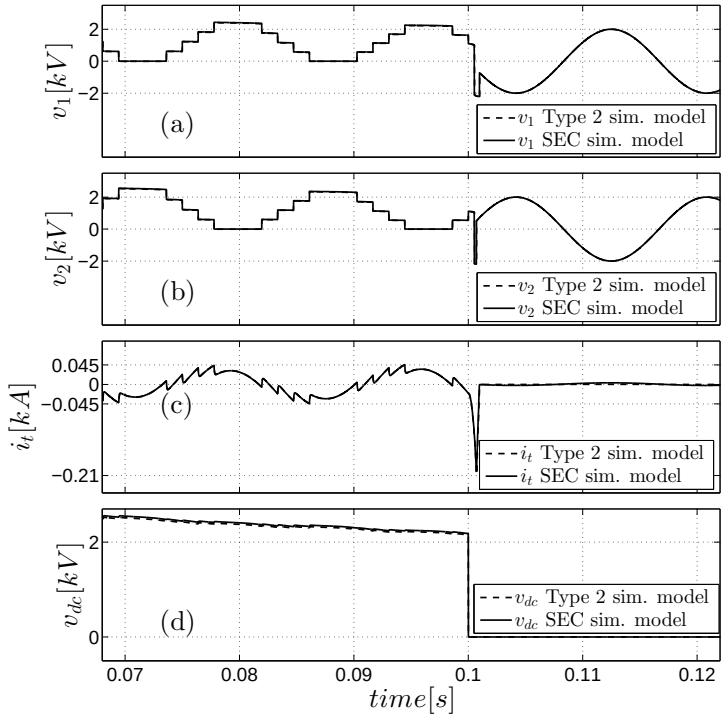

Figure 3.13: Case II system during a dc-side fault. (a) Upper arm voltage. (b) Lower arm voltage. (c) Ac-side terminal current. (d) Dc-side voltage.

Fig. 3.14 shows the waveforms of the ac-side terminal current, upper arm current, and upper arm voltage (all for phase-*a*) for the proposed SEC and the Type 2 simulation models. The figure also shows the waveforms of the *d*- and *q*-axis components of the ac-side terminal current. It is observed that, as expected, the arm current and the ac-side terminal current drop to zero once the fault is detected. It is also observed that the ac-side terminal current is noticeably distorted. The distortion, in turn, translates into considerable ripples in the *d*- and *q*-axis current components. The distortion is due to the small M for this simulation and, consequently, the low number of levels in the ac-side terminal voltage of the MMC. The modulation strategy adopted for this thesis, i.e., the NLC modulation strategy, produces quality ac-side voltage and current waveforms if M is large, as illustrated in the next case study, in Section 3.3.4.

In cases I, II and III, figs. 3.7, 3.9, 3.12, 3.13 and 3.14 show the proximity of the Type 2 and the proposed SEC simulation models.

3.3.4 Case IV - FBSM-based back-to-back three-phase MMC system for $M = 400$

In this case, a back-to-back system, similar to the system presented in [18] and [22]-[20], was simulated. The system, whose simplified schematic diagram is shown in Fig. 2.16, was simulated using only SEC simulation model. For both MMCs of the back-to-back system, the parameters were: $M = 400$, $C = 10\ mF$, $R = 338\ m\Omega$, $R_t = 377\ m\Omega$, $L = 50\ mH$, and $L_t = 60\ mH$. The simulation model also included a scheme for circulating current suppression [30], and schemes for ac-side terminal current control and dc-side voltage regulation [10]. The grid

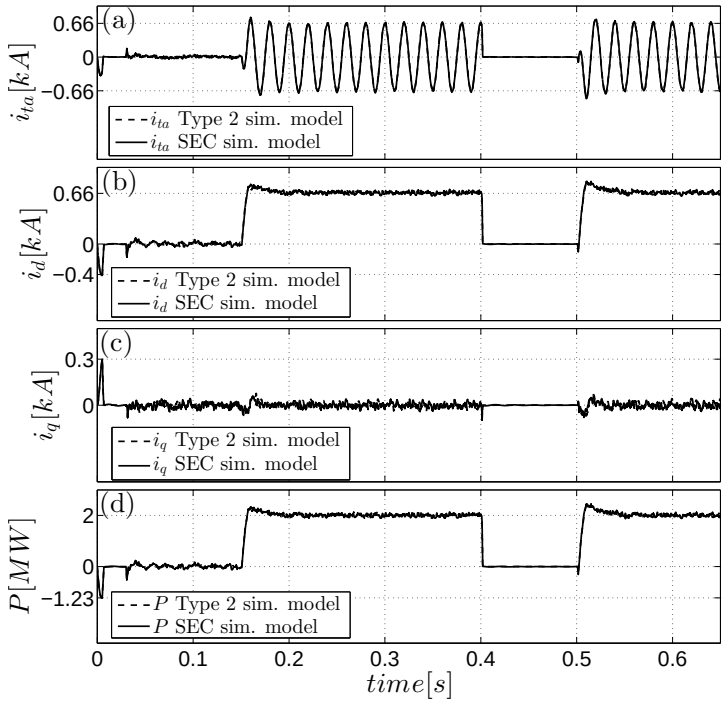

Figure 3.14: Waveforms of selected variables in a closed-loop controlled three-phase 9-level MMC, to various disturbances; Case III.

voltages, v_{gi} and v_{gr} (i =inverter and r =rectifier), were balanced, 50-*Hz*, sinusoids with a peak value of 272 *kV* (corresponding to a line-to-line rms voltage of 333 *kV*). Each MMC was equipped with the same fault detection mechanism as that in the system of Case III, albeit with a threshold of 2.0 *kA* and a disablement period of 200 *ms*.

Initially, switches SW_r and SW_i were open to isolate the dc-side terminals of the two constituting MMCs, and the gating pulses and the controllers were disabled. Thus, the capacitors of the two MMC were pre-charged by the corresponding grids, to about 875 *V* each. At $t = 0.03$ *s*, the gating pulses were released and the controllers were enabled, while the reactive-power setpoints of both MMCs were set to zero. However, the real-power setpoints were obtained from two corresponding dc-side voltage control loops, which raised the dc-side terminal voltages to 640 *kV*. At $t = 0.25$ *s*, SW_r and SW_i were closed and the real-power setpoint of the *rectifier MMC* was switched off from the corresponding dc-side voltage control loop, to be regarded as the real-power setpoint for the back-to-back system. However, the real-power setpoint of the *inverter MMC* was left in possession of the respective dc-side voltage regulation loop. Thus, the MMC was delegated the task of dc-side voltage regulation, for the back-to-back system. At $t = 0.3$ *s*, the real-power setpoint was stepped down to −1000 *MW*, and stepped up to 1000 *MW* at $t = 0.55$ *s*. At $t = 0.85$ *s*, a short link was placed across the dc-side terminals of the MMCs, and it was removed after 100 *ms*. Fig. 3.15 shows the system response to the aforementioned sequence of events.

As Fig. 3.15 shows, the dc voltage of the system drops to zero due to the fault. The fault also results in large ac-side terminal currents in both MMCs, until the fault is detected and the gating pulses are blocked (shortly after $t = 0.85$ *s*). The transient large ac-side terminal currents manifest themselves as current spikes, as Fig. 3.15 shows. The transient current

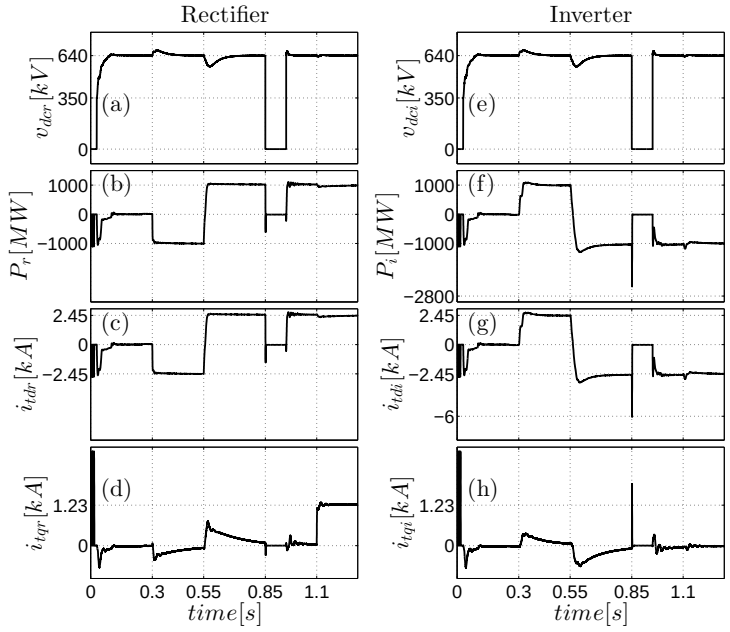

Figure 3.15: Waveforms of selected variables in the rectifier MMC (left column) and inverter MMC (right column); Case IV.

growth is larger for the inverter MMC, since the dc-side voltage regulation loop commands a large negative *d*-axis current for the inverter MMC, in a futile attempt to maintain the dc-side voltage. Once the fault is detected, the gating pulses are blocked, the controllers are disabled, and the ac-side terminal currents drop to zero, in both MMCs (that is, i_d and i_q also become zero).

Beside the validation provided by the simulation results in this section, the SEC simulation model was further validated by comparison to an independent dynamic model developed by Dr. Chaudhuri in North Dakota State University, [29].

3.3.5 Simulation Runtime Evaluation

To evaluate the computational efficiency of the proposed SEC simulation model, as compared with a Type 2 simulation model, the single-phase system of Case I was simulated with various number of SMs, $M = 4$, 6, 8, 10, and 20. Therefore, the system of Case I was chosen, for its simplicity and the fact that it features the minimum number of control schemes, auxiliary functions, and circuit elements, in order to enable one to better observe and appreciate the advantage of the proposed SEC simulation model over the Type 2 simulation model, from the simulation runtime standpoint. Fig. 3.16 shows the variation of the simulation runtime versus M, for the Type 2 simulation model (Fig. 3.16(a)) and the proposed SEC simulation model (Fig. 3.16(b)). For the Type 2 simulation model, the simulation runtime values that correspond to M larger than 20 were estimated by extrapolation, in view of the observed linearity of the curve for the five aforementioned values of M.

As Fig. 3.16(a) illustrates, the simulation runtime under the Type 2 simulation model is, approximately, 16.6 s/M. By contrast, the simulation runtime under the proposed SEC simulation model is only about 0.1 s/M. Both the Type 2 and proposed SEC simulation models can

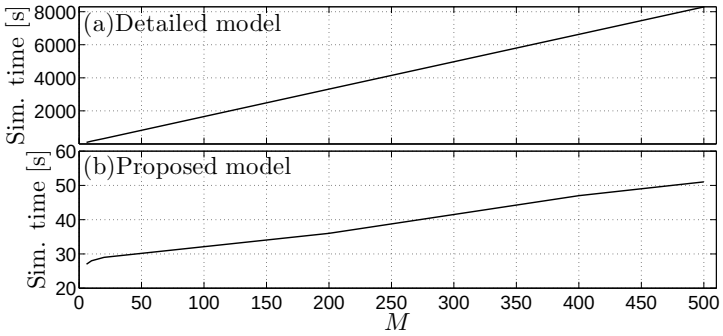

Figure 3.16: Simulation runtime versus number of SMs per arm.

be run faster by increasing the simulation time-step. The computational advantage of the proposed SEC simulation model over the Type 2 simulation model remains, however, independent of the simulation time-step.

3.4 Summary and Conclusions

A simulation model was proposed for the modular multilevel converter (MMC), the SEC simulation model. The proposed SEC simulation model combines a simple circuit model, which can be constructed in a general-purpose circuit simulation software environment, with a program code, which can be written in a universally diffused programming language such as *C*. The program code is linked to the circuit simulation software. Thus, the proposed SEC simulation model drastically reduces simulation runtime of the overall model and also offers a flexible interface through which the number of submodules and other parameters can be defined by the user. More importantly, the proposed SEC simulation model can simulate MMCs based on full-bridge submodule configurations, capturing pre-charge and other dynamic transients and showing almost imperceptible difference if compared to the Type 2 simulation model. It also enables simulation of faulted scenarios. The proposed SEC simulation model was shown to be significantly more efficient than the Type 2 simulation model and easier to implement than the Type 4 simulation model, as the switches are considered ideal. For example, it was shown in this chapter that, a 0.6-*s* simulation of a 800-submodule single-phase MMC system runs about 125 times faster using the proposed SEC simulation model, as compared with the Type 2 simulation model. Simulation study cases were conducted to demonstrate the accuracy and computational efficiency of the proposed SEC simulation model.

Chapter 4

Development of an Enhanced Control Strategy of the MMC

In MMC-based HVDC systems, the magnitude of the circulating current, if not suppressed, can reach that of the ac-side terminal current magnitude, reducing the efficiency. The most common way to suppress the circulating current, mainly its second harmonic component, is through closed-loop circulating current suppressing control strategies. The closed-loop circulating current suppressing control strategies are based on reading the second harmonic component in the arm current and generating a second harmonic component arm voltage to cancel it. However, the circulating current suppressing control and the ac-side terminal current control strategies both act in the variables n_1, in the upper arm, and n_2, in the lower arm, as it is observed in (3.1) and (3.2). Thus, saturation of both control loops may happen. Therefore, since a complete harmonic steady-state model for the MMC was developed in Chapter 2, the calculation of the arm voltage second harmonic component that cancels the circulating current follows naturally.

Thus, this chapter describes the development of an enhanced control strategy for suppressing the circulating current. The proposed control strategy uses the arm voltage second harmonic component calculated, applying the steady-state harmonic model, as a feedforward signal in the control loop to enhance the control damping action and diminish the possibility of saturation.

4.1 Ac-side terminal current compensator strategies

Using the equivalent circuit that Fig. 2.4 shows, and using (2.18), derived in Section 2.2.1, yields

$$\frac{v_{dc}}{2}m = L'\frac{di_t}{dt} + R'i_t + v_g \tag{4.1}$$

Equation (4.1) is true for all three phases of the MMC system. Thus,

$$\begin{aligned}\frac{v_{dc}}{2}m_a &= L'\frac{di_{ta}}{dt} + R'i_{ta} + v_{ga}\\ \frac{v_{dc}}{2}m_b &= L'\frac{di_{tb}}{dt} + R'i_{ta} + v_{gb}\\ \frac{v_{dc}}{2}m_c &= L'\frac{di_{tc}}{dt} + R'i_{tc} + v_{gc}\end{aligned} \tag{4.2}$$

Fig. 4.1 illustrates the block diagram corresponding to (4.1)

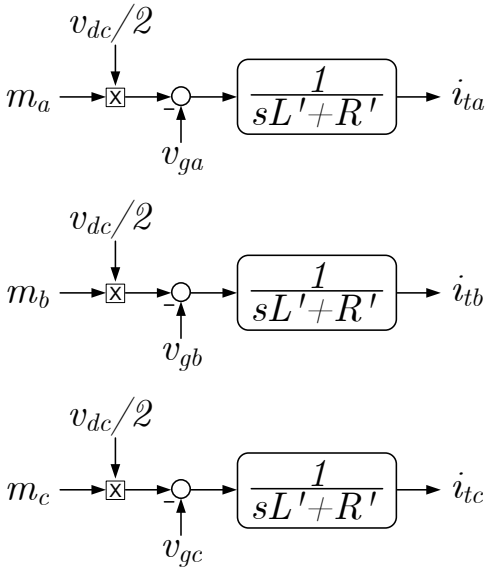

Figure 4.1: Block diagram for i_{ta}, i_{tb}, and i_{tc}.

4.1.1 PI compensator in *dq*-frame

One of the most common control strategies, for power converters in three-phase systems, is the proportional-integral compensator in *dq*-frame. Figure 4.2 illustrates the schematic diagram of the ac-side terminal current compensator in *dq*-frame. In Figure 4.2, i_{td}^* and i_{tq}^* represent the control reference currents for the compensators in *dq*-frame, and are calculated by the *Reference signal generator* block, which uses the following equations

$$i_{td}^* = \frac{2}{3}\frac{P_{ref}}{v_{gd}} \tag{4.3}$$

$$i_{tq}^* = -\frac{2}{3}\frac{Q_{ref}}{v_{gd}} \tag{4.4}$$

where P_{ref} and Q_{ref} are the active and reactive power, respectively, that are desired to be exchanged with the grid. Furthermore, in Figure 4.2, i_{td} and i_{tq} represent the *dq* components of the ac-side terminal currents, and v_{gd} and v_{gq} represent the *dq* components of the grid voltages.

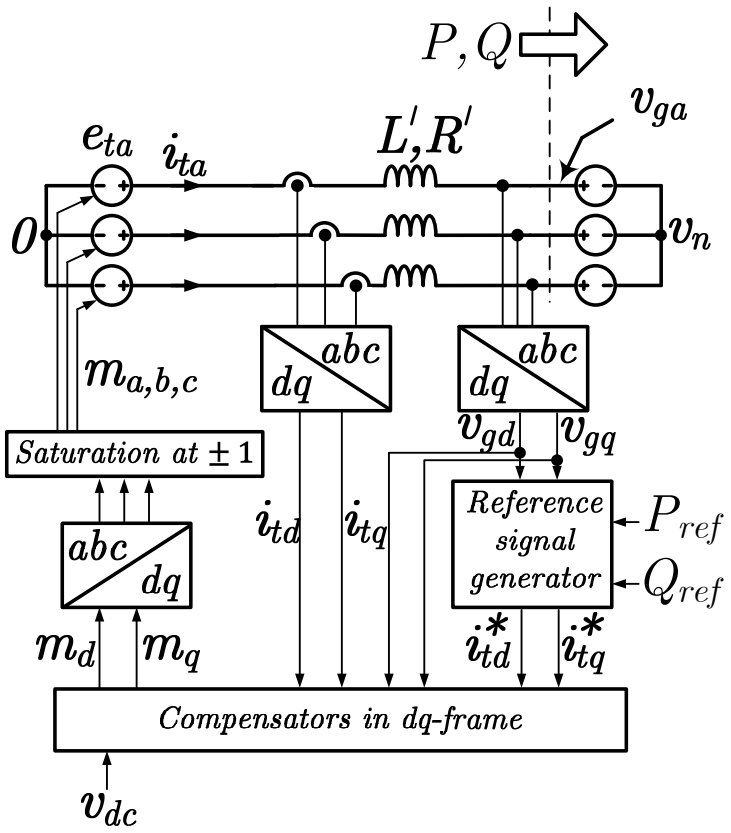

Figure 4.2: Schematic diagram of the ac-side terminal current compensator.

In (4.3) and (4.4), it is assumed that v_{gq} is driven to zero by a *phase-locked loop* (PLL), as described in [10]. The *dq*-frame transformation matrixes presented in Figure 4.2 are given as follows

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos(\rho) & cos\left(\rho - \frac{2\pi}{3}\right) & cos\left(\rho - \frac{4\pi}{3}\right) \\ -sin(\rho) & -sin\left(\rho - \frac{2\pi}{3}\right) & -sin\left(\rho - \frac{4\pi}{3}\right) \end{bmatrix}\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{4.5}$$

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} cos(\rho) & -sin(\rho) \\ cos\left(\rho - \frac{2\pi}{3}\right) & -sin\left(\rho - \frac{2\pi}{3}\right) \\ cos\left(\rho - \frac{4\pi}{3}\right) & -sin\left(\rho - \frac{4\pi}{3}\right) \end{bmatrix}\begin{bmatrix} f_d \\ f_q \end{bmatrix} \tag{4.6}$$

where f is the variable to be transformed to or from the *dq*-frame, and ρ represents the angle provide by the PLL in order to keep $v_{gq} = 0$, which guarantees the synchronism between the MMC and the ac grid. The angle ρ is given by

$$\rho = \int \omega(\tau)d\tau + \rho_0 \tag{4.7}$$

where ω is the grid angular frequency and τ is the integration variable. For a system with constant frequency, $\rho = \omega t$.

To design the gains of the PI compensator, the complete control loop must be analysed. Thus, (4.1) is transformed to *dq*-frame as follows.

Using the concept of space-phasor [10], (4.1) becomes

$$\frac{v_{dc}}{2}\vec{m} = L'\frac{d\vec{i}_t}{dt} + R'\vec{i}_t + \vec{v}_g \tag{4.8}$$

Then, substituting $\vec{i}_t = i_{tdq}e^{j\rho}$, $\vec{m} = m_{dq}e^{j\rho}$, and $\vec{v}_g = v_{gdq}e^{j\rho}$, separating the resultant equation in its *dq* components, and assuming $\rho = \omega t$ (PLL action [10]), results

$$\begin{aligned}\frac{v_{dc}}{2}m_d &= L'\frac{di_{td}}{dt} + R'i_{td} + v_{gd} + \omega L'i_{tq}\\ \frac{v_{dc}}{2}m_q &= L'\frac{di_{tq}}{dt} + R'i_{tq} + v_{gq} - \omega L'i_{td}\end{aligned} \tag{4.9}$$

Fig. 4.3 illustrates the block diagram corresponding to (4.9)

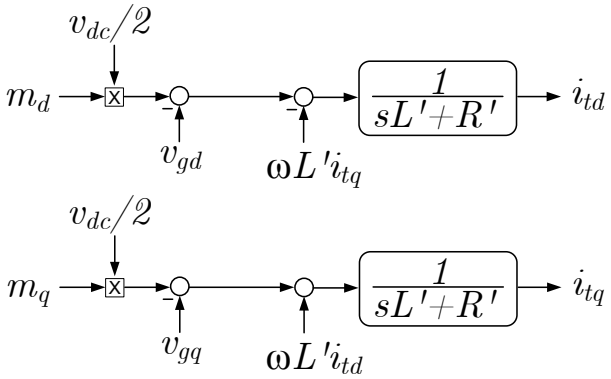

Figure 4.3: Block diagram for i_{td}, and i_{tq}.

Closing the loop in the block diagram that Fig. 4.3 illustrates, and applying feedforwards to cancel the action of $v_{dc}/2$, v_{gd}, v_{gq}, $\omega L'i_{tq}$, and $\omega L'i_{td}$, yields the complete block diagram of the ac-side terminal current control in *dq*-frame, illustrated in Fig. 4.4. In Fig. 4.4, $K_{td}(s)$ and

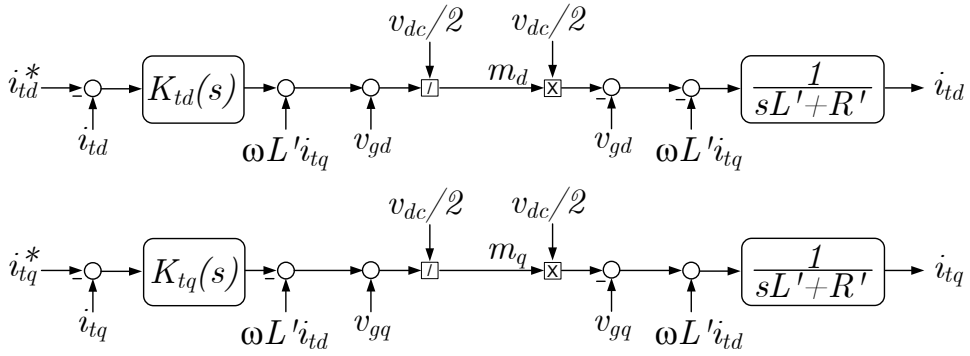

Figure 4.4: Complete block diagram of the ac-side terminal current control in *dq*-frame.

$K_{tq}(s)$ are the PI compensators in the frequency domain.

If the components that have been cancelled by the aforementioned feedforwards in Fig. 4.4 are omitted, the control loop can be represented by the simplified block diagram that Fig. 4.5 illustrates.

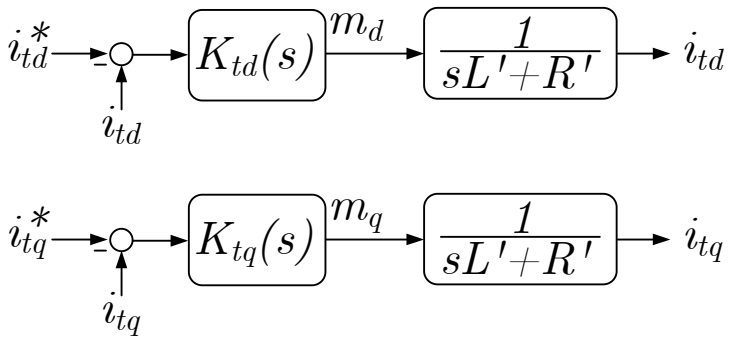

Figure 4.5: Simplified block diagram for the ac-side terminal current control in *dq*-frame.

Let $K_{td}(s) = K_{tq}(s) = K_p\left(s + \frac{K_i}{K_p}\right)/s$, then assuming that $K_i/K_p = R'/L'$, the closed-loop function becomes

$$\frac{i_{td}}{i_{td}^*} = \frac{1}{\frac{L'}{K_p}s + 1} \tag{4.10}$$

where L'/K_p is the time constant of the control loop, usually set between 0.5 to 2 ms.

4.2 Circulating current compensator

The even harmonic components in the arm voltages feature the same magnitude and polarity on both arms, adding themselves in the MMC leg and generating the circulating current. Such mechanism is described in detail in Section 2.3. Therefore, an arm voltage composed by even harmonic components must be generated equally in both arms, to suppress the circulating current. For this purpose, (2.19) and (2.20) are changed to include a *circulating current modulating function, e_{cm}*, as follows

$$n_1 = \frac{M}{2}[1 - m] - \frac{e_{cm}}{\overline{v}_c} = \frac{M}{2}\left[1 - m - \frac{2e_{cm}}{v_{dc}}\right] \tag{4.11}$$

$$n_2 = \frac{M}{2}[1 + m] - \frac{e_{cm}}{\overline{v}_c} = \frac{M}{2}\left[1 + m - \frac{2e_{cm}}{v_{dc}}\right] \tag{4.12}$$

where $e_{cm} = \widehat{e}_{cm} sin(2\omega t + \varphi_{cm})$

Assuming that the submodule capacitor voltages are controlled to approximately $\overline{v}_c$ by the VBA, yields $v_{C1} \approx v_{C2} \approx \overline{v}_c$. Thus, (2.33) can be approximated to

$$\frac{di_{cm}}{dt} = \frac{1}{L}\left[\frac{v_{dc}}{2} - \left(\frac{n_1 + n_2}{2}\right)\overline{v}_c - Ri_{cm}\right] \tag{4.13}$$

The addition of n_1 and n_2 in (4.13) causes m to be cancelled, as expected, showing that the ac-side terminal current control and the circulating current control are decoupled, for an

approximate model where only the fundamental component is taken into account. Therefore, substituting (4.11) and (4.12) into (4.13) yields

$$\frac{di_{cm}}{dt} = \frac{1}{L}\left(e_{cm} - Ri_{cm}\right) \tag{4.14}$$

Fig. 4.6 shows the block diagram for the circulating current in phase *a*.

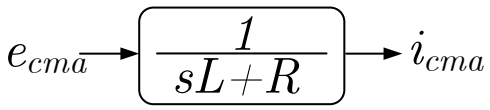

Figure 4.6: Block diagram for i_{cm} in phase *a*.

As the steady-state of the circulating current is known, from the model proposed in Chapter 2, a disturbance is added to the block diagram of Fig. 4.6 to represent the circulating current steady-state. Fig. 4.7 shows the augmented block diagram for the circulating current.

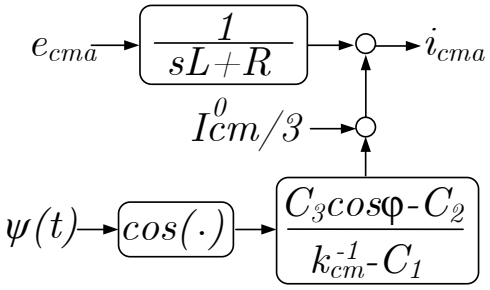

Figure 4.7: Block diagram for i_{cm} in phase *a*, with the circulating current steady-state added as a disturbance.

In Fig. 4.7, $\psi(t) = 2\omega t + \varphi_{cm}$, and $\varphi_{cm} \approx \varphi$. In addition, the values of C_1, C_2, and C_3 are calculated based on the system parameters, such as active and reactive power exchanged with the grid (see Table 2.1).

The circulating current can be suppressed using different strategies, as explained in 1.3.2. In this thesis, two control strategies, based on those proposed in [30] and [54], are described in the next two subsections.

4.2.1 Circulating current suppressing compensator in *dq*-frame

Similarly to the control strategy described in Section 4.1.1, the CCSC strategy in *dq*-frame is based on a PI compensator and *dq* transformation matrixes. The exception is that the circulating current phasor "rotates" at a frequency of 2ρ, and is of negative sequence. Therefore, the transformation matrixes have to be changed to

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos\left[\epsilon\right] & cos\left[\epsilon - \frac{4\pi}{3}\right] & cos\left[\epsilon - \frac{2\pi}{3}\right] \\ -sin\left[\epsilon\right] & -sin\left[\epsilon - \frac{4\pi}{3}\right] & -sin\left[\epsilon - \frac{2\pi}{3}\right] \end{bmatrix}\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{4.15}$$

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} cos[\epsilon] & -sin[\epsilon] \\ cos\left[\epsilon - \frac{4\pi}{3}\right] & -sin\left[\epsilon - \frac{4\pi}{3}\right] \\ cos\left[\epsilon - \frac{2\pi}{3}\right] & -sin\left[\epsilon - \frac{2\pi}{3}\right] \end{bmatrix} \begin{bmatrix} f_d \\ f_q \end{bmatrix} \tag{4.16}$$

where ϵ is given by

$$\epsilon = \int 2\omega(\tau)d\tau + \epsilon_0 \tag{4.17}$$

Fig. 4.8 illustrates the block diagram of the circulating current control loop, where $K_d(s)$ and $K_q(s)$ are the PI compensators for d and q components, respectively. Fig. 4.8 also shows the same disturbance showed in Fig. 4.7, transformed to dq-frame.

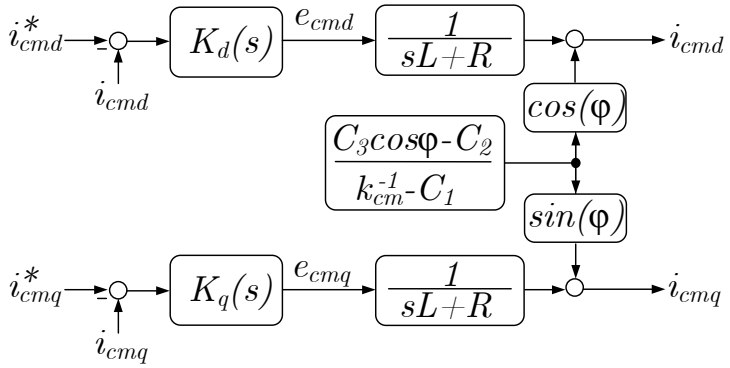

Figure 4.8: Block diagram for i_{cm} control loop.

Applying the same methodology followed in Subsection 4.1.1, and assuming $K_d(s) = K_q(s) = K_{cmp}\left(s + \frac{K_{cmi}}{K_{cmp}}\right)/s$, yields the closed-loop transfer function for the CCSC, as follows

$$\frac{i_{cmd}}{i^*_{cmd}} = \frac{1}{\frac{L}{K_{cmp}}s + 1} \tag{4.18}$$

where L/K_{cmp} is the time constant of the control loop.

As Table 2.1 shows, the harmonic components in the arm voltages receive the contribution of both i_{cm} and i_t. For this reason, the two control loops, ac-side terminal current and circulating current, are only decoupled in an approximate model (used in this subsection), but not in the complete model presented in Chapter 2. Therefore, the time constant for the CCSC must be close to the time constant chosen for the ac-side terminal current compensator, or the system might become unstable as demonstrated in [29].

4.2.2 Resonant compensator

The PI compensator in dq-frame was proved to be very efficient for balanced systems([10], [30]). However, if the system is unbalanced, the PI compensator in dq-frame is no longer able to bring the steady-state error to zero. For this reason, a compensator can be designed for each phase of the three-phase system, as Fig. 4.9 shows.

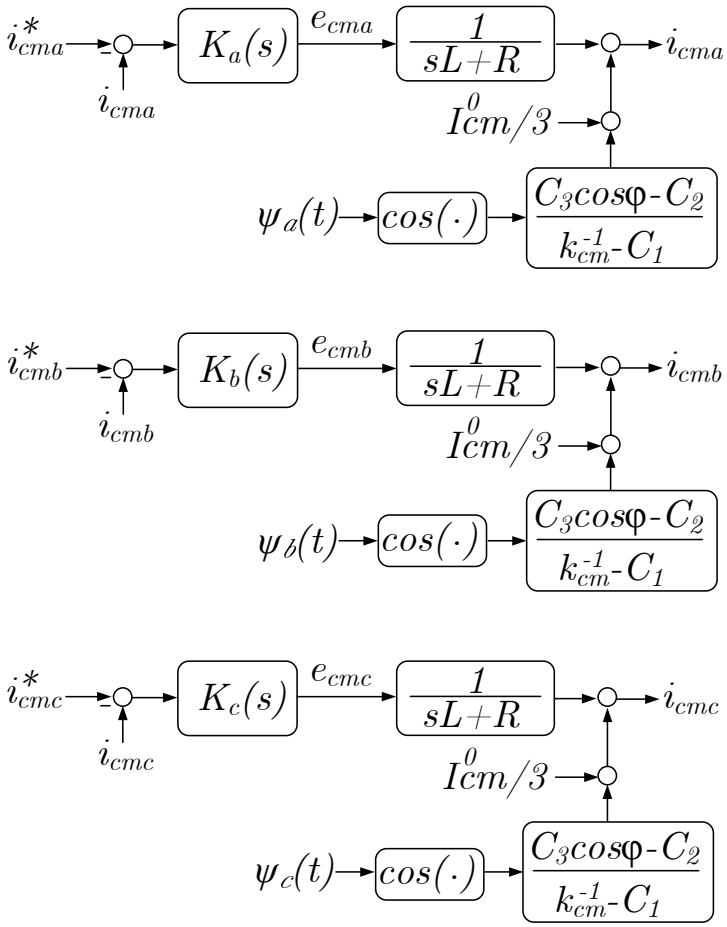

Figure 4.9: Block diagram for i_{cm} three-phase control loop.

In Fig. 4.9 $\psi_a(t) = (2\omega t + \varphi_{cm})$, $\psi_b(t) = (2\omega t + \varphi_{cm} - 2\pi/3)$, and $\psi_c(t) = (2\omega t + \varphi_{cm} + 2\pi/3)$.

The circulating current is mainly composed by a second harmonic and a dc component (2.66), thus, in order to present infinite gain at 2ω, the design of the compensator starts by setting resonant poles, i.e., two complex poles at $s = j2\omega$. Thus,

$$K_a(s) = K_b(s) = K_c(s) = K(s) = \frac{1}{s^2 + 4\omega^2} \tag{4.19}$$

If a zero is added to $K(s)$ to cancel the low frequency pole in the MMC leg, at $s = -R/L$, (4.19) is changed to

$$K(s) = \frac{s + \frac{R}{L}}{s^2 + 4\omega^2} \tag{4.20}$$

Assuming that $G(s)$ is the MMC leg transfer function, illustrated in Fig. 4.6, the open-loop transfer function, $\ell(s) = K(s)G(s)$, is given by

$$\ell(s) = \frac{1/L}{s^2 + 4\omega^2} \tag{4.21}$$

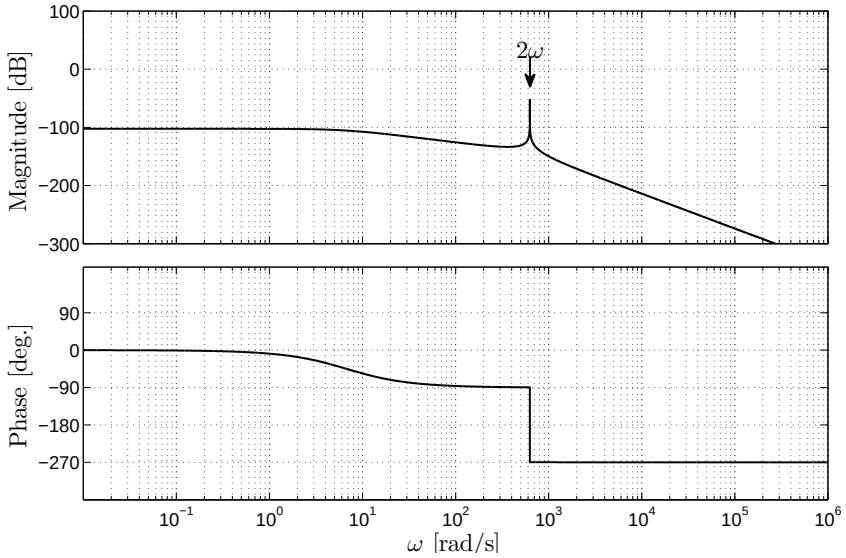

Figure 4.10: Bode diagram for the open-loop transfer function $\ell(s)$ without cancellation of the low frequency MMC leg pole.

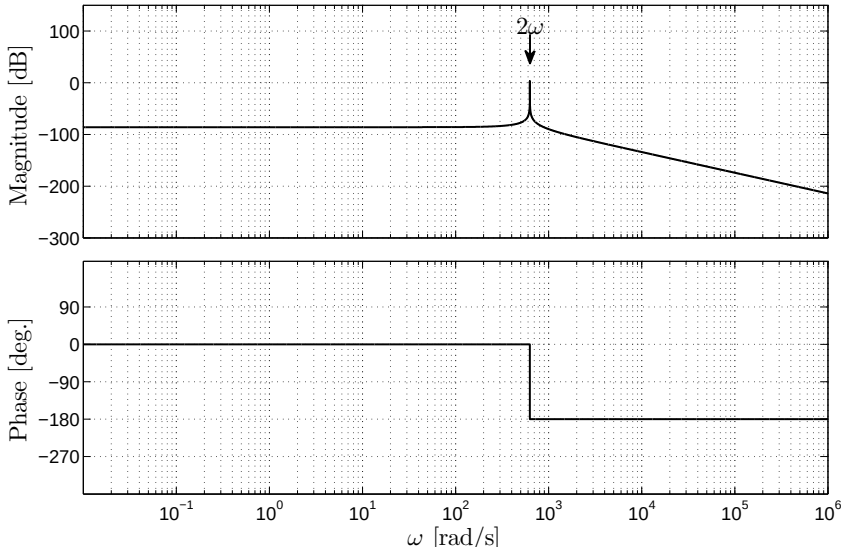

Figure 4.11: Bode diagram for the open-loop transfer function $\ell(s)$ with cancellation of the low frequency MMC leg pole.

Figures 4.10 and 4.11 show the bode diagram for $\ell(s)$ with and without the pole cancellation, respectively, using the same parameters as those of the example system described in Section 2.4.1.

It is noted that the pole cancellation moves the $\ell(s)$ phase to -180 for high frequencies. This means a phase margin of zero, that is, the system is unstable.

To increase the $\ell(s)$ phase margin for high frequencies, a zero at the origin is added. Also, the added zero will decrease the gain for the circulating current dc component, I_{cm}^0. Thus, a

zero at the origin is added to $K(s)$, changing it to

$$K(s) = \frac{s\left(s + \frac{R}{L}\right)}{s^2 + 4\omega^2} \tag{4.22}$$

Thus, $\ell(s)$ becomes

$$\ell(s) = \frac{s/L}{s^2 + 4\omega^2} \tag{4.23}$$

and its bode diagram is shown by Fig. 4.12.

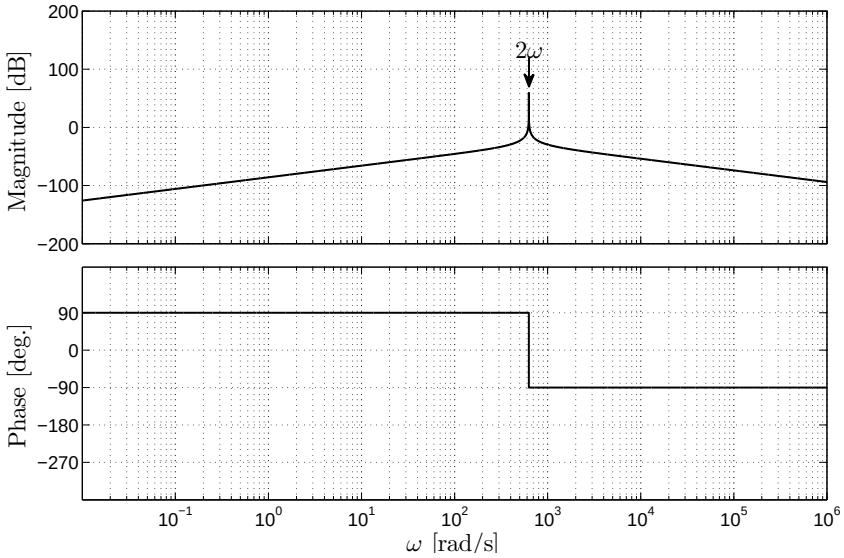

Figure 4.12: Bode diagram for the open-loop transfer function $\ell(s)$ with pole cancellation and a zero at the origin.

Adding a gain h to $\ell(s)$ yields

$$K(s) = h\frac{s\left(s + \frac{R}{L}\right)}{s^2 + 4\omega^2} \tag{4.24}$$

Simulations have shown that the circulating current control is not completely decoupled from the ac-side terminal current control, since both controls act upon n_1 and n_2, as (4.11) and (4.12) show. Further, the compensator $K(s)$ features a pair of complex poles, indicating that an oscillatory response is expected from it. If the transient oscillation in $\ell(s)$ drives the value of n_1 or n_2 to higher than M, the control becomes saturated and the system becomes unstable. Therefore, the gain h is used to avoid such saturation.

Fig. 4.13 shows the bode diagram using, as an example, the system described in Section 2.4.1, assuming a $h = 0.2$.

4.3 Proposed feedforward control strategy for circulating current suppressing

As it was shown in Chapter 2, the circulating current is formed by the even harmonics in the arm voltages, which are formed, in turn, by the integration of the arm current in the submodule

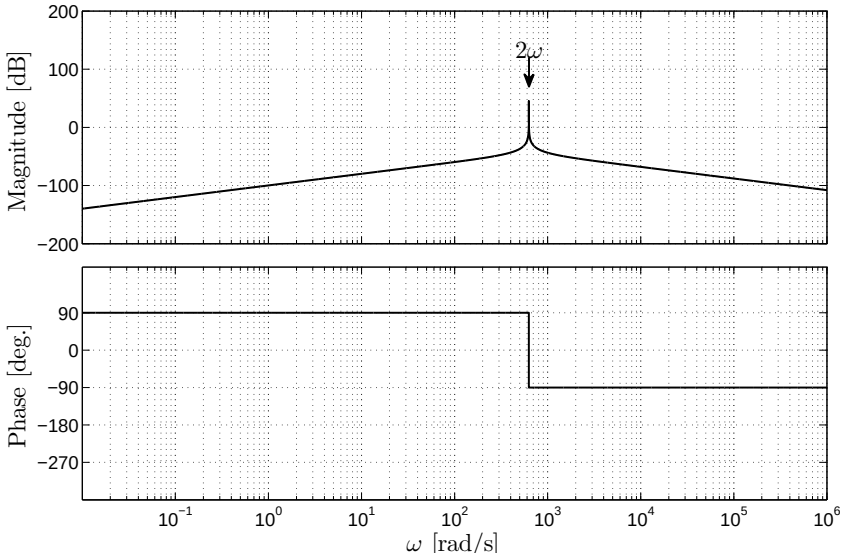

Figure 4.13: Bode diagram for the open-loop transfer function $\ell(s)$ with pole cancellation and a zero at the origin for $h = 0.2$.

capacitor. The arm voltage even harmonics are originated first, from the integration of the ac-side terminal current, and then have their amplitude increased by the integration of the circulating current in the submodule capacitor following a geometric series trend, as described in Section 2.3.1. Thus, if a feedforward signal is designed to cancel the action of the integration of the ac-side terminal current in the submodule capacitance, the even harmonics in the arm voltages will not appear, and the circulating current will remain zero.

The proposed feedforward control strategy is based on the off-line calculation of the steady-state magnitude of the leg voltage, $\frac{(v_1+v_2)}{2}$, for an $\widehat{I_{cm}} = 0$, and its use as a circulating current suppressing action. Thus, eliminating i_{cm}, $(v_1 + v_2)^{it}$, and $(v_1 + v_2)^{i_{cm}}$ between (2.56), (2.58), (2.62), and (2.66), and assuming a suppressed circulating current, $\widehat{I_{cm}} = 0$, and a stable system, that is, ramp components cancelled, yields

$$\frac{(v_1 + v_2)}{2} = -\frac{M}{4\omega C}\sqrt{\left(\frac{3\widehat{m}\widehat{I}cos\varphi}{4} - I_{cm}^0\widehat{m}^2\right)^2 + \left(\frac{3\widehat{m}\widehat{I}sin\varphi}{4}\right)^2} \tag{4.25}$$

Let e_{cm} be enhanced to

$$e_{cm} = (\widehat{e_{cm}} + e_0)sin(2\omega t + \varphi_0) \tag{4.26}$$

where e_0 and φ_0 correspond to the proposed feedforward action in the amplitude and phase of e_{cm}.

The circulating current modulating function is denoted by $(e_{cm})_{nf}$, instead of e_{cm}, when it is desired to represent only the CCSC action.

The feedforward control amplitude must cancel the magnitude of $\frac{(v_1+v_2)}{2}$, thus

$$e_0 = \frac{M}{4\omega C}\sqrt{\left(\frac{3\widehat{m}\widehat{I}cos\varphi}{4} - I^0_{cm}\widehat{m}^2\right)^2 + \left(\frac{3\widehat{m}\widehat{I}sin\varphi}{4}\right)^2} \tag{4.27}$$

and the phase φ_0 is given by

$$\varphi_0 = \arctan\left(\frac{\frac{3\widehat{m}\widehat{I}cos\varphi}{4} - I^0_{cm}\widehat{m}^2}{\frac{3\widehat{m}\widehat{I}sin\varphi}{4}}\right) \tag{4.28}$$

which is approximated by

$$\varphi_0 = 90 - \varphi \tag{4.29}$$

Fig. 4.14 shows the block diagram of the control loop for phase *a* with the feedforward control strategy.

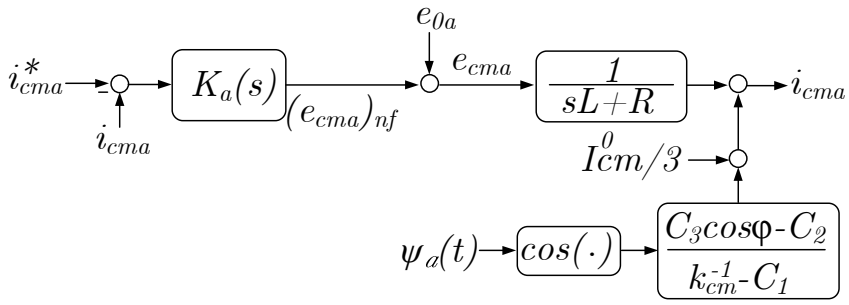

Figure 4.14: Block diagram for the i_{cm} control loop of phase *a*, with feedforward control strategy action.

4.4 Feedforward control strategy validation

The back-to-back system from Section 2.5, Fig. 2.16, is used here for the simulation of the validation of the proposed feedforward control strategy. Except that, in this section, two back-to-back systems, with identical parameters, are taken into account. The first system, referred to as System I, uses a CCSC strategy plus the feedforward proposed in Section 4.3, whereas System II uses the same CCSC strategy, with the exception that the proposed feedforward is not applied. Further, each system is divided in three cases. Case I represents the system in which the PI compensator in *dq*-frame, described in Section 4.2.1, is applied to suppress the circulating current, whereas Case II represents the system in which the resonant compensator, described in Section 4.2.2, is used. In Case III, only the proposed feedforward is used to suppress the circulating current, that is, there is no aid from any other control strategy. For a better understanding, Table 4.1 shows the aforementioned classification. All cases use the ac-side terminal current control strategy described in Section 4.1.

Table 4.1: Classification of cases and systems simulated

Case	System	CCSC strategy
I	I	PI compensator in *dq*-frame plus feedforward
	II	PI compensator in *dq*-frame
II	I	Resonant compensator plus feedforward
	II	Resonant compensator
III	I	Only feedforward
	II	No suppressing action

4.4.1 Case I - Back-to-back HVDC system with *dq*-frame PI and feedforward control

Fig. 4.15 shows the circulating current, the CCSC control signal, $(e_{cm})_{nf}$, the submodule capacitor voltage for capacitor 3 of the upper arm, and the ac-side terminal current for phase *a* of the inverter station for systems I and II.

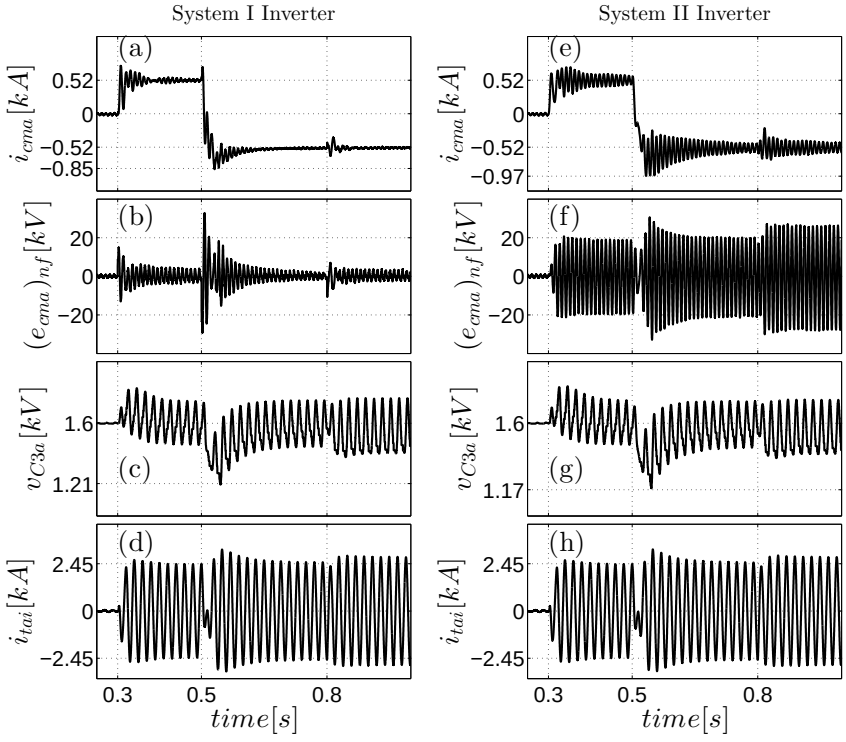

Figure 4.15: Circulating current, CCSC action, submodule capacitor voltage, and ac-side terminal current for phase *a* of the inverter station of systems I and II for Case I.

At $t = 0.3$ *s*, the control reference for the ac-side terminal current control changes from zero to 2.45 *kA*, corresponding to a power of 1000 *MW* exchanged with the grid. At this same moment, the CCSC is activated for both systems. Then, at $t = 0.5$ *s*, the control reference for

the ac-side terminal current is changed to $-2.45\ kA$, corresponding to an exchanged power of $-1000\ MW$. At $t = 0.8\ s$, the control reference for the ac-side terminal current is modified to allow a reactive power of 500 $MVAr$ to be absorbed from the grid.

It is noted that the addition of the proposed feedforward, i.e., System I, increases the damping action of the CCSC. This damping action is observed in the circulating current, Fig. 4.15 a, and submodule capacitor voltage, Fig. 4.15 c. Further, the proposed feedforward unloads the control action, observed in Fig. 4.15 b, diminishing the chances for control saturation.

Figures 4.16 and 4.17 show the dc-side voltage, the active power, and the *dq* components of the ac-side terminal current for both the rectifier and the inverter of systems I and II, for the same aforementioned disturbances.

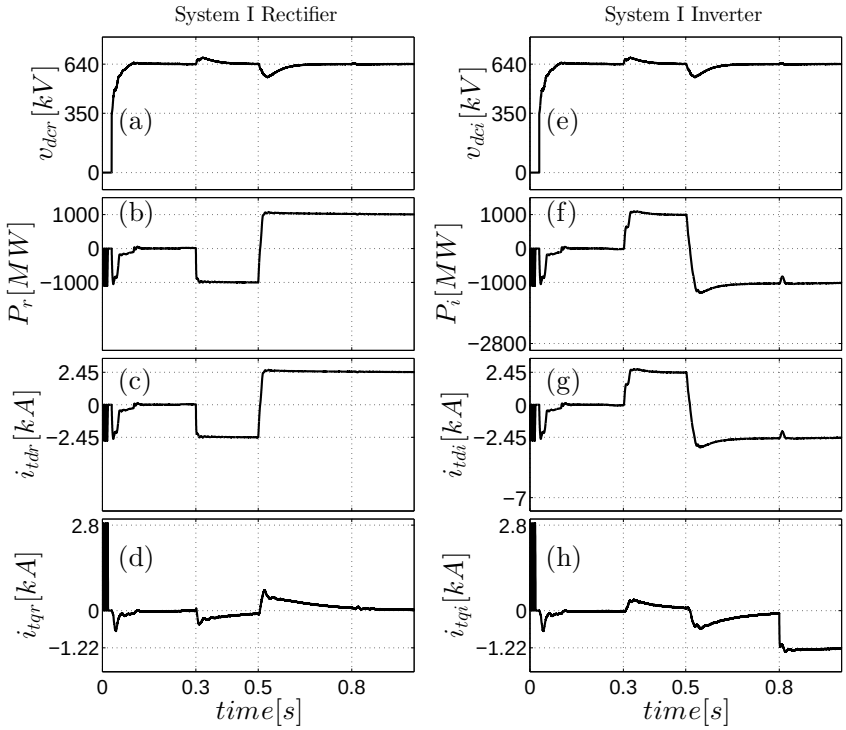

Figure 4.16: dc-side voltage, active power, and the *dq* components of the ac-side terminal current for both the rectifier and the inverter of System I for Case I.

One can observe that even though System I presents a higher damping action in the circulating current than that of System II, the ac-side terminal current, the active power, and the dc-side voltage waveforms exhibit, visually, the same transient behavior.

4.4.2 Case II - Back-to-back HVDC system with resonant and feedforward control

Fig. 4.18 shows the circulating current, the CCSC action, $(e_{cm})_{nf}$, the submodule capacitor voltage for capacitor 3, and the ac-side terminal current for phase *a* of the inverter station for systems I and II.

Both systems are submitted to the same disturbances as those from Case I, with the exception that the power exchanged with the grid is not reversed at $t = 0.5\ s$.

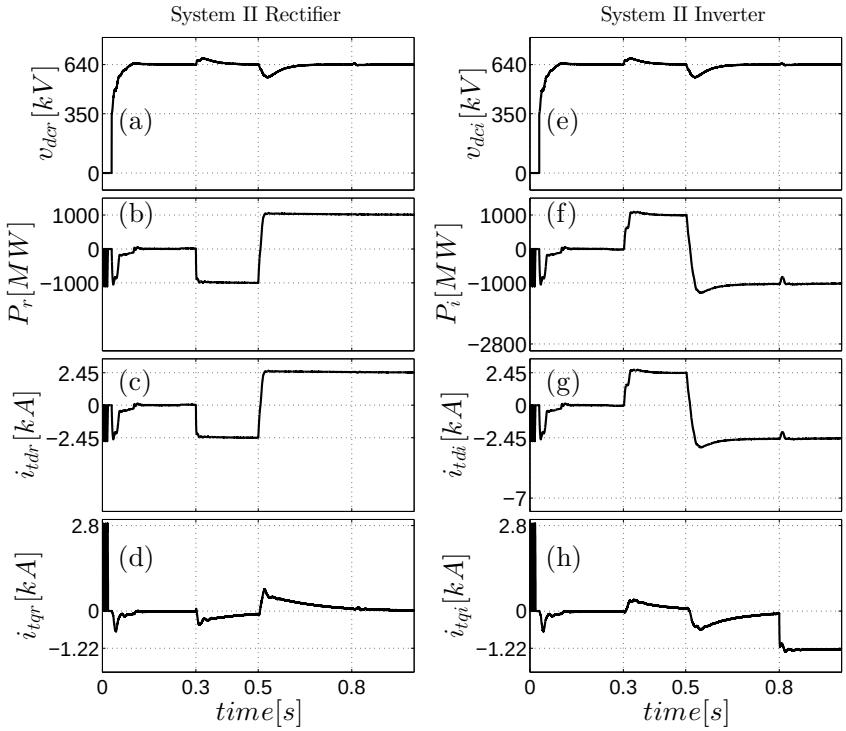

Figure 4.17: dc-side voltage, active power, and the *dq* components of the ac-side terminal current for both the rectifier and the inverter of System II for Case I.

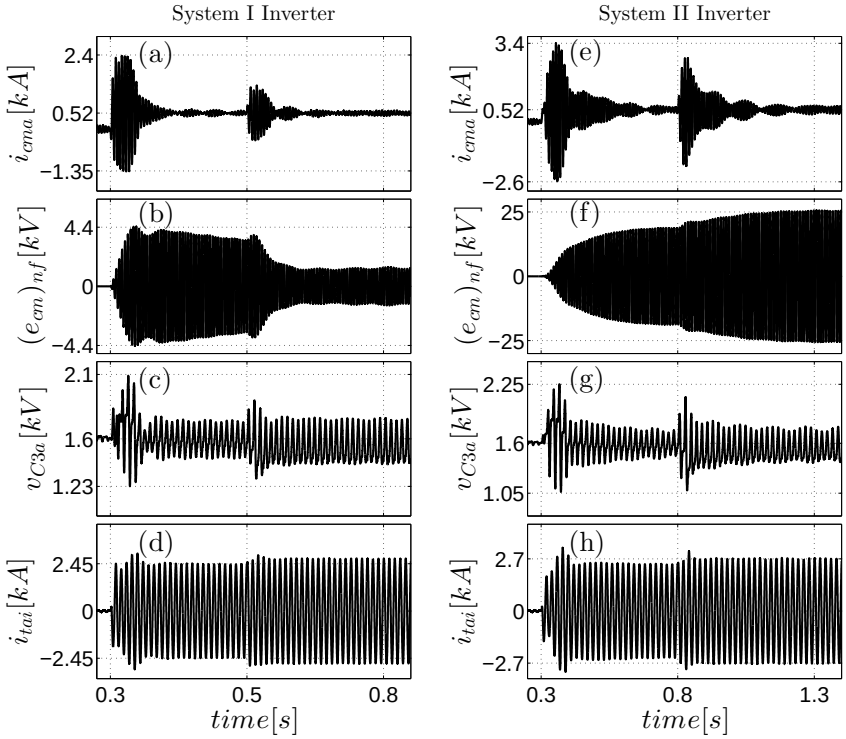

Figure 4.18: Circulating current, CCSC action, submodule capacitor voltage, and ac-side terminal current for phase *a* of the inverter station of systems I and II for Case II.

As it happens for Case I, the addition of the proposed feedforward, in System I, increases the damping action of the CCSC and decreases the required action from $(e_{cm})_{nf}$.

Figures 4.19 and 4.20 show the dc-side voltage, the active power, and the *dq* components of the ac-side terminal current for both the rectifier and the inverter of systems I and II.

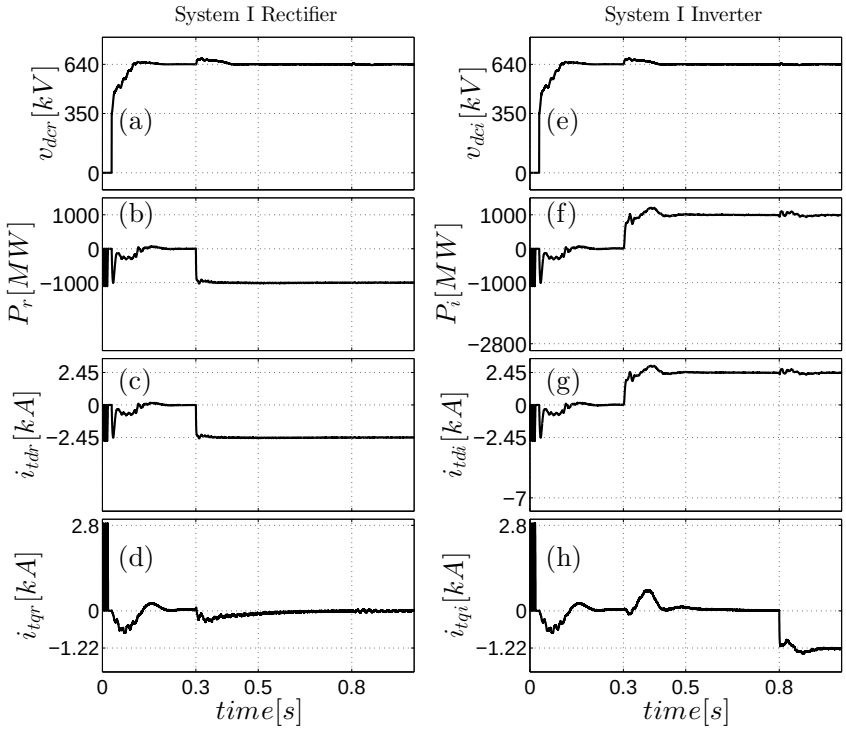

Figure 4.19: dc-side voltage, active power, and the *dq* components of the ac-side terminal current for both the rectifier and the inverter of System I for Case II.

Different than what it was observed in Case I, the high amplitude reached by the transient period of the circulating current in System II, has a bigger impact in the transient of the ac-side terminal current and the active power, for the same system, in comparison to the impact generated by the circulating current transient in System I.

4.4.3 Case III - Back-to-back HVDC system with feedforward control only

For this case, only the proposed feedforward is used to suppress the circulating current of the inverter station in System I, whereas in System II, no suppressing action is used, and the circulating current is allowed to assume its natural amplitude. For both systems, the CSCC of the rectifier station is activated.

Fig. 4.21 shows the waveforms of the circulating current, the submodule capacitor voltage for capacitor 3 of the upper arm, and the ac-side terminal current for phase *a* of the inverter station of systems I and II.

It is noted that without a auxiliary control strategy, as cases I and II, the circulating current takes much longer, in comparison to the referred cases, to decay to I_{cm}^0 value.

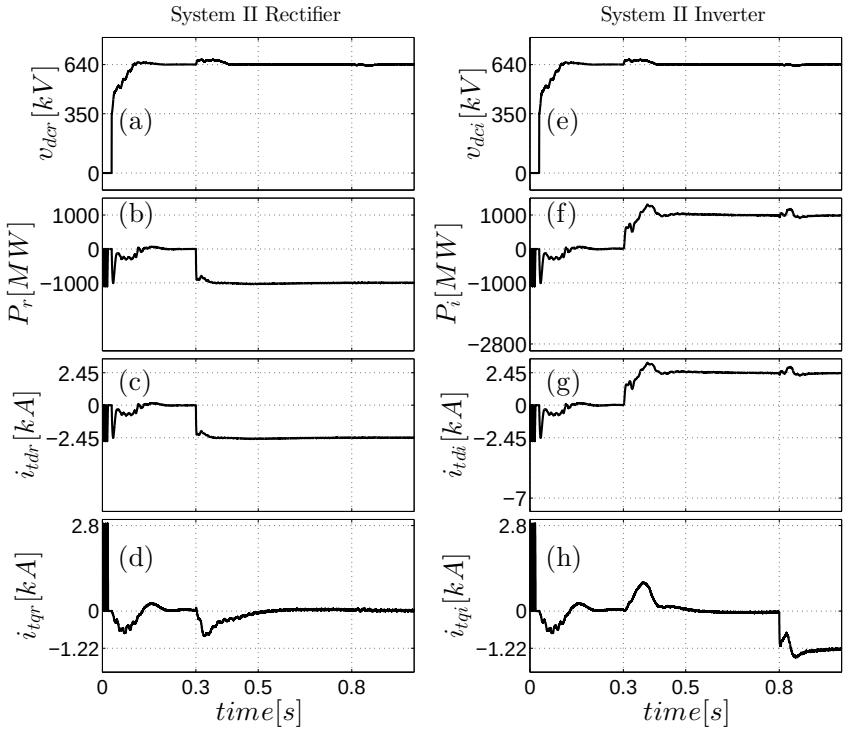

Figure 4.20: dc-side voltage, active power, and the *dq* components of the ac-side terminal current for both the rectifier and the inverter of System II for Case II.

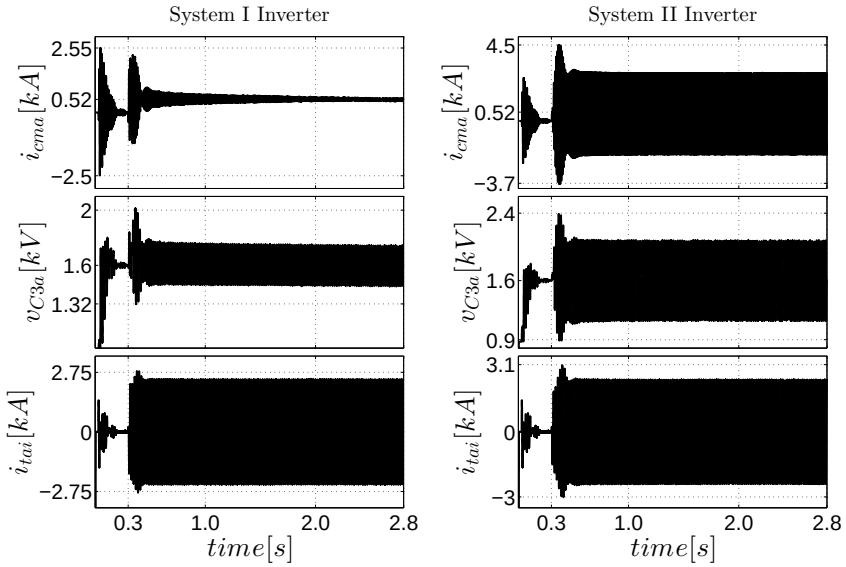

Figure 4.21: Circulating current, submodule capacitor voltage, and ac-side terminal current for phase *a* of the inverter station of systems I and II for Case III.

Fig. 4.22 shows the steady-state zoomed view of the waveforms displayed in Fig. 4.21.

At $t = 0.3$ *s*, the control reference for the ac-side terminal current control changes from zero to 2.45 *kA*, corresponding to a power of 1000 *MW* exchanged with the grid. At the same time, the feedforward is activated for System I, whilst, for System II, the circulating current is

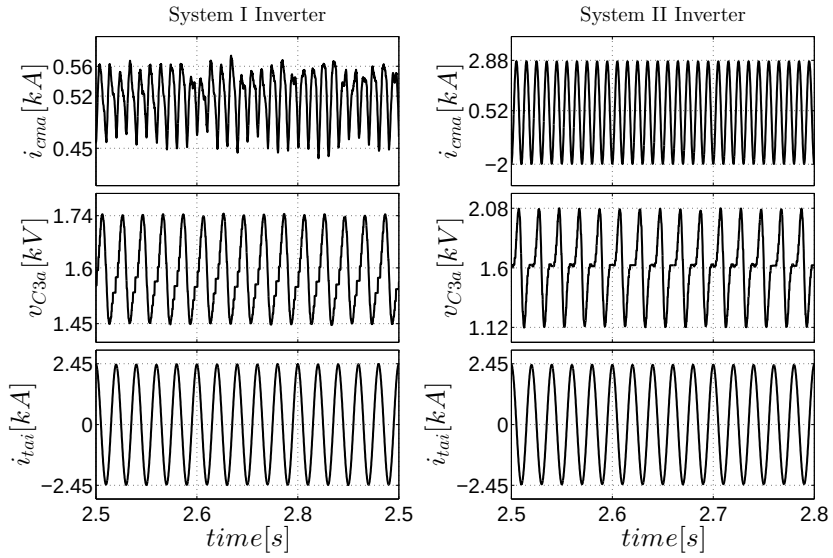

Figure 4.22: Circulating current, submodule capacitor voltage, and ac-side terminal current for phase *a* of the inverter station of systems I and II for Case III, zoomed view.

allowed to run free, that is, to assume its natural amplitude.

Fig. 4.22 shows that the feedforward action alone is capable of suppressing most of the circulating current (98%). The CCSC action is used to suppress the remaining circulating current, that exists due to small errors in the off-line calculation. In the case of practical implementations, deviations of the parameters values, such as arm inductances and resistances, used in the off-line calculation, is also corrected by the CCSC.

4.5 Summary and Conclusions

In this chapter, two strategies for suppressing the circulating current in the MMC leg were described. In addition, a feedforward control strategy, to increase the CCSC damping action, was proposed. The proposed feedforward control strategy was tested, through simulation, for both CCSC strategies described. The simulation results showed that the proposed feedforward control strategy decreased the stabilization time (increased damping) for the circulating current and submodule capacitor voltage, in comparison to cases where the proposed control strategy was not used.

Chapter 5

Lattice Modular Multilevel Converter

The need for grid integration and long-distance transmission of renewable energy resources requires the use of overhead HVDC transmission lines. As these lines are susceptible to faults, the MMC can no longer be based on HBSM. Thus, FBSM has been considered as the building block of the MMC, due to its dc-side fault handling capability, given by the fact that, when the switches have their gate pulses blocked, the IGBTs anti-parallel diodes insert the submodule capacitor in the MMC arm, with its voltage polarity against the grid voltage. This feature blocks the dc-side fault current from circulate through the MMC arms. However, with the FBSM, the number of switches in series with the MMC arm current path is doubled, generating higher power losses. This chapter proposes a new topology for the MMC, the *Lattice Modular Multilevel Converter* (LMMC) which aims to bring down, as much as possible, the number of switches connected in series with the arm current path, to decrease the conduction power losses, while maintaining the same dc-side fault handling capability as that of the FBSM. It is shown in this chapter that the proposed topology is superior to an HBSM-based MMC from the power losses perspective.

5.1 Proposed MMC: The LMMC

Figure 5.1 shows a schematic diagram of the LMMC, based on the assumption that $M + 1$ levels (M is assumed to be even) are to exist in the ac-side terminal voltage. As the figure shows, the upper arm of the converter, Arm 1, hosts $M - 1$ identical 5-terminal *networks*, M capacitors, and two half-bridge converters. Thus, starting from the top of an arm, Fig. 5.1 shows that, except for the first and last networks, the *input port* of each network, which is identified by respective terminals a and b of that network, is connected in parallel with the *output port* of the next network, which is identified by the corresponding terminals c and d of the network. However, terminals a and b of the first network are connected to, respectively, the positive and negative dc-side terminals of a half-bridge converter, the *positive half-bridge*, represented by switches S_1 and S_2. Also, terminals c and d of the last network are connected to the positive and negative dc-side terminals of another half-bridge converter, the *negative half-bridge*, which is constituted by switches S_3 and S_4. Figure 5.1 also shows that, with the exception of the last two networks, terminal h of each network is connected to terminal a of the network after the next. Therefore, terminal h of the last network in each arm is not

required. Figure 5.1 further shows that the input port of the first network, the output port of the last network, and each pair of interconnected ports are connected in parallel with a capacitor whose voltage is represented by v_{Cj} ($j = 1, 2, ..., M$). The M capacitors are assumed to all have the same (nominal) capacitance. The lower arm, Arm 2, has the same structure and properties as the upper arm. All node voltages are expressed with reference to the *dc-side midpoint*, 0, which may be a physical or a virtual node.

Each network is a circuit of three fully controllable electronic switches, S_{un}, S_{dn}, and S_{cn}, as shown in Fig. 5.2 for the nth network ($n = 1, 2, ..., M-1$). The electrical connection associated with switch S_{un} and terminals b_n and c_n is referred in this paper to as a *positive regular link*, whereas the connection between terminals a_n and d_n through switch S_{dn} is called a *negative regular link*; they may simply be referred to as *regular links*. In addition, the connection associated with switch S_{cn} and terminals b_n and h_n is referred to as a *high-efficiency link*. Switches S_{un} and S_{dn} must be of the reverse-conducting type, e.g., IGBTs, whereas the switch for a high-efficiency link, S_{cn}, must be a bidirectional reverse-blocking switch. Thus, as indicated in Fig. 5.2, it is assumed in this paper that S_{cn} is implemented by anti-parallel connection of two reverse-blocking IGCTs, such as those featured in [83]-[92]. Even though the IGCT is the preferred switch in applications with low switching frequencies, where the conduction power losses are dominant [84], [85], it is assumed to only be adopted for the high-efficiency links of the LMMC, due to its relatively high cost; the other switches are assumed to be of the IGBT type. Since terminal h is not used in the last network, switch $S_{c(M-1)}$ is not required.

It should be pointed out that, in each network only one switch at a time is permitted to be *on*. Thus, for example, if S_{cn} is turned *on*, S_{un} and S_{dn} are kept *off*, and so on. Also, the switches of each half-bridge converter are complementary, that is, only one of them is permitted to be *on* at a time.

Fig. 5.3 shows a 5-level LMMC arm schematic diagram, where the black lines represent the regular links and the blue lines the high-efficiency links. Fig. 5.3 further shows that the LMMC arm topology can be visualized as an imaginary cube (formed by the red lines), where each edge represents a capacitor, and the faces are formed by lattices (regular links). The high-efficiency links can be seen connecting the faces of the cube through "shortcuts", crossing the cube internally. It is important to point out that only the black and blue lines, in Fig. 5.3, represent actual electric connections, i.e., current paths.

As it is the case for a conventional MMC, the number of level that the LMMC is capable of producing in v_t is correlated to M. Therefore, for a high density LMMC, M must be high, and the LMMC arm topology becomes more and more similar to a cylinder, from a top view stand point, as it can be observed in Fig. 5.4 for a 7-level LMMC. Fig. 5.4 also shows that the high-efficiency links are better observed from the top view stand point.

Fig. 5.5 illustrates the top view for an LMMC arm with increasing values for M. It is noted that the high-efficiency links increase considerably with M, which decreases the LMMC power loss, as it is explained in detail in Section 5.5.

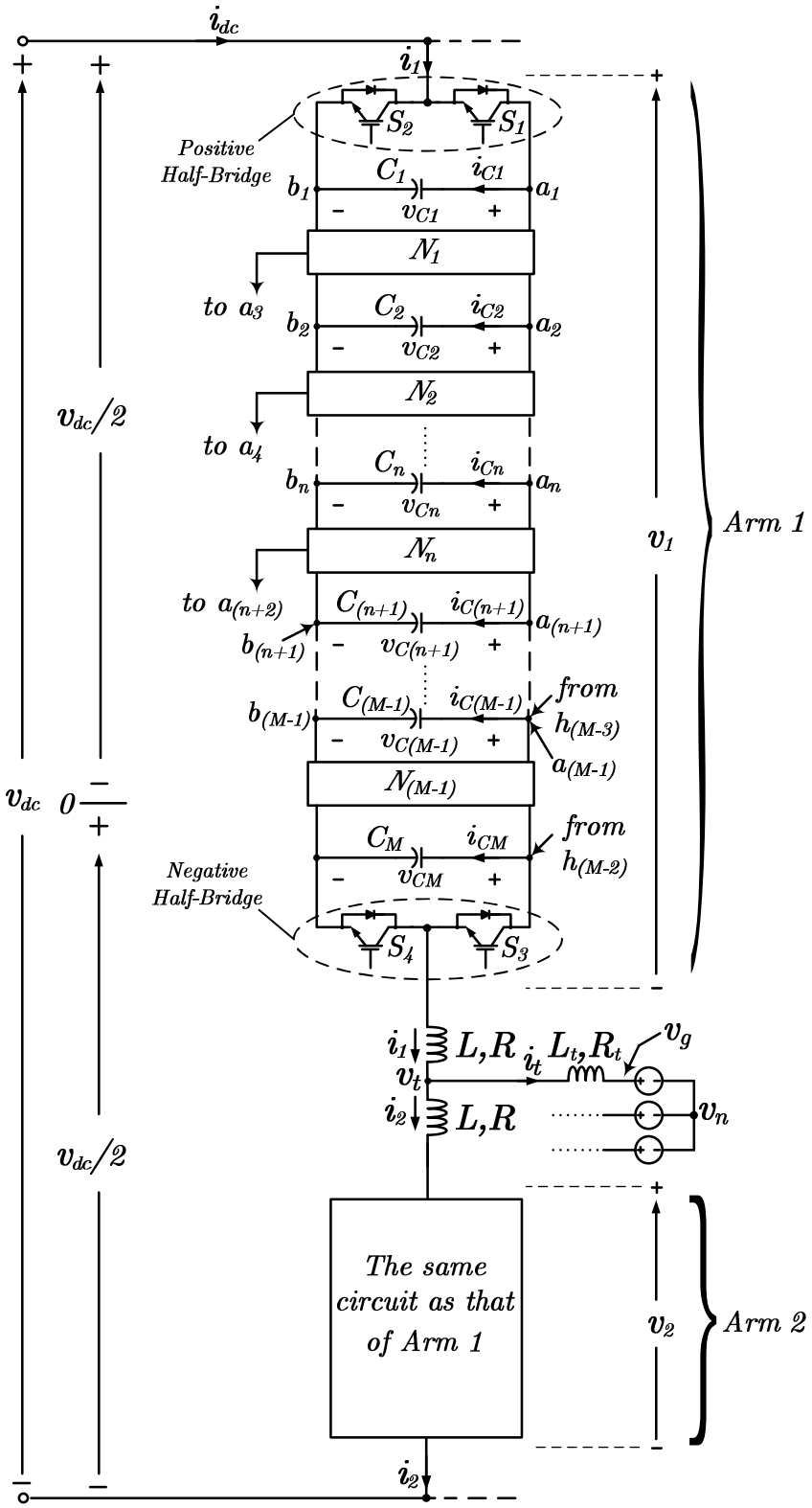

Figure 5.1: Schematic diagram for one leg of the proposed MMC, the *LMMC*.

5.2 Principles of Operation of the LMMC

5.2.1 Normal operation

Essentially, synthesis of the ac-side terminal voltage, v_t, and consequently the ac-side terminal current, i_t, boils down to the synthesis of arm voltages, v_1 and v_2 (see Fig. 5.1). In the LMMC,

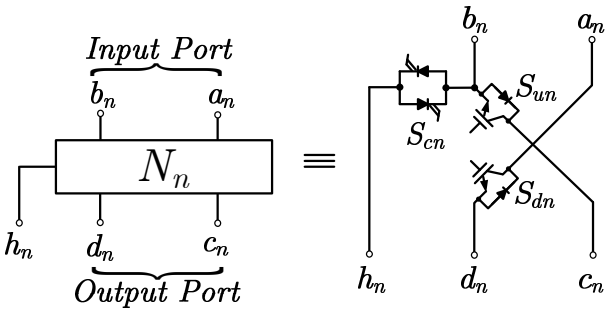

Figure 5.2: Circuit of the *network*, the building block of the LMMC ($n = 1, 2, ..., M-1$).

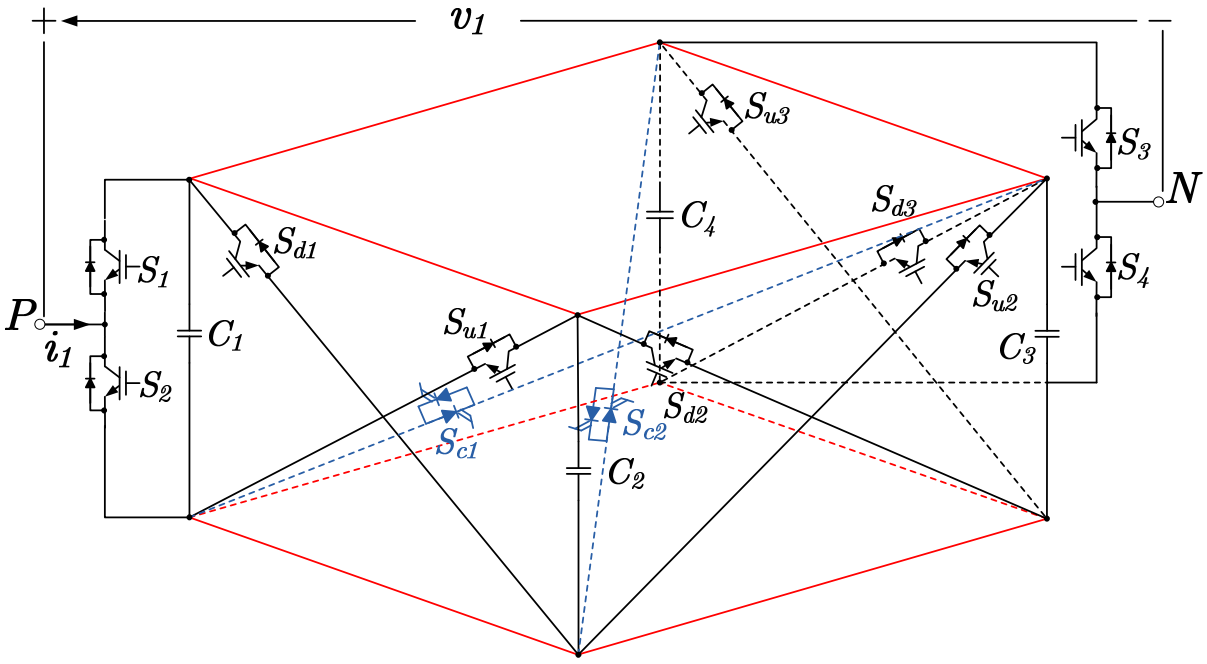

Figure 5.3: Schematic diagram of the upper arm circuit of a 5-level LMMC.

a particular arm voltage level is synthesized by inserting an appropriate number of capacitors in series with the path for the corresponding arm current, i_1 or i_2, in the same way as that of the conventional MMC described in Chapter 2. Therefore, the capacitors that are not required are *withdrawn*, that is, they are left out of the arm current path, by diverting the current away from them, and by redirecting the current through alternative regular links and/or high-efficiency links. Whenever possible, high-efficiency links are preferred over the regular links, due to their lower conduction power loss, and are turned *on* based on the algorithm described in Section 5.3. Since a desired ac-side terminal voltage level can almost always be synthesized by various combinations of a certain number of inserted capacitors, whether or not a capacitor is inserted also depends on the voltage across the capacitor (which must be maintained at about a nominal value). The LMMC assumes and requires the same nominal voltage for all capacitors.

For ease of visualization, and without loss of generality, the aforementioned principles of operation are illustrated for a 5-level LMMC in Fig. 5.6, in which a two-dimensional view of the LMMC upper arm is presented. In Fig. 5.6 the internal circuitry of the constituting

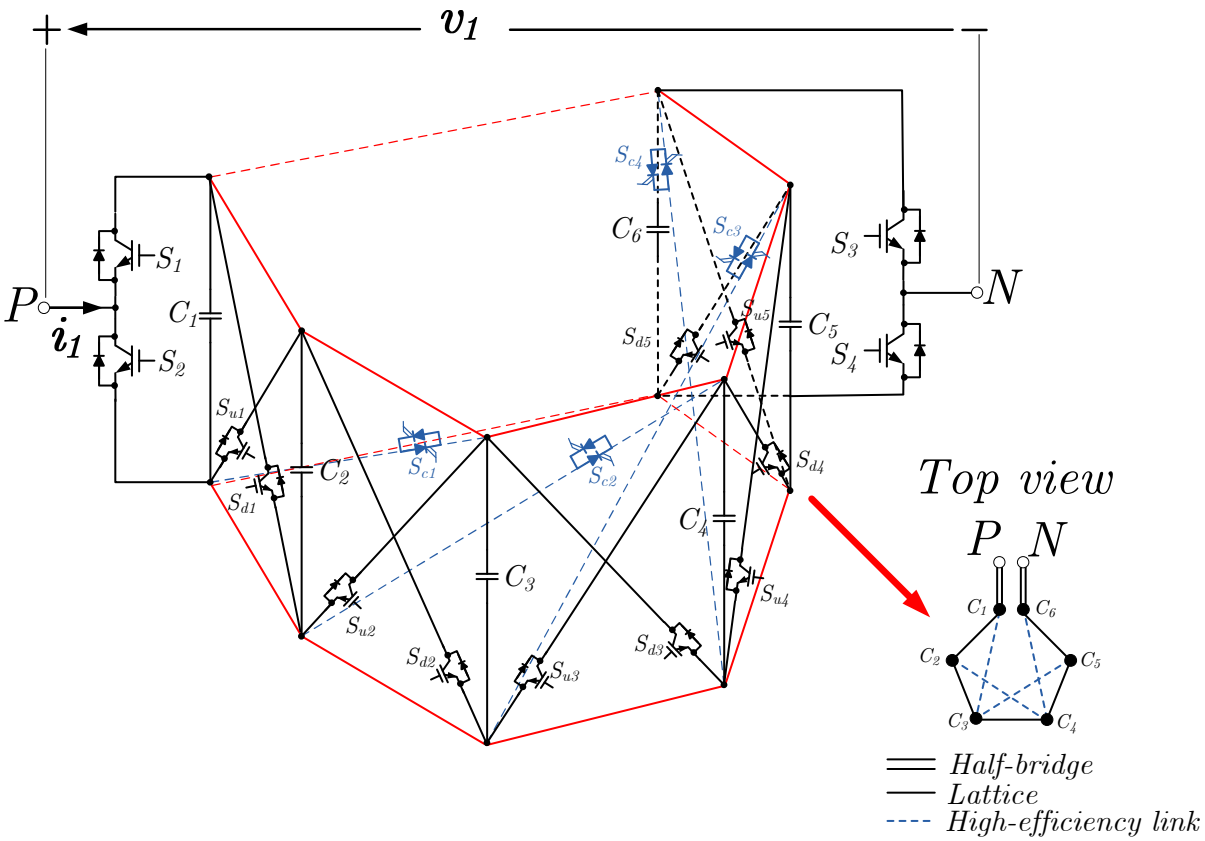

Figure 5.4: Schematic diagram of the upper arm circuit of a 7-level LMMC and its top view.

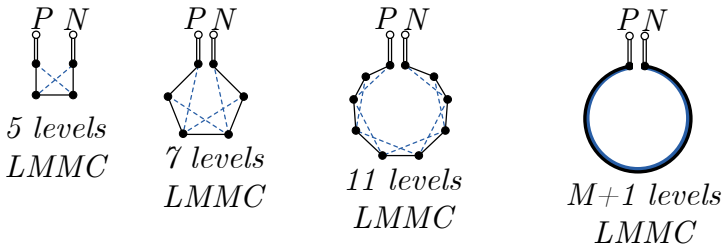

Figure 5.5: Top view of an LMMC arm for different values of M.

three networks are shown explicitly. For easiness of analysis, the two-dimensional view of the LMMC arm is adopted in this thesis.

Figure 5.7 illustrates a case where the maximum arm voltage is required and, therefore, the capacitors are all inserted (the thick line indicates the arm current path). In this case, no high-efficiency link can be tuned on and placed in series with the arm current path. By contrast, let us consider a situation in which half of the maximum arm voltage is to be synthesized, hence two inserted capacitors. Let us then assume that the control has specifically required capacitors C_3 and C_4 to be inserted. Then, a high-efficiency link can be turned on, as shown in Fig. 5.8, to withdraw capacitors C_1 and C_2 out of the current path. Alternatively, if the control requires C_2 and C_3 to be out of the current path, then no high-efficiency link can be used, but only regular links are employed, as Fig. 5.9 indicates.

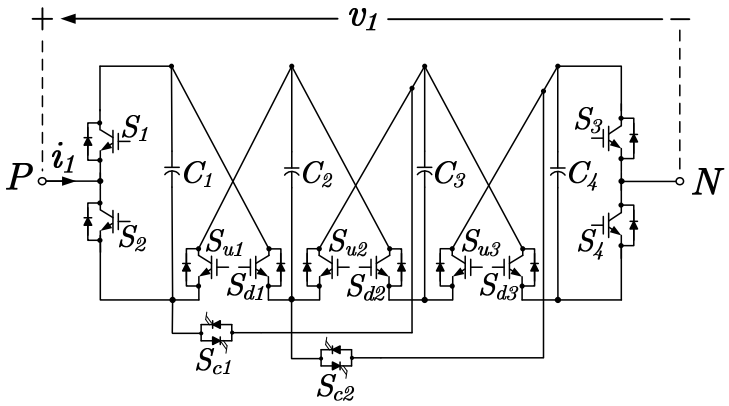

Figure 5.6: Schematic diagram of the upper arm circuit of a 5-level LMMC, two-dimensional view.

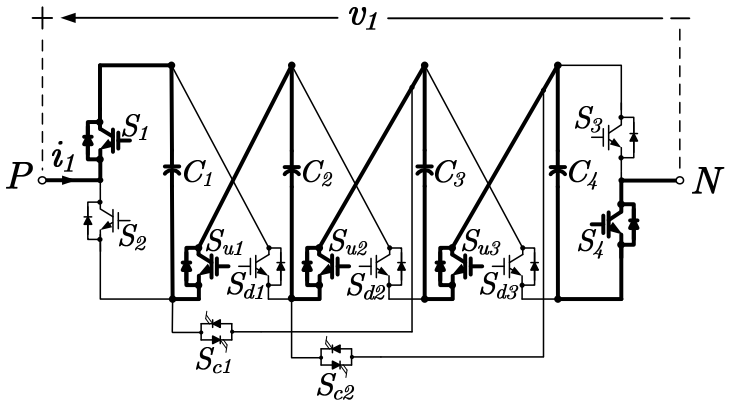

Figure 5.7: The current path for the upper arm of the 5-level LMMC of Fig. 5.6 if all capacitors must be inserted.

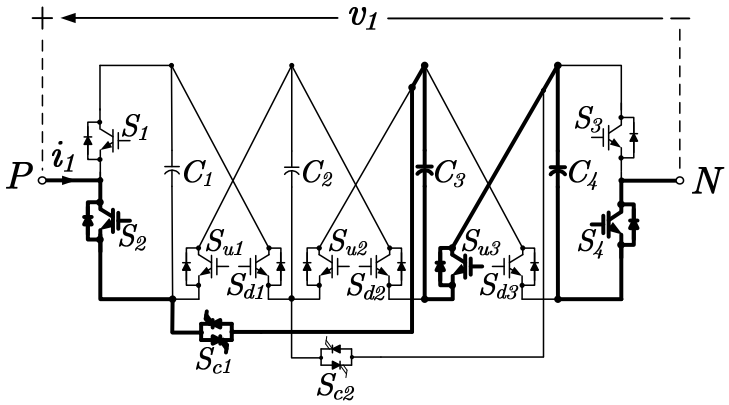

Figure 5.8: The current path for the upper arm of the 5-level LMMC of Fig. 5.6 if only capacitors C_3 and C_4 must be inserted.

For the circuit of Fig. 5.8, the number of switches in series with the arm current path is 4, due to the high-efficiency link that is on. This is the same number of switches as that in a HBSM-based MMC featuring 5 levels in its ac-side terminal voltage. By contrast, in the cases represented by Fig. 5.7 and Fig. 5.9, the number of switches in series with the arm current

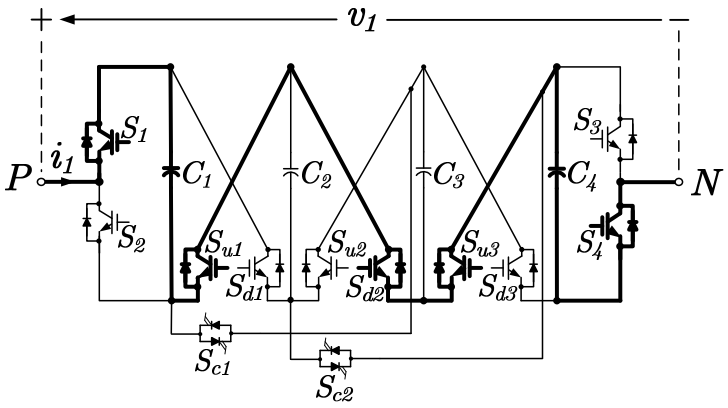

Figure 5.9: The current path for the upper arm of the 5-level LMMC of Fig. 5.6 if only capacitors C_1 and C_4 must be inserted.

path is 5, which is higher than that in the HBSM-based MMC. However, the situation where no high-efficiency link could be turned on is less common. Therefore, the 5-level LMMC is almost the same as the HBSM-based MMC, in terms of the number of switches in series with the arm current path. However, for an LMMC with a large M, which is typical in HVDC systems, the LMMC features a lower number of switches for each ac-side terminal voltage level than an equivalent HBSM-based MMC, due to the possibility of turning on a large number of high-efficiency links. Therefore, the LMMC, in general, offers a higher efficiency than an equivalent HBSM-based MMC, as Section 5.5 explains.

5.2.2 Operation under a dc-side fault

Subsequent to a dc-side fault, the switches are all turned *off* by the control. This, effectively, connects the capacitors in series with the anti-parallel diodes of the reverse-conducting switches of the negative regular links, while the high-efficiency link are open, as shown in Fig. 5.10 for the LMMC of Fig. 5.6. The LMMC in this condition can therefore be represented by an equivalent circuit, following the same scheme presented in Fig. 3.8. Therefore, assuming that prior to the fault the capacitor voltages have reached the steady-state value V_{dc0}/M (where V_{dc0} signifies the pre-fault steady-state value of v_{dc}), the diodes turn *off* subsequent to the fault and the arm current drops to zero, unless the grid line-to-line voltage, added to the inductor voltage, exceeds $2V_{dc0}$.

5.3 Switching Scheme of the LMMC

The switching scheme of the LMMC adopts the same NLC modulation strategy described in chapters 2 and 3, to determine the arm voltages that must be synthesized for a given ac-side terminal voltage. The switching scheme also employs the same sorting algorithm described in Chapter 3, in its VBA, to determine what specific capacitors must be inserted, to ensure that the capacitors all have voltages about the value $\overline{v}_c$. Thus, the output of the switching scheme is an M-element vector of the form $\mathbf{x} = [x_1, x_2, x_3, ..., x_{(M-1)}, x_M]$, for each arm. In the vector, referred in this thesis to as the *VBA array*, element x_j ($j = 1, 2, ..., M$) represents the state, inserted or withdrawn, of the jth capacitor in the host arm. Thus, $x_j = 1$ corresponds to an

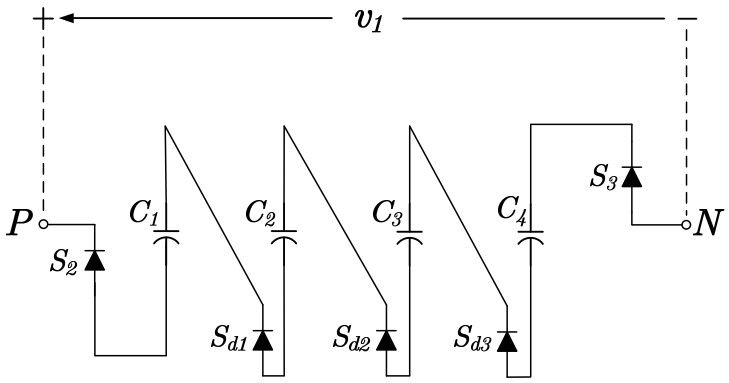

Figure 5.10: Schematic diagram of the upper arm circuit of the 5-level LMMC of Fig. 5.6 when the switches are *off*, e.g., subsequent to a dc-side fault.

inserted capacitor, whereas $x_j = 0$ indicates a withdrawn capacitor. The *VBA array* is then used to determine what switches must be turned *on* in the corresponding arm, starting from capacitor C_1 to capacitor C_M. Thus, advancing the index j (corresponding to the jth capacitor) from 1 to $M-1$, the switching scheme determines the current path and the switches that must be turned *on*. Five cases are faced, as explained below, depending upon what network a switch belongs to:

5.3.1 Capacitor connected to *positive half-bridge*: $j = 1$ corresponding to C_1

The first capacitor, C_1, is connected to the LMMC arm through the positive half-bridge. Therefore, the switching scheme must generate the state for the switches S_1 and S_2. If C_1 is to be inserted, then S_1 must be turned *on*, whereas S_2 is turned *off*, and vice versa.

5.3.2 First Capacitor and Intermediate Capacitors: $1 \leq j \leq (M-3)$ corresponding to $C_1, C_2, ..., C_{(M-3)}$

The first capacitor is also connected to a network, as are capacitors $C_2, C_3, ..., C_{(M-1)}$. Capacitors $C_{(M-2)}$ and $C_{(M-1)}$ are subject to different rules for their insertion into the arm and, therefore, are discussed separately in Sections 5.3.3 and 5.3.4. The rules mentioned in this section apply only to capacitors $C_1, C_2, ..., C_{(M-3)}$.

If the *jth* capacitor is to be inserted, i.e., $x_j = 1$, the series connection to the $(j+1)$th capacitor can be established through switch S_{uj} (positive regular link). On the other hand, the series connection to the $(j+2)$th capacitor can be established through switch S_{cj} (high-efficiency link). As mentioned in Section 5.2.1, the connection through switch S_{cj} is preferred, but it is subject to the two following constraints:

1. If capacitor $C_{(j+1)}$ is to be inserted (i.e., if $x_{(j+1)} = 1$ in the VBA array), then if S_{cj} is activated, C_j is connected directly to $C_{(j+2)}$. Consequently, $C_{(j+1)}$ is automatically withdrawn from the arm, and the VBA array state of $x_{(j+1)} = 1$ cannot be complied with.

2. If capacitors $C_{(j+2)}$ and $C_{(j+3)}$ are to be withdrawn and inserted, respectively (i.e., if $x_{(j+2)} = 0$ and $x_{(j+3)} = 1$), then if switch S_{cj} is *on* while $C_{(j+2)}$ is withdrawn, the only available path for the current is through $S_{d(j+2)}$ (corresponding to a negative regular link). On the other hand, if $S_{d(j+2)}$ is *on*, there is no connection available to $C_{(j+3)}$. Thus, $C_{(j+3)}$ is forced to be withdrawn from the arm, and the VBA array state of $x_{(j+3)} = 1$ cannot be complied with.

In both aforementioned situations, the VBA array states for $C_{(j+1)}$ and $C_{(j+3)}$ cannot be obeyed if S_{cj} is used. Therefore, in these two situations, S_{cj} must be kept *off*, and, instead, switch S_{uj} is turned *on*.

If the *jth* capacitor is to be withdrawn, that is, if $x_{(j)} = 0$, the only available connection to $C_{(j+1)}$ is through S_{dj}. Hence, S_{dj} must be turned on.

5.3.3 Capacitor connected to the last *high-efficiency link*: $j = (M - 2)$ corresponding to $C_{(M-2)}$

If capacitor $C_{(M-2)}$ is to be inserted, then the activation of switch $S_{c(M-2)}$ is subject to only one of the two constraints described in Section 5.3.2; if $C_{(M-1)}$ is to be inserted, switch $S_{c(M-2)}$ must be kept *off*, and, instead, $S_{u(M-2)}$ is turned *on*. If $C_{(M-1)}$ is to be withdrawn, then $S_{c(M-2)}$ must be turned *on*.

If capacitor $C_{(M-2)}$ is to be withdrawn, then $S_{d(M-2)}$ must be turned *on*.

5.3.4 Capacitor before the last: $j = (M - 1)$ corresponding to $C_{(M-1)}$

For capacitor $C_{(M-1)}$, there is no switch $S_{c(M-1)}$ in the $(M - 1)$th network. Therefore, if $C_{(M-1)}$ is to be withdrawn, then $S_{d(M-1)}$ must be turned *on*. Otherwise, $S_{u(M-1)}$ must be turned *on*.

5.3.5 Capacitor connected to *negative half-bridge*: $j = M$ corresponding to C_M

For capacitor C_M, i.e., the last capacitor, the only switches left are the switches that form the negative half-bridge. Thus, if C_M is to be inserted, then S_4 must be turned *on*. Otherwise, S_3 must be turned *on*.

The rules explained in 5.3.1 to 5.3.5 are implemented mathematically by the equations

$$
Case1 \rightarrow \begin{cases} k_{S1} = \mathbf{x}_j \\ k_{S2} = 1 - \mathbf{x}_j \\ p_j = 0 \end{cases}
$$

$$
Case2 \rightarrow \begin{cases} p_j = p_{(j-1)}(1 - \mathbf{x}_j) \\ k_{S3} = [1 - \mathbf{x}_j]p_j \\ k_{S4} = \mathbf{x}_j + [1 - \mathbf{x}_j - p_j] \\ p_j = 0 \\ j = j + k_{Snu} + k_{Snd} + 2k_{Snc} + k_{S3} + k_{S4} \end{cases}
$$

$$
Case3 \rightarrow \begin{cases} p_j = p_{(j-1)}[1 - \mathbf{x}_j] \\ k_{Snu} = [\mathbf{x}_{(j+1)})(1 - p_j)] + (1 - R_{1001}) \\ k_{Snd} = [1 - \mathbf{x}_j]p_j \\ k_{Snc} = [(1 - \mathbf{x}_{(j+1)})(1 - p_j)]R_{1001} \\ p_j = k_{Snu} + k_{Snc} \\ j = j + k_{Snu} + k_{Snd} + 2k_{Snc} \end{cases}
$$

$$
Case4 \rightarrow \begin{cases} p_j = p_{(j-1)}[1 - \mathbf{x}_j] \\ k_{Snu} = \mathbf{x}_{(j+1)}(1 - p_j) \\ k_{Snd} = [1 - \mathbf{x}_j]p_j \\ k_{Snc} = [1 - \mathbf{x}_{(j+1)}](1 - p_j) \\ p_j = k_{Snu} + k_{Snc} \\ j = j + k_{Snu} + k_{Snd} + 2k_{Snc} \end{cases}
$$

$$
Case5 \rightarrow \begin{cases} p_j = p_{(n-1)}[1 - \mathbf{x}_j] \\ k_{Snu} = 1 - p_j \\ k_{Snd} = p_j \\ k_{Snc} = 0 \\ p_j = k_{Snu} + k_{Snc} \\ j = j + k_{Snu} + k_{Snd} + 2k_{Snc} \end{cases} \tag{5.1}
$$

where R_{1001} is the parameter given by

$$
\begin{aligned} R_{1001} =& (1 - \mathbf{x}_j) + \mathbf{x}_{(j+1)} + \mathbf{x}_{(j+2)} + [1 - \mathbf{x}_{(j+3)}] \\ & \forall R_{1001} \in [0, 1] \end{aligned} \tag{5.2}
$$

, and k_{S1}, for example, represents the state of switch S_1, and $k_{S1} = 1$ indicates an activated S_1, whereas $k_{S1} = 0$ indicates the opposite. In (5.1), p indicates the "route" being followed during the creation of the S_w, that is, the activation of the switches in a particular network depends on the utilization of the high-efficiency and regular links by the previous networks.

The implementation of (5.1), for an LMMC arm, gives rise to a *switching matrix*, which is a 5 x M matrix containing the state of all switches in an LMMC arm.

For a better understanding of the switching matrix, the following example is analysed: a 7-level LMMC upper arm switching controller, receives the VBA array $\mathbf{x} = [0, 1, 0, 1, 1, 0]$,

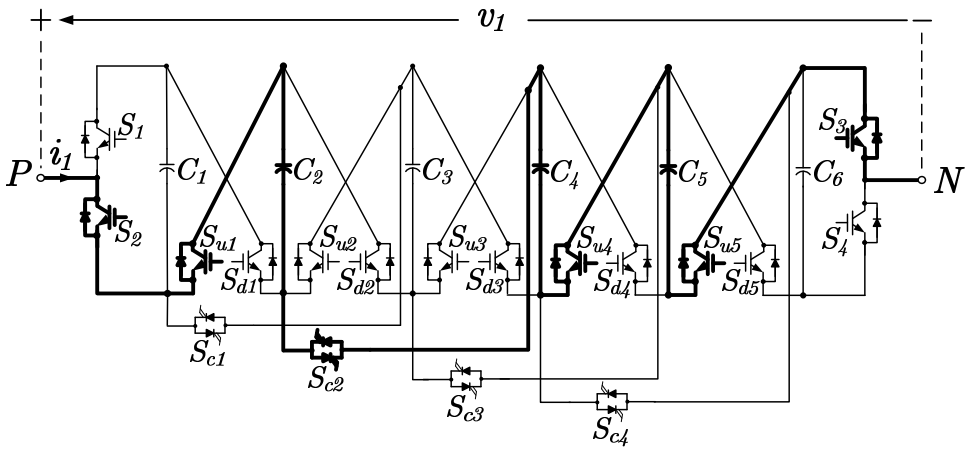

Figure 5.11: Arm current path and *on* switches in the upper arm of a 7-level LMMC, if $\mathbf{x} = [0, 1, 0, 1, 1, 0]$.

indicating that capacitors C_2, C_4, and C_5 must be inserted. Applying the equations given by (5.1) the following switching matrix S_w is formed

$$S_w = \begin{array}{c} Cap/Switch \\ C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \\ C_6 \end{array} \begin{bmatrix} k_{S1/S3} & k_{S2/S4} & k_{Sun} & k_{Sdn} & k_{Scn} \\ 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{5.3}$$

where every row corresponds to a capacitor of the LMMC, and the columns represent the switches connected to the capacitor. Analysing (5.3), it can be observed that, in the positive half-bridge of the upper arm, the switch S_2 is activated, since capacitor C_1 is bypassed. Then, still in C_1, switch S_{u1} is activated in order to connect the bottom of C_1 with the top of C_2. In C_2, the switching controller activates the high-efficiency link, inserting S_{c2} and bypassing completely capacitor C_3 (represented in the switching matrix by a row filled with zeros). In C_4, the controller cannot activate the high-efficiency link, as the next capacitor is also to be inserted, so switch S_{u4} is turned *on* instead. In C_6, switch S_3 is activated, as the capacitor to be bypassed, completing the switching configuration. Figure 5.11 shows the arm current path and the *on* switches for the aforementioned example.

The algorithm for the creation of the switching matrix can be illustrated by the fluxogram that Fig. 5.12 shows.

5.4 Comparison with the conventional MMC

The structures of the LMMC and conventional MMC differ in two major respects, as described below.

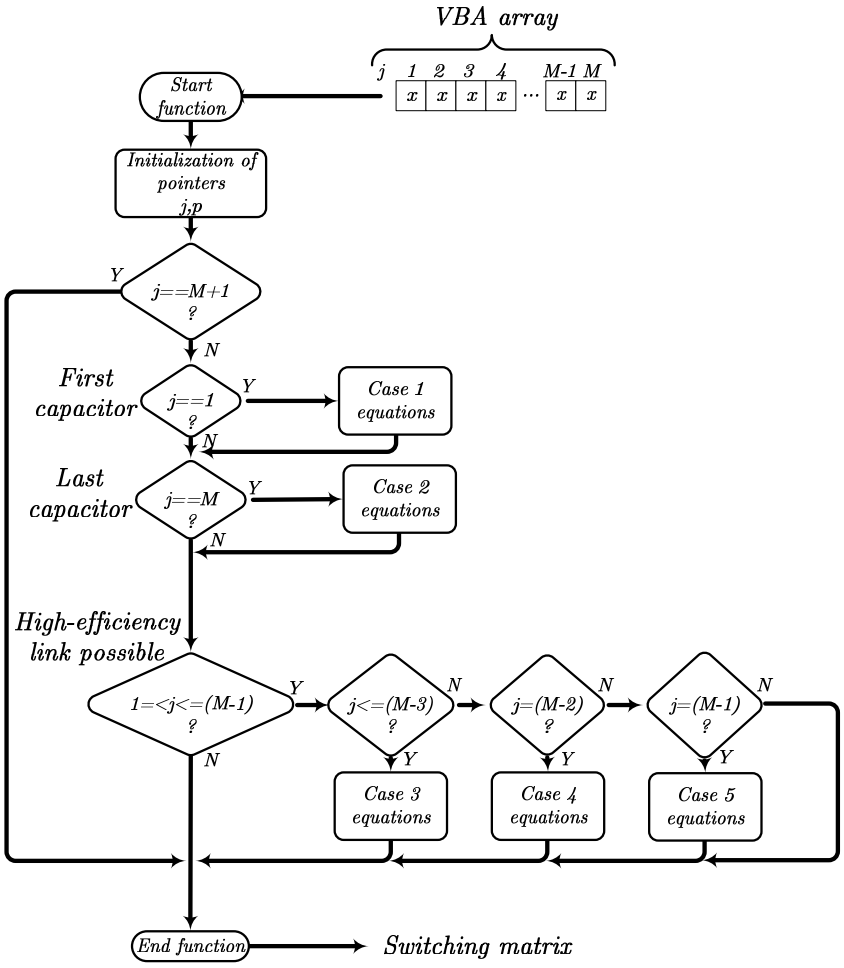

Figure 5.12: Fluxogram for the LMMC switching function matrix creation.

5.4.1 Comparison between LMMC and MMC building blocks

In HVDC applications, pulse-width modulation is avoided for its associated switching power losses. Rather, the right number of capacitors are inserted in series with the current path of the host arm, for a desired ac-side terminal voltage. This goal is achieved in the LMMC by the networks, whereas, as Fig. 5.13 illustrates, in the conventional MMC the submodules perform this task. Therefore, a network, together with the capacitor connected to its terminals *a* and *b*, constitute a building block of the LMMC, whereas the submodules are the building blocks of the conventional MMC.

In both the conventional MMC and the LMMC, the number of voltage levels in the produced ac-side terminal voltage, $M + 1$, is one more than the number of capacitors in series with the current path of the host arm, M. The number of capacitors, in turn, determines the number of networks or submodules. As mentioned in Section 5.1, in the LMMC the number of networks is one less than the number of capacitors, whereas in a conventional MMC the number of submodules equals either the number of capacitors (in the HBSM- and FBSM-based MMCs) or half of the same (in the CDSM-based MMC). Consequently, in both the LMMC and a conventional MMC, the operation boils down to inserting the right number of capacitors

in the arm current part.

Another difference between a conventional MMC and the LMMC is that, as explained in Section 5.1, in the LMMC the cascade of networks in each arm is interfaced with the rest of the converter through two half-bridge converters: the positive half-bridge and the negative half-bridge, whereas, in a conventional MMC, a submodule is directly interfaced at its ac-side terminals with the rests of the converter.

5.4.2 Comparison between LMMC and MMC interconnections

In the LMMC, the networks are interconnected through regular links and high-efficiency links. Therefore, a capacitor may be inserted in the current path of the host arm through various combinations of switches. This, in turn, means that the switches are switched less frequently, in comparison with those in a conventional MMC, thus reducing the switching stresses. In addition, as explained in Section 5.1, a network can be connected not only to the next network, but also to the network after the next, through the shortcuts offered by the high-efficiency links, thus, reducing the conduction power losses.

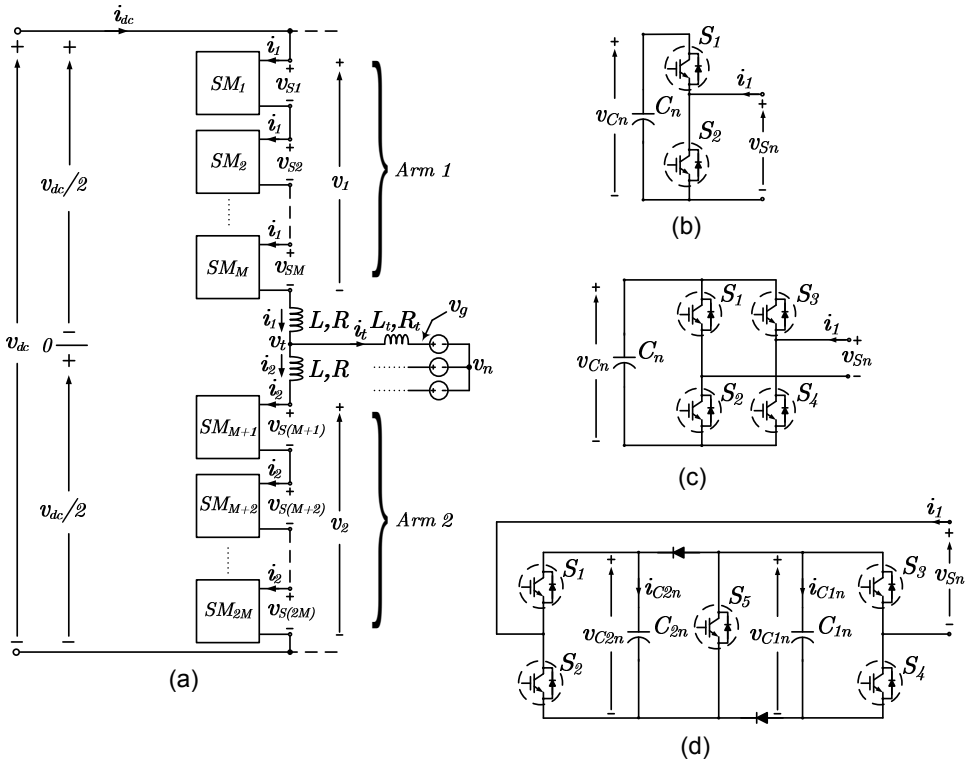

Figure 5.13: Schematic diagrams of (a) one leg of a conventional three-phase MMC, (b) an HBSM in the upper arm, (b) a FBSM in the upper arm, and (c) a CDSM in the upper arm.

5.5 Analysis of power losses

5.5.1 Number of series-connected switches in an arm

In an MMC adopting the NLC modulation strategy, switching power losses are negligible, and the overall power loss of the converter can be assumed to consist only of conduction power losses. Calculation of conduction power losses, on the other hand, requires knowledge of the number of switches in series with the arm current paths. In the HBSM-based MMC, CDSM-based MMC, and FBSM-based MMC, the number of series-connected switches per arm is fixed by the number of capacitors, M. In the LMMC, however, the number of series-connected switches depends not only on the number of inserted capacitors (or, equivalently, the ac-side terminal voltage at the instant), but also on what specific capacitors are inserted, due, in turn, to the number of *on* high-efficiency links that varies based on the (time-varying) VBA array. For example, as illustrated in Section 5.2.1, the number of series-connected switches required for an ac-side terminal voltage of $v_{dc}/2$ can be 4 (see Fig. 5.8) or 5 (see Fig. 5.9), whereas, independent from the ac-side terminal voltage level, it is 4 in an HBSM-based MMC, 6 in a CDSM-based MMC, and 8 in an FBSM-based MMC. Therefore, conduction power losses of the LMMC are computed based on the average number of series-connected switches and for a given ac-side terminal voltage swing (or, equivalently, for a given amplitude modulation index).

Figure 5.14 shows the average number of series-connected switches, $\overline{N_{ss}}$, versus the number of capacitors, M, for the LMMC, assuming the maximum ac-side terminal voltage swing, i.e., a modulation index of unity. For the HBSM-based MMC, CDSM-based MMC, and FBSM-based MMC, $\overline{N_{ss}}$ is the same as the number of series-connected switches, which is independent of the modulation index, as mentioned earlier, and equal to M, $1.5M$, and $2M$, respectively. However, to determine $\overline{N_{ss}}$ in the LMMC, the switching state generation algorithm of Section 5.3 was coded in MATLAB software environment, to count the number of series-connected switches and calculate its average for $M = 4$ through $M = 20$, in incremental steps of 2; the piece of of the curve that corresponds to $M > 20$ is then drawn based on the assumption that $\overline{N_{ss}}$ rises linearly with M, a trend observed over the range $4 \leq M \leq 20$. Further, an inspection of the curve indicates that $\overline{N_{ss}}$ equals $0.75M + 1.4$ in the LMMC; Table 5.1 summarizes this conclusion. It is observed the LMMC features a smaller average number of series-connected switches than the other topologies.

Table 5.1: Average number of series-connected switches per arm

Converter	$\overline{N_{ss}}$
LMMC	$0.75M + 1.4$
HBSM-based MMC	M
CDSM-based MMC	$1.5M$
FBSM-based MMC	$2M$

Figure 5.15 shows the variation of $\overline{N_{ss}}$ versus the modulation index, $\widehat{m}$, for three different values of M in the LMMC.

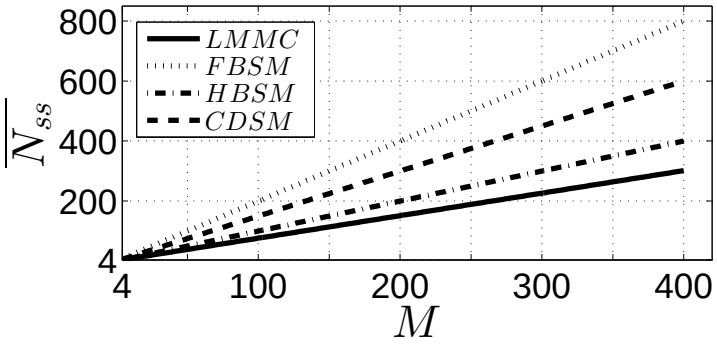

Figure 5.14: The average number of series-connected switches per arm versus the number of capacitors, for different MMC technologies.

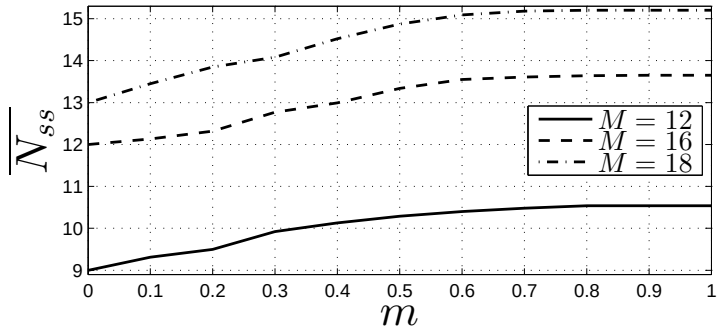

Figure 5.15: Variation of $\overline{N_{ss}}$ with the modulation index, in the LMMC.

In Fig. 5.15, it can be observed that the $\overline{N}_{ss}$, for a specific M, is a quadratic function of $\hat{m}$, given by

$$\overline{N}_{ss}(\hat{m}) = a\hat{m}^2 + b\hat{m} + c \tag{5.4}$$

where a, b and c are the quadratic equation coefficients. The c coefficient is the $\overline{N}_{ss}$ value for $\hat{m} = 0$, or $\overline{N}_{ss0}$ described by the equation

$$c = \overline{N}_{ss0}(M) = \left(\frac{M}{2} + 1\right) + round\left(\frac{M+2}{6}\right) \tag{5.5}$$

The total number of switches, N_{st}, used for the aforementioned topologies is calculated by the equations shown in Table 5.2, including diodes and IGCTs, in the case of the CDSM and the LMMC, respectively.

Fig. 5.14 shows the change in N_{st} in relation to M. It can be observed in Fig. 5.16 that the LMMC has the same number of switches as that of the FBSM topology.

5.5.2 Power losses

Using the corresponding average number of series-connected switches, as reported in Table 5.1, and the rms values of the arm currents, Table 5.3 reports the power loss expressions for the LMMC and the three other MMC topologies for a large M.

Table 5.2: Total number of switches for different topologies

Topology	$N_{st}(M)$
LMMC	$4M-2$
HBSM	$2M$
FBSM	$4M$
CDSM	$\frac{7}{2}M$

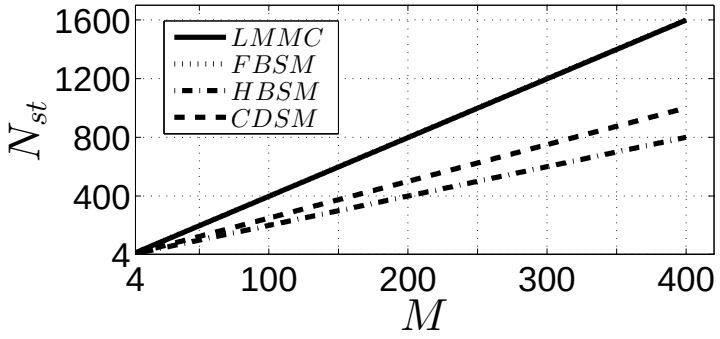

Figure 5.16: Comparison of the total number of switches for the HBSM, the FBSM, the CDSM, and the LMMC.

Table 5.3: Power loss expressions for large M

Converter	Power Loss	Power loss relative to LMMC
LMMC	$\approx (I_1^2 + I_2^2)(0.75M)R_{on}$	1
HBSM-based	$(I_1^2 + I_2^2)MR_{on}$	1.33
CDSM-based	$(I_1^2 + I_2^2)(1.5M)R_{on}$	2
FBSM-based	$(I_1^2 + I_2^2)(2M)R_{on}$	2.66

5.6 Analysis of Voltage Stress

The voltage stress on the switches of the LMMC can be characterized through the circuit of one sample *network*. The *network* considered here, Fig. 5.17, is a subset of the upper arm circuit of a five-level LMMC, Fig. 5.6, in which the switches are considered ideal to enable one to concentrate on the essentials.

5.6.1 Switch S_{u1}

The voltage across switch S_{u1} must be characterized for three different cases:

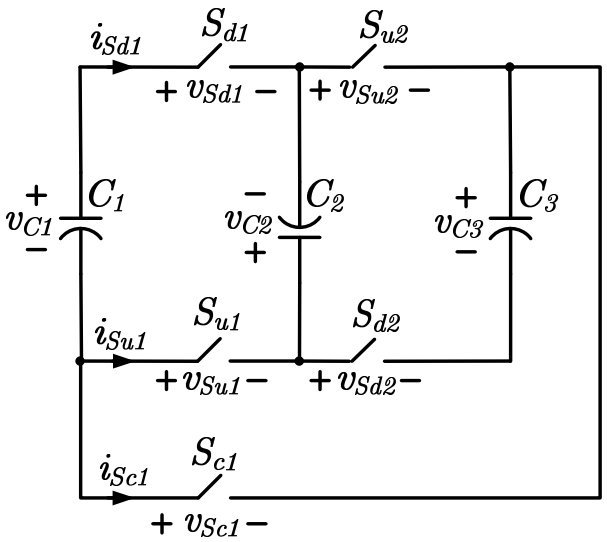

Figure 5.17: Rearranged partial circuit for the voltage stress analysis in the switches connecting three capacitors in the LMMC arm.

1. If S_{u2} is *on*, while all other switches are *off*, the voltage across S_{u1} can be found from the mesh formed by S_{u1}, C_2, and S_{c1}. As Fig. 5.17 illustrates, the voltage across capacitor C_2 is divided between S_{c1} and S_{u1}, such that $v_{Su1} = v_{C2}/2$;

2. If S_{c1} is *on*, while all other switches are *off*, the voltage of S_{u1} is governed by the the mesh formed by S_{u1}, S_{d2}, and C_3, and $v_{Su1} = v_{C3}/2$;

3. If S_{d1} is *on*, while the other switches are all *off*, the voltage across S_{u1} is governed by the mesh constituted by C_1, S_{u1}, and C_2. Thus, the sum of the voltages across C_1 and C_2 appears across S_{u1}, that is, $v_{Su1} = v_{C1} + v_{C2}$. This issue exists also in the *five-level cross-connected submodule* [76].

5.6.2 Switch S_{c1}

The voltage across switch S_{c1} is inspected for four different cases:

1. If S_{u1} and S_{u2} are *on*, while all other switches are *off*, the voltage across S_{c1} is governed by the mesh represented by C_2 and S_{c1}. Therefore, $v_{Sc1} = -v_{C2}$;

2. If S_{u1} and S_{d2} are *on*, while all other switches are *off*, the voltage across S_{c1} is governed by the mesh formed by C_3 and S_{c1}. Hence, $v_{Sc1} = v_{C3}$;

3. If S_{d1} and S_{u2} are *on*, while all other switches are *off*, the voltage across S_{c1} is governed by the mesh formed by C_1 and S_{c1}. Therefore, $v_{Sc1} = v_{C1}$.

4. If S_{u2} is *on*, while all other switches are *off*, the voltage across S_{c1} is governed by the mesh represented by S_{u1}, C_2, and S_{c1}, and $v_{Sc1} = v_{C2}/2$.

Table 5.4: Voltage across the switches in the LMMC arm

Switch	Most frequent voltage	Less frequent voltage
S_{un}	$\approx \overline{v}_c/2$	$\approx 2\overline{v}_c$
S_{dn}	$\approx 2\overline{v}_c$	-
S_{cn}	$\approx \pm\overline{v}_c$	$\approx \overline{v}_c/2$

5.6.3 Switch S_{d1}

Switch S_{d1} is rarely turned *on*. When *off*, it withstands a voltage of about $2\overline{v}_c$, based on the same analysis conducted under item 3 in Section 5.6.1, and assuming that the VBA regulates all capacitor voltages at about $\overline{v}_c$.

Switch S_{c1} constitutes the high-efficiency link and, therefore, closes the arm current path for most of the time. Thus, even though switches S_{u1} and S_{d1} experience two capacitor voltages, they are often bypassed by S_{c1} (when both S_{u1} and S_{d1} are *off*). This reduces the voltage across S_{u1} by a factor of two and, also, permits S_{d1} to be *on* less frequently than otherwise. It should be pointed out that the switching scheme of the LMMC (see Section 5.3) does not permit any other combination of switching states for S_{u1}, S_{d1}, S_{c1}, S_{u2}, and S_{d2}. Hence, no switch in a network can assume a voltage different in value from $0.5\overline{v}_c$, $\overline{v}_c$, and $2\overline{v}_c$. Table 5.4 summarizes the conclusions.

The conclusions made through the aforementioned analysis hold also for all the other networks of the LMMC.

5.7 Simulation results for the LMMC

Similar to other MMC technologies that adopt the NLC switching strategy, the LMMC produces low-distortion ac-side terminal current waveforms only if its ac-side terminal voltage has an adequately large number of levels (e.g., corresponding to $M > 100$). Simulation models based on detailed models of the semiconductor switches are, however, difficult to develop and run for such an LMMC, due to excessive simulation runtime, limited number of nodes accommodated by the software packages, etc. Therefore, in this thesis, *detailed models* were developed only for LMMCs with $M = 4$ and $M = 8$, for preliminary assessment of the principles of operation, salient features, and robustness to dc-side faults. All simulations were conducted in the PSCAD/EMTDC software environment [80].

5.7.1 Case I - Single-phase LMMC inverter for $M = 4$

For this case, a detailed model of a single-phase 5-level LMMC (i.e., with $M = 4$) was simulated. The LMMC, shown in Fig. 5.18 with its associated ac and dc systems, featured a dc-side

voltage, v_{dc}, of 8 kV, which was impressed by two identical dc sources. The ac grid voltage and the modulating signal were represented by $v_g(t) = 2\sin(2\pi f_g t)$ kV and $m(t) = \sin(2\pi f_g t)$, respectively, where $f_g = 60$ Hz. The other parameters of the system were $C = 3.1$ mF, $R = 15$ $m\Omega$, $L = 2$ mH, $R_t = 2$ Ω, and $L_t = 0$. The system also included a fault detection logics that compared the peak values of the arm currents, i_1 and i_2, with a threshold of 1.5 kA. Thus, the fault detection mechanism blocked the gating pulses of the switches, for 100-ms, if either of the two peak values exceeded the threshold.

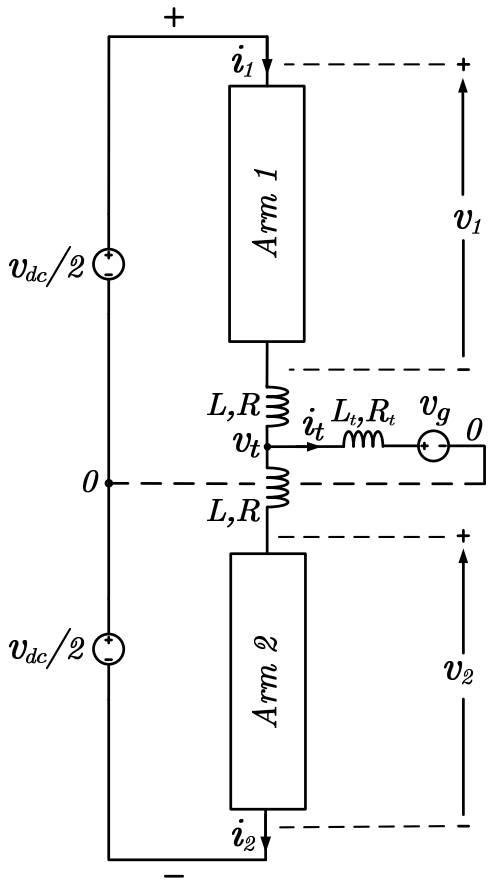

Figure 5.18: Schematic diagram of the single-phase LMMC system for Case I.

Initially, the gating pulses of the switches were disabled and the capacitors pre-charged. Then, at $t = 0.03$ s the gating pulses were unblocked and the LMMC functioned normally until $t = 0.1$ s. From $t = 0.1$ s to $t = 0.15$ s, nodes "+" and "−" were connected through a short link, to simulate a 50-ms long dc-side fault. Almost immediately after the fault inception, the fault detection mechanism of the LMMC detected the fault and blocked the gating pulses, until $t = 0.2$ s. Thereafter, the gating pulses were unblocked to allow the LMMC to revert to its normal operation. Figure 5.19 shows the responses of the LMMC and a detailed model of an equivalent 5-level FBSM-based MMC.

As Fig. 5.19 shows, from $t = 0.1$ s to $t = 0.15$ s, that is, during the fault, the arm current is zero and, consequently, the arm voltage is equal to the negative of the grid voltage, in both the LMMC and FBSM-based MMC. From $t = 0.15$ s onwards, that is, from the fault clearance moment onwards, the arm voltages assume a positive offset equal to half of the dc-side voltage,

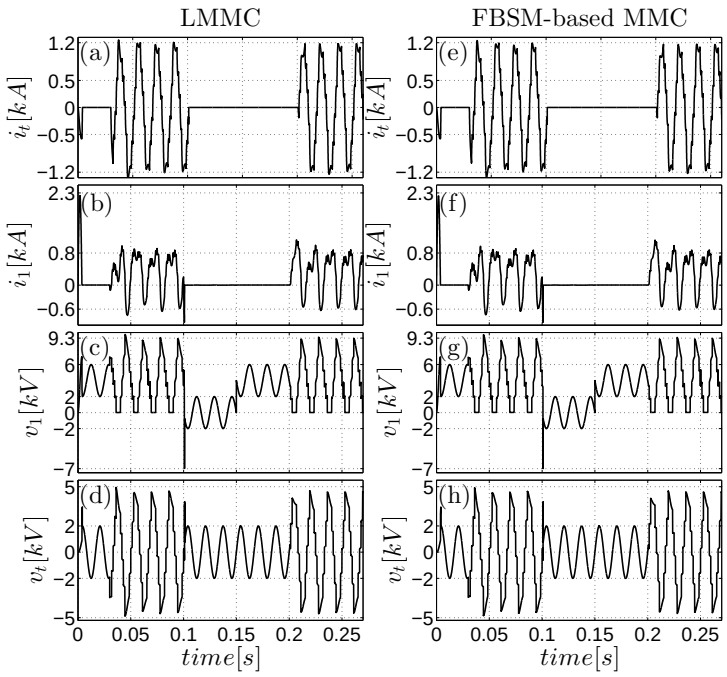

Figure 5.19: Waveforms of selected variables in an open-loop controlled single-phase 5-level LMMC (left column) and an equivalent FBSM-based MMC (right column), to various disturbances; Case I.

i.e., 4 *kV*, until the release of the gating pulses at $t = 0.2$ *s*, while the arm currents remains zero. From $t = 0.2$ *s* onwards, i.e., from the instant at which the gating signals are released, the currents and voltages revert to their pre-disturbance forms and magnitudes. Figure 5.19 demonstrates the similarity of the responses of the LMMC and FBSM-based MMC. Figure 5.19 also shows that the arm currents exhibits harmonic distortion due to circulating current components. This, in turn, is due to the fact that the simulation was run in open-loop, i.e., no circulating current suppression control was employed.

Figure 5.20 shows the voltage and current waveforms for the switches of the second *network* of the upper arm of the LMMC; the variables are labeled in accordance with the circuit of Fig. 5.17. It can be verified through the waveforms that the voltage magnitudes agree with the values predicted by the analysis of Section 5.6.

Figure 5.21 depicts the gating pulses for the switches of the second *network* of the upper arm of the LMMC, as well as the gating pulses for switch S_3 of the first FBSM, Fig. 5.18(c), in the upper arm of the equivalent five-level FBSM-based MMC. The figure indicates that, as compared to the FBSM-based MMC, the switches of the LMMC are switched less frequently. This is due to the multiple possible switch state combinations in the LMMC, offered by the high-efficiency links and the regular links.

5.7.2 Case II - Single-phase LMMC inverter for $M = 9$

In this case, a detailed model of a open-loop controlled single-phase 9-level LMMC was simulated, in the same system as that of Fig. 5.18, assuming the same sequence of events as those in Case I, and with the same parameters as those in Case I, with the exception that $C = 6$ *mF*. The

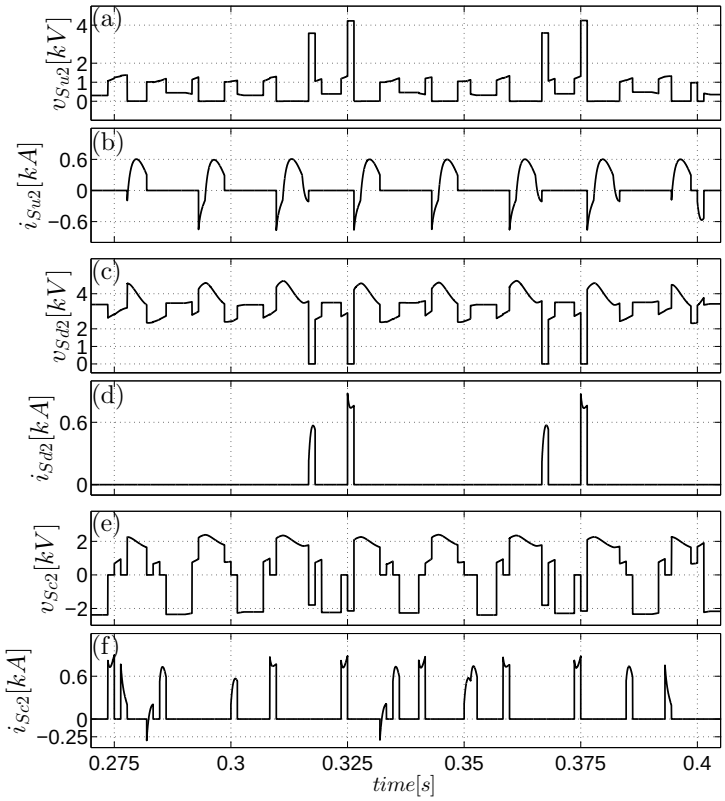

Figure 5.20: Voltage and current waveforms for the switches of the second network of the upper arm; Case I.

LMMC was also equipped with the same fault detection mechanism as that in the system of Case I. Figure 5.22 depicts that responses of the LMMC and a detailed model of an equivalent HBSM-based MMC.

As Fig. 5.22 shows, from $t = 0.1$ *s* to $t = 0.15$ *s*, i.e., during the fault, in the LMMC the arm current is zero and the arm voltage is equal to the negative of the grid voltage. However, in the HBSM-based MMC, a large arm current develops, which cannot be interrupted and is only impeded by the inductance of the arm inductance. The figure also shows that the arm current is superimposed with a decaying negative dc offset. The dc offset depends on the fault inception instant, relative to the zero crossing instant of the grid voltage. In this case, the relationship happens to be such that the maximum possible negative offset develops subsequent to the fault inception. Therefore, the arm current remains negative for the entire duration of the fault, as Fig. 5.22 shows. Consequently, the arm voltage of the HBSM-based MMC is almost zero in this interval, due to the conduction of the anti-parallel diode of the lower switches of the submodules. From the fault clearance moment, $t = 0.15$ *s*, the arm voltages of both the LMMC and HBSM-based MMC move up by half of the dc-side voltage, and the arm current of the HBSM-based MMC also becomes zero. After the gating pulses are released, that is, from $t = 0.2$ *s* onwards, the two converters resume their normal operations.

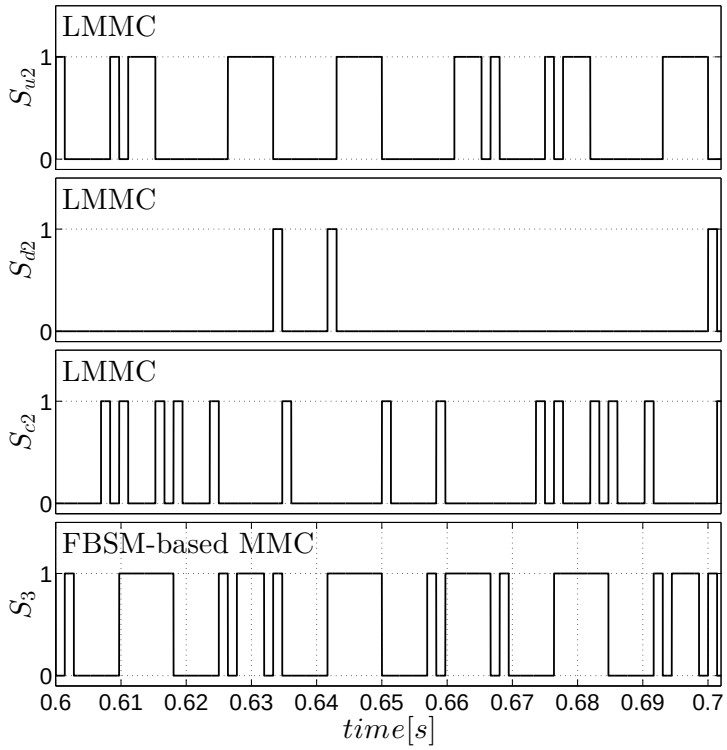

Figure 5.21: Gating pulses for the switches of the second network in the upper arm of the LMMC, and for S_3 of the first submodule in the upper arm of the FBSM-based MMC; Case I.

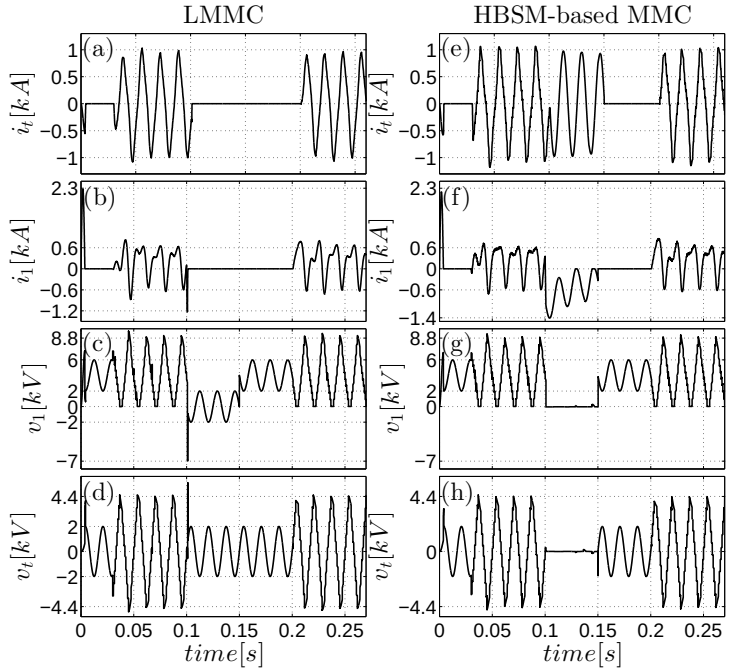

Figure 5.22: Waveforms of selected variables in an open-loop controlled single-phase 9-level LMMC (left column) and an equivalent HBSM-based MMC (right column), to various disturbances; Case II.

5.7.3 Case III - Three-phase LMMC inverter for $M = 8$

In this case, a detailed model of a three-phase 9-level LMMC, operated as an inverter in a system such as shown in Fig. 5.1, was simulated under closed-loop control. The parameters were $C = 6\ mF$, $R = 0.1\ \Omega$, $L = 4\ mH$, $R_t = 0.8\ \Omega$, and $L_t = 10\ mH$. The grid voltage had a peak value of 2 *kV* and its frequency was 50-Hz. The LMMC was current-controlled in a *dq* frame synchronized to the grid voltage, [10]. The converter was also equipped with a fault detection mechanism that compared the peak value of the arm currents with a threshold of 1.0 *kA* and disabled the current controller and the gating pulses for 100 *ms*, if any of the six arm current peak values exceeded the threshold. The fault detection mechanism also set the setpoint for the *d*-axis component of the ac-side terminal current to zero.

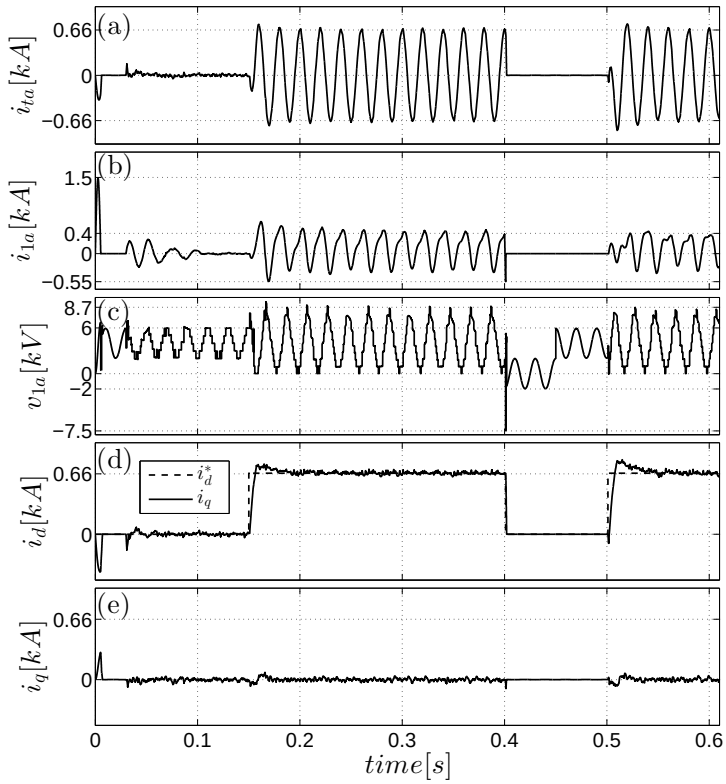

Figure 5.23: Waveforms of selected variables in a closed-loop controlled three-phase 9-level LMMC, to various disturbances; Case III.

From the start to $t = 0.03\ s$, the gating pulses and the current controller were disabled. At $t = 0.03\ s$, the gating pulses were released and the current controller was activated, with the real- and reactive-power setpoints both set to zero. At $t = 0.15\ s$, the real-power setpoint was stepped to 2 *MW*, thus raising the setpoint for the *d*-axis component of the ac-side terminal current to $i_d^* = 0.66\ kA$. At $t = 0.4\ s$, a short link was placed across the dc-side terminals of the LMMC, and was removed after 50 *ms*. The fault detection mechanism detected the fault, almost immediately, blocked the gating pulses, disabled the current controller, and set i_d^* to zero. At $t = 0.5\ s$, the gating pulses were unblocked, the current controller was enabled, and i_d^* was reset to its pre-disturbance value of 0.66 *kA*.

Figure 5.23 shows the waveforms of the ac-side terminal current, upper arm current, and

upper arm voltage (all for phase-a). The figure also shows the waveforms of the d- and q-axis components of the ac-side terminal current. It is observed that, as expected, the arm current and the ac-side terminal current drop to zero once the fault is detected. It is also observed that the ac-side terminal current is noticeably distorted. The distortion, in turn, translates into considerable ripples in the d- and q-axis current components. The distortion is due to the small M for this simulation and, consequently, the low number of levels in the ac-side terminal voltage of the LMMC. The modulation strategy adopted for this paper, i.e., the NLC modulation strategy, produces quality ac-side voltage and current waveforms if M is large.

5.7.4 Validation of the model for power losses

Cases I and II were also used to verify the predictions of Section 5.5 of the power losses of the LMMC, with the results reported in Table 5.5; the power losses were computed as $P_{loss} = v_{dc}i_1 - v_t i_t$, using the simulated variables. A closer look at the results of Table 5.5 reveals the fact that the predictions of Table 5.3 do not precisely hold. This is because the power loss expressions in Table 5.3 are derived, from those in Table 5.1, based on the assumption of adequately large values of M. Further, the average number of series-connected switches, $\overline{N_{ss}}$, in the LMMC, exhibits deviations from the values predicted by the corresponding expression in Table 5.1 if M is small. Thus, in Case I, where $M = 4$, the value of $\overline{N_{ss}}$ for the FBSM-based MMC is 1.8 times that for the LMMC, whereas, as shown in Table 5.5, the power loss of the FBSM-based MMC is 1.5 times that of the LMMC. However, for Case II, i.e., with $M = 8$, the ratio of the $\overline{N_{ss}}$ values is 1.08, which agrees with what Table 5.5 reports from the simulations.

Table 5.5: Simulated power losses for Cases I and II.

Converter	Case I	Case II	Relative to LMMC
LMMC	$0.0259MW$	$0.026MW$	–
5-level FBSM-based MMC	$0.038MW$	–	1.5
9-level HBSM-based MMC	–	$0.028MW$	1.08

5.8 Summary and Conclusions

In this chapter, a new topology for modular multilevel converter (MMC) was proposed. The proposed MMC, referred in this thesis to as the LMMC, offers the same fault handling capability of an equivalent full-bridge submodule (FBSM) -based MMC, while it features lower power losses than the half-bridge submodule (HBSM) -based MMC, the clamp-double submodule (CDSM) -based MMC, and the FBSM-based MMC. The effectiveness of the proposed MMC was demonstrated through time-domain simulation results, assuming various normal and faulted operating scenarios.

Chapter 6

Lattice Submodule

In Chapter 5, a new topology for the MMC was proposed, the LMMC. The proposed LMMC was shown to feature the same dc-side fault handling capability as that of the FBSM, with lower power losses as those of the HBSM. However, the LMMC positive and regular links must be selected such that they can withstand double the submodule capacitor voltage. This shortcoming means that the cost of the LMMC is higher than that of an FBSM-based MMC, even though the number of switches per arm is the same. Nevertheless, the LMMC produce much lower power losses than all other topologies known to date, at least that is the conclusion from the analysis in Chapter 5 and the simulation results, which makes the operation less costly. A more detailed analysis is needed, perhaps strengthened by experimental results, to verify the balance point where the use of LMMC topology becomes more economically feasible than the FBSM.

Therefore, a different topology, the *Lattice Submodule* (LSM), is proposed in this chapter. The LSM is a modification of the LMMC in the sense that the switches of the negative regular links are substituted by diodes, and a *parallel link* is added to enable all switching possibilities. These modifications also guarantee that no switch experiences higher than one capacitor voltage; the diodes of the negative regular link experience two capacitor voltages, but they are off in normal operation, hence no switching power losses. However, the topology can only be extended to four capacitors, and not the entire converter arm. Thus, an LSM-based MMC is not as efficient as the LMMC; its power losses are slightly larger than those of an HBSM-based MMC. However, the stress on its switches is lower than that of the switches in the LMMC as explained in this chapter.

6.1 Proposed submodule topology: The LSM

Figure 6.1 shows a schematic diagram of the proposed SM topology, i.e., the LSM, based on the assumption that $M + 1$ levels (M is assumed to be even) are to exist in the ac-side terminal voltage. Figure 6.1 also shows that the LSM hosts four capacitors, thus, the number of SMs in an arm is given by $N = M/4$. Therefore, the number of SMs in an arm is given by $N = M/4$. The capacitors in an arm are identified as C_{1n}, C_{2n}, C_{3n}, and C_{4n}, where n is the SM number($n = 1, 2, 3, ..., N$ for the upper arm, and $n = N + 1, N + 2, ..., 2N$ for the lower arm).

Figure 6.1 further shows that the positive terminal, P_S, and negative terminal, N_S, of the

LSM, similarly to the LMMC, are connected to the arm by a positive half-bridge and a negative half-bridge. Internally, the capacitors are connected between themselves by positive regular links, formed by B-C, D-E, and F-G, and by negative regular links, formed by A-D, C-F, and E-H. The capacitors can also connect to each other through high-efficiency links, formed by B-E and D-G, and through a *parallel link*, E-G. The M capacitors are assumed to all have the same (nominal) capacitance, as it is the case for conventional MMCs and the LMMC.

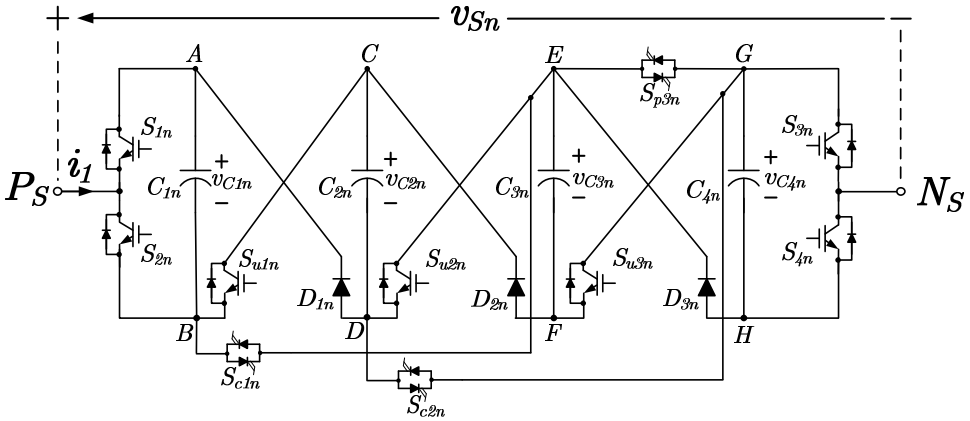

Figure 6.1: Schematic diagram for the LSM.

Similarly to the LMMC, the positive regular links, high-efficiency links, and parallel links embed fully controllable electronic switches, S_{u1n}, S_{c1n}, S_{u2n}, S_{c2n}, S_{u3n}, and S_{p3n}. By contrast, the negative regular links utilize diodes, D_{1n}, D_{2n}, and D_{3n}. Switches of the positive regular link, S_{u1n}, S_{u2n}, and S_{u3n}, must be of the reverse-conducting type, e.g., IGBTs, whereas switches of the high-efficiency links, that is, S_{c1n} and S_{c2n}, and the switch of the parallel link, that is, S_{p3n}, must be bidirectional reverse-blocking switches, e.g., such as the IGCTs featured in [83]-[92].

6.2 Principles of Operation of the LSM

6.2.1 Normal operation

In the LSM, the capacitors can be inserted through high-efficiency links, positive regular links or a parallel link.

Figure 6.2 shows the current path (thick line) in the first LSM of the upper arm (i.e., $n = 1$), if, for example, capacitors C_{31} and C_{41} are to be inserted in the MMC arm. It is noted that, in this case the number of switches in series with the arm current is 4, which is equal to the number of switches inserted in the HBSM. This is possible due to the use of a high-efficiency link, i.e, S_{c11}. Similarly, if capacitors C_{11} and C_{41} are to be inserted in the MMC arm, as Fig. 6.3 illustrates, the parallel link, i.e., S_{p31}, is activated, in addition to S_{c11}, to keep 4 of switches in series. By contrast, if capacitors C_{21} and C_{31}, Fig. 6.4, are to be inserted in the MMC arm, no high-efficiency links can be used, and the number of series-connected switches rises to 5.

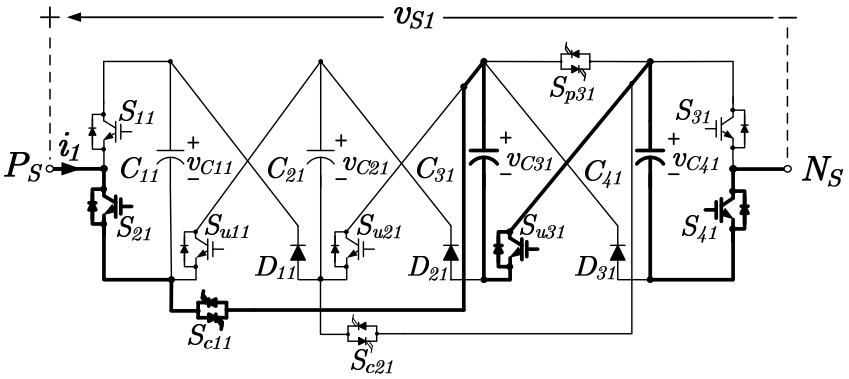

Figure 6.2: Current path in the LSM with C_{31} and C_{41} inserted for $n = 1$.

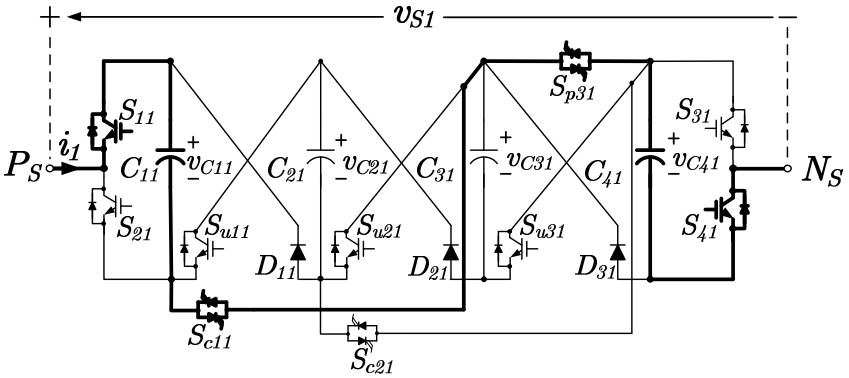

Figure 6.3: Current path in the LSM with C_{11} and C_{41} inserted for $n = 1$.

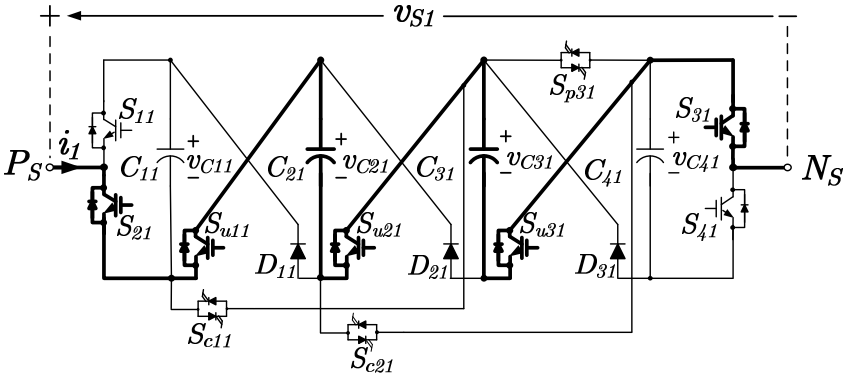

Figure 6.4: Current path in the LSM with C_{21} and C_{31} inserted, for $n = 1$.

6.2.2 Operation under a dc-side fault

The operation and the equivalent circuit of the LSM under a dc-side fault is exactly the same as that of the LMMC. Therefore, the behavior described in Section 5.2.2 is still valid here and will not be repeated.

Table 6.1: Switch States in Terms of VBA Array Elements for an LSM

	VBA Array Elements				Switch States										
Comb	x_{1n}	x_{2n}	x_{3n}	x_{4n}	k_{S1n}	k_{S2n}	k_{Su1n}	k_{Sc1n}	k_{Su2n}	k_{Sc2n}	k_{Su3n}	k_{Sp3n}	k_{S3n}	k_{S4n}	N_{ss}
0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	4
1	0	0	0	1	0	1	0	1	0	0	0	1	0	1	4
2	0	0	1	0	0	1	0	1	0	0	1	0	1	0	4
3	0	0	1	1	0	1	0	1	0	0	1	0	0	1	4
4	0	1	0	0	0	1	1	0	0	1	0	0	1	0	4
5	0	1	0	1	0	1	1	0	0	1	0	0	0	1	4
6	0	1	1	0	0	1	1	0	1	0	1	0	1	0	5
7	0	1	1	1	0	1	1	0	1	0	1	0	0	1	5
8	1	0	0	0	1	0	0	1	0	0	0	1	1	0	4
9	1	0	0	1	1	0	0	1	0	0	0	1	0	1	4
10	1	0	1	0	1	0	0	1	0	0	1	0	1	0	4
11	1	0	1	1	1	0	0	1	0	0	1	0	0	1	4
12	1	1	0	0	1	0	1	0	0	1	0	0	1	0	4
13	1	1	0	1	1	0	1	0	0	1	0	0	0	1	4
14	1	1	1	0	1	0	1	0	1	0	1	0	1	0	5
15	1	1	1	1	1	0	1	0	1	0	1	0	0	1	5

6.3 Switching Scheme of the LSM

The switching scheme of the LSM adopts the same NLC modulation strategy as that of the LMMC. Further, the switching scheme of the LSM is also based on a VBA array. However, in the LMMC there is no submodules, and the capacitors are indexed from 1 to M in the upper arm, and $M + 1$ to $2M$ in the lower arm, which is not the case in the LSM. Since the LSM is a submodule topology, its capacitors are indexed from 1 to 4 inside each submodule. Thus, the VBA array is modified to

$$\begin{aligned}\mathbf{x} = &\\ &[x_{11}, x_{21}, x_{31}, x_{41}, ..., x_{1n}, x_{2n}, x_{3n}, x_{4n},\\ &..., x_{1N}, x_{2N}, x_{3N}, x_{4N}]\end{aligned} \tag{6.1}$$

In the VBA array, an element, x_{2n}, represents the state of the second capacitor of the nth SM in the host arm. Thus, $x_{2n} = 0$ corresponds to a bypassed C_{2n}, whereas $x_{2n} = 1$ indicates an inserted C_{2n}. The VBA array is then used to determine what switches must be turned *on* in each SM in the corresponding arm, raging from capacitor C_{11} to capacitor C_{4N}, in the upper arm, and capacitor $C_{1(N+1)}$ to capacitor C_{42N}, in the lower arm.

Table 6.1 lists the switch conduction states corresponding to each of the 16 values of the VBA array for one LSM. Thus, the conduction state of a switch is represented by a binary variable, k, which is 0 if the switch is *off* and is 1 if the switch is *on*. For example, $k_{S1n} = 1$ indicates that switch S_1 of the *nth* SM is *on*, etc. Table 6.1 also lists the number of switches in series with the arm current path, N_{ss}. It is noted that N_{ss} is equal to 4 for 12 of the VBA array values, and it is equal to 5 for the remainder, resulting in an average number of series-connected switches, $\overline{N}_{ss}$, of 4.25. This information is used in Section 6.4, for estimating the conduction power loss of the LSM.

The switching scheme can be implemented based on Table 6.1 and through a look-up table. However, such an implementation requires the processor to access its memory every time a new step must be produced for the ac-side terminal voltage. A more efficient way of implementing

Table 6.2: Boolean Logic for the Switch States in Terms of VBA Array Elements

Switch state	k_{S1n}	k_{S2n}	k_{Sc1n}	k_{Su1n}	k_{Sc2n}	k_{Su2n}	k_{Sp3n}	k_{Su3n}	k_{S3n}	k_{S4n}
Equation	x_{1n}	$!x_{1n}$	$!x_{2n}$	x_{2n}	$x_{2n}!x_{3n}$	$x_{2n}x_{3n}$	$!x_{2n}!x_{3n}$	x_{3n}	$!x_{4n}$	x_{4n}

the switching scheme is to use Boolean algebra applied directly to Table 6.1, as shown in Table 6.2. In Table 6.2, symbol **!** represents a *negation* (NOT) operation, and the product of two VBA array elements signifies a *conjunction* (AND) operation. For example, $x_{2n}!x_{3n}$ means a conjunction between x_{2n} and the result of the negation of x_{3n}.

6.4 Power loss analysis

Since MMCs with a large M, including the LSM-based MMC, feature low average switching frequencies, the power loss is predominantly of the conduction nature. Thus, regardless of the SM topology, the aggregate conduction power loss of one leg of an MMC, for a normal operating condition, is given by

$$P_{loss} = \overline{N}_{ss} R_{on} (I_1^2 + I_2^2) \tag{6.2}$$

where R_{on} is the on-state resistance of one switch in the SM which, for ease of analysis, is assumed to be the same for all switches. It is assumed that the arm currents rms values I_1 and I_2 include all harmonic components. This assumption is plausible in view of the fact that an LSM-based MMC operates by inserting capacitors in its arm, as described in Section 5.2.1, in much the same way that the other known MMCs operate. Therefore, i_1 and i_2 in an LSM-based MMC are very similar to those in MMCs based on HBSM, FBSM, CDSM, or LMMC for a given set of parameters and operating condition.

Moreover, if one decides to calculate the power loss ratio between an LSM and an HBSM, for example, applying (6.2), the power loss ratio, H, can be simplified to

$$H = \frac{\overline{N}_{ss_{LSM}}}{\overline{N}_{ss_{HBSM}}} \tag{6.3}$$

Thus, applying the known $\overline{N}_{ss}$ of 4.25 (see Section 6.3), yields

$$H = \frac{4.25N}{M} \tag{6.4}$$

The same ratio calculated by (6.4) between a LSM and a HBSM can be derived for other SM topologies. For simplicity, in this thesis, H is always calculated in relation to the HBSM.

Substituting into (6.4) the relation between M and N in the LSM, i.e., $N = M/4$, results in a constant ratio of 1.063. Thus, independently of M or N, the power loss in an LSM is approximately 1.063 times the power loss in an HBSM. Therefore, the LSM and the HBSM feature, approximately, the same power loss.

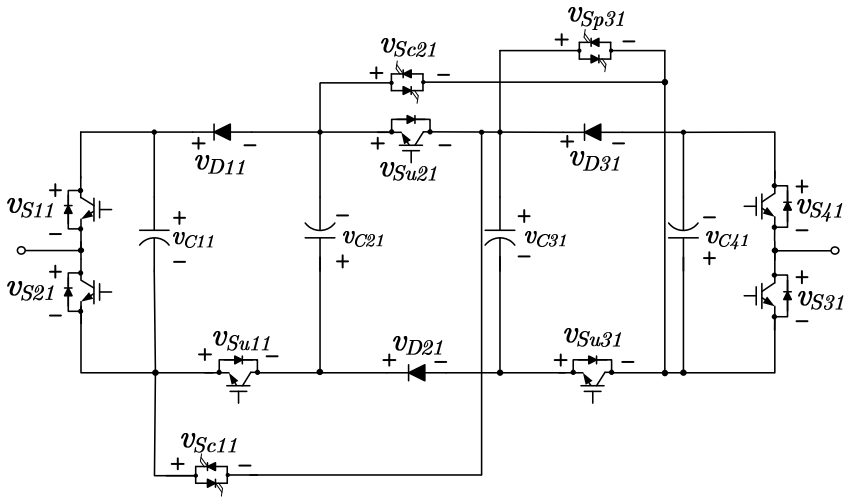

Figure 6.5: Rearranged LSM circuit, for $n = 1$.

6.5 Voltage stress analysis

One of the advantages of the LSM is the lower voltage stress of its switches. This section provides expressions for off-state switch voltage drops, for a given set of switch states.

Figure 6.5 shows a re-arranged circuit for, for example, the first LSM ($n = 1$) in an LSM-based MMC. From an analysis of the circuit of Fig. 6.5, the following equations emerge:

$$-v_{D11} + v_{Su11} = -v_{C11} - v_{C21} \tag{6.5}$$

$$-v_{D21} + v_{Su21} = -v_{C21} - v_{C31} \tag{6.6}$$

$$[!k_{Su31}!k_{Sp31}]v_{Su21} + v_{Sp31} = [k_{Su31}]v_{C31} \tag{6.7}$$

$$\begin{aligned}&[!(k_{Su21}k_{Sp31})!k_{Sp31}!k_{Su21}k_{Su31}]v_{D11}\\ -&[!(k_{Su21}k_{Sp31})k_{Sp31}!k_{Su21}]v_{Su21} + v_{Sc21} =\\ &[!(k_{Su21}k_{Sp31})!k_{Sp31}!k_{Su21}k_{Su31}]v_{C11}\\ +&[!(k_{Su21}k_{Sp31})!k_{Sp31}k_{Su31}]v_{C31}\end{aligned} \tag{6.8}$$

$$-[!k_{Sc11}]v_{D21} + v_{sc11} = -[!k_{Sc11}]v_{C31} \tag{6.9}$$

$$\begin{aligned}v_{D31} - [!k_{Sp31}!k_{Su31}]v_{Sp31} =&\\ [k_{Su31}!k_{Sp31}]v_{C31} + v_{C41}&\end{aligned} \tag{6.10}$$

$$v_{D11} + [k_{Sc11}]v_{Su21} = v_{C11} + [!k_{Sc11}]v_{C31} \tag{6.11}$$

$$-v_{D31} + v_{Su31} = -v_{C31} - v_{C41} \tag{6.12}$$

$$\begin{aligned}[k_{Su21} + k_{Sc21}]v_{D21} - [!k_{Su21}k_{Sc21}]v_{D31} = \\ [k_{Su21} + k_{Sc21}]v_{C21} + [k_{Su21} - !k_{Su21}k_{Sc21}]v_{C31}\end{aligned} \tag{6.13}$$

$$\begin{aligned}[!k_{Sc21}!k_{Sc11}]v_{D11} + [k_{Sc21}]v_{D31} + v_{Su21} = \\ \frac{1}{5}[!k_{Sc21}!k_{Sc11} + k_{Sc11}!k_{Sc21}]v_{C11} \\ + \frac{1}{5}[!k_{Sc21}!k_{Sc11} - 2!k_{Sc21}k_{Sc11}]v_{C21} \\ -\frac{1}{5}[2!k_{Sp31}!k_{Sc21}k_{Sc11} + k_{Sp31}!k_{Sc21}k_{Sc11}]v_{C31}\end{aligned} \tag{6.14}$$

where the switch states, $k's$, are Boolean variables, and the operations between them are also Boolean.

For a given set of switch states from Table 6.1, some equations, from the set (6.5) through (6.14), become redundant, while some others render an infinite number of solutions. Therefore, only a subset of the equations are sufficient for finding the voltages based on the following matrix equation:

$$\begin{bmatrix} v_{D11} \\ v_{D21} \\ v_{D31} \\ v_{Su11} \\ v_{Sc11} \\ v_{Su21} \\ v_{Sc21} \\ v_{Su31} \\ v_{Sp31} \end{bmatrix} = A^{-1}B \begin{bmatrix} v_{C11} \\ v_{C21} \\ v_{C31} \\ v_{C41} \end{bmatrix} \tag{6.15}$$

where A is a i x i matrix, and i is the number of switch voltage variables, whereas B is a i x 4 matrix. Both matrixes have, as entry values, -1, 0, and 1. In (6.5) to (6.14), a voltage variable is said to be *included* in an equation, if a set of switch states return 1 as the coefficient of that voltage in the equation. However, if a set of switch states return 0 as the coefficient, the voltage variable is *excluded* from the equation. For example, in (6.9), if $k_{Sc11} = 1$, the voltage variable v_{D21} is excluded from the equation. Thus, A is the matrix formed by the switch states that control the inclusion of the switch voltage variables, whereas B is the matrix formed by

the switch states that control the inclusion of the capacitor voltage variables. As an example, assuming that the capacitor voltages are $v_{C11} = 2.05\ kV$, $v_{C21} = 2.1\ kV$, $v_{C31} = 2.15\ kV$, and $v_{C41} = 2.2\ kV$, corresponding to a maximum capacitor voltage variation of 10% of $\overline{v}_c = 2\ kV$, and that the set of switch states in the first LSM are as per line 4 from Table 6.1, then (6.8), (6.11), and (6.14) are neglected, together with the voltage across switches S_{u11} and S_{c21} (short-circuit). Therefore, (6.15) yields

$$\begin{aligned}\begin{bmatrix} v_{D11} \\ v_{D21} \\ v_{D31} \\ v_{Sc11} \\ v_{Su21} \\ v_{Su31} \\ v_{Sp31} \end{bmatrix} &= A^{-1}B \begin{bmatrix} 2.05 \\ 2.1 \\ 2.15 \\ 2.2 \end{bmatrix} \\ &= \begin{bmatrix} 4.15 \\ 3.2 \\ 3.25 \\ 1.05 \\ -1.05 \\ -1.1 \\ 1.05 \end{bmatrix} kV \end{aligned} \tag{6.16}$$

where

$$A = \begin{bmatrix} -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & -1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & -1 \\ 0 & 0 & -1 & 0 & 0 & 1 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{6.17}$$

and

$$B = \begin{bmatrix} -1 & -1 & 0 & 0 \\ 0 & -1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & -1 & -1 \\ 0 & 1 & -1 & 0 \end{bmatrix} \tag{6.18}$$

The voltage across switches S_{11} and S_{41} can be easily determined as $v_{S11} = v_{C11}$ and $v_{S41} = v_{C41}$. Thus, the voltages across the switches in the positive and negative half-bridges are not calculated by (6.16).

6.6 Advantages of the proposed topology

The advantages of the LSM over the previously introduced topologies are described as follows:

The high-efficiency links in the LSM, and the parallel link, connect terminals P_S and N_S with the minimum number of switches in series with the arm current. For this reason, the conduction losses in the LSM are approximately the same as those in the HBSM, and are lower than the other mentioned topologies featuring dc-side fault handling capability, with the exception of the LMMC. More specifically, when compared to the HBSM, the LSM uses an average of only 0.25 more switches to insert or bypass capacitors in the MMC arm, as described in detail in Section 5.3. Moreover, the switching losses in the LSM are lower, as compared to the other topologies, except the LMMC, due to the fact that the insertion of capacitors in the arm, to generate the desired level of the ac-side terminal voltage, can be achieved by the high-efficiency links; the LMMC has more high-efficiency links than the LSM and, therefore, features a lower power loss. However, it experiences higher voltages across its positive regular links, as compared to the LSM, since its negative regular links are composed by IGBTs.

The LSM experiences a reduced off-state voltage across its switches, i.e., the voltage across the IGBTs and IGCTs in the LSM exhibits lower magnitudes, as compared to other MMC topologies for HVDC systems. More specifically, the switches that form the positive regular links of the LSM experience a voltage of $\overline{v}_c/2$ in all switching combinations. Further, the switches forming the high-efficiency links and the parallel link experience a voltage of either $\overline{v}_c/2$ or $\overline{v}_c$, depending on the conduction states of the switches. In addition, the switches that form the positive and negative half-bridges experience a voltage of $\overline{v}_c$. Finally, the diodes, which constitute the negative regular links experience a voltage of $2\overline{v}_c$. However, high-voltage diodes are considerably more commonplace and remarkably less costly than fully-controllable switches of similar voltage and current handling capabilities.

Taking the example of HVDC system presented in [18] and [20], if the LSM were used as the SM, each arm would host 100 LSMs. Therefore, for a three-phase back-to-back system, 2400 IGBTs would experience the aforementioned reduced voltage in normal operation, for all switching configurations, whereas the remaining switches (apart from the diodes) would experience voltages of either $\overline{v}_c/2$ or $\overline{v}_c$.

Considering power losses, voltage stress of the switches, and dc-fault handling capability, it can be concluded that the LSM features an optimum solution.

6.7 Simulation results for the LSM

As it is the case for other MMC technologies that use the NLC switching strategy, the LSM-based MMC produces low-distortion ac-side terminal current waveforms only if its ac-side terminal voltage has an adequately large number of levels (high-density MMC). However, simulation models based on detailed models are difficult to create, and even more difficult to run. Therefore, detailed models were developed for LSM-based MMCs with $M = 4$, $M = 8$, and $M = 12$, for preliminary assessment of the principles of operation, dynamics, and behavior during dc-side faults. It is important to point out that for these values of M (4, 8, and 12), the voltage and current waveforms in the LSM-based MMC are expected to feature visible harmonic distortion. All simulations were conducted in the PSCAD/EMTDC software envi-

ronment [80].

6.7.1 Case I - Single-phase LSM inverter for $M = 4$

In this case, the simulation of a detailed model of a single-phase 5-level LSM-based MMC (i.e., with $M = 4$) was executed. The MMC, shown in Fig. 6.6 and its ac and dc systems, featured a dc-side voltage, v_{dc}, of 8 kV, which was impressed by two identical dc sources. The modulating signal and the ac grid voltage were represented by $m(t) = \sin(2\pi f_g t)$ and $v_g(t) = 2\sin(2\pi f_g t)$ kV, respectively, for $f_g = 60$ Hz. The remaining parameters of the system were $C = 3.1$ mF, $R = 15$ $m\Omega$, $L = 2$ mH, $R_t = 0.1$ Ω, and $L_t = 5$ mH. The system was equipped with a fault detection mechanism that compared the peak values of the arm currents, i_1 and i_2, with a threshold of 2.5 kA. Thus, the fault detection mechanism blocked the gating pulses of the switches, for 100-ms, if either of the two peak values exceeded the threshold.

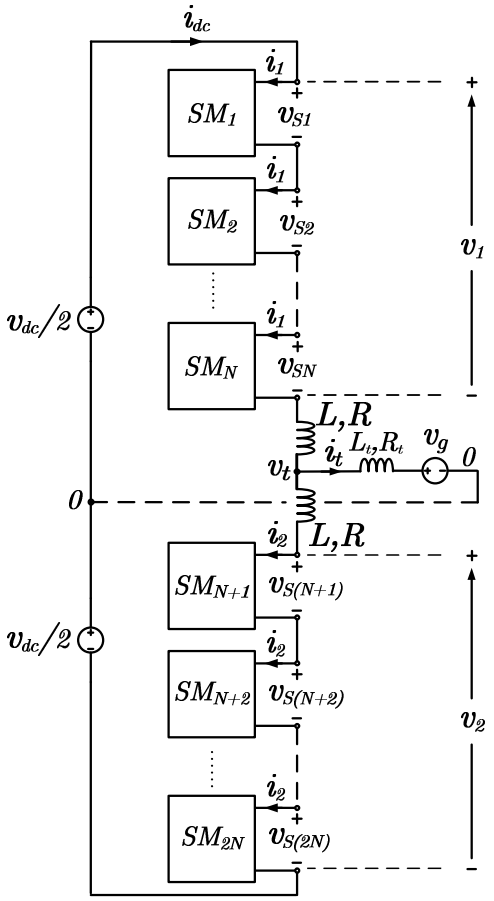

Figure 6.6: Schematic diagram of the single-phase LSM-based MMC system for Case I.

In the beginning of the simulation, the gating pulses of the switches were disabled and the capacitors were pre-charged. After the pre-charge, at $t = 0.03$ s the gating pulses were released and the LSM-based MMC operated normally until $t = 0.35$ s. From $t = 0.35$ s to $t = 0.4$ s, nodes "+" and "–" were connected through a short link, to simulate a 50-ms long dc-side fault. An instant after the dc-side fault occurrence, the fault detection mechanism of the LSM-based

MMC detected the fault and blocked the gating pulses, until $t = 0.45\ s$. Then, the gating pulses were unblocked and the LSM-based MMC went back to its normal operation. Figure 6.7 shows the waveforms of the LSM-based MMC detailed model.

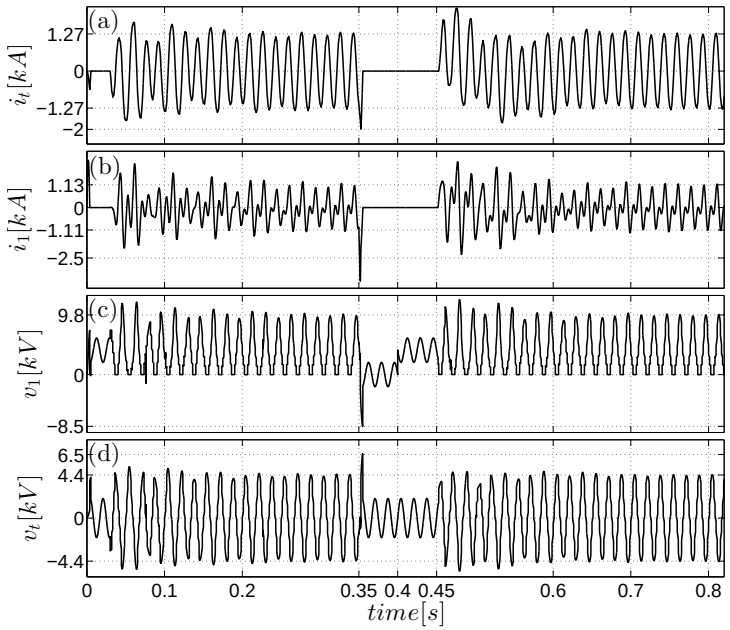

Figure 6.7: Waveforms of selected variables in an open-loop controlled single-phase 5-level LSM-based MMC, to various disturbances; Case I.

Figure 6.7 shows that, from $t = 0.35\ s$ to $t = 0.45\ s$, i.e., during the action of the fault detection mechanism, the arm current was driven to zero and, consequently, the arm voltage was equal to the negative of the grid voltage. From $t = 0.4\ s$ onwards, i.e., from the moment when the fault was cleared onwards, the arm voltages assumed the expected positive offset, i.e., $v_{dc}/2 = 4\ kV$, until the enabling of the gating pulses at $t = 0.45\ s$, while the arm currents remains zero. At $t = 0.45\ s$ and after, the currents and voltages went back to their pre-disturbance forms and magnitudes. Figure 6.7 also shows that the arm currents show harmonic distortion related to circulating current components. This effect is expected, due to the fact that the simulation was run in open-loop, and no circulating current suppression control was employed.

Figures 6.8 and 6.9 show the voltage and current waveforms for the switches of the first SM in the upper arm ($n = 1$) in the LSM-based MMC; the variables are labeled in accordance with the circuit of Fig. 6.5. It can be verified through the waveforms that the voltage magnitudes agree with the values predicted by the analysis of Section 6.5.

Figure 6.10 shows the voltage in the capacitor of the first SM in the upper arm. It can be verified that the voltage is balanced and that it remains constant during the action of the fault detection mechanism.

6.7.2 Case II - Three-phase LSM inverter for $M = 8$

For this case, the simulation of a detailed model of a three-phase 9-level LSM-based MMC, operating as an inverter in a system such as shown in Fig. 5.13, was executed under closed-loop control. The parameters were $C = 6\ mF$, $R = 15\ m\Omega$, $L = 2\ mH$, $R_t = 0.1\ \Omega$, and $L_t =$

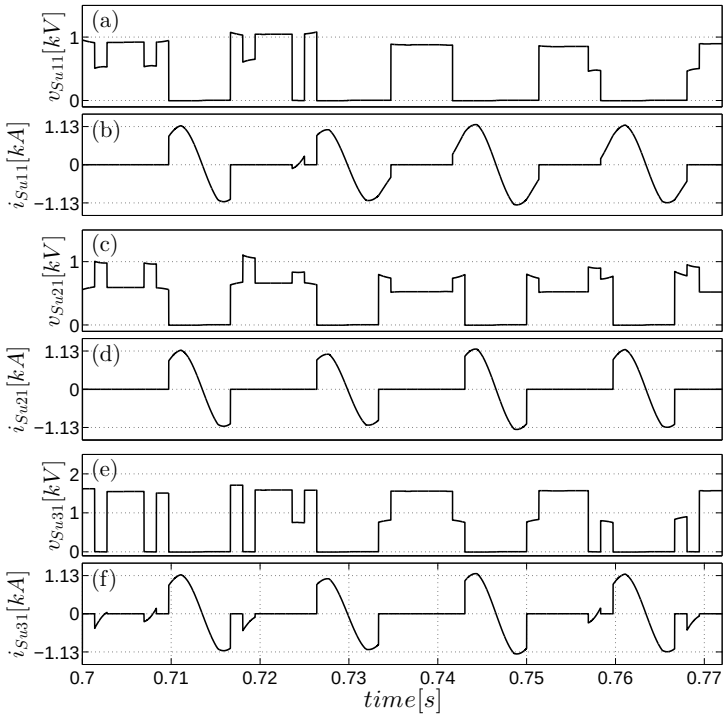

Figure 6.8: Voltage and current waveforms for the switches of the positive regular links for $n = 1$; Case I.

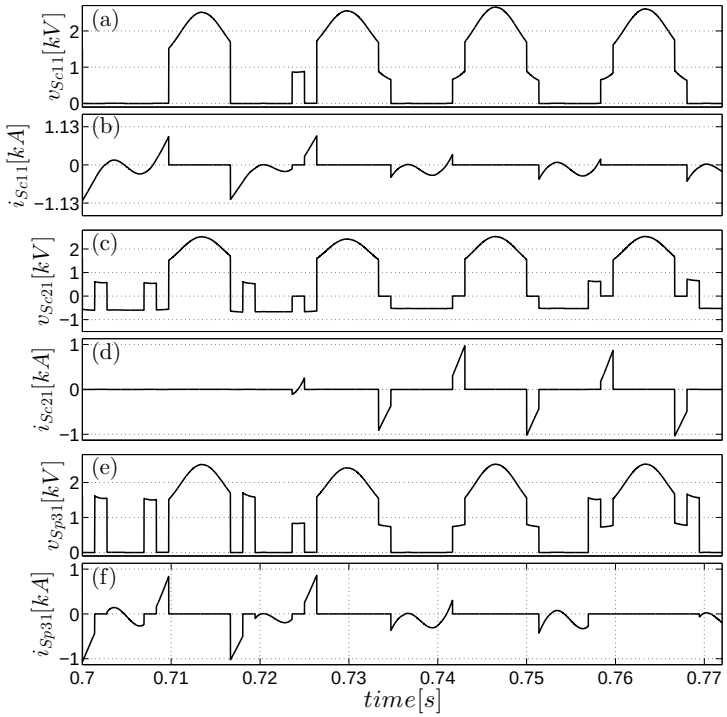

Figure 6.9: Voltage and current waveforms for the switches of the high-efficiency links and parallel link for $n = 1$; Case I.

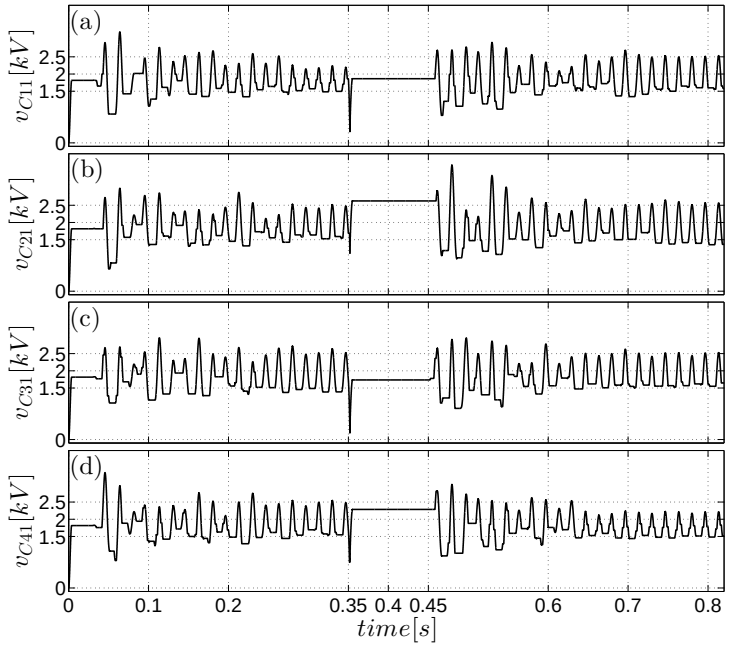

Figure 6.10: Waveforms of the capacitor voltages in the phase a of a open-loop single-phase 5-level LSM-based MMC, for $n = 1$, to various disturbances; Case I.

5 *mH*. The grid voltage presented a peak value of 2 *kV* with frequency of 60-Hz. The LSM-based MMC was current-controlled in a *dq* frame synchronized to the grid voltage, [10]. The converter was also equipped with the same fault detection mechanism as in Case I, except that the threshold was 1.5 *kA*. The fault detection mechanism disabled the current controller and the gating pulses for 100 *ms*, if any of the six arm current peak values exceeded the aforementioned threshold. Further, the fault detection mechanism also set the setpoint for the *d*-axis component of the ac-side terminal current to zero.

From the beginning of the simulation to $t = 0.03$ *s*, the gating pulses and the current controller were disabled. At $t = 0.03$ *s*, the gating pulses and the current controller were activated, with the real- and reactive-power setpoints both set to zero. At $t = 0.15$ *s*, the real-power setpoint was set to 2 *MW*, raising the setpoint for the *d*-axis component of the ac-side terminal current to $i_d^* = 0.66$ *kA*. At $t = 0.35$ *s*, a dc-side fault was simulated, by placing a short link across the dc-side terminals of the LSM-based MMC. The short link was removed after 50 *ms*. An instant after the dc-side fault occurrence, the fault detection mechanism of the LSM-based MMC detected the fault, blocked the gating pulses, and set i_d^* to zero. At $t = 0.45$ *s*, the gating pulses were unblocked, the current controller was enabled, and i_d^* was reset to its pre-disturbance value of 0.66 *kA*.

Figure 6.11 shows the waveforms of the ac-side terminal current, upper arm current, and upper arm voltage, for phase-*a*. Also, Fig. 6.11 presents the waveforms of the *d*- and *q*-axis components of the ac-side terminal current. It can be observed that, as expected, the arm current and the ac-side terminal current dropped to zero at the moment that the fault is detected. It can also be observed that the ac-side terminal current is visually distorted. In turn, the harmonic distortion, implicates in considerable ripples in the *d*- and *q*-axis current components. The harmonic distortion is, as mentioned in the beginning if this section, due to the small *M* applied

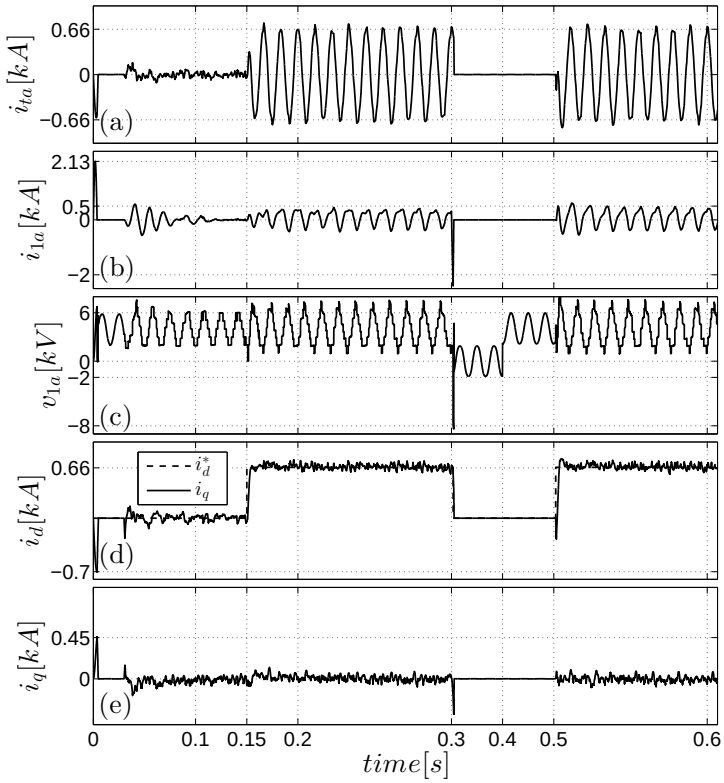

Figure 6.11: Waveforms of selected variables in a closed-loop controlled three-phase 9-level LSM-based MMC, to various disturbances; Case II.

in this case and, consequently, the low number of levels in the ac-side terminal voltage of the LSM-based MMC. If *M* is large, as illustrated in the back-to-back system simulated in Section 3.3.4, the NLC modulation strategy produces voltage and currents with no noticeable harmonic distortion.

Figure 6.12 depicts the balanced voltages in the capacitors belonging to the first SM in the phase a leg. As it was the case for Case I, the capacitor voltages remain constant during a fault.

6.7.3 Validation of the model for power losses

In this subsection, the detailed model presented in Case I was augmented to, first,$M = 8$, and then to $M = 12$. Also, detailed models for HBSM-based MMC featuring $M = 4$, 8, and 12 were developed. Then, the power losses were simulated for both the LSM-based MMC and HBSM-based MMC detailed models, and the power loss ratio, described in Section 6.4, was calculated for each model. Table 6.3 shows the power loss ratio, H, for the simulated MMCs.

The power loss ratio showed in Table 6.3 agrees well with the calculated power loss ratio presented in Section 6.4, with a maximum error of 2%.

6.8 Summary and Conclusions

This chapter proposed a new submodule topology for MMC-based HVDC system applications. The proposed submodule topology, referred in this thesis to as the *Lattice Submodule* (LSM),

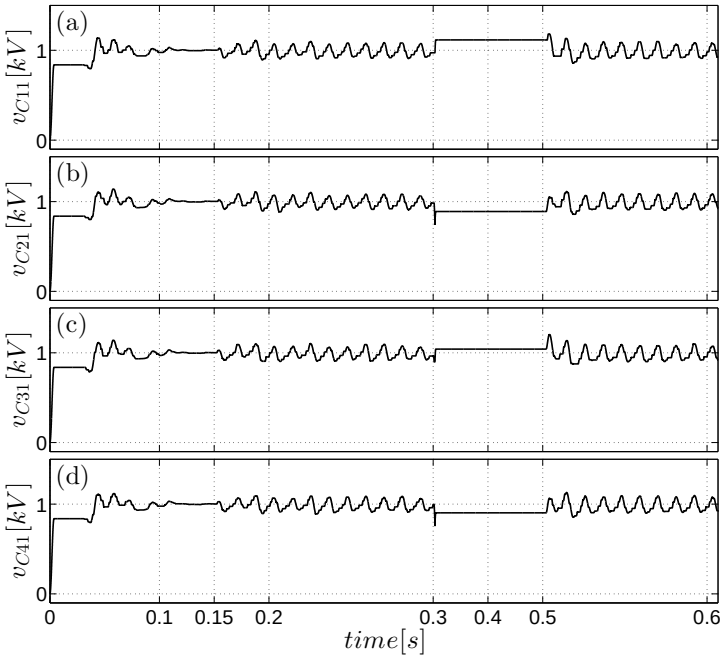

Figure 6.12: Waveforms of the capacitor voltages in the phase a of a closed-loop controlled three-phase 9-level LSM-based MMC, for $n = 1$, to various disturbances; Case II.

Table 6.3: Simulated power losses and H.

Converter	Power loss	H
5-level LSM-based MMC	$0.0289MW$	1.086
5-level HBSM-based MMC	$0.0266MW$	
9-level LSM-based MMC	$0.03MW$	1.071
9-level HBSM-based MMC	$0.028MW$	
13-level LSM-based MMC	$0.058MW$	1.076
13-level HBSM-based MMC	$0.054MW$	

was demonstrated to offer the same dc-side fault handling capability of an equivalent full-bridge submodule (FBSM), while it features, approximately, the same power losses as those of the half-bridge submodule (HBSM). Further, the LSM was shown to feature smaller voltage stress in the switches in comparison with other topologies mentioned in this thesis. The effectiveness of the LSM was demonstrated through time-domain simulation of single-phase and three-phase systems, assuming various normal and faulted operating scenarios.

Chapter 7

Conclusions, Contributions, and Future Work

7.1 Conclusions

The conclusions of this thesis are as follows:

1. To address the issues exhibited by the current submodule capacitor sizing methods, a new method was proposed in this thesis. The proposed method is based on a complete steady-state model that allows for the prediction of the magnitude of the harmonic components in the MMC submodule capacitor voltages, arm voltages, and arm currents. Consequently, it became possible to develop approximate equations for the submodule capacitor voltage harmonic components, that, in turn, allowed for the calculation of the voltage crest and trough. The summation of the submodule capacitor voltage crest and trough, gave rise to an analytical equation for the submodule capacitor calculation as a function of the submodule capacitor voltage variation. Further, the method proposed in this thesis can also calculate the impact of the circulating current (injected or not) in the size of the submodule capacitor.

2. This thesis demonstrated that the MMC can be simulated through a simplified equivalent-circuit simulation model, without losing information regarding the dynamics of the submodule capacitor voltage. The simplified equivalent-circuit model was proven to have negligible error in comparison to detailed models, while exhibiting a higher simulation speed.

3. This thesis also demonstrated that the dc-fault handling capability of the MMC can be maintained while the power losses in the MMC arm are decreased, in comparison to the topologies currently known. In addition, it was demonstrated that the voltage stress on the switches can also be decreased, through a new arrangement of the arm capacitors, giving rise to a new submodule topology. Fig. 7.1 illustrates the comparison between the topologies mentioned in this thesis, regarding dc-side fault handling capability, average number of series-connected switches, and voltage stress.

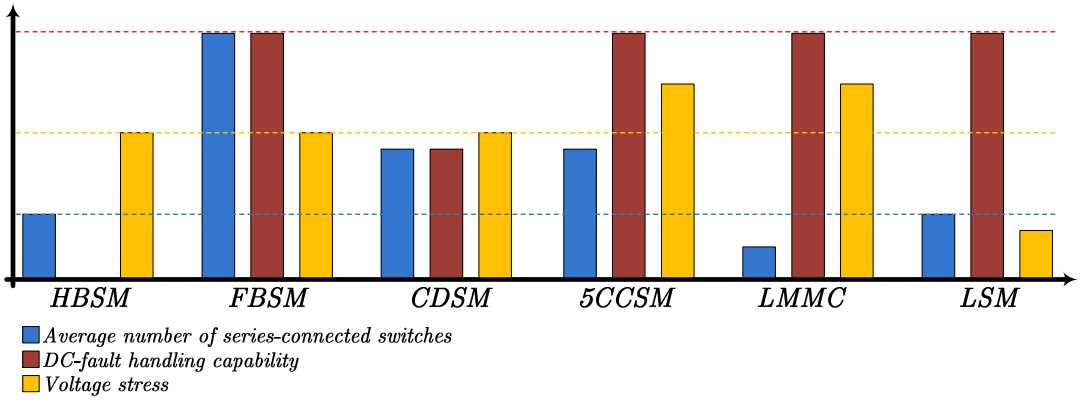

Figure 7.1: Illustrated comparison between the half-bridge submodule, the full-bridge submodule, the clamp-double submodule, the 5-level cross-connected submodule, the lattice modular multilevel converter, and the lattice submodule, regarding dc-side fault handling capability, average number of series-connected switches, and voltage stress.

7.2 Contributions

This thesis presents the following contributions:

1. A complete steady-state model that can be used to predict the amplitude of each harmonic component in the MMC currents and voltages, and an accurate and completely analytical method for sizing the submodule capacitor: The proposed harmonic model is capable of predicting the amplitude of the harmonic components of the MMC arm voltages, submodule capacitor voltages, and arm currents. Further, based on the proposed harmonic model, a capacitor sizing method is proposed to determine the capacitance of the submodule capacitor for a desired level of voltage variation, without a need for numerical algorithms or graphs used by the existing methods. In addition, the proposed capacitor sizing method can accurately determine the required capacitance even if circulating currents are injected to mitigate dc voltage fluctuations.

2. A new equivalent-circuit simulation model that enables convenient and fast simulation of MMC systems including those featuring dc-fault handling: The equivalent-circuit-based simulation model assumes ideal submodule switches to speed up the simulation, but is nonetheless capable of capturing the transients as well as harmonic components of the voltages and currents.

3. A feedforward control strategy for canceling the arm voltage component responsible for the formation of the circulating current: The proposed compensation strategy calculates the magnitude of the second harmonic component of an arm voltage, and uses the calculated value as a feedforward signal to cancel the circulating current of the corresponding MMC leg. The proposed feedforward compensation strategy, if combined with a closed-loop circulating current suppression strategy, greatly mitigates the possibility of control saturation and, also, results in better damped closed-loop dynamics.

4. New MMC topologies with dc-side fault current handling capability and higher efficiency than that featured by the topologies reported in the literature: Finally, the thesis

proposes two new MMC topologies for enhanced efficiency and dc-side fault handling capability. In the first proposed topology, that is the *lattice modular multilevel converter* (LMMC), the entire MMC arm is modified to accommodate *networks* that allow shortcuts between the arm capacitors, thus, reducing conduction power losses of the converter. In the second topology proposed, however, only the submodule is modified. In the proposed submodule topology, referred to as *lattice submodule* (LSM), the conduction power losses are decreased, as it is the case for the LMMC, with the difference that the voltage stress in the switches are also reduced.

7.3 Future Work

The following topics are suggested for a future work:

1. Equivalent-circuit simulation models for the LMMC and the LSM that can adequately simulate conduction and switching losses in the switches faster than detailed models;

2. A reliability and redundancy study for the LMMC and the LSM, where the behavior of the LMMC and the LSM are to be studied in detail. In addition, the fault conditions in which the LMMC and LSM continue to operate normally are to be addressed. Further, new switching schemes, that consider the possible redundant states of both topologies, are a important part of the suggested research. Finally, possible modifications to the topology, to increase the converter reliability, have also to be addressed;

3. The study of DC-DC topologies based on the LMMC and the LSM, for multiterminal HVDC (MTDC) transmission systems; and

4. The adaptation of the steady-state model and capacitor sizing method, presented in Chapter 2, for grid-connected medium-voltage systems, e.g., shipboard drives or off-shore wind energy systems, where the footprint is a major design consideration.

Appendix A

Example of program code for the SEC Simulation Model

A.1 Function calling and variables initialization

void integrate(double *iup, double *idw, double *vmu, double *vmd, double *aux, double *ts, double *c, int *m, double *clk, double *ref, double *vdc, double *aux2, double *balance, double *enable, double *vg, double *fs, double *cm, double *li, double *lit, double *zr)

```
int nm = *m; // number of submodules per arm - int
int narmi = nm;
double cap = *c; // submodule capacitance
double T = *ts; // numeric calculation sampling time - informed by user
int ct = (int) *clk; // level clock
double iu = *iup;
double id = *idw;
static double iue = 0;
static double ide = 0;
static double iu1 = 0; // current last sample
static double id1 = 0;
static double it1 = 0;
int freq = (int) *fs; // time step frequency
static double indvolt1 = 0; // inductor voltage
static double indvolt2 = 0; // inductor voltage
static double indvolt t = 0;
double ind = 0; // arm inductance
double ind t = 0;
double zero = *zr; // zero definition - 0.05
double narm = (double) nm; // number of modules per arm - double
double fref = *ref; // Vt voltage reference
static double r; // converter resolution
static double sh; // module shift
```

```
    double v = *vdc; // DC voltage
    int bal = (int) *balance; // voltage balancing algorithm frequency
    static int neg1 = 0;
    static int neg2 = 0;
    double vgrid = *vg; // grid voltage
    static double iuplast[500]; // upper arm last current vector
    static double idwlast[500]; // lower arm last current vector
    static double vuplast[500]; // upper arm last voltage vector
    static double vdwlast[500]; // lower arm last voltage vector
    static double vcup[500]; // upper arm module capacitor voltage vector
    static double vcdown[500]; // lower arm module capacitor voltage vector
    static double vcupaux[500]; // upper arm module capacitor voltage vector auxiliar
    static double vcdownaux[500]; // lower arm module capacitor voltage vector auxiliar
    static double vmu[500]; // upper arm module voltage vector
    static double vmd[500]; // lower arm module voltage vector
    static double mup[500]; // upper module activation vector
    static double mdw[500]; // lower module activation vector
    static double upperarm; // total voltage in the upper arm
    static double lowerarm; // total voltage in the lower arm
    static int count = 0; // start-up counter - if count is 1 the start up routine is disabled and i
must be 0
    static int countu = 0;
    static int countd = 0;
    static int count2 = 0; // vector zeroing counter
    static int i = 0;
    static int z = 0; // voltage balancing algorithm auxiliar variable
    static int faux = 0;
    int j = 0;
    int k = 0;
    int b = 0;
    static int x = 0;
    static int a = 0;
    int position;
    static int ndown = 0; // number of modules on in the lower arm
    static int nup = 0; // number of modules on in the upper arm
    int sw1 = 0;
    int sw2 = 0;
    double l;
    double h;
    static int test = 1;
    static int en;
    double vcm = *cm; // common-mode control contribution
```

A.2 Modulation routine - controlled by T_s

```
if((freq == 1)&&(faux == 0))
    r = v/narm; // resolution = Vdc / number of submodules per arm
    en = (int) *enable; // enable switches signal
    ind = *li; // inductance in henrys
    indt = *lit; // inductance in henrys


    if ((ct == 1)&&(i == 0)) // level clock
    sh = round(fref/r); // shift calculation
    if(sh > (narm/2)) // saturation
    sh = (narm/2);
    if(sh < -(narm/2))
    sh = -(narm/2);
    if (sh >= 0) // number of modules on per arm calculation - positive voltage
    ndown = (int)((narm/2) + sh - round(vcm/r));
    nup = (int)((narm/2) - sh - round(vcm/r));
    if (sh < 0) // number of modules on per arm calculation - negative voltage
    nup = (int)((narm/2) - sh - round(vcm/r));
    ndown = (int)((narm/2) + sh - round(vcm/r));
    if(nup > nm)
    nup = nm;
    if(ndown > nm)
    ndown = nm;
    if(nup < 0)
    nup = 0;
    if(ndown < 0)
    ndown = 0;
    i++;

if ((ct == 0)&&(i == 1)) // the second condition allows the modules voltage start-up
    i = 0;
```

A.3 VBA routine - controlled by T_{VBA}

```
if ((bal == 1)&&(z == 0))

for(j=0;j<nm;j++) // switch off all modules in the upper and lower arm
    mup[j] = 0.0; // turn off the activation signal on all upper modules
```

```
    mdw[j] = 0.0; // turn off the activation signal on all lower modules
    x = 0;
if (iu > 0.0) // positive current in upper arm - charge modules
    b = 0;
    for(j=0;j<nm;j++)
    if(b == nup) // stop condition
    break;
    for(k=0;k<nm;k++)
    if(k == 0) // first value
    l = vcupaux[k];
    position = k;
    if((vcupaux[k] < l)&&(vcupaux[k] != 1000)) // search the lowest value
    l = vcupaux[k];
    position = k;
    mup[position] = 1.0; // set the activation vector position
    vcupaux[position] = 1000; // erase module voltage
    b++;
    x++;

if (iu <= 0.0) // negative current in upper arm - discharge modules
    b = 0;
    for(j=0;j<nm;j++)
    if(b == nup) // stop condition
    break;
    for(k=0;k<nm;k++)
    if(k == 0) // first value
    h = vcupaux[k];
    position = k;
    if((vcupaux[k] > h)&&(vcupaux[k] != -1)) // search the lowest value
    h = vcupaux[k];
    position = k;
    mup[position] = 1.0; // set the activation vector position
    vcupaux[position] = -1; // erase module voltage
    b++;
    x++;

if (id > 0.0) // positive current in lower arm - charge modules
    b = 0;
    for(j=0;j<nm;j++)
    if(b == ndown) // stop condition
    break;
    for(k=0;k<nm;k++)
    if(k == 0) // first value
    l = vcdownaux[k];
    position = k;
```

```
    if((vcdownaux[k] < l)&&(vcdownaux[k] != 1000)) // search the lowest value
    l = vcdownaux[k];
    position = k;
    mdw[position] = 1.0; // set the activation vector position
    vcdownaux[position] = 1000; // erase module voltage
    b++;
    x++;

if (id <= 0.0) // negative current in lower arm - discharge modules
    b = 0;
    for(j=0;j<nm;j++)
    if(b == ndown) // stop condition
    break;
    for(k=0;k<nm;k++)
    if(k == 0) // first value
    h = vcdownaux[k];
    position = k;
    if((vcdownaux[k] > h)&&(vcdownaux[k] != -1)) // search the lowest value
    h = vcdownaux[k];
    position = k;
    mdw[position] = 1.0; // set the activation vector position
    vcdownaux[position] = -1; // erase module voltage
    b++;
    x++;
    a = 0;
for(j=0;j<nm;j++) // confirmation of the number of modules on - it must be always the number
of modules per arm
    if(mup[j] == 1.0)
    a++;
    if(mdw[j] == 1.0)
    a++;
    z++;

if ((bal == 0)&&(z == 1))
    z = 0;
```

A.4 Submodule Capacitor Voltage Calculation Routine - controlled by T_i

```
for(j=0;j<nm;j++) // sweep the whole arm

if(en == 1)
```

```
    sw1 = (int) mup[j]; // create equivalent int value
    switch (sw1) // test module activation signal - upper arm
    case 0: // module off
    vcup[j] = vuplast[j];
    vcupaux[j] = vuplast[j];
    vmu[j] = 0;
    iuplast[j] = 0;
    vuplast[j] = vcup[j];
    break;
    case 1: // module on
    vcup[j] = ((T/(2*cap))*iu)+(iuplast[j]*(T/(2*cap)))+vuplast[j]; // module capacitor voltage
equation - tustin integration
    if(vcup[j] < 0)
    vcup[j] = 0; // saturation, the SM voltage do not become negative
    vcupaux[j] = vcup[j];
    vmu[j] = vcup[j];
    vuplast[j] = vcup[j];
    iuplast[j] = iu;
    break;
    sw2 = (int) mdw[j]; // create equivalent int value
    switch (sw2) // test module activation signal - lower arm
    case 0: // module off
    vcdown[j] = vdwlast[j];
    vcdownaux[j] = vdwlast[j];
    vmd[j] = 0;
    idwlast[j] = 0;
    vdwlast[j] = vcdown[j];
    break;
    case 1: // module on
    vcdown[j] = ((T/(2*cap))*id)+(idwlast[j]*(T/(2*cap)))+vdwlast[j]; // module capacitor volt-
age equation - tustin integration
    if(vcdown[j] < 0)
    vcdown[j] = 0; // saturation, the SM voltage do not become negative
    vcdownaux[j] = vcdown[j];
    vmd[j] = vcdown[j];
    vdwlast[j] = vcdown[j];
    idwlast[j] = id;
    break;

if(en == 0) // switches disabled
    iue = iu;
    ide = id;
    if((iu >= -zero)&&(iu < zero))
    iue = 0;
    if((id >= -zero)&&(id < zero))
```

```
    ide = 0;
    vcup[j] = (((T/(2*cap))*fabs(iue))+(iuplast[j]*(T/(2*cap)))+vuplast[j]); // module capacitor voltage equation - tustin integration - current always positive due to SM topology
    vcupaux[j] = vcup[j];
    vmu[j] = vcup[j];
    vuplast[j] = vcup[j];
    iuplast[j] = fabs(iue);
    vcdown[j] = (((T/(2*cap))*fabs(ide))+(idwlast[j]*(T/(2*cap)))+vdwlast[j]); // module capacitor voltage equation - tustin integration
    vcdownaux[j] = vcdown[j];
    vmd[j] = vcdown[j];
    vdwlast[j] = vcdown[j];
    idwlast[j] = fabs(ide);
```

A.5 Arm Voltage Calculation Routine

```
upperarm = 0;
    lowerarm = 0;
if(fabs(iu) < zero)
    iu = 0;
    count = 0;

if(fabs(id) < zero)
    id = 0;

if(fabs(iu) >= zero)
    count = 1;

if(en == 0)
    for(j=0;j<nm;j++) // sweep the whole arm
    upperarm = vcup[j] + upperarm;
    lowerarm = vcdown[j] + lowerarm;
    if(((upperarm) < fabs(vgrid))——(fabs(iu) > zero))
    if(iu > zero)
    *vmu = upperarm;
    if(iu < -zero)
    *vmu = -upperarm;
    else
    *vmu = (v/2)-vgrid;
    if(((lowerarm) < fabs(vgrid))——(fabs(id) > zero))
    if(id > zero)
    *vmd = lowerarm;
    if(id < -zero)
```

```
    *vmd = -lowerarm;
    else
    *vmd = (v/2)+vgrid;

if(en == 1)
    for(j=0;j<nm;j++) // sweep the whole arm
    upperarm = vmu[j] + upperarm;
    lowerarm = vmd[j] + lowerarm;
    *vmu = upperarm;
    *vmd = lowerarm;
    *aux = vcup[3];
    *aux2 = vcdown[3];
    faux++;

if((freq == 0)&&(faux == 1))
    faux = 0;
```

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