Time-Mode Signal Processing and Application in $\Delta\Sigma$ ADC Design

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ABSTRACT

An all-digitally implemented 1^{st} order and a 2^{nd} order time-mode $\Delta\Sigma$ ADCs are proposed and presented in this dissertation. Each proposed $\Delta\Sigma$ ADC consists of a voltage-to-time integration converter, a seven-stage gated ring oscillator functioning as a 3-bit quantizer, and a 7-stage digital differentiator that provides noise-shaping and frequency feedback. The 2^{nd} order architecture differs from the 1^{st} order by cascading two digital differentiators. The 2^{nd} order design improves noise-shaping characteristic and SNDR. However it does not effectively suppress the harmonic tones due to the non-linear effect of the circuit components. Thus a detailed analysis of the nonlinear characteristics of the modulator is conducted. Designed in IBM 130 nm 1.2 V CMOS technology and with a 100 kHz 100 mV input, the 1^{st} order time-mode $\Delta\Sigma$ ADC exhibits an SNDR of 45.5 dB over 0.4 MHz bandwidth with power dissipation of 1.1mW. In comparison, the 2^{nd} order ADC provides 54.8 dB SNDR, which equivalently offers an ENOB of 8.8 and it consumes 1.45 mW RMS power. The figure-of-merit of the 2^{nd} order time-mode $\Delta\Sigma$ ADC is 407 pJ/step. Since the order of the system cannot be increased by simply cascading more differentiator stages, a time-mode $\Delta\Sigma$ ADC architecture employing a time-mode loop filter is suggested in the last chapter. Several key building blocks including a time amplifier, time register and time adder for implementing such a loop filter are presented. The time amplifier has an input dynamic range of 50ps and provides a gain of 20. The implemented time register has a dynamic range of $5ns$ and a peak error of $\pm 2\%$ over the $5ns$ full scale. The time adder remains high accuracy as long as the input time difference is no greater than $1.6ns$.

Keywords: TMSP, time-difference variable, open-loop ADC, closed-loop ADC, $\Delta\Sigma$ ADC, VTC, voltage-controlled delay unit, current-starved inverter, pulse generator, GRO, delay line, TDC, VCO-based quantizer, digital counter, digital differentiator, noise-shaping, SNDR, SFDR, OSR, ENOB, harmonics, FFT, time-mode loop filter, time amplifier, time register, gated delay cell, time adder, time accumulator.

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List of Abbreviations

ADC	Analog-to-Digital Converter
BW	Bandwidth
$CMOS$	Complementary MetalOxideSemiconductor
CP	Charge Pump
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DLL	Delay-Locked-Loop
FFT	Fast Fourier Transform
$FO4$	Fan-out of 4
GDC	Gated Delay Cell
GRO	Gated Ring Oscillotor
GSM	Global System for Mobile
LSB	Least Significant Bit
$MASH$	Multi-stage Noise Shaping
OSR	Over Sampling Ratio
PD	Phase Detector
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop

PSD	Power Spectral Density
PVT	Process (supply-)Voltage Temperature
PWM	Pulse Width Modulation
SAR	(Successive Approximation Register
S/H	Sample-and-Hold
$SNDR$	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
$SQNR$	Signal-to-Quantization-Noise Ratio
TDC	Time-to-Digital Converter
VCO	Voltage-Controlled Oscillator
VTC	Voltage-to-Time Converter
XOR	Exclusive OR

Chapter 1

Introduction

This chapter explains the motivation of this dissertation by introducing a circuit topology, known as time-mode circuits, for signal processing. Time-mode circuits where information is represented by the time difference variables possess a number of intrinsic characteristics that are scaled well with technology, making them a viable option to implement some key building blocks of mixed-signal systems such as analog-to-digital converters and phase-locked loops for signal processing.

1.1 Motivation

The rapid advance of CMOS technologies has primarily been geared towards optimizing the performance of digital systems. It is evident in Fig.1.1 Left that the power supply V_{DD} of CMOS circuit has dramatically dropped while the threshold voltage V_{TH} has very slow decline with technology scaling over the past years. Consequently, analog circuits are not only losing the benefit of process-controlled components, but they also must cope with rapidly voltage headroom loss. In addition to deteriorating signal-to-noise ratio, the shrinking voltage headroom also signifies the effect of the nonlinear characteristics of MOS transistors, while meeting ever-demanding performance specifications [15, 16, 17]. Although current-mode approaches offer an alternative means to combat voltage headroom loss, the existence of low-impedance nodes throughout current-mode circuits gives rise to high power consumption [18]. The improved switching characteristics of MOS transistors from technology scaling offer a superior timing accuracy quantified by the ratio of FO4 to the period of analog signals that has well surpassed the voltage resolution of analog circuits. As a result, a new design

paradigm where information is represented by the time difference of Boolean signals rather than the nodal voltages or branch currents of electric networks offers a new means to combat the scaling-induced design challenges that were once seemed unconquerable.

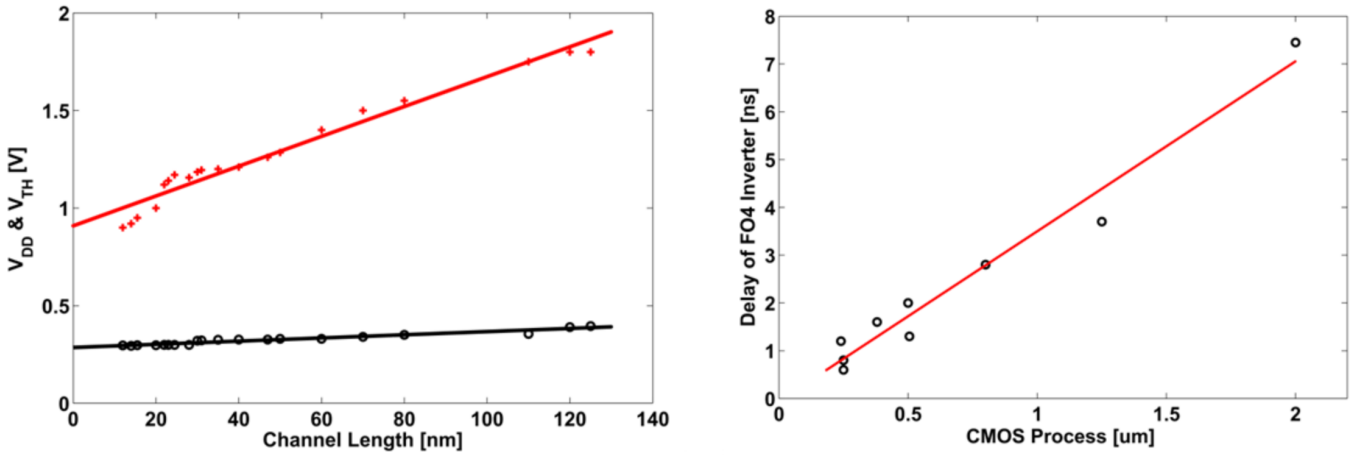


Figure 1.1: Left: Power Supply and Threshold Voltage Scaling in CMOS Technology. Right: Improvement in Delay for an FO4 Inverter due to Scaling

1.2 Overview of Time-Mode Signal Processing

Unlike voltage-mode or current-mode circuits, time-mode circuits depict an analog signal using the time difference between the rising edges of two digital signals with the time difference directly proportional to the amplitude of the analog signal. Because time-mode circuits perform analog signal processing in the digital domain, not only their performance scales well with technology, these circuits also offer a superior speed with low power consumption, enabling them to process high-frequency signals without sacrificing power consumption. Since the inception of time-mode signal processing, an immense effort has been made on researching for design techniques and exploring applications of time-mode circuits. Time-mode analog-to-digital converters with resolution up to 12.5 bits, bandwidth up to 20 MHz, signal-to-noise ratio (SNR) over 80 dB, and signal-to-noise-pulse-distortion-ratio (SNDR) over 70 dB have been reported [1, 19, 20]. Time-mode circuits have also been used

in audio [21], medical imaging [22], instrumentations [23], infinite-impulse-response (IIR) filters [24], finite-impulse-response (FIR) filters [25], and anti-imaging filters [26], frequency synthesizers [27, 28], delay-locked loops (DLL) [29], multi-Gbps serial links [30], and programmable band/channel select filters for software-defined radio [31], to name a few. In spite of these development, there are very few literatures that offer a comprehensive treament of the principle and design techniew of CMOS time-mode circuits for mixed-signal processing. Therefore a comprehensive treatment of time-mode circuits with an emphasis on both the principle and design techniques of the building blocks is provided in the next few chapters as part of this dissertation.

1.3 Current Literatures on Time-Mode ADC

Time-mode approaches of signal precessing represent analog signals as timing information of digital signals. They benefit from technology scaling and compensate deteriorated voltage accuracy in voltage-mode approaches. Therefore they offer a technology-friendly alternative means for data conversion[15, 17]. Li *et al.* showed that time-mode data conversion can be achieved by converting input voltage into time variables using a voltage-to-time converter (VTC) and then quantizing the time variable using a time-to-digital converter (TDC)[32]. Itawa *et al.* demonstrated a time-mode ADC implemented using a multi-stage ring VCO in conjuction with a reset counter[33]. The VCO-based ADC in Itawa's design allows the voltage-to-time conversion to operate in continuous time domain. In addition, this VCO-based ADC possesses inherent first-order noise-shaping. However, the conversion speed and samping rate is limited by the reset time of the counter. Hence the reset counter is undesired especially in $\Delta\Sigma$ADCs which require high OSR to achieve better SNDR. Hovin *et al.* replaced the reset counters with digital differentiators to achieve the same first-order noise-shaping [34, 35]. This type of VCO-based time-mode ADC offers the key advantage of high speed due to the absence of counters and an improved resolution, thereby permitting a large OSR. Straayer *et al.* showed that gated ring oscillator-based TDC also possess the desired first-order noise-shaping characteristics [19].

The performance of VCO-based time-mode ADCs, however, is greatly affected by the nonlinear voltage-to-frequency characteristics of VCOs [36]. It is well understood that $\Delta\Sigma$ modulators is effective in reducing the effect of nonlinear elements placed in the forward path of the modulators, provided that the loop gain in the desired frequency band is sufficiently large. In addition, quantization noise is both noise-shaped by the loop characteristics and suppressed by the loop gain. The reduced swing of the control voltage of VCOs due to negative feedback also improves the linearity of VCO quantizers. In order to increase the order of time-mode $\Delta\Sigma$ ADCs so as to better noise-shape quantization noise and suppress nonlinearity subsequently achieve a larger SNDR, voltage-mode active loop filters have been widely used [1, 37]. Unfortunately, the performance of active loop filters scales poorly with technology. The finite slew rate and high power consumption of active filters also limit their applications.

1.4 Thesis Outline

This dissertation is organized as the following: Chapter 2 provides some background information on conventional ADC and Time-Mode ADC and highlights some important design parameters for evaluating performance. Chapter 3 discusses the important building blocks in a time-mode ADC by giving circuit implementation examples. The proposed 1^{st} and 2^{nd} order time-mode $\Delta\Sigma$ ADCs are detailed in Chapter 4 where simulation results are also given. In Chapter 5, equipment set-up and experiment results are presented. Chapter 6 concludes the dissertation and an outline for future work is proposed in Chapter 7.

Chapter 2

Time-Mode ADC Design

2.1 Conventional ADC and Design Specifications

Analog-to-digital converter (ADC) is a circuit that converts a sampled analog signal in continuous time domain into a discrete digital code in discrete time domain. Based on sampling rate, conventional ADC can be classified into two types: Nyquist-rate ADC and oversampled ADC. A Nyquist-rate ADC samples the input at a frequency twice as that of the input signal bandwidth. This type of ADCs include: flash, pipeline, successive approximation register and integrating ADCs. An oversampled ADC performs data conversion at a frequency much higher than the Nyquist frequency. The oversampling ratio is defined as:

$$OSR = \frac{f_s}{2f_B}. \tag{2.1}$$

where f_s is the sampling frequency and f_B represents the signal bandwidth.

2.1.1 Introduction to Conventional ADC

Flash, pipeline, successive approximation register (SAR), integrating and delta-sigma are the five main conventional ADC architectures. They are best suited for different particular applications based on signal bandwidth, sampling frequency, resolution, power, area and noise rejection requirements.

Flash ADC - In a flash ADC, comparators are used in parallel to compare the input analog

signal to a specific reference value. The output from the parallel comparators is a thermometer code which later on will be encoded into a binary value. As implied by its name, a flash ADC can operate at an extremely fast speed. However, a high-resolution flash ADC consumes a large amount of power and silicon area.

Pipeline ADC - If the residue of a flash ADC, which is defined as the difference between the input analog signal and the corresponding digital output, is converted to a voltage using a DAC, amplified and processed in the next stage (a.k.a "pipelining"), then it becomes a pipeline ADC. The pipeline ADC has high data throughput because the entire converter operates on multiple input samples. One of the drawbacks of a pipeline ADC is the errors caused by process variation in flash ADC, DAC and amplifier in each pipeline stage. Also this type of ADC suffers from latency since each sample has to wait until the residue propagates through the pipeline.

SAR ADC - A successive approximation register (SAR) ADC performs binary search on the sampled input analog voltage. To implement teh binary search mechanism, the register output is initiated to the mid-scale digital value. The SAR ADC is best suited for low power and small area application with medium resolution requirement.

Integrating ADC - For an integrating ADC, it operates as follows: first a ramp is generated by integrating a reference voltage in the meanwhile a counter starts to count. A sampled input voltage is compared to the ramp value. The comparator output doesn't switch until the ramp value equals the sampled input voltage. Then the counter output is recorded before a reset action. The operation an integrating ADC is somewhat similar to a time-mode ADC since the counter output is a record of time duration which is proportional to the input voltage. The performance is highly dependant on the integrator accuracy.

Delta-Sigma ADC - $\Delta\Sigma$ ADC is different from other ADC types due its unique closed-loop architecture. The $\Delta\Sigma$ ADC operates by first quantizing the input voltage using a coarse quantizer. Then the digital output is subtracted from its corresponding analog input sample

to produce the quantization error. Next the quantization error is subtracted from the next analog input sample. In time domain, the operation can be represented by the equation:

$$V_{out}[n] = V_{in}[n] + (E_q[n] - E_q[n-1]). \tag{2.2}$$

It can be observed that in eqt. 2.2, quantization error can be minimized if the the quantization errors from two consecutive samples are very close. This can be achieved by purposely randomizing the quantization noise (dithering) and over sampling. From frequency domain perspective, the quantization noise power is a fixed value over the entire sampling frequency spectrum. Within the signal bandwidth, quantization noise power is being suppressed by the loop filter and is pushed to higher frequencies. This is known as noise-shaping. One benefit of the $\Delta\Sigma$ ADC is that the overall resolution can be improved by increasing over sampling ratio without requiring a high-resolution flash ADC.

2.1.2 ADC Performance and Design Specifications

There are many design specifications to be satisfied when designing an ADC. These specifications include the signal bandwidth or sampling rate, resolution, distortion, signal-to-noise-and-distortion ratio (SNDR), dynamic range, figure of merit, power, area, noise performance and latency. In this section, these specifications will be explained in details.

Signal Bandwith or Sampling Rate - The signal bandwidth of an ADC is defined as the frequency range over which the ADC maintains its designated resolution. For Nyquist-rate ADC, the signal bandwidth and sampling rate are related by the Nyquist criterion, which states that the sampling rate of the ADC should be at least twice of the signal bandwidth. For $\Delta\Sigma$ ADCs, the required sampling rate is much higher than the Nyquist rate.

Resolution, Dynamic Range and Distortion - The resolution of an ADC is defined as the smallest analog input change that will result in an least significant bit (LSB) change in the digital output code. Resolution measures how accurately the digital output can represent

the analog input. Quantization error is usually related to the resolution of the ADC and it generates a noise floor in the power spectral density (PSD) of the ADC's output. Eqt. can be used to approximate the power of noise floor.

$$P_\epsilon = \frac{LSB^2}{12} = \frac{(\frac{A_{FS}}{2^N-1})^2}{12}, \tag{2.3}$$

where A_{FS} represents the ADC's full scale. Distortion is usually caused by the nonliearity of semiconductor devices and mismatches between identical circuit components. The effect of mismatch can be minimized by careful layout with common centroid configuration, dynamic element matching (DEM) and calibration loop-up tables. The dynamic range of an ADC can be roughly defined as the range of input amplitude that is considered significantly greater than the noise. In modern CMOS technologies, the dynamic range of an ADC suffers from reduced signal swing due to scaling.

SNDR and SFDR - The signal-to-noise-and-distortion ratio (SNDR) is an important measure of the ADC performance. It is defined as the ratio of the RMS value of the input signal to the RNS value of the sum of all other spectral components over a defined bandwidth excluding the DC component. Spurious-free dynamic range (SFDR) is defined as the ratio between the RMS values of the input signal to the RMS value of the largest spurious tone in the output spectrum. The expressions for SNDR and SFDR are given in Eqt.2.4 and 2.5.

$$SNDR = 20\log(\frac{V_{in,RMS}}{V_{noise,RMS} + V_{distortion,RMS}}), \tag{2.4}$$

$$SFDR = 20\log(\frac{V_{in,RMS}}{V_{tone,RMS}}), \tag{2.5}$$

FoM - A commonly used definition for figures-of-Merit (FoM) is using a measure of conversion step per unit energy P. In Eqt.2.6

$$FoM = \frac{2^{ENOB} \cdot 2 \cdot BW}{P}, \tag{2.6}$$

where BW represents bandwidth, $ENOB$ is the effective number of bit and is defined in Eqt.2.7 as:

$$ENOB = \frac{SNDR - 1.76}{6.02}, \tag{2.7}$$

Power and Area - Power dissipation and silicon area important measurements of mixed-signal circuit and they are related to cost and budget of the chip. It is always appealing to minimize these two quantities in any circuit design.

2.2 Introduction to Time-Mode ADC

Based on the implemented architecture, the time-mode ADCs can be classified into two categories: open-loop time-mode ADC and closed-loop time-mode ADC. In the following sections, both architectures and related works will be reviewed and the pro's and con's are also commented.

2.2.1 Open-Loop Time-Mode ADC

An open-loop time-mode ADC performs analog-to-digital conversion in the time domain without employing negative feedback. This type of ADCs typically consists of a sample-and-hold (S/H), a multi-stage ring VCO, and a counter, as shown in Fig.2.1 [38, 39, 40, 41, 39, 42, 43]. The frequency of the VCO is controlled by the sampled input voltage. For each sampled input voltage there exists a one-to-one relation between the sampled input

and the frequency of the VCO. The number of the oscillation cycle of the oscillator within each sampling interval of the input provides the digital representation of the sampled input. The resolution of these ADCs is set by the oscillation frequency of the VCO. The higher the frequency of the VCO, the better the resolution, and the higher the power consumption. Since the phases of VCOs are continuous from one sampling period to the next sampling period, the residual phases of the current sampling period are the initial phases of the next sampling period, i.e. $e_i(k) = e_f(k-1)$ where subscripts i and f specify the initial and final phases of the VCO in phase k, respectively, as shown in Fig.2.1. The total phase accumulated in kth sampling period is therefore given by

$$\phi(k) = Gx(k) + e_f(k) - e_i(k), \tag{2.8}$$

where G is the phase gain. Note that the subtraction of $e_i(k)$ in (2.8) is needed as the initial phase is not a part of the phase accumulation in phase k. Let $e(k)$ be the residue phase in phase k, i.e., $e(k) = e_f(k)$, we have $e_i(k) = e_f(k-1) = e(k-1)$. Since the content of the counter increments for every 2π phase accumulation, the output of the counter, denoted by $y(k)$ or $Y(z)$ in z-domain, is obtained from

$$Y(z) = \frac{1}{2\pi}\left[GX(z) + \left(1 - z^{-1}\right)E(z)\right]. \tag{2.9}$$

Eq.(2.9) reveals that the VCO-quantizer possesses a built-in first-order noise-shaping characteristic.

The quantization error of open-loop time-mode ADCs can be reduced by either increasing the frequency of the oscillator, using interpolation [38, 39, 14] or using a phase detector to quantify the residue phase [39]. Among them, VCO quantizers with interpolation are widely favored as it not only utilizes a counter to record the number of the cycles of the VCO, the same as generic VCO-quantizers, it also makes the full use of the output of each delay stage of the VCO to provide the lower N bits of the digital code of the analog input where N is

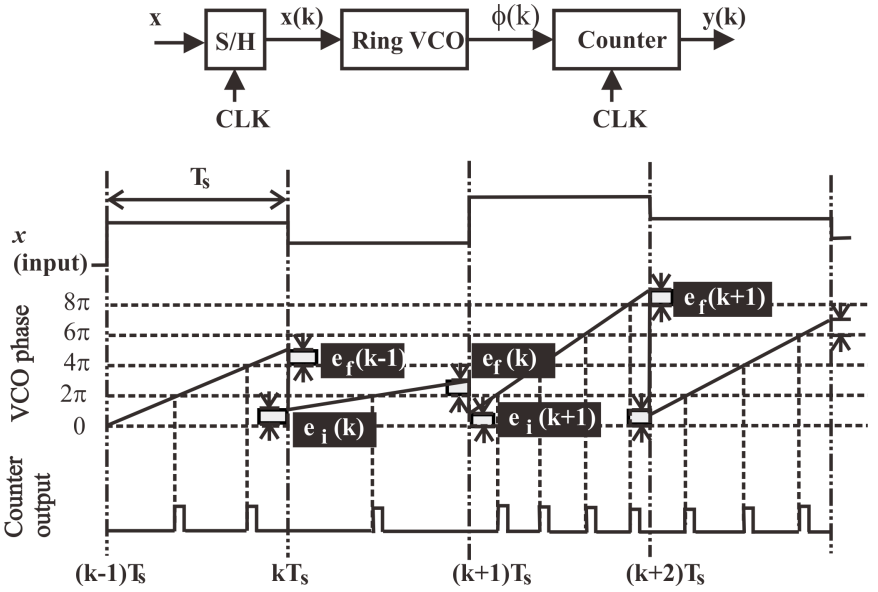


Figure 2.1: VCO quantizer. The residue phase of phase $k-1$, denoted by $e_f(k-1)$, is carried over to phase k as its initial phase, denoted by $e_i(k)$, i.e. $e_i(k) = e_f(k-1)$.

the number of the delay stages of the VCO. The upper digits of the digital code are provided by the counter.

Due to the lack of a negative feedback mechanism, the performance of open-loop VCO-based ADCs is severely affected by the nonlinear V/F characteristics of the VCO [32, 44]. Also, these ADCs only have first-order noise-shaping provided by the voltage-to-phase quantizer, far from the needed high-order noise-shaping in order to yield a larger SNDR. Further, when the transient edge of the output of the VCO is in the proximity of that of the sampling clock, the latency of the counter will prevent the counter from counting correctly [1]. To combat these drawbacks, a number of techniques emerged. The early work of Hovin and Toumazou [34] on frequency delta-sigma modulators was extended by Wismar *et al.* by utilizing the correlation of the quantization errors of the adjacent stages of the VCO and incorporating a differential quantization mechanism, achieving an additional 20 dB improvement of SNDR [35, 45]. The pseudo-differential VCO-based ADC approach proposed in [46, 47, 41] employs two identical VCO-based ADCs driven by differential inputs. The subtraction of the output of the VCOs removes even-order harmonics, resulting in 18 dB improvement in SFDR. The approach proposed in [48, 49, 50] converts the input signal to pulse-width-modulated (PWM) pulses. Since the frequency of the VCO is now only toggled between two constant

voltages, the voltage-to-frequency conversion of the VCO becomes intrinsically linear. SFDR over 70 dB was achieved. The drawback of this approach is the need for a pulse width modulator where both op-amps and comparators are typically needed in its realization, thereby undermining the very reason why time-mode approaches are wanted in the first place. The VCO-based ADC proposed in [51] performs coarse quantization using a multi-phase VCO. The residual phase is quantized with a gated-ring oscillator TDC that provides first-order noise shaping, thereby avoiding the difficulty associated with the poor nonlinear V/F characteristics of the VCO [19]. Open-loop time-mode low-pass ADCs have also been extended to bandpass ADCs by interleaving a set of low-pass VCO-based ADCs [52, 53].

Table 2.1: Performance comparison of open-loop time-mode ADCs.

Ref.	Tech.	Sampling frequency	SNR (dB)	SFDR (dB)	SNDR (dB)	Measurement bandwidth	Power (mW)
[35]	90 nm	3.4 MHz	47.4	—	44.2	20 kHz	0.44
[45]	90 nm	12 MHz	68.9	—	60.3	20 kHz	7.5
[46]	180 nm	100 MHz	58.2	60	56.5	5 MHz	0.56
[32]	65 nm	1 GS/s	—	25.2	19.9	—	1.02
[47]	65 nm	300 MS/s	—	79	65	30 MHz	11.4
[48]	90 nm	640 MHz	—	71	59	8 MHz	4.3
[44]	65 nm	1.2 GS/s	—	30.1	20.4	—	2
[50]	90 nm	560 MHz	68.4	74	67.3	20 MHz	3.1
[14]	130 nm	600 MHz	55	64	52.5	20 MHz	14.3

Table 2.1 compares the performance of recently reported open-loop time-mode ADCs. Counter-based open-loop time-mode ADCs offer a built-in first-order noise-shaping characteristic, the performance of these ADC, however, is severely affected by the large quantization error and the nonlinear V/F characteristics of VCO-quantizers. To reduce the quantization error, interpolation can be utilized. To minimize the effect of the nonlinear V/F characteristics of VCO-quantizers, the approach utilizing the correlation of the quantization error of adjacent delay stages is effective. Pseudo-differential VCO-quantizers are also effective, however, at the cost of doubled silicon and power consumption. Although PWM-based VCO-quantizers intrinsically eliminate the effect of the nonlinear V/F characteristics of VCO-quantizers, their

need for comparators and op-amps make them less attractive. Multi-stage ADCs effectively minimize the effect of the nonlinear V/F characteristics of VCO-quantizers but at the price of increased complexity subsequently silicon and power consumption.

2.2.2 Closed-Loop ADC

Although improving the linearity of the V/F characteristics of VCO-quantizers is critical in improving SNDR, it is rather difficult to achieve this over a large voltage range. It is well understood that negative feedback is an effective means to minimize the effect of nonlinearities when the nonlinear elements are placed in the forward path, the feedback path is highly linear typically achieved by employing passive devices only, and the loop gain is large [54]. In addition to linearity, to improve SNDR, in-band quantization noise must also be minimized. $\Sigma\Delta$ modulators are known for their intrinsic noise-shaping ability allowing in-band noise to be moved to high frequencies outside the signal band such that it can be removed in a post-processing step. The negative feedback of $\Sigma\Delta$ modulators also allows the unwanted harmonic tones caused by the nonlinearities in the forward path to be attenuated by the loop gain. Moreover, if a VCO-quantizer is used, the continuous feedback from the DAC will ensure that the control voltage of the VCO, the difference between the input and the feedback signal, be kept small. As a result, even though the VCO itself might exhibit a poor linearity over a large control voltage range, its linearity over a small control voltage range can be made significantly better [55, 1, 20]. Another intrinsic advantage of ring VCO-quantizers is their inherent multi-bit quantization without using voltage-mode multi-bit quantizers typically realized using voltage comparators whose performance deteriorates with technology scaling. The high oscillation frequency of VCOs benefited directly from technology scaling also permits a large oversampling ratio or equivalently a large input bandwidth for a given oversampling ratio. Lastly, since sampling and quantization take place inside the loop, they are inherently continuous-time (CT) $\Sigma\Delta$ modulators. Both the loop filter and VCO function as anti-aliasing filters, removing the need for an anti-aliasing filter and a sample-and-hold whose performance often dictates that of $\Sigma\Delta$ ADCs.

Another family of $\Sigma\Delta$ modulators employ a pulse width modulation (PWM) generator to convert an analog signal to a pulse and then digitize it using a TDC [56, 57, 58]. Since a loop

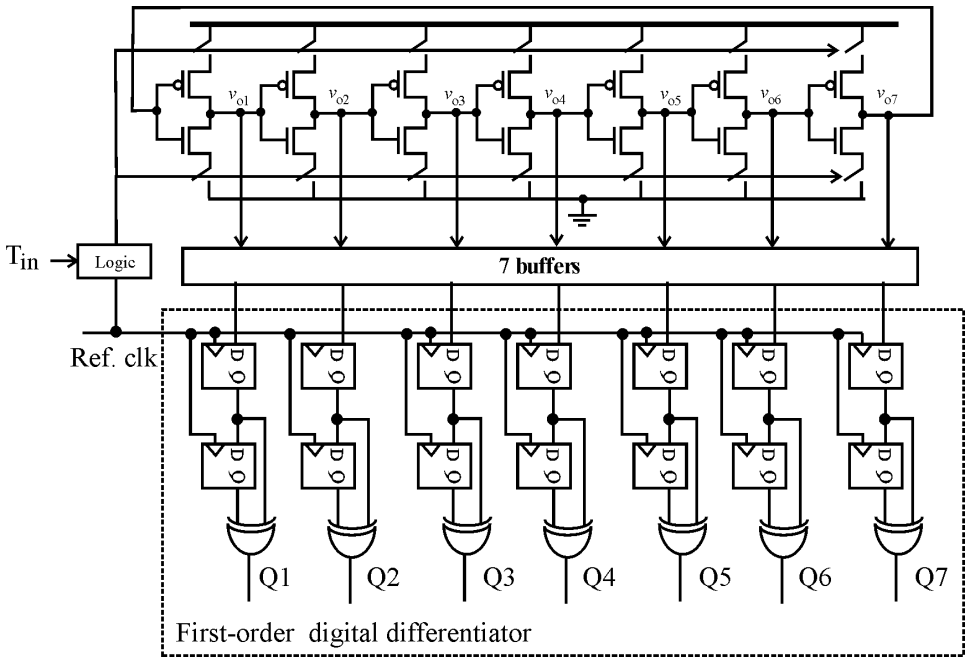


Figure 2.2: ΣΔ ADC proposed by Straayer and Perrott [1].

filter proceeds PWM generator and sampling takes place inside the loop, these modulators are also inherently CT-ΣΔ modulators. As compared with ΣΔ modulators with VCO-based quantizers, the order of noise shaping of TDC-based ΣΔ modulators is lower by one. As a result, their SNR and SNDR are poorer as compared with those of ΣΔ modulators with VCO-based quantizers.

There are other types of VCO-based CT ΣΔ ADCs. One of them is the gated ring oscillator based ADC [48]. In this ADC, the incoming signal to the gates of the ring oscillator has only two discrete levels so it can turn the oscillator on or off. Since the oscillator only works when the input signal is High, the power consumption could be reduced. Gated-ring VCO based ADCs also improve the linearity of the quantizer since only two input levels are available.

The ADC proposed in [59] quantizes the signal using a 4-bit flash ADC and the digitized signal is converted back to analog and subtracted from the next sample. Then the difference is quantized by a VCO-based quantizer. Since the input signal range to the VCO is reduced, the linearity is improved consequently. With another main feedback loop as required by a normal ΔΣ modulator, this ADC offers SNDR of 78.3 dB over 10 MHz bandwidth.

Since VCO-based ADCs are sensitive to nonlinear V/F characteristics of VCO-quantizers, Asl *et al.* showed that this drawback can be effectively eliminated by using a multi-rate VCO-based MASH architecture [60, 61, 51, 62]. The input is first digitized using a conventional $\Sigma\Delta$ modulator with a low oversampling ratio to minimize its power consumption. A second-stage time-mode $\Sigma\Delta$ modulator with a high oversampling ratio is then employed to digitize the quantization error of the first $\Sigma\Delta$ modulator. Since the quantization error of the first $\Sigma\Delta$ modulator is much smaller as compared with the input signal, the effect of the nonlinear V/F characteristic of the VCO-quantizer of the time-mode $\Sigma\Delta$ modulator becomes negligible thereby achieving a high SNDR.

Table 2.2: Performance comparison of closed-loop time-mode ADCs.

Ref.	Tech.	Sampling freq.	BW	SNR (dB)	SNDR (dB)	Power (mW)
[35]	90 nm	3.4 MHz	20 kHz	47.4	44.2	0.44
[55]	0.13μm	950 MHz	20 MHz	60	55	38.4
[**?**]	0.18μm	140 MHz	0.4 MHz	48.9	42.2	0.8
[56]	65 nm	950 MHz	20 MHz	62	60	4.5
[60]	0.13μm	100 MHz/1.2 GHz	4 MHz	77.3	77	13.8
[63]	65 nm	0.5-1.15 GHz	3.9-18 MHz	—	67-78	17
[64]	0.18μm	128 MHz	2 MHz	—	83.9	—
[58]	65 nm	250 MHz	20 MHz	68	60	5.66
[48]	90 nm	76 MHz/640 MHz	8 MHz	61.1	59.1	4.3
[59]	90 nm	600 MHz	10 MHz	83	78.3	16

Table 2.2 compile the key performance data of closed-loop time-mode ADCs. As compared with open-loop time-mode ADCs, closed-loop time-mode ADCs are in general preferred due to their higher order of noise-shaping and the ability to suppress the effect of nonlinear V/F characteristics of VCO-quantizers through a large loop gain and the reduced variation of the control voltage of VCO-quantizers. $\Sigma\Delta$ ADCs with digital differentiators provide an additional order of noise-shaping. MASH-configured $\Sigma\Delta$ ADCs are effective in minimizing the effect of nonlinear V/F characteristics of VCO-quantizers. Design challenges in design of closed-loop time-mode ADCs include the further suppression of the effect of the effect

of nonlinear V/F characteristics of VCO-quantizers to achieve SNDR larger than 80 dB over a large bandwidth, such as 20 MHz for GSM, and low power consumption without deploying analog blocks such as comparators and op-amps whose performance deteriorates with technology scaling.

2.3 Summary on Time-Mode ADC

Similar to conventional ADC design, time-mode ADC with an open-loop architecture suffer from distortion due to non-linear characteristics of circuit components. The open-loop architecture is also sensitive to process variations. In addition, an open-loop time-mode ADC requires high-resolution TDC to improve the overall ADC resolution. In contrast, a time-node ADC with closed-loop architecture can suppress non-linear effect by the loop gain and loop filter. It also relaxes the requirement for a high-resolution TDC by increasing OSR. However the design for loop filters is usually costly.

Chapter 3

Time-Mode ADC Circuit Components

An time-mode ADC is a circuit that performs conversion of an input analog signal (usually a voltage) into a digital number using time-mode approach. This is a achieved by first converting the input analog voltage into a *time difference variable*. Then the time difference variable is being processed by time-mode circuits and finally converted to a digital code. The circuits that perform these conversions include a voltage-to-time converter (VTC), a time difference amplifier or simply time amplifier, a time-to-digital converter (TDC) and digital counter.

VTC - a circuit that performs voltage-to-time difference conversion.

time amplifier - analogous to a voltage-mode amplifeir, a time amplifier provides gain by stretching a width of a time difference variable.

TDC - a circuit component that performs time-to-digital conversion.

digital counter - used for measurement readout and produces a digital code of the measurement result.

3.1 Voltage-to-Time Converter

One of the key building blocks of time-mode circuits is voltage-to-time converters (VTCs). A VTC maps an analog voltage to a time difference variable i.e. a pulse whose width

is proportional to the amplitude of the analog voltage. Key design specifications of VTCs include conversion gain, dynamic range or equivalently linearity, and bandwidth. A large and constant conversion gain over a large input voltage range is highly desirable. The bandwidth of VTC, on the other hand, determines the maximum frequency of the input that time-mode circuits can process. Since MOSFETs are highly nonlinear devices, the design of VTCs with a large conversion gain over a large input range, low power consumption, and a high conversion speed is rather challenging. VTCs are typically implemented using a voltage-controlled delay unit (VCDU) with a reference signal with which the input signal is compared from a timing ring voltage-controlled oscillator (VCO) whose frequency is constant [65]. VCDU can be loosely categorized into direct VCDU and current-starved VCDU [66, 67, 68, 20, 69].

3.1.1 Direct VCDU

The direct VCDU uses a constant current source to charge a capacitor during the sampling period and a current-steering amplifier to sense the difference between the input voltage and the capacitor voltage [29]. Initially the capacitor is fully discharged until the rising edge of a clock signal arrives. At the rising edge of the clock, the capacitor begins to charge by a constant current. The voltage at the capacitor node continues to increase and is compared with the sampled input analog voltage. Once the capacitor voltage exceeds the input analog voltage, the comparator output switches from log 0 to logic 1. The output delay is defined as the time difference between the input event and the comparator output switching instant. In order to implement the direct VCDU, a Wilson current mirror is used to generate the constant charging current. A current-steering amplifier senses the difference between the input voltage and the capacitor voltage permitting the output latch circuit to make a logic decision.

3.1.2 Current-Starved VCDU

The latter, which is more common in recent designs and based on the principle of digitally programmable delay elements detailed in [70, 71], adjusts the delay of a current-starving inverter either using a sampled input [72] or a variable resistor, as shown in Fig.3.1. In Fig.3.1(a), the load capacitor is first charged by the inverter clocked by CLK. The load

capacitor is then discharged via the path controlled by v_{in}. M3 is in the triode and behaves as a voltage-controlled resistor. Since this voltage-controlled resistor exhibits a good linearity only over a small range of drain-source voltage V_{DS3}, the linearity of this VTC is rather poor especially when v_{in} is small. To improve the linearity, Pekau *et al.* utilized both source degeneration and parallel current-starving MOSFETs, as shown in Fig.3.1(b). M4 is in the triode and behaves as a resistor for source degeneration. The current-starving transistor M5 is in the sub-threshold when v_{in} is low and moderate and strong inversion when v_{in} is large. It thus provides an additional discharge path for the load capacitor with its current conduction ability proportional to the voltage of the load capacitor thereby improving both the linearity and conversion gain. Since the input directly controls the discharge of the load capacitor, the frequency of the input will affect the performance of the VTC. This is because the higher the input frequency, the more severe the effect of the capacitances of M4 and the larger the error of the VTC [68]. In Fig.3.1(c), the input voltage is first sampled onto the sampling capacitor C during phase ϕ_1. The charge of the sampling capacitor is then drained by a constant current source I during the discharge phase ϕ_2 until the voltage of the sampling capacitor drops below the threshold of the following comparator [20, 73]. The discharge path is now dis-coupled from the input, removing the drawbacks of Fig.3.1(b). Like any sampling circuit, the effect of charge injection from the sampling switch onto the sampling capacitor must be considered in order to minimize the error caused by charge injection. Also, the sampling frequency is lower-bounded by Nyquist sampling frequency.

3.1.3 Summary on VTC

Direct VCDUs offer the advantages of a high conversion gain and a large dynamic range but suffer from a small bandwidth and high power consumption. Current-starving VCDUs, on the other hand, feature a small conversion gain, a large bandwidth, low power consumption, and a relatively large dynamic range especially when negative feedback and other techniques are used to improve the linearity. Since VTCs serve as the interface between voltage-domain and time-domain, linearity, gain, and speed are perhaps the most important design parameters. Primitive feedback mechanisms are the most effective in improving linearity without sacrificing speed and gain.

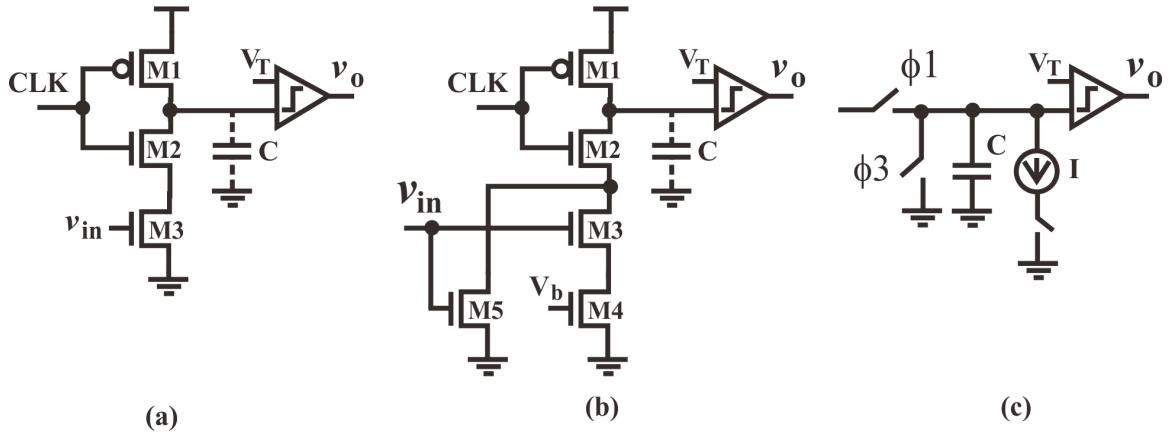


Figure 3.1: Voltage-to-time converters. (a) Current-starved VTC with input-controlled variable resistor M3. (b) Current-starved VTC with improved linearity and conversion gain. (c) Sample-and-hold VTC. The sampling capacitor is charged in phse ϕ_1, drained in phase ϕ_2, and reset in phase ϕ_3 to remove residual charge.

3.2 Time-Mode Amplifier

An ideal time amplifier amplifies the width of a given time difference variable, i.e., pulse width, by a constant gain. They plays a critical role in accurately digitizing time difference variables of a narrow width. In this section, several time amplifier topologies will be discussed.

3.2.1 Regenerative Time Amplifier

Time amplifiers that are based on the metastability of SR-latches were proposed by Abas *et al.* [2] and are shown in Fig.3.2(a). These time amplifiers utilize the re-generative mechanism of the SR-latch to expend narrow pulses [74, 75]. A key advantage of RS-latch time amplifiers is their fast response and ability to amplify a small time difference. The main drawback of these time amplifiers is that the gain of the amplifiers is set by the characteristics of the latch and is strongly subject to the effect of PVT. Another notable drawback of these time amplifiers is a small input range due to the positive feedback mechanism and poor gain nonlinearity. The SR-latch time amplifier proposed by Lee and Abidi and shown in Fig.3.2(b) improves the input range of the generic SR-latch time amplifiers by inserting two delay units with delay τ to generate an unbalanced re-generation mechanism [3]. A drawback of Lee-Abidi time amplifier is that the time mismatch of the buffer delays might be significant

once the input time difference to be amplified is small, introducing a negligible error. This drawback can be removed by using unbalanced active charge pump load proposed in [76].

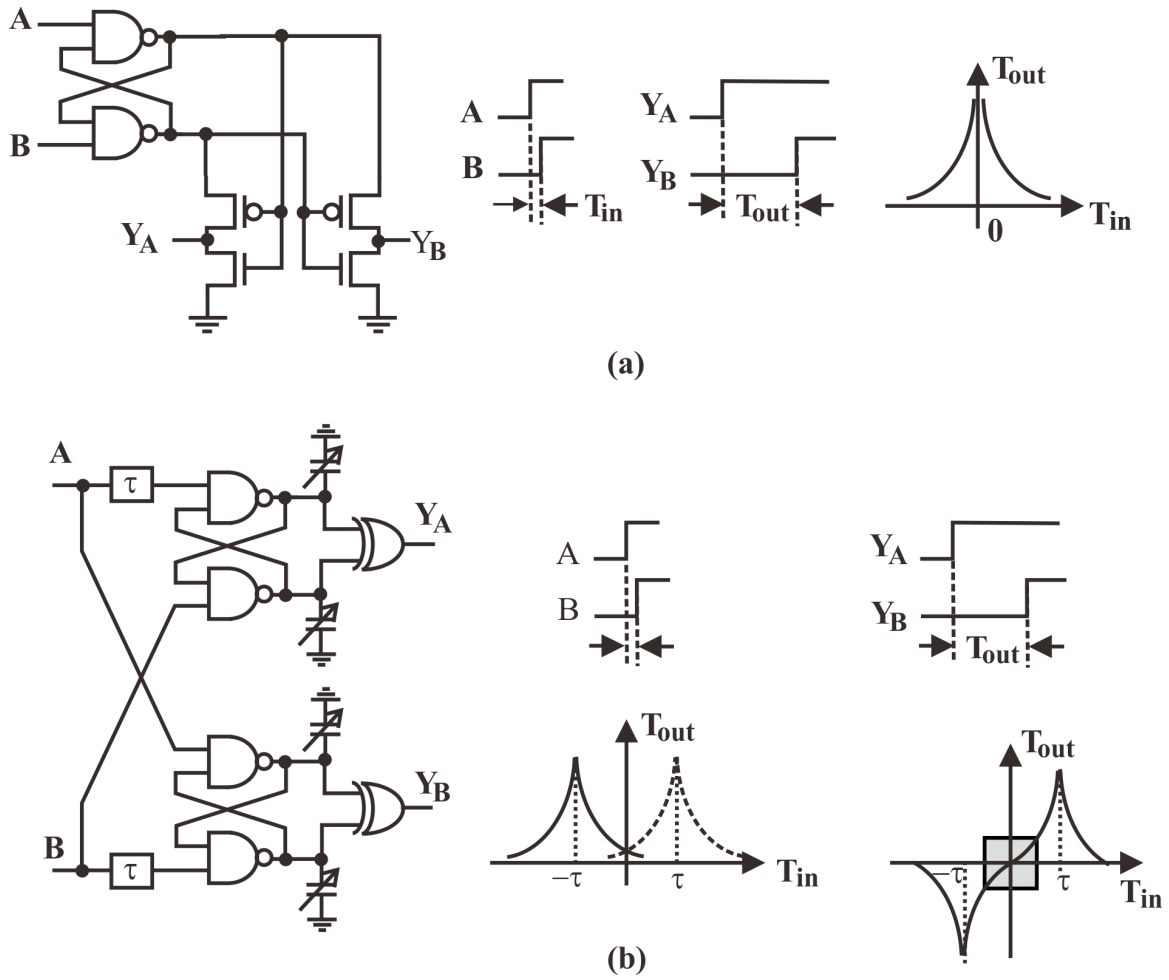


Figure 3.2: (a) RS-latch time amplifier [2]. (b) RS-latch time amplifier with an improved input range [3].

3.2.2 DLL-based Time Amplifier

The DLL-based time amplifier proposed by Rashidzadeh *et al.* and shown in Fig.3.3 uses a closed-loop approach to amply time while minimizing the effect of PVT on the delay [4, 77]. The two periodic inputs of identical period T are fed to two delay lines of the same number of delay stages N but different stage delays. The phase of the waveform at

nodes A and B is aligned using the DDL that adjusts the delay of delay line 1 such that $\phi_{in1} + 2\pi\tau_1/T = \phi_{in2} + 2\pi\tau_2/T$ from which we have $\tau_1 - \tau_2 = 2\pi/T(\tau_2 - \tau_1)$. The output of the time amplifier is given by $T_{out} = (N-1)(\tau_1 - \tau_2)$. Since the DDL must be settled in order to amplify the time difference, the deployment of this type of time amplifiers for high-speed applications is rather difficult. The mismatch of the delay of the delay stages, which is not corrected by the DLL, will also affect the accuracy of the amplifier especially when $\phi_{in1} - \phi_{in2}$ is small.

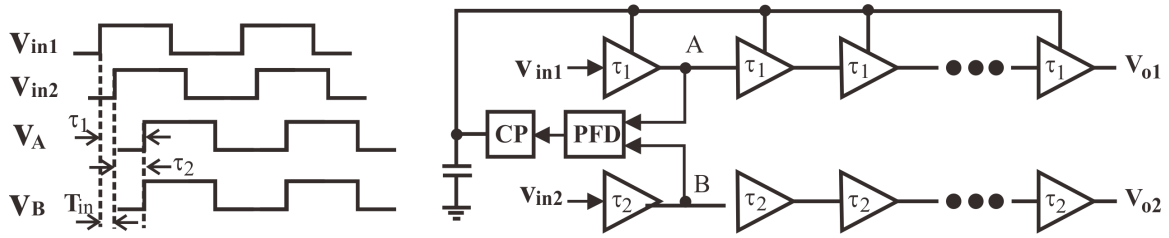


Figure 3.3: DDL-based time amplifier proposed by Rashidzadeh *et al.* [4].

In [5, 78, 79], an elegant closed-loop time amplification scheme shown in Fig. 3.4 was proposed. The two pulses whose time difference is to be amplified propagate in the opposite directions in two separate delay lines having the same number of delay cells. The delay of the delay cells can be toggled between τ_1 and τ_2 by Boolean control signal X, specifically, $\tau = \tau_1$ if $X = 0$ and $\tau = \tau_2$ if $X = 1$ with $\tau_2 = n\tau_1$ where n is an integer. The ratio of τ_1 to τ_2 is controlled by a DDL to minimize the effect of PVT. Before v_{in1} and v_{in2} propagating in the two delay lines meet, the delay of the delay cells ahead of v_{in1} and v_{in2} is τ_1. When v_{in1} and v_{in2} collide, the delay of the delay cell ahead v_{in1} and v_{in2} become τ_2 as the toggling signal X of these delay cells has already been set to logic-1. It can be shown that $\tau_{o1} = M\tau_1 + N\tau_2$ and $\tau_{o2} = N\tau_1 + M\tau_2$. As a result, $T_{out} = \tau_{o1} - \tau_{o2} = (M-N)\tau_2 + (M-N)\tau_1$. The location where v_{in1} and v_{in2} meet is clearly determined by T_{in} and τ_1, specifically, $T_{in} = (M-N)\tau_1$. The amplifier completes time amplification when v_{o1} and v_{o2} reach the end of the delay lines. The minimum time interval between two time amplifications is therefore given by $M\tau_1 + N\tau_2 + T_{in}$

or $N\tau_1 + M\tau_2$. Also, the time gain is directly proportional to $\tau_2 - \tau_1$ and the length of the delay lines.

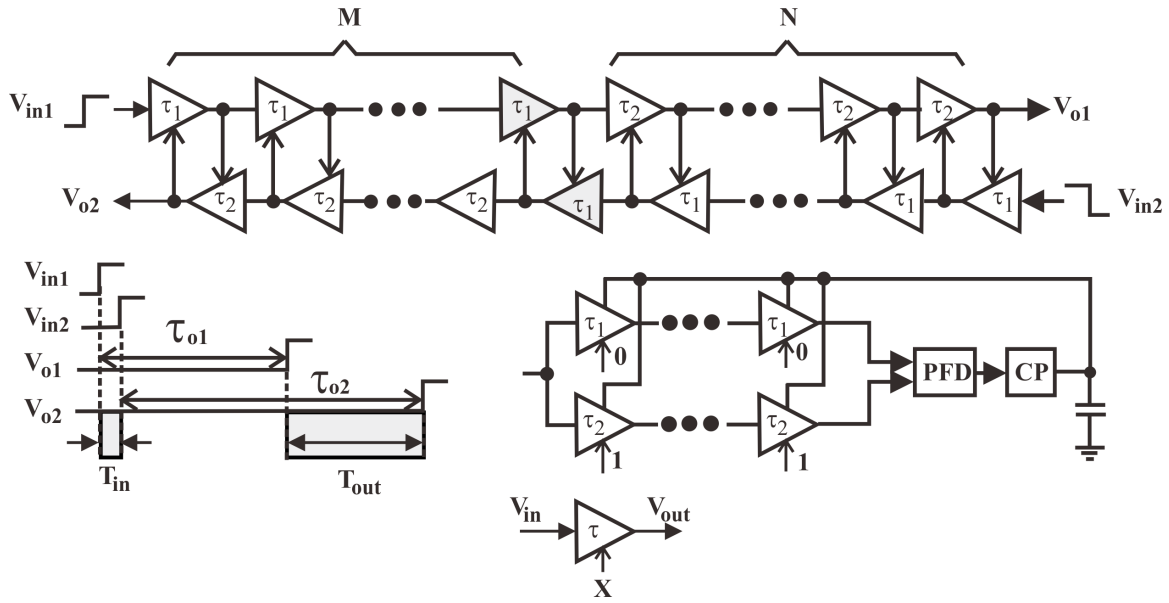


Figure 3.4: Time amplifier proposed by Nakura *et al.* [5]. Top : Configuration. Bottom left : Wave forms. Bottom right : DDL to preciously control the ratio of τ_2 to τ_1. The number of the delay cells in the two paths of the ratio control DDL is set such that the delay of the two delay lines is the same.

3.2.3 Charge-Pump Time Amplifier

Time amplification can also be accomplished by first charging a pair of capacitors with two digital signals whose time difference is to be measured and then sensing the difference of the voltage of the capacitors [80, 81]. The need for constant current sources and voltage comparators of this approach, however, undermines the very reason why time-mode approaches are wanted in the first place. The time amplifier proposed by Kim *et al.* in [82] utilizes a primitive logic operation to achieve a 3.75 ps resolution in 65 nm CMOS. Since the implementation is completely open-loop, its performance is subject to the effect of PVT.

3.2.4 Dual-Slope Time Amplifier

In [6], a time amplifier of gain of 2 was proposed, as shown in Fig.3.5. The capacitors at nodes 1 and 2 are pre-charged prior to the arrival of inputs A and B. When input A arrives, C_1 is discharged by two pull-down paths provided by M1 and M2 while no change in the right half circuit before input B arrives. When input B arrives, since M4 turns off due to the drop of V_1, only one pull-down path provided by M3 exists for input B. V_2 thus drops at approximately half the rate of that of V_1. A large time gain can be obtained by cascading more 2x-time amplifiers, of course, at the expense of power and silicon consumption. It becomes clearly that the gain of this time amplifier is not preciously defined.

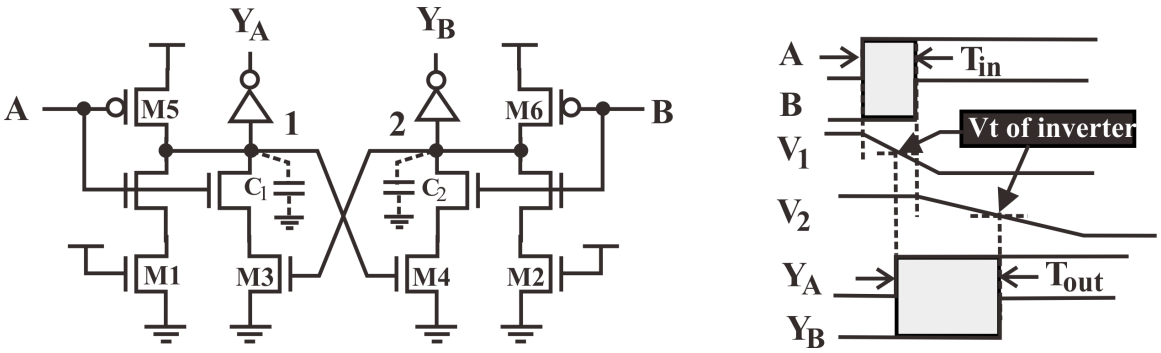


Figure 3.5: 2x-time amplifier proposed by Lee *et al.* [6].

Table 3.1 compares the performance of recently reported time amplifiers. It is seen that RS-latch time amplifiers enjoy a superior time resolution and low power consumption but suffer from a small input range. DDL-based time amplifiers offer a large input range and a large gain but but suffer from a speed penalty. Charge-pump time amplifiers provide a reasonable resolution and a large input range. Their need for comparators and constant current sources make them particularly less attractive for low-power high-speed applications. Dual-slope time amplifiers features simple configurations and low power consumption, however, with a low gain unless the ratio of the slopes is made large.

Table 3.1: Performance comparison of time amplifiers.

Ref.	Tech.	Gain	Resolution	Input range	Power
[2]	0.6 μm	5	10 ps	$\pm$30 ps	
[74]	0.18 μm	120	—	$\pm$30 ps	—
[83]	0.18 μm	4	—	$\pm$15 ps	—
[3]	90 nm	0	1.25 ps	—	0.3 mW
[4]	0.18 μm	10	50 ps	50-360 ps	3.6 mW
[5]	65 nm	4.78	5 ps	$\pm$300 ps	0.314 mW
[78]	0.18 μm	16.88	—	$\pm$250 ps	–
[77]	0.13 μm	10	2 ps	90 ps	0.634 mW
[80]	65 nm	5	4 ps	$\pm$400 ps	0.74 mW
[81]	0.13 μm	10-120	10 ps	10 ps-2 ns	—
[76]	90 nm	20	0	70 ps	—
[82]	65 nm	8	3.75 ps	10 ps-2 ns	—

3.3 Time-to-Digital Converter

Once an input voltage is converted to a time difference variable, it needs to be digitized for post digital signal processing. This is accomplished by a time-to-digital converter (TDC). Although the deployment of TDCs in particles and high-energy physics for life-time and time-of-flight measurement in nuclear science dates back to 1970s [84, 11], the broad spectrum of emerging applications of TDCs in digital storage oscillators [85, 86], laser range finders [87], digital frequency synthesizers [88], and analog-to-digital converters [9], to name a few, took place only recently. The performance of TDCs is typically quantified by a number of parameters among them resolution, input range, linearity quantified by differential nonlinearity (DNL) and integral nonlinearity (INL), and power consumption are perhaps the most important. The resolution of a TDC is the minimum time width that the TDC can digitize. Input range is the time range that TDCs can perform time-to-digital conversion while meeting linearity requirements. DNL quantifies the maximum difference between the step width of an actual TDC and that of an ideal TDC while INL quantifies the accumulated difference between the actual and ideal steps. This section investigates both the principle and design techniques of TDCs.

3.3.1 Direct-Counter TDC

A direct-counter TDC is basically a counter that quantizes a time-difference variable by counting the number of the cycles of a reference clock whose period T_c is much smaller as compared with the time-difference T_{in} to be measured, as shown in Fig.3.6(a). These TDCs have a dynamic range upper-bounded by the size of the counter. In addition, they enjoys a superior linearity as the linearity is only affected by the stability of the frequency of the reference clock. The quantization errors Δ_1 and Δ_2 are due to the misalignment of the rising edges of START, STOP, and that of the reference clock. Clearly, $0 \leq \Delta_1, \Delta_2 \leq T_c$. The resolution of direct-counter TDCs is set by the period of the reference clock. The higher the frequency of the reference clock, the better the resolution, and the smaller the quantization error. This, however, is at the cost of high power consumption and a deteriorating crosstalk. Direct-counter TDCs are therefore preferred only if T_{in} is large simply due to their ease of implementation.

To minimize the quantization error of direct-counter TDCs, Chen *et al.* showed that the quantization errors Δ_1 and Δ_2 can be first stretched much larger than T_c and then digitized by the reference clock, yielding a significantly reduced quantization error, as shown in Fig.3.6(b) [86]. Pulses T_1 and T_2 are generated at the rising edge of START and STOP, respectively with their falling edge aligned with the next rising edge of the reference clock. Pulse stretching starts with the assertion of a reset (RST) command that brings the voltage of C_1 and C_2 to V_{DD}. The discharge of C_1 and C_2 is controlled by J_1 and J_2, respectively. Since $J_1 = NJ_2$ and $C_2 = MC_1$ with $M, N > 1$, the discharge of C_1 is much faster than that of C_2. The discharge process is initiated by T_1. v_o is set to HIGH and will remain HIGH until $v_{c2} = v_{c1}$. Since v_{c2} drops much slower, it will take k cycles of CLK before $v_{c1} = v_{c2}$ occurs. The number of the cycles needed is recorded by the counter incremented by CLK. The content of the counter therefore provides the digital representation of the quantization errors Δ_1. The same process is followed when quantizing Δ_2. To determined k, from $\Delta v_{c1} = \Delta v_{c2}$ where Δv_{c1} and Δv_{c2} are the voltage drop of C_1 and C_2 from V_{DD}, respectively and noting $\Delta v_{c1} = (J_1/C_1)T_1$ and $\Delta v_{c2} = (J_2/C_2)T_c k$, we arrive at $k = MN(T_1/T_c)$ or equivalent $\hat{T}_1 = kT_c = MNT_1$. $\hat{T}_1$ is the stretched version of T_1. It is evident that T_1 is stretched by MN times.

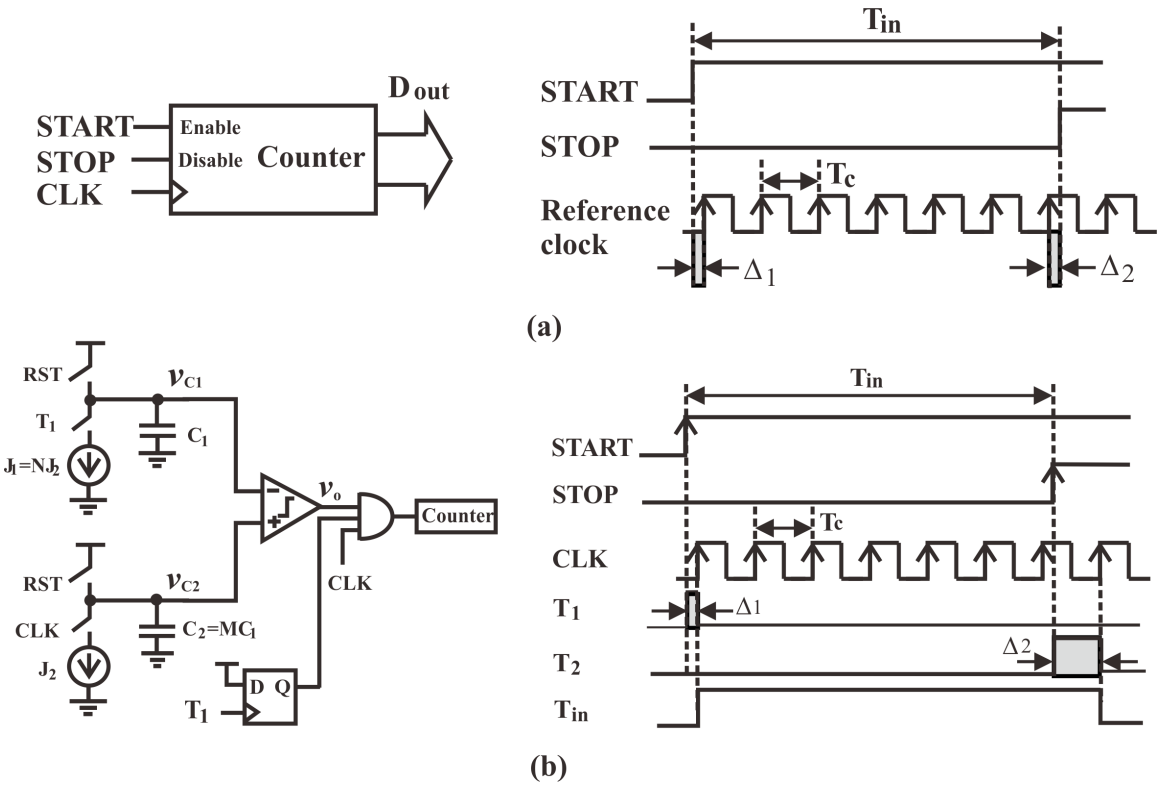


Figure 3.6: (a) Direct-counter TDC. The counter starts at START=1 and stops at STOP=1. Δ_1 and Δ_2 are quantization errors with $\Delta_1, \Delta_2 \leq T_c$. The input in the time domain is represented by : $T_{in} = nT_c + \Delta_1 + \Delta_2$. (b) Direct-counter TDC with pulse stretching.

The dual-slope of the preceding pulse stretching approach makes it less sensitive to the effect of PVT. This approach, however, suffers from a speed penalty due to the slow discharge of C_2. The need for a voltage comparator and two constant current sources also makes it less attractive in digital-oriented designs.

3.3.2 Delay-Line-based TDC

To reduce quantization error without sacrificing speed or deploying analog circuitry, the delay-line TDC shown in Fig.3.7 (without the counter) with a START signal propagating through the delay line and a STOP signal disabling D Flip-Flops (DFFs) can be used. The dynamic range of delay-line TDCs is from $\underbrace{00\cdots0}_{N}$ to $\underbrace{11\cdots1}_{N}$, thermometer coded, where N is the number of the delay stages. Clearly, the upper bound of the dynamic range of delay-line TDCs is set by the length of the delay line while the lower bound is set by the delay of the delay stages. Since the resolution is limited by the delay of the delay cells, the

performance of delay-line TDCs scales well with technology [7]. The linearity of delay-line TDCs is determined by the mismatch of the delay of the delay stages and worsens when the number of delay stages is large, simply due to the accumulation of delay mismatch-induced error. To minimize the effect of PVT on the delay of delay cells and error accumulation along the delay line, a delay-locked loop (DDL) is typically employed, as shown in Fig.3.7 [13]. If the delay of each deay stage is τ and the number of delay stages is N, then in the lock state, START and X_N are phase-aligned, i.e. X_N lags START by T_c where T_c is the period of START. Since START and X_N are phase-aligned, we have $\tau = T_c/N$ where τ is the delay of the delay stages. Clearly τ is only affected by T_c and N, and is not subject to the effect of PVT. Note that since the DLL locks to the input signal in this configuration, delay-line TDCs do not need a reference clock. It should also be noted that TDCs with DLLs locked to a reference rather than the input was also proposed [89]. In this approach, two identical delay lines, one locked to the reference and the other processes the input, are needed. The key advantage of this approach is that the delay of the dual delay lines is only determined by the reference clock and is independent of the input.

3.3.3 Direct-Counter TDC with Gated-Delay Interpolation

The quantization error of direct-counter TDCs presented earlier can be lowered to that of delay-line TDCs by digitizing the time difference between the rising edge of START/STOP and the edge of the reference clock using a delay-line TDC while retaining the upper bound of the dynamic range of that of direct-counter TDCs, as shown in Fig.3.7 (with the counter). We term these TDCs direct-counter TDCs with gate-delay interpolation [7, 8, 9, 10, 11]. The dynamic range of direct-counter TDCs with gate-delay interpolation is upper-bounded by the size of the counter and lower-bounded by the delay of the delay cells. The linearity of direct-counter TDCs with gate-delay interpolation is set by the stability of the reference clock and the delay mismatch of the delay cells.

3.3.4 Delay-Line TDC with Sub-Gate Delay Interpolation

To further improve the time resolution of TDCs to sub-gate-delay, interpolation between the transition edges of adjacent delay stages can be utilized to generate sub-gate delay and we

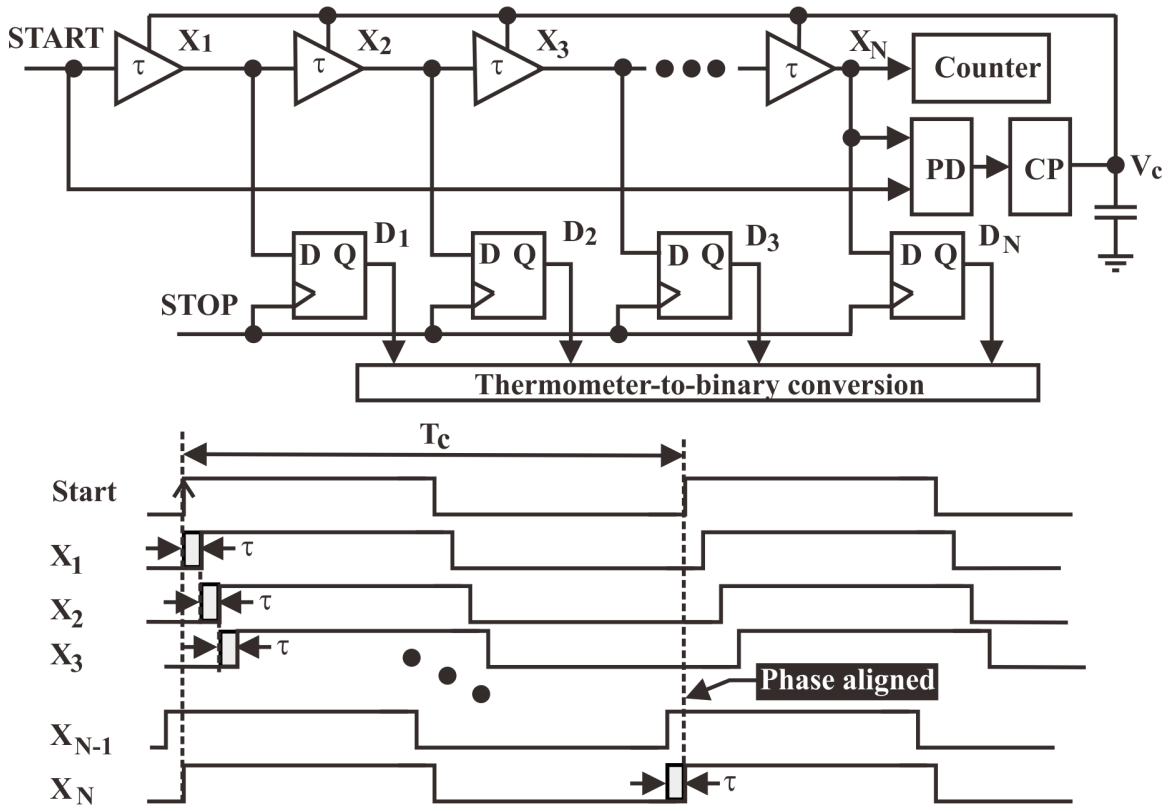


Figure 3.7: Delay-line TDCs (w/o counter) [7]. The delay of kth delay cell is given by $\tau_k = \tau + \Delta\tau_k$ where τ is nominal value of the delay and $\Delta\tau_k$ is the random deviation of the delay from τ. When the counter is added, it becomes a direct-counter TDC with gate-delay interpolation [7, 8, 9, 10, 11].

term them TDCs with sub-gate-delay interpolation. The interpolation approach proposed in [12] and shown in Fig.3.8(a) uses the weighted sum of the differential output voltage of adjacent delay stages v_1 and v_2 to interpolate the voltages of the adjacent delay stages. If $w = 1$ i.e. M1=ON and M2=OFF, v_o is determined by v_1 only. Similarly, when $w = 0$, M1=OFF and M2=ON, v_o is determined by v_2 only. However, when both M1 and M2 are ON and their currents are determined by w, v_o is a function of both v_1 and v_2. Interpolation can also be implemented using passive networks such as the resistor network shown in Fig.3.8(b) with the drawback of non-negligible static power consumption. This is because the resistance of the resistors must be kept small in order to lower the time constant subsequently meet speed requirements [13]. Another technique to achieve the resolution of sub-gate delay is to use an arrays of delay-locked loops [90]. The need for multiple DLLs, however, makes this approach less attractive. The phase interpolation method proposed in [14] and shown in

Fig.3.8(c) uses a hierarchical tree structure to increase time resolution. To ensure that the added interpolating points 2 and 3 are not overlapped in time, the rise and fall times of the inputs v_{1+} and v_{1-} are made unbalanced purposely.

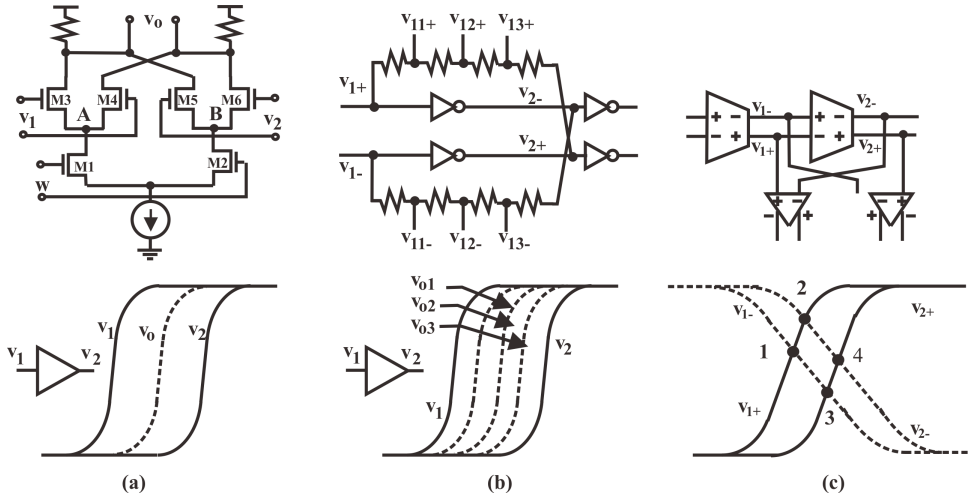


Figure 3.8: (a) Interpolation using the weighted sum of the voltage of the adjacent delay stages [12]. (b) Interpolation using resistor networks [13]. (c) Interpolation using hierarchical tree [14].

3.3.5 Vernier Delay-Line TDC

High-resolution TDCs can be obtained using Vernier delay lines where START and STOP signals whose time difference is to be measured propagate in two separate delay lines of the same length but different delays, as shown in Fig.3.9 [91, 92]. The delay line in which START propagates thereafter called START-line has a slightly longer delay as compared with that of STOP-line, i.e. $\tau_1 > \tau_2$. Since the delay of START-line is larger, STOP signal propagating in STOP-line will catch START signal in START-line if the lines are long enough and the time difference between START and STOP signals is not overly large. When this occurs, time-to-digital conversion is completed and the resultant digital code is given at the output of the DFFs. The time at which a catch-up occurs is determined from $T_{catch} = N\tau_1 = N\tau_2 + T_{in}$ where N is the number of the delay stages of the Vernier delay lines and T_{in} is the time difference between START and STOP. For a given T_{in}, the number

of the delay stages is determined from $N = \Delta T/(\tau_1 - \tau_2)$. Clearly, the dynamic range of Vernier delay line TDCs is upper-bounded by the length of the lines and lower-bounded by $\tau_1 - \tau_2$. Although theoretically as long as $\tau_1 - \tau_2$ is sufficiently small and Vernier delay lines are sufficiently long, the resolution of Vernier delay line TDCs can be made arbitrarily small. In reality, it is limited by the finite length of Vernier delay lines and the mismatch of the delay of the delay cells.

Vernier delay line TDCs suffer from a large hardware cost due to the need for two long delay lines and a finite dynamic range upper-bounded by the length of the delay lines, especially when $\tau_1 - \tau_2$ is small. The performance of Vernier delay line TDCs can be improved using two-level Vernier lines with the coarse Vernier lines having a large delay difference $\Delta\tau_c$ and the fine Vernier lines having a small delay difference $\Delta\tau_f$ where the subscripts c and f signify "coarse" and "fine", respectively [93]. Although the dynamic range is improved, the complexity of the TDC is also significantly increased.

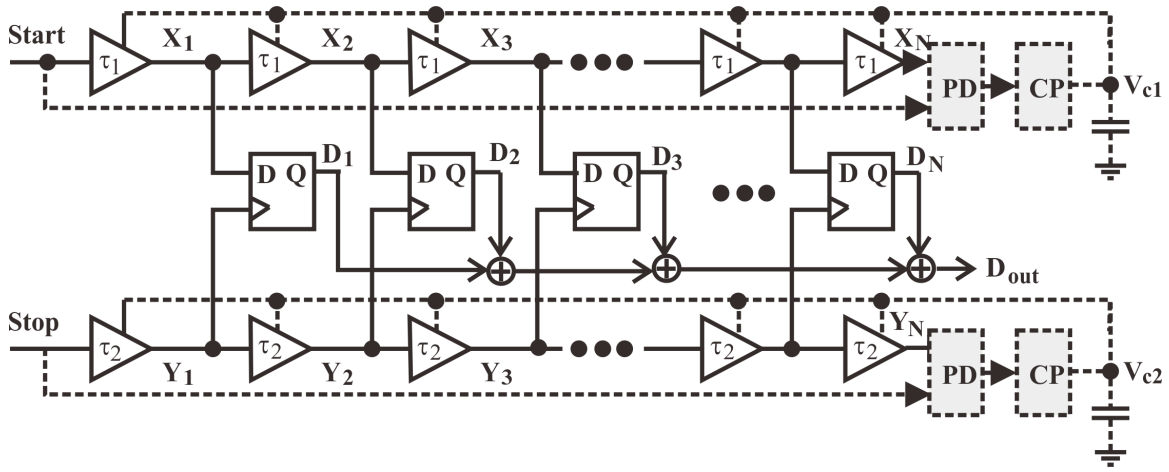


Figure 3.9: Vernier delay line TDCs.

To minimize the effect of PVT on Vernier delay line TDCs, DLL-stabilized Vernier delay line TDCs shown in Fig.3.9 (with dotted sections) can be utilized [92]. The transition edge of X_N is phase-aligned with START such that $N\tau_1 = T_1$ where T_1 is the period of START from which we have $\tau_1 = T_1/N$. Clearly this configuration does nothing to minimize the

effect of PVT on STOP-line. The minimize the effect of PVT on the delay of STOP-line, another DLL can be utilized, as shown in Fig.3.9(b).

For a given $\tau_1 - \tau_2$, the dynamic range of Vernier delay line TDCs is set by the length of the delay lines. To increase the dynamic range without employing overlong delay line TDCs, cyclic Vernier delay lines were proposed by Xing *et al.* and is shown in Fig.3.10 [89]. Two delay lines having N_1 and N_2 delay stages are employed with their delay τ_1 and τ_2 set by the two DLLs : $\tau_1 = 1/(M_1 N_1 f_o)$ and $\tau_2 = 1/(M_2 N_2 f_o)$ where f_o is the frequency of the reference clock and M_1 and N_1 are integers. START and STOP signals are fed to two cyclic loops consisting of a delay stage and a NAND2. Note that delay of the loop for START is τ_1 and that for STOP is τ_2. The loops are enabled on the arrival of START and STOP. Since $\tau_2 < \tau_1$, Y_f will catch up X_f. Once this occurs, $Q_1 = 0$. In the following phase of STOP, $Q_2 = 0$. $\overline{Q}_3 = 1$, disabling the coarse and fine counters.

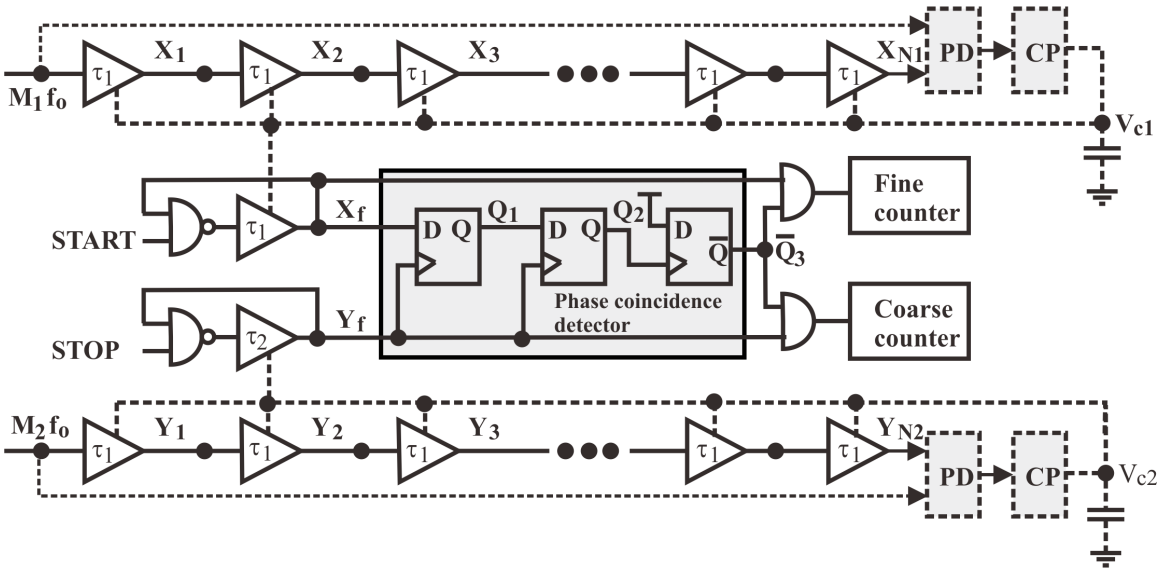


Figure 3.10: Cyclic Vernier delay line TDCs.

3.3.6 Pulse-Shrinking TDC

Pulse-shrinking TDCs uses skewed delay stages, i.e., delay stages with a larger propagation delay, in a delay line to reduce the width of the propagating pulse [94]. To increase the

amount of pulse width shrink without employing a large number of delay stages, the cyclic configuration shown in Fig.3.11 is often used. Although the large load of the skewed stage increases the propagation delay of the preceding stage, the large driving current of the skewed stage reduces the propagation delay of the following delay stage, resulting in an overall reduction of the propagation delay of the loop. In this configuration, the pulse propagates in a ring consisting of regular delay stages of delay τ_1 and a skewed delay stage of delay τ_2 until the width of the pulse diminishes. A counter is used at the end of the ring to record the number of the round trips the pulse makes. The content of the counter when the pulse diminishes in the ring gives the digital representation of the initial pulse width. Pulse-shrinking TDCs enjoy a large dynamic range as the upper bound is only set by the size of the counter. A key characteristic of cyclic pulse-shrinking TDCs is the absence of the effect of nonlinearities as the input pulse propagates through the entire delay line once per cycle. As a result, the amount of the cycle-to-cycle shrinkage of pulse width remains unchanged. One drawback of cyclic pulse-shrinking TDCs is the latency needed for the pulse to diminish completely before another input pulse can be applied [13]. Another drawback of pulse-shrinking TDCs is the effect of temperature variation on the delay of delay cells, which could be as high as $\pm 25\%$ over $0 \sim 100$ C [86]. Note that in delay-line TDCs, the effect of PVT on the delay of delay cells is minimized effectively using either a self-locked DLL that is locked to the input [92] or a reference-locked DLL that is locked to a reference clock [89]. The closed-loop configuration and cyclic operation of pulse-shrinking TDCs makes the compensation for PVT effect rather difficult. No PVT-compensated pulse-shrinking TDCs are available at the writing of this review. It should also be noted that pulse-shrinking TDCs is effective only if pulse width is sufficiently large as compared with the amount of the shrink of the pulse width per around trip. The lower bound of the number of the delay stages of the ring is set by the speed of the counter, specifically, the counter must have a sufficient time to settle each time the pulse completes a round trip.

3.3.7 Gated-Ring-Oscillator-based TDC

TDCs based on gated ring oscillators shown in Fig.3.12 digitizes the input voltage using a multi-stage ring oscillator. The input is the control voltage of the oscillator and the oscillation

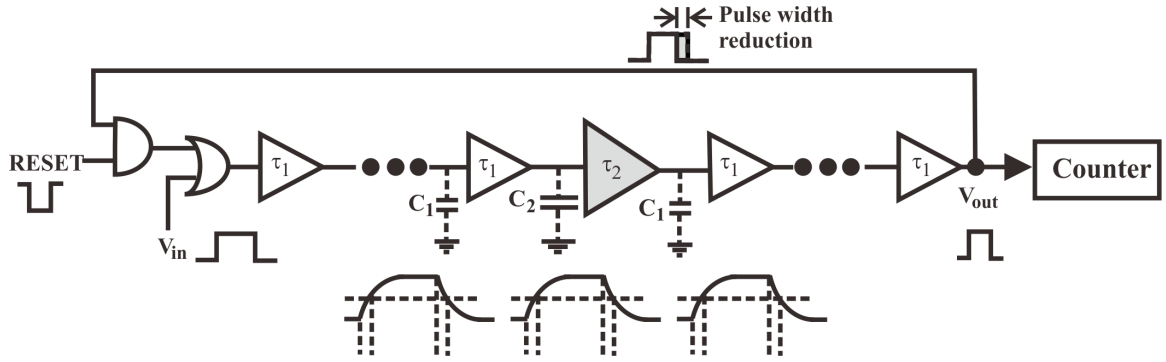


Figure 3.11: Pulse shrinking TDC.

is controlled by Boolean signal ENABLE. Upon the assertion of ENABLE signal, the outputs of the delay stages of the VCO are sampled and the register logic records the total number of the transition of the stages. Since the total number of the state transition of the VCO when ENABLE=1 is directly proportional to the frequency of the VCO subsequently the input voltage, an one-to-one relation between the input voltage and the total number of the state transition of the VCO exists. When ENABLE is inactivated, the output voltages or equivalently the phases of the VCO are frozen, allowing residual phases in phase $k-1$ to be transferred to the next sampling phase k, i.e., they become the initial phases of sampling phase k. This residual phase transfer characteristic gives rise to the first-order shaping of quantization noise, an intrinsic characteristic of gated ring oscillator TDCs. Similar to quantization noise shaping, gated ring oscillator TDCs also provide first-order shaping on mismatch-induced delays as they are sampled and held from one sample interval to the next. Moreover, the cyclic operation of these TDCs provides the built-in scrambling of quantization noise, similar to dithering in $\Sigma\Delta$ modulators, further improving the effectiveness of first-order noise-shaping.

Table 3.2 compares the performance of recently reported time-to-digital converters. Direct-counter TDCs enjoy a simple configuration and a large dynamic range but suffer from large quantization noise and a low conversion speed. The conversion speed of delay-line TDCs scales well with technology. These TDCs, however, have a small dynamic range. Direct-counter TDCs with gate-delay interpolation possess the intrinsic advantages of both direct-counter TDCs and delay-line TDCs. Their performance can be further improved using sub-

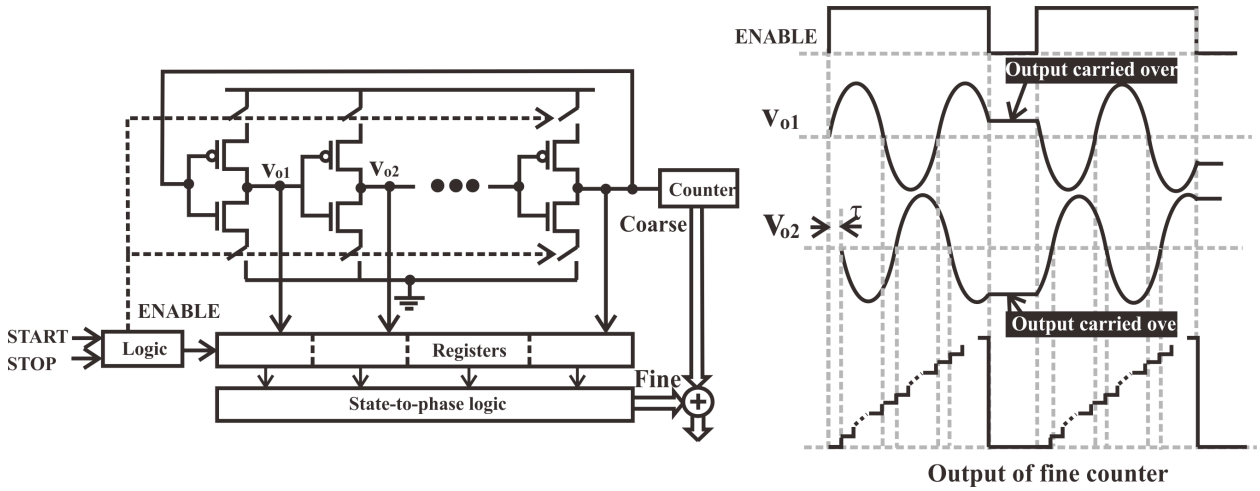


Figure 3.12: Gated ring oscillator TDC.

Table 3.2: Performance comparison of time-to-digital converters.

Ref.	Tech.	Resolution	DNL (LSB)	INL (LSB)	Range	Ref. clock	Power
[92]	0.7 μm	5 ps	$\pm$1	$\pm$1	3.84 ns	130 MHz	—
[10]	0.25 μm	24.5 ps	$\pm$0.2	$\pm$0.3	102.4μs	320 MHz	–
[95]	0.35 μm	65 ps	$\pm$0.03	$\pm$0.04	—	400 MHz	90 mW
[96]	0.35 μm	13.5 ps	$\pm$ 6 ps	12 ns	145 MHz		55 mW
[7]	90 nm	20 ps	$\pm$0.7	$\pm$0.7	0.96μs	1.6-2 GHz	6.89 mW
[86])	0.35μm	50 ps	—	$\pm$1.1	250 ns	80 MHz	0.75 mW
[97]	0.35μm	37.5 ps	$\pm$0.25	$\pm$0.35	50 ns		
[93]	0.18μm	29.6 ps	-0.33$\sim$0.69	-0.47$\sim$1.08	75 ns	200 MHz	150 mW
[98]	0.13μm	24.5 ps	$\pm$0.001	$\pm$0.52	–	26 MHz	1.09 mW
[99]	0.13μm	6.5 ps	—	—	4.5 ns	–	1 mW
[13]	90 nm	4.7 ps	$\pm$1.2	$\pm$0.6	131.6 ps	—	—
[100]	0.35μm	1.2 ps	—	—	327μs	100 MHz	33 mW
[19])	0.13μm	1 ps	—	—	—	100 MHz	31.5 mW
[89]	0.18μm	14.6 ps	$\pm$1	$\pm$1.5	50 ns	—	6.4 mW
[101]	0.25μm	200 ps	$\pm$4	$\pm$4	220 ns	—	30 mW
[102]	0.18μm	10 ps	—	—	162 ns	317 MHz	9.34 mW

gate-delay interpolation. Vernier delay-line TDCs offer an improved resolution as compared with delay-line TDCs at the price of doubled silicon and power consumption. To increase dynamic range, cyclic Vernier delay-line TDCs are favored. TDCs using gated ring oscillator

offer comparable conversion speed, resolution, and dynamic range as compared with delay-line TDCs but with built-in first-order noise-shaping of both quantization noise and delay mismatch.

3.4 Summary

This chapter provides a survey on the building blocks for a time-mode ADC. Different approaches to implementing such components are also presented. From the comparison made between those implementation approaches, it can be concluded that the current-starved VTC, regenerative time difference amplifier, GRO-based TDC will be fit for an all-digitally implemented time-mode ADC due to their small areas, low power consumptions and simple implementations. Therefore they are deployed in the proposed designs.

Chapter 4

Proposed Works

4.1 Prior Works

In this section, some significant works on time-mode $\Delta\Sigma$ ADC are reviewed. Based on different architectures, those works can be classified into open-loop time-mode ADC and closed-loop time-mode ADC, which is also known as $\Delta\Sigma$ ADC. A single-bit all-digital $\Delta\Sigma$ ADC design is being analysed due to its all-digitally implemented architecture.

4.1.1 Single-Bit Closed-Loop Time-Mode $\Delta\Sigma$ ADC

A single-bit time-mode $\Delta\Sigma$ ADC is proposed in [103] as shown in Fig.4.1(a) employs a voltage-to-time integrator to perform both voltage-to-time conversion and integration simultaneously. If we assume that the voltage-controlled delay units (VCDUs) are identical and linear, then $\tau_{in} = K_d v_{in}$ and $\tau_f = K_d v_f$ follow where K_d is the gain of the VCDUs, τ_{in} and τ_f are the delay of the input VCDU and feedback VCDU, respectively. The reference clock comes from a reference oscillator oscillating at a constant frequency. The DFF serves as a single-bit phase quantizer. The single-bit quantization ensures that the quantizer is perfectly linear. The block diagram of the modulator is shown in Fig.4.1(b) with Q representing quantization noise and N_{VTC} representing the nonlinearity of the voltage-to-time integrator. It can be shown that utilizing $1 - z^{-1} \ll 1$, we have

$$D_{out} \approx V_{in}(z) + K_{VTC} + \frac{(1 - z^{-1})Q(z)}{K_{VTC}}. \tag{4.1}$$

Eq.(4.1) shows that the modulator provides first-order noise-shaping on quantization noise. Both the input and the nonlinearity of the voltage-to-time integrator appear at the output with no attenuation. The former is desirable while the latter is not. Since K_{VTC} is typically low, the absence of the loop filter eliminates the ability of the modulator to suppress quantization noise, aside from first-order noise-shaping. Since single-bit quantization results in a high level of quantization noise, the inability of the modulator to suppress quantization noise limits its SNDR.

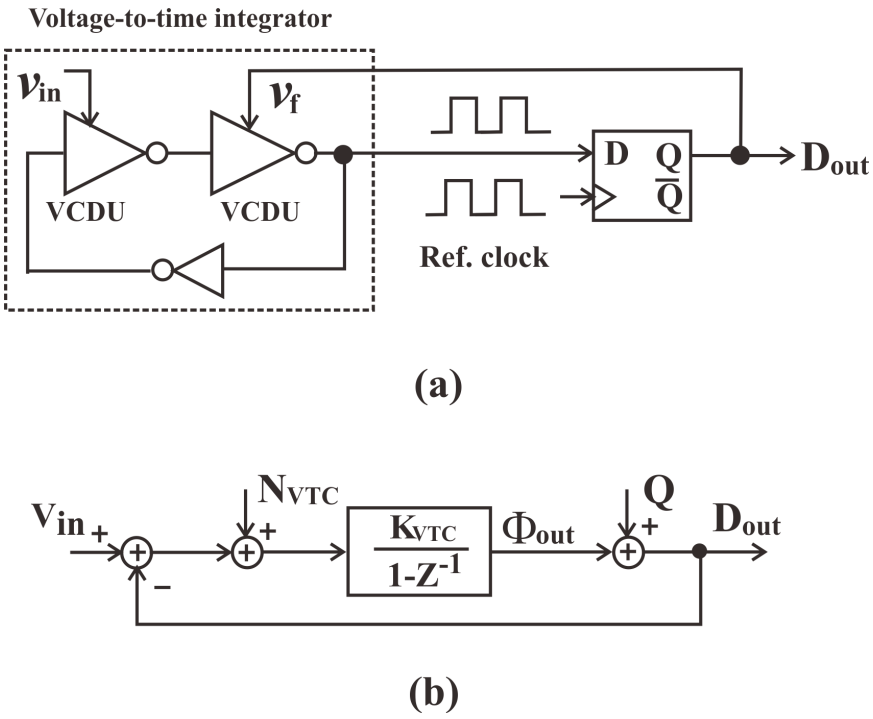


Figure 4.1: Single-bit Time-Mode ΔΣ ADC.

4.1.2 Multi-bit Time-Mode ΔΣ ADC with VCO-based Qauntizer

To closely analyse this type of multi-bit time-mode ΣΔ ADC, block diagrams of a VCO-based modulator, proposed by [33], which uses a VCO as a voltage-to-phase converter and a counter as a phase quantizer to perform voltage-to-digital conversion are given in Fig.4.2. The VCO quantizer consists of a VCO for voltage-to-phase conversion with its transfer function

$H_{VCO}(z) = K_{VCO}/(1 - z^{-1})$ and a counter for phase-to-digital conversion with its transfer function $H_C(z) = (1 - z^{-1})/(2\pi)$. Represent the effect of the nonlinear voltage-to-phase characteristics of the VCO by $N_{VCO}(z)$ while the quantization noise of the phase-to-digital quantizer is represented by $Q(z)$. Since the system consists of a continuous-time part (the loop filter) and a discrete-time part (the sample-and-hold, VCO-quantizer, and DAC), we make use of $z^{-1} = e^{-sT_s} \approx 1 - sT_s$ where T_s is the sampling period, $s = j\omega$, $\omega = 2\pi/T$, T is the period of the input signal, and $T_s \ll T$ to approximate the discrete-time part with a continuous-time counterpart shown in Fig.4.2(c). If the loop gain is sufficiently large

$$D_{out}(s) \approx V_{in}(s) + \frac{N_{VCO}(s)}{H_{LP}} + \frac{sT_sQ(s)}{H_{LP}K_{VCO}}. \tag{4.2}$$

It is seen that the input appears at the output no attenuation, the effect of the nonlinearity of the VCO is suppressed by the gain of the loop filter, and the quantization noise is 1st-order noise-shaped and attenuated by the loop gain.

Since the derivative of phase is frequency, the preceding time-mode modulator with a VCO phase quantizer can be implemented using a VCO frequency quantizer, as shown in Fig.4.2(a, the counter is replaced with the differentiator). The 1st-order digital differentiators perform phase-to-frequency conversion [55, 1]. The system diagram of the ADC is shown in Fig.4.2(b). Following the same arguments as those for the VCO phase quantizer, we transform Fig.4.2(b) to Fig.4.2(c). The output is given by

$$\begin{aligned} D_{out}(s) &= \frac{sT_sQ(s)}{D(s)} + \frac{K_{VCO}N_{VCO}(s)}{D(s)} \\ &+ \frac{K_{VCO}H_{LP}(s)V_{in}(s)}{D(s)}, \end{aligned} \tag{4.3}$$

where $D(s) = 1 + K_{VCO}H_{LP}(s)$. Consider the case where the loop filter is a 1st-order integrator $H_{LP}(s) = 1/(sT_s)$. Assume that a large loop gain exists, i.e., $K_{VCO}H_{LP} \gg 1$, Eq.(4.3) becomes

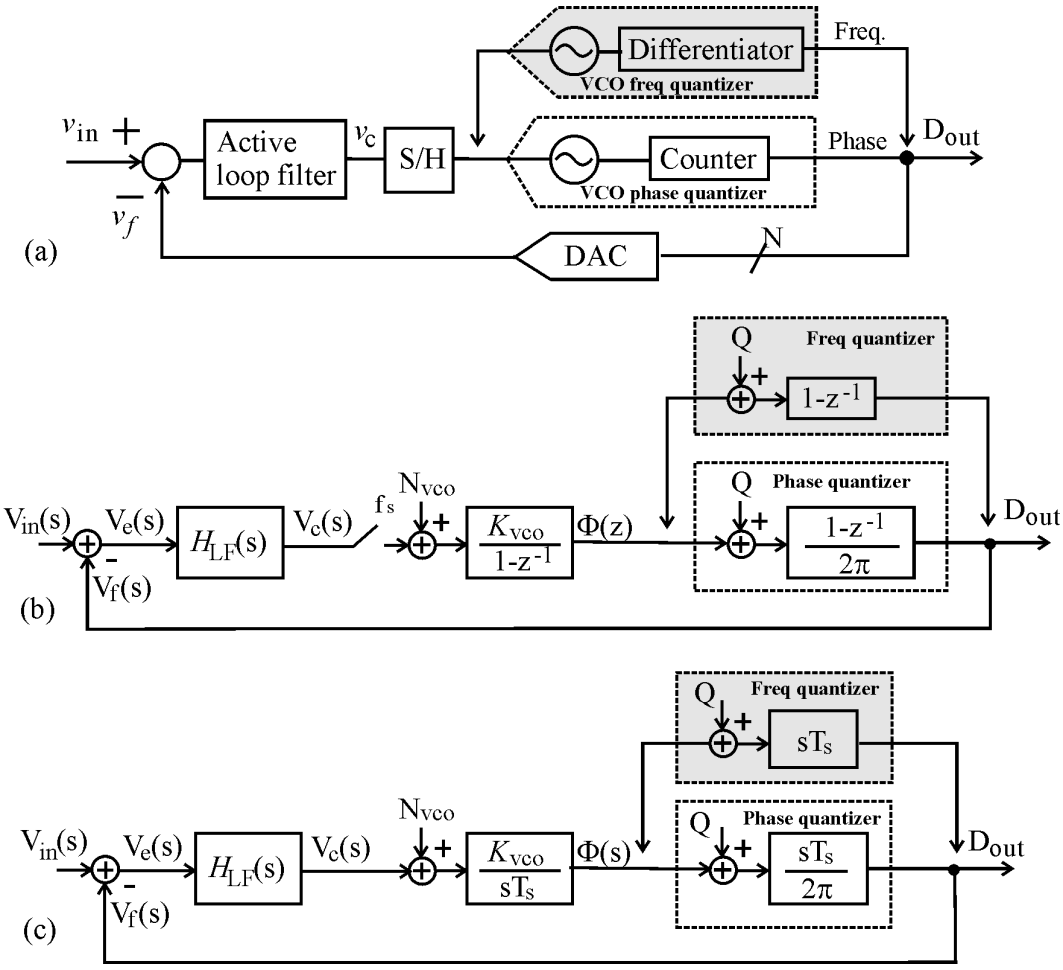


Figure 4.2: Time-mode $\Delta\Sigma$ modulators with VCO phase and frequency quantizers.

$$D_{out}(s) \approx V_{in}(s) + \frac{(sT_s)^2 Q(s)}{H_{LP} K_{VCO}} + \frac{N(s)}{H_{LP}}. \tag{4.4}$$

It is evident that the input signal passes through the modulator with no attenuation, the nonlinear effect is suppressed by the gain of the loop filter, and the quantization noise is both 2nd-order noise-shaped and loop gain suppressed.

As compared with $\Delta\Sigma$ modulators with a VCO phase quantizer, $\Delta\Sigma$ modulators with frequency feedback suffer from the drawback of increased harmonic tones in the spectrum. This is because VCOs are voltage-to-phase converters. In order to confine the phase of the VCO to a small range so as to minimize the effect of the nonlinear voltage-to-phase characteristics

of the VCO, phase feedback rather than frequency feedback is preferred. To overcome the drawback of $\Delta\Sigma$ modulators with a VCO frequency quantizer while avoiding the deployment of a counter phase quantizer, the time-mode $\Delta\Sigma$ modulator proposed in [20] and shown in Fig.4.3 employs a multi-bit phase detector to detect phase lead/lag of the VCO quantizer with respect to a reference phase Φ_{ref}. Since the output of the VCO is phase rather than frequency, the use of phase as the feedback signal enables the modulator to track the input signal more closely so as to confine the error voltage v_e subsequently the control voltage of the VCO v_c to a small region. This in turn reduces the effect of the nonlinear voltage-to-phase characteristics of the VCO subsequently reduced harmonic tones.

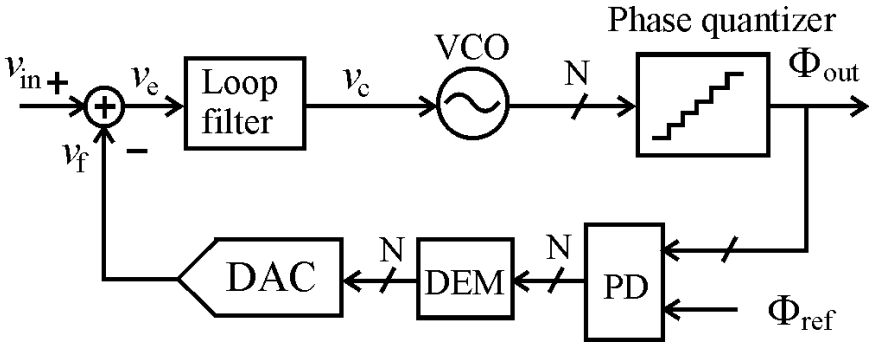


Figure 4.3: $\Delta\Sigma$ ADC with phase feedback.

4.1.3 Thesis Objective

By analysing the prior works on time-mode $\Delta\Sigma$ ADC, we conclude that the single-bit time-mode $\Delta\Sigma$ ADC has an all-digital architecture but its resolution very low. Multi-bit time-mode $\Delta\Sigma$ ADC can improve the resolution by increasing OSR, but since K_{VCO} is typically small, the loop filter must provide most of the loop gain needed to suppress noise due to non-linear effect of the VCO $N_{VCO}(z)$ and the quantization noise power $Q(z)$. To achieve this, active loop filters implemented using operational amplifiers (op-amps) are often used [55, 1, 61, 51]. This, however, is at the cost of high power consumption. The settling time of op-amps also limits the loop bandwidth subsequently the achievable OSR. The performance of op-amp based active filters scales poorly with technology. As a result, the performance of

these time-mode ΔΣ ADCs degrades with technology scaling.Therefore, the objective of this dissertation is to explore the possible architecture of all-digitally implemented time-mode ΔΣ ADC so as to take the full advantage of technology scaling without employing an active loop filter.

4.2 Proposed All Digital 1^{st} Order Time-Mode ΔΣ ADC

In this section, an all-digital time-mode first-order ΔΣ modulator with a 3-bit VCO frequency quantizer is presented. The proposed ΔΣ modulator consists of a voltage-to-time integrator that performs voltage-to-time integration conversion, a phase-frequency-detector-based (PFD) pulse generator, a seven-stage gated current-starved ring oscillator to perform 3-bit quantization, and seven digital differentiators to provide both first-order noise-shaping and frequency feedback. As the goal of this study is to explore possible architectures of all-digital time-mode ΔΣ modulators with multi-bit quantization, no active loop filter is attempted in this design. As a result, the order of the ADC is only one. All-digital time-mode high-order ΔΣ modulators can be readily implemented using digital integrators such as the time accumulators proposed in [104]. The proposed all-digital ΔΣ modulator differs from the all-digital ΔΣ modulator proposed by Taillefer and Roberts in [103] in the following aspects : (i) Taillefer-Roberts ΔΣ ADC performs single-bit quantization while the proposed ΔΣ ADC performs 3-bit quantization. Multi-bit feedback also allows the feedback signal tracks the input signal more closely so as to minimize the effect of the nonlinearity of VTC integrator. (ii) Although both perform first-order noise-shaping, the proposed ΔΣ allows the insertion of a time-mode integrator, such as a time accumulator proposed in [104], between PFD and GRO, so as to realize a high-order modulator subsequently achieve high-order noise-shaping. The insertion of a time-mode integrator also suppress the effect of the nonlinearity of the components in the forward path.

4.2.1 System Model

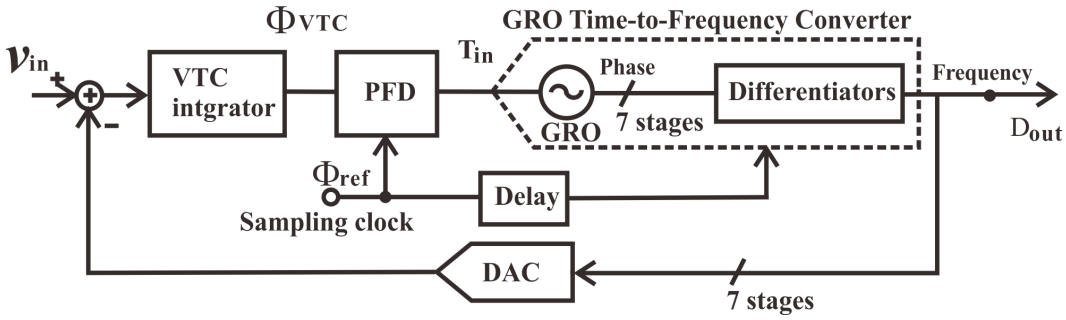


Figure 4.4: System Model of the Proposed 1^{st} Order $\Delta\Sigma$ ADC.

The block diagram of the proposed all-digital time-mode first-order $\Delta\Sigma$ ADC is shown in Fig.4.4(a). The ADC comprises of a voltage-to-time integrator, a DFF-based phase-frequency detector (PFD), a 3-bit GRO quantizer, and seven first-order digital phase differentiators providing both first-order noise-shaping and frequency feedback. All DFFs are implemented using true-single-phase-clock (TSPC) logic to take the advantage of their high speed and low power consumption.

4.2.2 Frequency Domain View and Analysis

To analyse the proposed model closely, let's take a look at the frequency domain view of the proposed 1^{st} order $\Delta\Sigma$ ADC as shown in Fig.4.5. Although the VTC is implemented using a ring oscillator, since the PFD detects the difference between the phase/frequency of the VTC integrator and those of the reference clock, and have it converted to a time variable T_{in} for an input voltage v_{in}, there is a corresponding T_{in} generated by the PFD. As a result, the VTC ring oscillator and PFD are modeled as a gain block of gain K_{VTC}. The output of the PFD is a time variable T_{in}.

Also in Fig.4.5, N_{VTC} and N_{GRO} represent the nonlinearity of the VTC integrator and GRO, respectively. It can be shown that

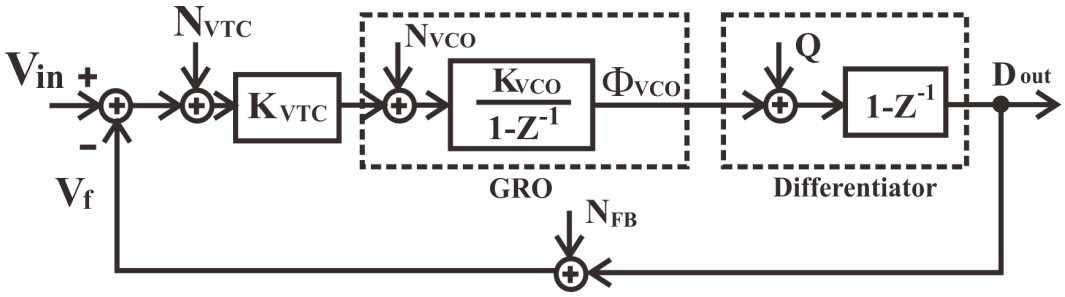


Figure 4.5: Frequency Domain View of the Proposed 1^{st} Order $\Delta\Sigma$ ADC.

$$\begin{aligned} D_{out} &= \frac{K_{VTC}K_{GRO}}{D(z)}\left[V_{in}(z) + N_{VTC}(z) + V_{FB}(z)\right] \\ &+ \frac{(1-z^{-1})Q(z)}{D(z)} + \frac{K_{GRO}}{D(z)}N_{GRO}(z), \end{aligned} \tag{4.5}$$

where $D(z) = 1 + K_{VTC}K_{GRO}$. If $K_{VTC}K_{GRO} \gg 1$, $D(z) \approx K_{VTC}K_{GRO}$ and Eq.(4.5) is simplified to

$$\begin{aligned} D_{out} &\approx V_{in}(z) + N_{VTC}(z) + V_{FB} \\ &+ \frac{(1-z^{-1})Q(z)}{K_{VTC}K_{GRO}} + \frac{N_{GRO}}{K_{VTC}}, \end{aligned} \tag{4.6}$$

It can be seen from Eq. (4.6) that when $K_{VTC}K_{GRO} \gg 1$ the quantization noise is first-order noise-shaped, the nonlinearity of the GRO is suppressed by the gain of the VTO integrator, and the nonlinearity of the VTC integrator and that of the feedback path appear at the output without attenuation. Due to the insufficient loop gain subsequently insufficient attenuation of the nonlinearity of the GRO and non-suppression of the nonlinearity of both th VTC integrator and the feedback path, it is expected that harmonic tones will exist in the spectrum of the ADC. Fig.4.6 provides the timing diagram of the critical nodes of the proposed ADC.

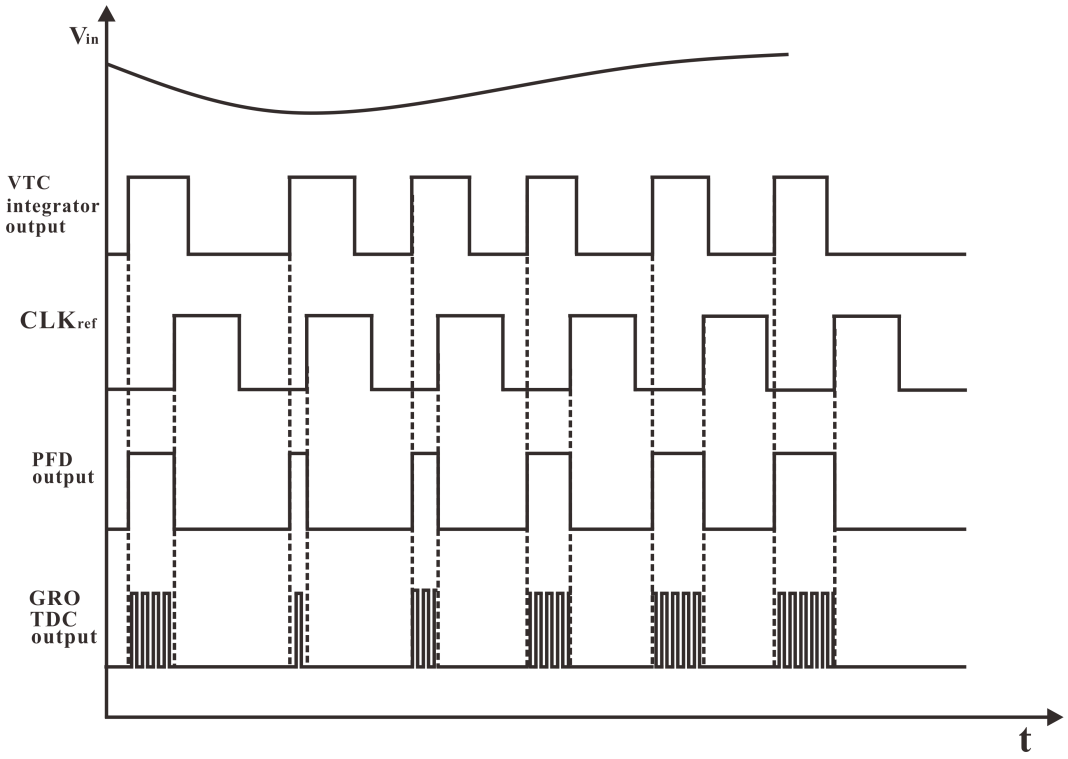


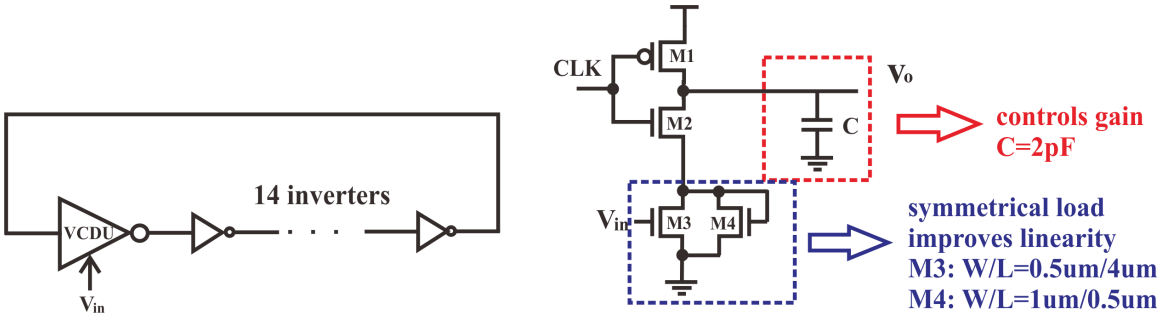
Figure 4.6: Timing diagram of the critical nodes of proposed all digital time-mode ΔΣ ADC.

4.3 Circuit Implementation

4.3.1 Voltage-to-Time Integrator

The VTC integrator shown in Fig.4.7(a) is a ring oscillator consisting of a voltage-controlled delay unit (VCDU) inverter and 14 static inverters. As shown in Fig. 4.7(b), the VCDU is implemented using a current-starved inverter with a large capacitor load capacitor to increase the gain. Note that the gain of the VCDU is the ratio of the amount of time delay to the amplitude of the input voltage. It should be noted that M3 should be in saturation and behaves as a voltage-controlled current source to ensure a constant transconductance. Since both the transconductance and output resistance of M3 are not constant by nature, the use of diode-connected M4 in parallel with M3 improves the linearity of the voltage-to-

current characteristics of M3. The effect of adding M4 to improve linearity is demonstrated in Fig.4.8.



(a) VTC integrator **(b) Voltage-controlled delay unit (VCDU)**

Figure 4.7: VTC Integrator.

As the input voltage only controls the discharging current of the load capacitor, only the falling edges will be delayed with a respect to the reference clock that charges the load capacitor. The delayed falling edge is inverted twice by the two static inverters in the loop and fed back to the input of the VCDU. Thus the delay accumulates while the signal travels around the loop and the loop is actually a first-order delay accumulator. To evaluate the performance of the implemented VCDU, a test input sinusoidal voltage of an amplitude of 100mV at frequency 100kHz is applied to the input of the VCDU. Clocked at 10MHz, the transient output delay from VCDU is plotted in Fig.4.9. In order to observe the non-linear characteristic of the VCDU, FFT is taken on the output delay and the plot is depicted in Fig.4.10.

4.3.2 Pulse Generator

After the VTC integrator, a DFF-based phase/frequency detector (PFD) is deployed to capture the time difference between the rising edge of the output of the VTC integrator and that of the reference clock and generate T_{in}. The DFFs in the PFD are implemented using TSPC DFFs, as shown in Fig.4.12. The frequency of the VTC integrator is set slightly higher than reference clock frequency in order to prevent the accumulated phase of the

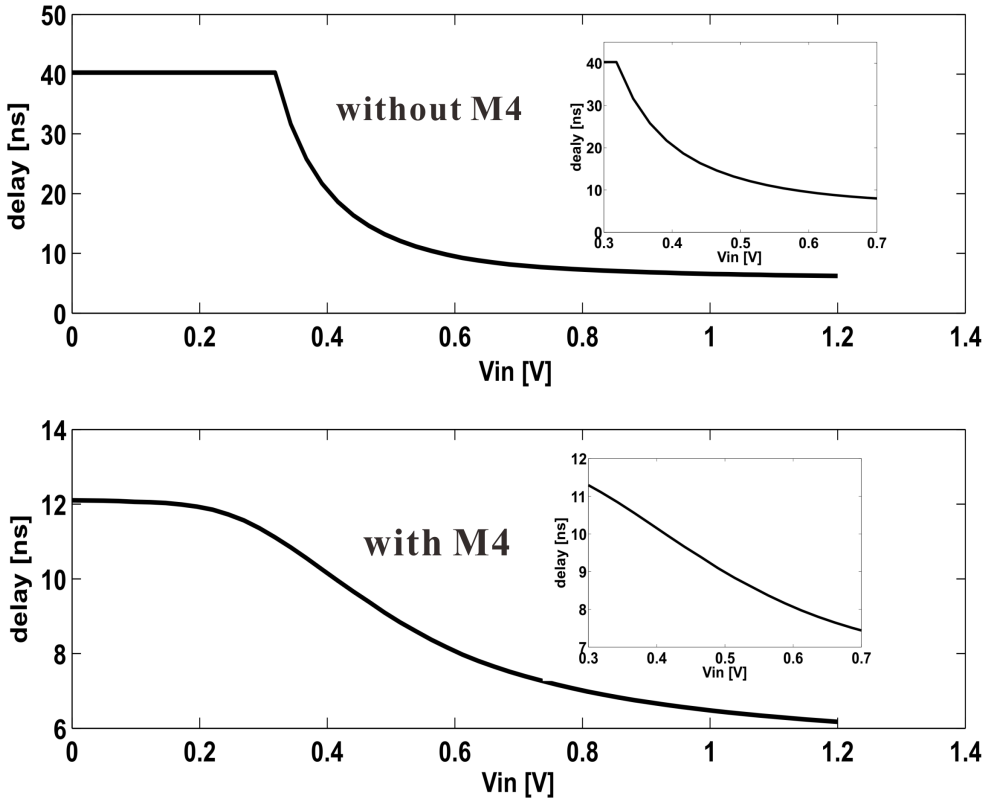


Figure 4.8: Improved Linearity by Adding M4

VTC integrator from exceeding one reference clock period known as phase wrapping. Phase wrapping must be avoided as the maximum time difference T_{in} between the rising edge of the VTC integrator and that of the reference clock is 2π. Beyond that T_{in} is reset. This is illustrated in Fig.4.11.

When negative feedback is present, the negative feedback will stabilize the frequency of the VTC integrator ensuring that phase wrapping will not occur [105].

4.3.3 Gated-Ring-Oscillator

The generated pulse, which is also a time difference variable, is quantized using a 7-stage GRO-based TDC as illustrated in Fig.4.13. The gated-ring-oscillator performed a time-to-phase integration function. This because the input time difference variable causes the output phase of the GRO to accumulate over time. Therefore the action is integration. As

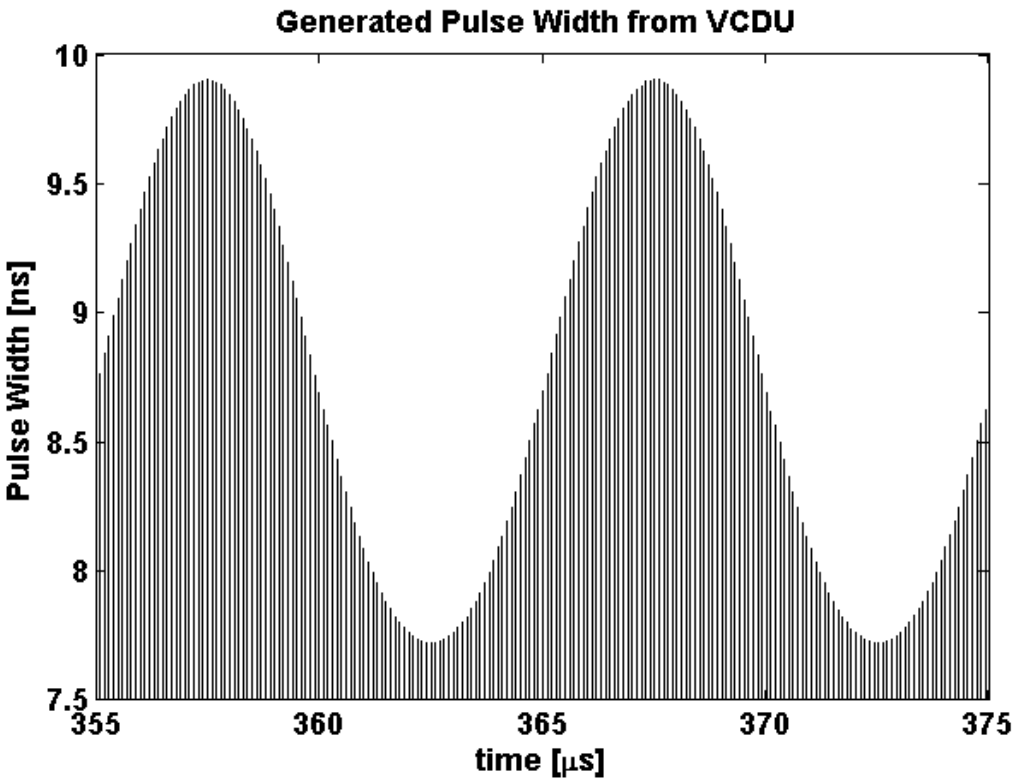


Figure 4.9: Output Delay from the VCDU with a Sinusoid Input Voltage

shown in Fig. 4.14, the simple 7-stage GRO is implemented using MOS device switches. A pMOS-based and a nMOS-based switch are added in series to the positive and negative power supply connection of a 7-stage static inverter-based ring oscillator. Each stage in such a GRO is known as a gated delay cell and the switches in gated delay cell share a common state. When there is no incoming time difference variable, the gated voltage is logic 0 and the switches are open. So the ring oscillator is disabled. When an incoming time difference variable (a pulse) arrives, the switches are closed and ring oscillator starts to run at a fixed frequency. The ratio of the switch transistors to the inverter transistors is 8:1 to allow for a fast operation speed. A load capacitor of $10pF$ is added to each stage to set the oscillation frequency of the GRO to 4.4MHz.

Fig.4.15 plots the relation of the pulse width of the gating voltage of the GRO and the sum of the output voltage of the seven first-order differentiators. It is observed that the GRO

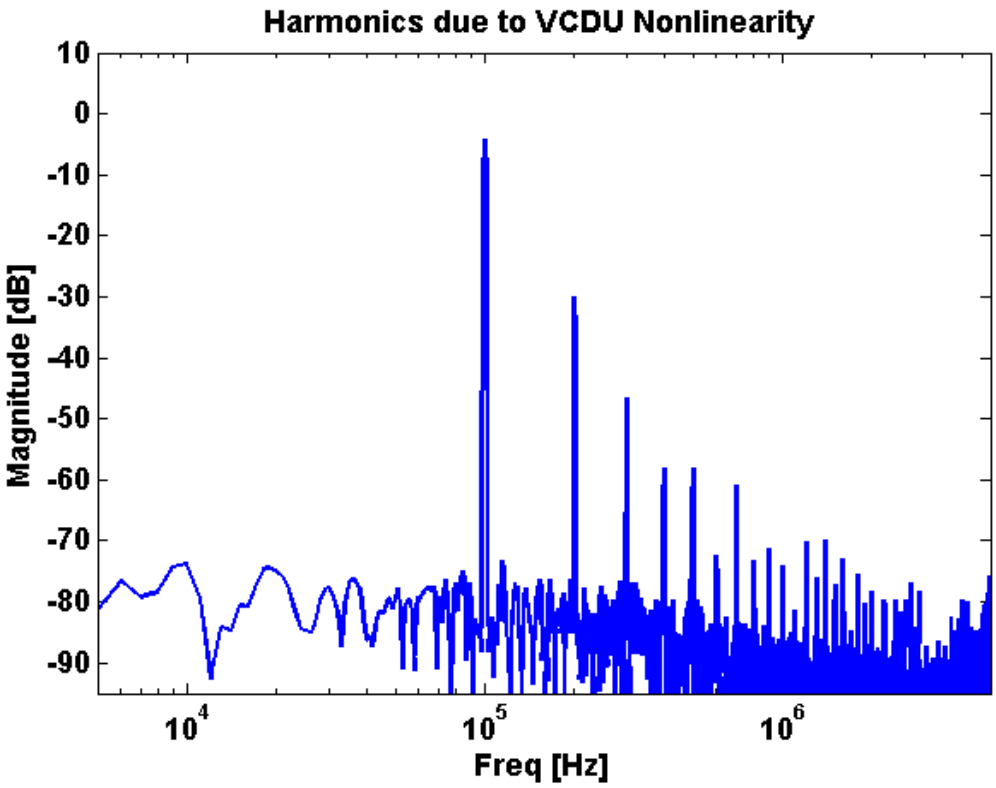


Figure 4.10: FFT showing harmonics of the Simulated Non-linear VCDU

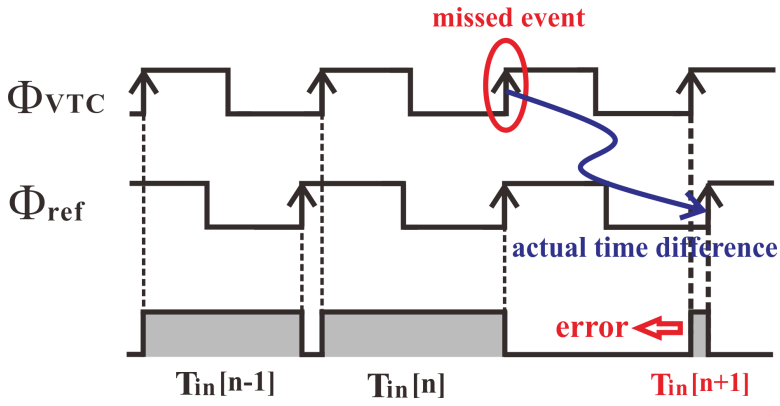


Figure 4.11: Phase wrapping due to Phase Accumulation.

exhibits a good linearity for input pulse width ranging from 0.5 ns to 100 ns, which fully covers the range of the VTC integrator.

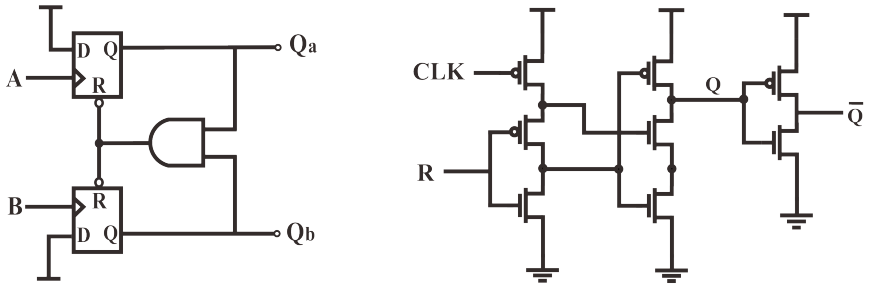


Figure 4.12: Left: Schematic of DFF-based PFDs. Right : Schematic of true single phase clocked DFFs.

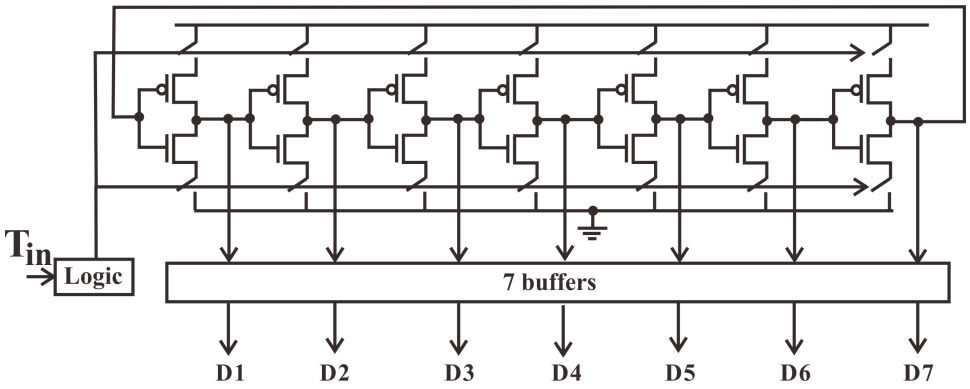


Figure 4.13: A 7-Stage Gated-Ring-Oscillator.

4.3.4 Digital Differentiator

It is the digital counter in a time-mode ADC that performs the actually time-to-digital conversion. The GRO only performs a time-to-digital conversion in the meanwhile provides 1^{st} order shaping on the quantization error. There are several topologies to implement a digital counter. However such a counter requires a reset mechanism and it complicates the design for the readout circuits. One approach to remove the need for a reset counter is to use non-reset registers XOR gates. The implementation is detailed in Fig.4.16 and it is known as a 1^{st} order digital differentiator. It operates by sampling the GRO output phase to an array of DFF-based registers and comparing the sampled output phase to the previous sample using an array of XOR gates.

The operation of the digital differentiator is explained in Fig.4.17 where the shaded inverters represent the ones that undergo phase transition during a sampling period. It should be

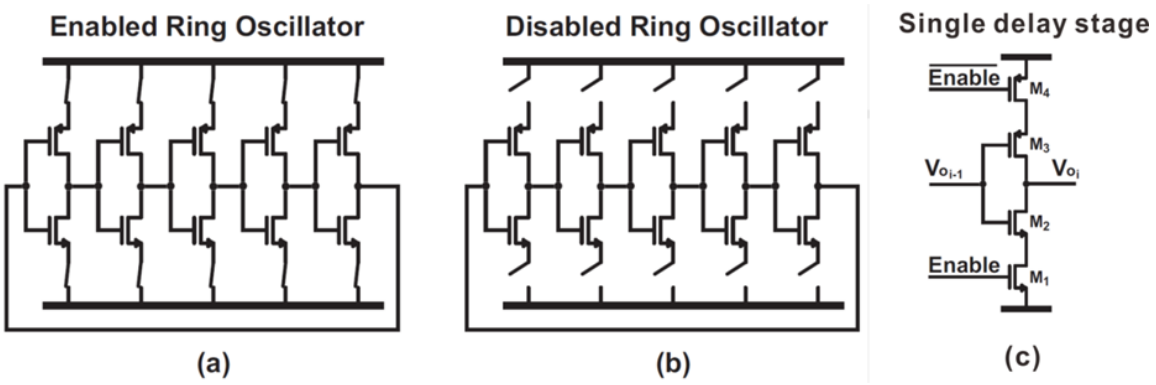


Figure 4.14: GRO Implementation.

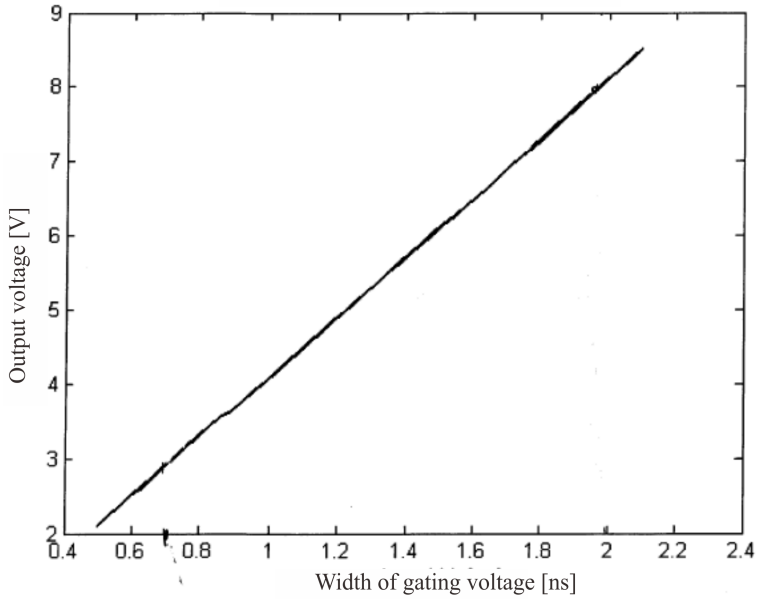


Figure 4.15: Simulated GRO Characteristics by Sweeping Input Pulse Width.

noted that the XOR gate array performs logic subtraction if an output phase of π from the GRO fully covers the input dynamic range. This is because the XOR gate array is able to track the phase transition for GRO stage only if each GRO stage undergoes a phase transition no more than once during the sampling period. Since the number of GRO stages that undergo a phase transition is proportional to the input time difference variable and the

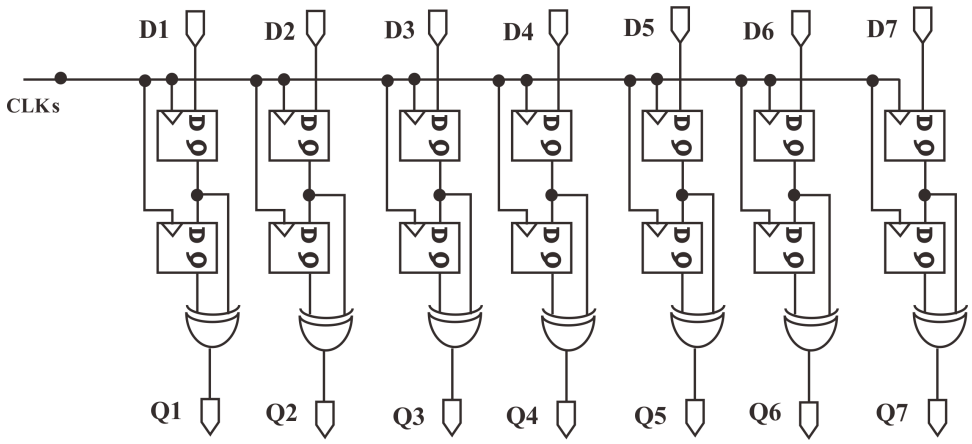


Figure 4.16: Implementation of 7-Stage Digital Digital Differentiator.

maximum possible value of $T_{in[n]}$ is T_S where T_S represent the sampling period, the frequency of the GRO and the sampling frequency of the ADC have to satisfy:

$$f_S > 2f_{GRO}, \tag{4.7}$$

Since in this work, f_{GRO} is set to 4.4MHz and the sampling frequency is 10MHz, Eqt.4.7 is satisfied. As depicted in Fig.4.18, the transfer function of the digital differentiator is $1 - Z^{-1}$ because the XOR gate array subtracts the GRO output phase from the previous sample from the current sample if Eqt.4.7 is met.

4.3.5 Frequency Feedback

Negative frequency feedback is formed by injecting the currents modulated by the thermometer-coded digital output of the first-order digital differentiators to the capacitor node of the VCDU, as shown in Fig.4.19. Since the input voltage discharges the capacitor, the feedback counteracts this by charging the capacitor with digitally modulated currents. If the input voltage increases, the discharge current of the capacitor will rise accordingly. As a result, the rising edge of v_o will advance in time and the time variable of the GRO increases. As a result, the thermometer-coded output of the GRO will also increase, i.e., more digits will become 1, resulting in the turn-on of more transistors that modulate the feedback currents.

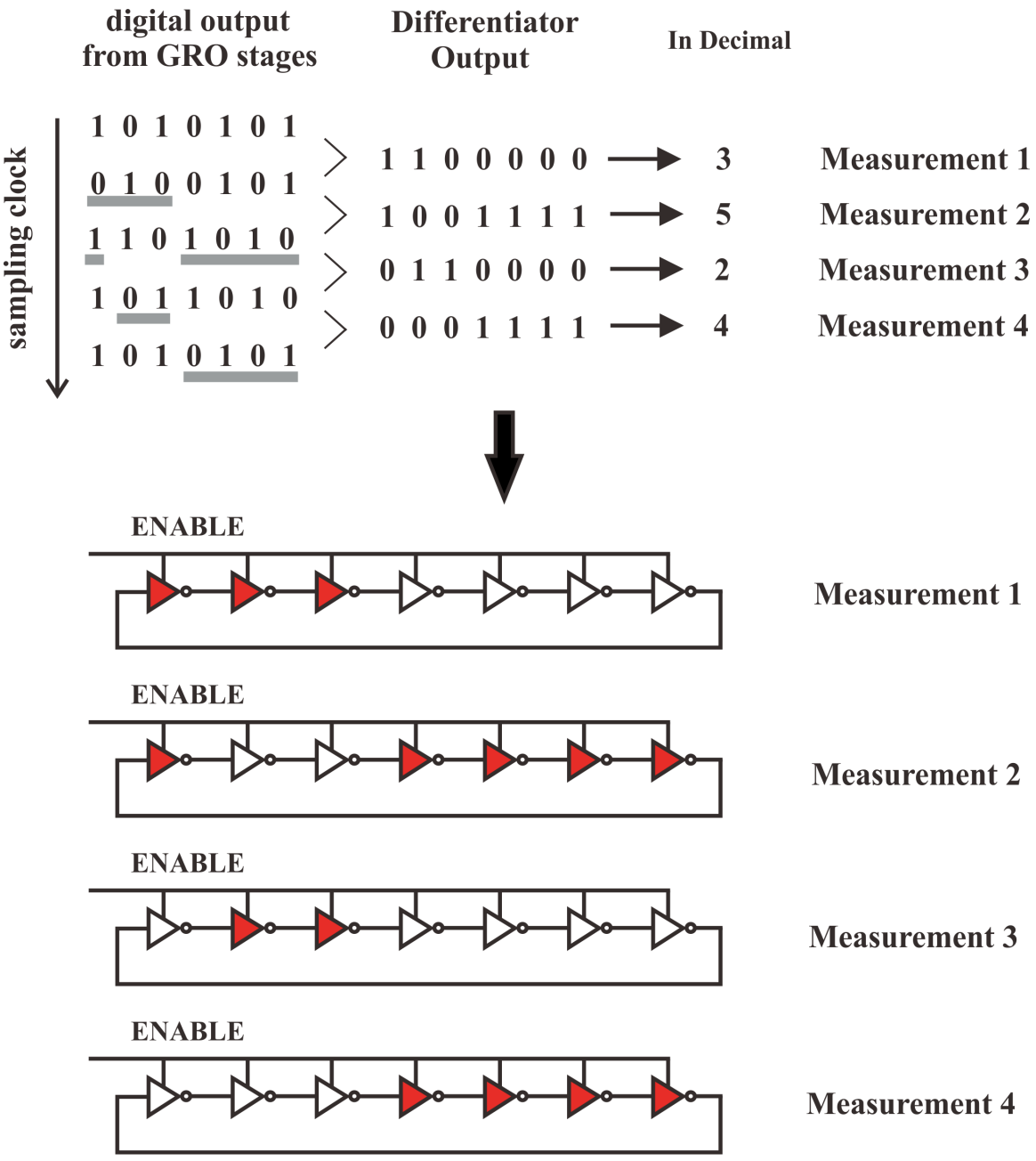


Figure 4.17: Operation of Digital Differentiator.

It becomes evident that the negative feedback will delay the advance of the rising edge of v_o in time subsequently stabilize the frequency of the VTC integrator and T_{in}.

The size of the transistors in the feedback path must be chosen properly to ensure the proper dynamics of the modulator. Specifically, if it is too small, the feedback will be too weak. If

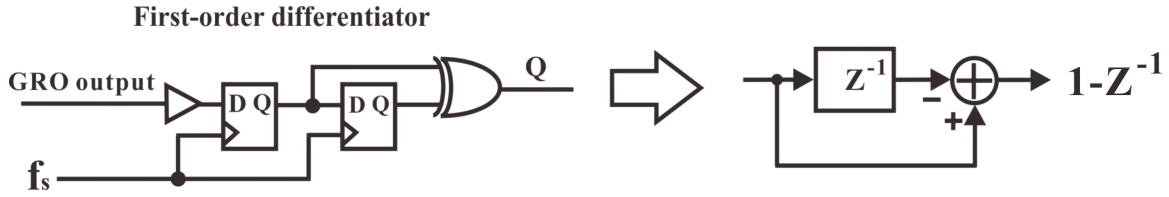


Figure 4.18: Transfer Function of Digital Differentiator.

it is too large, the feedback will be too strong. The size for the feedback pMOS transistors is $W_p = 3\mu m, L = 500nm$.

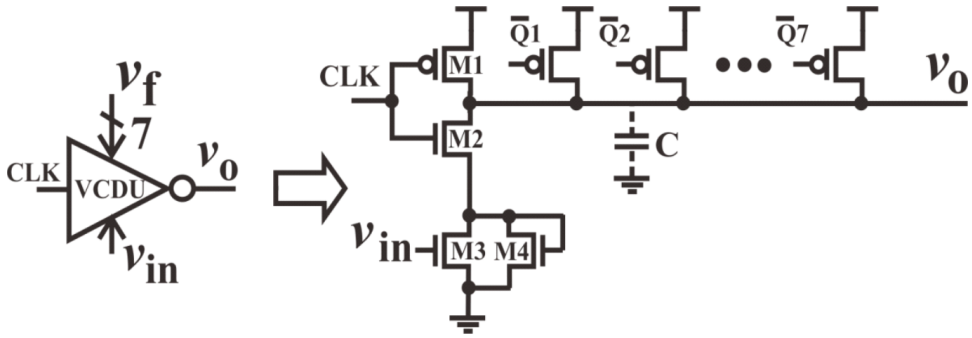


Figure 4.19: VCDU with Negative Feedback.

4.4 Simulation Result of the Proposed 1^{st} Order $\Delta\Sigma$ ADC

The proposed first-order all digital time-mode delta sigma ADC has been designed in an IBM 130 nm 1.2 V CMOS technology with its layout shown in Fig.4.20. GRO has seven stages and oscillates at 4.4 MHz. Each stage has a 10 pF capacitor load. The total silicon area including bonding pads is 1 mm × 1 mm. The core circuit occupies an area of 470 μm × 470 μm. The pads are laid out in accordance with the configuration of the probes available to us. Three pads configured for RF single-ended probes (GSG with G for ground and S for signal) are placed to the left of the chip core and another set of three pads with the same configuration are placed to the right of the chip core, one for probing the output

of the differentiator and the other for probing the output of the VTC integrator. Static inverter-based voltage buffers are employed between the internal modes and the pads so that the signals to be measured can drive test equipment. The buffers were sized in accordance to the input impedance of Agilent MSO-X 3024A oscilloscope (1 MΩ and 14 pF) with build-in logic analyzers that will allow us to capture the waveform and perform post signal processing. The five pads at the top of the chip are for supply voltage and ground. An external clock of 10 MHz will be brought to the chip via the bottom pads configured as per the differential RF probe (GSGSG) available to us. The ADC was analyzed using Spectre from Cadence Design Systems with BSIM4 device models. The input of the modulator is a 100 mV 100 kHz sinusoid.

Fig.4.21 plots the waveform of the sum of the output of the seven differentiators. The sinusoidal profile of the 100 mV 100 kHz sinusoid input is clearly observed.

To obtain the spectrum of the output of the modulator, FFT analysis was performed on the sum of the steady-state time-domain output stream of the seven differentiators. Since the input is at f_{in}=100 kHz, the high frequency of interest was set to f_{max}=20 MHz while the lowest frequency was set to f_{min}=5 kHz. In order to have a sufficient frequency resolution to capture the 100 kHz input tone and its harmonics while keeping the time-domain simulation time reasonably low, the bin size f_{bin}, i.e. frequency resolution, was set to f_{bin}=5 kHz. The corresponding steady-state time-domain window where the time-domain results were used for FFT analysis was set to $T_w = 1/f_{bin}$=0.2 ms. In order to force the simulator to calculate the exact point that DFT function will sample, in transient analysis, strobe option was set with strobe period T_w/pts where pts is the number of data samples used in FFT analysis. In our analysis, pts=8k. FFT was performed on the sum of the output stream of the seven differentiators. Hanning Window was used to reduce spectrum leakage. The spectrum of the modulator is shown in Fig.4.22. Evaluated over 4 MHz bandwidth, the ΔΣ ADC has an SNDR of 45.5 dB and an SFDR of 32.3 dB.

Fig.4.23 plots the dynamic range of the ADC. For each point of the plot, FFT analysis was performed and the corresponding SNDR was calculated. Fig.4.24 shows the spectrum of the ADC at different input levels.

The following Figure-of-Merit (FOM) widely used to quantify the performance of ADCs based on the amount of power per conversion step is used as a bench mark to compare the performance of ADCs [35, 32, 44, 63, 48]

$$\text{FOM} = \frac{PW}{2^{\text{ENOB}}(2\times BW)}, \tag{4.8}$$

where BW is the bandwidth of the input, ENOB is the effective number of bits and PW is the power consumption of the ADC. ENOB is obtained from ENOB=(SNDR-1.76)/6.02. In Table 4.1, the performances of some recent time-mode $\Delta\Sigma$ ADCs are compared. It is seen the proposed all-digital time-mode first-order $\Delta\Sigma$ modulator outperforms the all-digital time-mode first-order $\Delta\Sigma$ modulator in [103] with FOM approximately 19 times better. The OSR of the example presented in the paper is only 2.5. Should OSR increases, improved performance is expected.

4.5 Design of 2^{nd} Order $\Delta\Sigma$ ADC

$\Delta\Sigma$ ADC with higher-order noise shaping characteristics is more appealing because the in-band noise power is further suppressed. Consequently a better SNDR can be obtained. In this section, the implementation of a 2^{nd} order time-mode $\Delta\Sigma$ ADC is being presented. This is achieved by replacing the 1^{st} order differentiator with a 2^{nd} order digital differentiation in the original ADC design.

4.5.1 System Model and Frequency Domain Analysis

The system model of the proposed 2^{nd} order time-mode $\Delta\Sigma$ ADC is illustrated in Fig.4.25. Fig. frequency domain view of the 2^{nd} order system. The 2nd-order digital differentiation is obtained by cascading two 1st-order digital differentiators, as shown in Fig.4.27. Since $Q_k(z) = (1 - z^{-1})D_k(z)$ and $Q_k^*(z) = (1 - z^{-1})Q_k(z)$, we therefore have $Q_k(z) = (1 - z^{-1})^2 D_k(z)$.

By analysing the 2nd-order $\Delta\Sigma$ modulator in frequency domain, as shown in Fig.4.26m the signal, noise, and nonlinearity transfer functions of the modulator are given by

$$\mathrm{STF}(z) = \frac{K_{VTC}K_{GRO}}{K_{VTC}K_{GRO}+1}. \tag{4.9}$$

$$\mathrm{NTF}(z) = \frac{(1-z^{-1})^2}{K_{VTC}K_{GRO}+1}. \tag{4.10}$$

$$\mathrm{NonTF}_{GRO}(z) = \frac{K_{GRO}(1-z^{-1})}{K_{VTC}K_{GRO}+1} \tag{4.11}$$

and

$$\mathrm{NonTF}_{VTC}(z), \mathrm{NonTF}_{FB}(z) = \frac{K_{VTC}K_{GRO}}{K_{VTC}K_{GRO}+1}. \tag{4.12}$$

It is seen that the signal passes through the modulator without attenuation. Quantization noise is 2nd-order noise-shaped starting from low frequencies.Similar to the 1st-order modulator, the effect of the nonlinearity of GRO is 1st-order noise-shaped while that of VTC and feedback path are not.

4.5.2 Simulation Result

The proposed 2^{nd} order $\Delta\Sigma$ ADC is simulated and the FFT on the output waveform is plotted in Fig.4.28. It can be observed that the 2^{nd} order $\Delta\Sigma$ ADC exhibits a 40dB noise-shaping characteristic. Fig. compares the FFT results of the 1^{st} order and 2^{nd} order $\Delta\Sigma$ ADCs. It is evident that the 2^{nd} order $\Delta\Sigma$ ADC has better noise performance. In Table 4.1, the performance of some recently published time-mode $\Delta\Sigma$ modulators and that of the proposed 1st and 2nd-order all-digital time-mode modulators are compared. It is seen the proposed all-digital time-mode 1st-order and 2nd-order $\Delta\Sigma$ modulators outperform the

Table 4.1: Performance comparison of time-mode ΔΣ ADCs.

Ref.	Tech. (nm)	f_s/BW (MHz)	SNDR (dB)	ENOB (bit)	Power (mW)	FOM (fJ/step)	Bits/ Order
[103]	180	140/0.4	38.6	6.1	0.8	14382	1/1st
[55]	130	950/20	55	8.8	38.4	2089	5/2nd
[1]	130	950/10	72	11.7	40	615	5/3rd
[20]	130	900/20	78.1	12.7	87	331	5/4th
This	130	10/4	47	7.5	1.1	760	3/1st
This	130	10/4	54.8	8.8	1.45	407	3/2nd

all-digital time-mode 1st-order ΔΣ modulator in [103] with FOM approximately 19 and 35 times better, respectively.

4.6 Other Time-Mode Circuit Components

In this chapter, implementations for other important time-mode circuit components including a regenerative time amplifier, a time register and a time are provided. Those components are building blocks for a time-mode loop filter which is to be discussed in the next chapter.

4.6.1 Time Amplifier

A simple time amplifier can be implemented as a regenerative time amplifier whose operation is explain in Section 3.2.1. The implementation of the MULTEX circuit-based regenerative time amplifier is depicted in Fig.4.30. The load capacitors at the output nodes are for gain control. The capacitance value used in this work is $2pF$.

The implemented regenerative time amplifier is simulated in transient state by sweeping the input time difference between **A** and **B** in Fig. 4.30 and result is plotted in Fig.4.31. The implemented time amplifier exhibits an input dynamic range of $50ps$ and a gain of 20.

4.6.2 Time Register

As indicated in its name, a time register is a circuit that "registers" a time difference variable and stores it. Fig. 4.32(b) shows a possible implementation of such a "time storage" circuit using a gated delay cell (GDC) followed by a big capacitor and a static inverter. Fig.4.32(a)

shows an example of a gated delay cell. The input to the gated delay cell is an event(rising edge). There are two control signals $Hold$ and $Awake$ applied to the gated delay cell. Under normal operation, an event signal is applied at the input of the gated delay cell and the capacitor starts to discharge from V_{DD}. The output goes from logic 0 to 1 when the capacitor voltage drops below the threshold. When the $Hold$ signal arrives, the discharging process is interrupted and the state of the discharging capacitor is preserved until the $Awake$ signal releases gated delay cell from the hold state. Then the capacitor resumes discharging and output of the delay cell eventually goes to 1. Therefore the operation of the delay cell is "gated" by the two control signals.

The time register is implemented using two identical gated delay cells. To illustrate the operation of the time register, in Fig. the input time difference T_{in} is quantized by the two events **Start** and **Stop**. At the event **Start**, the capacitor in the top gated delay cell starts to discharge until **Stop** comes. The bottom gated delay cell is not gated and the capacitor in the bottom gated delay cell triggered by the **CLK** signal starts to discharge in the meanwhile the top gated delay cell is awake by **CLK** and resumes discharging at the same rate. Once the outputs from both gated delay cells go to logic 1, the time difference between the output rising edges is equal to T_{in}. This is because overall same amount of charge is being transferred from the capacitors. Thus same amount of time should be taken to entirely discharge the two capacitors. However the capacitor on the top is discharged ahead of the bottom one by $Stop - Start = T_{in}$. Then when they are both discharging at the same rate, the time difference for them to be entirely discharged is T_{in}. The simulation result in Fig. demonstrates that the time register has a dynamic range of $5ns$ with a peak error of $\pm 2\%$ over the $5ns$ full scale.

4.6.3 Time Adder

A time adder is implemented based on time registers. The principle is to align the first rising edges of two time difference variables T_{in1} and T_{in2}. Then the difference between the second rising edges of T_{in1} and T_{in2} is taken to produce a quantity equal to $|T_{in1} - T_{in2}|$. It can be easily inferred that the output time difference is a result of time-mode subtraction. Therefore this type of time adder is in fact a time subtracter instead of a time adder. In order

to use this "time subtracter" as an adder, one of the time variables, say, T_{in2} is reversed. As illustrated in Fig.4.35 the output now is the summation of T_{in1} and T_{in2}.

However the challenge arises: due to the non-reversibility of time, how to reverse T_{in2} in real time domain? One solution is to add offset time T_{off} to both the **Stop1** signal and **Start2** signal in Fig.4.36. If the offset time is large enough, then the **Start2** signal becomes the first rising edge of T_{in2}. Now taking the difference between **Stop1** and **Stop2** signals, the result T_{out} is the summation of T_{in1} and T_{in2}. Fig.4.37 provides the implementation details of a time adder. It should be noted that the offset time should be large enough to offset **Start2** and **Stop2**. This condition is described in Eqt.4.13. The simulation result shows that the time adder exhibits good accuracy input below $1.6ns$.

$$T_{off} \geqq max(T_{in2}) \tag{4.13}$$

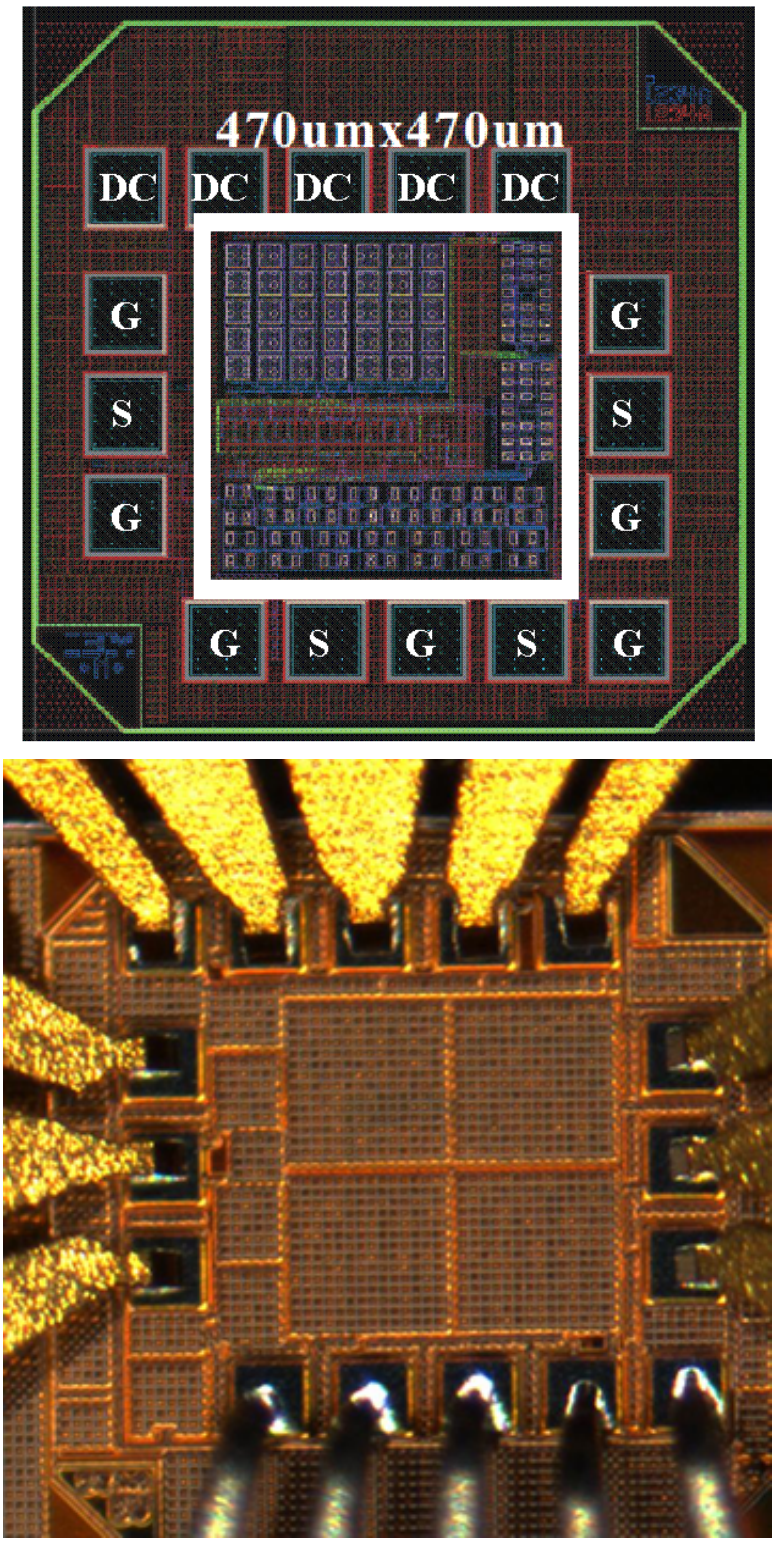


Figure 4.20: Layout of proposed all-digital time-mode first-order $\Delta\Sigma$ modulator.

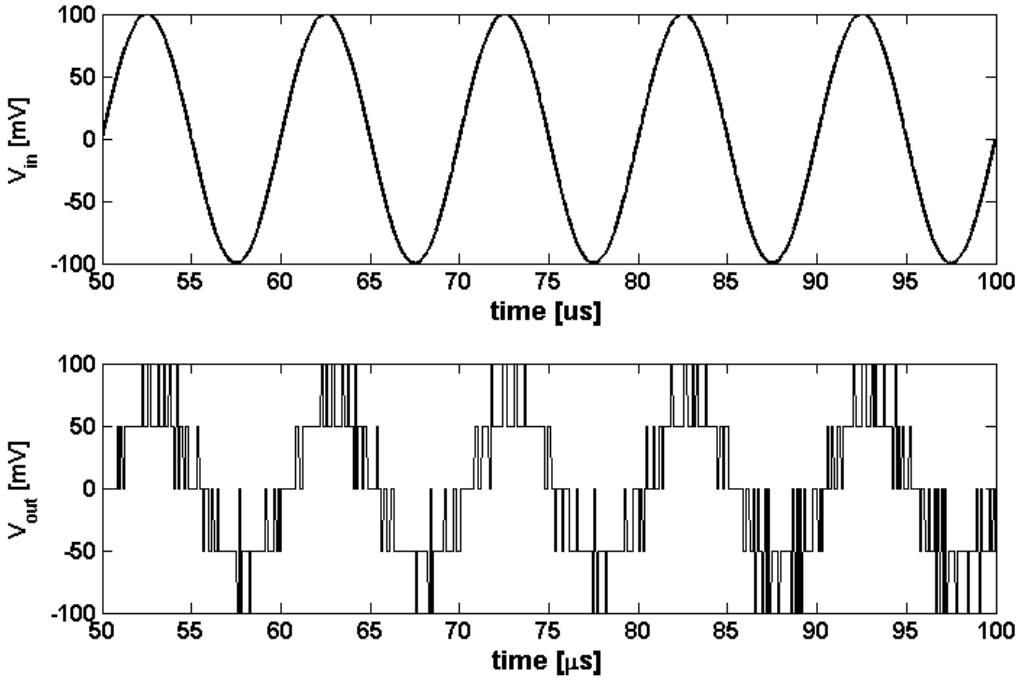


Figure 4.21: Simulated Waveform of the Proposed 1^{st} Order $\Delta\Sigma$ ADC.

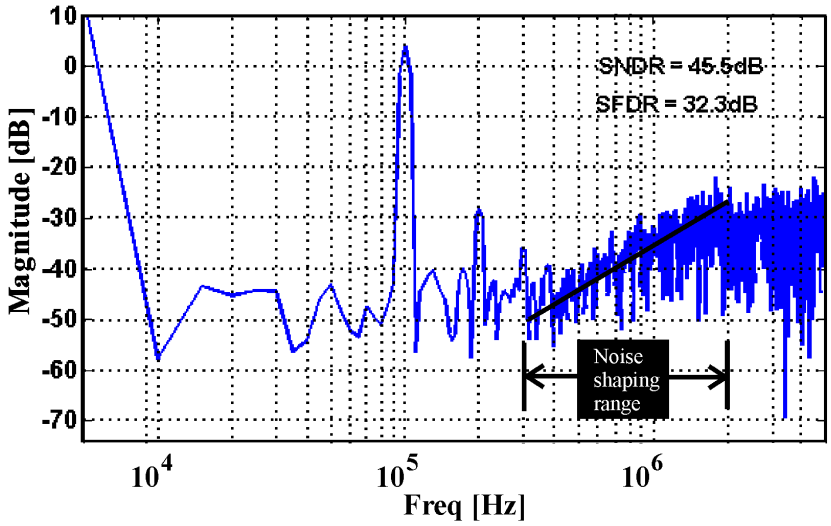


Figure 4.22: FFT of the Simulated Output Waveform of the 1^{st} Order $\Delta\Sigma$ ADC.

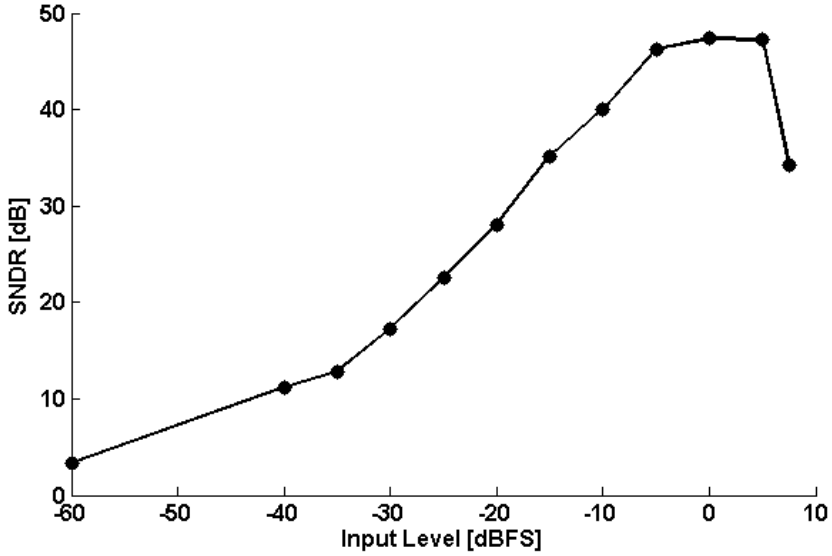


Figure 4.23: Simulated dynamic range of proposed all-digital time-mode first-order $\Delta\Sigma$ ADC.

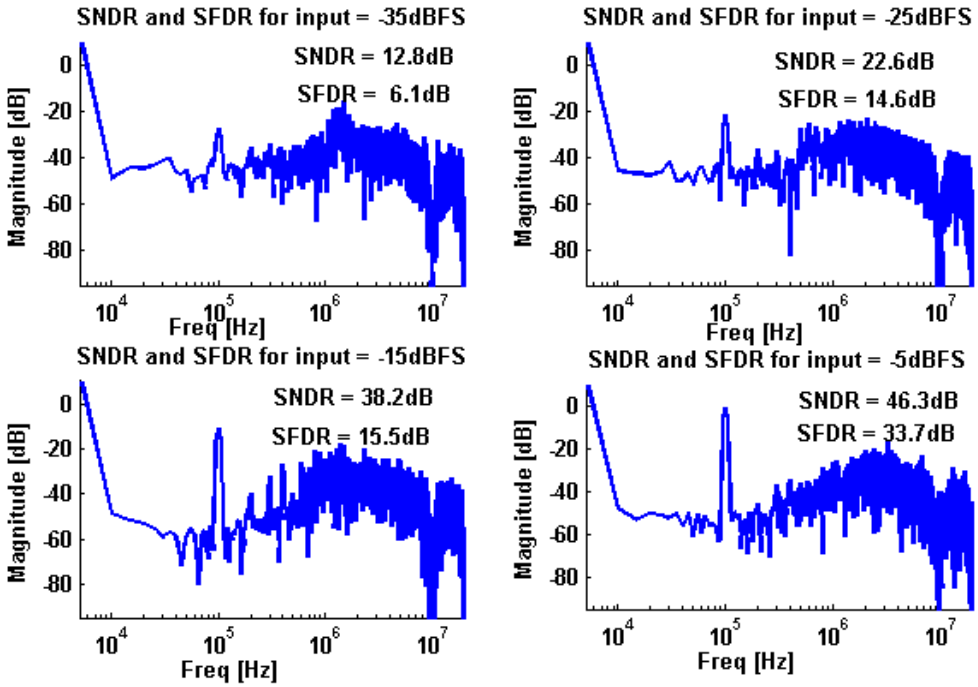


Figure 4.24: Simulated spectrum of proposed all-digital time-mode first-order $\Delta\Sigma$ ADC at various input levels.

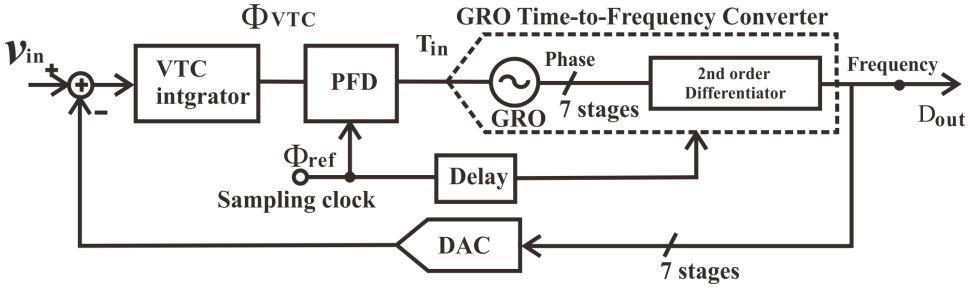


Figure 4.25: System Model of the Proposed 2^{nd} Order $\Delta\Sigma$ ADC.

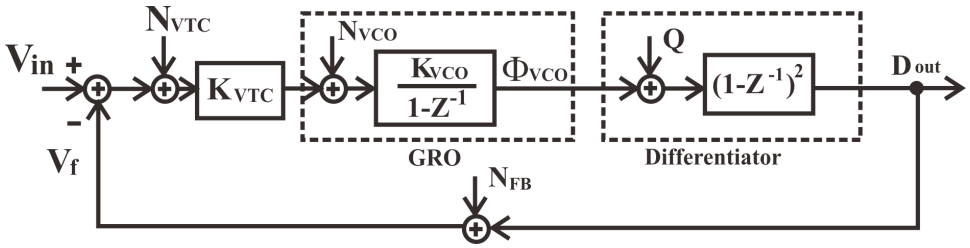


Figure 4.26: Frequency Domain View of the Proposed 2^{nd} Order $\Delta\Sigma$ ADC.

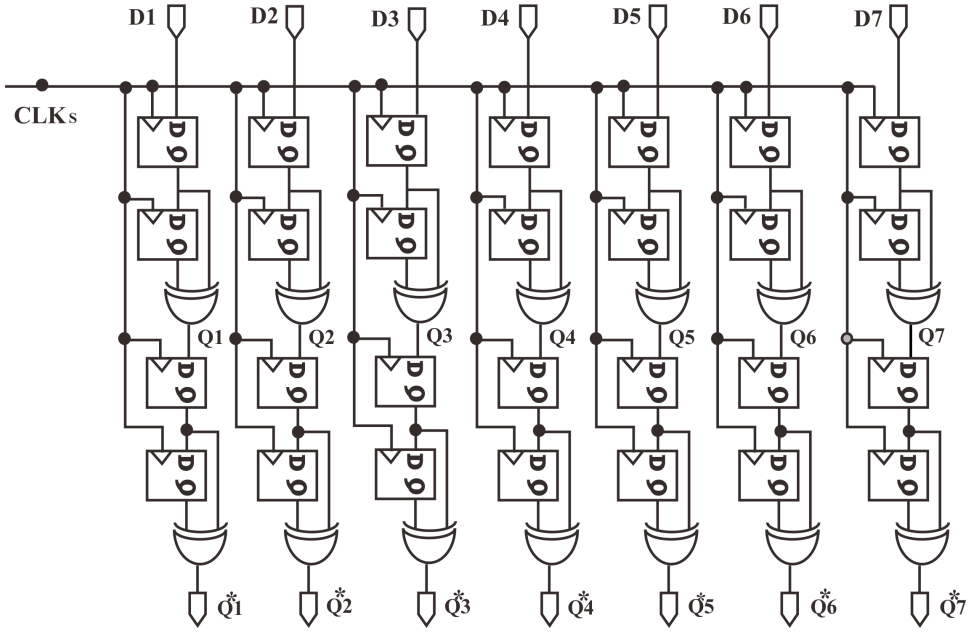


Figure 4.27: Implementation of a 2^{nd} Order Digital Differentiators.

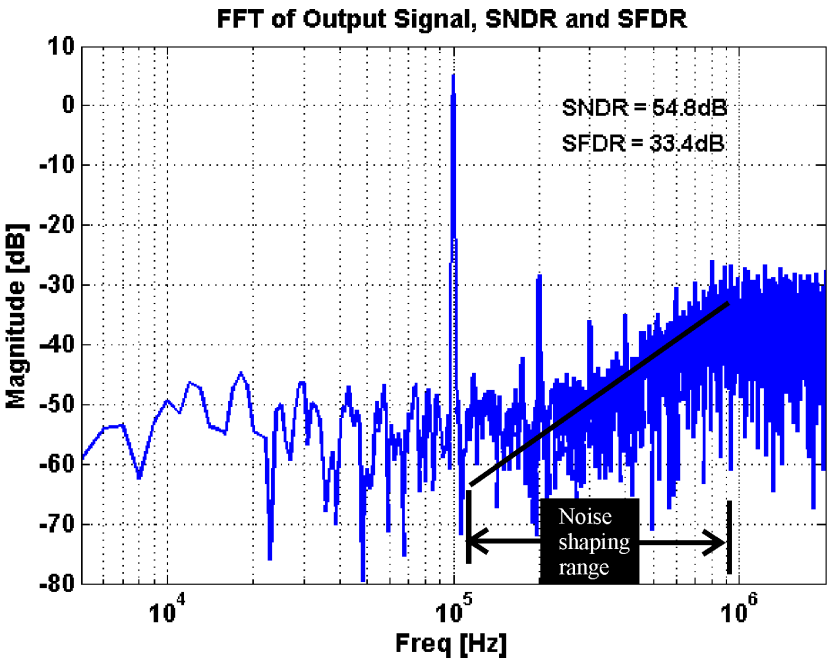


Figure 4.28: FFT of the Output Waveform for the Proposed 2^{nd} Order $\Delta\Sigma$ ADC.

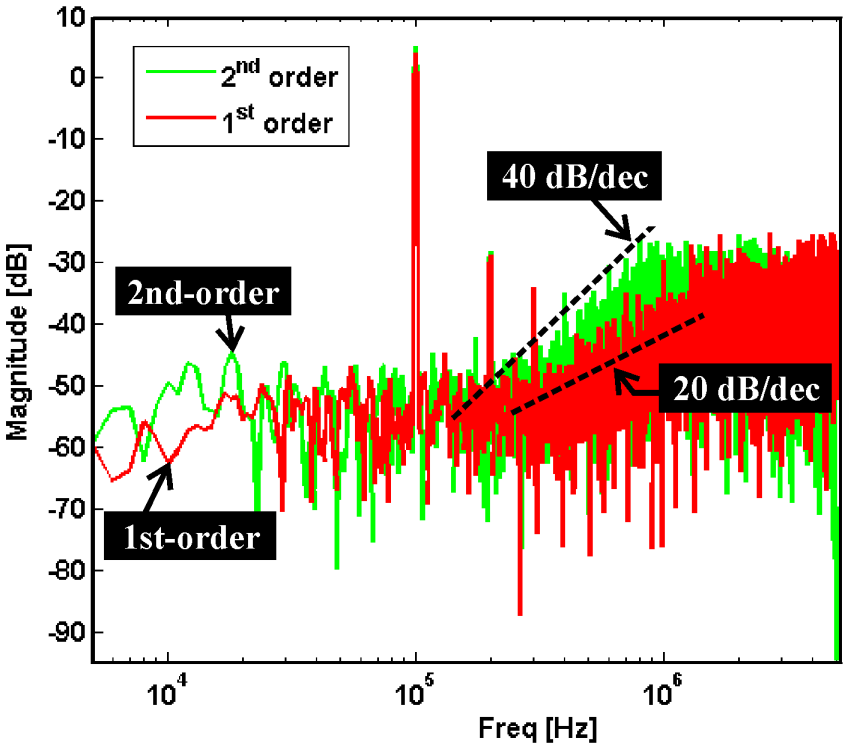


Figure 4.29: Comparison between the Proposed 1^{st} Order and 2^{nd} Order $\Delta\Sigma$ ADC.

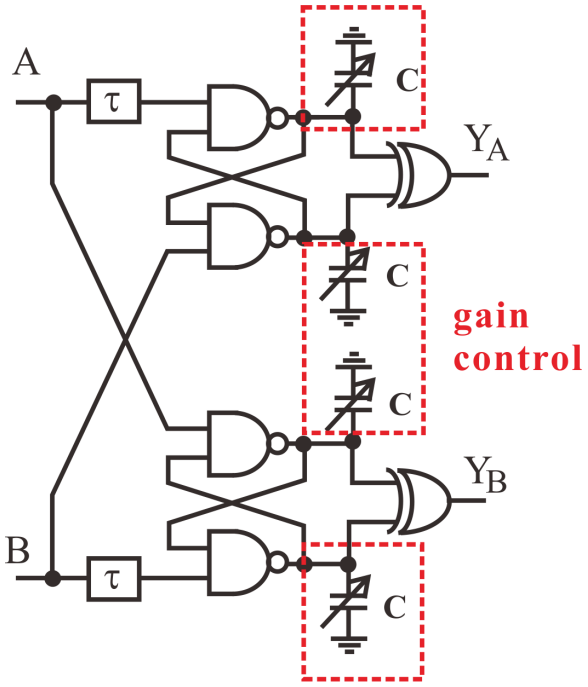


Figure 4.30: MULTEX Circuit for a Regenerative Time Amplifier.

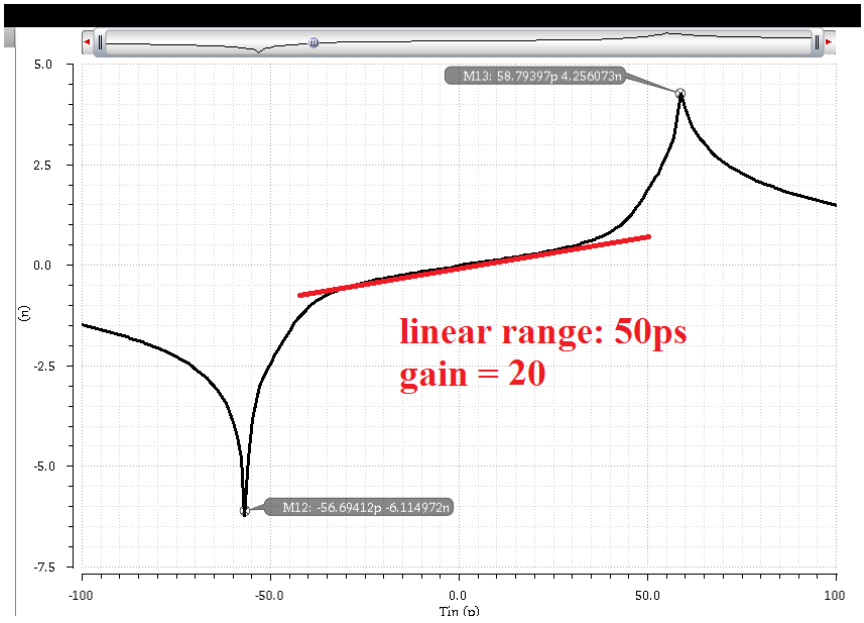


Figure 4.31: Time Amplifier Linear Range and Gain.

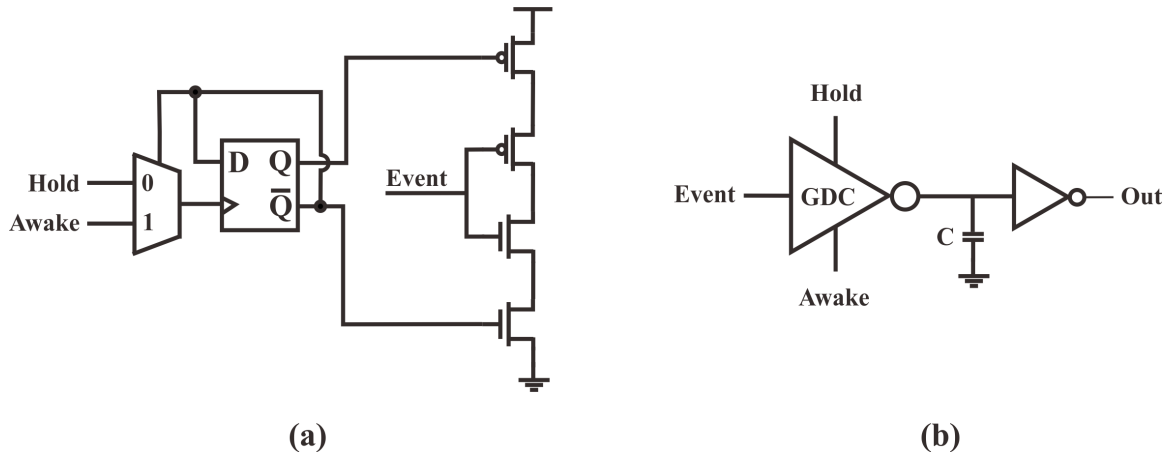


Figure 4.32: Implementation of a Gated Delay Cell.

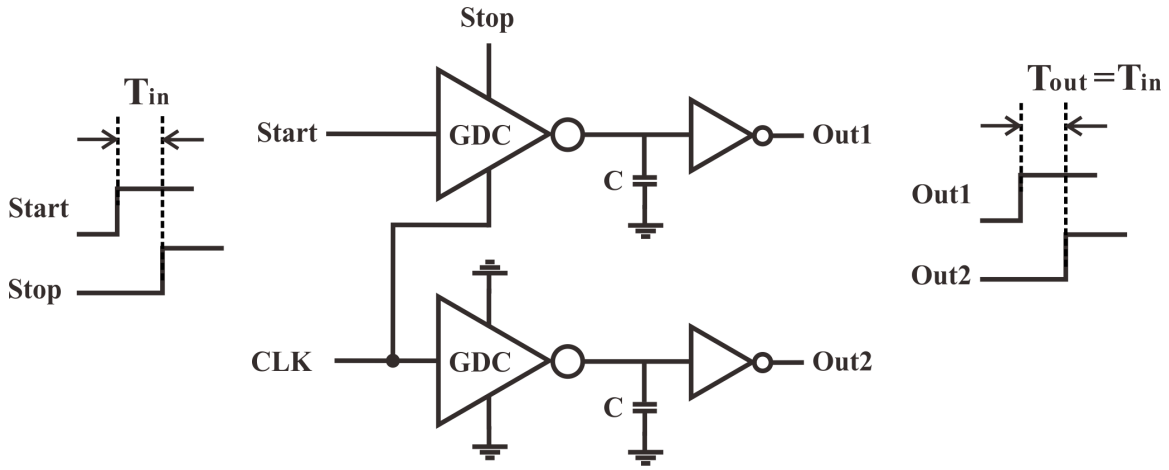


Figure 4.33: Implementation of a Time Register.

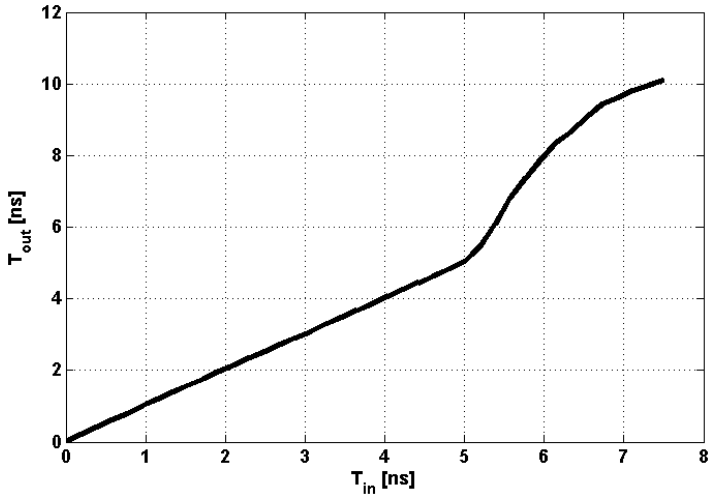


Figure 4.34: Performance of the Simulated Time Register.

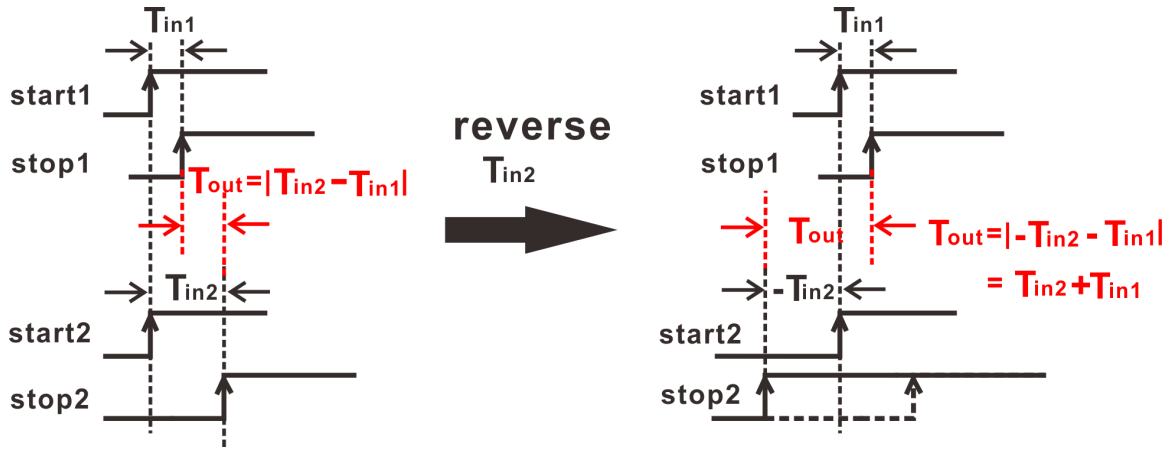


Figure 4.35: Using an Time Subtracter as an Adder.

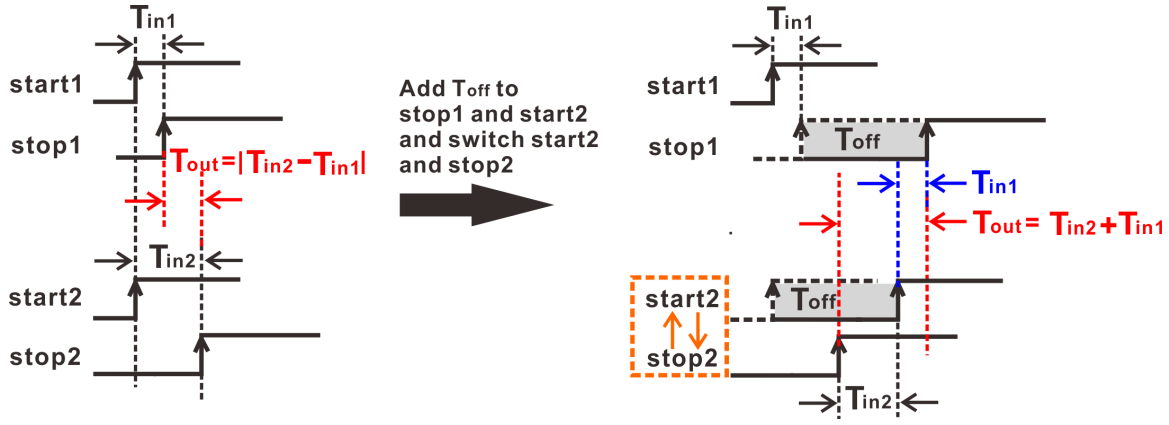


Figure 4.36: Using an Time Subtracter as an Adder by Adding T_{off} and Switching the inputs of T_{in2}.

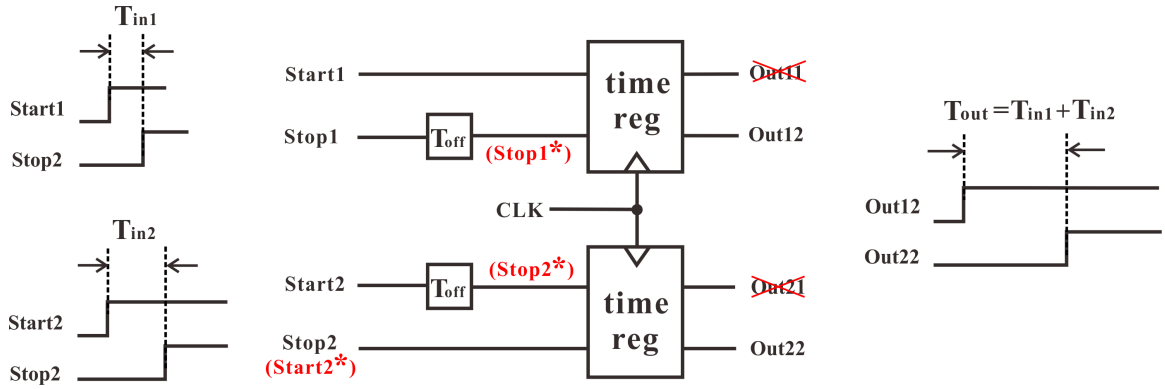
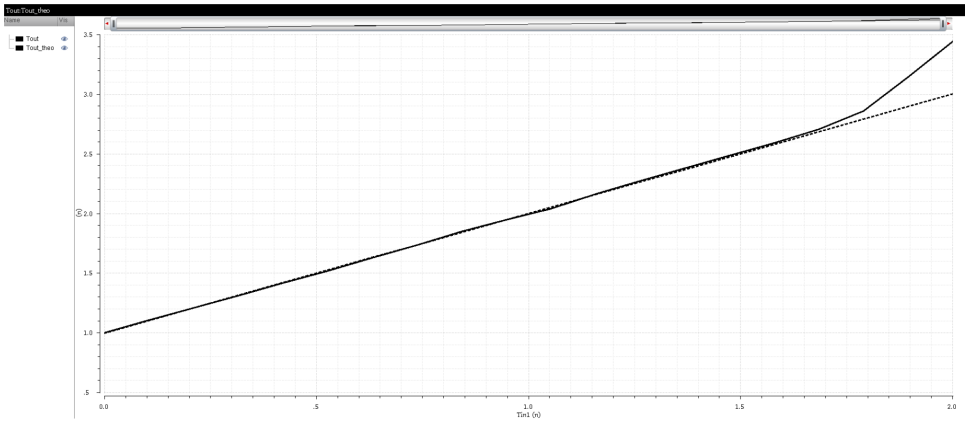


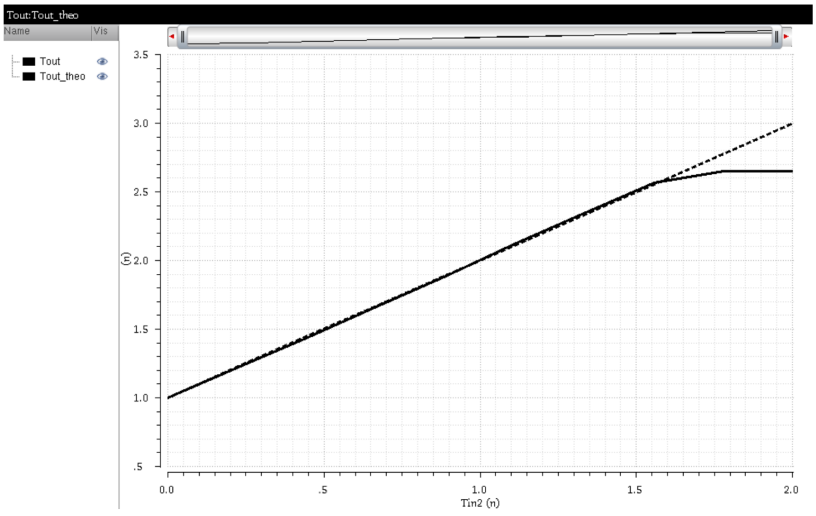
Figure 4.37: Implementation Details of the Time Adder.

4.7 Summary on Proposed Works

In this chapter, an all-digitally implemented 1^{st} and 2^{nd} order time-mode $\Delta\Sigma$ ADCs are proposed with implementation details provided. In addition to the proposed time-mode ADCs, other time-mode circuit components including a regenerative time amplifier, a time register and a time adder are also implemented and simulated. Those components are important building blocks for future designs.



(a)



(b)

Figure 4.38: Implementation Details of the Time Adder.

Chapter 5

Discussion and Conclusion

In this literature, an all-digital 1^{st} order and a 2^{nd} order time-mode $\Delta\Sigma$ ADCs with a 3-bit gated VCO quantizer have been presented. The time-mode $\Delta\Sigma$ ADCs also consist of a voltage-to-time integrator-based voltage-to-time converter, a 7-stage gated current-starved ring oscillator, and 7-stage digital differentiators. The all-digital implementation of the modulator allows their performances to scale well with technology so as to benefit from technology scaling. Implemented in an IBM 130nm 1.2 V CMOS technology, the 1^{st} order ADC demonstrates an SNDR of 45.5 dB over a 0.4 MHz bandwidth and consumes 1.1mW RMS power. The 2^{nd} order $\Delta\Sigma$ time-mode ADC provides a 54.8 dB SNDR over the same bandwidth and 40dB noise-shaping with power dissipation of 1.45 mW. The low SNDR is due to the absence of a high-gain loop filter to suppress in-band harmonics and large quantization noise due to 3-bit quantization. Quantization noise can be reduced should the GRO contains more stages, for example 31 stages (5-bit quantizer) [19].

It was observed in Fig.4.22 that harmonic tones are clearly visible in the spectrum of the ADC. In this section, we instigate the source of the nonlinearity of the proposed ADC that gives rise to th harmonic tones.

The GRO-based quantizer is quite linear. This is confirmed in Fig.**??**. Although the delay mismatch of the stages of the GRO gives rise to the nonlinearity of the quantizer, since only seven stages are used, the mismatch-induced nonlinearity of the GRO is rather mild. Further, since the GRO is located in the forward path, its nonlinearity is suppressed by the loop gain. As a result, the contribution of the nonlinearity of the GRO to the harmonic tones in the spectrum of the ADC is marginal.

The VTC integrator, PFD, and reference clock, together form a voltage-to-time converter that maps the input voltage to a time variable. Since the frequency of the VTC integrator of Fig.4.7 is controlled by v_{in} (neglect feedback), the linearity of VCDU, the only variable delay element in the VTC integrator, becomes critical. As the feedback is only applied to the load capacitor of the VCDU, the transconductor formed by M3 and M4 are located outside the feedback loop. Its nonlinearity therefore will not be suppressed by the loop gain.

If we assume that the output current of the transconductor, denoted by $i_{in}(t)$, is a pure sinusoid whose amplitude varies linearly with the input voltage $v_{in}(t)$, since $i_{in}(t)$ is sinusoidal and the threshold voltage of the static inverter remains unchanged, the relation between the amplitude of the $i_{in}(t)$ at a given frequency and the delay of the VCDU is intrinsically nonlinear. To illustrate this, consider Fig.5.1. Let the period of the pull-up clock be T_c and the frequency of the input signal be ω_{in}. Further, let the frequency of the input be much lower than that of the clock frequency. Consider the time interval $[nT_c, nT_c + Tc/2]$ where the load capacitor is discharged. The capacitor is fully charged during $[nT_c - T_c/2]$, i.e., $v_c(nT_c^-) = V_{DD}$, and then experiences a controlled discharge with discharging current $i_{in}(t) = I_{in}\cos(\omega_{in}t)$ in $0 \leq t \leq T_c/2$. It can be shown that the voltage of the capacitor is given by

$$v_c(t) = V_{DD} - \frac{I_{in}}{C}\int_{nT_c}^{nT_c+t} \cos(\omega_{in}t)dt. \tag{5.1}$$

Utilizing $v_c(nT_c^-) = V_{DD}$, we arrive at

$$v_c(t) = V_{DD} - \frac{2I_{in}}{\omega_{in}C}\cos\left(n\omega_{in}T_c + \frac{\omega_{in}t}{2}\right)\sin\left(\frac{\omega_{in}t}{2}\right). \tag{5.2}$$

where $0 \leq t \leq T_c/2$. To find out the time t^* at which $v_c(t)$ reaches the threshold voltage of the following static inverter, we let $v_c(t^*) = V_{DD}/2$ from which we obtain

$$\frac{V_{DD}}{2} = \frac{2I_{in}}{\omega_{in}C}\cos\left(n\omega_{in}T_c + \frac{\omega_{in}t^*}{2}\right)\sin\left(\frac{\omega_{in}t^*}{2}\right). \tag{5.3}$$

It becomes evident from (5.3) that a nonlinear relation between t^* and I_{in} exists. Note the preceding analysis does not include the effect of the nonlinearity of the transconductor formed by M3 and M4.

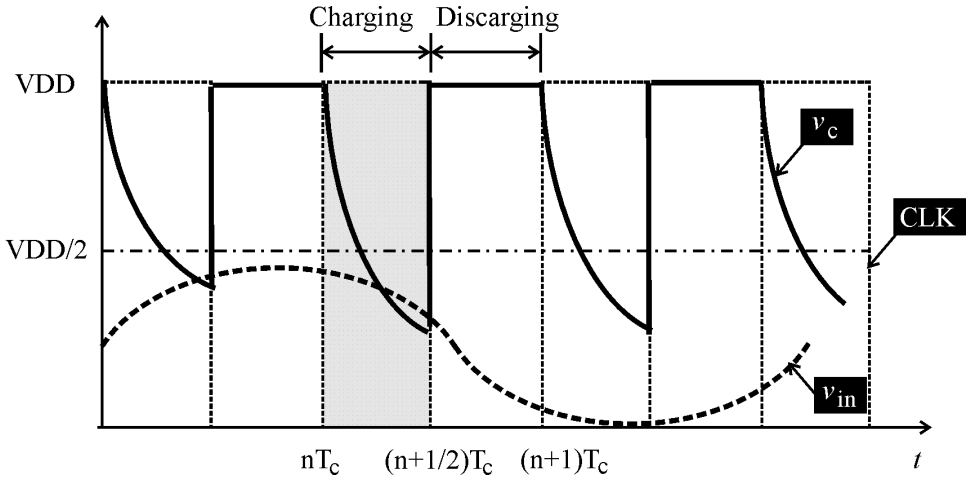


Figure 5.1: Operation of VCDU.

As explained in Section 4.3.5, the feedback path is formed by seven pull-up PMOS transistors that map the thermometer-coded output of the differentiators to the currents injected to the load capacitor of the VCDU. Since the PMOS transistors operate in an ON/OFF mode, when they are ON, their mode of operation is governed by the pinch-off condition, specifically, if $v_{SD} \leq V_{DD} - |V_{tp}|$, they are in triode and behave as resistors, otherwise, they are in saturation and behave as current sources. Since the gating voltage of the PMOS transistors is logic-0 to turn on the PMOS transistors, these transistors are in triode when ON. As a result, the relation between the pull-up time constant τ_{up} and the number of PMOS transistors that are ON is given by

$$\tau_{up} = \frac{R_{on}C}{n} \tag{5.4}$$

where $n = 1, 2, ..., 7$. Clearly the relation between τ_{up} and n is hyperbolic and nonlinear. It should be noted that the nonlinearity of the feedback path will not be suppressed by the loop gain and will make its way to the output of the ADC with no attenuation.

As compared with conventional $\Delta\Sigma$ modulators where only integrators and quantizers exist in the forward path, the deployment of differentiators in the forward path of the modulators, though improving read-out rate subsequently achieving a better OSR, is at the expense of canceling out the effect of the integrators so as to allow the input signal to pass though. For example, in [19], the desirable 1st-order noise-shaping obtained from using GRO is lost due to the deployment of the 1st-order differentiator. Should the differentiators be absent in the forward path, the order of the modulator would be increased by one. If one wants to implement a 3rd-order single-loop $\Delta\Sigma$ modulator using the proposed architecture by adding a time-mode integrator proposed in [104] between PFD and GRO in the forward path, a 3rd-order differentiator is needed in the forward path. It becomes evident that since GRO is a time-to-phase converter, a new phase readout mechanism that does not suffer from the latency of counter-based phase readout while avoiding differentiation-based frequency readout is critically needed. As pointed out in [20], frequency-based feedback obtained from differentiator-based readout hinders the harmonic suppression capability of $\Delta\Sigma$ modulators. In order to limit the phase of GRO to a small range so as to minimize the effect of the nonlinearity of GRO, phase-based feedback is preferred. This also signifies the importance of phase-based readout in achieving a better SNDR. While for conventional $\Delta\Sigma$ modulators, it is not a difficult task to achieve a large loop gain so as to provide better suppression of the effect of the nonlinearity of components in the forward path, this might not be trivial for all-digital time-mode $\Delta\Sigma$. Lastly, we have observed large harmonics in the spectrum of both modulators, arising from the nonlinearity of VCDU with its V/I converter located outside the feedback loop. It is highly desirable to have V/I conversion taken place inside the loop, specifically, the feedback signal should counteract the input voltage so that the signal fed to the V/I converter is limited to a small range so as to minimize the effect of its nonlinearity.

Chapter 6

Future Works

In order to suppress harmonic tones within the signal band and further improve SNDR without sacrificing the benefit of all-digital implementation, it is appealing to design a high-order digitally implemented time-mode loop filter. In [104], such a time-mode loop filer known as time accumulator has been proposed and applied in a $\Delta\Sigma$ TDC. In this chapter, a higher-order system witch employs such a time difference accumulator is introduced.

It is desirable to increase the order of the $\Delta\Sigma$ ADC by employ an time-difference accumulator loop filter as illustrated in Fig.6.1. It can be easily proved that the system in Fig.6.1 provides a 3^{rd} order noise-shaping. However, design of such a time-mode loop filter becomes challenging because unlike voltage or current, time has no physical representation. So a time-mode processing inside a time accumulator has to be accomplished with the aid of an intermediate quantity.

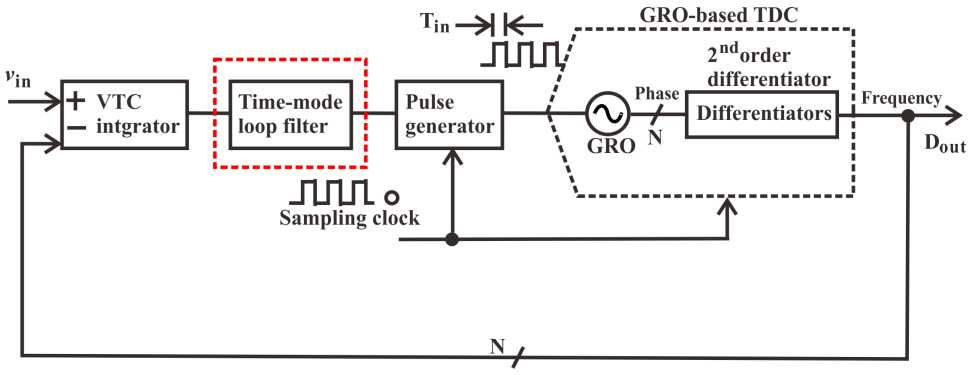


Figure 6.1: System Model of a 3^{rd} Order Time-Mode $\Delta\Sigma$ ADC.

Similar to a voltage-mode integrator, a time accumulation perform time-to-time integration (accumulation of a time difference variable over a time interval). A general block diagram of such circuit is shown in 6.2. The time accumulator operates by amplifying an input time difference variable, storing and delaying it, and then adding it to the next incoming time difference variable. The implementation of such a time accumulator requires a time amplifier, a time register which behaves as a $1 - Z^{-1}$ delay unit and a time adder which performs summation of two time difference variables.

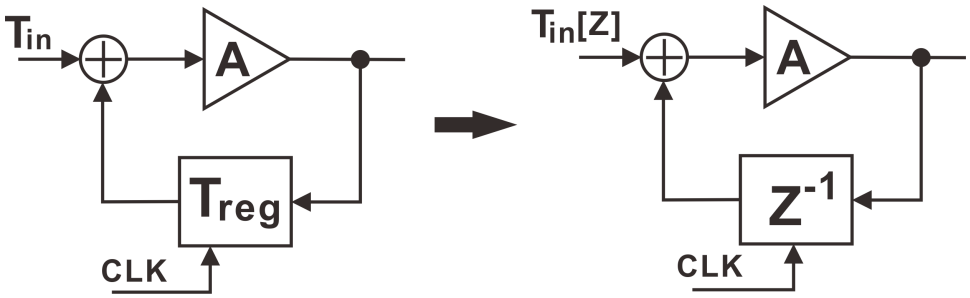


Figure 6.2: Implementation of a Time Accumulator

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