

**AN ISOLATED SOFT-SWITCHED DC-DC CONVERTER FOR INTERCONNECTION
OF MEDIUM- AND LOW-VOLTAGE DC GRIDS**

By

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Bachelor of Engineering, Azad University, Najafabad, 2011

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Author's Declaration

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Abstract

As the electric power grid increasingly hosts energy storage devices, renewable energy resources, plug-in hybrid and electric vehicles, and data centers, it is expected to benefit in the future from a multi-layer DC structure meshed within its legacy AC architecture. As such a multi-layer grid structure evolves, interconnection of DC grids with different voltage levels will become necessary. For such interconnections and for power-flow control, efficient isolated DC-DC converters are a key enabling technology. This thesis thus presents the results of an in-depth investigation into the operation, modulation, control, and performance assessment of a particular DC-DC converter configuration. The proposed DC-DC converter, which is based upon a hybrid combination of the conventional dual-active-bridge topology and the modular multi-level converter (MMC) configuration, is a potential candidate topology for interconnection of medium- and low-voltage DC grids. The thesis first introduces the circuit topology and presents the basics of operation and governing steady-state equations for the converter. Then, based on the developed mathematical model, it identifies a suitable modulation strategy for the converter bridges and submodules, as well as strategies for the regulation of the MMC submodule capacitor voltages and soft switching of the constituent semiconductor devices. The proposed converter topology offers significant benefits including galvanic isolation, utilization of the transformer's leakage inductance, soft switching for high-frequency operation, and bidirectional power flow capability. The validity of the mathematical model, effectiveness of the proposed modulation and control strategies, and the realization of soft switching are verified through off-line simulation of a detailed circuit model as well as experiments conducted on a 1-kW experimental setup.

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To My Family.

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CONVENTION FOR NOTATIONS

For clarity and consistency, the following are used in this thesis.

- Variables that are constant are represented using upper case characters (e.g., P and V_{dc1}).
- Variables that are varying are represented using lower case characters (e.g., v_{ac1} and i_{u1}).

LIST OF ABBREVIATIONS

DC	Direct Current
AC	Alternating Current
EMI	Electromagnetic Interference
HV	High Voltage
LVDC	Low-Voltage Direct Current
HVDC	High-Voltage Direct Current
MVDC	Medium-Voltage Direct Current
LV	Low Voltage
MMC	Modular Multilevel Converter
MV	Medium Voltage
TI	Texas Instruments
SM	Submodule
DAB	Dual Active Bridge
MF	Medium Frequency
ZCS	Zero Voltage Switching
ZVS	Zero Current Switching
SPS	Single Phase Shift
Si	Silicon
GaN	Gallium Nitride
QSW	Quasi Square Wave
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
PCB	Printed Circuit Board

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

Today's power grid is predominately based on Alternating Current (AC). As the grid is evolving and increasingly hosts energy storage devices, renewable energy resources, hybrid and electric vehicles, and data centers, the concept of direct current (DC) power systems is gaining traction [1]. Lower losses and higher power densities enabled by DC power transmission and distribution have sparked the implementation of high-voltage DC transmission (HVDC) systems as well as medium- and low-voltage DC (MVDC and LVDC) distribution systems [2].

DC interconnects are expected to play an important role in the future power grid as they offer advantages with respect to efficiency, power density, and control. Consequently, the landscape of the grid of future is envisioned to have a multi-layer DC structure meshed inside the AC grid, as illustrated in Fig. 1.1 [1].

As such a multi-layer grid structure evolves, interconnection of DC grids with different voltage levels will become necessary. Based on Fig. 1.1, possible scenarios of incorporating DC grids include:

- Interconnection of two HVDC systems. Since the existing HVDC systems are developed independently, the operating voltage can be different. Incorporating a mixture of HVDC grids with different voltage levels will be necessary [3, 4, 5, 6, 7, 8].
- Interconnection of HVDC and MVDC systems [4].
- Interconnection of MVDC and LVDC systems [9].

For the aforementioned interconnection scenarios and to enable power-flow control, DC-DC converters are a key enabling technology. Specifically, DC-DC converters for future DC networks need to meet the following requirements [4]:

- Bidirectional power-flow control capability.
- Galvanic isolation, which is often required for flexibility of system reconfiguration and meeting safety standards.
- High efficiency.
- High/medium voltage/power rating.

- High reliability and lifetime.

Before getting into the details of this thesis, it is important to understand the state-of-the-art in regards to this particular area. Hence, the following section will present a literature review of the concepts and topics that are relevant to this thesis.

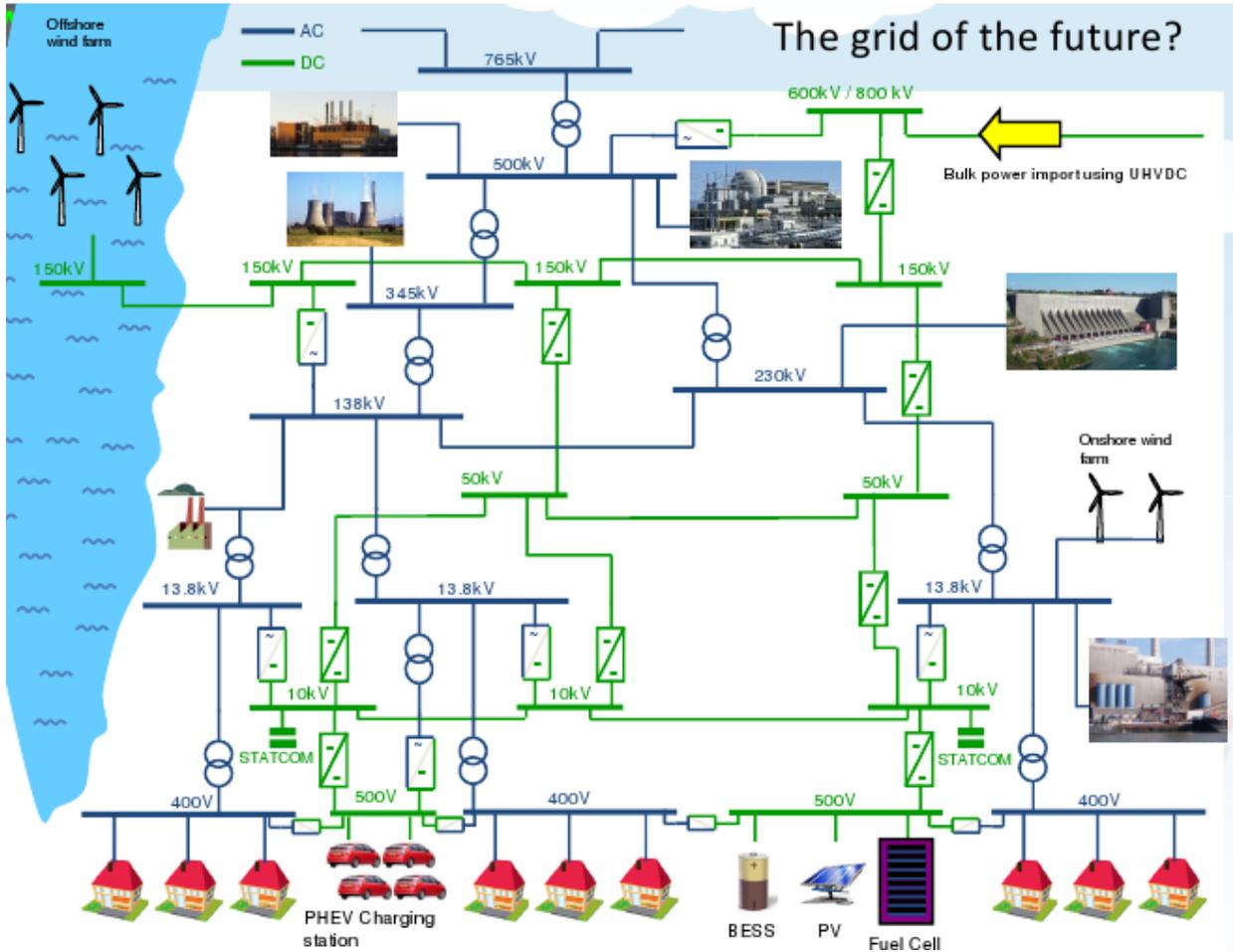


Figure 1.1: An overview of the envisioned multi-level future grid [1].

1.2 Literature Review Pertinent to Thesis Objectives

In the state-of-the-art bidirectional and isolated DC-DC converters, electrical isolation between the HV and LV sides is provided by an intermediate medium-frequency (MF) transformer. The dual-active-bridge (DAB) DC-DC converter, originally proposed in [10], has become one of the most commonly used bidirectional converter topologies that is well studied in the literature. As shown in Fig. 1.2, the DAB converter, classically employs two active-bridges that are interconnected by a MF transformer. Depending on the design criteria, the DAB converter can be configured using

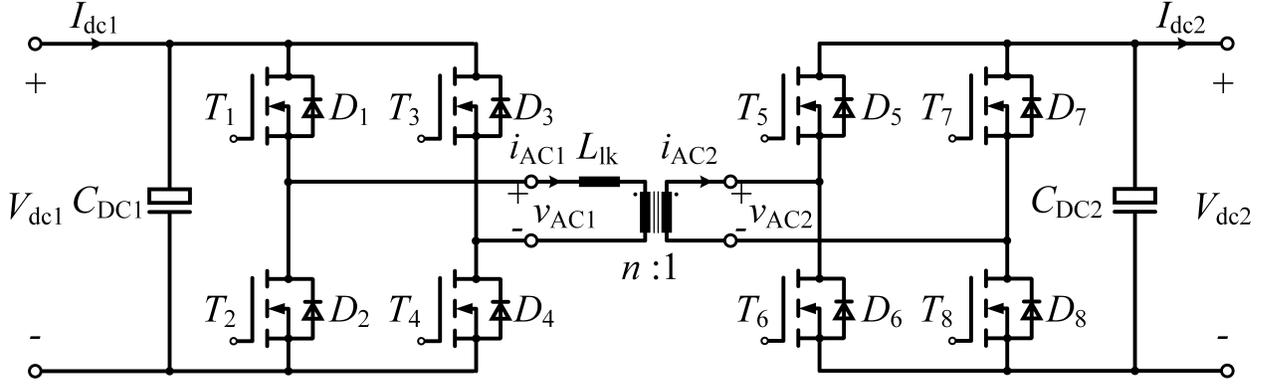


Figure 1.2: Circuit diagram of a single-phase DAB converter.

single-phase bridges [11, 10, 12, 13, 14, 15] or three-phase bridges [10, 16, 17, 18, 19, 20, 21]. In the single-phase DAB converter shown in Fig. 1.2, the leakage inductance of the intermediate transformer is utilized as the energy transferring element and limits the maximum power flow [10]. In the three-phase version, a three-phase transformer is used to interconnect the primary and secondary active bridges. The switches in the active bridges can be switched at zero voltage or zero current, within a certain operating range. Various control strategies are proposed to extend the soft-switching range and minimize the transformer current of the DAB converter [22, 23, 24, 25, 26, 11]. Moreover, a high-voltage conversion ratio for step-up or step-down operation can be achieved by selecting the turns ratio of the transformer.

The power throughput of a DAB converter is controlled by the voltage across its transformer leakage inductance. For modulation and control of a DAB converter, a number of modulation strategies have been proposed in the past [27, 28, 29, 30, 31, 32, 33, 11]. Among them, the single phase-shift (SPS) control based modulation is the most widely used one. With reference to Fig. 1.2, in the SPS control, the switches T_1 - T_4 and T_5 - T_8 receive square-wave gate signals with 50% duty ratio. In the SPS control, the cross-connected switch pairs in each bridge are switched in tandem to generate a square wave voltage with 50% duty ratio at the respective winding of the transformer. Then, by adjusting the phase shift, φ , between the voltages at the primary and secondary sides, the voltage across the leakage inductance of the transformer is controlled, which, in turn, controls the power-flow direction and magnitude.

Research in the area of DAB-based isolated bidirectional DC-DC converters has gained momentum in recent years due to the advancements in the fields of electrified transportation, integration of energy storage devices, and other applications. The main focus of the research has been to achieve high power density, higher efficiency, superior dynamic performance, and improved reliability of the DAB-based converters [34, 11, 35, 36, 37, 38, 39].

The DAB converter offers very attractive features in terms of low device and component

stresses, small filter components, low switching losses by virtue of zero voltage switching (ZVS), high power density and high efficiency, bidirectional power flow, buck-boost operation and low sensitivity to system parasitics. Nevertheless, it has the two following disadvantages that limit its usage in high-voltage/power applications [40]:

- The active bridges need to be rated for the full converter power and voltage. Consequently, for high-voltage/power applications, series and/or parallel connection of semiconductor switches are typically necessary for meeting the voltage and current requirements. This will consequently produce high dv/dt upon transformer insulation.
- For high-voltage applications, the parasitic components of the insulation transformer become more pronounced at higher voltages, rendering transformer design a challenging task [41].

To employ the DAB converter in high-voltage/power applications, the idea of connecting multiple DAB converter units in series and/or parallel to increase the voltage and current ratings without using series-connected semiconductor switches has been proposed [42, 43, 44]. An input-series-output-parallel (ISOP) DAB converter is proposed in [17, 45, 9], in which, as shown in Fig. 1.3, identical DAB modules are connected in series and parallel. The modular design allows easier scalability of the system. Moreover, improved system reliability can be achieved by inserting redundant modules [44]. However, the main drawback of the series/parallel connection of DAB converters is that a large number of low-power transformers need to be isolated from the high-voltage DC side. This high insulation requirement consequently leads to high cost and volume [46].

With the emergence of the DC-AC modular multilevel converter (MMC) [47], in which a number of identical half-bridge or full-bridge submodules (SMs) are switched to generate a multilevel AC voltage waveform, the concept of using multiple low-voltage SMs to replace the switches in the conventional DAB converter has gained traction [48, 49, 50, 27]. A MMC-based DAB converter is a potential candidate to interface MVDC/HVDC grids. In contrast to the ISOP DAB converter, the DAB converter based on the MMC concept does not require multiple low-power transformers. Instead, a multilevel voltage waveform is generated across the transformer winding. The salient features of the MMC are:

- It is fully modular and scalable by virtue of using identical low-voltage SMs. High-voltage ratings can thus be easily achieved by series connection of a large number of SMs.
- It features low Electromagnetic Interference (EMI) due to the low dv/dt .
- It offers high reliability by employing redundant SMs.

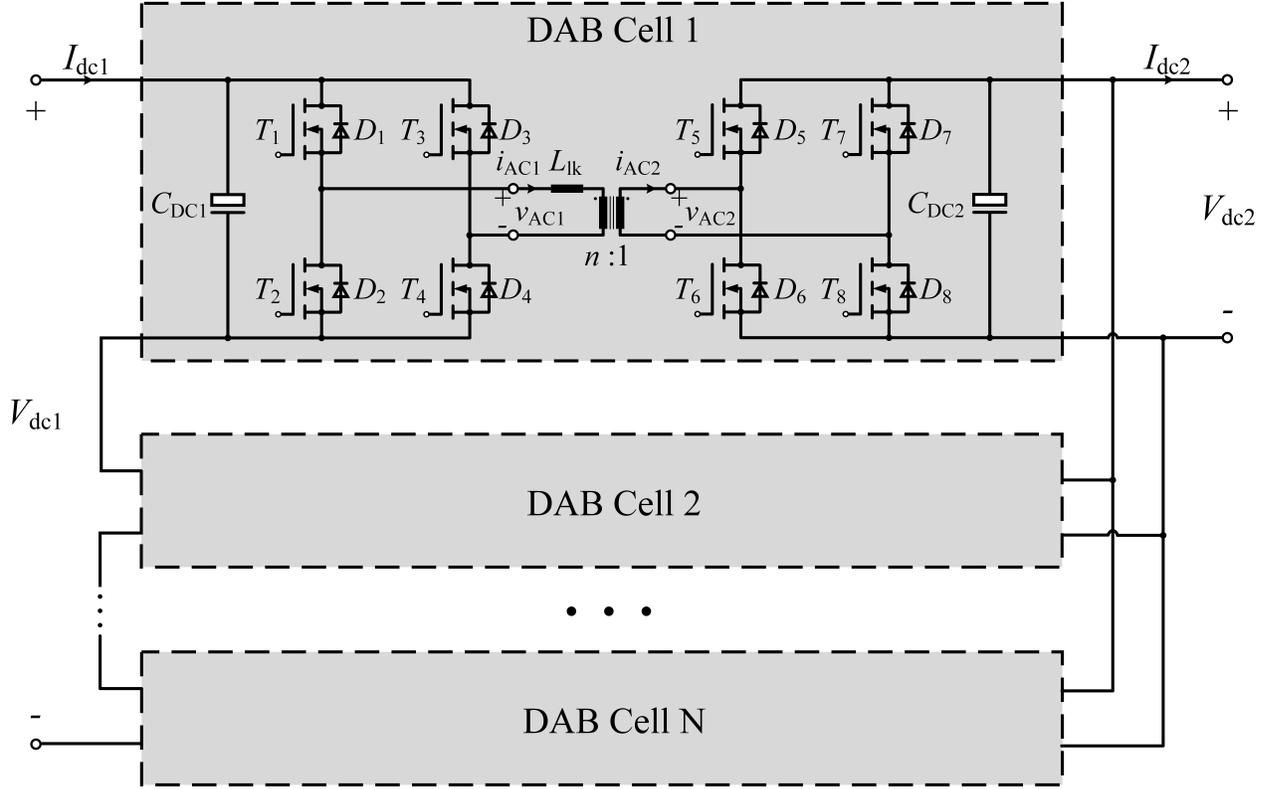


Figure 1.3: Circuit diagram of an ISOP DAB converter.

- It avoids series connection of semiconductor switches.

However, when a DC-DC converter is targeted for interfacing MVDC and LVDC grids, i.e., it is to serve as the DC-DC converters at the lowest layer of the grid in Fig. 1.1, the use of two DC-AC MMC stages in a DAB configuration results in poor utilization of total installed SM ratings on the LVDC side, thereby increasing the cost, volume and power losses [51, 50]. Furthermore, as of now, the MMC-based DAB converter topology has been realized by Silicon (Si) semiconductor devices by which an increase in the switching frequency does not necessarily result in a better performance in terms of efficiency and power density.

With the significant reduction in the footprint of power converters realized based on Gallium Nitride (GaN) semiconductor devices, topologies that require a larger number of semiconductor devices such as switched-capacitor and multilevel converters have become attractive [52, 53, 54, 55, 56, 57, 58, 59, 60]. Due to low switching energy of GaN devices, much higher switching frequencies, compared to Si devices, can be achieved without prohibitive switching power losses. As a result, reduced passive component size, which is the main barrier in the way of high power densities can be achieved.

Having illustrated a clear picture of the work done thus far, the following section will introduce the objectives of this thesis.

1.3 Thesis Objectives

The main objective of this work is to develop and investigate the feasibility of a DC-DC converter topology which fulfills the requirements specified in Section 1.2, for interfacing MVDC and LVDC grids. Furthermore, the converter topology and its modulation strategy are optimized for meeting a target efficiency more than 96%, within reasonable input and output voltage ranges and reasonable power ranges. The thesis describes the analysis, modulation, control, and performance assessment of a single-stage isolated DC-DC converter combining the DAB power stage and the MMC. The converter topology offers significant benefits including transformer isolation with leakage inductance incorporated in circuit operation, soft-switching capability, and bidirectional power flow. ZVS of the devices of the MMC on the primary-side bridge and the full-bridge circuit on the secondary-side bridge are achieved, which are particularly important for high efficiency.

Motivated by the possibility of higher-frequency switching without efficiency penalties, and the resulting transformer size reduction, the use of GaN devices is considered in the design of the converter of this thesis. The GaN device characteristics allow for faster turn on/off of the devices, and shorten the intervals required to achieve ZVS, thus allowing for increased switching frequencies. This subsequently leads to improved efficiency and smaller converter footprint. Moreover, it is expected that the concepts presented in this thesis should be verifiable by a practical system, and so a secondary objective is to present a fully functional converter that operates based on the theory presented in this thesis.

1.4 Thesis Structure

Including this chapter, there are five chapters in this thesis. This chapter identified the state-of-the-art isolated DC-DC converters suited for interfacing MVDC and LVDC grids.

In Chapter 2, the topology and basics of operation, modulation, and control of the developed converter are introduced, explored, and presented in details.

In the third chapter, the DC-DC converter presented in Chapter 2 will be simulated using the MATLAB/Simulink software. The simulation will subject the converter to several different operating conditions in order to test and validate the proposed theory of Chapter 2.

Experimental results are provided in Chapter 4 to (i) verify the developed converter topology and (ii) substantiate the performance of the proposed modulation and control strategy.

Finally, Chapter 5 summarizes the obtained results and concludes this work. Furthermore, Chapter 5 presents an outlook regarding future research in the field of the proposed converter.

In addition, the main body of the thesis will be followed by two appendices, which will present details relating to the experimental setup including the hardware used, and the details related to the control platform.

The Appendices include:

- Information regarding the practical implementation of the proposed modulation strategy (Appendix A).
- Details on the converter design (Appendix B).

CHAPTER 2

THEORETICAL ANALYSIS, MODULATION AND CONTROL OF THE PROPOSED DC-DC CONVERTER

In this chapter, the proposed converter is introduced and its principles of operation are discussed in details. Then, the mathematical model of the converter along with its modulation and steady-state characteristics for a general case, i.e., hybrid combination of a general $(N + 1)$ -level MMC stage with the conventional DAB converter stage will be presented. The ZVS operation of the converter as well as the conditions under which the ZVS is achieved are analyzed and investigated. To ensure proper operation of the converter and guarantee SM capacitor voltage balancing of the MMC stage, a balancing strategy is also proposed. Finally, a specific case study, i.e., when the MMC stage is a 5-level one will be presented in order to set the stage for the following chapters.

2.1 Basics of Operation

The circuit diagram of the proposed topology is shown in Fig. 2.1. The converter topology is comprised of a full-bridge MMC on the HV side and a full-bridge converter on the LV side, which are connected to a MF transformer. The MMC-based bridge is comprised of two legs in which each leg consists of two arms, i.e., an upper arm and a lower arm. Each arm is built based upon series connection of N identical SMs and an arm inductor L_{arm} . Each SM of the MMC on the HV side of Fig. 2.1 consists of a half-bridge circuit where its output voltage (i.e., v_{SM}) is either equal to its capacitor voltage v_{CSM} or zero, depending on the switching states of the complementary switches T_1 and T_2 . The switching states and their corresponding resultant voltages at the output of each SM are listed in Table 2.1. Assuming that the SM capacitor voltages are balanced through a capacitor voltage balancing scheme, the voltages of SM capacitors on the HV side are equal to V_{dc1}/N , where V_{dc1} is the HV side input DC voltage.

To transfer power between the HV and LV sides, time varying voltages $v_{prim}(t)$ and $v_{ac2}(t)$ are generated by the MMC and full-bridge conversion stages, respectively. To simplify the analysis of the converter, the voltage sources on the HV and LV sides can be replaced by the respective

Table 2.1: Switching states of a SM of Fig. 2.1.

State	T_1	T_2	v_{SM}
1	ON	OFF	v_{CSM}
2	OFF	ON	0

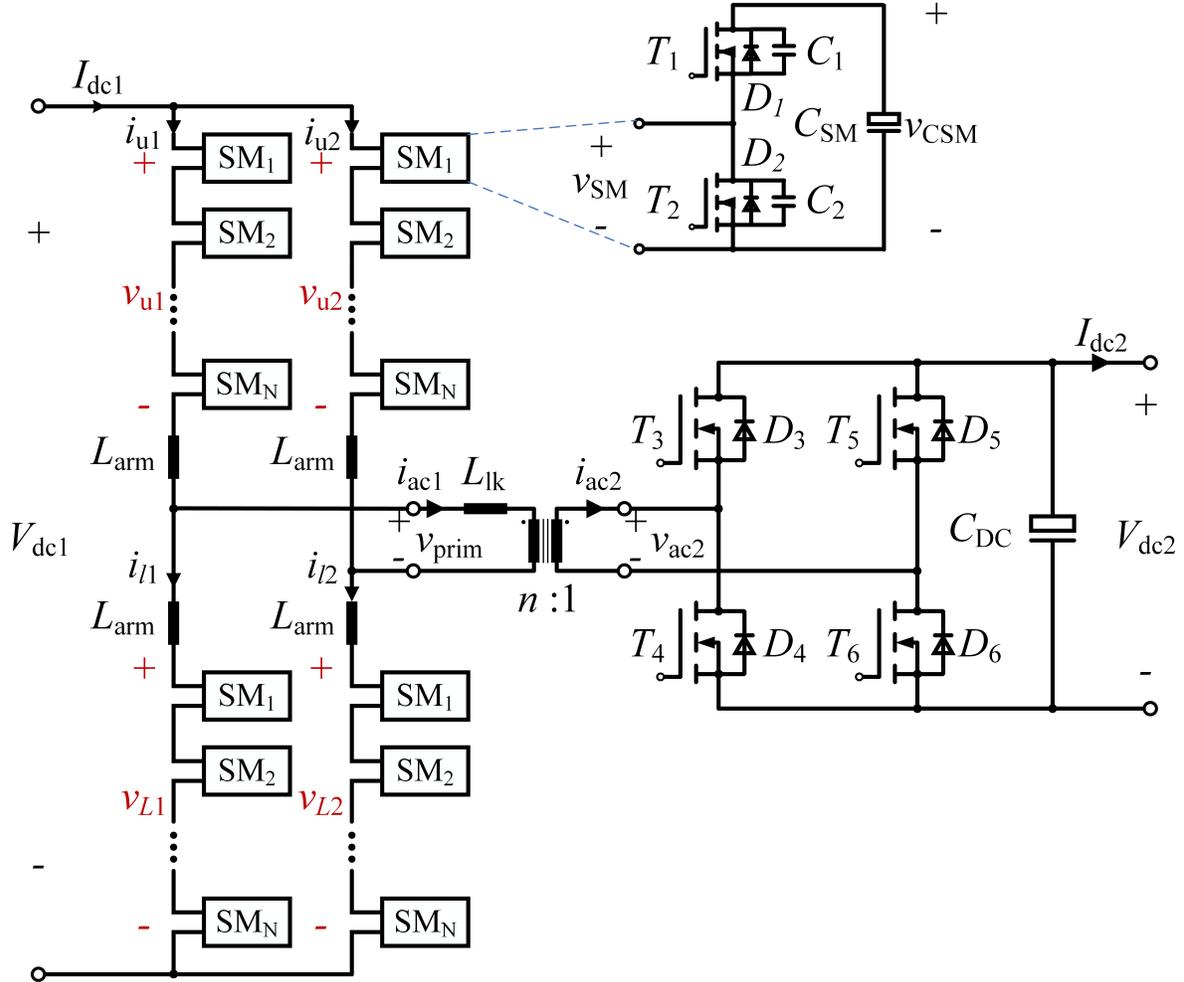


Figure 2.1: Circuit diagram of the converter.

voltage sources $v_{prim}(t)$ and $v_{ac2}(t)$.

For the sake of simplicity in the analysis, the following assumptions are made:

- The power losses are neglected.
- The transformer magnetizing inductance and parasitic capacitances (e.g., transformer coupling capacitance between LV and HV sides) are neglected.
- All LV-side quantities are referred to the HV side.
- The input and output voltages V_{dc1} and V_{dc2} are considered to be constant.

2.1.1 Modulation Method

For the modulation of the half-bridge circuit on the LV side, the switching states for T_3 , T_4 , T_5 , and T_6 are generated such that $v_{ac2}(t)$ is a square waveform with voltage levels V_{dc2} and $-V_{dc2}$.

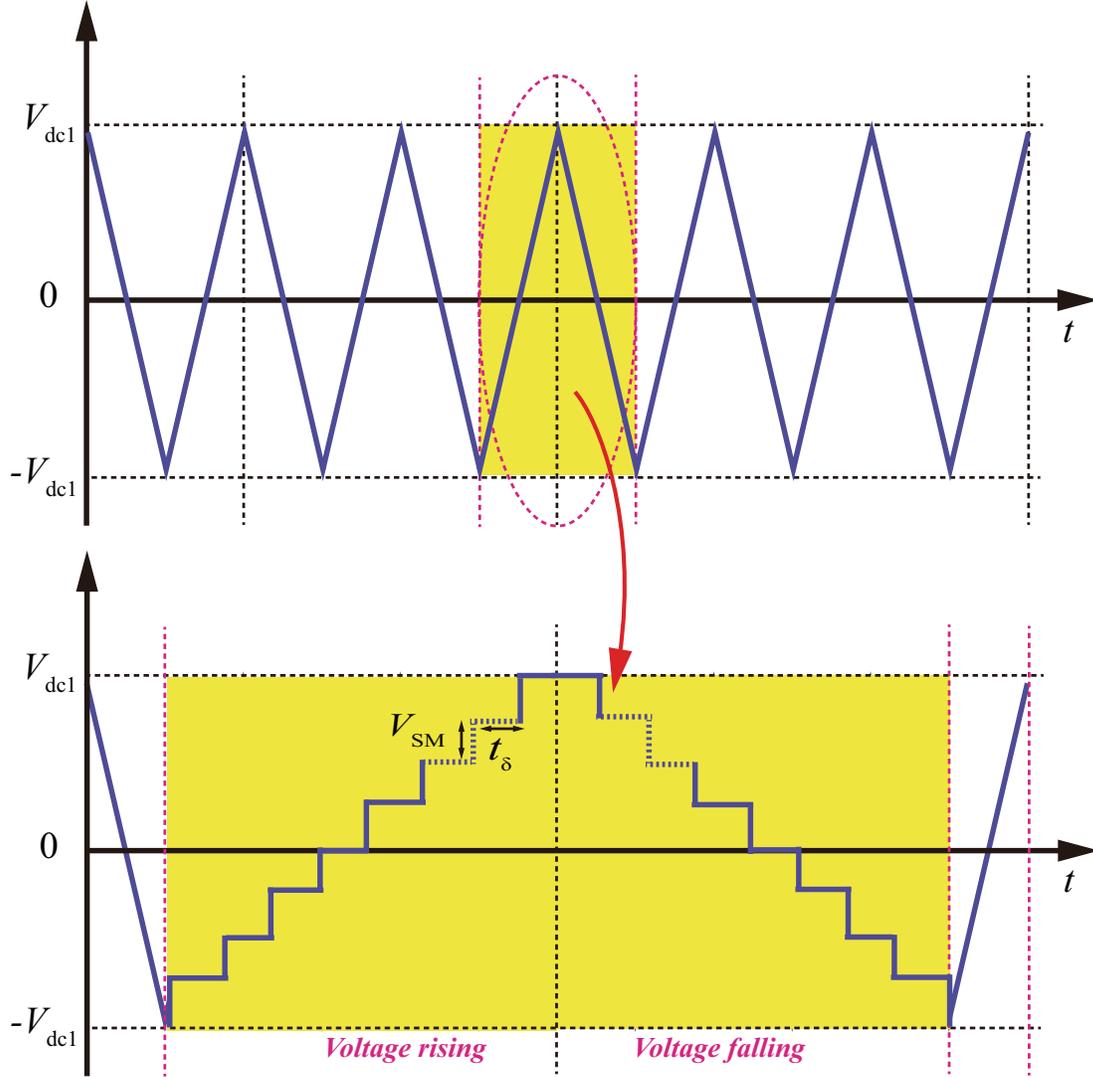


Figure 2.2: Modulation waveform of v_{prim} when using the triangular modulation scheme.

For the modulation of the MMC side, there are several options. The simplest option is similar to the modulation of the LV side, i.e., to generate a square waveform at the HV-side terminals of the transformer. In this modulation, all SMs on the diagonal arms of the two legs are simultaneously inserted or bypassed in such a way that $v_{prim}(t)$ equals V_{dc1} or $-V_{dc1}$. However, the resultant large dv/dt at the rising and falling edges of $v_{prim}(t)$ lead to issues such as destruction of transformer insulation and increased EMI. The second option is to insert or bypass the SMs such that $v_{prim}(t)$ approximates a triangular or a sinusoidal waveform, as shown in Figs. 2.2 and 2.3, respectively. However, these schemes are typically used when a large number of SMs are involved.

The other alternative is based on the trapezoidal or quasi-square-wave (QSW) modulation for the synthesis of $v_{prim}(t)$ as shown in Fig. 2.4. As shown in Fig. 2.5, based on the QSW modulation, the arm voltages v_{u1} , v_{l1} , v_{u2} , and v_{l2} are QSWs with their voltage rising and falling transitions

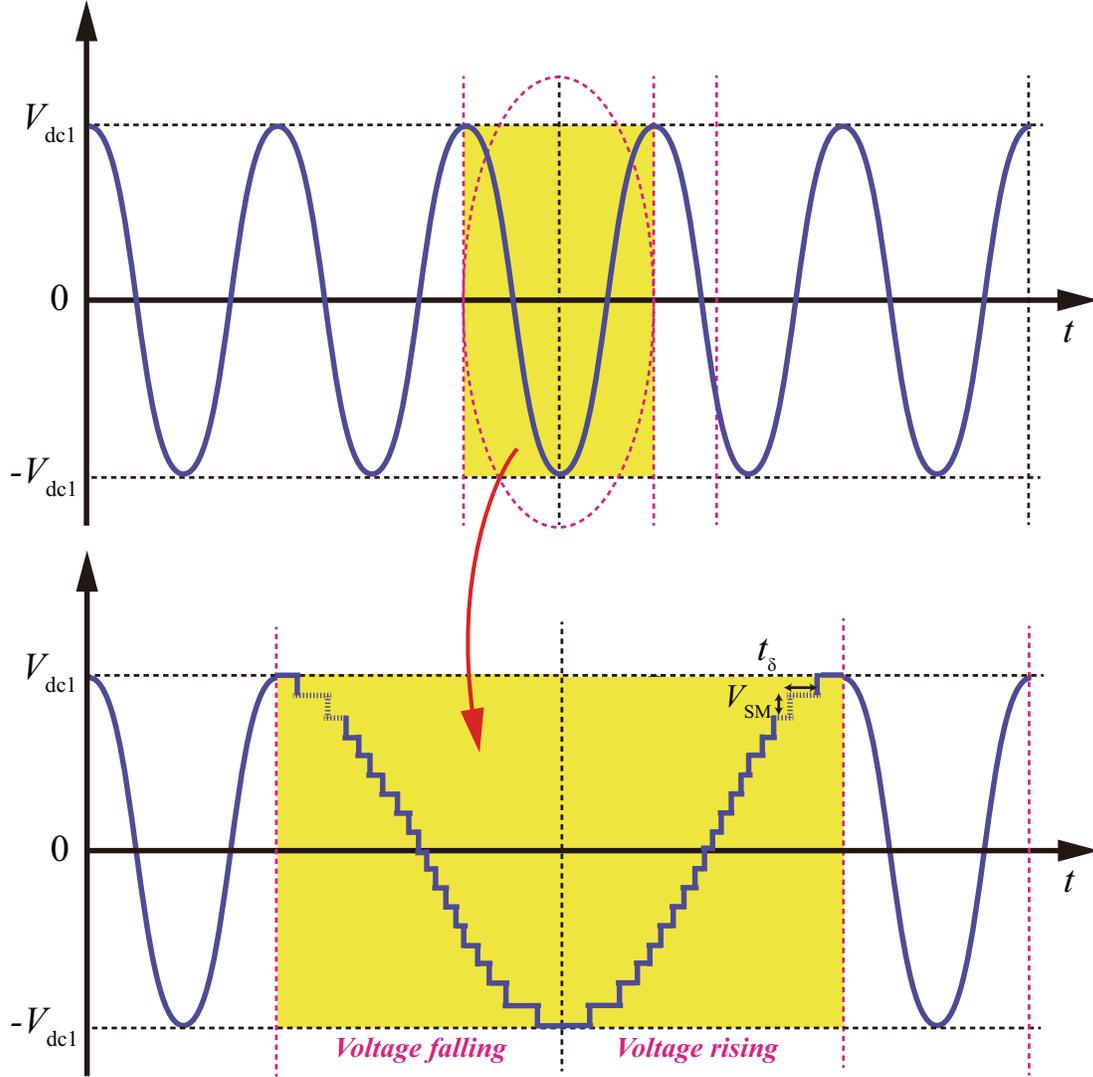


Figure 2.3: Modulation waveform of v_{prim} when using the sinusoidal modulation scheme.

intentionally arranged to be shaped in a staircase manner. During the voltage rising or falling transitions of either v_{u1} , v_{l1} , v_{u2} , or v_{l2} , SMs are inserted or bypassed one by one. Consequently, the voltage step sizes are limited to one SM capacitor voltage, i.e., V_{dc1}/N , for a duration of t_δ , thereby reducing the dv/dt of v_{u1} , v_{l1} , v_{u2} , and v_{l2} . This in turn reduces the dv/dt of $v_{prim}(t)$. It should be noted that the high- and low-level values of $v_{prim}(t)$ are V_{dc1} and $-V_{dc1}$, respectively, whereas, the high-level values of v_{u1} , v_{l1} , v_{u2} , or v_{l2} can be controlled to be equal to or lower than V_{dc1} . Similarly, their low-level values can be controlled to be equal to or higher than $-V_{dc1}$.

The arm voltages in Fig. 2.5 consist of a DC component and an AC component, and can be

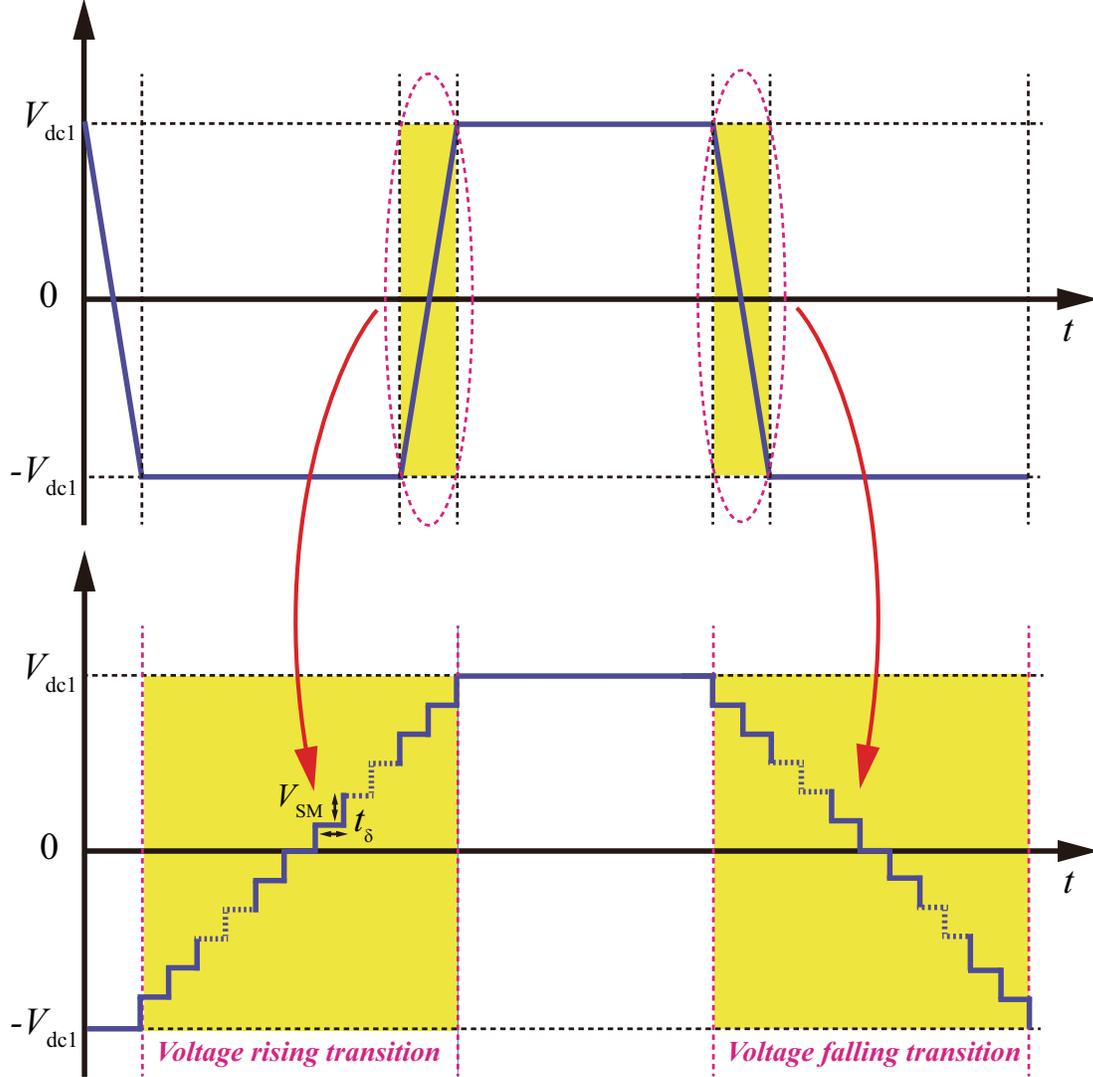


Figure 2.4: Modulation waveform of v_{prim} when using the QSW modulation scheme.

expressed by:

$$\begin{cases} v_{u1} = -v_{ac}^{arm} + \frac{V_{dc1}}{2}, \\ v_{l1} = v_{ac}^{arm} + \frac{V_{dc1}}{2}, \\ v_{u2} = v_{ac}^{arm} + \frac{V_{dc1}}{2}, \\ v_{l2} = -v_{ac}^{arm} + \frac{V_{dc1}}{2}, \end{cases} \quad (2.1)$$

where v_{ac}^{arm} represents that AC component of the arm voltages. As shown in Fig. 2.5, the arm voltages of each leg have the same DC component while their AC components are 180° out of phase.

The relationship between the upper and lower arm voltages of both legs in the converter of

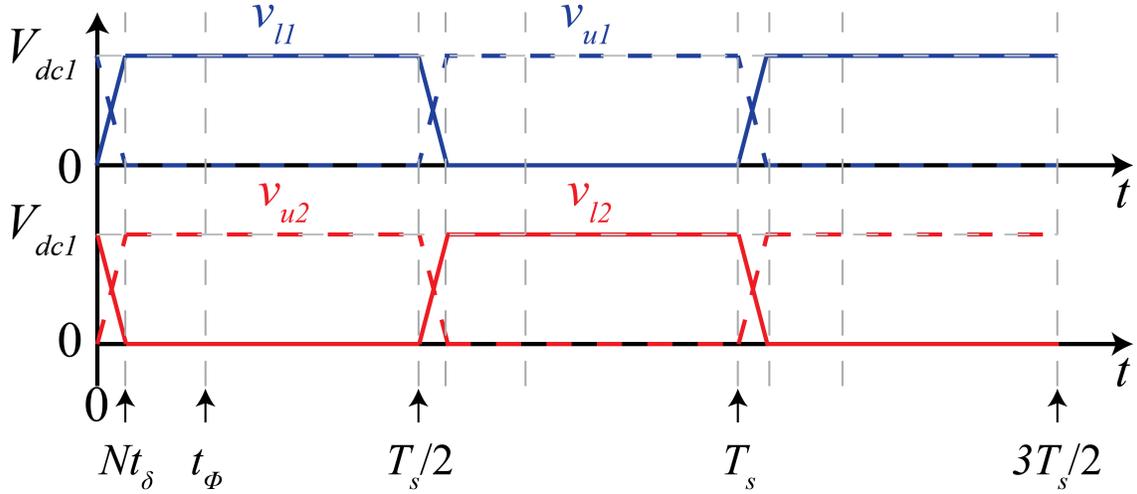


Figure 2.5: Typical arm voltage waveforms of the MMC under the QSW modulation.

Fig. 2.1, based on the QSW modulation, can be expressed by:

$$\begin{cases} v_{u1} = -v_{prim} - v_{l2} - L_{arm}\left(\frac{di_{u1}}{dt} + \frac{di_{l2}}{dt}\right) + V_{dc1}, \\ v_{l1} = v_{prim} - v_{u2} - L_{arm}\left(\frac{di_{l1}}{dt} + \frac{di_{u2}}{dt}\right) + V_{dc1}, \\ v_{u1} + v_{l1} = V_{dc1} + L_{arm}\left(\frac{di_{u1}}{dt} + \frac{di_{l1}}{dt}\right), \\ v_{u2} + v_{l2} = V_{dc1} + L_{arm}\left(\frac{di_{u2}}{dt} + \frac{di_{l2}}{dt}\right), \end{cases} \quad (2.2)$$

where i_{u1} , i_{l1} , i_{u2} , and i_{l2} represent the upper and lower arm currents of the two phase legs, respectively.

Similar to the conventional DC-AC MMC, the AC current i_{ac1} is distributed equally between the upper and lower arms of each leg. The current of each arm contains a circulating current component, i.e., i_{circ} . The current of each arm is expressed by:

$$\begin{cases} i_{u1} = \frac{I_{dc1}}{2} + \frac{i_{ac1}}{2} + i_{circ}, \\ i_{l1} = \frac{I_{dc1}}{2} - \frac{i_{ac1}}{2} + i_{circ}, \\ i_{u2} = \frac{I_{dc1}}{2} - \frac{i_{ac1}}{2} + i_{circ}, \\ i_{l2} = \frac{I_{dc1}}{2} + \frac{i_{ac1}}{2} + i_{circ}, \end{cases} \quad (2.3)$$

where i_{circ} represents the circulating current.

Under the QSW modulation, the power flow can be controlled based on the most common modulation and control principle for a DAB converter, i.e., the so called phase shift modulation, in which the primary and secondary sides operate with a constant switching frequency and 50% duty cycles. The transferred power is solely controlled by varying the phase shift φ between $v_{prim}(t)$ and $v_{ac2}(t)$. During steady-state operation, the voltages $v_{prim}(t)$ and $v_{ac2}(t)$ and the inductor current repeat every half-cycle with reversed signs.

2.1.2 Equivalent Circuit of the Converter and Power Analysis

The equivalent circuit of the converter operating based on the QSW method can be represented by the circuit shown in Fig. 2.6(a), which is derived based on the governing equations (2.1) and (2.2). By eliminating the DC components in the equivalent circuit of Fig. 2.6(a), as they counteract each other, the circuit in Fig. 2.6(b) is deduced. By further simplification of Fig. 2.6(a) and transferring the circuit on the LV side of the transformer to the HV side, the equivalent circuit of Fig. 2.6(c) is deduced, in which

$$L_{eq} = L_{arm} + L_{lk}. \quad (2.4)$$

Based on Fig. 2.6(c), the resultant voltage $v_{L_{eq}}(t)$, becomes

$$v_{L_{eq}}(t) = L_{eq} \frac{di_{ac1}(t)}{dt} = v_{ac1}(t) - nv_{ac2}(t), \quad (2.5)$$

where v_{ac1} represents the voltage generated by the MMC behind its arm inductors, that is, $2v_{ac}^{arm}$.

Assuming a large number of SMs, i.e., N , the conceptual converter waveforms are plotted in Fig. 2.7. Based on Fig. 2.7, v_{ac1} and v_{ac2} within half a cycle can be expressed by:

$$v_{ac1}(t) = \begin{cases} \frac{2V_{dc1}}{Nt_\delta}t - V_{dc1}, & t \in [0, Nt_\delta] \\ V_{dc1}, & t \in [Nt_\delta, \frac{T_s}{2}] \end{cases} \quad (2.6)$$

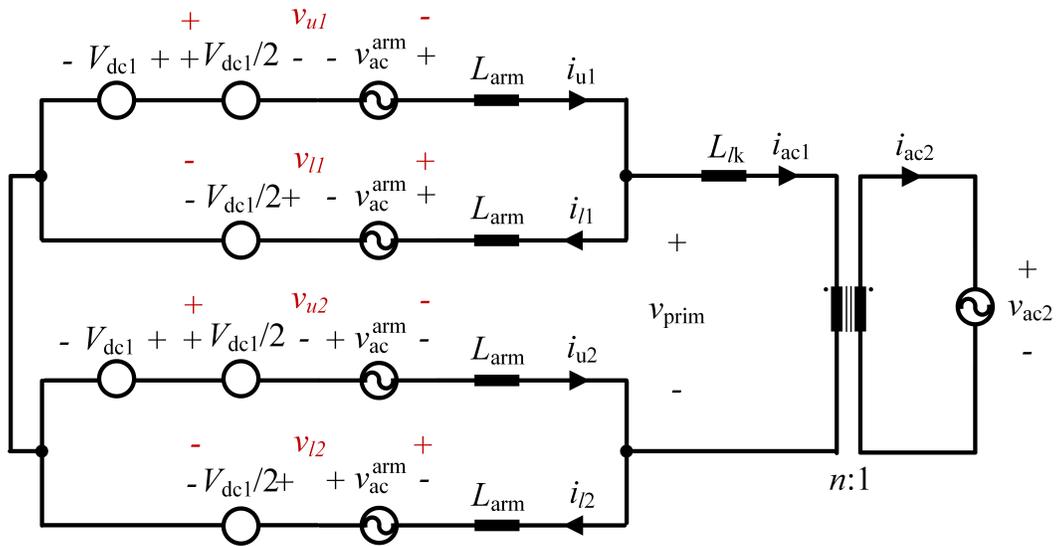
$$v_{ac2}(t) = \begin{cases} -\frac{V_{dc2}}{2}, & t \in [0, t_\varphi] \\ \frac{V_{dc2}}{2}, & t \in [t_\varphi, \frac{T_s}{2}] \end{cases} \quad (2.7)$$

where T_s represents the switching cycle and t_δ , as shown in Fig. 2.4, represents the time interval in which the individual SMs get inserted or bypassed. Consequently, Nt_δ represents the rising or falling time of v_{ac1} . Based on the half-cycle symmetry of v_{ac1} and v_{ac2} , during steady-state operation and as shown in Fig. 2.7, the voltages $v_{ac1}(t)$ and $v_{ac2}(t)$ and the inductor current repeat every half-cycle with reversed signs, i.e.,

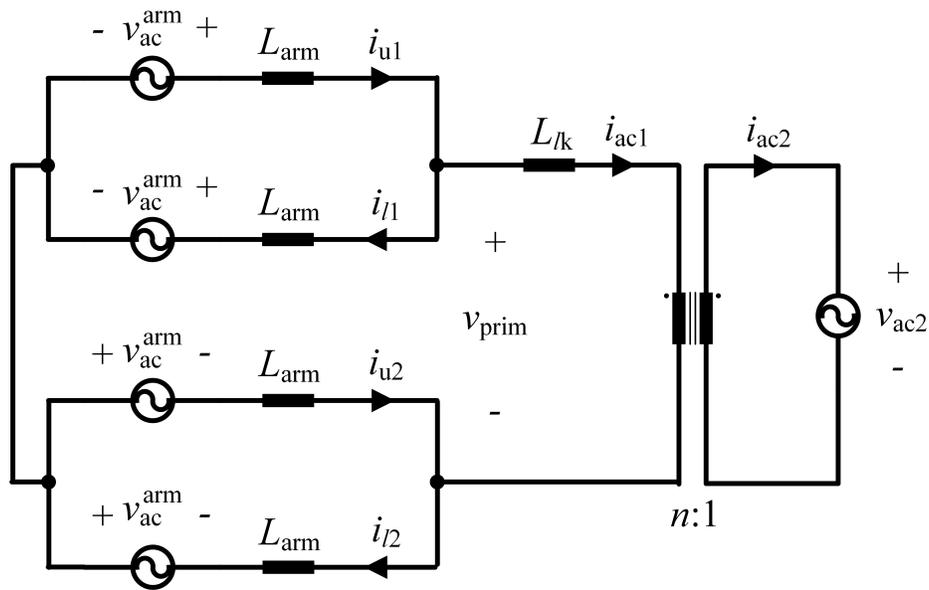
$$v_{ac1}(t) = -v_{ac1}\left(t - \frac{T_s}{2}\right), \quad t \in \left[\frac{T_s}{2}, T_s\right] \quad (2.8a)$$

$$v_{ac2}(t) = -v_{ac2}\left(t - \frac{T_s}{2}\right), \quad t \in \left[\frac{T_s}{2}, T_s\right] \quad (2.8b)$$

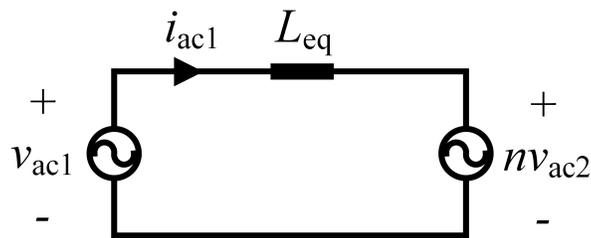
$$i_{ac1}(t) = -i_{ac1}\left(t - \frac{T_s}{2}\right), \quad t \in \left[\frac{T_s}{2}, T_s\right]. \quad (2.8c)$$



(a)



(b)



(c)

Figure 2.6: Equivalent circuit of the converter operating based on the QSW modulation: (a) overall equivalence on both sides, (b) AC equivalent circuit on both sides, and (c) equivalent circuit referred to the primary side.

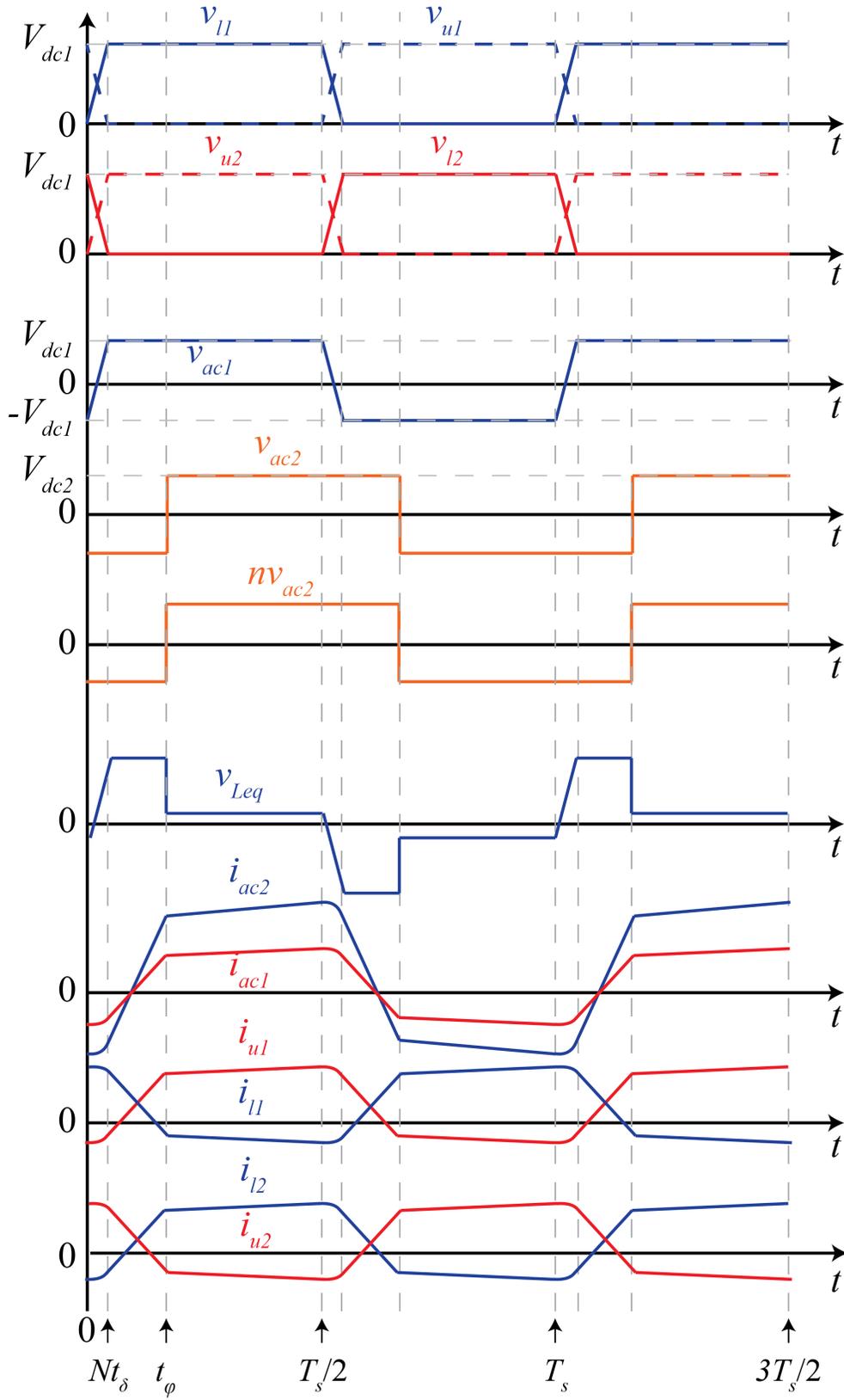


Figure 2.7: Conceptual converter voltage and current waveforms for a general case with N SMs per arm.

Since the phase shift time t_φ and the input and output supply voltages V_{dc1} and V_{dc2} remain the same during the first and the second half-cycles, for the calculation of the transferred power, only the first half-cycle needs to be considered. With $t_0 = 0$, we have

$$P = \frac{1}{T_s} \int_0^{T_s} p(t) dt = \frac{2}{T_s} \int_0^{T_s/2} v_{ac1}(t) \cdot i_{ac1}(t) dt. \quad (2.9)$$

To obtain an analytical expression for P , the current $i_{ac1}(t)$ needs to be determined. On the assumption of a positive phase shift, $0 < \varphi < \pi$, the resulting expressions for the inductor current $i_{ac1}(t)$ within $[0, \frac{T_s}{2}]$ are:

$$i_{ac1}(t) = \begin{cases} \frac{V_{dc1}}{2L_{eq}} \left[\frac{t^2}{Nt_\delta} - \left(\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \right) t \right] + i_{ac1}(0), & t \in [0, Nt_\delta] \\ \frac{V_{dc1}}{2L_{eq}} \left(\frac{V_{dc1} + nV_{dc2}}{V_{dc1}} \right) (t - Nt_\delta) + i_{ac1}(Nt_\delta), & t \in [Nt_\delta, t_\varphi] \\ \frac{V_{dc1}}{2L_{eq}} \left(\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \right) [t - (t_\varphi)] + i_{ac1}(t_\varphi), & t \in [t_\varphi, \frac{T_s}{2}] \end{cases} \quad (2.10)$$

where $t_\varphi = \varphi / (2\pi f_s)$.

The currents on the boundaries of each interval, i.e., $i_{ac1}(0)$, $i_{ac1}(Nt_\delta)$, $i_{ac1}(t_\varphi)$, and $i_{ac1}(\frac{T_s}{2})$, can be obtained by solving the following set of equations:

$$i_{ac1}(Nt_\delta) = \frac{V_{dc1}}{2L_{eq}} \left(\frac{nV_{dc2}}{V_{dc1}} Nt_\delta \right) + i_{ac1}(0) \quad (2.11a)$$

$$i_{ac1}(t_\varphi) = \frac{V_{dc1}}{2L_{eq}} \left(\frac{V_{dc1} + nV_{dc2}}{V_{dc1}} \right) (t_\varphi - Nt_\delta) + i_{ac1}(Nt_\delta) \quad (2.11b)$$

$$i_{ac1}\left(\frac{T_s}{2}\right) = \frac{V_{dc1}}{2L_{eq}} \left(\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \right) \left[\frac{T_s}{2} - (t_\varphi) \right] + i_{ac1}(t_\varphi) \quad (2.11c)$$

$$i_{ac1}\left(\frac{T_s}{2}\right) = -i_{ac1}(0). \quad (2.11d)$$

The results are:

$$i_{ac1}(0) = \frac{V_{dc1}}{4L_{eq}} \left(-\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \frac{T_s}{2} - 2\frac{nV_{dc2}}{V_{dc1}} t_\varphi + Nt_\delta \right), \quad (2.12a)$$

$$i_{ac1}(Nt_\delta) = \frac{V_{dc1}}{4L_{eq}} \left(-\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \frac{T_s}{2} - 2\frac{nV_{dc2}}{V_{dc1}} t_\varphi + \left(1 + \frac{2nV_{dc2}}{V_{dc1}}\right) Nt_\delta \right), \quad (2.12b)$$

$$i_{ac1}(t_\varphi) = \frac{V_{dc1}}{4L_{eq}} \left[-\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \frac{T_s}{2} - 2t_\varphi - Nt_\delta \right]. \quad (2.12c)$$

By substituting for v_{ac1} and i_{ac1} from (2.6) and (2.10) in (2.9), the transferred power for positive phase shift, $0 < \varphi < \pi$ is deduced as

$$P = \frac{nV_{dc1}V_{dc2}}{12T_sL_{eq}} [4(Nt_\delta)^2 + (3T_s - 12t_\varphi)Nt_\delta + (12t_\varphi - 6T_s)t_\varphi]. \quad (2.13)$$

A similar result is obtained for negative phase shift, $-\pi < \varphi < 0$, where

- $P > 0$ denotes power transfer from the HV to the LV side; and
- $P < 0$ denotes power transfer from the LV to the HV side.

As compared with the DAB converter in [10], the transferred power by the converter of Fig. 2.1 is equal to that of the DAB converter, except the terms associated with Nt_δ , i.e., $4(Nt_\delta)^2 + (3T_s - 12t_\varphi)Nt_\delta$ in (2.13), which attenuate the power transfer capability. However, since t_δ is very small, Nt_δ would be small as well and the loss of power transfer capability would be negligible.

2.2 Capacitor Voltage Balancing

Similar to any multilevel converter topology, proper operation of the MMC bridge on the HV side necessitates a capacitor voltage balancing technique to maintain the SM capacitor voltages at their nominal values, i.e., V_{dc1}/N . The most widely adopted strategy to carry out the capacitor voltage balancing task of the class of MMCs is based on a sorting method. That is, the capacitor voltages of SM string of each arm are measured and sorted within each control period. Then, based on the direction of the arm current through the capacitors and the number of required on-state SMs within each control period, a number of SMs are inserted/bypassed. This method needs one current sensor per each arm which adds to the system cost and footprint, particularly when the switching frequency is high as this necessitates high bandwidth current sensors. Here, a modified capacitor voltage balancing strategy based on sorting algorithm is proposed which avoid using per-arm high-bandwidth current sensors. In the proposed strategy, rather than using arm current sensors, the zero-crossing points of each arm current along with their slope signs are detected. By substituting for $i_{ac1}(0)$, $i_{ac1}(Nt_\delta)$, and $i_{ac1}(t_\varphi)$ from (2.12) in (2.10), as an example, the instantaneous value

of the upper arm current of leg 1, based on (2.3), is expressed by:

$$i_{u1}(t) = \frac{1}{2} \left[\frac{V_{dc1}}{2L_{eq}} \left[\frac{t^2}{Nt_\delta} - \left(\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \right) t \right] + \frac{V_{dc1}}{4L_{eq}} \left(-\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \frac{T_s}{2} - 2\frac{nV_{dc2}}{V_{dc1}} t_\varphi + Nt_\delta \right) \right] + \frac{I_{dc1}}{2}, \quad t \in [0, Nt_\delta] \quad (2.14a)$$

$$i_{u1}(t) = \frac{V_{dc1}}{2L_{eq}} \left(\frac{V_{dc1} + nV_{dc2}}{V_{dc1}} \right) (t - Nt_\delta) + \frac{V_{dc1}}{4L_{eq}} \left(-\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \frac{T_s}{2} - 2\frac{nV_{dc2}}{V_{dc1}} t_\varphi + \left(1 + \frac{2nV_{dc2}}{V_{dc1}}\right) Nt_\delta \right), \quad t \in [Nt_\delta, t_\varphi] \quad (2.14b)$$

$$i_{u1}(t) = \frac{V_{dc1}}{2L_{eq}} \left(\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \right) (t - t_\varphi) + \frac{V_{dc1}}{4L_{eq}} \left[-\frac{V_{dc1} - nV_{dc2}}{V_{dc1}} \frac{T_s}{2} - 2t_\varphi - Nt_\delta \right]. \quad t \in \left[t_\varphi, \frac{T_s}{2} \right] \quad (2.14c)$$

Note that circulating current component in (2.3) is ignored as is assumed to be small and negligible. Similarly, the other arm currents, i.e., i_{l1} , i_{u2} and i_{l2} can be derived by substituting for $i_{ac1}(t)$ in (2.3).

As illustrated in the flowchart of Fig. 2.8, the zero-crossing points of i_{u1} along with their slope signs at each zero-crossing point can be easily detected. This information, then, is fed into the SM capacitor voltage sorting algorithm in which the sign of the arm current and measured SM capacitor voltages of the arm are used to select the most appropriate SM for insertion or bypassing.

2.3 Soft Switching Operation

As shown in Fig. 2.7, the current waveform on the secondary side of the MF transformer is similar to that of a DAB converter and consequently, the soft-switching region determined by this bridge is similar to the DAB converter. However, on the primary side, in contrast to the DAB converter in which the current in each power device only consists of the primary winding current, the arm current which includes a DC current as well flows through each switch. Consequently, the soft switching region of the primary side MMC will be different.

- Soft-switching operation of SMs in the MMC bridge

During switching transitions of SMs, the parasitic capacitances C_1 and C_2 which are in parallel with the power switches T_1 and T_2 , as shown in Fig. 2.1, enable ZVS operation. Taking T_1 as an example, soft switching is achieved when prior to its turn-on transition, the arm current, i.e., $i_{arm} = i_{SM}$ is enforced to discharge C_1 first, which has been already

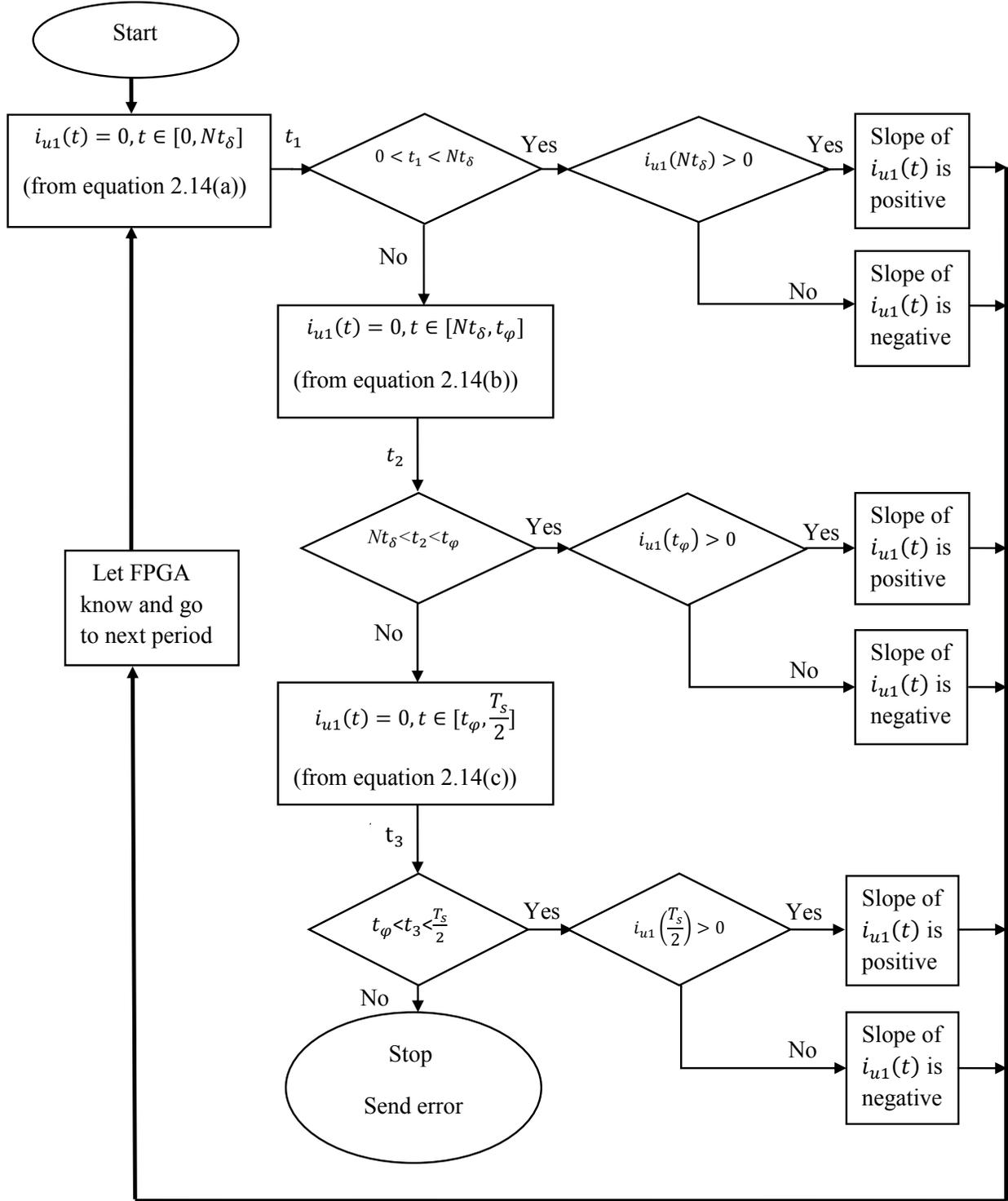


Figure 2.8: Block diagram representation of the proposed zero-current crossing point detection along with slope sign of the arm current for SM capacitor voltage balancing.

charged to V_{SM} . Once C_1 is fully discharged, the diode D_1 will conduct, thereby clamping the voltage across T_1 to zero and providing the provision for ZVS turn-on.

Fig. 2.9 shows the SM operation in inserted mode, where i_{arm} flows through T_1 . Based on the previous discussion, prior to the switching instant when T_1 is turned on, to achieve soft-switching operation, i_{arm} must flow into the SM to discharge C_1 . Meanwhile, i_{arm} charges C_2 and dv/dt is limited by the equivalent capacitance consisted of C_2 and C_1 in parallel. For further reduction of dv/dt and consequently turn-off losses, additional capacitances can be added in parallel to C_1 and C_2 . Once C_1 is fully discharged, i_{arm} flows through D_1 so the voltage across T_1 is clamped at a negligible value, which provides the provision and ensures ZVS turn-on for T_1 .

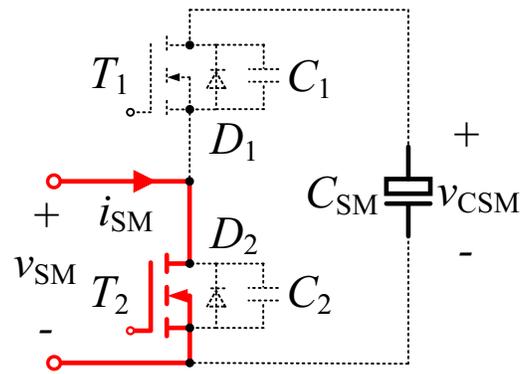
Fig. 2.10 shows the SM operation in the bypass mode, where i_{arm} flows through T_2 . Based on the previous discussion, prior to the switching instant when T_2 is turned on, to achieve soft-switching operation, i_{arm} must flow out of the SM to discharge C_2 . Meanwhile, i_{arm} charges C_1 and dv/dt is limited by the equivalent capacitance consisted of C_1 and C_2 in parallel. Similar to the inserted mode, additional capacitance can be added to further reduce the dv/dt and consequently turn-off losses. Once C_2 is fully discharged, i_{arm} flows through D_2 so the voltage across T_2 is clamped at a negligible value, which provides the provision and ensures ZVS turn-on for T_2 .

In conclusion, to achieve ZVS turn on and to reduce turn-off dv/dt for T_1 and T_2 , in the insertion mode, i_{arm} must flow into the SM while in the bypass mode, it must flow out of the SM.

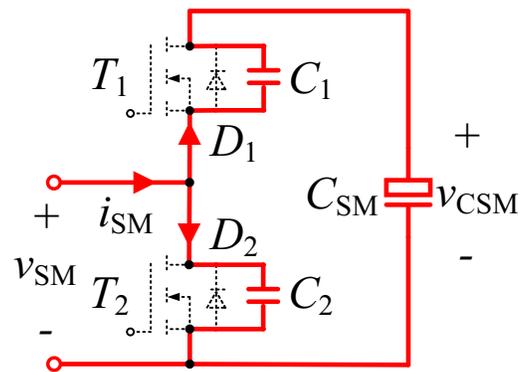
- ZVS condition for the MMC bridge

Following on the previous discussion, the soft-switching condition can be derived by the direction of i_{arm} . For the DAB converter, checking 1 out of 4 switches in the full-bridge on the LV side of the transformer is sufficient to derive the soft-switching condition due to the symmetry of the current. However, for the MMC bridge, the existence of the DC component makes the currents in the upper and lower arms, i.e., i_{u1} and i_{l1} , respectively, non symmetric. This asymmetry leads to two boundaries for the soft-switching condition where one boundary dominates the other one, depending on the operating point.

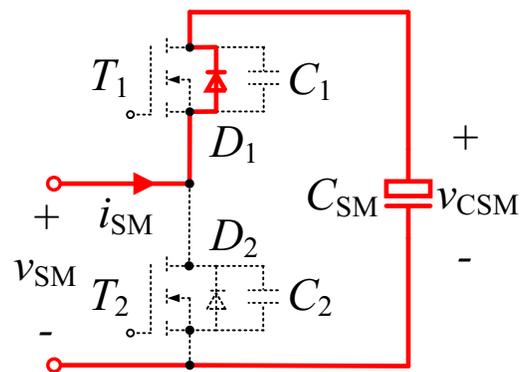
In the following part, the soft-switching boundary of the 4-level MMC bridge, i.e., with 4 SMs within an arm, is derived. The corresponding conceptual waveforms for such a case are shown in Fig. 2.11. In the derivations, all variables are in p.u. values, where the base value



(a)

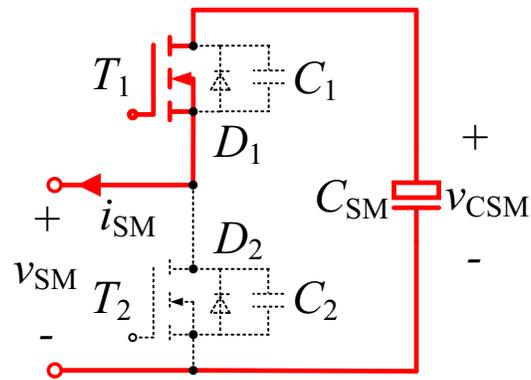


(b)

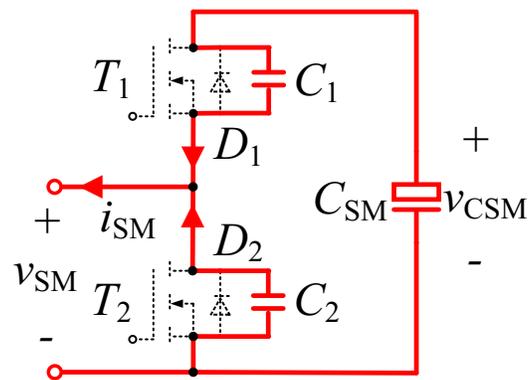


(c)

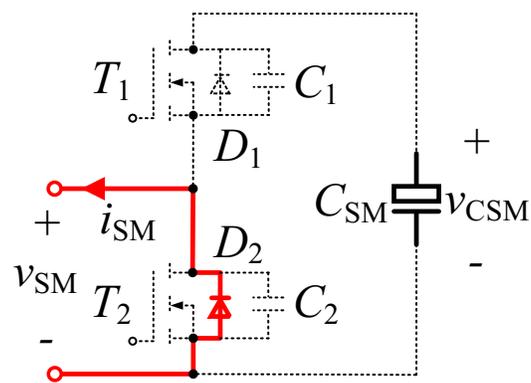
Figure 2.9: ZVS operation of the switches of a SM during insertion. (a) bypassed state. (b) T_2 is turned off. (c) D_1 is conducting, providing zero-voltage turn-on provision for T_1 .



(a)



(b)



(c)

Figure 2.10: ZVS operation of the switches in a SM during bypassing. (a) inserted state. (b) T_1 is turned off. (c) D_2 is conducting, providing zero-voltage turn-on provision for T_2 .

of each variable is defined as:

$$P_{base} = \frac{V_{dc1}^2}{2\pi f_s L_{eq}}, \quad (2.15a)$$

$$V_{base} = V_{dc1}, \quad (2.15b)$$

$$I_{base} = \frac{V_{dc1}}{2\pi f_s L_{eq}}. \quad (2.15c)$$

In addition, the staircase time t_δ and the conversion ratio D are defined as:

$$t_\delta = KT_s, \quad (2.16a)$$

$$D = \frac{nV_{dc2}}{V_{dc1}}. \quad (2.16b)$$

As shown in Fig. 2.11, by using v_{ac1} and v_{ac2} , $v_{L_{eq}}$, the voltage across L_{eq} can be calculated. Based on $v_{L_{eq}}$ and the time interval between each two switching instants, Δi_{ac1} is derived as:

$$i_{ac1}\{t = t_i\} = i_{ac1}\{t = t_{i-1}\} + \frac{v_{L_{eq}}\{t = t_i\}(t_i - t_{i-1})}{L_{eq}}, \quad (2.17)$$

where $i_{ac1}\{t = t_0\}$ is the current when the phase of v_{ac1} is 0 and $i_{ac1}\{t = t_6\}$ is the current when the phase of v_{ac1} is π . Based on the symmetry of the waveform, $i_{ac1}\{t = t_0\}$ and $i_{ac1}\{t = t_6\}$ satisfy:

$$i_{ac1}\{t = t_0\} + i_{ac1}\{t = t_6\} = 0. \quad (2.18)$$

By solving (2.17) and (2.18), the normalized value of i_{ac1} within its various subintervals, is deduced as:

$$i_{ac1}\{t = t_0\} = 2\pi K - 0.5\pi + 0.5\pi D - D\varphi, \quad (2.19a)$$

$$i_{ac1}\{t = t_1\} = 2\pi K - 0.5\pi + 0.5\pi D - D\varphi + \pi DK, \quad (2.19b)$$

$$i_{ac1}\{t = t_2\} = 3\pi K - 0.5\pi + 0.5\pi D - D\varphi + 3\pi DK, \quad (2.19c)$$

$$i_{ac1}\{t = t_3\} = \varphi - 0.5\pi + 0.5\pi D, \quad (2.19d)$$

$$i_{ac1}\{t = t_4\} = 0.5\pi - 3\pi K - 0.5\pi D + D\varphi + 3\pi DK, \quad (2.19e)$$

$$i_{ac1}\{t = t_5\} = 0.5\pi - 2\pi K - 0.5\pi D + D\varphi + \pi DK. \quad (2.19f)$$

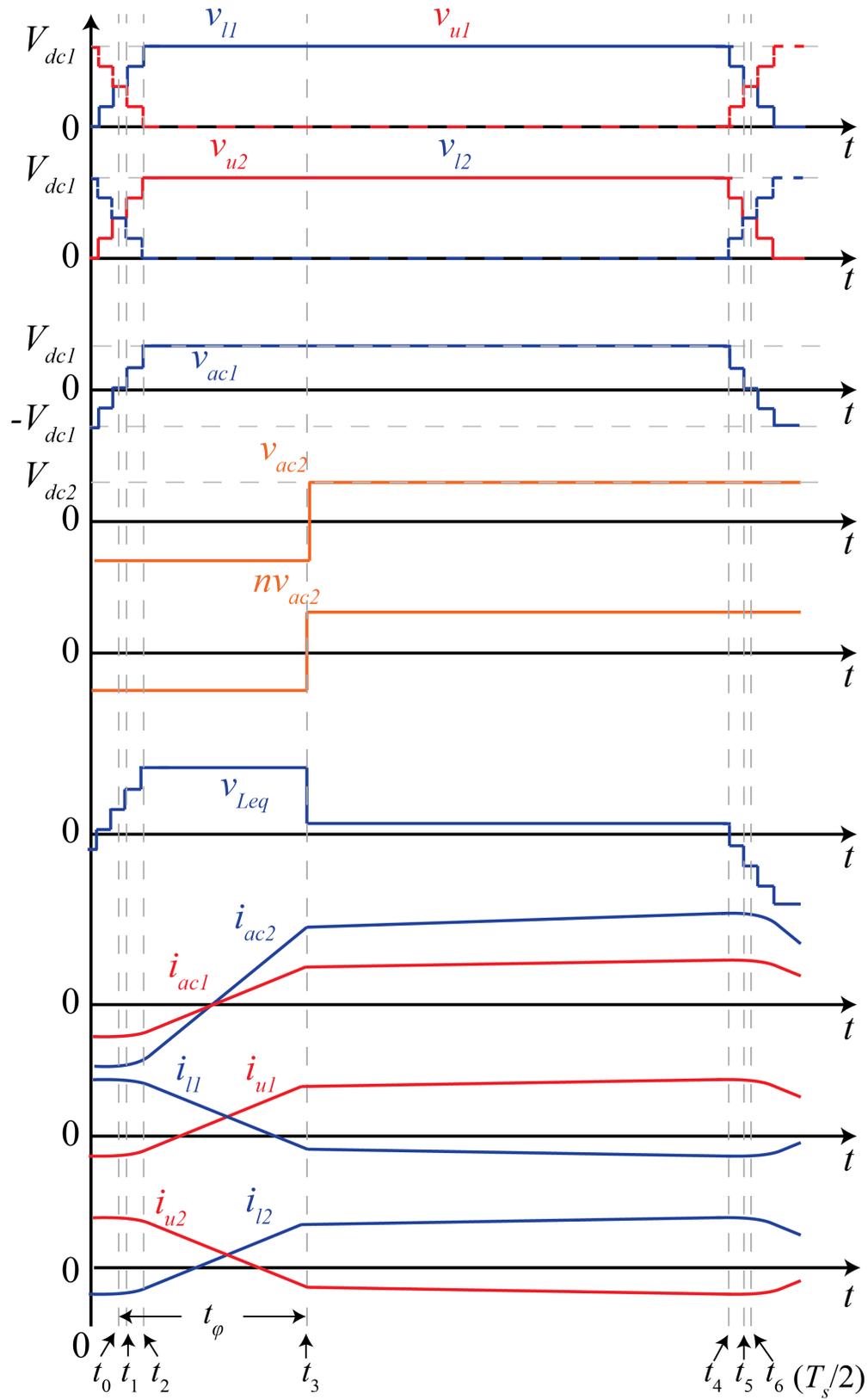


Figure 2.11: Conceptual converter voltage and current waveforms for a MMC with 4 SMs per arm.

Based on Fig. 2.11, the normalized v_{ac1} within the various subintervals is expressed by:

$$v_{ac1}\{t = t_0\} = 0, \quad (2.20a)$$

$$v_{ac1}\{t = t_1\} = 0, \quad (2.20b)$$

$$i_{ac1}\{t = t_2\} = \frac{1}{2}, \quad (2.20c)$$

$$i_{ac1}\{t = t_3\} = 1, \quad (2.20d)$$

$$i_{ac1}\{t = t_4\} = 1, \quad (2.20e)$$

$$i_{ac1}\{t = t_5\} = \frac{1}{2}. \quad (2.20f)$$

By substituting for i_{ac1} and v_{ac1} from (2.19) and (2.20) in (2.9), the transferred power and the DC current are calculated by:

$$P = -\frac{D}{\pi}(\varphi^2 - \varphi\pi + 5\pi^2 K^2), \quad (2.21a)$$

$$I_{dc1} = -\frac{D}{\pi}(\varphi^2 - \varphi\pi + 5\pi^2 K^2). \quad (2.21b)$$

Each arm current is expressed by (2.3). Assuming a negligible circulating current within the legs, the arm currents are expressed by:

$$\begin{cases} i_{u1} = \frac{I_{dc1}}{2} + \frac{i_{ac1}}{2}, \\ i_{l1} = \frac{I_{dc1}}{2} - \frac{i_{ac1}}{2}, \\ i_{u2} = \frac{I_{dc1}}{2} - \frac{i_{ac1}}{2}, \\ i_{l2} = \frac{I_{dc1}}{2} + \frac{i_{ac1}}{2}. \end{cases} \quad (2.22)$$

Based on calculated I_{dc1} , i_{ac1} and (2.22), the upper and lower arm currents for leg 1 at each

switching instant are:

$$i_{u1}\{t = t_0\} = -\frac{(2D\varphi^2 + 10D\pi^2K^2 - 4\pi^2K - D\pi^2 + \pi^2)}{4\pi}, \quad (2.23a)$$

$$i_{u1}\{t = t_1\} = \frac{(D\pi^2 - 2D\varphi^2 + 4\pi^2K - \pi^2 - 10D\pi^2K^2 + 2DK\pi^2)}{4\pi}, \quad (2.23b)$$

$$i_{u1}\{t = t_2\} = \frac{(D\pi^2 - 2D\varphi^2 + 6\pi^2K - \pi^2 - 10D\pi^2K^2 + 6DK\pi^2)}{4\pi}, \quad (2.23c)$$

$$i_{u1}\{t = t_4\} = -\frac{(D\pi^2 + 2D\varphi^2 + 6\pi^2K - \pi^2 + 10D\pi^2K^2 - 4\pi D\varphi - 6DK\pi^2)}{4\pi}, \quad (2.23d)$$

$$i_{u1}\{t = t_5\} = -\frac{(D\pi^2 + 2D\varphi^2 + 4\pi^2K - \pi^2 + 10D\pi^2K^2 - 4\pi D\varphi - 2DK\pi^2)}{4\pi}, \quad (2.23e)$$

$$i_{l1}\{t = t_0\} = -\frac{(2D\varphi^2 - 4D\pi\varphi + 10D\pi^2K^2 + 4\pi^2K + D\pi^2 - \pi^2)}{4\pi}, \quad (2.23f)$$

$$i_{l1}\{t = t_1\} = -\frac{(D\pi^2 + 2D\varphi^2 + 4\pi^2K - \pi^2 + 10D\pi^2K^2 - 4\pi D\varphi + 2DK\pi^2)}{4\pi}, \quad (2.23g)$$

$$i_{l1}\{t = t_2\} = -\frac{(D\pi^2 + 2D\varphi^2 + 6\pi^2K - \pi^2 + 10D\pi^2K^2 - 4\pi D\varphi + 6DK\pi^2)}{4\pi}, \quad (2.23h)$$

$$i_{l1}\{t = t_4\} = -\frac{(2D\varphi^2 - D\pi^2 - 6\pi^2K + \pi^2 + 10D\pi^2K^2) + 6DK\pi^2}{4\pi}, \quad (2.23i)$$

$$i_{l1}\{t = t_5\} = -\frac{(2D\varphi^2 - D\pi^2 - 4\pi^2K + \pi^2 + 10D\pi^2K^2) + 2DK\pi^2}{4\pi}. \quad (2.23j)$$

For the full bridge on the secondary of the MF transformer, where the device current is the same as i_{ac1} , the current at the switching instant is calculated as:

$$i_{ac2} = i_{ac1}\{t = t_3\} = \varphi - 0.5\pi + 0.5\pi D. \quad (2.24)$$

Consequently, the following inequalities need to be met to ensure soft-switching operation for all switching instants:

$$\begin{cases} i_{u1}\{t = t_1\}, i_{u1}\{t = t_2\}, i_{l1}\{t = t_4\}, i_{l1}\{t = t_5\} < 0, \\ i_{l1}\{t = t_1\}, i_{l1}\{t = t_2\}, i_{u1}\{t = t_4\}, i_{u1}\{t = t_5\} > 0, \\ i_{ac1}\{t = t_3\} > 0. \end{cases} \quad (2.25)$$

The inequalities in (2.25) will be used in the next chapter to determine the full ZVS region of the converter.

CHAPTER 3 SIMULATION STUDIES

This chapter evaluates performance of the DC-DC converter of Fig. 2.1 when it operates under the proposed modulation and control strategy. The studies are conducted to demonstrate effectiveness of the proposed modulation and capacitor voltage balancing to maintain the SM capacitor voltages at their nominal value while ZVS is achieved.

The reported studies in this chapter are carried out based on time-domain simulation in the MATLAB/SIMULINK software environment. The system parameters are given in Table 3.1.

To evaluate the converter performance based on the parameters listed in Table 3.1, 4 simulation case studies as summarized in Table 3.2, are considered.

Table 3.1: Specifications and parameters of the simulation test system.

Nominal Power, P	1 kW
DC-link 1 voltage, V_{dc1}	200 V
DC-link 2 voltage, V_{dc2}	50 V
Number of Submodules, N	4
Submodule Capacitance, C_{SM}	1 μ F
Arm inductance, L_{arm}	15 μ H
Operating Frequency, f_{sw}	200 kHz
Transformer Turns Ratio, n	4
Transformer Leakage Inductance, L_{lk}	50 μ H
Step time, t_δ	1.3% T_s

3.1 ZVS Region

According to (2.25), the family of output power versus phase shift curves for different values of D , when $t_\delta = 1\%T_s$, is shown in Fig. 3.1. The soft switching boundary for all the power MOSFETs of

Table 3.2: Summary of cases according to operating conditions.

Case	Transferred Power, P	Modulation	Switching—	Voltage Conversion Ratio, D
Case 1	250 W	5-step Modulation	Hard Switching	1
Case 2	300 W	5-step Modulation	Soft Switching	1
Case 3	250 W	9-step Modulation	Hard Switching	1
Case 4	300 W	9-step Modulation	Soft Switching	1

the MMC is specified by the green curve while the light blue curve is the soft-switching boundary for all devices of the full-bridge stage. Consequently, the region confined between the two curves is the soft-switching region for all devices of the overall converter. As shown in Fig. 3.1, the soft switching region is greatly impacted by the value of D . Although for $0.5 < D < 1$, the full ZVS region is wider than the one for $D = 1$, the power flow transfer capability is lower. Nevertheless, as D becomes larger than one, the soft switching region shrinks.

Fig. 3.1 shows the soft switching characteristics for positive power flow direction where the MMC leads the half bridge, designated as positive phase shifts. However, for negative power flow direction, the opposite is true and a similar family of curves can be deduced.

To show the impact of the staircase time, t_δ , on the soft switching region, similar families of curves for the cases when $t_\delta = 2\%T_s$, $t_\delta = 4\%T_s$ and $t_\delta = 6\%T_s$ are shown in Figs. 3.2 to 3.4, respectively. Comparison of the soft-switching regions for identical values of D , φ , and P in Figs. 3.1 to 3.4 confirms that, as t_δ increases, the soft-switching region shrinks. When t_δ is 2% of T_s , almost one third of the operating points for $D = 1$ is within the soft-switching region. When t_δ is 4% of T_s , only a small part of operating points is within the soft-switching region. When staircase time is 6% of T_s , there is no operating point within the soft-switching region for $D = 1$. In conclusion, with a significant staircase time, this converter can hardly transfer power under full soft-switching conditions. This is also the reason why the QSW modulation is selected for this converter rather than sinusoidal or triangular modulation schemes shown in Figs. 2.2 and 2.3, respectively.

In practice, the soft-switching boundary is not only determined by the direction of the arm currents as expressed by (2.25) but also by their amplitudes at the switching instants. First, the energy stored in the inductance should be larger than the energy required to discharge the capacitance, which may include both device parasitic capacitance and an additionally added external capacitance to reduce dv/dt . Secondly, the dead time and current amplitude should match so that the capacitance is fully discharged before dead time ends. In general, during turn-on transition of T_1 , i.e., SM insertion, ZVS is achieved under the following requirement:

$$C_1 + C_2 < \frac{i_{u1}(\text{turn-on})t_{\text{dead}}}{v_{CSM}}, \quad (3.1)$$

while during turn-off transition, ZVS is achieved under:

$$\frac{dv}{dt} = \frac{i_{u1}(\text{turn-off})}{C_1 + C_2} < \frac{dv^*}{dt}, \quad (3.2)$$

where $\frac{dv^*}{dt}$ is the upper limit of the designed $\frac{dv}{dt}$ and $i_{u1}(\text{turn-off})$ is the switch current during turn-off transition. Therefore, selection of t_{dead} and the switch parallel capacitance are intertwined based

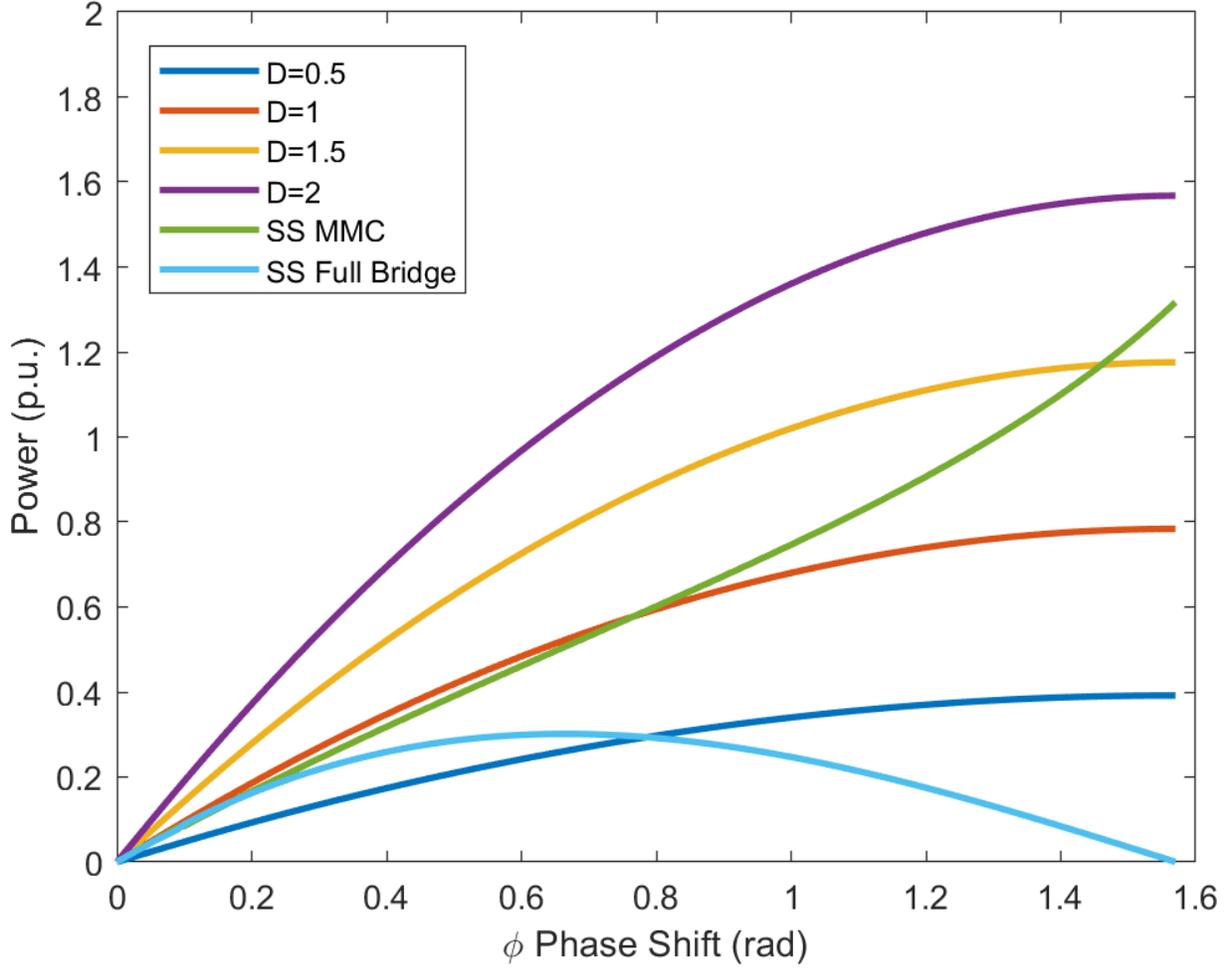


Figure 3.1: Soft-switching region for $t_\delta = 1\%T_s$.

on (3.1) and (3.2). In this thesis, the GaN power MOSFET GS66506T is used in which $C_{OSS} = 49$ pF and $C_{RSS} = 1.59$ pF. This is equivalent to $C_{DS} = C_{OSS} - C_{RSS} = 47.41$ pF. Therefore, without adding any external additional capacitance, $C_1 + C_2 = 2(47.41)$ pF= 94 pF. Consequently, the dead-time is adjusted accordingly to meet the full ZVS requirements.

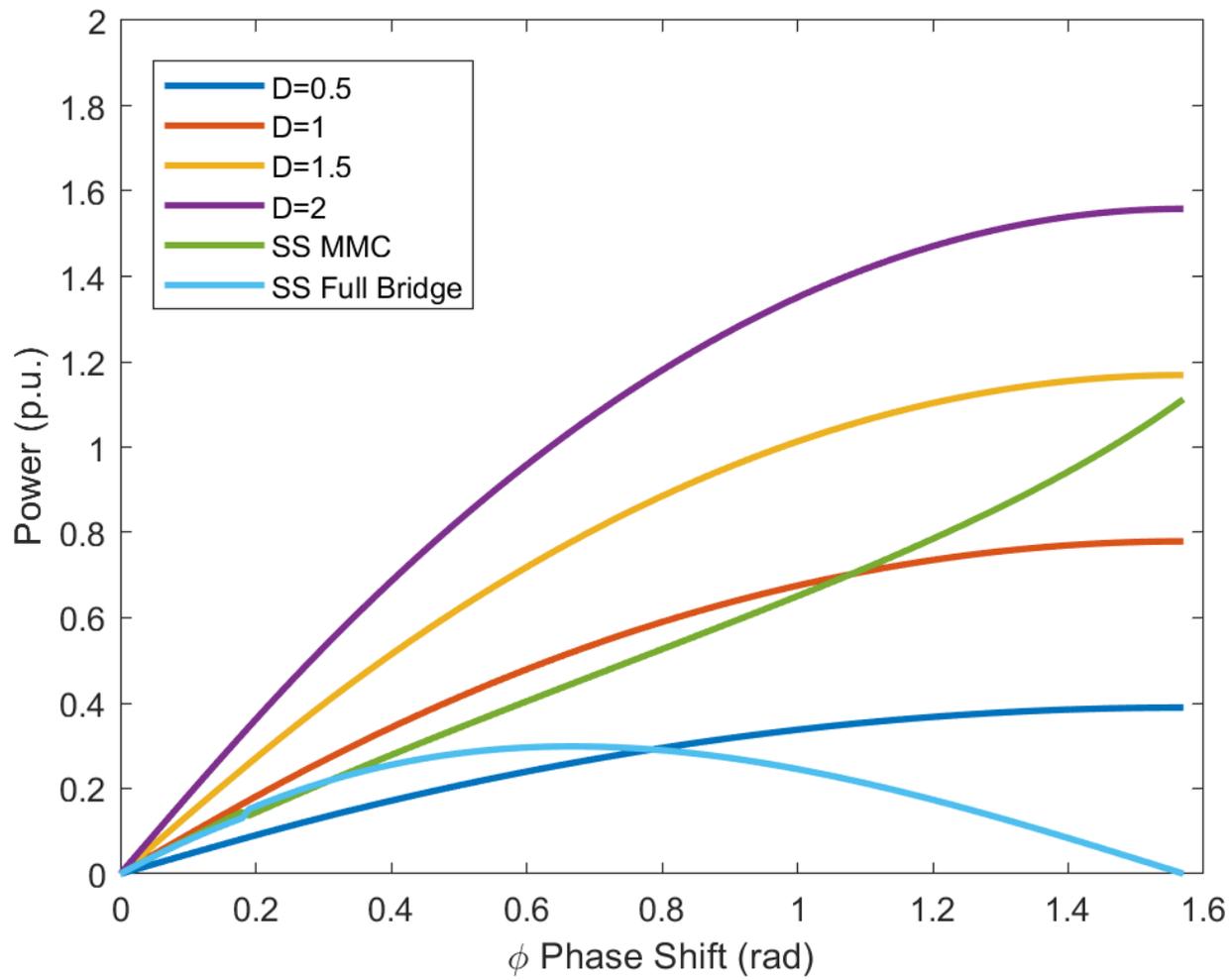


Figure 3.2: Soft-switching region for $t_{\delta} = 2\%T_s$.

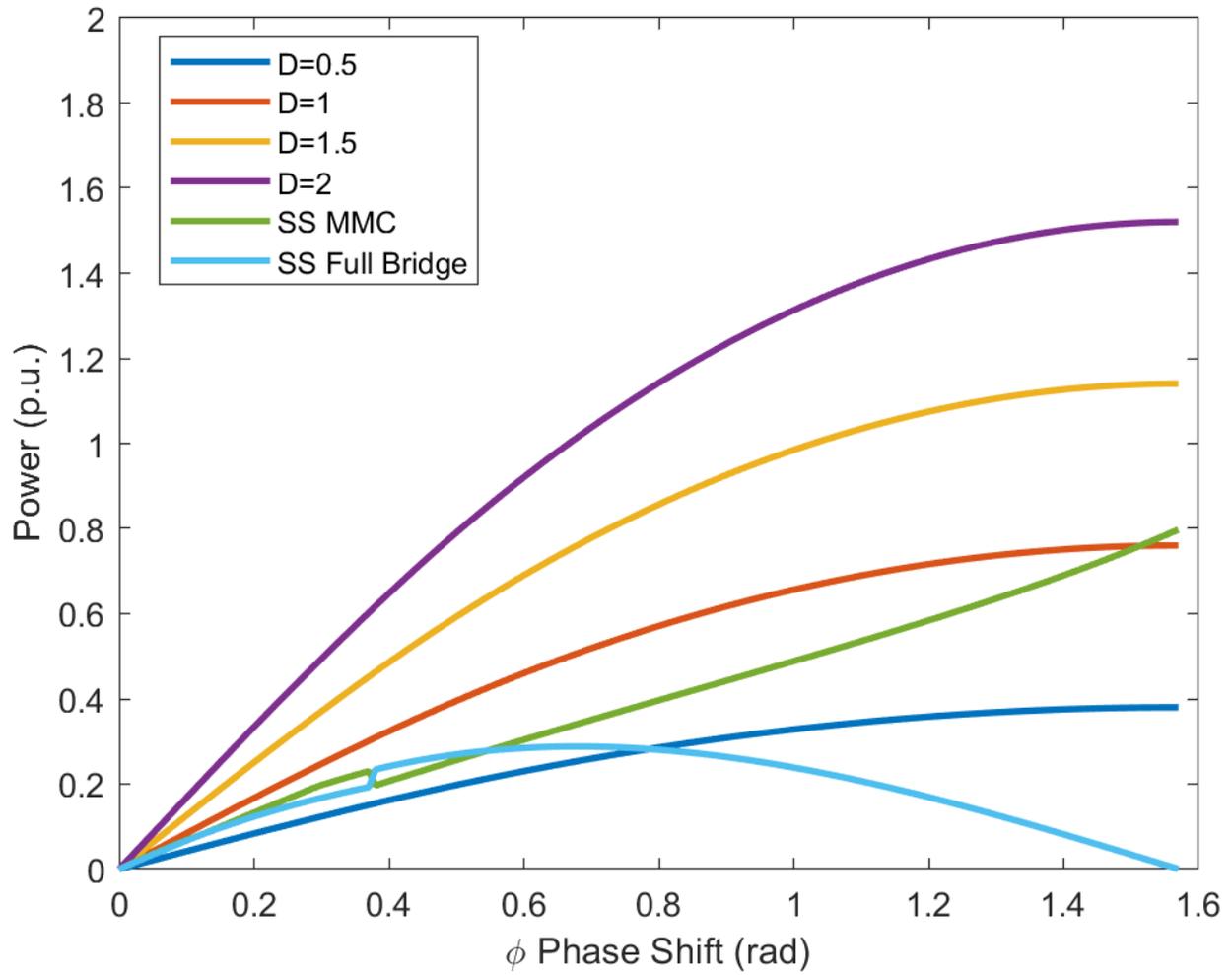


Figure 3.3: Soft-switching region for $t_{\delta} = 4\%T_s$.

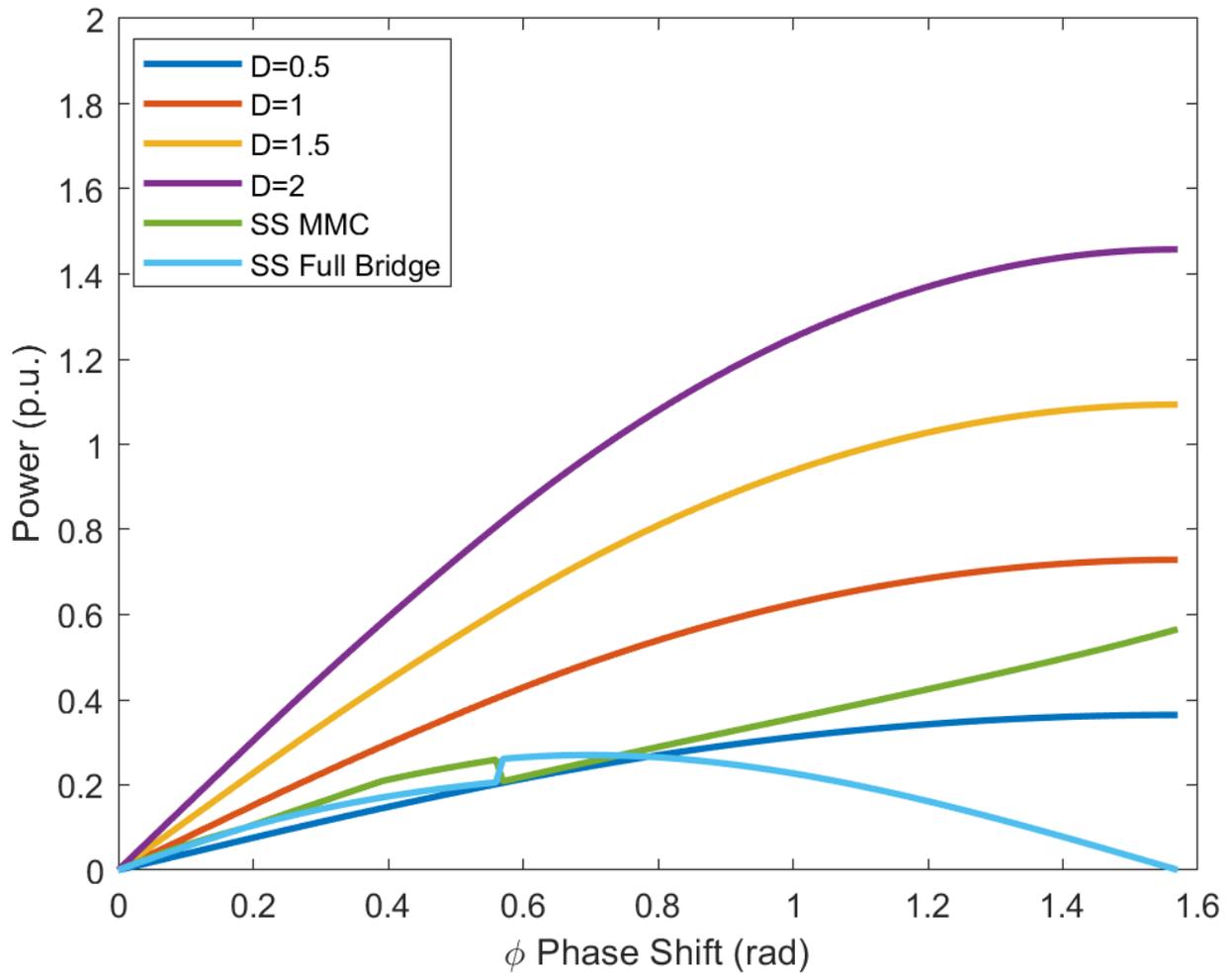


Figure 3.4: Soft-switching region for $t_\delta = 6\%T_s$.

3.2 Steady-State Operation: Case 1

Fig. 3.5 provides the steady-state converter current and voltage waveforms. Under this operating scenario, $\varphi = 0.9$ rad and as can be traced by the families of soft-switching region curves in Figs. 3.1 and 3.2, the operating point falls outside of the soft switching region and the converter operates under hard switching. Fig. 3.5 also shows the upper and lower arm voltages of the two legs of the MMC, i.e., v_{u1}, v_{l1}, v_{u2} and v_{l2} , which are staircase quasi-square 5-level waveforms. The primary and secondary voltage and current waveforms of the transformer, i.e., $v_{prim}, i_{ac1}, v_{ac2}$ and i_{ac2} are also illustrated in Fig. 3.5. As expected, v_{ac2} is a two-level waveform while v_{prim} is a staircase 5-level waveform. Under this case, the SMs in the diagonal MMC arms are inserted and bypassed at the same time, as analyzed in Chapter 2, and that is why v_{prim} voltage is also a five-level waveform with a voltage step size of 50 V. Fig. 3.5 shows the circulating current waveform of the MMC which has a negligible magnitude. In fact, the arm inductor of this converter must be sized such that the magnitude of the circulating current becomes negligible. This is particularly important when the converter operates under soft-switching conditions. Otherwise, the magnitude of the circulating current impacts soft-switching boundary of the MMC.

The upper and lower arm currents of the two legs of the MMC, i.e., i_{u1}, i_{l1}, i_{u2} and i_{l2} , as shown in Fig. 3.5, are in close agreements with their corresponding conceptual waveforms illustrated in Figs. 2.7 and 2.11. The SM capacitor voltages of the MMC, as shown in Fig. 3.5, are all well balanced at their nominal values, i.e., 50 V.

To show the hard switching operation of the SMs of the MMC, Fig. 3.6 shows the gate-source voltage, the drain-source voltage and the drain current of the lower switch, T_2 , of SM1 in leg 1 of the MMC. As shown in Fig. 3.6, the switch T_2 is turned on under hard switching.

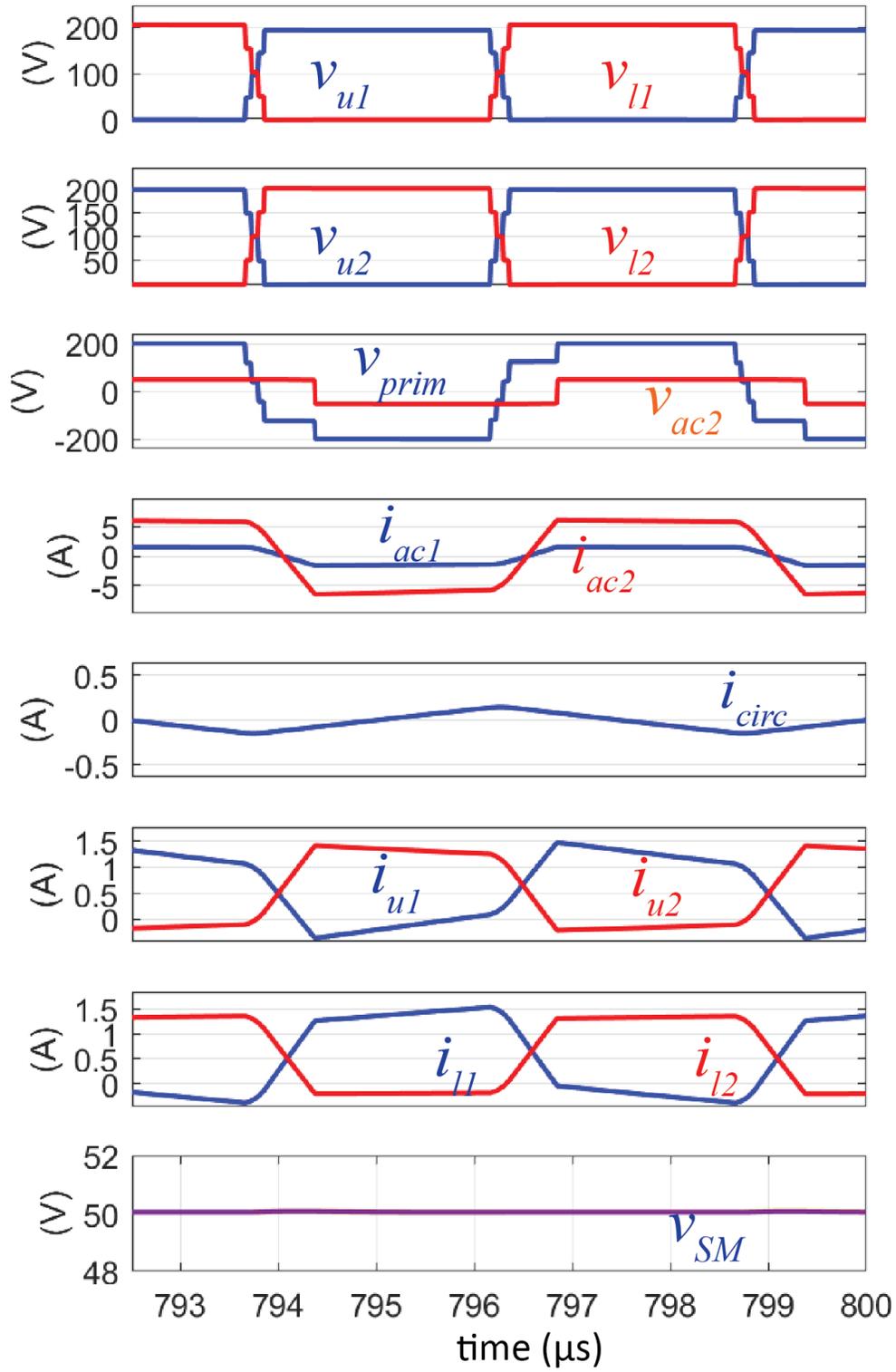


Figure 3.5: Steady-state converter waveforms in Case 1.

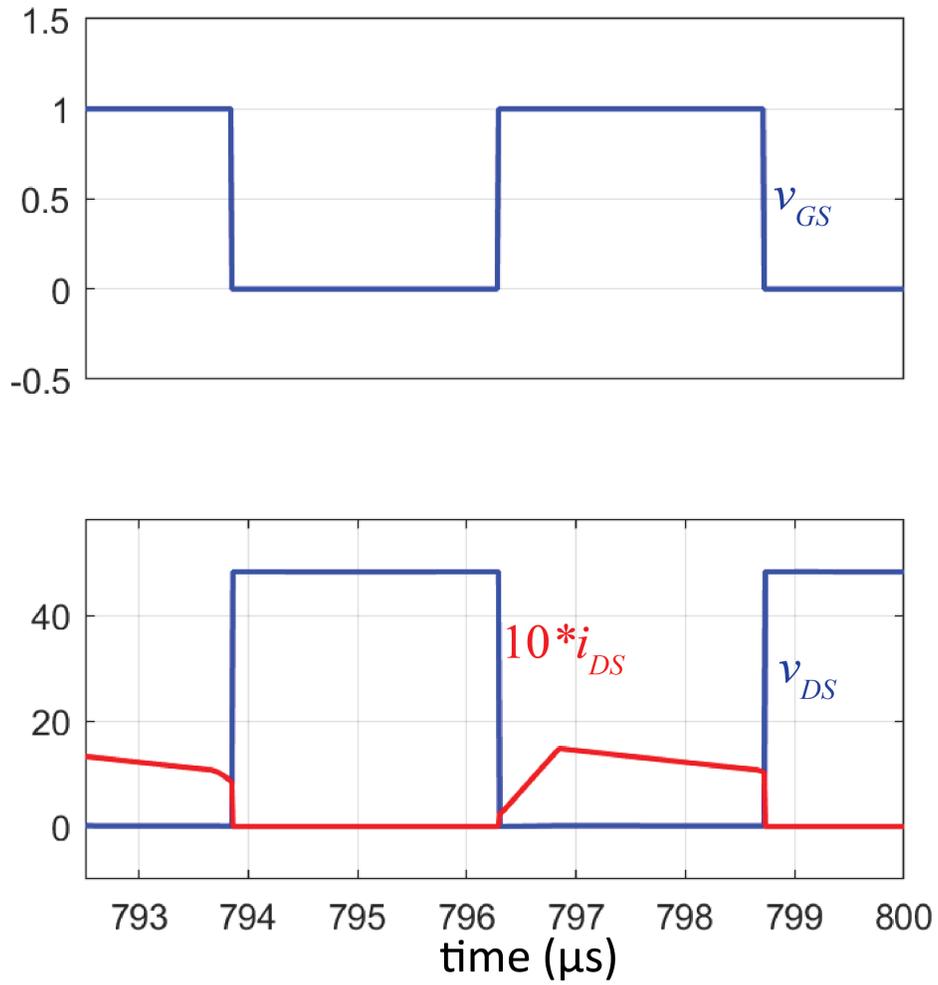


Figure 3.6: Voltage and current waveforms of the switch T_2 of SM1 in leg 1 of the MMC under the operating condition of Fig. 3.5.

3.3 Steady-State Operation: Case 2

Fig. 3.7 shows the steady-state converter current and voltage waveforms. Under this operating condition, $\varphi = \pi/2$ and as can be traced by the families of soft-switching region curves in Figs. 3.1 and 3.2, the operating point falls within the soft-switching region. In this case, the voltage and current waveforms of the converter are similar to those in Case 1 except that the converter operates under soft switching.

To show the soft switching operation of the SMs of the MMC, Fig. 3.8 shows the gate-source voltage, the drain-source voltage and the drain current of the switch T_2 of SM1 in leg 1 of the MMC. As shown in Fig. 3.8, prior to turn-on transition of the switch T_2 , its drain current becomes negative, thereby enforcing its diode to conduct. Consequently, T_2 is turned on under ZVS.

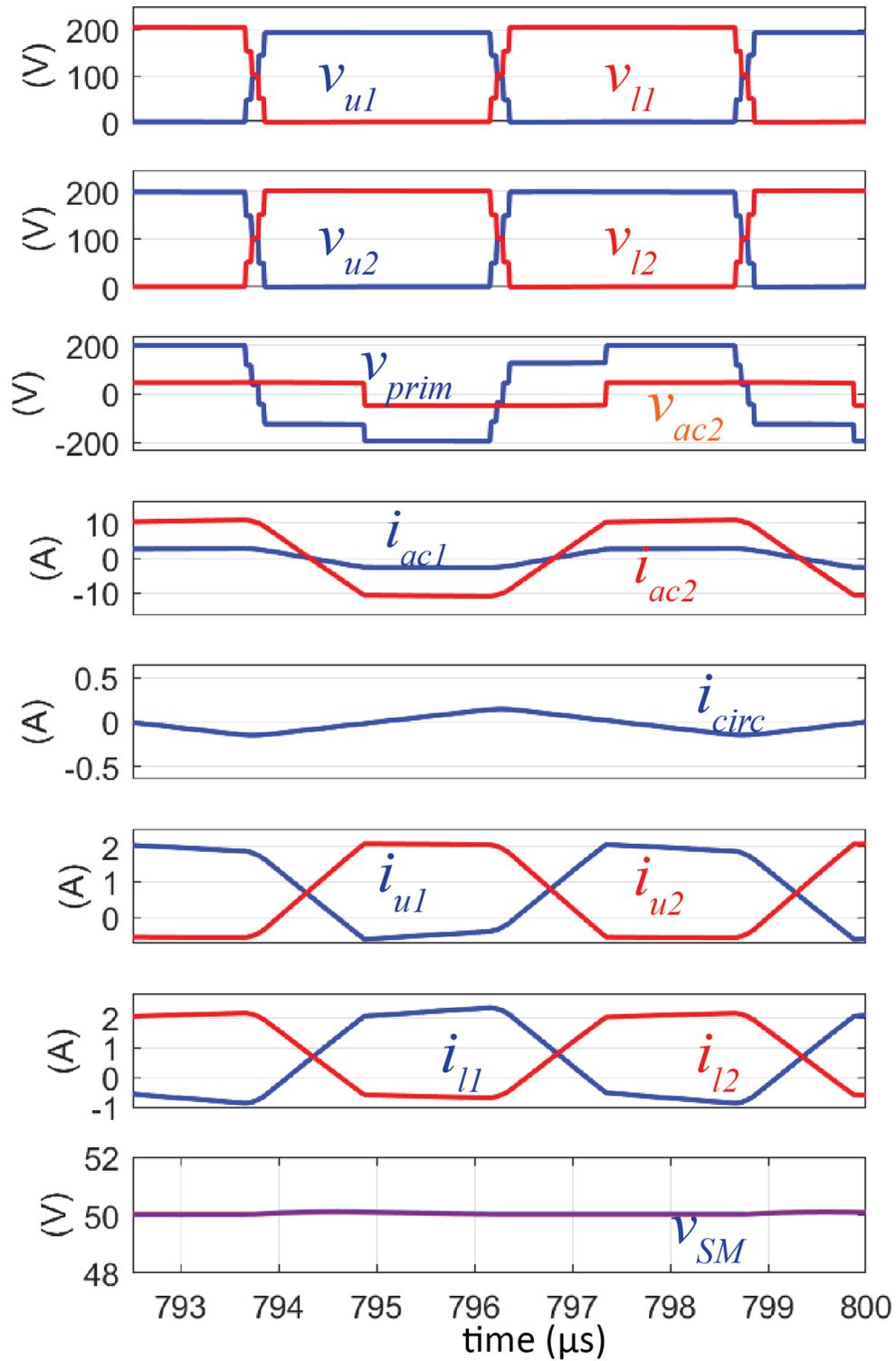


Figure 3.7: Steady-state converter waveforms in Case 2.

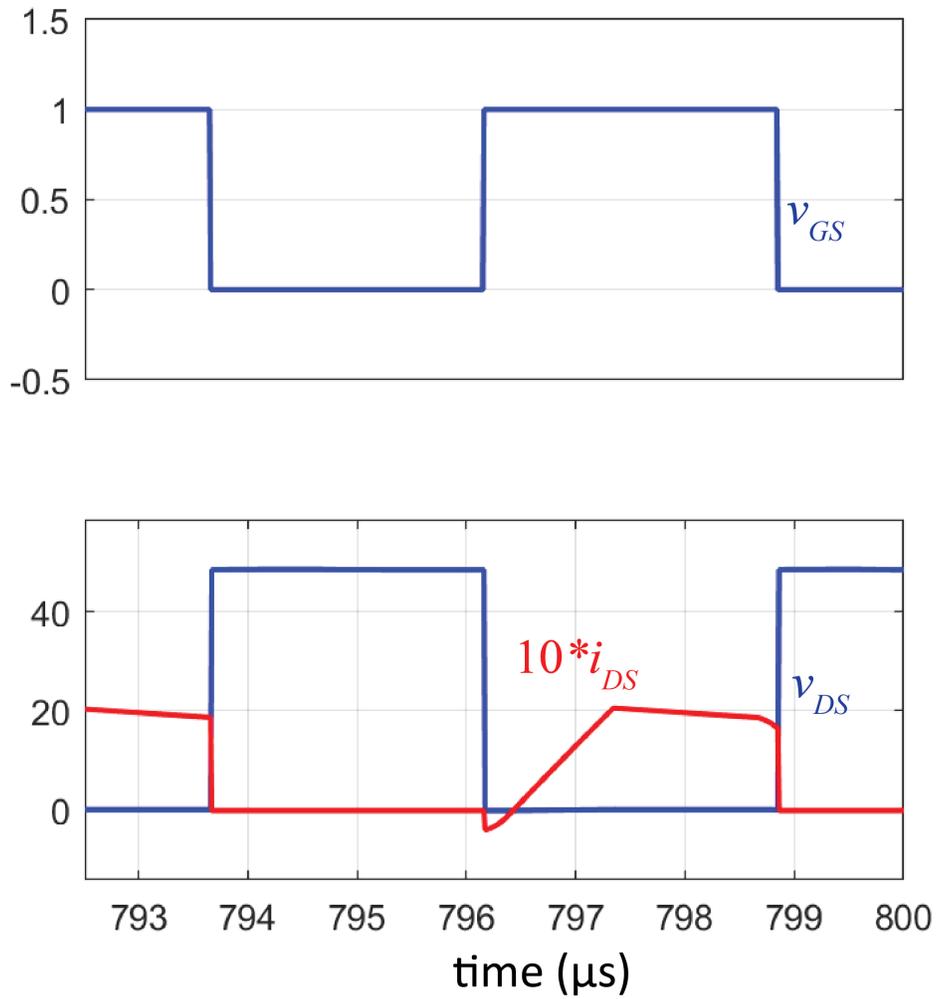


Figure 3.8: Voltage and current waveforms of the switch T_2 of SM1 in leg 1 of the MMC under the operating condition of Fig. 3.7.

3.4 Steady-State Operation: Case 3

In this case, the operating condition is similar to Case 1 except that the modulation strategy is slightly modified such that the SMs in the diagonal arms of the MMC are inserted and bypassed with a small delay, as opposed to Case 1 in which they are switched on and off in tandem. As a result, v_{prim} becomes a staircase 9-level waveform, as shown in Fig. 3.9.

The gate-source voltage, the drain-source voltage and the drain current of the switch T_2 of SM1 in leg 1 of the MMC are shown in Fig. 3.10, which confirm the hard switching operation of the switch T_2 .

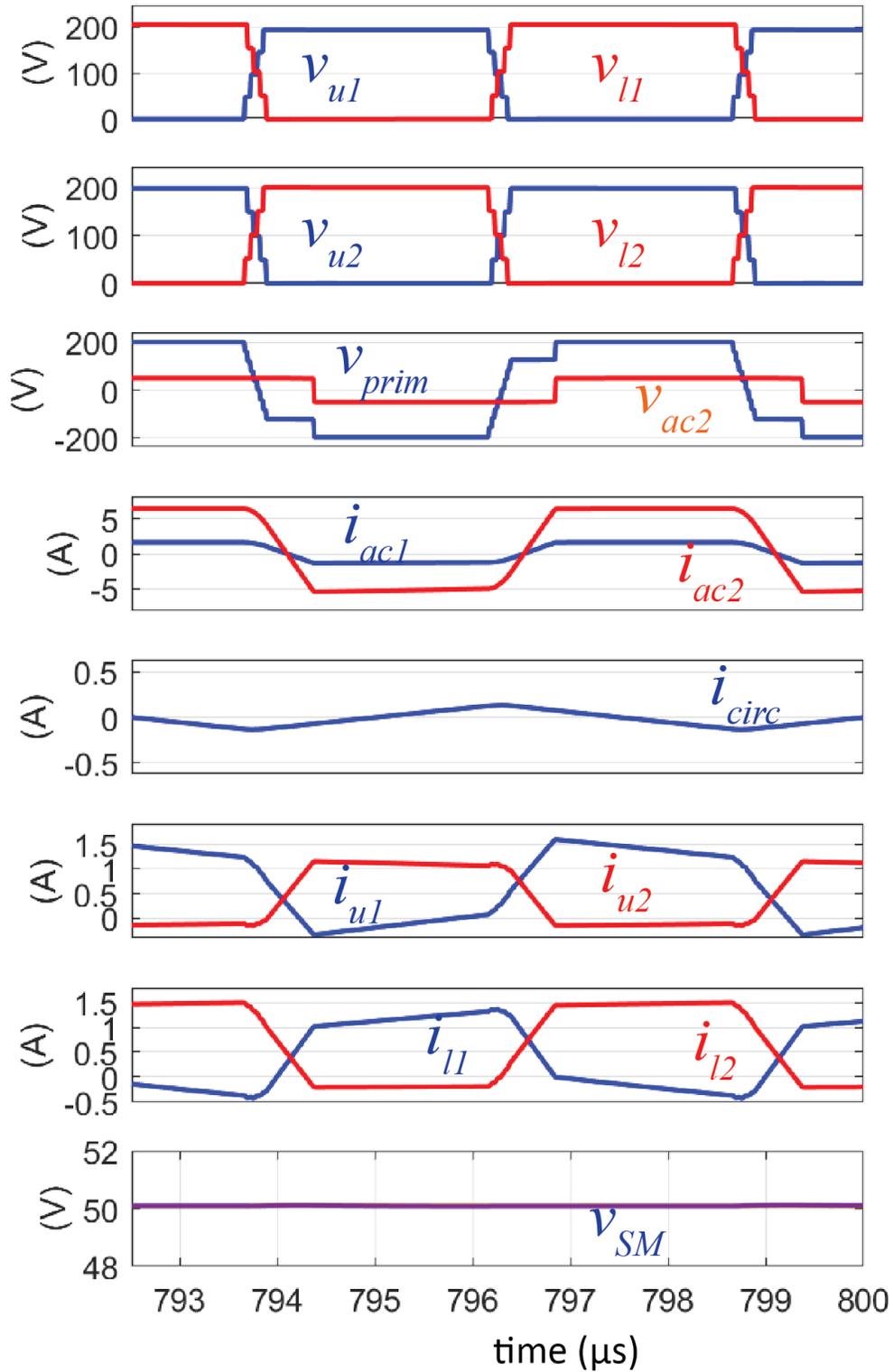


Figure 3.9: Steady-state converter waveforms in Case 3.

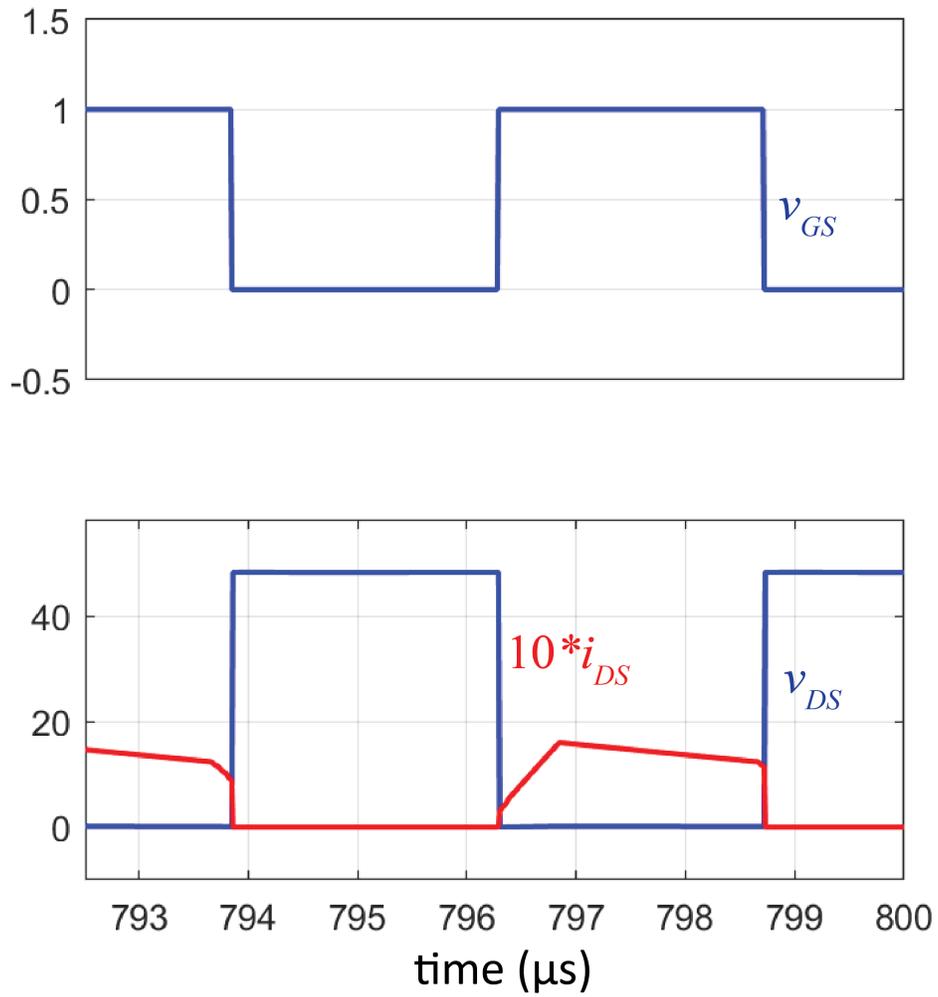


Figure 3.10: Voltage and current waveforms of the switch T_2 of SM1 in leg 1 of the MMC under the operating condition of Fig. 3.9.

3.5 Steady-state Operation: Case 4

The operating condition under this case is identical to Case 2 except that the modulation strategy is slightly modified such that the SMs in the diagonal arms of the MMC are inserted and bypassed with a small delay, as opposed to Case 2 in which they are switched on and off in a synchronous manner. Consequently, despite generating 5-level voltage waveforms across the upper and lower arms, v_{prim} becomes a staircase 9-level waveform shown in Fig. 3.11.

The gate-source voltage, the drain-source voltage and the drain current of the switch T_2 of SM1 in leg 1 of the MMC are shown in Fig. 3.12. As shown in Fig. 3.12, prior to turn-on transition of the switch T_2 , its drain current becomes negative, thereby enforcing its diode to conduct. Consequently, T_2 is turned on under ZVS.

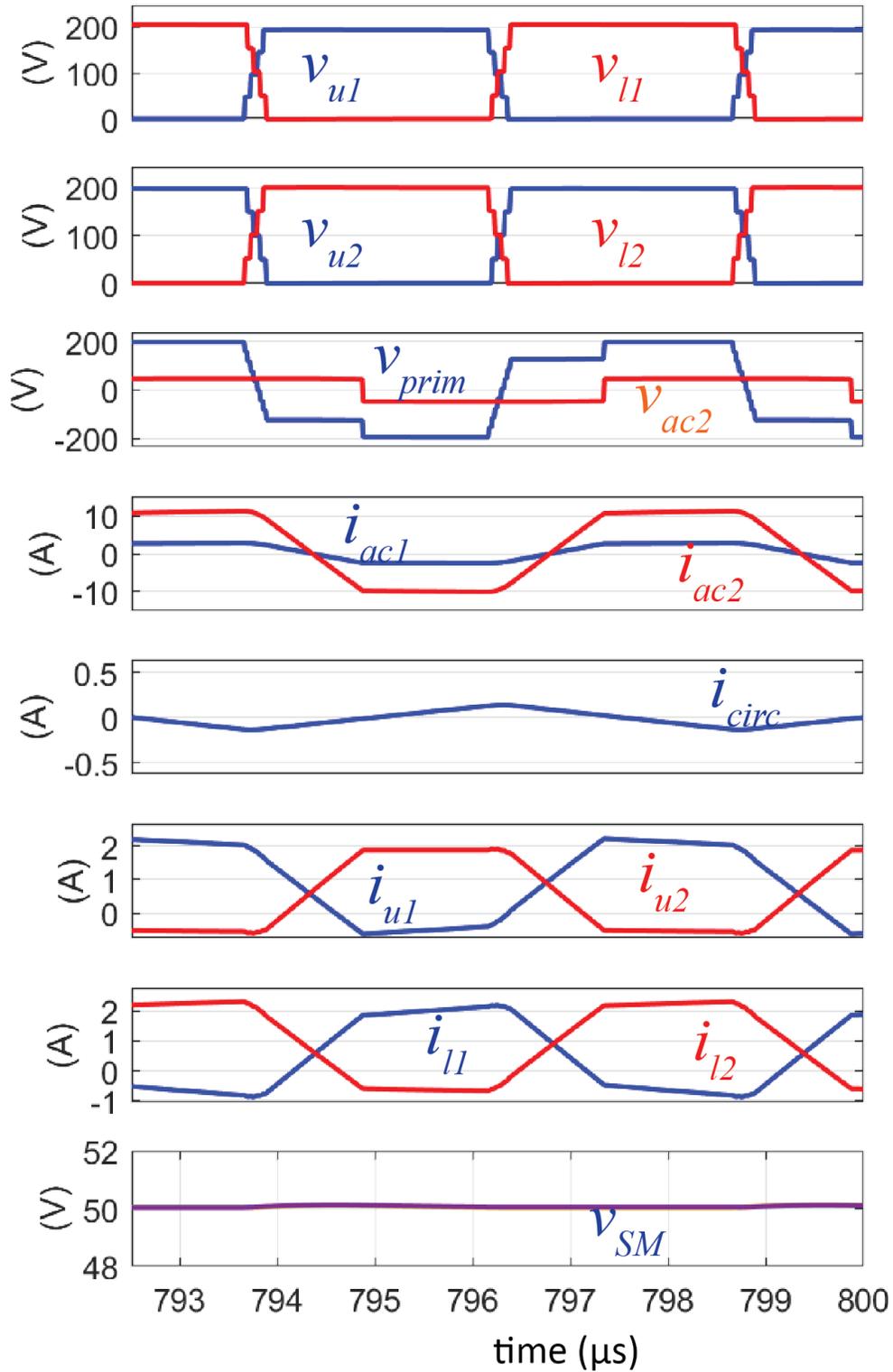


Figure 3.11: Steady-state converter waveforms in Case 4.

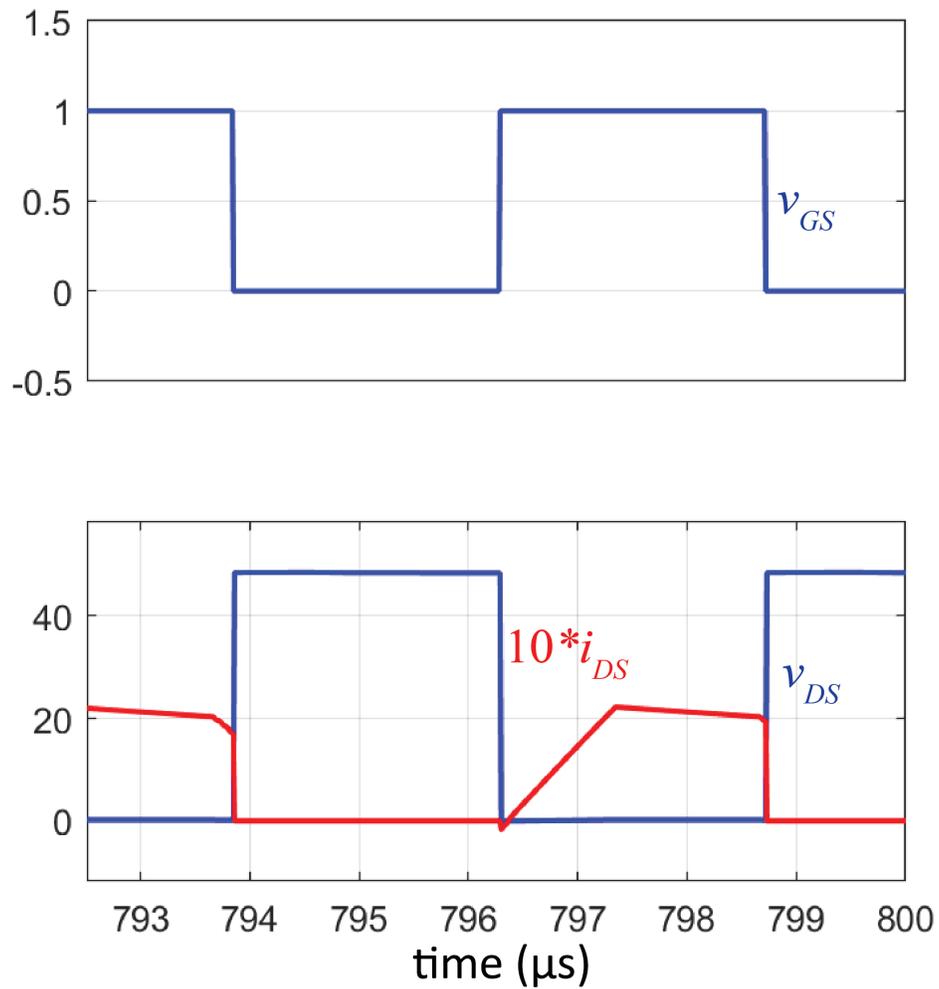


Figure 3.12: Voltage and current waveforms of the switch T_2 of SM1 in leg 1 of the MMC under the operating condition of Fig. 3.11.

CHAPTER 4

EXPERIMENTAL PROTOTYPE AND RESULTS

In this chapter, development of a 1-kW DC-DC converter prototype is presented. Experimental results are then provided to:

- validate the developed mathematical model of the converter, and
- validate the developed modulation and capacitor voltage balancing strategy.

4.1 Prototype Development

In this section, the design of the prototype is provided, which includes components sizing/selection and implementation of the modulation and capacitor voltage balancing strategy on Digital Signal Processor (DSP) and Field Programmable Gate Array (FPGA) boards. The graphical layout of the circuit boards as well as the DSP/FPGA board and their interconnections are shown in Fig. 4.1. As Fig. 4.1 shows, several boards with their own unique functionality are involved as follows:

- **SM Board:** This board houses a half-bridge SM circuit of the MMC. The SMs of the MMC are totally 16 using 16 PCBs, where each consists of a power stage half-bridge circuit realized based on GaN MOSFETs, i.e., GaN Systems GS66506T, the associated identical gate drivers, an isolated DC-DC converter to supply the gate drivers, a capacitor, a capacitor voltage sensing circuit, and a dead-time delay circuit. The capacitor voltage sensing circuit is implemented using an isolated amplifier from Texas Instruments (TI). A low-pass filter is used to remove the high-frequency noise from the output signal of the voltage sensor. An input digital signal from the controller controls the state of each half-bridge SM. This signal is inverted by using a logic gate to generate a pair of complementary gating signals. A dead-time period during which both switches in the half-bridge SM are in blocked state is required to prevent current shoot-through during commutation. The dead time is generated using an RC circuit in each SM PCB. The dead time should be chosen carefully. A shorter than required dead-time may cause both MOSFETs conducting at the same time. A longer than required one, however, leads to discontinued arm current and spike on arm voltages.
- **Full-bridge Board:** This board accommodates a full-bridge power stage circuit on the LV side of the converter. The four power switches are realized based on GaN MOSFETs, i.e., GaN Systems GS66506T, two identical gate drivers, a capacitor, a capacitor voltage sensing circuit based on an isolated amplifier from TI, and a dead-time delay circuit. Two isolated

DC-DC converters are also included to supply the gate drivers. An input digital signal from the controller controls the switching state of the full-bridge circuit. This signal is inverted by using a logic gate to generate a pair of complementary gating signals and to drive the four MOSFETs. A current and a voltage sensor are also mounted on this board to enable output current and voltage measurements.

- **Main Motherboard:** The aforementioned assembled boards and the MF transformer are mounted on the main motherboard where the whole prototype is accommodated. In addition, 4 arm inductors are assembled and accommodated on this board as well.
- **Controller Board:** The modulation and control strategy is implemented on a controller board. The board consists of three TI TMS320F28335 DSP chips and one Intel Cyclone10 FPGA chip. A host computer is interfaced with the controller board to adjust controller parameters. On the controller board, a 12 V/5 V and a 12 V/1.9 V DC-DC converter to supply the DSP chips. There also exist a few linear regulators for FPGA and DSPs.

The assembled configuration of all the aforementioned boards and the overall prototype are shown in Appendix B. The specifications and parameters of the prototype are listed in Table 4.1.

Table 4.1: Specifications and parameters of the experimental prototype.

Nominal Power, P	1 kW
DC-link 1 voltage, V_{dc1}	200 V
DC-link 2 voltage, V_{dc2}	50 V
Number of Submodules, N	4
Submodule Capacitance, C_{SM}	1 μ F
Arm inductance, L_{arm}	15 μ H
Operating Frequency, f_{sw}	200 kHz
MOSFET Model	GaN Systems GS66506T
Transformer Turns Ratio, n	4
Transformer Leakage Inductance, L_{lk}	40 μ H

As a key component in the dual active bridge, the transformer must also be selected carefully. It is also important that it have a turns ratio of 4:1 so that the voltage conversion ratio is equal to one and ZVS is easier to achieve.

Having discussed the details of the physical implementation of the prototype, the following sections will present the results obtained from the experimental tests. The experiments that are conducted correspond to the cases 3 and 4 explored through simulations in Chapter 3.

4.2 Experimental Results for Case 3

Figs. 4.2 to 4.4 show the steady-state converter current and voltage waveforms corresponding to the same operating condition in Case 3 of Table 3.2. The upper and lower arm voltages of the two legs of the MMC, shown in Fig. 4.2, as expected, are the staircase quasi-square 5-level waveforms with a step size of 50 V. The upper and lower arm voltages of each leg are 180° out of phase with respect to each other. Furthermore, the diagonal arm voltages have identical waveforms with a small phase shift, which ensures a 9-level voltage waveform.

Fig. 4.3 (a) shows the primary and secondary voltage and current waveforms of the transformer while Fig. 4.4 shows the arm current waveforms of leg 1 of the MMC. Comparison of the arm voltages and currents along with the primary and secondary voltages of the transformer in Figs. 4.2 and 4.4 with their corresponding simulation waveforms in Fig. 3.9 confirms that all waveforms are in close agreement except the oscillations on the experimental waveform of the primary voltage of the transformer, i.e., red waveform in Fig. 4.3(a). Those oscillations, which occur at the time instants when the secondary full-bridge stage changes its switching state, are due to the undesired resonance between the circuit inductance and device/transformer capacitance. The circuit inductance is comprised of devices internal inductance, wiring inductance, and equivalent series inductance of the SM capacitance. Since these parasitic inductances/capacitances were neglected in the simulation, there is no footprint of such resonances in Fig. 3.9.

The SM capacitor voltages of the upper arm of leg 1 of the MMC, which are all well balanced at their nominal values, i.e., 50 V, are shown in Fig. 4.3(b) along with their zoomed-in ripple components shown in Fig. 4.3(c). The peak-to-peak ripple components are limited to below 0.05%.

For the sake of demonstration of hard-switching condition, Fig. 4.5 shows the gate-source voltage, the drain-source voltage and the drain current of the switch T_2 of SM1 in leg 1 of the MMC. As shown in Fig. 4.5(a), prior to applying the gating pulse to turn T_2 on, its drain-source voltage has not reached zero. As shown in Fig. 4.5(b), at the turn-on time instant of T_2 , the arm current is positive, thereby turning T_2 on under hard switching.

4.3 Experimental Results for Case 4

Figs. 4.6 and 4.8 show the steady-state converter current and voltage waveforms under the same operating condition of Case 4 in simulation studies, i.e., $D = 1$ and $P = 300W$, which corresponds to $\varphi = \pi/2$.

Fig. 4.6 shows the upper and lower arm voltages of the two legs of the MMC, i.e., v_{u1}, v_{l1}, v_{u2} and v_{l2} , which are staircase quasi-square 5-level waveforms with a step size of 50 V. As expected, the upper and lower arm voltages of each leg are 180° out of phase with respect to each other. Furthermore, the diagonal arm voltages have identical waveforms with a small phase shift, which

ensures a 9-level voltage waveform.

The primary and secondary voltage and current waveforms of the transformer, i.e., v_{prim} , i_{ac1} , v_{ac2} and i_{ac2} are illustrated in Fig. 4.7. As expected, v_{ac2} is a two-level waveform while v_{prim} is a staircase 9-level waveform. Nonetheless, due to the presence of the arm inductors, v_{prim} is slightly filtered and not all 9 levels are visible on the waveform. The phase shift φ between the primary and secondary voltages of the transformer is $\pi/2$, thereby transferring the maximum power at that operating point. Comparison of the arm voltages and the primary and secondary voltages of the transformer in Figs. 4.6 and 4.8 with their corresponding simulation waveforms in Fig. 3.11 confirms that all waveforms are in close agreement except the oscillations on the experimental waveform of the primary voltage of the transformer, which were discussed in the previous subsection.

Fig. 4.7(b) shows the SM capacitor voltages of the upper arm of leg 1 of the MMC, which are all well balanced at their nominal values, i.e., 50 V. Fig. 4.7(c) shows the zoomed-in ripple components of the SM capacitor voltage waveforms, which are below 0.05%.

To illustrate the soft-switching operation of the SMs of the MMC, Fig. 4.9 shows the gate-source voltage, the drain-source voltage and the drain current of the switch T_2 of SM1 in leg 1 of the MMC. As shown in Fig. 4.9(a), prior to applying the gating pulse, the drain-source voltage is zero. This is due to the negative current at the time of T_2 turn-on transition, as shown in Fig. 4.9(b), which forces the diode of T_2 to conduct. Consequently, when the gating pulse is toggled to high voltage level, the switch T_2 is turned on under ZVS.

4.4 Efficiency and Thermal Performance Comparison

The efficiency performance of the overall converter under the hard switching condition when $P = 250$ W, is measured at 91% while it increases to 96.5% under the soft switching condition when $P = 300$ W. The high efficiency performance under soft switching can significantly reduce the complexity of thermal management design. As shown in Fig. 4.10, the converter under soft switching can operate at a reasonable temperature at 300 W with heatsinks only. Although under hard switching condition, the converter is operating even with 50 W less power, its devices reach a much higher temperature. Comparison of the thermal performance results in Fig. 4.10 confirms that necessity and of soft switching for operation of the converter.

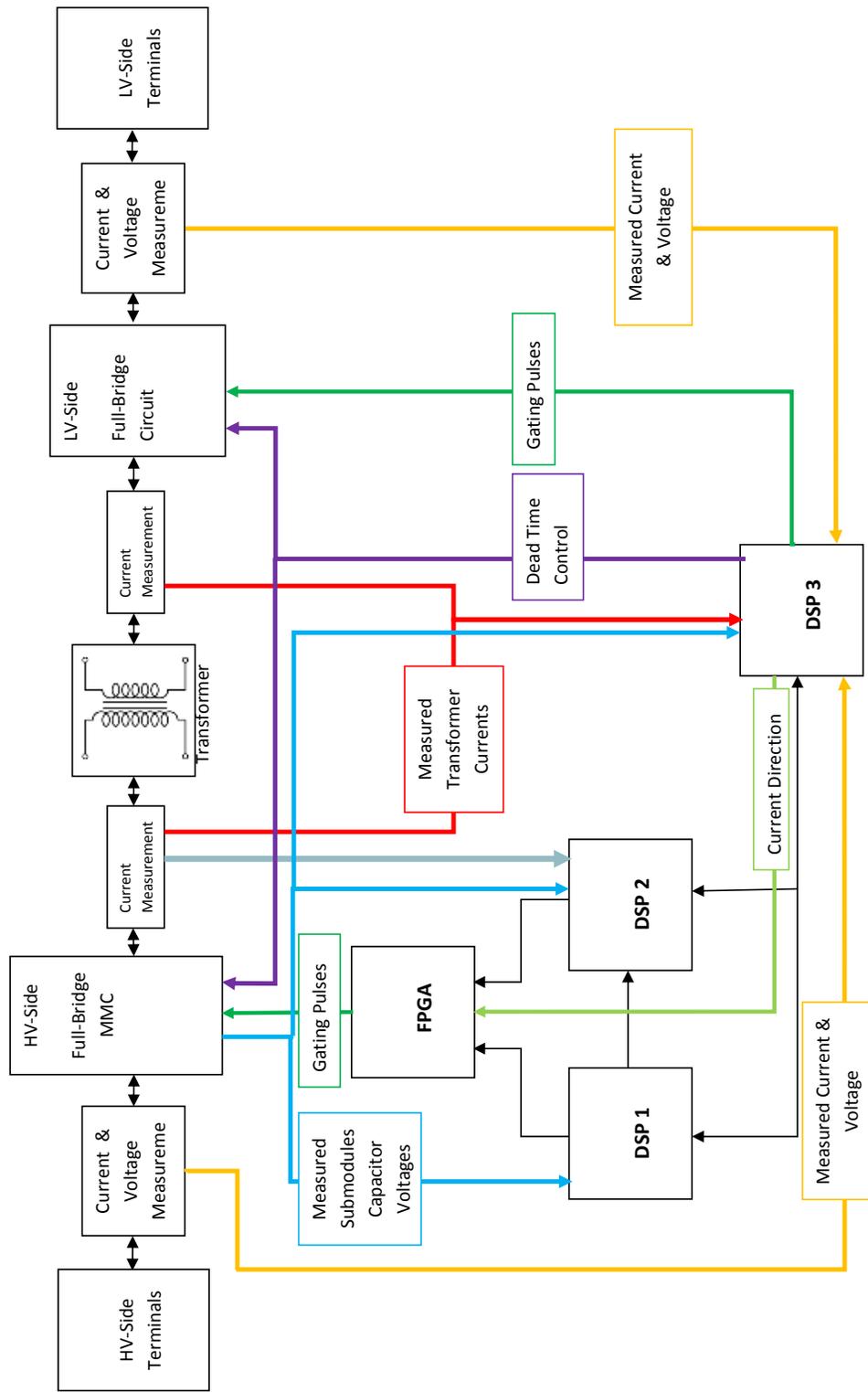
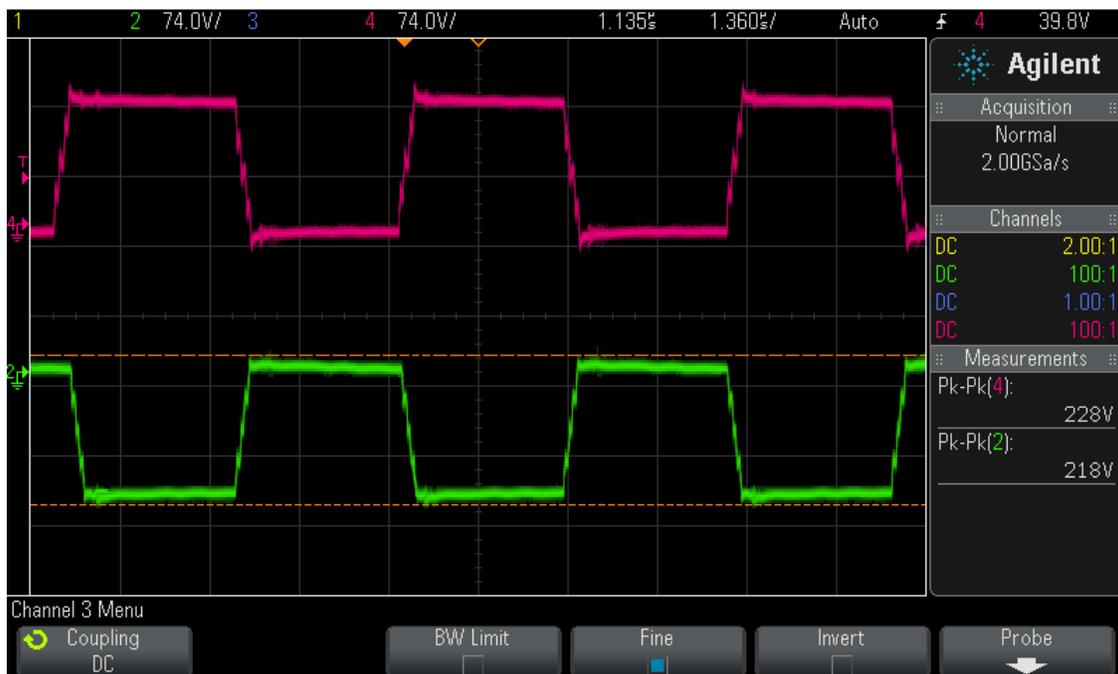


Figure 4.1: The graphical layout of the circuit boards as well as the DSPs/FPGA board and their interconnections.

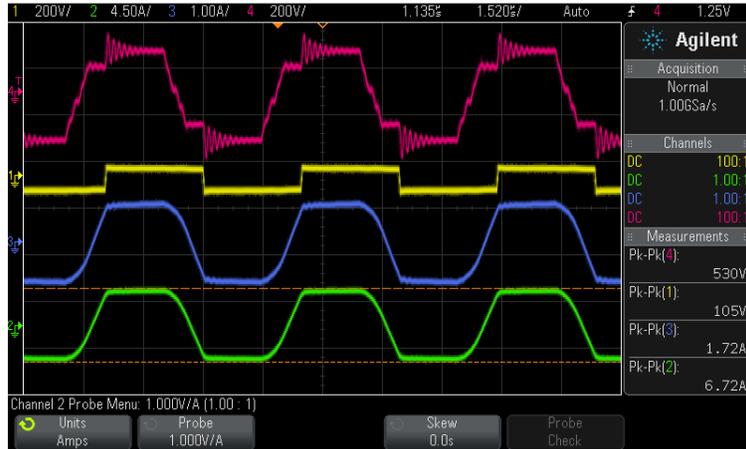


(a)



(b)

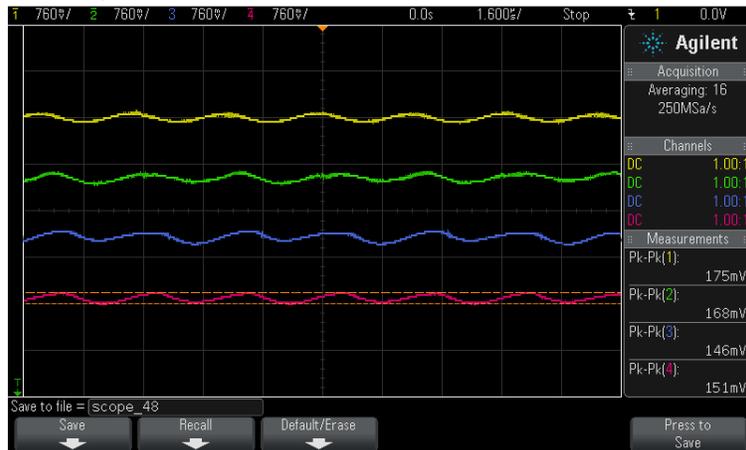
Figure 4.2: Steady-state arm voltages of the two legs of the MMC when $P=250$ W: (a) upper and lower arm voltages of leg 1, and (b) upper and lower arm voltages of leg 2.



(a)

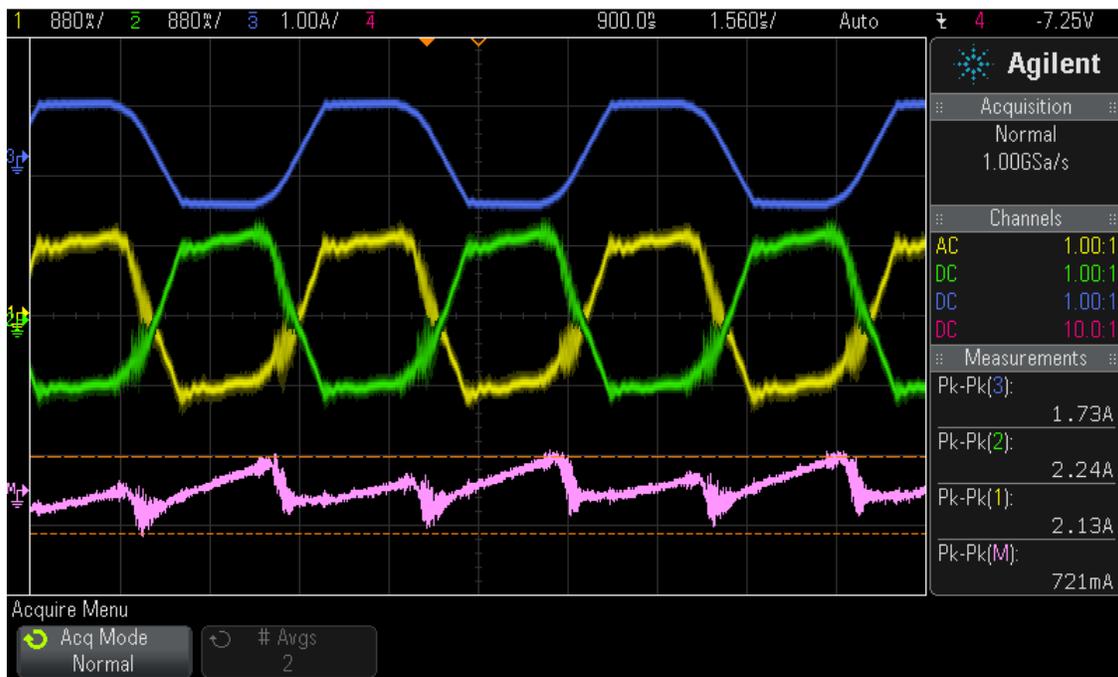


(b)

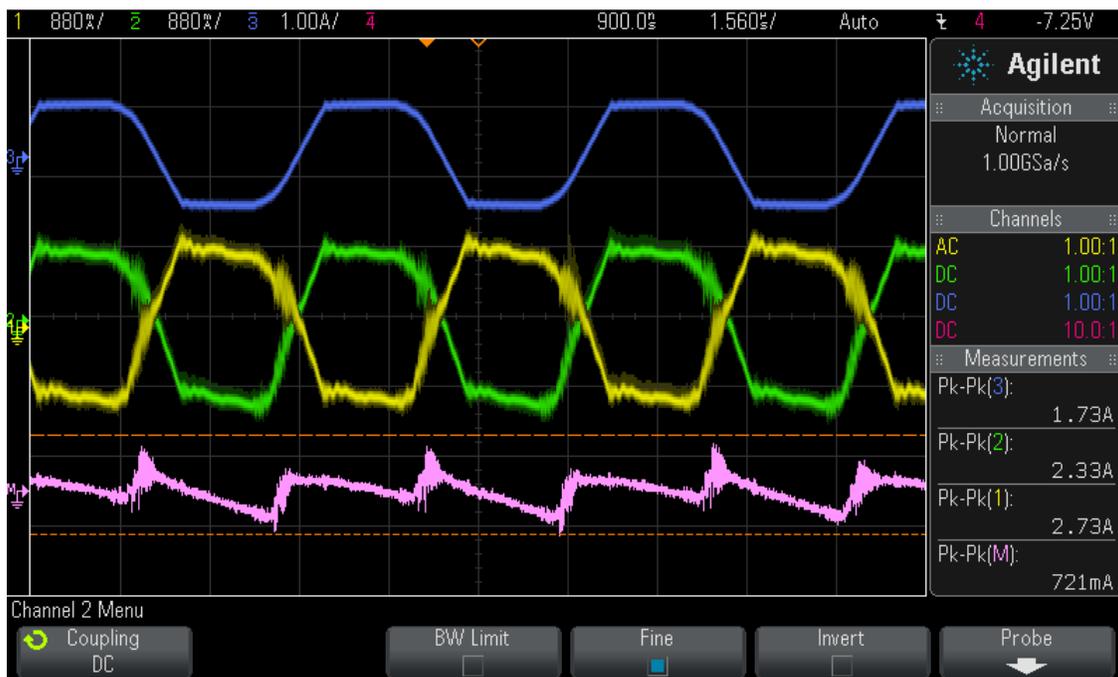


(c)

Figure 4.3: Steady-state voltage and current waveforms of the converter when $P=250$ W: (a) primary (red) and secondary (yellow) voltages and currents (blue and green, respectively) of the transformer, (b) SM capacitor voltages of the upper arm of leg 1 of the MMC, and (c) their ripples.



(a)



(b)

Figure 4.4: Steady-state voltage and current waveforms of the converter when $P=250$ W: (a) primary current (blue), upper and lower arm currents (yellow and green) of leg 1 of the MMC, and circulating current (purple), and (b) primary current (blue), upper and lower arm currents (yellow and green) of leg 2 of the MMC, and circulating current (purple).



(a)



(b)

Figure 4.5: Voltage and current waveforms of the switch T_2 in SM1 of leg1 of the MMC when $P=250$ W: (a) drain-source voltage (red) and gate pulse (yellow), and (b) drain-source voltage (red) and drain current (yellow).

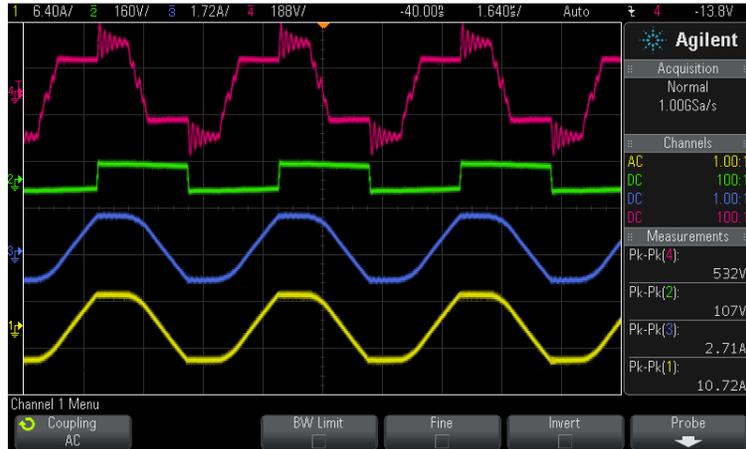


(a)



(b)

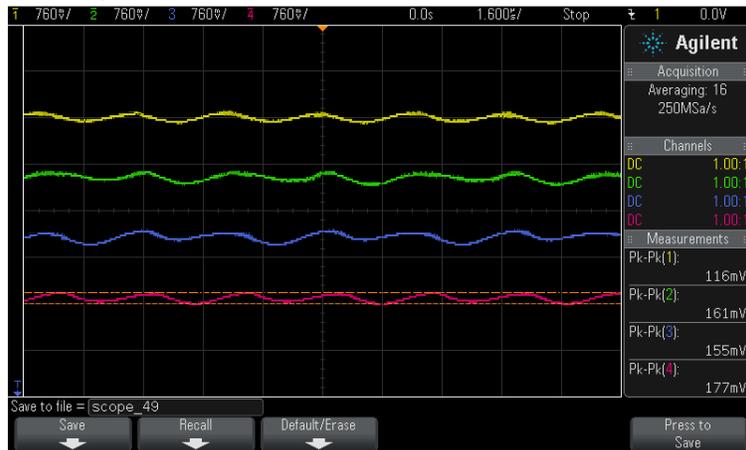
Figure 4.6: Steady-state arm voltages of the two legs of the MMC when $P=300$ W: (a) upper and lower arm voltages of leg 1, and (b) upper and lower arm voltages of leg 2.



(a)



(b)

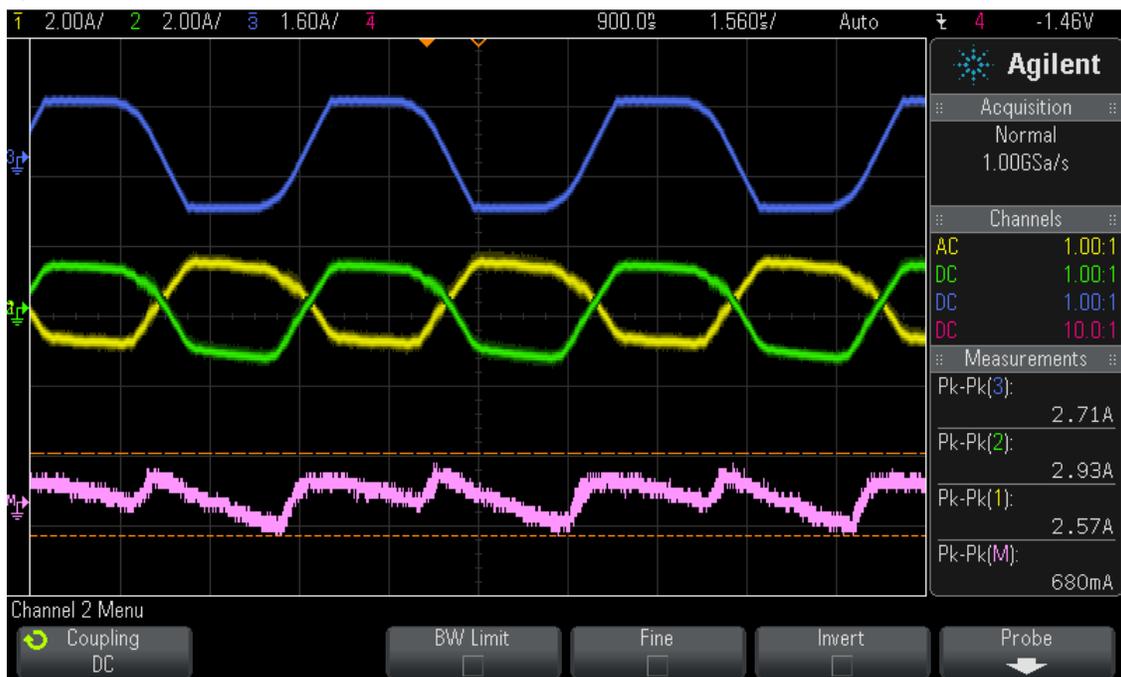


(c)

Figure 4.7: Steady-state voltage and current waveforms of the converter when $P=300$ W: (a) primary (red) and secondary (yellow) voltages and currents (blue and green, respectively) of the transformer, (b) SM capacitor voltages of the upper arm of leg 1 of the MMC, and (c) their ripples.



(a)

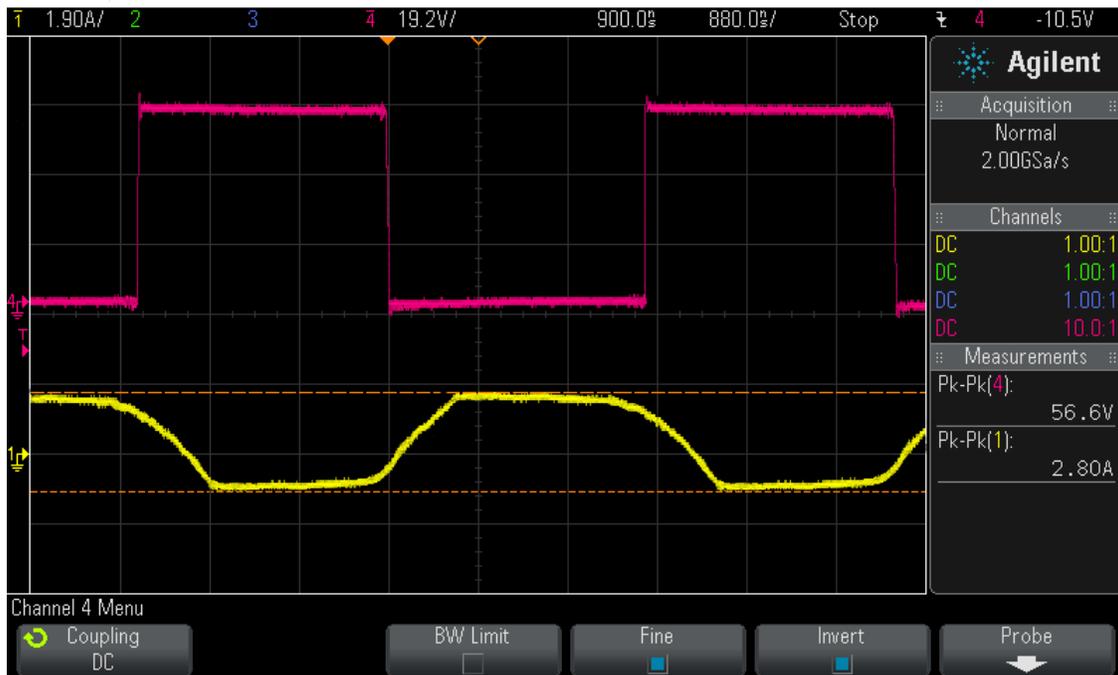


(b)

Figure 4.8: Steady-state voltage and current waveforms of the converter when $P=300$ W: (a) primary current (blue), upper and lower arm currents (yellow and green) of leg 1 of the MMC, and circulating current (purple), and (b) primary current (blue), upper and lower arm currents (yellow and green) of leg 2 of the MMC, and circulating current (purple).

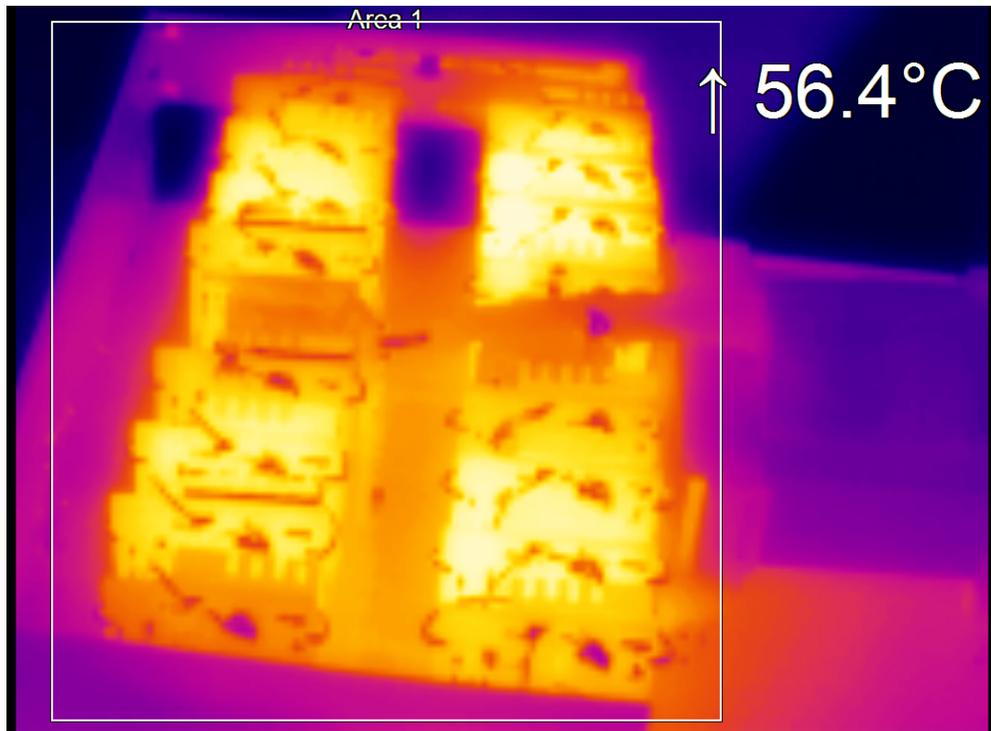


(a)

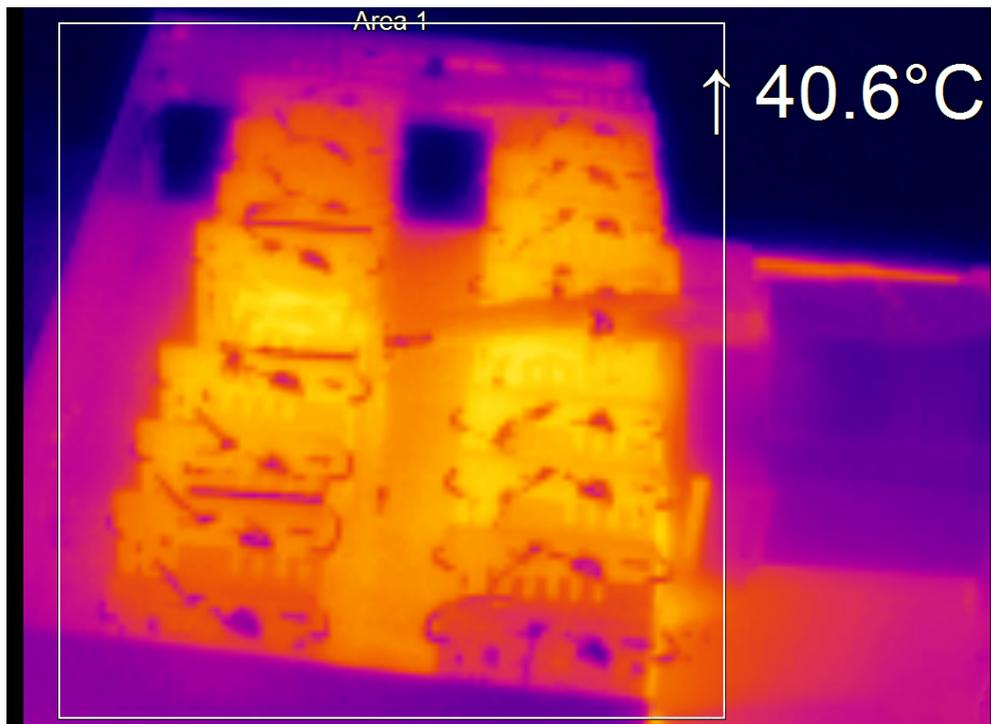


(b)

Figure 4.9: Voltage and current waveforms of the switch T_2 in SM1 of leg1 of the MMC when $P=300$ W: (a) drain-source voltage (red) and gate pulse (yellow), and (b) drain-source voltage (red) and drain current (yellow).



(a)



(b)

Figure 4.10: Thermal performance of the input side MMC with heatsink cooling only: (a) hard switching operation when $P = 250$ W, and (b) soft switching operation when $P = 300$ W.

CHAPTER 5

CONCLUSION AND FUTURE WORK

In this thesis, an isolated bi-directional DC-DC converter, which is realized based on hybrid combination of a conventional DAB power stage and a MMC, is developed. The thesis investigates the analysis, modulation, control, and performance assessment of the converter. For the sake of efficiency improvement, the converter is realized by using GaN semiconductor devices while achieving ZVS operation. The performance of the converter is evaluated based on both simulation studies and experiments on a scaled-down prototype. The proposed converter is a potential topology for high step-up/step-down applications, particularly for interconnection of MVDC and LVDC grids. In continuation of this work, the following aspects can be explored and expanded:

- Development an optimization-oriented design approach for the overall converter including the transformer.
- Increasing the number of SMs such that sinusoidal and triangular waveforms with sufficiently small voltage step sizes can be realized. In this way, other control strategies along with their soft switching regions can be explored.
- Investigation of the impacts of DC faults and exploring potential SM configurations such as full-bridge ones to handle the DC-side faults.
- Investigation of zero-current switching possibility on the MMC side by embedding an *LCL* filter on the MMC side of the converter.
- Expansion of the full-bridge side of the converter to MMC such that both sides can be realized based on MMC bridges. In this case, the converter can be analyzed and investigated for interconnection of DC grids with different voltage levels.

Appendices

A. PRACTICAL CONSIDERATIONS OF CONTROL IMPLEMENTATION

As the main contribution of this work is modulation, soft-switching operation and control of the proposed DC-DC converter, the details relating to the practical implementation are of particular importance. The purpose of this appendix is to highlight the implementation aspects of the modulation and control platform used in this work. In Chapter 4, it was mentioned that the converter is controlled by a custom-designed controller board using 3 TI DSPs and one FPGA. The programming of the controller board is done through the Code Composer Studio (CCS), MATLAB Simulink Embedded Coder software and Intel Quartus Design Prime software, which is a graphical programming language executed on FPGA. The functions performed by the DSPs and FPGA in this setup and their interactions with each other are shown in the block diagrams of Figs. 1 to 4.

As highlighted in Figs. 1 to 4, one part of the overall program used for the modulation and control is run on the three synchronized DSPs and is responsible for reading the data from the converter, translating it into the appropriate form, and passing it to the FPGA after initial calculations for further processing. The other runs on the FPGA and is responsible for PWM and generating the gating pulses for the SMs.

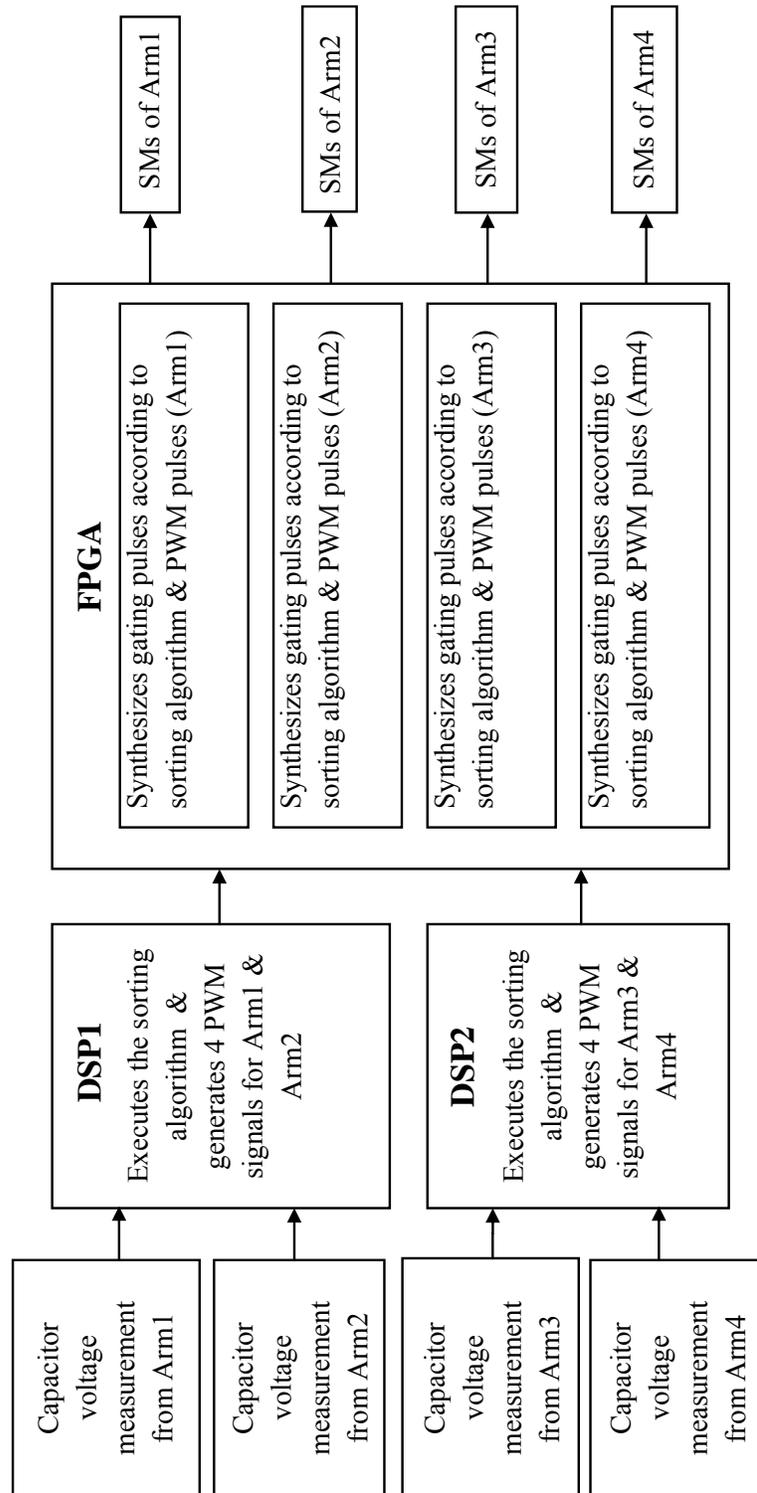


Figure 1: Control block diagram of the MMC side.

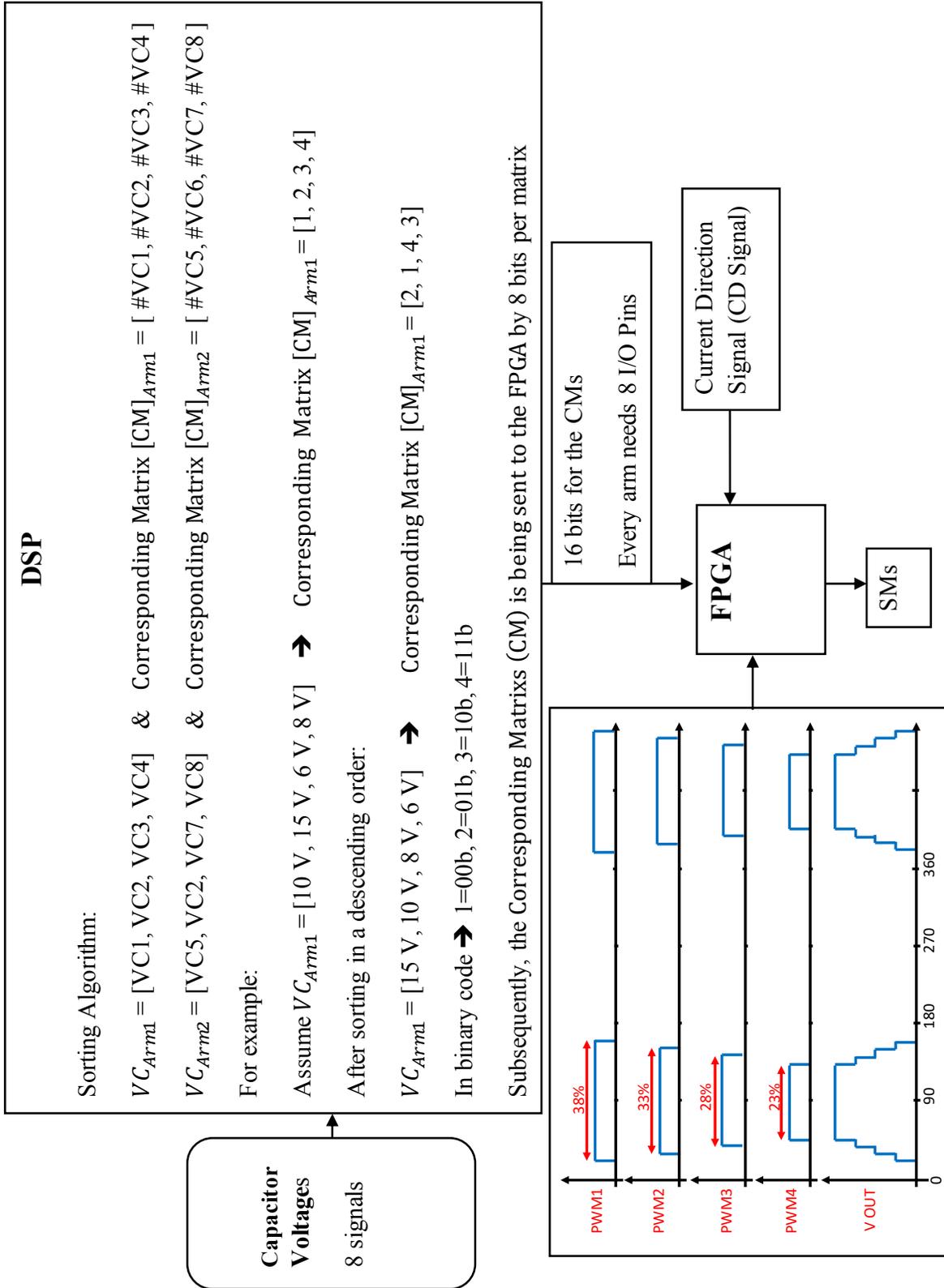


Figure 2: Implementation block diagram of the capacitor sorting algorithm.

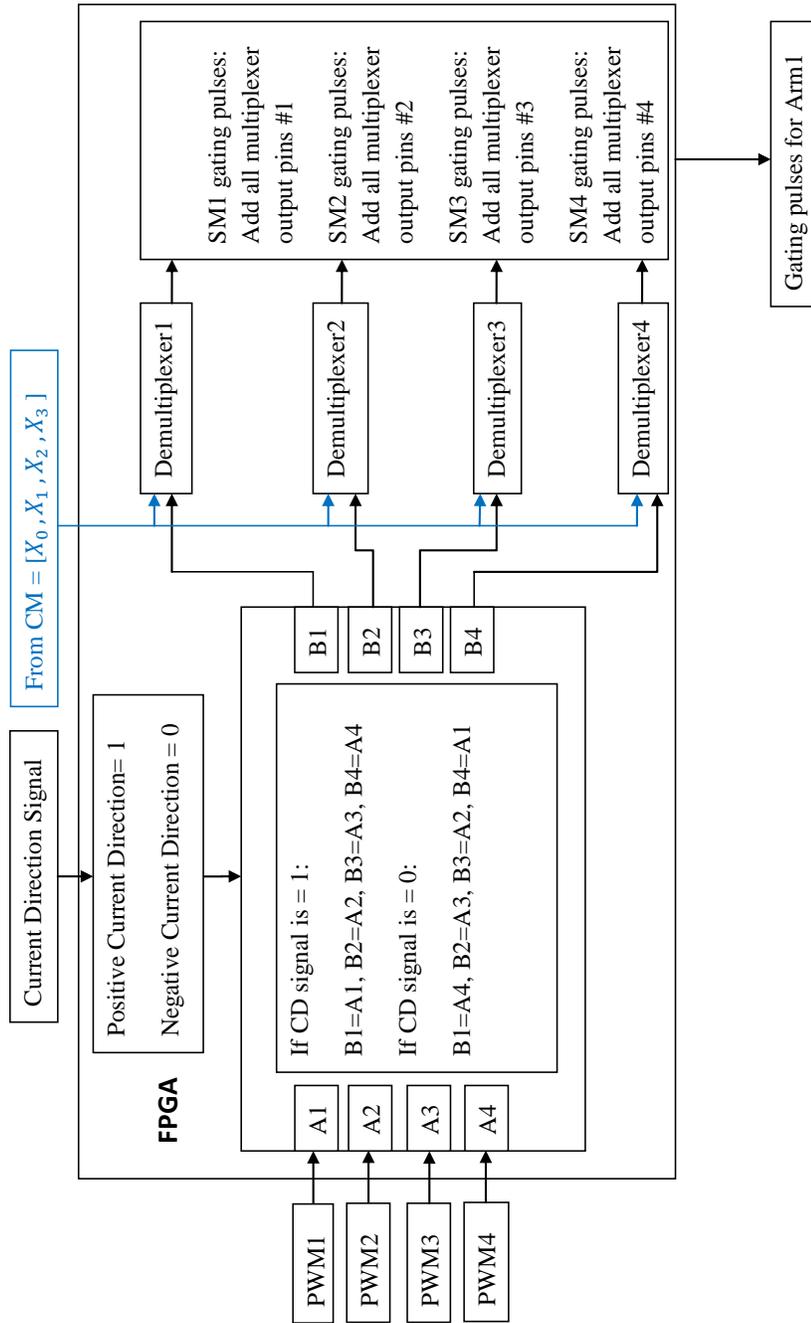


Figure 3: Implementation block diagram of the algorithm for one arm of the MMC inside FPGA.

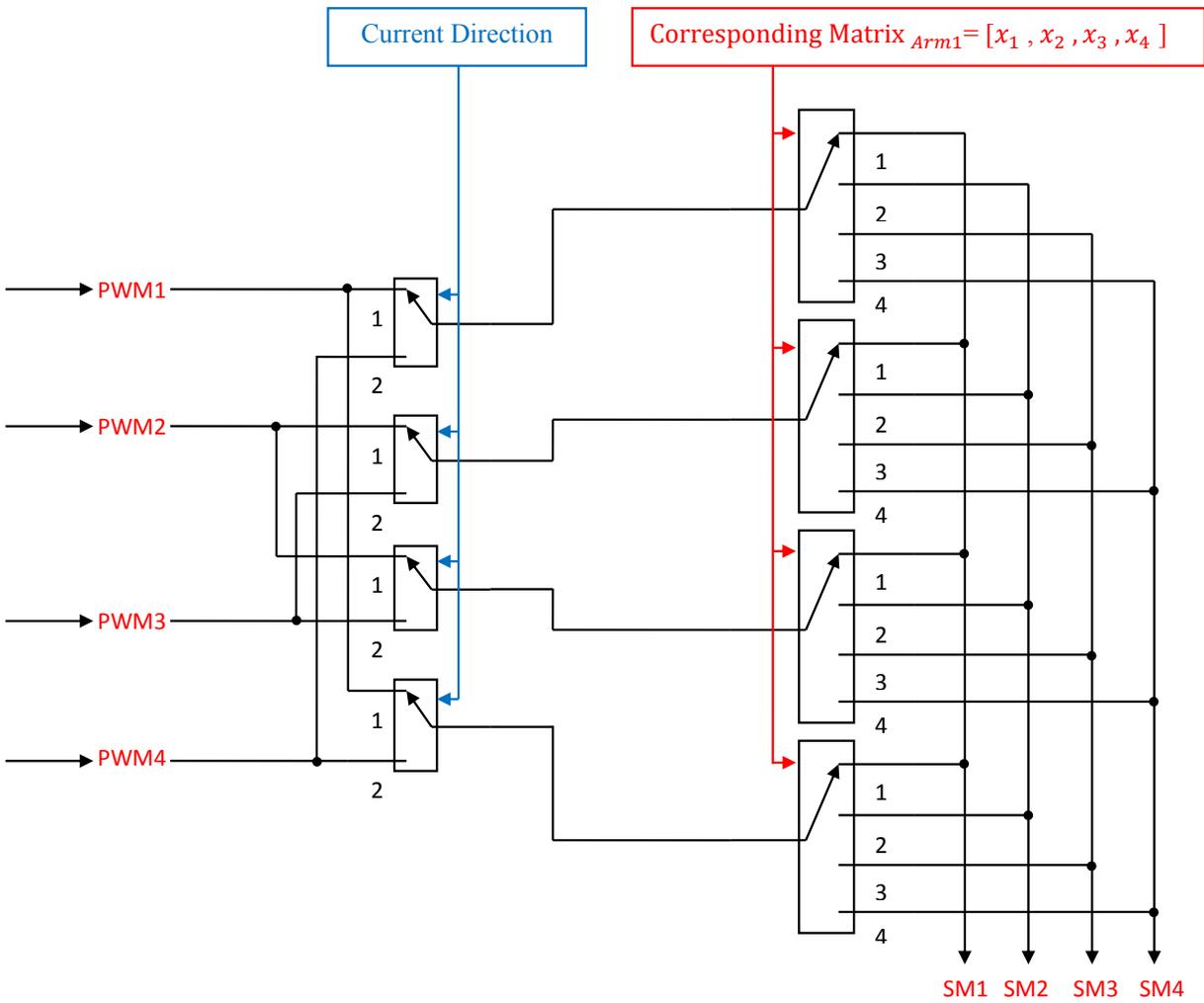


Figure 4: Implementation block diagram of the gating pulse generator for one arm of the MMC inside FPGA.

B. DETAILS OF EXPERIMENTAL SETUP

This appendix presents a set of snapshots of the experimental setup constructed in the lab. The various designed PCBs as well as the final converter assembled are shown in Figs. 5 to 9. A detailed description of the functionality of each PCB is provided in Section 4.1.

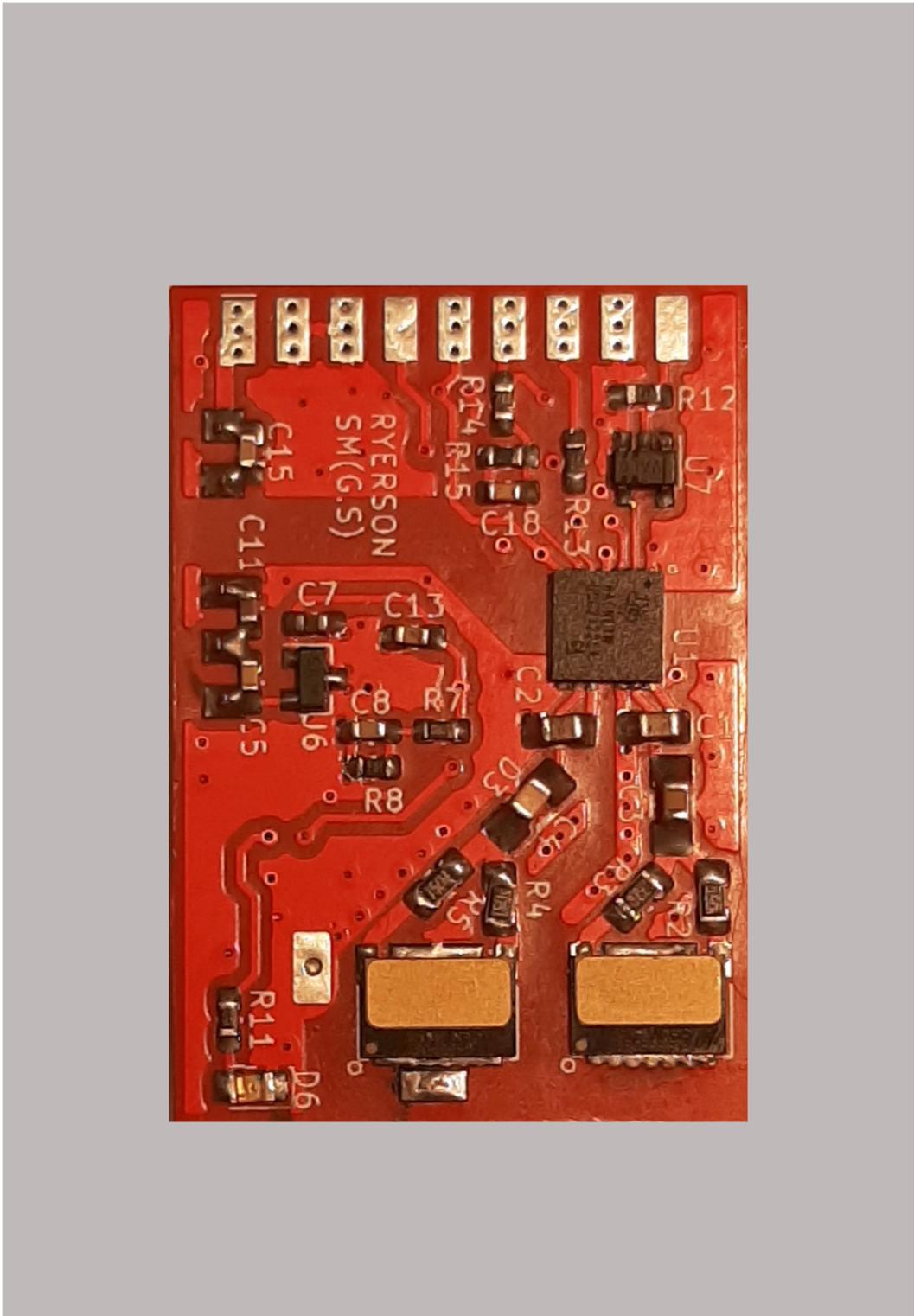


Figure 5: Top side of experimental circuit board of a SM.

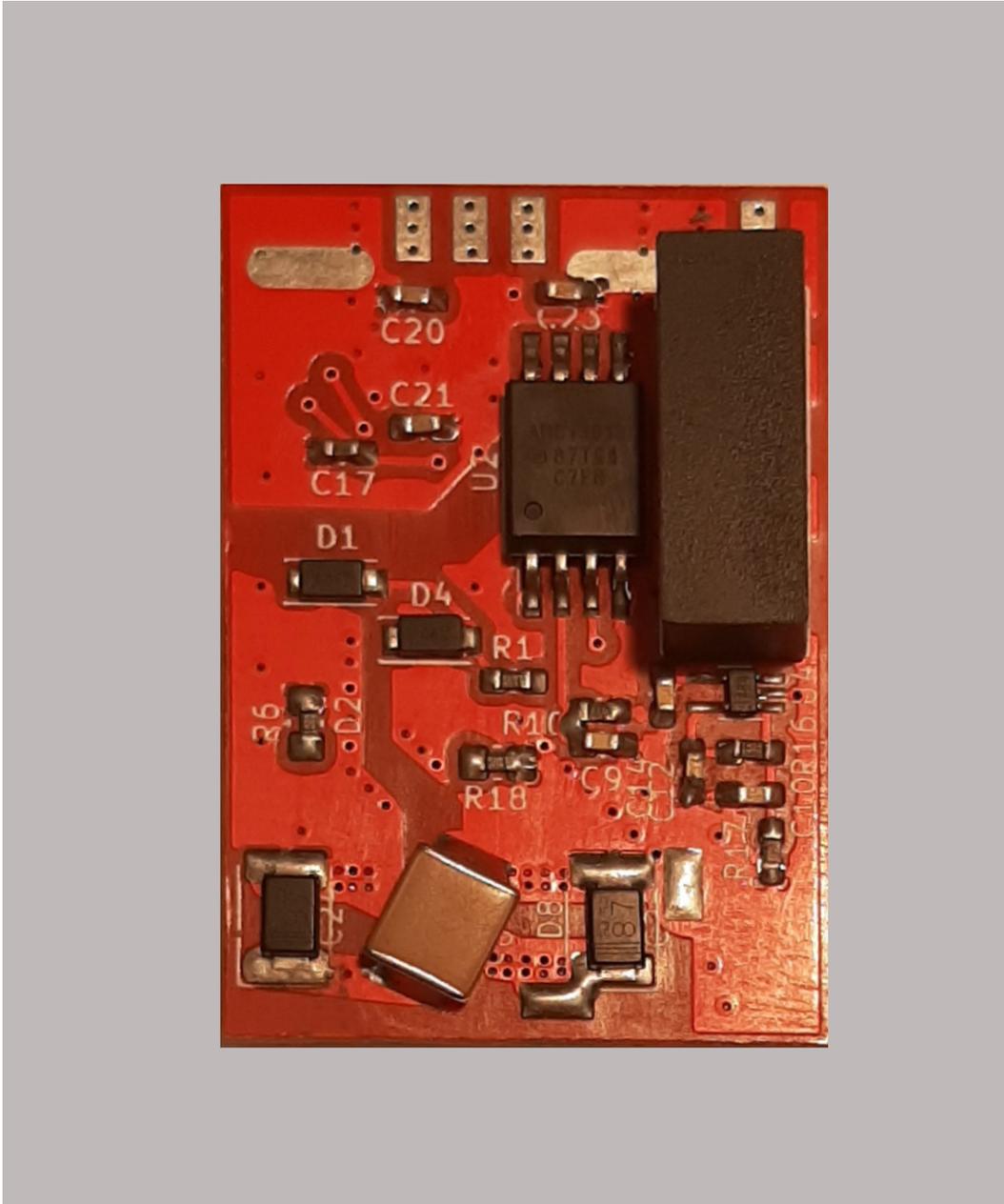


Figure 6: Bottom side of experimental circuit board of a SM.

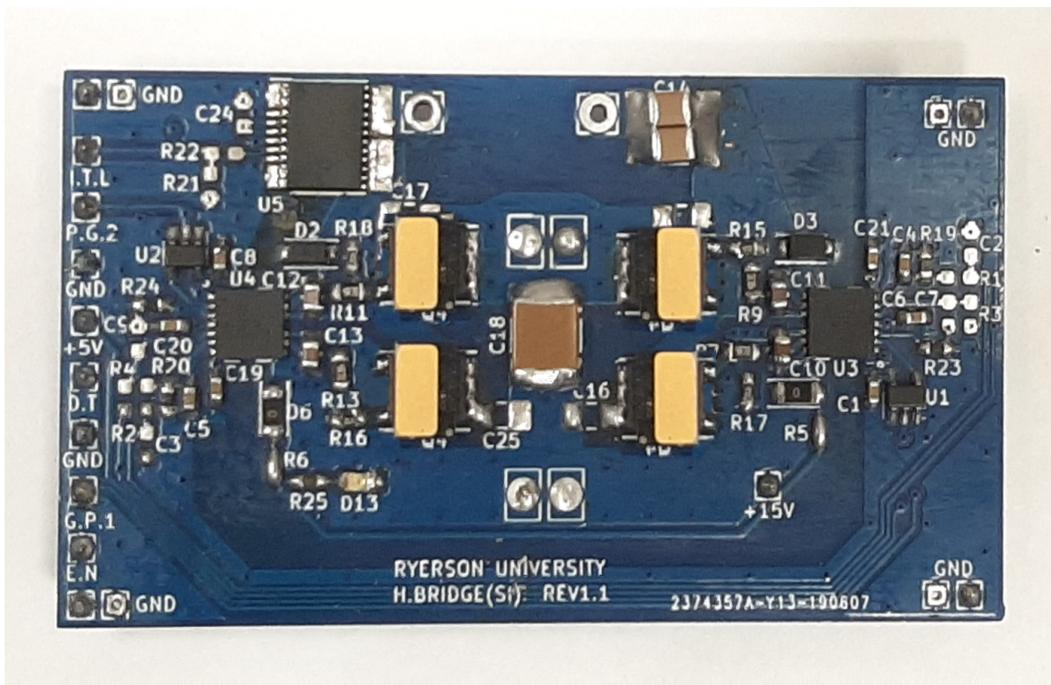


Figure 7: Experimental PCB of the full-bridge board.

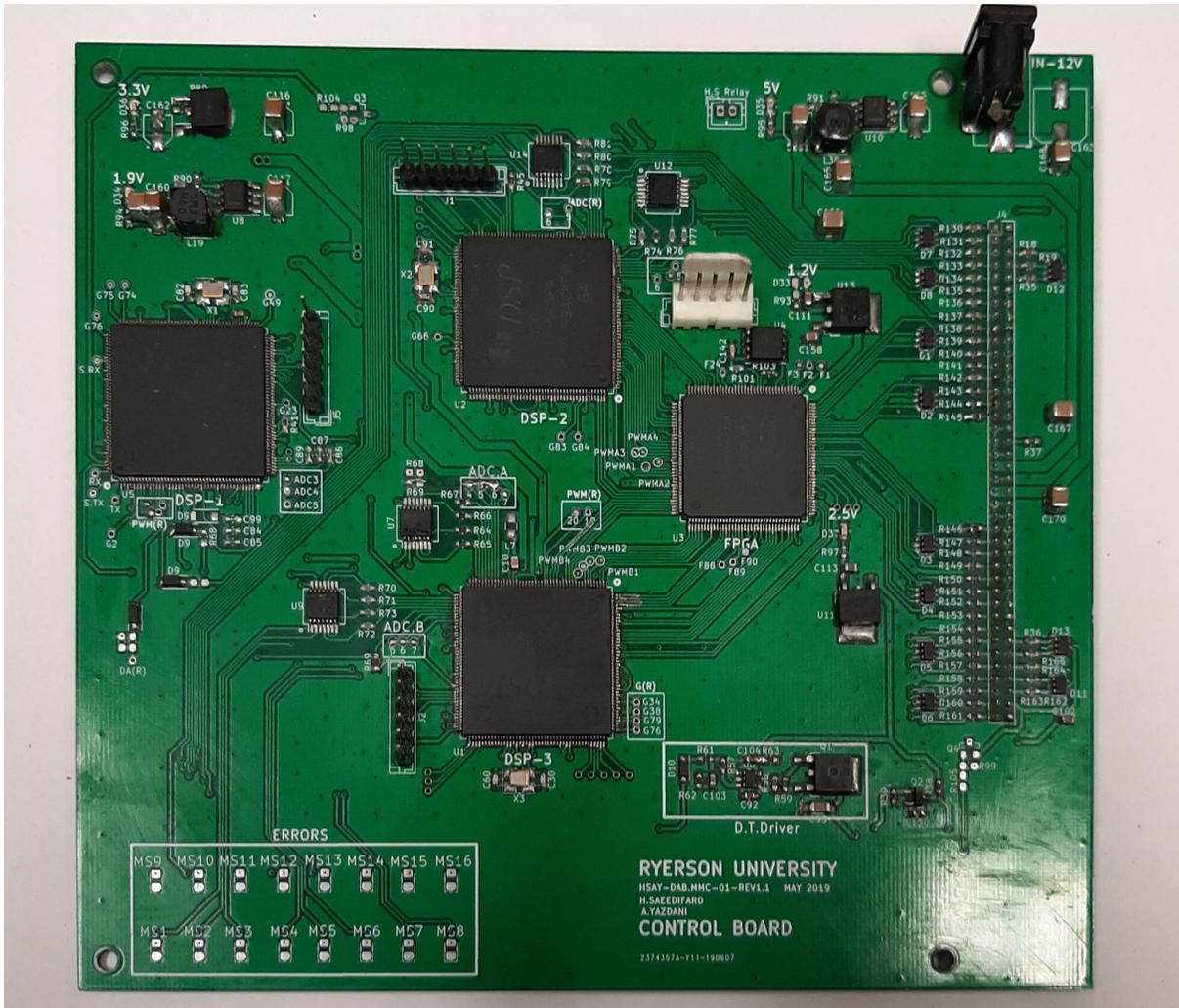


Figure 8: Experimental PCB of the controller board with DSPs and FPGA.

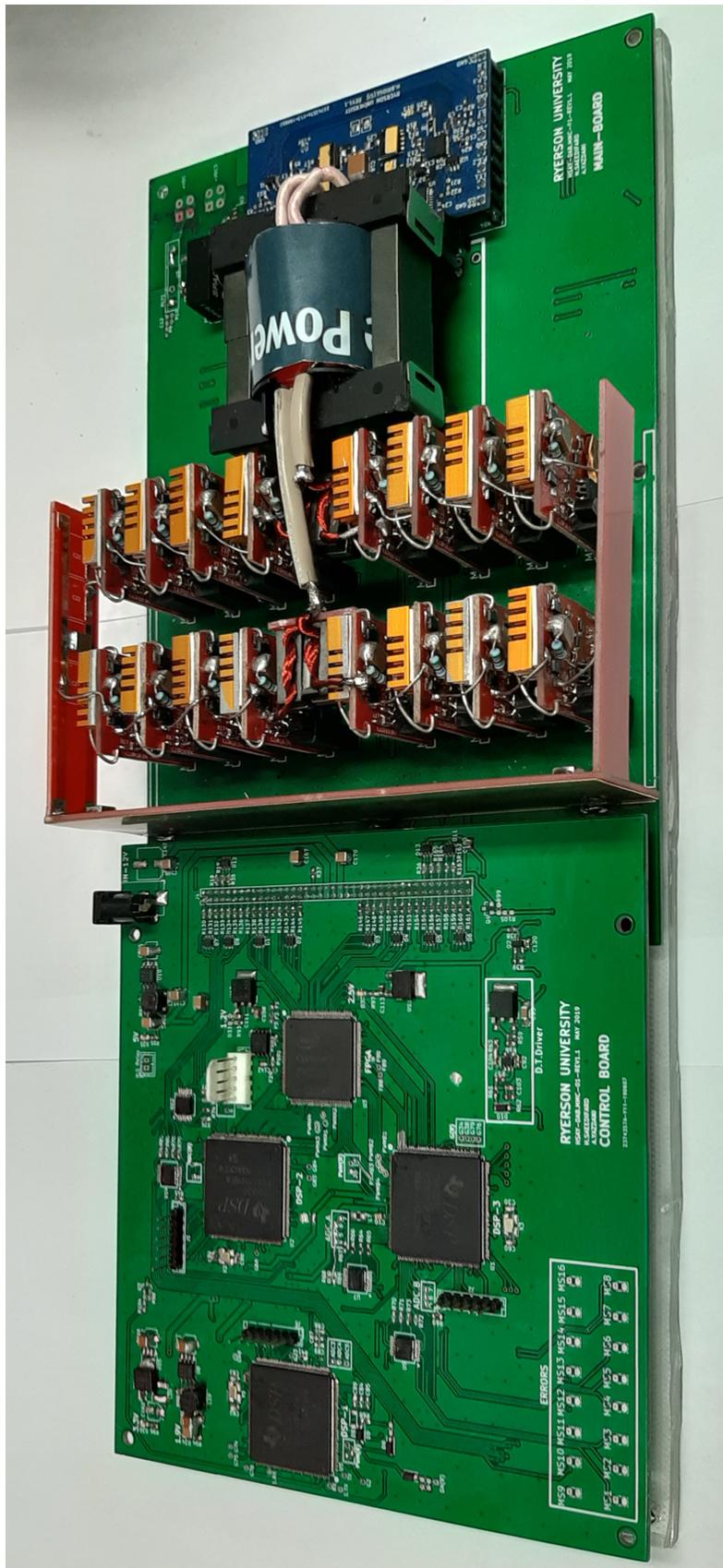


Figure 9: Snapshot of the overall prototype.

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